Reliability of Lead-Free and Advanced Interconnects in Fine Pitch and High I/O Electronics Subjected to Harsh Thermo-Mechanical Environments

by

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Abstract

Industry is moving towards lower cost, increased functionality, and miniaturized electronics placed in ever closer proximity of higher operating temperatures, typical of harsh environments. In this thesis, three aspects of harsh environment thermo-mechanical reliability of fine-pitch electronics has been studied. (1) Effect of underfills on reliability enhancement of high I/O area-array packages on two board finishes including immersion silver, and Hot Air Solder Level under harsh thermo-mechanical environment. (2) Relative comparison of thermo-mechanical reliability of Sn3Ag0.5Cu, Sn3.5Ag, Sn1Ag0.5Cu, SAC-X, SAC-X-plus has been studied on chip-scale packages under harsh thermo-mechanical environment. (3) Comparison of thermo-mechanical reliability of five interconnect systems including Microperal SOL, Sn3Ag0.5Cu, 90Pb10Sn, 63Sn37Pb, and Copper Column. High-lead packages used in the study are the control group. In each case the reliability models have been developed to validate that the measured response of the experimental assemblies is consistent with the expected inherent trends. Failure analysis of the assemblies has been conducted to understand the failure mechanisms.

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CHAPTER 1

INTRODUCTION

1.1 Project overview

The first project presented involves four different electronic packages of varying geometry and architecture. The first package is a fine pitch high I/O flip chip. The second package is a perimeter array multi chip plastic ball grid array (PBGA) having four chips housed in the package molding. The third package is a full array PBGA. Fourthly, there is a perimeter array PBGA with a smaller die and smaller body. All packages have been subjected to a harsh thermal environment and modeled in ANSYS finite element program. Once the packages were thermal cycled, they were cross sectioned and analyzed so that the failure modes and life predictions made by the finite element model could be validated. With this project, it was hoped that a better understanding of how package parameters, such as pad finish, die size, and underfill can effect the performance of a package in a harsh thermal environment. On top of this, it was also hoped that the finite element models would validate the thermal cycling tests so that computer simulation can one day be reliable enough to replace expensive, actual thermal cycling testing.

The second project involves lead free interconnects. In this project, 6 different lead free alloys are tested. The alloys tested included two low silver content packages Sn1.0%Ag0.5%Cu (SAC 105) and Sn0.3%Ag0.7%Cu; two high silver content packages,

Sn3.5%Ag and Sn3.0%Ag0.5%Cu (SAC 305); and two alloys containing rare earth dopants, Sn0.3%Ag0.7%Cu0.1Bi, called SAC X, and Sn0.2%Ag0.7%Cu0.1%Bi0.1%Ni, called SAC X-Plus. All of the packages were identical with the exception of the solder alloy used as the interconnect. All of the packages were subjected to the same harsh thermal environment, but only two could be created in the ANSYS finite element program due to a lack of information regarding Anand's constants necessary for simulation. While more information has been coming in about lead free alloys, much is still unknown. It is hoped that through this study a life model for lead free alloys can be validated and more information can be gained about how the different lead free alloys hold up in harsh thermal environments so that a clear cut, superior lead free alloy can be identified.

The third project involved ceramic packages with different interconnect architectures and designs. Aside from the standard tin lead eutectic ball, four new and unique interconnects were tested. The first interconnect is called the SOL interconnect. It is a compliant plastic core with a copper shell that has been encased in eutectic solder. The second interconnect presented is a copper reinforced high-lead ceramic grid array (CCGA). The interconnect consists of a high-lead core, spiral wrapped with a copper ribbon, and encased in eutectic tin lead solder. For the third interconnect, a high-lead sphere is wetted with a eutectic bridge. It is thought that the more compliant high-lead sphere will lead to better thermal environment performance. The fourth interconnect is a lead free Sn3.0%Ag0.5%Cu (SAC 305) interconnect. Conflicting reports on SAC 305 thermal reliability have been reported to date. The test in this project offers some conclusive evidence as to how the SAC 305 alloy performs in a harsh thermal

environment. In this project, all packages were subjected to harsh thermal environment testing and modeled in the ANSYS finite element program. The thermal environment was simulated and the finite element model was validated with the actual thermal cycling results. Through this project, it was hoped that a superior interconnect architecture could be discovered to replace and surpass the standard tin lead eutectic solder ball used in most applications today. Also, it was further hoped that the finite element life predictions would be good enough to add growing confidence to simulation models, so that expensive actual thermal testing of the interconnects could be substituted for cheaper computer simulations.

1.2 Packaging Overview

In order to understand the ramifications of the tests presented, it is important to have some understanding of electronic packaging. Electronic packaging, according to Suhling, is the art (Based on Science) of establishing interconnections between various levels of electronic devices, components, modules, and systems [Suhling MECH 6310 Notes]. Electronics can be found in nearly every device used today from large vehicles and automobiles to hand held electronic devices. No matter what the application, there is a constant drive to make electronic packages smaller, cheaper, and faster. Because of this, the industry is constantly being driven to test out new designs and improve on older applications. While these new designs may perform optimally from an electronic perspective, they do not always perform that well from a mechanical reliability view point.

Many of these package are subjected to harsh thermal environments, shock/drop loads, or random vibration loads. Today's electronics must withstand harsh environments, and are not just used in benign environments such as the desktop computer in a cubicle. Under thermal cycling load, packages deform due to mismatches in the coefficient of thermal expansion (CTE) found in the different materials of the package. This deformation is taken up by the more compliant solder interconnects. When exposed to repeated thermal cycles, the materials in the package expand and contract at different rates. This cyclic expansion and contraction is a repeated stress on the interconnects and eventually causes their failure by way of low cycle fatigue. Obviously, the longer the fatigue life of the interconnect, the better. Below, in Figure 1-1 an image of an electronic package can be seen demonstrating the different components and their CTE's.

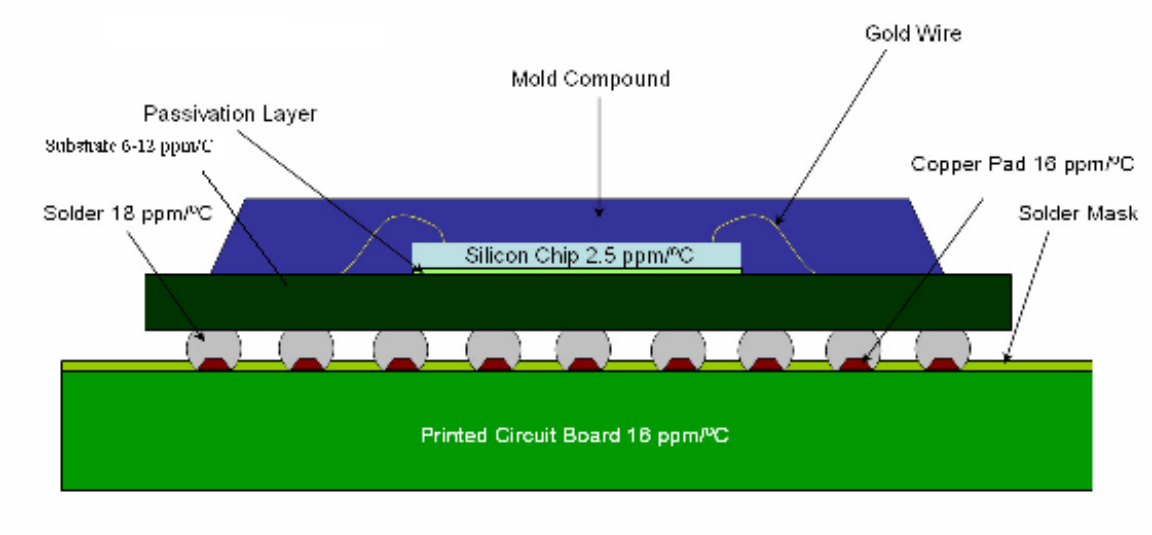

Figure1-1 CTE Electronic package

The main problem area is usually found in the region where the silicon die meets the substrate. In a plastic package, the substrate has a CTE of 12ppm/°C while the silicon chip has a CTE of 2.5ppm/°C. The stiffer silicon die lowers the effective CTE in the

substrate region, which increases the CTE mismatch between the printed circuit board and the substrate. This increased CTE mismatch causes more stress and deformation in the presence of thermal loads and this stress and deformation is in turn taken up by the second level interconnect, leading to a shortened fatigue life of the interconnect. [Syed 1996]. Cracking most often occurs in the neck of the solder ball where the stress concentration is increased. However, failures can be seen at the lower side of the solder ball as well.

1.3 Lead Free Electronics

Recently there has been a movement in the electronics industry to get rid of the lead found in most interconnects. The eutectic tin lead interconnect, 63Sn37Pb, has been used since the inception of the ball grid array due to it's electrical characteristics, wetabiltiy in soldering, and superior reliability performance. However, some health concerns regarding the amount of lead found in electronic packages has caused a movement against lead free interconnects. Solder alloys composed of tin, silver, and copper have emerged as leading candidates to replace the lead based alloys. There is still much to be learned about the alloys, and testing is still ongoing in order to create a Sn-Ag-Cu (SAC) alloy that is as convenient as the tin lead eutectic. Researchers have experimented with varying the composition of the three SAC components and doping the SAC elements with additional earthen metals such as Nickel and Bismuth. Generally, high silver content alloys hold up better in thermal testing than do the lower silver content packages. The material characteristics of the SAC alloys can be changed by doping, either hardening or softening the alloys and effecting the melting point of the

solder alloys. To date, several life prediction equations have been proposed but an accurate life prediction equation has not been determined. With further finite element modeling and thermal testing, a life prediction model can be determined.

1.4 Unique Interconnect Designs

Industry is constantly developing new ways to improve the performance and life of electronic packages. Because the weak point in the package is the solder interconnect new interconnects are often designed and old interconnects are modified. Different interconnects can include solder columns, high-lead spheres with eutectic bridges, and polymer studded interconnects to name a few. In the third project presented, 4 new interconnect designs were created. These new designs include a copper reinforced column grid array; a SOL interconnect, which is a plastic sphere surrounded by a copper ring and encased in eutectic tin lead solder; a lead free Sn3.0%Ag0.5%Cu (SAC 305) interconnect; and a high-lead sphere bridged with eutectic tin lead solder. All of these interconnects were thermal cycled on test boards that had a strip of ceramic with no chip or mold and were connected to FR-4 PCB. The high-lead core interconnects are thought to be more compliant than the stiffer eutectic tin lead solder balls. This increased compliancy should allow the interconnects to deform easier and take on more stress. This should increase the life of the package. The column grid interconnects outperform the standard tin lead eutectic alloys because they have a taller standoff height which reduces the stress found in the interconnect and adds to the compliancy of the interconnect. It was hoped that one of the new designs would greatly improve the life of the package over the standard eutectic solder ball.

All packages were created and simulated in the ANSYS finite element environment. Upon failure of the packages in thermal cycling, they were removed and cross sectioned in order to validate the failure mode shown by the finite element simulation. Good correlation between actual testing failure mode and simulation failure mode was achieved. The package lives were also estimated by way of ANSYS and the simulation lives were matched up with the real thermal testing lives. Again, all of the simulation lives were within 25% error of actual thermal cycle lives.

In sum, the main focus of all the tests is on second level interconnect failure. All of the interconnects are subjected to low cycle fatigue which causes their failure and the failure of the electronic package. The thesis presents data on underfilled packages, packages with different surface finish, packages with different design, new lead free interconnects, newly designed unique interconnects, and finite element simulations. If it can be shown that the finite element simulation closely follows the real world thermal cycling then it may be possible to skip actual thermal cycling, which would save money and time. The thesis presents more information on new lead free alloys, new interconnect designs, and how unique architecture packages hold up against one another.

CHAPTER 2

LITERATURE REVIEW

Electronic packaging started with the dual in line package (DIP). This package consisted of a thin ceramic body housing a chip wired out to a lead frame. This package allowed for more I/O's at the time, but required through hole technology in order to be bonded to the PCB. In the 1970's, the industry created the plastic leaded chip carrier. This package could be surface mounted to the PCB but offered poor reliability due to J-lead connections. From this, the quad flat pack was created which offered a more reliable package due to gull wing leads, which were compliant and didn't fail as easy. As packages evolved, the need for more interconnects became apparent. This need lead to the creation of the pin grid array. In this package, pins were dispensed on the bottom of the package in an area array fashion. These leads, however, gave raise to reliability issues involving the bending of leads and were expensive due to the alloy used in creating the pins. In an attempt to reduce cost and abate pin bending while still allowing for high I/O density and reliability, the ball grid array package was created. In this package, smaller pitch packages with superior reliability and better manufacturing yields were made available. The BGA technology offers high I/O packages that are cheaper, smaller, faster, and more reliable than most other leaded packages.

The major problem with the BGA is the thermal mismatch between components in the package. The BGA featuring an alumina substrate called a ceramic ball grid array

has a ceramic substrate featuring a CTE of $6\,^{o}C/ppm$ while the PCB has a CTE of $13\,^{o}C/ppm$. This difference in CTE causes the materials in the package to expand and contract at different rates when exposed to thermal loads. This expansion and contraction leads to a cyclic stress or fatigue which is taken up in the second level solder alloy interconnect. The main focus of BGA reliability is trying to reduce the stress on the second level interconnects.

2.1 General Packaging Architecture

Many studies have been done involving the reliability of the second level I/O's based on package dimensions. Initially it was thought that the plastic ball grid arrays would not be strong enough to withstand harsh environments such as under the hood of a car. [Syed 1996] showed that packages designed with perimeter arrays, thicker BT substrates, and an increased pad size can provide packages reliable enough to withstand the under the hood environment. Further studies on reliability have showed that the die size has the greatest impact on reliability [Ghaffarian 2002]. In this study, Ghaffarian showed that the smaller die increases the life of the package. It was also shown that the larger pitched ball grid arrays tend to outperform the fine pitch ball grid arrays. Syed discussed the impact of the die on the package reliability in his 1996 paper [Syed 1996]. In this study, he states that the close proximity of the die increases the effective CTE in the region of the die making it lower. This causes a greater CTE mismatch between the PCB and the package which causes more deformation and stress in the face of a thermal load. The compliant solder ball connections end up taking on the stress and this repeated stress, termed low cycle fatigue, eventually leads to their failure.

Other studies have shown the effect that pad finish and solder mask can have on the interconnections. [Bradley 1995] showed that HASL finish is superior to the immersion nickel based finishes. Oxidation of the nickel through gold layer can lead to poor solderability resulting in a bad connection between the solder ball and copper pad. [Suhling 2002] showed the superiority of HASL pad finish over Palladium based pad finishes in thermal testing on BGA's. It has also been shown that perimeter arrays perform better than the full arrays because the impact of the die is lessened and that a thicker BT substrate also helps abate the CTE mismatch between the die and the PCB [Syed 1996, Ghaffarian 2002]. [Mawer 1999] showed the increased reliability packages have with non solder mask defined copper pads.

The effect of underfill on PBGA's has been the focus of many previous studies. [Elkaday 2004] tests the impact of underfill on the thermal performance of smaller perimeter array packages and shows that the underfill improves the life of the tested packages. [Pyland 2000] shows that a low CTE higher young's modulus underfill improves the reliability of a super BGA, but higher CTE underfills deteriorate the life of the packages. [Qi 2005] tests two different underfills on a smaller full array package. One of the underfills increases reliability while the other underfill did not. An increase in life for PBGA's was seen in [Liji 2002]. [Burnette 2001] presents the effects of six different underfills on different package architectures and determines that having an underfill with a CTE of approximately 15 ppm/°C is optimal for improving life. [Suhling 2002] tests 15,17, and 23 mm packages under the effects of four different underfills and determines that the proper underfill can increase the reliability of a package so that it can be used in an under the hood environment.

In lead free electronics, much work is still being done to understand the deformation and characteristics of lead free interconnects. In particular, an overall superior SAC alloy for replacement of lead based alloys is still being researched.

2.2 Lead Free Electronics

[Zhang 2003] tried to define the overall solder deformation using four major modes over deformation including time independent elastic strain γ_{el}, time independent plastic strain γ_{p}, time dependent primary strain γ_{pr}, and time dependent secondary strain γ_{sec}. He also defines 4 distinct regions of strain including the Nabarro-Herring creep and superplasticity given by

$$\frac{d\gamma_{scr}}{dt} = A\tau^{n} \exp\left(\frac{-Q}{RT}\right) \qquad 2.1$$

as well as the climb controlled dislocation and power law breakdown given by

$$\frac{d\gamma_{scr}}{dt} = A'[\sinh(\alpha\tau)]^{n} \exp\left(\frac{-Q}{RT}\right) \qquad 2.2$$

He also hypothesizes that the lead free or SAC alloys will perform better in low stress regions where Ag_3Sn and Cu_6Sn_5 intermetallics block grain boundary sliding. However, in high stress regions, the deformation is dominated by dislocation climb and glide, as well as matrix diffusion which is better suited for the lead rich particulates commonly found in lead based alloys leading to better lead based reliability in high stress regions. These results have been validated by many reseachers including [Clech 2005] who showed that the SAC alloys underperform the lead based alloys on ceramic packages where the stress is higher. [Schubert 2003] showed that the SAC outperforms the lead based alloy in a more compliant package, such as a PBGA with low CTE mismatch.

Zhang and Syed have separately shown that the point where 63Sn37Pb begins to outperform SAC is temperature dependent. One of the main points regarding lead free testing is that the lead free results are strongly dependent on package type and temperature profile as shown by [Roubaud 2001]. A test performed by Syed involving many different alloy compositions including doping the SAC alloys with earth additives was performed wherein the tin silver alloys underperform the tin silver copper alloys, but again, the results are strongly dependent upon temperature and package type [Syed 2001].

A study involving lead free electronics and polymer stud grid array (PSGA) packages showed that the SAC alloy performance is strongly dependent upon package type with the solder alloys characteristic life doubling when the package architecture changed [Vandevelde 2004]. In a power cycling environment, Young et al. showed that the SAC alloy can outlast the traditional tin lead alloy at low temperatures, but that the tin lead outperforms the lead free alloy at high temperatures in a power cycling test [Young 2008]. In another test, the lead free alloy Sn3.8Ag.7Cu was tested on plastic ball grid array (PBGA), plastic quad flat pack (PQFP), and thin small outlying package (TSSOP) wherein the different failure modes of the solder were demonstrated as well as the solder's performance on different pad finishes [Che 2005].

It has also been shown by many researchers including [Engelmaier 2003] and [Darveaux 2005] that the lead free alloys creep slower than the lead based alloys. In fact, Engelmaier states that the lead free alloys creep up to 100 times slower than the lead based alloys. On top of this, it has been shown by [Schubert 2002] and [Lau 2003] that the SAC alloys have a higher young's modulus when compared to the lead based eutectic alloy. So while the lead free alloys creep slower than the lead based alloys, they are

stiffer and may not hold up as well in a drop shock environment. The creep rate of the lead free alloys is also dependent on silver content as demonstrated by [Zhang 2008], [Darveaux 2008], and [Rooney 2008] wherein they stated that SAC 105 exhibits poorer creep properties than SAC 305. The trade off is that the higher silver content alloys have a higher young's modulus meaning that they are stiff and of little use in shock drop environments [Rooney 2008].

In an effort to create lead free alloys that are both creep resistant and compliant enough so that they may be used in thermal and drop shock applications; rare earth metals have been doped with tin silver copper based alloys to change the mechanical properties of the lead free alloy. [Amagai 2006] reported that the addition of no more than .03 wt % Ni to Sn.3Ag alloy reduces the grain size and IMC thickness. [Rooney 2008] stated that the addition of nickel to high silver content alloys produces a compliant and creep resistant alloy. [Huang 2008] reported similar findings by stating that nickel reduces IMC size and thickness. Huang states that doping SAC 405 with nickel softens so that it is as compliant as SAC 105, but still maintains the creep properties of SAC 305. [Kariya 2004] showed similar findings when he doped SAC 105 with nickel. Kariya states that the alloy becomes stiffer with nickel addition wherein the nickel creates a finer microstructure which gives good mechanical strength and good ductility. Because of this more of the deformation is elastic as opposed to plastic.

Other experiments involving the doping of SAC alloys with Bismuth have been performed by [Kanchanomai 2002] wherein he has shown that the bismuth causes an initial hardening in the alloy so that the stress in the alloy is higher but the plastic strain is lessened. The addition of Bismuth leads to a significant decrease in fatigue life for the

alloy. The bismuth addition has less cracking, but their increased stiffness increases the stress in the alloy. [Kanchanomai 2002] also shows that the addition of bismuth lowers the melting temperature of the alloy but raises the homologous temperature which enhances the occurrence of thermally activated processes such as creep and grain growth. [Zhao 2003] reported similar findings when doping SAC alloys with bismuth when he says that the tensile strength of the alloy increases, but the elongation of the alloy decreases. [Zhao 2003] also says that the optimal amount of bismuth is below 3%. Zhao also shows that the tin rich phase decreases with bismuth addition. Other experiments with Cerium have been performed by [Song 2008] wherein it is reported that Cerium greatly deteriorated the SAC alloy's life span. [Rooney 2008] reported findings where the Cerium increased the strength of the solder joint.

In addition to the creep models presented above in equations 1 and 2 the Anand model as proposed by [Anand 1982] for high temperature metals has also been shown to accurately represent the creep properties of lead free SAC alloys. The equation was modified by brown in his 1989 work [Brown 1989]. The Anand model is a unified creep theory model containing one flow equation and three evolution equations. The flow equation is

$$\frac{d\varepsilon_p}{dt} = A\left[\sinh\left(\frac{\xi\sigma}{s_o}\right)\right]^{\frac{1}{m}} \exp\left(\frac{-Q}{kT}\right), \qquad 2.3$$

the three evolution equations appear as

$$\frac{ds_o}{dt} = \left\{h_o\left(|B|\right)^a \frac{B}{|B|}\right\}\frac{d\varepsilon_p}{dt}, \qquad 2.4$$

$$B = 1 - \frac{s_o}{s^*}, \tag{2.5}$$

$$\text{and } s^* = \hat{s}\left[\frac{\frac{d\varepsilon_p}{dt}}{A}\exp\left(\frac{Q}{kT}\right)\right]^n \tag{2.6}$$

The Anand equations unify both time dependent strain and time independent plastic strain through a common internal stress variable "s". [Rodgers 2005] has proven that the Anand model is valid for SAC finite element simulation by performing stress strain tests on different alloys and simulating the same stress strain test in ANSYS, where the results matched up closely. Anand constants for some of the lead free SAC alloys have been discovered. [Amagai 2002] reported eight of the nine Anand constants necessary for FEM simulation. [Chang 2006] presented Anand constants for SAC 305 that appear to give accurate simulation results. [Chen 2005] presented Anand constants for Sn3.5Ag lead free solder alloy. Though the Anand constants for some of the alloys have been presented, a valid life prediction model for lead free solders is yet to emerge.

Lead based alloys have well established life prediction models. [Darveaux 2000] established 63Sn37Pb eutectic alloy damage relationships correlating crack growth rate with inelastic strain energy density per cycle. These constants were later updated by Lall in his 04 paper [Lall 2004]. Other researchers have presented life models based on coffin manson based equations such as Zhan in his 03 paper [Zhan 2003]. For lead free alloy, [Syed 2004] has proposed a life prediction equation based on creep models making use of the hyperbolic power law breakdown constitutive equation

$$\frac{d\gamma_{scr}}{dt} = A'\left[\sinh(\alpha\tau)\right]^n \exp\left(\frac{-Q}{RT}\right) \tag{2.7}$$

wherein he derives:

$$N_f = (0.0014\omega_{acc})^{-1} \quad 2.8$$

In his 2004 paper Syed also proposed life equations based on many other constitutive equations. As well as lead free solder interconnects, much work is being done to develop interconnects of new geometry and design.

2.3 Unique Interconnect Information

In an attempt to abate the damage found in the second level interconnect new interconnect designs are often proposed. Some examples of uniquely designed interconnects include elastomer interconnects with particle embedding which were tested for thermal reliability in the work proposed by [Liu 2003]. [Chandraskekhar 2003] showed promising results thermal cycling polymer stud grid arrays from -55 to 125 Celsius. [Vandevelde 2004] tested polymer stud grid array packages with SAC and SnPb based solder joints. Multi-copper column interconnects are designed by [Liao 2005] in his work. [Aggarwal 2007] looks at using metal-polymer composites to replace metallic components for packaging interconnects. [Okinaga 2001] shows a 4X reliability of plastic core solder balls over normal tin lead eutectic solder balls. Okinaga proves that the resistivity is not too high and the interconnect is a viable solution for normal solder balls. [Galloway 2005] shows that the polymer core package has a 1.6X life improvement over standard solder balls. Galloway also shows a 10% higher standoff with the interconnect adding to increased reliability. [Movva 2004] demonstrates how the polymer core acts as a strain buffer reducing stress in the rest of the interconnect. Movva also gives the material properties of the polymer core interconnect. [Whalley

2008] established optimal dimensions and material properties in the polymer core interconnect so that the maximum reliability can be achieved. As well as improving the solder ball, efforts have also been made to enhance the column grid array packages.

[Ghaffarian 2006] tests new lead free CCGA designs against plastic ball grid arrays. [Hong 2000] tested solder columns coated in a lead free solder for enhanced connectivity. [Winslow 2005] offers a copper reinforced column in his paper. He shows that the copper ribbon is intended to hold the interconnect together at the normal cracking location. He gives a concise summary of developments in column grid arrays and recent failures and designs. [Perkins 2003] tests a high-lead eutectic tin lead dual alloy column grid array. The failure mode is identified at the location where the high-lead alloy and tin lead eutectic alloy interface. New designs, as seen in [Winslow 2005], hope to abate the failure at the dual alloy interface. The column grid array has an established foundation as being a reliable interconnect as shown in the reliability tests run by [Master 1995] and [Engelmaier 1995].

Another interconnect commonly used on ceramic packages is the high-lead core solder ball. The interconnect has a high-lead sphere that is wetted with a eutectic bridge for connectivity to the component. Within the interconnect, the high-lead sphere is more compliant and takes up the majority of the interconnect strain during thermal loading. Past tests have examined failure mode and strain patterns in high-lead interconnect. [Howieson 2001] tests CBGA dual alloy interconnects and identifies failure modes as well as offering a method for modeling failure of the interconnects. [Farroq 2003] compares SAC CBGA's to dual alloy High-lead etutectic interconnects and shows that the SAC outperforms the dual alloy interconnects. He offers reasoning on why the dual

alloy concept should work. [Hong 1996] gives detailed models on stress in the dual alloy interconnect suggesting that the eutectic alloy has 2X the plastic strain of the 90Pb10Sn alloy. [Interrante 2003] also compares SAC alloys to the dual alloy interconnects and shows the superior reliability of the lead free, SAC, alloys. [Interrante 2003] determines that SAC has twice the fatigue life of the dual alloy CBGA.

CHAPTER 3

UNIQUE ARCHITECTURE BGA PACKAGES

In this chapter, the thermo-mechanical reliability of four different packages of varying architecture and dimensions are presented. The study includes the effects of underfill on different PBGA's and a high I/O flip chip package as well as the effects of pad finish on the lives of the different packages. All of the packages were thermal cycled in a harsh thermal environment and recreated in ANSYS finite element environment for simulation purposes. In depth failure analysis and reliability data is presented in the pages to follow.

3.1 Modeling techniques and life prediction method

All models presented in this paper were modeled using ANSYS V.10.0 finite element program. According to the distance to neutral point formula (DNP)

$$\gamma_{xy} \approx \frac{L(\alpha_{PWB} - \alpha_{CC})\Delta T}{2h} \qquad 3.1$$

where L is the distance from the neutral point, which is taken as the point in the center of the package; a diagonal slice symmetry model was used for finite element modeling because the worst case, or critical solder ball can be captured in a diagonal slice model of the package. An example of a diagonal slice model is shown below in figure 3-1:

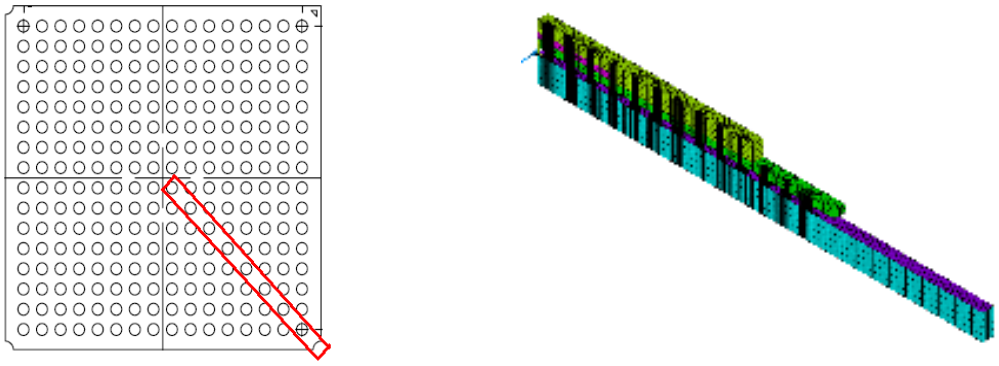

Figure 3-1 Diagonal symmetry model

It should be noted that the corner solder ball will not always be the limiting solder ball. In the presence of a die, the effective CTE is low. This creates a greater CTE mismatch between the package and the printed circuit board. This greater mismatch causes a greater stress which is taken up by the solder ball in the "die shadow" region [Syed 1996]. A finite element model demonstrating the die shadow is shown below:

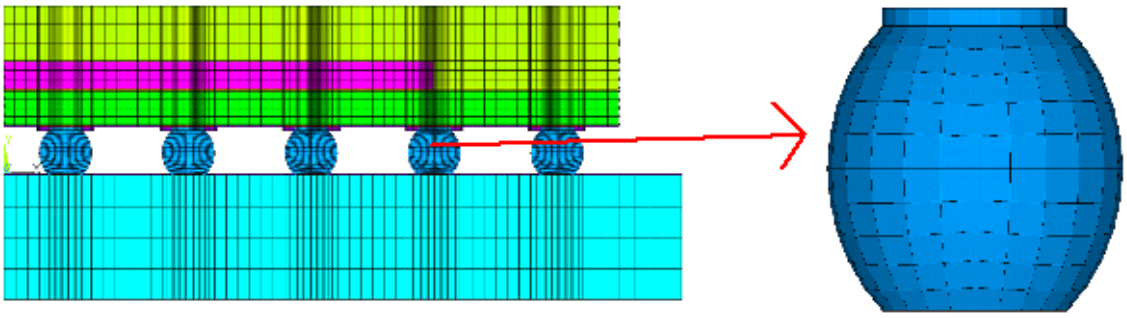

Figure 3-2 Solder ball located in the die shadow region

The elements used for modeling were the VISCO107 and eight node SOLID45 brick elements.

Eight node SOLID45 elements were used to model all of the materials in the package except for the solder ball, which was modeled using VISCO107 elements. All of

the materials in the package were modeled as isotropic except for the PCB and the substrate which were modeled as orthotropic. As taken from the ANSYS element library, SOLID45 is used for 3-D modeling of solid structures. It is an eight noded element with u_x, u_y, and u_z at each node. The element has the capability to model plasticity and creep as well as other deformation features. Body temperature can be put in as a nodal load. The VISCO107 element also has eight nodes with u_x, u_y, and u_z at each node. The VISCO107 element is used to model rate dependent plasticity. Body temperature can be applied as a body force at each node. For this element, the Anand model is used.

As mentioned in the previous chapter, the Anand equation consists of one flow equation,

$$\frac{d\varepsilon_p}{dt} = A\left[\sinh\left(\frac{\xi\sigma}{s_o}\right)\right]^{\frac{1}{m}} \exp\left(\frac{-Q}{kT}\right) \tag{3.2}$$

with three evolution equations,

$$\frac{ds_o}{dt} = \left\{h_o\left(|B|\right)^a \frac{B}{|B|}\right\}\frac{d\varepsilon_p}{dt} \tag{3.3}$$

$$B = 1 - \frac{s_o}{s^*} \tag{3.4}$$

$$\text{and } s^* = \hat{s}\left[\frac{\frac{d\varepsilon_p}{dt}}{A}\exp\left(\frac{Q}{kT}\right)\right]^n \tag{3.5}$$

The Anand model is a unified equation that unifies rate dependent and rate independent plasticity by an internal state variable "s", the deformation resistance, to describe the averaged isotropic resistance to macroscopic plastic flow [Wilde 2000]. The nine constants required for the Anand equation are seen in table 3-1:

Table 3-1 Nine Anand Contants

Anand variable	
s_o (MPa)	Initial Value of deformation resistance
A(1/sec)	Pre-exponential factor
Q/k(1/K)	Activation energy over boltzmann's constant
a	Strain rate sentivity of hardening
h_o (MPa)	Hardening Constant
ξ	Multiplier of stress
n	Stain Rate Sensitivity of Saturation
$\hat{s}$ (MPa)	Coefficient of Deformation Resistance
m	Strain rate sensitivity of stress

In order to obtain the nine constants a series of constant strain rate tests and constant load creep tests must be performed at different temperatures and equations fitted to the generated stress and strain curves. Two things that the Anand equation does not take into effect are the Bauschinger effect and thermal recovery. The Baushinger effect has an impact on the amount of inelastic strain incurred while the material undergoes a cyclic fatigue load. The Baushinger effect must be accounted for when calculating life via a Coffin-Manson power law type of equation [Wilde 2000]. In fact, some researchers have reported error in the fact that Anand doesn't take into account aging, specifically with respect to lead free tin silver copper alloys where aging has a pronounced impact [Vasudevan 2008].

3.2 Modeling and real world failure

As mentioned earlier, when the electronic device is used in real world applications, the repeated thermal stresses put on the package cause cyclic fatigue. This cyclic fatigue leads to the eventual failure of the device by way of crack growth through the second level interconnect. The dominating deformation mechanism in the second level interconnect is creep deformation. This creep deformation leads to the generation of plastic work, which is defined by the equation

$$\sigma\dot{\varepsilon} \qquad 3.6$$

Which is also called the stress power. Essentially, it leads to an increase in energy in the body. The inelastic strain energy is defined as the unrecoverable potential energy of the deforming body. Essentially, this energy is lost when the body deforms plastically. This is why so much effort is put into defining the creep properties of the solder alloys, as will be seen throughout the thesis. When the viscoplastic solder creeps, it has three regions. The first region is the primary, or initial region. Next is the secondary region, and thirdly, the final, or tertiary region. The secondary region is also termed the steady state creep. Steady state creep is the dominant creep mechanism seen in the solder alloy. The tertiary region is the final region before the solder ruptures and fails. In ANSYS, the plastic work is a ready output of the program and is used as a damage parameter. The inelastic strain energy density is represented by the hysteresis plot of the finite element simulation. An example of a hysteresis loop is shown below.

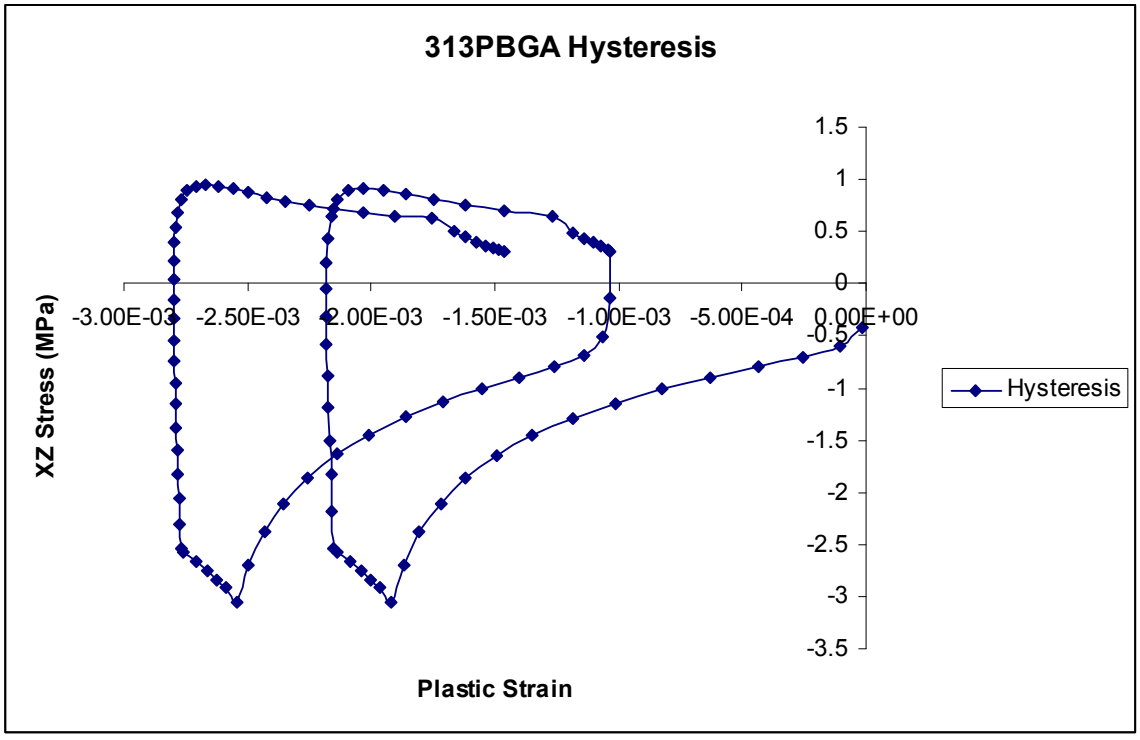

Figure 3-3 PBGA 313 Hysteresis loop

The area enclosed by the curve in the hysteresis loop represents the inelastic strain energy density for the package. When the hysteresis loop stabilizes it can be said that the amount of damage incurred per cycle is constant. This way, only two cycles need to be run in the finite element simulation in order to get a valid damage parameter such as plastic work. Then, the plastic work can be used in the crack growth equations presented in equations 3.8 and 3.9. Essentially, the crack growth is constant per cycle so long as the damage accrued per cycle is constant. If the hysteresis loop has not stabilized after two cycles, then more cycles need to be simulated until the hysteresis loop does finally stabilize. When determining the plastic work of the package from simulation, the plastic work values must be volume averaged over a layer of elements in order to reduce mesh sensitivity according to the formula given by Zhan [Zhan 2003].

$$\Delta W_{ave} = \frac{\Sigma \Delta W \cdot V}{\Sigma V} \qquad 3.7$$

Generally, the plastic work is volume averaged over the layer of elements where the damage is maximum and most likely to propagate in real world testing. For example, if the maximum damage is seen in the top of the interconnect, the top layer of elements will be selected for volume averaging. If the bottom layer, at the board side interface, sees maximum damage, then a layer of elements at the copper pad interface on the board side will be selected for volume averaging. The volume selected for averaging the plastic work has a great impact on the simulated life of the package and selection of the right layers should be done wisely.

Once the package has a sufficient number of failures, a two parameter Weibull plot can be generated. The Weibull plot gives the number of cycles to a component failure. On the X-axis, the number of cycles to failure is plotted. On the Y-axis, the percentage of the failed population is plotted. β and η are the two constants in the Weibull plot and they represent the slope and the characteristic life of the Weibull plot. The characteristic life is the point where 63.2% of the population has failed. The number of cycles for any percentage of failed components can be found by using

$$N = \eta \left[\ln \left[\frac{1}{1 - F(N)} \right] \right]^{\frac{1}{\beta}} \qquad 3.8$$

Where F(N) is the percentage of failed parts.

3.3 Unique Architecture PBGA packages

In the first experiment, four packages of varying architecture and package type are presented. The first package to be presented is a high I/O flip chip. Secondly, we have a more standard PBGA with a full array and large chip size. Thirdly, we have a perimeter array multi chip module featuring four chips in the mold. All the chips are of varying size. Fourthly, we have a perimeter array PBGA 256 package. Within the four packages everything varies from substrate thickness, die length, die thickness, pitch, solder ball height, I/O count, etc. On top of this, one batch of these packages were underfilled and tested against non underfilled packages. An equal number of packages with ImAg and HASL finish are tested and the reliabilities are plotted against each other. The differences in life due to underfilling and different surface finish are documented in the pages to follow.

Previously, it was thought that PBGA packages would not be able to withstand the harsh under the hood environment. However, it has been proven that the properly designed PBGA can easily meet the extreme environment conditions [Lindley 1995]. Previous studies have shown that packages with larger solder balls and a higher pitch have greater reliability [Syed 1996, Ghaffarian 2002]. Also, many studies have been done on surface finish. In Bradley's paper, he investigates HASL and ImAu packages. He finds that the consistency achieved with an immersion nickel plated pad is desired, but the pad ultimately underperforms the HASL and OPC packages [Bradley 1996]. Studies on solder mask and non solder mask defined pads have shown that NSMD pads provide nearly a 2X increase in life [Mawer 1999]. For our paper, all I/O's are SMD at the package interface, but NSMD on the board side. Out of all of these parameters,

perhaps the most important is die size [Ghaffarian 2002]. Because the die is so stiff, the package has a low effective CTE in the die-substrate region. This thermal mismatch is felt by the compliant solder balls, which deform under the stress. On top of this, the further the balls are away from the neutral point of the package, the quicker they fail. So the combined effect of distance and the low effective CTE due to die/substrate interaction puts an increased amount of stress on the interconnects [Syed 1996]. In this paper, dies of various size and thickness are tested.

The test vehicle also contains four chips that all have unique designs. Two of the packages on the board are high I/O flip chip. Flip chip packages are unique to standard wire bonded packages in that they can accommodate higher circuit density and provide more I/O's for the chip. Also, they have an area where a heat spreader can be attached providing greater heat transfer from the chip [Matsushima 1998]. 20 high I/O flip chips are tested in this paper. Half are ImAg finished while the other half is HASL finish. The failure results are shown. On top of this, we had a 128 I/O multi-chip package. The package consisted of a perimeter array featuring 4 different chips all of varying size housed in a diallyl phthalate mold. The different die sizes affected the life of the package with the largest chip causing the greatest thermal stress and driving the package to failure. The third package is a standard PBGA while the fourth package is a smaller perimeter array package featuring a smaller die. The test vehicle is shown below in figure 3-4.

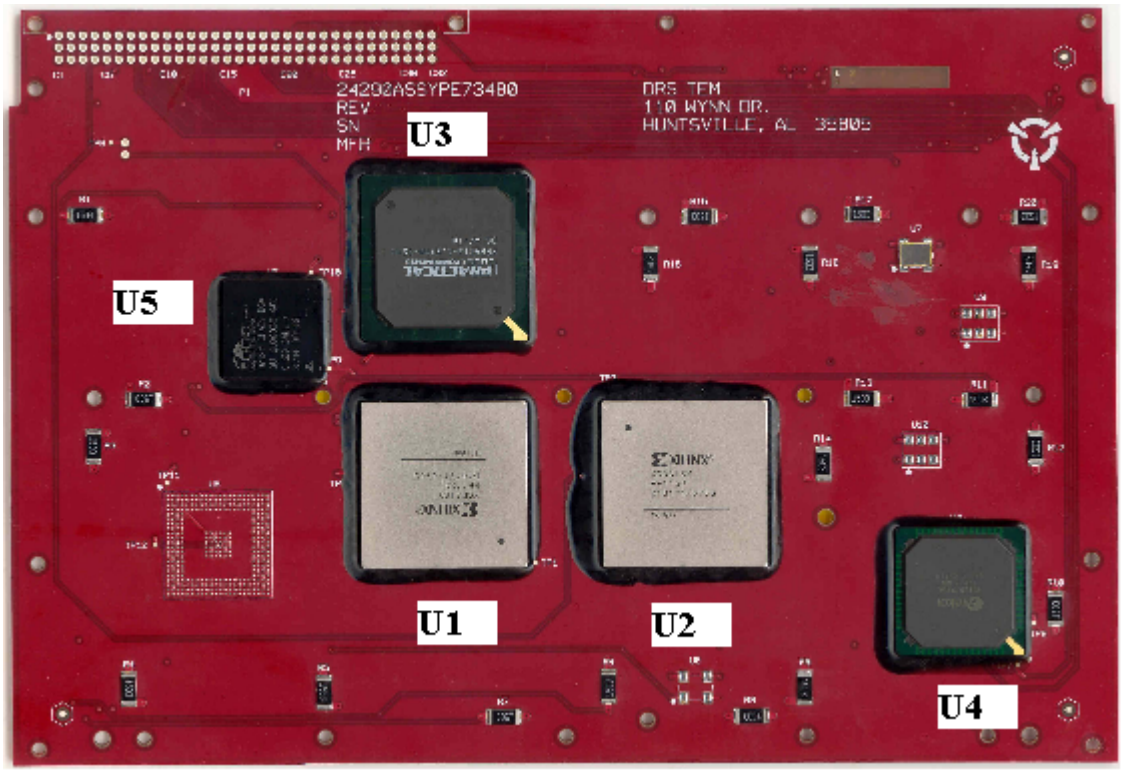

Figure 3-4 Test Vehicle Study 1 with unique I/O packages

The dimensions of the packages can be seen below in table 3-2:

Table 3-2 Package Dimensions for test vehicle

Parameter	BGA 1152 (U1 & U2)	PBGA 256 (U4)	PBGA 313 (U3)	PBGA 128 (U5)	Resistor 1503
Length	35 mm	27 mm	35 mm	20.7 mm	150 mils
Width	35 mm	27 mm	35 mm	20.7 mm	30 mils
Thickness	3.2 mm	2.13 mm	1.46 mm	3.05 mm	-
I/O	1152	256	313	128	-
Pitch	1 mm	1.27 mm	1.27 mm	1 mm	-
Ball Diameter	.6 mm	.75 mm	.63 mm	.56 mm	-
Ball Height	.5 mm	.7 mm	.6 mm	.56 mm	-
Package Type	Flip Chip Fine Pitch BGA	PBGA	PBGA	Multi-Chip PBGA	-

The test was specified as -40 to 125 Celsius with 30 minute dwells and 30 minute ramps at either end giving a 120 minute cycle. The chamber was profiled using Slim Kic software and the temperature plot can be seen below in Figure 3-5 :

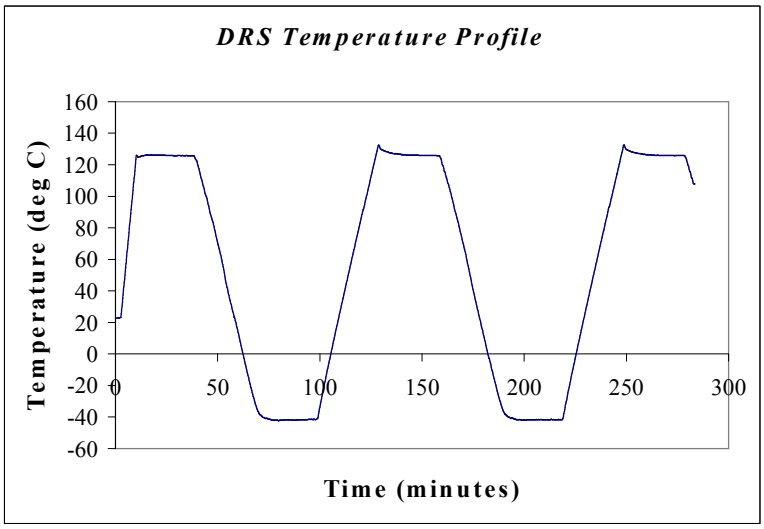

Figure 3-5 Unique I/O Thermal Profile

For testing purposes, all of the packages were daisy chained. In daisy chaining, all of the interconnects are connected to one another through metallic traces. In this manner an electrical current can be sent through all of the interconnects with the daisy chain providing conductivity. As the package is thermal cycled and damage is accrued in the interconnects, the measured resistance of the current sent through the daisy chain will change. This change in resistance of the signal is used to denote the point of failure in the package. When the resistance is infinite, this indicates an open interconnect where a crack has grown all the way through the interconnect. The resistances of the packages presented were constantly monitored using a switch box and multimeter. The packages were also manually probed to validate failure data. The resistances were recorded via a LABview program. Failure of a package was denoted as a 10% increase in resistance

where the package resistance stayed 10% or higher for the duration of the test. Failure was traced back to the original cycle count where the 10% increase in resistance was initially seen.

Lord Thermoset ME-531 underfill was chosen for the packages. It is a self filleting semiconductor grade epoxy used for the encapsulation of packages. The material properties of the underfill will be seen in the BGA 1152 finite element modeling section of this chapter. The effect of underfill on PBGA's is varying, either increasing or decreasing the life of the packages depending on the material properties of the underfill used. The effects of the underfill as well as some explanation as to underfill effect on packages is given in the package discussions to follow.

3.4 BGA 1152

The first package to be discussed is a high I/O flip chip. Flip chips are commonly used in high end logic devices. The flip chip has a large circuit density, operates at high speed, and generates a large amount of heat. A cross section of a flip chip can be seen below in figure 3-6.

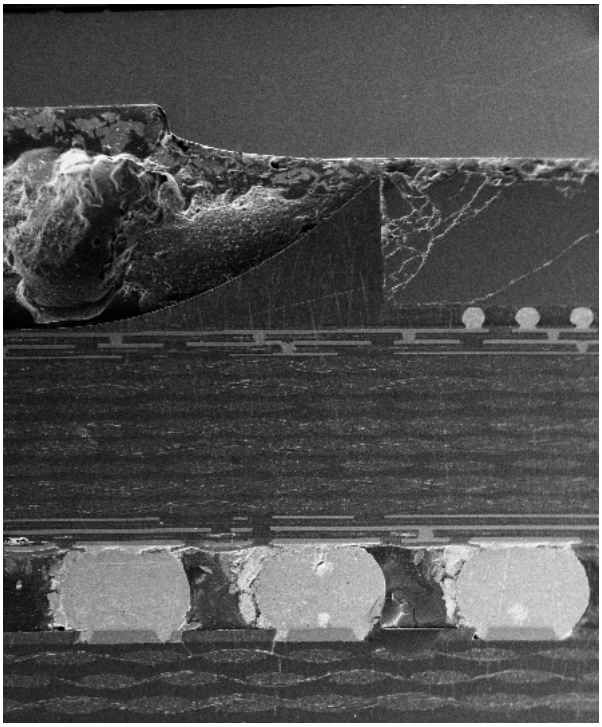

Figure 3-6 Flip Chip Cross Section

From Figure 3-6, the chip is attached to the substrate via flip chip solder bumps. A copper lid is attached to the top of the package and a thin insulating material is put between the copper lid and the chip. This whole assembly is mounted on the PCB with standard size solder balls. Matsushima has shown that the flip chip can accommodate large pitch count packages with improved reliability characteristics [Matsushima 1998]. Li has shown that a higher young's modulus and higher CTE heat spreader will lower warpage in the package. Li also showed that a hi-CTE ceramic substrate is more reliable than a BT substrate. The stress reduction in package reduces with increasing die size and package size. When using a hi-CTE ceramic substrate the corner ball is usually the first to fail because the influence of the die is abated due to the large CTE mismatch between the substrate and PCB [Li 2001]. For the package presented in this test, a ceramic substrate was used. Table 3-3 shows the package dimensions for BGA 1152.

Table 3-3 BGA 1152 Package Dimensions

Length	35 mm
Width	35 mm
I/O	1152
Pitch	1 mm
Ball Diameter	.6 mm
Ball Height	.5 mm
Substrate Thickness	1.2 mm
PCB Thickness	2.11 mm

An equal number of flip chip packages were underfilled and tested as well as an equal number of HASL and ImAg finish packages were tested against each other. The first package is the ImAg finish package. In previous tests involving the reliability of different solder pad finishes, Bradley and Banerji reported that the HASL finished boards outperformed other finishes commonly found in electronic packages. One problem with the HASL finish is that it is difficult to get an even coating, whereas the immersion nickel based finishes can give a smooth and even coating. However, it is thought that the nickel migrates through the porous gold layer and leads to eventual corrosion [Bradley 1996]. Our results showed that the ImAg finish BGA 1152 package greatly underperformed the HASL finish BGA 1152 package. The results can be seen in figure 3-7 below.

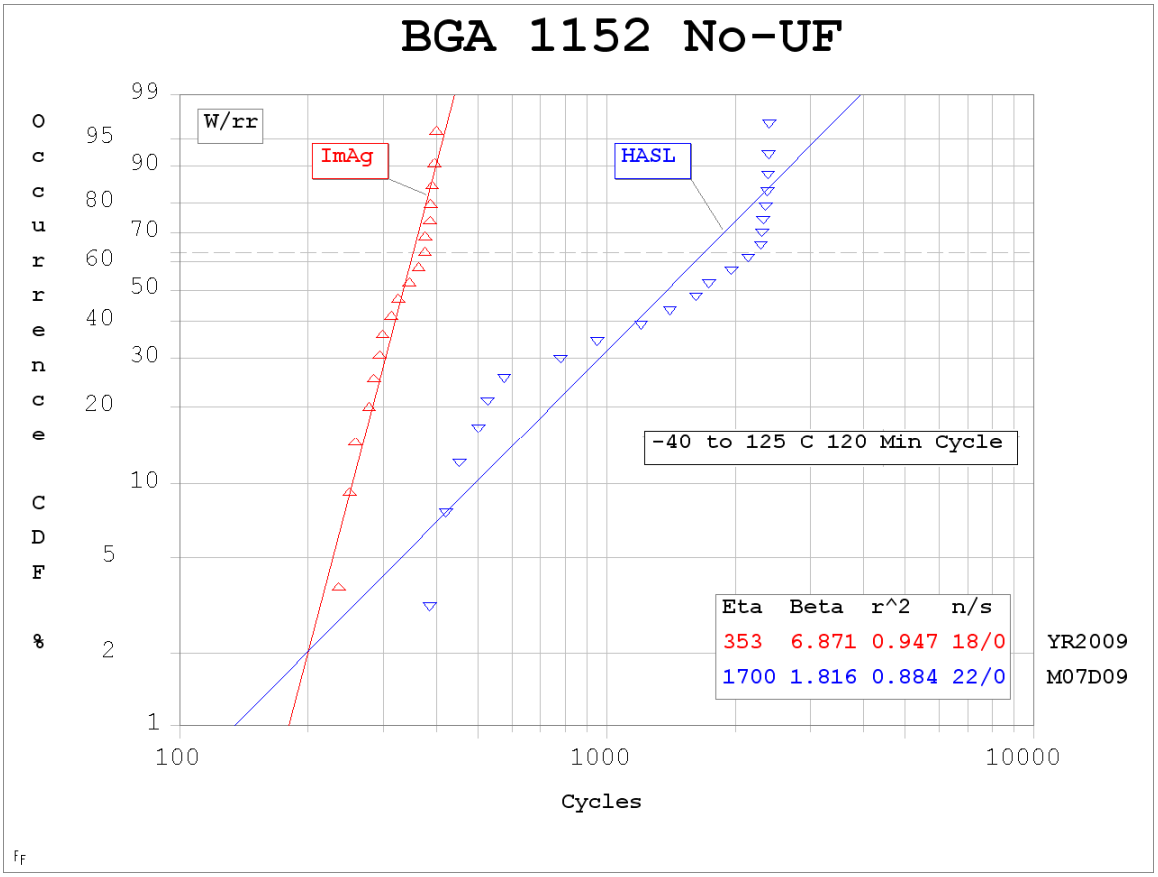

Figure 3-7 Weibull plot BGA 1152 ImAg and HASL

As can be seen from figure 3-7, the HASL board greatly outperforms the ImAg board. The HASL board has a nearly 5X life improvement over the ImAg finish board. This trend seems to be constant throughout all of the unique I/O packages tested, however, none are as pronounced as for the high I/O BGA 1152 flip chip. The HASL finish shown above demonstrates at least two different failure modes as indicated by the change of slope in the failure distribution. The performance of the HASL finish vs. the ImAg finish supports previous findings by Bradley, though the difference is more extreme in the BGA 1152 package.

Secondly, an equal number of the packages were underfilled and thermal cycled under the same temperature profile. The underfill greatly improved the life of the package as can be seen in figure 3-8 below.

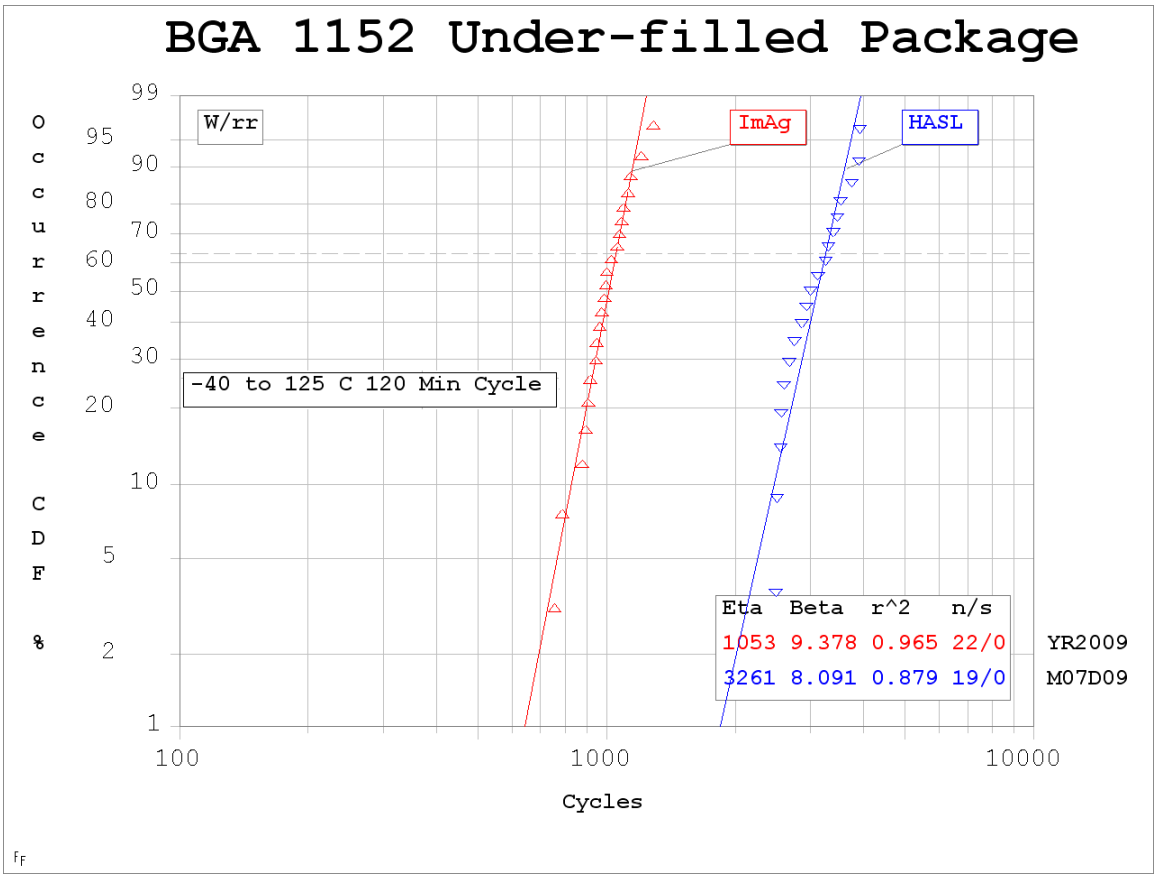

Figure 3-8 Weibull plot for underfilled Xilinx packages

The characteristic life greatly improved for both packages, but the HASL still outperformed the ImAg finish by nearly 3X. In this plot, only one failure mode is demonstrated as the failure distributions fall on a linear line with a steep slope. Comparisons of how the different pad finishes performed when underfilled our shown in figure 3-9 and figure 3-10.

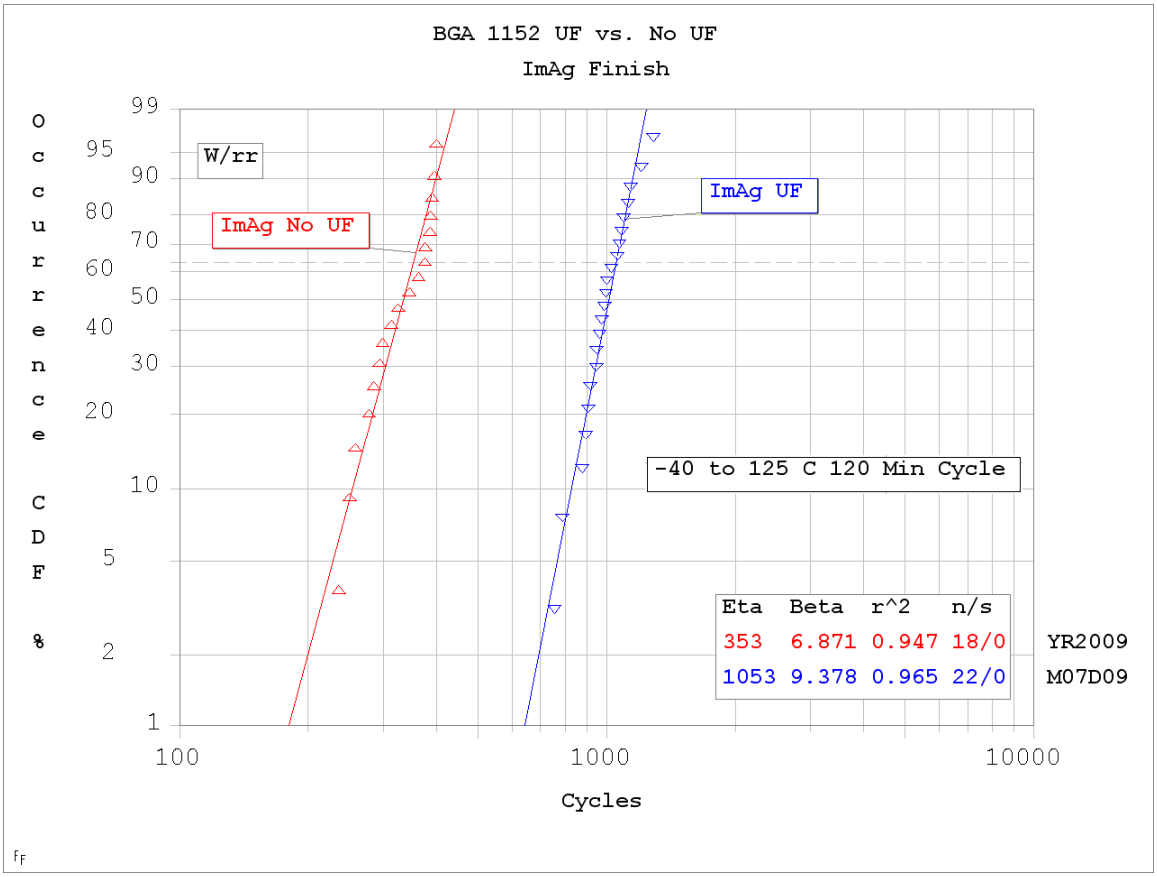

Figure 3-9 Weibull plot for ImAg finish underfill vs. non underfilled

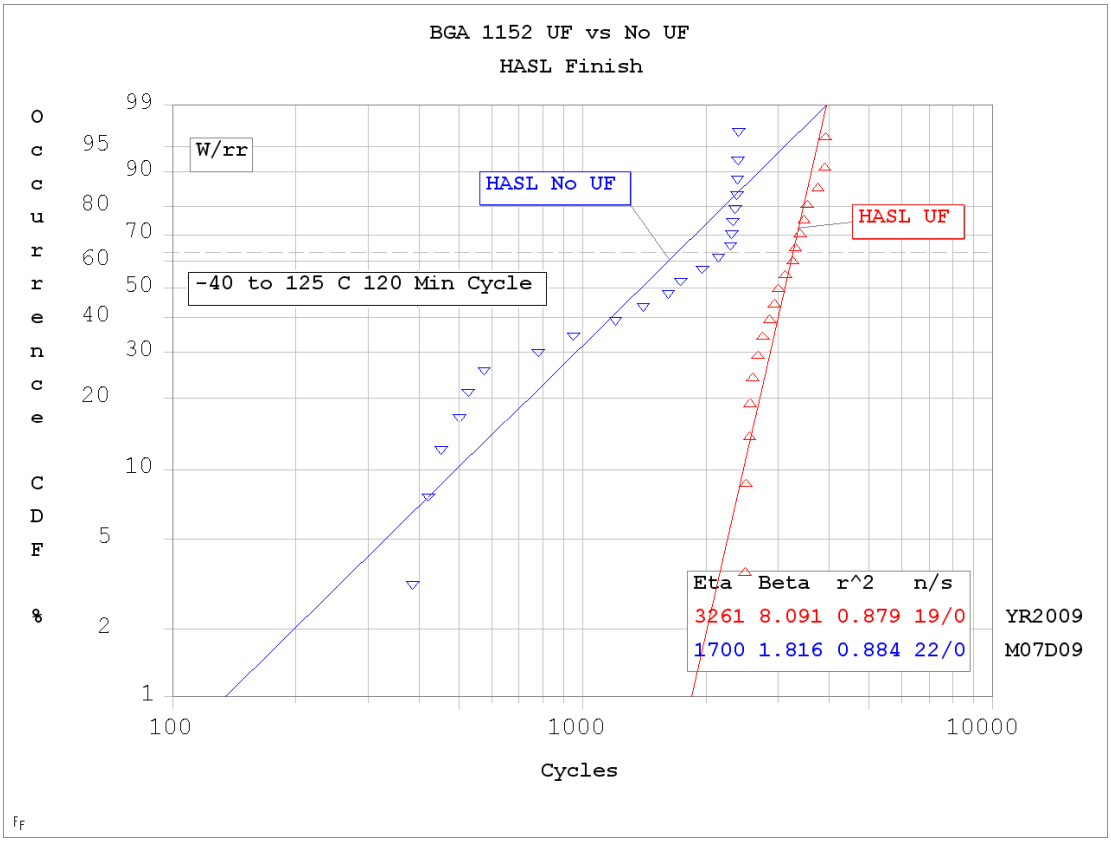

Figure 3-10 Weibull plot for HASL finish underfill vs. non underfill

In the ImAg finish, the life improvement was more pronounced with a nearly 3X life improvement due to underfill and in the HASL, it was a 1.7X life improvement. The table below summarizes the characteristic lives of all the BGA 1152 packages.

Table 3-4 BGA 1152 life comparison

Pad Finish	UF	(η) Characteristic Life
ImAg	No	353 cycles
ImAg	Yes	1,053 cycles
HASL	No	1,700 cycles
HASL	Yes	3,261 cycles

3.4.1 BGA 1152 FEM

For modeling purposes a smear plate was used to represent the chip, flip chip solder joints, the thin insulating material, and the copper heat lid. A volume averaging technique was used to get the material properties for the smear plate. A rule of mixtures shown below in equations 3.7 and 3.8 was used to get the effective young's modulus and an effective CTE for the smear plate. [Clech 1996].

$$\alpha_{Eff} = \frac{\sum E_i V_i \alpha_i}{\sum E_i V_i} \qquad 3.7$$

$$E_{eff} = \frac{\sum E_i h_i}{\sum h_i} \qquad 3.8$$

Where h is the thickness of the respective layers, V is the volume of the layers, E is the young's modulus and α is the coefficient of thermal expansion. The following values were used for the material properties:

Table 3-5 Properties of smear plate components

Material	$\alpha_x (ppm/^oC)$	$\alpha_y (ppm/^oC)$	$\alpha_z (ppm/^oC)$	E(MPa)
Copper Lid	16.3	16.3	16.3	128932
Thin insulating material	80	80	80	1240
Silicon Die	26	26	26	131000
Solder Bumps	20	20	20	51000
Underfill	38	125	38	6500

Using the rule of mixtures shown above, the following dimensions were used for the smear plate:

Table 3-6 Smear plate properties used in simulation

E(MPA)	α_x(PPM)	α_y(PPM)	α_z(PPM)
114357	13.3	13.6	13.3

The dimensions of the smear plate components can be seen below in table 3-7

Table 3-7 Flip Chip Dimensions

Component	Thickness (mm)	Length (mm)
Lid	.07	35
Glue	.5	22
Chip	.7	22
Solder bumps	.05	--
Underfill	.05	22

A diagonal view of the finite element model is seen below in figure 3-11

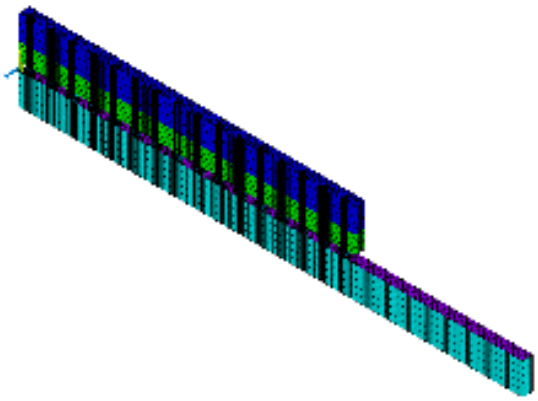

Figure 3-11 BGA 1152 Finite Element Model

A diagonal slice symmetry model of the package was created in order to cut down on simulation time. The solder balls are 63Sn37Pb eutectic tin lead interconnects. A table of the material properties used in the simulation can be seen below.

Table 3-8 Material properties used in BGA 1152 FEM.

Component	E GPa	α ppm/°C	υ
PCB	17(x,z) 7(y)	15(x,z) 67 (y)	.39
Solder Ball	30	24	.35
Ceramic Substrate	276	6.7	.3
Solder Mask	3	30	.3
Copper Pad	128	16	.34

The Anand constants used for simulation can be seen in the table below

Table 3-9 63Sn37Pb Anand constants [Darveaux 2000]

63Sn37Pb Anand constants	
S_o	12.41 (MPa)
Q/k	9400 $\left(1/K\right)$
A	4.0e6 $\left(1/\text{sec}\right)$
ζ	1.5
m	.303
h_o	1378.95(MPa)
n	.007
a	1.3
$\hat{s}$	13.79(MPa)

Similarly to the results reported by Li, the corner ball was the first to fail as the effect of the die is abated by the stiffer ceramic substrate [Li 2001]. In figure 3-12 below, the corner ball experienced the most damage.

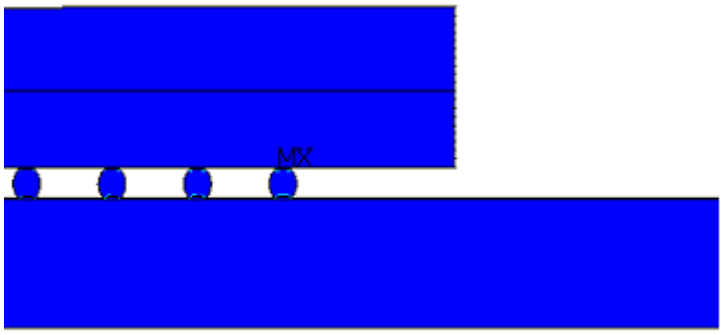

Figure 3-12 BGA FEM 1152 Failure

As mentioned above, corner ball failure was expected in this model as the ceramic substrate abates the effect of the die and causes the distance to neutral point formula to come into action, causing the greatest amount of stress in the corner, or furthest, solder ball. Below, an image of the failed solder ball as identified by the ANSYS simulation is placed next to an actual failed ball. Figure 3-13 shows that the crack propagated through the top of the interconnect along the package interface.

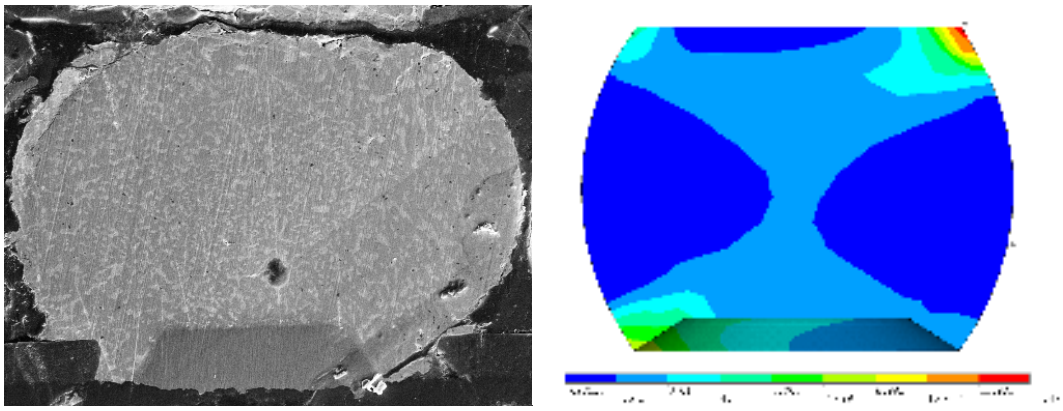

Figure 3-13 Failed ball compared to failed simulation

An image of the top layer of the solder ball with maximum damage is shown below in figure 3-14. This is also the layer that was used for plastic work calculation.

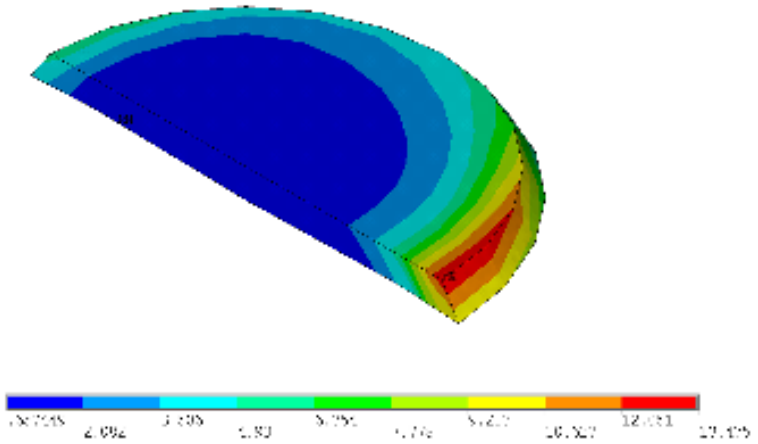

Figure 3-14 showing the top layer failure

The hysteresis plot and the plastic work plot for the package are shown below in figures 3-15 and 3-16.

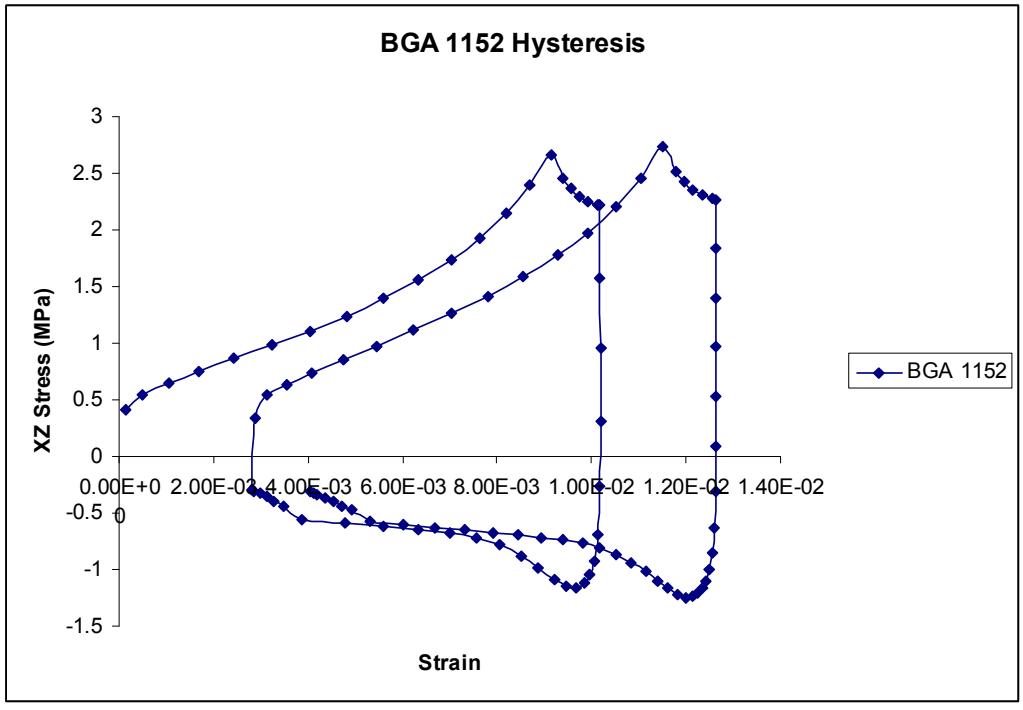

Figure 3-15 Hysteresis BGA 1152

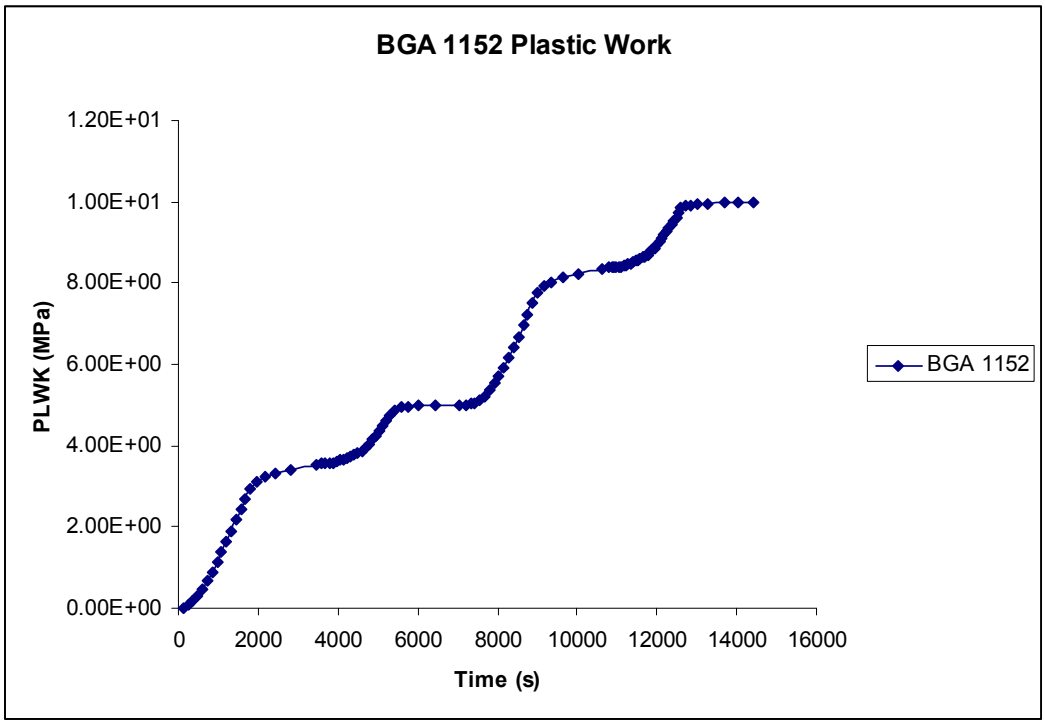

Figure 3-16 Plastic Work Plot BGA 1152

Figure 3-15 shows show that the hysteresis loop stabilized after two simulated thermal cycles. The inelastic strain energy is represented by the area enclosed in the hysteresis loop. The plastic work is plotted for the package in Figure 3-16. It approaches ten MPa when the simulation ends.

As mentioned previously, the BGA 1152 was underfilled and thermal cycled. Previous tests have shown that the effect of underfill on larger BGA's can be both detrimental and beneficial to the life of the package depending on the material properties of the underfill. Pyland in his 2000 paper shows that higher CTE underfills cause an increase in strain in super BGA's [Pyland 2000]. For smaller packages, the effect of underfill has been shown to increase life [Elkaday 2004, Liji 2002]. In this test, the larger BGA 1152 package was underfilled as were the smaller U3, U4, and U5 packages shown earlier. The results are documented in the pages to follow.

The first underfilled package presented is the BGA 1152 flip chip. An image of the finite element model is shown below in figure 3-17.

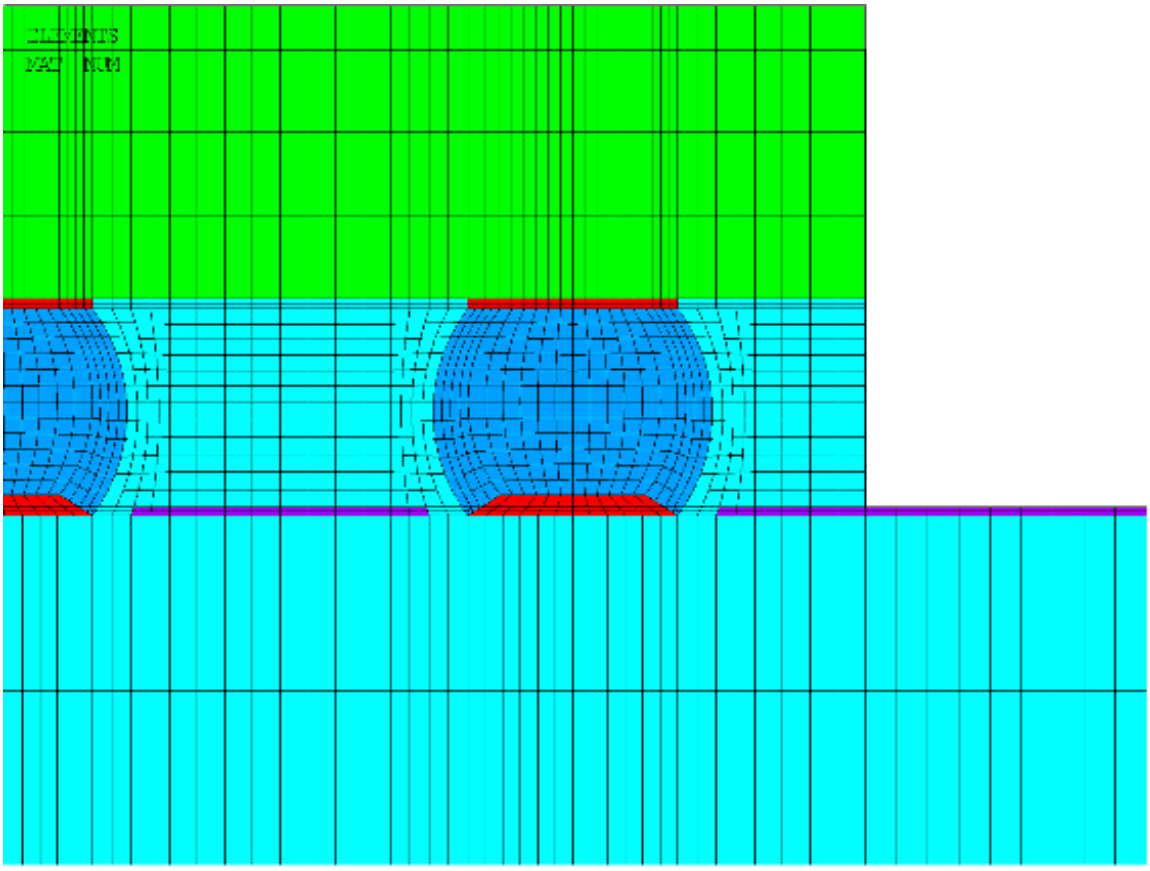

Figure 3-17 Underfilled BGA 1152 package

The sky blue elements encircling the solder ball in Figure 3-17 were elements representing the underfill. The material properties of the underfill can be seen below in Table 3-10

Table 3-10 ME-531 Underfill Properties

E(MPA)	α_x(PPM)	α_y(PPM)	α_z(PPM)
6000	21	21	85

Other than the underfill, the material properties of the package were identical to the ones used for the non underfilled BGA 1152. A diagonal view of the underfilled BGA 1152 package can be seen below in Figure 3-18.

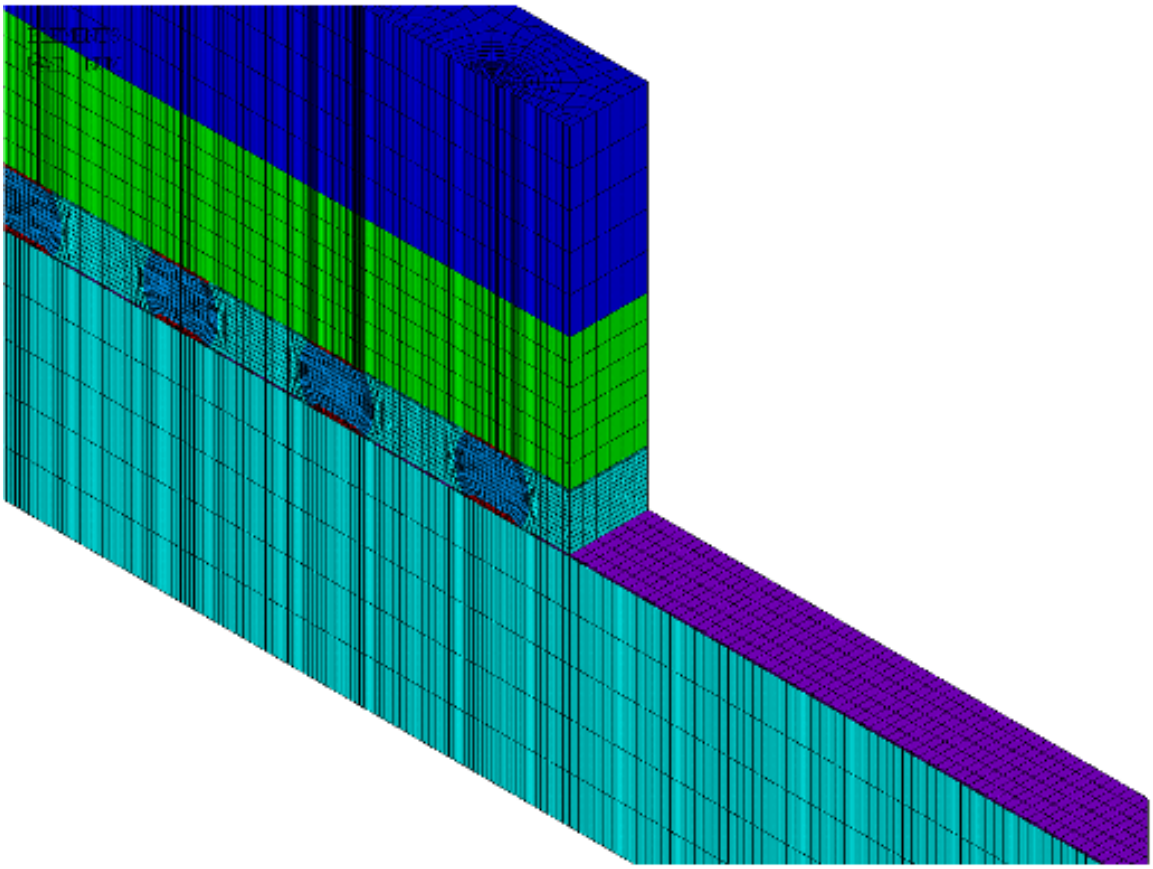

Figure 3-18 diagonal view of UF BGA 1152

Similarly to the non underfilled BGA 1152, the underfilled BGA 1152 showed first failure in the corner solder ball as can be seen in Figure 3-19 below.

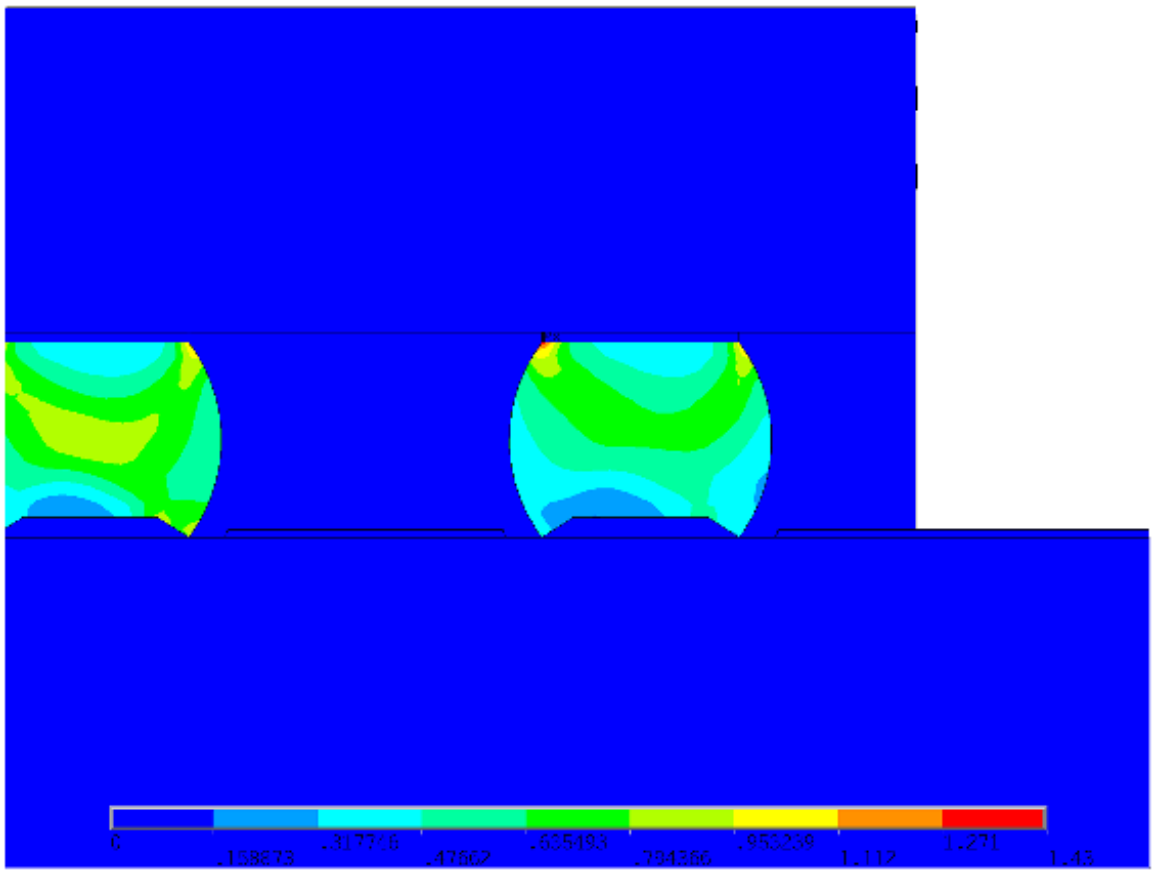

Figure 3-19 UF BGA 1152 failure in corner ball

Below in Figure 3-20, a diagonal shot of the failed solder ball can be seen.

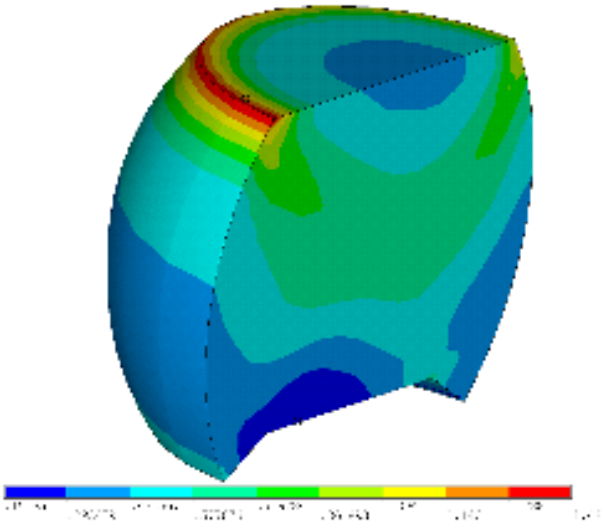

Figure 3-20 diagonal UF solder ball BGA 1152

Figure 3-20, above, shows that the maximum damage has moved from the top right corner of the solder ball to the top left corner of the solder ball. For comparison purposes, the hysteresis plots of the underfilled and non underfilled models were plotted against each other and can be seen in figure 3-21 below.

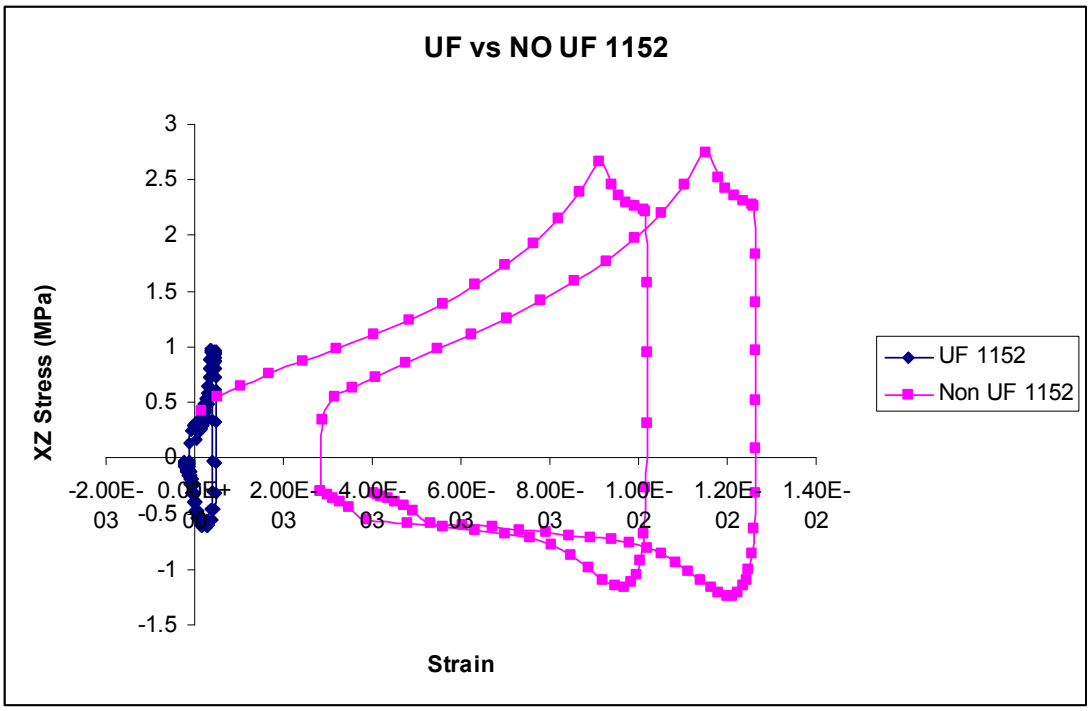

Figure 3-21 hysteresis loop of UF and non UF BGA 1152

In Figure 3-21, the underfilled BGA 1152 hysteresis loop is much smaller than the non underfilled BGA 1152 indicating that the underfilled package incurred significantly less damage than the non underfilled package. The Weibull plots in figure 3-9 and figure 3-10 prove this by tracking the characteristic lives of the packages in a harsh thermal environment. The plastic work plot comparing the plastic work of the two packages is shown below in Figure 3-22.

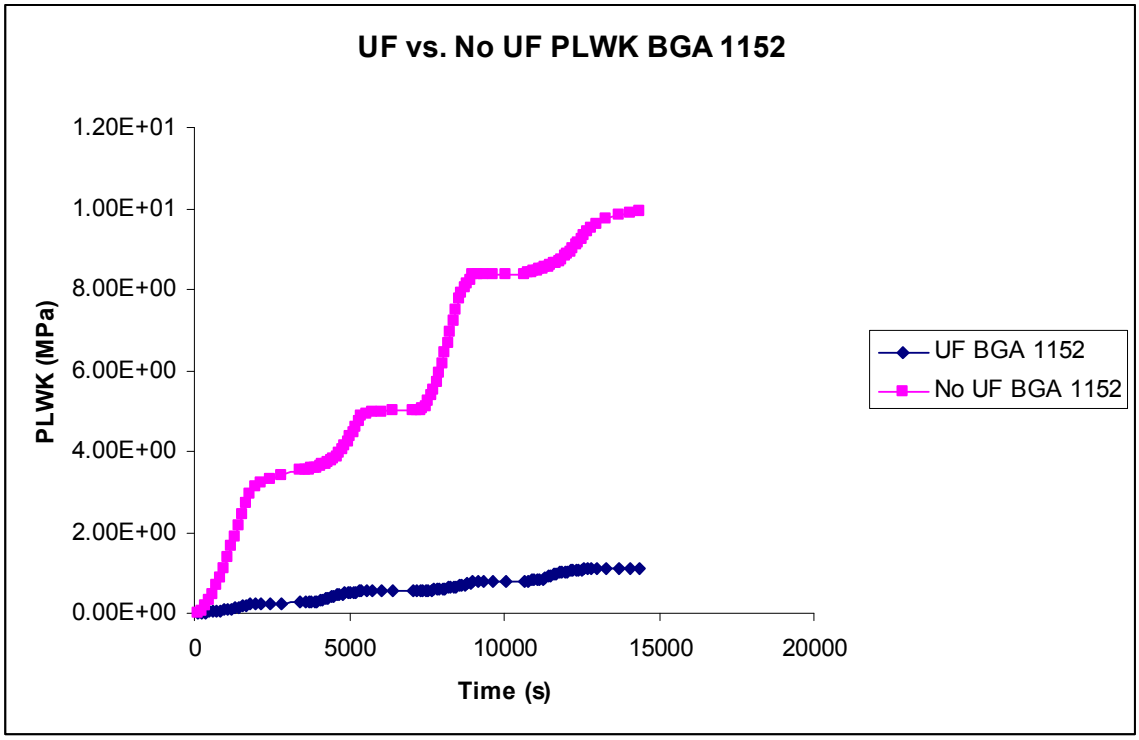

Figure 3-22 plastic work of the UF and non UF package BGA 1152

Figure 3-22 shows the plastic work of the two packages. Similarly to the hysteresis loop of the two packages, the underfilled BGA 1152 incurs much less damage than the non underfilled package. The damage in the non underfilled BGA 1152 is approximately 10X the damage in the underfilled BGA 1152. The slopes of the two packages also show drastic difference. The slope of the non underfilled BGA 1152 is approximately 10X the non underfilled package indicating that the package develops plastic work ten times as fast as the underfilled package. The underfill clearly improves the fatigue life of the BGA 1152 package.

3.4.2 BGA 1152 Life Prediction

[Darveaux 2000] originally proposed a life prediction model for solder interconnects on CBGA assemblies with solder mask defined pads. [Lall 2004] later measured these constants for non solder mask defined pads on plastic packages. The measurements for growth constants were made by measuring crack growth vs. cycle count and crack growth vs. inelastic strain energy density. The crack growth and life prediction models can be seen below and are taken from [Lall 2004].

$$N_i(\text{cycles}) = K_1\left(\Delta W_{AVE}\right)^{K_2} \tag{3.9}$$

$$\frac{da}{dN}\left(\frac{mm}{cycle}\right) = K_3\left(\Delta W_{AVE}\right)^{K_4} \tag{3.10}$$

$$K_1\left(\frac{cycles}{MPa^{K_2}}\right) = 14.062$$

$$K_2 = -1.53$$

$$K_3\left(\frac{mm}{cycle \cdot MPa^{K_4}}\right) = 6.967E-04$$

$$K_4 = .7684$$

Failure is achieved when the crack grows across the pad interface. The characteristic life can be defined as

$$\alpha_W(\text{cycles}) = N_i + \frac{a}{\frac{da}{dn}} \tag{3.11}$$

The simulation results are highlighted Table 3-11 below

Table 3-11 Experimental vs. Simulation results for BGA 1152

	Characteristic Life (η)	Error
Experiment	353 cycles	18%
Simulation	286 cycles	

Table 3-11 shows that the model predicted failure within 18% of the actual experimental failure from testing.

3.5 PBGA 313

The PBGA 313 is a full array PBGA with eutectic tin lead solder balls. The dimensions of the package can be seen in the table below.

Table 3-12 Dimensions of PBGA 313

Length	35 mm
Width	35 mm
I/O	313
Pitch	1.27 mm
Ball Diameter	.63 mm
Ball Height	.6 mm
Substrate Thickness	.57 mm
Die Length	4.44
PCB Thickness	2.11 mm

Initially, it was thought that PBGA packages would not be sturdy enough to withstand the harsh environment found under the hood of a car, but tests by [Syed 1996] and others

showed that the properly designed PBGA's with large pitch and larger substrates could withstand the harsh temperatures found in extreme environments. The PBGA 313 is an example of such a PBGA designed to withstand harsh thermal environments. The chip thickness is .5mm while the length is 4.44mm. The BT substrate thickness is .6mm. Generally, it has been shown that a substrate of .35-.55mm is optimal for reliability. The thicker the substrate, the less the effect of the die on the package so that the effective CTE in the die region is not as pronounced [Syed 1996]. Also, a larger diameter solder ball offers more stress relief according to the equation

$$\sigma = \frac{P}{A} \qquad 3.12$$

So that increasing the solder ball and pad diameter offers more area to take up the stress [Mawer 1999]. With larger interconnects, a larger pitch, thicker substrate, and a relatively small die, it was assumed that the PBGA 313 package would have a good performance in the thermal cycling experiment. Similarly to the BGA 1152 package, the PBGA 313 package had an equal number of ImAg and HASL boards as well as an equal number of underfilled to non underfilled boards. Once again, the ImAg underperformed the HASL finish boards while the underfilled boards offered an increase in life. A cross section of the package can be seen on the next page in Figure 3-23.

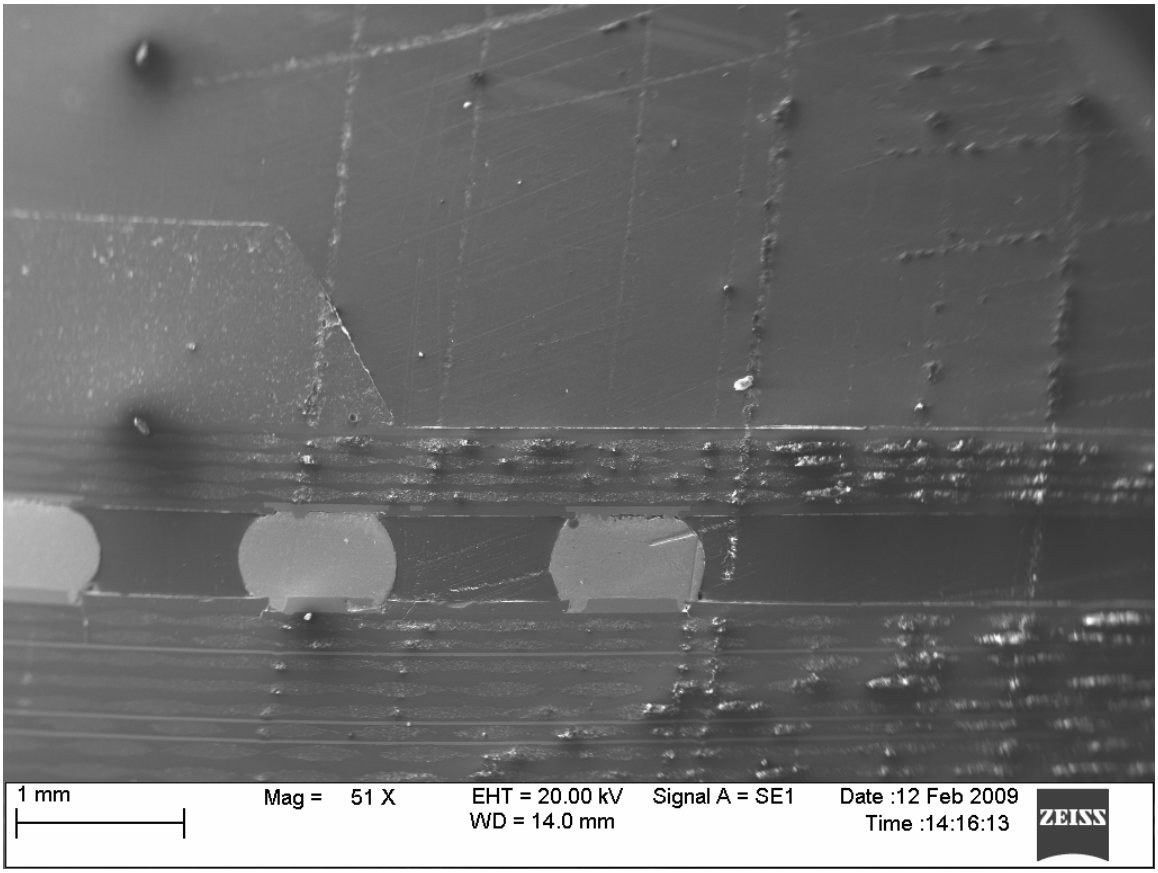

Figure 3-23 SEM Cross Section of PBGA 313

The solder interconnects were eutectic tin lead 63Sn37Pb. Again, the HASL finish outperformed the ImAg finish, but nowhere near as drastically as in the BGA 1152 package. The results can be seen below in Figure 3-24.

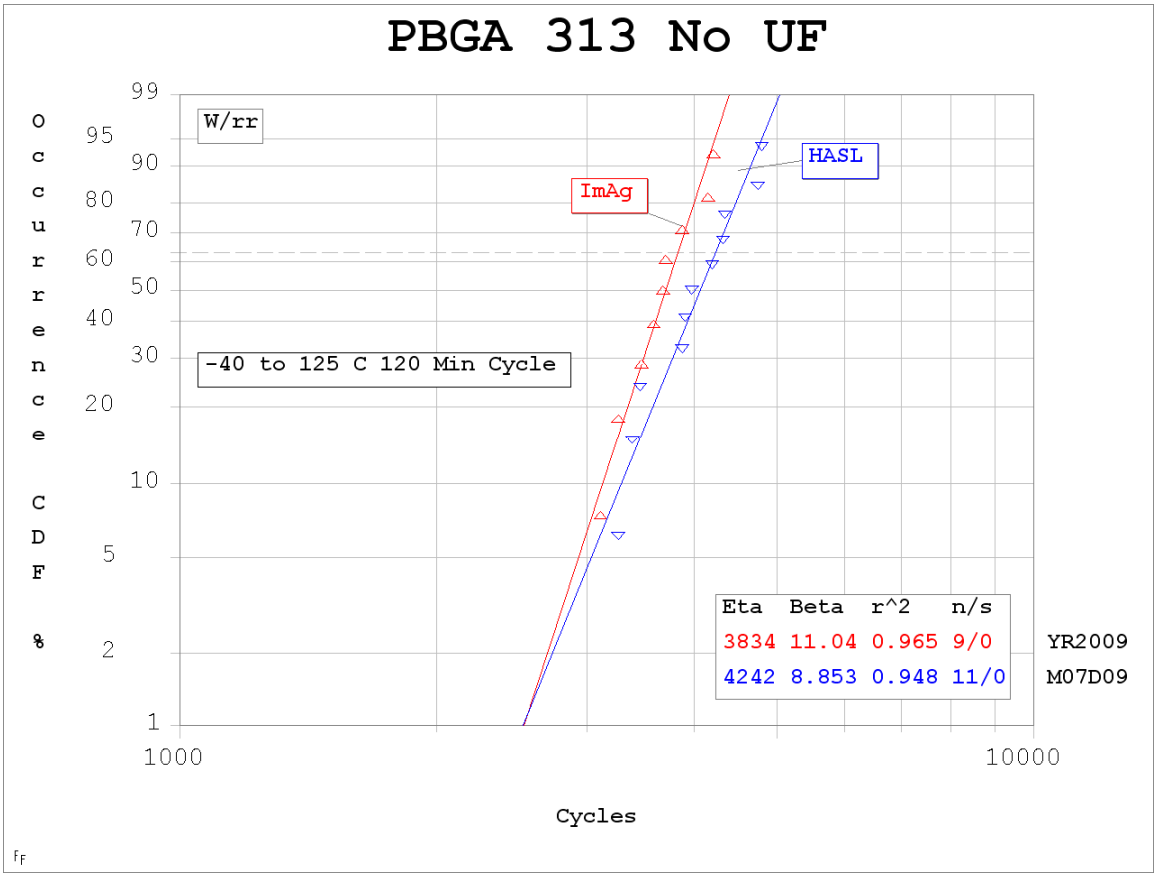

Figure 3-24 PBGA 313 non underfilled Weibull plot

The HASL characteristic life was 400 cycles larger than the ImAg pad finish characteristic life. The underfilled packages had not failed as of 3,400 cycles, so a Weibull plot can not be generated. With no failures as of 3,400 cycles the underfilled packages have clearly outperformed the non underfilled packages. Failure of the non underfilled packages was seen in the die shadow of the package where the crack propagated across the top of the interconnect along the package interface. An SEM image shown below in Figure 3-25 shows the failed solder ball in the die shadow region.

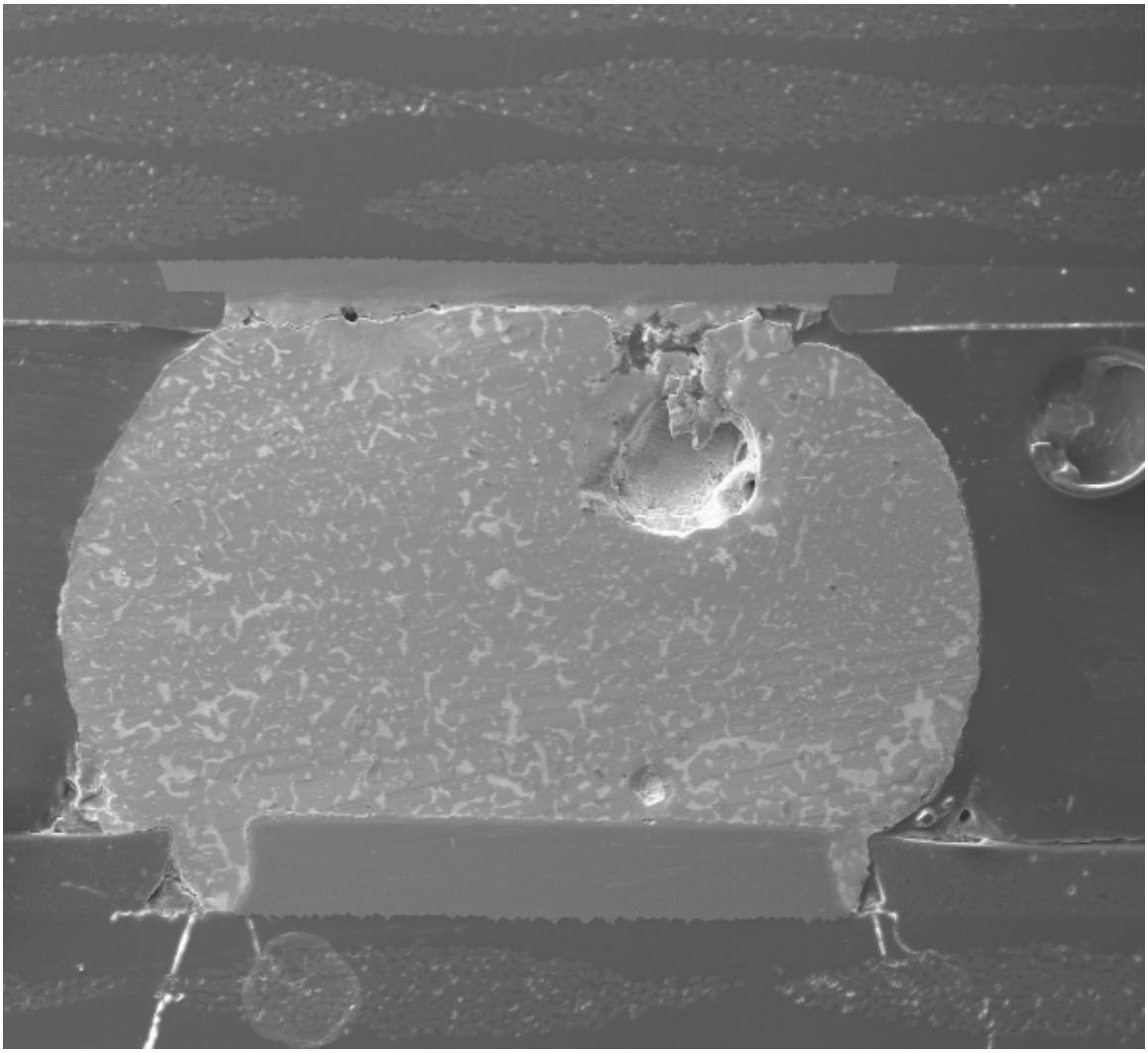

Figure 3-25 PBGA 313 Failure

Figure 3-25 shows a crack at the top of the interconnect which propagated along the package side interface. This solder ball was located in the right die shadow of the package and was the first to fail in testing and simulation.

3.5.1 PBGA 313 FEM

The PBGA 313 diagonal symmetry model was recreated in ANSYS and the thermal cycle simulated. A diagonal view of the model can be seen below in Figure 3-26

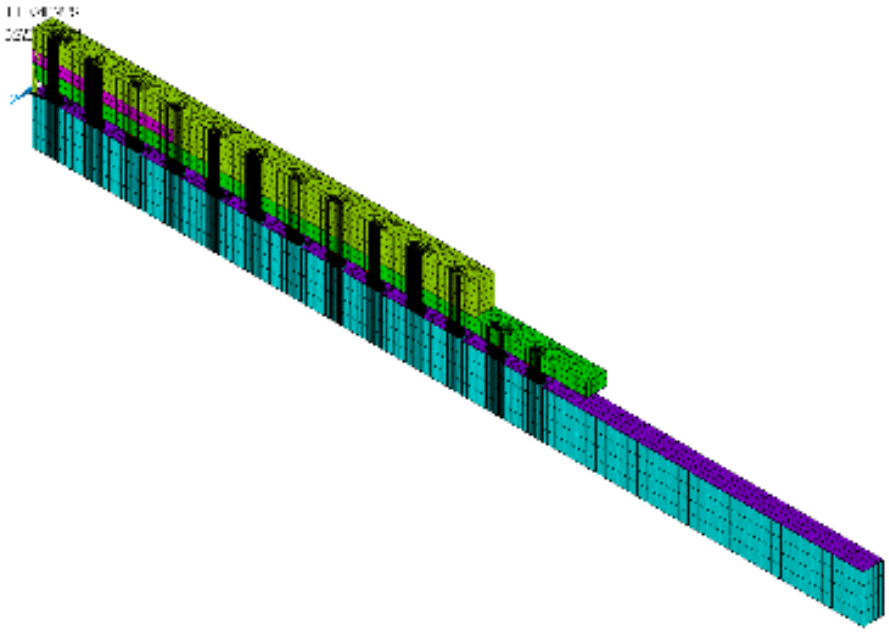

Figure 3-26 Diagonal symmetry model PBGA 313

A close up image of the modeled solder ball can be seen below in Figure 3-27

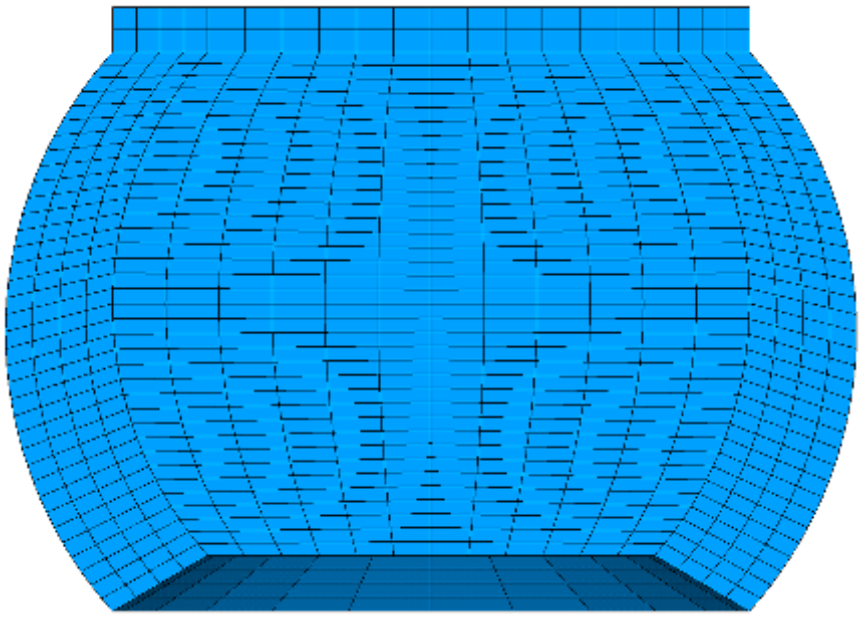

Figure 3-27 PBGA 313 FEM Solder Ball

The same Anand constants used for the BGA 1152 were used for the PBGA 313 as both packages had tin lead eutectic solder interconnects. The material properties of the package can be seen below in Table 3-13

Table 3-13 Material properties PBGA 313

Component	E GPa	α ppm/^{o}C	υ
PCB	17(x,z) 7(y)	15(x,z) 67 (y)	.39
Solder Ball	30	24	.35
BT Substrate	18(x,z)7(y)	12(x,z)57(y)	.3
Solder Mask	3	30	.3
Die Adhesive	7	52	.35
Silicon Die	162	2.5	.28
Mold	23	15	.3
Copper Pad	128	16	.34

The model and experiment showed the same failure mode with the solder ball in the die shadow region being the first to fail. A crack started in the top corner of the solder ball and propagated across the package interface. Figure 3-28 below demonstrates the die shadow failure from the simulation. Figure 3-29 below that shows the die shadow failure identified by finite element simulation.

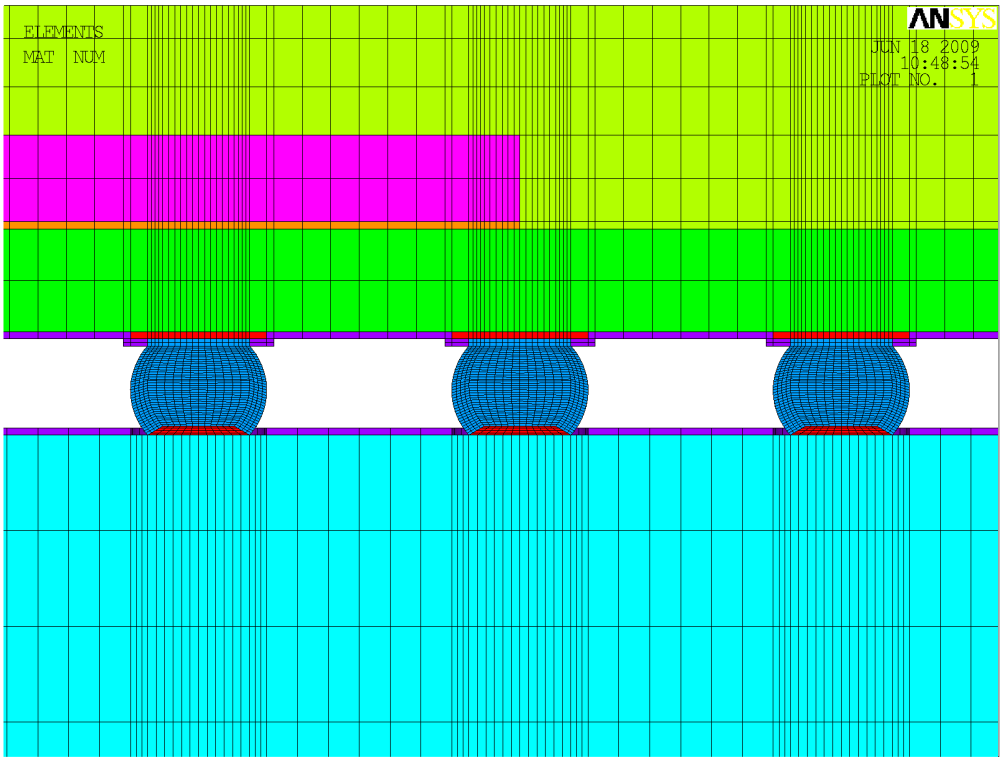

Figure 3-28 PBGA 313 Die Shadow Region

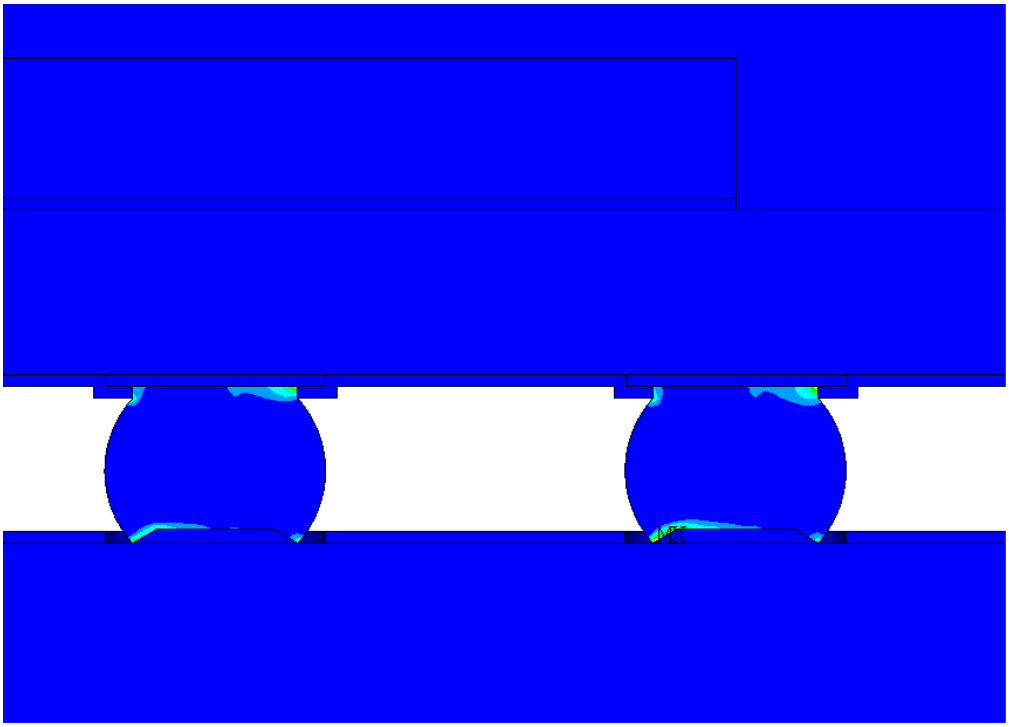

Figure 3-29 PBGA 313 Failed Die Shadow Region

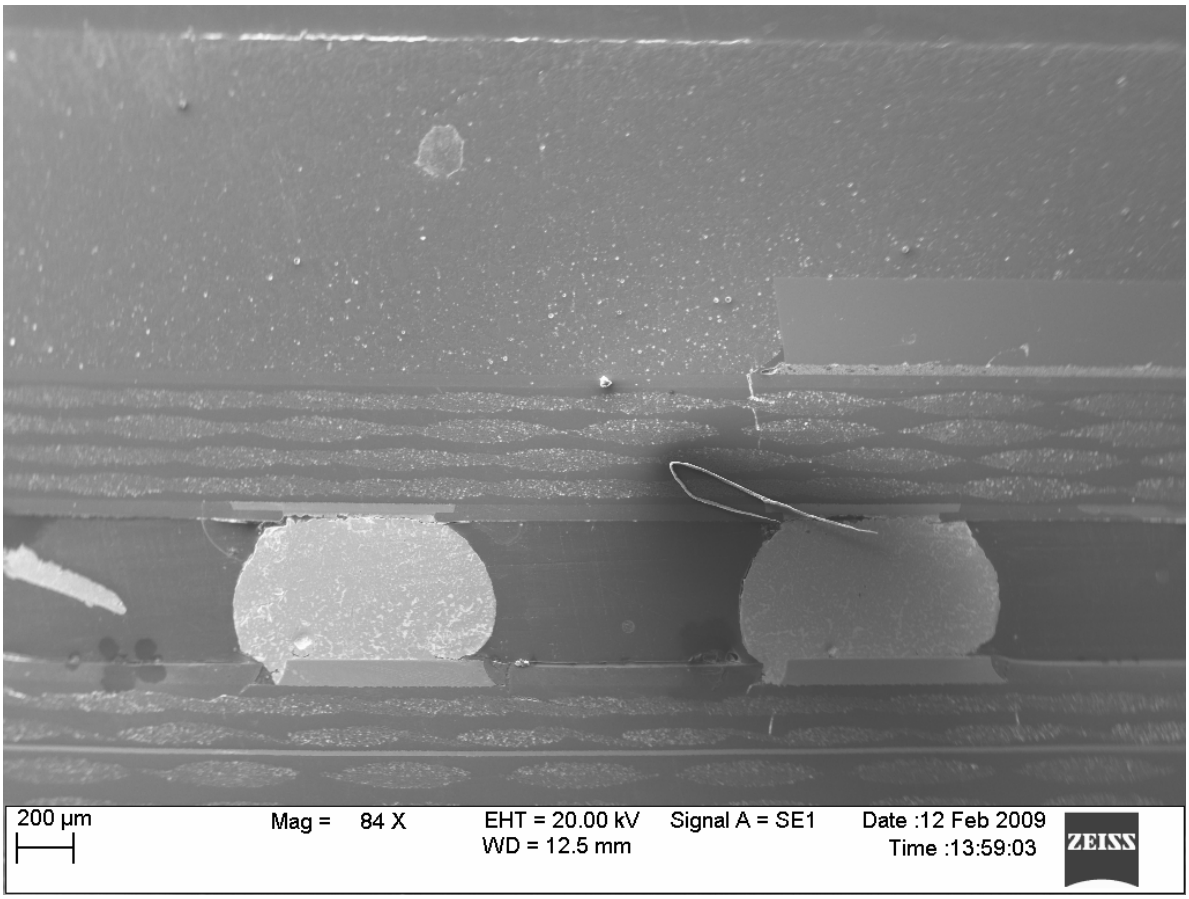

Figure 3-30 SEM results showing die shadow failure

Figure 3-30 shows a crack that has grown all the way across the package interface in the left most interconnect. A close up of the interconnect demonstrating crack growth is seen below in figure 3-31. Notice that the crack initiates in the top left corner of the interconnect and propagates across the top part of the interconnect at the package interface causing a loss of signal.

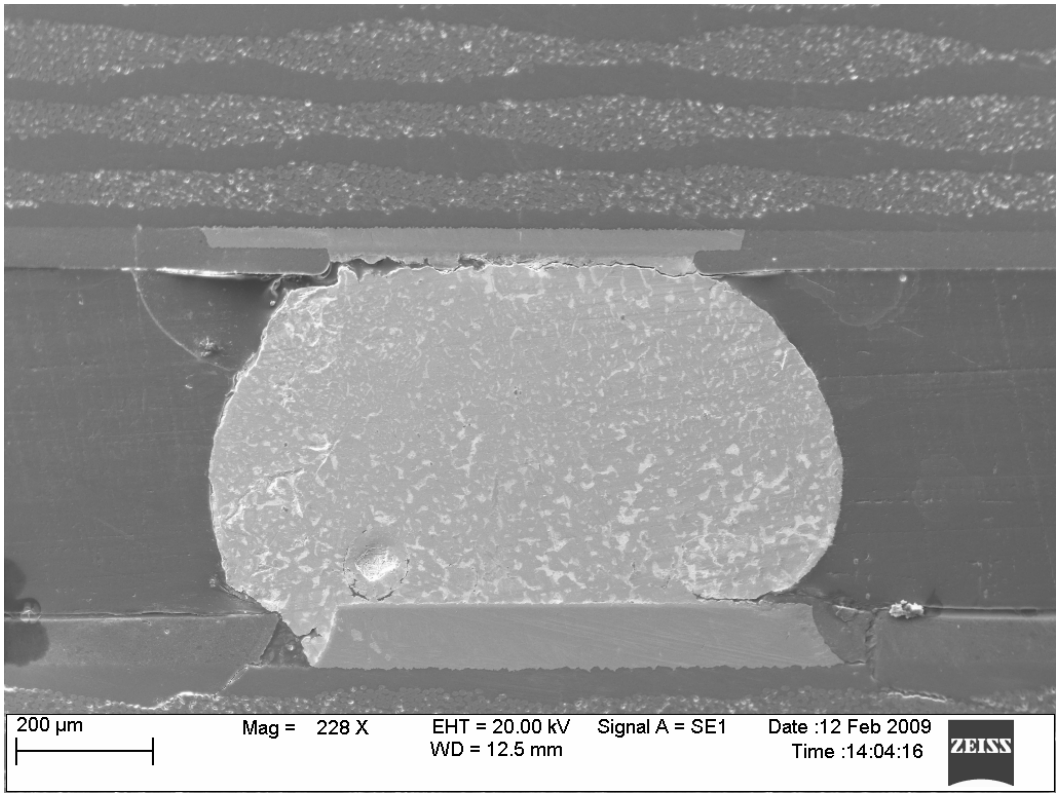

Figure 3-31 PBGA 313 Die Shadow Failure

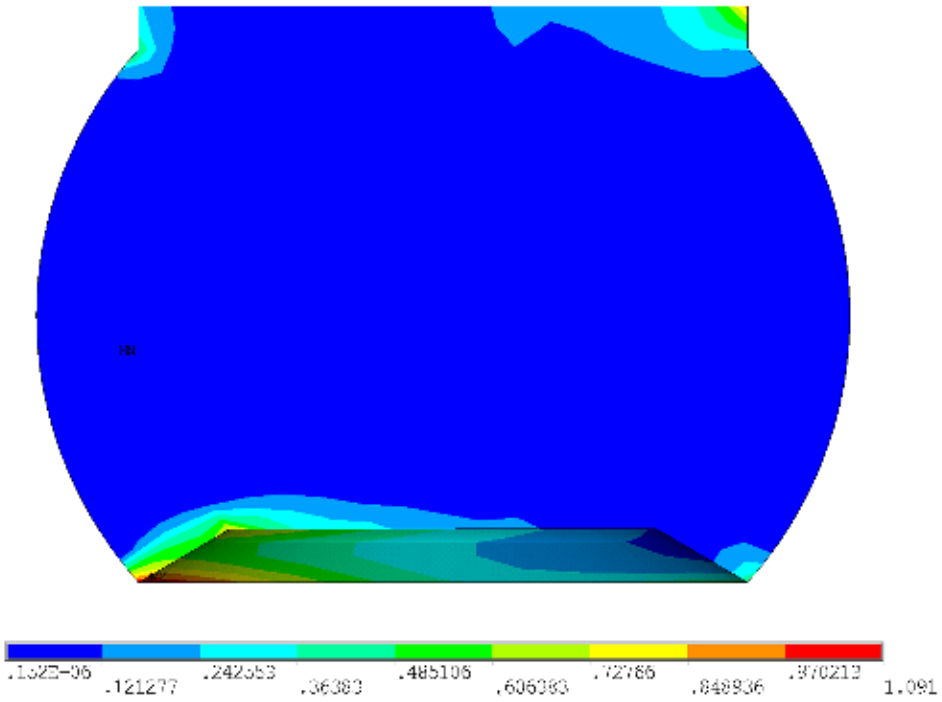

Figure 3-32 PBGA 313 Failed FEM

As can be seen, the simulation showed a large amount of stress at the top and bottom of the interconnect along both the package and PCB interface. The experiment showed maximum damage along the top of the interconnect at the package interface. The crack initiated and propagated along the package side interface. Some of the interconnects showed damage at the PCB interface, but the maximum damage was consistently seen at the package interface. In Figure 3-31, the crack along the top of the interface from experiment can be clearly seen. Damage along the bottom of the interconnect can also be seen, coinciding with the simulation results.

3.5.2 PBGA 313 FEM Validation

The Hysteresis plot and the plastic work plot for the package are presented below in figure 3-33 and figure 3-34.

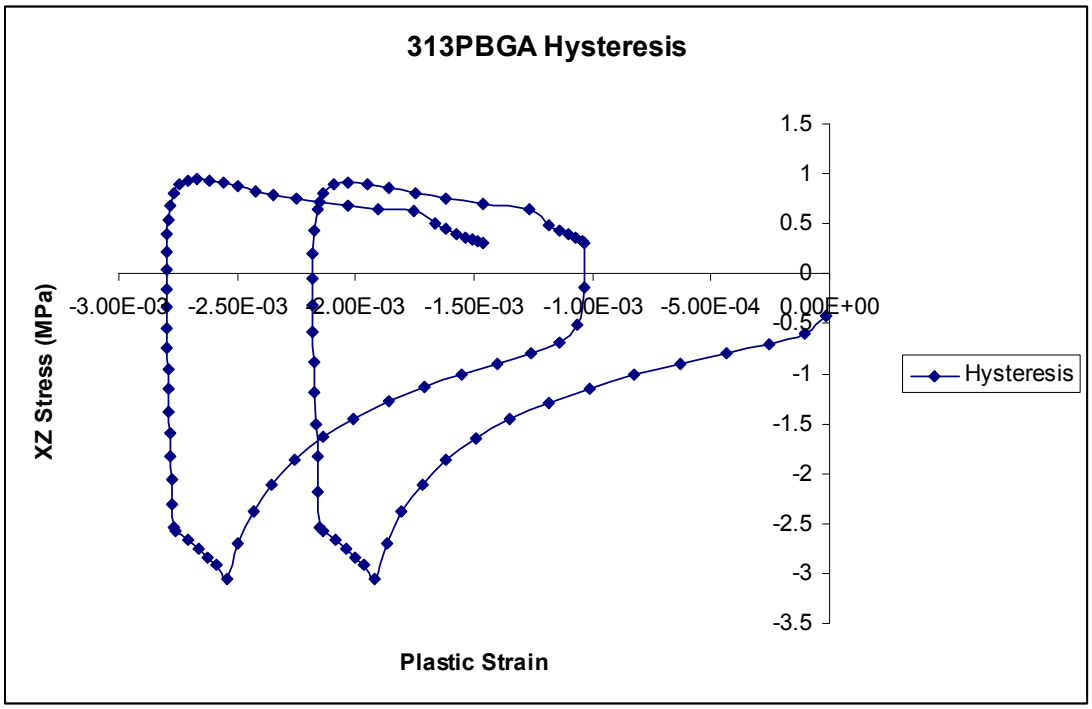

Figure 3-33 Hysteresis plot PBGA 313

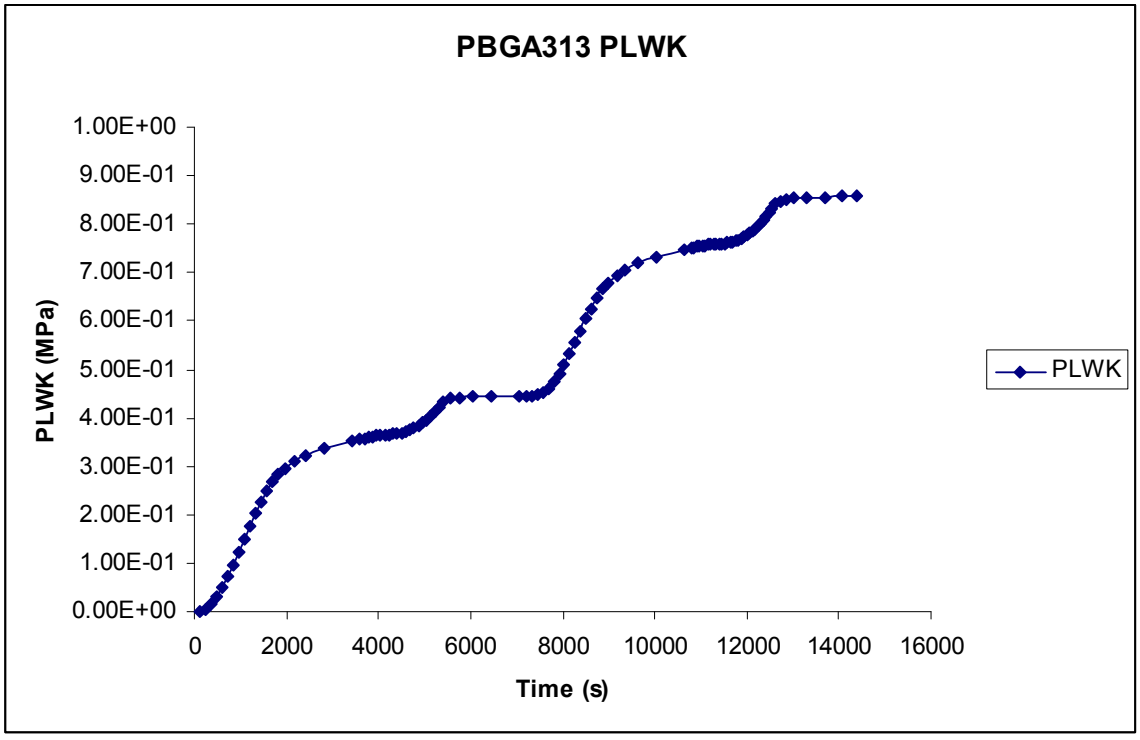

Figure 3-34 Plastic work plot PBGA 313

The hysteresis loop showed stabilization after two cycles. The plastic work of the PBGA 313 was lower than the BGA 1152 at around 8.5 MPa as opposed to 10MPa. The same life prediction as used for the BGA 1152 was used for the PBGA 313 model. The life validation can be seen in table 3-14.

Table 3-14 PBGA 313 Life Correlation

	Characteristic Life (η)	Error
Experiment	3834 cycles	13%
Simulation	3336 cycles	

The model closely tracked the experiment with only 13% error reported and a simulated characteristic life of 3,336 cycles.

3.6 PBGA 128

The PBGA 128 package is a multi chip module featuring four dies housed in a Diallyl Phthalate mold. The package features a perimeter array with 63Sn37Pb eutectic tin lead solder interconnects. A CSAM (C-mode scanning acoustic microscopy) image of the package can be seen below.

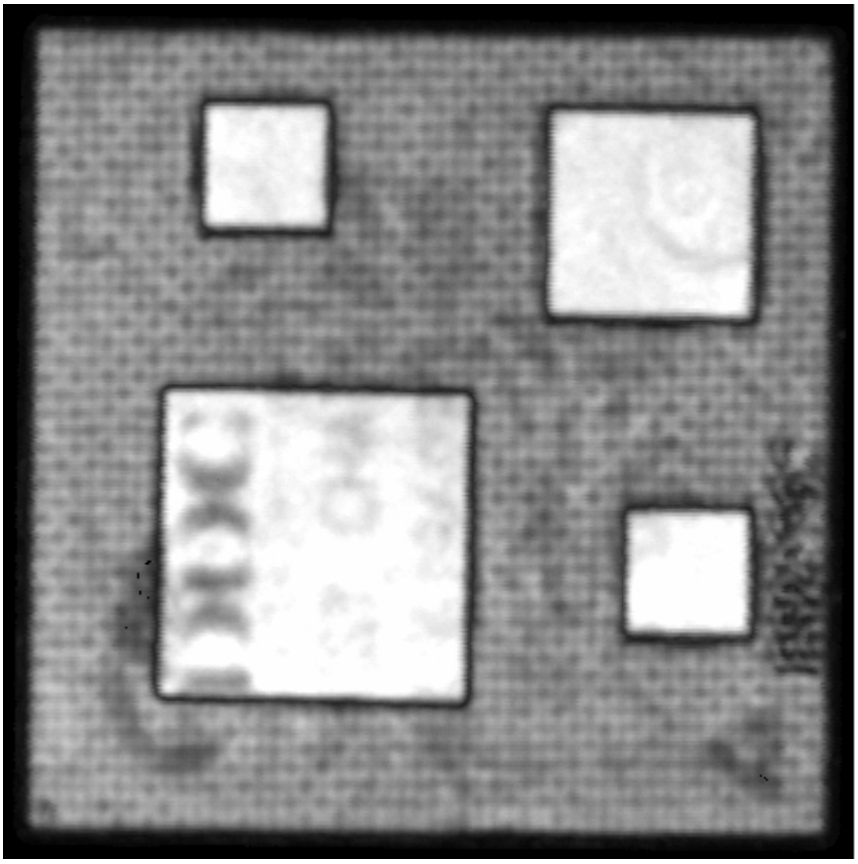

Figure 3-35 CSAM of PBGA 128 package

From the CSAM, the four die are clearly seen. CSAM is generally used to check for delamination. With CSAM, the board is submerged in a fluid and sound waves are sent to the board. The method is similar to sonar waves. In this case, it was used to make sure that the underfill had evenly distributed throughout the package. All of the die are

the same thickness but different length. The package dimensions are shown in table 3-15 below:

Table 3-15 PBGA 128 multichip dimensions

Length	20.7 mm
Width	20.7 mm
I/O	128
Pitch	1 mm
Ball Diameter	.56 mm
Ball Height	.56 mm
Substrate Thickness	.8 mm
Die Length	7.57 mm
PCB Thickness	2.11 mm

Overall, this package performed the worst of all the packages found on the test vehicle. While the ImAg finish PBGA 128 did outperform the ImAg finish BGA 1152 package, it was not by a substantial amount and the HASL finish PBGA 128 greatly underperformed any other HASL finish packages that were tested. The Weibull plot of the non underfilled PBGA 128 can be seen below in figure 3-36.

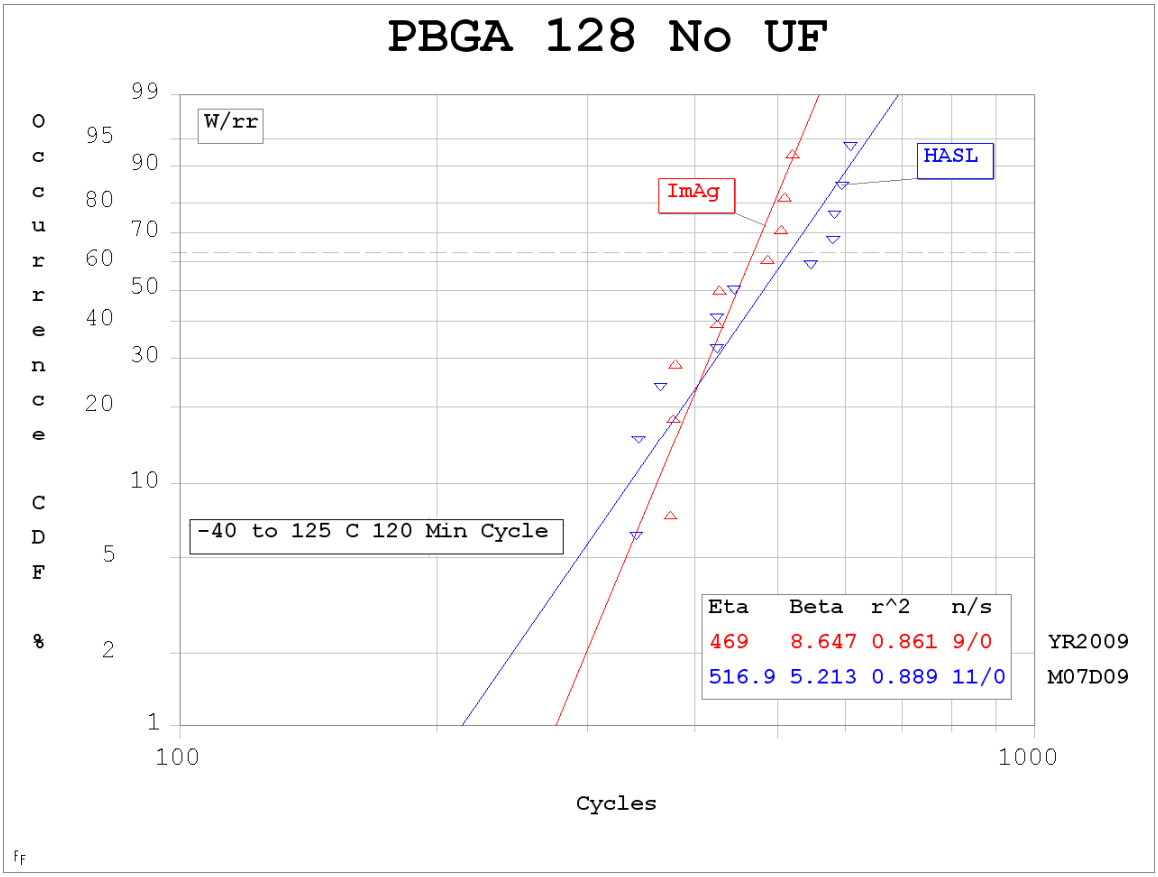

Figure 3-36 Weibull plot of PBGA 128

The HASL and ImAg pad finished packages performed similarly. Similar to the other packages, an equal number of underfilled packages were tested. The underfilled results can be seen below in figure 3-37.

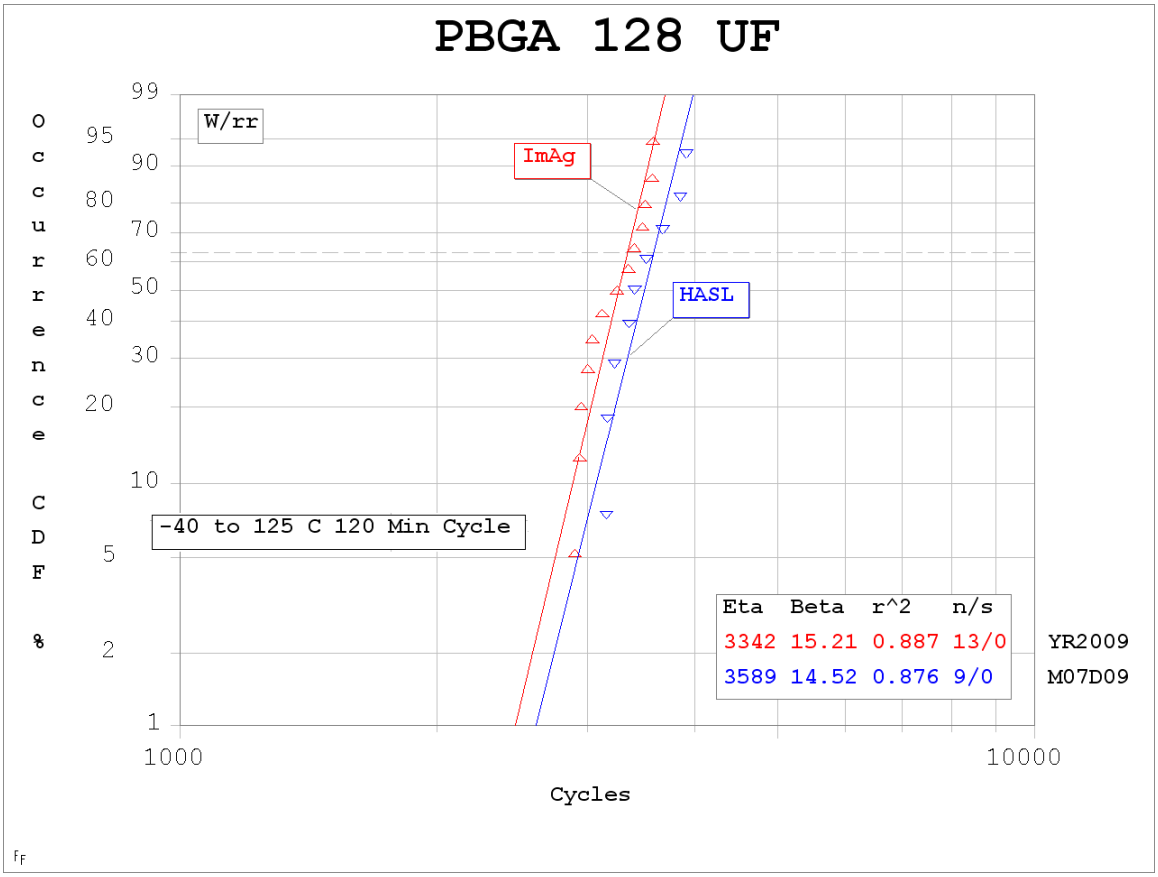

Figure 3-37 Underfilled PBGA 128

In the case of PBGA 128, the underfill offered the greatest life improvement at approximately 7X in both the HASL and ImAg cases. The underfill results on a per finish basis are presented below in figure 3-38 and figure 3-39.

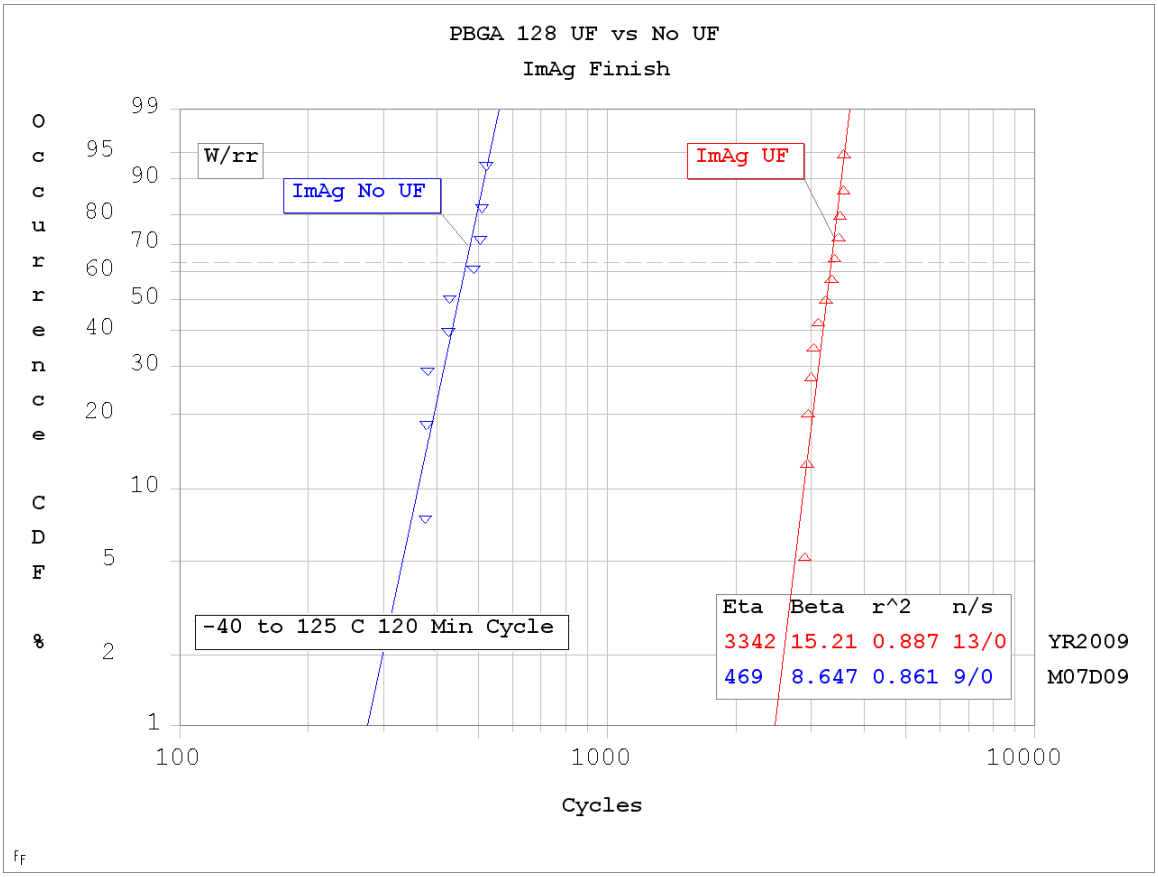

Figure 3-38 PBGA 128 ImAg finish underfill and non underfill

In the case of the ImAg finish package, the underfill offered a 7X life improvement. The characteristic life without underfill is 469 cycles where as with underfill the characteristic life is bumped up to 3,342 cycles. This is the most improved of any of the packages tested except for the PBGA 128 HASL finished boards. The underfill had the greatest impact on the PBGA 128 package. This supports previous results where a low CTE underfill has a great impact on the life of smaller PBGA's [Elkaday 2004, Suhling 2002].

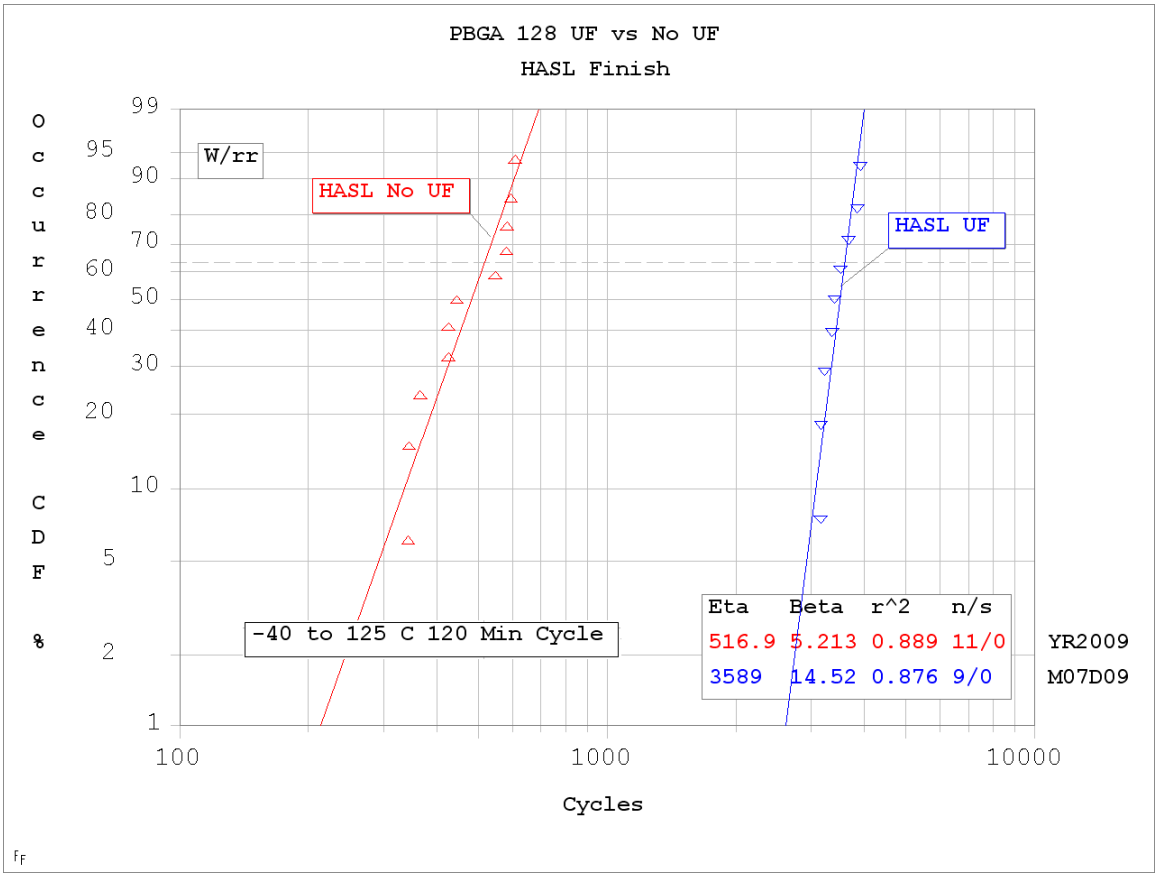

Figure 3-39 PBGA 128 HASL finish underfill and non underfill

Again, with the HASL finish the underfill offered a 7X life improvement. In the case of the PBGA 128 multichip, the underfill is a wise investment for reliability. The characteristic life for the HASL finish boards without underfill is 517 cycles where as with underfill it is bumped up to 3,589 cycles. Table 3-16 below shows a comparison of the different PBGA 128 packages.

Table 3-16 PBGA 128 Life Comparisons

Pad Finish	UF	(η) Characteristic Life
ImAg	No	469 cycles
ImAg	Yes	3,342 cycles
HASL	No	517 cycles
HASL	Yes	3,589 cycles

3.6.1 PBGA 128 FEM

For modeling purposes, the largest chip was modeled in a diagonal symmetry slice despite the fact that the package did not offer diagonal symmetry. It was assumed that the largest die would create the greatest stress per the studies published by [Zhang 2001], where the largest die in the package has the greatest effect on package warpage. The smaller dies are shown to have little impact. The FEM results closely tracked those of the actual thermal cycling. An image of the FEM can be seen below in figure 3-40.

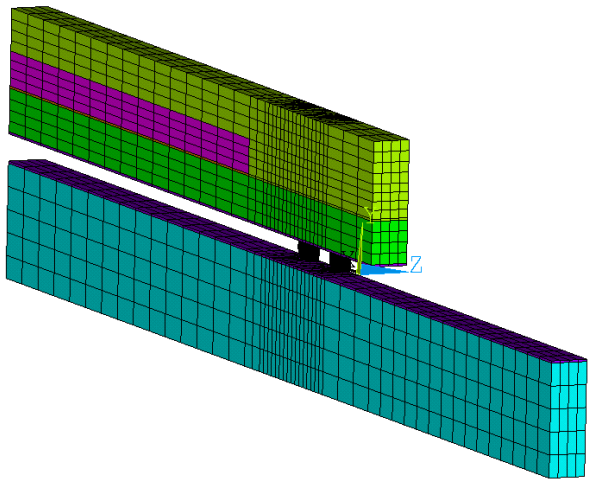

Figure 3-40 Diagonal view PBGA 128 FEM

The material properties for the PBGA 128 finite element model are presented in table 3-17 below.

Table 3-17 PBGA 128 material properties

Component	E GPa	α ppm/°C	υ
PCB	17(x,z) 7(y)	15(x,z) 67 (y)	.39
Solder Ball	30	24	.35
BT Substrate	18(x,z)7(y)	12(x,z)57(y)	.3
Solder Mask	3	30	.3
Die Adhesive	7	52	.35
Silicon Die	162	2.5	.28
Mold	23	15	.3
Copper Pad	128	16	.34

The package used the same material properties as the PBGA 313 package. The same Anand constants as presented earlier for 63Sn37Pb solder alloy were used in the PBGA 128 model. A close up image of the die shadow region can be seen below in figure 3-41, and figure 3-42 shows the failure results of the simulation where maximum damage occurs in the top right corner of the solder ball furthest away from the die near the edge of the package. Both solder balls showed similar damage and either the one on the outside, or the solder ball nearest the die could be taken as the one to fail first as both experienced similar plastic work values.

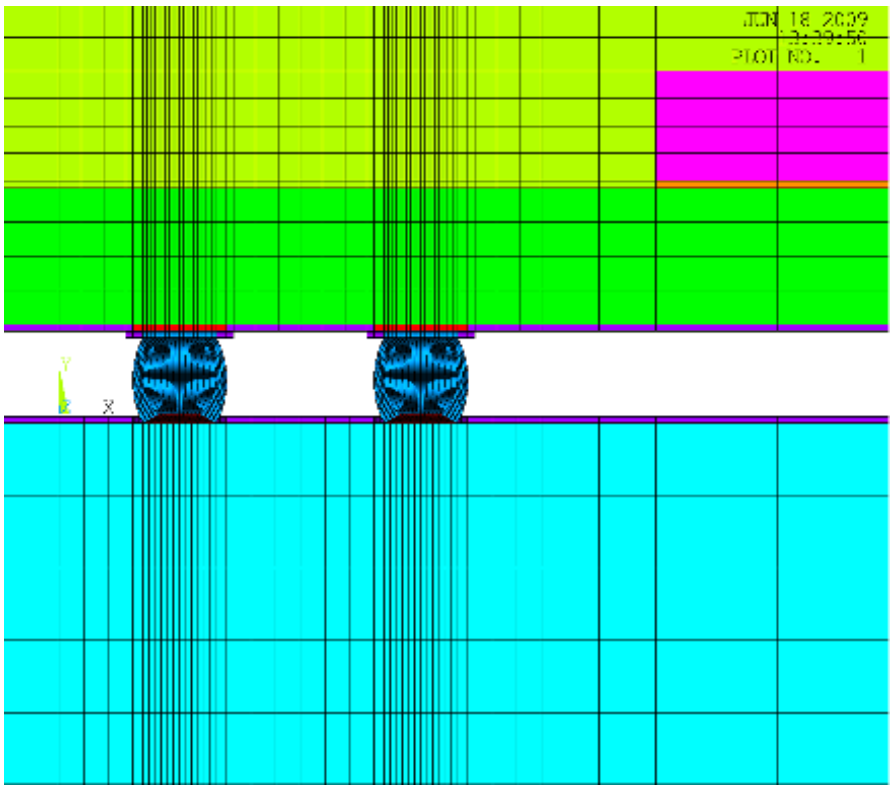

Figure 3-41 PBGA 128 FEM

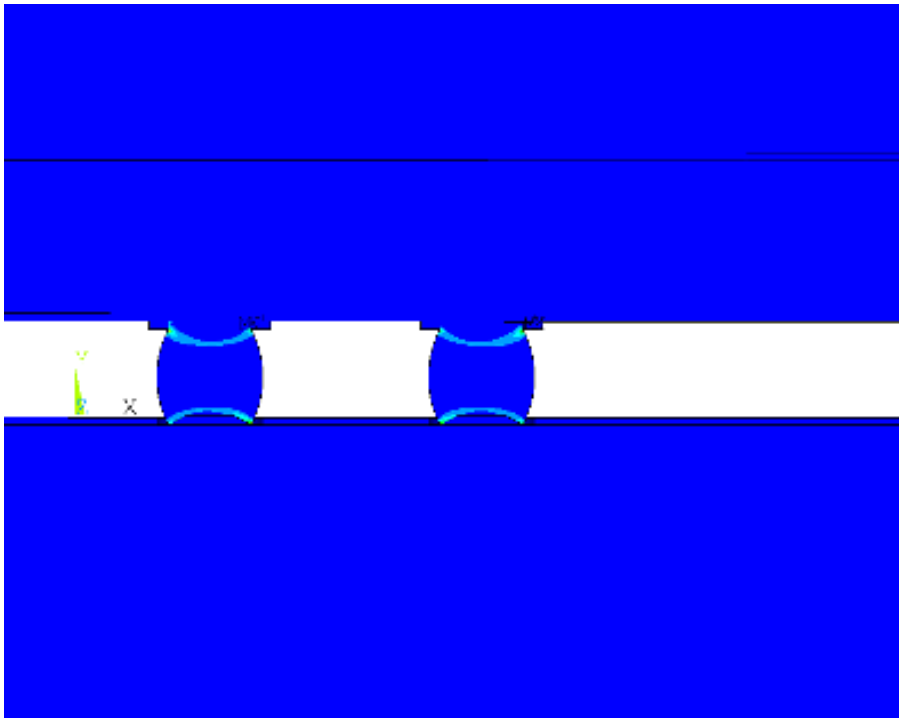

Figure 3-42 PBGA 128 Failure

As can be seen in figure 3-42, both solder balls incurred nearly the same amount of damage in the FEM simulation. The ball furthest from the die is identified as having the most plastic work, but both solder balls incur nearly the same amount of damage. An image of the actual failed solder ball with the failed simulation is shown below.

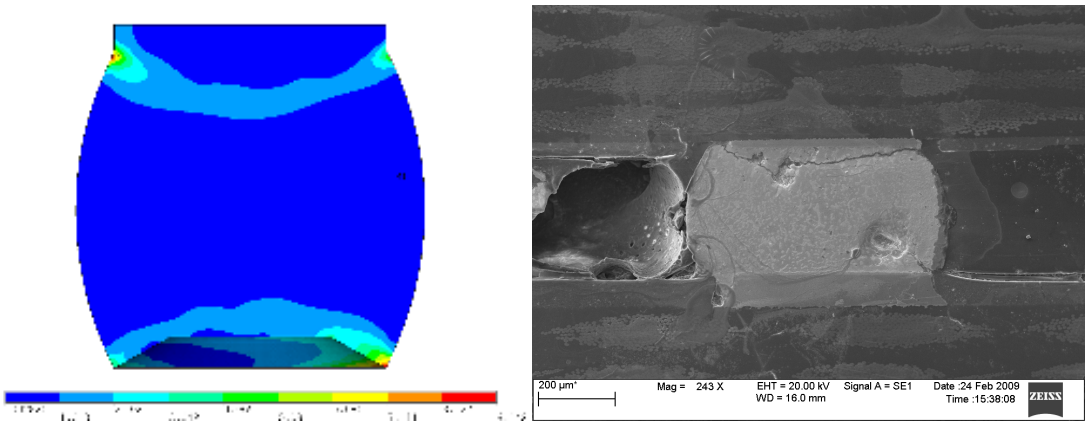

Figure 3-43 Simulation Failure and experimental failure PBGA 128

The crack initiates at the top of the solder ball and propagates along the package interface. The simulation and experimental results closely mirror one another. Similarly to the BGA 1152 package, the PBGA 128 underfilled package was recreated in ANSYS. Figure 3-44 below shows an image of the underfilled finite element model.

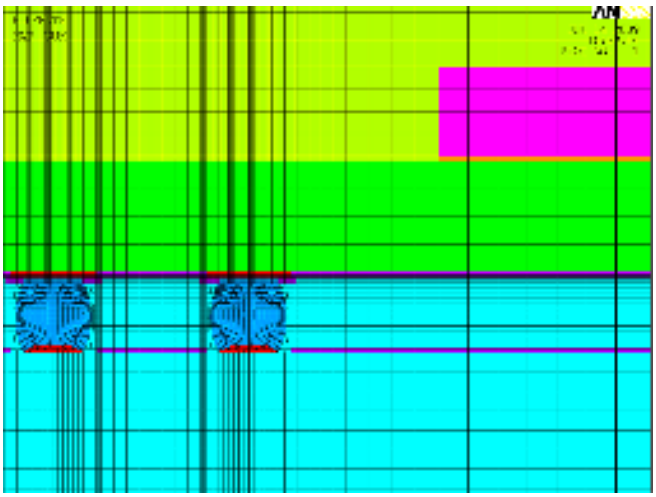

Figure 3-44 Underfilled PBGA 128 Package

Figure 3-45 below shows the solder balls encapsulated by the underfill.

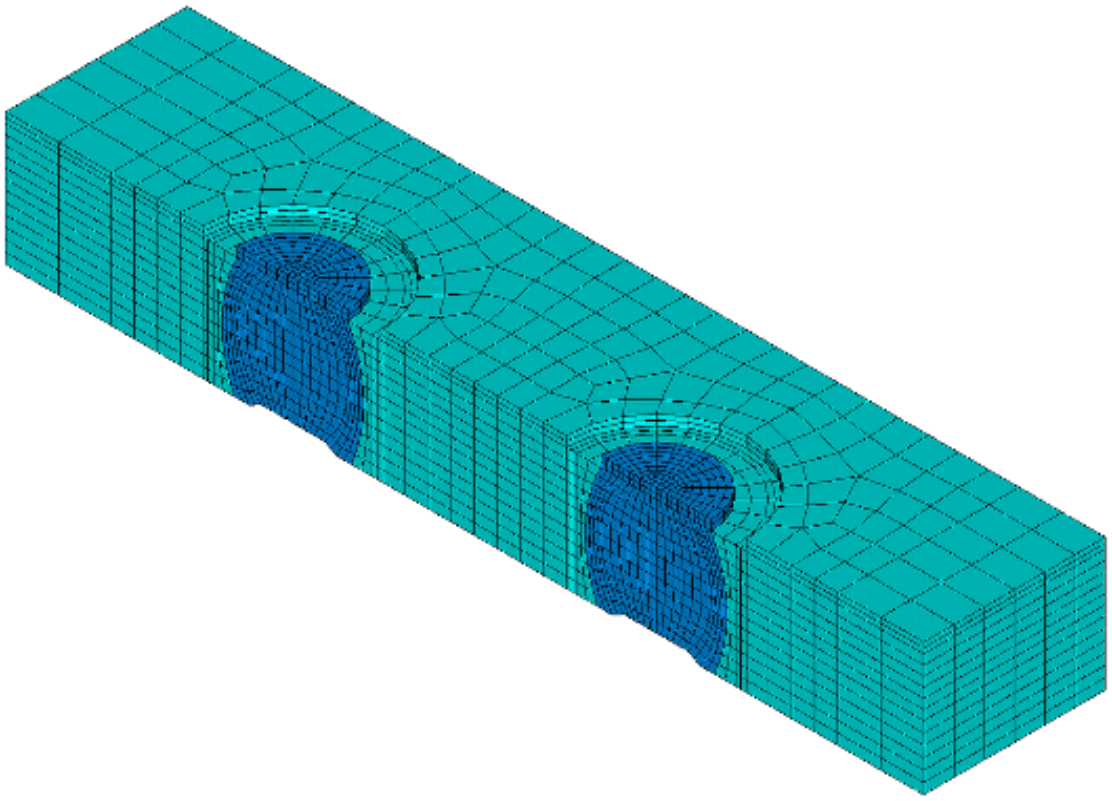

Figure 3-45 encapsulated PBGA 128 solder balls

The same underfill presented for the BGA 1152 was used in the PBGA 128 package. As mentioned previously, the effect of underfill on PBGA's is still not that well known. Generally, it increases the lives of smaller PBGA's [Lili 2002, Elkaday 2004], but the underfill effect is largely dependent on the underfill material properties [Qi 2005,Burnette 2001]. The hysteresis plot comparisons of the underfilled and non underfilled PBGA 128 packages as well as the plastic work comparisons of the underfilled and non underfilled PBGA 128 packages are presented in figure 3-46 and figure 3-47 below.

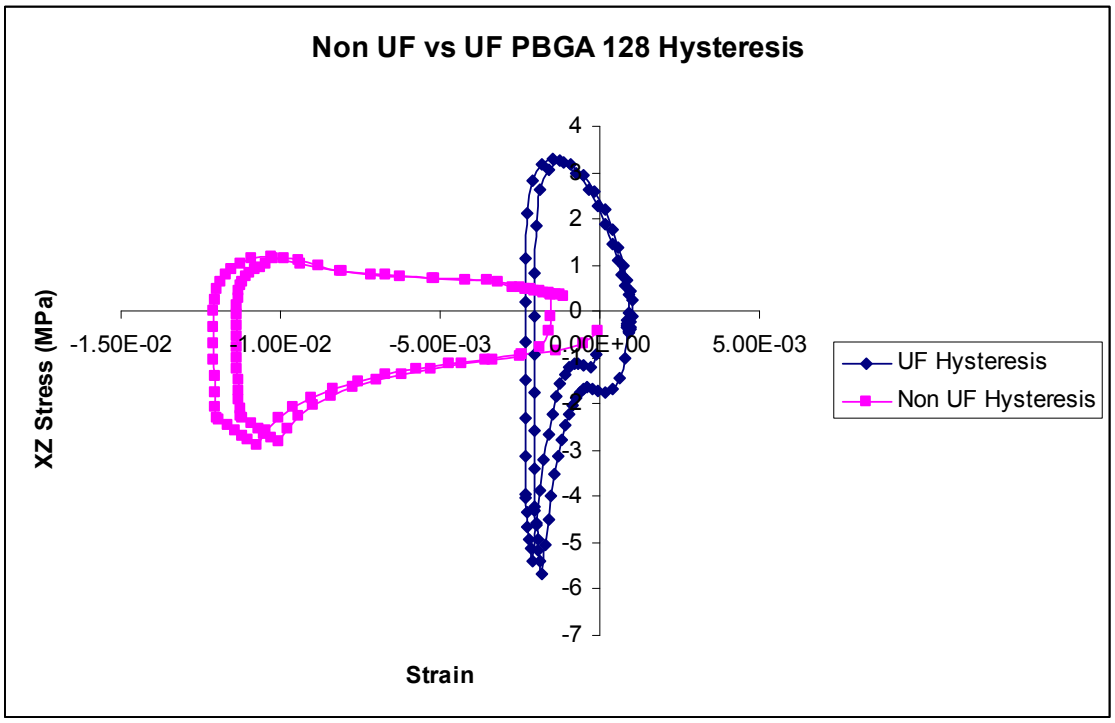

Figure 3-46 PBGA 128 UF vs No UF Hysteresis

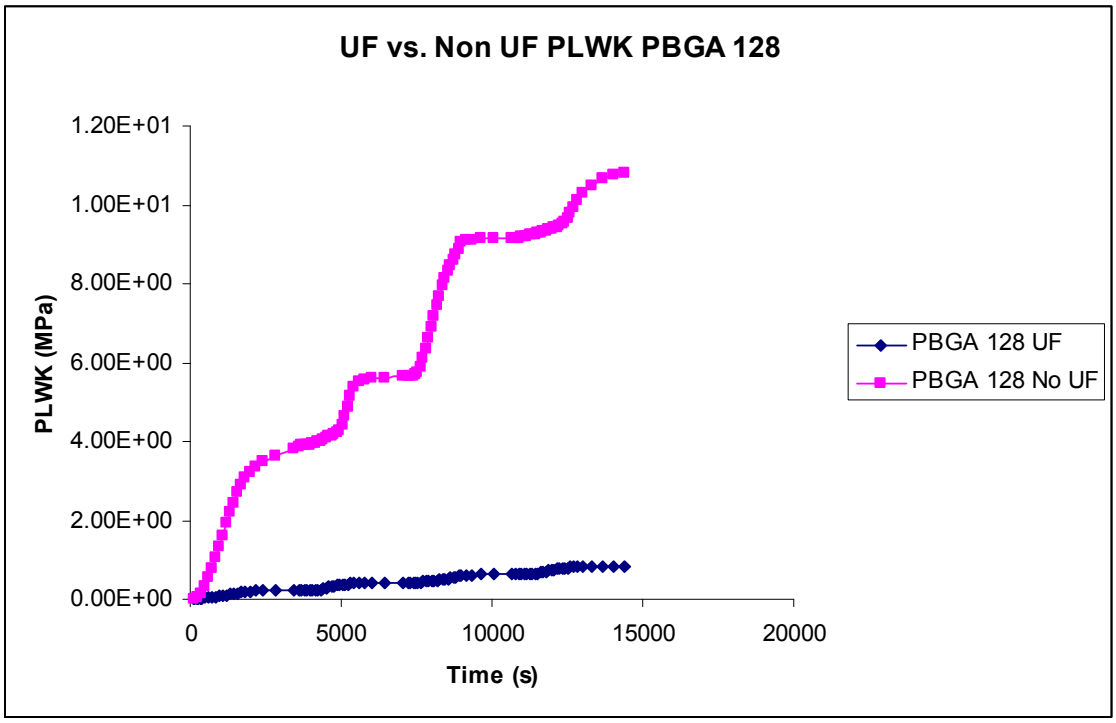

Figure 3-47 PBGA 128 UF vs No UF Plastic Work

Similarly to the BGA 1152 model, the plastic work offered a reduction in hysteresis size and in plastic work. In figure 3-47 the plastic work without underfill is nearly 11MPa while the plastic work with underfill has not even reached 1MPa. This means that the non underfilled package accrues damage at a rate of eleven times that of the underfilled package. As mentioned earlier, the underfill had a greater impact on the PBGA 128 package when compared to the BGA 1152 package offering a 7X life improvement. It can be concluded that the underfill had a greater impact on life in the smaller PBGA packages.

3.6.2 PBGA 128 Life Correlation

The life of the package was predicted in a method identical to those used for the BGA 1152 and PBGA 313 packages. Though either solder ball could have been used for life prediction, the one furthest from the die was chosen as it had slightly more damage than the solder ball closest to the die. The life correlation is given below in Table 3-18.

Table 3-18 Life Correlation PBGA 128

	Characteristic Life (η)	Error
Experiment	469 cycles	9%
Simulation	427 cycles	

As is seen in Table 3-18, the simulation gives excellent life correlation with the actual experiment at only 9% reported error.

3.7 PBGA 256

The PBGA 256 is a perimeter array PBGA. It features a very small die with large solder balls and a large pitch. With large solder balls, a small die, and a large pitch the stress generated in the package is expected to be minimal. A CSAM image of the package can be seen below in figure 3-48

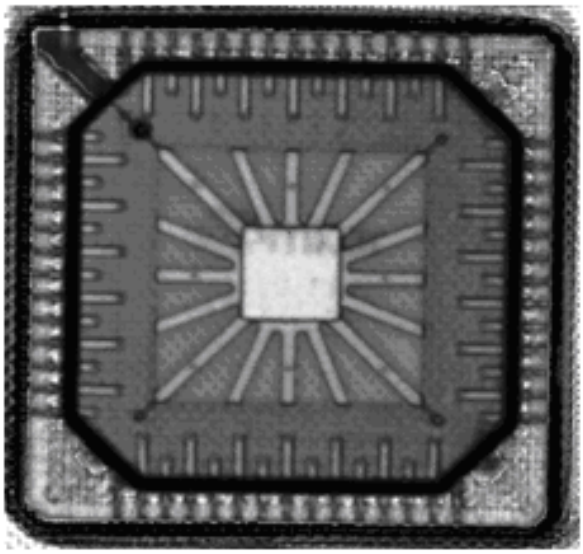

Figure 3-48 PBGA 256 CSAM

In figure 3-48, the smaller die can clearly be seen in the center of the package. Table 3-19 below gives the package dimensions.

Table 3-19 PBGA 256 Dimensions

Length	27 mm
Width	27 mm
I/O	256
Pitch	1.27 mm
Ball Diameter	.75 mm
Ball Height	.7 mm
Substrate Thickness	.4 mm
Die Length	2.6 mm
PCB Thickness	2.11 mm

An image of a pristine solder ball can be seen below in figure 3-49

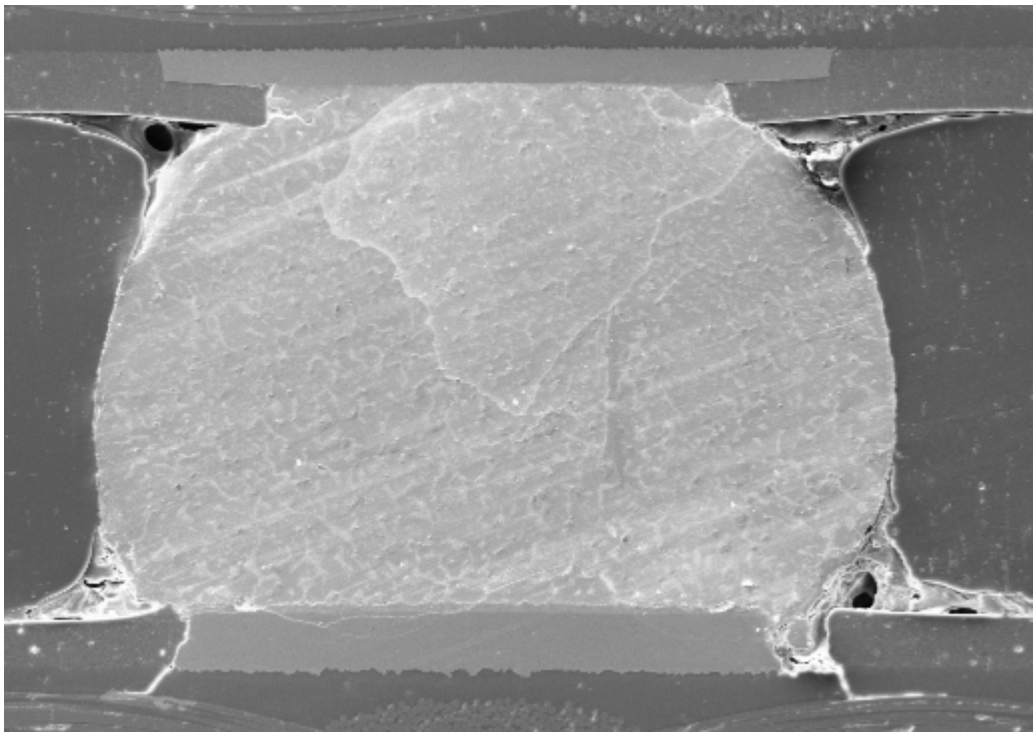

Figure 3-49 Undamaged PBGA 256

This package has performed extremely well with only one reported failure as of 6,500 cycles. None of the underfilled packages have failed and should go on for a considerable amount of time judging by the way the non underfilled packages have held up. The solder ball nearest the chip was the first to fail. Below in figure 3-50 the fourth ball to the right is the one that failed first. In figure 3-51 below, the crack is seen to propagate across the top at the package interface.

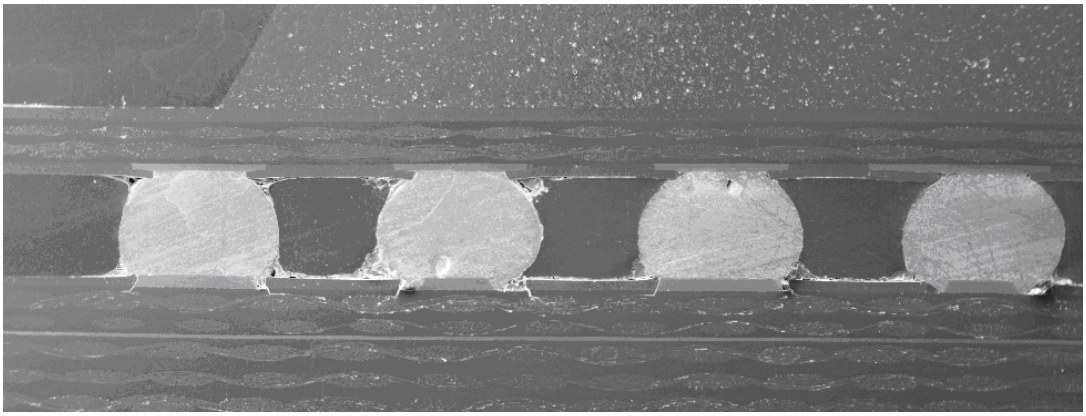

Figure 3-50 PBGA 256 Cross Section

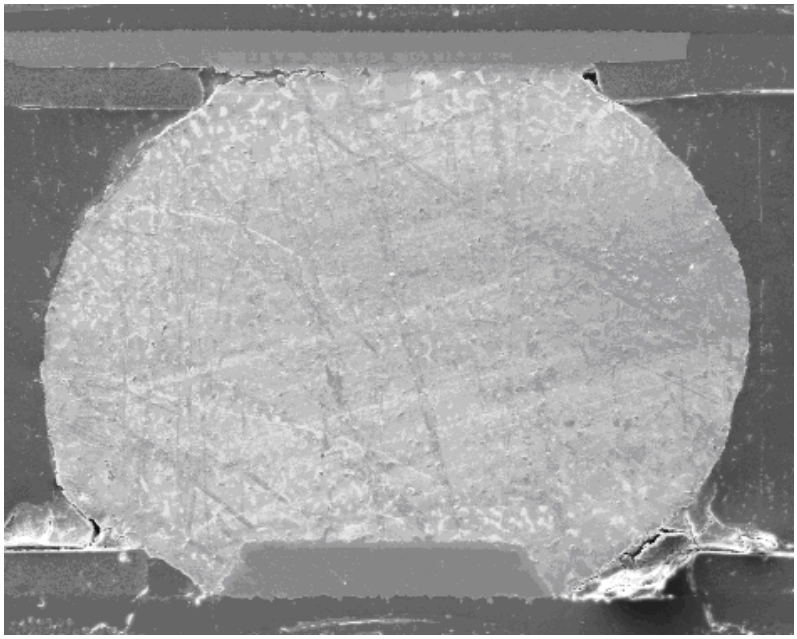

Figure 3-51 Cracked Right Most Solder Ball

As can be seen in figure 3-50 very little damage has occurred in this package. Two of the four solder balls shown in figure 3-50 seem to be completely undamaged and the crack shown in 3-51 is small though it has caused loss of signal in the I/O. A Weibull plot for this package can not be generated as there has been only one reported failure to date.

3.7.1 PBGA 256 FEM

The package was recreated in ANSYS. The same material properties as presented in table 3-11 were used for this package. The solder alloys are 63Sn37Pb eutectic so the Anand constants presented in table 3-9 were used for the simulation. A diagonal view of the finite element model can be seen below in figure 3-52

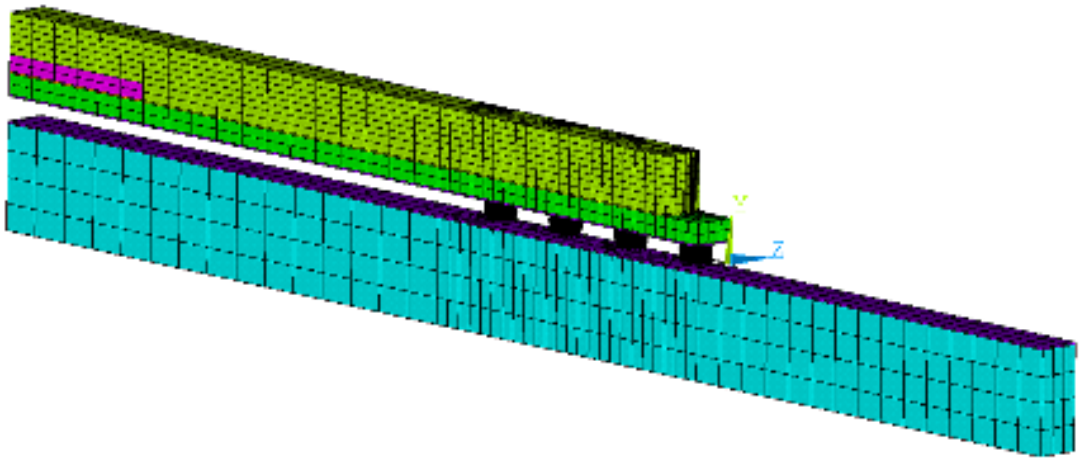

Figure 3-52 Diagonal View PBGA 256

As the finite element model shows, the die takes up a very small amount of the package. A close up image of the modeled solder interconnect can be seen below in figure 3-53.

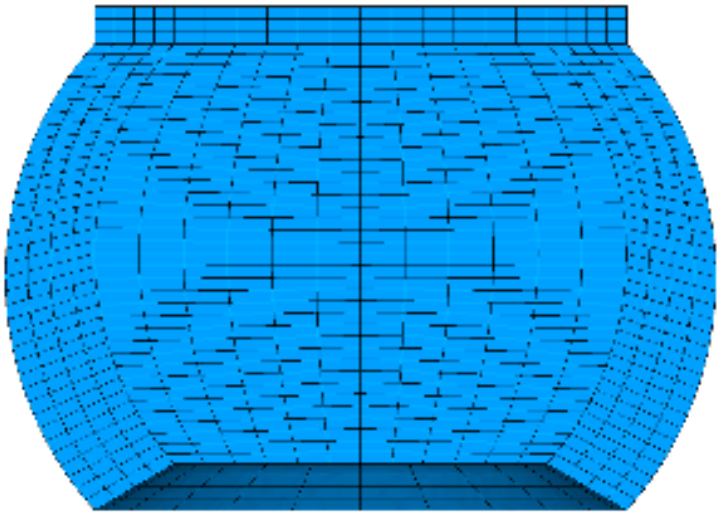

Figure 3-53 FEM PBGA 256 Solder Ball

The failed solder ball is shown below in figure 3-54

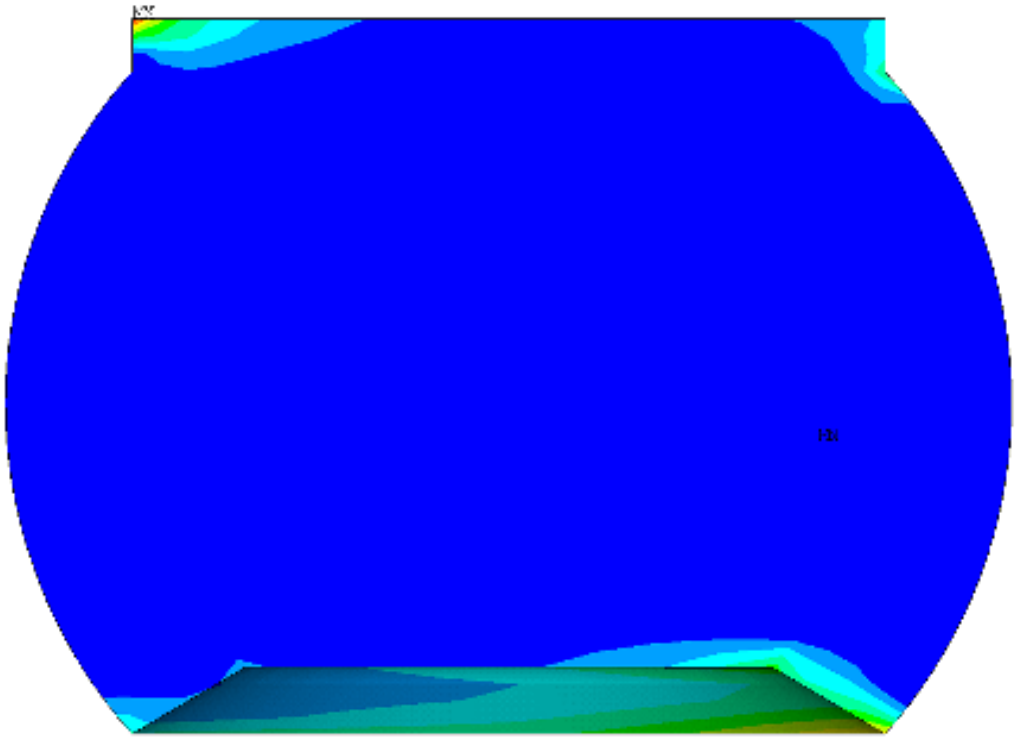

Figure 3-54 Failed PBGA 256 FEM solder ball

Images of the finite element model showing failure in the fourth solder ball are shown below in figure 3-55 along with SEM images showing the same failure mode in figure 3-56.

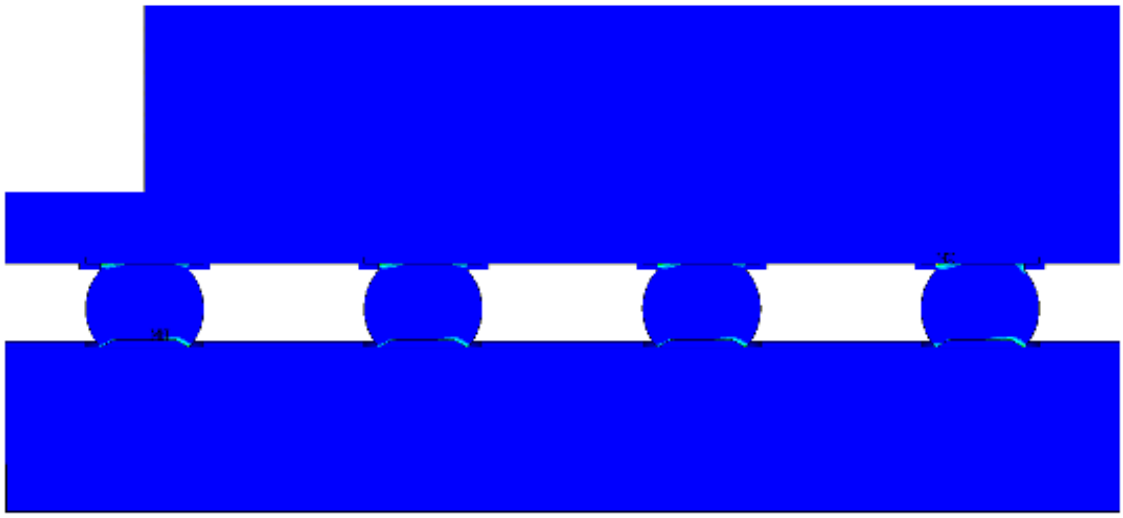

Figure 3-55 PBGA 256 FEM failed solder balls

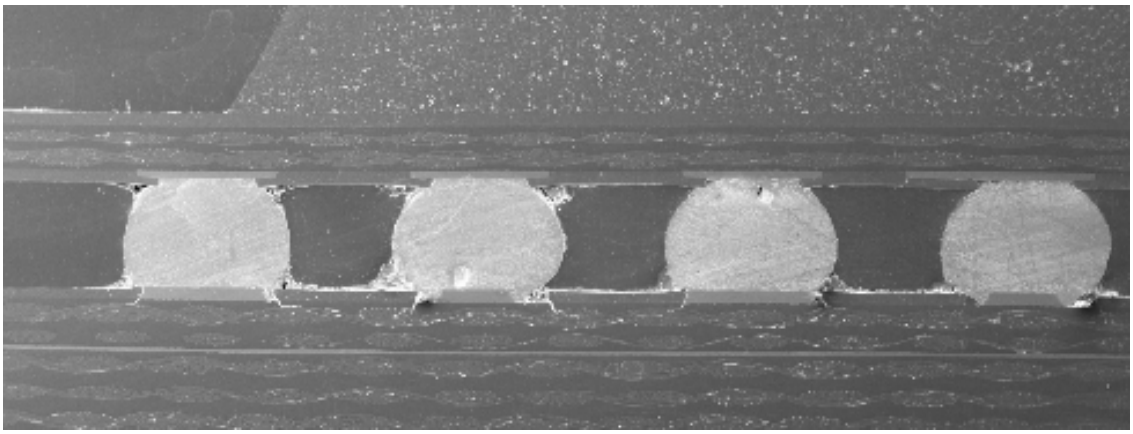

Figure 3-56 SEM PBGA 256 Failed Perimeter Ball

3.7.2 PBGA 256 Model Validation

Though a Weibull plot can not be generated and the experimental life of the package is still unknown, an estimation was made using the plastic work from the simulation. The life equation model proposed by [Lall 2004] and used on previous packages was used here. Figure 3-57 and Figure 3-58 below show the hysteresis loop and plastic work of the package.

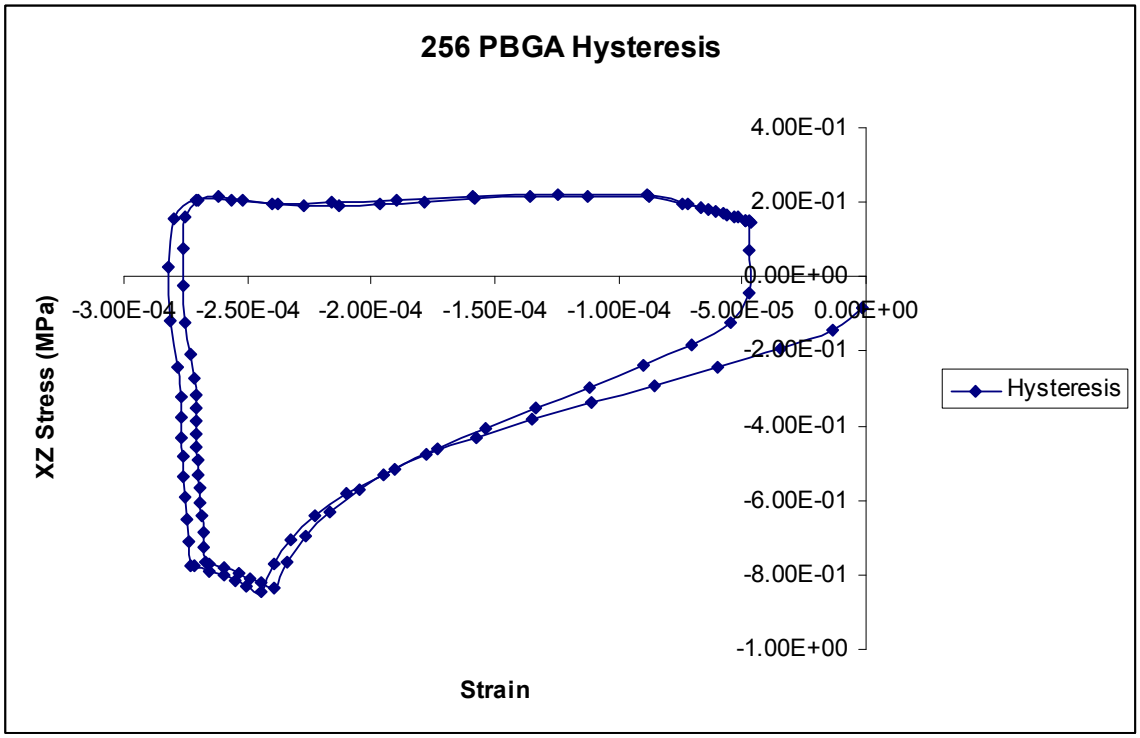

Figure 3-57 PBGA 256 Hysteresis Plot

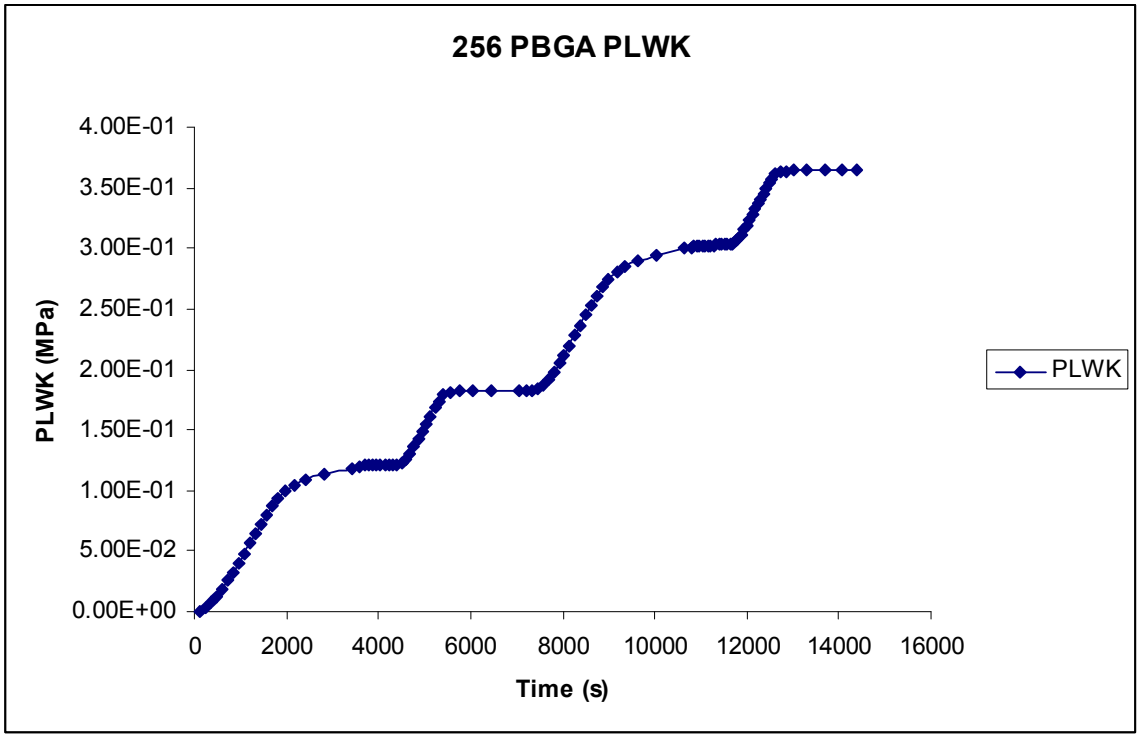

Figure 3-58 PBGA 256 Plastic Work

Figure 3-58 shows a smaller plastic work value than the other packages at .4 MPa. A more detailed comparison of all the plastic work values for the packages will be shown later. The life validation of the package is given below in table 3-20.

Table 3-20 PBGA 256 Life Correlation

PBGA 256	Characteristic Life (η)	Error
Experiment	NA	NA
Simulation	9,199 cycles	

Table 3-20 shows a simulated life of 9,199 cycles. This number can not yet be validated as there have not been enough PBGA 256 failures. However, with the rate at which the package has been failing, a high cycle count seems to be a good estimate of the package life.

3.8 Package comparisons

The characteristic lives of all the package is shown below in figure 3-59. In figure 3-59, the PBGA 313 is more reliable than the BGA 1152 and PBGA 128. The results of the Weibull plot are incomplete as the PBGA 256 package can not be plotted because the package has not had enough failures to generate a Weibull chart. However, the package has so far shown to be superior to the other three packages reported.

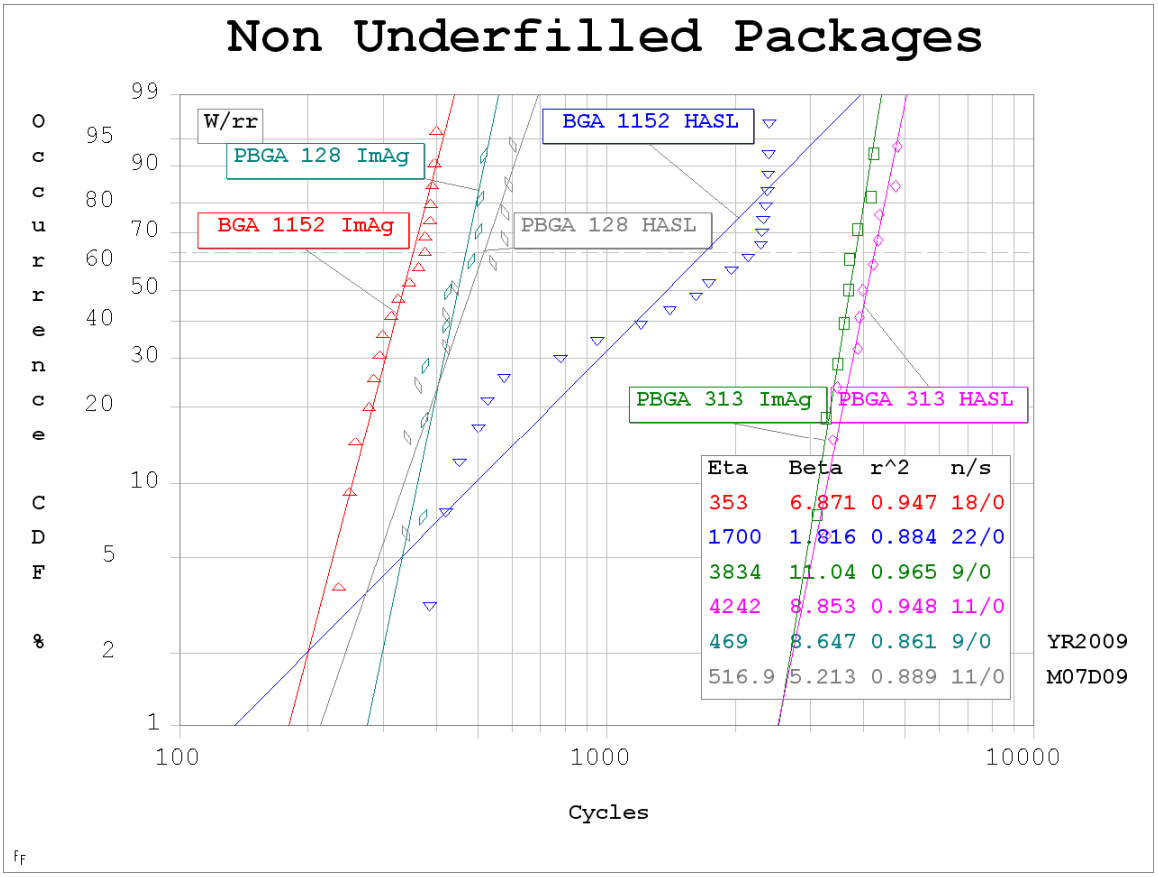

Figure 3-59 Weibull comparison of boards

The results support published results from literature mentioned previously in this chapter. Namely, the smaller die, perimeter array package has shown superior reliability when compared to the other packages [Syed 1996]. Also, the HASL surface finish consistently outperformed the ImAg surface finish, though the life improvement was not

always that drastic [Bradely 1996]. In fact, in all the packages except for the BGA 1152 flip chip, the difference was within a few hundred cycles. A bar graph shown below demonstrates the difference in pad finish.

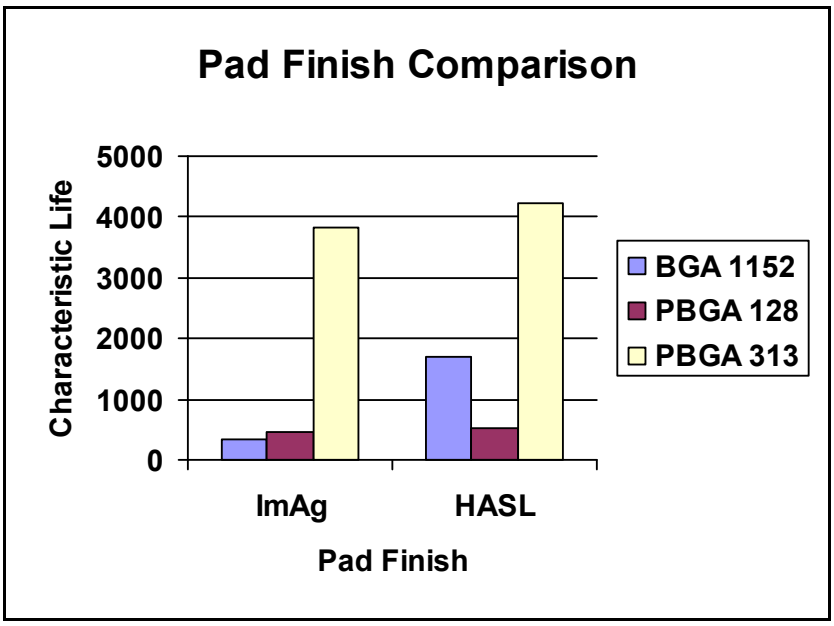

Figure 3-60 Comparison of surface finish for all packages

As can be seen, the only package with noticeable difference is the BGA 1152 package. The larger BGA 1152 package seemed more sensitive to pad finish compared to the smaller PBGA's. The number of I/O per package gave mixed results as the higher I/O BGA 1152 underperformed both the PBGA 313 packages but outperformed the smaller I/O PBGA 128 package, giving mixed results as to the impact of I/O count on package life. A bar graph demonstrating the life of all the packages tested is shown below in figure 3-61.

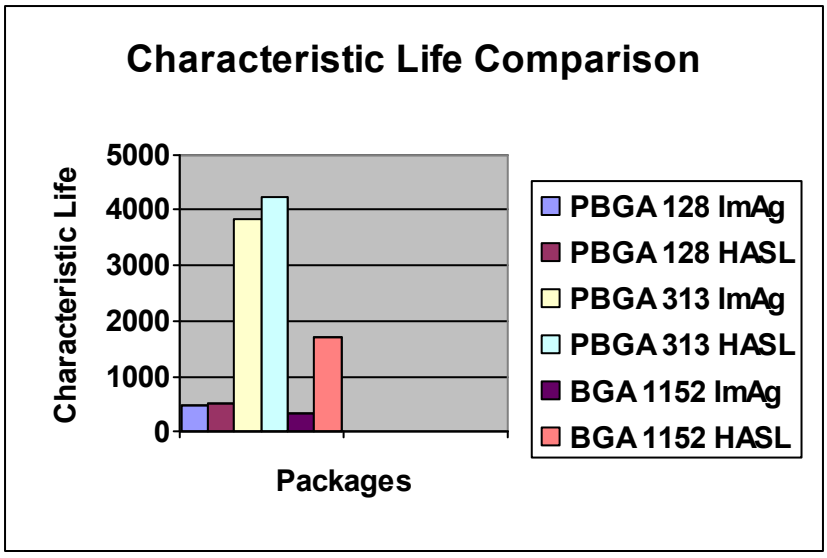

Figure 3-61 Package characteristic life comparison

Similar results were shown for the underfilled packages as can be seen below in figure 3-62. The underfilled PBGA 128 package outperformed the underfilled BGA 1152 package. The PBGA 128 package saw the greatest improvement in life when underfilled. The PBGA 313 package is not shown in figure 3-62 as it has not had any failures as of 3,400 cycles. The same can be said for the PBGA 256 package which has not shown any failures as of 3,400 cycles. Both packages will outlast the BGA 1152 and PBGA 128. The underfill improved the life of all the packages. The underfill had the greatest impact on the smaller packages. The larger BGA 1152 package did see an increase in fatigue life, but not to the extent that the smaller PBGA 313, PBGA 256, and PBGA 128 packages saw an increase in life. The underfill improved the life of both perimeter array and full array PBGA's. It can be concluded that the underfill had the greatest impact on the smaller PBGA packages and had less of an impact on the larger fine pitch flip chip BGA 1152 package. Figure 3-62 compares the underfilled BGA 1152 and PBGA 128.

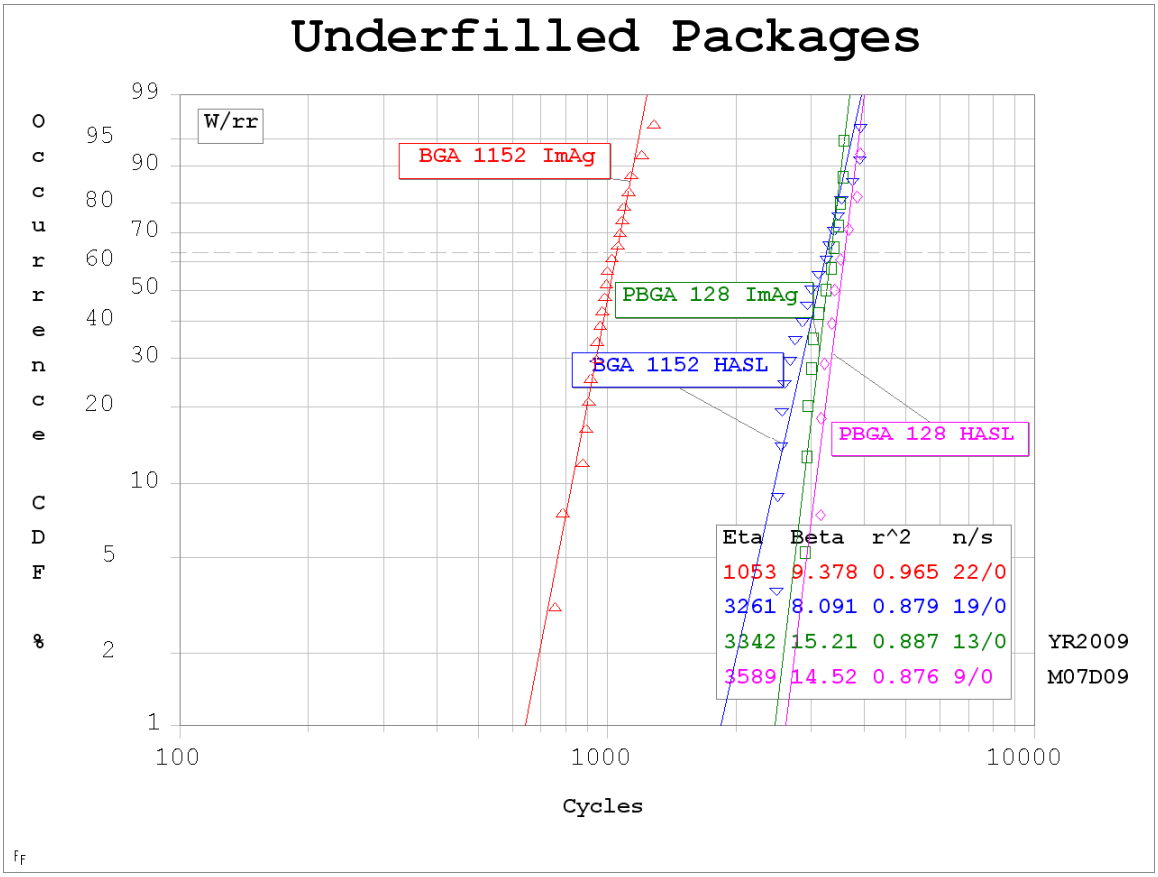

Figure 3-62 Comparison of underfilled packages

The plastic work and hysteresis loop of all the simulated packages were plotted against one another and can be seen below in figure 3-63 and figure 3-64.

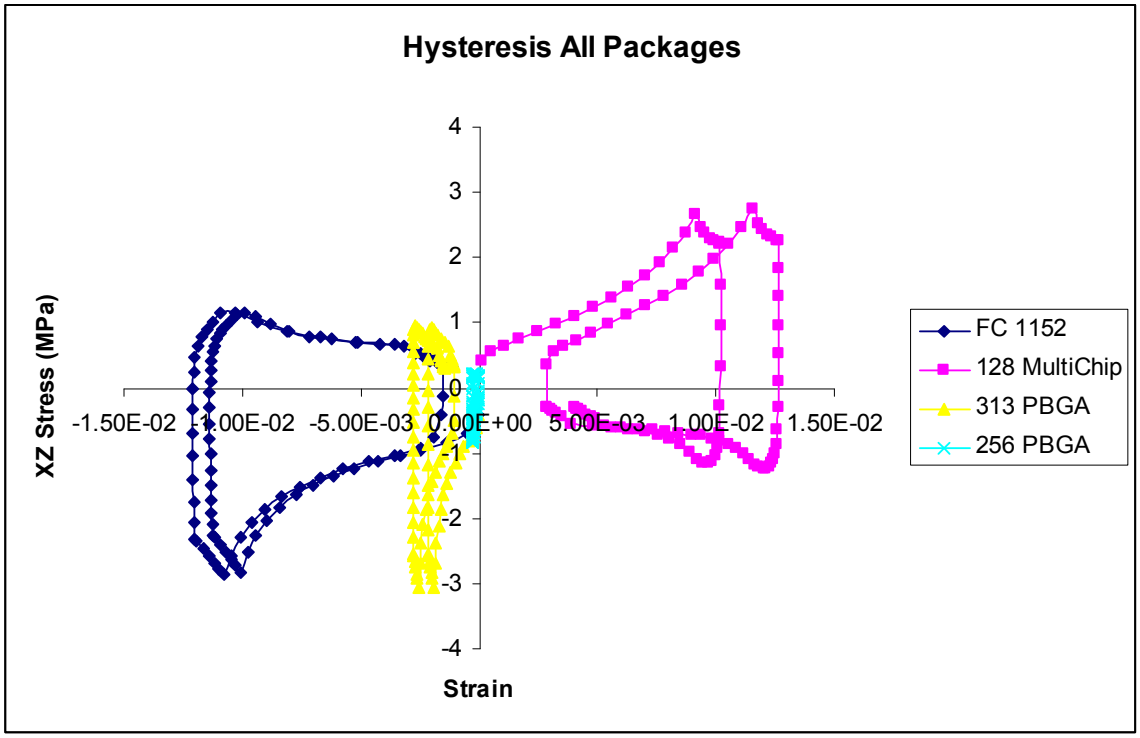

Figure 3-63 Non UF Hysteresis Plot

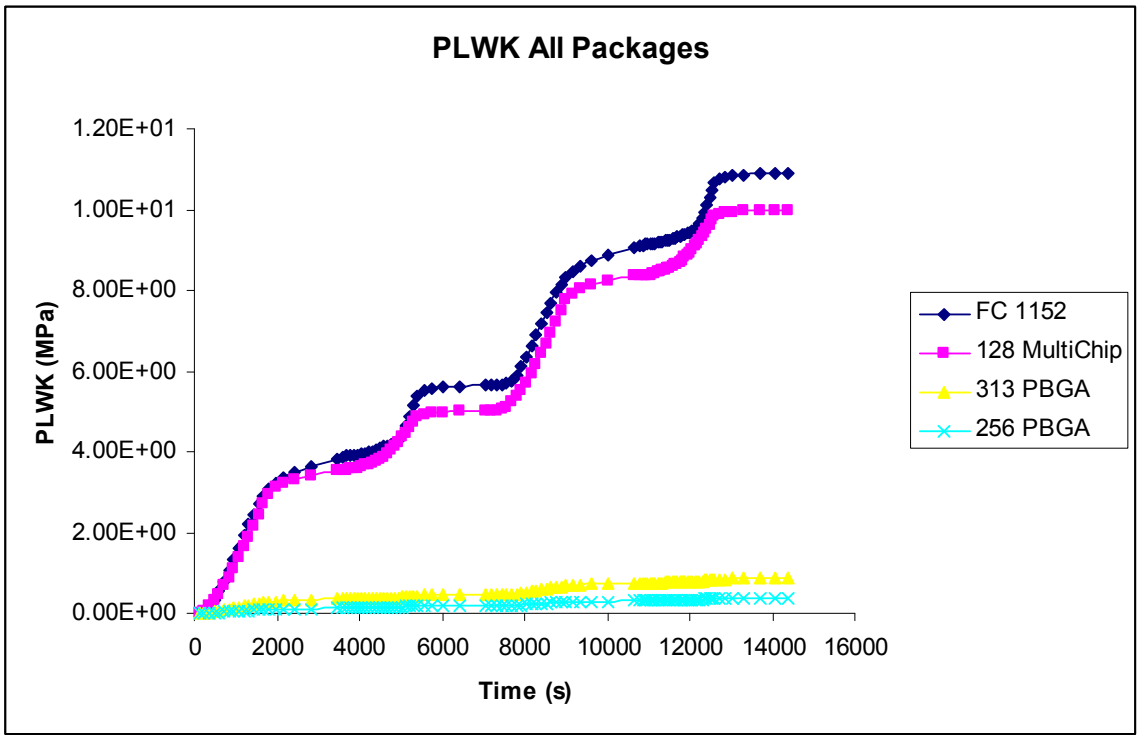

Figure 3-64 Non UF Plastic Work Plot

As figure 3-63 shows, the PBGA 256 package has a very small hysteresis loop when compared to the other three packages. The hysteresis loop of the PBGA 256 appears as a line when compared to the other three loops plotted. In figure 3-64, the plastic work of the BGA 1152 and PBGA 128 are much larger than the PBGA 313 and PBGA 256 packages as is supported by the harsh thermal environment reliability testing. Figure 3-65 below shows the difference in plastic work of the PBGA 313 and PBGA 256 packages.

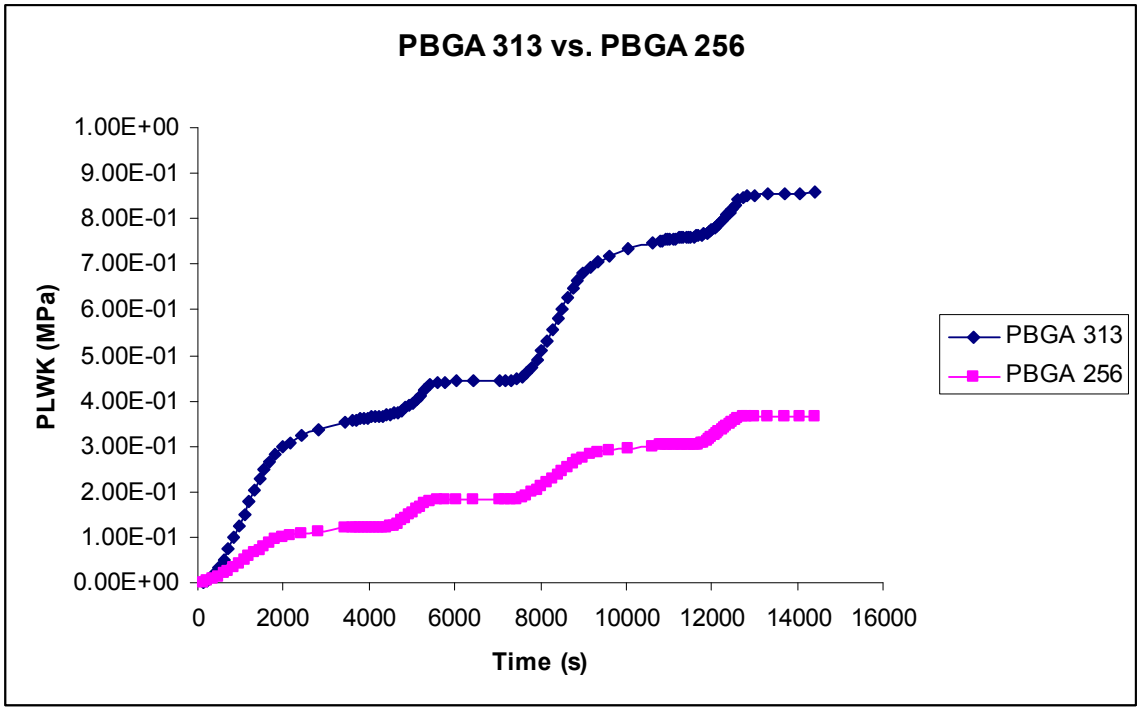

Figure 3-65 PBGA 313 vs PBGA 256 Plastic Work

While figure 3-65 shows that the PBGA 313 and PBGA 256 are closer to one another than to the BGA 1152 and PBGA 128 in terms of damage, the PBGA 313 still accrues more damage than the PBGA 256 package.

CHAPTER 4

LEAD FREE ELECTRONICS

4.1 Introduction

In this chapter, the thermo-mechanical reliability of lead free solder alloys are examined in a harsh thermal environment. The packages are subjected to harsh environment thermal cycling and recreated in ANSYS finite element program for simulation purposes. Interesting results regarding the thermo-mechanical reliability of high and low silver content alloys are presented as are the thermo-mechanical reliabilyt of doped lead free tin silver copper (SAC) based alloys.

Citing environmental concerns, the electronics industry has begun banning the use of lead in its electronic packages. While the transition from lead based to lead free has been gradual, legislation from the EU as well as growing environmental concern has driven the industry to a green or lead free electronic package. Within the electronic package the solder ball, used as a second level interconnect, is usually lead based and a major reliability factor. As the move to ban lead has taken hold, the need to develop a lead free solder alloy that is as reliable and convenient as the lead based solder alloys has become essential. So far, alloys containing tin, silver, and copper (SAC) have proven to be the most reliable and readily available solder alloys. However, the reliability and nature of these alloys is not as well known or documented as the traditional lead based solder balls.

In many reports [Syed 2001, Zhang 2003] as well as others, these lead free alloys have outperformed the common eutectic tin lead based alloys. Previous studies have compared the reliability of lead free alloys, but many of the tests have done so on different package types and under different temperature conditions. In this manner, it is hard to define a clear cut superior lead free alloy because the results have been shown to be strongly dependent on package type and thermal environment [Syed 2001, Roubaud 2001].With this test, 6 different test boards were assembled all having identical package dimensions and thermal conditions with the exception of the solder alloy used for the solder ball interconnect. SAC 105, SAC 305, Sn03Ag07, SAC X, SAC X plus, and Sn3.5Ag are all tested. The thermal environment was specified as -55 to 125 with ten minute dwells at each end.

As well as lacking reliability information, many of the alloys do not have documented Anand constants for finite element testing making it hard for life predictions based on finite element simulations. In this paper, finite element life predictions based on fatigue models proposed by other researchers [Syed 2004] are tested and their validity is shown. Also, the deformation and failure mode of the lead free solder ball is captured and better understood in a finite element environment. The hopes of this test are to show which alloys stand out as viable replacements for the well understood lead based alloys, as well as to further develop lead free finite element simulations and to better understand how the lead free alloys come to failure. The results of the tests, as well as finite element simulations, are presented in the pages that follow.

Lead free solders operate at temperatures close to 0.5 of their homologous temperature which means that creep will dominate the deformation kinetics [Syed 2004].

Depending on the stress level, the creep will follow certain deformation rules. In the low stress region you have both the Nabarro-Herring creep and the super-plasticity given by the following equation given in [Zhang 2003]:

$$\frac{d\gamma_{scr}}{dt} = A\tau^{n} \exp\left(\frac{-Q}{RT}\right) \tag{4.1}$$

In the higher stress region, known as climb controlled dislocation or power law breakdown, the deformation is dictated by:

$$\frac{d\gamma_{scr}}{dt} = A'\left[\sinh(\alpha\tau)\right]^{n} \exp\left(\frac{-Q}{RT}\right) \tag{4.2}$$

where alpha represents the stress in the power law breakdown region. For our modeling purposes, the Anand constitutive equation is used. Anand's equation consists of a flow equation and three evolution equations:

$$\frac{d\varepsilon_{p}}{dt} = A\left[\sinh\left(\frac{\xi\sigma}{s_{o}}\right)\right]^{\frac{1}{m}} \exp\left(\frac{-Q}{kT}\right) \tag{4.3}$$

$$\frac{ds_{o}}{dt} = \left\{h_{o}\left(|B|\right)^{a}\frac{B}{|B|}\right\}\frac{d\varepsilon_{p}}{dt} \tag{4.4}$$

$$B = 1 - \frac{s_{o}}{s^{*}} \tag{4.5}$$

$$s^{*} = \hat{s}\left[\frac{\frac{d\varepsilon_{p}}{dt}}{A}\exp\left(\frac{Q}{kT}\right)\right]^{n} \tag{4.6}$$

Many tests have been performed on the SAC alloys in an attempt to find out which alloy performs the best and to find a viable life prediction method. In this paper, six identical chip array ball grid arrays (CABGA) are tested. The packages are identical in every way except for the varying solder alloy. The hope here is to clearly show a difference between the different solder alloys tested and discover a clear cut, superior solder alloy and to gain a better understanding of the failure mechanism exhibited by the different alloy compositions. Previous tests have shown superior thermal performance of higher silver content alloys.

Schubert found that the SAC 405 alloy outperformed the Sn96.5Ag3.5 alloy [Schubert 2002]. In a test run by Darveaux, SAC 305 was shown as the strongest alloy based on shear strain tests [Darveaux 2005]. It has also been shown by Zhang that alloys with lower silver content have a greater increase in strain rate with longer aging times, even at room temperature [Zhang 2008]. Generally speaking, the higher silver content alloys have a lower strain rate, but are stiffer. Therefore, they do not hold up well in drop test performance, but do perform well in harsh thermal cycling environments [Huang 08]. In a power cycling environment, Young et al. showed that the SAC alloy can outlast the traditional tin lead alloy at low temperatures, but that the tin lead outperforms the lead free alloy at high temperatures in a power cycling test [Young 2008]. Roubaud shows that the SAC clearly outperforms the tin lead solder alloys, but that the performance is strongly dependent on profile temperature and package type [Roubaud 2001]. A test performed by Syed involving many different alloy compositions including doping the SAC alloys with earth additives was performed wherein the tin silver alloys

underperform the tin silver copper alloys, but again, the results are strongly dependent upon temperature and package type [Syed 2001].

A study involving lead free electronics and polymer stud grid array packages showed that the SAC alloy performance is strongly dependent upon package type with the solder alloys characteristic life doubling when the package architecture changed [Vandevelde 2004]. In another test, the lead free alloy Sn3.8Ag.7Cu was tested on plastic ball grid array (PBGA), plastic quad flat pack (PQFP), and thin small outlying package (TSSOP) wherein the different failure modes of the solder were demonstrated as well as the solder's performance on different pad finishes [Che 2005].

Recently, experimentation has been done involving the doping of SAC alloys in an attempt to soften the alloys while maintaining a low strain rate so that the interconnects will be useful in both a harsh thermal environment and in a drop or shock situation. Many additives have been tested, some working better than others [Rooney 2008, Huang 2008, Amagai2006]. Huang has shown some success in getting SAC 405 to be softened to the level of SAC 105 while still maintaining the creep properties of SAC 305. [Huang 2008] has shown that the addition of nickel to the SAC 405 alloy can help soften the alloy to the level of a low silver content alloy. When the interconnect is softened in this manner, it maintains its favorable creep properties, but increases drop test reliability as the more compliant interconnect holds up better under shock loading.

Other researchers have experimented with Bismuth doping [Kanchanomai 2002, Zhao 2003]. The Bismuth is added in order to lower the melting point of the Sn-Ag alloys. Though the Bismuth does lower the melting temperature, it also raises the homolgous temperature, leading to a rise in thermally activated processes such as creep

and grain growth. It was shown that with Bismuth, the alloy takes on an initial hardening, creating a less compliant interconnect. This increased stiffness decreases fatigue life of the interconnect [Kanchanomai 2002]. It has also been shown that an optimal amount of Bismuth is less than 3% [Zhao 2003]. For our alloy, the Bismuth content was 1%. Perhaps it is hoped that by adding the nickel the alloy will be softened to act more like a low silver alloy in drop tests applications, but that the addition of Bismuth will counteract the nickel addition in the thermal applications, thus creating a robust alloy that can be used in any application. The results of the dopants can be seen in the test results of the SAC-X and SAC-X Plus alloys. As mentioned earlier, all of the previous tests performed are helpful in documenting the performance of new lead free solder alloys, but tests that involve identical package types with different solder alloys are seldom performed. This paper offers new information about how each solder alloy fractures and how comparatively reliable each interconnect is in a harsh thermal environment.

4.2 Test Vehicle and Setup

In this experiment, 6 different lead free alloys are cycled in a harsh thermal environment. The thermal cycle runs from -55 to 125 Celsius with a 172 minute total cycle, ten minute dwells at each extreme. The thermal profile can be seen in figure 4-1 below.

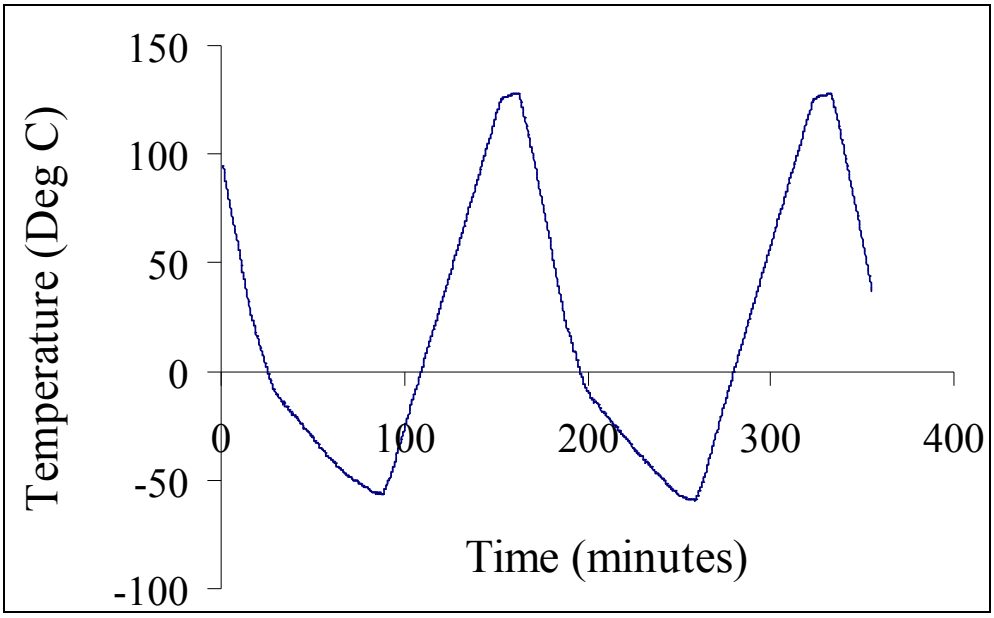

Figure 4-1 Thermal profile for lead free experiment

All boards are daisy chained and constantly resistance monitored. Any failure is denoted by a 10% rise in resistance wherein the resistance permanently stays 10% or greater after initial failure. The test board is shown in FIGURE 4-2 below. The test board dimensions are shown in table 4-1 below.

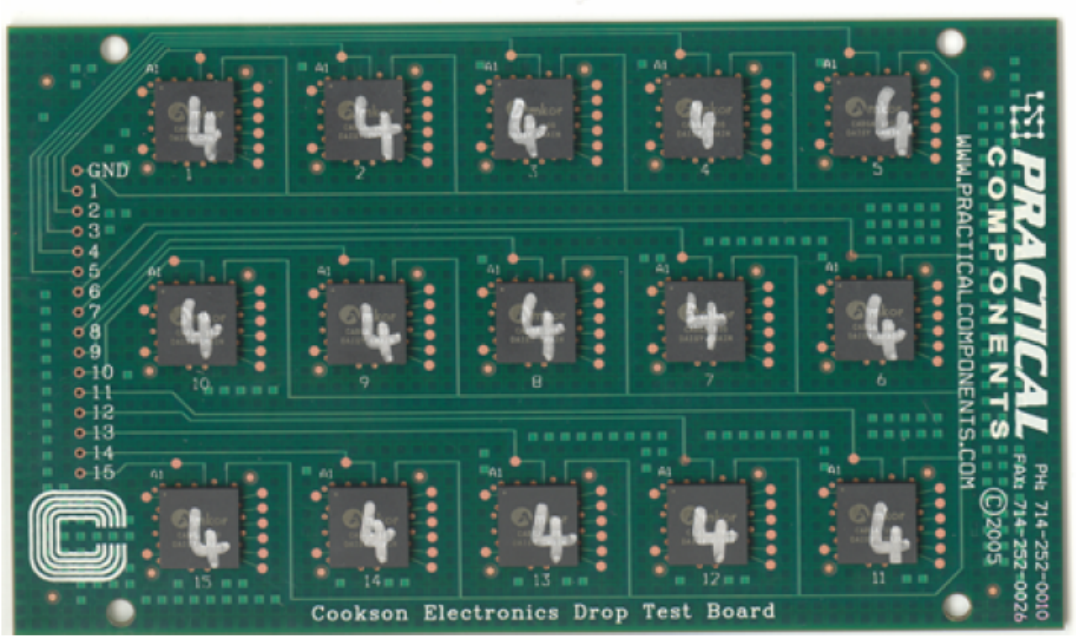

Figure 4-2 Test Vehicle Study 2 Lead Free Electronics

Table 4-1 Package dimensions Lead Free experiment

Ball Count	100
Ball Pitch (mm)	.8
Substrate thickness (mm)	.232
Pad Type	NSMD
Ball Diameter (mm)	.48
Die Size (mm)	5.55

4.3 Lead Free Reliability Results

4.3.1 SAC 105

Sn1%Ag0.5%Cu (SAC 105) alloy is a commonly used low silver content alloy that is more compliant, but has a high strain rate under thermal load. Generally, this alloy and all alloys having a low silver content are more compliant, but do not hold up well in creep deformation [Rooney 2008]. The Weibull plot showing the characteristic life of the SAC 105 alloy is in figure 4-3.

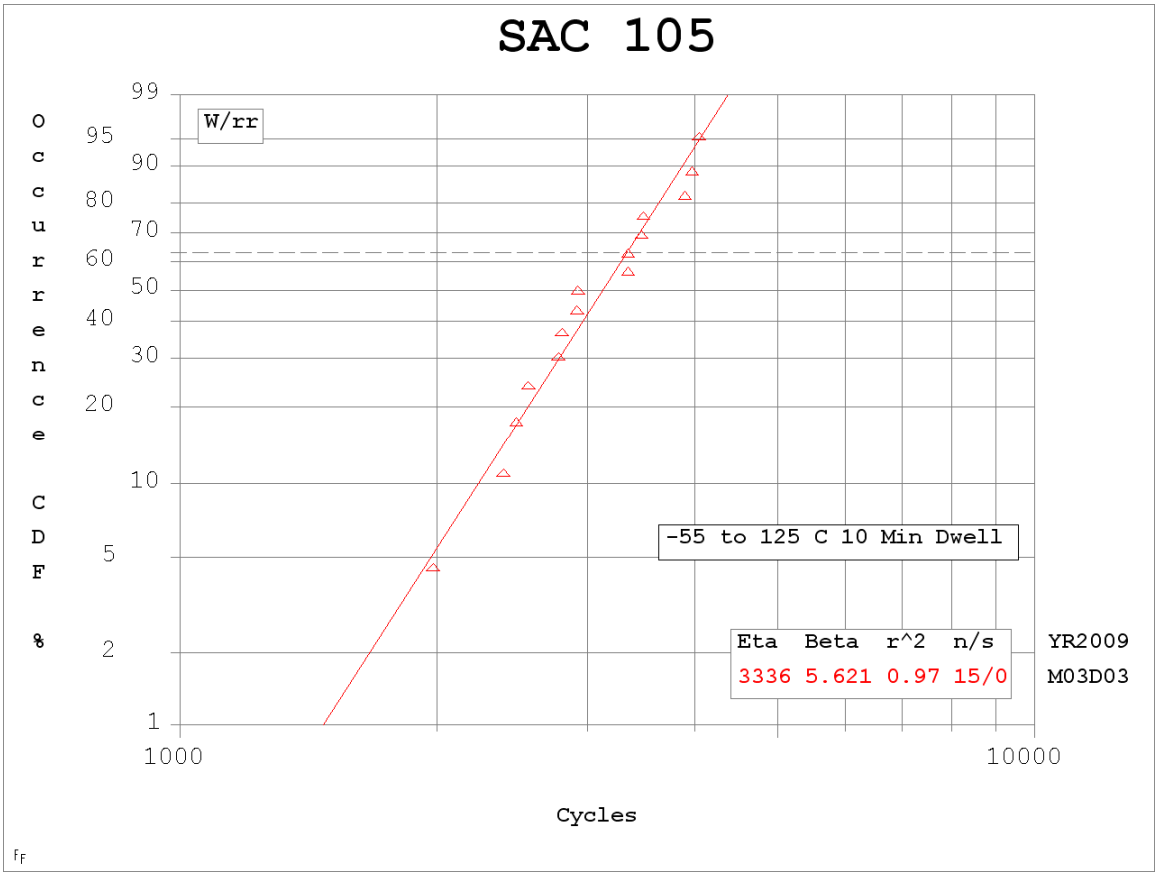

Figure 4-3 SAC 105 Wiebull plot

The SAC 105 alloy had a characteristic life of 3,336 cycles. The N1% life was 1,467 cycles while the β, slope, is 5.6. The SAC 105 greatly underperformed the high silver

content alloys as was expected. Failure results of the experiment can be seen below in figure 4-5. The package chosen for cross sectioning is highlighted in red in 4-4 below.

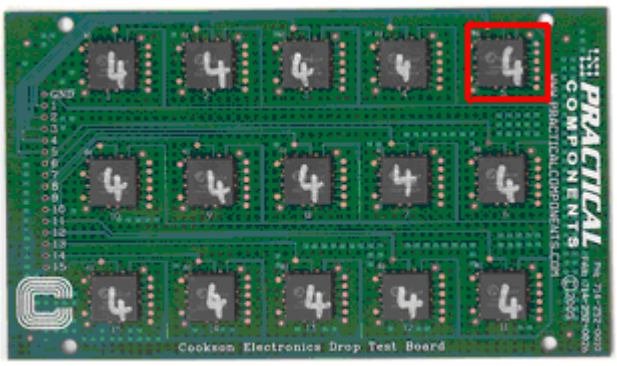

Figure 4-4 Sectioned Package

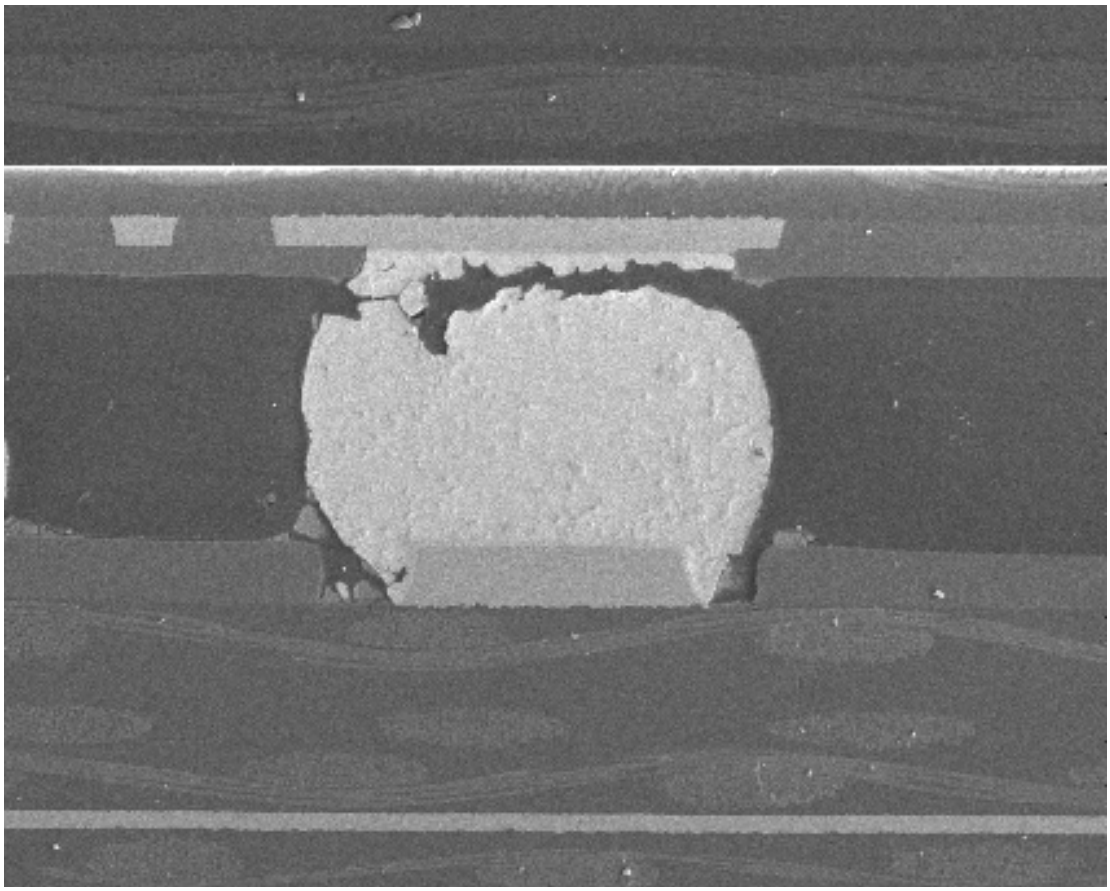

Figure 4-5 Failed Solder Ball in right die shadow

The solder ball in figure 4-5 is located in the right die shadow of the package. The interconnect showed maximum damage at the top of the interconnect along the package side interface. This was the dominant failure mode in all of the SAC 105 images taken. Another SEM image seen in figure 4-6 below shows a crack in the bottom of the interconnect along the PCB interface. A blown up picture of the crack along the bottom of the interconnect is seen in figure 4-7

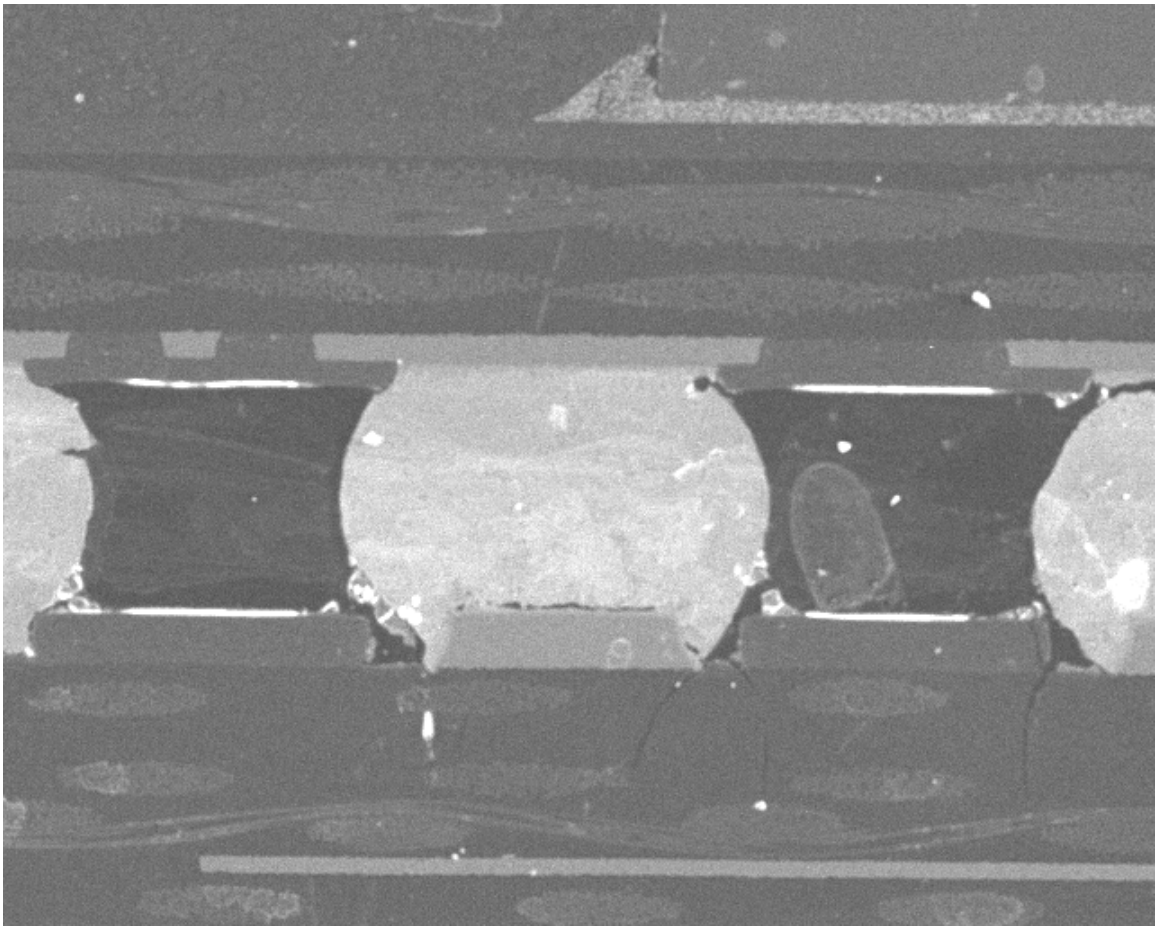

Figure 4-6 SAC 105 left die shadow showing board side crack

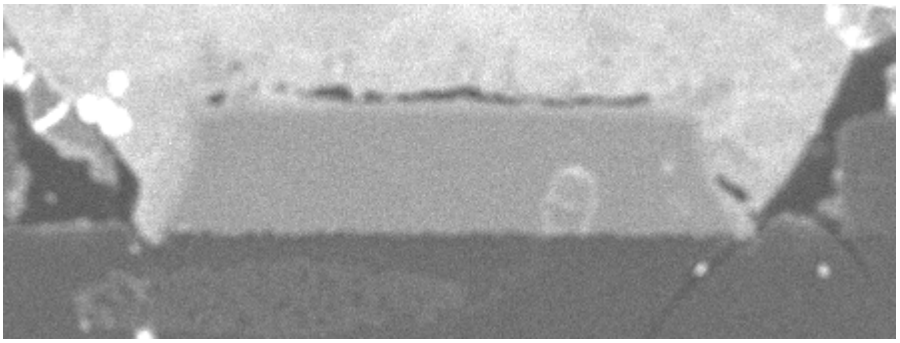

Figure 4-7 Blown Up SAC 105 Crack

The SAC 105 alloy outperformed both the SAC 0307 and SAC X alloys, but underperformed the SAC X-Plus, Sn3.5Ag, and SAC 305 alloys.

4.3.2 Sn.0.3%Ag0.7%Cu (SAC0307)

This alloy had the lowest silver content of all the alloys tested at 0.3%. Therefore, it would be thought that this alloy would perform worst in the thermal test. The Weibull plot can be seen in figure 4-8 below.

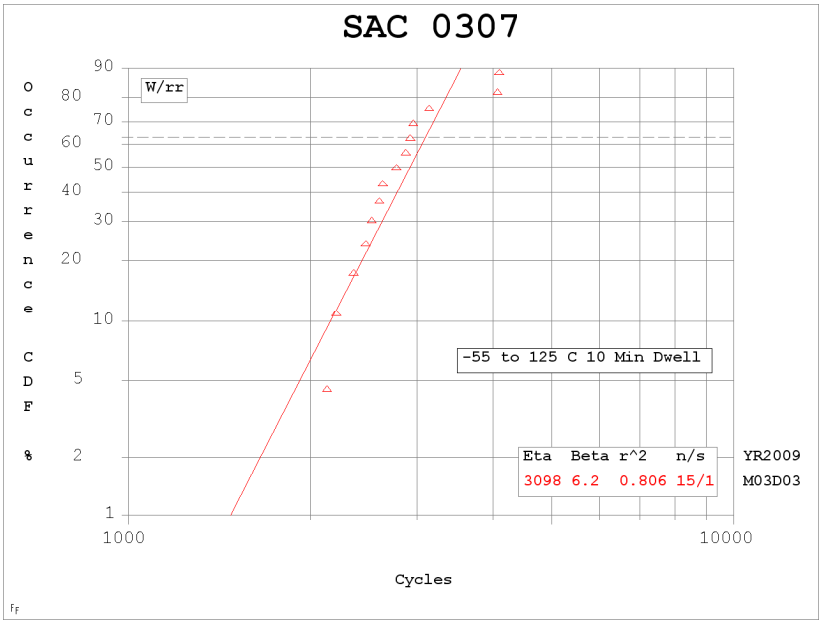

Figure 4-8 Weibull plot SAC0307

The characteristic life, where 63.2% of the population has failed, is 3,098 cycles with one suspension remaining. The N1% is 1,475 cycles while the β is 6.2. As expected, this alloy performed the worst most likely due to its low silver content. The alloy still performed fairly well with a characteristic life above 3,000 cycles, but comparatively it was the worst of all six solder alloys tested. Anand constants for this alloy were not available, so a finite element model could not be created. SEM pictures are available and the failure mode can be clearly seen in figure 4-9.

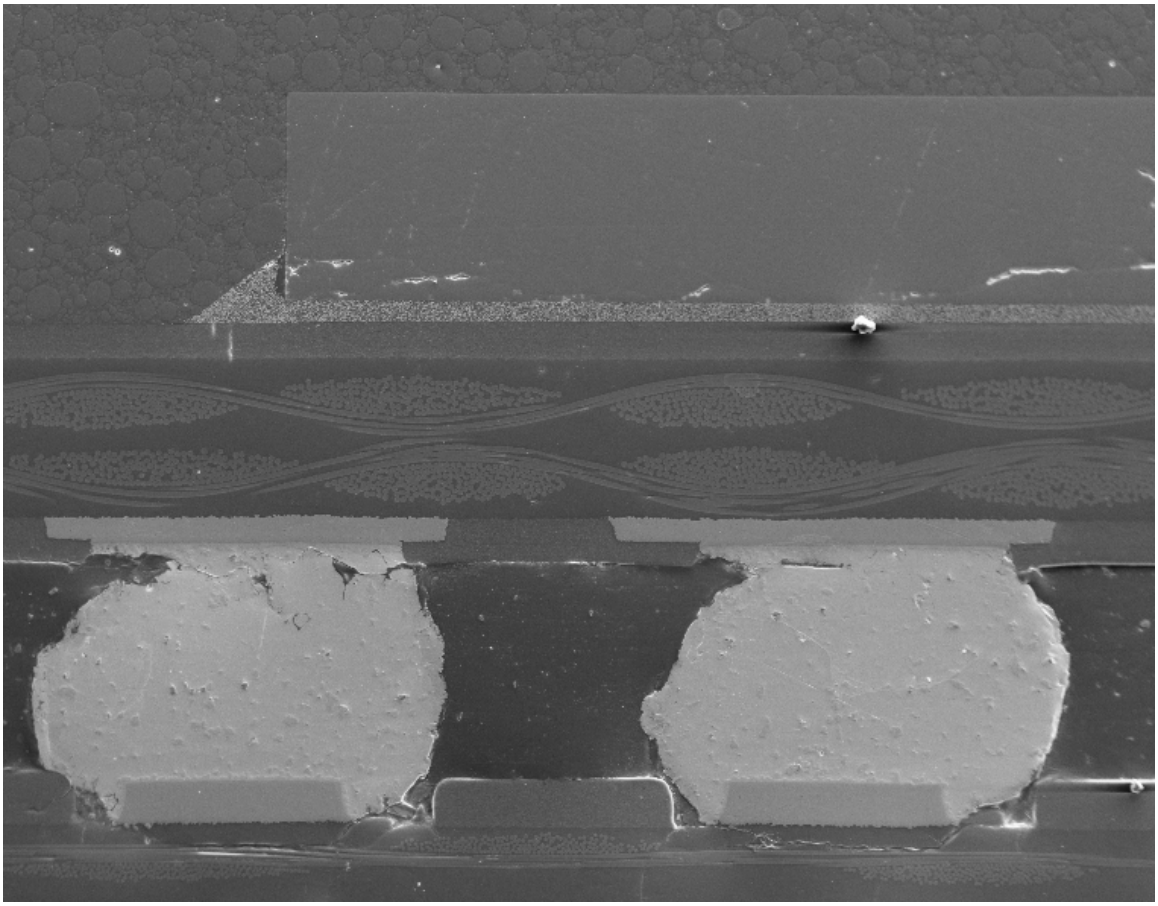

Figure 4-9 Failed SAC0307 interconnect

Figure 4-9 shows the die shadow of the SAC 0307 package. The ball under the die shadow was the first to fail. A crack can be seen across the top of the interconnect to the

left in the Figure. A close up of this interconnect demonstrating the crack can be seen below in figure 4-10.

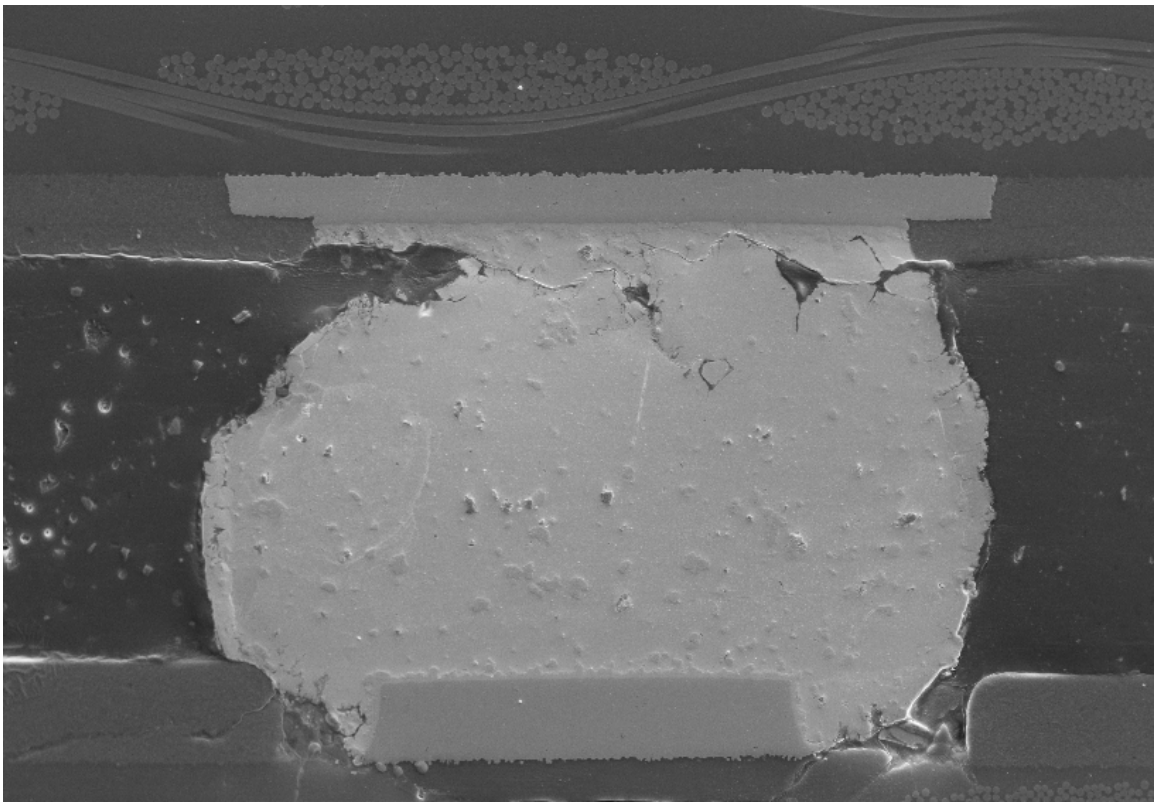

Figure 4-10 Crack in top of SAC 0307 interconnect

Unlike the SAC 105 alloy, the SAC 0307 showed no damage at the bottom of the interconnect. All of the damage was at the top of the interconnect and the dominating failure mode was crack growth across the top of the interconnect at the package side interface. The SAC 0307 underperformed the SAC 105 alloy by 238 cycles.

4.3.3 SAC X

The SAC X alloy has the following composition: Sn.3%Ag.7%Cu.1%Bi. As mentioned earlier, most doping of alloys has proven to reduce the interconnect stiffness while maintaining the fatigue life of the alloy. This effect has generally been seen in high

silver content alloys. Because the SAC X alloy has a low silver content to begin with, the fatigue life is already thought to be poor. The hope here is that the Bismuth dopant will provide the compliance of a low silver alloy while bumping the fatigue life up to that of a high silver content alloy. The results, however, don't seem to show a great increase in fatigue life as the characteristic life was low when compared to the higher 3% silver alloys such as SAC 305. The alloy was stronger than the other low silver content alloy SAC0307, suggesting that the doping did help with creep properties, but not enough to make the interconnect as reliable as a high silver content alloy. The Weibull plot for the alloy is presented below in figure 4-11.

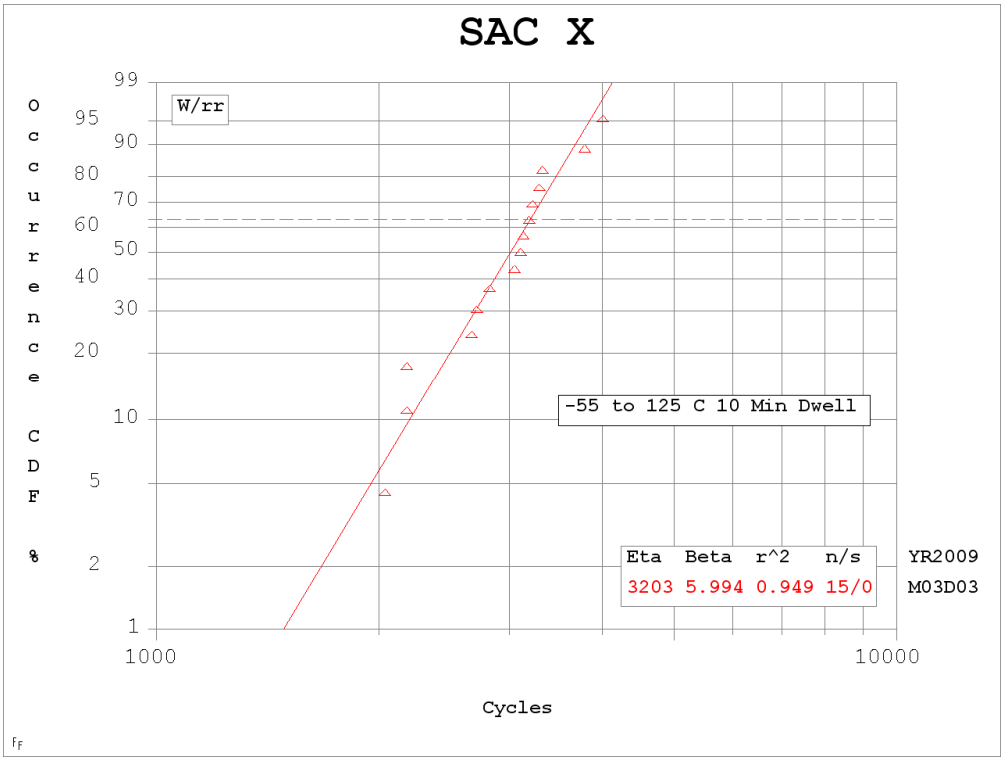

Figure 4-11 Weibull plot for SAC X alloy

The characteristic life of the SAC X alloy is 3,203 cycles. The N1% life is 1,486 cycles and the β is 5.99. Again, a finite element model of the SAC X alloy could not be created

because valid Anand constants are not available. An SEM image of the failed package with failure mode identified is presented in figure 4-12 below.

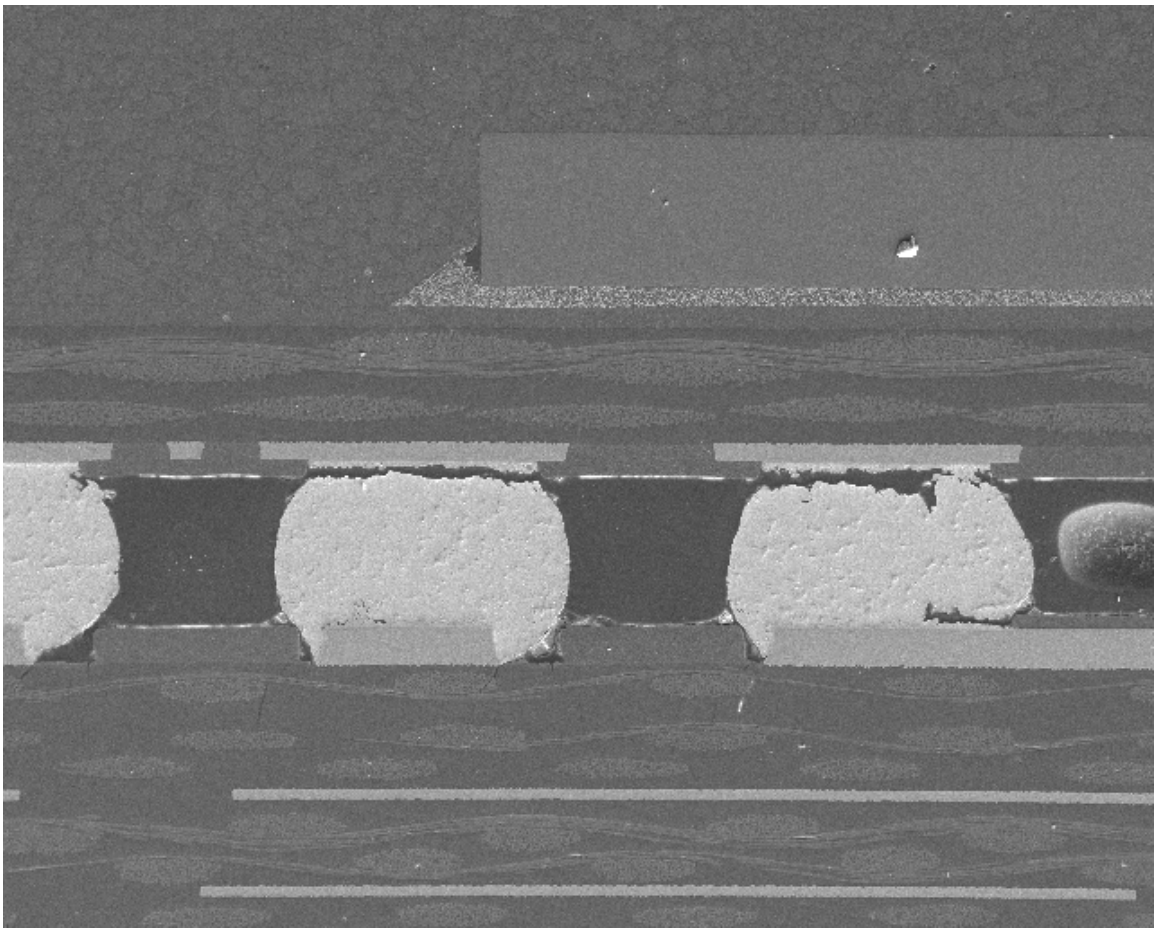

Figure 4-12 SAC X Die Shadow failure

Similarly to both the SAC 105 and the SAC0307, the ball in the die shadow was the first to fail. The crack initiated in and propagated along the package side interface growing across the top pad. The solder ball to the right of the interconnect in the die shadow shows some damage at the bottom of the solder ball along the board interface. Crack growth in the top of the interconnect at the package side interface was the dominant failure mode seen in all packages, though some damage was seen in the board

side interface. Figure 4-13 below shows a partial crack in the solder ball located in the right die shadow of the package.

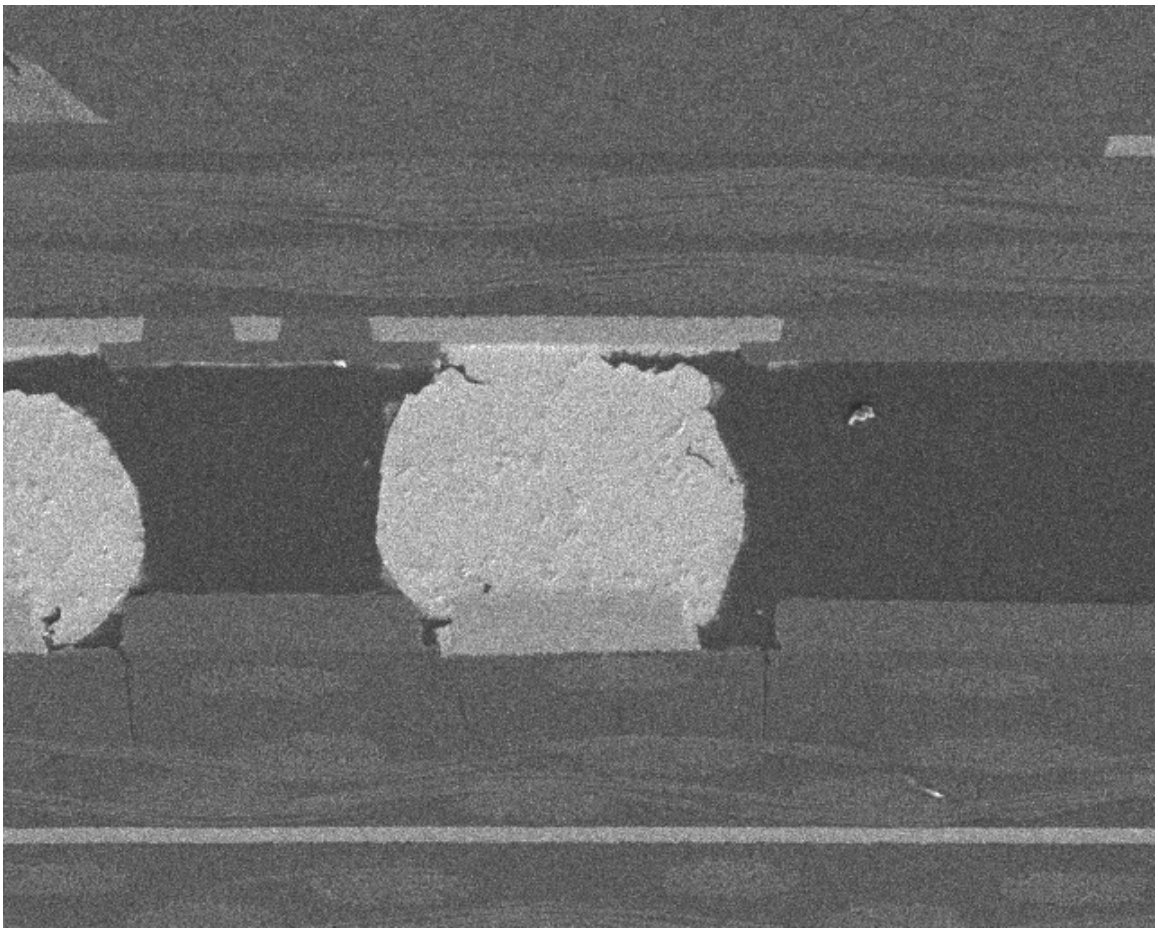

Figure 4-13 SAC X Partial Crack

In figure 4-13, the crack has grown across half of the interconnect. Minimal damage is seen at the bottom of the interconnect. A summary of the package performances to this point is given below in table 4-2. The SAC X is the second most reliable package so far.

Table 4-2 Characteristic life comparison

Alloy	Characteristic Life (η)
SAC 105	3,336
SAC 0307	3,098
SAC X	3,205

4.3.4 SAC X-Plus

The SAC-X Plus alloy has the composition of Sn.2%Ag.7%Cu.1%Bi.1%Ni. With this alloy, the hope is that the dopants will give the interconnect the creep properties of a high silver alloy while maintaining the stiffness and drop reliability of a low silver alloy. In particular, the Bismuth initially hardens the alloy while the addition of Nickel is used to improve ductility of a low silver alloy [Kanchanomai 2002]. The results for this alloy were better than some of the other alloys, but it still underperformed the high silver content alloys. The Weibull plot can be seen in figure 4-14 below.

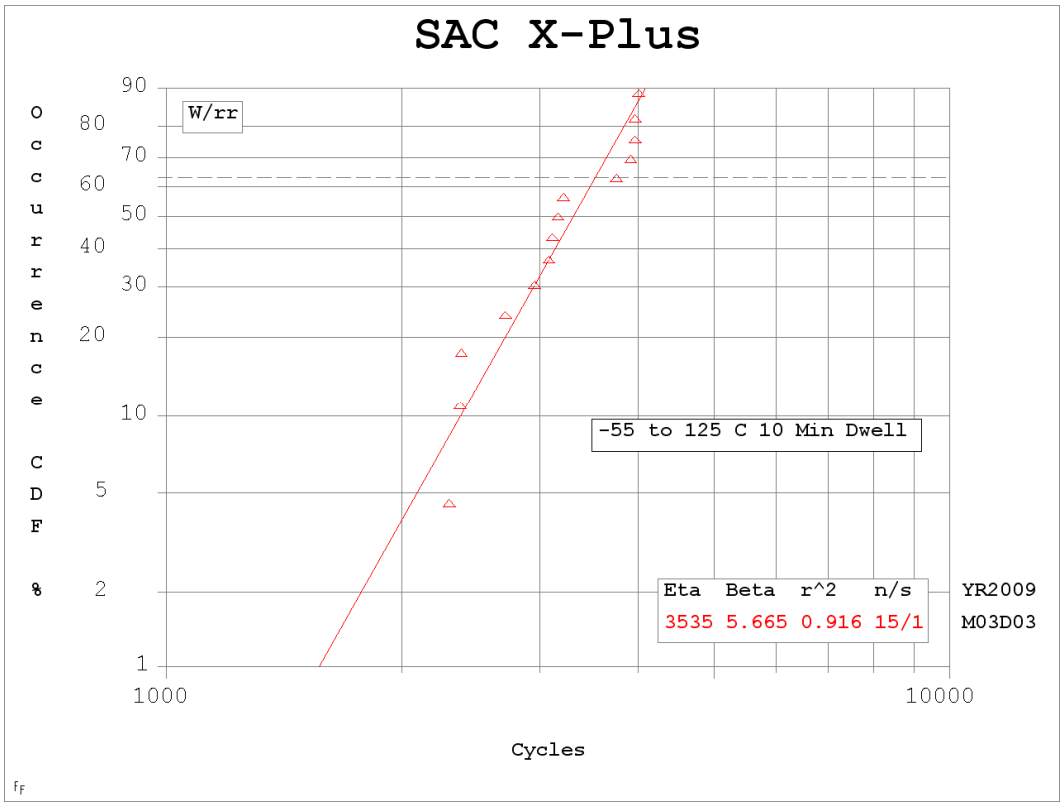

Figure 4-14 SAC X-Plus Weibull plot

The characteristic life is 3,535 cycles. The N1% life is 1,554 cycles and the β is 5.6. The SAC-X+ alloy outperformed the other alloys by nearly 200 cycles. The higher silver content boards, SAC 305 and Sn3.5Ag, still outperformed this alloy by hundreds of

cycles. Seen in figure 4-15 below is an SEM image of the failed interconnect in the right die shadow region.

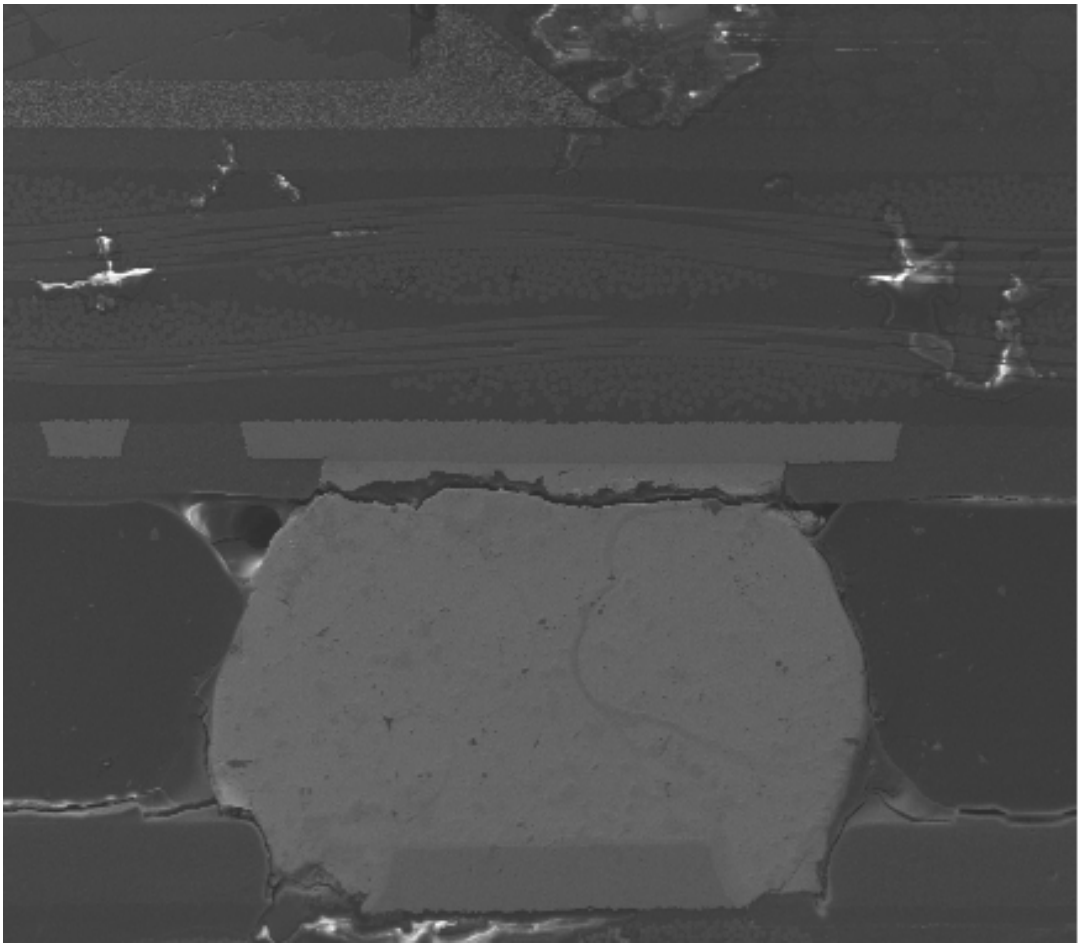

Figure 4-15 Failed SAC X-Plus Solder Ball

As can be seen, the ball in the die shadow region was the first to fail. Once again, the crack propagated along the top of the interconnect at the package side interface. The same is shown figure 4-16 below. Some damage can be seen to the left of the ball in the die shadow region. Some cracking can be seen in the PCB underneath the left solder ball in figure 4-16.

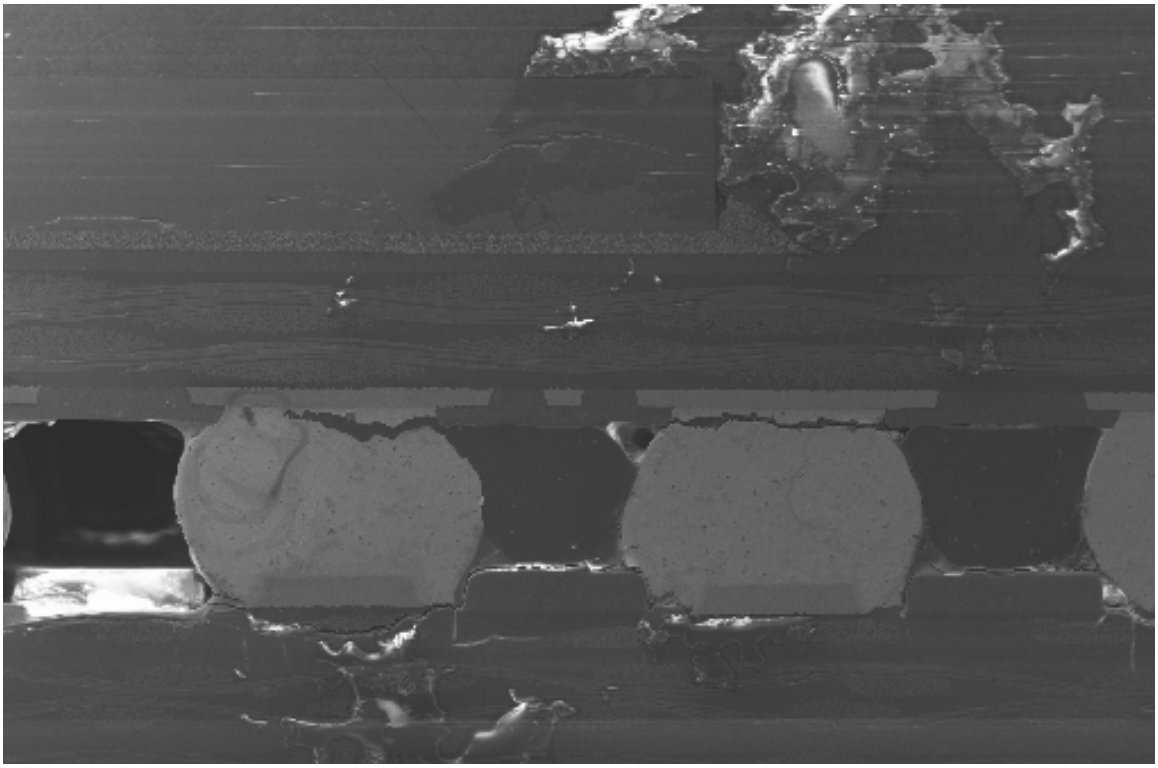

Figure 4-16 SAC X Plus Failed solder ball

The results for this interconnect were better than the other low silver alloys presented previously, but still paled in comparison to the high silver content SAC 305 and Sn3.5Ag. Thus, it can be shown that the best material for an extreme temperature environment is still the high silver board, despite any attempts to make a low silver board similar to a high silver board by dopants. The superior creep properties of the high silver board have been shown. The SAC 305 and Sn3.5Ag interconnects have not had enough failures to do intrusive research on. To date, a Weibull plot has not been generated and SEM images of the packages are not available. It is interesting to note that all of the alloys had the similar failure mode of cracking at the package side interface of the solder interconnect. The high silver alloys showed greater thermal reliability. Table 4-3 below compares the lives of all the alloys.

Table 4-3 Life comparison of all solder alloys

Alloy	Characteristic Life (η)
SAC 0307	3,098
SAC X	3,205
SAC X Plus	3,535
SAC 105	3,336
SAC 305	NA
Sn3.5Ag	NA

4.4 Finite Element Models

The solder materials were meshed with VISCO 107 elements. All other materials were meshed with eight node SOLID 45 elements. All the materials except the PCB and the BT substrate were modeled as isotropic. The Anand's constants for SAC 305 are shown in table 4-4 and were taken from [Chang 2006]. The Anand constants for Sn3.5Ag are shown in table 4-5, taken from [Chen 2005].

Table 4-4 Anand constants SAC 305 [Chang 2006]

SAC 305 Anand constants	
S_o	45.9 (MPa)
Q/k	7460 $\left(1/K\right)$
A	5.87e6 $\left(1/\text{sec}\right)$
ζ	2
m	.0942
h_o	9350(MPa)
n	.015
a	1.5
$\hat{s}$	58.3(MPa)

Table 4-5 Anand constants Sn3.5Ag

Sn3.5Ag Anand constants	
S_o	9.6278 (MPa)
Q/k	8549 $\left(1/K\right)$
A	177016 $\left(1/\text{sec}\right)$
ζ	7
m	.207
h_o	27782(MPa)
n	.0177
a	1.6
$\hat{s}$	52.4(MPa)

The material properties for the finite element models of both packages are shown below in table 4-6.

Table 4-6 Material Properties for finite element models

Component	E GPa	α ppm/°C	υ
PCB	17(x,z) 7(y)	15(x,z) 67 (y)	.39
Solder Ball	54	25	.3
BT Substrate	18(x,z)7(y)	12(x,z)57(y)	.3
Solder Mask	3	30	.3
Die Adhesive	7	52	.35
Silicon Die	162	2.5	.28
Mold	23	15	.3
Copper Pad	128	16	.34

4.4.1 SAC 305 Model

A diagonal view of the SAC 305 model can be seen below in figure 4-17

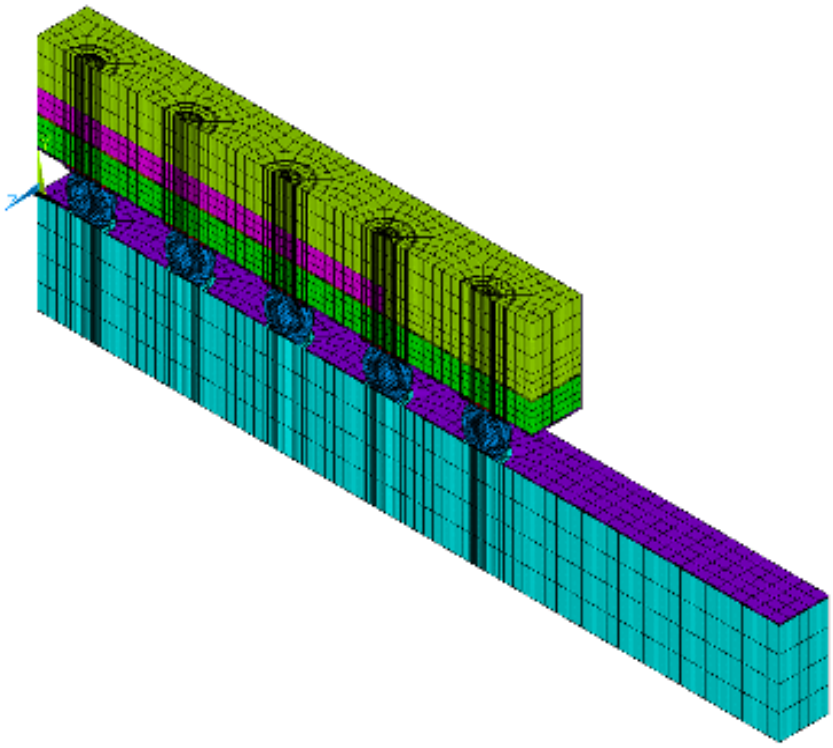

Figure 4-17 Diagonal view SAC 305

A close up of the interconnect can be seen below in figure 4-18

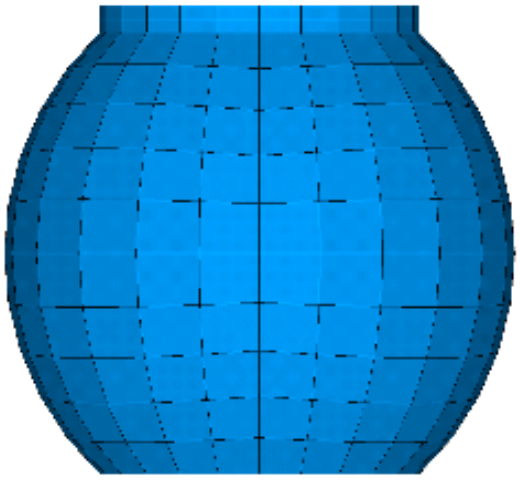

Figure 4-18 SAC 305 Interconnect

The dimensions in table 4-1 were used to recreate the model. The thermal cycle was recreated in ANSYS. The failure results of the simulation are shown below in figure 4-19. The bottom layer was chosen for plastic work calculation, as mentioned previously.

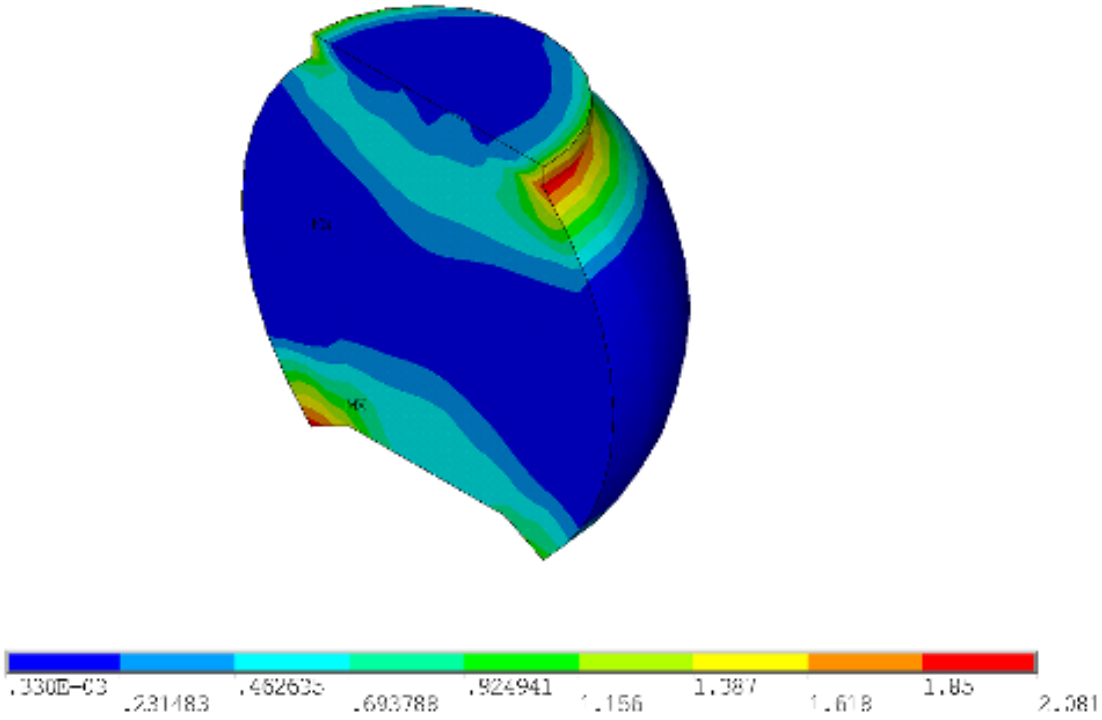

Figure 4-19 SAC 305 FEM Failure

Maximum damage was seen in the lower left hand corner at the board side interface while a lot of damage was also seen in the top right corner at the package side interface. The results for the SAC 305 simulation are similar to the same failure modes presented for the other lead free alloys in cross sectioning in that a large amount of damage is seen at the board side and package side interface. The ball in the die shadow was the first to fail. The ball shown here is the corner solder ball furthest away from the center of the package. Hysteresis plots and plastic work plots for the package are shown below in figure 4-20 and figure 4-21.

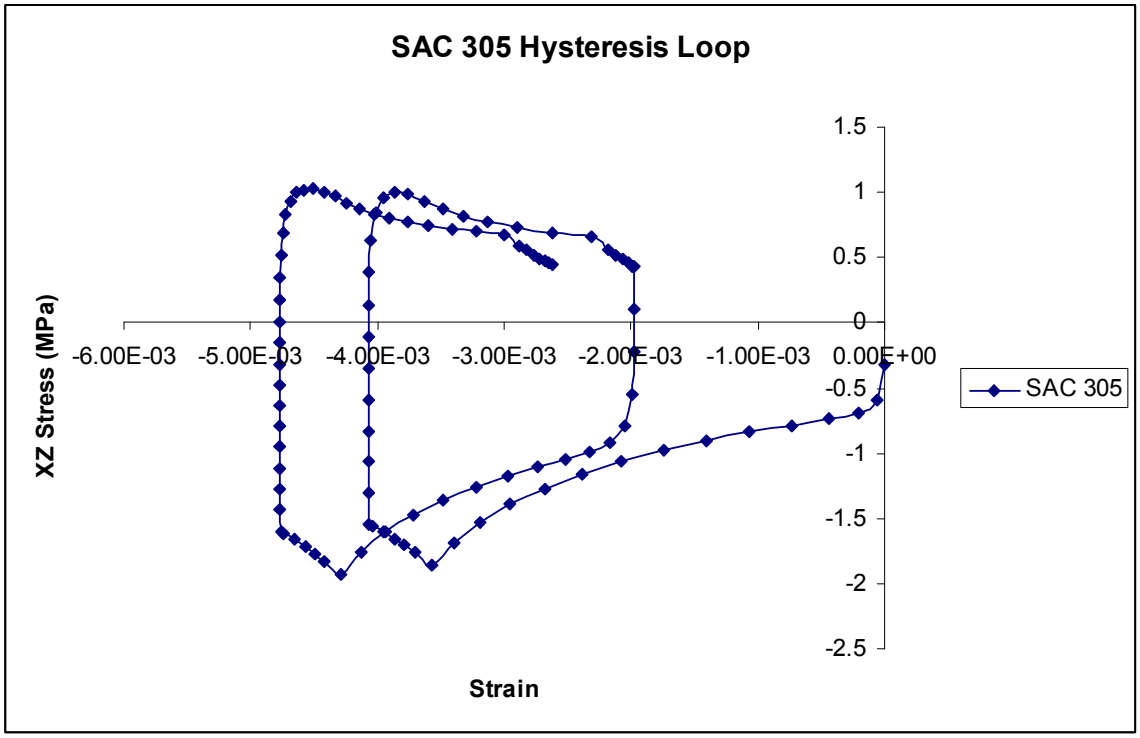

Figure 4-20 SAC 305 Hysteresis Loop

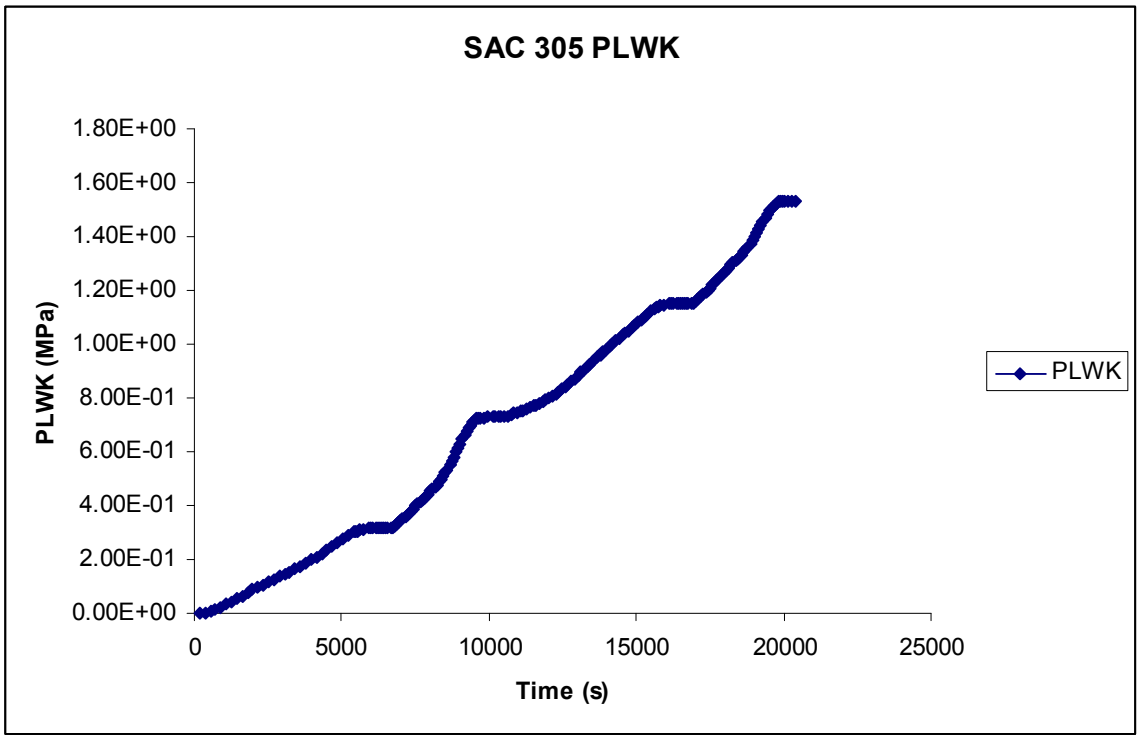

Figure 4-21 SAC 305 Plastic Work Plot

Figure 4-20 shows that the hysteresis loop has stabilized after two simulated thermal cycles. The plastic work plot shown in figure 4-21 shows the plastic work accrued with time which has a maximum value of 1.6 MPa. While a clear cut life prediction method has not yet emerged, Syed's life prediction method was used for correlation. Syed uses the following constitutive equation when developing his life prediction:

$$\dot{\varepsilon}_{cr} = A_1[\sinh(\alpha\sigma)]^n \exp\left(\frac{-H_1}{kT}\right) \tag{4.7}$$

which was first proposed by Schubert. Using this constitutive equation along with some regression analysis, Syed develops the life equation $N_f = (.0014\omega_{acc})^{-1}$ [Syed 2004]. The life prediction equation has given good results on one simulation involoving SAC 305 and poor correlation on the SAC 305 and Sn3.5Ag models presented here. The problem with using this equation exists in the fact that the FEM creep model is based on the Anand equation, while Syed uses Schubert's model for the constitutive equation. For this model, the life prediction correlation can be seen below in table 4-7.

Table 4-7 Life Correlation SAC 305

Simulation	2,359
Experiment	No failures as of 4,200 cycles

Though no exact error can be put on the life estimation, the simulation does not seem to closely track the actual results as the experiment has reported no failures as of 4,200 cycles and the characteristic life of the simulation is 2,359 cycles. The life reported by Syed's equation is the mean life of the package. In order to get the characteristic life, one must modify the answer by using the slope of the Weibull plot according to the equation

$$\eta = \text{MeanLife} / \exp(\text{GAMMALN}(1 + 1/\beta)) \tag{4.8}$$

4.4.2 Sn3.5Ag

The finite element model for the Sn3.5Ag is identical to the SAC 305 model except for the solder composition. A diagonal view of the package can be seen below in figure 4-22.

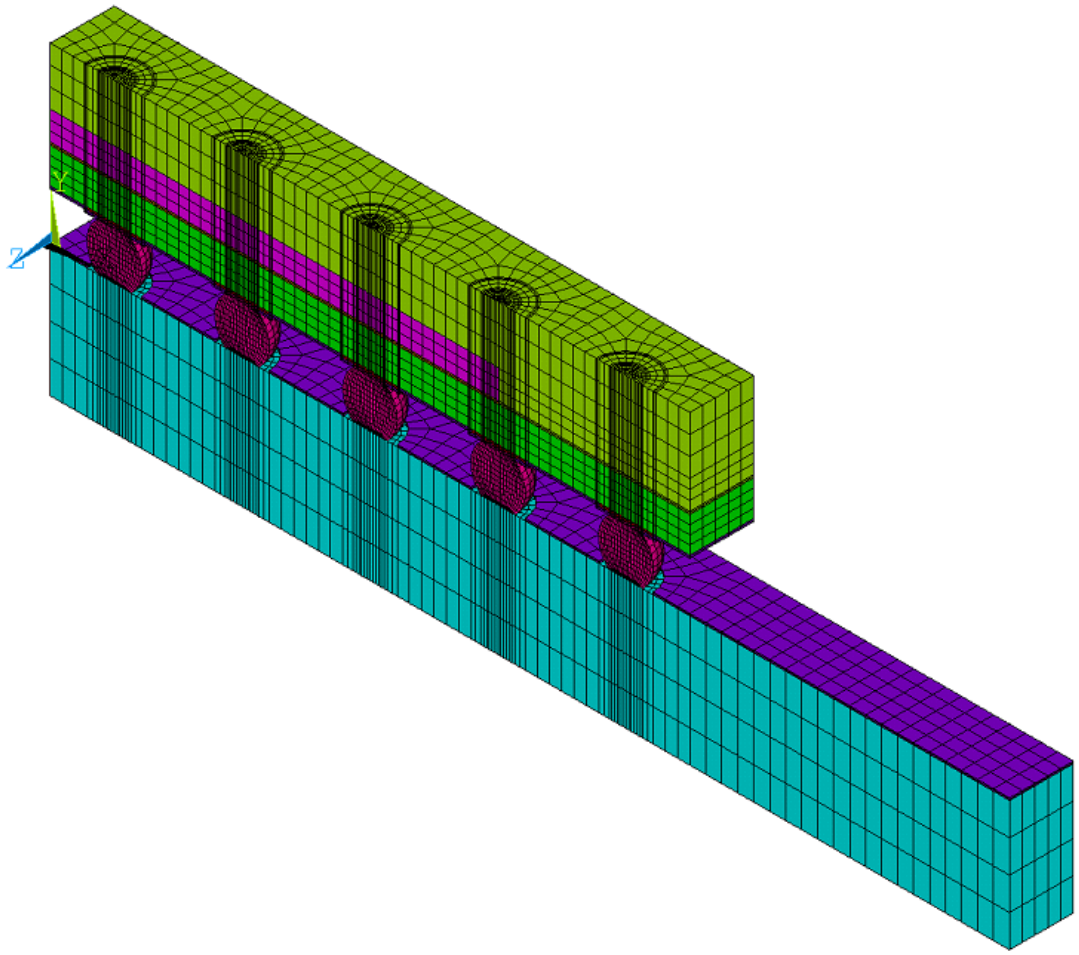

Figure 4-22 Sn3.5Ag Finite Element Model

The Sn3.5Ag model uses the Anand constants given in table 4-4. The simulation results can be seen below in figure 4-23

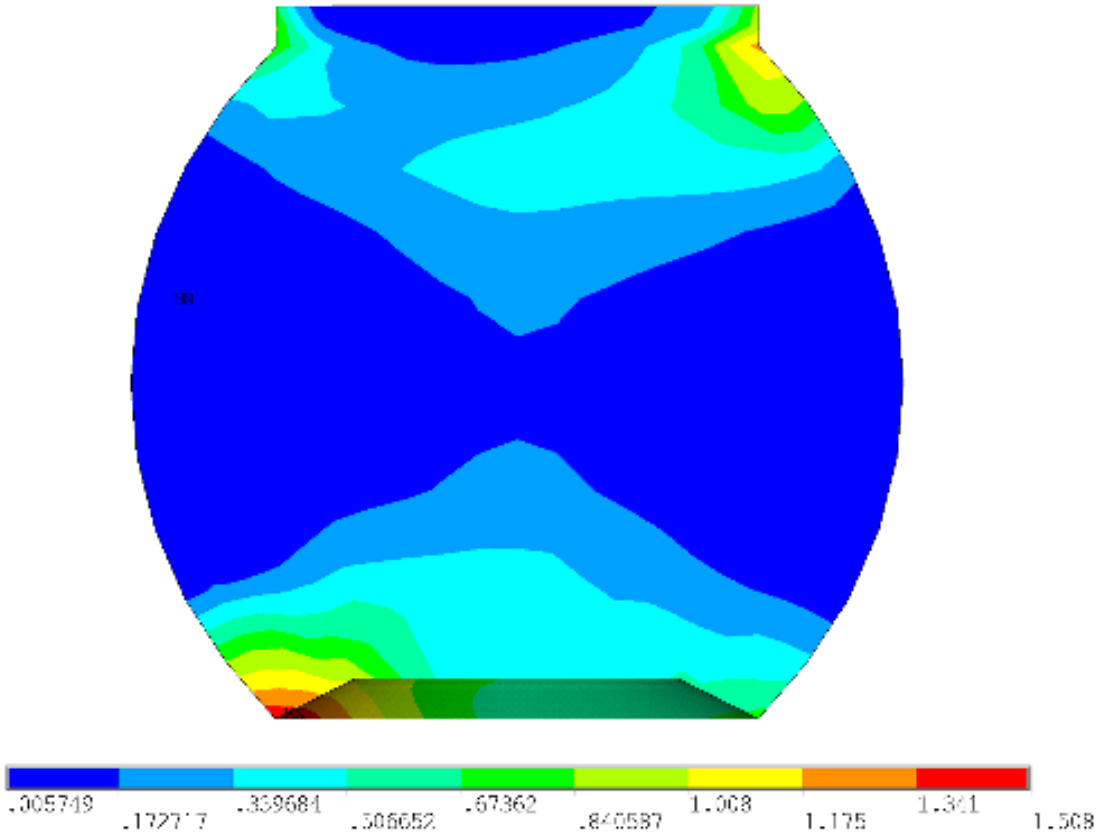

Figure 4-23 Sn3.5Ag Failure Results

The results of this model were very similar to those shown for the SAC 305 model. The maximum damage is once again in the lower left hand corner of the interconnect while a large amount of stress is also seen in the top right corner of the interconnect. The plastic work of the Sn3.5Ag model is less than that seen in the SAC 305 model. The hysteresis loop and plastic work plot of the Sn3.5Ag model are shown below in figure 4-24 and figure 4-25. Similarly to the SAC 305, the lower layer of elements was selected for plastic work calculation.

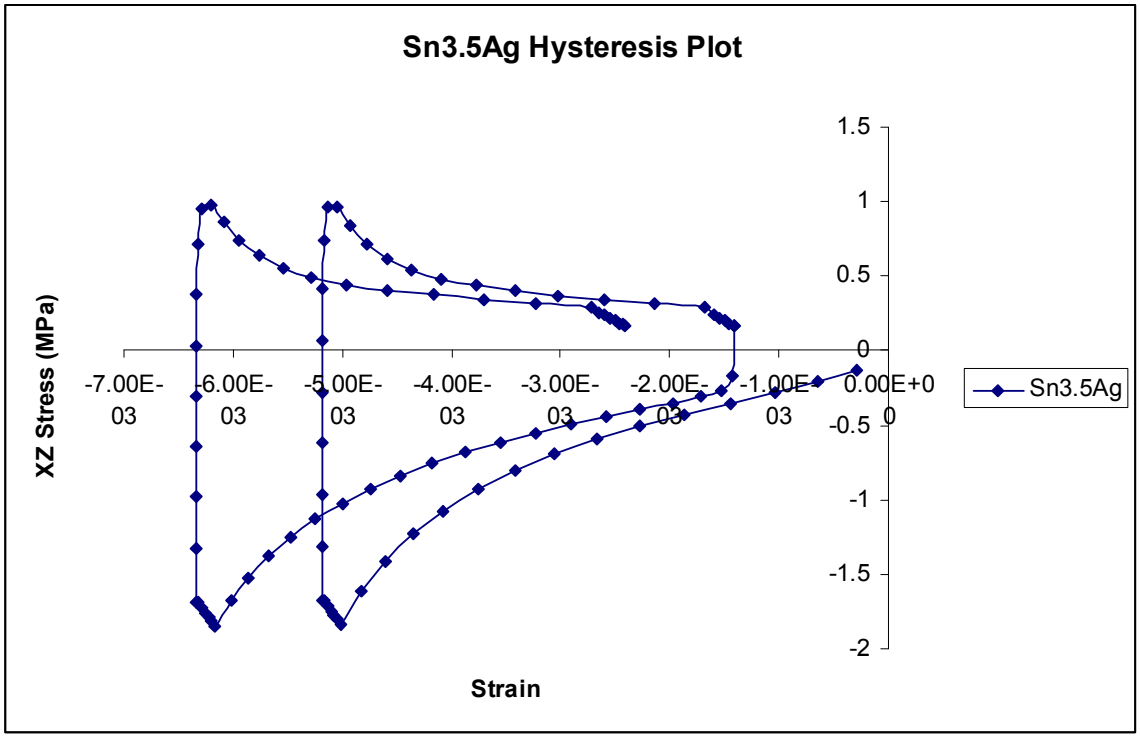

Figure 4-24 Sn3.5Ag Hysteresis Loop

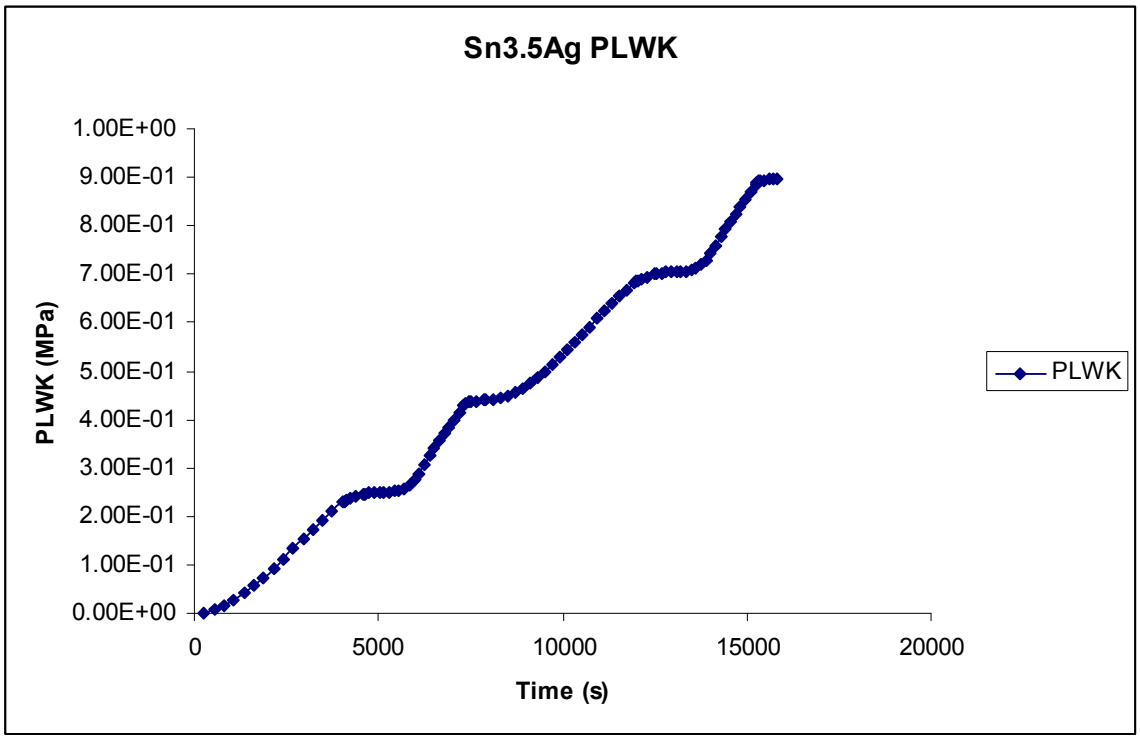

Figure 4-25 Sn3.5Ag Plastic Work

The same life prediction equation used on the SAC 305 model was used here on the Sn3.5Ag model. The life correlation is given in table 4-8 below.

Table 4-8 Sn3.5Ag Life Correlation

Simulation	2,192
Experiment	No failures as of 4,200 cycles

No exact error can be put on the Sn3.5Ag life prediction, however, the life prediction does not seem to closely track reality as the simulated characteristic life is 2,192 cycles and there are only two reported failures as of 4,200 cycles. A comparison of the hysteresis loop and plastic work for the two packages is given below in figure 4-26 and figure 4-27.

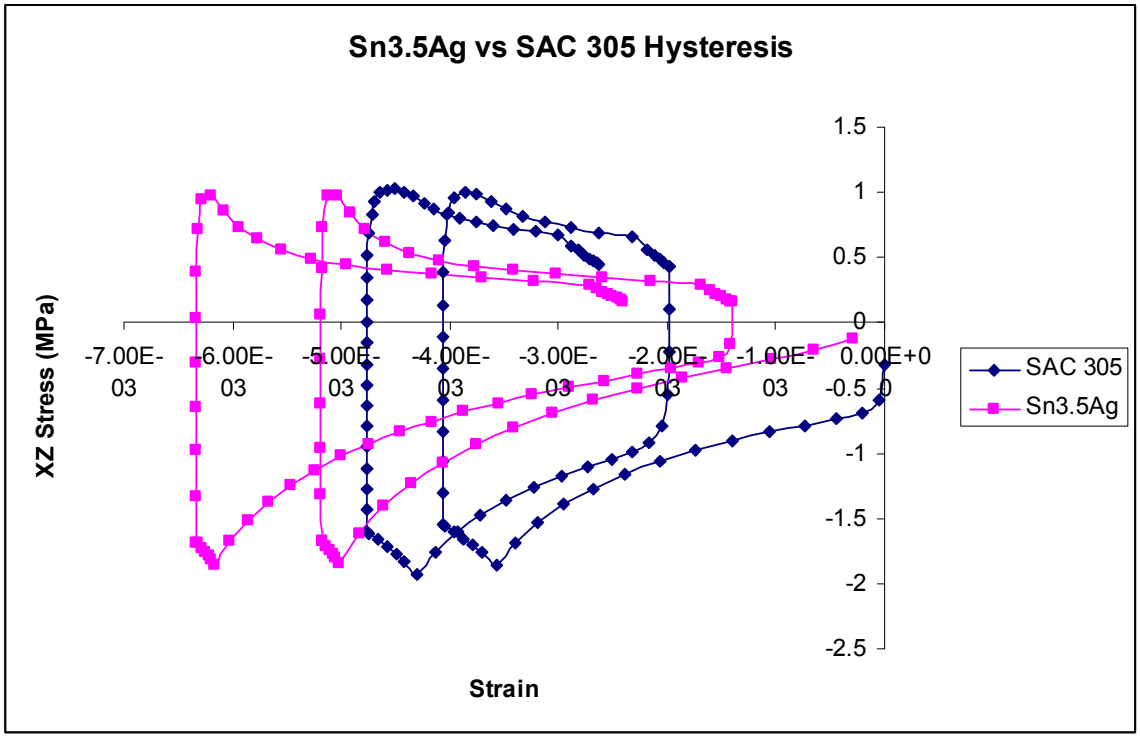

Figure 4-26 Hysteresis Loop Comparison

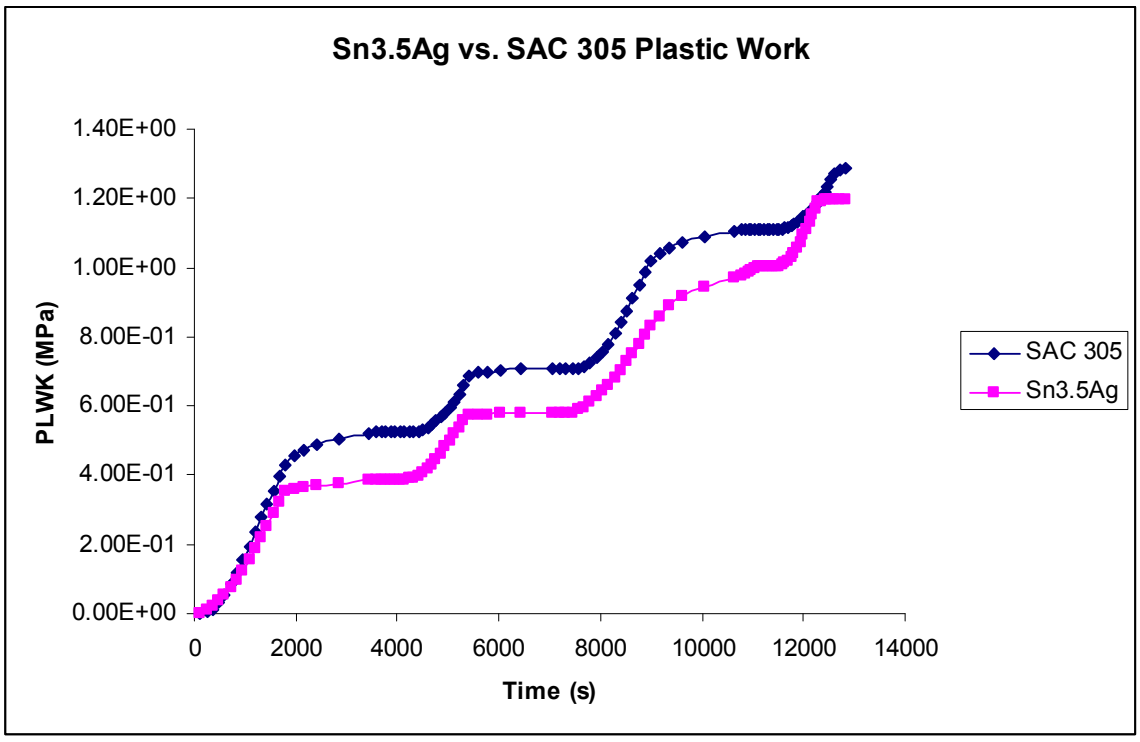

Figure 4-27 Plastic Work Comparison

The hysteresis loop and plastic work comparison show similar results. The damage incurred by the SAC 305 and Sn3.5Ag model seem to be very similar both in magnitude and location. Both packages experienced maximum damage in the lower left hand corner and both packages reached plastic work values of 1.2MPa.

4.5 Summary

The high silver alloys outperformed the low silver alloys in a harsh thermal environment as expected. The doped alloys did show some improvement over the other low silver alloys, but did not meet the level of the high silver alloys. The life prediction equation,

$$N_f = \left(.0014\omega_{acc}\right)^{-1} \qquad 4.9$$

as presented by [Syed 2004] has not given good life correlation in finite element simulations. As of 4,200 cycles neither of the high silver content alloys have had more than 2 out of 15 failures where as the other alloys have failed completely. The failure results of the packages are summarized below in figure 4-28 and below that in table 4-8, showing characteristic life.

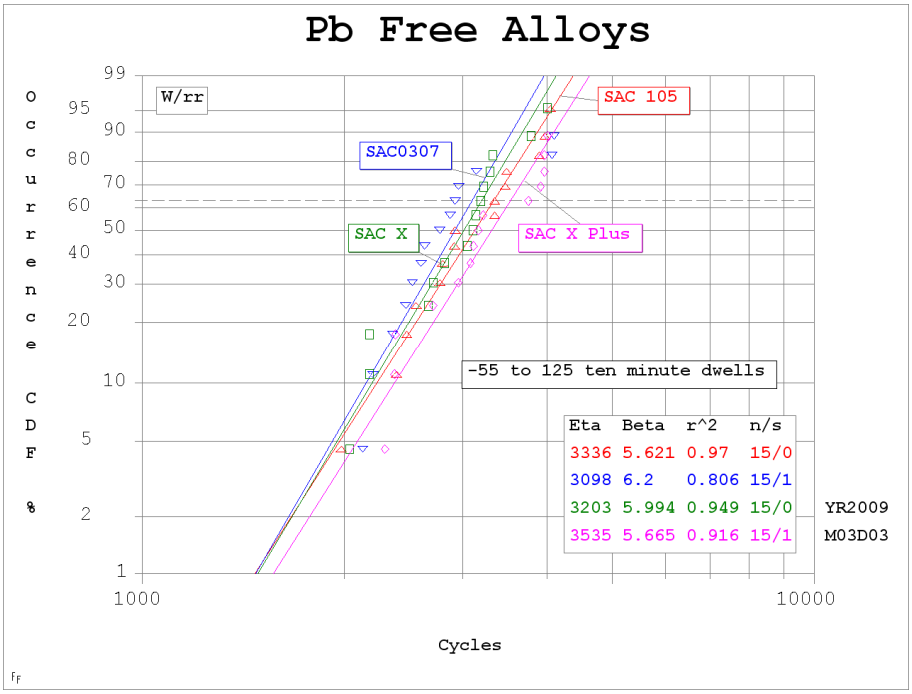

Figure 4-28 Lead Free Alloys Comparison

Table 4-8 shown below summarizes the characteristic lives of the packages. SAC 0307 was the worst while the high silver content alloys were the best.

Alloy	Characteristic Life (η)
SAC 105	3,336
SAC 0307	3,098
SAC X	3,205
SAC X Plus	3,535
SAC 305	0 of 15 at 4,200 cycles
Sn3.5Ag	2 of 15 at 4,200 cycles

Table 4-8 Lead Free Characteristic Life Comparison

CHAPTER 5

UNIQUE I/O PACKAGES IN HARSH THERMAL ENVIRONMENTS

5.1 Introduction

In this project, the thermo-mechanical reliability of five second level interconnect technologies have been studied. The failure modes and characteristic lives have been examined in finite element simulation and harsh thermal environment testing. Within the electronic package, the second level interconnect is a major area of concern for package reliability. In harsh thermal environments, the second level interconnect will often crack and fail due to CTE mismatch of materials found in the package. In an attempt to abate the damage found in the second level interconnect new interconnect designs are often proposed. Some examples of uniquely diesigned interconnects include elastomer interconnects with particle embedding [Liu 2003], polymer stud grid arrays [Chandraskekhar 2003, Vandevelde 2004], multi-copper column interconnects [Liao 2005], and metal polymer composite interconnects [Aggarwal 2007]. New designs involving plastic core interconnects have shown promising reliability [Okinaga 2001, Galloway 2005, Movva 2004, Whalley 2008] as well as variations on the column grid array (CGA) which include high-lead cores, lead free solder bridging, and copper wire reinforcement [Ghaffarian 2006, Hong 2000, Winslow 2005, Perkins 2003]. With plastic core interconnects it is thought that the more compliant core will reduce the strain in the interconnect allowing for longer package life [Movva 2004, Okinaga2001]. In previous

tests, the plastic core solder ball has shown superior reliability to a normal solder ball [Galloway 2005, Movva 2004]. The same plastic core interconnect is tested in this experiment with detailed failure mode and finite element models. In addition to the polymer core ball, a newly designed copper reinforced column grid array originally proposed by Winslow [Winslow 2005] is tested. The column grid array has an established foundation as being a reliable interconnect for certain applications [Master 1995, Engelmaier 1995]. Recently, attempts to improve the reliability of the standard column grid array have been made. Perkins created a column that had a high-lead core with eutectic fillets for connection to the board [Perkins 2003]. Other researchers have tested lead free column interconnects [Lau 2004, Ghaffarian 2006]. Winslow explains three main column grid array designs and tests a copper reinforced column grid array [Winslow 2005]. In this paper, a copper reinforced high-lead core column grid array package is tested and recreated in the finite element environment. Detailed results on failure mode and characteristic life are given in the pages to follow.

Another interconnect commonly used on ceramic packages is the dual alloy tin lead eutectic high-lead core solder ball. The interconnect has a high-lead sphere that is wetted with a eutectic bridge for connectivity to the component. Past tests have examined failure mode and strain patterns in the dual alloy interconnect [Howieson 2001, Farroq 2003, Hong 1996]. Within the interconnect, the high-lead sphere is more compliant and takes up the majority of the interconnect strain during thermal loading. In this manner, the damage is often found in the eutectic tin lead briding at either the package or board side interface [Howieson 2001]. Recently the dual alloy interconnect has been tested against lead free SAC alloys in harsh thermal environments and shown

poor reliability in comparison [Interrante 2003, Farroq 2003]. Similarly, the dual alloy interconnect is tested in comparison to the lead free Sn3.0Ag0.5Cu (SAC 305) alloy in this study. For our dual alloy interconnect the eutectic tin lead bridging was made much thicker than in past tests [Farroq 2003, Howieson 2001]. By increasing the eutectic bridging the interconnect had a taller standoff height and more area within which to take up the strain induced by thermal cycling. Detailed failure modes and finite element simulations are offered in the pages to follow.

In addition to the interconnect systems presented, a lead free SAC 305 solder ball was used for second level interconnection in one of the test boards. Though the reliability data for lead free alloys is still being developed, a few main things have been determined about the new alloys. Generally, the SAC alloys performance is largely based on package type and thermal profile [Rouband 2001, Syed 2001, Vandevelde 2004]. In addition, the higher silver content lead free alloys exhibit better creep properties than the lower silver content lead free alloys [Schubert 2002, Darveaux 2005, Zhang 2008]. When compared to the standard tin lead eutectic interconnect the lead free solder alloys have generally shown increased reliability [Dai 2005, Rouband 2001, Syed 2001, Lau 2003, Yang 2008]. However, some reports have shown that the SAC alloy will underperform the tin lead eutectic interconnect when under higher stress generated by ceramic packages [Clech 2005]. The results of the test from actual thermal cycling and finite element simulation are given in the pages to follow.

5.2 Test Vehicle and Setup

The boards used in this experiment were composed of a ceramic strip bound to the PCB by way of the interconnects. The ceramic package did not have a silicon chip or copper pads at the solder interface. There were metal traces in the ceramic for daisy chain purposes. The PCB thickness was 2mm. The ceramic strip was 2 mm thick. The pitch was 1 mm for all packages. The packages were 21mm by 21mm. There were 8 packages per board and 400 I/O per package. An image of the board can be seen below in figure 5-1

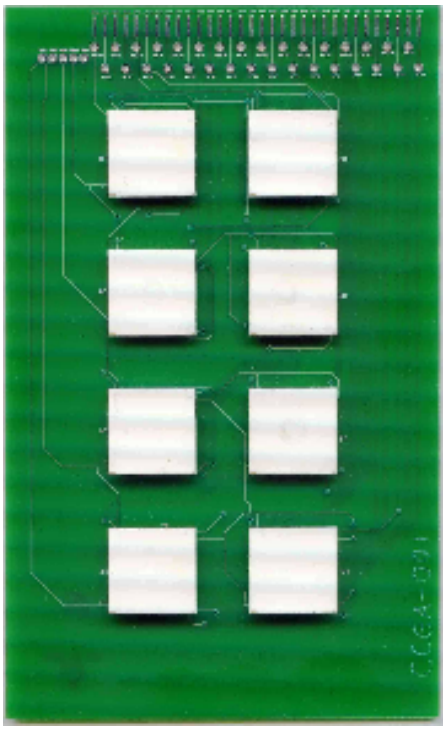

Figure 5-1 Test Vehicle Study 3 Unique I/O Systems

The dimensions of the packages are given in table 5-1 below.

Table 5-1 Unique I/O Board Dimensions

Size	21X21 mm
Pitch	1 mm
I/O	400
PCB Thickness	2 mm
Ceramic Thickness	2.5 mm

All of the packages were daisy chained and continuously resistance monitored using a switch box and multimeter. Any failure is denoted by a 10% rise in resistance wherein the resistance permanently stays 10% or greater after initial failure. The thermal cycle went from -55 to 125 Celsius with 15 minute dwells and 35 minute ramps giving a 100 minute cycle time. The thermal profile was mapped with SlimKic software and can be seen below in figure 5-2

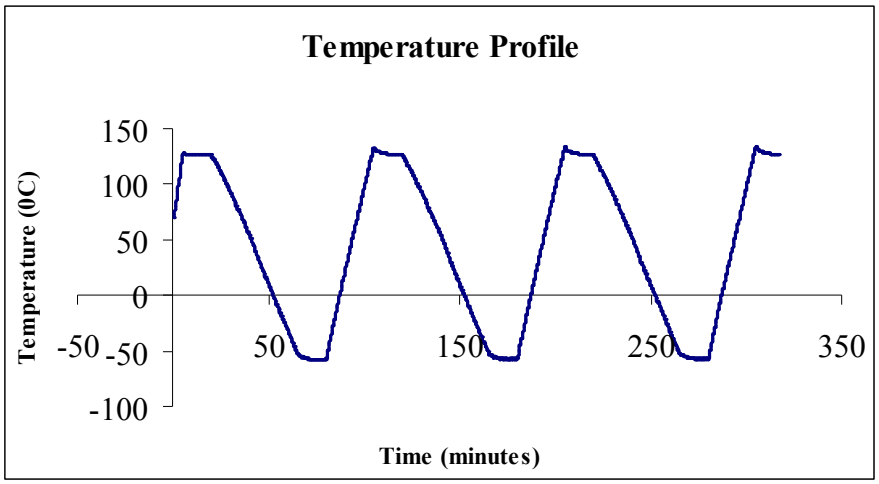

Figure 5-2 Thermal Profile Unique I/O Test

5.3 SOL Plastic Core I/O

The interconnect is a plastic core encased by a spherical copper shell and then encapsulated in a eutectic solder alloy. The plastic core is approximately 1/3 the young's modulus of a typical solder alloy, allowing for a much more compliant interconnect. The plastic core is intended to act as a buffer against the strain induced in the interconnect. In this manner, the plastic core will relieve most of the strain [Movva 2004]. These interconnects have a higher standoff height from traditional solder balls. This feature also adds to the reliability of the SOL interconnect [Galloway 2005]. Okinaga tested a similar interconnect in his 2001 paper. His interconnect had a thinner copper ring and solder layer and showed superior reliability to the standard eutectic solder ball. In Okinaga's paper, the failure was seen in the middle of the interconnect as a crack through the solder encapsulate and copper ring [Okinaga 2001]. Movva showed a similar failure mode with the crack propagating through the middle of the interconnect causing separation in the copper ring and eutectic encapsulate [Movva 2004]. Galloway demonstrated a different failure mode in an interconnect that had a thicker eutectic casing where the crack occurred in the eutectic solder at the package side interface [Galloway 2005]. The results form our thermal cycling tests showed a failure mode where the cracking and damage occurred at the top of the interconnect. An image of the interconnect can be seen in figure 5-3 below

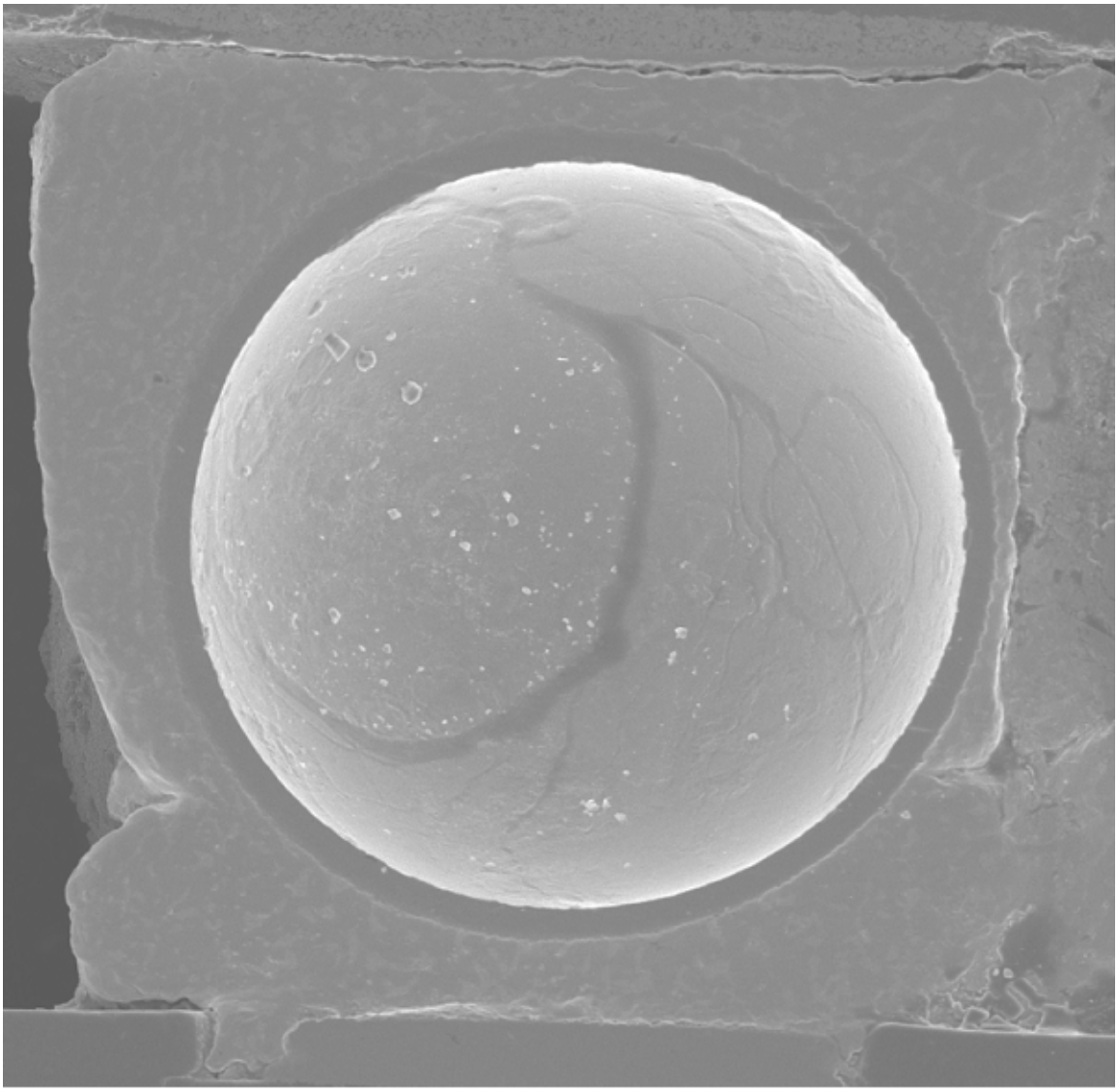

Figure 5-3 SOL Interconnect

Figure 5-3 shows the plastic sphere, the copper ring, and the eutectic tin lead encasing.

In figure 5-4 below a schematic of the package construction is shown.

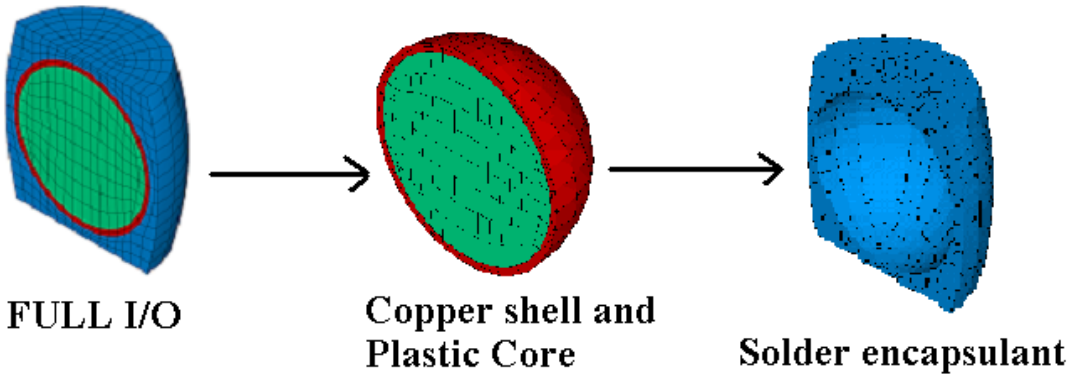

Figure 5-4 Schematic of SOL Interconnect construction

The dimensions of the package are given below in table 5-2.

Table 5-2 Package Dimensions SOL I/O

Plastic Sphere Diameter	.5mm
Copper Ring Thickness	.02mm
63Sn37Pb Thickness	.03mm
Solder Joint Height	.6mm
Pad Diameter	.52mm

The interconnect was subjected to harsh thermal -55 Celsius to 125 Celsius in a 100 minute cycle with 15 minute dwells and 35 minute ramps presented in section 5.2 The interconnect experienced early failures in many of the joints. The Weibull plot below in figure 5-5 shows the reliability of the SOL interconnect.

Figure 5-5 Weibull Plot SOL I/O

The SOL interconnect was the weakest of the five interconnects tested with a characteristic life of 518 cycles, an N1% life of 38 cycles and a slope of 1.76. The interconnect failed much faster than expected and much quicker than previous reports have shown. An image of a failed solder ball can be seen below in figure 5-6.

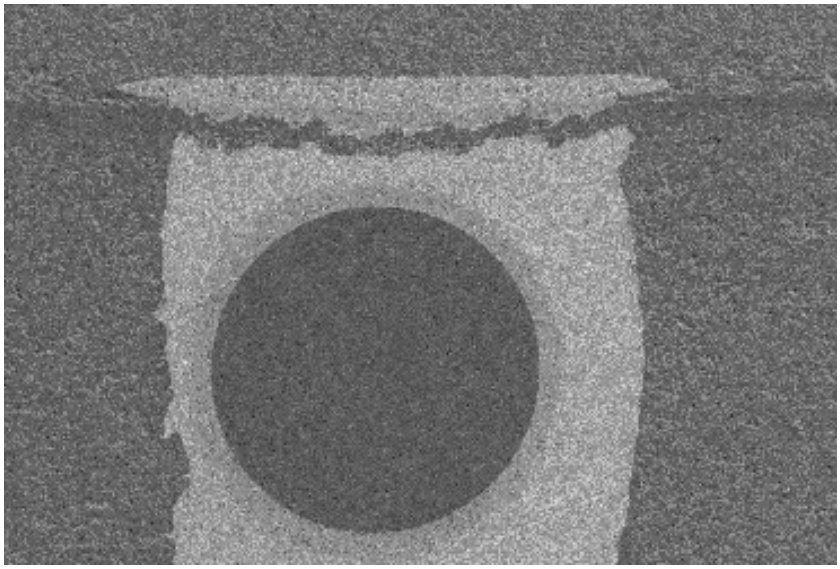

Figure 5-6 Failed SOL I/O

As figure 5-6 shows, cracking occurred at the top of the interconnect package interface and propagated throughout the eutectic solder until the interconnect had lost connection with the ceramic strip. No damage is seen in the lower parts of the interconnect at the copper ring. Another failure image in figure 5-7 below shows some amount of damage at the top of the interconnect in the copper ring region.

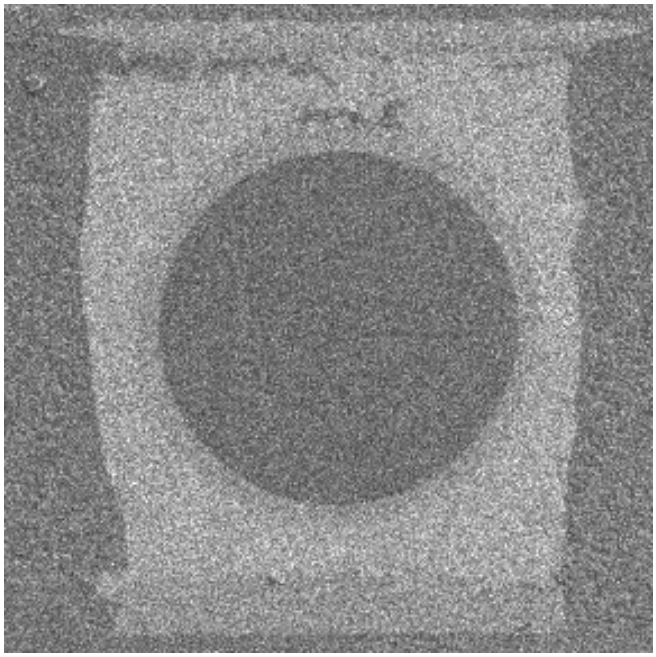

Figure 5-7 Top Cracking SOL I/O

Figure 5-7 shows damage at the top of the copper ring above the plastic core. Much like figure 5-6 the damage occurs in the top part of the eutectic encasing. During cross sectioning, some packages were seen that had damage at the top of the copper ring and others were seen where there was no damage at the copper ring. The primary failure mode was cracking at the top of the interconnect through the top eutectic layer above the plastic core. [Galloway 2005] reported similar failure results. Others, [Okinaga 2001], had shown cracking to occur in the middle of the solder ball through the copper ring and eutectic encasing. The copper ring loses its purpose if the crack occurs at the top of the

interconnect as connectivity is lost in this case. The finite element model showed similar failure results.

5.3.1 SOL Finite Element Model

The package was recreated in ANSYS finite element model environment. The same modeling procedure as presented previously was used for all of the packages in this experiment. The material properties of the package can be seen below in table 5-3. The Anand constants for 63Sn37Pb were used in the model.

Table 5-3 SOL Finite Element Material Properties

Component	E GPa	α ppm/°C	υ
PCB	17(x,z) 7(y)	15(x,z) 67 (y)	.39
Plastic Core [Hande 2008]	9	20	.38
63Sn37Pb	30	24	.35
Solder Mask	3	30	.3
Ceramic strip	27	6.7	.3
Copper	128	16	.34

Table 5-3 shows the compliance of the plastic core interconnect compared to the standard tin lead eutectic solder as its young's modulus is approximately 1/3 that of the 63Sn37Pb solder. Figure 5-8 shows a diagonal view of the SOL package. Figure 5-9 below shows the finite element model of the plastic core interconnect. Figure 5-10 below that shows a dimensioned image of the finite element model.

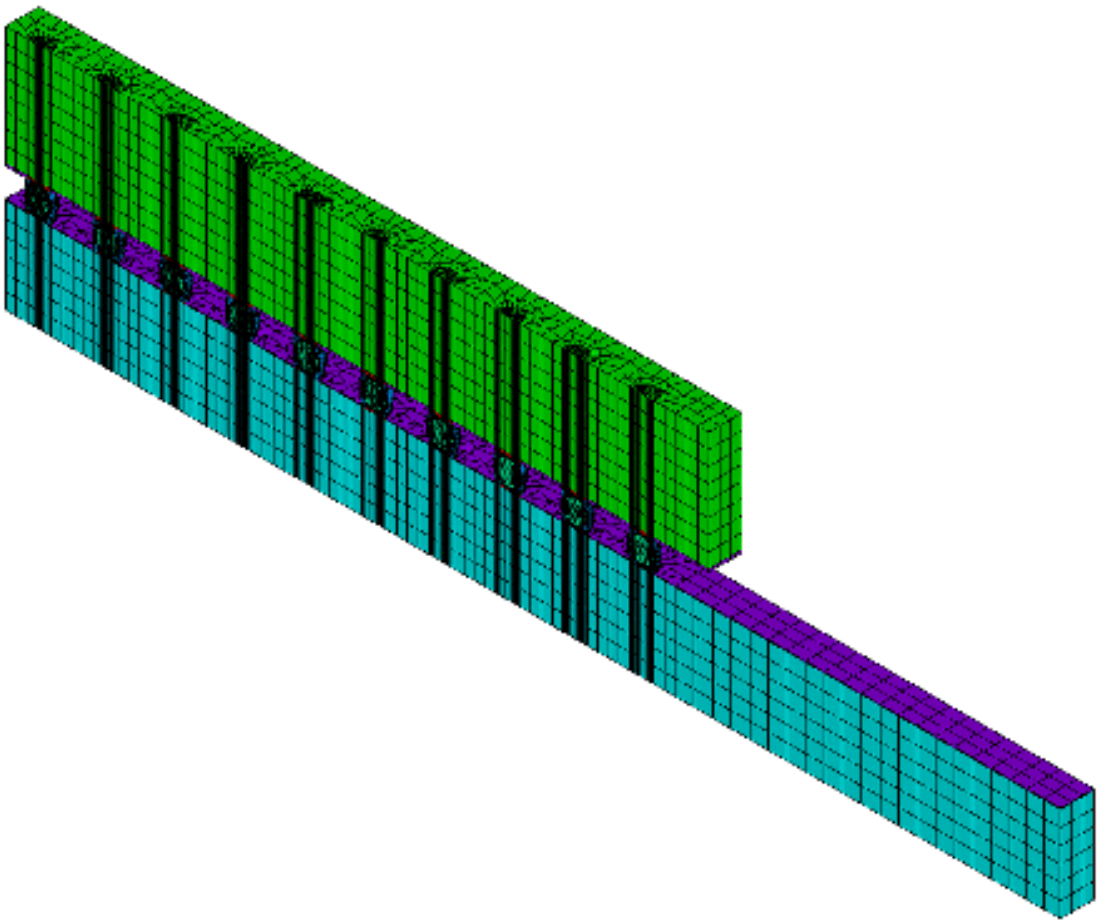

Figure 5-8 Diagonal view SOL finite element model

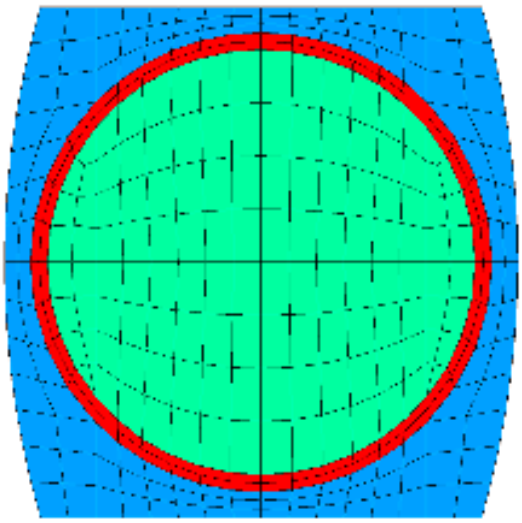

Figure 5-9 Finite Element Model SOL I/O

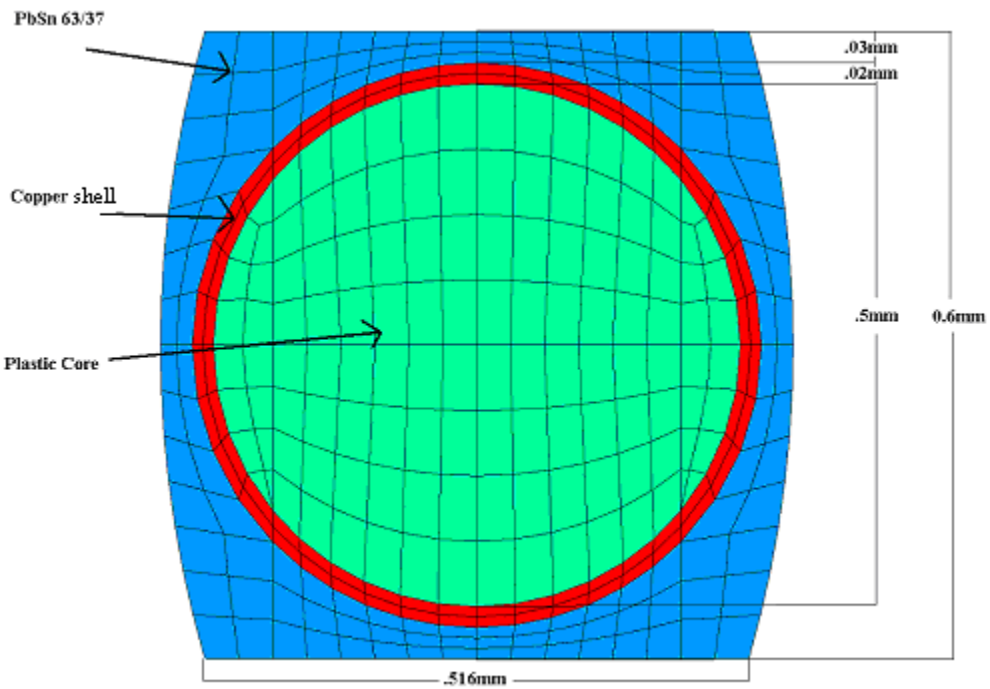

Figure 5-10 Dimensioned SOL Finite Element Model

The simulation showed similar failure modes to those seen in actual thermal testing. Figure 5-11 shows the damage from simulation. The corner ball was the first ball and showed maximum damage in simulation as was expected as the package did not have a silicon die and the distance to neutral point formula was the dictating stress accumulation rule in the package.

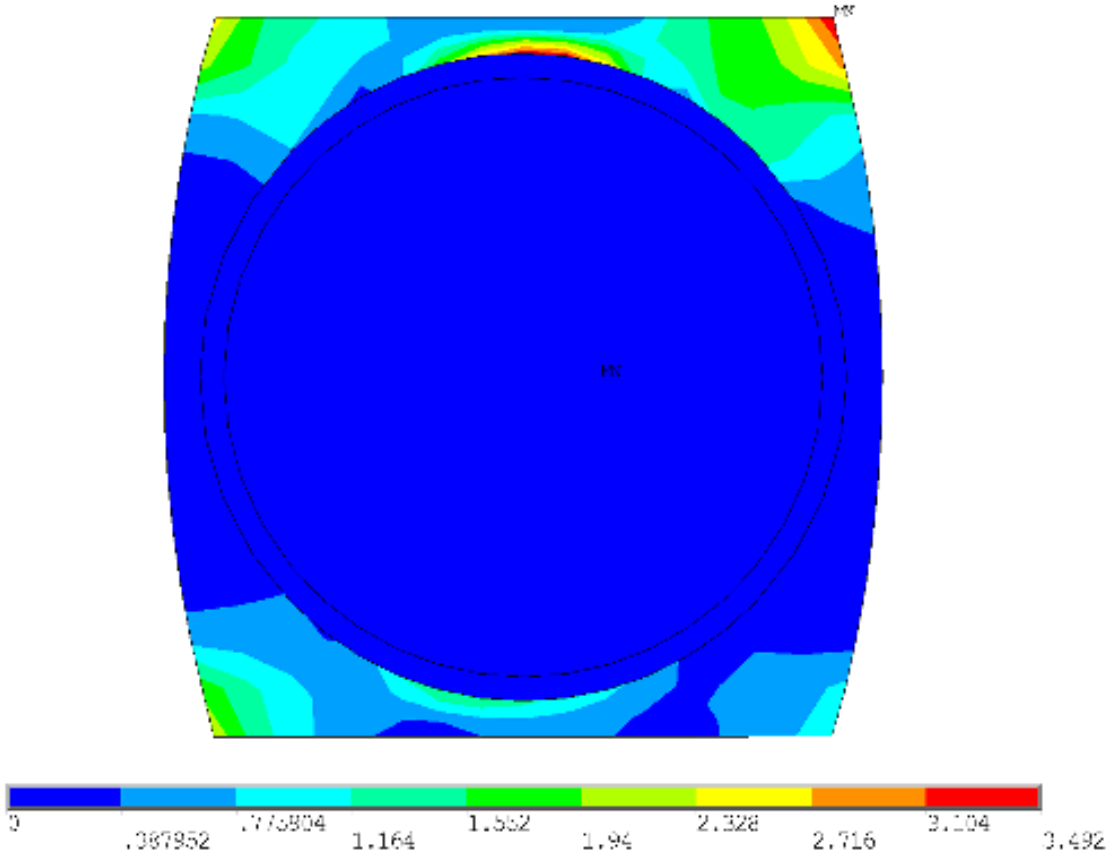

Figure 5-11 Failed Finite Element Model SOL I/O

Figure 5-11 shows maximum damage in the top right hand corner of the interconnect at the ceramic interface. There is also a large amount of damage seen at the top of the copper ring. There is some damage seen in the lower parts of the interconnect, but not as much as at the ceramic interface. No damage is seen through the middle of the interconnect. The failure mode shown by figure 5-11 closely tracks the damage seen in figure 5-7, where cracking can be seen at the top of the copper ring and the top right hand corner of the interconnect. Figure 5-12 and figure 5-13 below show the hysteresis loop and plastic work of the package from simulation.

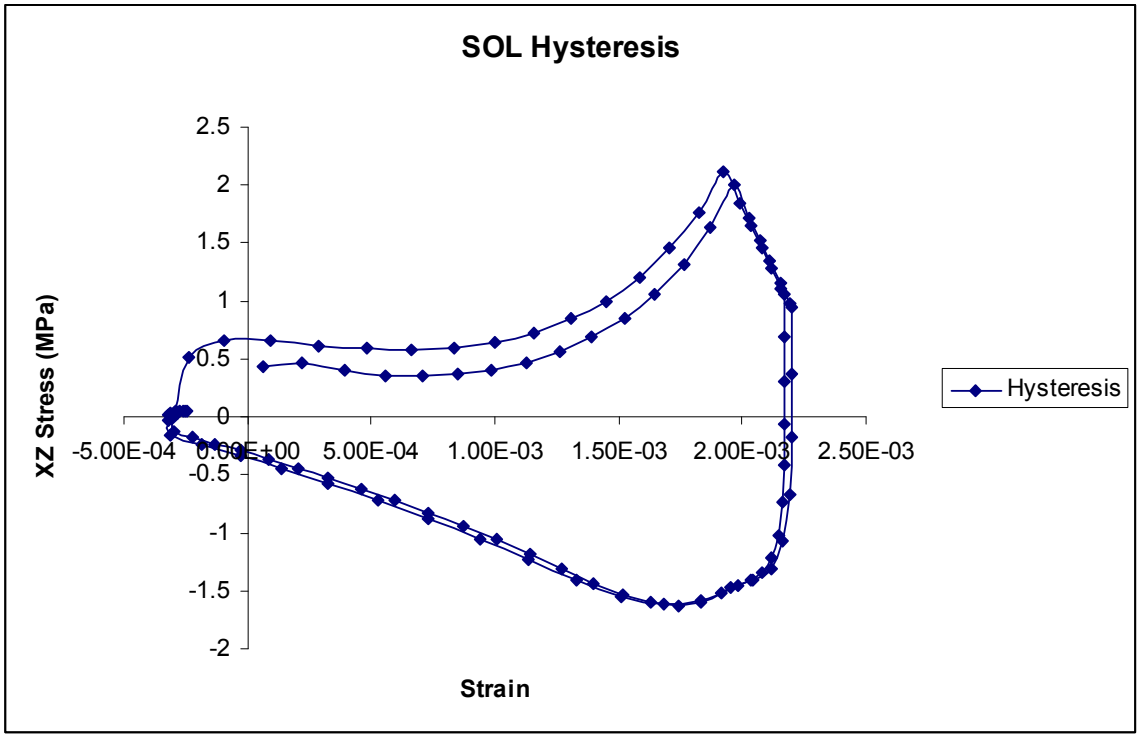

Figure 5-12 Hysteresis Loop SOL interconnect

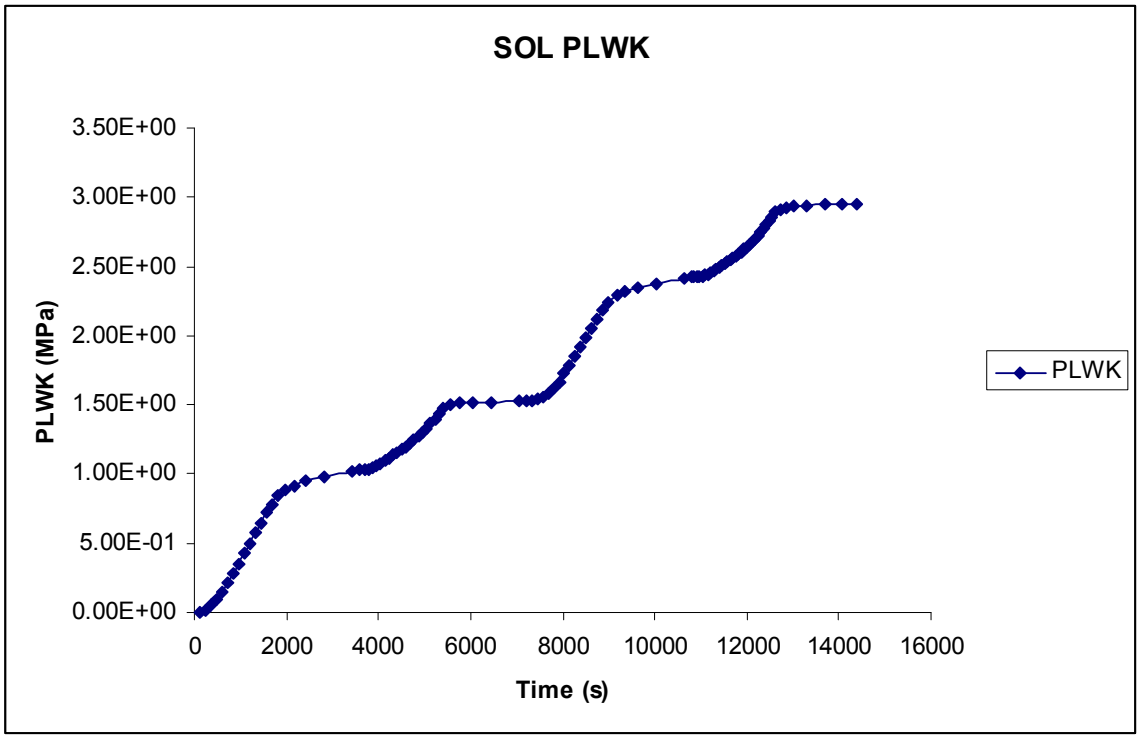

Figure 5-13 Plastic Work SOL interconnect

Figure 5-12 above shows stabilization of the simulation after two cycles. In figure 5-13, the plastic work of the package is plotted. The plastic work tops out at 3 MPa at the end of the cycle. The life prediction equations presented in equations 3.9 and 3.10 were used for this package and all other packages in this experiment. The package showed good life correlation as is shown below in table 5-4.

Table 5-4 SOL Life Correlation

SOL	Characteristic Life (η)	Error
Experiment	518 cycles	19%
Simulation	646 cycles	

The simulation closely tracked the experiment having showing a simulated life of 646 cycles while the experiment showed 518 cycles. The life correlation showed a 19% error. Overall, the package did not perform as well as expected. As mentioned, it was the worst of all the interconnects tested. Previous results have shown superior performance of a plastic core interconnect, but this experiment did not.

5.4 CCGA

The column grid is an interconnect commonly used in ceramic packages as it's increased standoff height offers better reliability in comparison to a standard solder ball. It is reported that the stress in the interconnect reduces as a square of the height [Winslow 2005]. Lately, attempts at making the column grid more reliable have been made including using a copper ribbon to reinforce the column, using copper core interconnects, and using high-lead, compliant cores in an attempt to reduce stress [Winslow 2005, Interrante 2003, Perkins 2003]. In this test, an interconnect featuring a high-lead SnPb core is spiral wrapped with a copper ribbon and then encased in a eutectic tin lead solder.

The interconnect features a taller standoff height than the typical solder ball interconnect, has a compliant high-lead core, and uses a copper ribbon for reinforcement purposes. It is expected that the high-lead core will relieve strain in a manner similar to that proposed for the plastic core solder ball. The copper ribbon is expected to maintain conductivity even if the interconnect cracks throughout the center of the column as has been the failure mode seen in previous tests [see Perkins 2003]. An SEM image of the interconnect can be seen below in figure 5-14.

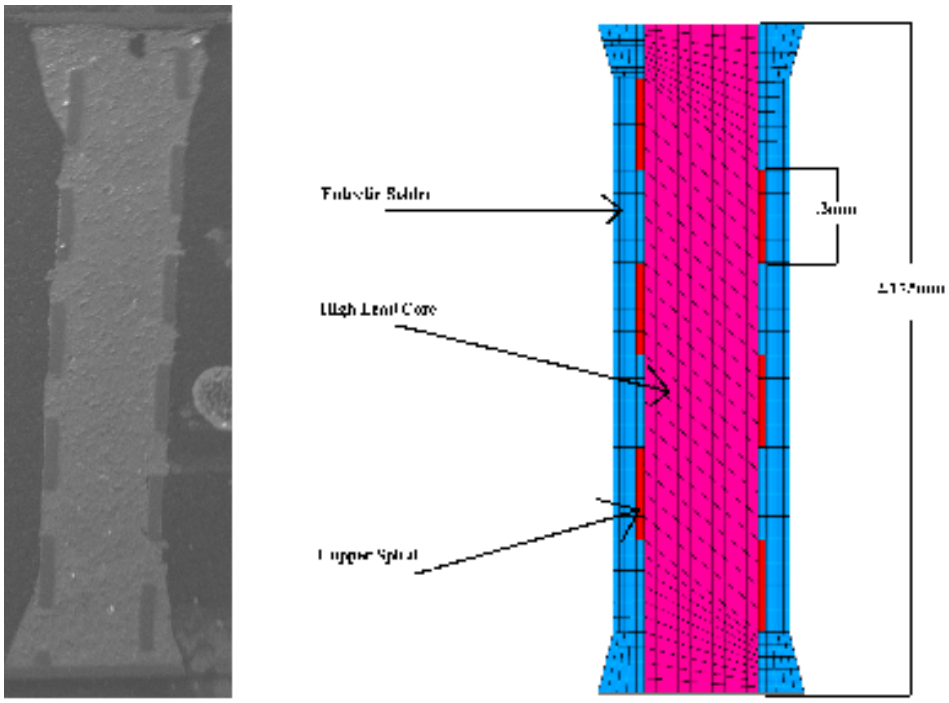

Figure 5-14 CCGA Interconnect

A schematic of the interconnect can be seen below in figure 5-15 demonstrating construction of the interconnect.

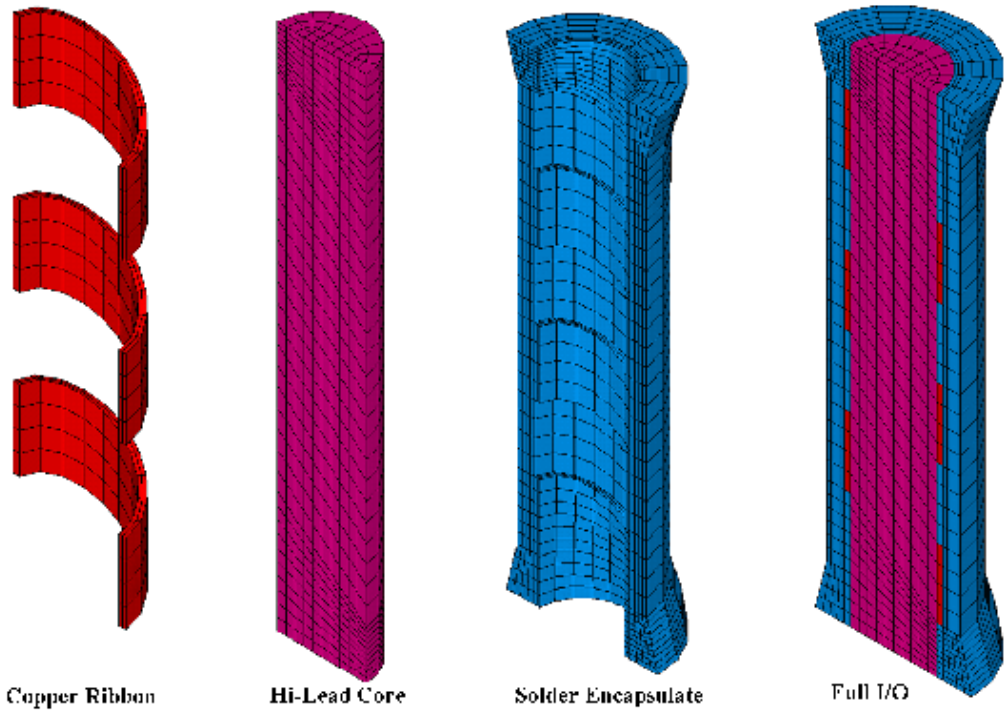

Figure 5-15 CCGA I/O Construction

As Figure 5-15 shows, the copper ribbon is placed around the pink high-lead core and the solder encapsulate encases the assembly. The dimensions of the interconnect are give below in table 5-5.

Table 5-5 CCGA Dimensions

Solder Joint Height	2.175mm
Copper Ribbon Thickness	.025mm
High-lead core radius	.1875mm
Eutectic thickness	.15mm
Pad Diameter	.675mm

The package was tested in the harsh thermal environment presented in section 5.2. The package showed the best characteristic life of all the packages tested on the unique I/O test board. The Weibull plot for the interconnect is presented below in figure 5-16.

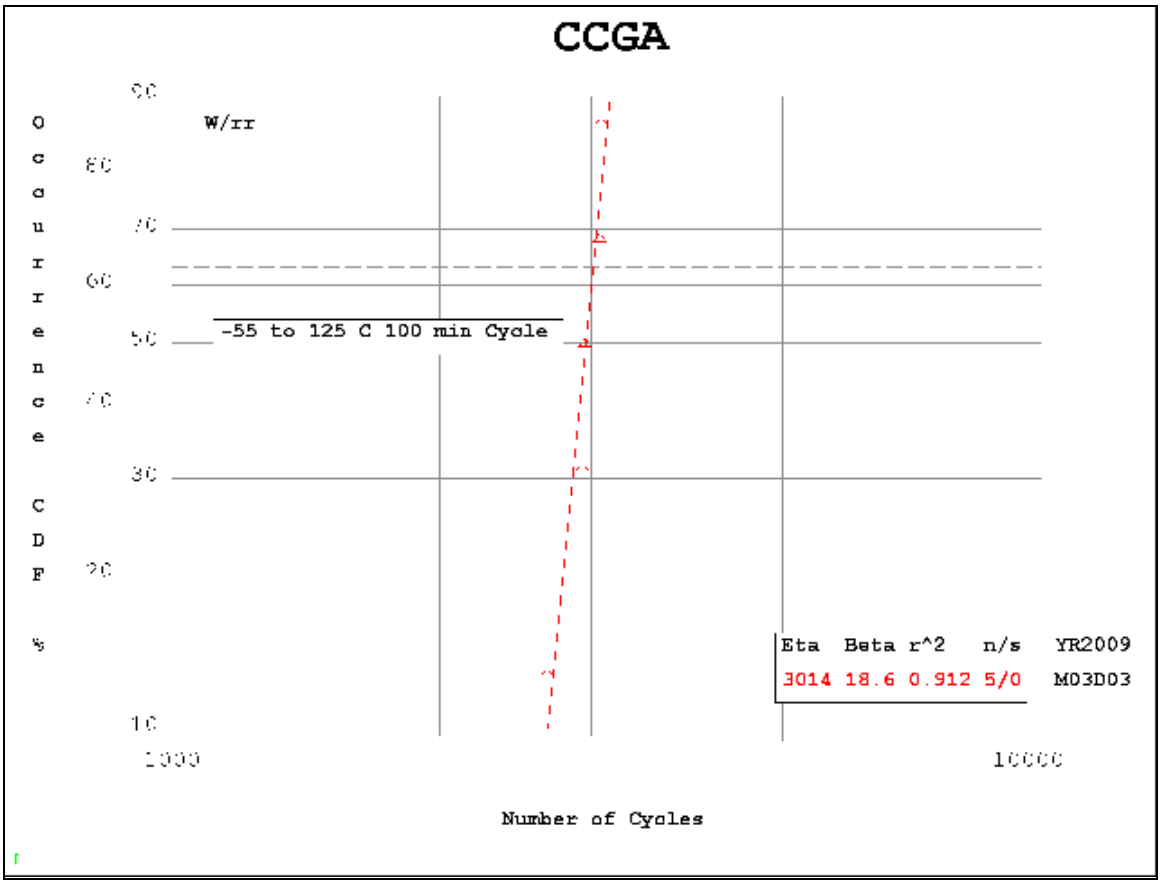

Figure 5-16 CCGA Weibull Plot

Figure 5-16 shows a characteristic life of 3,014 cycles. The N1% life is 2,353 cycles. The β is 18.6, which is a very steep slope implying that all of the packages failed at about the same cycle count. Figure 5-17 below shows a failed interconnect from SEM imaging.

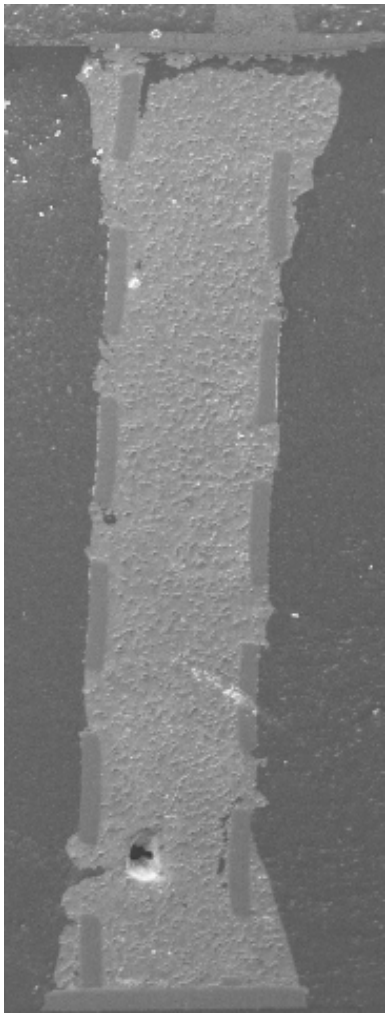

Figure 5-17 Failed CCGA SEM

Figure 5-17 shows cracking at the top of the interconnect at the ceramic interface. Some damage is seen in the lower part of the interconnect at the copper ribbon, but the mode of failure is crack propagation at the top of the interconnect. The copper ribbon held the interconnect together throughout the middle of the interconnect and at the fillet where the high-lead and eutectic solder interface. As a result of the copper ribbon reinforcement, the failure mode shifted to the top of the interconnect. Figure 5-18 below shows several more interconnects with the same failure mode.

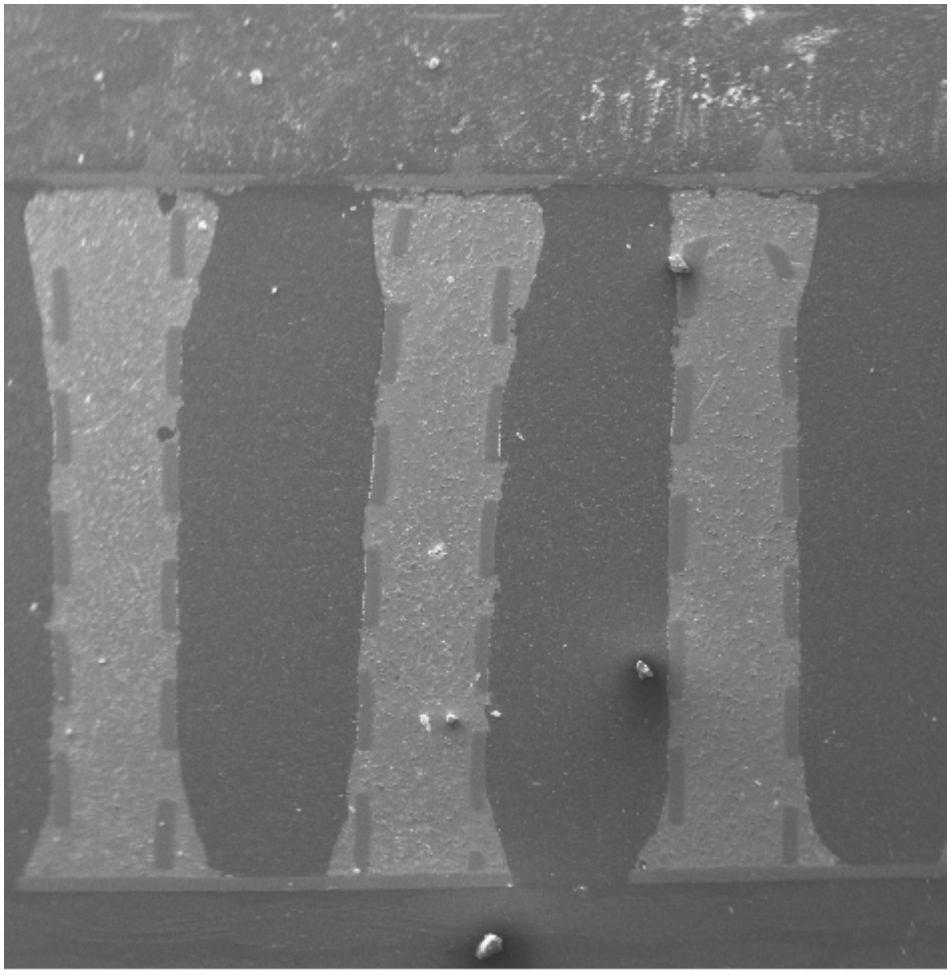

Figure 5-18 Failed CCGA SEM

Figure 5-18 shows three interconnects with the same failure mode, crack growth at the top of the interconnect. In these three interconnects, no damage is seen in any other areas other than the top portion of the interconnect.

5.4.1 CCGA Finite Element Model

The package was recreated in ANSYS finite element environment and the thermal environment simulated. The same method for plastic work calculation as used in Chapter 3 and Chapter 4 were used here. The elements in the region of maximum damage were

selected for volume averaged plastic work calculations. Figure 5-19 below show a diagonal view of the CCGA package. Figure 5-20 below that shows a dimensioned picture of the CCGA interconnect.

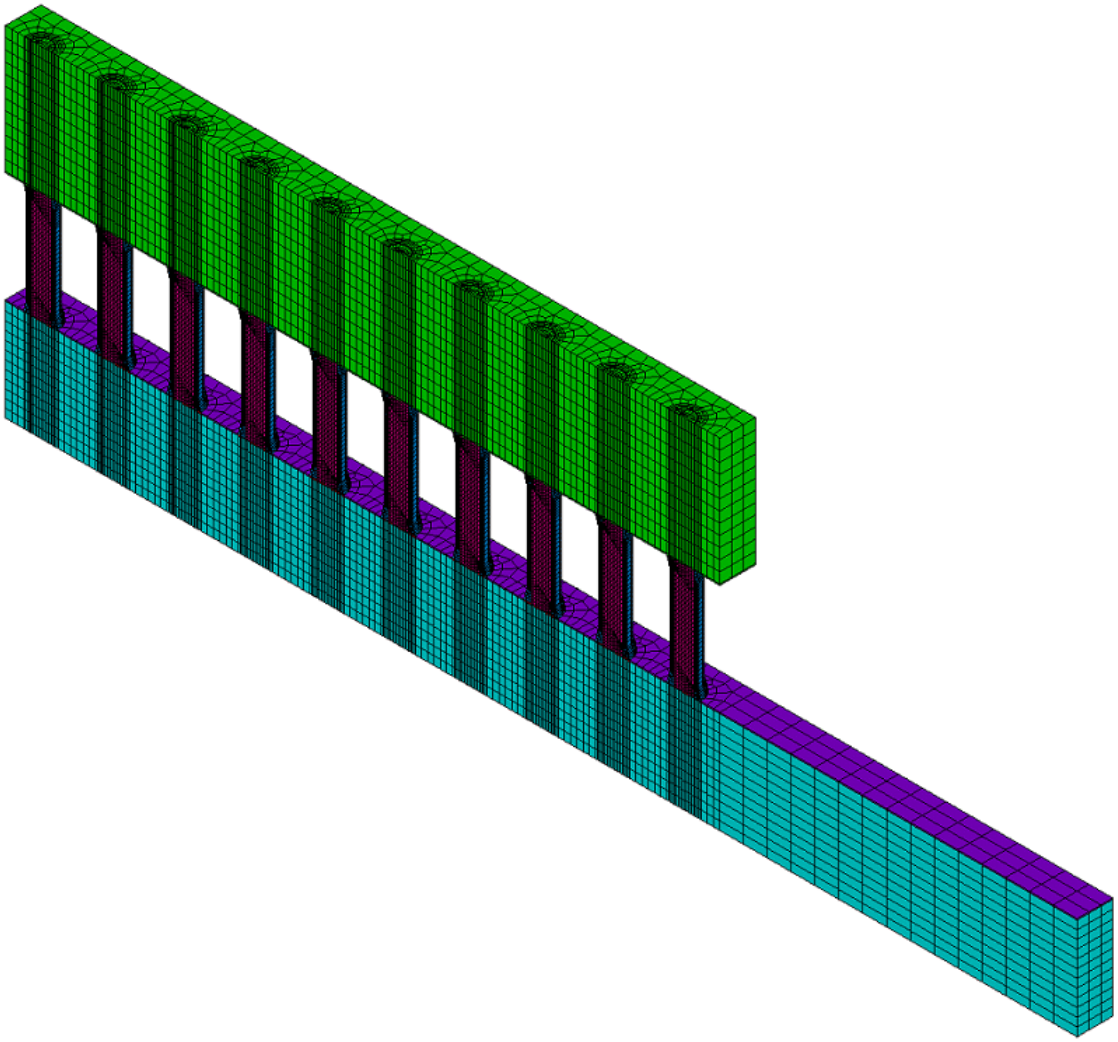

Figure 5-19 Diagonal View CCGA Model

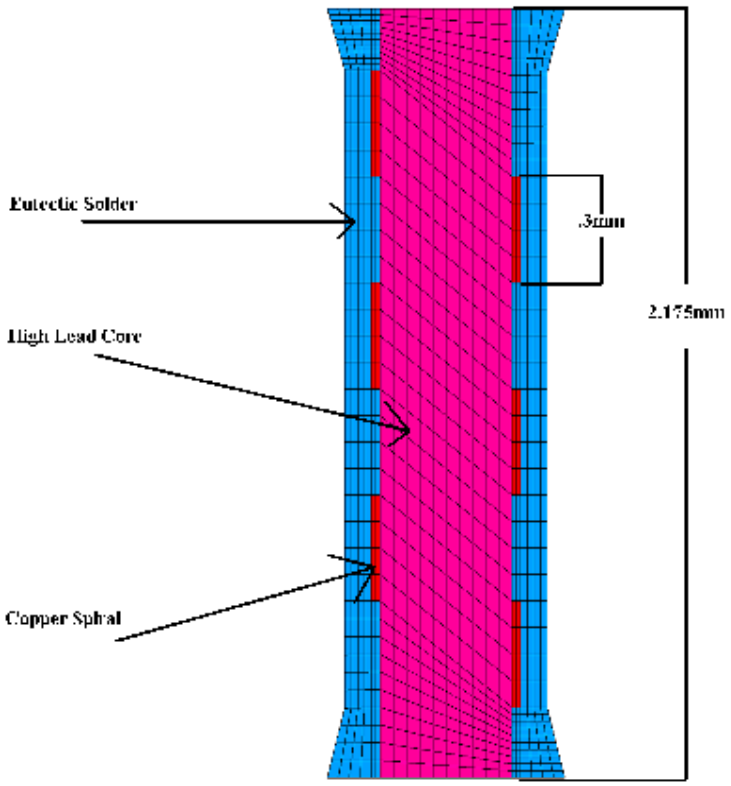

Figure 5-20 Dimensioned CCGA I/O

Figure 5-21 below shows the copper ribbon wrapped around the high-lead core.

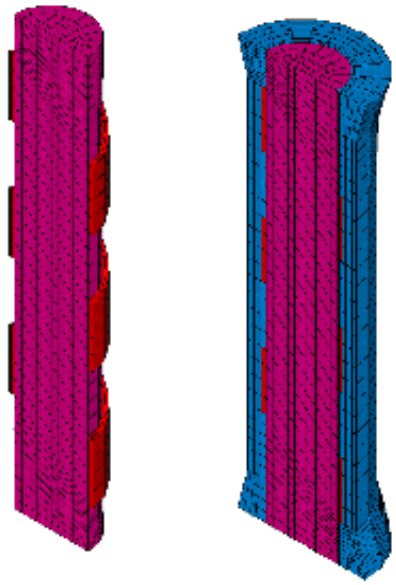

Figure 5-21 Copper Spiral around high-lead core.

The material properties for the package are shown below in table 5-6

Table 5-6 CCGA Material Properties

Component	E GPa	α ppm/°C	υ
PCB	17(x,z) 7(y)	15(x,z) 67 (y)	.39
Substrate	276	6.7	.3
Eutectic SnPb	30	24	.35
Solder Mask	3	30	.3
90Pb10Sn	19	27.6	.31
Copper	128	16	.34

The high-lead 90Pb10Sn Anand constants are presented below in table 5-7.

Table 5-7 90Pb10Sn Anand Constants [Hande 2008]

90Pb10Sn Anand constants	
S_o	4.72 (MPa)
Q/k	76231 $\left(1/K\right)$
A	7,073 $\left(1/\text{sec}\right)$
ζ	5.21
m	.27
h_o	33,884(MPa)
n	.019
a	2.05
$\hat{s}$	25.75(MPa)

The simulation results showed similar damage to that seen in cross sectioning of the package. Figure 5-22 below shows damage accruing in the top right hand corner of the interconnect at the ceramic interface.

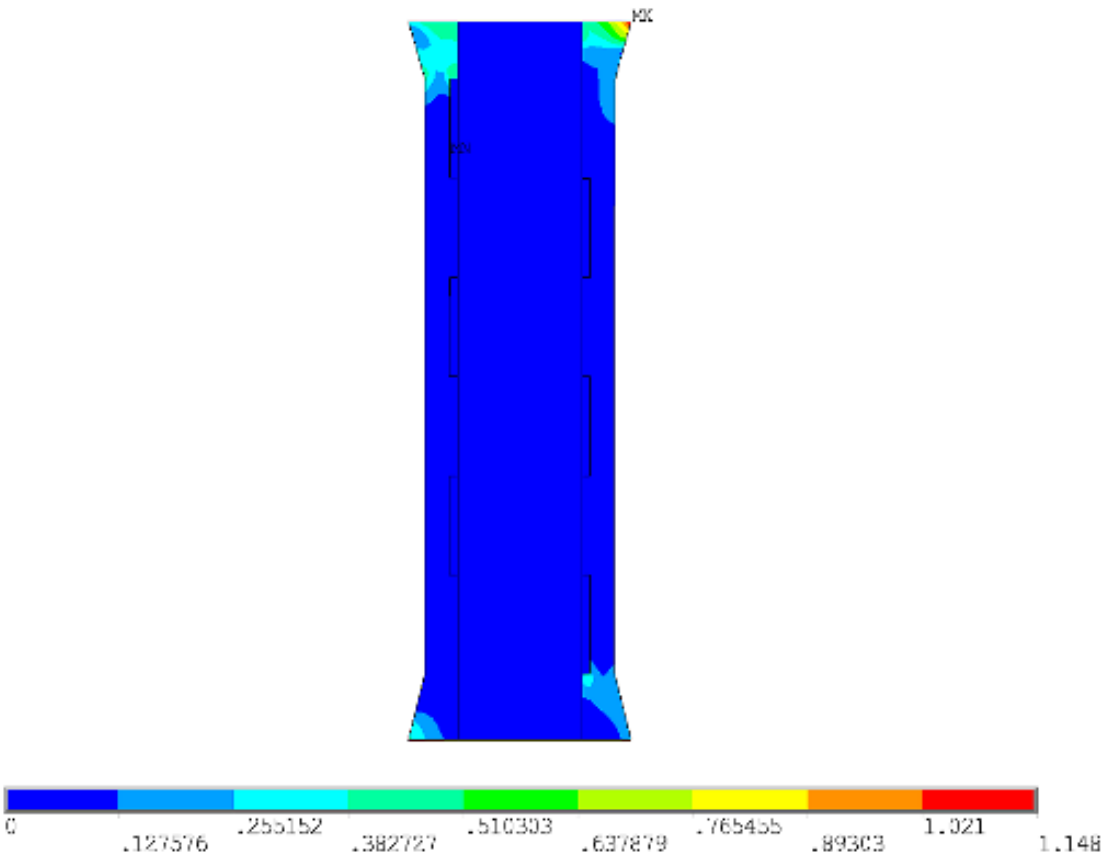

Figure 5-22 Failed CCGA FEM

Similarly to the SOL package, the corner interconnect was the first to fail and saw the most damage. Figure 5-22 shows maximum damage at the top right corner and minimal damage in the lower portion of the interconnect near the copper ribbon. The hysteresis plot for the package can be seen in figure 5-23 below and the plastic work for the package is shown in figure 5-24.

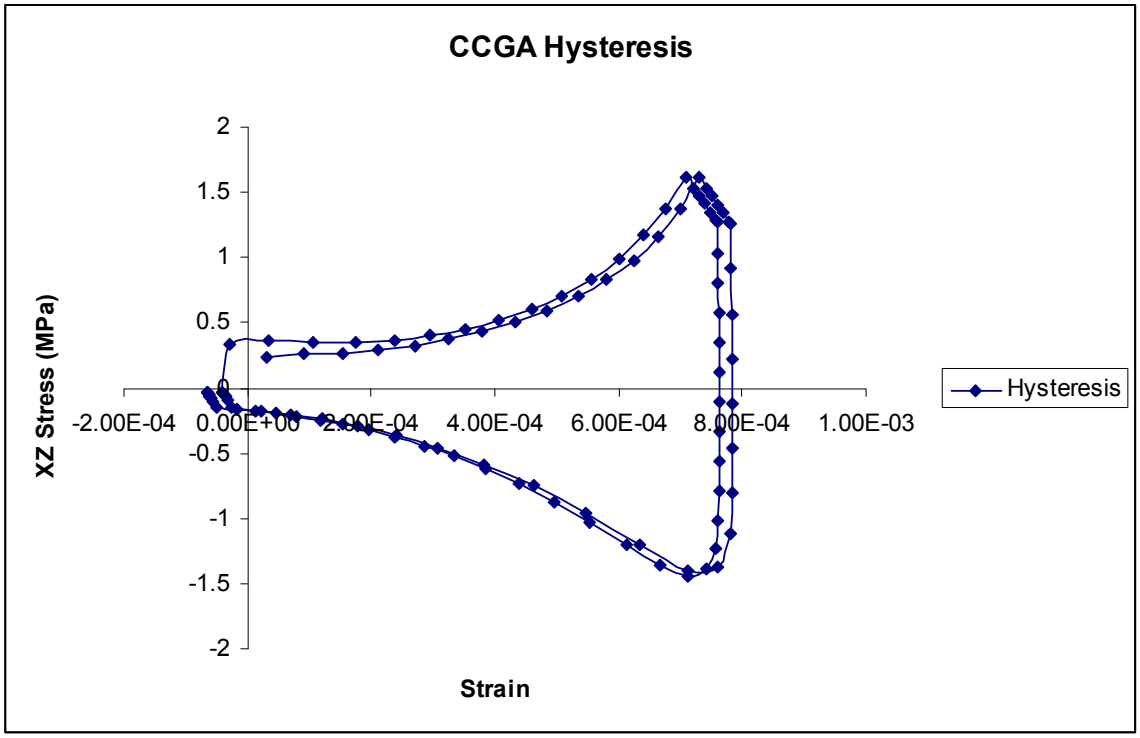

Figure 5-23 CCGA Hysteresis Plot

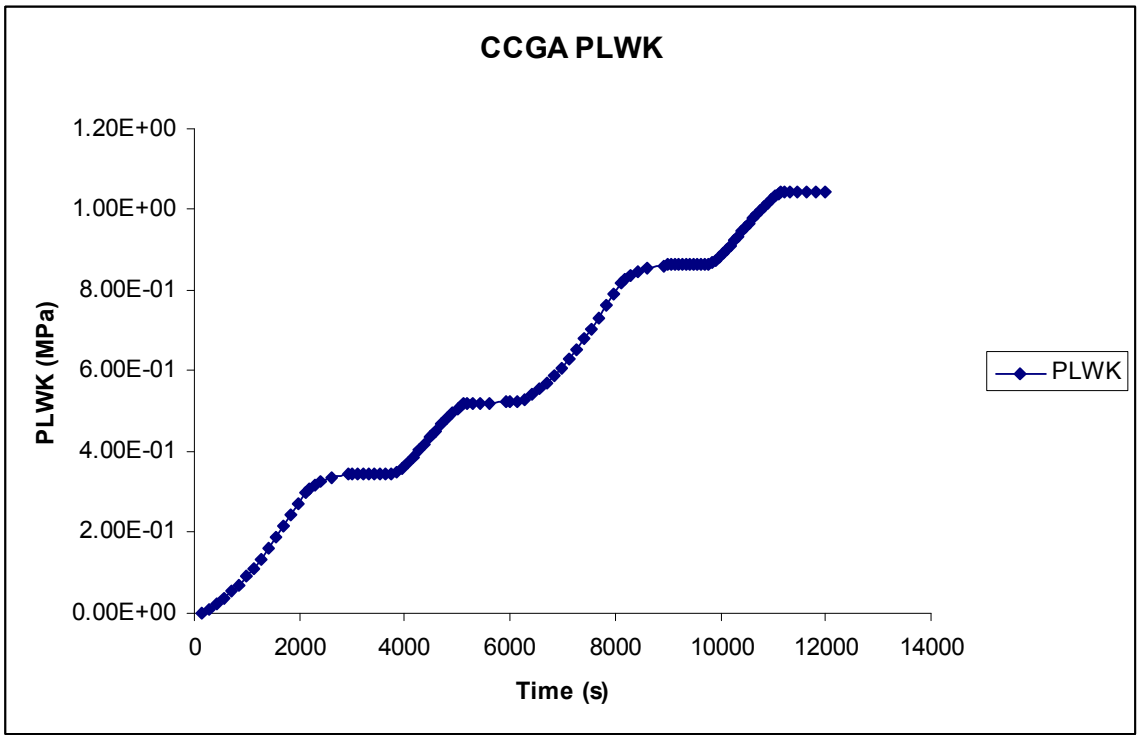

Figure 5-24 CCGA Plastic Work Plot

Figure 5-23 shows stabilization after two thermal cycles. The plastic work shown in Figure 5-24 approaches 1.1 MPa. This is less than the 3 MPa plastic work seen in the SOL interconnect. The package offered good life correlation both in predicted life and the failure mode presented previously. The life correlation can be seen below in table 5-8

Table 5-8 CCGA Characteristic Life

CCGA	Characteristic Life (η)	Error
Experiment	3,023 cycles	20%
Simulation	2,417 cycles	

Table 5-8 shows a simulated life of 2,417 cycles compared to the actual experimental life of 3,023 cycles. The simulation reported a 20% error. The CCGA package greatly outperformed the SOL package and nearly doubled the life of the tin lead eutectic. Table 5-9 below demonstrates the different characteristic lives of the three packages.

Table 5-9 Characteristic Life Comparison

Package	η
CCGA	3,014
SOL	518
63Sn37Pb	1,754

Table 5-9 shows that the CCGA has an approximately 6X life improvement over the SOL package.

5.5 High-lead Interconnect

The next model was a high-lead core solder interconnect with a eutectic bridge at the top and bottom. The core consists of a 90Pb10Sn alloy while the bridging solder is a standard 63Sn37Pb eutectic solder. The idea here is similar to those presented previously

for dual alloy CBGA packages. The lower youngs modulus core will add compliance to the interconnect, acting as a strain buffer, and minimizing the amount of strain incurred in the eutectic solder. In this model the eutectic bridge at the top was significantly wider than the bridge at the bottom of the interconnect. The eutectic bridging is significantly thicker than that typically found in previous CBGA dual alloy designs. Past tests have examined failure mode and strain patterns in the dual alloy interconnect [Howieson 2001, Farroq 2003, Hong 1996]. Within the interconnect, the high-lead sphere is more compliant and takes up the majority of the interconnect strain during thermal loading. In this manner, the damage is often found in the eutectic tin lead briding at either the package or board side interface [Howieson 2001]. Figure 5-25 below shows an SEM image of a high-lead interconnect.

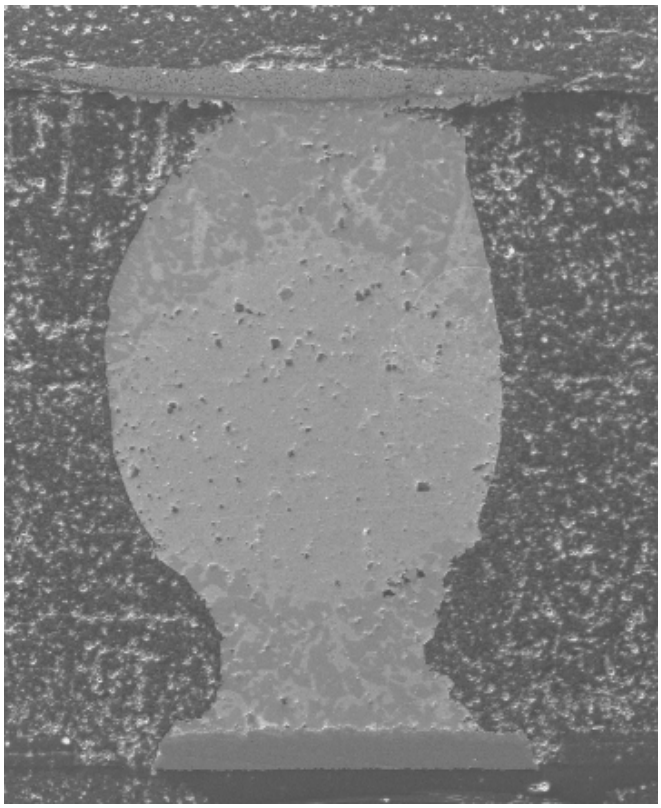

Figure 5-25 High-lead Interconnect

Two different regions of solder can be seen. The lighter grey, round center is a high-lead core. The darker colored solder along the top and bottom is the eutectic tin lead solder. This image was taken after thermal cycling. The core consists of a 90Pb10Sn alloy while the bridging solder is a standard 63Sn37Pb eutectic solder. In figure 5-25 it can be seen that the eutectic bridge at the top was significantly wider than the bridge at the bottom of the interconnect. This image was taken after thermal cycling and apparently some amount of warping has occurred in the board distorting the interconnects. Normally, the high-lead interconnects do not appear this stretched out. The eutectic bridging is significantly thicker than that typically found in previous CBGA dual alloy designs. The dimensions of the interconnect can be seen below in table 5-10.

Table 5-10 High-lead Dimensions

Ball Diameter	.52mm
Eutectic Thickness	.21mm
Pad Diameter	.51mm
Joint Height	.95mm

On top of the compliant high-lead core, the interconnect offers a taller standoff height which adds to the reliability of the interconnect. The package was submitted to the thermal environment presented in section 5.2. The package performed well as the Weibull plot in figure 5-26 shows.

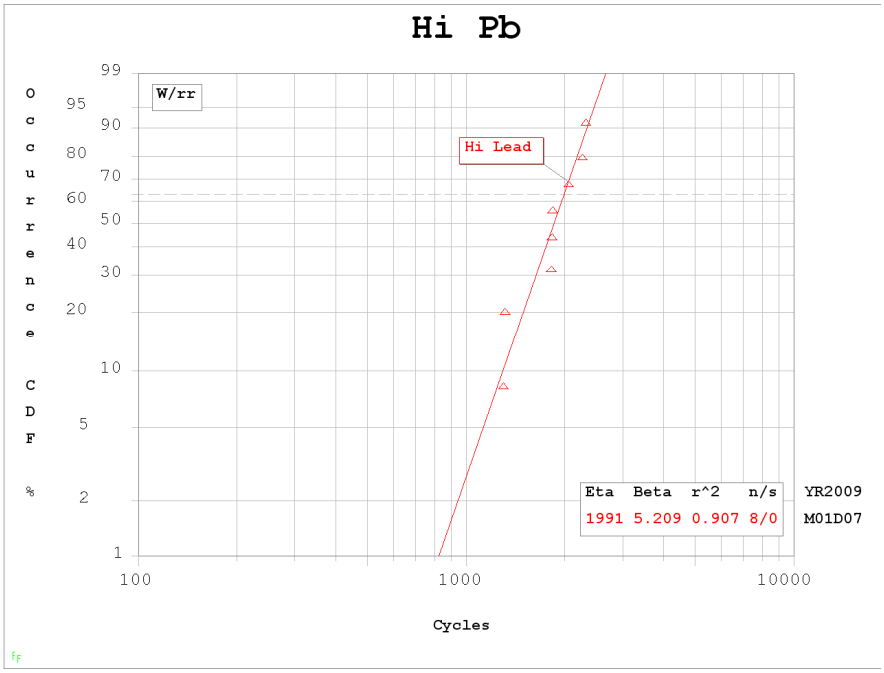

Figure 5-26 High-lead Weibull Plot

Figure 5-26 shows a characteristic life of 1,991 cycles, an N1% life of 823 cycles and a β of 5.2. This package held up well outperforming the SOL package presented earlier. Figure 5-27 below shows an SEM image of a failed interconnect from cross sectioning. Figure 5-27 shows a clear crack across the top of the interconnect where the eutectic solder interfaces with the ceramic package. Failure was seen when the crack had propagated through the interconnect. The corner interconnect was the first to fail in experimentation as expected from the distance to neutral point formula. Little to no damage is seen in other areas of the interconnect, though a crack through the lower eutectic bridging can also be seen.

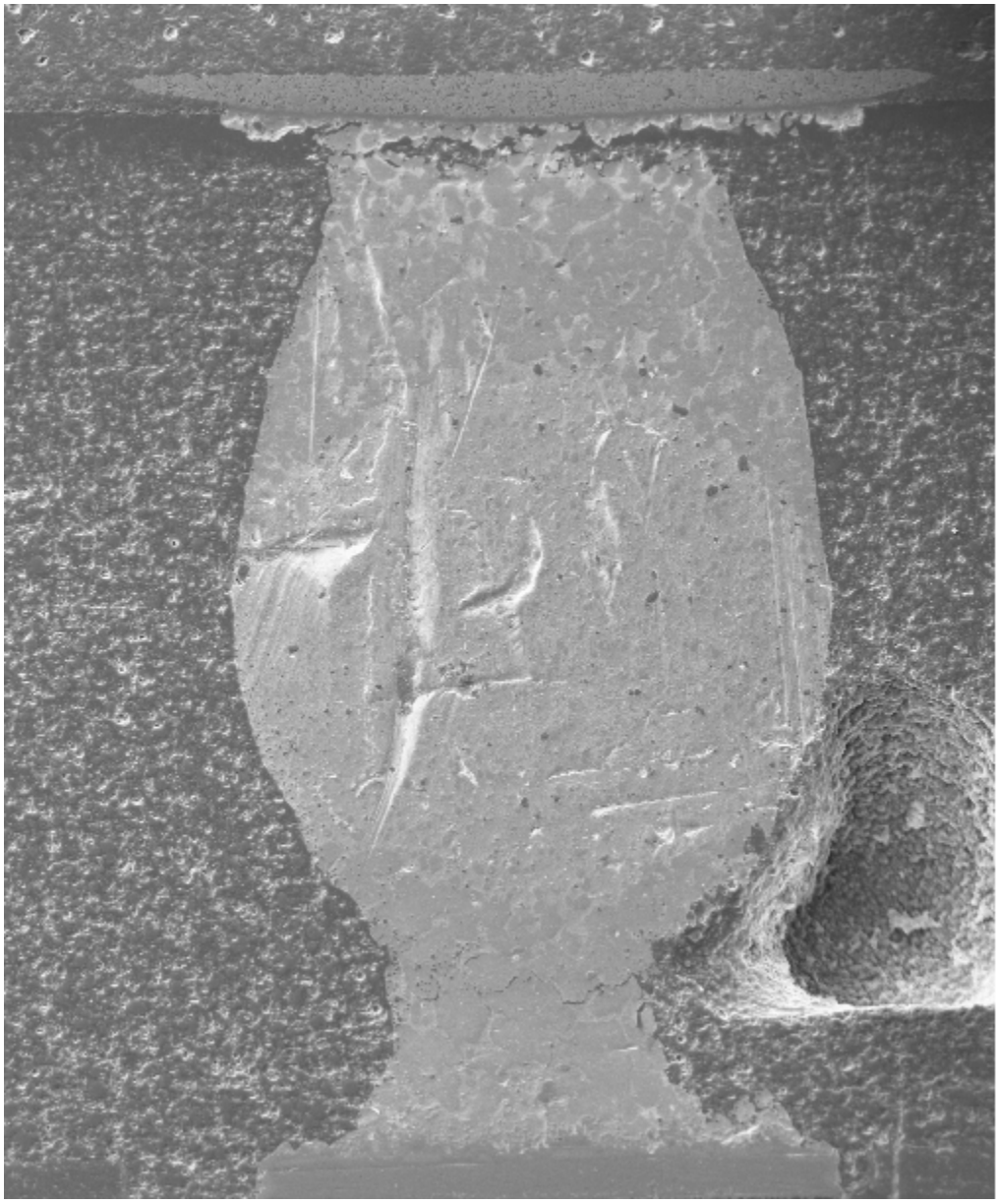

Figure 5-27 SEM Failed High-lead

Figure 5-28 below shows several more interconnects exhibiting the same failure mode.

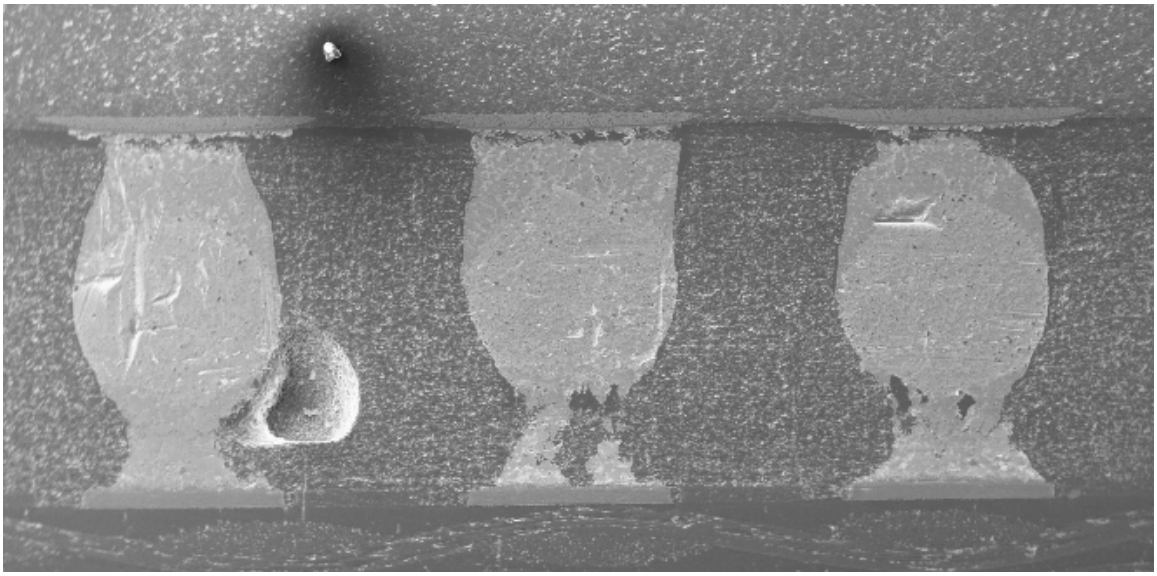

Figure 5-28 SEM Failed High-lead interconnects

Figure 5-28 shows several interconnects with damage at the top of the interconnect in the upper eutectic layer. Any damage seen in the lower bridging of figure 5-28 is a result of damage from package warping mentioned previously in this section. The interconnects presented here are not pristine, undamaged high-lead solder interconnects. Generally, the eutectic solder at the top and bottom is not as elongated as figure 5-28 shows.

5.5.1 High-Pb Finite Element Model

The package was recreated in ANSYS using the dimensions presented previously. Figure 5-29 below shows a diagonal view of the finite element model. Figure 5-30 below shows a close up of the modeled High-lead I/O.

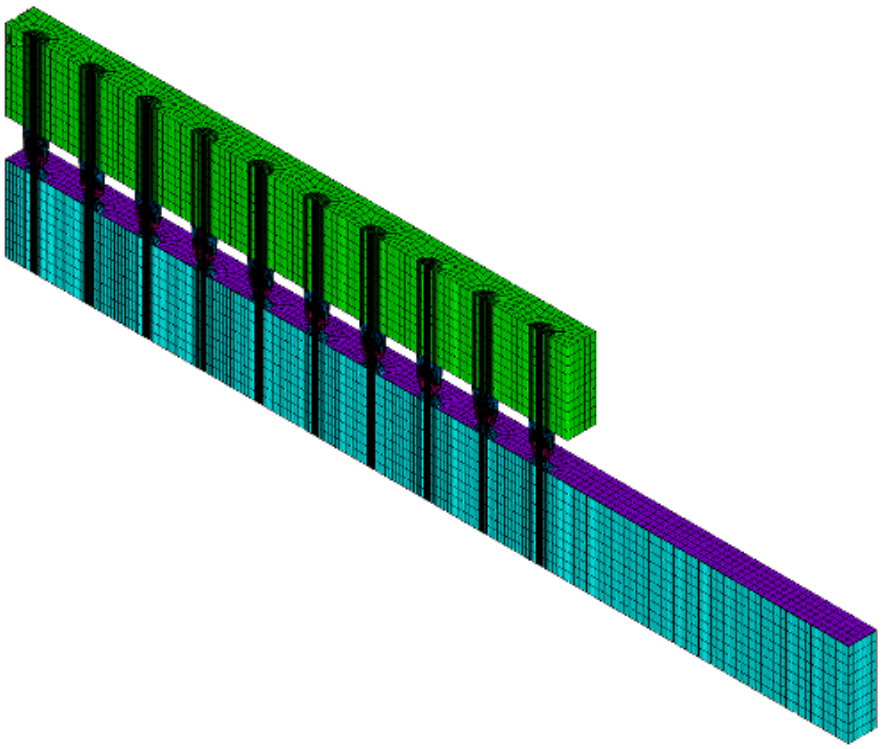

Figure 5-29 High-lead FEM Diagonal View

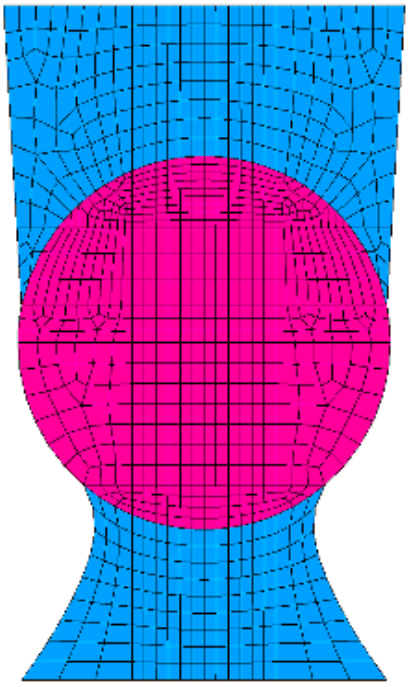

Figure 5-30 High-lead Interconnect

The pink portion of figure 5-30 represents the high-lead core while the blue represents the eutectic solder. The material properties for the package are given in table 5-11 below.

Table 5-11 High-lead Material Properties

Component	E GPa	α ppm/°C	υ
PCB	17(x,z) 7(y)	15(x,z) 67 (y)	.39
High-lead core	9	20	.38
63Sn37Pb	30	24	.35
Solder Mask	3	30	.3
Ceramic strip	27	6.7	.3
Copper	128	16	.34

The Anand constants for High-lead and 63Sn37Pb as shown in table 5-7 and table 3-9 previously were used for this simulation. Figure 5-31 below shows a failed interconnect.

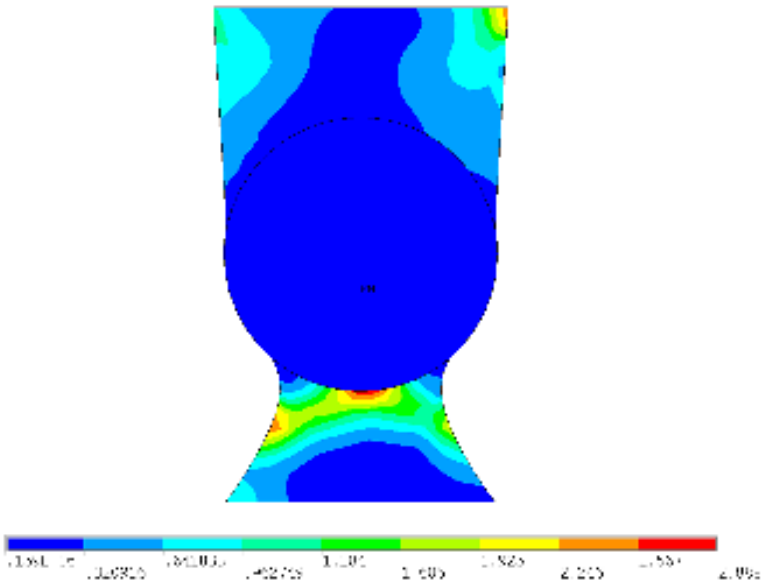

Figure 5-31 Failed High-lead FEM

Figure 5-31 shows similar results to the actual experimental results. Maximum damage is seen in the top right hand corner of the interconnect. Other regions of the interconnect show a significant amount of damage, namely at the bottom of the high-lead sphere where the eutectic bridging interfaces with the compliant core. While some damage was seen in the lower half of the cross sectioned high-lead interconnects, the dominating failure mode was cracking at the top of the interconnect. The corner ball was the first to fail and saw the most damage in both experiment and simulation. The Hysteresis plot for the package can be seen below in figure 5-32 and the plastic work is shown in figure 5-33 below that.

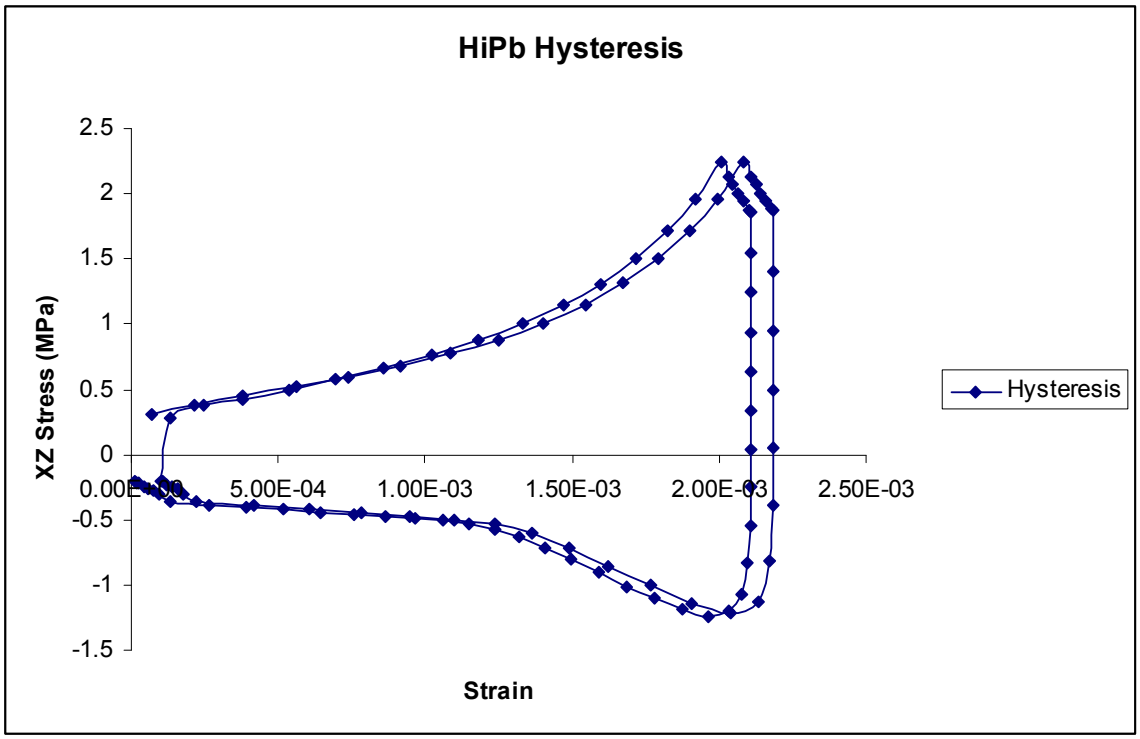

Figure 5-32 High-lead Hysteresis Loop

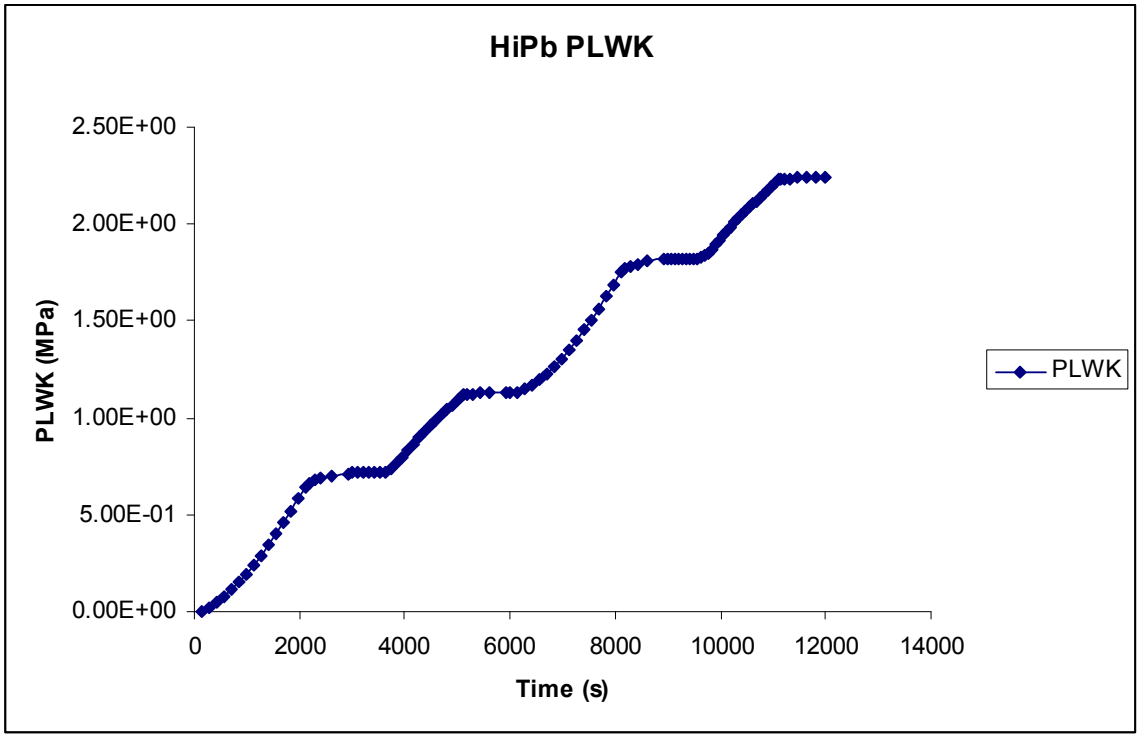

Figure 5-33 High-lead Plastic Work

The hysteresis loop shows stabilization after 2 cycles. The plastic work approaches 2.2 MPa at the end of the simulation. The same life prediction equations used for the CCGA and SOL models were used for the high-lead model. Life correlation for prediction and experiment can be seen below in table 5-12.

Table 5-12 High-lead Life Correlation

High-lead	Characteristic Life (η)	Error
Experiment	1,991 cycles	37%
Simulation	1,246 cycles	

The High-lead simulation closely tracked the experimental results showing a simulated life of 1,246 cycles while the actual experimental characteristic life was 1,991 cycles. All in all the high-lead package performed well outperforming the SOL package but underperforming the more reliable CCGA. The high-lead outperformed the tin lead

eutectic by approximately 200 cycles. Table 5-13 below summarizes the package results so far.

Table 5-13 Package Comparisons

Package	η
CCGA	3,014
High-lead	1,991
SOL	518
63Sn37Pb	1,754

5.6 SAC 305

Due to the ban of lead based solder alloys, the industry has searched for a lead free solder interconnect to replace the well documented and understood tin lead eutectic solder alloy. Generally speaking, the SAC alloys outperform the tin lead eutectic alloys. However, some researchers [Clech 2005] have shown that the tin lead eutectic will outperform the SAC alloys in high stress situations, such as on ceramic packages where the CTE mismatch between board and substrate is large. Whether or not the SAC alloy outperforms the tin lead alloy has proven to be largely dependent on package type and thermal conditions [Rouband 2001, Syed 2001, Vandevelde 2004]. In this test, a lead free Sn3.0%Ag0.5%Cu (SAC 305) alloy is tested on the ceramic board. The dimensions of the interconnect are presented in table 5-14 below.

Table 5-14 SAC 305 Dimensions

Ball Diameter	.7mm
Ball Height	.4mm
Pad Diameter	.45mm

Figure 5-34 below shows the performance of the SAC 305 lead free solder alloy in harsh thermal testing.

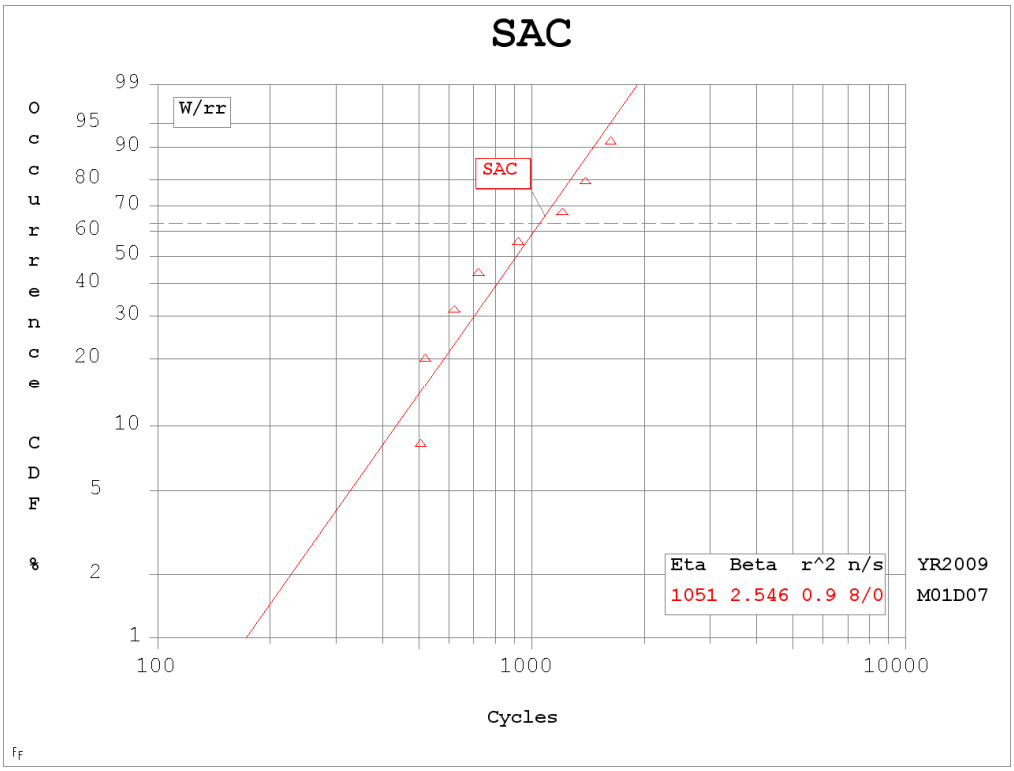

Figure 5-34 SAC 305 Weibull Plot

The characteristic life of the package was 1,051 cycles. The package showed an N1% life of 172 cycles and a β of 2.5. This was the second worst package tested as it only outperformed the SOL package. Figure 5-35 below shows an SEM image of a failed I/O.

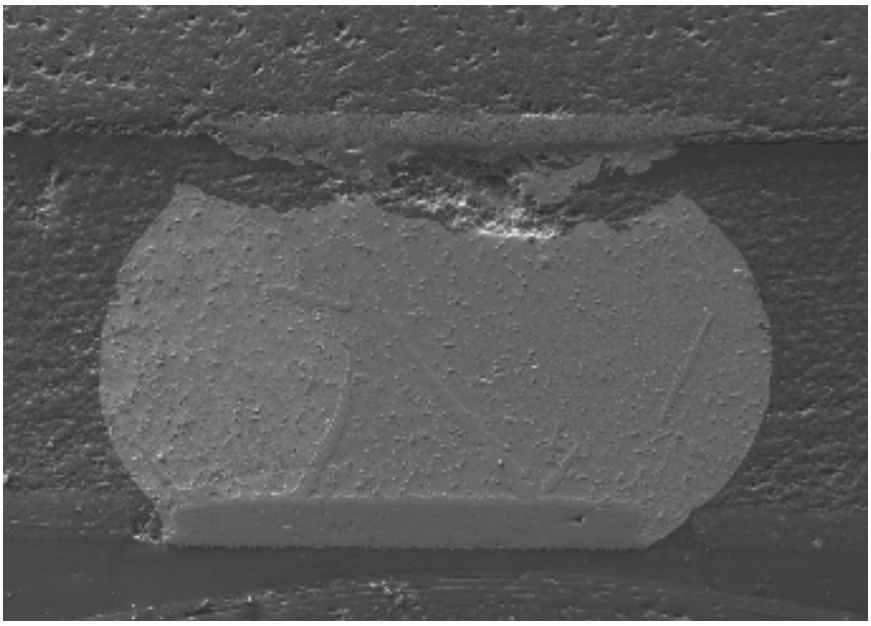

Figure 5-35 Failed SAC 305 Interconnect

Figure 5-35 shows a large amount of damage at the top of the interconnect. The crack has clearly grown across of the interconnect at the package interface. No damage is seen in other parts of the interconnect. Figure 5-36 below shows a similar failure mode.

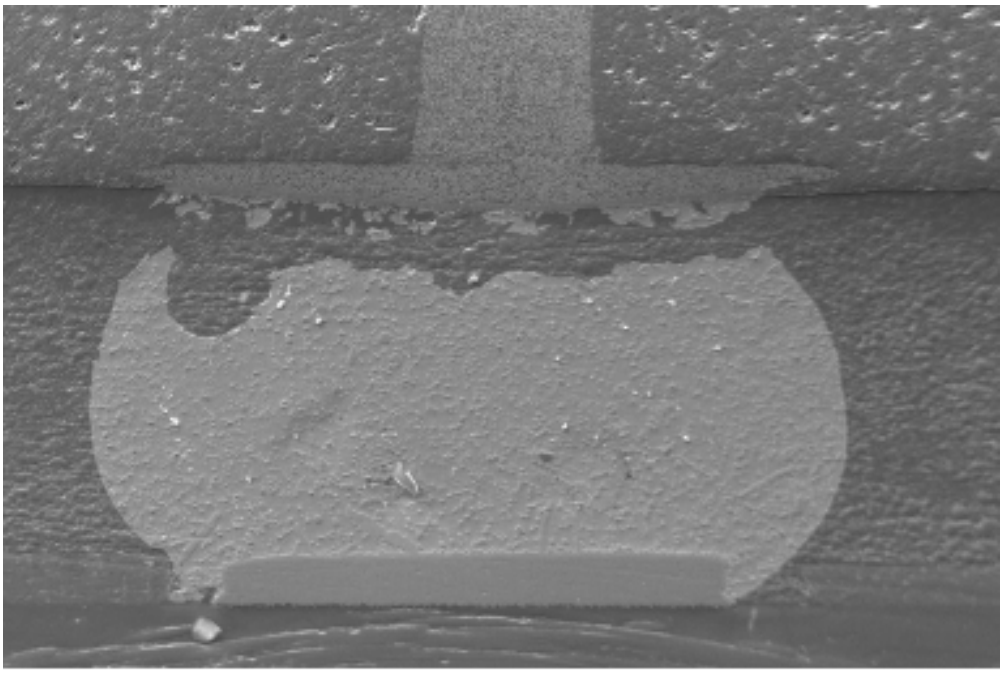

Figure 5-36 Failed SAC 305 interconnect

Figure 5-36 shows maximum damage in the top of the interconnect. No damage is seen in the rest of the interconnect. A void can be seen in the top left corner which exacerbated the damage and crack growth.

5.6.1 SAC 305 Finite Element Model

The package was recreated in the ANSYS finite element environment. A diagonal view of the package can be seen in Figure 5-37 below.

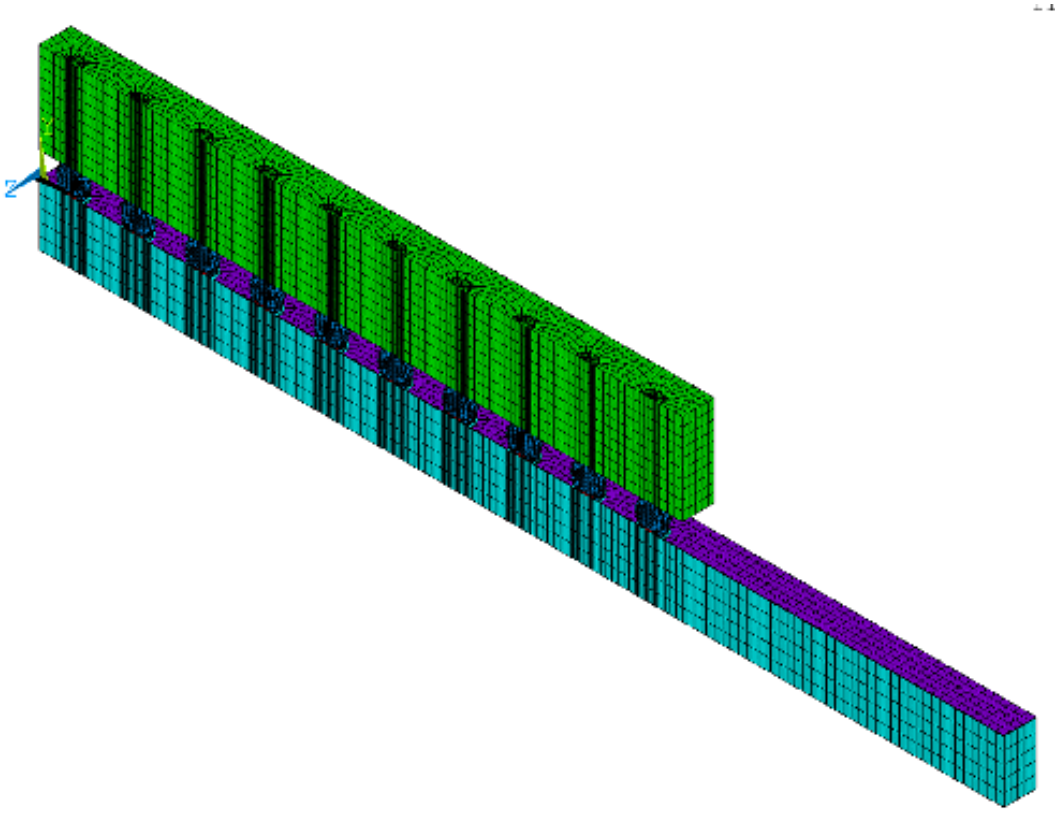

Figure 5-37 Diagonal view SAC 305

A close up of the SAC 305 interconnect is shown below in figure 5-38

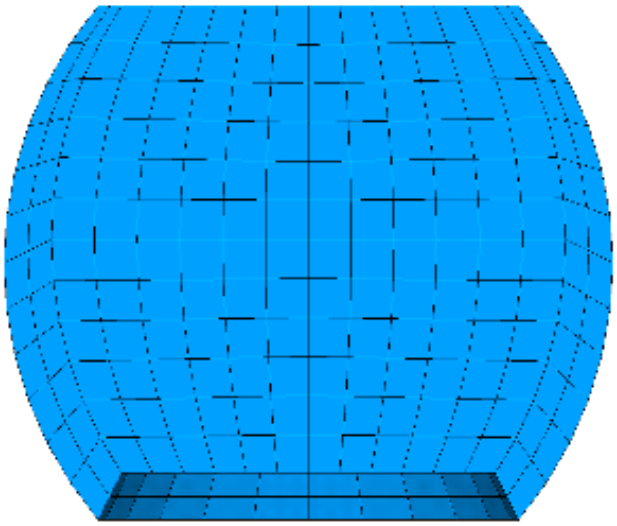

Figure 5-38 FEM SAC 305 I/O

The material properties for the model are given below in table 5-15

Table 5-15 SAC 305 Material Properties

Component	E GPa	α ppm/°C	υ
PCB	17(x,z) 7(y)	15(x,z) 67 (y)	.39
Plastic Core	9	20	.38
SAC 305	54	25	.3
Solder Mask	3	30	.3
Ceramic strip	27	6.7	.3
Copper	128	16	.34

The Anand constants for SAC 305 are shown below in table 5-16.

Table 5-16 SAC 305 Anand Constants [Chang 2006]

SAC 305 Anand constants	
S_o	45.9 (MPa)
Q/k	7460 $\left(1/K\right)$
A	5.87e6 $\left(1/\text{sec}\right)$
ζ	2
m	.0942
h_o	9350(MPa)
n	.015
a	1.5
$\hat{s}$	58.3(MPa)

Figure 5-39 below shows the failure results of the finite element simulation.

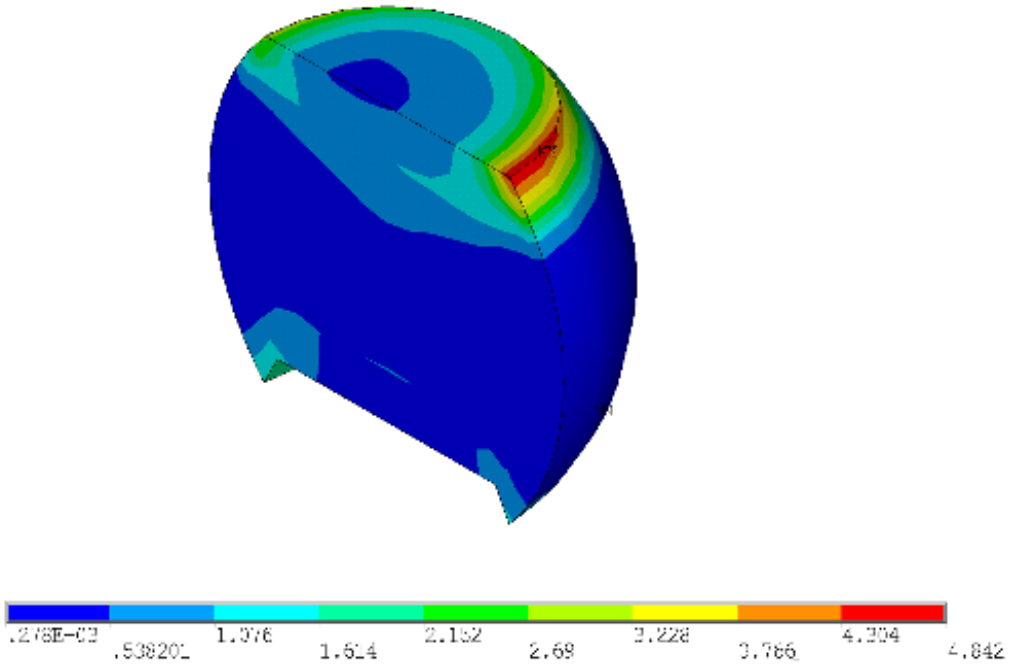

Figure 5-39 Failed SAC 305 FEM

Figure 5-39 shows maximum damage in the top right corner of the interconnect. The crack initiated in the top right corner and then proceeded to propagate throughout the

interconnect causing separation from the ceramic strip. Minimal damage was seen in the lower portion of the interconnect along the board side interface. The hysteresis plot and the plastic work for the package are shown below in figure 5-40 and figure 5-41.

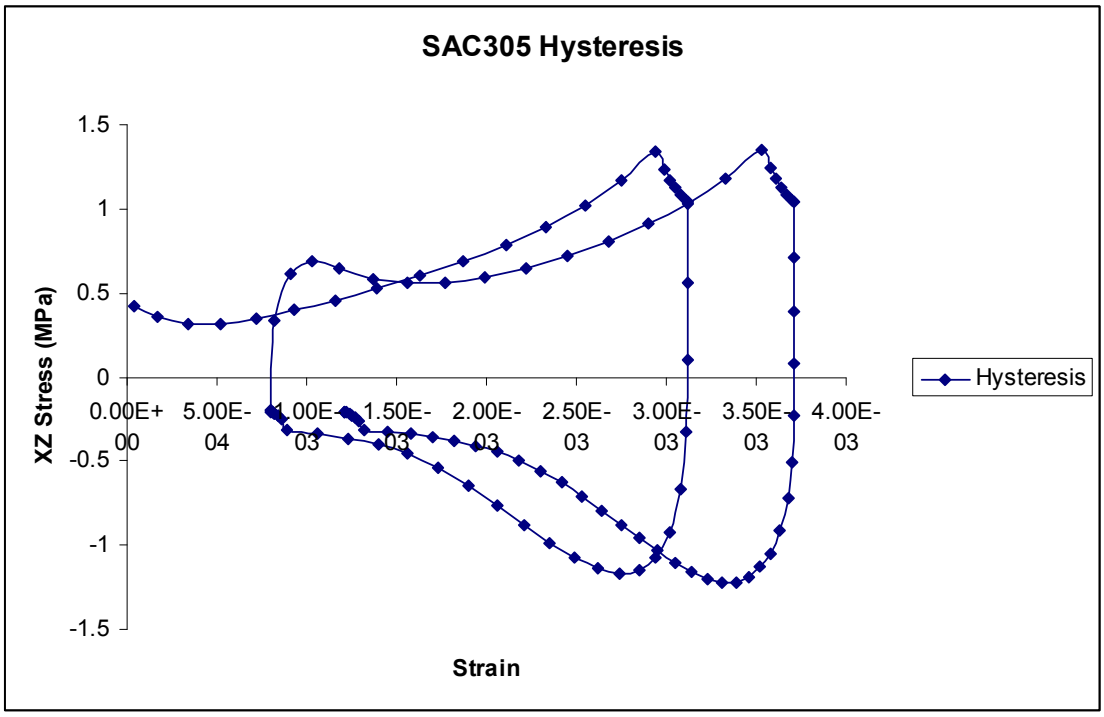

Figure 5-40 SAC 305 Hysteresis Loop

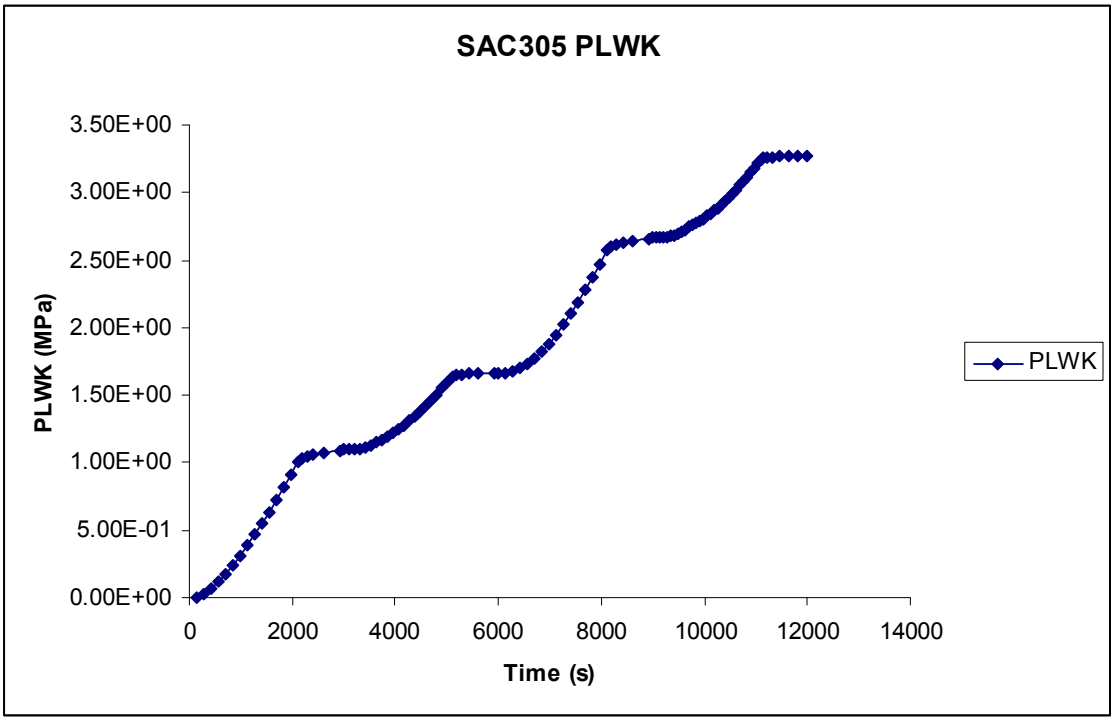

Figure 5-41 SAC 305 Plastic Work

Figure 5-40 shows stabilization of the hysteresis loop after two simulated thermal cycles. Figure 5-41 shows the plastic work topping off at 3.5 MPa when the simulation ends. For the lead free, SAC 305 alloy, Syed's lead free life prediction method was used. The life equation showed good results and the life correlation is shown below in Table 5-17.

Table 5-17 SAC 305 Life Correlation

SAC 305	Characteristic Life (η)	Error
Experiment	1,051 cycles	8%
Simulation	1,140 cycles	

Table 5-17 shows a simulated life of 1,140 cycles and an experimental life of 1,051 cycles giving an 8% error. A comparison of the package lives is shown below in table 5-18.

Table 5-18 Package Comparison

Package	η
CCGA	3,014
Hi Pb	1,991
SOL	518
SAC 305	1,051
63Sn37Pb	1,754

Table 5-18 shows that the SAC 305 package only outperformed the SOL package. It is important to note that the SAC 305 underperformed the tin lead eutectic alloy by approximately 700 cycles further proving that the lead free alloy's thermal performance is strongly dependent on package type and thermal environment as results showing the superiority of lead free to tin lead eutectic [Dai 2005, Rouband 2001, Syed 2001, Lau 2003, Yang 2008] and the inferiority of SAC 305 to tin lead eutectic have both been shown [Clech 2005]. Here, the inferiority of the SAC 305 alloy on a ceramic package in a harsh thermal environment is shown supporting the findings in [Clech 2005].

5.7 Package Comparison

A Weibull plot comparing all of the packages is shown below in figure 5-42.

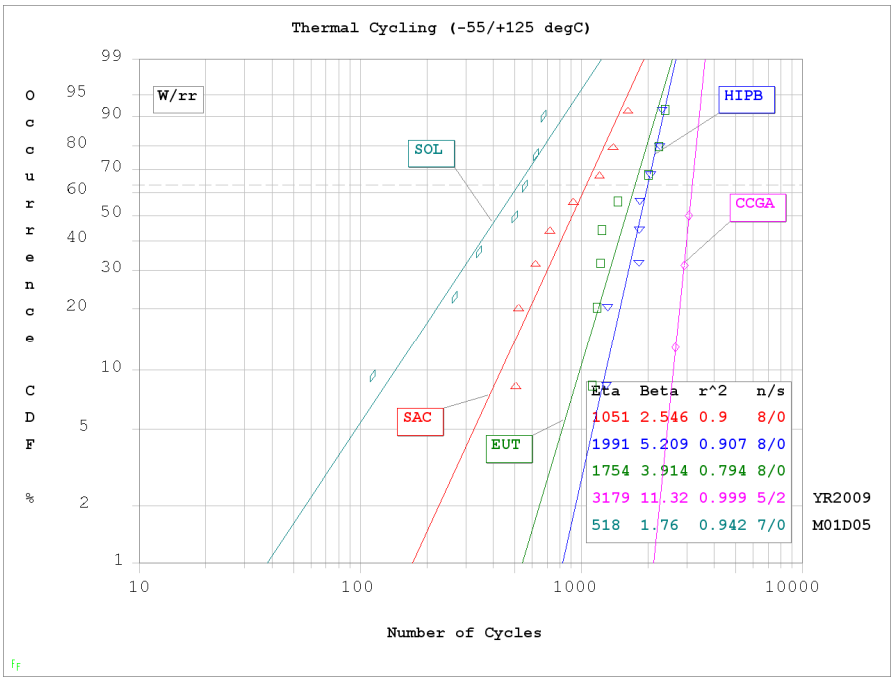

Figure 5-42 Weibull Plot Comparison All Packages

Figure 5-42 shows the superiority of the CCGA package in harsh thermal testing. The SOL package was clearly the worst of all the packages examined. The high-lead sphere provided better reliability than the eutectic with the lower young's modulus high-lead sphere acting as a buffer and relieving stress on the interconnect. Only the SOL and SAC 305 interconnects underperformed the standard tin lead eutectic solder ball. Table 5-19 below summarizes the characteristic lives of the packages.

Table 5-19 Characteristic Life of all packages

Package	η
CCGA	3,014
High-lead	1,991
SOL	518
SAC 305	1,051
63Sn37Pb	1,754

The Weibull plot comparing all of the packages from simulation is shown in figure 5-43 below.

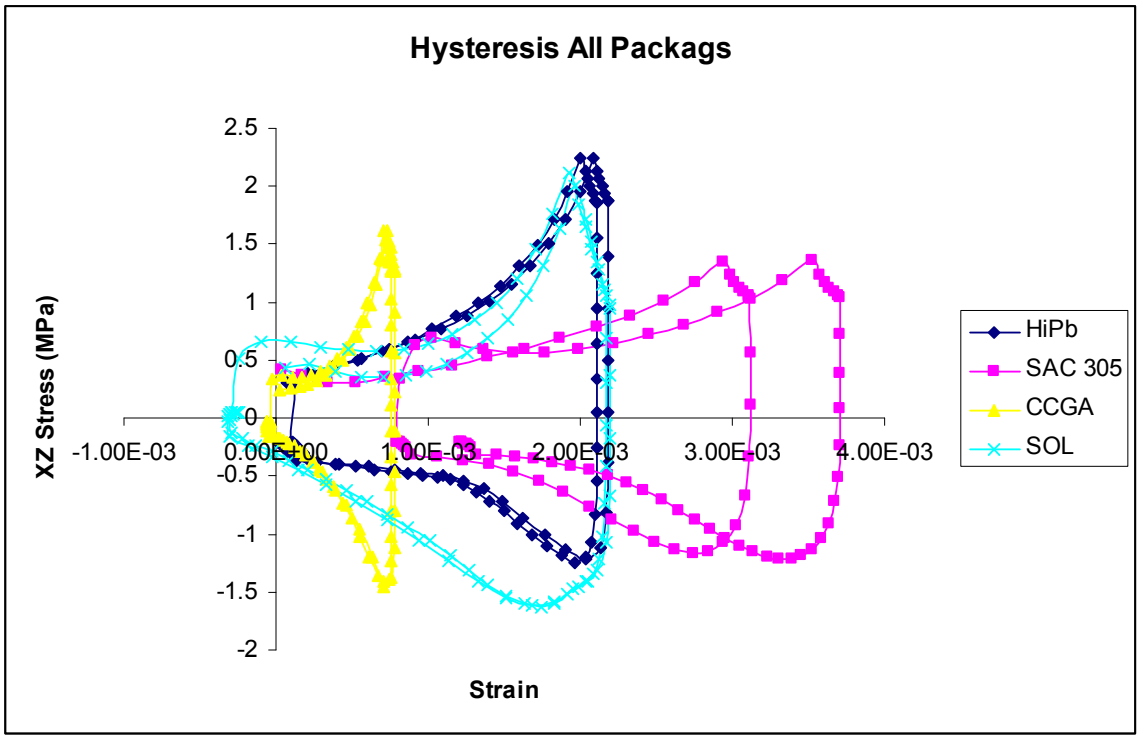

Figure 5-43 Comparative Hysteresis Loop All Packages

The CCGA clearly shows a smaller hysteresis loop when compared to the other three packages indicating that it accrued the least damage. The other packages were all comparable with the SAC 305 and SOL loops being the largest. The plastic work comparison of the packages is shown in Figure 5-44 below

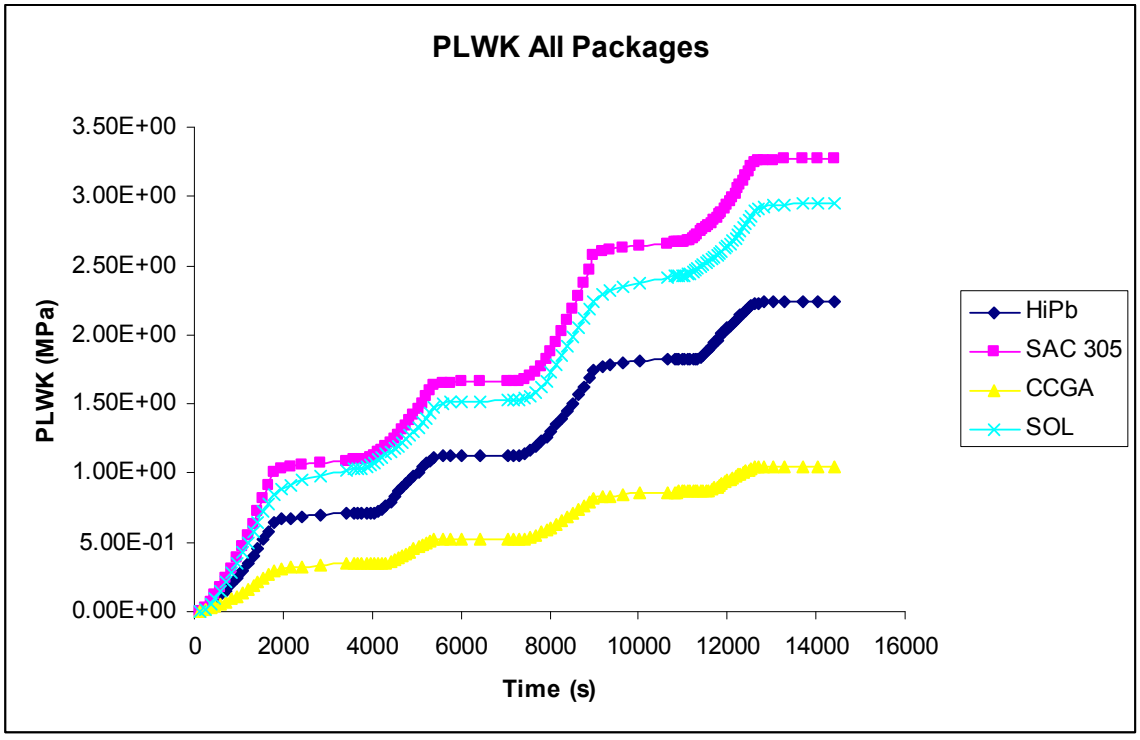

Figure 5-44 Plastic Work Comparison of all packages

From figure 5-44 the SAC 305 and SOL showed the most plastic work while the CCGA showed the least as would be expected from the simulation and experimental results. The SAC 305 seemed to be accruing more damage than the SOL package as time went on as it had a steeper slope than the SOL package. However, the SOL interconnect still showed a shorter characteristic life.

CHAPTER 6

SUMMARY AND CONCLUSIONS

To conclude the report, the following key results should be remembered. In the first study, the effect of underfill and pad finish on the enhancement of PBGA's and high I/O clip chips, BGA 1152, was studied. The underfill had a significant impact on the life of the smaller PBGA's increasing the characteristic life of the PBGA 128 package by 7X. The maximum improvement of characteristic life for the BGA 1152 package was 3X for the HASL pad finish. The underfill was shown to have a greater impact on the smaller PBGA packages. When analyzing the pad finish, the HASL pad finish consistently outperformed the ImAg pad finished packages. In the case of the BGA 1152 package the HASL outperformed the ImAg pad finish by approximately 1,350 cycles. In the smaller PBGA packages, the difference in characteristic life due to pad finish was not as drastic.

In the second study, the thermo-mechanical reliability of lead free alloys was tested. The higher silver content alloys outperformed the low silver content alloys on identical chip scale packages in a -55 to 125 Celsius thermal environment. Of all the alloys tested the SAC 305 has been the most reliable in terms of characteristic life. The SAC X and SAC-X+ alloys were low silver content alloys doped with Bismuth and Nickel. The SAC-X+ alloy showed a marginal improvement in characteristic life in comparison to the other low silver content alloys, but still significantly underperformed the high silver content SAC 305 and Sn3.5Ag alloys. Finite element models for the SAC

305 and Sn3.5Ag models were created and simulation showed promising results in terms of predicting failure mode, but not in predicting the characteristic lives of the packages.

In the third and final study, the thermo-mechanical reliability of five different interconnect systems was tested in a harsh thermal environment. The copper column grid array (CCGA) outperformed the other four interconnects. The SOL plastic core packaged performed the worst of all the interconnects with a characteristic life of 518 cycles. All of the packages were recreated in ANSYS and their harsh thermal environment simulations showed good correlation with actual testing in both failure mode and life prediction.

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APPENDIX

LIST OF SYMBOLS

α_{PWB}	Coefficient of thermal expansion for the printed wiring board
α_{cc}	Coefficient of thermal expansion for the ceramic carrier
α_{eff}	Effective Coefficient of Thermal Expansion
γ_{el}	Time independent elastic strain
γ_{p}	Time independent plastic strain
γ_{pr}	Time dependent primary strain
γ_{sec}	Time dependent secondary strain
γ_{xy}	Shear Strain
$\frac{d\gamma_{scr}}{dt}$	Secondary strain change with time
β	Weibull Slope
η	Characteristic Life
$\dot{\varepsilon}_{p}$	Inelastic Strain Rate
$\frac{d\varepsilon_{p}}{dt}$	Plastic Strain with time
τ	Shear Stress
ϖ_{acc}	Plastic Work Accumulated

σ	Equivalent Stress
ξ	Multiplier Of Stress
A	Material dependent constant
A	Pre-exponential factor
a	Strain rate sentivity of hardening
a	Pad Diameter
$\frac{da}{dN}$	Crack Growth Per Cycle
Ag	Silver
BT	Bismaleimide triazene
CABGA	Chip Array Ball Grid Array
CBGA	Ceramic Ball Grid Array
CCGA	Copper Column Grid Array
CTE	Coefficient of thermal expansion
Cu	Copper
DIP	Dual Inline Package
DNP	Distance to Neutral Point
E_{eff}	Effective Young's Modulus
FEM	Finite Element Model
h_o	Hardening Constant
h	Solder Joint Height
HASL	Hot Air Solder Level
HiPb	High Lead

I/O	Interconnect
ImAu	Immersion Gold
ImAg	Immersion Silver
IMC	Intermetallic Compound
L	Package Length
m	Strain Rate Sensitivity
M	Strain rate sensitivity of stress
MPa	Mega Pascal
N_f	Cycles To Failure
N	Stain Rate Sensitivity of Saturation
n	Material Dependent constant
NSMD	Non Solder Mask Defined
OPC	Organic Protective Coatings
P	Load
PBGA	Plastic Ball Grid Array
Pb	Lead
PCB	Printed Circuit Board
PPM	Parts per million
PQFP	Plastic Quad Flat Pack
PSGA	Polymer Stud Grid Array
Q	Activation Energy
Q/k	Activation energy over boltzmann's constant
R	Universal Gas Constant

Sn	Tin
SAC	Tin Lead Silver Alloy
SMD	Solder Mask Defined
s_o	Initial Value of deformation resistance
$\hat{s}$	Coefficient of Deformation Resistance
SEM	Scanning Electron Microscopy
T	Temperature
TSSOP	Thin Small Outlying Package
ΔT	Temperature Difference
UF	Underfill
u_x	Displacement in the x-direction
u_y	Displacement in the y-direction
u_z	Displacement in the z-direction
VISCO	Viscoplastic