Design and Implementation of High-Speed Low-Power Analog-to-Digital and Digital-to-Analog Converters

by

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Abstract

With the rapid development of modern communication and personal wireless products, there are increased demands for next generation communication transceivers that feature ultra-high data conversion rates with reconfigurable architectures. As the essential building block in most communication and control system, data converters, including analog-to-digital converter (ADC) and digital-to-analog converter (DAC), are serving as the link between analog and digital worlds. Featuring high sampling rate, low power supply voltage and low power consumption, next generation data converters in transceivers will be architecturally closer to the signal interface, antenna.

By digitizing the received signal or converting digital code back to analog signal at ultra-high frequency instead of baseband frequency or intermediate frequency, RF transceivers can significantly simplify the radio architecture. For example, as for high-speed ADC, moving as many of the radio functions from the RF transceiver IC to the baseband digital chip as possible will improve the radio performance, cut the overall power and, most importantly, allow re-configurability of the radio designs for multi-band and multi-standard coexistence.

In this research, multiple ADC/DAC designs are implemented in different technologies to address either high-speed or low-power design challenges or even both. Circuit design techniques and considerations are extensively and carefully discussed in both architectural and transistor level. Simulation and measurement results are also given to verify functionality and performance of proposed designs.

For 3-bit over X-band high-speed ADCs, 0.12μm SiGe HBT technology featured with f_t/f_{max} of 210/310 GHz is used to enhance the device operation speed. CML circuits are employed for digital logic implementation to provide fast switching speed. For 12-bit low power high speed pipeline ADCs, low supply voltage is applied to reduce the overall power consumption. In addition, sharing operational amplifiers (OpAmp) between two time-interleaved pipeline ADC channels is used to further save power and double sampling rate. For 12-bit cryogenic DAC, current steering architecture is utilized to maintain a good trade-off between high-speed and low-power. 6+4+2 bit segmentation scheme is to keep the best balance between minimizing the circuit area of thermometer decoders and optimizing the DAC static and dynamic performance.

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List of Abbreviations

ADC	Analog-to-Digital
DAC	Digital-to-Analog
ENOB	Effective Number of Bits
INL	Integral Non-Linearity
DNL	Differential Non-Linearity
SFDR	Spurious-Free Dynamic Range
SNR	Signal-to-Noise Ratio
SNDR	Signal-to-Noise-and-Distortion Ratio
SINAD	SIgnal-to-Noise-And-Distortion
FET	Field Effect Transistor
MOS	Metal–Oxide–Semiconductor
CMOS	Complementary Metal–Oxide–Semiconductor
BiCMOS	Bipolar and Complementary Metal–Oxide–Semiconductor
SiGe	Silicon-Germanium
BJT	Bipolar Junction Transistor
HBT	Hetero-junction Bipolar Transistor
OPAMP	OPerational AMPlifier
SAR	Successive Approximation Register
UWT	Ultra-Wide range Temperature

ULT	Ultra-Low Temperature
FoM	Figure of Merit
DIP	Dual In-line Package
THA	Track and Hold Amplifier
SHA	Sample and Hold Amplifier
CML	Current Mode Logic
DFF	D-Flip-Flop
LNA	Low Noise Amplifier
MUX	Multiplexer
VGA	Variable Gain Amplifier
IF	Intermediate Frequency
RF	Radio Frequency
PA	Power Amplifier
LPF	Low-Pass Filter
VCO	Voltage Controlled Oscillator
PLL	Phase Locked Loop
BIST	Build-In-Self-Test
LSB	Least Significant-Bit
MSB	Most Significant-Bit
CLCC	Ceramic Leadless Chip Carrier

Chapter 1 Introduction

1.1 Background and Motivation

Serving as the link between the analog and digital world, analog-to-digital converter (ADC) and digital-to-analog converter (DAC) are the crucial part in many modern circuit systems. Especially due to the rapid development of modern communication and personal wireless products, there are increased demands for next generation communication transceivers that feature ultra-high data conversion rates with reconfigurable architectures. Digitizing the received signal at ultra-high frequency instead of baseband frequency will greatly simplify the radio architecture. Moving as many of the radio functions from the RF transceiver IC to the baseband digital chip as possible will improve the radio performance, cut the overall power and, most importantly, allow re-configurability of the radio designs for multi-band and multi-standard coexistence[1][2][3][4].

In a software defined radio transceiver, as shown in Fig. 0.1, the received signal will not be down-converted to an inter-mediate frequency (IF) or a baseband frequency. Instead, the received signal will be digitized by an ultra-high speed ADC directly at radio frequency (RF). Thus, mixers and frequency synthesizers that are power hungry and standard related can be eliminated from the RF transceiver. The only blocks needed in the receiver path is a low noise amplifier (LNA) and a variable gain amplifier (VGA), while the transmitter requires only a high-speed DAC, power amplifier (PA) and filter. With all the benefits a software defined radio can

provide, the burden lies upon the design of the ultra-high speed ADC and DAC. Since A/D converters generally are more power-hungry and complicated than D/A converters to achieve a given speed and resolution, ADC often becomes the bottleneck in whole communication systems and limits overall performance in signal processing systems [5][6][7]. Therefore, ultra-high speed data converters, especially high-speed ADCs, become the most crucial building blocks for software defined radio designs. Ideal ADCs for software defined radio applications should feature high linearity, large dynamic range and small area.

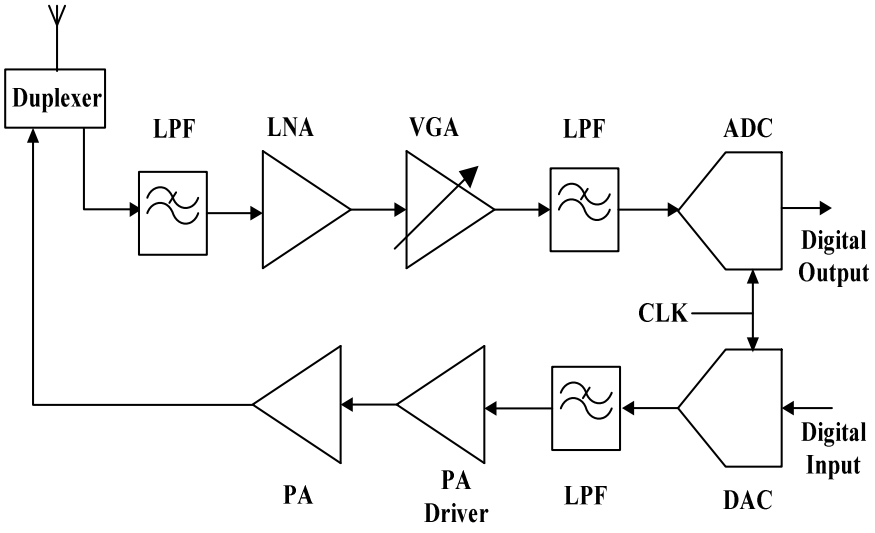

Fig. 0.1 Architecture of the RF front-end for software defined radio transceiver.

Meanwhile, with the explosive growth of wireless communication and portable devices, low power operation is another important key factor for those battery-powered systems. In the applications like notebook computers, cell phones, camcorders and portable storage devices, etc., the low power operation is indispensable and mandatory. This inevitably demands the whole communication system and especially power-hungry data conversion blocks to robustly operate

under both low power consumption and low power supply voltage condition, which will put big challenge on already-complicated A/D and D/A converters [8][9][10][11][12]. Low power supply voltage not only means smaller head room and more margin region operation in device level, but also significantly affects the overall linearity, speed, matching and accuracy for the whole data conversion system. More design consideration and technique needs to be involved to assure correct functionality of both device and block levels.

In this research, multiple ADC/DAC designs are implemented to address either high-speed or low-power design challenges. Circuit design techniques and considerations are given in both device and system level. For 3-bit over X-band high-speed ADCs, 0.12 μm SiGe HBT technology featured with f_t/f_{max} of 210/310 GHz is used to enhance the device operation speed. Current mode logic (CML) circuits are adopted for digital logic implementation to provide fast switching speed. For 12-bit high-speed low power pipeline ADC, 1.5V low supply voltage is applied to reduce the overall power consumption. In addition, sharing operational amplifiers (OpAmp) between two time-interleaved pipeline ADC channels is used to further save power and double sampling rate. For 12-bit cryogenic DAC, current steering architecture is utilized to maintain a good trade-off between high-speed and low-power. 6+4+2 bit segmentation scheme is to keep the best balance between minimizing the circuit area of thermometer decoders and optimizing the DAC static and dynamic performance.

1.2 Organization of the Dissertation

The organization of the dissertation is as follows:

Chapter 2 gives an overview of the various A/D and D/A converter architectures. For A/D converters, flash type one is most straightforward structure and can achieve fastest speed but

only with low resolution bits, usually smaller than 6-bit. Folding ADC is second fastest structure and can reach over giga sample per second (GS/s) sampling rate with medium resolution bits, from 6 bits to 9 bits. Two-step ADC can provide up to 12-bit high resolution and medium high speed which can be over multiple mega sample per second (MS/s). Pipeline ADC is currently most favored structure in most communication systems which feature excellent performance combination of high speed and high resolution. The reported high performance pipeline ADCs already can achieve up to 16-bits very high resolution and over one GS/s sampling rate. For D/A converters, binary-weighted R-2R DAC and hybrid segmented current-steering DAC are mainly discussed. R-2R type can be implemented with good matching and relatively high resolution, but its conversion speed is limited due to suffering from the increasingly large RC-constants for each added R-2R link. By using current source matching and thermo-code weighted structure, hybrid segmented current-steering DAC can reach very high resolution bits and very high speed conversion rate, up to 16 bits and over 10GHz clock speed.

In chapter 3, ultra high speed 3-bit flash ADC designs are presented and discussed in technical details. Several high speed design techniques like using CML, current comparator, etc. are given to address the challenges due to more significant ultra high speed parasitic RC constant effect. Design considerations for low power and low voltage are also included to conform to research objective. Finally implementation and experimental results are given to verify design performance.

Chapter 4 discusses high resolution low voltage time-interleaved OpAmp-sharing pipeline ADC design. Architecture, building block and its limitations are studied. Trade-offs among resolution, speed, power and area are also given. Design requirement for building blocks, such as

OpAmp gain, gain bandwidth product, comparator tolerated offset voltage, etc., are intensively studied. Finally, experimental results are presented.

A 12-bit cryogenic segmented current-steering DAC for extreme environments application is described in chapter 5. Architectural and circuit-level design for cryogenic applications is comprehensively discussed, which includes building block structures, circuit performance under cryogenic conditions and design trade-offs among speed, static and dynamic accuracy, and power consumption, etc.

Finally, chapter 6 draws conclusions and makes recommendations for future work.

Chapter 2 Overview of Data Converter Architectures

2.1 ADC Architectures

According to frequency ranges its effective input bandwidth can reach, A/D converters can be divided into two different categories, Nyquist ADCs and Oversampling ADCs (also be known as Delta-Sigma ADCs). Since most ADCs used in aforementioned applications usually require high-speed operation and large sampling rate, high-speed Nyquist ADCs are of interest in this research. Among various ADC design considerations and optimization techniques, the major design trade-off lies between resolution and speed of the given architecture. Therefore, based on different combinations of resolution bits and sampling rate, high-speed Nyquist ADCs can be mainly sorted as, Flash ADC, Folding ADC, Two-Step ADC, and Pipeline ADC. The advantages and disadvantages of each architecture are given and discussed in following sections. In addition, due to its simplicity and straight-forwardness, time-interleaving ADC is also briefly introduced.

2.1.1 Flash ADC

The flash A/D converter is thus far the fastest and conceptually simplest ADC architecture. By using parallelism and distributed sampling network, flash ADC achieves highest conversion efficiency at the cost of employing more device and power. As shown in Fig. 0.1, an N-bit flash ADC consists of an array of 2^N-1 comparators and a set of 2^N-1 threshold values. Each of the comparators samples the input signal and compares the signal to one of the threshold

values which is usually provided by resistor ladder network. By comparing input signal with assigned reference threshold, each comparator correspondingly generates a digital code, “0” or “1” according to either smaller or larger than reference voltage. The set of 2^N-1 comparator outputs is often referred to as a thermometer code because every comparator output below some point along the array is a logic “1” (similar to the mercury-filled portion of a thermometer) while all other comparator output above this point are logic “0” (similar to the empty portion of a thermometer). The level of the boundary between ones and zeros would indicate the value of the signal, similar as the level of mercury in a thermometer indicates the temperature. These thermometer-coded comparator outputs are later converted into Binary or Gray digital code according to different application demands. The flash structure can be easily implemented in integrated circuit as a repetition of a comparator block and a ROM-based decoder. Fundamentally, flash architecture does not require a front-end sample and hold amplifier (SHA) or track and hold amplifier (THA). However, such a block can significantly reduce sampling error for comparators due to clock jitter and thus improve ADC’s dynamic accuracy, such as spurious free dynamic range (SFDR), signal-to-noise ratio (SNR), signal-to-noise and distortion ratio (SNDR) and input bandwidth. Note that all comparator inputs are tied together with the signal input. A THA or SHA can help reduce loading capacitance and consequently enhance sampling rate.

The advantages for flash ADC is self-evident and clear. Due to its parallelism operation mechanism, all comparators can finish the comparison almost at the same time and then output the final digital code within only one clock cycle. Without signal folding or amplifying, this structure can easily achieve over GS/s sampling rate [13][14][15]. The simplicity of architecture

and repetition feature of building blocks also makes it easy to implement and compatible with most integrated circuit building blocks.

However, the disadvantages of flash ADCs are also apparent. First, large device cost and power consumption is required to achieve high-speed conversion performance. For an N-bit flash ADC, 2^N-1 comparators are required, if no interpolating is used, which means power and area will increase exponentially with the resolution. For example, for a 8-bit flash ADC, it demands almost prohibitively 255 comparators while a 6-bit flash one only asks for 63 comparators. Therefore, flash ADCs can only provide up to 7-bit resolution. Beyond that, the implementation will become enormously difficult. Second, as mentioned earlier, since input is tied together with all compactors, the input capacitance increases rapidly with the increased resolution bits. For a 6- or 7-bit flash ADC, input capacitance can easily reach to more than 10pF which will need large input driving current and swing range to still achieve high-speed operation. Third, comparator offset and mismatch in reference ladder prevent flash structured ADC to reach over 7-bit resolution. To obtain an 8-bit resolution with a 1 Vp-p input signal, the comparator offset will need to be much smaller than the reference step size 4mV which is quite hard to reach in sub-micron CMOS technology. According to [16], the offset for a comparator is given by

$$V_{offset} = \frac{a_{vth}}{\sqrt{WL}} \tag{2.1}$$

where a_{vth} is unit offset voltage and its usual value is about 10 mV·μm, W and L is the CMOS transistor width and length. In order to a 1 σ offset of 1mV, we have to increase the product of W and L to 100 μm^2 which means W=200μm and L=0.5μm for a 0.5μm feature size CMOS technology. With unit capacitance C_{unit}=2fF/μm^2, the input capacitance for each comparator reaches to 200fF. Counting 255 comparators for an 8-bit flash ADC, the overall input

capacitance becomes 51pF which usually cannot be directly driven by external signal source. Thus, a buffer amplifier with excellent driving strength is needed, and necessarily requires more power and area. This dilemma between offset and input capacitance further restrict flash ADC to reach higher resolution and higher speed.

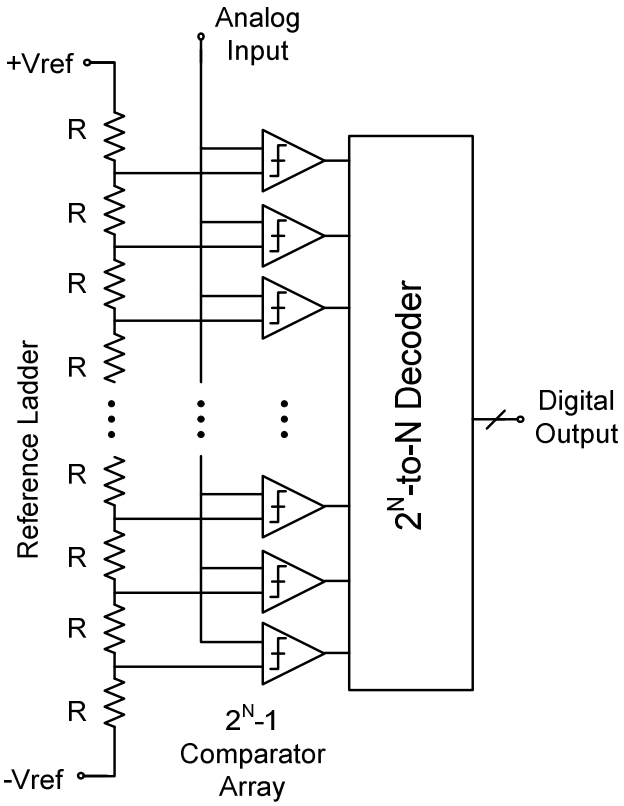

Fig. 0.1 Architecture of an N-bit flash ADC

2.1.2 Two-Step ADC

The exponential growth of power, area and input capacitance of flash structured ADCs as a function of resolution bits demands other topologies which can reach over 8-bit resolution and provide a more relaxed trade-off among these parameters. The two-step architecture is developed to reduce hardware complexity, reduce power dissipation and die area, and also to reduce input

capacitance which loads the preceding circuit to achieve a better balance among aforementioned trade-off [17][18][19][20].

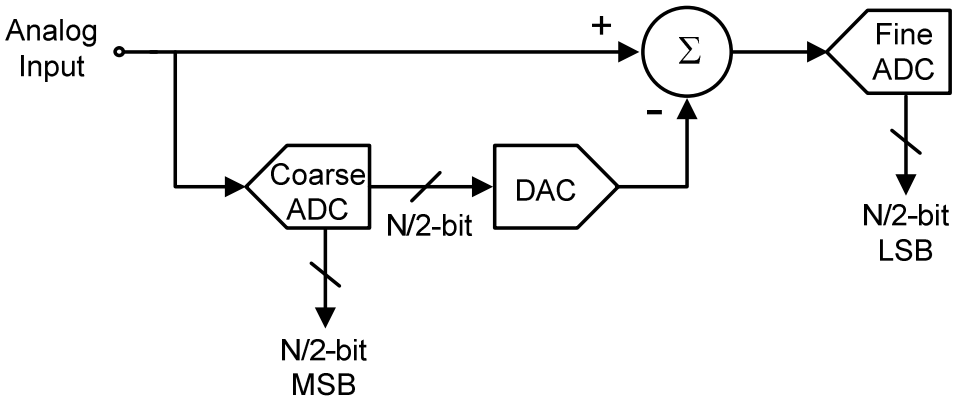

Fig. 0.2 Architecture of two step ADC

Fig. 0.2 shows the block diagram of a two-step ADC. It consists of a THA, two ADCs with N/2-bit, an N/2-bit DAC and a subtractor. It will take two steps for this type of ADC to finish one conversion process. During the first step, the N/2 MSBs of the digital output are determined by the first coarse N/2-bit ADC. Then a DAC converts this N/2 MSBs digital code back to an analog signal and feeds it into the subtractor which will subtract this portion from the original input signal. Then during the second step, the residue generated by subtractor is sent to fine N/2-bit ADC to output N/2 LSBs of the full-length N-bit digital code. Apparently, the conversion efficiency for two-step structure is only half of that for flash one. But this structure, which theoretically needs only $2*2^{N/2}$ comparators, saves a large number of required devices compared to its flash counterpart. For instance, a 8-bit full flash ADC needs 2^8-1=255 comparators while a 8-bit two-step ADC needs only $2*(2^4-1)$=30 comparators, which is a huge

saving by a number of 225. This saving also helps two-step architecture tremendously reduce required power consumption and die area when implementing an over 8-bit resolution ADC.

The disadvantages of a two-step ADC mainly include lower sampling rate, requirement for a THA or SHA, and the inaccuracy introduced by subtractor. First two can be regarded as the cost to trade speed for less device cost and lower power consumption. The critical design challenge for two-step structure is how to realize a super linear subtraction from original input signal in analog domain. The subtraction accuracy requirement for an N-bit ADC is the LSB step size which is one 2^N-th of full-scale signal. Still considering an 8-bit ADC with 1Vp-p full-scale, the subtracting error needs to be smaller than 4mV to achieve monotonicity and less than 1LSB accuracy. This tough requirement becomes even more challenging with higher resolution bits. Thus, some error correction or over-range needs to be given in order to reach more than 8-bit resolution for a two-step ADC.

2.1.3 Folding ADC

Folding architecture is proposed to combine the advantages of both flash and two-step ADCs. Without suffering from the two step mechanism, folding ADC can complete conversion process within one clock cycle as well as maintain the component saving feature [21][22][23]. As shown in Fig. 0.3, an 8-bit folding-and-interpolating ADC is composed of a THA, 32 preamplifiers, four folding amplifiers, 8x resistor passive interpolating, 32 comparators, digital encoder and a coarse flash ADC. When ADC is in operation, the input analog signal is buffered by THA to provide enough current drive strength by input buffer stage. The input signal drives a preamplifier array and a 3-bit coarse quantizer. The pre-amplified signals are fed into 4 folding blocks with a folding rate of 8. A reference ladder is used to generate a set of reference voltages

for preamplifier array. The 4 folding blocks governed by the appropriate combination of the reference voltages produce sinusoidal-like signals phase-shifted by 45^{o}. These sinusoidal signals are applied via buffers across differential interpolation resistive strings to create an array of 32 equally phase-shifted sinusoids. After interpolation, 32 wave patterns are available and contain all the information necessary to define the 5 fine bits, D4 to D0. A comparator array is then utilized to translate the analog information into digital data. On the other hand, a 3-bit coarse quantizer operates simultaneously to identify in which cycle of the folding characteristic the input signal lies. Finally, a digital encoder is required to obtain the 8-bit binary digital codes.

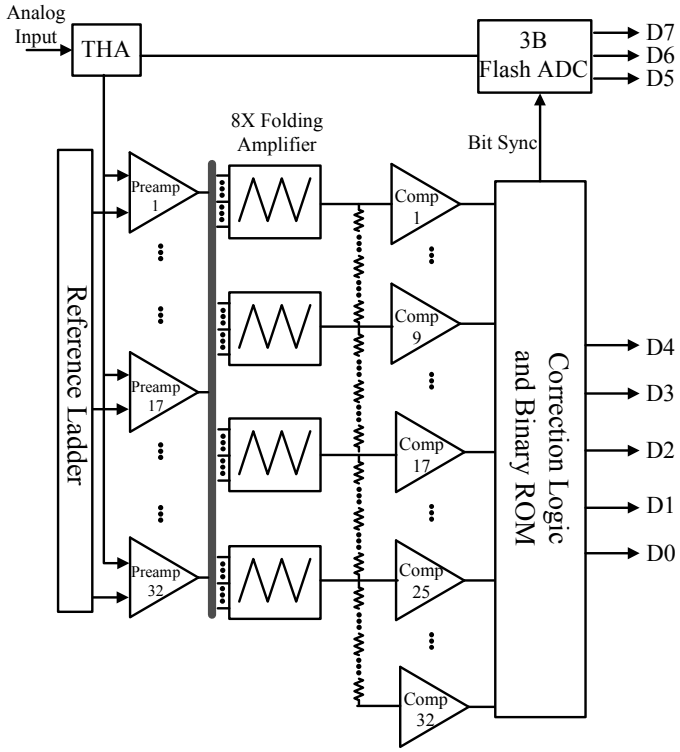

Fig. 0.3 Simplified block diagram for an 8-bit high-speed folding-interpolating ADC

The major drawback of folding architecture is that the folding of input signal actually increases the signal bandwidth for folding amplifier which will lower the effecitve input signal bandwidth for whole ADC. 8x folding means the input frequency is also increased by eight times. When folding amplifier reaches the frequency limit f_{fa}, the effective input signal frequency can only be $f_{fa}/8$. In order to achieve the same sampling rate, folding ADC requires more power, faster device and more complicated distributed THA scheme than flash ADC to overcome this inherent limitation existing in folding structure.

2.1.4 Pipeline ADC

Fig. 0.4 shows the common topology of a pipelined ADC, which consists of a cascade of P stages. Each pipeline stage needs not be identical. Fig. 0.5 gives a basic configuration which comprises an sample-and-hold amplifier (SHA), a low resolution coarse ADC (sub-ADC), a DAC (sub-DAC), and a subtracter. In operation, each stage initially samples and holds the output from the previous stage and the held input is then converted into a low resolution digital code by the sub-ADC and back into an analog representation by the sub-DAC. Finally, the SHA amplifies the difference between the held analog signal and the reconstructed analog representation to give the residue for the next stage.

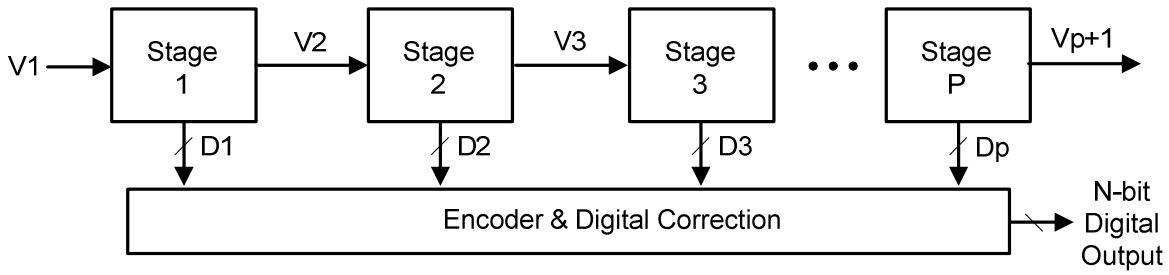

Fig. 0.4 Architecture for a P-stage pipeline ADC

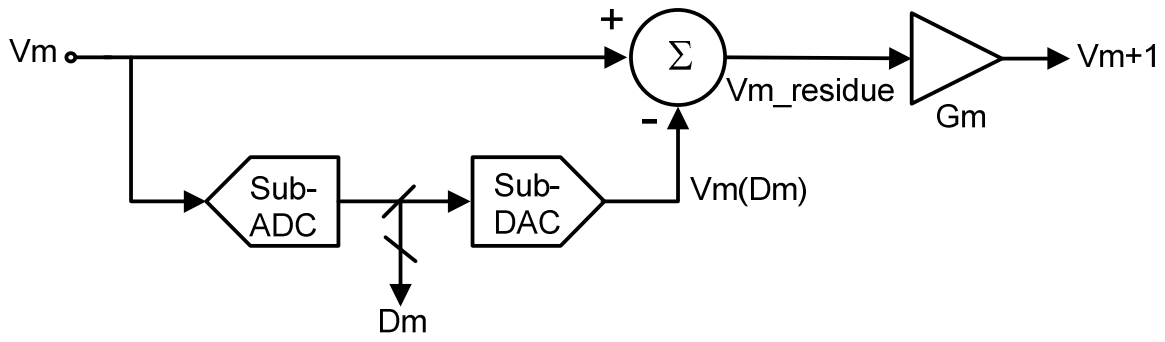

Fig. 0.5 Block diagram for a pipeline stage

The primary advantage of pipelined ADCs is that they provide high throughput rates and occupy small die areas. Both advantages stem from the use of SHA technique which allows each of the stages to operate concurrently; that is, at any time, the first stage operates on the most recent sample while all other stages operate on residues from previous samples [24][25]. If the sub-ADCs are realized with flash converters, pipelined architectures require only two main clock phases per conversion step. Hence the maximum throughput rate can be quite high. In additional, since all stages operate concurrently, the number of stages used to obtain a given resolution is not constrained by the required throughput rate. The speed of a pipelined ADC is limited only by the settling of the inter-stage SHA.

While the throughput rate is regardless of the number of stages used in pipelined ADC, the conversion time for any given sample is still proportional to the number of stages. This is true because the signal must work its way through all of the stages before the complete output word is generated. If used in a feedback system, this delay can be an issue for pipelined ADC. Before the sampling phase for next stage, the amplifier in each pipeline stage needs to amplify the residue according to the number of output digital bits. By doing this, the resolution requirements for the

following stages are relaxed. One significant advantage of this is that the comparators in the last stages of the pipeline don't need to be as accurate to the full ADC resolution as they are required to be in other two-step ADCs. However, the disadvantage of adding the gain blocks is that they tend to be the dominant source of the power dissipation in the ADC and the major nonlinearity error source. Therefore, pipelined ADCs usually need dissipate more power to realize wide bandwidth and high amplification gain to get the expected resolution bits. Nonetheless, like the other two-step or multi-step ADCs, pipelined ADCs can achieve high resolutions with relatively little hardware cost. Furthermore, mismatches in comparators or reference threshold, which are the major limitation to prevent flash, folding and two-step ADCs from achieving high resolution bits, can easily be eliminated by digital correction logic. Because of their tolerance to comparator offsets and the ability of the pipeline stages to operate in parallel, pipelined ADCs are well suited for high resolution applications where high speed is required.

2.1.5 Time-Interleaved ADC

Time-interleaving, as shown in Fig. 0.6, is to utilize paralleled ADCs to increase the overall conversion rate for the whole system [26][27]. Usually, paralleled ADCs are built with the same structure to maintain good matching between different channels. It is also apparent that the overall sampling rate will be N-time increased if N-channel interleaving is used. Interestingly, except the digital multiplexer final stage, the clock for each channel doesn't need to run faster to obtain higher conversion rate. This is because among ADC trade-offs, device cost and die area are traded to get higher sampling rate. Although time-interleaving can help the whole system to reach higher conversion rate without increasing the clock speed for each individual ADC, the accuracy for clock phase in each channel is required to be commensurate with the accuracy of

system clock speed which is much higher and N-times the channel clock frequency for a N-channel time-interleaving. Another issue for time-interleaving is the mismatch between channels. Even if each channel exhibits ideal A/D conversion, gain mismatch among SHAs and phase jitter among clock used in each channel might still affect the accuracy of sampled signal voltage and thus cause some nonlinearity error which will cause non-monotonicity for the whole conversion system. As mentioned earlier, this non-monotonicity for the overall conversion system and preclude its possible usage in feedback system. Therefore, design techniques and considerations for good matching need to be carefully and extensively taken into account in both transistor-level and layout-level for a time-interleaving ADC to realize expected linearity and resolution.

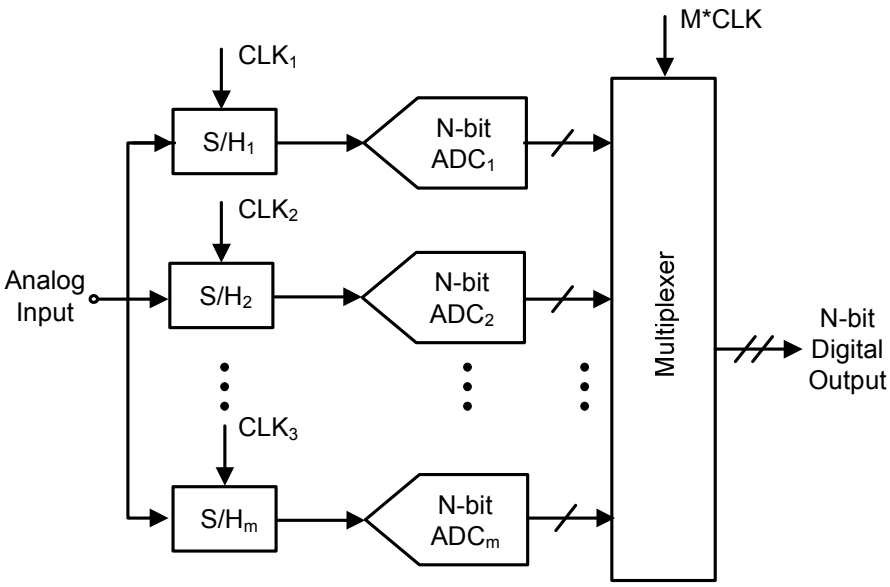

Fig. 0.6 Block diagram for n-channel time-interleaving ADC

2.2 DAC Architectures

According to different internal signal formats, DACs can be sorted as voltage DAC, current DAC and charge-redistribution DAC. Meanwhile, according to different implementation

methods, DACs can also be classified as binary-weighted DAC, thermo-code weighted DAC and hybrid/segmented DAC. In such a variety of types, current DAC can have the best matching effect and consequently achieve highest resolution bits. Without significant static current, voltage and charge-redistribution DACs feature the lowest power consumption. Binary-weighted DAC has conceptually the smallest device cost and die area. In contrast, by trading component cost for better matching and accuracy, thermo-code weighted DAC can theoretically achieve the highest resolution bits. Finally, hybrid/segmented DAC keeps the best balance for performance combination of resolution and device cost. Again, since most DACs used in aforementioned applications, such as communication system and wireless handheld devices, usually require high-speed operation and high sampling rate, high speed DACs are of interest in this research. Therefore, R-2R binary-weighted current DAC and segmented current DAC, which are suited architectures for high-speed applications, are mainly discussed in following sections.

2.2.1 R-2R Binary-Weighted DAC

Binary weighted DAC uses the binary input digital signal to directly control switches and output corresponding value in analog formation. The controlled unit value is binary weighted which means the value of each unit output is twice that of its previous one. The overall output value can be expressed as

$$X_{out} = I_{unit}(D_{N-1} \cdot 2^{N-1} + D_{N-2} \cdot 2^{N-2} + \cdots + D_0 \cdot 2^0) \tag{2.2}$$

where X_{out} is DAC's analog output, I_{unit} is the LSB current, D_{N-1} is the *N-th* digital input bit. Fig. 0.7 shows binary weighted current DAC implementation in two different formations.

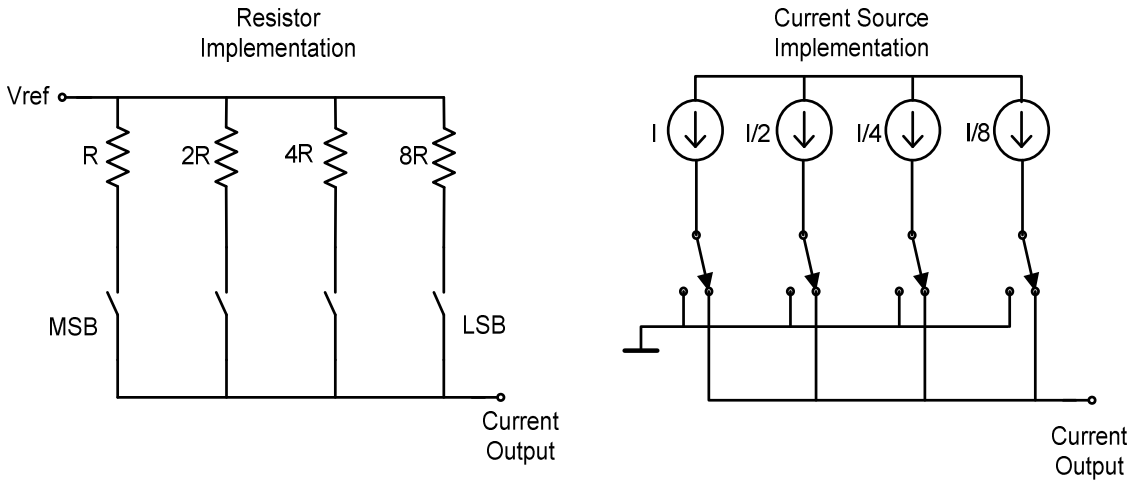

Fig. 0.7 Binary weighted current DAC implementation in two different formations

This type of DAC has several advantages such as very small switch cost and no additional decoder circuit, which means it can be easily implemented and area efficient. However, due to the limitation of matching accuracy in a technology, the mismatch between MSB and LSB is usually quite large which will prevent this structure to achieve more than 6-bit resolution. This mismatch not only worsen the static accuracy performance of DAC like INL and DNL, but also affect the monotonicity which is critical in some certain applications like sigma-delta modulation and system control.

The R-2R ladder implementation of binary weighted DAC, shown in Fig. 0.8, is one of the most common DAC building-block structures [28][29][30]. It uses resistors of only two different values and their ration is 2:1. This improves the DAC's overall precision due to the relative ease of maintaining good ratio matching all through LSB to MSB. However, this architecture with high resolution suffers from increasingly large RC-constants for each added R-2R link, which indicates, if no hybrid segmentation scheme is used, R-2R DAC cannot easily realize both high speed and high resolution at the same time.

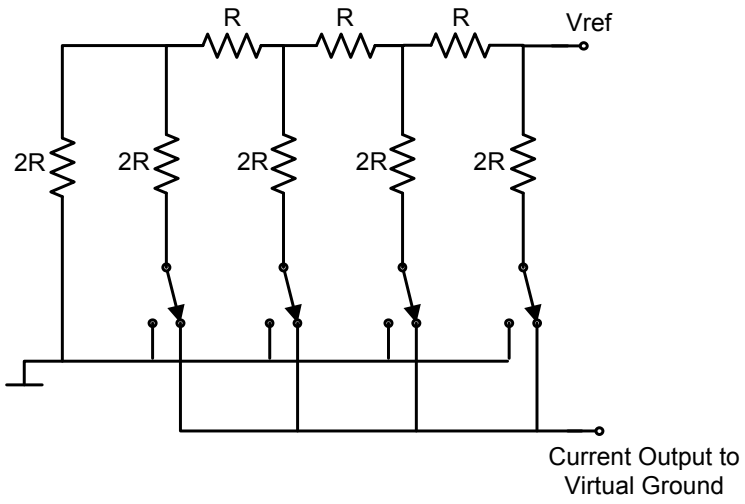

Fig. 0.8 Current mode R-2R binary weighted DAC

2.2.2 Hybrid Segmented Current-Steering DAC

The current-steering DAC is the most common and almost exclusive type of DAC for high-speed high-resolution applications when compared with other typical DAC architectures [31][32][33]. As shown in Fig. 0.9, this architecture provides a good balance between die size, power consumption, accuracy and dynamic performance. The thermo-code weighted DAC has several advantages over its binary weighted counterpart, such as low DNL, guaranteed-monotonicity and reduced glitch noise. For a high resolution, such as 12-bit, current-steering DAC, thermometer-coded segmentation for significant bits can be applied to shrink the chip area and reduce the currents through current switches [16][34]. There are two types of segmentation: full segmentation and hybrid segmentation. Full segmentation can guarantee good dynamic performance, monotonicity and reduce glitches because every level in the DAC has a switch with a reference current connected to this switch. However, full segmentation in high resolution converters is hard to implement due to worse jitter or time skews at high frequency, larger die size and increased circuit complexity. For example, in a 12-bit fully segmented DAC, there will

be 2^{12}-1 = 4095 switches which have to be addressed and switched at very accurate times. Hybrid segmentation is implemented by combining some segmentation in the MSB with a binary weighting for the LSB (Since thermo-code weighted DAC has better matching and more accuracy than binary weighted counterpart, to achieve good overall linearity for whole DAC system thermo-code and binary are employed for MSB and LSB, respectively), which can obtain a good accuracy and dynamic performance with an acceptable chip area and circuit complexity. Therefore, for a high resolution DAC design, there is a trade-off between how to segment the significant bits and the effect on layout complexity, glitches, monotonicity, precision, INL, DNL and speed [35][36].

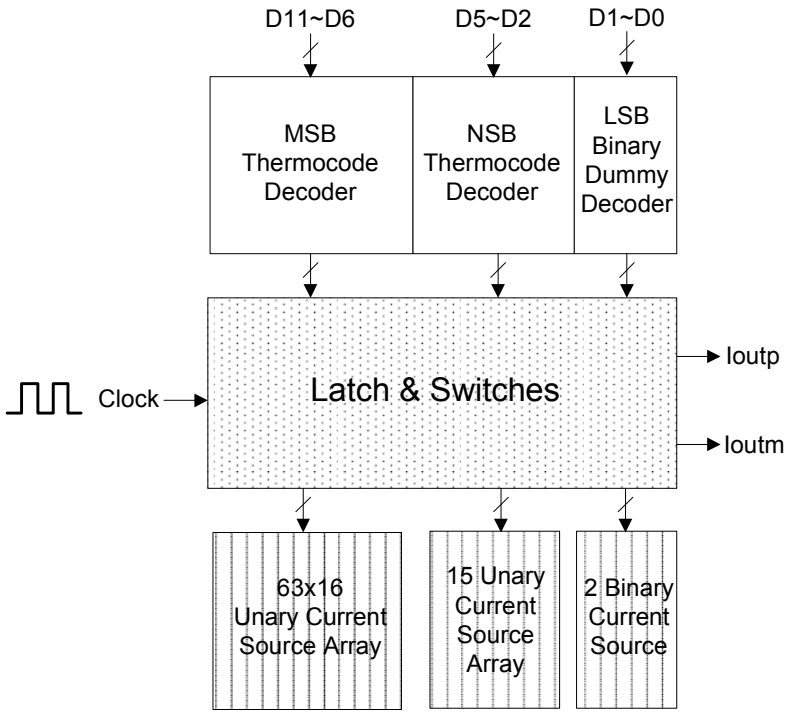

Fig. 0.9 Block diagram for a hybrid segmented current-steering DAC architecture

Chapter 3 High-Speed Flash ADC Designs

3.1 3-Bit 20GS/s Flash ADC

As digital signal processing (DSP) integrated circuits become increasingly complicated and sophisticated, higher operation speed is inevitably required in modern digital systems. Driven by the enhanced capability of DSP circuits, ADCs must necessarily operate at ever-increasing frequencies while maintaining the accuracy previously obtainable at only moderate speeds. This trend has put multi-giga sample per second ADCs in high demand for high-speed data acquisition systems like digital storage oscilloscopes, waveform digitizers and even direct sampling RF incident signal in broadband communications and radar[37].

Although a 10~20 GS/s 3~4-bit ADC in InP technology [38] and a 40 GS/s 3-bit ADC in SiGe technology [39] have been reported to demonstrate the capability of over 10 GHz sampling speed, their large power consumption and die area prevent them from being integrated in a single chip for software defined radio applications. In this section, a time-interleaved 3-bit flash ADC with low power consumption and small die area is presented for Ku-band software-defined-radio applications. A high-speed DAC is designed to form a complete data converter pair, which facilitates the ADC testing as well.

The 0.12 μm SiGe HBT technology is featured with a f_t/f_{max} of 210/310 GHz. The flash ADC architecture was chosen to achieve the maximum sampling frequency for the ADC design. The

CML circuits are adopted for digital logic implementations to provide fast switching speed. Finally, two identical flash ADCs are time-interleaved to double the conversion rate.

3.1.1 Flash ADC Architecture

As shown in Fig. 0.1, the proposed 3-bit ADC-DAC RFIC is composed of two 3-bit time-interleaved flash ADCs and one 3-bit DAC for ADC testing. Each ADC contains an SHA, current comparators, thermometer-to-gray coder and D-flip-flops (DFFs) for retiming and buffer. The outputs of the two ADCs are time-interleaved and combined using a high-speed multiplexer (MUX). In order to obtain the maximum sampling rate, a current-steering DAC is implemented. When ADC-DAC is in operation, the input analog signal is sampled by two S/Hs for both odd and even channel ADCs driven by out-of-phase clocks. The signals after S/H are compared with 7 current-mode comparators which are set with 7 successive offset currents representing the 7 quantization threshold levels. After thermometer-to-gray coder and DFFs, the original analog input signal is converted into digital signals with gray code weight. Due to time-interleaving, the digital outputs in every stage are needed to be multiplexed by a clock signal with double frequency to generate the desired output at the doubled sampling rate. The 3-bit DAC converts the digital signals back to an analog signal that can be tested and measured easily using a digital scope or a spectrum analyzer.

Fig. 0.2 shows the simplified schematic of the differential sample/hold amplifier used in the proposed ADC [40][41]. As known, the sample/hold amplifier can effectively eliminate the sampling jitters resulting from the phase noise in the sampling clock source and the sampling uncertainty of the ADC. In order to reach the highest operation frequency and improve noise rejection, an open-loop architecture and fully differential structure are employed, respectively.

The use of cascode structure in input and output amplifier stages can provide better isolation as well as avoids the breakdown problems of the SiGe HBTs in a 4.2 V power supply. The value of holding capacitor C_H is designed in the order of several hundred fF to ensure fast charging/discharging and a stable holding voltage at a 20 GS/s rate. In order to achieve better linearity, the product of total bias current and emitter degeneration resistor should be more than twenty times V_T [42].

Gray code is applied to simplify the coder/decoder logic circuits in order to obtain best speed performance [16]. Employing no more than three input CML cells, gray coder can cut the original four-stage logic (counting one gate and one emitter follower as one stage) to three-stage in the longest signal path of the LSB, compared to the traditional binary code. By saving one stage, the compensation circuits for balancing the propagation delay in other signal paths can also be removed so that lower power consumption and higher speed can be simultaneously achieved.

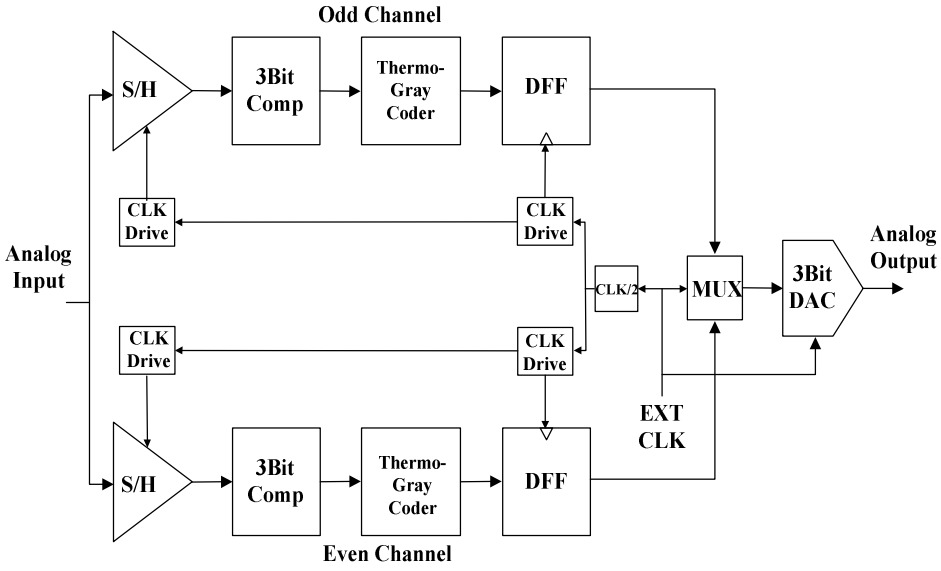

Fig. 0.1 Simplified block diagram for proposed 3-bit time-interleaved high-speed flash ADC and BIST DAC.

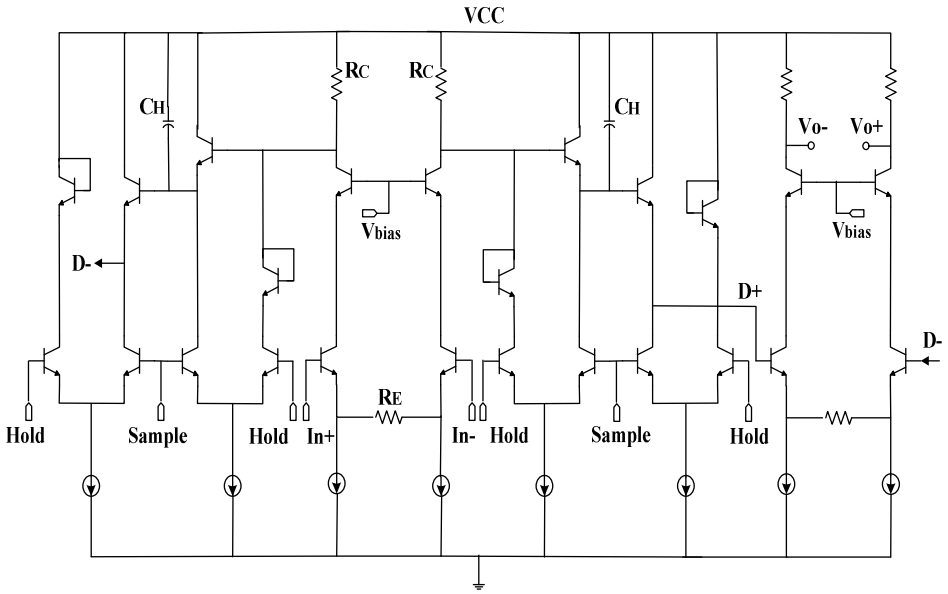

Fig. 0.2 Simplified schematic of differential sample/hold amplifier used in proposed ADC

As the key block of the flash type ADC design, current comparators convert the received analog input signal to digital outputs with different quantization threshold levels [39]. The accuracy and speed of the conversion directly affect the static and dynamic performance of the ADC, such as differential nonlinearity (DNL), integral nonlinearity (INL), signal-to-noise (SNR), spurious free dynamic range (SFDR) and effective number of bits (ENOB) etc. Unlike conventional voltage comparators using resistor network to set up the voltage threshold levels, current-mode comparators using active unit current sources can reduce parasitic RC effect in the crucial signal path during the conversion. As illustrated in Fig. 0.3, the signals coming from S/H are applied to a differential pair that has been optimally biased to realize the fastest switch speed. Meanwhile, pre-offset current which ranges from 0 to 7 unit currents will be added or subtracted from input analog signal at the collectors of the differential pair, based on the analog signal

magnitude. The current offsets play the same role as the voltage thresholds in a voltage-mode comparator for quantizing the input signal. To reduce the headroom lost through the degeneration resistors and to eliminate the mismatch caused by multiple resistors, only one degeneration resistor is used in the current comparators differential pair. Similarly, large bias current and emitter degeneration resistor should be used to increase its linearity range. In addition, the current comparator circuit needs to be redesigned after layout to take into consideration parasitic effects.

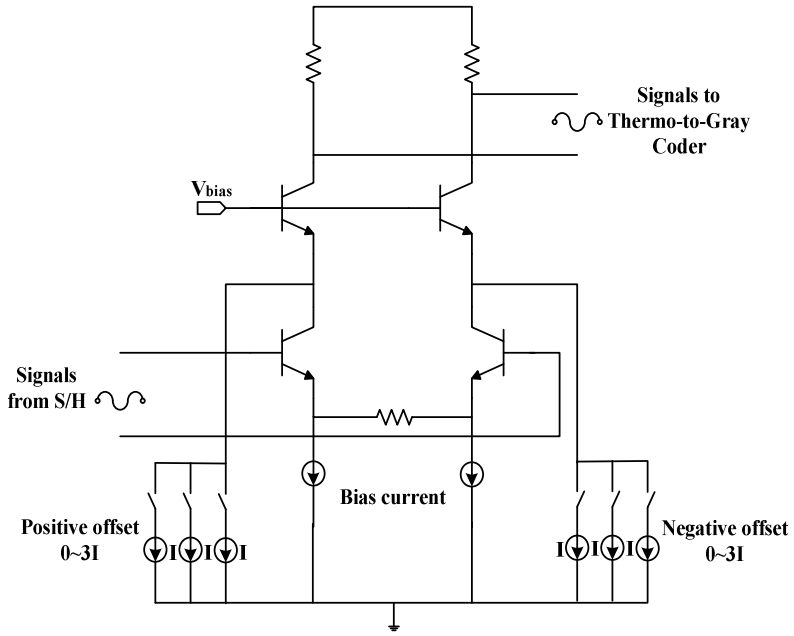

Fig. 0.3 Current comparator with quantization threshold levels set by the offset current.

3.1.2 Measurement Results

The 20GS/s 3-bit ADC and DAC were implemented in a 0.12 μm SiGe BiCMOS technology, as shown in the chip micrograph in Fig. 0.4. In order to demonstrate the software defined RF receiver, the ADC-DAC chip also includes a 10GHz RF front-end with an LNA and a VGA and a VCO generating the internal clock. The ADC circuit occupies 1.5 x 1.7 mm^2 die

area and the 3-bit DAC takes an area of 0.5 x 1.0 mm^2. Operating at a 20 GS/s sampling rate with a single 4.2 V power supply, the total power consumption of the ADC and the DAC is 2.36 W.

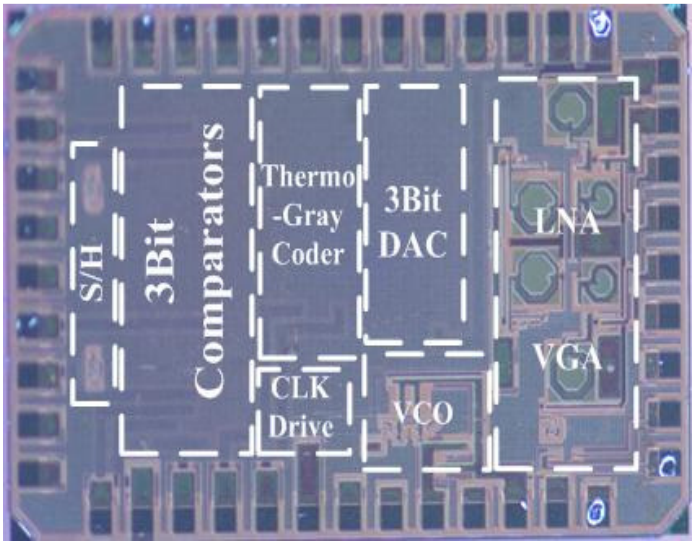

Fig. 0.4 Microphotograph of proposed 3-bit time-interleaved 20GS/s flash ADC chip

For Ku-band testing, the PCB test board was developed using a Rogers RO4003 laminate board, which has a loss tangent of less than 0.003 and good temperature stability. To convert the single-ended signal to differential inputs needed to drive the chip, a 180 degree 3dB hybrid coupler is employed at the clock input. For the differential output, another hybrid coupler is inserted into the output path. The ADC/DAC chip is packaged in a 44-pin ceramic leadless chip carrier (CLLC) package. The junction-to-ambient thermal resistance θ_{JA} of the ceramic package is about 40 °C/W with zero air flow. Therefore, the device junction temperature of the ADC/DAC chip could reach above 100°C at the room ambient temperature with 2.3W power consumption. For this reason, an external fan is used to cool the device during measurements.

The θ_{JA} of the package is estimated as 30 °C/W with the fan air flow. All measurements were done using packaged prototypes, while other reported high-speed ADCs were tested on wafer [39], which has less problems associated with the package heat dissipation and bonding wire effect.

Fig. 0.5 shows the measured 40 MHz sinusoidal time domain waveform reconstructed by the on-chip DAC with a 20 GS/s sampling rate. The 8 step quantization is clearly shown in the waveform without de-glitch low pass filter after the DAC, which verifies the proper operation of both the ADC and the DAC functions. Fig. 0.6 gives the measured DAC output spectrum for a 1.5 GHz ADC input signal at 20 GS/s sampling rate. The Measured SFDR, signal-to-noise-distortion-ratio (SNDR) and ENOB under this condition are 23.2 dBc, 18.6 dBc and 2.8 bits, respectively. It demonstrates a good dynamic performance for the 3-bit ADC-DAC pair.

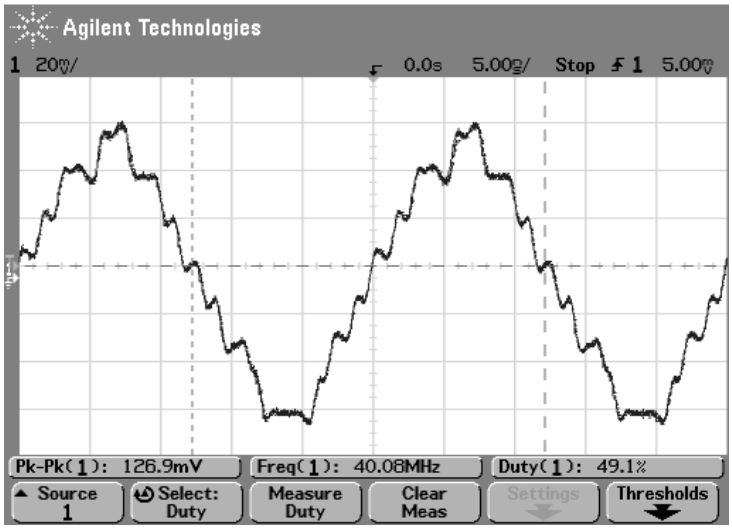

Fig. 0.5 Measured DAC output waveform showing 8 step quantization of a 40 MHz input signal sampled at 20 GS/s rate.

The measured SFDR for different ADC input frequencies at the maximum sampling rate of 20 GS/s is given in Fig. 0.7. The maximum dynamic range the implemented ADC-DAC can achieve is 30.5 dBc with a 4.2 GHz ADC input. For larger than 20 dBc SFDR, the ADC achieves an input bandwidth larger than 5.5 GHz. When the ADC input frequency is close to the Nyquist frequency, the dynamic performance is degraded due to the channel mismatch in odd and even channels of the time-interleaved ADC and the bandwidth limitation of the S/H circuit.

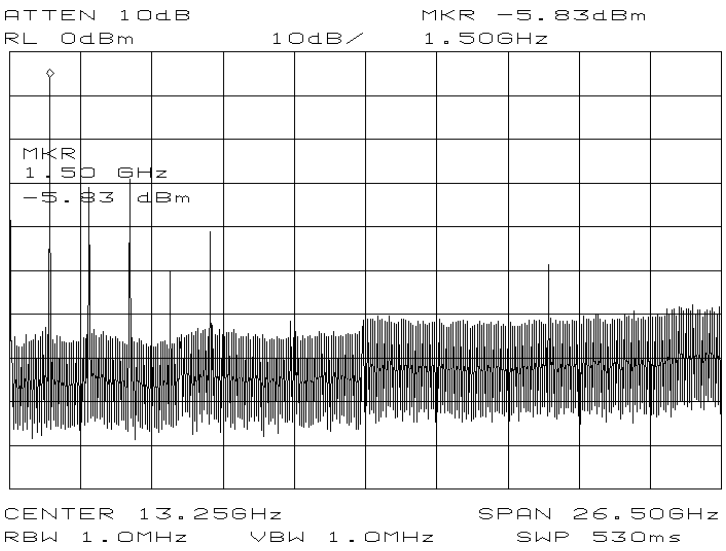

Fig. 0.6 Measured DAC spectrum for 1.5 GHz input signal at the sampling rate of 20 GS/s.

The performance comparison of the 3-bit flash ADCs operating at above 10 GS/s sampling rate is shown in Table 1. Note that other reported ADCs except this work were measured by wafer-probe, while this ADC and DAC were tested with packaged chips. Considering the performance degradation due to the package effects, this work demonstrates a good SFDR and ENOB with low power consumption and small die area. As a result, the proposed ADC and DAC provide an efficient means for data conversion in software defined radios.

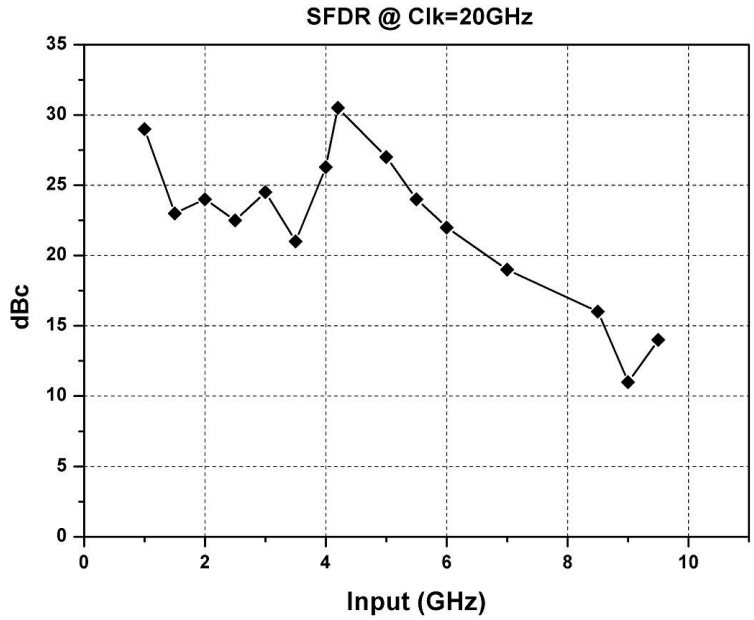

Fig. 0.7 Measured SFDR for 3-bit ADC-DAC pair as a function of input frequency at the sampling rate of 20 GS/s.

Table 1 Performance comparison of ultra-high speed ADCs.

	[38]	[39]	[43]	**This work**
Sample Rate (GS/s)	10	40	24	20
SFDR / Input (dBc / GHz)	30.1/6	33/9	25/6	30.5/4.2
ENOB / Input (bits / GHz)	2.8/1	2.8/0.05	2.3/10	2.8/1.5
Power Supply (V)	4	--	-4	4.2
Power (W)	4.25	4.46	3.84	2.36
Technology (- / f_T in GHz)	InP/80	SiGe/210	InP/150	SiGe/210
Die Area (mm^2)	--	2.2 x 1.8	3 x 3	1.5 x 1.7
Figure of Merit (Power/2^{ENOB}*2*f_s) (pJ/step)	30.5	8.0	16.2	8.5
Test Prototypes	Wafer	Wafer	Wafer	Packaged

3.1.3 20GS/s Flash ADC Summary

A 3-bit ADC for software defined radio applications that can work at a sampling rate of 20 GS/s is presented. In order to operate at Ku-band, two flash CML ADCs are time-interleaved to achieve a 20GHz sampling rate. A 3-bit current-steering DAC is also designed for testing the high-speed ADC. The ADC-DAC RFIC is implemented in a 0.12 μm SiGe technology and occupies an area of 1.5 x 1.7 mm^2. The total power consumption for the entire ADC-DAC chip is 2.36 W with a 4.2 V power supply. The ADC-DAC RFIC is packaged in a 44-pin CLLC package and achieves a peak SFDR of 30.5 dBc and a peak ENOB of 2.8 bits at a 20 GS/s sampling rate.

3.2 3-Bit X-band Low-Power ADC

Analog-to-digital converters with X-band sampling rates are critical components for applications such as digital oscilloscopes, waveform recorders and radar signal capture, etc [44]. Meanwhile, the development of modern communication and wireless applications requires the next generation receivers to have higher data transmission rates and lower power consumption. By moving the ADC closer to the system front-end, the majority of the processing can be performed in the digital domain [45]. ADCs with X-band sampling capability make it possible for next generation receivers to digitize the received signal at radio frequency instead of baseband frequency which will greatly simplify the radio architecture. To take advantage of the increasing speed and complicity of digital signal processing, ADCs in the above applications are required to be implemented with small area and low power as well as fast sampling rates. Although a 10~20 GS/s 3~4-bit ADC in InP technology [38] and a 40 GS/s 3-bit ADC in SiGe technology [39] have been reported to demonstrate the capability of over 10 GHz sampling speed, their multi-watt power consumption, high supply voltage and large die area prevent them

from being integrated in a single fully-integrated transceiver chip for X-band frequency applications. In this section, a 3-bit Flash ADC demonstrates good X-band sampling rate performance with the lowest power supply voltage, lowest power consumption, smallest core area[46].

To achieve the maximum sampling frequency for the ADC design, the flash ADC architecture is chosen and the CML circuits are adopted for digital logic implementation to provide fast switching speed. Meanwhile, the 0.12 μm SiGe HBT technology featured with f_t/f_{max} of 210/310 GHz is used to enhance the device operation speed. Finally, low power supply voltage is used to minimize total power consumption and avoid breakdown issues in HBTs and FETs in the technology. As a built-in-self-test (BIST) block for the X-band ADC, a 3-bit current-steering high speed digital-to-analog converter (DAC) is included in this design to ease problems with data acquisition of multi-GHz digital signals.

3.2.1 Building Blocks for High-Speed Flash ADC

As shown in Fig. 0.8, the proposed 3-bit ADC-DAC RFIC is composed of a 3-bit flash ADC and a 3-bit DAC for ADC testing. The ADC contains a 7-level current comparator, thermometer-to-gray decoder and D-flip-flops (DFFs) for retiming and buffering. A current-steering type DAC is used to obtain maximum sampling rate. During operation, the input analog signal is compared with 7 current-mode comparators which are set using 7 successive offset currents representing the 7 quantization threshold levels. Digital outputs can be obtained after thermometer-to-gray decoder and DFFs. The reconstructed analog signal by 3-bit DAC can be directly measured from the using a digital oscilloscope or a spectrum analyzer.

With a 2.2 V low voltage power supply, the CML circuit can only realize two level logic which will prolong the critical signal path and consequently increase inter-stage delay. Gray code is applied to mitigate the low power supply effect and obtain best speed performance by simplifying the decoder logic circuits [16].With a two level logic CML circuit, the gray decoder can cut the original three-stage logic (counting one gate and one emitter follower as one stage) to two-stage in the longest LSB signal path, compared to the traditional binary decoder. By saving one stage, the compensation circuits for balancing the propagation delay in other signal paths can also be removed so that lower power consumption and higher speed can be simultaneously achieved. Due to the limitation of 2.2 V power supply voltage, the head room for the bottom current source transistor is only about 300 mV. Because of the small amount of headroom, a BJT is not used for the bottom current source. Despite a smaller transconductance compared with the BJT, a FET with large enough width should be used to ensure that it operates in saturation region. Decoupling capacitors are also needed on the gates of some critical current source FETs such as comparators and the DAC output stage.

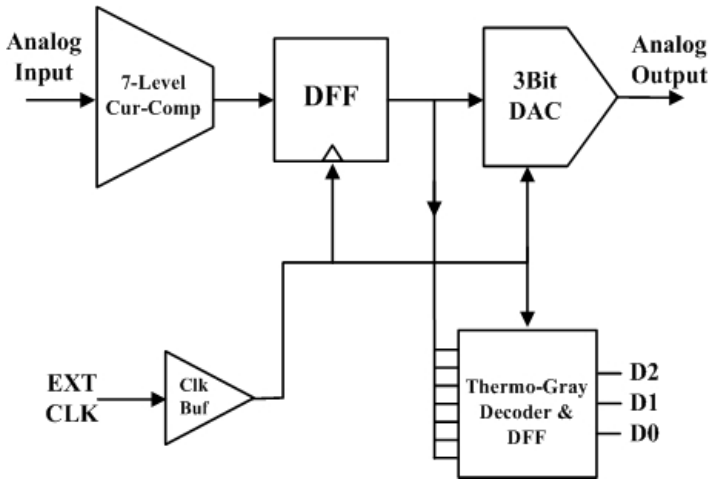

Fig. 0.8 Simplified block diagram for proposed 3-bit high-speed flash ADC and BIST DAC.

In flash type ADCs, current comparators convert the received analog input signal to digital outputs by setting different quantization threshold levels [39]. The accuracy and speed of the conversion directly affects almost all of its static and dynamic performance, such as differential nonlinearity (DNL), integral nonlinearity (INL), signal-to-noise (SNR), spurious free dynamic range (SFDR) and effective number of bits (ENOB). Unlike the resistor network used to set up voltage thresholds for conventional ADCs, current-mode comparators using active unit current sources can reduce parasitic RC effects in the crucial signal path during the conversion. As shown in Fig. 0.9, the current offsets set up by different current sources play the same role as the voltage thresholds in a voltage-mode comparator for quantizing the input signal. Large bias current and emitter degeneration resistors should be used to increase the linearity range [42]. For X-band application, the current comparator circuit needs to be redesigned post layout to take into consideration the parasitic RC effects.

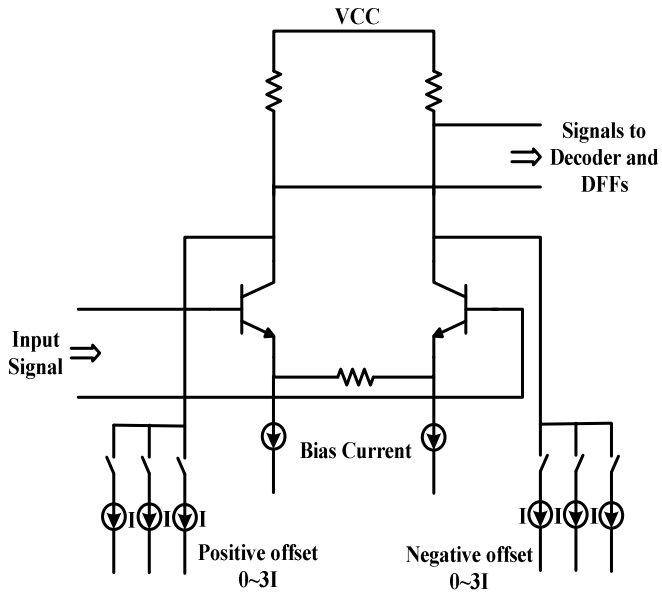

Fig. 0.9 Current comparator with quantization threshold levels set by the offset current.

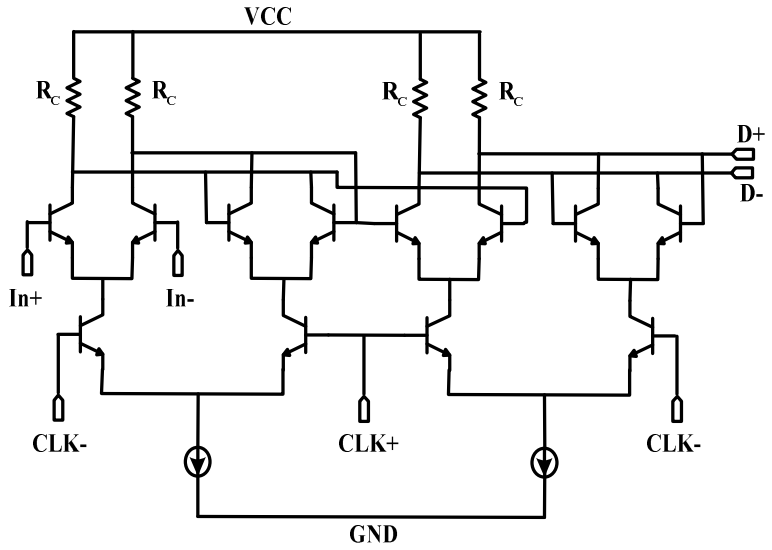

Fig. 0.10 Schematic for DFF used in this high-speed ADC.

Fig. 0.10 show the topology of the DFF used in this design. Due to the low-voltage design with a 2.2 V power supply, although emitter followers between two-stage D latches are often used to suppress the kickback noise and isolate the unbalanced interference from the succeeding stages [45], they must be removed to provide enough headroom for the following clock input stage to make sure correct operation of the D latch. In the DFF design, larger bias current and larger HBT devices are used in the second D latch in order to offer better driving strength for the following stages, which also improves the capacitance loading effect at outputs nodes, leading to an increased DFF speed.

3.2.2 Implementation and Experimental Results

The 11GS/s 3-bit ADC is implemented in a 0.12 μm SiGe BiCMOS technology, as shown in the chip micrograph in Fig. 0.11. For an integrated radar application, the ADC chip was embedded in a radar receiver MMIC that includes a 16 GHz RF front-end with an LNA and a mixer. The ADC circuit occupies 0.7 x 0.6 mm^2 die area and the 3-bit DAC takes an area of 0.3 x 0.6 mm^2. Operating at an 11 GS/s sampling rate with a single 2.2 V power supply, the power consumption of the ADC is only 0.22 W. This ADC realizes the lowest power supply voltage, lowest power consumption and smallest core area in all reported X-band ADC designs.

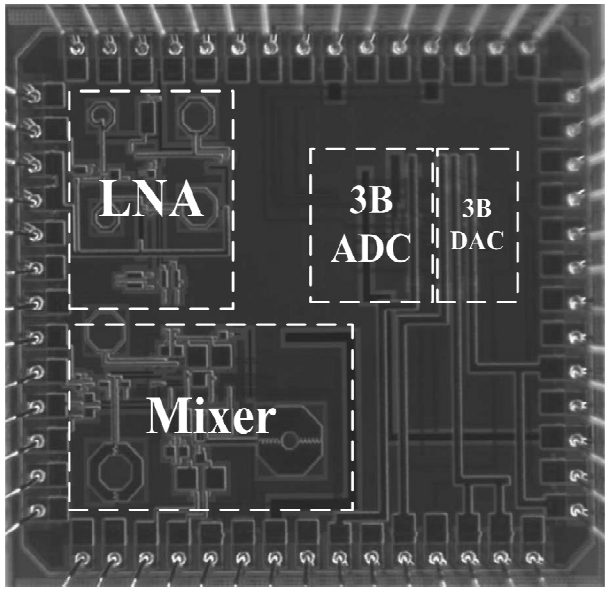

Fig. 0.11 Microphotograph of the 3-bit 11GS/s flash ADC-DAC RFIC chip.

For X-band testing, a Rogers RO4003 laminate PCB with a loss tangent of less than 0.003 is developed to provide good high frequency performance and temperature stability. At the DAC differential outputs, a 180 degree 3 dB hybrid coupler is used to provide differential-to-single-ended conversion for a spectrum analyzer to test the spectral performance of the overall ADC-

DAC RFIC. During the measurement, the SINC roll-off from the DAC reconstruction must be considered to give the accurate results. All measurements were done using CLLC packaged prototypes, while other reported high-speed ADCs [3][4][7] were all tested on wafer, which has less problems associated with the package heat dissipation and bonding wire parasitic effect.

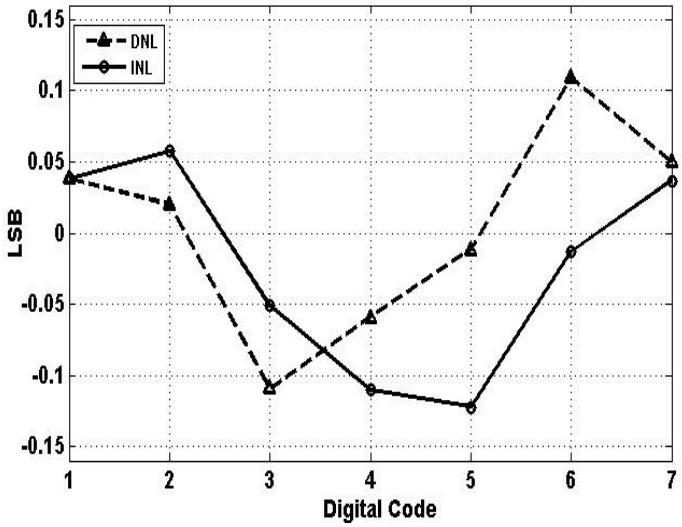

Fig. 0.12 Measured ADC DNL/INL at an 11GS/s sampling rate..

Typical DNL and INL plots, which are measured at an analog input frequency of 2 MHz at the 11GS/s sampling rate, are shown in Fig. 0.12. The DNL is less than ±0.11 LSB and the INL is less than ±0.12 LSB. The DNL and INL are limited by the matching properties of the current source and differential pairs in current comparators. They can be further improved by using larger area devices, but this will affect the analog input bandwidth of the ADC.

The measured ADC output waveform reconstructed by the on-chip DAC given in Fig. 0.13 clearly demonstrates the 8 quantization steps with an 11 GS/s sampling rate. Fig. 0.14 gives the measured DAC output spectrum for a 1.102 GHz ADC input signal at 11GS/s sampling rate.

The measured SFDR, SNDR and ENOB under this condition are 26.5 dBc, 17.8 dBc and 2.7 bits, respectively. It demonstrates a good dynamic performance for the 3-bit ADC-DAC RFIC.

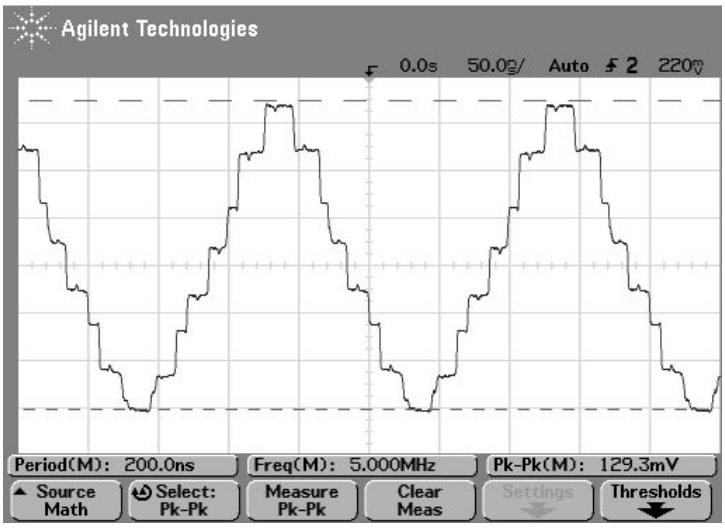

Fig. 0.13 Measured ADC/DAC output waveform with 8 quantization steps at an 11GS/s sampling rate.

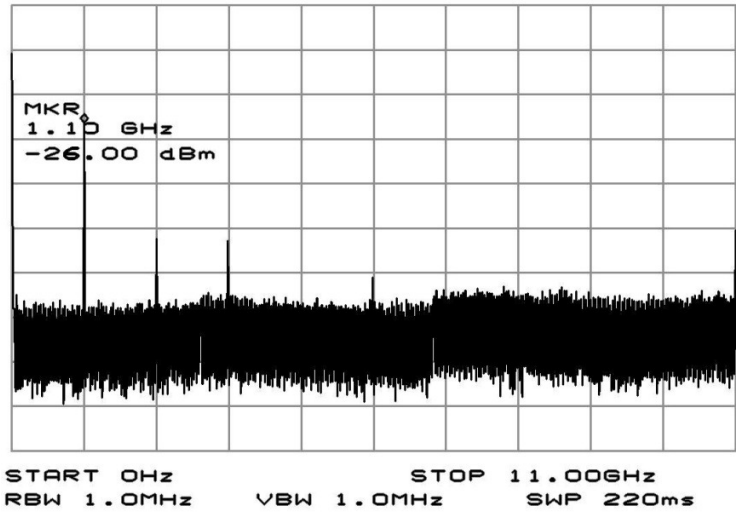

Fig. 0.14 Measured output spectrum of the ADC-DAC pair for a 1.102 GHz input signal with the sampling rate of 11 GS/s.

The measured SFDR for different ADC input frequencies at the maximum sampling rate of 11GS/s is given in Fig. 0.15. The maximum dynamic range of the implemented ADC-DAC is measured as 28 dBc with a 1.5 GHz ADC input. For larger than 20 dBc SFDR, the ADC achieves an input bandwidth larger than 3.5 GHz. The ADC dynamic performance will be improved once a track-and-hold amplifier is applied at the input stage of the ADC with additional power consumption. The performance comparison of the 3-bit flash ADCs operating at above 10 GS/s sampling rate is given in Table 2. The presented ADC realizes the best FOM of 3.08 pJ/conversion-step with a 2.2 V power supply and 0.22 W power consumption implemented in a 1.0 x 0.8 mm^2 core chip area. In addition, this ADC was the only one measured using packaged parts, while all other mm-wave ADCs were measured using wafer-probe.

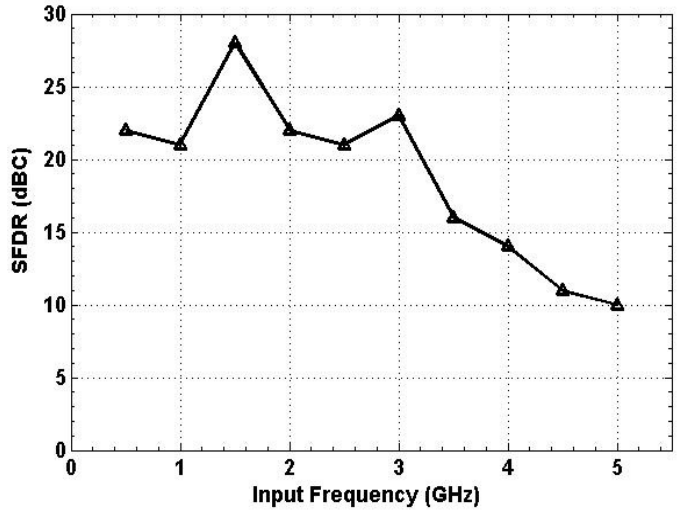

Fig. 0.15 Measured SFDR for 3-bit ADC-DAC pair as a function of input frequency at the sampling rate of 11GS/s.

Table 2 Performance comparison of mm-wave ADCs.

	[38]	[39]	[43]	**This work**
Sample Rate (GS/s)	10	40	24	**11**
SFDR / Input (dBc / GHz)	30.1/6	33/9	25/6	**28/1.5**
ENOB / Input (bits / GHz)	2.8/1	2.8/0.05	2.3/10	**2.7/1.102**
Power Supply (V)	4	--	-4	**2.2**
Power (W)	4.25	3.8	3.84	**0.22**
Technology (- / f_T in GHz)	InP/80	SiGe/210	InP/150	**SiGe/210**
Die Area (mm^2)	--	2.2 x 1.8	3 x 3	**1.0 x 0.8**
FOM($Pw/2^{ENOB}*f_s$) (pJ/step)	61.0	16.0	32.4	**3.08**
Test Prototypes	Wafer	Wafer	Wafer	**Packaged**

3.2.3 X-Band Flash ADC Summary

A 3-bit ADC for X-band applications that can work at a sampling rate of 11 Gs/s is presented. Flash architecture, CML circuits and current comparators are used to achieve the high sampling rate at X-band. To test the ADC, a 3-bit current-steering DAC is also included in this design. The ADC-DAC RFIC is implemented in a 0.12 μm SiGe technology and occupies a core area of 1.0 x 0.8 mm^2. The ADC operates with 0.11 LSB DNL, 0.12 LSB INL and a FoM of 3.08 pJ/conversion-step by consuming 0.22 W power with a 2.2 V power supply. At the X-band sampling rate, the ADC has the lowest power supply voltage, lowest power consumption, smallest core area and best FoM reported so far. Tested in a 44-pin CLLC package, the X-band ADC achieves a peak SFDR of 28 dBc and a peak ENOB of 2.7 bits at 11 Gs/s.

Chapter 4 High-Speed and Low-Power Pipeline ADC Designs

Pipeline ADC is currently the most popular structure in a variety of ADC architectures due to its good balance between high speed and high resolution. In contrast, other structures are hard to achieve both high speed and high resolution at the same time. Although several different implementation methods are available for pipelined ADC, switched-capacitor (SC) structure is particularly popular because of its capability of high-precision sampling and residue amplification. The resolution of the SC pipeline structure is mainly limited by the matching of the capacitors and the error introduced by the finite gain of OpAmp. Speed-wise, the settling time and gain bandwidth product of OpAmp determines the overall conversion rate for whole pipeline ADC system. Meanwhile, as the most power-hungry component in all pipeline ADC building blocks, OpAmp also needs to lower its power dissipation to effectively meet the requirement of low-power design. As a result, as the key building block of pipeline structure, an OpAmp with large DC gain, wide gain bandwidth product and low power consumption is a must for a pipeline ADC featuring high-speed, high-resolution and low-power. Several design techniques and considerations for OpAmp implementation are carefully studied with in-depth technical discussion. In addition, aforementioned time-interleaving technique is employed to further enhance ADC's sampling rate at the cost of more power consumption, more component usage and larger die area.

4.1 OpAmp Sharing Pipeline Architecture

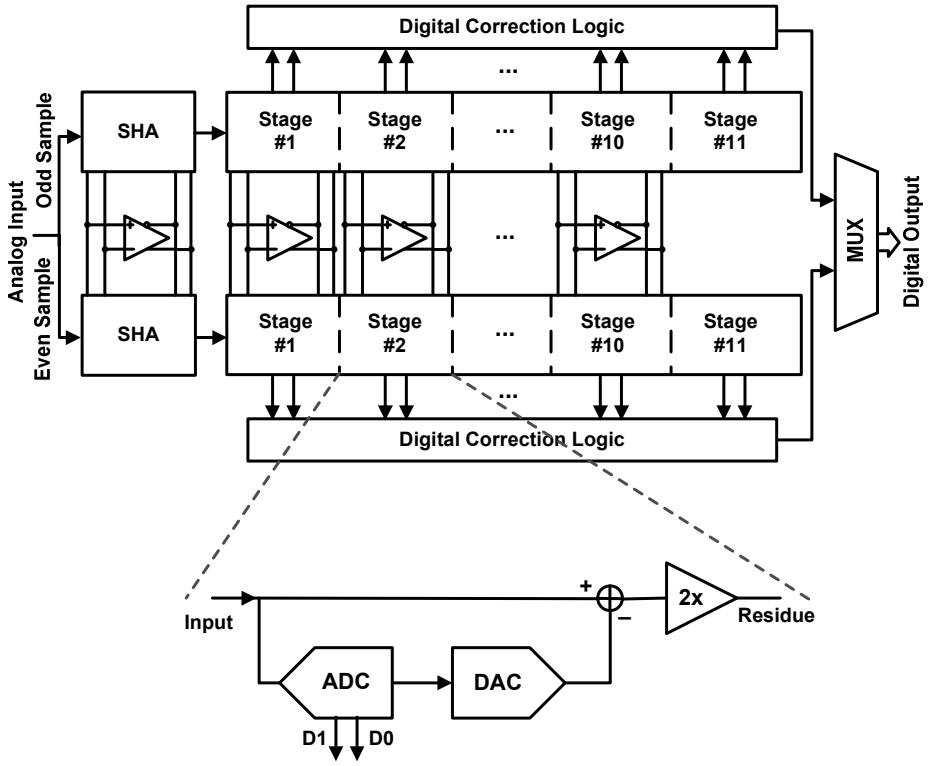

Fig. 0.1 Block diagram of time-interleaved OpAmp sharing pipeline ADC

Fig. 0.1 gives the block diagram of proposed 12-bit low-power time-interleaved OpAmp sharing pipeline ADC. It consists of two eleven-stage 1.5-bit/stage time-interleaved pipeline ADCs. One pipeline processes the even samples, while the other pipeline works on odd samples. For both pipeline ADC channels, two clock phases, multiplying and sampling, are used and complementary for each other. However, the OpAmp only works in multiplying phase for every single channel, which is half of one complete clock cycle. Thus, both pipeline ADCs are capable of sharing their OpAmps by only using corresponding multiplying clock phase. This makes a large power saving since as mentioned earlier OpAmp is the most power-consuming component

in pipeline architecture. In addition, it can also help to minimize offset and gain mismatches between pipelines that could degrade the ADC's performance [47]. Note that there is no OpAmp required in last stage which only uses comparator to generate two LSBs.

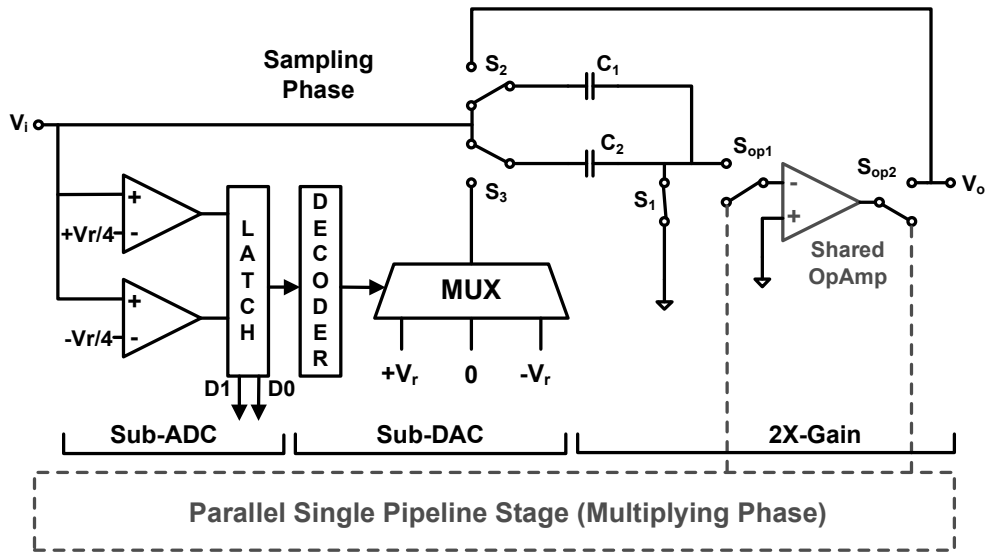

Fig. 0.2 Simplified schematic of single 1.5b/stage pipeline stage. Upper stage is sampling the input signal while lower stage is multiplying the residue.

Each pipeline stage includes a 3-level flash sub-ADC, a 3-level sub-DAC, and a residue doubler. In operation, each stage initially samples and holds the output from the previous stage and the held input is then converted into a low resolution digital code by the sub-ADC and back into an analog representation by the sub-DAC. Finally, the OpAmp residue doubler amplifies the difference between the held analog signal and the reconstructed analog representation to give the residue for the next stage. As shown in Fig. 0.2, the sharing of the OpAmp is realized by adding controlling switches between OpAmp inputs and outputs. When upper pipeline stage is in sampling phase, the OpAmp is not needed to finish the input signal sampling action on both C_1 and C_2 which can be done by switching on S_2 and S_3. Meanwhile, S_{op1} and S_{op2} switch shared

OpAmp to lower stage to multiply the residue. In next half clock phase, shared OpAmp is switched back to upper stage for multiplying and lower stage goes into sampling phase. S_2 and S_3 are also switched back to OpAmp circuit to realize residue doubling according to generated digital code. Note that although single-end system is shown in Fig. 0.2, differential signal processing is actually used in proposed pipeline ADC.

The input signal for each stage ranges from $-V_{ref}$ to $+V_{ref}$, the same as the input range for whole ADC, and the sub-ADC has two comparator thresholds at $-V_{ref}/4$ and $+V_{ref}/4$. Therefore, the residue transfer function is

$$V_{OUT} = \begin{cases} 2V_{IN} - V_{REF} & if \quad +V_{REF}/4 < V_{IN} \\ 2V_{IN} & if \quad -V_{REF}/4 < V_{IN} < +V_{REF}/4 \\ 2V_{IN} + V_{REF} & if \quad V_{IN} < -V_{REF}/4 \end{cases} \tag{4.1}$$

The corresponding binary digital outputs are 10, 01, and 00, respectively. The residue-amplifying gain in each stage is lower, 2x instead of 4x, and there are more stages, 11- instead of 6- than the 2-bit/stage architecture because digital error correction are employed. By reducing inter stage gain and introducing redundant bits, the stringent accuracy requirements on the sub-ADCs are greatly alleviated. The redundancy allows the implementation of a digital correction circuit that eliminates the comparator's offset effects [24]. In this case, a maximum comparator offset of $V_{ref}/4$ can be tolerated before the bit errors occur. The transfer curve for single 1.5b/stage pipeline ADC stage is shown in Fig. 0.3.

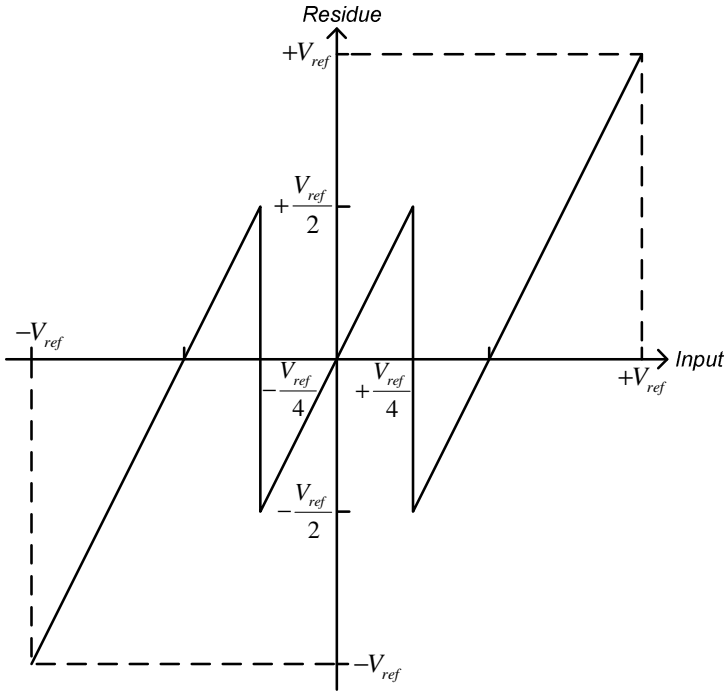

Fig. 0.3 Transfer curve for single 1.5b/stage pipeline ADC

Finally, a total of 22 bits from 11 stages are generated and combined using digital correction to give 12 effective bits at the final output of whole ADC chain. The bits are combined as follows,

$$D_{OUT} = \sum_{i=1}^{n} 2^{n-i} D_i \tag{4.2}$$

where n is the total number of stages, 11 for the proposed ADC, and D_i is the output code for the i-th stage.

4.2 Building Block Design for High-Speed and Low-Power

4.2.1 Sample and Hold Amplifier Design

Fig. 0.4 shows the schematic of the front-end sample-and-hold amplifier, which uses the

conventional flip-around configuration. This flip-around structure obtains the input on the sampling capacitors during the track phase, and flips the same capacitors to make the sampled voltage transparent to the output during the hold phase. Unlike the famous precise SC doubler used in each pipeline ADC stage, the OpAmp used in flip structured SHA does not have to provide the charge to the sampling capacitor in following stage, which can significantly enhance its speed performance and realize low noise and fast settling behavior [24][48]. Similar to each pipeline stage, SHA also uses OpAmp sharing technique to save required power. By using ϕ_1 and ϕ_2 non-overlapping clocks, OpAmp can be switched between two time-interleaved channels according to corresponding sampling/holding phases.

In order to achieve high accuracy for sampled voltage on sampling capacitor in SHA, bottom-plate sampling technique is employed. Still in Fig. 0.4, ϕ_1 and ϕ_2 are non-overlapping clocks to control the turn-on or –off of the switches in SHA. During the sampling phase, clock ϕ_1 controlled switches are turned off later than ϕ_{1e} switches to eliminate the sampling error due to the charge injection effect of the switches. In high-speed low-voltage designs, the MOS switch's turn-on resistance plays a key role on the performance of tracking speed and settling time. Furthermore, the turn-on resistance has a nonlinear voltage dependence, which leads to distortion when tracking continuous time signals. To reduce the turn-on resistance, a voltage higher than the supply can be used to control the sampling switches to maintain a large overdrive voltage. Thus, the typical bootstrap technique [47][49][50], whose schematic is also shown in Fig. 0.4, is utilized. The transistor gate voltage of sampling switch, S12, is locally boosted by a built in charge pump circuit. It is also possible to have the sampling switch gate voltage track the switch input voltage with the constant overdrive voltage. This brings two significant advantages. First, the reliability for sampling transistors is improved since the gate-drain voltage never exceeds the

power supply voltage and free from potential break-down problem. Second, with the constant overdrive voltage, the turn-on resistance becomes almost constant, which significantly reduces the distortion and improve the sampling accuracy.

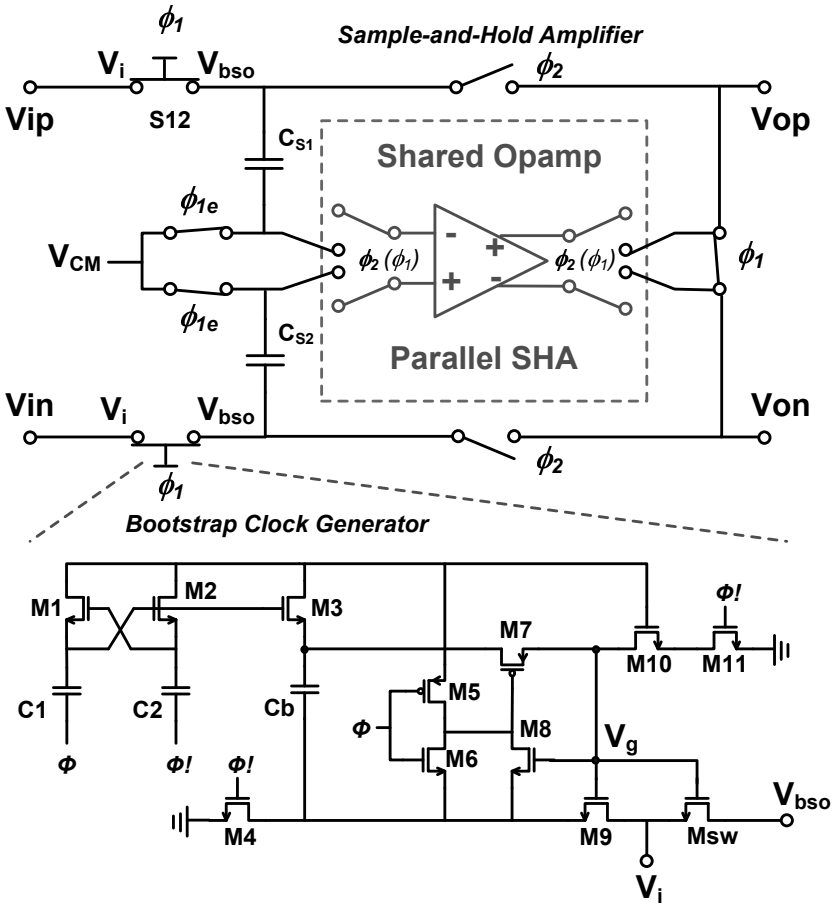

Fig. 0.4 Schematic for SHA and bootstrap clock generator

Bootstrap clock generator uses only a single phase clock ϕ to generate required boosted gate voltage for sampling transistor, M_{sw}, in SHA. When ϕ is low, M10 and M11 reset the gate of M_{SW} to ground and SHA is in holding phase. Meanwhile, M4 and M3 pass the power supply voltage Vdd to capacitor Cb that acts as a battery with Vdd voltage across the gate and the source

during the sampling phase. M7 and M9 are used to isolate M_{sw} from Cb while it is in holding phase. When ϕ becomes high, M6 pulls down the gate voltage of M7 to allow the charge on Cb to apply on the M_{SW} gate. This high voltage will turn on M9 and M_{SW} at the same time. M9 makes the sampling transistor M_{SW} capable of tracking the input signal. As a result, the voltage drop between gate and source of M_{SW} is almost constant, if don't count the charge loss, and reaches to Vdd. The bulk of M8 is tied to its source to reduce body effect and lower the possibility of latch up. M1,2 and C1,2 build up a clock multiplier to provide M3 with gate voltage that can be over Vdd. This can guarantee that M3 will continue to charge C_b even if the input signal is close to power supply voltage. In addition, due to the added capacitance for clock ϕ, larger driving capability is needed for clock buffer used in SHA block. Fig. 0.5 shows the conceptual bootstrap clock generator output. As mentioned above, the input-independent Vgs of sampling transistor can keep the turn-on resistance constant and also input-independence, which will significantly contribute to smaller distortion and better sampling accuracy.

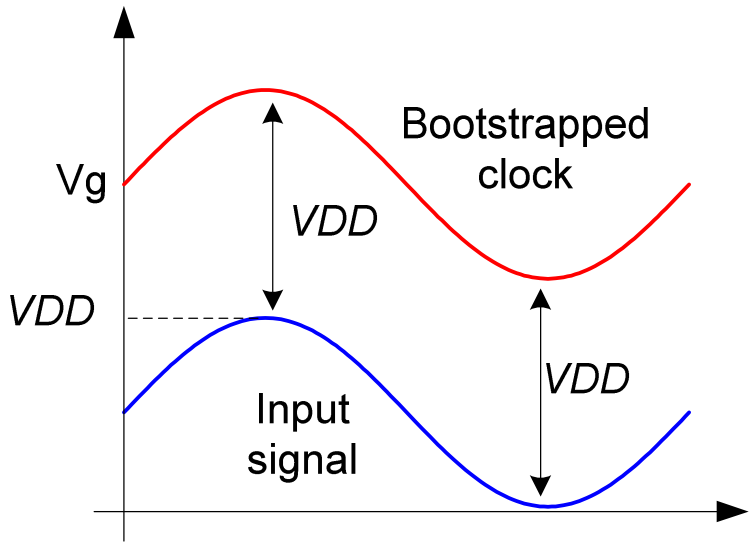

Fig. 0.5 Bootstrapped clock signal for time-interleaving SHA.

Another important component in SHA is sampling capacitor, which is closely related to the accuracy of sampled voltage and determines how many resolution bits the whole ADC system can reach. Matching of sampling capacitors in different channels of time-interleaving architecture is crucial to ADC's monotonicity and resolution. More importantly, capacitor value dominates both sampling rate and thermal noise performance for whole ADC [51][52]. Fig. 0.6 shows a simplified model for switched capacitor sampling circuit, where C is the sampling capacitor, R is turn-on resistance for sampling transistor, V_{in} is signal input and V_n is signal output.

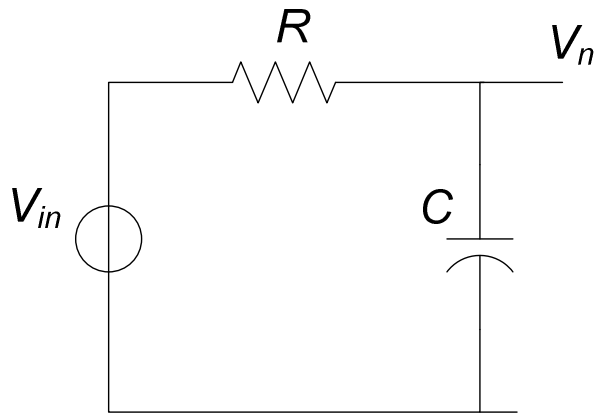

Fig. 0.6 Simplified model for SC sampling circuit

Its transfer function is

$$V_n(s) = V_{in}(s)\frac{1}{1+sRC} \tag{4.3}$$

Correspondingly, its output noise spectral density can be written as

$$S_n(f) = S_r(f)\left|\frac{1}{1+j2\pi fRC}\right|^2 \tag{4.4}$$

Thus, the expected noise power at output port is

$$\begin{aligned} v_n^2 &= 4kTR\int_0^\infty \frac{1}{1+(2\pi fRC)^2}df \\ &= \frac{4kTR}{2\pi RC}\int_0^\infty \frac{1}{1+x^2}dx \\ &= \frac{2kT}{\pi C}\int_0^{\frac{\pi}{2}} d\theta = \frac{kT}{C} \end{aligned} \tag{4.5}$$

Eq. (4.5) is the famous *kT/C* equation and places a fundamental limitation on SC sampling circuit. Interestingly, the noise on sampling capacitor is independent of the value of switch's turn-on resistance and inversely proportionally to capacitor value. This means that in order to achieve higher resolution, capacitor value is needs to be increased to lower the output noise, which will dramatically degrade the sampling speed performance because more time is required to charge a larger capacitor. Although this fundamental trade-off existing between speed and resolution for SC sampling circuit prevents ADC from obtaining both high-speed and high-resolution at the same time, it still give us some very useful guidelines to finalize design parameters. The root-mean-square (rms) quantization noise for a N-bit ADC is given by

$$V_{Q\sigma} = \frac{V_{LSB}}{\sqrt{12}} = \frac{V_{PP}}{2^N \cdot \sqrt{12}} \tag{4.6}$$

where V_{LSB} and V_{PP} are the LSB step size and full scale for a N-bit ADC, respectively. If assuming that noise contribution is equally dominated from OpAmp and *kT/C* rule, it has

$$\sigma_T^2 = \sigma_{Amp}^2 + \sigma_{kT}^2 = \frac{V_{LSB}^2}{12} \tag{4.7}$$

Therefore,

$$\sigma_{Amp} = \sigma_{kT} = \frac{\sqrt{2}}{2}\frac{V_{LSB}}{\sqrt{12}} \approx \frac{V_{LSB}}{5} \tag{4.8}$$

Eq. (4.8) gives the required noise levels for both OpAmp and *kT/C* SC sampling block of an N-bit ADC. For example, for a 1V V_{PP} 10-bit ADC with a bandwidth of 1GHz, the LSB is approximately 1mV so that the rms noise requirement of the OpAmp and *kT/C* is 200μV. According to Eq. (4.8), it has

$$\sigma_{Amp}^2 = 4kTBR_{gm} = \left(200\mu\text{V}\right)^2$$

$$R_{gm} = 2400\Omega$$

$$\sigma_{kT}^2 = \frac{kT}{C} = \left(200\mu\text{V}\right)^2$$

$$C = 104 \text{ fF}$$

where R_{gm} is the trans-impedance of OpAmp used in pipeline ADC, that is g_m=1/2400 S. If we increase resolution to 14-bit and still the same expected performance, 1GHz bandwidth and 1V full scale, the LSB step size becomes 62.5μV so that the rms noise requirement correspondingly is 12.5μV, thus

$$R_{gm} \approx 8\Omega$$

$$C \approx 32 \text{ pF}$$

Apparently, both 1/8 S OpAmp trans-conductance and 32pF sampling capacitor are prohibitively difficult for the ADC which targets high-speed and low power applications. Thus, in order realize high speed performance for a high-resolution ADC, large full scale V_{PP} is greatly needed to ease the stringent requirement for both OpAmp and sampling capacitor. Meanwhile, by giving up some SNR performance, above requirements can be relieved to some extent. For instance,

losing 0.5-bit effective resolution bits can cut both trans-conductance and capacitor value by half at the same time.

According to Eq. (4.8), for a 12-bit time-interleaving ADC design, 1.5pF sampling capacitor and 3mA OpAmp bias current are used for each SHA to guarantee over 100MHz bandwidth and over 11.5-bit resolution under the condition of a 1.2V full scale and a single 1.5V power supply voltage.

4.2.2 OpAmp Design

For pipeline ADCs, OpAmps need to provide good open loop gain to assure the accuracy of residue amplifying so that theoretically the whole ADC doesn't generate error code throughout all pipelined stages. The minimum open loop gain of OpAmp used in residue doubler is determined as a function of the ADC resolution. The ideal output voltage of each pipeline stage is

$$V_o = 2V_{in} - S_o V_{ref} \tag{4.9}$$

where S_o is sub-DAC input selection which ranges among -1, 0, +1. Taking into account the finite OpAmp gain,

$$V_o^{'} = (\frac{1}{1+1/A_0\beta})(2V_{in} - S_o V_{ref}) \tag{4.10}$$

where A_0 is OpAmp open loop gain and the feedback factor β is given by $\beta = \frac{C_1}{C_2 + C_1 + C_{in}} \approx \frac{1}{2}$,

where C_{in} is the OpAmp input capacitance. Usually A_0 is very large, so

$$V_o^{'} \approx (1-1/A_0\beta)(2V_{in} - S_o V_{ref}) \tag{4.11}$$

The difference between V_o and $V_o^{'}$ is the multiplying error for each pipeline stage, $V_e = V_o^{'} - V_o$.

When V_{in}=V_{ref}/4, V_e can have largest error which is

$$\begin{aligned} V_{e\_\max} &= \left| V_o - V_o^{'} \right|_{V_{in}=\frac{V_{ref}}{4}} \\ &= \frac{1}{2}\frac{1}{A_o\beta}V_{ref} \end{aligned} \tag{4.12}$$

For a N-bit ADC, first stage multiplying error will be amplified by N-3 stages (error amplification starts from second stage and no amplification in last stage), so the total multiplying error due to the finite OpAmp gain for the whole N-bit pipeline ADC is

$$V_{e\_all} = 2^{N-3} \cdot V_{e\_\max} \tag{4.13}$$

In order to avoid code error in last stage, V_{e_all} should be less than half of LSB in last stage which is V_{ref}/4.

$$V_{e\_all} = 2^{N-3} \cdot V_{e\_\max} < V_{ref} \big/ 4 \tag{4.14}$$

Finally, the OpAmp open loop gain requirement in the first stage for an N-bit pipeline ADC can be obtained as

$$A_o > 2^{N-1} \tag{4.15}$$

More generally, for the OpAmp open loop gain requirement used in the *i-th* stage, it has

$$A_{o\_ith} > 2^{N-i} \tag{4.16}$$

Note that above derivation doesn't count any settling and capacitor mismatch effect which also significantly contributes to pipeline ADC's inaccuracy. Therefore, the required minimum open loop gain for each stage should be increased or even doubled to give more design margin to alleviate those effects, so it has

$$A_{o\_ith} > 2^{N+1-i} \tag{4.17}$$

For the proposed 12-bit pipeline ADC, the minimum OpAmp open loop gain in first stage needs to be larger than 2^{12} which is 4096 and 72dB.

Above discussion mainly focuses on the effect of DC gain on pipeline ADC resolution. Another OpAmp parameter is closely related to whole ADC performance is its gain bandwidth product ω_{un}. After taking into account OpAmp's settling time, the output voltage of each pipeline stage becomes,

$$V_o^{'} = (1 - e^{-\frac{t}{\tau}})(2V_{in} - S_o V_{ref}) \tag{4.18}$$

where τ is

$$\tau = \frac{1}{\omega_{-3dB}} = \frac{1}{\beta \cdot \omega_{un}} \tag{4.19}$$

where ω_{3dB} is the -3dB gain bandwidth and b is still the feedback factor. Similar to the OpAmp DC gain requirement, amplification error V_e reaches to maximum for each pipeline stage when V_{in}=V_{ref}/4, it has

$$V_{e\_\max} = \frac{1}{2} e^{-\frac{t}{\tau}} V_{ref} \tag{4.20}$$

Similar to Eq. (4.14)

$$\frac{1}{2} e^{-\frac{t}{\tau}} V_{ref} < \frac{V_{ref}}{2^{N-1}} \tag{4.21}$$

regroup Eq. (4.21), it has

$$t \cdot \omega_{un} > 2 \cdot \ln 2 \cdot (N-2) \tag{4.22}$$

During amplification phase, OpAmp is needed to be settled no more than half of sampling clock period, which implies t_{max} is $1/2f_{sample}$. Finally,

$$\omega_{un} > 4 \cdot \ln 2 \cdot (N-2) f_{sample} \approx 2.77(N-2) f_{sample} \tag{4.23}$$

$$f_{un} > 0.44(N-2) f_{sample} \tag{4.24}$$

For the proposed 12-bit pipeline ADC, in order to reach requirement resolution, $f_{un} > 4.4 f_{sample}$ is required. Considering no DC gain error is counted in Eq. (4.21), even larger gain bandwidth product for proposed OpAmp is needed.

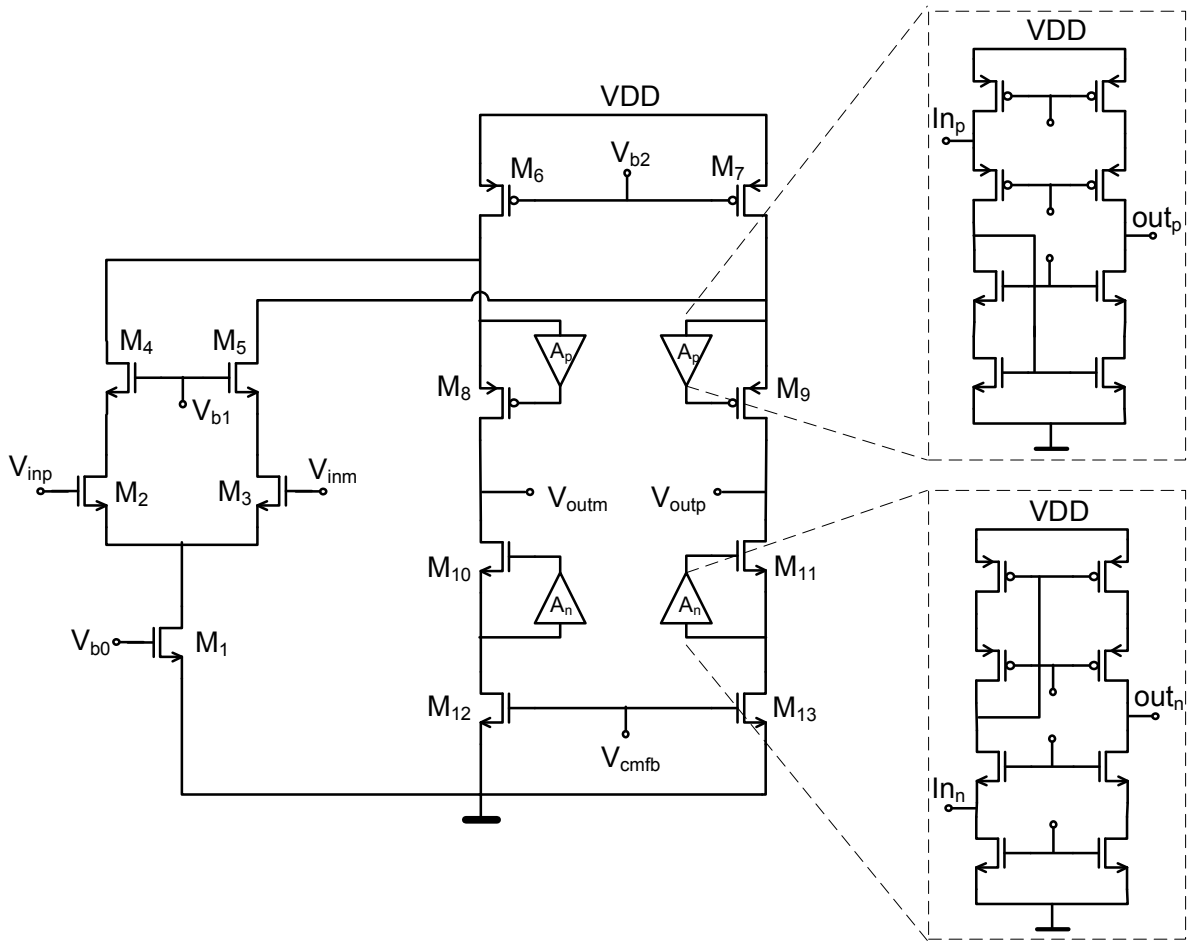

Fig. 0.7 Simplified schematic for OpAmp used in proposed pipeline ADC

Fig. 0.7 shows the structure of fully differential OpAmp used in proposed low voltage pipeline ADC. It utilizes folded amplifier topology to fit in the low power supply voltage design requirement. In order to reach required DC gain, gain-boost is used in second stage to increase the output impedance. No need to provide loading current for following stage, boosting amplifiers can operate in a very low current bias condition to save power dissipation. Due to biased in very low current, all transistors can be set up to almost minimum size to further reduce parasitics. In addition, these amplifiers are single-ended and self-biased to avoid extra common-mode feedback (CMFB) circuit. For the main amplifier, CMFB is applied on bottom NMOS pair, M12 and M13, and uses switched capacitor topology to reach high resolution by eliminating the signal dependence of amplifier outputs. Capacitors in SC CMFB circuit should be kept to small size to lower the capacitance load to preceding OpAmp.

As shown if Fig. 0.7, cascode transistor pair M4 and M5 is added to reduce the input capacitance by easing both transistors' length requirement. Since paralleling with input differential pair, the impedance seen from drain of M8,9 is smaller than that seen from drain of M10,11 at amplifier outputs. To reach required DC gain and be commensurate with the impedance of NFET output transistors, M1 and M2 should maintain both large W/L and wide length simultaneously. Inevitably, this will result in very large width and overall input gate area for both input transistors, which implies that the OpAmp input capacitance, will be significantly increased. Recall that

$$\beta = \frac{C_1}{C_2 + C_1 + C_{in}} \tag{4.25}$$

Large C_{in} can affect amplifier accuracy and bring uncorrectable error to pipeline stages. Therefore, by using cascode transistor pair M4 and M5, input differential pair can use minimum

length transistors to increase overall transconductance as well as maintain large output impedance for first stage due to the inherent characteristic of cascading structure.

4.2.3 Comparator Design

One very unique advantage that 1.5b/stage pipeline architecture can provide is that the ADC as a whole can tolerate up to $\pm V_{ref}/4$ comparator offset. This offset can be automatically corrected by back-end digital correction block. This feature significantly eases the usually very challenging accuracy requirement for comparator threshold, which makes it possible to use very low power and fast dynamic comparator structures with only moderate accuracy. The dynamic comparator discussed here is referenced to those which have only single-stage topologies and no static power consumption. Most of the published topologies are based on sense amplifiers used in static random access memories (SRAM), which are very close to comparators in function [53][54]. Another feature of dynamic comparators used in pipeline ADCs is that the trip points, that also is reference thresholds, can be adjusted by introducing imbalance in the transistors or capacitor sizes, instead of conventionally generating them by using reference ladder. However, in spite of these mentioned advantages, the large offset, which comes from the mismatch of used small transistors, might still limit the performance of the whole pipeline ADC. Therefore, it is necessary to find out an appropriate structure for proposed low voltage and high-resolution ADC. In following sections, several different single-stage, fully differential dynamic comparator structures are studied to manifest the advantages and disadvantages of each structure, implementation limitation and its respective application.

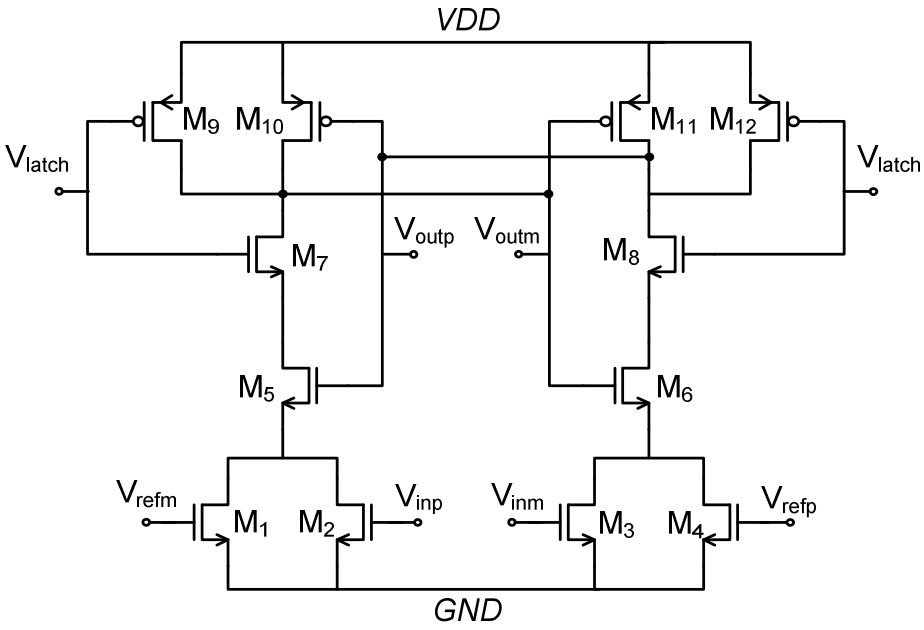

Fig. 0.8 Schematic of resistive divider comparator

Fig. 0.8 shows the simplified schematic of resistive divider dynamic comparator which is widely used in many popular pipeline ADCs [55][56]. Its reference threshold is set up by biasing transistor M_1~M_4 in triode region and intentionally introducing *W/L* mismatch between $M_{1,3}$ and $M_{2,4}$ .When V_{latch} is low, M_9 and M_{12} are turned on and reset both outputs to V_{DD} power supply voltage. Meanwhile, M_7 and M_8 are turned off and there is no current path to ground that indicates no power is dissipated. At the moment of V_{latch} becoming high, both M_7 and M_8 are turned on so that M_5 and M_6 with gate tied to V_{DD} go into saturation and begin to amplify the voltage difference between their sources. Due to the intentionally introduced mismatch on $M_{1,3}$ and $M_{2,4}$, the voltage difference is amplified by a positive feedback and eventually one output reaches V_{DD} and another becomes "0". When operating in triode region, MOS transistor M_1~M_4 behave like a voltage controlled resistor. Eq. (4.26) and Eq. (4.27) give the conductance of left and right branch, respectively.

$$G_L = \mu_0 C_{ox} \frac{W_2}{L}\left(V_{IN}^{+} - V_{T2} - V_{DS1,2}\right) + \mu_0 C_{ox} \frac{W_1}{L}\left(V_{REF}^{-} - V_{T1} - V_{DS1,2}\right) \tag{4.26}$$

$$G_R = \mu_0 C_{ox} \frac{W_4}{L}\left(V_{IN}^{-} - V_{T4} - V_{DS3,4}\right) + \mu_0 C_{ox} \frac{W_3}{L}\left(V_{REF}^{+} - V_{T3} - V_{DS3,4}\right) \tag{4.27}$$

Assuming no mismatch exists and threshold difference is negligible, it has $V_{DS3,4}=V_{DS1,2}$, $G_R=G_L$, and we can finally get

$$\frac{W_{2,4}}{L}\left(V_{IN}^{+} - V_{IN}^{-}\right) = \frac{W_{1,3}}{L}\left(V_{REF}^{+} - V_{REF}^{-}\right) \tag{4.28}$$

Obviously, by sizing the ratio of $M_{1,3}$ and $M_{2,4}$, the threshold of the comparator can be easily adjusted to desired value. If using the same length transistors in order to improve matching, threshold can be determined by only changing width.

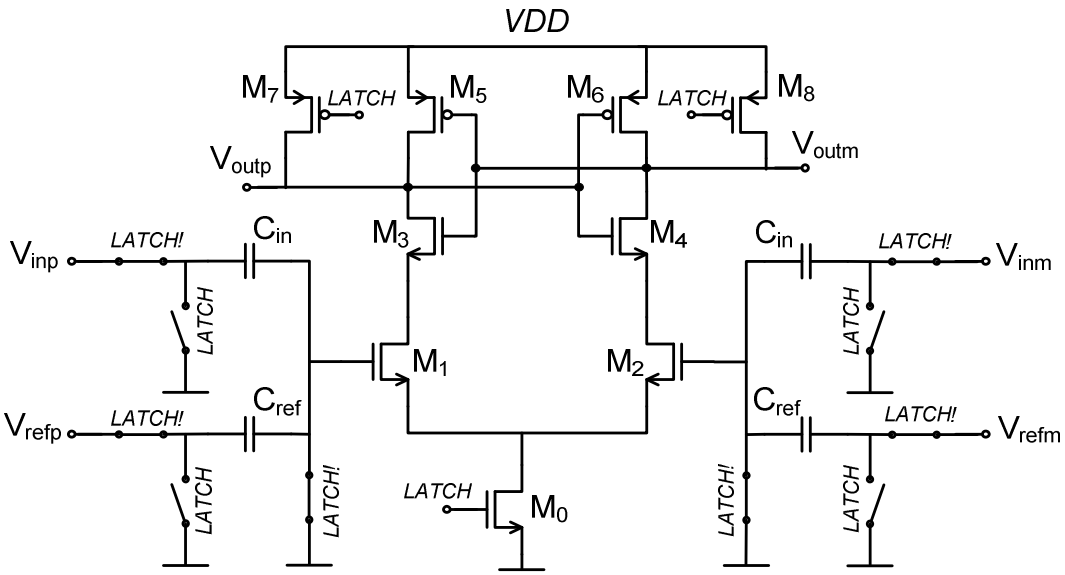

Fig. 0.9 Schematic of charge distribution dynamic comparator

The main advantages of the resistive divider dynamic comparator are easy-to-implement and good isolation between reference and latch signal. On the other hand, its accuracy greatly

relies on the matching of the amplifying transistors M_5 and M_6 and threshold voltage between M_1~M_4. Therefore, this structure often suffers from quite large offset that might cause code error for high-resolution pipeline ADC designs. In addition, biasing M_1~M_4 into triode region also results in bad matching and can only provide a small gain, which further limits it to reach higher accuracy.

One possible way to improve accuracy is to employ differential pair amplifying stage instead of common-gate one used in resistive divider comparator. By providing much better matching performance, differential pair can reduce the offset smaller than one hundred milli-volt which can be tolerated by most of high-resolution pipeline ADC designs. At the same time, eliminating triode region operation, it also enhances the speed performance for comparators. Fig. 0.9 shows the capacitor implementation of differential pair dynamic comparator [57][58], which is also based on similar regeneration circuit as the resistive divider one is. When *LATCH* signal is low, both comparator outputs are also reset to V_{DD} and no current sink is available for differential pair, M_1 and M_2, which implies there is also no static power dissipation. Meanwhile, sampling capacitor pair C_{in} are pre-charged to $V_{IN} = V_{IN}^{+} - V_{IN}^{-}$ and the other pair C_{ref} to $V_{REF} = V_{REF}^{+} - V_{REF}^{-}$. When *LATCH* signal is high, the M_1 and M_2 differential pair is enabled and begins to amplify the voltage difference between V_{IN} and V_{REF}. According to charge preservation law, the trip point of comparator is given by

$$C_{in}\left(V_{IN}^{+} - V_{IN}^{-}\right) = C_{ref}\left(V_{REF}^{+} - V_{REF}^{-}\right) \tag{4.29}$$

Similarly to its resistive counterpart, comparator threshold can be easily set up by adjusting the ratio of C_{in} and C_{ref}. Even if in a pure CMOS digital technology, the matching between capacitor can still be good enough to obtain required accuracy for high-resolution pipeline ADC designs. One major disadvantage of capacitive differential comparator is that the sampling capacitors

used will load OpAmp in preceding stage which can probably degrade the speed performance for whole ADC system and worsen OpAmp stability by providing larger load capacitance. This inevitably restricts this type of dynamic comparator from being used in applications featuring high speed and high sampling rate. Thus, for proposed 12-bit high-speed time-interleaving pipeline ADC, the above two dynamic comparators are not suitable and needs to be modified to reach expected high-speed and high-resolution performance.

As shown in Fig. 0.10, another differential dynamic comparator implementation is given by combining differential pair amplifying stage and divider structure. In addition to still keeping no static power consumption advantage, *LATCH* signal controlled M_0 transistor configures the conventional resistive divider structure as differential pair and consequently help to provide better matching performance as mentioned earlier. Meanwhile, by adding transistor M_{13} and M_{14}, the source terminals of M_5 and M_6 are also reset to V_{DD} when *LATCH* is low. At the very moment of *LATCH* becoming high, these sources will still keep V_{DD} voltage which makes M_1~M_4 operate out of triode region by increasing the drain-source voltage. Furthermore, instead of working in full saturation region, M_5 and M_6 operate in cut-off or triode region with very limited gain which will contribute much less to comparator offset even if large mismatch does exist. The threshold can be adjusted by introducing *W/L* mismatch between M_1~M_4. Note that the linear ratio rule cannot be applied here because all transistors operate in saturation region. Thus, careful simulation is needed to determine desired trip points for proposed comparators. For proposed 12-bit high-speed pipeline ADC, the differential divider dynamic comparator is used to maintain both high speed and small offset simultaneously.

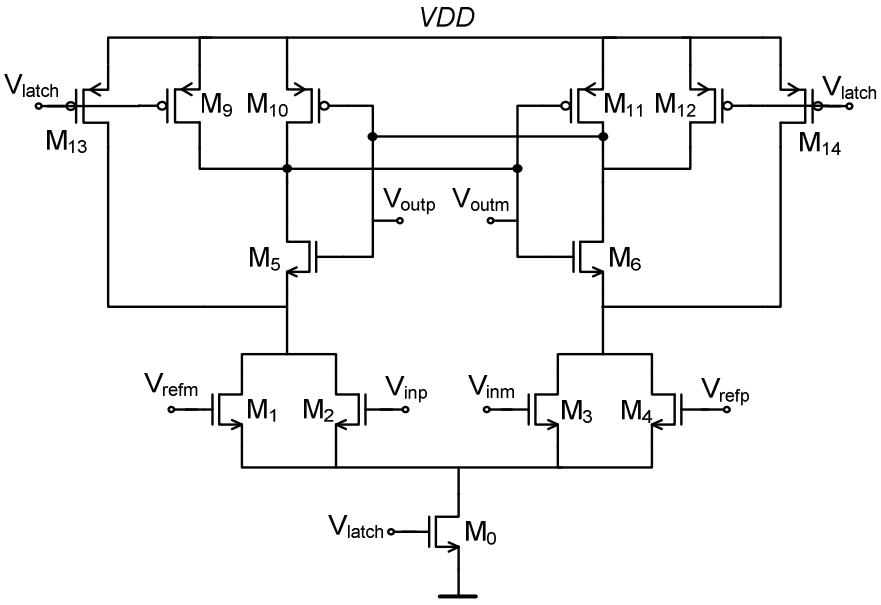

Fig. 0.10 Schematic of differential divider dynamic comparator with improved smaller offset

4.3 Implementation and Measurement

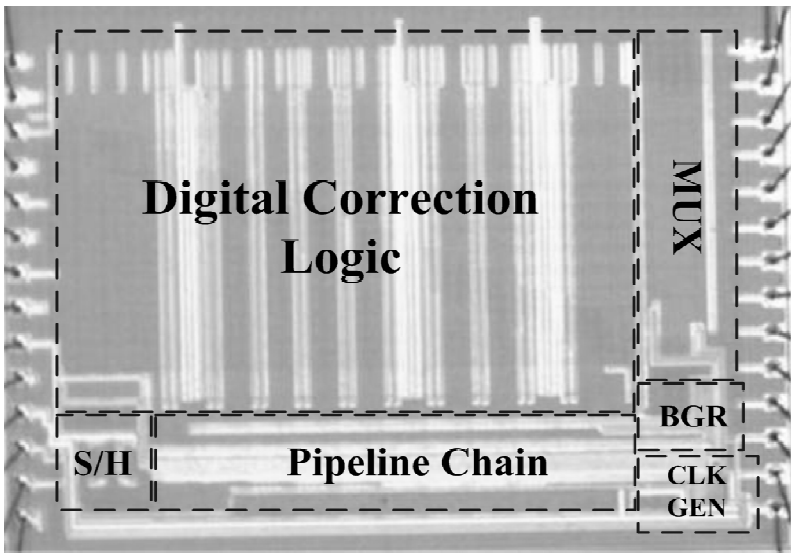

Fig. 0.11 Micrograph of the 12-bit cryogenic pipeline ADC

Based on proposed 12-bit OpAmp sharing and time-interleaving structure, an ADC design for cryogenic and aerospace extreme environments applications has been implemented in a

0.5μm CMOS technology. The micrograph photo of the ADC chip is given in Fig. 0.11. The active area of the ADC chip is 5.2×3.4mm^2. To test the cryogenic ADC, an airproof chamber with electrical heating and liquid Nitrogen cooling is used. The temperature inside the chamber can be controlled from -230°C to +120°C. A cryogenic 12-bit current-steering DAC, which is also designed for aerospace extreme environment, is used to reconstruct the input signal from ADC digital output code. During test, both the proposed cryogenic ADC and DAC are placed into the chamber and wired out to test equipments such as spectrum analyzer and multi-meter, etc. In order to maintain the input signal integrity and avoid the possible damage in ULT condition, other supporting electronic components and equipments are placed out the chamber and connected to the ADC through cryogenic-resistant cables.

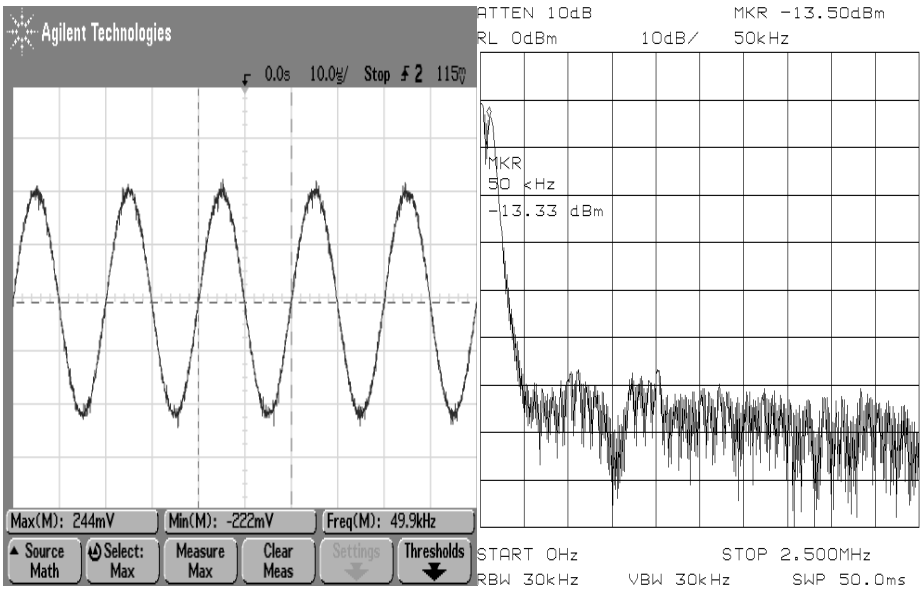

Fig. 0.12 Measured reconstructed sinusoidal output waveform and its spectrum by ADC-DAC pair for f_{in}=50kHz and f_{clk}=5MHz at -230°C.

Fig. 0.12 gives the measured sinusoidal output waveforms and its corresponding spectrums by ADC-DAC test setup pair with 5MHz sampling clock frequency at temperature of -230°C for

a 50kHz input signal. The SFDR for 50kHz output frequency at the temperature of -230°C is 53dBc. The spectrum results are measured with only a single-ended output and without a de-glitch low-pass filter. The measured SFDR also includes the nonlinearity of current-steering DAC, thus ADC may suffer from a degraded dynamic performance when tested with ADC-DAC pair. The total power consumption at 5MHz sampling rate with 3.3V power supply voltage is only 30.4mW at -230°C. Measurement results have showed that the proposed cryogenic ADC can operate over the complete UWT range from -230°C to +120°C which verifies the robustness and capability of this ADC for aerospace extreme environment applications. Table **3** gives a summary for measured cryogenic ADC performance.

Table 3 Summary for measured 12-bit cryogenic pipeline ADC performance

Parameter	**Performance**
Technology	0.5μm CMOS
Temperature Range	-180°C ~ +120°C and -230°C
Resolution Bits	12
Conversion Type	Pipeline
Differential full-scale input	-0.5V ~ +0.5V
ADC-DAC Pair SFDR	53dBc@50k,5MS/s, -230°C
Power Supply	3.3 V
Power dissipation	30.4mW@-230°C@5MS/s
Active Die Size	5.2×3.4 mm^2
Package	40 pin DIP

4.4 Summary

In this chapter, 12-bit OpAmp sharing time-interleaved pipeline ADC for high-speed, low voltage and low power applications are extensively analyzed and discussed. Major building blocks for pipeline structure, including SHA, OpAmp and comparator, are also examined and studied. Architecture and transistor level circuit design techniques and considerations are given to address the trade-off and challenge caused by low power supply voltage and high speed operation requirements. Based on proposed OpAmp-sharing time-interleaving structure, a 12-bit pipeline ADC design is implemented in 0.5μm CMOS technologies for high-speed/low-power and cryogenic aerospace applications. Measurement results show that proposed cryogenic ADC can operate at 5MS/s sampling rate with low power consumption and demonstrate its capability of robustly working under aerospace extreme environments.

Chapter 5 Cryogenic Low-Power Current-Steering DAC Design

5.1 DAC Introduction

With the development of aerospace exploration, the considerations for extreme environments have been included more comprehensively into most designs related to aerospace engineering. The extreme environments, such as temperature, radiation, pressure, vibration, etc, will easily preclude the use of conventional terrestrial engineering designs for operation, actuation and movement under ambient conditions. Although the moon is relatively close to the earth and the radiation level there is not too high, the extreme temperature conditions on the lunar surface can still invalidate conventional electronic components and systems for control, sensing, and communication. This is problematic, since the development of modular, expandable, and reconfigurable human and robotics systems for lunar missions clearly requires electronic components and integrated packaged electronics modules which can operate robustly without external thermal control [59][60].

Unmanned lunar missions necessitate the combination of the mobility of a rover on the surface with sensing functions, electronics, and actuators for control of the rover. Therefore, the sensing and control modules on the rover, usually advanced electronics systems, need not only to sense and monitor the performance of the rover to guarantee good operation of the mechanical systems but also to successfully accomplish the tasks in scientific experiments and research [61]. Since remote electronics are in principle distributed over the entire rover, they cannot be

efficiently located within conventional protective “warm boxes”. Thus, in order to remove the bulky protective “warm boxes,” newly-designed electronics systems must robustly operate in extreme environments on the lunar surface, in the ultra-wide temperature (UWT) range from -180 ^{o}C to +120 ^{o}C and radiation exposure environment[62].

To support NASA’s goals of robotic missions and manned missions to the Moon before 2020, we have been developing and demonstrating extreme environment electronic components such as basic digital logic circuits, data converters, voltage controlled oscillator and other building blocks required for lunar robotic systems with distributed architectures, using commercial SiGe BiCMOS technology. SiGe BiCMOS is a monolithic technology that inherently provides both novel bipolar devices (SiGe HBTs) and Si CMOS. Unlike conventional Si transistors, SiGe HBTs are very well suited for operation in the lunar environment [63][64]. The addition of Ge allows tailoring of the device bandgap which can be used to optimize device behavior as a function of temperature. SiGe BiCMOS offers unparalleled low temperature performance, wide temperature capability, and optimal mixed-signal design flexibility at the monolithic level by offering power efficient, high speed SiGe HBTs and high density Si CMOS [63][64][65][66]. The effort of IC development for extreme environment begins with evaluating SiGe BiCMOS devices across temperature and verifying performance and reliability of circuit designs against system needs for UWT. Circuits are designed and fabricated in commercially-available SiGe BiCMOS technology, tested, and then integrated into the packaging technology developed for system prototype delivery.

The DAC is a crucial component in modern mixed signal systems. High-speed high-accuracy DACs are increasingly demanded by many modern communication systems [67]. However, current DACs cannot properly operate when exposed to extreme temperature and

radiation environments due to the limits of characteristics of fabrication material, model accuracy in cryogenic conditions, and design difficulty in the UWT range. Due to the limitations on power, the electronics systems on the rover require low power consumption to provide longer operation time. Thus, there is an urgent need for a specific DAC design which can solve the issues discussed above such as extreme temperature environments, radiation exposure conditions, lower power and so on. This chapter presents a lower-power 12-bit current-steering cryogenic DAC design that is capable of operating over the UWT range and under radiation conditions on the lunar surface. This DAC design uses commercial SiGe BiCMOS technology to provide better performance in cryogenic condition.

5.2 Current-Steering Architecture

5.2.1 Architectural Design

The current-steering DAC is the most common and almost exclusive type of DAC for high-speed high-resolution applications when compared with other typical DAC architectures [31][32][33]. This architecture provides a good balance between die size, power consumption, accuracy and dynamic performance.

This on-chip current-steering 12-bit DAC is implemented by using a 6MSB+4NSB+2LSB segmented current steering architecture shown in Fig. 0.1, that includes thermometer decoder, current switch logic array, segmented current source array, clock driver and bandgap voltage reference.

The thermometer-coded DAC has advantages over its binary counterpart, such as low differential nonlinearity (DNL), guaranteed-monotonicity and reduced glitch noise. For a 12-bit current-steering DAC, thermometer-coded segmentation for significant bits can be applied to

shrink the chip area and reduce the currents through current switches [16][34]. There are two types of segmentation: full segmentation and partial segmentation. Full segmentation can guarantee good dynamic performance, monotonicity and reduce glitches because every level in the DAC has a switch with a reference current connected to this switch. However, full segmentation in high resolution converters is hard to implement due to worse jitter or time skews at high frequency, larger die size and increased circuit complexity. For example, in a 12-bit fully segmented DAC, there will be 2^{12}-1 = 4095 switches which have to be addressed and switched at very accurate times. Partial segmentation is implemented by combining some segmentation in the most significant bits (MSB) with a binary weighting for the less significant bits, which can obtain a good accuracy and dynamic performance with an acceptable chip area and circuit complexity. Therefore, for the 12-bit DAC design, there is a trade-off between how to segment the significant bits and the effect on layout complexity, glitches, monotonicity, precision, integral non-linearity (INL), DNL and speed [35][36].

Trade-offs also applies to segmentation, die area and static INL and DNL performance [16][68]. Although digital area is very small without segmentation, extra die area is needed to obtain the required accuracy and linearity. Similarly, when a full segmentation is applied, the total area is still dramatically large due to the exponential increase in digital circuitry. With the determined performance specifications, there is an optimal range in die area for thermometer-coded segmentation. If we define that the *M* MSBs are thermometer coded in one cluster, the *K* LSBs are kept in binary coding, and the *N-M-K* intermediate bits are also thermometer coded in another separate cluster for the 12-bit DAC, we can choose 6MSB+4NSB+2LSB within the optimal range to keep the best balance between minimizing the circuit area of thermometer decoders and optimizing the DAC static and dynamic performance [68].

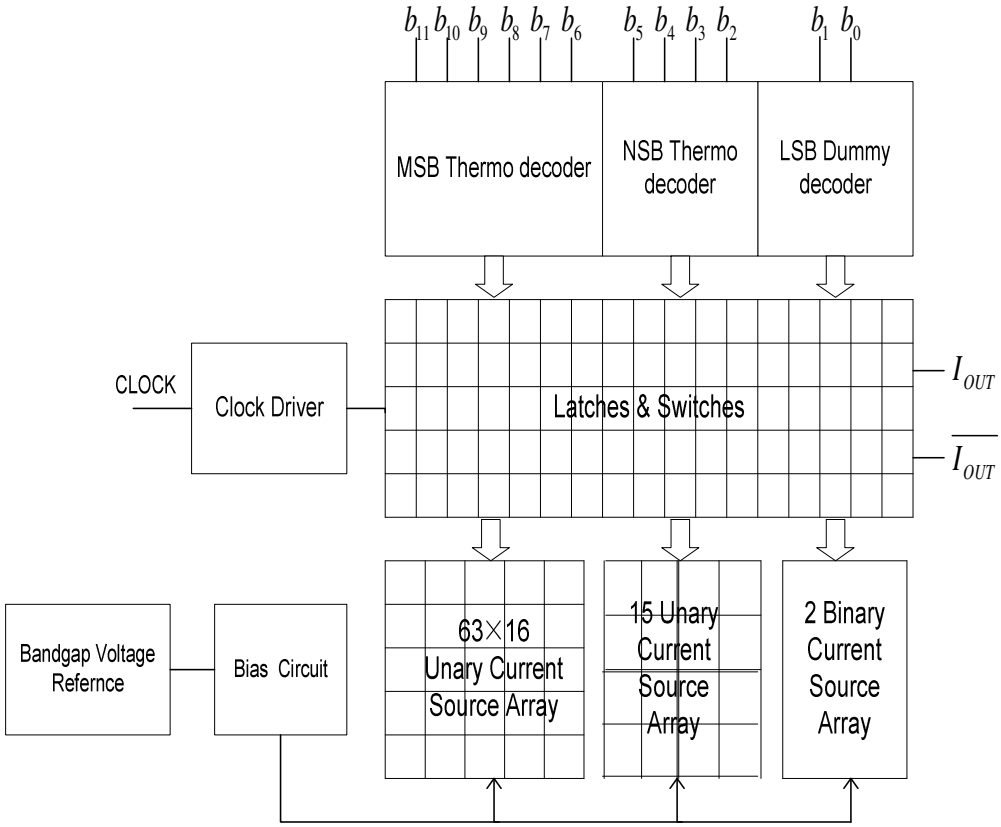

Fig. 0.1 Block diagram of the proposed cryogenic DAC

5.2.2 Unit Current Sources and Switches

The proposed 6MSB+4NSB+2LSB 12-bit current-steering DAC is implemented as follows. The 6 MSBs of the digital binary inputs are thermometer-decoded to control 63 current sources, each having 16-NSB current weighting, and 4 thermometer-decoded NSBs to control 15 current sources with unit-NSB current weighting, while the remaining 2LSBs control 2 binary-weighted current sources. The output currents of all current sources, which are switched ON or OFF according to the digital input codes, are summed and driven into an external resistive load to generate the required analog output voltage [69].

Since switches need to be turned ON or OFF at the same time, they should be clearly prevented from both being completely off. Otherwise, the voltage potential at the output of the current source will increase to the power supply voltage when both branches are shut completely off, and then the output voltage will return to normal low level when switches are turned on again. In some cases, the current source transistors may also get into the linear operation region and will then have much worse output impedance. Furthermore, this big change in output voltage will cause serious output glitches, which badly affect the DAC dynamic performance, including signal-to-noise ratio (SNR), spurious free dynamic range (SFDR), and effective number of bits (ENOB). To avoid this problem, we need to ensure that the crossing point for the transfer curve of the differential switch pair can't simultaneously turn off both transistors. For a P-type FET switch pair, the crossing point should be a low voltage to give enough overdrive voltage to open the PFETs. Fig. 0.2 shows the schematic for the basic current switches used in the DAC, which can realize the required low-voltage crossing point. When CLK arrives, the switch will be turned on or off according to the state of control signal, which is coming from preceding decoder and will enable or disable the switch based on digital inputs. During operation, parallel inverters Inv2 and Inv3 simply add a time delay of the order of a nano second between the differential switch pair transfer curves. This delay can increase the switch transition time and shift the transfer curve in one branch a little bit off the original high voltage crossing point to get the desired level. It is also necessary for switching signals to be properly matched to reduce the glitches. Meanwhile, we need to keep the rise and fall behavior of the switch signals as equal as possible to improve the dynamic performance of the DAC.

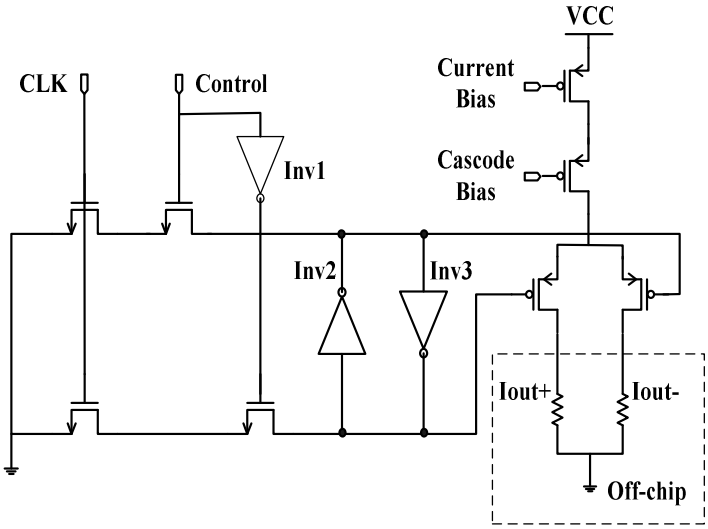

Fig. 0.2 Schematic diagram of the basic current switch block

To prevent the output signal of the converter from modulating the division accuracy due to channel length modulation, a cascade structure is applied for the current cell circuit. Fig. 0.3 shows the current source units for four different segmented bit cells, MSB, NSB, LSB1 and LSB2. The current relationship between them is

$$I_{MSB} = 16I_{NSB} = 32I_{LSB1} = 64I_{LSB2} \tag{5.1}$$

which corresponds to the segmentation of DAC. In addition, all bit cells are composed of PMOS FETs with the same size to minimize the process mismatch error during fabrication. Precise design and simulation is necessary to make all bit cells operate in the saturation region. Transistors for the NSB current source are set to the basic size device used in whole DAC current source array. For MSB current source, the required 16 times NSB current can be obtained by paralleling 16 unit size transistors. Due to the channel length modulation, the LSB1 and LSB2 current source which is constructed by putting the same basic size transistors in series might be

slightly smaller than expected value. Accurate PMOS device size must be obtained through precise post-layout simulation.

For this DAC design, we use PMOS FETs as current sources to achieve high accuracy at the cost of more area. Compared with NMOS devices, PMOS FETs have smaller 1/f noise and don't need additional output pull-up resistors which provide convenience and compatibility when cascaded with following circuits. At the same time, the N-well of PMOS FETs can effectively eliminate the crosstalk transmitted by substrate and other noises.

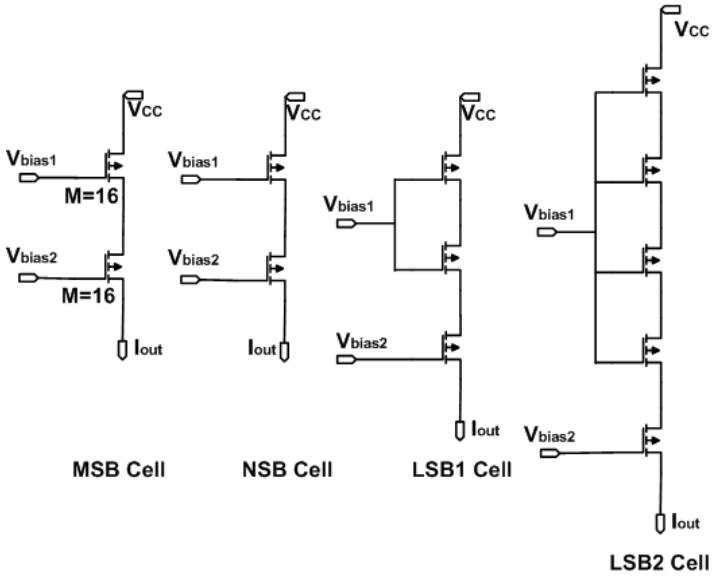

Fig. 0.3 Current source units for different significant bit cells.

As shown in the DAC architecture for the LSB_1 and LSB_2 current switch cells, since the LSB D_0 and D_1 input signals aren't converted into thermometer code, there is an apparent delay difference compared with other significant bits. This delay difference will make the MSB and LSB switches switched ON asynchronously at high frequency, which consequently causes worse DNL and INL as well as larger output current error. Therefore, one LSB dummy decoder composed of an even number of inverters is used to remove this effect.

In the current steering DAC, the impedance Z_{imp} seen in the drain of the switch transistors of each current cell has to be made large enough so its impact on the INL specification of the DAC can be tolerated [70]. However, Z_{imp} is frequency dependent. The impedance that is required to obtain a certain resolution is approximately equal to

$$Z_{imp} = \frac{NR_L}{4Q} \tag{5.2}$$

where R_L is the load resistance, N represents the total number of unit current sources, and Q is the ratio between the signal and the second harmonics. To obtain 12 bit output resolution, Z_{imp} has to be about 750 kΩ. When the frequency goes above 80 MHz, cascode current sources are needed to meet the requirement of Z_{imp}.

To minimize the systematic error introduced by the voltage drop in the ground lines of the current-source transistors and take account of the increased device current at cryogenic temperature, metal lines widths were chosen based on precise simulation. The maximum delay of the metal wire on chip is approximately 75 ps, and the clock tree is carefully built to ensure an acceptable clock skew.

5.2.3 UWT Bandgap Reference

For a current-steering converter, the static and dynamic characteristics of the DAC such as DNL, INL, SNR, SFDR, and ENOB are very sensitive to the accuracy and stability of the on-chip current reference. Therefore, it's rather critical to design a stable and temperature-independent bandgap reference capable of operating over the UWT range from -180°C to +120°C.

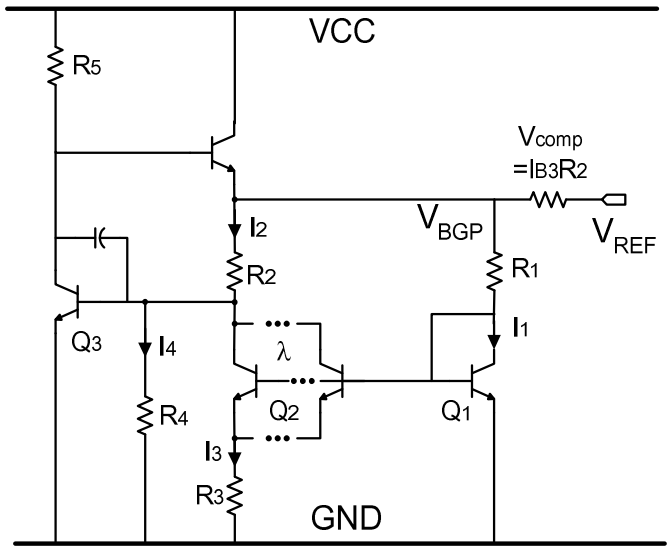

Fig. 0.4 Schematic of UWT bandgap voltage reference.

The bandgap reference circuit for UWT application is illustrated in Fig. 0.4. The design utilizes the SiGe HBT transistors to generate the temperature independent voltage sources. For BJTs Q_1 and Q_2,

$$V_{R3} = I_3 R_3 = V_{BE1} - V_{BE2} \tag{5.3}$$

Meanwhile,

$$V_{BE1} = V_T \ln(\frac{I_1}{I_{s1}}) \tag{5.4}$$

$$V_{BE2} = V_T \ln(\frac{I_3}{I_{s2}}) \tag{5.5}$$

where $V_T = kT/q$. Thus,

$$V_{R3} = I_3 R_3 = V_T \ln(\frac{I_1 I_{s2}}{I_3 I_{s1}}) \tag{5.6}$$

If λ is the number of transistors Q_2 in parallel, the current in R_3 is

$$I_3 = \frac{V_T}{R_3} \ln(\lambda \frac{I_1}{I_3}) \tag{5.7}$$

Thus collector current for Q_2 is

$$I_{C2} = \frac{\beta}{\beta+1} I_3 = \frac{\beta}{\beta+1} \frac{V_T}{R_3} \ln(\lambda \frac{I_1}{I_3}) \tag{5.8}$$

Finally, the bandgap reference voltage at node V_{BGP} can be found as

$$\begin{aligned} V_{BGP} &= V_{BE3} + I_2 R_2 \\ &= V_{BE3} + R_2 (I_{B3} + I_{C2} + I_{R4}) \\ &= R_2 I_{B3} + V_{BE3} \left(1 + \frac{R_2}{R_4}\right) + V_T \frac{\beta}{\beta+1} \frac{R_2}{R_3} \ln\left(\lambda \frac{I_1}{I_3}\right) \end{aligned} \tag{5.9}$$

As shown in Fig. 0.4, when using the bandgap reference output to generate temperature-independent current, a compensating resistor needs to be placed between bandgap output and the base of the load transistor to compensate the base current drawn by Q_3. This compensation scheme fine tunes the temperature coefficient of the bandgap reference. Thus

$$V_{REF} = V_{BGP} - V_{comp}$$

$$= V_{BE3}\left(1+\frac{R_2}{R_4}\right)+V_T\,\frac{\beta}{\beta+1}\frac{R_2}{R_3}\ln\left(\lambda\frac{I_1}{I_3}\right) \tag{5.10}$$

Utilizing the positive temperature coefficient of V_T and the negative temperature dependence of V_{BE} [42], a constant and accurate voltage source over the UWT range can be generated. Furthermore, by changing the ratios of $\frac{R_2}{R_4}$ and $\frac{R_2}{R_3}$, we can adjust the coefficients of the negative and positive temperature terms, respectively, to accomplish the temperature independence for output current or output voltage.

5.3 Design for Aerospace Extreme Environments

5.3.1 Design Considerations for Low Temperature

At low temperatures, the device characteristics for MOS FETs will differ from those in room temperature. As a result, circuit designs must consider device performance at low temperatures. When temperature decreases, the channel conductance of MOSFETs increases [71]. In addition, this increase is quite symmetrical and this means that the design parameters with which proposed circuit can properly work in room temperature can also be maintained in low temperature condition. Therefore, for some digital blocks in the DAC, design for low temperature applications can be quite straightforward, just keeping all aspect ratios the same as the room temperature design.

The threshold voltage for MOSFETs can be approximately modeled by [63][65]

$$V_{TH} = V_{FB} + 2\phi_F + \sqrt{2q\cdot N_A\cdot\varepsilon_{Si}\cdot(2\phi_F+V_{BB})}\Big/C_{ox} \tag{5.11}$$

where N_A is the acceptor concentration of the well, V_{FB} is the flat-band voltage, ε_{Si} is the

dielectric constant of silicon, V_{BB} is the bulk back bias voltage, C_{ox} the capacitance of the gate oxide, and ϕ_F is the voltage difference between Fermi potential E_F and intrinsic Fermi potential E_{Fi}. From [72], we can know with the decrease of temperature, ϕ_F is slightly increased. This effect will give rise to an increased V_{TH} when temperature decreases, which also occurs for PMOS FETs.

However, the threshold variation for both transistors is also exactly symmetrical, which means that the thresholds that work well at room temperature will still maintain some of CMOS digital logic circuit's performance like symmetry in rise and fall time and fan-in fan-out ability [73]. But higher voltage will be required to keep the device on and maintain the same overdrive capability when compared with room temperature. Extremely low-voltage applications at low temperature may be significantly limited by this effect. Careful and complete simulations are needed to ensure the proper operation status at low temperatures.

5.3.2 Aerospace Radiation Tolerant Design

Due to the lack of atmosphere on the moon, the semiconductor devices working on the lunar surface need to sustain high-energy radiation as well as extreme temperature environments. High-energy radiation will dramatically impair the performance of devices and even cause destruction of the devices [74]. The damage suffered by microelectronics mainly comes from three different sources, total dose effect, displacement damage and single event effects. For the proposed DAC, the cumulative effects, mainly total dose effect, are more related to the factors that usually limit chip's operation lifetime and give rise to device malfunction. Some design considerations are addressed to improve proposed DAC's radiation-tolerance capability. Single-event effect related design considerations are mainly carried out in chip's physical layout domain.

Total dose effect will cause most significant damage and performance degradation to the DAC. When an energetic particle such as a proton is passing through an electronic device, it may be trapped and accumulated inside the device which may dramatically affect the device characteristics like threshold, leakage current, etc, and finally cause the malfunction of the DAC. At the same time, these energetic particles knock silicon atoms out of their proper crystal lattice locations, creating defects in the crystal structure which appear as wells in the electrical potential. Those wells trap conduction electrons, increasing the resistance and changing the threshold voltage of the device. This problem is especially important for current-steering DAC, where the output currents are summed up from the precise unit current sources. The radiation causes significant inaccuracy in the unit currents that inevitably leads to the degradation of the DAC static performance such as INL and DNL, and its dynamic performance such as SFDR and ENOB. One possible radiation-tolerant design technique that is suitable for DAC design is to use large W/L transistors. By providing larger switch current, large W/L transistors can overcome the threshold shift and gate oxide capacitance increase caused by radiation trapped holes. Meanwhile they reduce not only the possibility of device invalidation but also the cumulative change in device characteristics due to total dose effect. Usually, switching transistors with minimum size are chosen to achieve the fastest switching speed with minimum power consumption and to reduce the effect of clock feed-through (CFT). For the cryogenic DAC design, medium size NMOS with W/L = 10/1μm and 3-paralleled PMOS with W/L = 10/1μm are chosen. Moreover, switching transistors with larger size were used for MSB cells in order to lower the voltage across the transistors, which lead to some penalty of increased clock feed-through due to increased gate capacitance.

In order to prevent the single event upset latch-up caused by the positive feedback formed in

the parasitic transistors, some special radiation hardened by design (RHBD) layout rules are applied in our design to reduce the well/substrate parasitic resistance and reduce the gain product of the parasitic NPN/PNP pairs. The RHBD rules include: active N+ (P+) guard rings are added around PMOS (NMOS); n-well and p-sub contacts are generously and frequently used; deep trench rings are added for isolation between PMOSs and NMOSs; keep n-well and n+ source/drain father apart if possible.

In order to verify the radiation-tolerance of the proposed DAC, different total high-energy proton doses, 30 krad(Si), 100 krad(Si) and 300 krad(Si), were used to mimic the radiation environments on the lunar surface. In order to mimic the worst-case radiation, the 63.3 MeV protons were directed perpendicular to the bare dies of the DAC with a 7.71 p/cm^2/sec rate. No package was used as a protection in the experiment. The measurement results and discussions are presented later in following section.

5.4 Implementation and Experimental Results

The proposed cryogenic DAC has been implemented in a 0.5μm SiGe BiCMOS technology. The package and micrograph photo of the DAC chip are given in Fig. 0.5 and Fig. 0.6, respectively. The size of the DAC chip is 3.5 × 1.8 mm^2 including pads. In the layout of the DAC, the current source array and the switches are placed in separate arrays to avoid coupling from the digital signals to the current sources. For aerospace applications, some special layout techniques should be taken into consideration during the whole layout process. To reduce the radiation effect, dummy transistors and duplicate cells are required to provide radiation protection for crucial circuit blocks. With the large W/L transistors and the protection cells, the area for crucial circuit blocks is enlarged so that the capability of resisting the radiation effects is improved. Guard rings are also used to provide good isolation for DAC current source array to reduce total dose effect.

For increased transconductance and freeze-out effect at very low temperatures, the interconnection metals with larger width should be used to provide margin for larger current conduction such that a sudden current increase will not damage the interconnection wires and invalidate DAC operation.

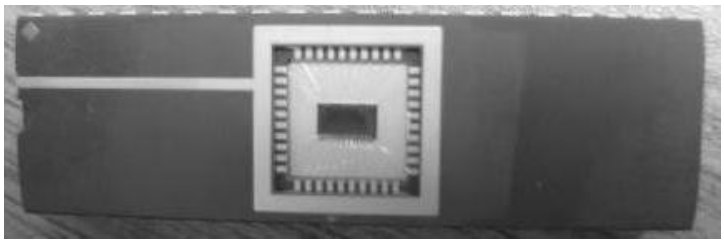

Fig. 0.5 40 pin DIP package photograph of the DAC chip.

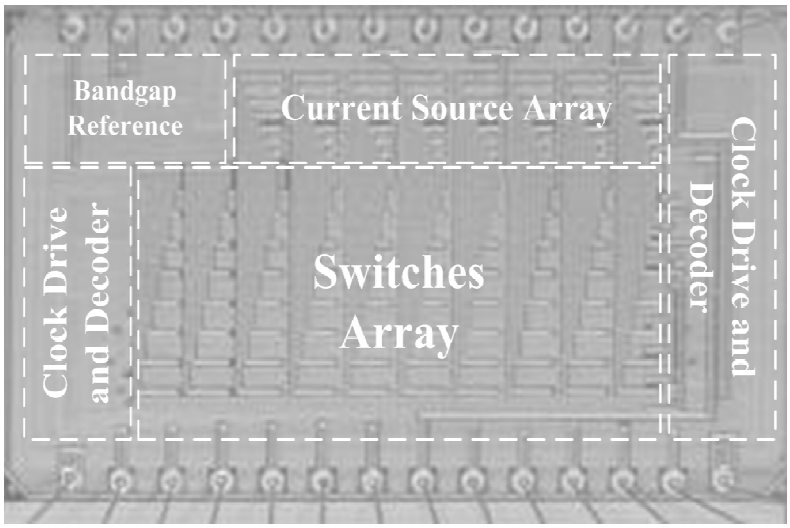

Fig. 0.6 Micrograph of the 12-bit cryogenic BiCMOS DAC.

To test the cryogenic DAC, an airproof chamber with electrical heating and liquid Nitrogen cooling is used. The temperature inside the chamber can be controlled from -180°C to +120°C. The inputs and outputs of the DAC chip placed into the chamber are connected to a test board

outside of the chamber using SMA cables. The test board outside of the chamber contains an FPGA chip for DAC input generation. This test setup guarantees the integrity of input test signals and avoids the damage of the supporting electronic components against the wide temperature variations [75][76][77].

5.4.1 Measurements Before Radiation

Fig. 0.7 gives the measured DAC sinusoidal output waveforms at 121 kHz output frequency with the 25 MHz input sampling clock frequency at temperature of -180°C. Fig. 0.8 shows the measured sinusoid waveform at 625 kHz output frequency with an 80 MHz input sampling clock frequency at room temperature.

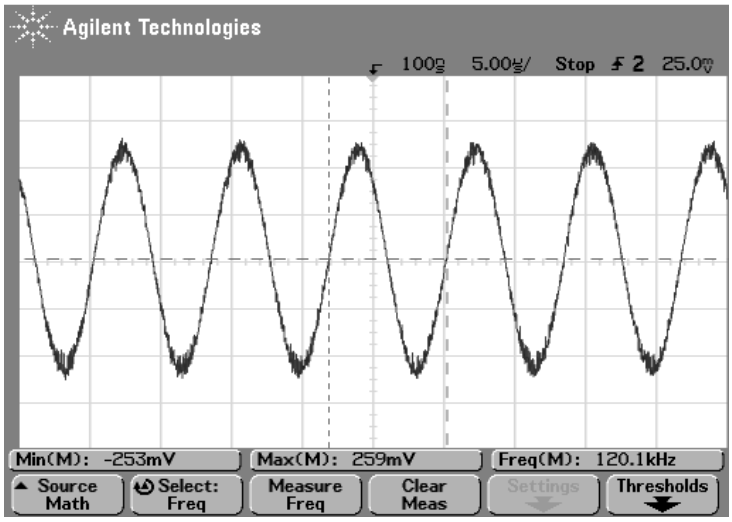

Fig. 0.7 Measured DAC differential output waveform without deglitch filter for f_{out} = 121 kHz and f_{clock} = 25 MHz at -180°C.

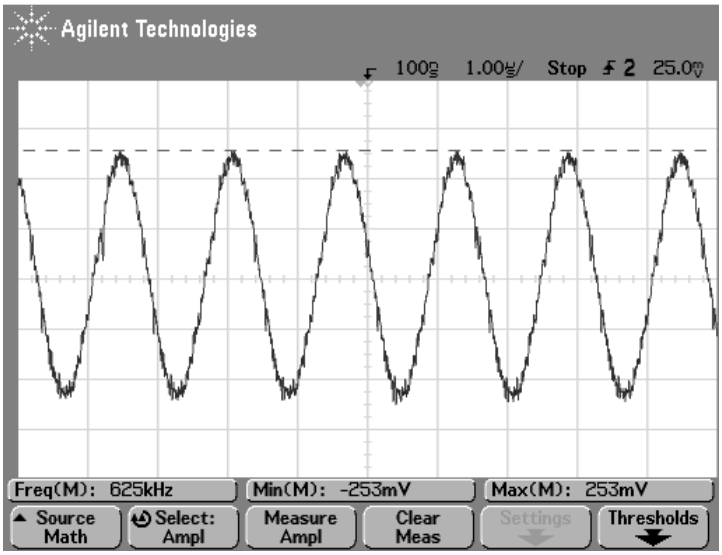

Fig. 0.8 Measured DAC differential output waveform without deglitch filter for f_{out} = 625kHz and f_{clock} = 80MHz at room temperature

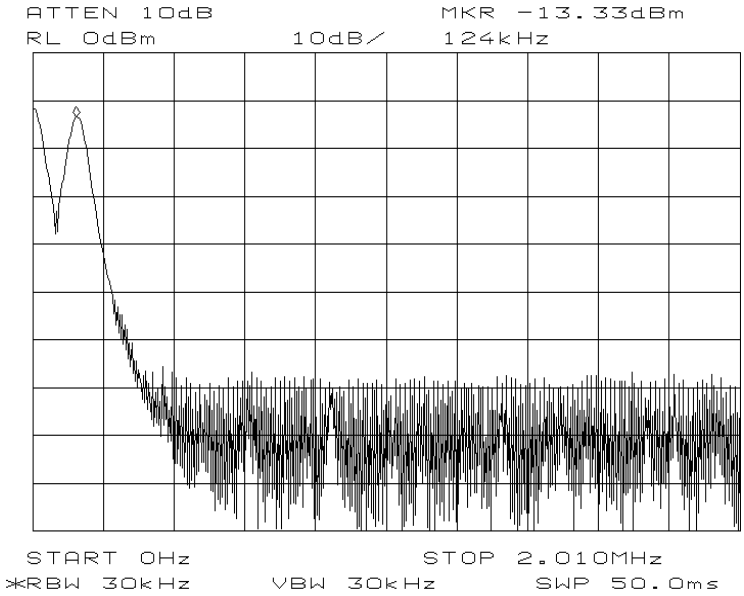

Fig. 0.9 Measured DAC output spectrum without deglitch filter for f_{out} = 121kHz and f_{clock} =25MHz at -180°C

The SFDR at the 121 kHz output frequency with 25 MHz clock at the temperature of -180°C is about 54 dBc, as shown in Fig. 0.9. The spectrum results are measured with only a

single-ended output and without a deglitch low-pass filter. The total power consumption at 25 MHz with 3.3 V power supply voltage is 39.6 mW at -180°C. Fig. 0.10 shows the measured DAC full-scale output current over UWT range. The current output at -180 °C is 5.25 mA, and the standard output current is 5.12 mA at 25°C. Thus, the effective temperature coefficient for the DAC is 97.7 ppm/°C.

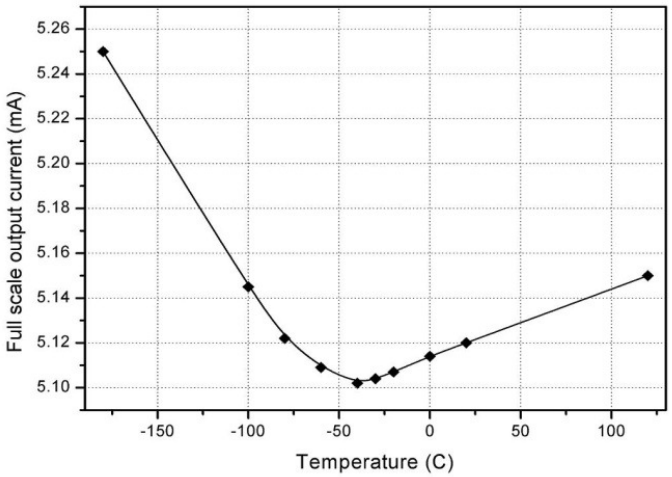

Fig. 0.10 Measured DAC full-scale output current over the UWT range.

5.4.2 Measurements After Radiation

Fig. 0.11 gives the measured 121 kHz output sinusoid waveform with 300 krad(Si) proton radiation dose at temperature of -180°C. Fig. 0.12 also shows the measured 625 kHz output sinusoid waveform with 300 krad(Si) proton radiation dose at room temperature in the same test condition as above.

With a 300 krad(Si) proton radiation dose, the SFDR at the 121 kHz output frequency with 25 MHz clock at the temperature of -180°C is about 52 dBc, as shown in Fig. 0.13. Though there is a slight degradation in DAC's SFDR performance which comes from the inaccuracy of unit

current sources caused by total dose effect, the DAC still shows good radiation-tolerance and robustness to properly operate in extreme environments. Compared to the commercial DAC given in [78], the DAC presented shows much better performance in extreme temperatures environment and is more appropriate for aerospace extreme environment applications. The total power consumption with a 3.3 V power supply voltage for different temperatures, operating frequencies and total radiation doses is listed in Table 4. The power consumption at -180°C is larger than that at +120°C, and both are larger than that at room temperature, which results from the increased unit current at extreme temperature conditions corresponding to the results shown in Fig. 0.10. At the same time, the power consumption of the DAC becomes larger with the increase of total radiation dose and the operating frequency. When the DAC works at higher sampling frequencies, the digital circuits are switched more rapidly which gives rise to larger dynamic power consumption. As for radiation effects, with the increase of total dose, more holes trapped in the oxide induce a threshold voltage shift for PMOS transistors. The additional interface state will degrade both the transconductance and the sub-threshold slope, inducing a further threshold shift. The threshold shift and the variation of sub-threshold slope will increase the off-state leakage current and, consequently, the power consumption of the device. Therefore, the total power consumption will gradually become larger for large total radiation doses when compared with smaller dose cases. Despite affected by total dose effect, the proposed DAC with design considerations for extreme environments still demonstrates a good radiation tolerant performance.

Measurement results have indicated that the proposed cryogenic DAC is capable of operating over the complete range from -180°C to +120°C. At the same time, good radiation-tolerance and robustness of the proposed DAC have also been verified by the post-radiation measurements. Therefore, practical applications of this DAC for lunar aerospace exploration are possible. The

cryogenic chip was packaged in a 40-pin DIP package. Higher operation frequency and better performance could be achieved if a PQFP package with shorter leads had been used. Table 5 gives a summary of the cryogenic DAC performance.

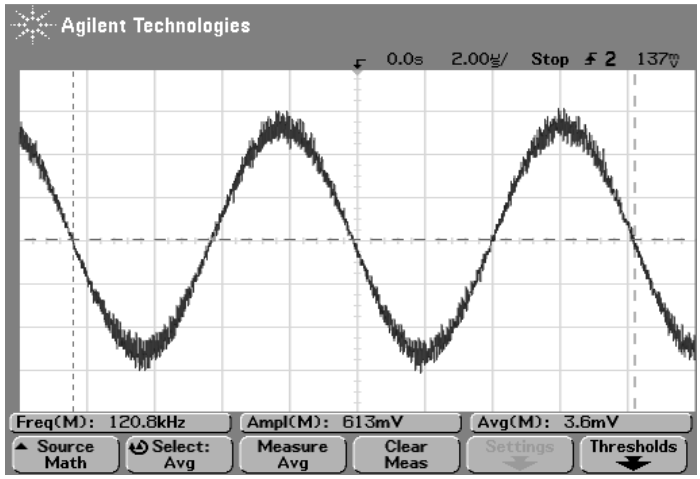

Fig. 0.11 Measured DAC differential output waveform with 300 krad(Si) proton radiation dose for f_{out} = 121 kHz and f_{clock} = 25MHz at -180°C.

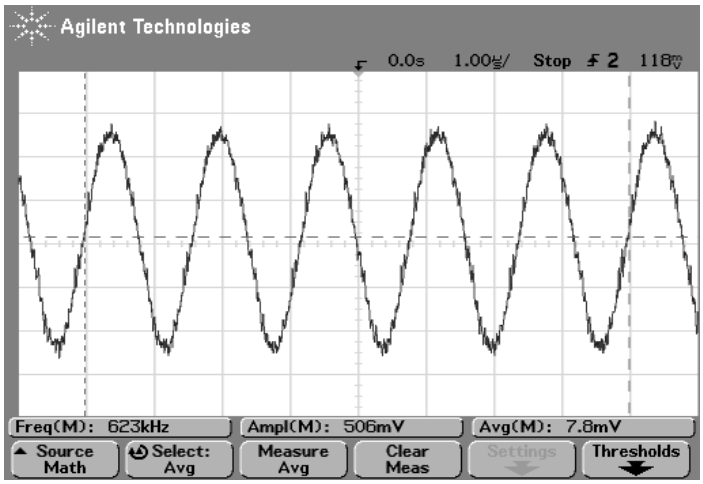

Fig. 0.12 Measured DAC differential output waveform with 300 krad(Si) proton radiation dose for f_{out} = 625 kHz and f_{clock} = 80MHz at room temperature.

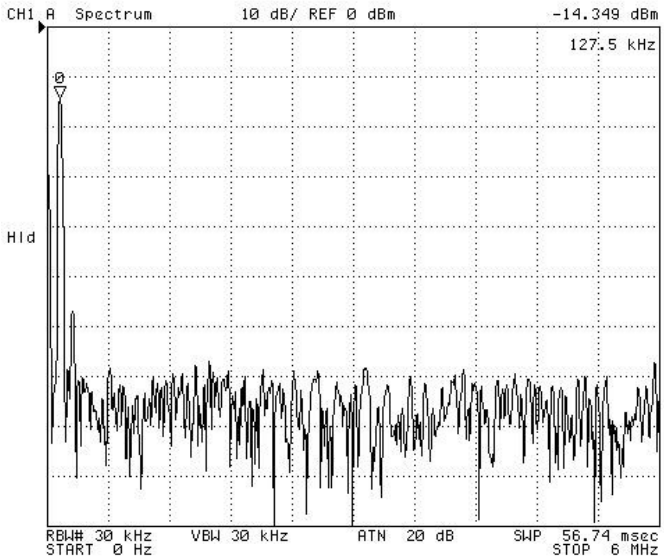

Fig. 0.13 Measured DAC output spectrum with 300 Krad(Si) radiation dose for f_{out} = 121 kHz and f_{clock} = 25 MHz at -180°C.

Table 4 Summary of measured DAC power consumption

T (°C) Dose (Krad(Si))	**-180**	**25**	**120**
0	39.6mW@25MHz 85.8mW@80MHz	39.6mW@25MHz 82.5mW@80MHz	39.6mW@25MHz 84.2mW@80MHz
30	39.6mW@25MHz 87.5mW@80MHz	39.6mW@25MHz 82.5mW@80MHz	39.6mW@25MHz 85.8mW@80MHz
100	46.2mW@25MHz 89.1mW@80MHz	46.2mW@25MHz 85.8mW@80MHz	46.2mW@25MHz 87.5mW@80MHz
300	49.5mW@25MHz 95.7mW@80MHz	46.2mW@25MHz 85.8mW@80MHz	46.2mW@25MHz 89.1mW@80MHz

With verified performance under aerospace extreme environments, the proposed cryogenic radiation-tolerant DAC can be used for resistance sensor system in aerospace industry to

accomplish scientific exploration task on lunar surface. Through a Wheatstone bridge, an analog-to digital converter and other auxiliary circuits, the target resistance value can be automatically obtained by the sensor in 12 bit digital code. These code will be sent into logic block to make digital signal processing. By converting the digital output from logic block, the DAC provides the bridge with a feedback control signal which will adjust the bias current and consequently set up different measurement gears for the sensor. The resistance sensor can be applied to measure the temperature characteristics for electronic devices used in aerospace extreme environments. In addition, the DAC can also be widely used in other industrial fields which need to work under aerospace extreme environment, like space remote control, satellite communication and further aerospace exploration, etc.

Table 5 Summary of measured DAC performance

Parameter	**Performance**
Technology	0.5μm SiGe BiCMOS
Temperature Range	-180°C ~ 120°C
Resolution	12
Conversion Type	Current Steering
Maximal Sampling Frequency	80 MS/s
Differential full-scale output	0.52 V
SFDR without radiation	52dBc@121k,25MS/s 120°C 54dBc@121k,25MS/s -180°C
SFDR with 300Krad(Si) proton dose	51dBc@121k,25MS/s 120°C 52dBc@121k,25MS/s -180°C
Power Supply	3.3 V
Power dissipation	39.6 mW@-180°C@25 MS/s
Die Size	3.5×1.8 mm^2
Package	40 pin DIP

5.5 Summary

An 80 MHz 12-bit DAC was implemented in 0.5μm SiGe BiCMOS technology for aerospace extreme environment applications. The measurement results showed that the proposed DAC is capable of operating over the ultra-wide temperature range from the -180°C to +120°C. Meanwhile, for the aerospace radiation environment, the DAC also shows good radiation-tolerance and robustness which has been verified by the measurement results of three different dose cases. In order to achieve temperature-independence, a bandgap reference was designed to provide different segmented current source cells with stable and accurate current over the UWT range. Design considerations for both extreme temperature and aerospace radiation environments have also been discussed. The chip die area is 3.5×1.8 mm^2 and the total power consumption with a 3.3 V power supply is only 39.6 mW at -180°C and 25 MHz sampling frequency.

Chapter 6 Conclusion and Future Work

6.1 Conclusions

It is obvious that data converters will always be demanded to provide higher sampling rate, lower power consumption and lower power supply voltage operation. Correspondingly, design techniques and considerations for next generation data conversion components need to meet the persistently increasing challenges, such as shorter settling time, smaller operation headroom, tougher noise requirement, and so on, which all result from above stringent requirements. In this research, multiple ADC/DAC designs are implemented in different technologies to address either high-speed or low-power design challenges or even both. Circuit design techniques and considerations are extensively and carefully discussed in both architectural and transistor level. Simulation and measurement results are also given to verify functionality and performance of proposed designs.

For 3-bit ultra-high-speed ADCs, X- and K-band sampling rate is achieved by using 0.12 μm SiGe HBT technology featured with f_t/f_{max} of 210/310 GHz to enhance the device operation speed. CML structure and time-interleaving are also employed to further boost overall speed performance. For 12-bit pipeline ADCs, multiple low voltage high speed circuit design techniques are used in both architectural and transistor level, such as time-interleaving , OpAmp sharing, bootstrapped switch, folded gain-boost amplifier, revised dynamic comparator, etc. With a single 3.3V power supply, proposed high-speed pipeline ADC can achieve 5MS/s sampling

rate with a total power consumption of 30mW. For 12-bit cryogenic DAC, current steering architecture and 6+4+2 bit segmentation scheme are utilized to maintain a good trade-off between high-speed and low-power performance. Verified by experimental results, cryogenic ADC demonstrates the capability of operating under aerospace extreme environment with low power and good robustness.

6.2 Future Work

High speed and low power data converters will continue to be the important and hot topics in the field of wireless communication system. The techniques and architectures presented in this research are only a part of the innovations in this promising area and consequently will have great opportunities to be further improved and optimized to meet the future demands.

1) For ultra high-speed flash ADC, more resolution bits should be implemented to further meet the dynamic range requirement in complicated communication protocols. In addition, bubble correction block can be added to provide self-correction in future flash ADC designs.

2) For high-speed pipeline ADC, background digital assisted calibration can be employed to further improve resolution performance. The effect of capacitor mismatch on ADC resolution can be studied in following design to provide theoretical guidance.

3) For high-speed current-steering DAC, lower power supply voltage can be used to reduce required power consumption. Study on current source matching can be performed to improve DAC's accuracy and linearity in future works.

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