Integrated Circuit Design for Ultrahigh Speed Frequency Synthesis: Direct Digital Synthesizer and Variable Frequency Oscillator

by

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Abstract

This dissertation presents design and implementation of the high speed direct digital frequency synthesizer (DDS) and variable-frequency oscillator (VFO). DDS is a digital technique for frequency synthesis, waveform generation, sensor excitation, and digital modulation/demodulation in modern communication systems. The VFO can be used as the reference clock of the DDS system, either standalone or combined with other phase-locked-loop (PLL) components.

DDS provides many advantages including fine frequency-tuning resolution, continuous-phase switching and accurate matched quadrature signals. DDS can directly generate and modulate signal at microwave frequencies. A high-speed DDS can be significantly simplified the transceiver architecture. Thus the cost of radio and radar systems can be reduced considerably.

Ultrahigh speed DDS over GHz is demanding for modern radar and communication systems. This research proposes work on designing ultrahigh speed DDS chips with sine-weighted digital-to-analog converter (DAC) in Silicon Germanium (SiGe) BiCMOS technology and using a VFO as the reference clock. Sine-weighted DAC is necessary for ultrahigh speed DDS design to overcome the speed limitation of the ROM lookup table (LUT) in conventional DDS designs. The sine-weighted DAC replaces ROM LUT and linear DAC to perform the phase-to-amplitude conversion (PAC) as well as digital-to-analog conversion. A segmented sine-weighted DAC is designed and implemented to achieve 10-bit amplitude resolution.

Due to the code dependent and frequency dependent non-ideal effects from the sine-weighted DAC, the unwanted harmonics and spurs of the DDS outputs have more significant impacts on the whole systems. In this dissertation, the spurs and harmonics from different

sources such as truncation errors, limited DAC amplitude resolutions and non-ideal effects of DAC will be discussed.

Four fabricated silicons are implemented in SiGe BiCMOS technology and discussed in the dissertation, including three DDSs and one VFO. The first DDS is a 11-bit 8.6 GHz ROM-less DDS with 10-bit segmented sine-weighted DAC. The second one is a 9-bit 2.9 GHz ROM-less DDS with direct digital modulation capabilities. The last DDS is a 24-bit 5.0 GHz ROM-less DDS with direct digital modulation capabilities. Besides the DDS designs, an 8.7-13.8 GHz VFO, implemented by a transformer coupled current-controlled varactor-less oscillator with quadrature outputs, will be presented in this dissertation, too. Circuit and layout designs of DDS building blocks such as current mode logic (CML), pipeline accumulator, carry look-ahead adder/accumulator, ripple-carry adder/accumulator and segmented and non-segmented sine-weighted DAC are presented. The quadrature current-controlled oscillator (QCCO) is discussed as well as the design and implementation of the on-chip transformer.

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List of Abbreviations

11B DDS the 11-Bit 8.6 GHz DDS

24B DDS the 24-Bit 5.0 GHz DDS

9B DDS the 9-Bit 2.9 GHz DDS

ADC Analog-to-Digital Converter

BFSK Binary Frequency Shift-Keying

BPSK Binary Phase Shift-Keying

CCO Current-Controlled Oscillator

CCW Chirp Control Word

CLA Carry-Look-Ahead

CLCC Ceremic Leadless Chip Carrier

CML Current Mode Logic

CMOS Complementary Metal-Oxide-Semiconductor

DAC Digital-to-Analog Converter

DDFS Direct Digiral Frequency Synthesizer

DDS Direct Digital Synthesizer

DFF D-Flip-Flop

DT Deep Trench

ENOB Effect Number of Bit

FA Full Adder

FCW Frequency Control Word

FM Frequency Modulation

FOM Figure-of-Merit

GCD the Greatest-Common-Divisor

HBT Heterojunction Bipolar Transistor

IC Intergrated Circuit

InP Indium Phosphide

LO Local Oscillator

LPF Linear Frequency Modulation

LPF Low-Pass Filter

LSB Least-Siginificant Bit

LUT Look-Up Table

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor

MSB Most-Siginificant-Bit

P-QVCO Parallel Voltage-Controlled Oscillator

PAC Phase-to-Amplitude Conversion/Converter

PCB Printed Circuit Board

PCW Phase Control Word

PGS Patterned Ground Shield

PLL Phase-Locked-Loop

PM Phase Modulation

PSAC-DAC Phase-to-Sine Amplitude Conversion Digital-to-Analog Converter

QCCO Qudrature Current-Controlled Oscillator

RCA Ripple Carry Adder

RFIC Radio Frequency Intergrated Circuit

RMS Root-Mean-Square

ROM Read Only Memery

S-QVCO Series Voltage-Controlled Oscillator

SFDR Spurious-Free-Dynamic-Range

SiGe Silicon Germanium

SINAD Signal-to-Noise and Total Harmonic Distortion

SMA SubMiniature version A

SNR Siginal-to-Noise Ratio

THD Total Harmonic Distortion

VCO Voltage-Controlled Oscillator

VNA Vector Network Analyzer

Chapter 1

Introduction

Ultrahigh speed [1] direct digital synthesizers (DDS)[2] RFIC [3] will play key roles in next generation radar and communication systems. Recent developments in radar systems require frequency synthesis with low power consumption, high output frequency, fine frequency resolution, fast channel switching and versatile modulation capabilities. Linear frequency modulation (LFM) or chirp modulation is widely used in radars to achieve high range resolution, while pulsed phase modulation (PM) can provide anti-jamming capability. With fine frequency resolution, fast channel switching and versatile modulation capabilities, the DDS provides frequency synthesis and direct modulation capabilities that cannot be easily implemented by other synthesizer tools such as analog-based phase-locked loop (PLL) synthesizers. It is difficult for conventional PLL-based frequency synthesizers to meet these requirements due to internal loop delay, low resolution, modulation problems and limited tuning range of the voltage-controlled oscillator (VCO). Ultrahigh-speed heterojunction bipolar transistors (HBT) allow a DDS to operate up to mm-wave frequency, which is a preferable solution to the synthesis of sine waveforms using in modern ultrahigh speed radar and other communication systems. [1, 2].

[1] Ultra high frequency (UHF) in ITU radio band means 300MHz to 3 GHz. In this dissertation, ultrahigh speed represents that DDS output frequency is over 1 GHz.

[2] Sometimes, use direct digital frequency synthesizer (DDFS). They represent same circuits and systems.

[3] Usually, the term of RFIC refers to the radio frequency or wireless integrated circuit fabricated in Si/SiGe CMOS/BiCMOS technologies. While the term of MMIC refers to the microwave monolithic integrated circuit fabricated in GaAs/InP high f_T technology. With the development of modern technology, the two terms appear to be merged together. So in this dissertation, both RFIC and MMIC represent RF/Microwave monolithic integrated circuit regardless what technology is fabricated in.

1.1 DDS Architectures

1.1.1 Conventional DDS

Conventional DDS design normally consists of a phase accumulator, a ROM lookup table (LUT) and a linear digital-to-analog converter (DAC). The phase accumulator computes the correct phase angle for the output sine wave by accumulating the input frequency control word (FCW) on each clock cycle. If the size of the accumulator is N bits, as shown in Fig. 1.1, the maximum phase value will be $2\pi(2^N - 1)/2^N$. To save power and reduce the complexity of the sinusoidal LUT, the N-bit output of the accumulator may be truncated to P bits before addressing the ROM. The ROM LUT performs a phase-to-amplitude conversion (PAC) of the output sinusoidal wave. Once the amplitude information is obtained, it may be further truncated to D bits that correspond to the number of input bits of the DAC. The digital amplitude codes are then fed into a linear DAC that generates an analog replica of the synthesized waveform. A low pass filter (LPF) usually follows the DAC to remove the unwanted frequency components. The input clock frequency and FCW determine the frequency step size of the DDS as

$$\Delta f = \frac{f_{clk}}{2^N}, \tag{1.1}$$

and the output frequency of the DDS is given by

$$f_{out} = f_{clk} \cdot \frac{\mathrm{FCW}}{2^N}, \tag{1.2}$$

where f_{clk} is the DDS clock frequency, FCW is the input frequency control word, and N is the size of the phase accumulator. Based upon the Nyquist theorem, at least two samples per clock cycle are required to reconstruct a sinusoidal wave without aliasing. Thus, the largest value of the FCW is $2^N - 1$. Therefore, the maximum output frequency of the DDS is limited to less than $f_{clk}/2$. However, the output frequency of the DDS is usually constrained to be less than $f_{clk}/3$ in a practical implementation of the deglitch LPF.

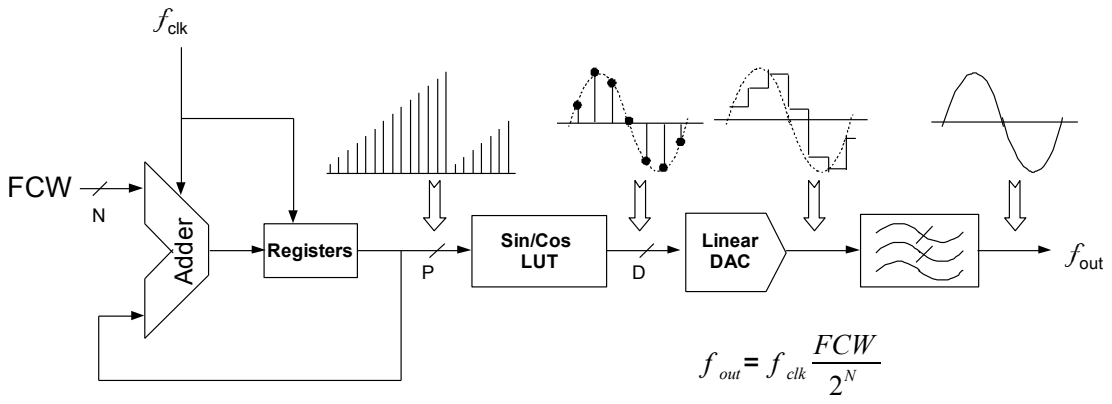


Figure 1.1: Block diagram of the conventional ROM-based DDS.

1.1.2 ROM-less DDS with Sin-weighted DAC

The ROM size of the conventional DDS increases exponentially with an increase of the number of phase bits used to address the LUT. In general, increasing the ROM size results in higher power consumption and larger area in ROM-based DDS designs. Numerous attempts have been made to compress or eliminate the ROM LUT in the PAC. Langlois has published a comprehensive review of the PAC techniques [3], including angular decomposition [4,5,6], angular rotation, sine amplitude LUT compression [7], polynomial approximation and phase-to-sine amplitude conversion (PSAC)-DAC combinations. All the phase-to-amplitude conversion methods with the exception of PSAC-DAC involve either a large ROM or a complex architecture, yet operate at relatively low speed. To overcome the speed and power performance limits of the ROM-based DDS with high resolution, a ROM-less DDS with sine-weighted DAC (identified as PSAC-DAC by Langlois) has been developed in both low speed and ultrahigh speed DDSs.

The conceptual block diagram of the ROM-less DDS employing a sine-weighted DAC is shown in Fig. 1.2. The ROM-less DDS replaces the ROM and linear DAC with a sine-weighted DAC that serves as a PAC block as well as a DAC. It eliminates the sine LUT, which is the speed and area bottleneck for high-speed DDS implementations. But, it is a

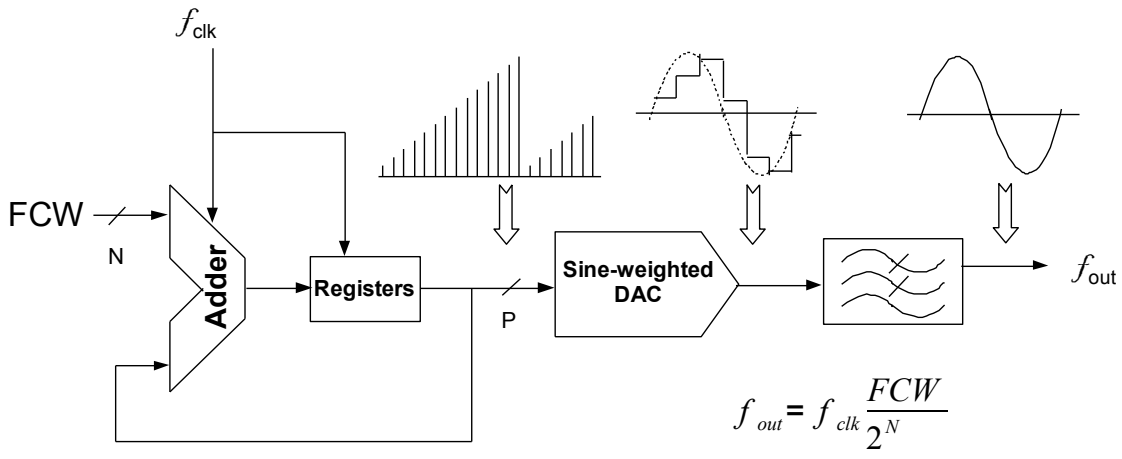


Figure 1.2: Block diagram of the ROM-less DDS.

design challenge to achieve high resolution in the sine-weighted DAC due to the required nonlinear segmentation process.

Fig. 1.3 shows a ROM-less DDS with segmented sine-weighted DAC. [8, 9]. The major part of the ROM-less DDS is an N-bit phase accumulator and a current-steering sine-weighted DAC. Since the output frequency cannot exceed the Nyquist rate, the most-significant-bit (MSB) of the accumulator input is tied to zero. The N-bit FCW (including MSB = 0) feeds the accumulator which controls the output frequency of the synthesized sine wave. The two MSBs of the accumulator output are used to determine the quadrant of the sine waveform. The remaining (P-2)-bits are use to control the segmented sine-weighted DAC in generating the amplitude for a quarter phase ($0 \sim \pi/2$) sine wave. With the segmentation method described in the following sections, (a + b) MSBs are used to control the coarse DAC, while the a-bit MSBs and c-bit least-significant-bits (LSB) are used to control the fine DACs.

1.1.3 ROM-less DDS with Direct Digital Modulations

With proper designs, DDS can be used to implement modulations and generate waveforms such as phase modulation (PM), linear frequency modulation (LFM), step frequency modulation (frequency hopping), binary frequency shift-keying (BFSK), binary phase shift-keying (BPSK) and other hybrid modulations. Fig. 1.4 shows a general architecture of a

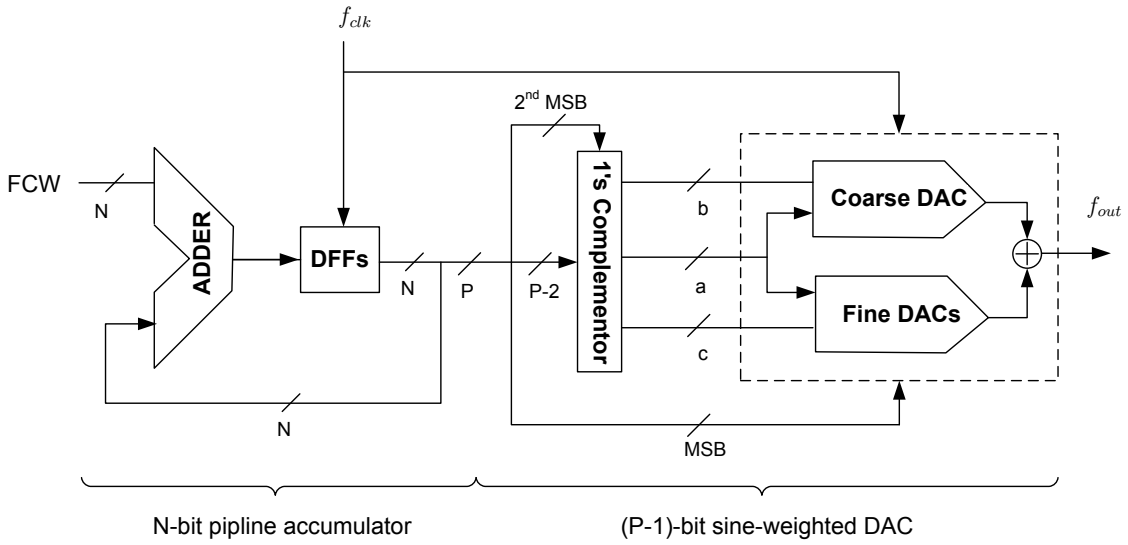


Figure 1.3: Block diagram of the ROM-less DDS with segmented sine-weighted DAC.

ROM-less DDS with direct digital modulation capabilities designed for radar system. The architecture has four parts, a D-bit sine-weighted DAC, a P-bit adder used as a phase modulator, an N-bit phase accumulator and another N-bit accumulator used as an N-bit chirp ramp signal generator. Chirp control words (CCW), frequency control words (FCW) and phase control words (PCW) provide the control signal for the chirp accumulator, phase accumulator and phase modulator, respectively. Through the direct use of digital control words to change the values of registers in the data path of the DDS, the frequency, phase, and amplitude of the output waveforms can be precisely controlled. Since all the modulations are done in the digital domain, many disadvantages associated with normal analog modulations can be avoided. In this ROM-less DDS architecture, the sine-weighted DAC assumes the responsibility for phase-to-amplitude conversion as well as digital-to-analog conversion. Without a ROM, which is usually the speed bottleneck, this DDS architecture can be developed to produce over-GHz frequency waveforms. To perform the direct digital modulations, the accumulators and modulator (full adder) must be updated in every clock cycle. As a result of this requirement, a pipeline accumulator is not suitable for the modulation, and the

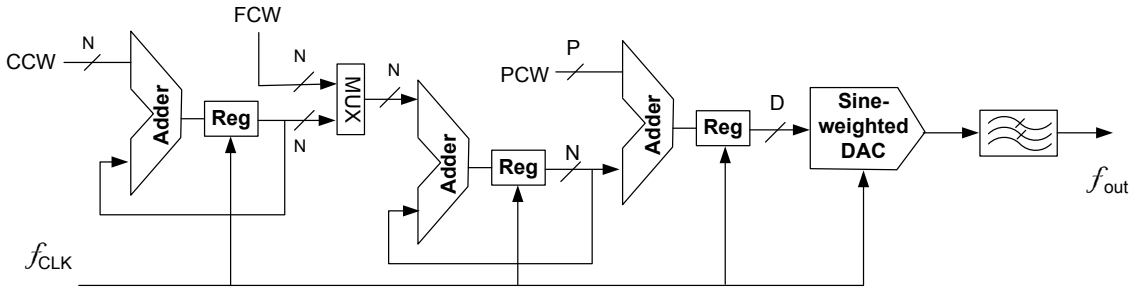


Figure 1.4: DDS block diagram with direct digital modulations.

carry-look-ahead (CLA) or ripple carry adder (RCA) architecture is used with an attendant sacrifice in speed.

Fig. 1.5 shows some direct digital modulation waveforms generated from a 16-bit phase resolution DDS. This DDS has both 16-bit FM resolution as well as 14-bit PM capabilities. Fig. 1.5(A) displays a BFSK modulation waveform. The input CCW switches between 16 and 32 for frequency f_1 and f_2 labeled in the waveform. Fig. 1.5(B) shows an LFM waveform with CCW = 2, which performs as though FCW is swept from 2 to 32, repeatedly. Fig. 1.5(C) shows a BPSK modulation waveform with FCW = 255 and PCW = 2^{15} for a phase shift of 180°.

1.2 Direct Digital Synthesizer Used in Modern Radar Systems

Range resolution is the ability of a radar system to distinguish between two or more targets on the same bearing but at different distances. Weapon-control radar, which requires great precision, should be able to distinguish between targets that are only yards apart. Search radar is usually less precise and only distinguishes between targets that are hundreds of yards or even miles apart. The degree of range resolution depends on the width of the transmitted pulse, the types and sizes of the targets, and the efficiency of the receiver and indicator. The range resolution of simple single pulse radar is $cT/2$, where c is the pulse transmitting velocity and T is the pulse width transmitted by the pulse radar. In pulse compression radar shown in Fig. 1.6, with the help of a versatile modulated signal generated

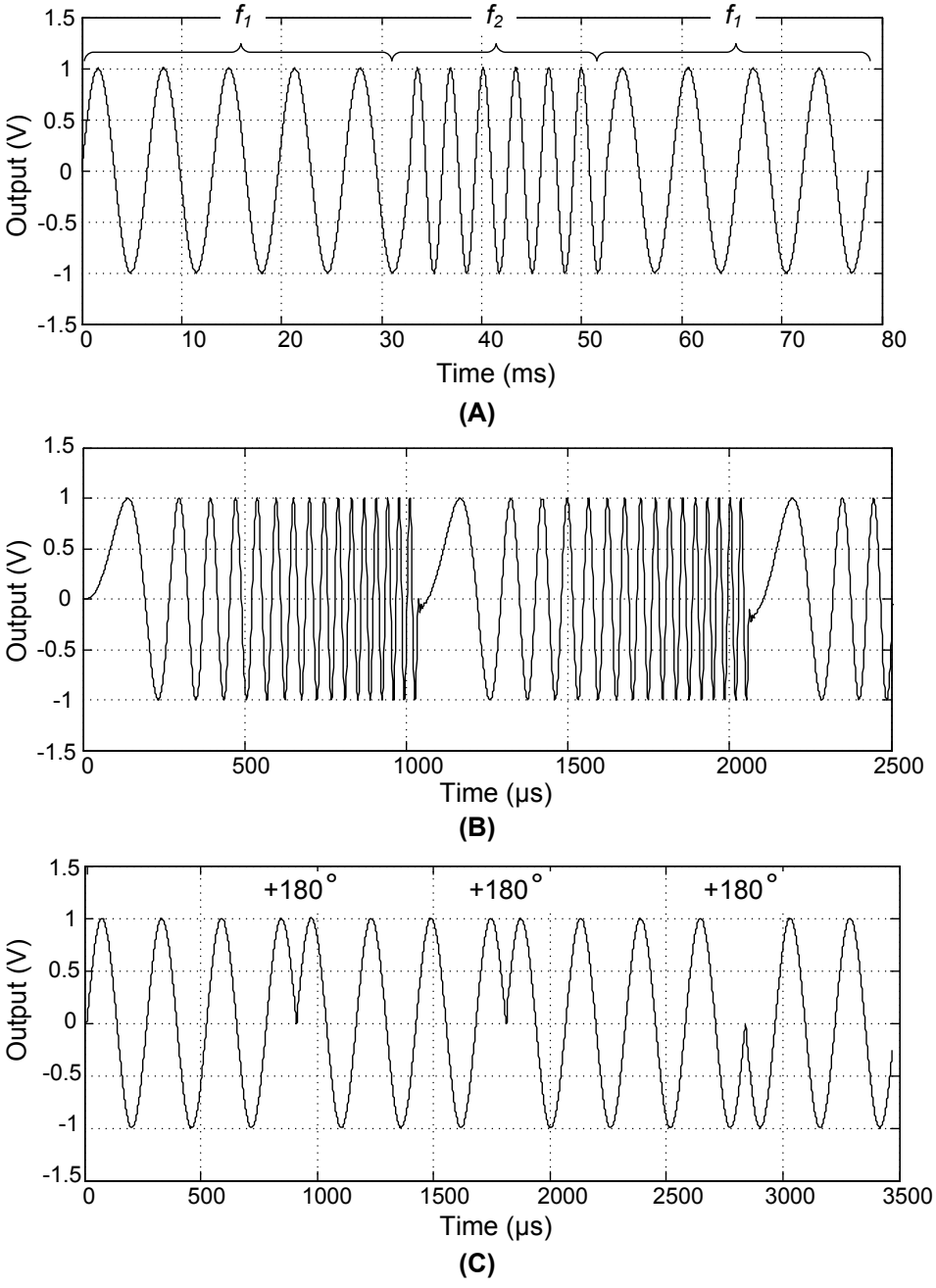


Figure 1.5: DDS direct digital modulations (A) BFSK (FCW = 16, ΔFCW = 32) (B) LFM (CCW = 2 or FCW sweeps from 2 to 32) (C) BPSK (FCW = 255, PCW = 2^{15}).

by a DDS, such as LFM, nonlinear FM or phase-coded waveforms, the range resolution can be improved to $c/(2B)$ without losing received pulse strength [10], where c is the signal

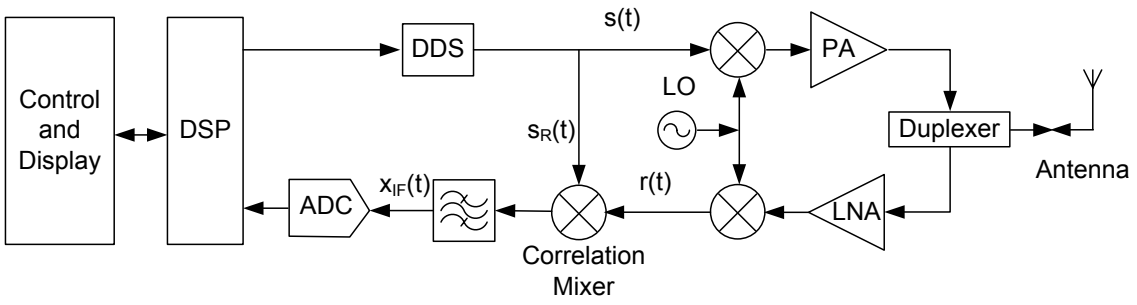


Figure 1.6: Simplified pulse compression radar with stretch processing.

transmitting velocity and B is the bandwidth of the transmitted signal. In comparison to the simple single pulse radar, the range resolution is increased by T/B times while the transmitted signal maintains the same instantaneous power. The quantity T/B is the pulse compression ratio, and it is usually much greater than 1.

The traditional radar receiver uses a wide bandwidth convolution processor with a matched filter to process the received pulse compression signal. It requires high bandwidth for the analog-to-digital converter (ADC) as well as the back-end processing. In modern radar system, stretch processing is used to reduce the bandwidth requirement of the ADC and back-end processing. Stretch processing is a technique for processing LFM, or other modulated wideband waveforms, using a signal processor with a bandwidth that is much smaller than the transmitted signal bandwidth, without losses in the signal-to-noise ratio (SNR) or range resolution [11, 12]. As shown in Fig. 1.6, stretch processing can be implemented in modern radar systems with the help of a simple mixer and the modulated reference signal generated from the same DDS as in the transmit path.

1.3 DDS Spectral Purity

In order to achieve fine step size, a large phase accumulator is desired. However, the phase accumulator output is normally truncated to save die area and power. For instance, the output of the phase accumulator is truncated into P bits (P<N). The number of phase

bits (P) is chosen based on the power and area budgets, as well as the signal-to-noise ratio (SNR) requirement of the DDS.

In the process of discrete phase accumulation and phase word truncation, spurs and quantization noise are introduced at the DDS output spectrum that can be modeled as a linear additive noise to the phase of the sinusoidal wave. Phase truncation error is periodic. If the MSBs of an N-bit phase word are used to address the DAC or LUT, the resultant spurs are mixed with the DDS output frequency generating spurs at multiples of that frequency [13], given by

$$f_{spur} = f_{clk} \cdot \frac{\mathrm{GCD}\left(\mathrm{FCW}, 2^{N-P}\right)}{2^{N-P}}, \tag{1.3}$$

where GCD(A, B) denotes the greatest-common-divisor (GCD) of A and B.

In addition to the spurious components, the DDS output waveform will suffer from amplitude distortion due to the finite number of quantization levels in the DAC. The envelope of the DDS output waveform is modulated by a sine wave with the frequency of

$$f_{Envelope} = f_{clk} \cdot \frac{2^{N-1} \mod \mathrm{FCW}}{2^{N-1}}. \tag{1.4}$$

Note that the envelope of the DDS output waveform is modulated by a low-frequency signal except when the FCW is an integer power of 2. For a Nyquist output, the frequency of the amplitude distortion, which looks like amplitude modulation (AM), is given by

$$\begin{aligned} f_{Envelope} &= f_{clk} \cdot \frac{2^{N-1} \mod \left(2^{N-1}-1\right)}{2^{N-1}} \\ &= f_{clk} \cdot \left(\frac{1}{2}\right)^{N-1}. \end{aligned} \tag{1.5}$$

In addition to the spurs that come from phase truncation, DAC spurs represent another big source of error. Spurious-free-dynamic-range (SFDR) is one of the most important specifications for the dynamic performance of a DAC, as well as a DDS. The sine-weighted DAC

shares many design challenges with the linear DAC. The most important factors affecting linear and sine-weighted current-steering DACs are summarized below [14]:

a. imperfect synchronization of the control signal at the switches;

b. digital signal feed-through via the C_{GD} or C_{BC} of the switch transistors;

c. voltage variation at the drain or collector of the current source transistors;

d. finite output impedance of the current switches.

The first three problems can be minimized by careful layout to balance the delays of the signal and clock paths such that the signals arriving at the switches are synchronized. However, it is not easy to distribute the high frequency clocks across long distances. To ensure clock synchronization, a specific clock distribution scheme, such as an H-tree or a grid topology, need to be employed.

SFDR is also affected by the output impedance of the DAC [15]. For an N-bit current-steering DAC with a typical switching structure shown in Fig. 1.7, the SFDR can be estimated as

$$\text{SFDR} \approx 20 \log \left(\frac{R_{unit}}{R_{load}} \right) - 6 \left(N - 2 \right), \tag{1.6}$$

where R_{unit} is the output impedance at the drain, or collector, of each switch, and R_{load} is the load resistance for the DAC output. In addition to other factors, R_{unit} must be maintained as high as possible in order to obtain a high SFDR in the desired frequency bandwidth. A cascode current source is a simple and effective way to increase the output impedance, and is adopted in this ultrahigh-speed sine-weighted DAC design.

1.4 Outline and Contribution

This dissertation is organized in the following chapters and the author's contributions are as follows:

Chapter 1: This chapter discussed the fundamental of DDS architecture, including the conventional ROM-based DDS and ROM-less DDS with sine-weighted DAC. A ROM-less

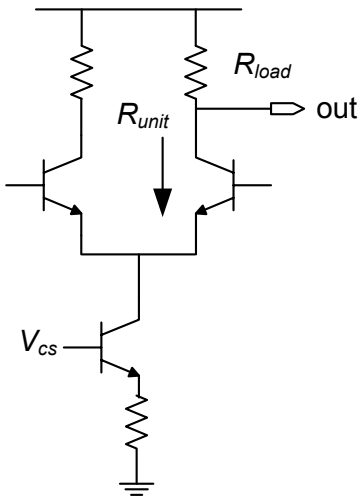


Figure 1.7: Typical switching structure of current-steering DAC

DDS with segmented DDS is presented, too. Direct digital modulation capabilities is very important when the DDS used in modern radar and communication systems. How the DDS with modulation capabilities works in stretch processing radar is evaluated. Finally, the DDS spectral purity is summarized.

Chapter 2: Sine-weighted DAC is introduced in this chapter. A segmented sine-weighted DAC used in ultrahigh speed ROM-less DDS is presented in the second part.

Chapter 3: A 11-bit 8.6 GHz DDS with 10-bit sine-weighted DAC (11B DDS) will be presented at Chapter 3. It is a low power, ultrahigh-speed and high resolution SiGe DDS RFIC with 11-bit phase and 10-bit amplitude resolutions. Using more than twenty thousand transistors, including an 11-bit pipeline accumulator, a 6-bit coarse sine-weighted DAC and eight 3-bit fine sine-weighted DACs, the core area of the DDS is 3×2.5 mm^2. The maximum clock frequency was measured at 8.6 GHz with a 4.2958 GHz output. The DDS consumes 4.8 W of power using a single 3.3 V power supply. It achieves the best reported phase and amplitude resolutions, as well as a leading power efficiency figure-of-merit (FOM) of 81.1 GHz$\cdot 2^{\mathrm{SFDR}/6}$/W in the ultrahigh speed DDS design. The measured SFDR is approximately 45 dBc with a 4.2958 GHz Nyquist output, and 50 dBc with a 4.2 MHz output in the Nyquist band at the maximum clock frequency of 8.6 GHz. Under a 7.2 GHz clock input,

the worst-case Nyquist band SFDR and narrow band SFDR are measured as 33 dBc and 42 dBc respectively. The measured phase noise with an output frequency of 1.57 GHz is -118.55 dBc/Hz at a 10 kHz frequency offset with a 7.2 GHz clock input generated from an *Agilent E*8257*D* analog signal generator. All the measurements were taken with the chips bonded in a CLCC[4]-52 package.

Chapter 4: A 9-bit 2.9 GHz DDS (9B DDS) with direct digital modulation capabilities will be presented at Chapter 4. It is a low power, high speed SiGe DDS RFIC with 9-bit phase and 7-bit amplitude resolutions. This DDS is one of the first reported GHz range output DDS RFIC with direct digital frequency and phase modulation capabilities. Using more than eight thousand transistors, the DDS RFIC includes a 9-bit CLA accumulator for phase accumulation, a 9-bit CLA adder for phase modulation and a 7-bit sine-weighted DAC. The core area of the DDS occupies 1.7×2.0 mm^2. The DDS consumes low power of 2.0 W under a 3.3 V single power supply even with the added modulation blocks. The narrow band SFDR is measured as 35 dBc with the maximum update frequency of 2.9 GHz. The DDS RFIC is tested in a CLCC-44 package.

Chapter 5: A 24-bit 5.0 GHz DDS (24B DDS) with direct digital modulation capabilities will be presented at Chapter 5. This design is a ultrahigh speed DDS with direct digital modulation capabilities used in a pulse compression radar. This design represents one of the first DDS RFIC in over-GHz output frequency range with direct digital modulation capabilities. It adopts a ROM-less architecture and has the capabilities for direct digital frequency and phase modulation with 24 bit and 12 bit resolution, respectively. The DDS includes a 24-bit RCA accumulator for phase accumulation, a 12-bit RCA for phase modulation and a 10-bit segmented sine-weighted DAC for phase-to-amplitude conversion as well as digital-to-analog conversion. The DDS core occupies 3.0×2.5 mm^2 and consumes 4.7 W of power with a single 3.3 V power supply. This 24-bit DDS has more than 20,000 transistors and achieves a maximum clock frequency of 5.0 GHz. The measured worst-case SFDR is 45

[4]CLCC represents ceramic lead-less chip carrier

dBc under a 5.0 GHz clock frequency and within a 50 MHz bandwidth. At 1.246258914 GHz output frequency, the 50 MHz narrow band SFDR is measured as 82 dBc. The best Nyquist band SFDR is 38 dBc with a 469.360351 MHz output using a 5.0 GHz clock frequency. This DDS was tested in a CLCC-68 package.

All the DDSs discussed in the above chapter outlines were developed in 0.13 μm silicon germanium (SiGe) BiCMOS technology with $f_T/f_{MAX} = 200/250$ GHz.

Chapter 6: Chapter 6 presents an 8.7-13.8 GHz transformer-coupled varactor-less quadrature current-controlled oscillator (QCCO) RFIC. It incorporates a transformer-coupled technique and tuned by changing the operation current through the primary and secondary windings. Fabricated in a 0.18 μm SiGe BiCMOS process, the prototype QCCO achieves a 45.3% wide tuning range. With two stacked octagonal transformers the QCCO core circuit occupies 0.4×0.5 mm^2 chip area and draws 8-18 mA current under a 1.8 V power supply. The measured phase noise is about -86.83 dBc/Hz at 1 MHz offset and 110 dBc/Hz at 10 MHz offset with 11.02 GHz quadrature outputs. The QCCO achieves a phase noise figure-of-merit of -154 dBc/Hz.

Chapter 7: The dissertation concludes in Chapter 7 with future research topics suggested.

Chapter 2

Design and Analysis of Sine-weighted DAC

2.1 Sine-weighted DAC

The sine-weighted DAC combines the sine/cosine mapping block with the digital-to-analog amplitude converter. The major difference between the linear DAC and sine-weighted DAC is that the linear DAC has an identical current source or a power of 2 weighted current sources for each bit, depending upon the decoder scheme, while the sine-weighted DAC has a variety of weighted current sources. Fig. 2.1 shows the structure of sine-weighted DAC with thermometer decoder. For the P-bit phase word, the first two MSBs are used to determine the quadrant of the sine wave, and the remaining P-2 bits will be used to represent one quarter phase ($0 \sim \pi/2$) of the sine wave. The current source matrix is calculated by Eq. (2.1).

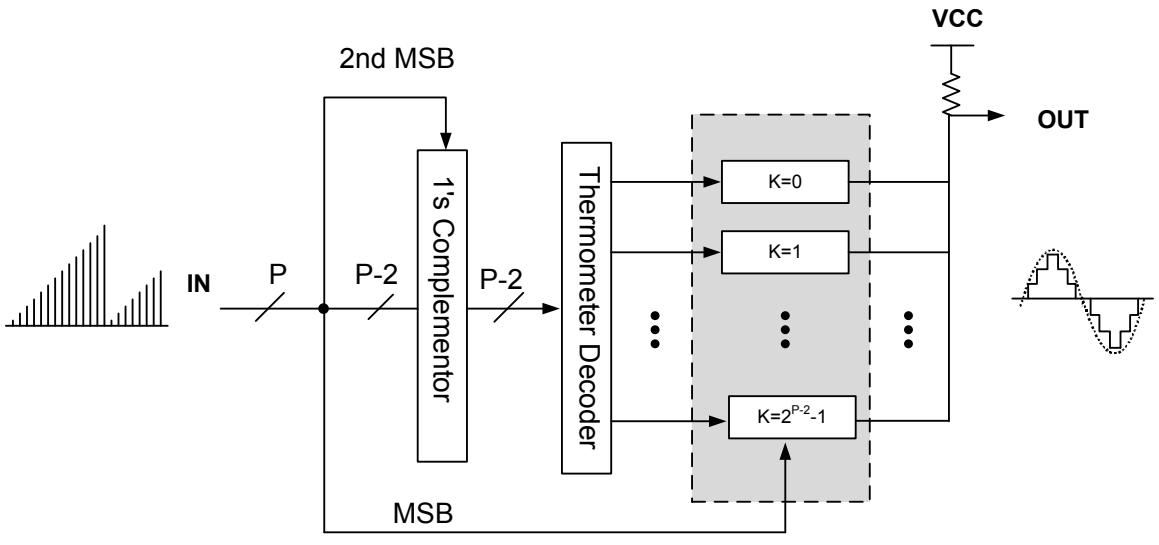


Figure 2.1: Block diagram of (P-1)-bit sine-weighted DAC.

$$I_k = \begin{cases} \lfloor \left(2^M - 1\right) \sin\left(\frac{\pi}{2} \cdot \frac{(0.5)}{2^{P-2}}\right) \rfloor, \text{for } k = 0 \\ \lfloor \left(2^M - 1\right) \sin\left(\frac{\pi}{2} \cdot \frac{(k+0.5)}{2^{P-2}} - \sum_{n=0}^{k-1} I_n\right) \rfloor, \ 0 \leq k \leq 2^{P-2} - 1 \end{cases} \tag{2.1}$$

In Eq. (2.1), P is the phase resolution of the sine-weighted DAC, which is the total input number of bit of the sine-weighted DAC. M is the amplitude resolution including the mirroring effect of the MSB. Usually, M=P-1, generated by the (P-2)-bit quater sine-wave and the mirroring of the MSB.

2.2 Segmented Sine-Weighted DAC

It is quite difficult to build a non-segmented DAC with more than 10 bit resolution due to the exponential increase in area and power consumption that results from increasing the DAC resolution. The problem becomes even more pronounced for sine-weighted DAC designs than the linear DAC. In linear DAC design, high accuracy can be achieved using segmentation. For instance, a 10-bit DAC can be segmented into a 5-bit coarse DAC and a 5-bit fine DAC, i.e., a 5+5 segmentation, while a 12-bit DAC can be segmented into an 8-bit coarse DAC and a 4-bit fine DAC, i.e., 8+4 segmentation [16, 13]. Similarly, a sine-weighted DAC can also be segmented into coarse DAC and fine DACs [17].

2.2.1 Quantization and Segmentation of the Sine Wave

For the P-bit phase word, since the quadrant of the sine waveform was determined by the two MSBs, only one quarter of the sine wave needs to be generated by the left P-2 bits. If we further segment the remaining P-2 phase bits in three parts with a, b and c bits (a + b + c = P-2), there are 2^{a+b+c} phase words for one quarter of the sine wave. The phase word can thus be represented as

$$\phi = x \cdot 2^{b+c} + y \cdot 2^c + z \tag{2.2}$$

with $0 \leq x \leq 2^a - 1, 0 \leq y \leq 2^b - 1$ and $0 \leq z \leq 2^c - 1$, where x, y and z are the phase sequence numbers related to the segmented parts a, b and c. Thus, if the amplitude of the sine wave is given by $A = 2^M - 1$, where M is number of amplitude bits, and for a specific phase word ϕ, the quarter sine wave can be represented as

$$\begin{aligned} & A \sin\left(\frac{\pi}{2} \cdot \frac{\phi}{2^{a+b+c}}\right) \\ & = (2^M - 1) \sin\left(\frac{\pi}{2} \cdot \frac{x \cdot 2^{b+c} + y \cdot 2^c + z}{2^{a+b+c}}\right) \\ & = (2^M - 1) \sin\left(\frac{\pi}{2} \cdot \frac{x \cdot 2^{b+c} + y \cdot 2^c}{2^{a+b+c}}\right) \cos\left(\frac{\pi}{2} \cdot \frac{z}{2^{a+b+c}}\right) \\ & + (2^M - 1) \cos\left(\frac{\pi}{2} \cdot \frac{x \cdot 2^{b+c} + y \cdot 2^c}{2^{a+b+c}}\right) \sin\left(\frac{\pi}{2} \cdot \frac{z}{2^{a+b+c}}\right). \end{aligned} \tag{2.3}$$

Since

$$z \ll x \cdot 2^{b+c} + y \cdot 2^c \ll 2^{a+b+c}, \tag{2.4}$$

we have

$$\cos(\frac{\pi}{2} \cdot \frac{z}{2^{a+b+c}}) \approx 1. \tag{2.5}$$

Thus, the sine wave can be approximated as

$$\begin{aligned} & A \sin\left(\frac{\pi}{2} \cdot \frac{\phi}{2^{a+b+c}}\right) \\ & \approx (2^M - 1) \sin\left(\frac{\pi}{2} \cdot \frac{x \cdot 2^{b+c} + y \cdot 2^c}{2^{a+b+c}}\right) \\ & + (2^M - 1) \cos\left(\frac{\pi}{2} \cdot \frac{x \cdot 2^{b+c} + y \cdot 2^c}{2^{a+b+c}}\right) \sin\left(\frac{\pi}{2} \cdot \frac{z}{2^{a+b+c}}\right) \\ & = C(x, y) + F(x, y, z), \end{aligned} \tag{2.6}$$

with

$$C(x, y) = (2^M - 1) \sin\left(\frac{\pi}{2} \cdot \frac{x \cdot 2^{b+c} + y \cdot 2^c}{2^{a+b+c}}\right), \tag{2.7}$$

$$F(x,y,z) = (2^M - 1)cos\left(\frac{\pi}{2}\cdot\frac{x\cdot 2^{b+c}+y\cdot 2^c}{2^{a+b+c}}\right) \cdot \sin\left(\frac{\pi}{2}\cdot\frac{z}{2^{a+b+c}}\right), \tag{2.8}$$

where $C(x,y)$ is the sinusoidal value to be stored in a coarse DAC, and $F(x,y,z)$ denotes the sinusoidal value to be stored in fine DACs, respectively. From the above decomposition, two sub-DACs can be designed to convert a complete sine wave to its analog waveform. The fine DAC data $F(x,y,z)$ can be used to interpolate the coarse DAC data $C(x,y)$. In order to quantize $C(x,y)$, the amplitude differences between the two adjacent coarse phase words are derived as shown in Eq. (2.9).

$$\Delta C(x,y) = \begin{cases} \lfloor (2^M-1)\sin\left(\frac{2\pi(0.5)}{2^P}\right)\rfloor, \text{for } x=y=0 \\ \lfloor (2^M-1)\sin\left(\frac{2\pi\left(x\cdot 2^{b+c}+y\cdot 2^c\right)}{2^P}\right) - \sum_{m=0}^{x-1}\sum_{n=0}^{2^b-1}\Delta C(m,n) - \sum_{n=0}^{y}\Delta C(x,n)\rfloor, \\ \qquad\qquad \text{for } 0\le x\le 2^a-1, 1\le y\le 2^b-1 \end{cases} \tag{2.9}$$

To simplify the quantization of $F(x,y,z)$, the average of y is used to represent every y value and $F(x,y,z)$ is thus simplified to $F(x,z)$. Hence, the amplitude difference between the two adjacent fine phase words for the fine DACs can be obtained as shown in Eq. (2.10).

$$\Delta F(x,z) = \begin{cases} \lfloor (2^M-1)\cos\left(\frac{2\pi\left(x\cdot 2^{b+c}+\overline{y}\cdot 2^c\right)}{2^P}\right)\sin\left(\frac{2\pi(0.5)}{2^P}\right)\rfloor, \text{for } z=0 \\ \lfloor (2^M-1)\cos\left(\frac{2\pi\left(x\cdot 2^{b+c}+\overline{y}\cdot 2^c\right)}{2^P}\right)\sin\left(\frac{2\pi(z+0.5)}{2^P}\right) - \sum_{n=0}^{z-1}\Delta F(x,n)\rfloor, \text{ for } 1\le z\le 2^c-1 \end{cases} \tag{2.10}$$

In Eqs. (2.9) and (2.10), it should be pointed out that

a. P is the truncated phase resolution, $P = a+b+c+2$;

b. $\lfloor A\rfloor$ denotes the rounding of number A down to the nearest integer toward zero;

c. $\overline{y} = \frac{0+1+\cdots+(2^b-1)}{2^b} = \frac{2^b-1}{2}$ is the average value of y; and

d. $F(x,z) = F(x,\overline{y},z) \approx F(x,y,z)$, where y is replaced with its averaged value. With Eqs. (2.9) and (2.10), the sine function can be rewritten as

$$\begin{aligned}(2^M - 1)\sin\left(\frac{\pi}{2}\cdot\frac{\phi}{2^{a+b+c}}\right) \\ &\approx C(x,y) + F(x,z) \\ &= \sum_{i=0}^{x}\sum_{j=0}^{y}\Delta C(x,y) + \sum_{i=0}^{x}\sum_{k=0}^{y}\Delta F(x,z),\end{aligned} \tag{2.11}$$

where the first term denotes the data stored in the coarse DAC current sources and the second term denotes the data stored in the fine DAC current sources.

This trigonometric decomposition is similar to the ROM compression in the ROM-based DDS. In the approaches by Sunderland [4] and Nicholas [5],

$$\begin{aligned}\sin(A+B+C) &= \sin(A+B)\cos(C) + \cos(A+B)\sin(C) \\ &\approx \sin(A+B) + \cos(A)\sin(C).\end{aligned} \tag{2.12}$$

The following two approximations

$$\begin{cases}\cos(C) \approx 1 \\ \cos(A+B) \approx \cos(A)\end{cases} \tag{2.13}$$

have been made, while in the approach adopted here, the approximation is improved by using

$$\begin{cases}\cos(C) \approx 1 \\ \cos(A+B) \approx \cos(A+\overline{B}),\end{cases} \tag{2.14}$$

where $\overline{B}$ is the mean value of B. The approximation error will be analyzed in the next subsection.

2.2.2 Approximation Error Analysis

In the previous subsection, two approximations are used for the coarse DAC and fine DACs respectively. The first is represented in Eq. (2.5). The second is the use of the mean value of y for the computation of $F(x, y, z)$. Both the approximations lead to errors in the computation of the sine wave's amplitude. For the coarse DAC the approximation error is

$$E_C = \cos\left(\frac{\pi}{2} \cdot \frac{x \cdot 2^{b+c} + y \cdot 2^c}{2^{a+b+c}}\right) - 1. \tag{2.15}$$

The maximum value of E_C is

$$\max\{E_C\} = \sin\left(\frac{\pi}{2} \cdot \frac{1}{2^{a+b}}\right), \tag{2.16}$$

when $x = 2^a - 1$ and $y = 2^b - 1$.

For the fine DACs,

$$E_F = \cos\left(\frac{\pi}{2} \cdot \frac{x \cdot 2^{b+c} + y \cdot 2^c}{2^{a+b+c}}\right) - \cos\left(\frac{\pi}{2} \cdot \frac{x \cdot 2^{b+c} + \overline{y} \cdot 2^c}{2^{a+b+c}}\right), \tag{2.17}$$

and the maximum value of E_F is

$$\max\{E_F\} \leq 2\sin\left(\frac{\pi}{2} \cdot \frac{1}{2^{a+2}}\right), \tag{2.18}$$

when $x = 2^a - 1$, $y = 2^b - 1$ and $\overline{y} = (2^b - 1)/2$.

If the whole DAC requires a 9-bit amplitude resolution, excluding the MSB mirroring, then the coarse DAC should have at least a 9-bit resolution and the fine DACs should have c-bit resolution. From Eqs. (2.16) and (2.18),

$$\begin{cases} \sin\left(\frac{\pi}{2} \cdot \frac{1}{2^{a+b}}\right) \leq \frac{1}{2^9} \\ 2\sin\left(\frac{\pi}{2} \cdot \frac{1}{2^{a+2}}\right) \leq \frac{1}{2^c}. \end{cases} \tag{2.19}$$

From Eq. (2.19),

$$\begin{cases} a+b \geq 4 \\ c \leq 6, \text{when } a=0 \\ c \leq 10, \text{when } a=4. \end{cases} \tag{2.20}$$

As long as a, b and c are in the range of Eq. (2.20), the approximation errors are less than the quantization noise and can be ignored.

2.2.3 Optimizing the Segmentation

From the above discussion, the quantization noise is significantly affected by the segmentation. To optimize the segmentation for better performance, one or more optimization parameters need to be considered. SFDR, power consumption and die area are the most critical parameters in the ultrahigh speed DDS design. An optimized segmentation figure-of-merit, normalized by the non-segmented values, is defined as

$$\text{FOM}_{sg} = -(\text{SFDR}_{sg} - \text{SFDR}_{ns}) \cdot \frac{P_{sg}}{P_{ns}} \cdot \frac{A_{sg}}{A_{ns}}. \tag{2.21}$$

where FOM_{sg}, SFDR, P and A represent the segmentation figure-of-merit, spurious-free-dynamic-range, power consumption and occupied area, respectively. The subscript "sg" means segmented DAC and "ns" denotes non-segmented DAC. Unlike CMOS logic design, where the power consumption results mainly from dynamic power, the primary power consumed by the current-mode-logic (CML) circuits that are used in the ultrahigh speed DDS designs is the static bias current in the CML current sources. Moreover, we assume that both the DAC power consumption and area are proportional to the number of DAC switch cells. If we segment the switch cells to a, b and c, the normalized number of switch cells is given by

$$\frac{2^{a+b} + 2^{a+c}}{2^{a+b+c}}. \tag{2.22}$$

Table 2.1: Simulated Segmentation FOM for Different Segmenations with 11-bit Phase and 10-bit Amplitude Resolutions

Segmentation a-b-c	SFDR	Normalized Power Consumption or Area	FOM_{sg}
2-2-5	51.08	0.2813	2.1895
2-3-4	57.73	0.1875	0.7390
2-4-3	65.44	0.1875	0.4679
3-2-4	64.03	0.3125	1.4375
3-3-3	71.07	0.2500	0.4675
3-4-2	72.19	0.3125	0.6406
4-2-3	72.05	0.3750	0.9422
4-3-2	70.87	0.3750	1.1081
4-4-1	71.27	0.5625	2.3667
4-5-0	78.75	1	0

which can be used to represent either the normalized power consumption P_{sg}/P_{ns} or the normalized area A_{sg}/A_{ns}. For a sine-weighted DAC with total 9 input bits, Table 2.1 shows the simulated SFDR, normalized power consumption or area and the FOM_{sg}. The results in Table 2.1 demonstrate that with a larger a or b, a better SFDR can be achieved, but power consumption and area will increase as well. Segmentation with $a + b = 9$ yields the best SFDR, yet it also leads to the highest power consumption and largest area. This result is understandable since $a + b = 9$ means a non-segmented DAC. The segmentation with $a = b = c = 3$ results in a good power and area efficiency, and a relatively high SFDR. Moreover, it achieves the best FOM_{sg} of 0.47. Note that the simulated SFDR in Table 2.1 includes only the effect of static quantization errors of the sine-weighted DAC, whereas the practical integrated circuit also suffers from other nonlinearities and distortions. As a result, the measured SFDR will be worse than what is given in Table 2.1.

Chapter 3

An 11-bit 8.6 GHz DDS RFIC with 10-bit Segmented Sine-weighted DAC

3.1 Introduction

Ultrahigh-speed HBTs allow a DDS to operate up to mm-wave frequency, which is a preferable solution to the synthesis of sine waveforms with fine frequency resolution, fast channel switching and versatile modulation capability [1,2]. There are several ultrahigh speed DDS designs reported with clock frequencies from 9 GHz to 32 GHz and DAC resolution from 5 bits to a maximum of 8 bits [18, 19, 20]. These DDSs have been implemented in indium phosphide (InP) (HBT) technology and only tested on-wafer [18, 19, 20]. The maximum achieved SFDR in these DDS designs is less than 30 dBc, which is not sufficient for typical radar and wireless applications. The low yield and high power consumption of InP HBTs limits the InP HBT-based DDS from achieving higher resolution. Several DDSs have been developed in SiGe BiCMOS technology with more robust and higher yield devices than the InP counterpart [21, 22]. However, theses earlier versions of SiGe DDSs still suffer from less than 30 dBc SFDR. A higher spectrum purity and higher amplitude resolution are required in modern radar and communication systems. With a segmented sine-weighted DAC, the DDS presented in this chapter achieves 11-bit phase and 10-bit amplitude resolutions with a maximum clock frequency of 8.6 GHz [8,9]. The DDS consumes 4.8 W with a leading power efficiency FOM of 81.1 GHz$\cdot 2^{\mathrm{SFDR}/6}$/W and the best reported Nyquist band worst-case SFDR of 33 dBc in ultrahigh speed DDS designs.

The proposed DDS adopts a ROM-less architecture, which combines both the sine/cosine mapping and digital-to-analog conversion together in a sine-weighted DAC [8,9]. The block diagram of the ROM-less DDS, with 11-bit phase and 10-bit amplitude resolution is shown in Fig. 3.1. The major part of the ROM-less DDS is an 11-bit pipeline phase accumulator

and a 10-bit current-steering segmented sine-weighted DAC. Since the output frequency cannot exceed the Nyquist rate, the MSB of the accumulator input is tied to zero. The 11-bit FCW (including MSB = 0) feeds the accumulator which controls the output frequency of the synthesized sine wave. The two MSBs of the accumulator output are used to determine the quadrant of the sine waveform. The remaining 9-bits are use to control the segmented sine-weighted DAC in generating the amplitude for a quarter phase ($0 \sim \pi/2$) sine wave. With the segmentation method described in Chapter 2, 3+3 MSBs are used to control the coarse DAC, while the 3-bit MSBs and 3-bit LSBs are used to control the fine DACs.

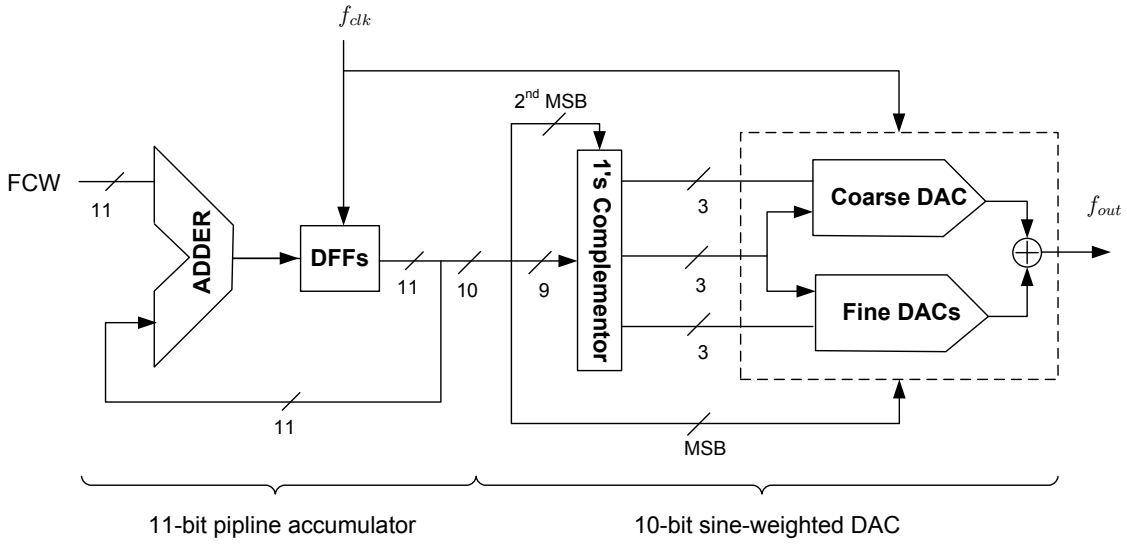


Figure 3.1: Block diagram of the ROM-less DDS with 10-bit segmented sine-weighted DAC .

3.2 Circuit Implementation of the 11-bit Rom-less DDS

With a 3.3 V power supply and a SiGe HBT base-collector voltage of 0.85 V∼0.9 V, all of the digital logic is implemented using 3-level CML with differential output swings of 400 mV. A trade-off has been made between the DDS operational speed and its power consumption. For an 11-bit packaged DDS RFIC, power consumption is the primary concern. To save

power, each tail current in a CML current source is set to 0.3 mA, which is close to 40% of the peak f_T current. In the contrast, traditional CML circuits are biased at 70∼80% of the peak f_T current. A traditional implementation of the CML circuits would end up with a DDS with power consumption larger than 9.0 W.

3.2.1 11-Bit Pipeline Accumulator

To achieve the maximum operating speed with a fixed FCW, a pipeline accumulator is used in this design. It uses the most hardware, but achieves the fastest speed. The total delay of the accumulator is one full adder (FA) propagation delay plus one D flip-flop (DFF) propagation delay.

Fig. 3.2 illustrates the architecture of the 11-bit pipeline phase accumulator, which has a total of 11 pipelined rows. Each row has a total of 12 DFF delay stages placed at the input and output of a 1-bit FA. Eleven DFF stages are needed for an 11-bit pipeline accumulator. One more DFF is used for each row to retime the signal for data synchronization. This scheme retimes the signal to remove the timing mismatch due to the metal wire delays from the accumulator output to its input. Obviously, the pipeline accumulator has a propagation delay of 12 clock cycles, including a latency period of 11 clock cycles plus one retiming clock cycle. Note that an accumulator requires at least one delay stage even without any pipelined stages. So the pipeline architecture shown in Fig. 3.2 allows the 11-bit accumulator to operate at the speed of a 1-bit accumulator consisting of an FA and a DFF.

3.2.2 10-Bit Segmented Sine-Weighted DAC

The block diagram of the 10-bit sine-weighted DAC is shown in Fig. 3.3. It has a 9-bit complementor and a current-steering sine-weighted DAC, which includes a 6-bit coarse DAC and eight 3-bit fine DACs. The MSB of the DAC input is used to provide the proper mirroring of the sine waveform about the π phase point. The 2nd MSB is used by the complementor to invert the remaining 9 bits for the 2nd and 4th quadrants of the sine waveform. The outputs

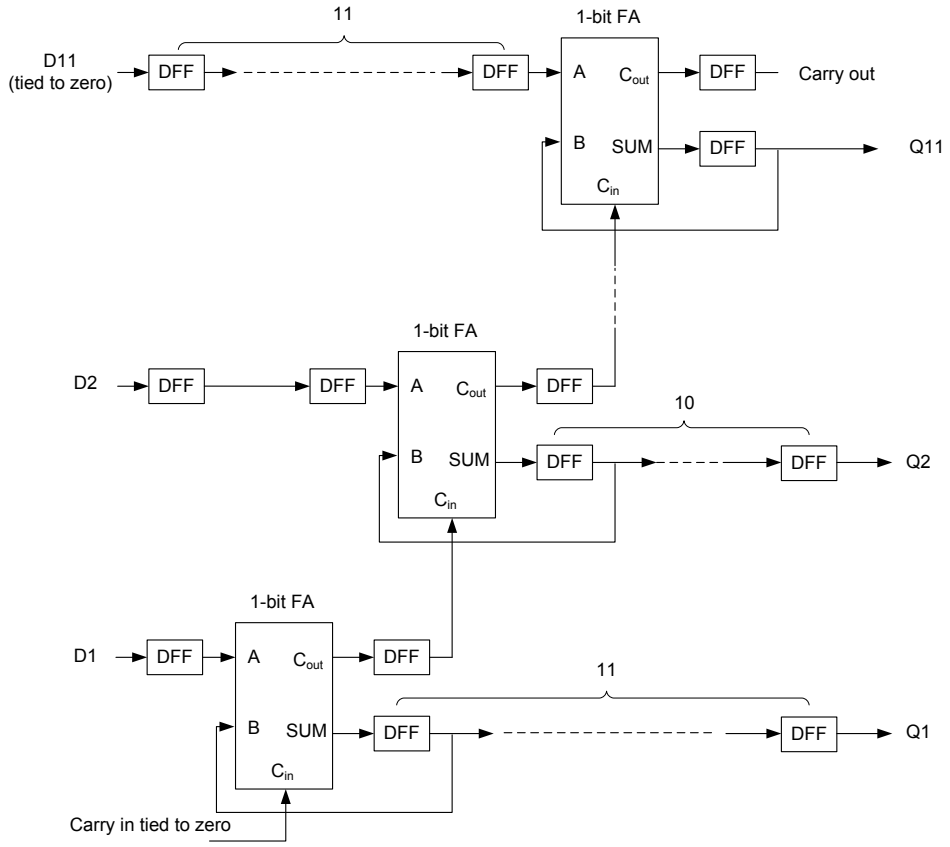


Figure 3.2: The 11-bit pipeline phase accumulator.

of the complementor are applied to the segmented sine-weighted DAC to form a quarter of the sine waveform. Because of the quadrant mirror, the total amplitude resolution of the sine-weighted DAC is 10-bits, while a 9-bit segmented sine-weighted DAC is used to generate the amplitude for a quarter phase ($0\sim \pi/2$) sine wave.

Based on the discussion in Chapter 2, setting $a = b = c = 3$ results in a segmentation with the best segmentation FOM. Therefore, the 9-bit sine-weighted DAC is divided into a 6-bit coarse sine-weighted DAC and eight 3-bit fine sine-weighted DACs. The first 6 bits of the complementor output control the coarse sine-weighted DAC, and the highest 3 bits also address the selection of the fine DACs. The lowest 3 bits of the complementor output determine the output value of each of the fine DACs.

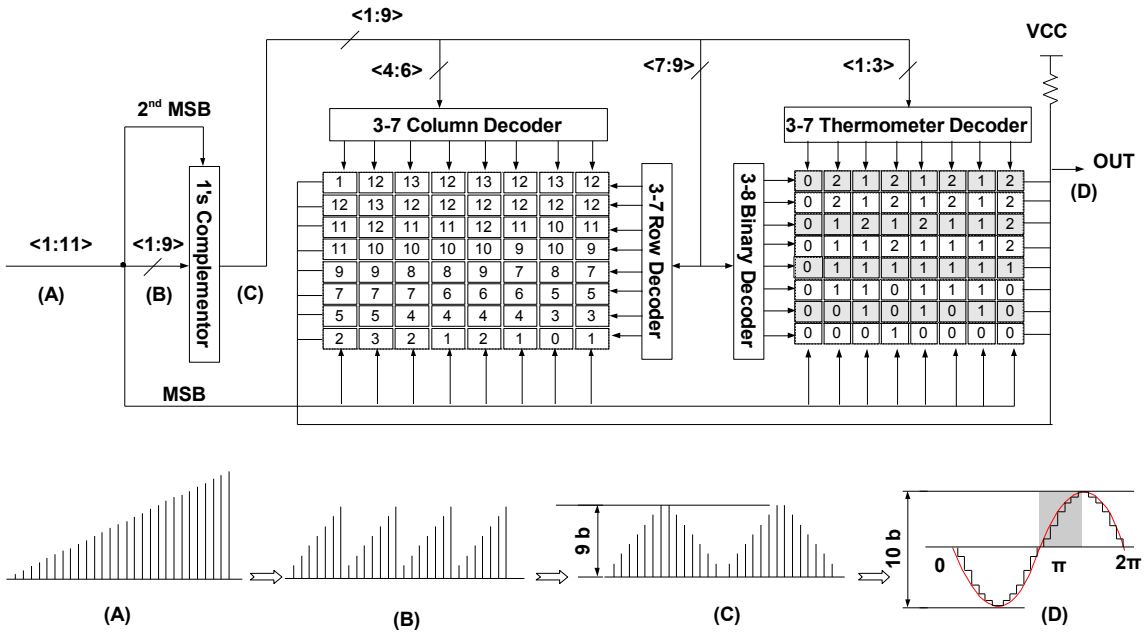


Figure 3.3: 10-bit segmented sine-weighted DAC.

With 11-bit phase and 10-bit amplitude resolutions, the weighted current sources of the coarse DAC and fine DACs can be calculated from Eqs. (2.9) and (2.10). The numbers within the coarse DAC and fine DACs in Fig. 3.3 represent the weights of the various current sources. To describe the DAC core architecture and its operation, an operator is defined between two 8×8 square matrices.

$$A \circledast B = a_{ij} \circledast b_{ij} = \sum_{i=0}^{7} \sum_{j=0}^{7} a_{ij} \cdot b_{ij}. \tag{3.1}$$

To match the sine-weighted DAC description, the matrix indices start from 0 instead of 1. As an example, for a specific phase word

$$\begin{aligned} \phi &= x \cdot 2^{b+c} + y \cdot 2^{c} + z \\ &= 64x + 8y + z, \end{aligned} \tag{3.2}$$

the quarter sine wave is rebuilt using Eq. (2.11) and represented in Eq. (3.3),

$$(2^M-1)\sin\left(\frac{\pi}{2}\cdot\frac{\phi}{2^{a+b+c}}\right)=1023\sin\left(\frac{\pi}{2}\cdot\frac{64x+8y+z}{2^9}\right)$$

$$=\underbrace{\begin{bmatrix}1&12&13&12&13&12&13&12\\12&13&12&12&12&12&12&12\\11&12&11&11&12&11&10&11\\11&10&10&10&10&9&10&9\\9&9&8&8&9&7&8&7\\7&7&7&6&6&6&5&5\\5&5&4&4&4&4&3&3\\2&3&2&1&2&1&0&1\end{bmatrix}}_{\text{Coarse current matrix}}\circledast\underbrace{\begin{bmatrix}c_{00}&c_{01}&c_{02}&c_{03}&c_{04}&c_{05}&c_{06}&c_{07}\\c_{10}&c_{11}&c_{12}&c_{13}&c_{14}&c_{15}&c_{16}&c_{17}\\c_{20}&c_{21}&c_{22}&c_{23}&c_{24}&c_{25}&c_{26}&c_{27}\\c_{30}&c_{31}&c_{32}&c_{33}&c_{34}&c_{35}&c_{36}&c_{37}\\c_{40}&c_{41}&c_{42}&c_{43}&c_{44}&c_{45}&c_{46}&c_{47}\\c_{50}&c_{51}&c_{52}&c_{53}&c_{54}&c_{55}&c_{56}&c_{57}\\c_{60}&c_{61}&c_{62}&c_{63}&c_{64}&c_{65}&c_{66}&c_{67}\\c_{70}&c_{71}&c_{72}&c_{73}&c_{74}&c_{75}&c_{76}&c_{77}\end{bmatrix}}_{\text{Coarse switch matrix}}$$

$$+\underbrace{\begin{bmatrix}0&2&1&2&1&2&1&2\\0&2&1&2&1&2&1&2\\0&1&2&1&2&1&1&2\\0&1&1&2&1&1&1&2\\0&1&1&1&1&1&1&1\\0&1&1&0&1&1&1&0\\0&0&1&0&1&0&1&0\\0&0&0&1&0&0&0&0\end{bmatrix}}_{\text{Fine current matrix}}\circledast\underbrace{\begin{bmatrix}f_{00}&f_{01}&f_{02}&f_{03}&f_{04}&f_{05}&f_{06}&f_{07}\\f_{10}&f_{11}&f_{12}&f_{13}&f_{14}&f_{15}&f_{16}&f_{17}\\f_{20}&f_{21}&f_{22}&f_{23}&f_{24}&f_{25}&f_{26}&f_{27}\\f_{30}&f_{31}&f_{32}&f_{33}&f_{34}&f_{35}&f_{36}&f_{37}\\f_{40}&f_{41}&f_{42}&f_{43}&f_{44}&f_{45}&f_{46}&f_{47}\\f_{50}&f_{51}&f_{52}&f_{53}&f_{54}&f_{55}&f_{56}&f_{57}\\f_{60}&f_{61}&f_{62}&f_{63}&f_{64}&f_{65}&f_{66}&f_{67}\\f_{70}&f_{71}&f_{72}&f_{73}&f_{74}&f_{75}&f_{76}&f_{77}\end{bmatrix}}_{\text{Fine switch matrix}}\tag{3.3}$$

where c_{ij} and f_{ij} represent the operation state (0 means open and 1 means closed) of the respective coarse DAC and fine DAC switches. Comparing to Eqs. (2.11) and (3.3), we have

$$c_{ij} = \begin{cases} 1, \text{ when } i < x \\ 1, \text{ when } i = x, j \leq y \\ 0, \text{ others,} \end{cases} \tag{3.4}$$

$$f_{ij} = \begin{cases} 1, \text{ when } i = x, j \leq z \\ 0, \text{ others,} \end{cases} \tag{3.5}$$

and

$$0 \leq x \leq 7, 0 \leq y \leq 7, \text{and } 0 \leq z \leq 7. \tag{3.6}$$

From Eq. (3.4), the control bits of the coarse DAC switch matrix can be generated through thermometer decoders. Fig. 3.4 shows the coarse DAC decoders. $d_{10} \sim d_4$ represent the input bits to the coarse DAC and $e_9 \sim e_4$ represent the complemented bits at the complementor output. The full 6-bit thermometer decoder includes 3 parts: a column decoder, a row decoder and second level decoders. $e_9 \sim e_7$ and $e_6 \sim e_4$ are inputs to the column decoder and row decoder, respectively. Following the second level thermometer decoder, 6-bit binary codes are converted to 64-bit thermometer codes represented by c_{ij}. As shown in Fig. 3.5, the control bits of the fine DAC's switch matrix can be generated through a thermometer decoder, a binary decoder and a second level address-select decoder. $d_{10} \sim d_7$ and $d_3 \sim d_1$ represent the input bits to the fine DACs. $e_9 \sim e_7$ and $e_3 \sim e_1$ represent the complemented bits at the complementor output. $e_3 \sim e_1$ is input through the thermometer decoder and converts the input bits for each fine DAC, and $e_9 \sim e_7$ is input through the binary decoder to generate the address-select code. The binary decoder and the address-select decoder work together to select which fine DAC is used to interpolate the respective coarse DAC steps. Through a combination of all the decoders, the 64-bit fine DAC control matrix is generated and represented by f_{ij} as described in Eq. (3.5).

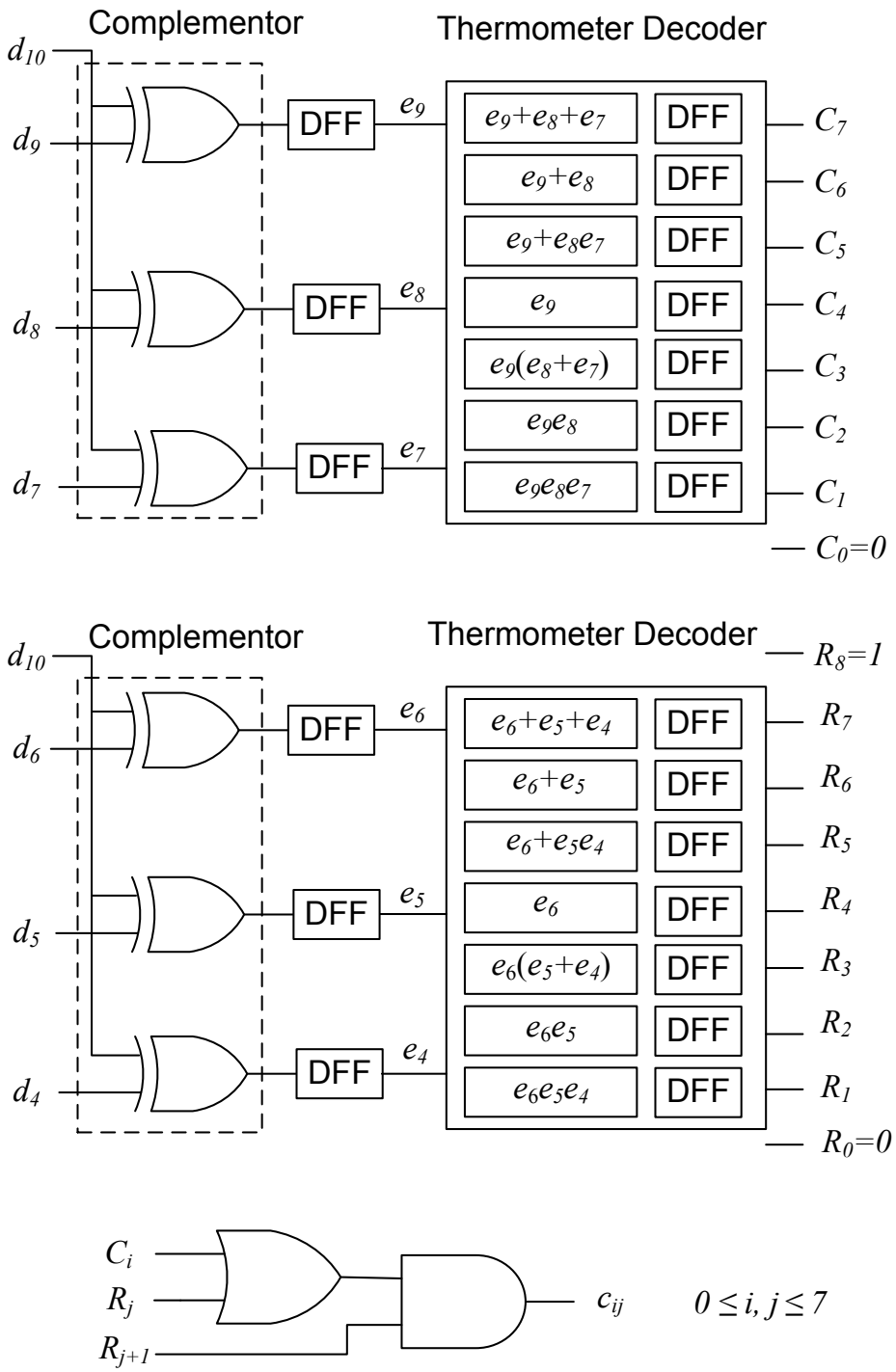


Figure 3.4: Coarse DAC thermometer decoder.

As shown in Fig. 3.6, the coarse DAC current source matrix provides 512 unit current sources. Each fine DAC uses about 8 unit current sources to interpolate the two adjacent outputs of the coarse DAC. For example, for a phase value represented by $x = 2$, $y = 3$ and

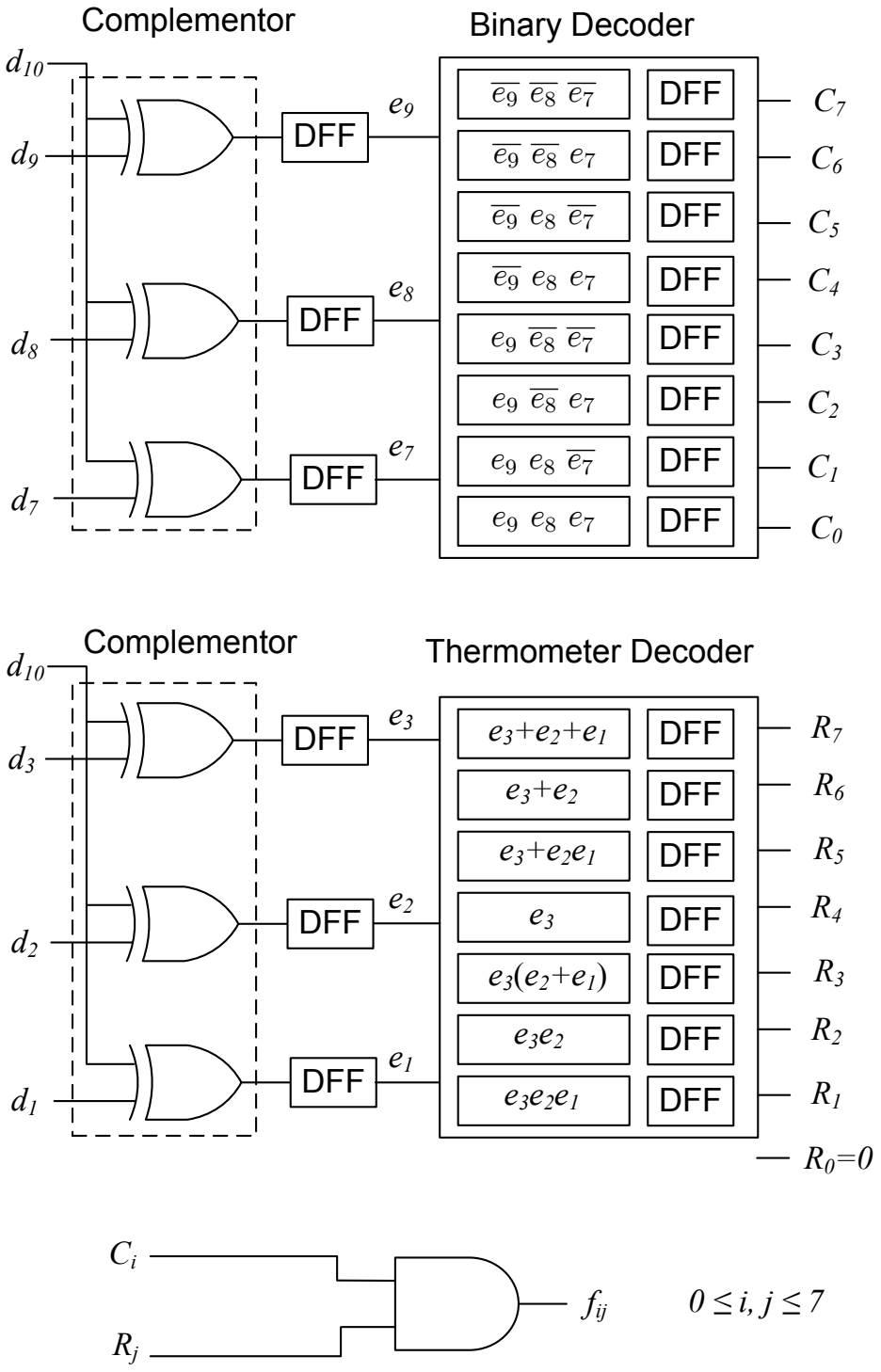


Figure 3.5: Fine DACs thermometer decoders.

$z = 5$, the coarse DAC current output is the sum of all the numbers filled in the gray-shaded boxes in the coarse DAC current matrix in Fig. 3.6. The fine DAC current output, which is

the sum of all the numbers filled in the gray-shaded boxes in the fine DAC current matrix, is added to the coarse DAC output. As a result, the total current output of the DAC is the sum of all the gray-shaded boxes and equal to 237 unit current sources. The unit current of each current source is set at 26 μA. The largest current in the current source matrix of this 10-bit sine-weighted DAC is 338 μA, which is composed of 13 unit current sources.

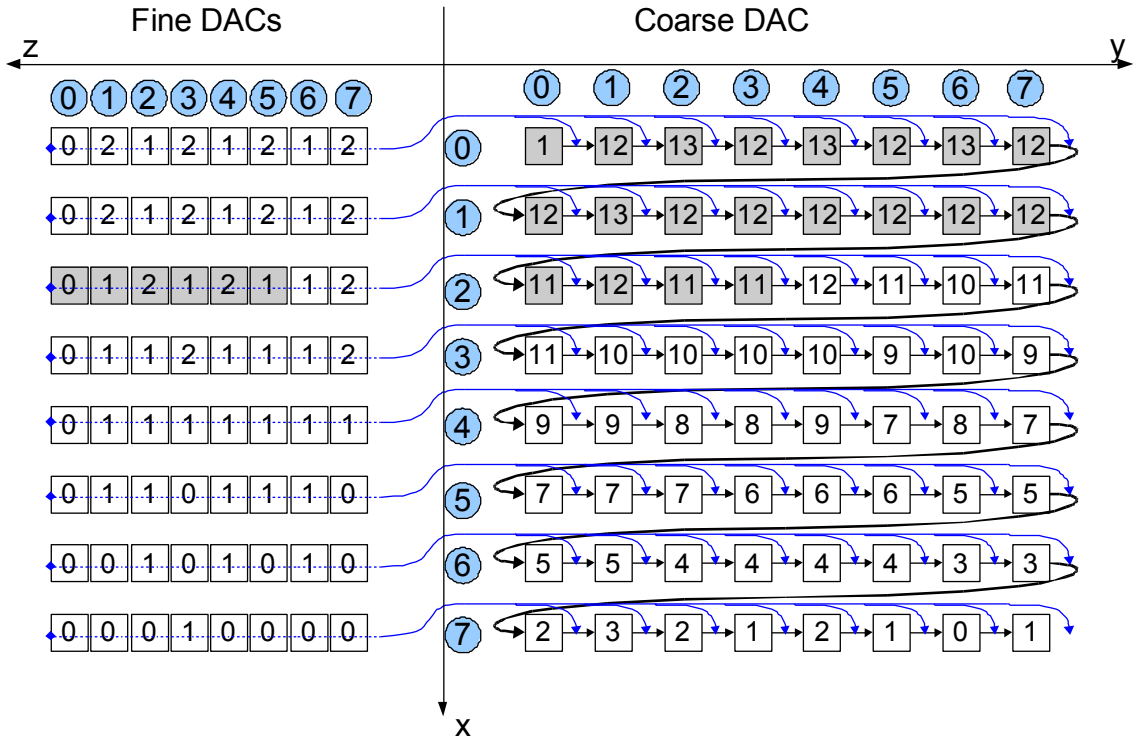


Figure 3.6: Illustration of interpolating the two adjacent outputs of a coarse DAC using the fine DAC current matrix.

The current switch contains two differential pairs with cascode current sources for improved output impedance and current mirror accuracy. The current outputs are converted to differential voltages by a pair of off-chip 15 Ω pull-up resistors. Fig. 3.7 shows that the currents from the cascode current sources are fed to outputs OUT_p and OUT_m by pairs of switches (M_{sw}). The MSB controls the selection between different half periods. The current switch contains two differential pairs with minimum size transistors and a cascode transistor to isolate the current sources from the switches, which also improves the bandwidth of the switching circuits.

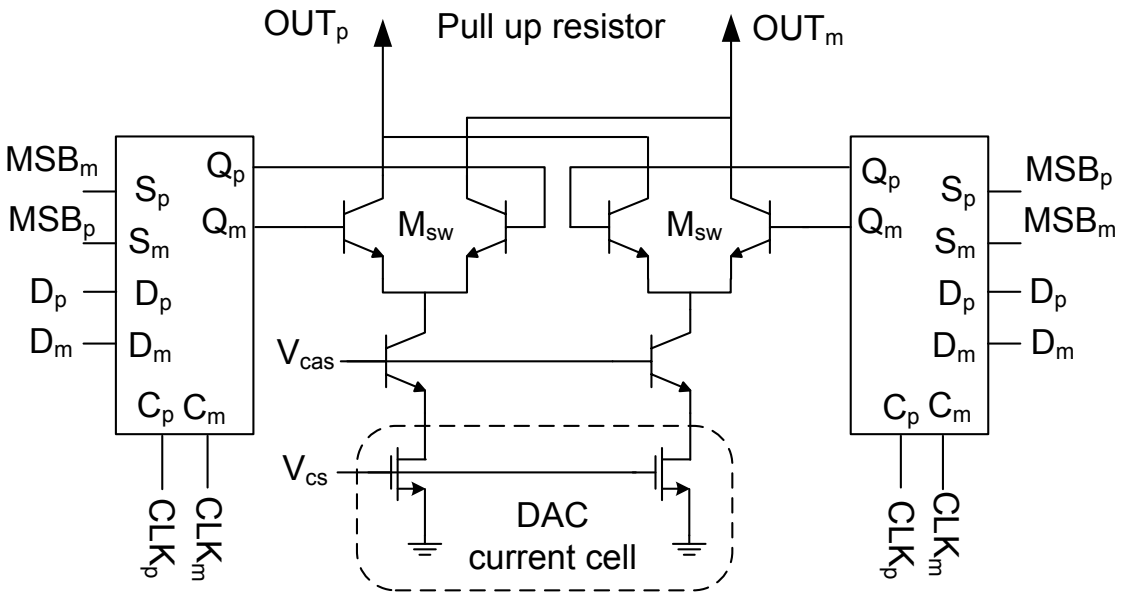


Figure 3.7: Current switch circuit of the sine-weighted DAC.

In order to achieve current source matching in the layout, each current source is split into four identical small current sources which carry a quarter of the required current. To further improve this matching, all the current source transistors, including those in the coarse DAC and fine DACs, are distributed in the current source matrix with a pseudo-double-centroid switching scheme [23]. The coarse DAC and fine DACs use a total of 568 current sources. Therefore, a 24 row by 24 column current source cells are used to build the current matrix in Fig. 3.8. All the current sources are distributed through a rotation from the matrix center to the edge. The total number of current source cells used for the coarse DAC are 511 and 57 are used for fine DACs. The remaining 8 current sources are used for bias. Four 24 by 24 current source matrices are placed around a common cenrtoid. Two dummy rows and columns are added around the current source matrix to avoid edge effects. So the complete current matrix has 52 rows and 52 columns.

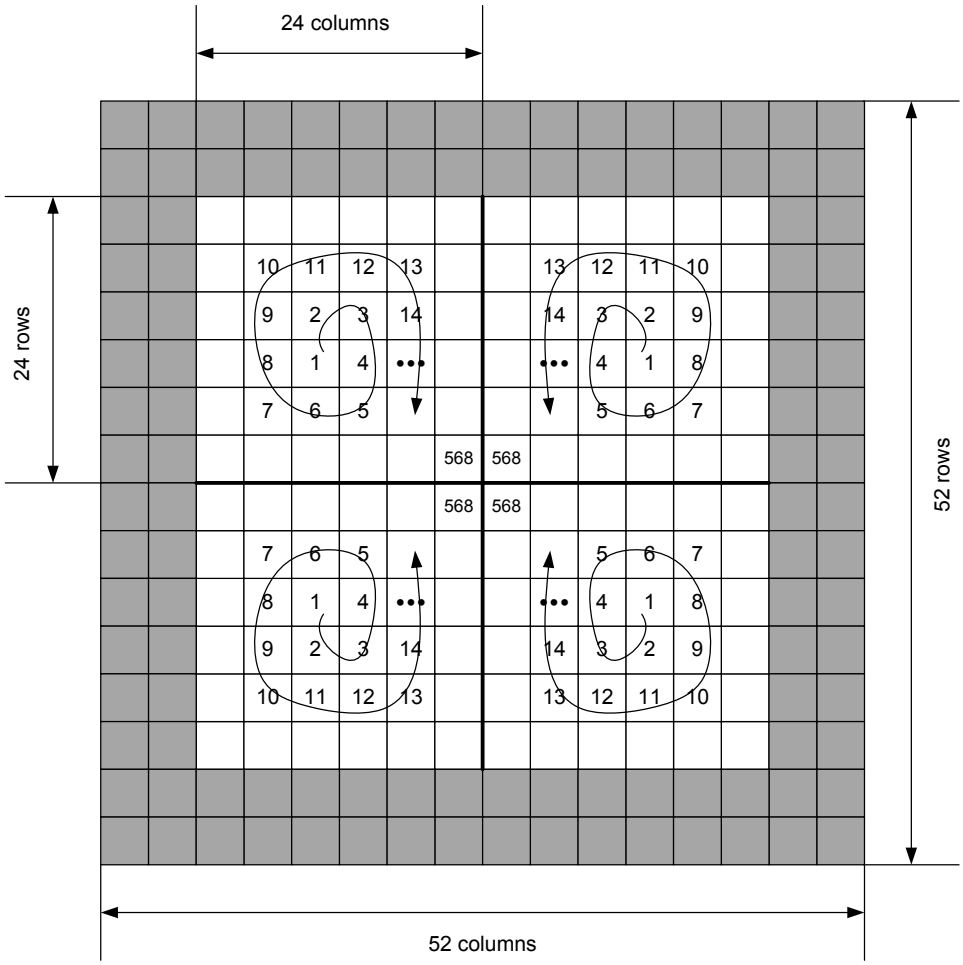


Figure 3.8: Diagram of the current source matrix.

3.2.3 Clock Distribution

To synchronize the signal in high speed circuit design, numerous DFFs are used between the logic elements. In the accumulator design, the number of the DFFs in the pipeline accumulator increases rapidly with the increasing number of the pipeline stages. Hence there are more than 100 DFFs used in the 11-bit pipeline accumulator. Counting the number of the DFFs used in the sine-weighted DAC to synchronize the current switches, it yields approximately 300 DFFs. All of these DFFs must be synchronized with a simultaneous clock edge. In order to minimize the phase difference and maintain the same drive strength between the clock and DFFs, an H-tree clock scheme is used to ensure that the clock signal reaches each block simultaneously. Fig. 3.9 shows a simplified architecture of the "H"-shaped clock

tree. The actual clock tree is 3 times bigger than the simplified version shown in Fig. 3.9. The external clock is buffered by a differential pair and then drives two emitter follower pairs which are used as a level-shifter as well as a buffer. Each emitter follower pair drives two or four differential pairs and each differential pair drives other emitter follower pairs, until the clock reaches the leaves that finally drive the DFFs. The number of differential pairs or emitter follower pairs driven by the previous stage depends on the driving strength of the previous stage and is proportional to the CML tail current. To keep enough swing fully switching the next stage, a 1-driving-2 current ratio is maintained throughout the whole clock buffer tree.

3.3 Experimental Results

The die photo of the SiGe DDS RFIC is shown in Fig. 3.10. This DDS design is quite compact with an active area of 3×2.5 mm^2 and a total die area of 4×3.5 mm^2. The DDS was tested in a CLCC-52 package. Fig. 3.11 shows the packaged chip soldered on a PCB fabricated with *RO*4004 material. The clock signal is generated from an *Agilent E*8257*D* analog signal generator and is converted to differential signals by a hybrid coupler. Two SMA connectors and symmetrical tracks are used to send the clock signal to the DDS chip. The DDS current outputs are converted to voltage outputs through a pair of 15 Ω on-board resistors and connected to the spectrum analyzer or oscilloscope through SMA connectors and RF cables.

The package has a thermal resistance of approximately 30 °C/W. With a 4.8 W power consumption at room ambient temperature, the junction temperature of the SiGe devices can theoretically reach as high as 180 °C. At such high temperature, the device performance is greatly degraded and the DAC current switches are no longer synchronized due to increased internal delays, which introduce noticeable distortion in the output waveform. When the device is effectively cooled, the DDS operates at a maximum clock frequency of 8.6 GHz.

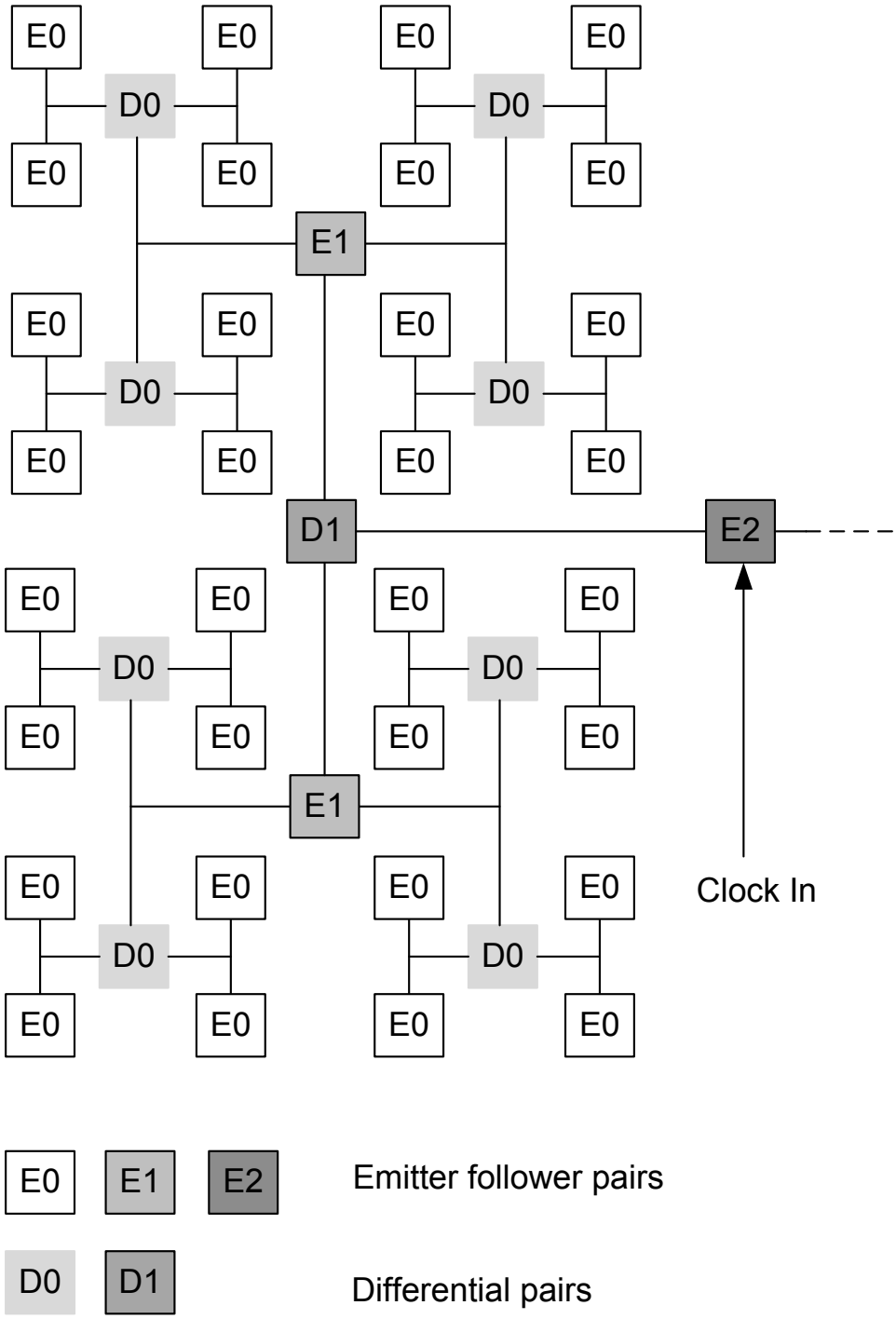


Figure 3.9: Simplified clock tree distribution.

At room temperature, the packaged DDS operates at the maximum clock frequency of 7.2 GHz.

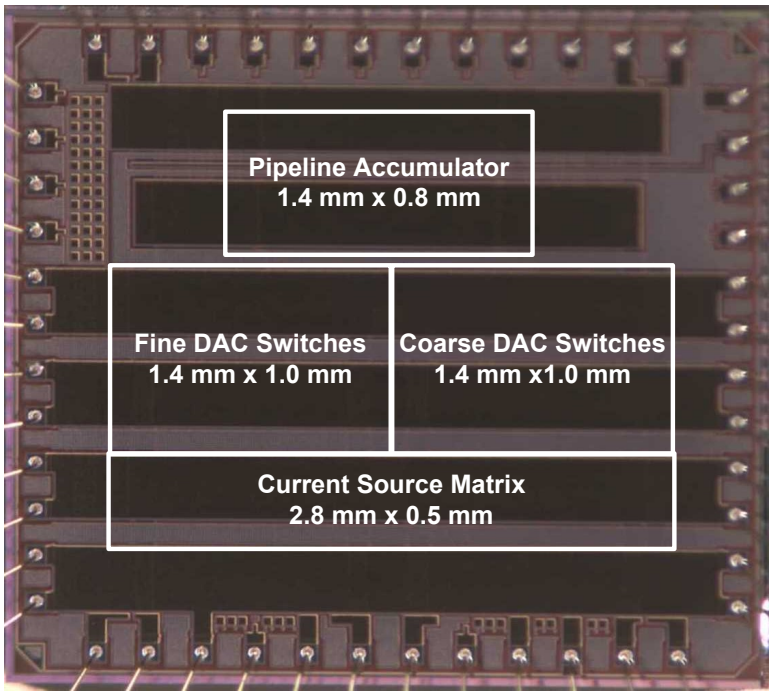


Figure 3.10: Die photo of the 11-bit ROM-less DDS RFIC.

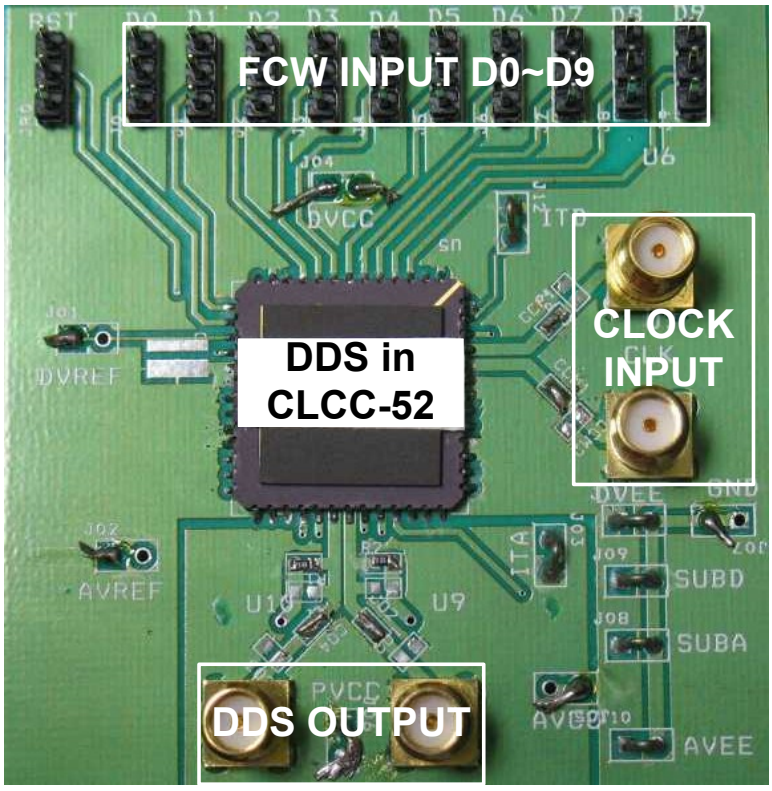


Figure 3.11: Evaluation board for the 11-bit ROM-less DDS RFIC.

Figs. 3.12-3.15 illustrate the measured DDS output spectra and waveforms for different outputs and clock frequencies. All measurements were done with packaged parts and without calibrating the losses of the cables and PCB tracks. Fig. 3.12 presents a 4.2 MHz DDS output spectrum with an 8.6 GHz clock input, and a minimum FCW of 1. The measured output power is approximately -8.3 dBm, and the measured SFDR is about 50 dBc. The tone at 91.7 MHz was generated by the nearby campus FM radio station. To show the signal tone clearly, a 100 MHz band spectrum plot is used instead of the full Nyquist band. However, the worst-case spur is located within this band, so within both the Nyquist band and the narrow band the SFDR is 50 dBc. Fig. 3.13 shows the waveform for the spectrum in Fig. 3.12.

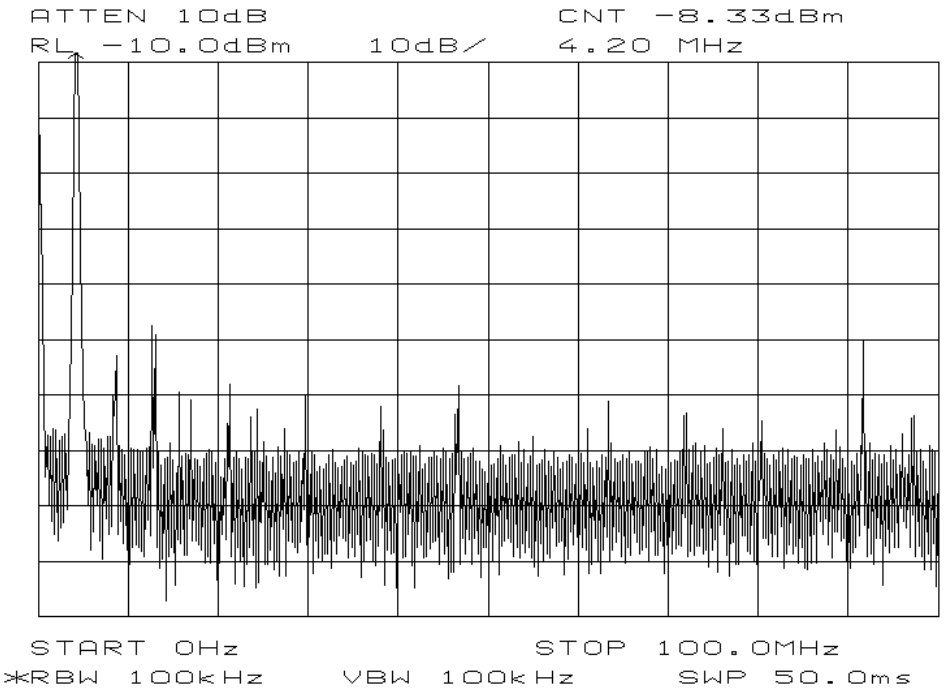


Figure 3.12: Measured DDS output spectrum with a 4.2 MHz output and a maximum 8.6 GHz clock (FCW = 1), illustrating about 50 dBc SFDR. The tone at 91.7 MHz is from the nearby campus FM radio station.

Fig. 3.14 demonstrates the operation of the DDS at a maximum clock frequency of 8.6 GHz with Nyquist output (i.e., FCW = 1023). Thus, the output frequency is set as

$$\frac{2^{10}-1}{2^{11}} \times f_{clk} = 4.2958 \text{ GHz}. \tag{3.7}$$

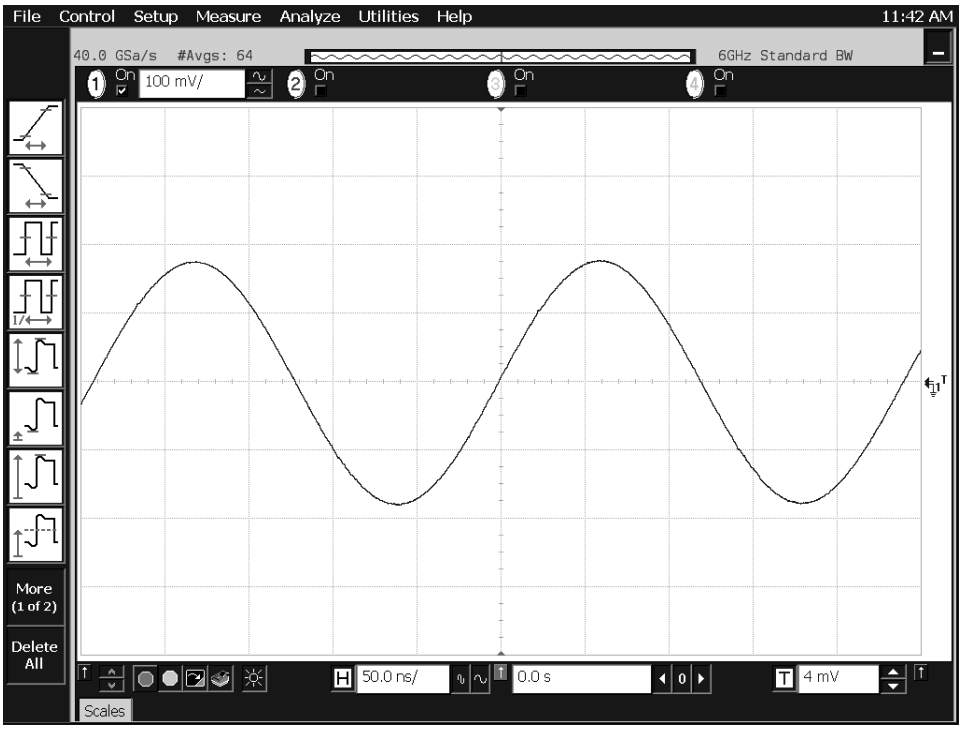


Figure 3.13: Measured DDS output waveform with a 4.2 MHz output and an 8.6 GHz clock.

The first order image tone due to mixing the clock frequency and the DDS output frequency occurs at

$$8.6 \text{ GHz} - 4.2958 \text{ GHz} = 4.3042 \text{ GHz}. \tag{3.8}$$

The measured SFDR of the device is approximately 45 dBc. The tone at 91.7 MHz once again appears in the spectrum. Fig. 3.15 illustrates the measured DDS output waveform with a 4.2958 GHz Nyquist output and an 8.6 GHz clock. The signal envelope frequency results from mixing the output and its image, which is

$$\frac{2^{10}+1}{2^{11}} \times f_{clk} - \frac{2^{10}-1}{2^{11}} \times f_{clk} \approx 8.4 \text{ MHz}. \tag{3.9}$$

Fig. 3.16 shows the measured DDS SFDR plot at both the Nyquist band (3.6 GHz) and the narrow band (100 MHz) versus the FCW with a clock frequency of 7.2 GHz. The worst-case SFDR is 33 dBc and 42 dBc for the Nyquist band and narrow band, respectively.

Fig. 3.17 shows the measured DDS phase noise at an output frequency of 1.57 GHz with a 7.2 GHz clock input frequency. There is a -118.55 dBc/Hz phase noise at a 10 kHz frequency offset. The input clock is generated from an Agilent E8257D analog signal generator. The spurs showing in the measurement are not harmonically related to the synthesized output frequency. It is test environment related.

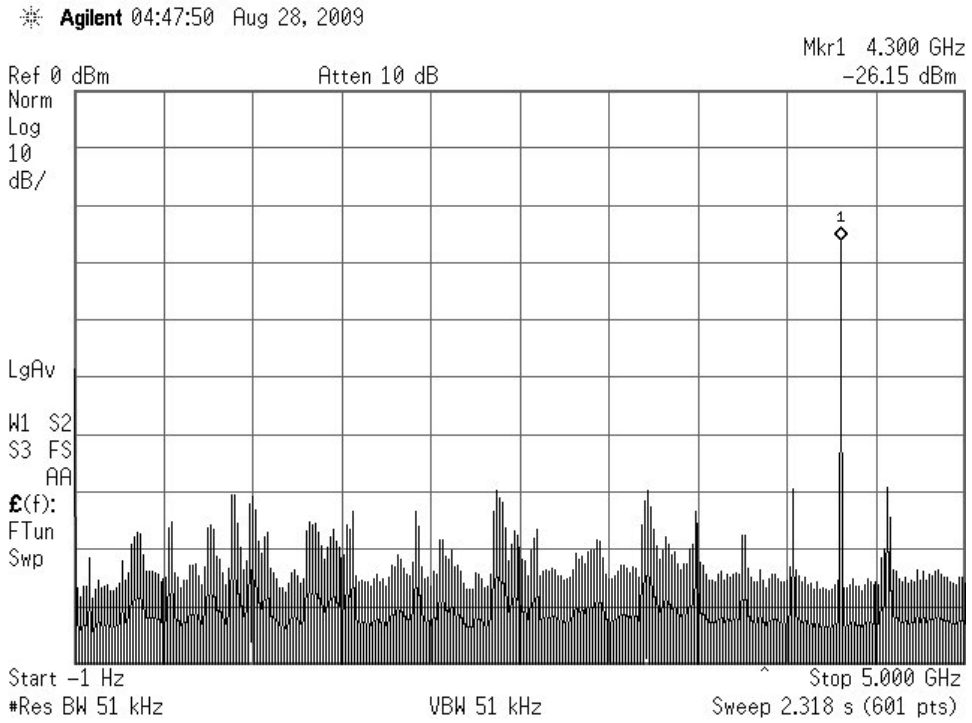


Figure 3.14: Measured DDS Nyquist output spectrum with a 4.2958 GHz output and a maximum 8.6 GHz clock (FCW = 1023), illustrating about 45 dBc SFDR. The image tone is located at 4.3042 GHz.

To evaluate the performance of ultrahigh speed DDSs, an easily measured and calculated FOM must be defined from a combination of performance parameters. In the previous literature [24], a power efficiency FOM has been defined as

$$\text{FOM} = \frac{\text{Max. Clock(GHz)}}{\text{Power(W)}}. \tag{3.10}$$

This previously defined FOM includes the maximum update frequency as well as the power consumption, but does not consider the amplitude resolution information, which is

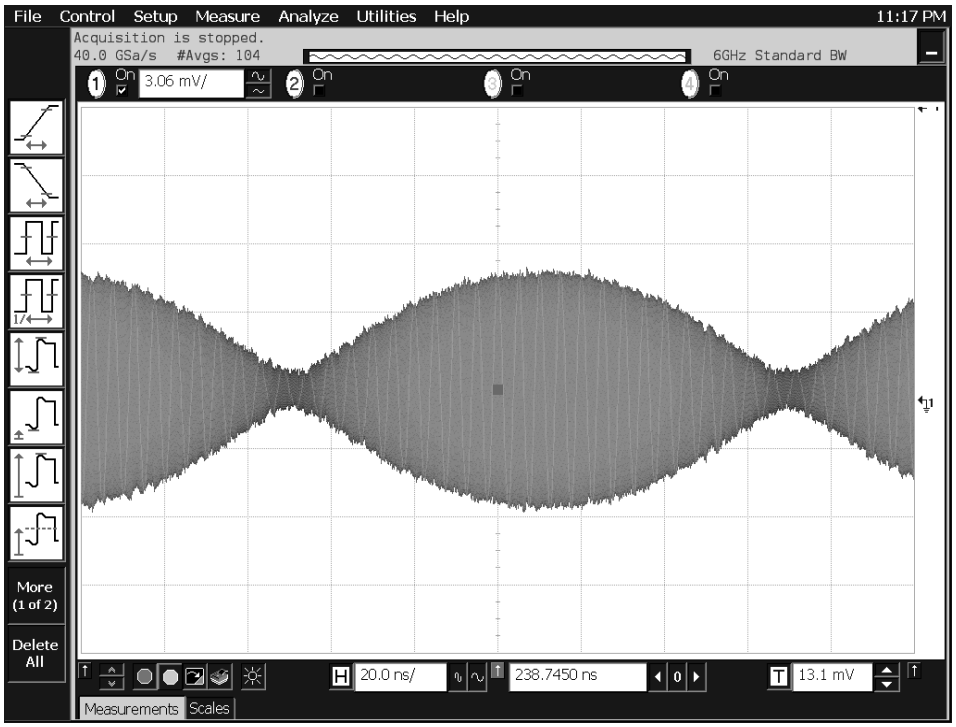


Figure 3.15: Measured DDS output waveform with a 4.2958 GHz Nyquist output and an 8.6 GHz clock. The 8.4 MHz envelope frequency results from mixing the output and its image.

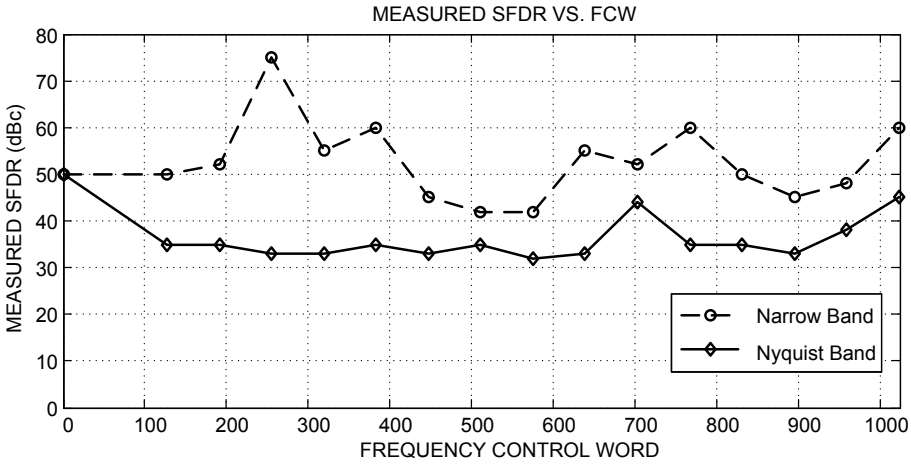


Figure 3.16: The measured DDS SFDR versus FCW at clock frequency of 7.2 GHz. Illustrating a worst-case SFDR of 33 dBc for the Nyquist band (3.6 GHz) and 42 dBc for the narrow band (100 MHz), respectively.

limited by the DAC. For an ultrahigh speed DDS, this lack of information is unfortunate since the DAC is the most challenging part of these DDS designs. Thus, we define a new FOM including the effective number of bits (ENOB) that measures the DAC spurious performance.

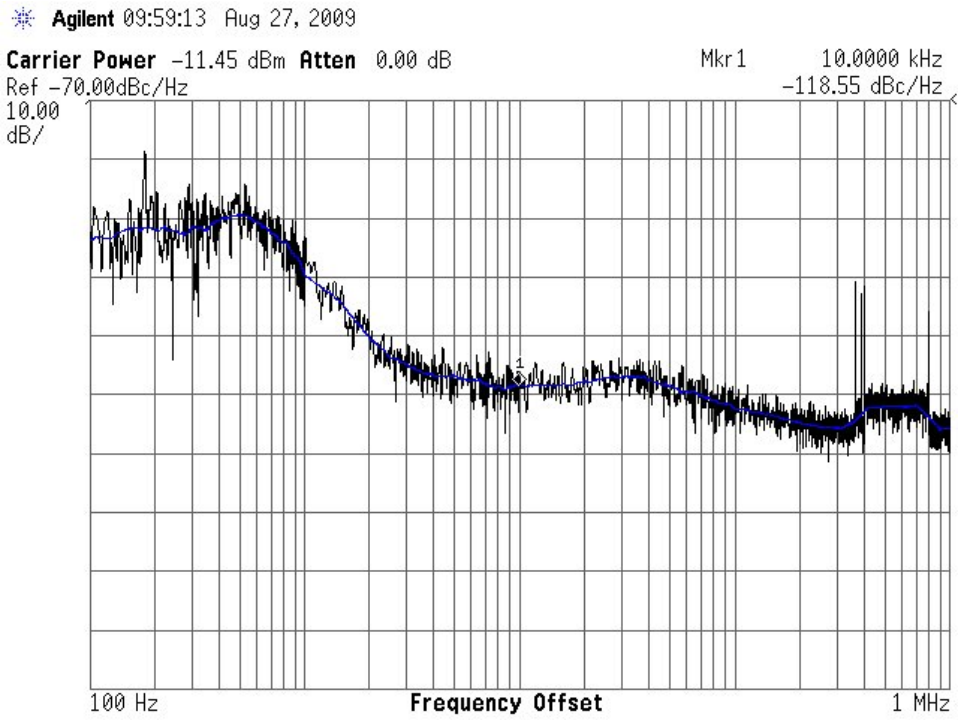


Figure 3.17: The measured DDS phase noise at an output frequency of 1.57 GHz with a 7.2 GHz clock input frequency. The input clock is generated from an Agilent E8257D analog signal generator. The graph illustrates a -118.55 dBc/Hz phase noise at a 10 kHz frequency offset.

From [25], the signal to noise and total harmonic distortion (SINAD) are used to calculate the ENOB as follows:

$$\text{ENOB} = \frac{\text{SINAD}_{dB} - 1.76}{6.02}. \tag{3.11}$$

SINAD is the ratio of the root-mean-square (RMS) value of the sine wave (reconstructed output of a DAC) to the RMS value of the noise plus the total harmonic distortion (THD) up to the Nyquist frequency, excluding the fundamental and the DC offset. SINAD is typically expressed in dB as

$$\text{SINAD} = \frac{S}{N + \text{THD}}, \tag{3.12}$$

where S and N are the RMS energy values of the signal and noise; THD is the total harmonic distortion defined as

$$\begin{aligned}\text{THD} &= \frac{P_{HD1} + P_{HD2} + \cdots}{P_{signal}} \\ &= \frac{\text{the biggest spur power}}{P_{signal}} \\ &+ \frac{\text{the sum of all other spurs' power except the biggist}}{P_{signal}} \\ &= \frac{1}{\text{SFDR}} \\ &+ \frac{\text{the sum of all other spurs' power except the biggist}}{P_{signal}}.\end{aligned} \tag{3.13}$$

P_{HD1}, P_{HD2}, $\cdots$ are the first and second harmonic distortion energy. P_{signal} is the fundamental tone or signal tone energy.

Table 3.1: Performance Comparison of Ultrahigh Speed DDS RFICs with over 8 GHz Maximum Clock Frequency

	[18]	[19]	[20]	[21]	[this work]
Technology	InP	InP	InP	SiGe	SiGe
f_T/f_{MAX} [GHz]	137/267	300/300	300/300	100/120	200/250
Phase resolution [bit]	8	8	8	9	11
Amplitude resolution [bit]	7	7	5	8	10
Maximum clock [GHz]	9.2	13	32	12.3	8.6
Nyquist band SFDR [dBc]	<30	26.67	21.56	**20**	**33**
Power consumption [W]	15	5.42	9.45	1.9	4.8
Die area [mm^2]	8×5	2.7×1.45	2.7×1.45	3×3	4×3.5
FOM [GHz·$2^{\text{SFDR}/6}$/W]	<16.0	42.6	34.8	65.3	**81.1**

Although the second items in Eq. (3.13) may be larger than the first item, the SFDR is easily obtained since it can be read directly from the spectrum analyzer. Herein, we use 1/SFDR to represent the THD. In general, the RMS value of the noise is far below the THD. As a result, the SFDR is used to represent SINAD to calculate the FOM, which can

be defined as

$$\begin{aligned} \text{FOM} &= \frac{\text{Max. Clock(GHz)} \times 2^{(\text{SFDR}_{\text{dB}}-1.76)/6.02}}{\text{Power(W)}} \\ &\approx \frac{\text{Max. Clock(GHz)} \times 2^{\text{SFDR}_{\text{dB}}/6}}{\text{Power(W)}}. \end{aligned} \tag{3.14}$$

$\text{SFDR}_{dB}/6$ represents the ENOB obtained from the SFDR measurement [26]. Although the SFDR is defined in the Nyquist band, the narrow band SFDR is often more important since wideband spurs can be removed relatively easily. It is only a specific narrow band near the output, which is usually less than 1% of the update frequency, which is of the interest of many applications.

Table 3.1 is a performance comparison of ultrahigh speed DDS RFICs with more than 8 GHz maximum clock frequency. Compared to the InP DDS RFICs, this SiGe DDS significantly improves the resolution, and it is the most complicated ultrahigh speed DDS design containing approximately twenty thousand transistors. Most of the InP DDS RFICs were measured using probe stations [18, 19, 20], while this DDS RFIC was packaged. As mentioned earlier, the package has a thermal resistance of approximately 30 °C/W, and at room ambient temperature, the junction temperature of the SiGe devices can theoretically reach as high as 180 °C. At such high temperature, the device performance is greatly degraded and the DAC current switches are no longer synchronized due to increased internal delays. When the device is effectively cooled, the DDS operates at a maximum clock frequency of 8.6 GHz. At room temperature, the packaged DDS operates at the maximum clock frequency of 7.2 GHz. When compared with the 9-bit 12.3 GHz DDS [21], this design achieves two more bits for both phase and amplitude. As a result, this DDS achieves a 10 dB larger SFDR.

3.4 Conclusion

This chapter presented an 11-bit 8.6 GHz SiGe DDS RFIC design with a 10-bit segmented sine-weighted DAC, implemented in 0.13 μm SiGe BiCMOS technology with f_T/f_{MAX}

of 200/250 GHz. With Nyquist output, the DDS achieves a maximum clock frequency of 8.6 GHz. The Power consumption of the DDS is approximately 4.8 W and the power efficiency FOM is 81.1 GHz·$2^{\mathrm{SFDR}/6}$/W. This DDS RFIC is the first ultrahigh speed DDS with 11-bit phase and 10-bit DAC amplitude resolutions that achieves a record high SFDR of 33 dBc with leading power efficiency.

Chapter 4

A 9-bit 2.9 GHz DDS RFIC with Direct Digital Modulations

4.1 Introduction

So far, no DDS with over-GHz output that have been developed provide desired modulation capabilities to be used in next generation radar and communication systems. [18, 19, 20, 27, 22, 21, 8]. To achieve an over-GHz output frequency, all existing DDS RFICs use pipeline accumulators that work only with a constant input FCW, and thus no FM can be performed [18, 19, 20, 27, 22, 21, 8]. To implement direct FM or PM, CLA or RCA must be used with the attendant penalty of reduced speed. Ref. [28] reported a 9-bit DDS with RCA accumulator. It has the capability of FM, but only at low frequency because the FCW cannot change too fast with the bipolar plus NMOS adder architecture, and no PM can be performed. The 9B DDS using CLA accumulator and adder to implement the direct digital modulation capabilities is presented in this chapter. And in next chapter, the 24B DDS using RCA accumulator and adder to implement the direct digital modulation capabilities is presented. This two DDS RFICs represent the first reported GHz range output DDSs with direct digital frequency and phase modulation capabilities.

4.2 Circuit Implementation

The 9B DDS adopts a ROM-less architecture which combines both the sine/cosine mapping and digital-to-analog conversion together in a sine-weighted digital-to-analog converter (DAC). The block diagram of the 9-bit 2.9 GHz ROM-less DDS is shown in Fig. 4.1. The major parts of the ROM-less DDS are a 9-bit CLA phase accumulator, a 9-bit CLA full adder and a 7-bit sine-weighted DAC. The 9-bit phase accumulator output modulates with

the 9-bit PCW and truncated to 8 bits. After phase modulation and truncation, the highest 8 bit output is fed into the sine-weighted DAC. The two MSBs of the residue are used to determine the quadrant of the sine wave. The MSB output of the phase accumulator is used to provide the proper mirroring of the sine waveform about the π phase point. The 2nd MSB is used to invert the remaining 6 bits for the 2nd and 4th quadrants of the sine wave by a 1's complementor, and the outputs of the complementor are applied to the sine-weighted DAC to form a quarter of the sine waveform. Because of the π phase point mirroring, the total amplitude resolution of the sine-weighted DAC is 7 bit.

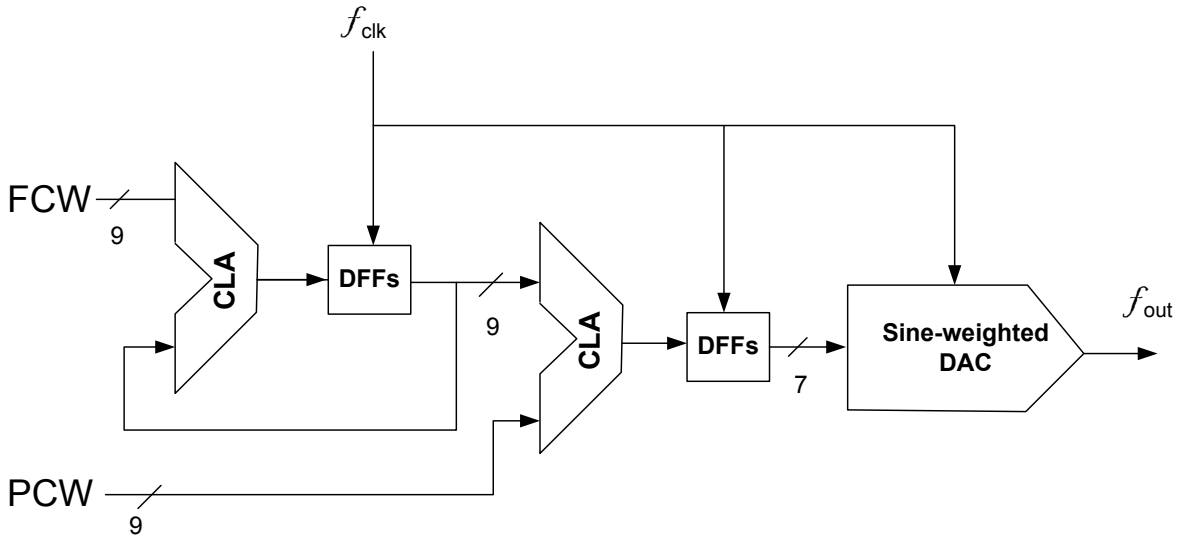


Figure 4.1: Block diagram of 9-bit ROM-less DDS.

4.2.1 9-bit Carry Look Ahead Adder/Accumulator

To perform a direct digital modulation, the adder must have no latency. Pipelined accumulator is not suitable because of its big latencies and can only handle a fixed FCW. In this design, CLA adder is used to implement the direct digital modulations due to its small delays beyond other zero latency architectures. A 9-bit CLA adder is used to implement the 9-bit accumulator. Fig. 4.2 shows the architecture of the 9-bit CLA adder. The output and carry out for each bit are calculated as

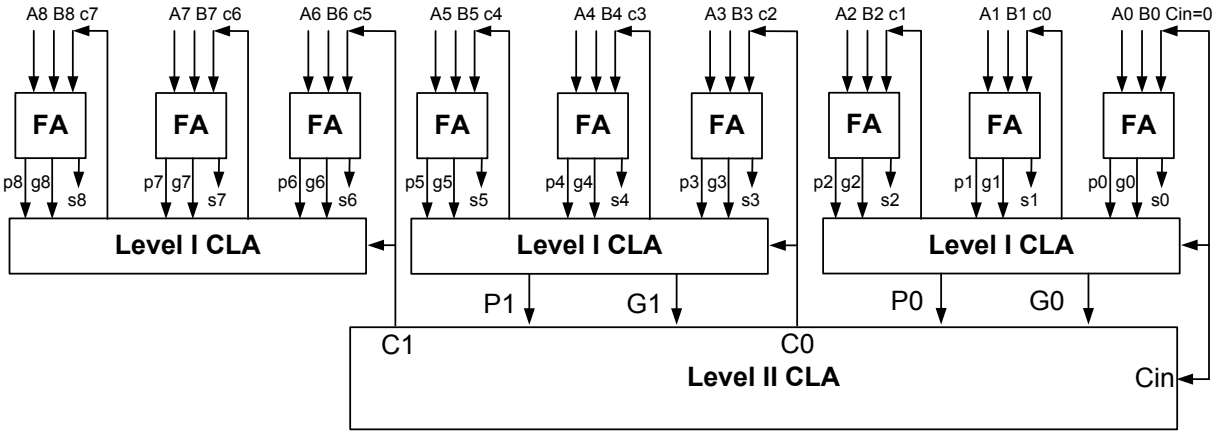


Figure 4.2: Block diagram of 9-bit CLA accumulator (full adder).

$$\begin{cases} \text{Carry out: } c_i = g_i + p_i \cdot c_{i-1} \\ \text{Sum: } s_i = pi \bigoplus c_{i-1} \end{cases} \tag{4.1}$$

where c_i is the carry out and c_{i-1} is the carry in or the carry out from the previous bit. g_i and p_i are the carry generate and carry propagate in level I CLA. The first level carry out can be obtained by

$$\begin{cases} c_0 = g_0 + p_0 \cdot C_{in} \\ c_1 = g_1 + p_1 \cdot g_0 + p_1 \cdot p_0 \cdot C_{in} \end{cases} \tag{4.2}$$

where

$$\begin{cases} \text{Carry generate: } g_i = A_i \cdot B_i \\ \text{Carry propagate: } p_i = A_i \bigoplus B_i \end{cases} \tag{4.3}$$

and the second level carry out can be obtained by

$$\begin{cases} C_0 = G_0 + P_0 \cdot C_{in} \\ C_1 = G_1 + P_1 \cdot G_0 + P_1 \cdot P_0 \cdot C_{in} \end{cases} \tag{4.4}$$

where second level propagates are obtained by

$$\begin{cases} P_0 = p_2 \cdot p_1 \cdot p_0 \\ P_1 = p_5 \cdot p_4 \cdot p_3 \end{cases} \tag{4.5}$$

and second generates are obtained by

$$\begin{cases} G_0 = g_2 + p_2 \cdot g_1 + p_2 \cdot p_1 \cdot g_0 \\ G_1 = g_5 + p_5 \cdot g_4 + p_5 \cdot p_4 \cdot g_3 \end{cases} \tag{4.6}$$

In the above equations, all the logics must be implemented within less than three inputs. This is selected to compromise with the power supply voltage and CML logics. Under a 3.3 V power supply and a SiGe HBT base-collector voltage of 0.85 V$\sim$0.9 V, all the digital logic is implemented using 3 level CML with differential output swings of 400 mV. Level shifters may be needed to shift between different voltage level inputs. The level shifter usually runs much faster than other CML gates. It can be ignored when counting the gate delays. Suppose XOR gate's delay is two times of the AND gate. The total delays can be calculated from the equations and diagram. (A) two gates delay to calculate level I carry generate g_i and propagate p_i in Eq. (4.3); (B) two gate delays to calculate level II carry generate G_i and propagate P_i in Eqs. (4.5) and (4.6); (C) two gate delays to calculate level II carry in Eq. (4.4); (D) two gate delays to calculate level I carry in Eq. (4.2); and (E) two gates delay to calculate sum and carry out from Eq. (4.1). Therefore the 9-bit CLA adder needs only 10 AND gates delay, which has a much less delay than the ripple carry adder's (2N-1) = 17 gate delays especially for high resolution adders (It is true without considering the wire delay. The effect of the wire delay will be discussed in Chapter 5), while it is much slower than the pipelined counterpart.

Table 4.1: Current Source Matrix in Sine-weighted DAC

2	3	3	3	3	3	3	3
3	3	3	3	3	3	3	3
3	3	3	2	3	3	3	2
3	2	3	2	3	2	2	3
2	2	2	2	2	2	2	2
1	2	2	1	2	1	1	2
1	1	1	1	1	1	1	0
1	0	1	0	1	0	0	0

4.2.2 7-bit Sine-weighted DAC

The structure of the sine-weighted DAC is shown in Fig. 4.3. Since the quadrant of the sine waveform was determined by the two MSBs, the left 6 bits are used to control the switch matrix and generate the amplitude for a quarter phase ($0 \sim \pi/2$) sine wave. The current source matrix is calculated by the below equations and shown in Table 4.1.

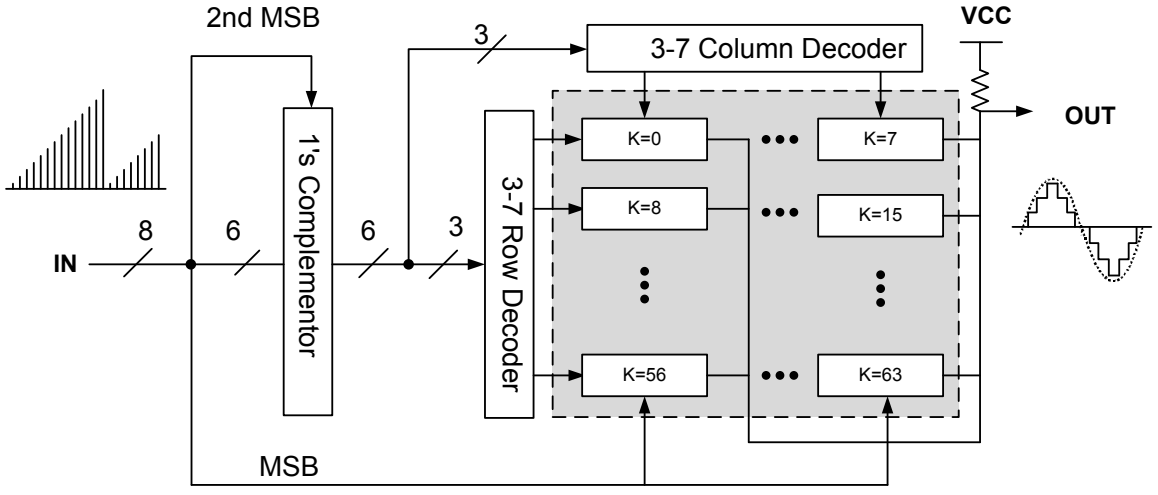


Figure 4.3: Block diagram of 7-bit sine-weighted DAC.

$$I_k = \begin{cases} \lfloor (2^9 - 1) \sin\left(\frac{\pi}{2} \cdot \frac{(0.5)}{2^6}\right) \rfloor, \text{for } k = 0 \\ \lfloor (2^9 - 1) \sin\left(\frac{\pi}{2} \cdot \frac{(k+0.5)}{2^6} - \sum_{n=0}^{k-1} I_n\right) \rfloor, \ 0 \leq k \leq 2^6 - 1 \end{cases} \tag{4.7}$$

The sine-weighted DAC current source matrix provides totally 128 unit current sources. The unit current of each current source is set as 105 μA. The largest current in the current source is 315 μA, which is composed of 3 unit current sources. The current switch contains two differential pairs with cascode current sources for better isolation and current mirror accuracy. The current outputs are converted to differential voltages by a pair of off-chip 15 Ω pull-up resistors. Fig. 4.4 shows that the currents from the cascode current sources are fed to outputs $\mathrm{OUT_p}$ and $\mathrm{OUT_m}$ by pairs of switches ($\mathrm{M_{sw}}$). The MSB controls the selection between different half periods. The current switch contains two differential pairs with minimum size transistors and a cascode transistor to isolate the current sources from the switches, which improves the bandwidth of the switching circuits. For the layout, vertical devices SiGe HBTs are used with a degeneration resistor to improve the current source matching. All the current source transistors are randomly distributed in the current source matrix. Two dummy rows and columns have been added around the current source array to avoid edge effects. In order to minimize the phase difference of the clock to the flip-flops, an H-tree clock scheme is used to make the clock signal reach each block simultaneously in both the adder/accumulator and DAC.

4.3 Experimental Results

Figs. 4.5-4.7 illustrate the measured DDS output spectra and waveforms for different output and clock frequencies without modulations. Fig. 4.5 presents a 509 MHz DDS output with a 2.5 GHz clock input, with the FCW equals to 104. The measured output power is approximately 0 dBm and the measured narrow band SFDR is approximately 48 dBc. Fig. 4.6 gives the measured DDS output spectrum with 1.444 GHz Nyquist output under

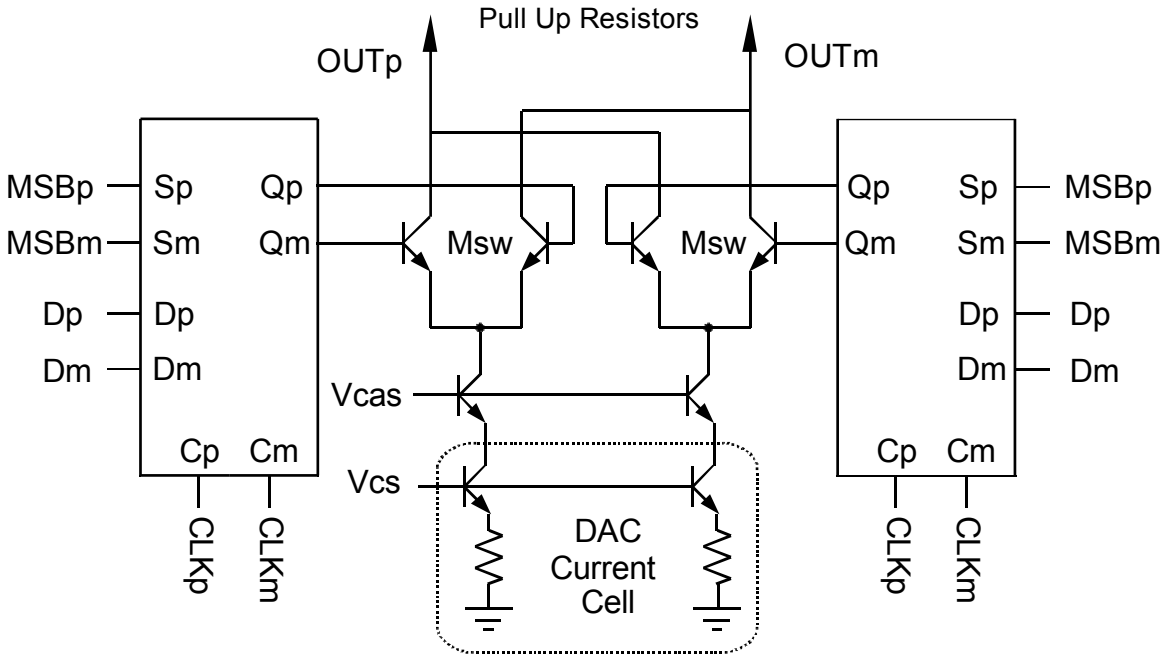


Figure 4.4: Diagram of DAC switch and current source matrix cell.

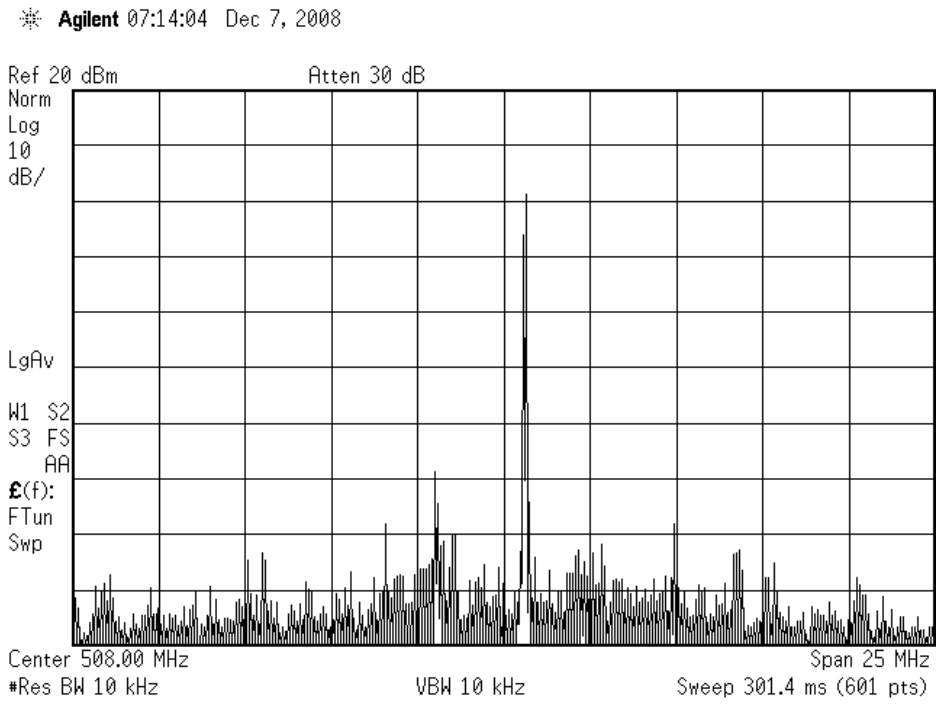


Figure 4.5: Measured DDS output spectrum with 509 MHz output under 2.5 GHz clock (FCW=104), showing about 48dBc narrow band SFDR.

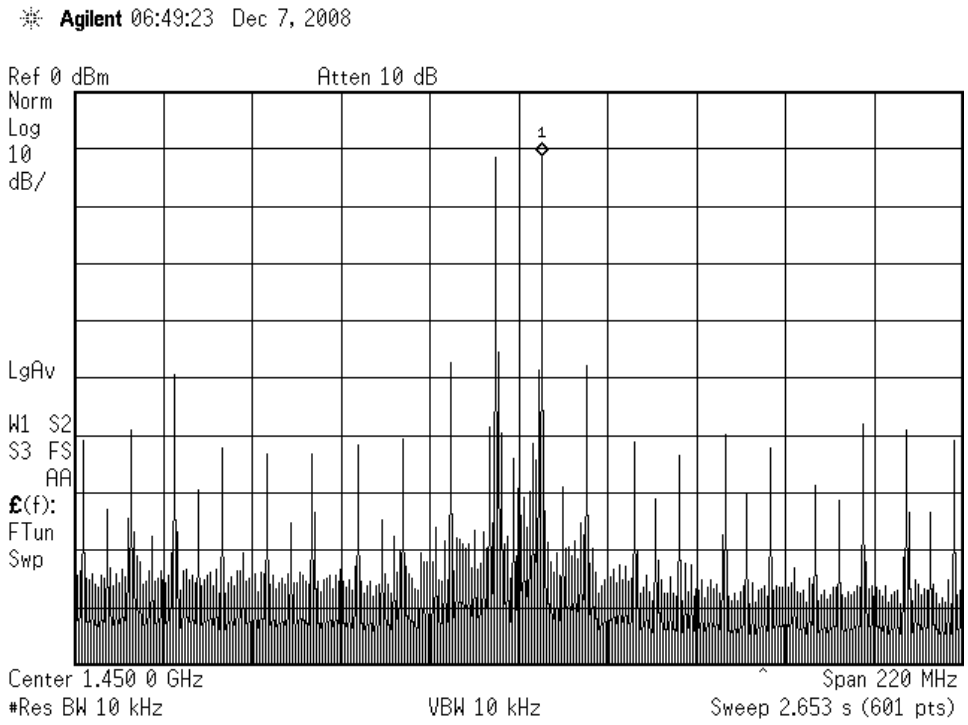


Figure 4.6: Measured DDS output spectrum with 1.444 GHz output and 2.9 GHz clock (FCW = 255), showing about 35dBc narrow band SFDR. The image tone is located at 1.455 GHz.

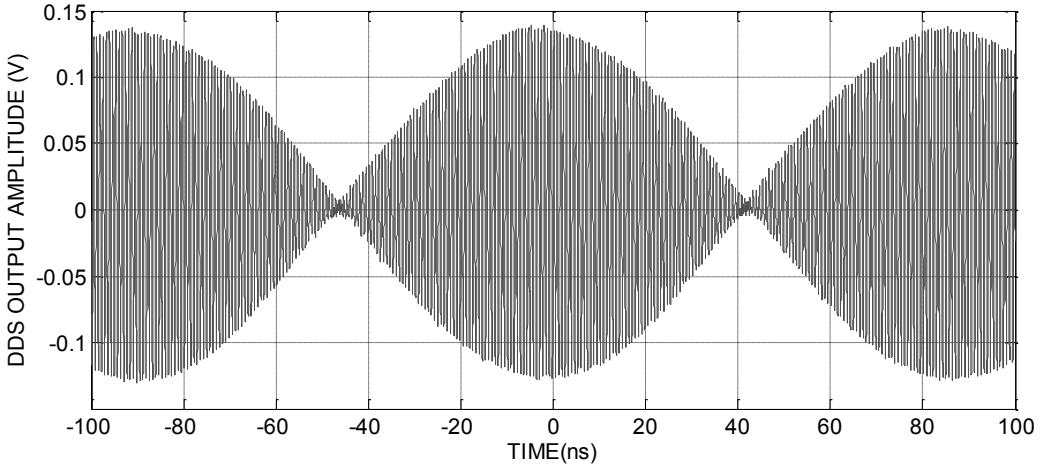


Figure 4.7: Measured DDS output waveform with 1.444 GHz output and 2.9 GHz clock (FCW=255). The envelope frequency is 12 MHz

2.9 GHz clock. Since FCW = 2^8-1 = 255, the output frequency is

$$\frac{\text{FCW}}{2^N} \times f_{clk} = \frac{255}{2^9} \times 2.9 \text{ GHz} = 1.444 \text{ GHz}$$

The first order image tone mixed by the clock frequency and the DDS output frequency occurs at

$$2.9 \text{ GHz} - 1.444 \text{ GHz} = 1.456 \text{ GHz}$$

Fig. 4.7 shows the time domain waveform of Fig. 4.6. The envelope frequency of the waveform is

$$\frac{2^{9+1}}{2^9} \times f_{clk} - \frac{2^{9-1}}{2^9} \times f_{clk} \approx 12 \text{ MHz}$$

Fig. 4.8 shows the measured DDS output with FCW = 2 frequency modulated by a step of ΔFCW = 1. The frequency before the step is 9.375 MHz with FCW = 2 and after the step is 14.0625 MHz with FCW = 3. Fig. 4.9 shows the measured DDS output with FCW = 2 phase modulated by a step of ΔPCW=256 with respect to 180° phase shift. The output frequency is 10 MHz with a 2.5GHz clock.

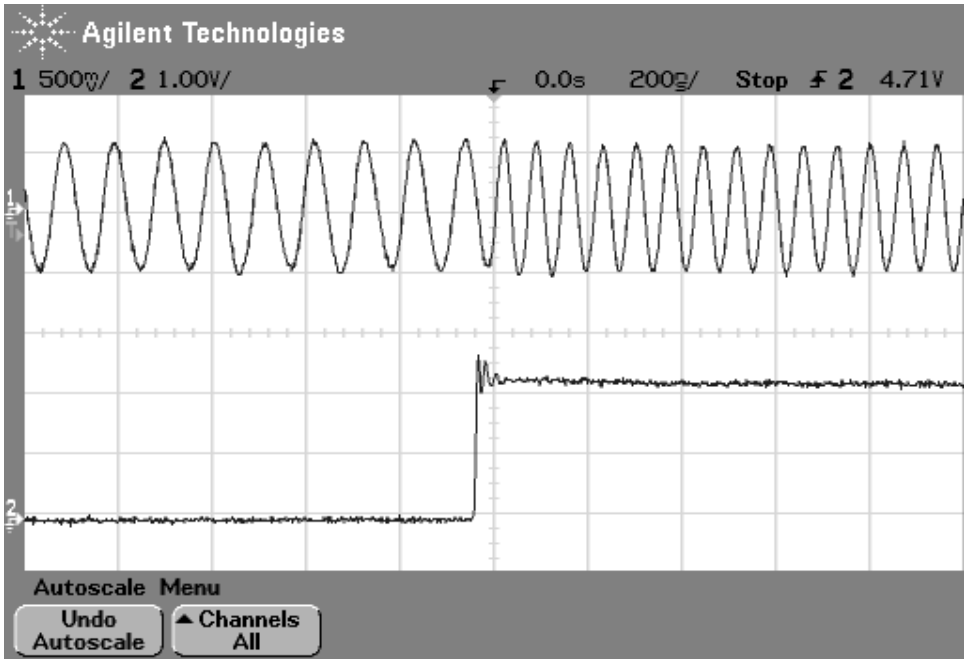


Figure 4.8: Measured DDS output with FCW = 2 frequency modulated by a frequency step of ΔFCW = 1. The frequency before the step is 9.375 MHz with FCW = 2, after the step is 14.062 MHz with FCW=3.

All measurements were done in CLCC-44 packaged parts without deglitch filter or calibrating the losses of the cables and PCB tracks.

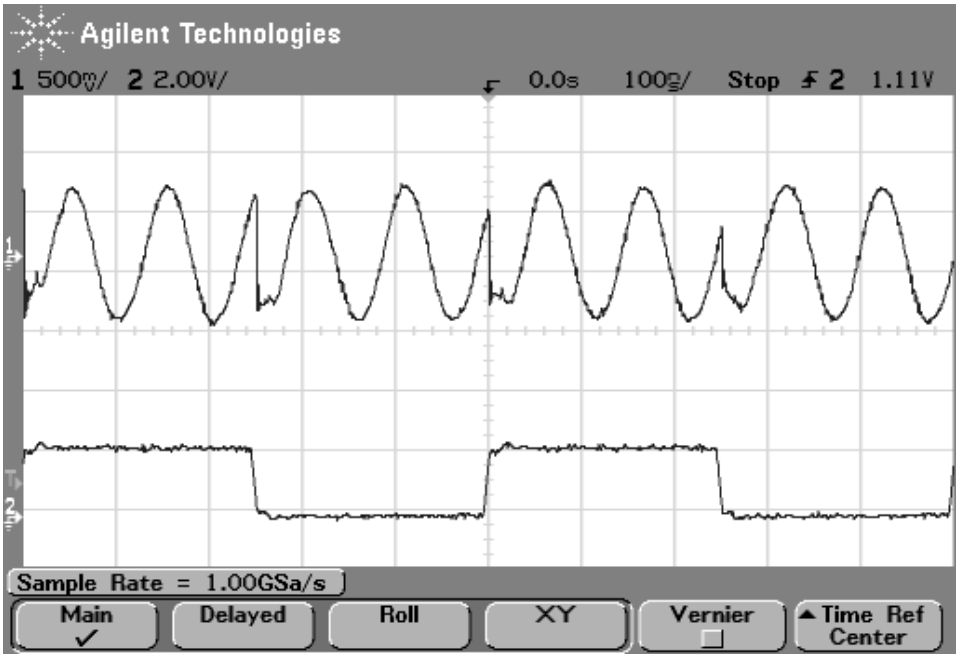


Figure 4.9: Measured DDS output with FCW = 2 phase modulated by a phase step of ΔPCW = 256 with respect to 180° phase shift. The output frequency is 10 MHz with a 2.5 GHz clock.

Table 4.2 compares mm-wave DDS RFIC performances. Although this DDS have a relatively low frequency than others, it is the first DDS with direct digital frequency and phase modulation capabilities and has more than GHz output frequency. Some commercial parts have the FM and PM capabilities, but all the parts work no more than 1 GHz and can only output less than 500 MHz frequency. The die photo of the SiGe DDS RFIC is shown in Fig. 4.10. This DDS design is quite compact with an active area of 1.7×2.0 mm^2 and a total die area of 2.5×3.0 mm^2.

4.4 Conclusion

Implemented in a 0.13 μm SiGe BiCMOS technology with f_T/f_{max} of 200/250 GHz, this chapter presented a 9-bit 2.9 GHz SiGe DDS RFIC design with direct digital 9-bit frequency and 9-bit phase modulations. With Nyquist output, the DDS achieves a maximum clock frequency of 2.9 GHz, and a narrow band SFDR of 35 dBc. It has low power consumption as well. The power consumption is approximately 2.0 W under a single 3.3 V power supply

Table 4.2: Selected Ultrahigh Speed DDS RFIC Performance Comparison

	[18]	[19]	[20]	[22]	[8]	[9B DDS]
Technology	InP	InP	InP	SiGe	SiGe	SiGe
f_T/f_{max} [GHz]	137/267	300/300	300/300	100/120	200/250	200/250
Phase [bit]	8	8	8	9	11	9
Amplitude [bit]	7	7	5	8	10	7
FM [bit]	None	None	None	None	None	9
PM [bit]	None	None	None	None	None	9
Max clock [GHz]	9.2	13	32	9.6	8.6	2.9
SFDR [dBc]	30	26.67	21.56	30	40	35
Power [W]	15	5.42	9.45	1.9	4.8	2.0
Area [mm^2]	8.0 × 5.0	2.7 × 1.45	2.7 × 1.45	3.0 × 3.0	4.0 × 3.5	2.5 × 3.0

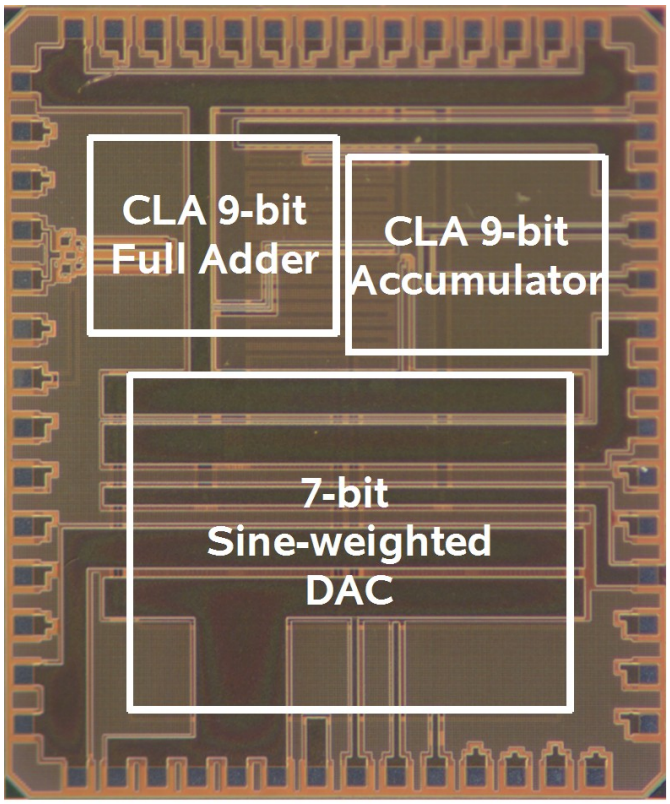


Figure 4.10: Die photo of the 9-bit DDS with direct digital modulations.

even with added modulation blocks. This DDS RFIC is the first reported GHz range output DDS with direct digital frequency and phase modulation capabilities.

Chapter 5

A 24-bit 5.0 GHz DDS RFIC with Direct Digital Modulations

5.1 Introduction

This chapter presents a 24-bit 5.0 GHz DDS with over-GHz output frequency and direct digital modulation capabilities. This work represents one of the first DDS RFIC with over-GHz range output as well as direct digital FM and PM capabilities. The 24B DDS is implemented with direct digital FM and PM capabilities using RCA adders. The block diagram of the 24-bit 5.0 GHz ROM-less DDS with RCA accumulator and modulator is shown in Fig. 5.1 [2, 29]. The major parts of the ROM-less DDS are a 24-bit RCA phase accumulator, a 12-bit RCA modulator, and a 10-bit sine-weighted DAC. The 24-bit RCA phase accumulator output is truncated to 12 bits and modulated with a 12-bit PCW. After PM, the output is truncated again, and the highest 11 bits are fed into the sine-weighted DAC. The sine-weighted DAC maps the 11-bit linear phase word to the digital amplitude and generates the analog waveform. The ultrahigh speed RCA accumulator/adder and sine-weighted DAC will be described in the following two sections, respectively.

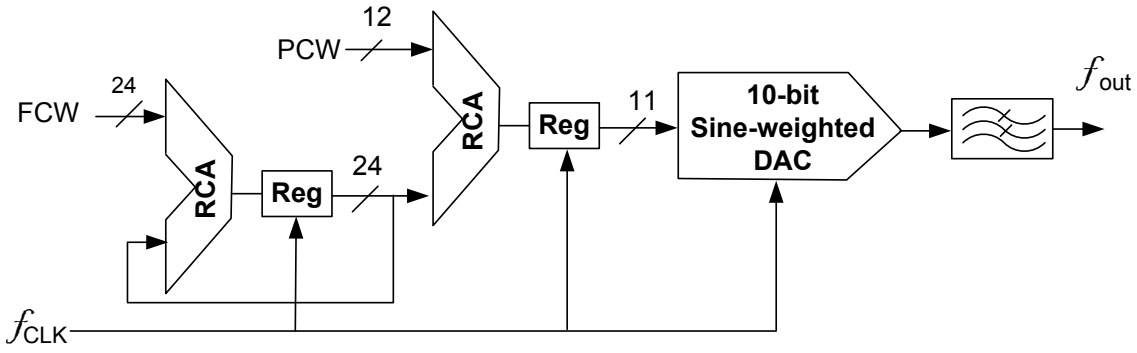


Figure 5.1: Block diagram of the 24-bit 5.0 GHz DDS RFIC.

5.2 Ultrahigh Speed Adder Design

5.2.1 Wire Delay in the 0.13 μm SiGe BiCMOS Technology

With the introduction of deep submicron semiconductor technology, the parasitic effects introduced by the wire delay begin to dominate the performance of high speed digital integrated circuits. The typical buffer delay in the 0.13 μm SiGe BiCMOS technology is less than 4 ps while the wire delay of a 2 μm wide and 100 μm long wire can be as high as 10 ps. From [30], the transmission line effects should be considered when the rise or fall time of the input signal is smaller than the time of flight of the transmission line. The following equation is used to determine when transmission line effects should be considered.

$$t_{rf} \leq 2.5 t_{flight} = 2.5 \frac{L}{v} \tag{5.1}$$

In Eq. (5.1), t_{rf} is the rise and the fall time of the signal transmitted through the wire. t_{flight} is the flight time, which is the time it takes for the wave to propagate from one end of the wire to the other, and is 15 cm/ns in silicon oxide (SiO_2). So the minimum length that must be considered as a transmission line for a signal is

$$L_{min} = 0.4 \; t_{rf} \cdot v. \tag{5.2}$$

For a 5.0 GHz signal the rise and fall time should not be longer than 67 ps. If the wire length is less than 4 mm, a lumped RC model can be used to evaluate the propagation delay through the wire. Fig. 5.2 shows the equivalent circuit of a wire with length L. From the Elmore delay rule, the dominant time constant is

$$\tau_D = R_s c L + 0.5 r c L^2, \tag{5.3}$$

where R_s is the internal resistance of the driver, and r and c are the unit length parasitic resistance and capacitance of the wire. The delay introduced by the wire resistance becomes dominant when the second term is bigger than first, i.e. when $L \geq 2R_s/r$. In the 0.13 μm SiGe BiCMOS technology, the first term in Eq. (5.3) will dominate the propagation delay, as long as L <2 mm, and as a result the propagation delay of the wire is approximately proportional to the length.

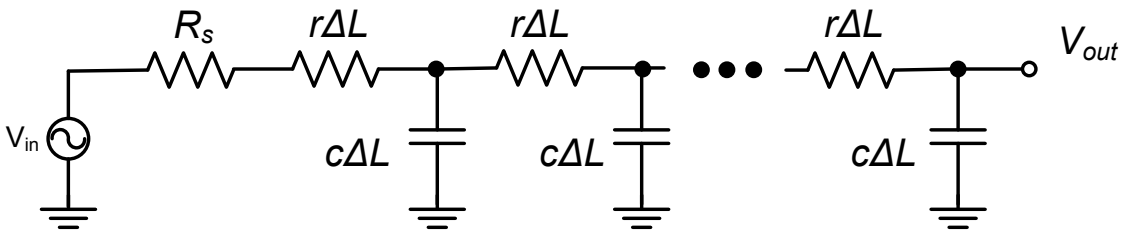


Figure 5.2: Lumped RC model for a wire with length of L.

To evaluate wire delay effects in high speed digital logic design, several simulations have been performed in a 0.13 μm SiGe process for a current-mode-logic (CML) cell implemented using a differential pair without an emitter follower as the output buffer and its connection wires. Fig. 5.3 shows the test bench used to simulate the wire delay effects. Fig. 5.3(A) is the schematic view. It is used to find the intrinsic propagation delay of the CML buffer that is 2 μm wide and 100 μm long. Differential wires with the third metal layer are inserted between the two buffers in Fig. 5.3(B). The space between the two differential wires is typically maintained at 2 μm in the layout. Fig. 5.3(C) uses the same test bench as that employed in Fig. 5.3(B), with the exception of an additional piece of metal under the differential wires. Fig. 5.3(D) uses the same test bench as that in Fig. 5.3(B), except in this case two pieces of metal are used to sandwiched the differential wires. Clearly, cases Fig. 5.3(C) and (D) result in a larger parasitic capacitance than Fig. 5.3(B). However, it is not always possible to place the wire without any overlap with the metals that are under and above the wires, especially for modern processes with more than 5 layer metal connections. The simulated results are plotted in Fig. 5.4. In Fig. 5.4, plot (A) represents the propagation delay of

Fig. 5.3(A), and illustrates the propagation delay of only the input and output buffers. It does not include the wire delay so it is constant along the wire length. Plots (B), (C) and (D) show the propagation delay of test bench (B), (C) and (D) but does not include the buffer delays in the test benches. These three plots reflect the third metal wire propagation delay in a 0.13 μm SiGe process. It is proportional to the wire length as long as the length is less than 2 mm. Comparing (B), (C) and (D), the wire delay with shielded metal is two (for (C)) or three (for (D)) times larger than an unshielded metal wire. This conclusion, as well as the linear relationship between the wire delay and the wire length, indicates that the wire delay is dominated by the time constant of the product of parasitic capacitance and the input buffer output impedance, as described by the first term of Eq. (5.3). Note that test benches (C) and (D) are more practical cases than (B), because in a real layout environment all the wires overlap each other and produce several times more parasitic capacitance than the coupling capacitance with the substrate. From the wire delay plot of Fig. 5.4, the wire delay coefficient (delay for 1 μm wire) for case (C) is about 0.10 ps/μm. This number will be used to estimate the adder delay in the following sections.

5.2.2 Propogation Delay Comparison Between the CLA and RCA Accumulator/Adder

A pipeline accumulator can only handle a fixed input FCW. Direct modulations such as LFM require a varying input FCW. Thus, either RCA or CLA adders must be used to implement direct modulations. Chapter 4 has calculated a 9-bit CLA adder delay for the critical path with 3-input CML implementations. However, the calculation did not count the level shifters that are used to shift between different input voltage levels, as well as the wire delays. In general, level shifters usually run much faster than CML gates, and thus can be ignored when counting the gate delays. Furthermore, the XOR gate delay is treated the same as the AND gate delay since CML gate delays are essentially identical for different gates. For example, both the carry and sum logic in a full adder can be implemented by

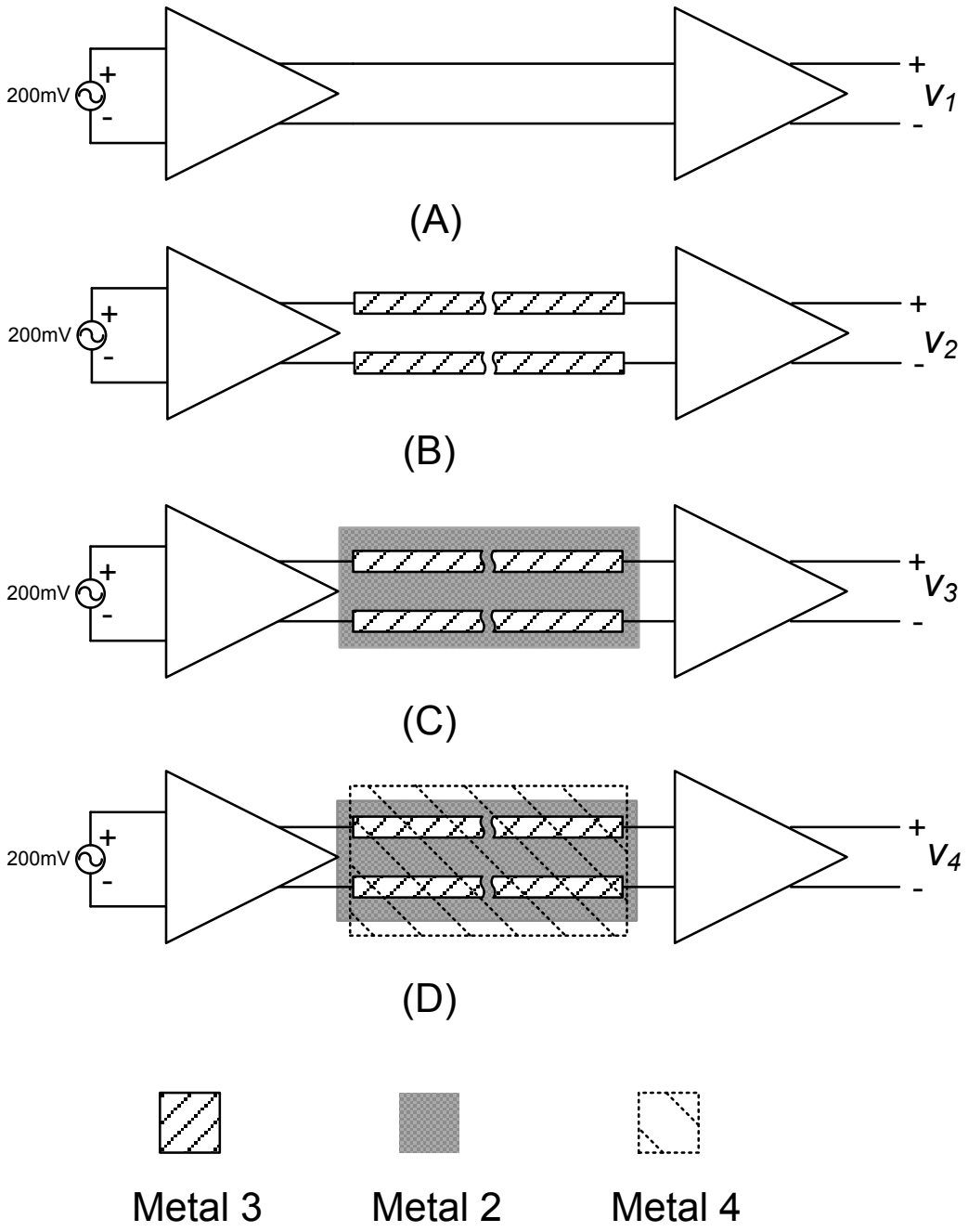


Figure 5.3: Test bench to simulate the wire propagation delay.

only one current tail CML gate. Given this information, the 9-bit CLA adder has a total of 8 CML gate delays. One CML gate delay is about 9 ps in the 0.13 μm SiGe BiCMOS technology. In the 9-bit full adder, the total logic delay is approximately 72 ps without the wire delay. From Fig. 4.2 in Chapter 4 and the actual layout, the wire delay in the critical

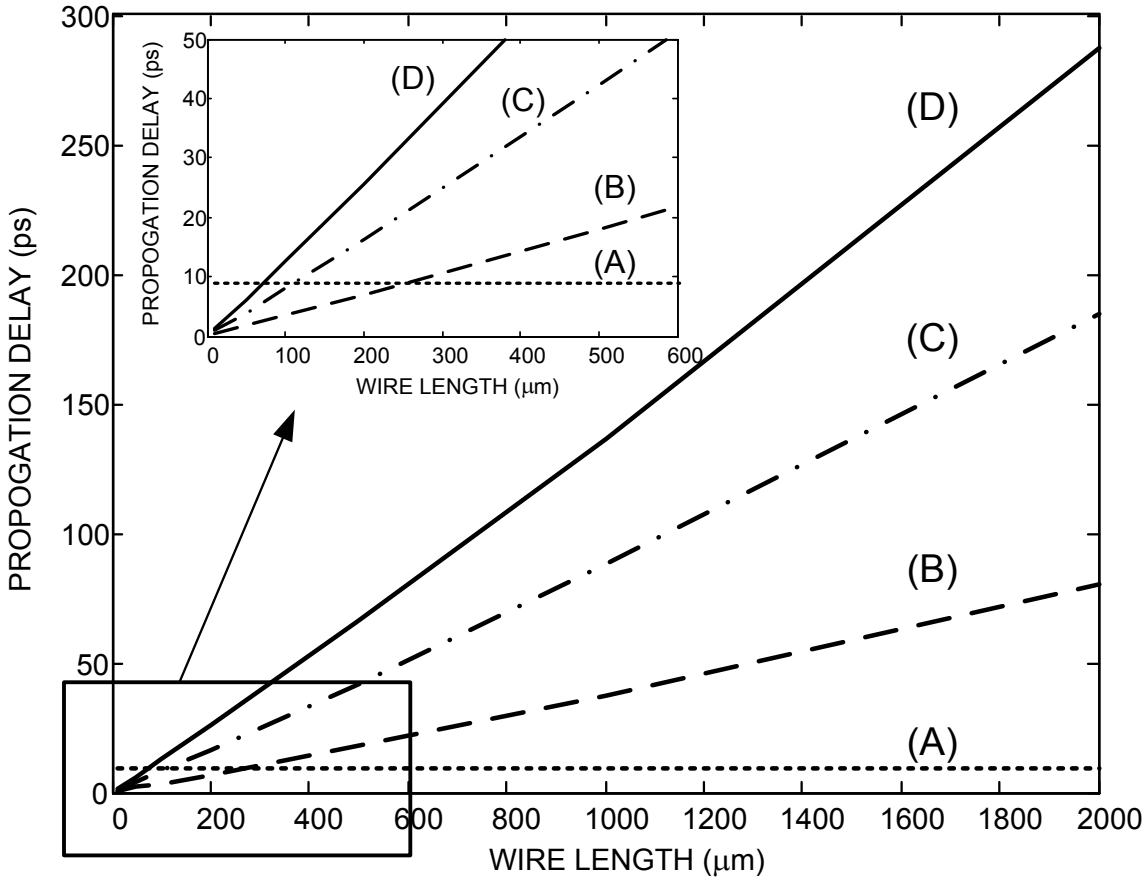


Figure 5.4: Simulated wire propagation delay versus length.

path of the 9-bit CLA adder is calculated as follows: (A) A 200 μm wire is added to calculate the delay of level I generate g_i and propagate p_i; (B) A 200 μm wire is added to calculate the delay of level II generate G_i and propagate P_i; (C) A 300 μm wire is added to calculate the delay of the level II carry; (D) A 200 μm wire is added to calculate the delay of level I carry; (E) A 200 μm wire delay is added to calculate the delay of the sum and carry-out. Therefore, the total wire length to calculate the delay of the critical path is 1100 μm. If the bit number of the adder is higher than 9-bit and less than 27-bit, level III CLA block is needed to calculate the carry-out. To generate the third level CLA logic and the carry-in signal for the second level CLA block, the total gate delay increases to 12 CML gate and the total wire length increases to 1800 μm. The worst-case delay from a 10-bit CLA adder to 27-bit CLA adder remains the same since these adders have an identical critical path.

The calculation of propagation delay for the RCA is much easier than the CLA adder. Fig. 5.5 shows the architecture of an N-bit RCA. It represents the layout floor plan and the component placement as well as the schematic wire connection. The output and carry-out for each bit are calculated as

$$\begin{cases} \text{Carry out: } c_i = A_i B_i + B_i c_{i-1} + c_{i-1} A_i \\ \text{Sum: } s_i = A_i \bigoplus B_i \bigoplus c_{i-1}, \end{cases} \tag{5.4}$$

where A_i and B_i are the input of the N-bit full adder, i = 0, 1, $\cdots$, (N-1). c_i is the carry-out of the ith-bit full adder. $c_{-1} = C_{in} = 0$ is the initial carry-in of the N-bit full adder. $C_{out} = c_{N-1}$ is the last bit carry-out of the N-bit full adder. Therefore, the worst-case propagation delay of the N-bit full adder is the delay of N-1 carry logic gates and one sum logic gate. There is almost no wire delay since the carry logic can be placed as close as possible to minimize the amount of wire in the connection. The level shifter delay can be eliminated as well because the input voltage level can be intentionally removed from the critical path.

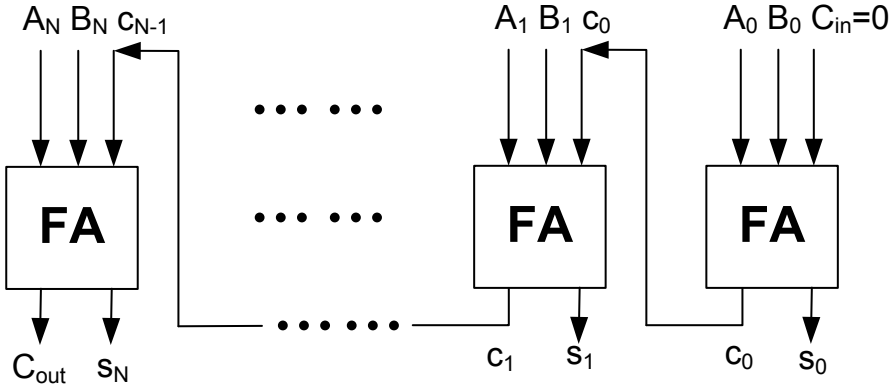


Figure 5.5: Diagram of N-bit RCA.

Fig. 5.6 shows the comparison of the estimated propagation delay of the CLA adder and RCA. Not counting the wire delay, the speed of the CLA adder is close to that of the RCA for small numbers of bits. At high numbers of bits, the CLA adder runs much faster than

the RCA. With the added wire delay, the RCA delay does not change too much because the RCA is very compact and can be layed out very closely, thus having almost no wire delays. However the layout of the CLA is very complex and introduces significant wire delay. So the CLA adder runs much slower than the RCA especially for 10-bit to 25-bit adders. In addition to the internal wire delays of the CLA adder, the CLA adder layout area is several times larger than the RCA adder, which results in more wire delays for global wiring.

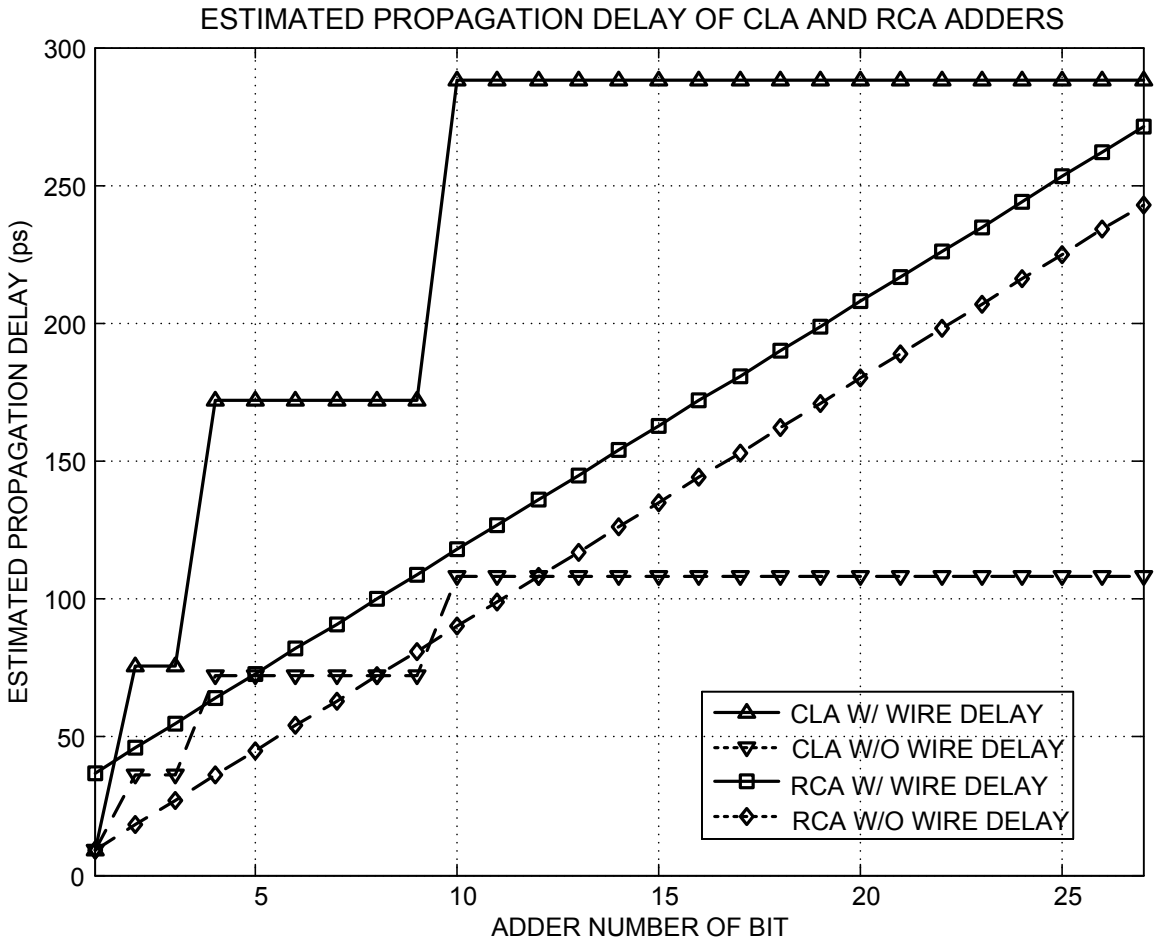


Figure 5.6: Estimated adder propagation delays with number of bits.

In conclusion, at the low or medium speed with an older and slower fabrication technology, the CLA speeds up the adder operation by using additional logic for carry calculations. However, for high speed implementation with fast technology (e.g., <0.13 μm), adder delay is mainly dominated by the wire delays. When compared to a CLA adder, the RCA adder

has a simple ripple architecture, which can be layed out in cascaded format one bit after another, leading to very compact layout with short wire interconnections between stages.

5.2.3 Circuit Implementation of the 24-bit 5.0 GHz RCA

In this DDS design, a 24-bit RCA is used to implement the 24-bit accumulator. The 24-bit RCA is composed of 24 1-bit full adders carefully designed in a compact manner. The output of the carry-out logic remains at the top CML level, and no level shifter is needed to convert the signal level for the critical path. Therefore the longest delay from input to output of the 24-bit RCA is 23 carry-out CML delays and 1 sum CML gate delay. The wire delay in the RCA can be minimized since the carry-in can be directly connected to the carry-out of the previous bit, leading to a compact layout in a cascaded format. Another 12-bit RCA was implemented for the 12-bit phase modulator. In addition, the 24-bit CLA adder runs slower than the RCA adder as shown in Fig. 5.6. When the 0.13 μm SiGe BiCMOS technology is used, long wires contribute much more delay than the logic gates. So a 24-bit CLA adder cannot run as fast as the RCA adder, not only because of the amount of cascade CLA logic with the attendant limited CML fan-in numbers but also because of the much longer wire delays needed by CLA logic. The wire delay in the RCA adder can be minimized since the carry-in can be directly connected to the carry-out of the previous bit, leading to a compact layout in a cascaded format.

5.3 10-Bit Segmented Sine-weighted DAC

5.3.1 Architecture of the 10-bit Sine-weighted DAC

The structure of the 10-bit sine-weighted DAC is shown in Fig. 5.7. The total phase word input for the sine-weighted DAC is 11 bits. The two MSB are used to determine the quadrants of the sine wave. The MSB output of the phase word is used to provide the proper mirroring of the sine waveform about the π phase point. The 2nd MSB is used to invert the remaining 9 bits for the 2nd and 4th quadrants of the sine wave by a 1's complementor, and

the outputs of the complementor are applied to a 9-bit sine-weighted DAC core to form a quarter of the sine waveform. Because of this π phase point mirroring, the total amplitude resolution of the sine-weighted DAC is 10 bits.

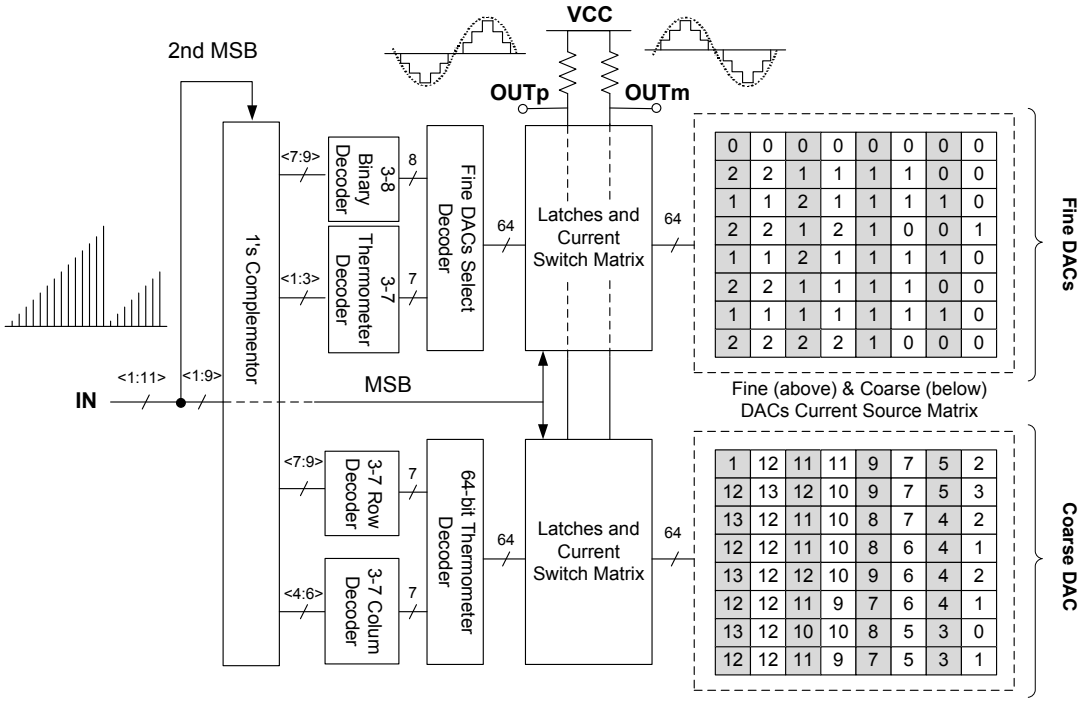


Figure 5.7: Block diagram of the 10-bit segmented sine-weighted DAC.

To reduce the complexity of the sine-weighted DAC, segmentation has been employed [8, 9]. The 9-bit sine-weighted DAC core is divided into a 6-bit thermometer-decoded coarse sine-weighted DAC and eight 3-bit thermometer-decoded fine sine-weighted DACs. The first 6 bits of the complementor's output control the coarse DAC and the highest 3 bits also address the selection of the fine DACs. The lowest 3 bits of the complementor's output determines the output value of each fine DAC. The bit division between the 6-bit coarse DAC and the 3-bit fine DACs is based on the trade-off of static and dynamic accuracies, chip area and power consumption. As shown in Fig. 5.7, the bottom current source array implements the coarse DAC. The coarse DAC current source array provides 512 unit current sources. The top current source array implements the fine DACs. Each column of the fine DAC current source array forms the current sources of one fine DAC. Every fine DAC has

about 8 unit current sources used to interpolate the coarse DAC. The unit current of both the coarse and fine DACs is set at 26 μA. The largest current in the current source matrix is 338 μA, which is composed of 13 unit current sources. In the layout, with consideration for current source matching, each current source is split into four identical current sources which carry a quarter of the whole current. To further improve their matching, all current source transistors, including those used in both the coarse and fine DACs, are randomly distributed in the whole current source matrix.

The current switch contains two differential pairs and improves the bandwidth of the switching operation with minimum logic transistors and cascode current sources that provide better isolation and current mirror accuracy. The current outputs are converted to differential voltages by a pair of off-chip 15 Ω pull-up resistors. Fig. 5.8 shows that the currents from the cascode current sources are fed to outputs OUTp and OUTm by pairs of switches (Msw). The MSB controls the selection between different half periods.

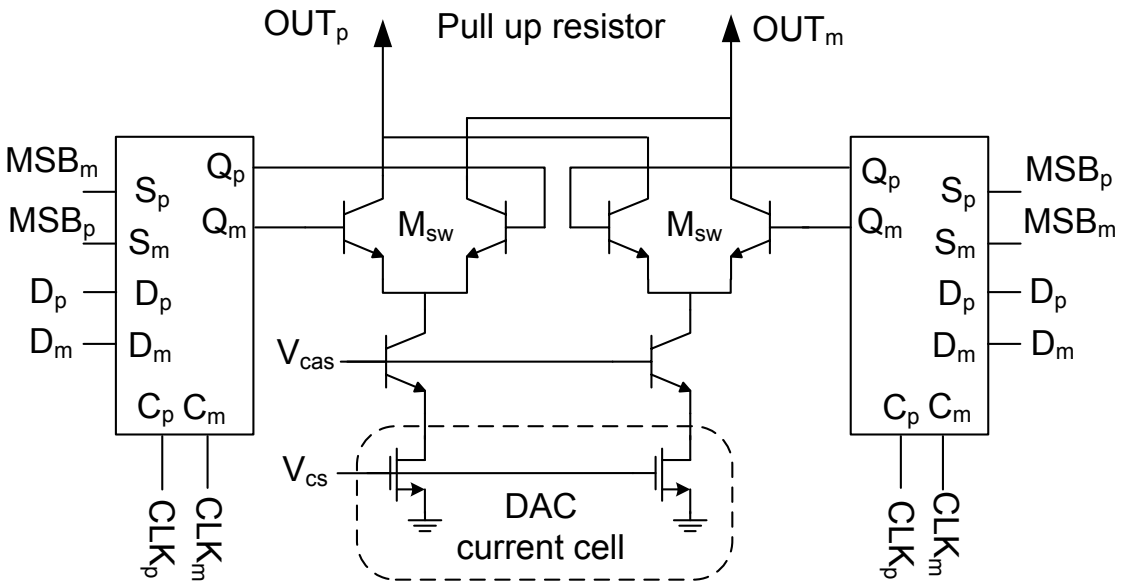


Figure 5.8: Diagram of the DAC switch and current source matrix cell.

5.3.2 Bandwidth Limitation of the DAC Switch Output Impedance

The dynamic performance of the current-steering DAC is closely related to the current switch output impedance as well as the frequency response of the output impedance. With a full thermometer decoded DAC, the SFDR can be written as the function of the output impedance Z_{out} and the DAC's number of bit resolution N [23].

$$SFDR = 20\log\left(\frac{Z_{out}}{R_L}\right) - 6.02(N-2), \tag{5.5}$$

where R_L is the load resistance of the current switch. The core switch cell of the sine-weighted DAC is shown in Fig. 5.9(A). C_0 and C_1 denote the parasitic capacitance at the drain of the current source transistor and the collector of the cascade transistor, including the device parasitic capacitance and the wire capacitance. The small signal equivalent circuit is drawn in Fig. 5.9(B). If r_π is neglected, the total output impedance looking through the switch output is given by

$$Z_{out} = g_{msw}r_{osw} \cdot \left(\frac{1}{sC_1} // \left(g_{mcas}r_{ocas} \cdot \left(\frac{1}{sC_0} // r_{ocs}\right)\right)\right). \tag{5.6}$$

In Eq. (5.6), g_{msw} and g_{mcas} denote the transconductance of the switch and the cascode transistor, respectively. r_{osw}, r_{ocas} and r_{ocs} denote the output resistance of the the switch, the cascode and the current source transistor, respectively. At low frequency, the output impedance can be simplified as

$$Z_{out} = g_{msw}r_{osw} \cdot (g_{mcas}r_{ocas}) \cdot r_{ocs}. \tag{5.7}$$

$g_{mcas}r_{ocas}$ is the maximum gain of the cascode transistor. The bipolar transistor is chosen since it has higher maximum gain than the MOS counterpart, while an MOS transistor is chosen for the current source because it has higher output resistance than the bipolar transistor as well as a lower overdrive voltage.

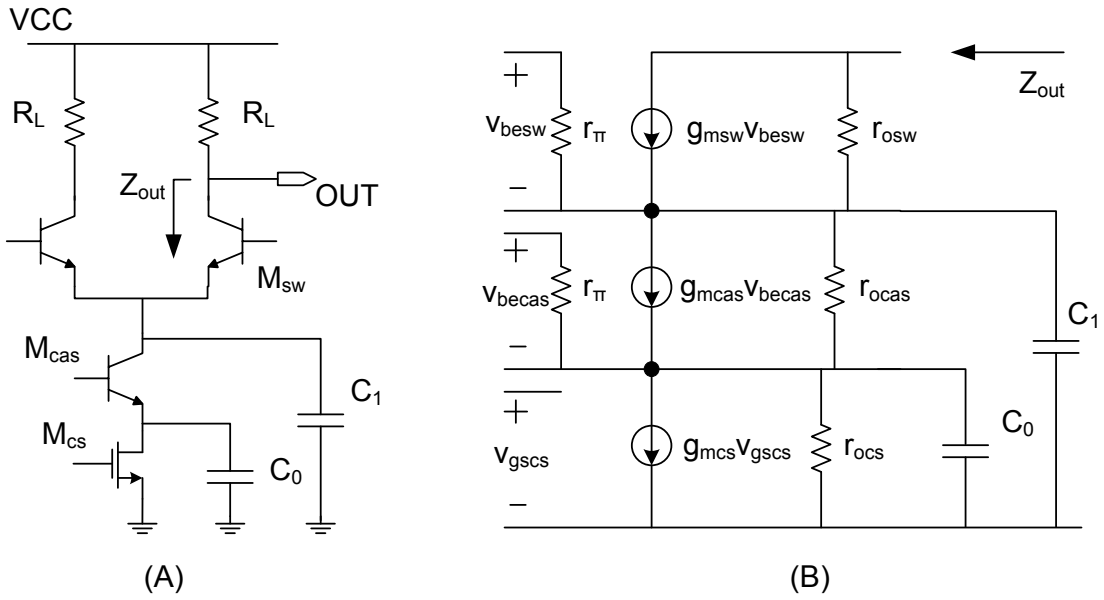


Figure 5.9: DAC switch core circuit and its small signal equivalent circuit.

From Eq. (5.6), the dominant pole of the output impedance is

$$\omega_p = -\frac{1}{r_{ocs}(C_0 + r_{ocas} g_{mcas} C_1)}. \tag{5.8}$$

To increase the bandwidth of the output impedance, the parasitic capacitances C_0 and C_1 must keep as small as possible. Because the maximum gain of the cascode transistor gmcasrocas is much larger than 1, the parasitic capacitance C_1 affects the bandwidth of the output impedance much more significant than C_0. So the long wire connection between the current source and current switch is used in the drain of the current source transistor. It results in a much larger capacitance C_0 than C_1.

5.4 Experimental Results

Figs. 5.10 and 5.11 illustrate the measured DDS output spectra and waveforms for different outputs and clock frequencies. All measurements were done in single output and using CLCC-68 packaged parts without calibrating the losses of the cables and PCB tracks.

Fig. 5.10 shows a 469.360351 MHz DDS output with a 5.0 GHz clock input with a FCW = 0x180800 in hex format. Because of the MSB mirroring shown in Fig. 5.8, the single output peak to peak voltage is 400 mV. So the output power in theory can be calculated as

$$10 \log \frac{(400 \text{ mV}/(2\sqrt{2}))^2}{15 \ \Omega \times 1 \text{ mW}} \approx 1.25 \text{ dBm}. \tag{5.9}$$

Counting the loss due to the parasitic capacitances, PCB tracks and RF cables, the measured output power is approximately -2.12 dBm. The measured SFDR is approximately 38 dBc in Nyquist bandwidth. Since the FCW = 0x180800, the output frequency is given by

$$\frac{\text{FCW}}{2^N} \times f_{clk} = \frac{\text{0x180800}}{2^{24}} \times 5.0 \text{ GHz} = 469.360351 \text{ MHz}. \tag{5.10}$$

In the stretch processing radar, which is essentially narrow band system, the narrow band SFDR of the DDS is often more important since wideband spurs can be removed relatively easily. It is only a specific narrow band near the output, which is usually less than 1% of the update frequency, which is of the interest of many applications [9]. Fig. 5.11 provides an example of a 1.246258914 GHz output frequency (FCW = 0x3FCFE7) with a 5.0 GHz clock frequency in 50 MHz band nearby. The measured narrow band SFDR is about 82 dBc.

Fig. 5.12 demonstrates the operation of the DDS with an LFM output. With a 300 MHz clock input, a 24-bit 300 MHz ramp from 0x000001 to 0x00AD9C is fed into the FCW input. The output sweeps from 18 Hz to 397.367947 kHz. In this DDS, CMOS logic was used to provide the modulation data inputs. The speed is limited by the speed of the data source that was provided by an Agilent pattern generator through the PCB board. A maximum of 2.5 GHz LFM can be reached if the modulation ramp is generated inside the DDS chip.

Fig. 5.13 shows the measured DDS output with FCW = 7, phase modulated by a step of PCW = 0x800 resulting in an 180° phase shift. The output frequency is 1.251 kHz with a 3.0 GHz clock. Both the LFM and the PM waveforms can be used in radar transceivers as

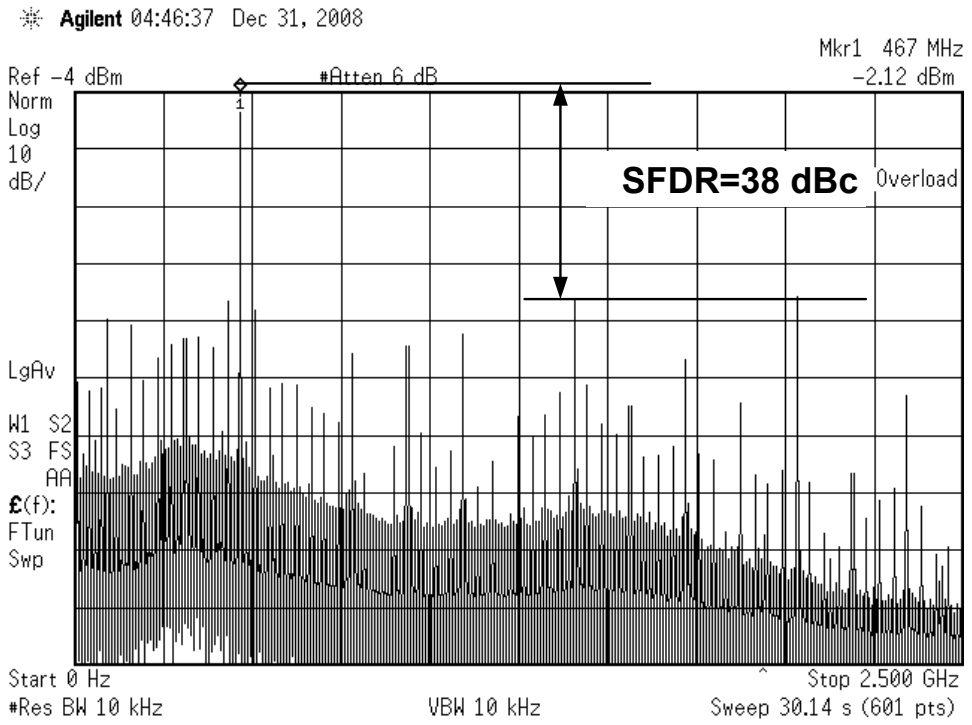


Figure 5.10: Measured DDS output with a 469.360351 MHz output and the maximum 5.0 GHz clock (FCW = 0x180800), showing a 38 dBc Nyquist band SFDR.

the source of transmitted chirp signal and the reference chirp signal for stretch processing, as described in Section II. Based on the discussion in Section II, chirp modulated waveform improves the radar range resolution, while the stretch processing using LFM reduces the bandwidth requirement for the ADC in receiver path.

Fig. 5.14 provides a plot of the measured SFDR versus the output frequency for the 24-bit 5.0 GHz DDS within a 50 MHz bandwidth, and demonstrates about 45 dBc narrow band worst-case SFDR. In addition, the DDS has several sweet spots, in which its output spectrum purity and its dynamic performance are much better than what can be obtained in other frequency bands. Fig. 5.11 gave an example of an 82 dBc SFDR in 50 MHz narrow band.

The die photo of the DDS is shown in Fig. 5.15. This DDS design is quite compact with an active area of 3.0×2.5 mm^2 and a total die area of 3.7×3.0 mm^2. Table 5.1 compares all the reported ultrahigh speed DDS RFIC performances with over-GHz output frequency,

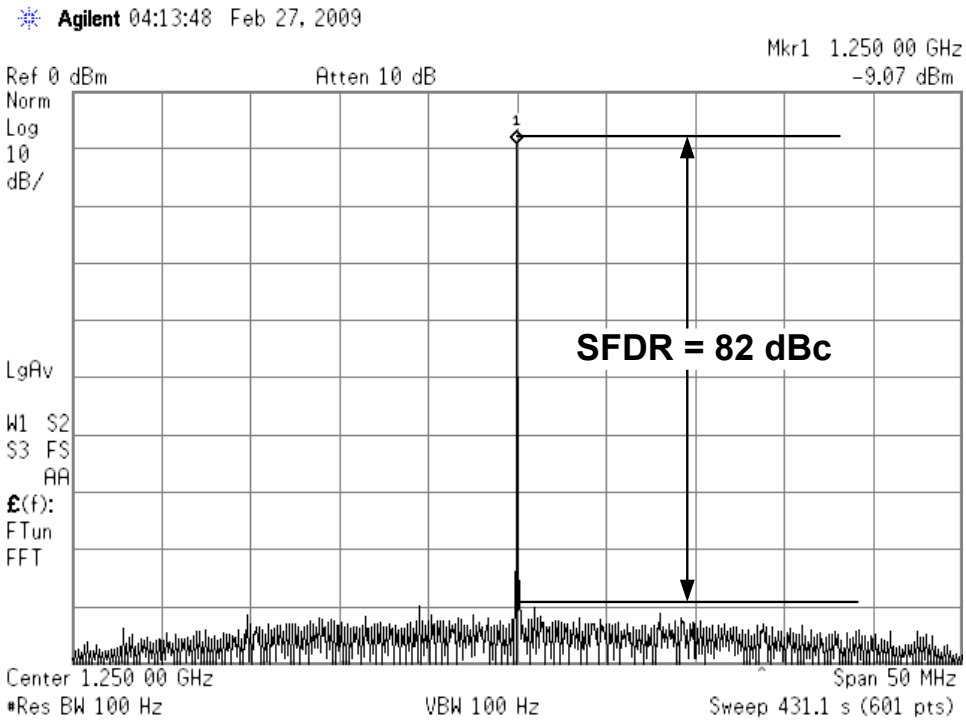


Figure 5.11: Measured DDS output with a 1.246258914 GHz output and the maximum 5.0 GHz clock (FCW = 0x3FCFE7), showing an 82 dBc narrow band SFDR.

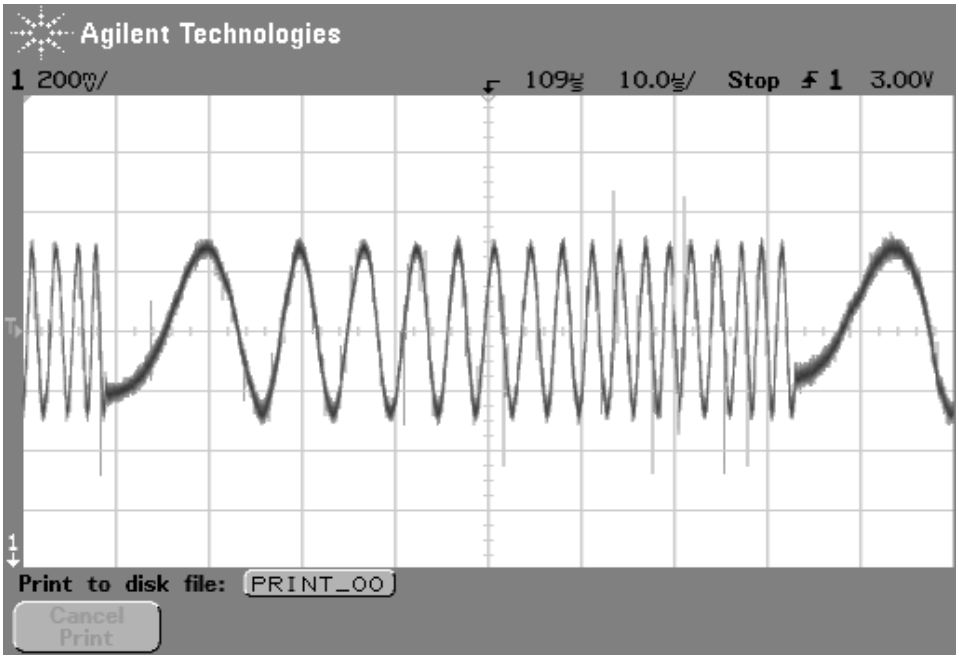


Figure 5.12: Measured DDS LFM output with a FCW sweeps from 1 to 0x005AD9C and using a 300 MHz clock.

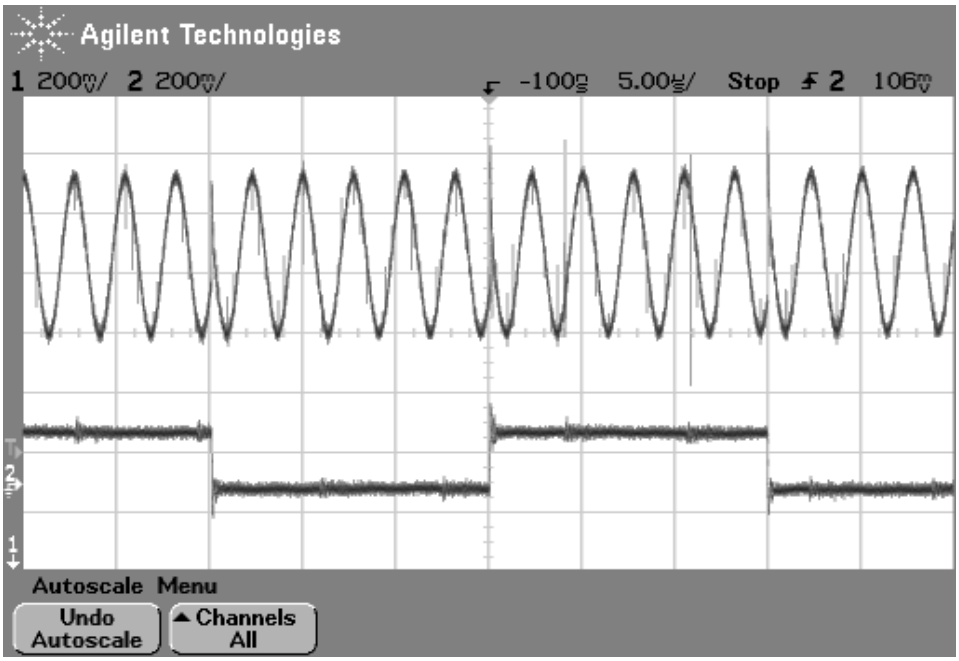


Figure 5.13: Measured DDS output with FCW = 7 phase modulated by a phase step of ΔPCW = 0x800 causing an 180° phase shift. The output frequency is 1.251 kHz with a 3.0 GHz clock.

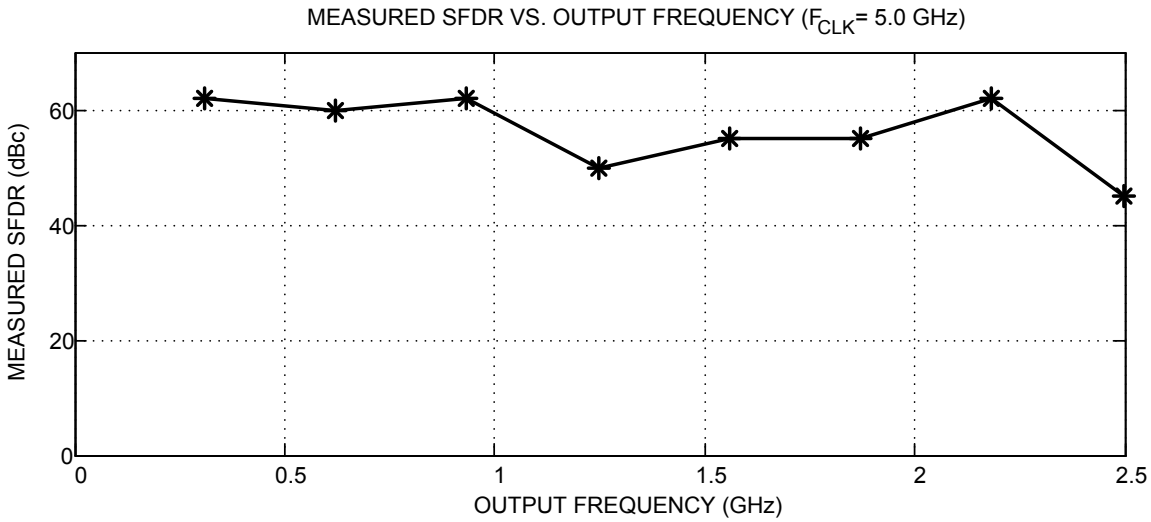


Figure 5.14: Measured DDS narrow band SFDR versus output frequency within a 50 MHz bandwidth.

including the DDSs presented in the previous chapters. Although the DDS reported here has relatively low frequency when compared with others, it is the first over-GHz output frequency implementation with direct digital FM and PM capabilities. Some commercial

parts have the direct digital FM and PM capabilities, but all the parts only work up to 1.0 GHz with an output of less than 500 MHz [31].

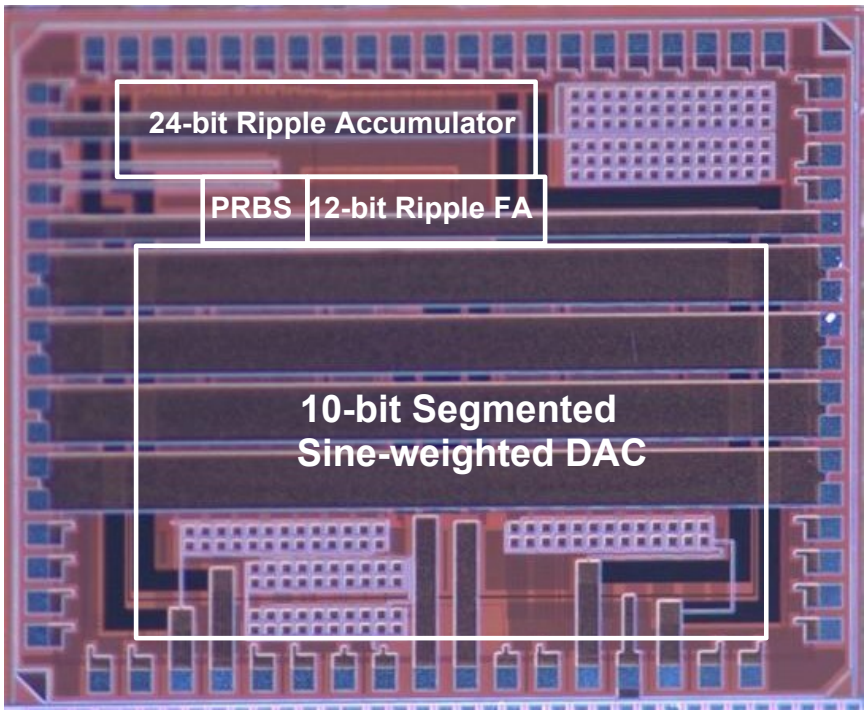


Figure 5.15: Die photo of the 24-bit DDS RFIC.

5.5 Conclusion

This chapter presented a 24-bit 5.0 GHz DDS RFIC with direct digital modulation capabilities, developed in a 0.13 μm SiGe BiCMOS technology for pulse compression radar applications. A 24-bit RCA accumulator and a 12-bit RCA are implemented for the use of modulator designs with over-GHz frequency output. For high-speed DDS implementation, adder delay is mainly dominated by the wire delays. A comparison between the RCA and CLA adder has been performed in this chapter. Compared to a CLA adder, the RCA has a simple ripple architecture, which can be layed out in a cascaded format one bit after another, resulting in a very compact layout with short wire interconnections between stages. Thus, the RCA actually ends up with higher operation frequency than the CLA adder.

This 24-bit DDS has more than 20,000 transistors and achieves a maximum clock frequency of 5.0 GHz. The measured worst-case SFDR is 45 dBc under a 5.0 GHz clock frequency and within a 50 MHz bandwidth. The best Nyquist band SFDR is 38 dBc with a 469.360351 MHz output using a 5.0 GHz clock frequency. This DDS represent the first implemented RFICs with direct digital modulations at over-GHz output frequency.

Table 5.1: Ultrahigh Speed DDS RFIC Performance Comparison

	Technology	f_T/f_{MAX} [GHz]	Phase [bit]	Amplitude [bit]	Max Clock [GHz]	FM [bit]	PM [bit]	SFDR [bit]	Power [W]	Area [mm^2]	FOM [GHz·$2^{\mathrm{SFDR}/6}$/W]
[18]	InP	137/267	8	7	9.2	None	None	<30	15	8×5	<16.0
[19]	InP	300/300	8	7	13	None	None	26.67	5.42	2.7×1.45	42.6
[20]	InP	300/300	8	5	32	None	None	21.56	9.45	2.7×1.45	34.8
[27]	InP	370/370	12	7.5	24	None	None	30.7	19.8	5.0×3.3	42.1
[21]	SiGe	100/120	9	8	12.3	None	None	20	1.9	3.0×3.0	65.3
[8, 9]	SiGe	200/250	11	10	8.6	None	None	33	4.8	4.0×3.5	81.1
[28]	SiGe:C	f_T=70	9	8	6.0	9	None	17	0.308	1	138.8
[9B DDS]	SiGe	200/250	9	7	2.9	9	9	35	2.0	2.5×3.0	82.7
[24B DDS]	SiGe	200/250	24	10	5.0	24	12	45	4.7	3.7×3.0	192.6

Chapter 6

An 8.7-13.8 GHz Transformer-coupled Varactor-less QCCO RFIC

6.1 Introduction

Quadrature signals are widely used in the wireless transceivers as local oscillator (LO) to generate the up- and down-conversions with image-reject mixing. There are several ways to generate quadrature signals. A frequency divider can be used to divide a voltage-controlled-oscillator (VCO) output at higher frequency to quadrature phase outputs. Divided-by-four is usually used because the divided-by-two method requires a 50% duty cycle for the VCO output. However, the divided-by-four method requires a VCO frequency output running at four times of the LO frequency, which results in higher power consumption and poor phase noise. A VCO followed by a passive poly-phase complex filter can be used to generate the quadrature outputs as well. However, the output has poor phase accuracy for wide band input. In addition, large loss due to the poly-phase network requires power-hungry buffers to boost the LO magnitude. At higher frequency, poly-phase filter is very difficult to be implemented because the reduced component values are more sensitive to the process variations and parasitic influences. Cross-coupling two single phase LC-VCO architectures are widely used to generate a quadrature output at high frequency. This technique provides wide-band quadrature accuracy and superior phase noise performance with increase power consumption.

There are various ways to couple the two VCOs and lock their oscillation frequency. The most common quadrature VCO (QVCO) topology shown in Fig. 6.1 utilizes the parallel coupling proposed by Rofougaran et al. [32]. The parallel VCO (P-QVCO) delivers quadrature signals with low phase and amplitude errors, yet has a narrow tuning range with the tuning limit of the varactor. Series QVCOs (S-QVCO) have been proposed using CMOS or

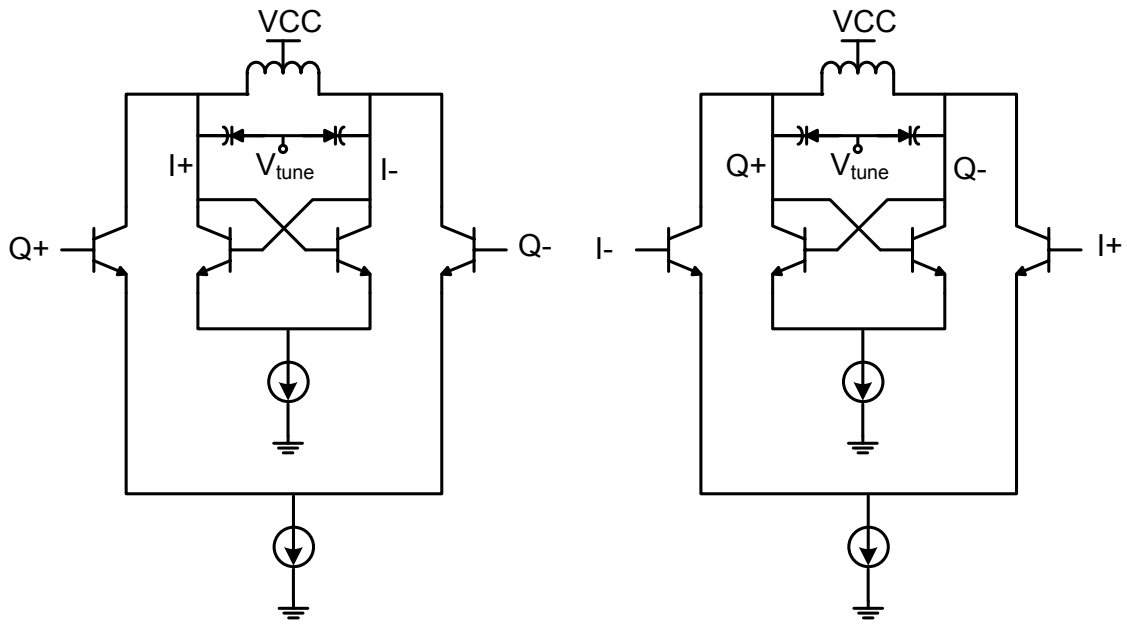


Figure 6.1: Quadrature VCO circuits with parallel coupling.

BiCMOS technology by connecting the coupling transistors in series [33, 34, 35]. It reduces the noise by using the cascode devices and provides better isolation between the VCO output and its current sources. However, the S-QVCO also suffers from a narrow frequency tuning range because of the varactor's small tuning capability. A magnetically tuned quadrature oscillator has been reported by Cusmai et al. and the output frequency can be tuned from 3.2 GHz to 7.3 GHz [36]. Modern communication and radar systems require quadrature signal generation at X- and Ku-bands with wide tuning range for the frequency source used in phase-locked-loops (PLL) or direct digital frequency synthesizers (DDS) [8,9,21]. An 8.7-13.8 GHz transformer-coupled varactor-less quadrature current-controlled oscillator (QCCO) is presented in this chapter [37, 38]. It employs the same mechanism as what presented in [36] but has a higher output frequency.

This chapter will present the principle and oscillator implementation as well as the phase accuracy and phase noise analysis. The implementation and modeling of the adopted stacked octagonal transformers will be discussed. Finally, it gives the experimental results and the conclusion is drawn.

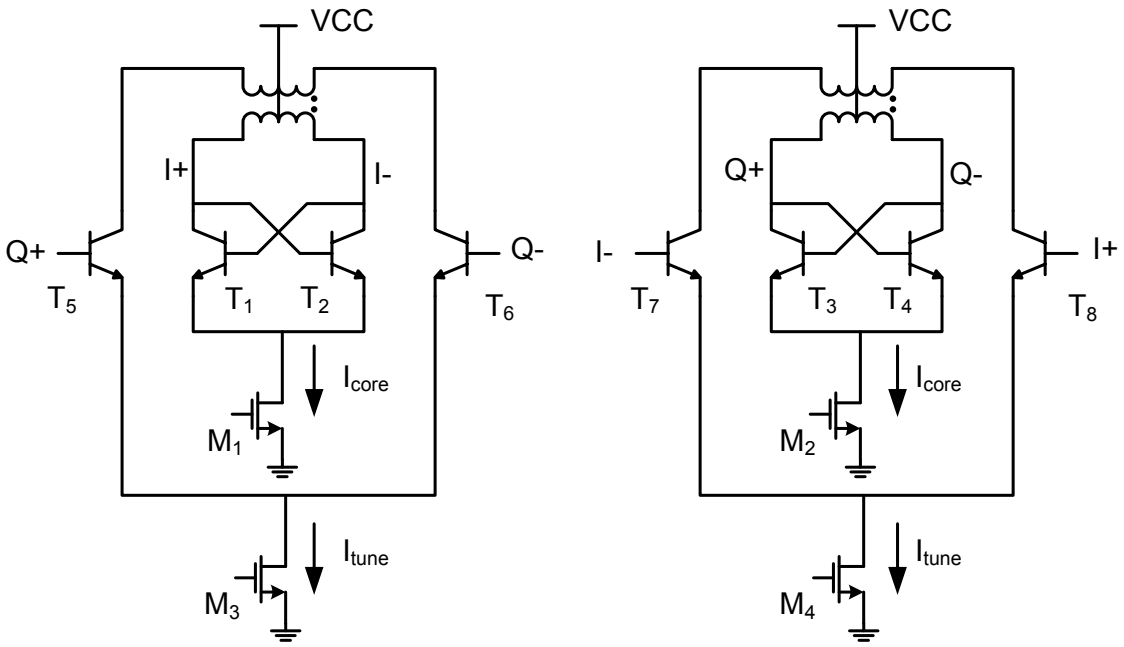


Figure 6.2: Schematic of transformer-coupled varactor-less QCCO.

6.2 Analysis and Design of Transformer Coupled Quadrature Oscillator

6.2.1 Oscillation Analysis and Design

The varactor-less QCCO presented here is a transformer-coupled current-controlled LC oscillator that utilizes SiGe hetero-junction bipolar transistors (HBT) for oscillation and current tuning. The NPN HBTs achieve very high oscillation frequency and low phase noise. The proposed QCCO circuit is illustrated in Fig. 6.2, in which two pairs of cross-coupled NPN HBTs T1, T2 and T3, T4 are used to generate the negative resistance for in-phase CCO (I-CCO) and quadrature phase CCO (Q-CCO) output respectively. Another two pairs of NPN HBTs T5, T6 and T7, T8 are used to provide the tuning currents for the transformers. All the HBTs operate near the peak f_T bias current in order to maximize the switching speed. Fig. 6.3 shows an AC equivalent circuit of one of the I-CCO or Q-CCO. The discussions presented below take I-CCO as an example, since the Q-CCO has the same structure. The primary winding of the transformer has the same function as the LC-tank in the conventional LC coupled VCO. $-1/g_m$ is generated from the cross-coupled transistor

pair T1 and T2. cp and rp are the total parasitic resistance and capacitance between the two terminals of the primary transformer winding in the oscillator circuit. The capacitance cp includes all the transformer capacitances as well as the transistor parasitic capacitance. The secondary winding parasitic devices do not show up since they have little effect on the CCO output. To achieve high frequency, no extra capacitor or varactor is used. With intuitive analysis based on Fig. 6.3, the output voltage V_o of the I-CCO equivalent circuit can be expressed as

$$\begin{aligned} V_o &= j\omega L_p I_{core} + j\omega M I_{tune} \\ &= j\omega I_{core}(L_p + \alpha M), \end{aligned} \tag{6.1}$$

where $\alpha = I_{tune}/I_{core}$. M is the mutual inductance between the primary and secondary windings. The mutual inductance M can be calculated using

$$M = k\sqrt{L_p L_s}. \tag{6.2}$$

where k is the coupling factor of the transformer. Thus, the effective inductance for the oscillation tank is given by

$$L_{eff} = L_p + \alpha M. \tag{6.3}$$

For either I-CCO or Q-CCO the oscillation frequency can be found as

$$f_{osc} = \frac{1}{2\pi\sqrt{(L_p + \alpha M)c_p}}. \tag{6.4}$$

By changing the tuning current I_{tune}, α will be changed, so does the oscillation frequency of the QCCO output. Because α can be tuned arbitrarily by the QCCO core current and turning current, and can be negative or positive, the ideal oscillation frequency can be tuned from a small value to infinity when α is tuned from positive infinity to L_p/M. So the QCCO output frequency can be very widely tuned with carefully selected devices and current ratios.

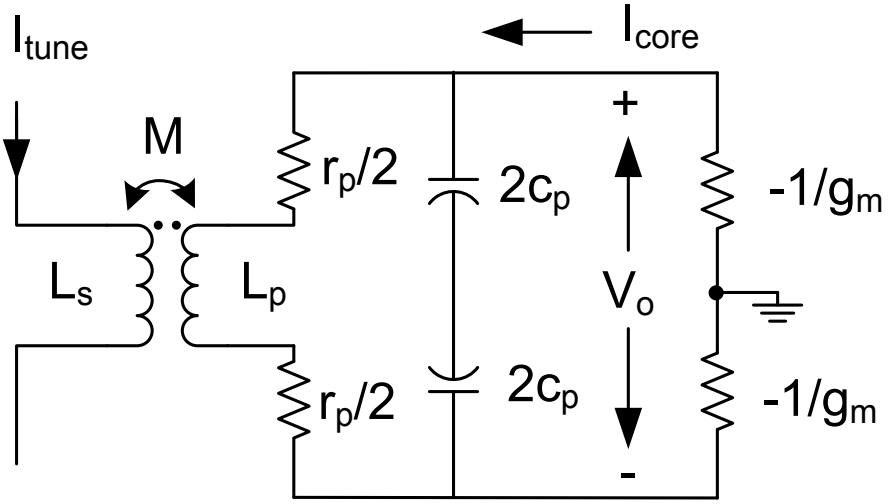


Figure 6.3: AC equivalent circuit of the transformer tank.

To determine the actual accuracy output voltage and oscillation frequency, from the circuit analysis of the AC equivalent circuit shown in Fig. 6.3, the output voltage of the oscillator can be calculated as

$$V_o = I_{core}\left[\frac{1}{j\omega c_p}//(r_p + j\omega L_p)\right] - j\omega M. \tag{6.5}$$

Separation Eq. (6.5) into real and imaginary parts leads to the following expression for the oscillation amplitude V_o and frequency ω_{osc}:

$$V_o = I_{core}\frac{L_p}{r_p c_p} = I_{core}\cdot\omega_0 Q L_p. \tag{6.6}$$

$$\begin{aligned}\omega_{osc}^2 &= \omega_0^2\left[(1-\frac{1}{2m}-\frac{1}{2Q^2}) \pm \frac{1}{2m}\sqrt{\left[\frac{m\omega_0^2}{\omega_c^2}+(3-2m)\right]^2 - 4\left[(m-1)^2+1\right]}\right] \\ &\approx \omega_0^2\left[(1-\frac{1}{2m}-\frac{1}{2Q^2}) \pm \frac{1}{2m}\sqrt{1-4m}\right].\end{aligned} \tag{6.7}$$

where $Q = (\omega_0 L_p)/r_p$, $\omega_0 = 1/\sqrt{L_p c_p}$ and $\omega_c = 1/(r_p c_p)$ are the quality factor, self-resonance frequency and corner frequency of the transformer primary winding. $m = \frac{M}{L_p}\cdot\frac{I_{tune}}{I_{core}}$ can be

considered as the coupling strength of the transformer [36, 39, 40]. The oscillation amplitude is independent of the tuning current and is determined by core current and transformer parameters only. The approximation of osc is acceptable when $\omega_c \gg \omega_0$, which is true for the transformer windings. The oscillation frequency is determined by the quality factor as well as m, which is the function of the self-inductance and mutual inductance of the transformer and the current ratio of the tuning current and core current of the oscillator.

To increase the tuning capability with small tuning current, transformer need to be carefully designed to maximize its mutual inductance. A stacked octagonal transformer shown in Fig. 6.4, which has the maximum mutual inductance in theory, is designed to reduce the magnetic flux leakage [41]. The transformer design will be discussed in the following section.

6.2.2 Quadrature Coupling Phase Accuracy and Phase Noise

Fig. 6.5 shows the full AC equivalent circuit of the varactor-less QCCO. If we take T5, T6 and T7, T8 as -Gm amplifiers, Fig. 6.5 can be further simplified to Fig. 6.6. Fig. 6.6(a) shows the transformer in-phase case of the QCCO, while Fig. 6.6(b) shows the transformer anti-phase. Suppose the phase delay of both -Gm amplifiers is ϕ, from Barkhausen criteria, the phase delay for the in-phase and anti-phase oscillators can be determined by

$$\phi + \phi + \pi = 2n\pi,\ n = 1, 2, \cdots . \tag{6.8}$$

and

$$\phi + \pi + \phi + \pi + \pi = 2n\pi,\ n = 1, 2, \cdots . \tag{6.9}$$

Thus, the phase delay of the -Gm amplifier is given by

$$\phi = \pm\frac{\pi}{2}. \tag{6.10}$$

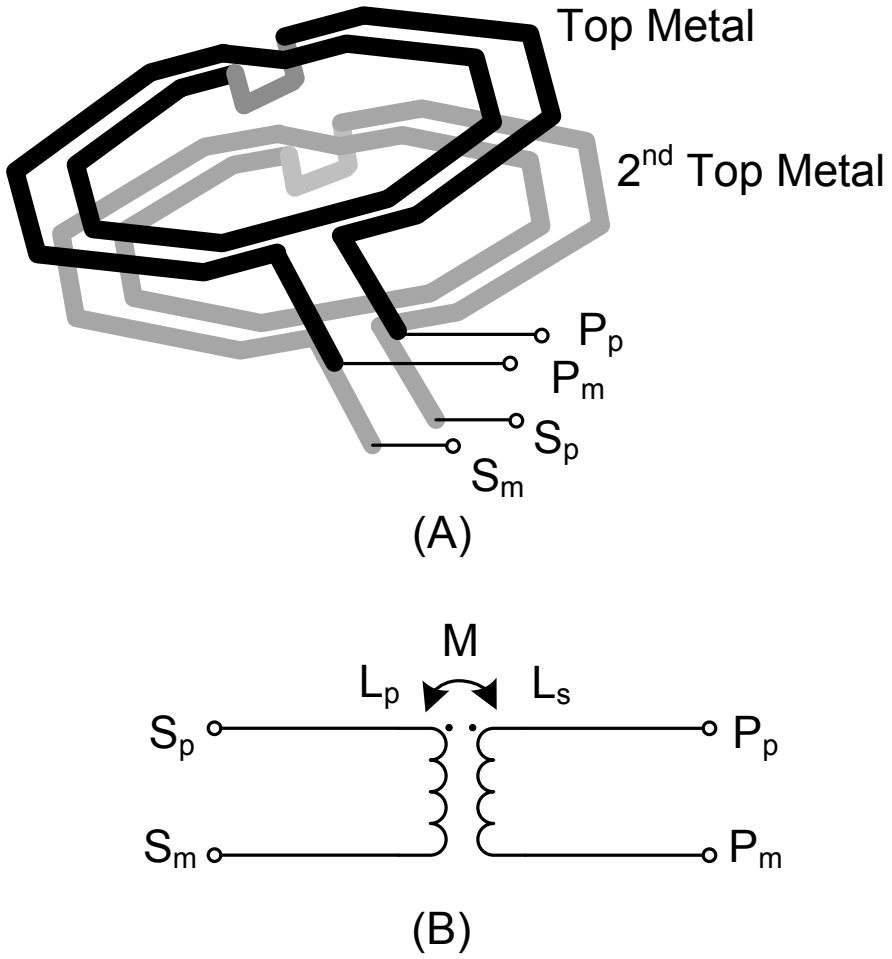


Figure 6.4: Stacked octagonal transformer.

Therefore, regardless of in-phase or anti-phase, the phase delay between I and Q is $\pi/2$ or $-\pi/2$. In another word, quadrature frequency outputs can be generated. In practice, there are mismatches between the devices used in the oscillator circuit, which results in slightly different phase delays between the two -Gm amplifiers as well as the two transformers. The device and transformer mismatches are the major contributors of phase error between the quadrature outputs. Another phase error source comes from the coupling between the two transformers used in I oscillator and Q oscillator. From [40], the total phase error ϕ_e can be determined by

$$\phi_e = \frac{1}{2}\frac{Q}{m^2}\varepsilon + k'\frac{Q}{m}. \tag{6.11}$$

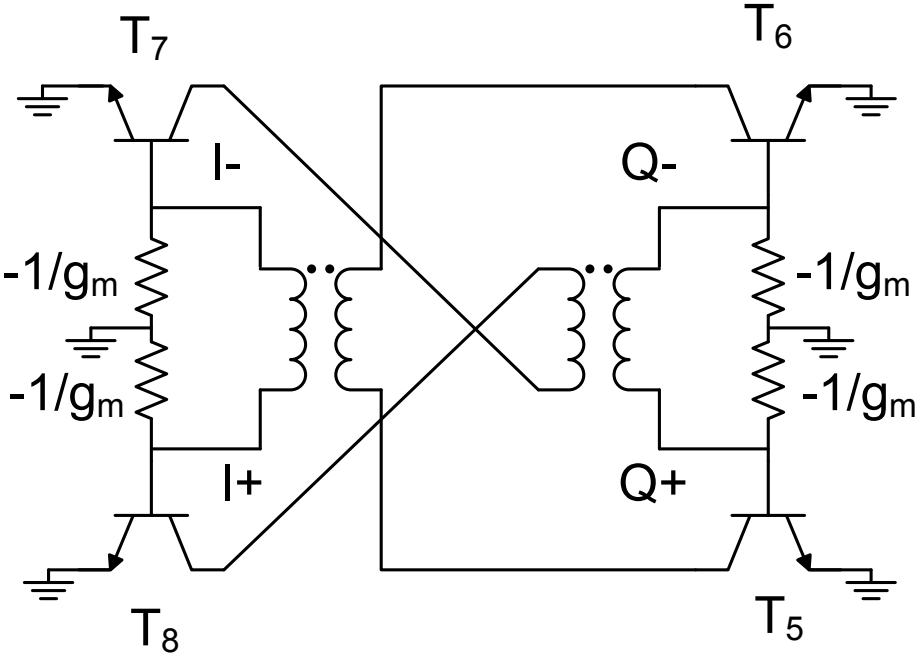
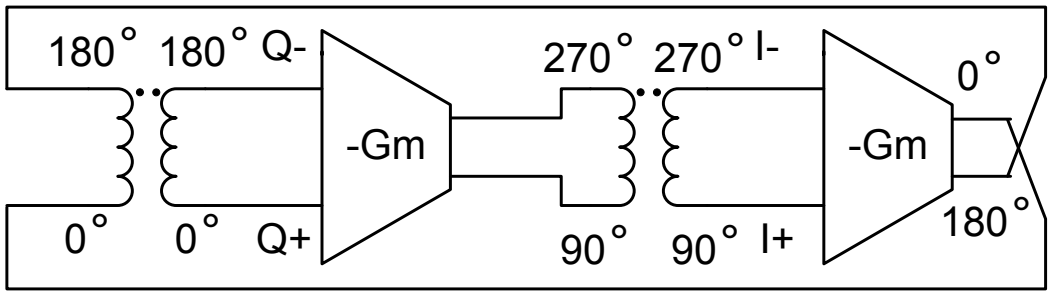
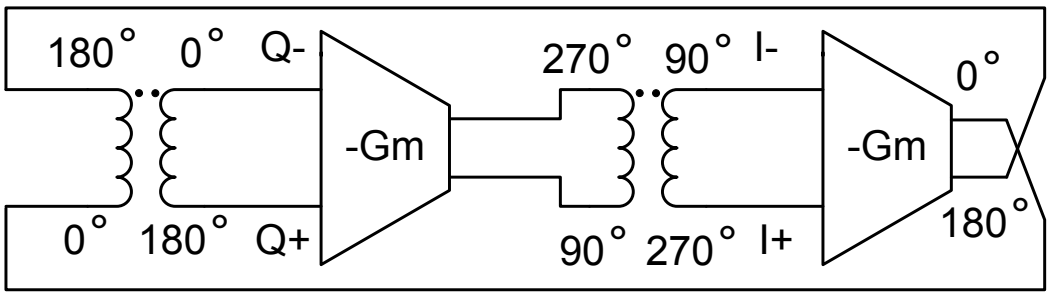


Figure 6.5: AC equivalent circuit of the varactor-less QCCO.



(a) Transformer in phase



(b) Transformer anti phase

Figure 6.6: Equivalent circuits of the varactor-less QCCO.

where ε represents the mismatches between the devices and transformers, k' is the coupling factor between the primary windings of the two transformers. m is the coupling strength of the transformer defined same as that in Eq. (6.7). So the phase error will increase with a better quality factor and a bigger coupling strength of the transformer.

The phase noise of the oscillators has been intensively investigated previously [41,42,43]. The analysis of the conventional quadrature oscillator has been proposed in [33,39,44]. The phase noise of the transformer coupled oscillator is similar with the conventional quadrature oscillators defined in [39], namely,

$$\mathcal{L}(\Delta\omega) = \frac{kT}{C} \cdot \frac{\omega_{osc}}{Q} \cdot \frac{1+m^2}{2} \cdot \frac{1}{\Delta\omega^2} \cdot \frac{1+(1+m)F}{A_0^2} \tag{6.12}$$

where A_0 is the oscillation amplitude across one of the tanks, F is the noise factor of the conventional single-phase oscillator. From Eq. (6.12), the phase noise of the quadrature oscillator increases rapidly with the increasing of m and reduced with a better quality factor of coupling inductors or transformers. This conclusion can be obtained by the phase noise analysis in [36], as well. So, a trade-off needs to be considered between the phase accuracy and phase noise with respect to m and Q in the quadrature oscillator designs.

6.3 Transformer Implementation

6.3.1 Geometry Design of Transformers

The transformer coupled QCCO has been designed in a 0.18 μm SiGe BiCMOS technology. The transformer design has been optimized in simulations, by means of the full-wave electromagnetic solver, *Agilent Momentum*, in order to maximize magnetic coupling k or the M/L ratio and the primary winding quality factor Q. For different transformer structures, the self-inductance L, the mutual inductance M or the coupling coefficient k, the turn ratio n, the quality factor Q and the self-resonance frequency ω_0 may vary significantly. Depending on the transformer structure and the magnetic coupling method (lateral

or vertical), different approaches in transformer layout have been proposed [45, 46]. Usually, transformers are formed by magnetically coupling two or more inductors. There are four commonly used inductor shapes: square, hexagonal, octagonal and circular. Based on these inductors, inter-winding or stacked transformer can be built with different geometry shapes. Considering the transformer performance (usually inductance and quality factor), the circular is the best choice, followed by octagonal and hexagonal, and the square is the worst. But the circular layout of the transformers is not compatible with most of the design rules. So octagonal is the most commonly used shape to build inductors and transformers. For differential circuits, such as what used in the proposed quadrature oscillator, symmetrical shape is required. Based on above discussions, Fig. 6.7 illustrates three transformers: concentric, inter-wound and stacked. The concentric transformer has a worse coupling factor than the inter-wound and stacked structure. A stacked structure transformer is used in this design because of a smaller layout area than the inter-wound one as well as a better magnetic coupling than the concentric one. Fig. 6.4 shows the adopted stacked transformer drawing diagram with terminal names labeled with respect to the transformer symbol. In this SiGe technology, top metal layer is much thicker than any of other metals and stays farthest to the substrate. It is thus used to fabricate the primary winding in order to achieve a better quality factor. The second top metal layer is used to fabricate the secondary windings. While the top metal is thicker than the second top metal, both top and second top metals in the chosen 0.18 μm SiGe technology are much thicker than other metal layers and both are optimized with lower sheet resistance for analog routing. Both the primary and secondary windings are 10 μm wide and have two turns with diameter of 200 μm. The two windings are exactly overlapped and the winding wire space is 5 μm, which is the minimum design rules allowed space, between the two turns, to maximize the fill ratio (defined later). At low frequencies, the Q of the inductor is limited primarily by the resistance of the metal layer. At high frequency, Q degradation is dominated by the loss mechanisms caused by the substrate [32]. To minimize the Q dependence on the substrate resistivity, the transformer

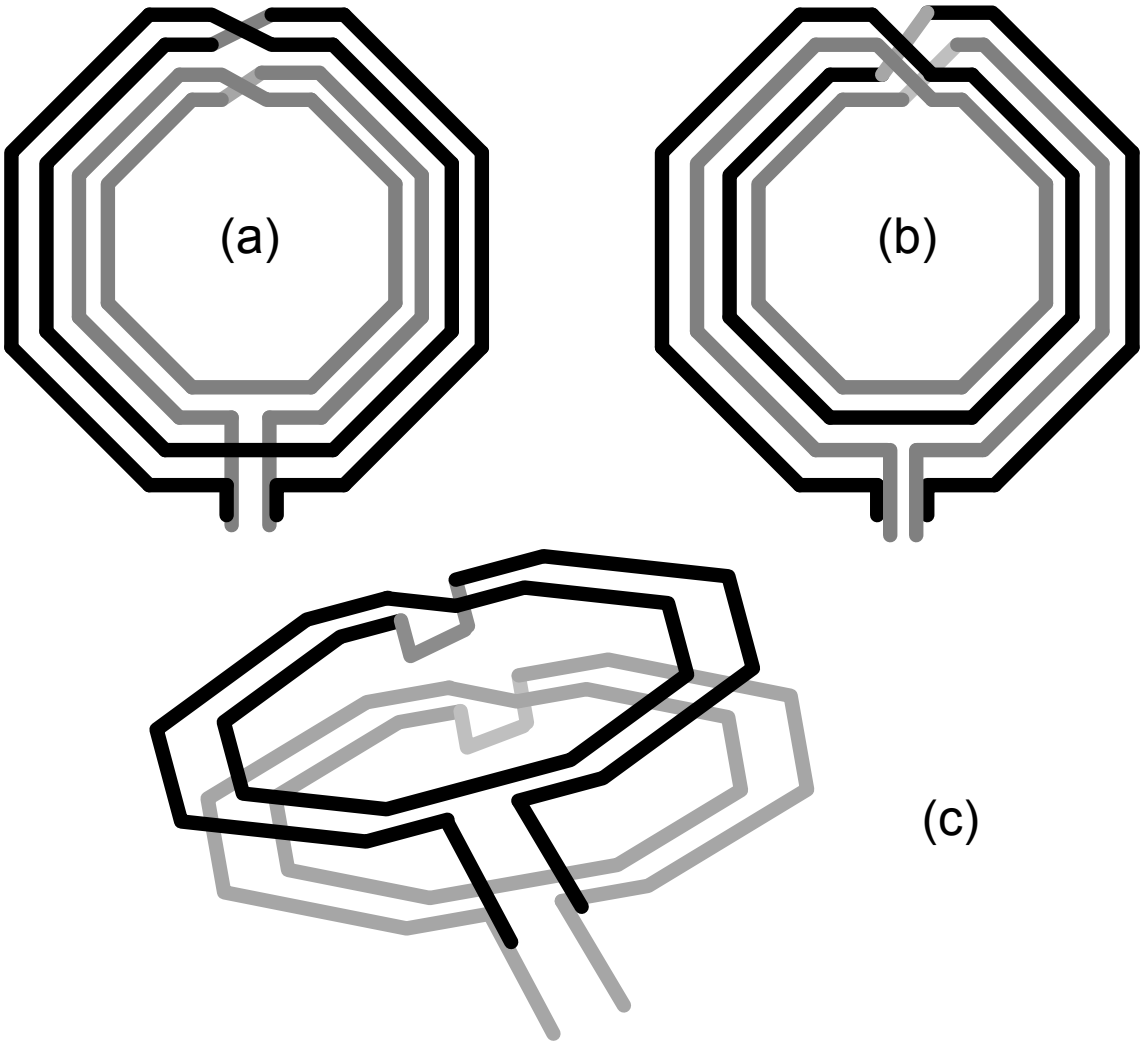


Figure 6.7: Octagonal symmetrical transformer: (a) concentric, (b) inter-wound, and (c) stacked.

is placed on top of a patterned ground shield (PGS) to minimize the current injected into the substrate. The PGS is a patterned conductive layer and formed by a lattice of highly resistive deep trench (DT) isolation layer in this design. Fig. 6.8 shows the diagram of the three-dimension substrate and two-dimension DT lattice used in this design. The PGS substrate is used to reduce the parasitic capacitance of the transformer to the substrate as well as increase the parasitic resistance to the substrate.

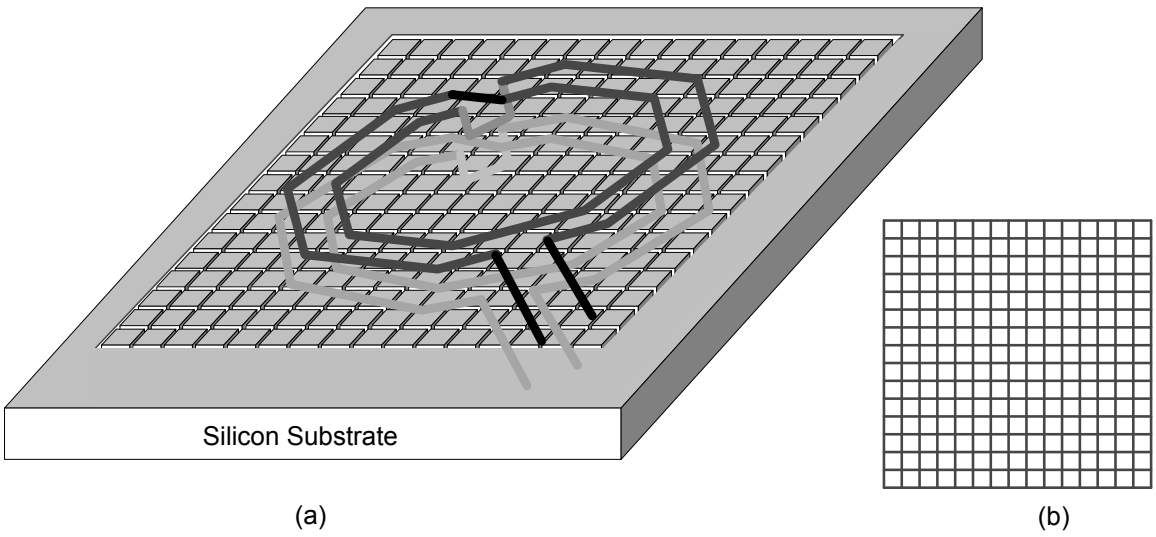


Figure 6.8: Diagram of the (a) three-dimension PGS substrate and (b) two-dimension deep trench lattice.

6.3.2 Transformer Equivalent Circuit and Parameters

Usually the frequency domain model of the transformer is more important since most performances of the oscillator are analyzed in frequency domain. However the time domain equivalent circuit is more intuitive. Fig. 6.9 shows the 2-π equivalent circuit of the stacked transformer. L_p and L_s are the self-inductance of the primary and secondary windings. R_p and R_s are the series resistance of the primary and secondary windings. C_{pp} and C_{ss} are the inter-winding capacitance between the two turns of the primary or secondary winding. C_{ps} is the capacitance between the stacked primary and secondary winding. C_{bp} and C_{bs} are the parasitic capacitances of primary and secondary windings coupled to the PGS. R_b is the parasitic resistance to the PGS substrate.

The self-inductance for the octagonal inductor can be estimated using equation developed by Mohan [46, 47], namely,

$$L = 2.25\mu_0 \frac{n^2 d_{avg}}{1 + 3.55\rho} \tag{6.13}$$

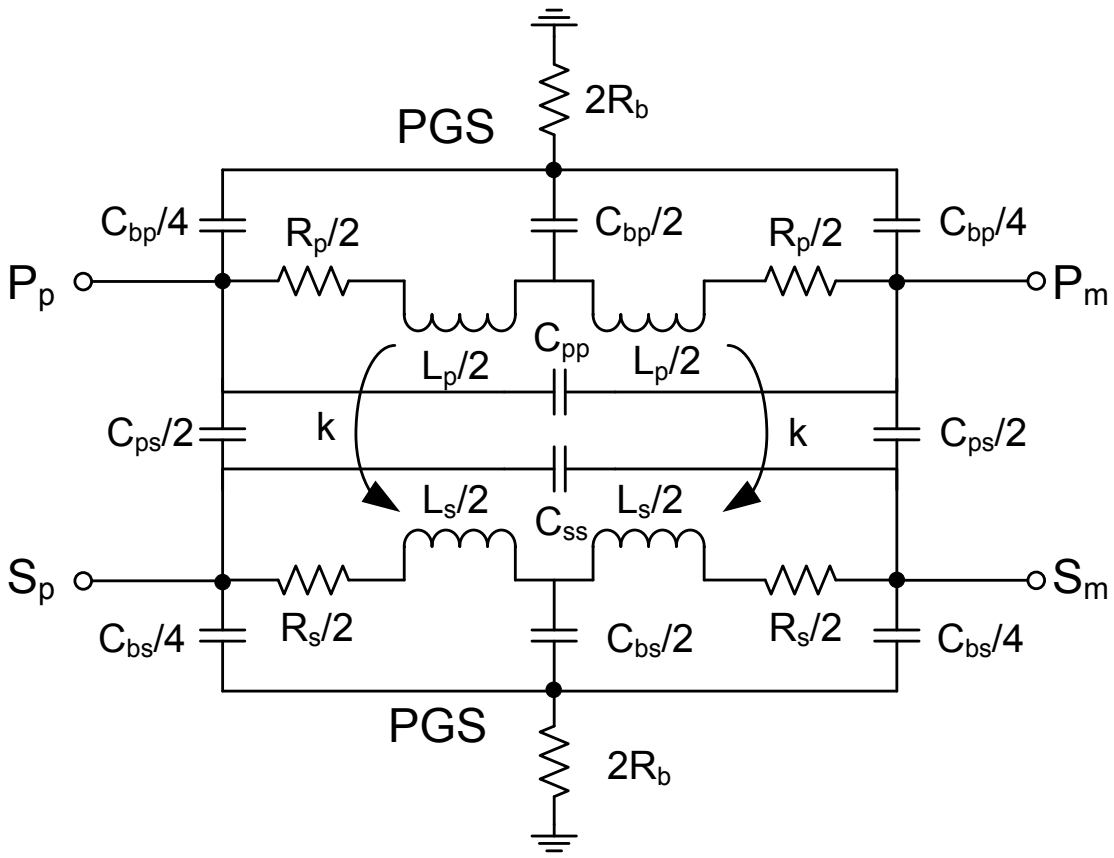


Figure 6.9: Transformer time domain equivalent circuit model.

where, $d_{avg} = 0.5(d_{out} + d_{in})$ is the average value of the outer diameter d_{out} and the inner diameter d_{in} of the octagonal inductor. ρ is the fill ratio defined as $\rho = (d_{out} - d_{in})/(d_{out} + d_{in})$. The mutual inductance M is defined in Eq. (6.2). The coupling factor k of the stacked transformer is over 0.8.

More accurate self-inductance and mutual inductance or coupling factor can be obtained by electromagnetic simulation and vector network analyzer (VNA) measurement. Fig. 6.10 shows the simulated parameters of the octagonal stacked transformer. Fig. 6.10(a) is the plot of primary and secondary self-inductance. They are almost identical since the metal material and thickness doesn't affect the inductance greatly [45]. Fig. 6.10(b) shows the coupling factor of the transformer. It is around 0.8 and approaches to 1 at high frequency. Fig. 6.10(c) is the plot of quality factor of the primary and secondary windings. The peak Q

of the primary winding is about twice of that of the secondary winding because the primary winding metal is thicker and has a lower sheet resistance than the secondary one.

In this oscillator design, the parallel capacitance between the terminals of the transformer primary winding is used as the oscillation tank capacitance. The total parallel capacitance is given by

$$C_p = C_{pp} + \frac{C_{bp}}{8} + \frac{C_{ps}}{4} // (C_{ss} + \frac{C_{bs}}{8}). \tag{6.14}$$

With the geometry and electronic parameters of the transformer, all these capacitance C_{pp}, C_{bp}, C_{ps}, C_{ss} and C_{bs} represent the total capacitance corresponding to the respective nodes and can be calculated using simple parallel-plate capacitor model. The PGS is far away from the windings, so C_{bp} is much smaller than other capacitance. The accurate frequency dependent capacitance paralleled with the primary winding can be simulated from electromagnetic simulation tools, too. Fig. 6.11 gives the plot of the total capacitance with simulated capacitance value of 0.6 pF at 10 GHz frequency.

In practical, it is not easy to find out the exact inductance and capacitance associated with the transformer. With the help of S-parameter, all the simulations can be performed through hybrid simulation tools. In this design, *Agilent Dynamic Link* tool is used to recall the $SPICE$ simulator and $Momentum$ electromagnetic simulator for all time domain and frequency domain simulations. Therefore, the oscillator was designed by directly specifying the geometric parameters of the transformers instead of giving the L, C parameters in the traditional design flows. The more flexible electromagnetic and circuit co-simulation approach increases the design speed dramatically since the modeling process is removed.

6.4 Experimental Results

The transformer-coupled varactor-less QCCO was implemented and fabricated in a 0.18 μm SiGe BiCMOS process with the chip die photo shown in Fig. 6.12. The QCCO

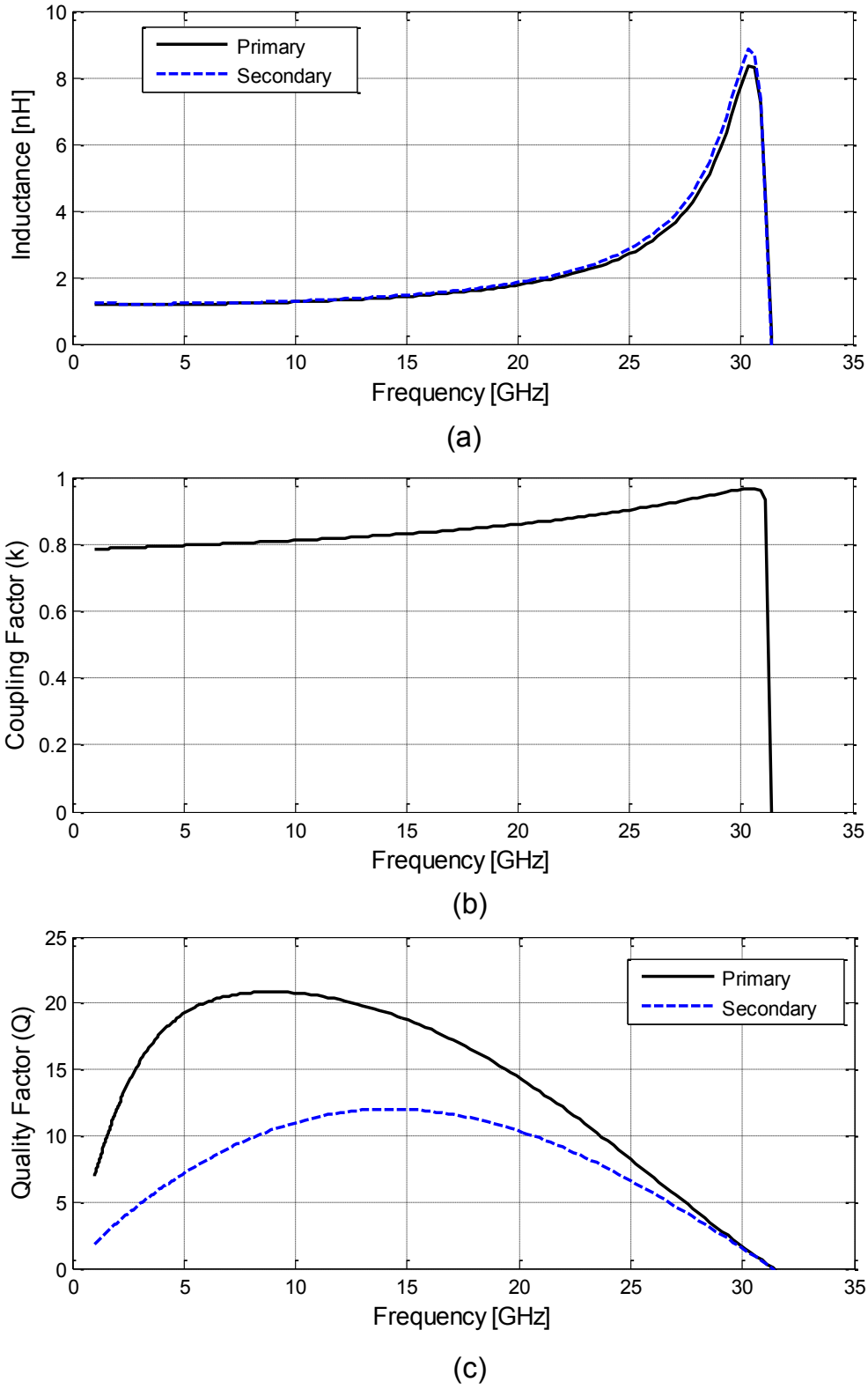


Figure 6.10: Simulated parameters of the transformer windings: (a) self-inductance L, (b) coupling factor k, and (c) quality factor Q.

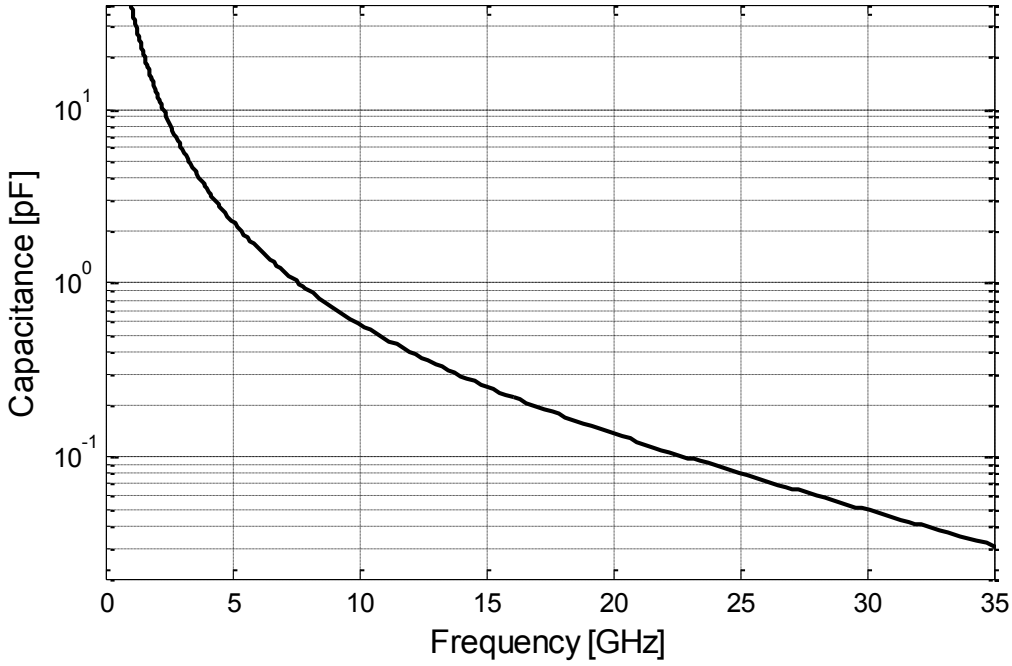


Figure 6.11: Simulated capacitance parallel with the transformer primary winding.

core area is 0.5×0.4 mm^2. As shown in the die photo, the I-CCO and Q-CCO are symmetrically placed. The layout is also optimized to lower the effect of layout parasitic on the QCCO performance including the harmonic distortion and phase noise. The QCCO is tested in the package of CLCC-28. A buffer is included on-chip in order to drive 50 *Omega* load provided at the input of a spectrum analyzer or a digital oscilloscope. Due to the limitation of the test set up, all the test results were measured based on the single-ended output, although the QCCO has full differential frequency output capability. Single-ended testing ends up with degraded phase noise and I-Q mismatch.

A wide tuning range of 45.3% is achieved with the tuning current I_{tune} tuned from 0.4 to 2.9 mA and the QCCO core current I_{core} tuned from 1.2 to 5.5 mA. The measured QCCO turning range is given in Fig. 6.13. It shows continuous tuning range from 8.7 to 13.8 GHz. Fig. 6.14 shows the measured quadrature outputs with 11.5 GHz frequency.

The measured phase noise with an 11.02 GHz output frequency is shown in Fig.6.15. With the single-ended test, the transformer-coupled varactor-less QCCO achieves 86.8 dBc/Hz

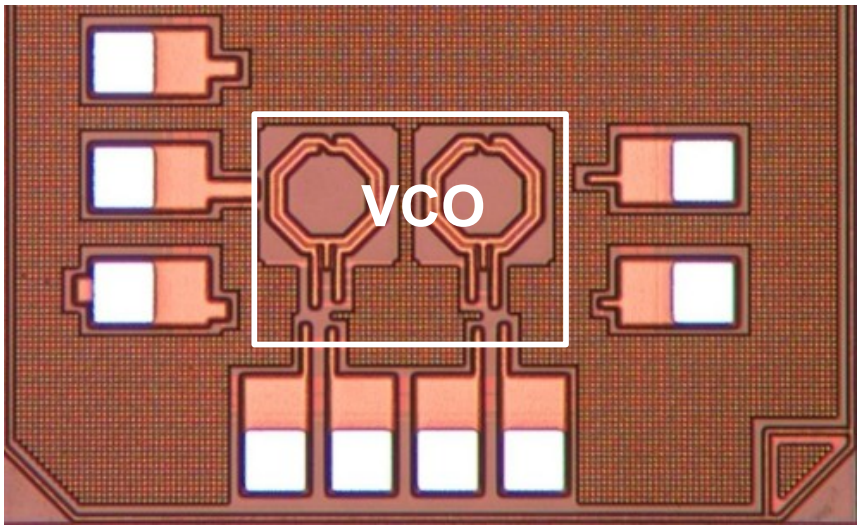


Figure 6.12: Fabricated QCCO RFIC die photo.

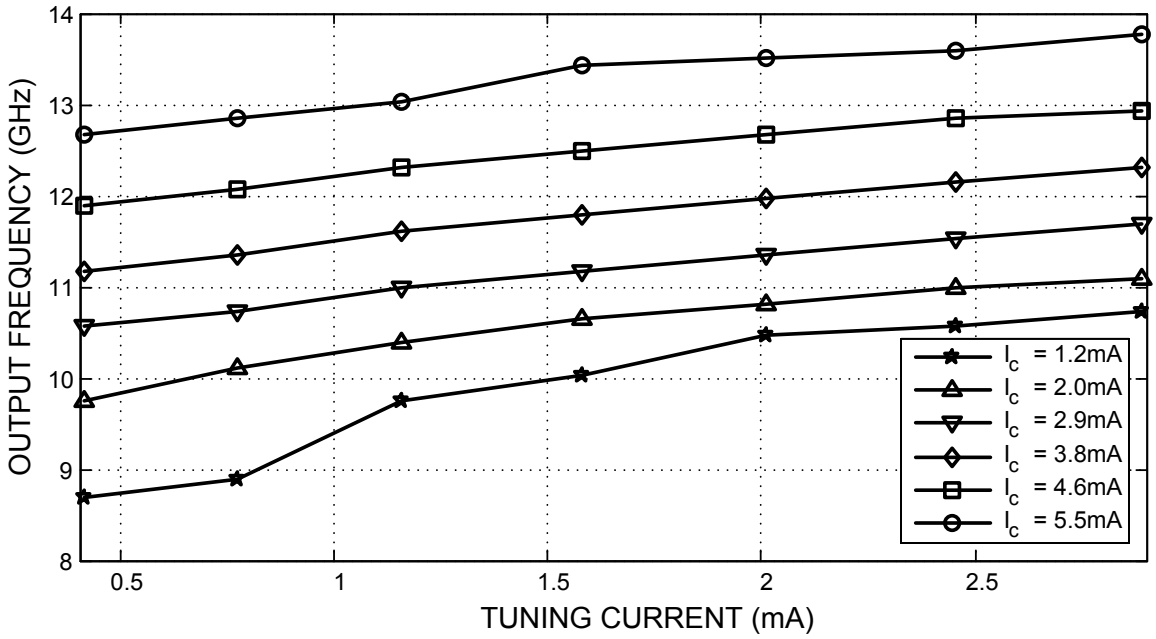


Figure 6.13: Measured QCCO tuning range.

phase noise at 1 MHz offset frequency and 110 dBc/Hz at 10 MHz offset frequency. A widely accepted figure-of-merit (FOM) for VCO designs is proposed in [48]. The FOM takes into account output frequency, phase noise performances and power consumption and is expressed by

$$FOM = L(\Delta f) - 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P_{diss}}{1mW}\right). \tag{6.15}$$

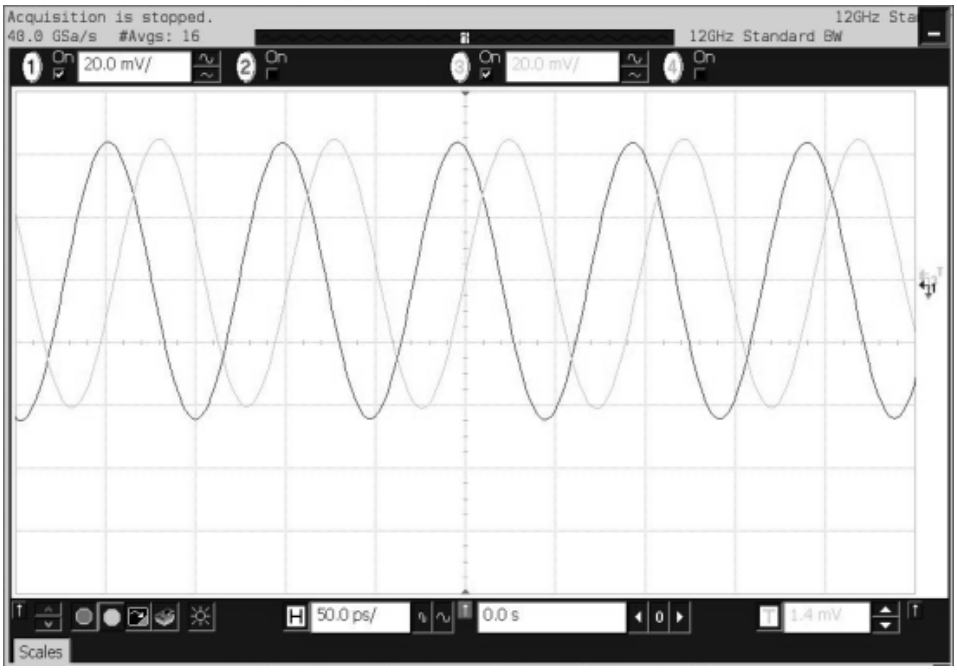


Figure 6.14: Measured QCCO outputs at 10.5 GHz with tuning current of 1.5 mA and core current of 2 mA.

where $L(\Delta f)$ is the phase noise at the offset frequency Δf from the carrier frequency f_0. P_{diss} is the total core power dissipation of the I-CCO and Q-CCO. The FOM of this transformer-coupled varactor-less QCCO is calculated as -154 dBc/Hz.

Table 6.1 summarizes the measured results of the transformer-coupled varactor-less QCCO. It achieves 45.3% wide tuning range and the core circuit occupies 0.4×0.5 mm^2 chip area in a 0.18 μm SiGe BiCMOS process. It draws 8-18 mA current over the tuning range under a 1.8 V power supply. Table 6.2 compares the frequency, tuning range, power consumption and phase noise for several variable-frequency oscillators. Compared to [32,33, 35], the proposed oscillator has a much higher output frequency and tuning range. Compared to [36], it has higher frequency, yet a worse phase noise.

6.5 Conclusion

A transformer-coupled varactor-less wide tuning QCCO is presented in this chapter. It achieves 45.3% wide tuning range by tuning the oscillator currents flowing through the

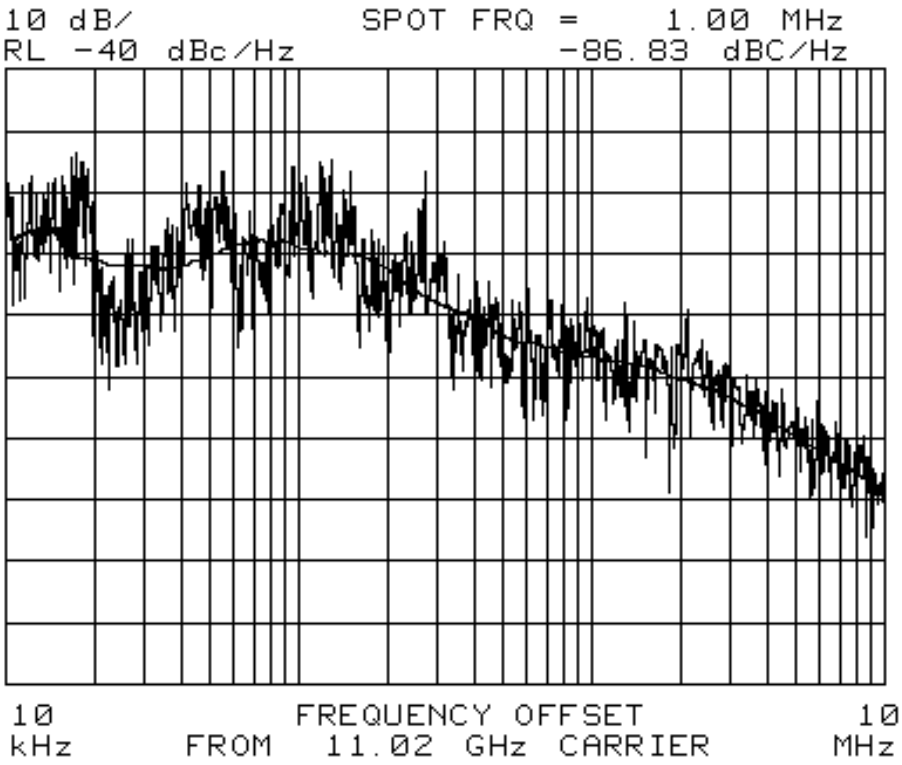


Figure 6.15: Measured QCCO phase noise with output frequency of 11.02 GHz.

Table 6.1: QCCO Performance Summary

Technology	0.18 μm SiGe BiCMOS
Supply voltage	1.8 V
Oscillation frequency	8.7-13.8 GHz
Tuning range	45.3%
Core current	8-18 mA
Buffer current	8 mA
Phase noise @ 1MHz	-86.8 dBc/Hz
Phase noise @ 10MHz	-110 dBc/Hz
QCCO area	500 μm$\times$400 μm
FOM	-154 dBc/Hz

primary and secondary winding of the stacked octagonal transformers. The prototype QCCO is fabricated in 0.18 μm SiGe BiCMOS technology and the core circuit occupies 0.4$\times$0.5 mm^2 chip area. It draws 8-18 mA current under a 1.8 V power supply. The measured phase noise

Table 6.2: Performance Comparison of Variable-frequency Oscillators

Ref	Technology	Frequency [GHz]	Tuning Range	Power [mW]	Phase Noise [dB/Hz]
[32]	1 μm CMOS	0.9	17%	30	-110@1MHz
[33]	0.35 μm CMOS	1.8	18%	50	-140@3MHz
[35]	0.5 μm BiCMOS	4.3-5	14.6%	19.8	-115@2MHz
[36]	65 nm CMOS	3.2-7.3	67%	7.2-24	-120∼-135@1MHz
[37] /This Work	0.18 μm BiCMOS	8.7-13.8	45.3%	14.4-32.4	-86.8@1MHz, -110@10MHz

of the single-end output is about -86.8 dBc/Hz at 1 MHz offset and 110 dBc/Hz at 10 MHz offset with a 11.02 GHz quadrature output. The phase noise FOM of this transformer-coupled QCCO is -154 dBc/Hz.

Chapter 7

Summary and Future Work

7.1 Summary of Original Work

This dissertation presents detailed design procedure of ultrahigh speed DDS. The main target is to achieve microwave range speed and high resolution performance as well as keep moderate power consumption. A transformer-coupled frequency variable oscillator is designed to provide the clock frequency of the DDS system.

Three DDSs with different architectures have been implemented in 0.13 μm SiGe BiCMOS technology. The sine-weighted DAC brings in the system additional spurs to the final DDS output spectra. The major problem is the non-ideal nature of a sine-weighted DAC is more noticeable than that of a linear DAC. The detailed analysis shows that the DAC associated spurs coming from two major sources. One is the static performance of a DAC, such as DNL or INL. The other is the dynamic performance of a DAC, which is input code dependent and clock frequency dependent. To make the whole situation more complicate, the noise coming from digital block will also inject into the substrate and power supply. To suppress the crosstalk and power and ground bouncing, more unknown variables need to be taken into account.

7.2 Possible Future Directions

The main difficulty comes from good model to accurately reflect the real natures of a working DDS. Though there are some theoretical works appeared in this field, there is still something to be desired. Especially, to predicate the dynamic performance of the DAC and the DDS with good accuracy, up to now hardly anyone can give satisfied results. The

following works are intend to make further study of modeling of the DDS, provide some new thoughts into this problem and hopefully find alternative solution to answer the questions when designing a DDS.

Bibliography

[1] **Xueyang Geng, F. F. Dai, J. D. Irwin, and R. C. Jaeger, "A 9-bit 2.9 GHz direct digital synthesizer MMIC with direct digital frequency and phase modulations," in *IEEE MTT-S International Microwave Symposium Digest*, June 2009, pp. 1125–1128.**

[2] **Xueyang Geng, F. F. Dai, J. D. Irwin, and R. C. Jaeger, "A 24-bit 5.0 GHz direct digital synthesizer MMIC with direct digital modulations and spur randomization," in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2009 IEEE*, June 2009, pp. 419–422.**

[3] J. M. P. Langlois and D. Al-Khalili, "Phase to sinusoid amplitude conversion techniques for direct digital frequency synthesis," in *IEE Proc. Circuits Devices Syst.*, Dec. 2004, pp. 519–528.

[4] D. A. Sunderland, R. A. Strauch, S. S. Wharfield, H. T. Peterson, and C. R. Cole, "CMOS/SOS frequency synthesizer LSI circuit for spread spectrum communications," *IEEE J. of Solid-State Circuits*, vol. sc-19, no. 4, pp. 497–506, Aug. 1984.

[5] H. T. Nicholas, III, H. Samueli, and B. Kim, "The optimization of direct digital frequency synthesizer performance in the presence of finite word length effects," in *Proc. of the 42nd Annual Frequency Control Symposium*, 1988, pp. 257–263.

[6] C. C. Wang, Y. L. Tseng, H. C. She, C. C. Li, and R. Hu, "A 13-bit resolution ROM-less direct digital frequency synthesizer based on a trigeometric quadruple angle formula," *IEEE Trans. on Very Large Scale Integration Systems*, vol. 12, no. 9, pp. 895–900, Sept. 2004.

[7] D. De Caro, N. Petra, and A. G. M. Strollo, "Reducing lookup-table size in direct digital frequency synthesizers using optimized multipartite table method," *IEEE Trans. on Circuits and Systems II*, vol. 55, no. 7, pp. 2116–2127, Aug. 2008.

[8] **Xueyang Geng, X. Yu, F. F. Dai, J. D. Irwin, and R. C. Jaeger, "An 11-bit 8.6 GHz direct digital synthesizer MMIC with 10-bit segmented nonlinear DAC," in *34th European Solid-State Circuits Conference (ESSCIRC)*, Sept. 2008, pp. 362–365.**

[9] **Xueyang Geng, F. F. Dai, J. D. Irwin, and R. C. Jaeger, "An 11-bit 8.6 GHz direct digital synthesizer MMIC with 10-bit segmented sine-weighted DAC," *IEEE J. of Solid-State Circuits*, vol. 45, no. 2, pp. 300–313, Feb. 2010.**

[10] P. Lacomme, J.-P. Hardange, J.-C. Marchais, and E. Normant, *Air and Spaceborne Radar System: An Introduction*, ISBN 1-891121-13-8. William Andrew Publishing, LLC, 2001.

[11] J. R. Klauder, A. C. Price, S. Darlington, and W. J. Albersheim, "The theory and design of chirp radars," *The Bell System Technical Journal*, vol. 39, no. 4, pp. 745–808, 1960.

[12] M. Skolnik, *Radar handbook*, 3rd ed., ISBN-10: 0071485473, ISBN-13: 978-0071485470, McGraw-Hill Professional, 2008.

[13] F. F. Dai, W. Ni, Y. Shi, and R. C. Jaeger, "A direct digital frequency synthesizer with fourth-order phase domain $\Delta\Sigma$ noise shaper and 12-bit current steering DAC," *IEEE J. Solid-State Circuits*, vol. 41, no. 4, pp. 839–850, April 2006.

[14] A. Van den Bosch, M. Steyaert, and W. Sansen, *Static and Dynamic Performance Limitations for High Speed D/A converters*, ISBN 1402077610, Kluwer Academic Publishers, chapter 5.

[15] J. J. Wikner and N. Tan, "Modeling of CMOS digital-to-analog converters for telecommunication," *IEEE Trans. on Circuit and Systems II: Analog and Digital Signal Processing*, vol. 46, no. 5, pp. 489–499, May 1999.

[16] **W. Ni, Xueyang Geng, Y. Shi, and F. Dai, "A 12-bit 300 MHz CMOS DAC for high-speed system applications," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, Kos, Greece, May 2006, pp. 1402–1405.**

[17] J. Jiang and E. K. F. Lee, "A low-power segmented nonlinear DAC-based direct digital frequency synthesizer," *IEEE J. Solid-State Circuits*, vol. 37, no. 10, pp. 1326–1330, Oct. 2002.

[18] A. Gutierrez-Aitken, J. Matsui, E. Kaneshiro, B. Oyama, A. Oki, and D. Streit, "Ultra high speed direct digital synthesizer using InP DHBT technology," *IEEE J. of Solid-State Circuits*, vol. 37, no. 9, pp. 1115–1121, Sept. 2002.

[19] S. E. Turner and D. E. Kotecki, "Direct digital synthesizer with ROM-less architecture at 13-GHz clock frequency in InP DHBT technology," *IEEE Microwave and Wireless Components Letters*, vol. 16, no. 5, pp. 296–298, May 2006.

[20] S. E. Turner and D. E. Kotecki, "Direct digital synthesizer with sine-weighted DAC at 32-GHz clock frequency in InP DHBT technology," *IEEE J. of Solid-State Circuits*, vol. 41, no. 10, pp. 2284–2290, Oct. 2006.

[21] X. Yu, F. F. Dai, J. D. Irwin, and R. C. Jaeger, "A 12 GHz 1.9 W direct digital synthesizer RFIC implemented in 0.18μm SiGe BiCMOS technology," *IEEE J. of Solid-State Circuits*, vol. 43, no. 6, pp. 1384–1393, June 2008.

[22] X. Yu, F. F. Dai, J. D. Irwin, and R. C. Jaeger, "A 9-bit quadrature direct digital synthesizer implemented in 0.18-μm SiGe BiCMOS technology," *IEEE Trans. on Microwave Theory and Technique*, vol. 56, no. 5, pp. 1257–1266, May 2008.

[23] A. Van den Bosch, M. A. F. Borremans, M. S. J. Steyaert, and W. Sansen, "A 10-bit 1-Gsample/s Nyquist current-steering CMOS D/A converter," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 315–324, March 2001.

[24] K. R. Elliott, "Direct digital synthesis for enabling next generation RF systems," in *IEEE Compound Semiconductor Integrated Circuit Symposium (CSIC)*, Nov. 2005, pp. 125–128.

[25] P. G. A. Jespers, *Integrated Converters: D to A and A to D Architectures, Analysis and Simulation*, ISBN 0198564465, Oxford University Press.

[26] R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE J. on Selected Areas in Communications*, vol. 17, no. 4, pp. 539–550, April 1999.

[27] S. E. Turner, R. T. Chan, and J. T. Feng, "ROM-based direct digital synthesizer at 24 GHz clock frequency in InP DHBT technology," *IEEE Microwave and Wireless Components Letters*, vol. 18, no. 8, pp. 566–568, Aug. 2008.

[28] S. Thuries, E. Tournier, A. Cathelin, S. Godet, and J. Graffeuil, "A 6-GHz low-power BiCMOS SiGe:C 0.25 μm direct digital synthesizer," *IEEE Microwave and Wireless Components Letters*, vol. 16, no. 1, pp. 46–48, Jan 2008.

[29] **Xueyang Geng, F. F. Dai, J. D. Irwin, and R. C. Jaeger, "A 24-bit 5.0 GHz direct digital synthesizer RFIC with direct digital modulations in 0.13 μm SiGe BiCMOS Technology," *IEEE J. of Solid-State Circuits*, vol. 45, no. 5, pp. 944–954, May 2010.**

[30] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits, A Design Perspective (Second Edition)*, 2nd ed., ISBN 0-13-597444-5, Pearson, Inc, 2003.

[31] *AD9912 datasheet, Analog Devices.*

[32] A. Rofougaran, J. Rael, M. Rofougaran, , and A. Abidi, "A 900 MHz CMOS LC-oscillator with quadrature outputs," in *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, 1996, pp. 392–393.

[33] P. Andreani, A. Bonfanti, L. Romano, , and C. Samori, "Analysis and design of a 1.8-GHz CMOS LC quadrature VCO," *IEEE J. of Solid-State Circuits*, vol. 37, no. 12, pp. 1737–1747, Dec. 2002.

[34] P. Andreani and X. Wang, "On the phase-noise and phase error performance of multi-phase LC CMOS VCOs," *IEEE J. of Solid-State Circuits (JSSC)*, vol. 39, no. 11, pp. 1883–1893, Nov. 2004.

[35] V. Kakani, F. Dai, , and R. C. Jaeger, "A 5GHz BiCMOS quadrature LC VCO with wide tuning range," in *IEEE Bipolar/BiCMOS Circuits and Technology meeting (BCTM)*, 2006, pp. 138–141.

[36] G. Cusmai, M. Repossi, G. Albasini, A. Mazzanti, , and F. Svelto, "A magnetically tuned quadrature oscillator," *IEEE J. of Solid-State Circuits (JSSC)*, vol. 42, no. 12, pp. 2870–2877, Dec. 2007.

[37] **Xueyang Geng and F. F. Dai, "An 8.7-13.8 GHz transformer-coupled varactor-less quadrature current -controlled oscillator," in *the 2009 Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), IEEE*, 2009, pp. 63–66.**

[38] **Xueyang Geng and F. F. Dai, "An X-band transformer-coupled varactor-less quadrature current-controlled oscillator in 0.18 μm SiGe BiCMOS technology," Invited to submit to *IEEE J. of Solid-State Circuits (JSSC), BCTM Special Issue*, vol. 45, no. 9, Sep 2010.**

[39] L. Romano, S. Levantino, A. Bonfanti, C. Samori, , and A. L. Lacaita, "Phase noise and accuracy in quadrature oscillators," in *in IEEE International Symposium on Circuits and Systems (ISCAS)*, 2006, pp. 161–164.

[40] A. Mazzanti, F. Svelto, , and P. Andreani, "On the amplitude and phase errors of the quadrature LC-tank CMOS oscillators," *IEEE J. of Solid-State Circuits (JSSC)*, vol. 41, no. 6, pp. 1305–1313, Jun. 2006.

[41] D. B. Leeson, "A simple model of feedback oscillator noise spectrum," in *in Proc. IEEE*, 1966, pp. 329–330.

[42] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. of Solid-State Circuits (JSSC)*, vol. 33, no. 2, pp. 179–194, Feb. 1998.

[43] T. H. Lee and A. Hajimiri, "Oscillator phase noise: A tutorial," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 35, no. 3, pp. 326–336, Mar. 2000.

[44] A. Andreani, "A time-variant analysis of the $1/f^2$ phase noise in CMOS parallel LC-tank quadrature oscillators," *IEEE Trans. Circuits Syst. I*, vol. 53, no. 8, pp. 1749–1770, Aug. 2006.

[45] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits, 2nd ed.*, Cambridge University Press.

[46] S. S. Mohan, M. D. Hershenson, S. P. Boyd, , and T. H. Lee, "Simple accurate expressions for planar spiral inductances," *IEEE J. of Solid-State Circuits (JSSC)*, vol. 34, pp. 1419–1424, 1999.

[47] J. Rogers and C. Plett, *Radio Frequency Integrated Circuit Design*, Artech House.

[48] P. Kinget, *Integrated GHz Voltage Controlled Oscillators*, New York: Kluwer Academic Publisher, 1999.