Development of Multi Chip Modules for Extreme Environments

by

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Abstract

Multi chip module technology offers numerous advantages such as reduced signal delays, higher performance, lower power consumption, smaller space, its simplification. In this paper, the fabrication process of multi chip module for extreme environments will be presented including 2 IC interconnection techniques, flip chip and wire bond. The chips has been subjected to extreme thermal cycles, from -180°C to 125°C, for a reliability test. Resistance measurements were also performed at room temperature after thermal shock cycles. Finally, conclusions are made from the results.

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Chapter 1

Introduction

The extreme environmental conditions on the surfaces of the Moon and Mars are exceptionally harsh with the worst case from -180°C to 125°C. These extremes need thermally protective electronic warm boxes to protect the electronics. This leads to increased launch weight, system complexity, lack of modularity, degradation in system performance and reliability. Now, if a System-In-Package operates correctly in an earth-like climate in space, it brings about huge advantages. This paper focuses on a multi chip module process; developments including flip chip and wire bond IC interconnection techniques for extreme environments.

A single chip package was commonly used in a variety of applications in the past, but MCM (Multi Chip Module) technology is widely accepted now. MCM is a hybrid manufacturing technique for multiple IC (Integrated Circuits) chips as a single IC. The basic concept of MCM is to reduce the space, decrease the interconnection-delays between the paths on the different chips. Therefore, it has higher performance results from reduced signal delays between chips, improved signal quality, lower power supply needed because of shorter interconnect lengths, reduced weight, much higher functionality in a smaller space, and simplification of complexity and reduced number of external components.

There are three types of MCMs; MCM-C, MCM-D, and MCM-L. It is based on substrate selection. An MCM-C uses a ceramic substrate. MCM-D technology uses deposited dielectric [1].

There are two types of IC interconnection solutions, flip chip and wire bond. The choice between flip chip and wire bond is determined by production cost, packaged device performance, and overall size. Flip chip is called Direct Chip Attach (DCA), because the chip is directly attached to the substrate. This means the chip is assembled face down onto the board without wire bonding.

Even though flip chip is not a new technology, it is becoming popular because it has several advantages. Since IBM introduced flip chip technology in the 1960s for their mainframe computers, it has been widely used in various engineering fields [2]. Today it is applied in most electronic watches and increasingly in cellular phones, pagers, LCD and high speed microprocessors. This technology gives several advantages including smaller size, higher performance, lower cost, and flexibility. However, it has also several disadvantages as well; such as difficulty in the testing of bare dies, limited availability of bumped dies, fine pitch substrates, limited repair possibility, and the difficult handling of bare chips. Wire bonding is another semiconductor device fabrication method to make electrical interconnects. The difference with Flip chip is that each bond is connected individually. The biggest advantages of wire bonding are its process flexibility and the sheer quantity of wire bonders. As a result, it is a mature technology in which the production process is thoroughly researched. In addition, wire bonding is very flexible compared to flip chip. If the die size changes, it can be accommodated without additional costs as well as tighter control of wire length. Wire bonding also has several disadvantages which are its larger size, higher cost and increase of inductance and capacitance of the connection.

The goal of this thesis is to develop Multi-Chip-Module technology with high reliability in extreme environments in both high and low temperature. A spacecraft flying in space is faced with harsh surroundings. Along with temperature, the atmosphere is totally different from the earth. Therefore, special requirements are necessary for chip interconnections used in packaging of semiconductor devices. The process is based on thin copper/polyimide substrate technology to build electronics capable of operating in extreme environments, without the need for warming or cooling, to maintain an earth-like environment. First, it provides a background of flip chip, wire bond and a multi chip module with their basic architectures. In Chapter 3, the processes of flip chip and wire bond are presented which is satisfied in these extreme conditions. In Chapter 4 the process of MCM is presented which is satisfied in these extreme conditions. Then several tests are implemented with extremely high temperature and low temperature in chapter 5. It demonstrates the results as well as a discussion. Finally, it comes to a conclusion about the research.

Chapter 2

Potential Reliability Issues

A Thermo-mechanical reliability issue of chip packaging is a major concern when the assemblies are exposed to harsh environments like space. There are several main potential problems such as the coefficient of thermal expansion (CTE), thermal stress and cracks.

The coefficient of thermal expansion (CTE) is a very basic physical property which has considerable importance in mechanical and structural design applications of a material. CTE is defined as relative increase in length per unit temperature rise. The stored energy typically expands in response to temperature change [3]. This dimensional response is called coefficient of thermal expansion (CTE). As a component of electronic packages is comprised of dissimilar materials, the operation reliability issues are often present due to the CTE mismatch between these materials. If the CTEs of the substrate and the packages are different, they will expand or contract as the temperature changes. This CTE mismatch causes serious problems. It will stress the joint thus, the solder joint may be fractured. In addition, mechanical stresses usually happen at every stage of fabrication with a CTE mismatch. These stresses may cause degradation of device characteristics, reliability of the assembled components, and the power dissipation of the circuit. Therefore, it is key to match CTE between different layers.

One severe limitation on the reliability issues of present electronics is the stress caused by CTE. Typical IC packages are made by a variety of materials which have different CTEs. If one of them has unique CTE compared with the other materials, it leads to thermal stresses. It is recommended to solve stresses at an early stage of semiconductor manufacturing. As a semiconductor wafer undergoes fabrication processes, it is stressed due to the coefficient of thermal expansion mismatches between the silicon substrate and the deposited thin film layers. Therefore, it may

cause the severe problems; quality, reliability of the assembled components, and deformation between the chip and substrate[4]. Such stresses can be increased due to several reasons such as CTE mismatches, geometrical discontinuities, cyclical and random thermal loadings, and handling during assemblies operations including wafer preparation, oxidation, diffusion, metallization, die and wire bonding, encapsulation, and curing [5]. The amount of stress is normally proportional to the CTE mismatch and the polymer film thickness. The polymer tends to be delaminated from the substrate with a growing stress [6].

The occurrence of microcracks is also a potential reliability problem because the cracks are normally time dependent, which means they grow in response to thermal cycling. In most cases, microcracks which are not quickly detectable can also occur between, or within, individual grains of brittle materials. The microcracks are usually observed at the edges of the chip and then propagate into the entire chip [7]. Optimization of the fabrication process could have an effect on minimizing it. Several guide lines have been proposed to avoid high stress such as low CTE with low CTE mismatch, optimized curing processes, and prevention of moisture absorption [8], [9], [10]. Package cracking, wire cracking, thin film cracking on the die, and thermal shock cycle tests are also associated issues that need to be considered [11], [12].

The substrate plays a crucial role in ensuring the electrical, thermal, and mechanical reliability of electronic assemblies. It is quite important to have an intimate CTE between die to substrate and substrate to package. Otherwise, it incurs huge stresses on the edge of the corner due to the CTE mismatch. If the CTE of the test die and package increase with decreasing temperature, substrate should increase with decreasing temperature and then at last it is condiderable. Thermally induced strains lead to a severe problem in their reliability under these conditions. Thus, material selection can be critical. Ceramic substrate was used for wire bond and silicon substrate was used for flip chip.

Chapter 3

Two Possible Solutions for MCM

Two possible interconnect solutions for MCM will be discussed with respect to mechanical and electrical performance. Because of CTE mismatch, thermal strains, stresses, and cracks will occur at the both chip to substrate interconnection and substrate to package interconnection. The initial concept is to match the coefficient of thermal expansion (CTE) of the package. Both Si and AlN substrates were used for flip chip and wire bond. The temperature range used to study the stress in flip chip and wire bond from CTE mismatches was from -180°C to 125°C.

Devices operating under high power conditions may be exposed to high voltages, and so high voltage breakdown may occur between adjacent electrical connections. To prevent this, an effective dielectric passivation layer must be applied to ensure reliable package operation [13]. Introduced interconnect substrate technology was made of thin film copper and polyimide (HD Microsystems, PI-2611 with CTE of 3ppm/°C). Polyimides are the most commonly used material for flexible, high-density interconnection circuit applications. Polyimide films are amber in color and highly transparent, being formed by the condensation reactions of aromatic dianhydrides with aliphatic or aromatic diamines. They belong to the family of high temperature thermosetting polymers originally developed by the DuPont Company, and have been mass produced since 1955. This stiff structure exhibits an exceptional combination of high thermal stability, a very low CTE, high heat resistance, excellent dielectric properties (2.9 of dielectric constant), and relatively low moisture uptake (0.5%) compared to most other polymeric materials.

3.1 Filp Chip Solution

An underfill encapsulation, shown in figure 3.1, is normally used for the flip chip die assemble process to minimize the solder joint strains and to improve the reliability. A polymer material is

usually used to fill in the space between the die and the substrate. Epoxies are the primary material used for an underfill because it has great storage stability, long-established safety, wide availability, and high versatility. However, an underfill with epoxy was not applied for this flip chip process because epoxy becomes brittle at extremely low temperature, while indium remains malleable at the same temperature[15]. An indium was used for substrate attachment to package and solder bump was used for flip chip die to substrate attachment. Silicon substrate was chosen for flip chip because it is well matched to Si die without underfill.

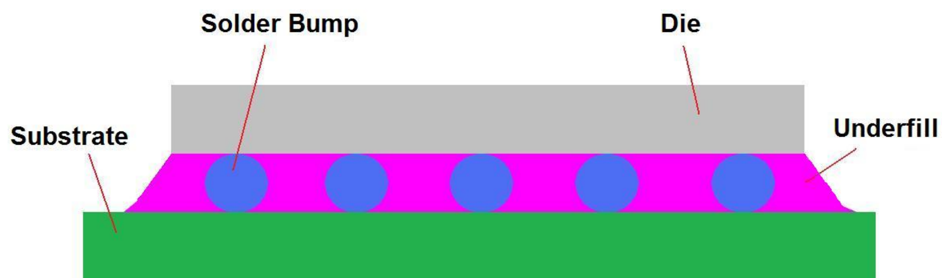


Figure 3.1: Flip chip structure with underfill

Flip chip was fabricated on 4-inch diameter Si substrates. The Si substrate provides a perfect CTE match to the Si flip chip die. An oxide insulating layer of thickness 6000Å was grown on the Si substrate in an oxidation furnace. The oxidation was performed in the presence of oxygen and hydrogen gases at 1050°C.

3.1.1 Coating of Polyimide

The first step is to make a coating of polyimide on the surface. Prior to the application of polyimide, the silicon wafer was placed in a dehydration bake oven at 120°C for 30 minutes. For non-polyimide surfaces - a thin layer of adhesion promoter was applied by spinning VM652 (HD Microsystems) onto the surface at 5000 rpm for 30 seconds to improve the adhesion [16], and to avoid silicon delamination or peel off. The layer was soft-baked at 120°C for 60 seconds. And then polyimide PI2611 was spun on the surface at 500 rpm for 5 seconds with an acceleration speed of 250 rpm, then spun at 3000 rpm for 30 seconds with an acceleration speed of 1000 rpm.

It was then soft-baked at 120°C for 5 minutes in the dehydration bake oven. The next step was a ”low stress” curing process. The curing process converts the polyamic acid into a fully aromatic with high temperatures to completely imidize the film [17]. It can be done in the programmable YES oven (model 450-PB8-2P-CP). After the wafer was placed in a programmable nitrogen oven at ambient temperature, the process began by purging the oven with N2. Table 3.1 is the process used to cure the polyimide layer under low stress using YES oven.

After the curing process, E-beam process was applied to deposit thin layers of metals to form the electrodes, conducting traces, and connection pads. It was selected with Ion Clean (5 minutes), Chrome (250Å), and Copper (2000Å) as the seed layer deposition.

Table 3.1: YES Oven Procedure

STEP	PROCESS
Step1	Target Temperature: 90 Ramp rate: 1/Min Curing time:30 min
Step2	Target Temperature: 150 Ramp rate: 1/Min Curing time:30 min
Step3	Target Temperature: 350 Ramp rate: 2/Min Curing time:60 min
Step4	The nitrogen oven is then ramped down to ambient temperature at a rate of 2°C/min

3.1.2 Pattern the Seed Layer

The second step is to make the seed layer pattern. The silicon wafer was placed in the dehydration bake oven at 120°C for 20 minutes ahead of the application of photoresist. HMDS was then evaporated on the surface of the silicon wafer for 5 minutes to improve the photoresist adhesion. A layer of thick photoresist, AZ9245 (AZ Electronic Materials), was used for patterning. It was spun on the surface at a speed of 1700 rpm for 5 seconds with an acceleration speed of 500 rpm and spun at 2700 rpm for 30 seconds with an acceleration speed of 1000 rpm. It was then soft-baked

at 110°C for 90 seconds. After that, the silicon wafer was exposed (Mask Alligner MA6/BA6) to make a pattern with 1 cycle for 60 seconds. Exposure was performed immediately after soft bake, as soon as the wafer had cooled to room temperature. It was then developed with AZ400K positive photoresist developer for 5 minutes which was in the ratio of 1:2.5 with deionized water. Then, a plasma descum with Matrix (300W, 20sec) was performed to remove any residual photoresist. After completing this step, photoresist thickness was about 4.5 um. The mask layout is shown in figure 3.2.

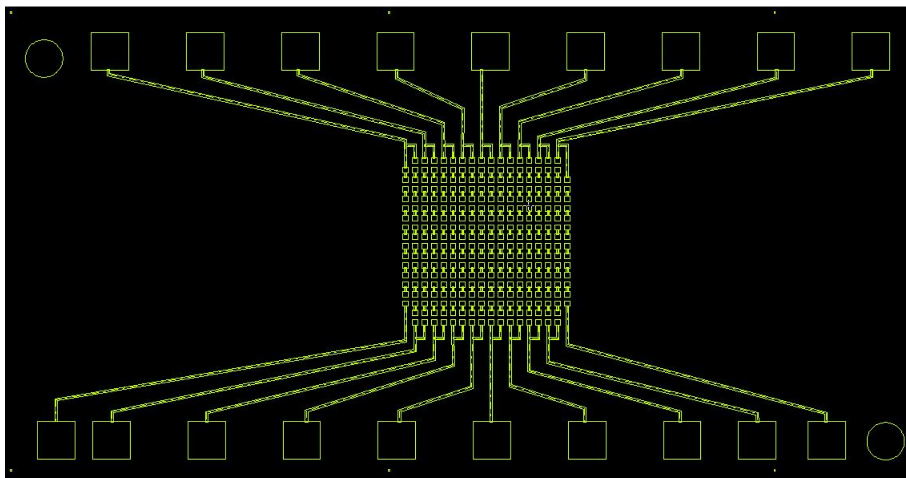


Figure 3.2: Flip chip mask1

3.1.3 Plating

The next step is metallization. The electroplating setup is shown in Figure 3.3. First, copper (2.5um, 12mA) was plated. Nickel was then plated (0.5um, 10mA, 35-40°C). Finally, Au was plated (0.5um, 6mA, 35-40°C). The Nickel layer served as a thermal barrier; It was used to improve the adhesion to the resistor material. As a top layer, Au usually protects it from oxidation and corrosion to the Ni layer [17]. Plating was very slowly done in order to obtain a smooth, even coating of the plated metal. During the process, it should have no interval, especially between nickel plating and gold plating. It was observed to be contaminated if interval existed between nickel and Au plating. As a result, it was not evenly plated and thus, it was peeling off. To avoid unexpected failure, orostrike C RTU was suggested. After finishing nickel plating, it gave the wafer a short

soak in orostrike C RTU solution for 30 seconds and then plated Au immediately using 434 HS RTU Gold without water cleaning. After plating, positive photoresist was stripped by acetone and was cleaned by methanol and water. Then the seed layers were etched by Cu etchant, Potassium Permanganate.

Table 3.2: Plating Mixing Formula

SOLUTION	QUANTITY
Copper	Microfab SC Makeup 1L Microfab SC MD 8mL/L Microfab 10 70/30 2mL/L
Nickel	Nickel Sulfamate RTV 1L Nickel Stress Reducer 8mL/L
Gold	RTV HS434 - Straight
Polyimide adhesion	Prepoly is done to coat polyimide on polyimide Adhesion promoter for polyimide on oxide

Table 3.3: Cr Etching Mixing Formula

SOLUTION
80 gm KmnO4 (Potassium Permanganate) 20 gm NaOH (Sodium Hydroxide) 1 L H2O

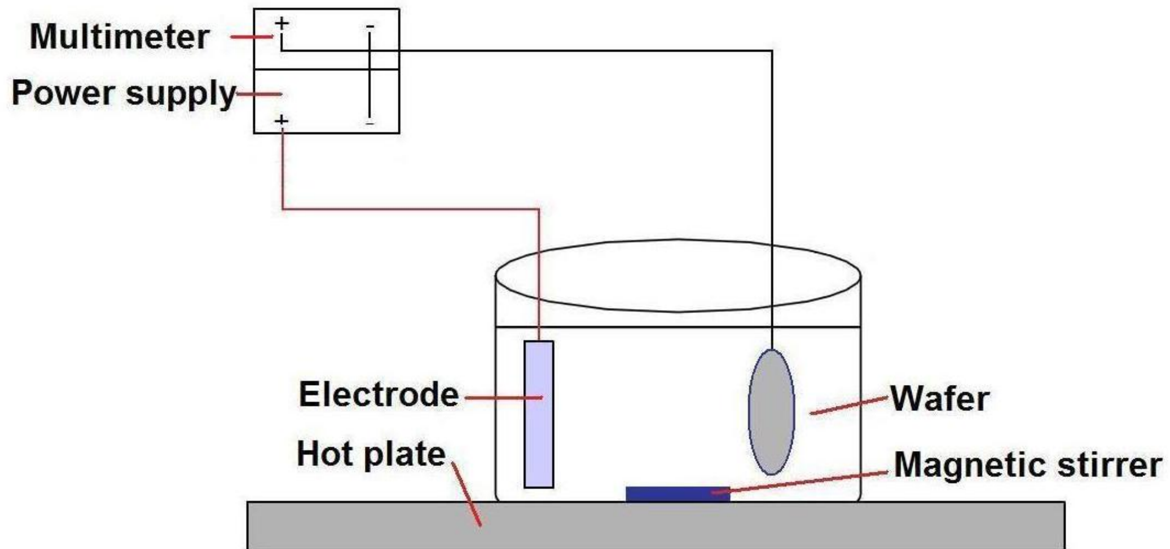


Figure 3.3: Cu, Ni, Au electroplating setup

3.1.4 Coating of Polyimide

The following step is to make the second coating of polyimide on the surface. Prior to the application of polyimide, the silicon wafer was placed in a dehydration bake oven at 120°C for 30 minutes. Openings were then etched by AOE Nitrogen for 30 seconds. After that, a thin layer of adhesion promoter was formed by spinning VM652 (HD Microsystems) onto the surface at 3000 rpm for 30 seconds. Next, the layer was soft-baked at 120°C for 60 seconds. And then polyimide PI2611 was spun on the surface at 500 rpm for 5 seconds with an acceleration speed of 250 rpm then, spun at 3000 rpm for 30 seconds with an acceleration speed of 1000 rpm. It was then soft-baked at 120°C for 5 minutes in the dehydration bake oven. Then, it was placed in a programmable nitrogen YES oven (model 450-PB8-2P-CP) at ambient temperature for a ”low stress” curing process. Table 3.1 shows the curing process under low stress using YES oven.

3.1.5 Photoresist Layer 1

The silicon wafer was placed in the dehydration bake oven at 120°C for 20 minutes ahead of the application of photoresist. HMDS was then evaporated on the surface of the silicon wafer for 5 minutes to improve the photoresist adhesion. Positive photoresist AZ4620 was then spun on

the surface at a speed of 1000 rpm for 30 seconds with an acceleration speed of 250 rpm and soft-baked at 110°C for 90 seconds. After that, it was immediately exposed (Mask Alligner MA6/BA6) to make a pattern with 3 cycles for 90 seconds as soon as the wafer had cooled down to room temperature. It was then developed with AZ400K positive photoresist developer for 4 minutes which was in the ratio of 1:2.5 with deionized water. Next, a plasma descum with Matrix (300W, 20sec) was performed to remove any residual photoresist. After completing this step, photoresist thickness is about 20 um. The mask layout is shown in figure 3.4.

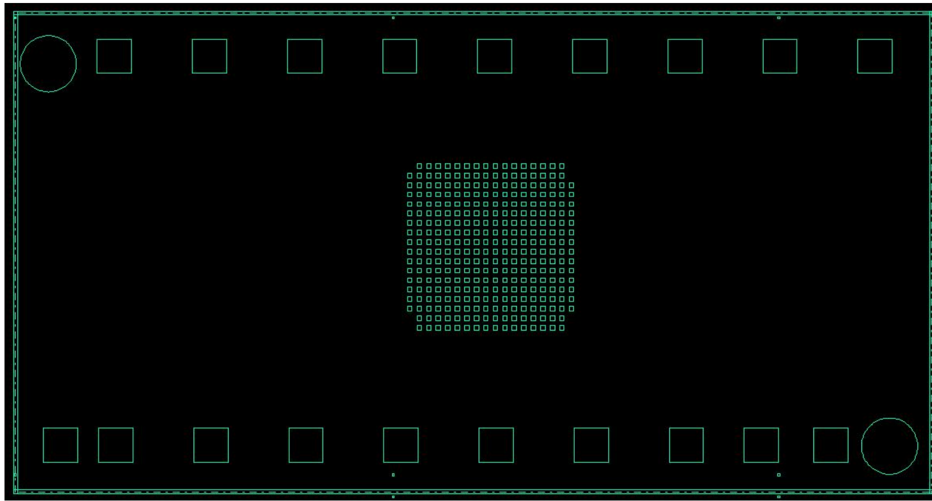


Figure 3.4: Flip chip mask2

3.1.6 Polyimide Etching

The last step is polyimide etching using A.O.E. The etching process was P-imide2 which contains ICP-2min, Polyetch1-3min, Polyetch2-4min.

3.1.7 Backside Metal Deposition

It began with E-beam deposition process. It was selected with Titanium (500Å) and Nickel (800Å) Gold (1200Å) as backside metal deposition [14]. Average shear strength with Ti/Ni/Au backside metal deposition is shown in figure 3.5. Then, the silicon wafer is diced to separate all the individual probe arrays.

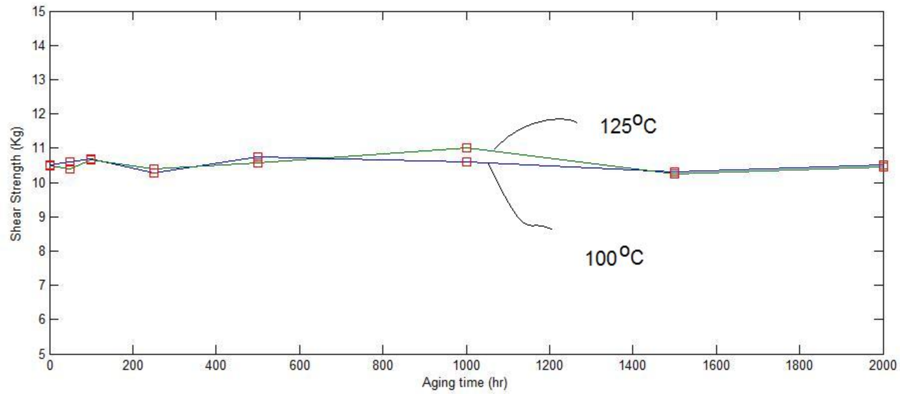


Figure 3.5: Die shear strength with backside metal deposition

3.2 Wire Bond Solution

Ceramic substrates (AlN) were selected for wire bond solution because they provide an intermediate CTE match between the die (si) and the package ($Al_2 0_3$). Indium was used for Die and Substrate Attach. Indium is known that it deforms viscoplastically with over than 300°C operating temperature range [15]. The attached die were thermosonically wire bonded using an automatic wire bonder and 25.4 m diameter Au wire. The stage temperature was 125°C. It is also used for substrate to package electrical interconnection.

An oxide insulating layer of thickness 6000Å was grown on the ceramic substrate in an oxidation furnace. The oxidation was performed in the presence of oxygen and hydrogen gases at 1050°C . The general concept of ceramic substrates is that they have the same CTE with ceramic package. That is, they do not face any problems related to any CTE mismatch. So, ceramic substrates are widely used in hybrid applications.

3.2.1 Seed Layer Deposition

Wire bond process began with E-beam deposition process. It was selected with Titanium (250Å) and Copper (2000Å) as the seed layer deposition

3.2.2 Pattern the Seed Layer

The second step is to make the seed layer pattern. The silicon wafer is placed in the dehydration bake oven at 120°C for 20 minutes before the application of photoresist. HMDS was then evaporated on the surface of the silicon wafer for 5 minutes to improve the photoresist adhesion. A layer of thick photoresist, AZ9245 (AZ Electronic Materials), was used for patterning. It was spun on the surface at a speed of 1700 rpm for 5 seconds with an acceleration speed of 500 rpm and spun at 3000 rpm for 30 seconds with an acceleration speed of 1000 rpm. It was then soft-baked at 110°C for 90 seconds. After that, the silicon wafer was exposed (Mask Alligner MA6/BA6) to make a pattern with 1 cycle for 60 seconds. Exposure was performed immediately after soft bake, as soon as the wafer had cooled to room temperature. It was then developed with AZ400K positive photoresist developer for 5 minutes which was in the ratio of 1:2.5 with deionized water. Then, a plasma descum with Matrix (300W, 20sec) was performed to remove any residual photoresist. After completing this step, photoresist thickness should be about 4.5 um. The mask layout is shown in figure 3.6.

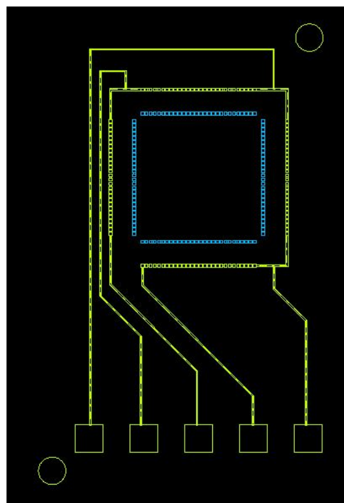


Figure 3.6: Wire bond mask1

3.2.3 Plating

The next step is metallization. First, copper (1.25um, 12mA) was plated. Nickel was then plated (1.0um, 10mA, 35-40°C). Then, Au was plated (1.5um, 6mA, 35-40°C). The Nickel layer served as a thermal barrier; It was used to improve the adhesion to the resistor material. After plating, positive photoresist was stripped by acetone and was cleaned by methanol and water. Then the seed layers were etched by Cu etchant, Potassium Permanganate.

3.2.4 Coating of Polyimide

This step is to create a coating of polyimide on the surface. Prior to the application of polyimide, the silicon wafer was placed in a dehydration bake oven at 120°C for 30 minutes. For non-polyimide surfaces - a thin layer of adhesion promoter was applied by spinning VM652 (HD Microsystems) onto the surface at 5000 rpm for 30 seconds to improve the adhesion [16], and to avoid silicon delamination or peel off. Next, the layer was soft-baked at 120°C for 60 seconds. Then, polyimide PI2611 was spun on the surface at 500 rpm for 5 seconds with an acceleration speed of 250 rpm, then spun at 3000 rpm for 30 seconds with an acceleration speed of 1000 rpm. It was then soft-baked at 120°C for 5 minutes in the dehydration bake oven. The next step was a ”low stress” curing process in the programmable YES oven (model 450-PB8-2P-CP). The wafer was placed in a programmable nitrogen oven at ambient temperature and the process began by purging the oven with N2. Table 3.1 is the process used to cure the polyimide layer under low stress using the YES oven.

3.2.5 Etch Openings in Polyimide

And then, it made each opening in polyimide. The silicon wafer was placed in the dehydration bake oven at 120°C for 20 minutes before the application of photoresist. HMDS was then evaporated on the surface of the silicon wafer for 5 minutes to improve the photoresist adhesion. A layer of thick photoresist, AZ4620 (AZ Electronic Materials), was used for patterning. It was spun on the surface at a speed of 1000 rpm for 30 seconds with an acceleration speed of 250 rpm. It

was then soft-baked at 110 for 90 seconds. After that, the silicon wafer was exposed with 3 cycles for 90 seconds. Exposure was performed immediately after the soft bake, as soon as the wafer had cooled to room temperature. It was then developed with AZ400K positive photoresist developer for 5 minutes which was in the ratio of 1:2.5 with deionized water. Then, a plasma descum with Matrix (300W, 20sec) was performed to remove any residual photoresist. After completing this step, photoresist thickness was about 20 um. The mask layout is shown in figure 3.7.

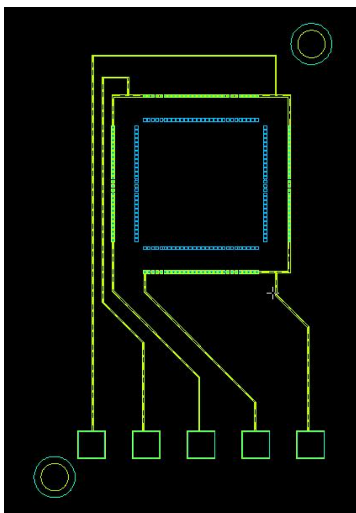


Figure 3.7: Wire bond mask2

3.2.6 Polyimide Etching

The last step is polyimide etching using A.O.E. The etching process was P-imide2 which contains ICP-2min, Polyetch1-3min, Polyetch2-4min.

3.2.7 Photoresist Layer 1

The silicon wafer was placed in the dehydration bake oven at 120°C for 20 minutes ahead of the application of photoresist. HMDS was then evaporated on the surface of the silicon wafer for 5 minutes to improve the photoresist adhesion. Positive photoresist AZ4620 was then spun on the surface at a speed of 1000 rpm for 30 seconds with an acceleration speed of 250 rpm and soft-baked at 110°C for 90 seconds. After that, it was immediately exposed (Mask Alligner MA6/BA6)

to make a pattern with 3 cycles for 90 seconds as soon as the wafer had cooled down to room temperature. It was then developed with AZ400K positive photoresist developer for 4 minutes which was in the ratio of 1:2.5 with deionized water. Then, a plasma descum with Matrix (300W, 20sec) was performed to remove any residual photoresist. After completing this step, photoresist thickness is about 20 um. The mask layout is shown in figure 3.4.

3.2.8 Backside Metal Deposition

It began with E-beam deposition process. It was selected with Titanium (500Å) and Nickel (800Å) Gold (1200Å) as backside metal deposition. Then, the ceramic wafer is diced to separate all the individual probe arrays.

3.2.9 Summary

Due to reasons which will be discussed in a later part of this paper, it was found that flip chip solution has larger inelastic stress / strain than wire bond solution since flip chip has the largest CTE mismatch between Si substrate and Al_20_3 package compared to wirebond, AlN substrate and Al_20_3 package. Moreover, wire bond solution is more suitable for multi chip module in harsh environments.

Chapter 4

Selected Optimum Solutions for Multi Chip Module Technology

As more complex IC (Integrated Circuit) designs are utilized, IC needs to be packaged more densely than before. Now MCMs are being widely used in several applications for military, space, medical, and commercial products. This chapter addresses an overview of MCM design for harsh conditions implemented in systems in package (SiP) technologies. The basic idea of the MCM is to combine multiple chips as a single chip.

It uses two different dielectric materials, BCB and Polyimide. An advanced electronic resin, BCB which is drived from B-staged bisbenzocyclobutene chemistry [18], has been developed for use as dielectrics in thin film microelectronics applications. BCB has significant advantages over the polyimide such as lower dielectric constant, a lower dissipation factor, reduced water absorption, a shorter cure time and a lower cure temperature [18], [19], [20]. However, BCB has significantly higher CTE than polyimide. That is, it is important to use a passivation film at the uppermost layer in MCM with thick polyimide. Moreover, BCB was used as dielectrics at lower layers and polyimide was used as dielectrics at higher layers. Table 4.1 shows a comparison of BCB with Polyimide.

Table 4.1: Comparison of BCB with Polyimide

Properties	BCB	Polyimide
Dielectric constant(1kHz)	2.65	2.9
CTE(ppm/°C)	42	3
Tensile strengh(MPa)	87±9	350
Modulus(GPa)	2.9±0.2	8.5
Dissipation factor	0.0008	0.002

4.1 MCM Process Procedures

This is the MCM solution using BCB and Polyimide. Figure 4.1 shows basic MCM process flows. Either BCB or Polyimide can be used as a dielectric layer.

MCM were fabricated on 4 X 4 inch AIN substrates. An oxide insulating layer of thickness 1600Åwas grown on the ceramic substrate in an oxidation furnace. The oxidation performed in the presence of oxygen and hydrogen gases at 1050°C.

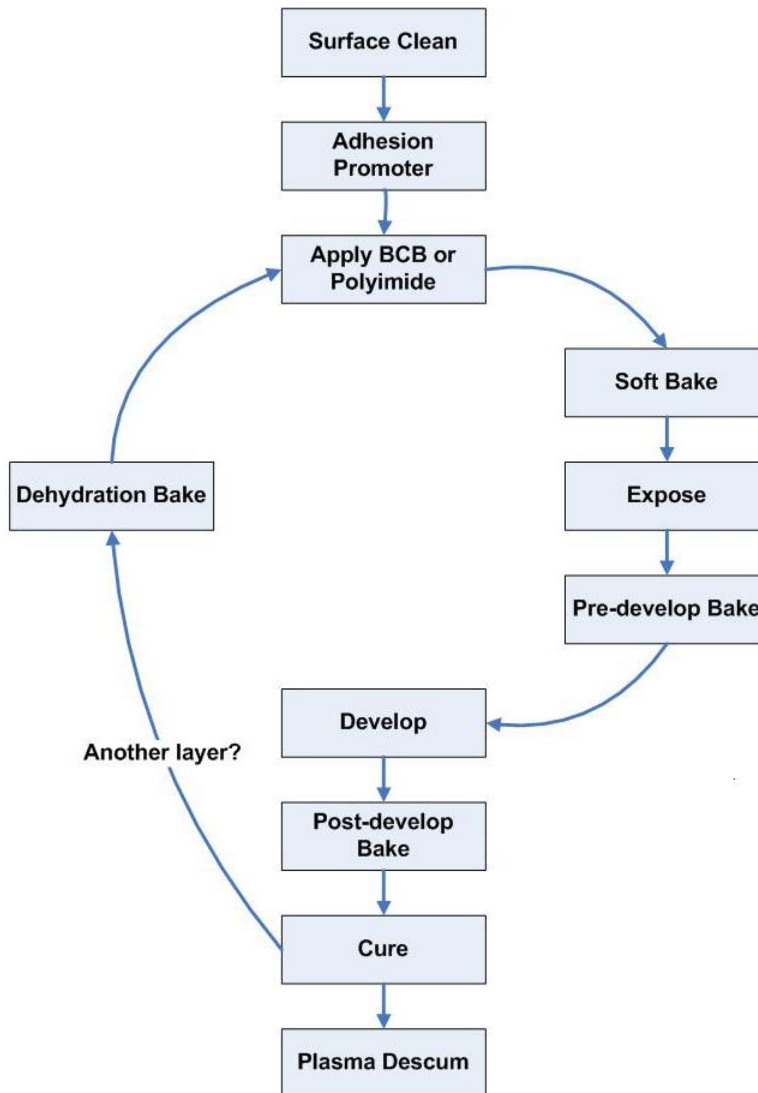


Figure 4.1: MCM process flow

4.1.1 Seed Layer Deposition

The multi Chip Module process began with E-beam deposition process with 1 minute Ion Clean. It was selected with Titanium (250Å) and Copper (2000Å) as the seed layer deposition.

4.1.2 Ground plane Patterning

The second step is to make the Ground pattern. The ceramic wafer was placed in the dehydration bake oven at 120°C for 20 minutes ahead of the application of photoresist. HMDS was then evaporated on the surface of the ceramic wafer for 5 minutes to improve the photoresist adhesion. A layer of thick photoresist, AZ9245 (AZ Electronic Materials), was used for patterning. It was spun on the surface at a speed of 1700 rpm for 5 seconds with an acceleration speed of 500 rpm and spun at 2700 rpm for 30 seconds with an acceleration speed of 1000 rpm. It was then soft-baked at 110°C for 90 seconds. After that, the ceramic wafer was exposed (Mask Alligner MA6/BA6) to make a pattern with 1 cycle for 60 seconds. Exposure was performed immediately after soft bake, as soon as the wafer had cooled to room temperature. It was then developed with AZ400K positive photoresist developer for 5 minutes which was in the ratio of 1:2.5 with deionized water. Then, a plasma descum with Matrix (300W, 20sec) was performed to remove any residual photoresist. After completing this step, photoresist thickness is about 4.5 um. The mask layout is shown in figure 4.1.

4.1.3 Plating

The next step is metallization. First, copper (2um, 26mA) was plated. Nickel was then plated (0.2um, 23mA, 35-40°C). The Nickel layer served as a thermal barrier. It was used to improve the adhesion to the resistor material. After plating, positive photoresist was stripped by acetone and was cleaned by methanol and water. Then the seed layers were etched by Cu etchant, Potassium Permanganate.

4.1.4 BCB Application

Prior to the application of BCB, the ceramic wafer was placed in a dehydration bake YES oven at 150°C. For BCB application - a thin layer of adhesion promoter was formed by spinning AP3000 onto the surface at 3000 rpm for 30 seconds to improve the adhesion to the BCB layer. Poor adhesion of ceramic materials can show up as delamination or peel off during the rest of the processing steps. The layer was soft-baked at 120°C for 60 seconds. After that, BCB was dispensed on the surface at 500 rpm for 5 seconds with an acceleration speed of 100 rpm then, spun at 500 rpm for 5 seconds. It was then spun at 5000 rpm for 10 seconds with an acceleration speed of 450 rpm then, spun at 5000 rpm for 30 seconds. Next, it was soft-baked at 60°C for 90 seconds. Then, the ceramic wafer was exposed (Mask Alligner MA6/BA6) to make a pattern with 1 cycle for 30 seconds. Then, pre-develop baked at 60°C for 5 minutes. Without the pre-develop process, the development time will increase. Next, it was then developed with DS3000 at 35°C for 2.2minutes and then, it was develop-rinse step with DS3000 at the room temperature for 2.2 minutes. Next, it was done Nitrogen-dry. When it was water cleaned, it got cracks everywhere on areas with metal underneath. After blow-drying the wafer, post-develop bake was done at 100°C for 1 minute. When inspecting wafers after bake, a lot of particles were exposed all over the surface which means cleaning was very important on them using BCB and they needed N2 blow every step. The next step was a "low stress" curing process in the programmable YES oven (model 450-PB8-2P-CP). The wafer was placed in a programmable nitrogen oven at ambient temperature and the process began by purging the oven with N2. Table 4.1 is the process used to cure the polyimide layer under low stress using YES oven.

4.1.5 2nd Layer BCB Application

Prior to the application of BCB, the ceramic wafer was placed in a dehydration bake YES oven at 150°C. And then, the layer was soft-baked at 120°C for 60 seconds. Next, BCB was dispensed on the surface at 500 rpm for 5 seconds with an acceleration speed of 100 rpm and spun at 500 rpm for 5 seconds. It was then spun at 5000 rpm for 10 seconds with an acceleration speed

Table 4.2: YES Oven Procedure

STEP	PROCESS
Step1	Target Temperature: 150 Ramp rate: 1/Min Curing time:15 min
Step2	Target Temperature: 150 Soak rate: 1/Min Curing time:15 min
Step3	Target Temperature: 210 Ramp rate: 2/Min Curing time:60 min
Step4	Target Temperature: 210 Soak rate: 2/Min Curing time:60 min
Step5	Cool down to ambient temperature at a rate of 2degree/min

of 450 rpm and then spun at 5000 rpm for 30 seconds. After this, it was then soft-baked at 60°C for 90 seconds. Then, the ceramic wafer was exposed (Mask Alligner MA6/BA6) to make a pattern with 1 cycle for 40 seconds. The next step was pre-develop bake at 60°C for 5 minutes. It was then developed with DS3000 at 35°C for 2.2minutes and then it was develop-rinse step with DS3000 at the room temperature for 2.2 minutes. After blow-drying the wafer, post-develop bake was done at 100°C for 1 minute. The next step was a ”low stress” curing process in the programmable YES oven (model 450-PB8-2P-CP). The wafer was placed in a programmable nitrogen oven at ambient temperature and the process began by purging the oven with N2. Table 4.2 is the process used to cure the polyimide layer under low stress using YES oven.

4.1.6 Descum

To remove a thin film of polymer residue left behind in the develop process, it was descummed by plasma matrix. An etch gas was 80:20 02/CF4(30 seconds) [18].

4.1.7 Copper Brightening(oxidized during descum)

An O2/CF4 plasma will cause corrosion of copper. After the descum, a 30 second dip in 10 percent acetic acid was immediately necessary to prevent corrosion and discoloration of the copper surface [18].

4.1.8 Seed Layer Deposition

For the next layer deposition, E-beam deposition was processed with 3 minutes Ion Clean. It was selected with Chrome (250Å) and Copper (2000Å) as the seed layer deposition.

4.1.9 Layer 2 Patterning

The second step is to make the second plane pattern. The ceramic wafer was placed in the dehydration bake oven at 120°C for 30 minutes ahead of the application of photoresist. HMDS was then evaporated on the surface of the ceramic wafer for 10 minutes to improve the photoresist adhesion. A layer of thick photoresist, AZ9245 (AZ Electronic Materials), was used for patterning. It was spun on the surface at a speed of 1700 rpm for 5 seconds with an acceleration speed of 500 rpm and spun at 2700 rpm for 30 seconds with an acceleration speed of 1000 rpm. It was then soft-baked at 110°C for 90 seconds. After that, the ceramic wafer was exposed (Mask Alligner MA6/BA6) to make a pattern with 1 cycle for 60 seconds. Exposure was performed immediately after soft bake, as soon as the wafer had cooled to room temperature. It was then developed with AZ400K positive photoresist developer for 5 minutes which was in the ratio of 1:2.5 with deionized water. Then, a plasma descum with Matrix (300W, 20sec) was performed to remove any residual photoresist. After completing this step, photoresist thickness should be about 4.5 um. The mask layout is shown in figure 4.4.

4.1.10 Plating

The next step is metallization. First, copper (2um, 26mA) was plated. Nickel was then plated (0.2um, 23mA, 35-40°C). The Nickel layer served as a thermal barrier. It was used to improve the

adhesion to the resistor material. After plating, positive photoresist was stripped by acetone and was cleaned by methanol and water. Then the seed layers were etched by Cu etchant, Potassium Permanganate.

4.1.11 Polyimide Application

This step is to make a coating of polyimide on the surface. Prior to the application of polyimide, pre-poly etch was accomplished. Then, the ceramic wafer was placed in a dehydration bake oven at 120°C for 30 minutes. For non-polyimide surfaces - a thin layer of adhesion promoter VM652 (HD Microsystems) was formed to improve the adhesion to the polyimide layer. It was spun on the surface at a speed of 500 rpm for 5 seconds with an acceleration speed of 500 rpm and spun at 4000 rpm for 30 seconds with an acceleration speed of 1000 rpm. Poor adhesion of silicon materials can show up as silicon delamination or peel off during the rest of the processing steps. The layer was soft-baked at 120°C for 60 seconds. Next, the polyimide PI2611 was spun on the surface at 500 rpm for 5 seconds with an acceleration speed of 500 rpm then, spun at 3000 rpm for 30 seconds with an acceleration speed of 1000 rpm. Next, it was soft-baked at 120°C for 5 minutes in the dehydration bake oven. The next step was a ”low stress” curing process in the programmable YES oven (model 450-PB8-2P-CP). The wafer was placed in a programmable nitrogen oven at ambient temperature and the process began by purging the oven with N2. Table 3.1 is the process used to cure the polyimide layer under low stress using YES oven.

4.1.12 Photoresist Patterning for Polyimide Etching

The next step is to make the patterning for polyimide etching. The ceramic wafer was placed in the dehydration bake oven at 120°C for 60 minutes ahead of the application of photoresist. HMDS was then evaporated on the surface of the ceramic wafer for 10 minutes to improve the photoresist adhesion. A layer of thick photoresist, AZ 4620(AZ Electronic Materials), was used for patterning. It was spun on the surface at a speed of 1000 rpm for 30 seconds with an acceleration speed of 250 rpm and it was then soft-baked at 110°C for 90 seconds. Rest period (43.5, 73.5, 1hr)

was applied. To make a pattern, it was exposed with 3 cycles 25 seconds, 30 seconds in between. Exposure was performed immediately after soft bake, as soon as the wafer had cooled to room temperature. It was then developed with AZ400K positive photoresist developer for 3.5 minutes which was in the ratio of 1:2.5 with deionized water. Next, a plasma descum with Matrix (300W, 20sec) was performed to remove any residual photoresist. After completing this step, photoresist thickness should be about 15 um. The mask layout is shown in figure 4.5.

4.1.13 Polyimide Etching

After mounting on 5-in wafer with blue wax(105, 30 seconds), it was etched by (A.O.E). Conversely, it released substrate from the backing (105 to remove, clean with Amyl Acetate).

4.1.14 Seed Layer Deposition

For the next layer deposition, E-beam deposition was processed with 3 minutes Ion Clean. It was selected with Chrome (250Å) and Copper (2000Å) as the seed layer deposition.

4.1.15 Photoresist Patterning

The ceramic wafer was placed in the dehydration bake oven at 120°C for 30 minutes ahead of the application of photoresist. HMDS was then evaporated on the surface of the ceramic wafer for 10 minutes to improve the photoresist adhesion. A layer of thick photoresist, AZ9245 (AZ Electronic Materials), was used for patterning. It was spun on the surface at a speed of 1700 rpm for 5 seconds with an acceleration speed of 500 rpm and spun at 2700 rpm for 30 seconds with an acceleration speed of 1000 rpm. It was then soft-baked at 110°C for 90 seconds. After that, the ceramic wafer was exposed (Mask Alligner MA6/BA6) to make a pattern with 1 cycle for 60 seconds. Exposure was performed immediately after soft bake, as soon as the wafer had cooled to room temperature. It was then developed with AZ400K positive photoresist developer for 5 minutes which was in the ratio of 1:2.5 with deionized water. Then, a plasma descum with

Matrix (300W, 20sec) was performed to remove any residual photoresist. After completing this step, photoresist thickness should be about 4.5 um. The mask layout is shown in figure 4.6.

4.1.16 Plating

The next step is metallization. First, copper (1.25um, 26mA) was plated. Nickel was then plated (1.0um, 23mA, 35-40°C). And then Au was plated (1.5um, 20mA, 35-40°C). The Nickel layer served as a thermal barrier. It was used to improve the adhesion to the resistor material. And then, a plasma descum with Matrix (300W, 20sec) was performed to remove any residual photoresist. It was very helpful to prevent any current leakages in testing MCMs. After plating, positive photoresist was stripped by acetone and was cleaned by methanol and water. Then the seed layers were etched by Cu etchant(49-1), Potassium Permanganate.

4.1.17 Polyimide Application

This step is to make a coating of polyimide on the surface. The ceramic wafer was placed in a dehydration bake oven at 120°C for 30 minutes. For non-polyimide surfaces - a thin layer of adhesion promoter VM652 (HD Microsystems) was formed to improve the adhesion to the polyimide layer. It was spun on the surface at a speed of 500 rpm for 5 seconds with an acceleration speed of 500 rpm and spun at 4000 rpm for 30 seconds with an acceleration speed of 1000 rpm. Poor adhesion of silicon materials can show up as silicon delamination or peel off during the rest of the processing steps. The layer was soft-baked at 120°C for 60 seconds. Next, polyimide PI2611 was spun on the surface at 500 rpm for 5 seconds with an acceleration speed of 500 rpm and then spun at 3000 rpm for 30 seconds with an acceleration speed of 1000 rpm. It was then soft-baked at 120°C for 5 minutes in the dehydration bake oven. The next step was a ”low stress” curing process in the programmable YES oven (model 450-PB8-2P-CP). The wafer was placed in a programmable nitrogen oven at ambient temperature and the process began by purging the oven with N2. Table 3.2 is the process used to cure the polyimide layer under low stress using YES oven.

4.1.18 Photoresist Patterning for Polyimide Etching

Next, it is to make the patterning for polyimide etching. The ceramic wafer was placed in the dehydration bake oven at 120°C for 60 minutes ahead of the application of photoresist. HMDS was then evaporated on the surface of the ceramic wafer for 10 minutes to improve the photoresist adhesion. A layer of thick photoresist, AZ 4620(AZ Electronic Materials), was used for patterning. It was spun on the surface at a speed of 1000 rpm for 30 seconds with an acceleration speed of 250 rpm and it was then soft-baked at 110°C for 90 seconds. Rest period (43.5, 73.5, 1hr) was applied. To make a pattern, it was exposed with 3 cycles 25 seconds, 30 seconds waiting time in between. Exposure was performed immediately after soft bake, as soon as the wafer had cooled to room temperature. It was then developed with AZ400K positive photoresist developer for 3.5 minutes which was in the ratio of 1:2.5 with deionized water. Then, a plasma descum with Matrix (300W, 20sec) was performed to remove any residual photoresist. After completing this step, photoresist thickness should be about 15 um. The mask layout is shown in figure 4.6.

4.1.19 Polyimide Etching

After mounting on 5-in wafer with blue wax(105, 30 seconds), it was etched by (A.O.E). Conversely, it released substrate from the backing (105 to remove, clean with Amyl Acetate).

4.1.20 Backside Metal Deposition

It was selected with Chrome (500Å), Nickel (800Å), and Gold (1200Å) as backside metal deposition with 1 minute Ion Clean.

4.1.21 Dice

The silicon wafer is diced to separate all the individual probe arrays.

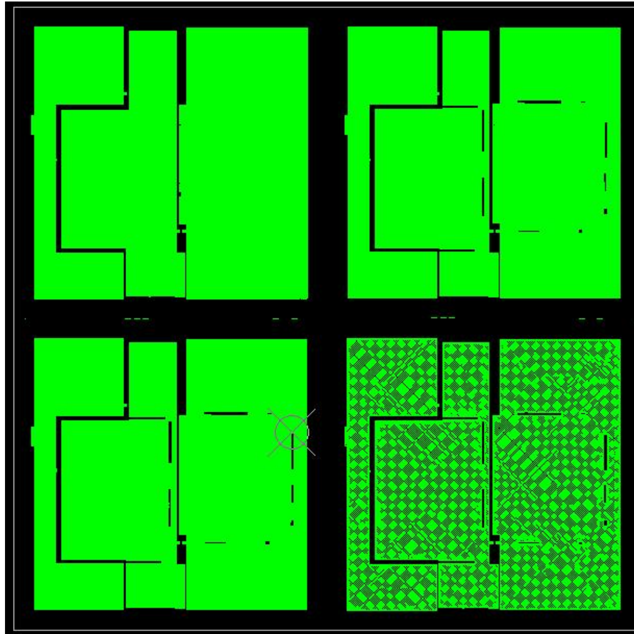


Figure 4.2: MCM Layout 1

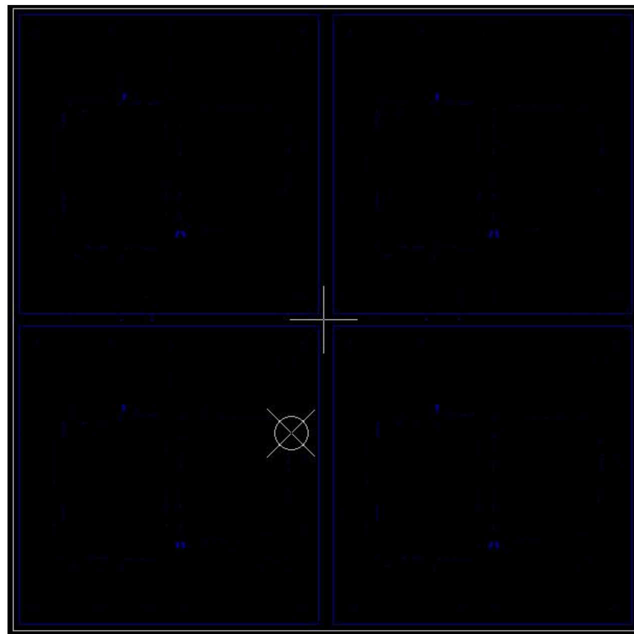


Figure 4.3: MCM Layout 2

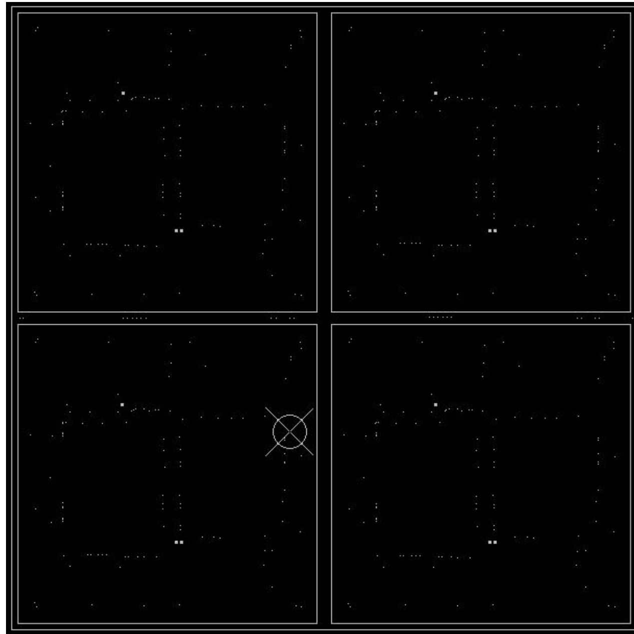


Figure 4.4: MCM Layout 3

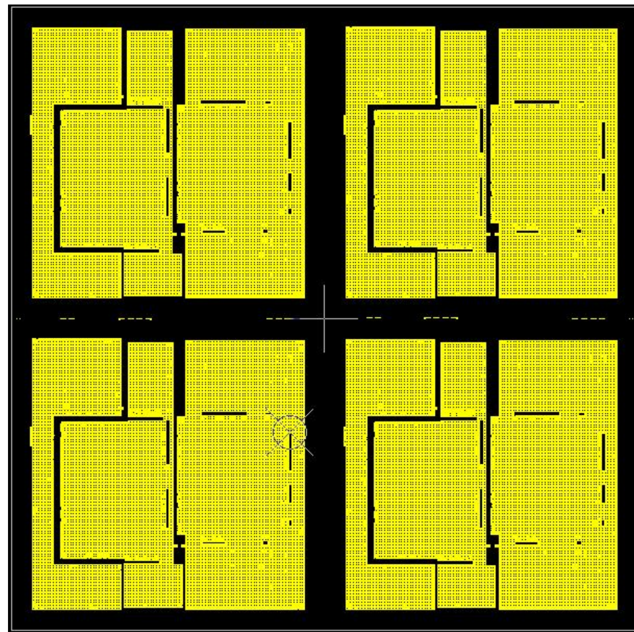


Figure 4.5: MCM Layout 4

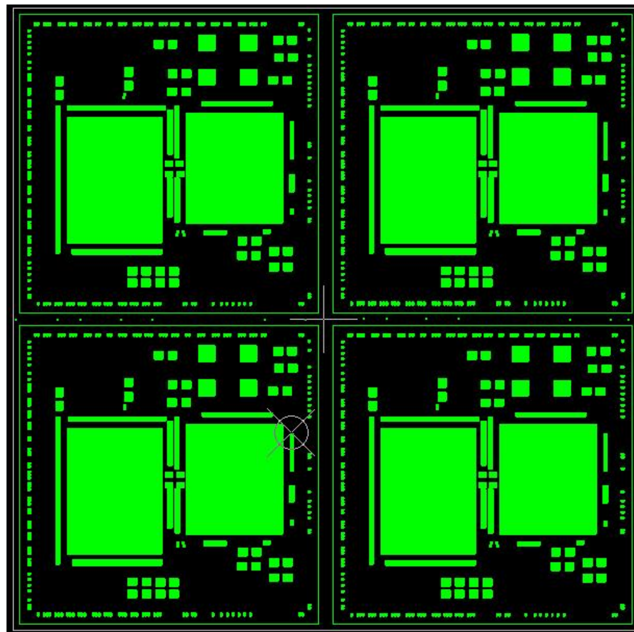


Figure 4.6: MCM Layout 5

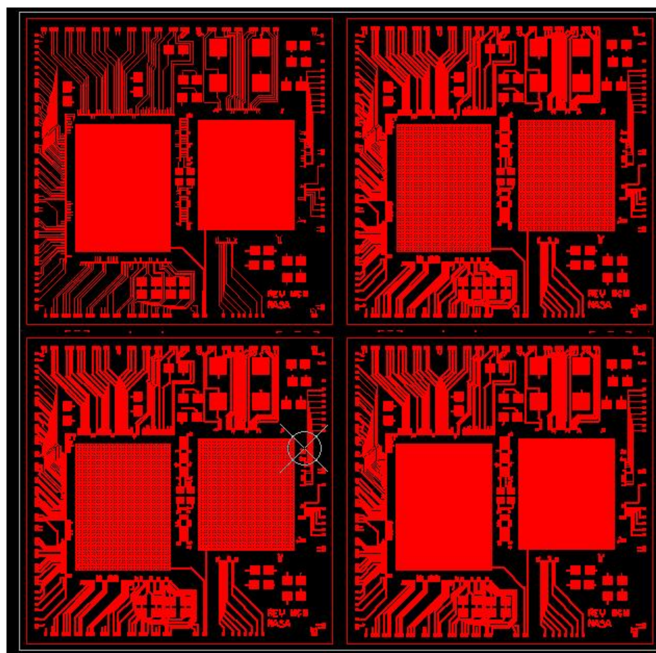


Figure 4.7: MCM Layout 6

4.2 Test Chip Procedures for MCM

The test chips are fabricated on 4-inch diameter silicon substrates. Based on the analysis presented in the previous chapter, wire bond solution is adopted to interconnect the test chip to MCM.

4.2.1 Patterning

The first step is to make the seed layer pattern. The silicon wafer was placed in the dehydration bake oven at 120°C for 20 minutes ahead of the application of photoresist. HMDS was then evaporated on the surface of the silicon wafer for 5 minutes to improve the photoresist adhesion. A layer of thick photoresist, AZ9245 (AZ Electronic Materials), was used for patterning. It was spun on the surface at a speed of 1700 rpm for 5 seconds with an acceleration speed of 500 rpm and spun at 2700 rpm for 30 seconds with an acceleration speed of 1000 rpm. It was then soft-baked at 110°C for 90 seconds. After that, the silicon wafer was exposed (Mask Alligner MA6/BA6) to make a pattern with 1 cycle for 60 seconds. Exposure was performed immediately after soft bake, as soon as the wafer had cooled to room temperature. It was then developed with AZ400K positive photoresist developer for 5 minutes which was in the ratio of 1:2.5 with deionized water. Next, a plasma descum with Matrix (300W, 20sec) was performed to remove any residual photoresist. After completing this step, photoresist thickness should be about 4.5 um.

4.2.2 Plating

The next step is metallization. First, copper (2.5um, 12mA) was plated. Nickel was then plated (0.5um, 10mA, 35-40°C). And then Au was plated (0.5um, 6mA, 35-40°C). Positive photoresist was stripped by acetone and was cleaned by methanol and water. Then the seed layers were etched by Cu etchant, Potassium Permanganate. Next, the silicon wafer is diced to separate all the individual probe arrays.

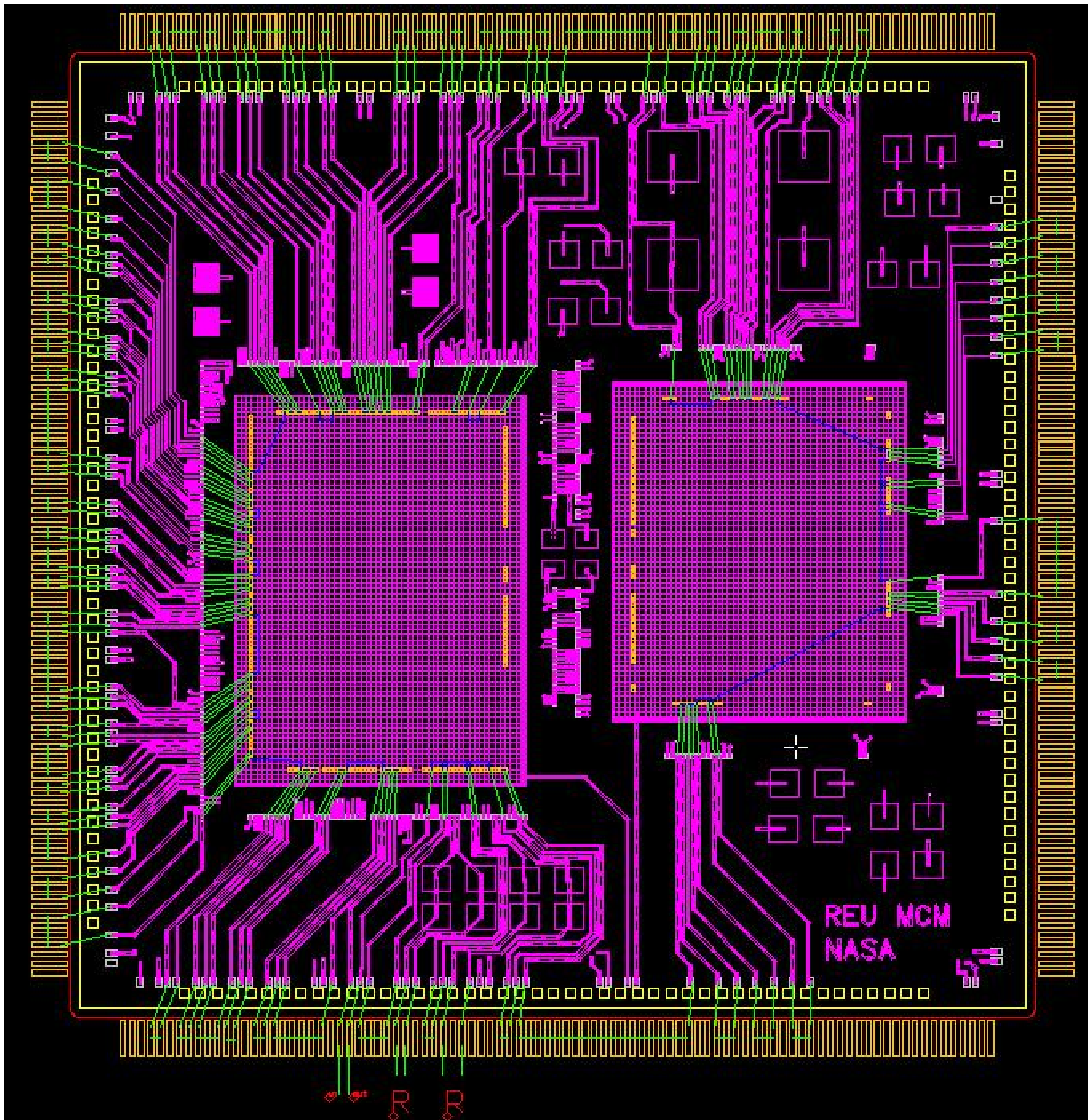


Figure 4.8: Test chip layout for MCM

Chapter 5

Test & Results

Flip chip and Wire bond test vehicles were packaged by Dr. Johnson's group. Various packaging structures were tested in order to evaluate the effectiveness of their design and to lay the groundwork for future models. The first step was to expose the temperature and stress distributions of the various models to extreme temperature cycling. This was simulated using commercially available software. Both of the two types of packaging structures, die to substrate and substrate to package, were designed and developed. An indium was used for substrate attachment to package of wire bond and solder was used for flip chip. Both indium substrate attachments were used.

5.1 Interaction between Die to Substrate Attach

They were exposed to temperature cycles(100), -180°C and +125°C, by dipping them into liquid nitrogen, then they were allowed to cool down to room temperature. Then, a half-diagonal finite element model has been constructed, which covers all the critical joints between die to substract attach and substrate to package attach.

5.1.1 Wire Bond

As it was discussed, each bond of face-up chips is connected individually with a wire. It was used Indium(0.05mm thick) which is used with high temperature alloys to attach a 5mm x 5mm die onto an AlN substrate(48mm x 13mm) and to attach an an AIN substrate(48mm x 13mm) onto an Al_20_3 package(53mm x 14mm) as shown in Figure 5.1. The commercial FEM software package ANSYS 5.2 was utilized to perform a detailed analysis of temperature and stress/strain distribution in the package. According to simulation (Figure 5.2), the edge-corner of the substrate attachment

has the maximum stress/strain instead of that of the die attachment because it has smaller CTE mismatch, AIN to $Al_2 0_3$, compared with that of die to substrate, SiGe to AIN CTE mismatch. In the result, substrate to package interconnection is the critical issue in reliability.

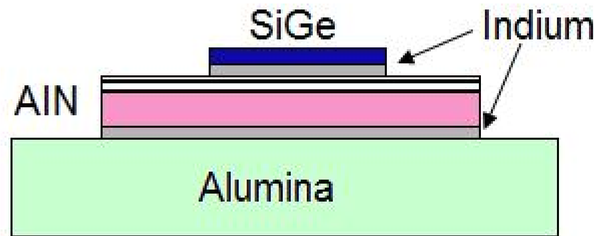


Figure 5.1: Wire bond

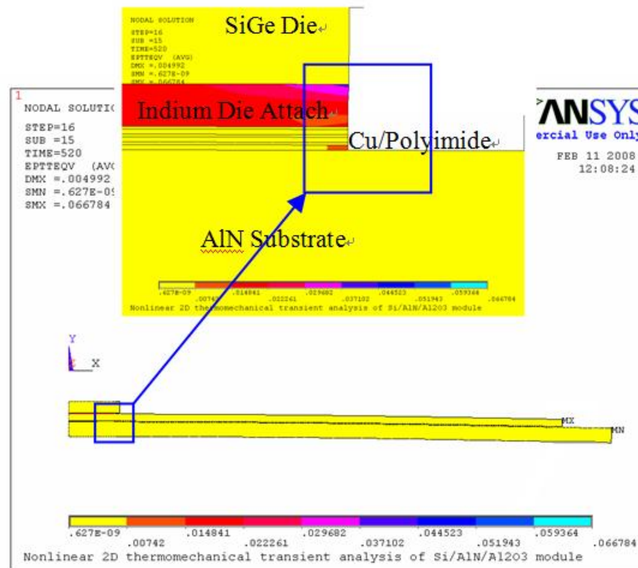


Figure 5.2: Strain distribution in the whole wire bond die attach type package[14]

5.1.2 Flip Chip

As it was discussed, it uses the direct electrical connection of face-down chips in opposition to wire bond. It was used solder bump(In50Pb) to attach a die onto an Si substrate as shown in Figure 5.3. It has the largest CTE mismatch between the substrate(Si) and the package($Al_2 0_3$). Therefore the maximum stress/strain was found to be accumulated at substrate and package interconnection (Figure 5.4).

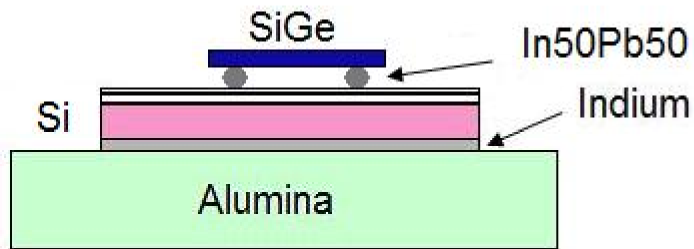


Figure 5.3: Flipchip

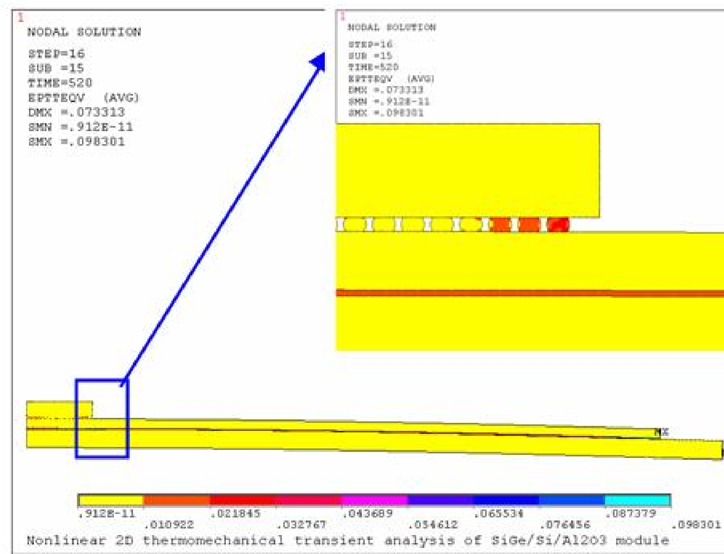


Figure 5.4: Strain distribution in the whole flip chip type package[14]

5.2 Interaction between Substrate to Package Attach

The CTE mismatch between die and substrate is negligible compared to that of between substrate(Si / AIN) and package(Alumina). The strain is mainly concentrated at the outer upper side of the indium substrate attach (Figure 5.5). Moreover, the substrate attachment is the critical concern in reliability.

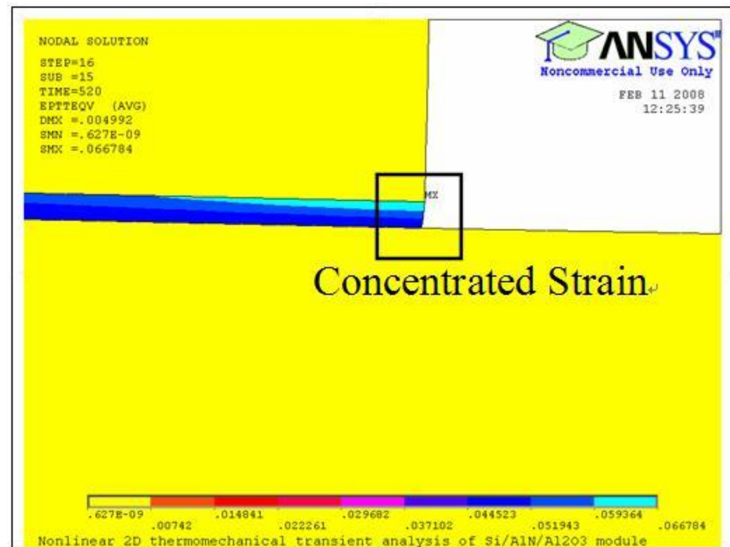
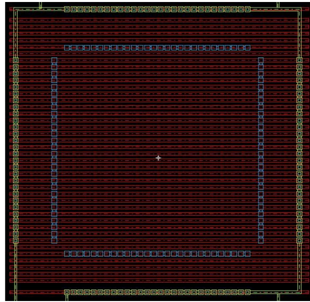


Figure 5.5: FEM model of substrate to package[14]

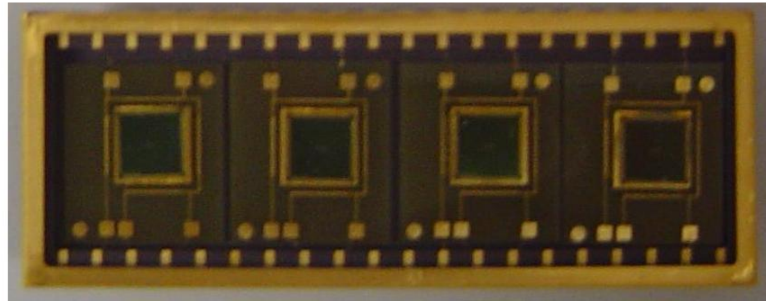
5.3 Test Vehicles

Two test vehicles were fabricated for test. A single array chip of wire bond and flip chip are shown in Figure 5.6 and Figure 5.7. The 5mm x 5mm PB6 wire bond test die and 5mm x 5mm FA-10 flip chip test die were purchased from Delphi Electronics. The die was backside metal deposited with Ti/Ni/Au. Two hermetically sealed packages were subjected to temperature thermal shock cycles(100), -180°C and +125°C, by repeatedly dipping them into liquid nitrogen and then they were allowed to cool down to room temperature [20]. It was not observed solder joint failures and degradation of the dielectric layers. However, flip chip was not as good as the wire bond, because flip chip has the largest CTE mismatch between Si substrate and $Al_2 0_3$ package compared

to the wire bond, AlN substrate and $Al_2 0_3$ package. The maximum deformation of flip chip and wire bond were 0.004992 and 0.073313. The corresponding maximum stress values are 0.066784 and 0.098391 at the edge of the corner between substrate and package.

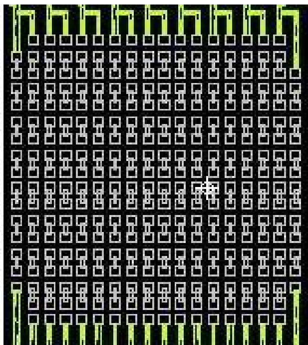


(a) Wire bond single array

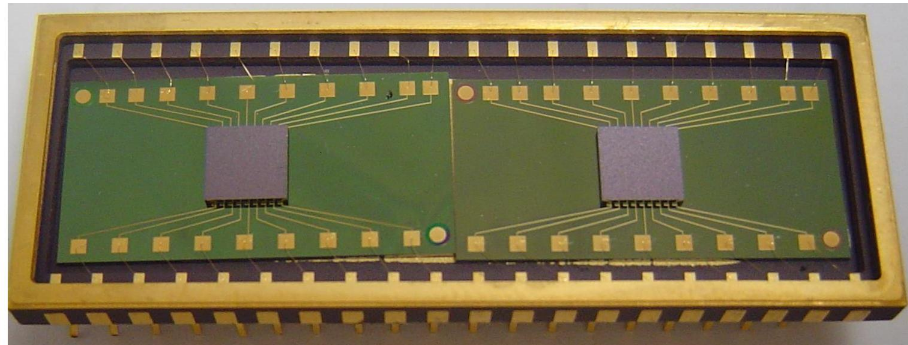


(b) Wire bond testing chip

Figure 5.6: Wire bond test vehicle



(a) Flip chip single array



(b) Flip chip testing chip

Figure 5.7: Flip chip test vehicle

5.4 MCM Package

Two MCM packages shown in Figure 5.8 and 5.9 were hermetically sealed and each sealed package has been cycled between -180°C and 125°C for 20 complete cycles. The inter-connections between wire bond pad and lead are shown in figure 5.10 and 5.11. Reliability screening tests were performed for MCM. It was observed that no electrical or solder joint failures occured.

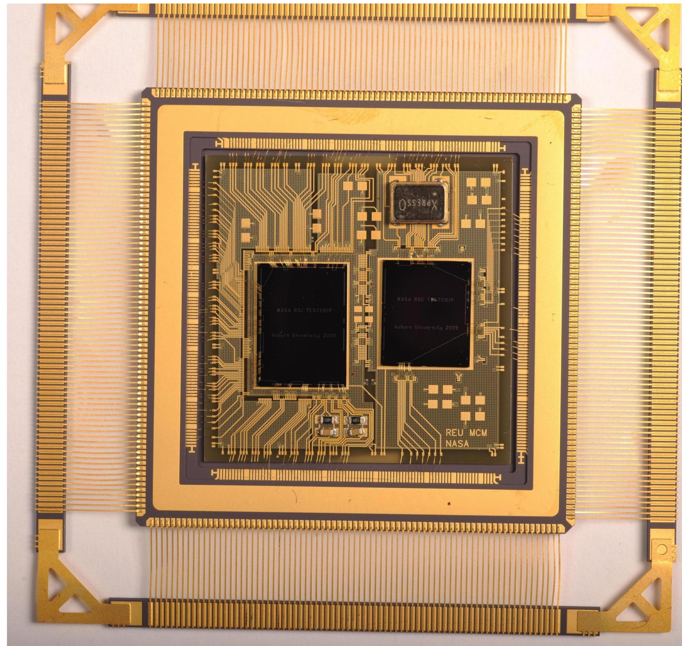


Figure 5.8: MCM before sealed

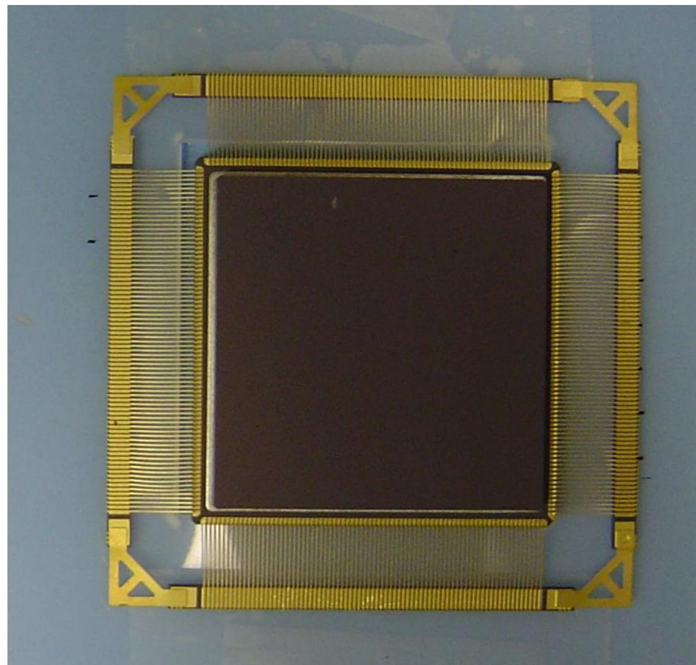


Figure 5.9: MCM after sealed

Wirebond Pad	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
LEAD	1	GRD	2	4	5	VDD	6	7	8	GRD	10	11	12	VDD	13	14	16	GRD	17	18
Wirebond Pad	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
LEAD	19	VDD	20	22	23	GRD	24	25	26	VDD	28	29	30	GRD	31	32	34	VDD	35	36
Wirebond Pad	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60
LEAD	37	GRD	38	40	41	VDD	42	43	44	GRD	46	47	48	VDD	49	50	52	GRD	53	54
Wirebond Pad	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
LEAD	55	VDD	56	58	59	GRD	60	61	62	VDD	64	65	66	GRD	67	68	70	VDD	71	72
Wirebond Pad	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
LEAD	73	GRD	74	76	77	VDD	78	79	81	GRD	82	83	84	VDD	85	87	88	GRD	89	90
Wirebond Pad	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120
LEAD	91	VDD	93	94	95	GRD	96	97	99	VDD	100	101	102	GRD	103	104	106	VDD	107	108
Wirebond Pad	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140
LEAD	109	GRD	111	112	113	VDD	114	115	117	GRD	118	119	120	VDD	121	123	124	GRD	125	126
Wirebond Pad	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160
LEAD	127	VDD	129	130	131	GRD	132	133	135	VDD	136	137	138	GRD	139	141	142	VDD	143	144
Wirebond Pad	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180
LEAD	145	GRD	147	148	149	VDD	150	151	153	GRD	154	155	156	VDD	158	159	160	GRD	161	162
Wirebond Pad	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200
LEAD	164	VDD	165	166	167	GRD	168	170	171	VDD	172	173	174	GRD	176	177	178	VDD	179	180

Figure 5.10: PAD-LEAD connection-1

Wirebond Pad	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220
LEAD	182	GRD	183	184	185	VDD	186	188	189	GRD	190	191	192	VDD	194	195	196	GRD	197	198
Wirebond Pad	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240
LEAD	200	VDD	201	202	203	GRD	204	206	207	VDD	208	209	210	GRD	212	213	214	VDD	215	216
Wirebond Pad	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260
LEAD	218	GRD	219	220	221	VDD	222	224	225	GRD	226	227	228	VDD	230	231	232	GRD	233	235
Wirebond Pad	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280
LEAD	236	VDD	237	238	239	GRD	241	242	243	VDD	244	245	247	GRD	248	249	250	VDD	251	253
Wirebond Pad	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300
LEAD	254	GRD	255	256	257	VDD	259	260	261	GRD	262	263	265	VDD	266	267	268	GRD	269	271
Wirebond Pad	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320
LEAD	272	VDD	273	274	275	GRD	277	278	279	VDD	280	281	283	GRD	284	285	286	VDD	287	289
Wirebond Pad	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340
LEAD	290	GRD	291	292	293	VDD	295	296	297	GRD	298	299	301	VDD	302	303	304	GRD	305	307
Wirebond Pad	341	342	GRD	GRD	GRD	GRD	GRD	GRD	GRD	GRD	GRD	GRD	GRD	GRD	GRD	GRD	GRD	GRD	GRD	GRD
LEAD	308	VDD	3	15	27	39	51	63	75	80	92	104	116	128	140	152	157	169	181	193
Wirebond Pad	GRD	GRD	GRD	GRD	GRD	GRD	GRD	GRD	GRD	GRD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
LEAD	205	217	229	234	246	258	270	282	294	306	9	21	33	45	57	69	86	98	110	122
Wirebond Pad	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD						
LEAD	134	146	163	175	187	199	211	223	240	252	264	276	288	300						

Figure 5.11: PAD-LEAD connection-2

Figure 5.12 shows temperature cycles. The resistances of MCM were initially 140.5Ω and 183.1Ω at room temperature. It was observed that the resistances were slightly increased after 1 cycling to 142.2Ω and 185Ω at room temperature shown in Figure 5.13. Then, they were 144.8Ω, 189Ω at room temperature after 5 thermal shock cycles, and 144.2Ω, 188.7Ω at room temperature after 10 thermal shock cycles. Next, they were 141.8Ω, 187.2Ω at room temperature after 20 thermal shock cycles. The possible reason in decreasing the resistance after 20 cycles was the difference of the room temperature on that day. Resistance was observed 145.0Ω, 188.6Ω after 30 cycles and 144.4Ω, 188.1Ω after 50 cycles.

There was an initial increase in resistance. However, this result seems to be very reasonable since the resistance remained almost constant after 10 thermal shock cycles. Even though the resistance was changed slightly by temperature, the processes have been demonstrated and initial reliability screening results are verified.

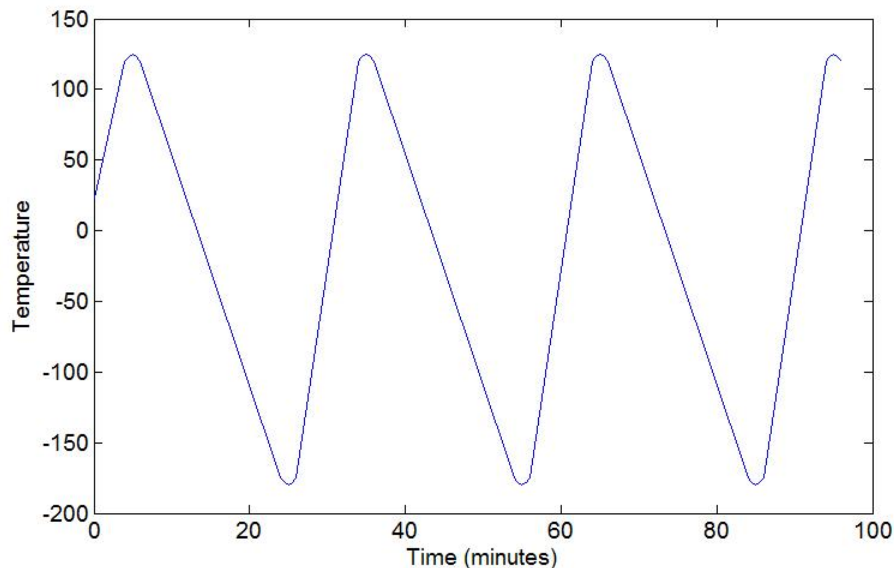


Figure 5.12: Temperature cycling

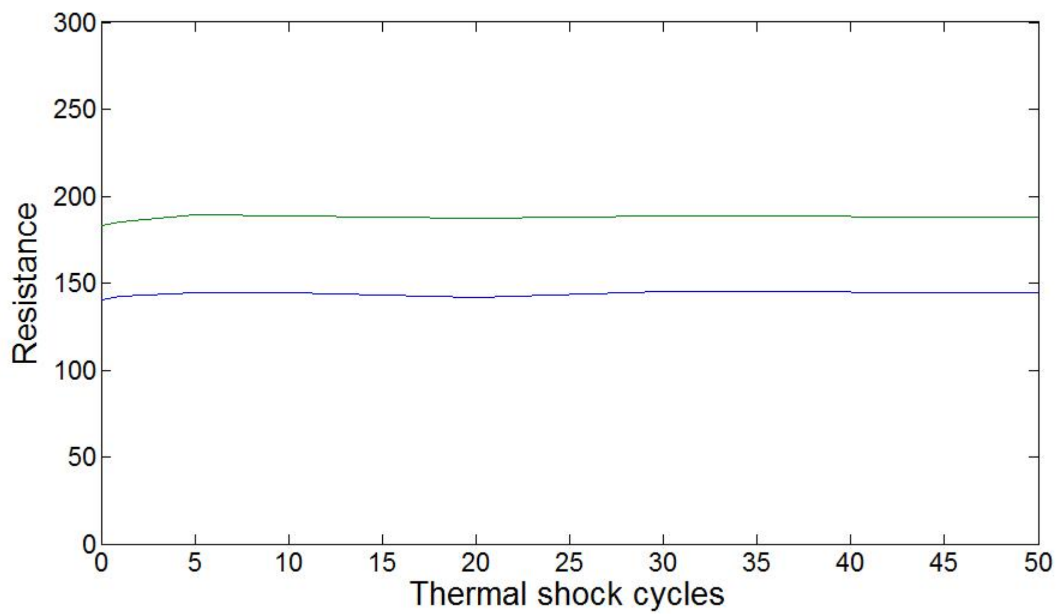


Figure 5.13: Resistance changes after 50 thermal shock cycles

Chapter 6

Conclusion

This paper presents a design fabrication technology of Multi Chip Module which is suitable for wide range temperature. In this work, multi chip module chips using wire bond have been successfully fabricated. Thermal shock cycle tests have been performed for flip chip and wire bond before adapting MCM. Then, wire bond and flip chip solution were compared. It was shown that Flip chip and Wire bond are working exactly as expected even though wire bond has less stress campared with flip chip. Minimizing the stress is especially important when mulitiple copper/low-k interconnection layers are present. These results have indicated that wire bond is more suitable for the multi chip module.

The surface of flip chip and wire bond which is electroplated on the gold layer tends to disintegrate because of repeated use of the plating solution. Identifying the reason for this occurrence and the improvement in the plating process will make the chips more durable by preserving the required electrical characteristics of the electrode.

Multi chip module packages using wire bond solution were fabricated. Then, thermal reliability testing of MCM was performed. The resistance of MCM was getting larger, but it was stable after 10 thermal shock cycle tests. Additional long-term stability test will be subjected in the future including failure analysis.

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