

# **Considerations and Options for High Temperature Die Attach**

by

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A thesis submitted to the Graduate Faculty of  
Auburn University  
in partial fulfillment of the  
requirements for the Degree of  
Master of Science

Auburn, Alabama  
December 13, 2010

Keywords: High Temperature Electronics, Electronics Packaging, Die attachment

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## Abstract

Development of electronics that can withstand temperatures ranging from 200°C up to 600°C is a growing research area. More electronic aircraft, space exploration and in engine automotive electronics are some examples of these research areas. As these operating temperatures rise so does the need for electronics packages that can handle these temperature ranges. A major aspect of this packaging is die attachment. There are currently two main metallurgy options proposed for high temperature die attachment. One is silver based metallurgies and the other is gold based metallurgies.

Silver at high temperatures in the presence of an electric field will migrate between electrodes. This presents a major risk when using silver as a die attachment material for high temperature electronics. Part of the work presented here looks at silver's migration characteristics and highlights the potential risks involved when using silver as a die attach material.

Gold does not suffer from the same problem of migration as silver and therefore is a better choice for high temperature die attachment. Several gold based metallurgies have been used for die attachment. One other very useful feature of gold is that gold will self diffuse at elevated temperature and pressure. The other work presented here investigates the use gold-gold diffusion to form an acceptable die attachment for high temperature devices.

## Acknowledgments

First I would like to thank Almighty God for endowing me with the abilities to succeed in the work I have done here at Auburn. Second I would like to thank my wife Sarah, who has supported me and pushed me to do my best even when I thought I wasn't capable. I am very grateful for the love and encouragement she has given me while I have pursued my education. Third I would like to thank my parents who have supported me emotionally and financially through my entire college career and who have always been willing to help me reach my goals.

I would like to thank Dr. R. Wayne Johnson for taking me on as an undergraduate and then a graduate student. Without his expertise and guidance I would not have been able to complete this work. He has taught me problem solving skills I will carry with me the rest of my life. I want to thank Dr. Wentworth and Dr. Dean for taking the time to read my thesis and work me into their schedules; I know they are both busy and I appreciate all they have done for me.

I would like to thank Mike Palmer and John Marcell. Mike taught me to operate a large portion of the equipment I can now and I could always depend on him to provide a fresh idea to solve a problem. I am convinced John can find any part or tool that I could ever need and will most likely have it in his office.

I want to thank Charles Ellis for helping me find a way to fabricate each new step of this project Dr. Johnson gave me and for working with me to answer the numerous questions I had about microfabrication.

I want to thank the other students in our research group Ping, Vikki, and Rui. I have learned so much about packaging from each of them and I greatly appreciate their willingness to provide a helping hand whenever I might have needed it. I also want to thank Colin and Ryan for allowing me to talk through fabrication processes with them and for answering the many questions I had.

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# Chapter 1

## INTRODUCTION

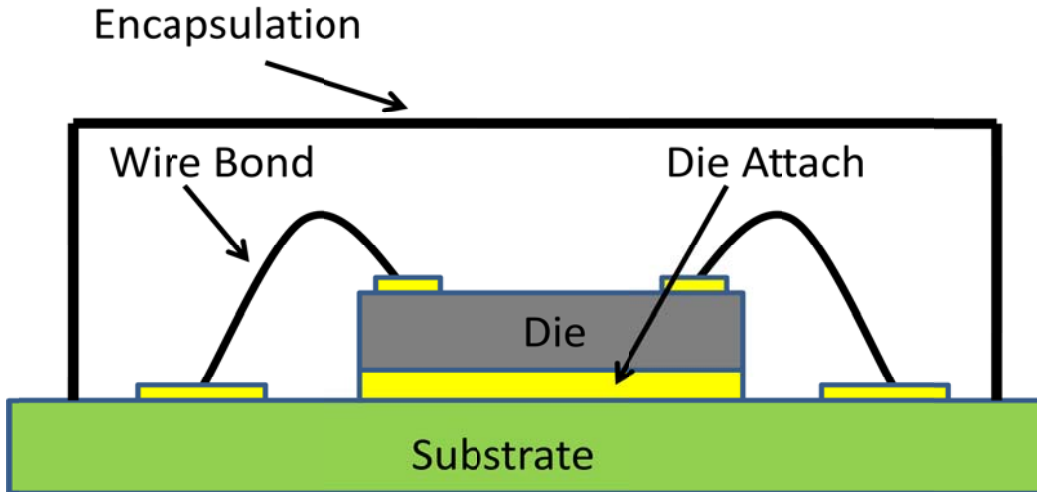
High temperature electronics is a continually growing field and are used in many different areas. Oil and gas industries are interested in deep well monitoring, which will require electronics that operate at up to 325°C. These electronics will provide information on present temperature, pressure, direction, and angle of the drill head as well as information on the material encountered by the drill head [1]. Exploration of the surface of Venus by NASA will require electronics capable of operation in high temperature environments up to 485°C [2]. SiC operational amplifiers have been produced for operation at 350°C as well as some power electronic devices that have extended operating temperature of 600°C [3]. Table 1.1 shows some of the application areas and corresponding temperature requirements.

Table 1.1: The potential application for high temperature electronics.[4]

High Temperature Electronics Application	Peak Ambient	Chip Power	Current Technology	Future Technology
<b>Automotive</b>				
Engine Control Electronics	150 °C	< 1 kW	BS & SOI	BS & SOI
On-cylinder & Exhaust Pipe	600 °C	< 1 kW	NA	WBG
Electric Suspension & Brakes	250 °C	> 10 kW	BS	WBG
Electric/Hybrid Vehicle PMAD	150 °C	> 10 kW	BS	WBG
<b>Turbine Engine</b>				
Sensors, Telemetry, Control	300 °C	< 1 kW	BS & SOI	SOI & WBG
	600 °C	< 1 kW	NA	WBG
Electric Actuation	150 °C	> 10 kW	BS & SOI	WBG
	600 °C	> 10 kW	NA	WBG
<b>Spacecraft</b>				
Power Management	150 °C	> 1 kW	BS & SOI	WBG
	300 °C	> 10 kW	NA	WBG
Venus & Mercury Exploration	550 °C	~ 1 kW	NA	WBG
<b>Industrial</b>				
High Temperature Processing	300 °C	< 1 kW	SOI	SOI
	600 °C	< 1 kW	NA	WBG
<b>Deep-Well Drilling Telemetry</b>				
Oil and Gas	300 °C	< 1 kW	SOI	SOI & WBG
Geothermal	600 °C	< 1 kW	NA	WBG

BS = bulk silicon, SOI = SOI, NA = not presently available, WBG = wide bandgap.

A significant aspect of these high temperature devices is packaging that can handle the environmental requirements. In traditional electronics the operating temperatures are 0 to 85°C, but as temperature become more extreme traditional materials begin to fail. With high temperature electronics, not only must the package be functional at room temperature but also this functionality must be consistent over a large temperature range. Electronics packages most often contain a die attached to a substrate, with wirebonds connecting the circuitry on the die to electrical contracts on the substrate and an encapsulating body most often plastic or ceramic that will cover the assembly, protecting it from the environment and enabling handling and next level connection of the device (Figure 1.1).



1.1: A typical electronics package.

Many electronics use plastic or epoxy encasement; however for high temperature environments these will fail. Ceramic packages are often used for high temperature electronic devices. A major component of these packages is the die attachment, these materials can be epoxy or glass, for non conduction die attachment or silver filled epoxy or solder for conducting die attach, however many traditional metallic attachments such as soft solders have low melting temperatures  $183^{\circ}\text{C}$  (eutectic tin-lead solder) and  $217^{\circ}\text{C}$  (Sn-Ag-Cu). While inexpensive and proven for lower temperature applications, these will not withstand the temperatures experienced by the high temperature electronics. There are many die attach metallurgies that are currently being used for high temperature applications, mostly gold and silver based metallurgies and a few high temperature epoxies [5].

Several people have suggested using a Ag based metallurgies for die attachment, because of the cost advantages to Au metallurgies, however Ag will migrate in the presence of an electric field at higher temperatures, presenting a possible failure

mechanism. Au based metallurgies, though more expensive, do not suffer from this potential failure mechanism and are a better choice for high temperature die attachment.

The work presented here is divided into two parts. The first part examines Ag migration characteristics of several forms of Ag to verify the possible failure mechanism of silver in high temperature applications. The second part of this work is to develop an Au die attachment method using thermocompressive bonding.

The next chapter of this thesis reviews bonding mechanism for high temperature die attachment and failure mechanism for die attachment. Also it examines current silver based metallurgies for die attachment and previous work on Ag migration. Lastly it reviews Au based die attachment metallurgies and some of the work on die attachment using Au thermocompressive bonding.

The third chapter presents the results of the Ag migration study. A detailed description of the experiment performed is given, followed by the data gained from the experimentation. The analysis of the data includes a qualitative analysis and then a statistical analysis.

The fourth chapter will explain the Au thermocompressive die attachment process. A detailed description of the samples, methods and verification techniques used is given, followed by an analysis of the experimental results.

The fifth chapter will be a summary of the work presented and a brief discussion of the implications of this work.

The last chapter will discuss the directions for future work.

## Chapter 2

### LITERATURE REVIEW

#### **2.1 Background**

The work presented here focused on die attachment metallurgies for applications above 200°C. Die attachment for high temperature electronics is done with metallic systems and uses several methods; Transient Liquid Phase (TLP) bonding, solid state diffusion, and sintering which is based on solid state diffusion. The metals used can be either a single metal such as silver or a metallic system such as Ag-In. Metallurgies for die attachment are highly varied, since the work presented here focuses on Ag and Au die attachment, die attachment with those metals will be reviewed.

TLP bonding is the joining of a metal system, usually a two or three metal system, where one metal has a much lower melting temperature than the others. Bonds form when one material melts and diffusion between the liquid and solid begins leaving an intermetallic alloy of the two metals with a higher melting temperature than the original low melting temperature material. The bond is completely formed when all the liquid material is absorbed in the new intermetallic. This process can take between a few minutes to a few hours [6]. Table 2.1 presents some common TLP bonding systems and bonding time and temperatures.

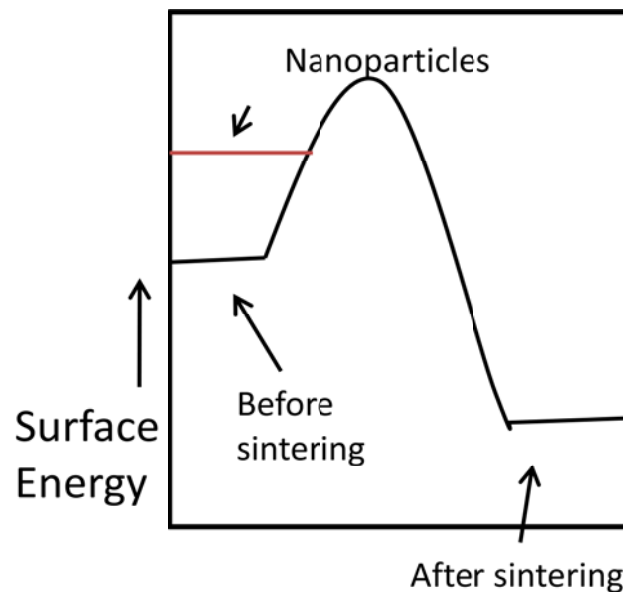
Table 2.1: Common TLP bonding systems. [6]

<b>Material System</b>	<b>Process Time and Temp.</b>	<b>Remelt Temp.</b>
Copper - Indium	4 min at 180 °C	> 307 °C
Copper - Tin	4 min at 280 °C	> 415 °C
Silver - Tin	60 min at 250 °C	> 600 °C
Silver - Indium	120 min at 175 °C	> 880 °C
Gold - Tin	15 min at 260 °C	> 278 °C
Gold - Indium	0.5 min at 200 °C	> 495 °C
Nickel - Tin	6 min at 300 °C	> 400 °C

Solid state diffusive bonding is very similar to TLP bonding except, instead of a liquid layer between two materials; a solid layer of material is placed between two parent metals. This interlayer consists of a material that will diffuse into the metal layers it is placed between, forming a solid bond. The interlayer can be a single material, an alloy or multiple layers of metals. Elevated temperature and pressure allow the needed diffusion mechanisms. One difficulty with solid state diffusion is ensuring contact across the diffusion surface to form a uniform bond with minimal voiding. Solid state diffusion also takes longer than liquid to solid diffusion, making time the other limiting factor in solid-state bonding.

Sintering is similar in mechanism to solid state bonding, because both utilized solid state diffusion to produce the bond; however sintering is the process of forming a solid from tightly compacted particles and the diffusion occurs only along the particle surfaces. Tightly compacted particles have much higher surface energy than solid bulk material; since systems try to move to the lowest energy state, diffusion along the particle surfaces occurs to minimize surface area. This diffusion produces a solid material with

significantly less total surface energy. There is an energy barrier preventing diffusion at room temperature, by raising the temperature of compacted particles the needed energy is provided to overcome this barrier (pressure can also be used to help raise the energy level). Figure 2.1 helps to visualize this; the line at the left shows the initial energy level, by adding energy to the system the energy level rises to the peak allowing diffusion and the particle begin to solidify. As the material sinters the gaps between the spheres begin to fuse together forming a solid and lowering the total surface energy as seen on the right of the figure. The smaller a spherical particle is the higher the surface energy for a given amount of material will be, this means nanoscale particles have higher surface energies than microscale particles. This higher initial surface energy results in lower temperatures being required to overcome the energy barrier (Figure 2.1 red line) [7].



2.1: Sintering energy diagram

For sintering in packaging, generally a paste or ink is used, which consists of solid spheres of a similar size held together by a binding agent which is generally a solvent. These spheres range in size from the nanometer scale to a few hundred microns. Once



printed on a substrate the solvents are baked off and the spheres that are in contact begin to diffuse together forming a solid material.

## **2.2 Die attachment**

The material used to attach a die to a substrate or package provides a path for thermal conduction and electrical conduction as well as mechanical support for the die in the package. For applications requiring thermal and electrical conduction, such as power devices, metallic die attachments are the best choices because of their superior performance in both of these areas.

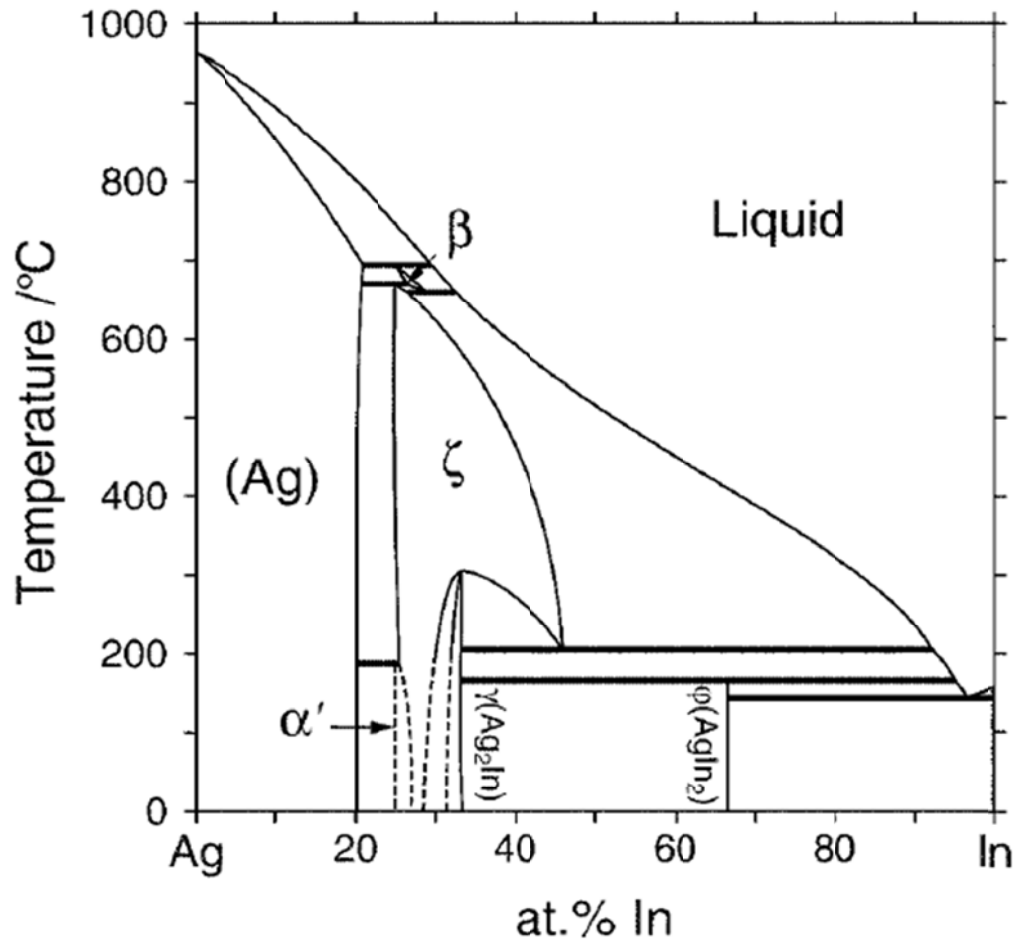
Failure of a die attachment generally results in a crack forming in the die attachment material. This is due to stresses caused by the coefficient of thermal expansion (CTE) mismatch between the die, the die attachment materials, and the substrate. Stresses also form in the die attach during processing and can accelerate failures. During the die attachment process, sections of the die attach may not bond leaving voids. These voids can also cause areas of increased stress during the life of the device [8, 9]. Stresses are proportional to the diagonal dimension of the die; this means the larger the die that is to be attached, the larger the stress will be on the die [10]. These stresses increase as the radial distance from center increases, so highest stresses are found at the corners of the die attachment.

### **2.2.1 Silver based die attachment**

Silver die attachments are mainly divided into two categories; TLP bonding, and sintered nanoparticles. Silver is an excellent electrical and thermal conductor, which is one of the main attributes that make silver so attractive for electronics and die attachment

in particular. Silver also has a melting temperature of 981°C which is desirable for high temperature electronics [7].

TLP bonding using Ag-In relies on a mixture of Ag and In either as thin film layers [11] or a mixture of particles [12]. The ratio of Ag-to-In is selected so that the resulting material after processing is in the Ag-rich region (>70wt%Ag, 71.2at%Ag) of the Ag-In phase diagram (Figure 2.2). The melting point of In is 156.6°C which allows for lower temperature processing, however significant time at temperature is required for In diffusion (2 hours according to Welch [6]) [13].



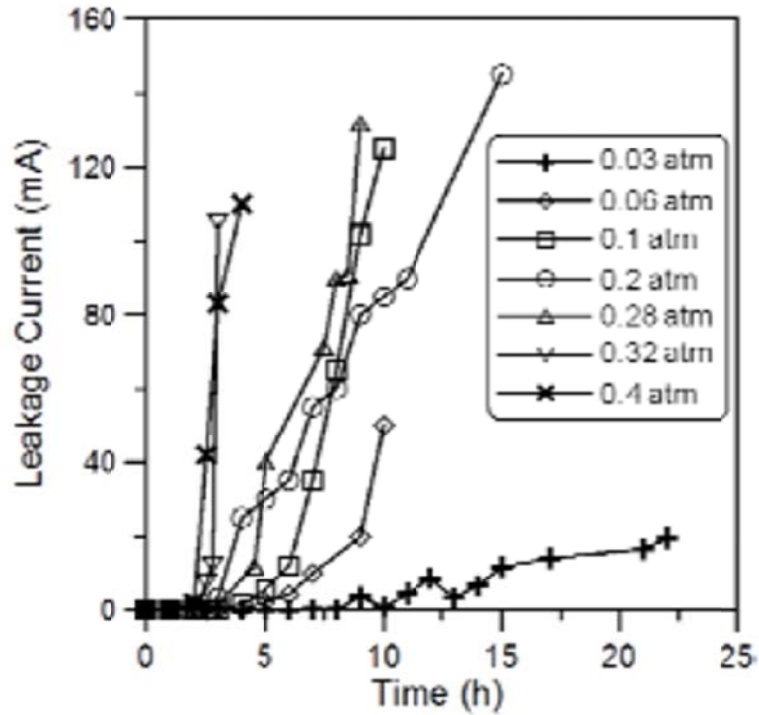
2.2: The Ag-In Phase diagram [14].

Sintered nanoparticle Ag die attach begins with Ag nanoparticles in a paste with an average silver particle size of 30 nm [15]. After dispensing and die placement, the assembly is heated to drive off the volatiles from the paste and the Ag nanoparticles sinter forming a continuous structure with low void content. Pressures of up to 5 MPa are used to ensure contact and improve sintering [7]. The sintering temperature is significantly depressed for nanoparticle Ag due to the large surface area-to-volume ratio of the nanoparticles [15]. Sintering can be done at 285°C and the resulting die attachment is expected to withstand 400°C [5]. Another advantage of sintered nano silver die attachment is that this would be a single metal system. This fact precludes it from intermetallic formation which is a potential failure mechanism for multiple metal systems [7].

However, Ag potentially presents a significant disadvantage when used as a die attach material. Nano Ag and Ag in a Pd-Ag film in the presence of an electric field will migrate with an exponential dependence on temperature [16, 17, 18, 19, 20,]. Ag migration occurs by two major mechanisms [21]. 1) Electrochemical migration occurs when Ag ions migrate through an absorbed water layer from anode to cathode and then deposit themselves on the cathode. The reaction starts with Ag at the anode dissolving forming  $\text{Ag}^+$ ;  $\text{Ag} \rightarrow \text{Ag}^+ + \text{e}^-$ . The  $\text{Ag}^+$  ion combine with  $\text{OH}^-$  to form AgOH; this compound is unstable and forms  $\text{Ag}_2\text{O}$  plus water. This compound is dispersed in a colloided form and undergoes a hydration reaction producing Ag ions. These ions drift under a electric field to the cathode where they are deposited:  $2\text{AgOH} \rightarrow \text{Ag}_2\text{O} + \text{H}_2\text{O} \rightarrow 2\text{Ag}^+ + 2\text{OH}^-$  [22]. 2) Dry migration occurs in the absence of humidity and is much more apparent at higher temperatures ( $>120^\circ\text{C}$ ). It is thought this reaction starts with  $\text{Ag}_2\text{O}$

that dissociates into Ag ions:  $\text{Ag}_2\text{O} \rightarrow 2 \text{Ag}^+ + \text{O}^{2-}$ . These ions drift under the electric field to the cathode. The  $\text{O}^{2-}$  anions provide charge neutrality and the depletion of Ag cations continues to drive the oxidation and dissociation reactions [16]. Both types of migration result in a buildup of Ag at the cathode in the form of dendrites that eventually reach the anode causing catastrophic failure of the device.

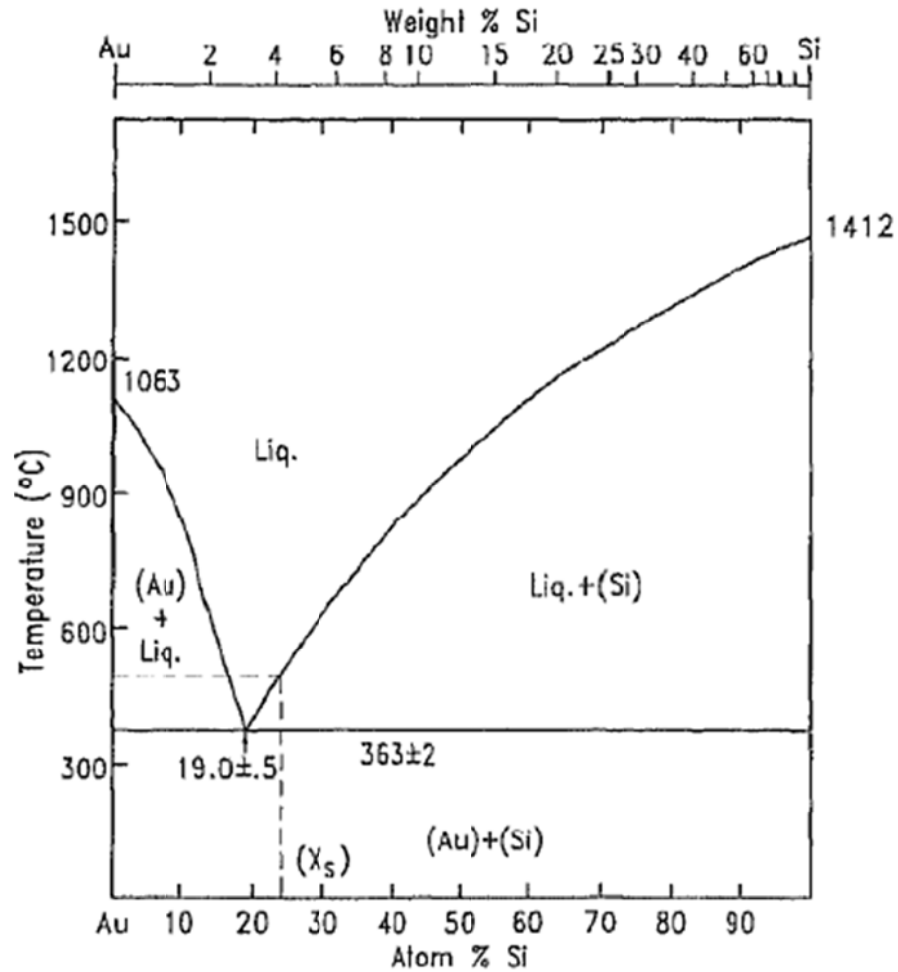
The majority of the research in this area has examined migration of Ag in Pd-Ag film through glass dams at temperatures between 150°C and 375°C [17, 18, 19]. The phenomenon of dry silver migration in open air at 300°C with thick film PdAg has been reported [20]. The high temperature migration of Ag from Nano-Ag paste in open air and with  $\text{O}_2$  partial pressure controlled has also been studied [16]. This study showed dry Ag migration is dependent on  $\text{O}_2$  partial pressure. Figure 2.3 show the leakage current across a  $\text{Al}_2\text{O}_3$  gap with nano-Ag electrodes at 400°C with a 20V/mm bias. The “life time” of a sample increased 25 times by lowering the  $\text{O}_2$  partial pressure from 0.4 atm to 0.03 atm. [16]



2.3: Nano-Ag Leakage current vs time at various O<sub>2</sub> partial pressures[16]

### 2.1.2 Gold Die attachment

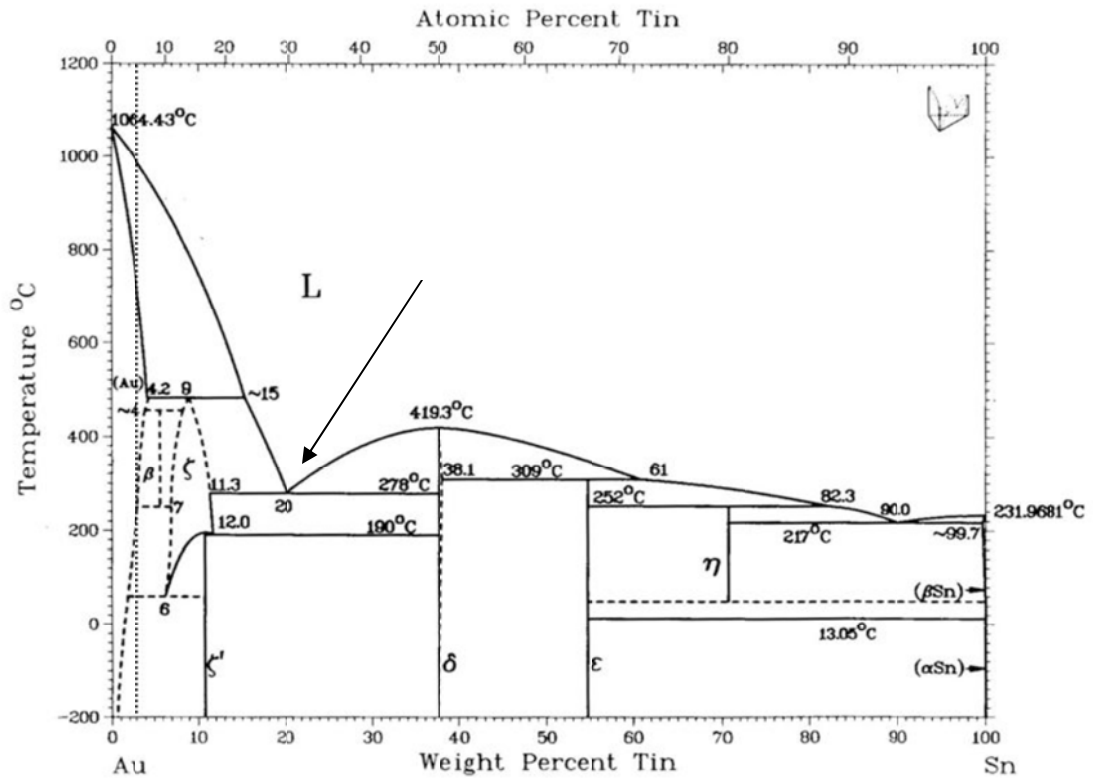
Gold is a very common metal in electronics due to its resistance to oxidation and excellent thermal and electronic conduction. Au/Si at one point was considered the industry standard for hard solders used in die attachment. Eutectic Au/Si (m.p. 363°C) (Figure 2.4) bonding is most often performed above 400°C [23]. It is done generally with either a pure gold preform or a gold silicon preform. Pure gold preforms can only be used with silicon die because the silicon for the reaction is taken from the back side of the die. Au/Si bonding has been used for silicon die as well as SiC die [2], and GaN wafer bonding [24].



2.4 Gold silicon phase diagram [25]

Eutectic Au/Sn has a lower melting temperature (280°C) than Au/Si and has also been used for die attachment (Figure 2.5). Die attachment is done most often with a preform of eutectic AuSn, however work at Auburn University has had success with performs of Sn plated onto a thin layer of Au. Sn plated Au is a transient liquid phase bonding method, the Sn layer will melt first and diffuse into the Au. Off-eutectic Au/Sn can also be achieved by using a smaller eutectic Au/Sn preform than the size of the die, limiting the amount of Sn present. A source of Au must be present to achieve the off eutectic composition; the source used is a thick (~20 um) layer of Au on the die [2]. The

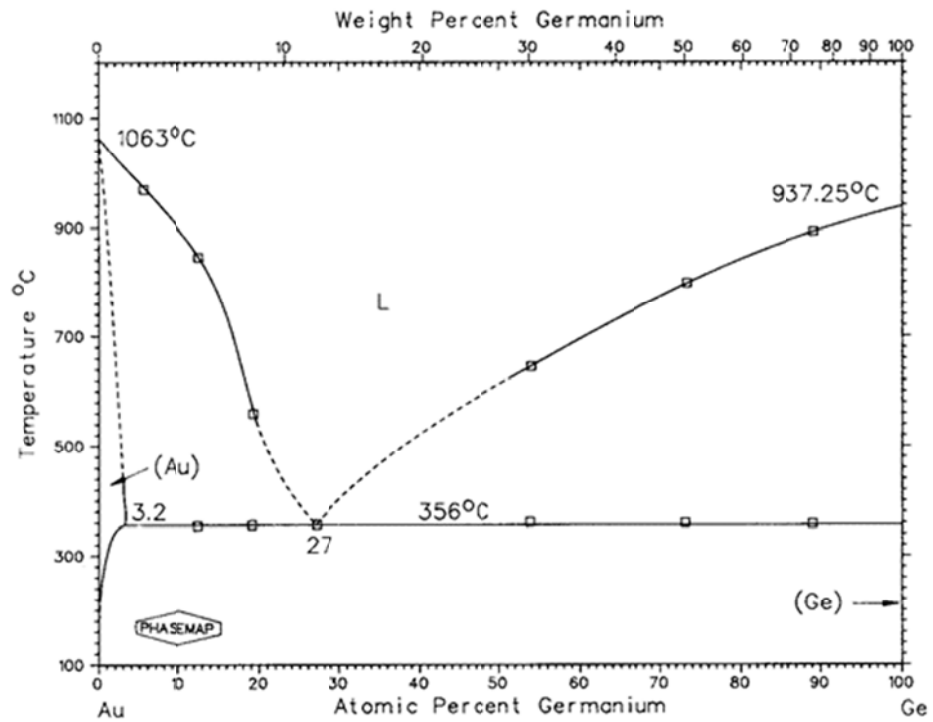
result is a higher melting temperature. This material system has been demonstrated with SiC die by Johnson et al. [2, 26]. The longer the Sn has to diffuse at processing temperatures, the higher the remelt temperature will be, because there will be a lower concentration of Sn; moving the final composition further left of the eutectic point. One of the major problems with Sn containing preforms is the formation of tin oxide on the surface of the preform. This thin oxide layer inhibits bonding and results in a higher concentration of voids under the die. [27]



2.5 The Au-Sn Phase diagram [2]

Au-Ge has a eutectic melting temperature of 356°C [28] and has been used as a solder in electronics; as a die attach generally it is found in a hypo-eutectic preform (Figure 2.6) [29]. Ge will form a brittle intermetallic with Ni which can cause problems,

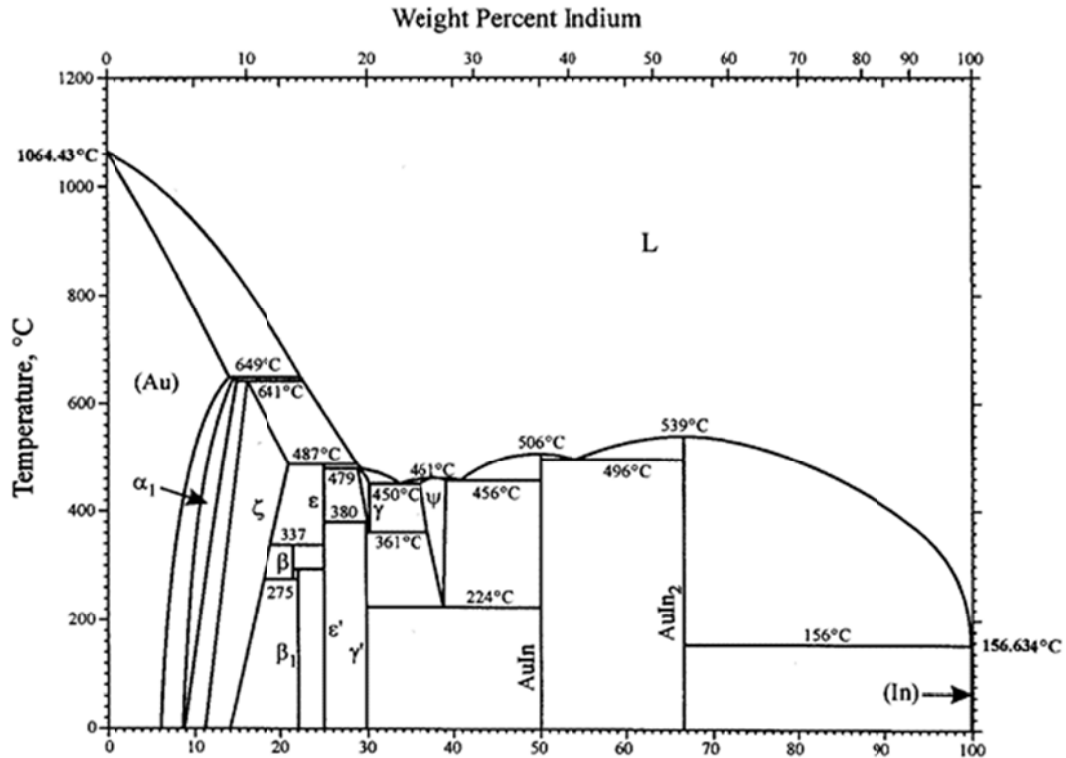
however for metal systems not containing Ni, Au-Ge has been examined with positive results by Zheng et al and Palmer et al [28, 30, 31].



2.6: Au-Ge phase diagram [32]

Au-In is a TLP bonding system that has found use as die attachment metallurgy. Bonding temperatures range from 156°C to 250°C, with shorter bonding times required as temperature increases (Figure 2.7) [33].





2.7: Au-In Phase diagram [34]

Die attachments with multiple metals always have the risk of forming harmful intermetallics depending on the metallurgy used on the die and the substrate. Au to Au thermocompressive (TC) bonding avoids this problem by producing a bond that is only solid Au.

TC bonds only form if there is a direct bare metal contact between metal surfaces. This is further exemplified by Equation 2.1 which shows a direct relation between increased bond strength and increased surface contact [35, 36, 37]. Most metals form a thin oxide layer on the surface and this oxide is the major inhibitor to TC bonding; removal of this oxide is critical to forming bonds [37, 38]. Methods such as plasma cleaning will remove the majority of this layer, but it will not completely remove it. However, deformation will breakdown and disperse this oxide layer increasing the

surface contact area and therefore the bond strength. This is highlighted by looking at  $Y$  from equation 2.1 as a function of local strain [37]. Though bare Au will not form an oxide layer on the surface it is found to have a contamination layer of C and other materials that prevents bonding just as oxide does in other metals.

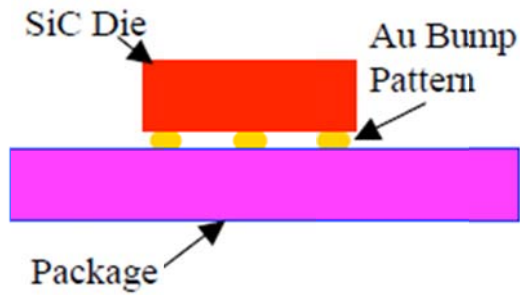
$$Y = \frac{(A-A_0)}{A} = \frac{\epsilon}{(\epsilon+1)} \quad [2.1]$$

$Y$  = increase in bond strength  
 $A$  = initial surface contract area  
 $A_0$  = new surface contract area  
 $\epsilon$  = local strain

TC bonding of Au has been used in electronics extensively for many years. It has been used for wire bonding and wafer bonding for MEMS fabrication. Wafer bonding is used to produce multilayer micromachined devices such as pressure sensors [39, 40]. Drost et. al looked at TC bonding on a die level, testing bonding forces between 0.06 N/mm<sup>2</sup> and 2.2 N/mm<sup>2</sup> and temperature ranges from 350°C to 450°C. His conclusion was the amount of pressure used for the bond is not the most important factor; rather uniformity of the pressure across the surface is the most important factor. He claims forces of up to 0.13 N/mm<sup>2</sup> produced the highest bond yield and that bonding time greater than 1 min improved the bond [41]. Tsau et. al disagree with this last statement reporting that bonding time did not produce a significant difference in bond strength [39].

A TC bonding based technique has been presented before [2, 42, 43]. This technique used gold balls in a similar fashion to flip chip die, but used only as a die attach and not for individual connections. In Johnson's work the die attachment was done with multiple gold bumps on a substrate then thermocompressively bonded to the die. This method yielded shear strengths of 1.5 kg to 2.5 kg with 8 bumps per die, and 2 kg to 4 kg

with 25 Au bumps [2]. Figure 2.8 shows a cross sectional view for a die and substrate bonded in this method.



2.8: Au thermocompression bonding using gold bumps. [2]

Ang et. al have done similar work reporting a minimum bonding temperature of 150°C and ideal bonding force of 350g/bump at 200°C and 500 g/bump at 150°C .

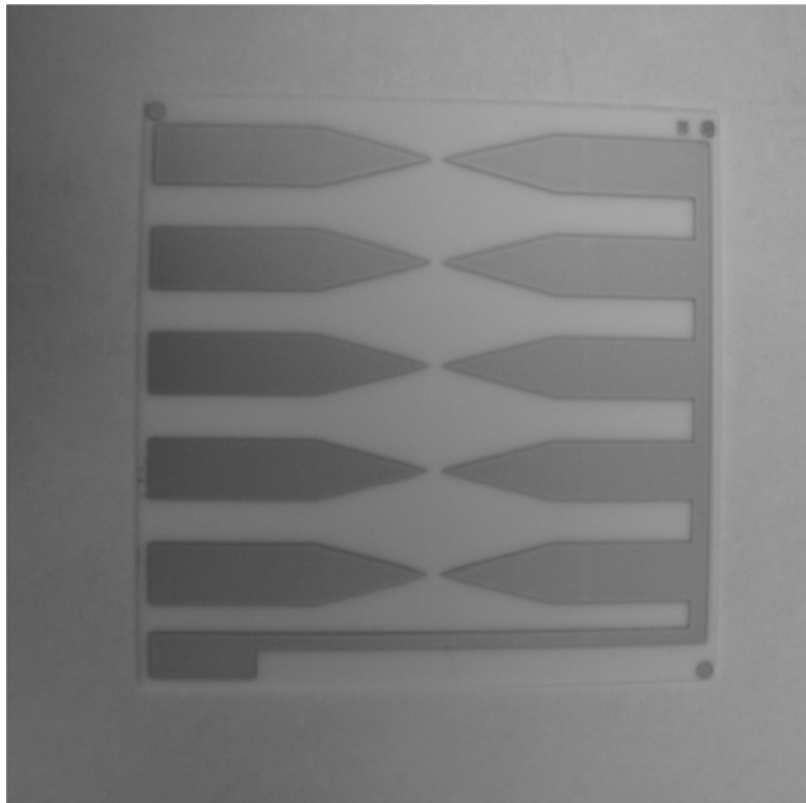
Tensile strength increased as bonding force increased up to the ideal bonding force, but then decreased as bonding force continued to increase [43]. This is confirmed by Zheng et al [42].

## Chapter 3

### SILVER MIGRATION EXPERIMENT

#### 3.1 Silver Migration Experimental Setup

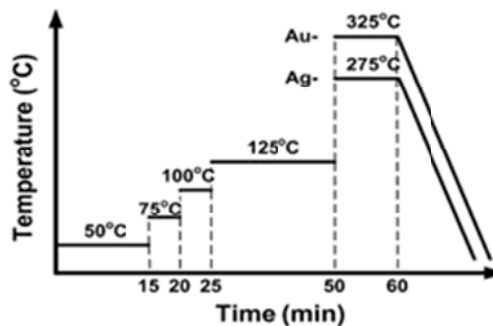
The goal of the experiment was to examine the silver migration characteristics of three different forms of silver: thin film Ag, sintered nano Ag, and thick film PdAg. The test structure consisted of two 100 mil wide lines tapering to a point leaving a 40 mil gap between the points (Figure 3.1). Each substrate had 5 test structures.



3.1: The silver migration test structure on a 2in x 2in substrate

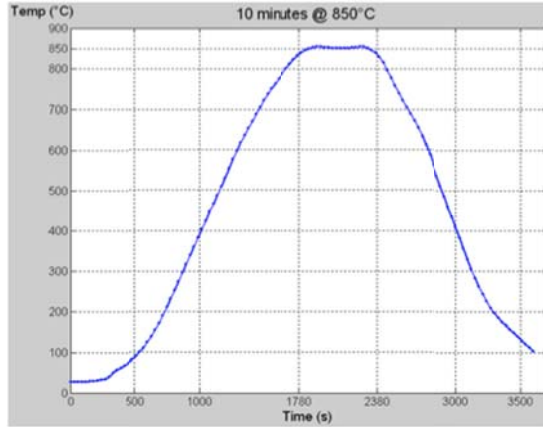
The thin film Ag samples were produced on a 2 in by 2 in  $\text{Al}_2\text{O}_3$  substrate from Coors Tech using a lift off technique. The substrate was first coated with P5640 negative photo resist made by AZ Electronic Materials at 3000 RPMs for 30 seconds. This resulted in 3-4  $\mu\text{m}$  of photoresist, that was exposed for 15 seconds using a Karl Suss mask aligner. The photoresist was developed for 1 minute leaving the desired pattern exposed. 1000  $\text{\AA}$  of Ti was e-beam deposited on the substrate then 1  $\mu\text{m}$  of Ag was deposited. The final step was to remove the photoresist and metal that was on top of it with acetone leaving the pattern pictured in Figure 3.1.

The nanoAg samples were first processed exactly the same as the thin film samples up to the deposition step. These samples had 1000  $\text{\AA}$  layer of Ti e-beam deposited, then 1  $\mu\text{m}$  of Cu was e-beam deposited followed by 1000  $\text{\AA}$  e-beam deposited Ag. The photoresist was removed with acetone taking the extra metal with it leaving the same pattern previously mentioned. A 2  $\mu\text{m}$  layer of Ag was electroplated on the thin film Ag by Component Surfaces. An 8  $\mu\text{m}$  thick layer nanosilver paste from NBE Tech, LLC was screen printed onto the tips of the test structures using a MPM corp. Model TP-100 screen printer. Once screen printed, the paste was processed according to Figure 3.2 with a max temperature of 275°C for ten minutes. [44]



3.2: The thermal profile for sintering the nanosilver paste [44]

The thick film palladium silver paste was similar to the one used in the previous silver migration report [20]. This paste was directly screen printed onto an  $\text{Al}_2\text{O}_3$  substrate and dried at  $150^\circ\text{C}$  for 10 minutes. Then it was fired with a 60 minute temperature profile with 10 minute peak at  $850^\circ\text{C}$  (Figure 3.3).

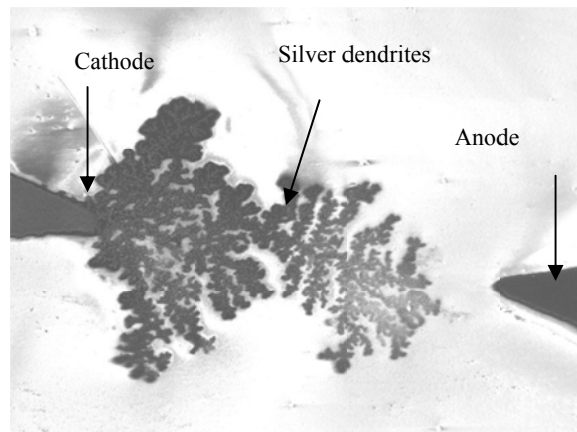


3.3: The firing profile for the silver palladium.

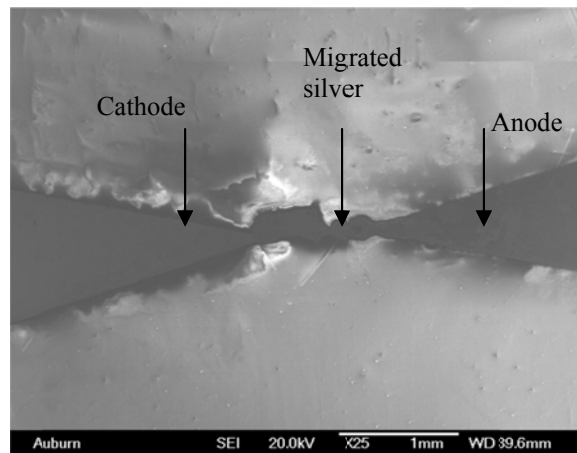
Tests were conducted in air at  $300^\circ\text{C}$  and  $375^\circ\text{C}$ , with bias voltages of 100 V, 50 V, and 25 V. Monitoring of the test structures was done with a Keithley 7002 switching box connected to a Keithley 2001 multi-meter used to monitor the voltage across a series resistor. A  $68\text{ k}\Omega$  resistor was placed in series with each test structure to limit current when the gap shorted as well as to provide a measurement point to monitor the leakage current of each test structure. A voltage of 5V corresponding to a leakage current of  $73.5\text{ }\mu\text{A}$  was considered a failure. The switching box was computer controlled to monitor each part once every minute and 5 failure readings were required to log a failure to ensure no false failures.

### 3.2 Silver Migration Results

Short circuit failures appear in two types: Figure 3.4 shows the silver fanning out but the final connection point is not clearly visible. The second failure type was a solid line across the gap. (Figure 3.5) The second type is thought to be the result of migration of the dendrites back to the shortest path between electrodes. This is supported by the thicker lines closer to the cathode, which seem to be the beginning of this convergence. Failures indicate growth as expected from cathode to anode.

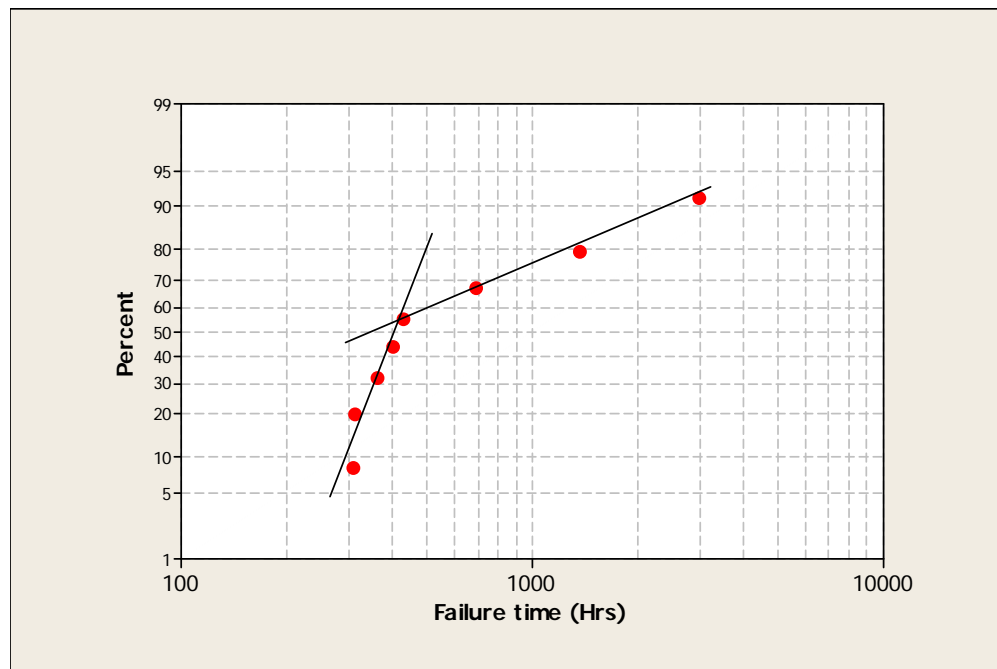


3.4: Silver Dendrites mode one, thin film Ag



3.5: Silver migration Failure Mode Two with Thin Film Ag

The data was analyzed using SAS. Median time to failure was determined by fitting each group to a lognormal distribution as used by Hornung and Gagne [17, 19]. Unfailed samples were treated as censored data unless mentioned below. All data collected was used in the analysis except half of the 300°C 100V thin film data, which showed a significant difference between the two substrates tested. The 100 V thin film data when plotted (Figure 3.6) on a lognormal plot showed evidence of two different failure mechanisms. Data from the substrate with the fastest failure rate was used in the analysis.



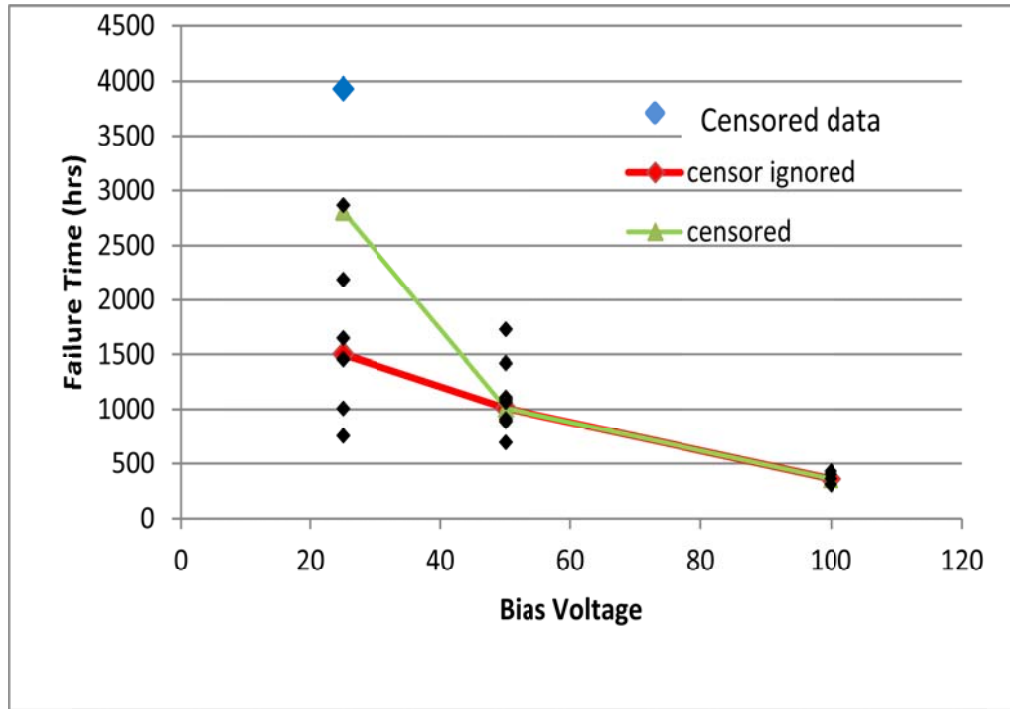
3.6: Lognormal plot of 300°C thin film Ag samples at 100V bias

The 300 V thin film data is presented in Figure 3.7. Four of the samples biased at 25 V did not fail before the test was stopped so median time to failure was taken by two methods for these samples. The failure times were fit to a lognormal distribution using the four unfailed samples as censored data at the time the test was stopped which was 3931 hours, resulting in a median time to failure of 2812

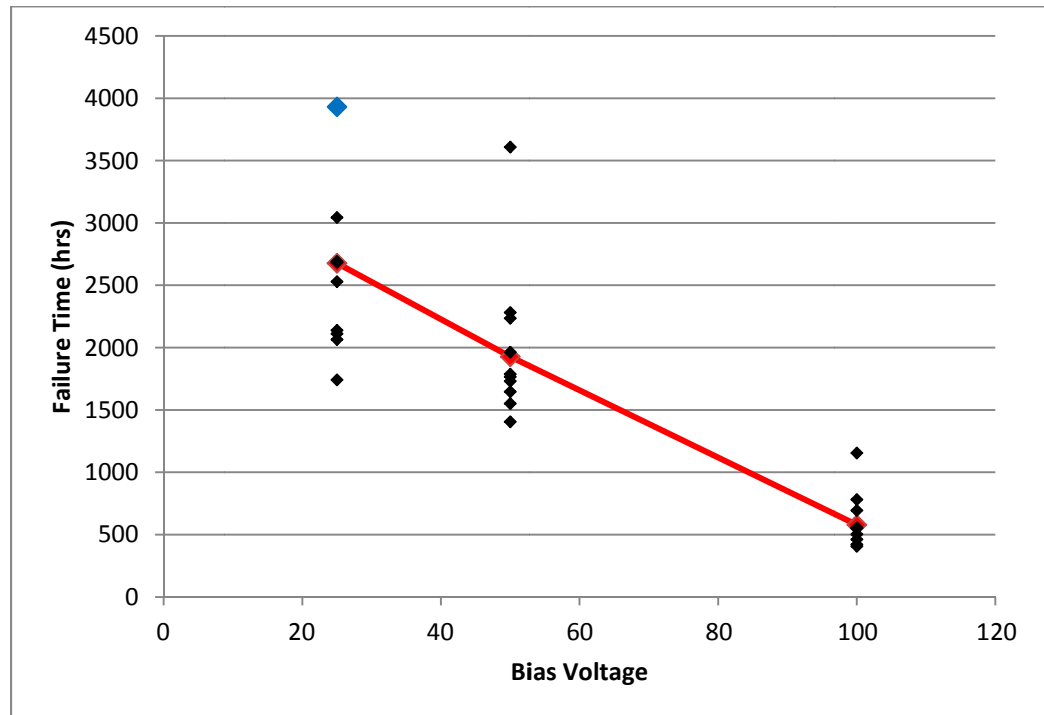


hours. The green line in the plot shows the median failure times with this method. The censor time is over 1000 hours beyond the longest actual failure time (2864 hours), so the median failure time was also calculated with the censored time removed. The red line shows this data, and this is much more consistent with the expected direct inverse relationship between bias voltage and failure time. The blue points represent censored data points; there are four censored points at 25 V and one at 100 V.

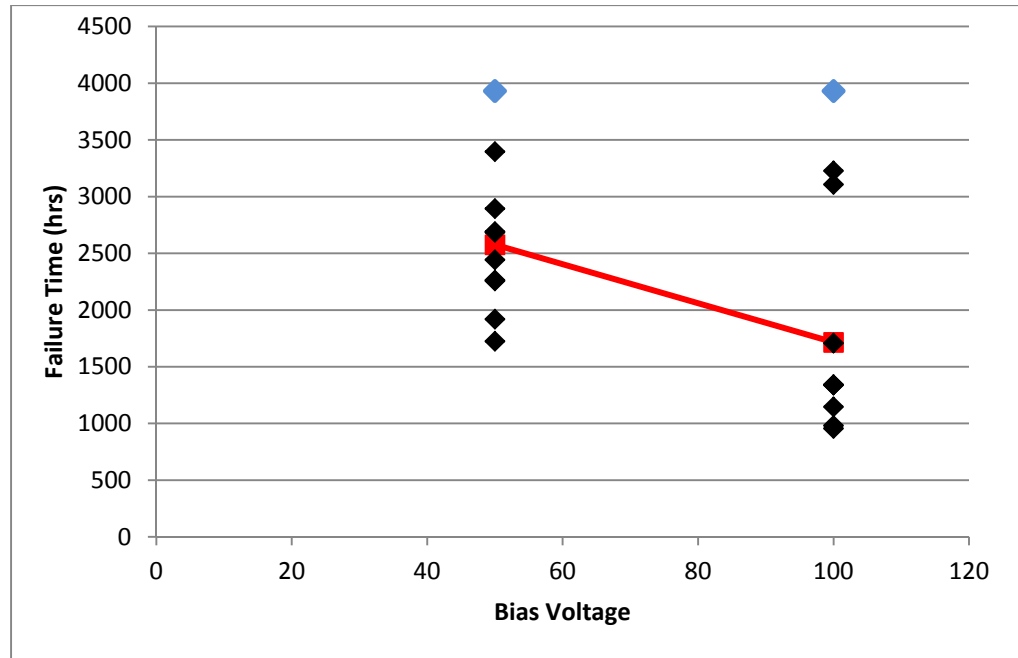
The 300°C Nano-Ag silver data is presented in Figure 3.8. The red line in the graph shows the median time to failure at each bias voltage. As with the thin film data the expected inverse relationship between bias voltage and failure time is shown. The 25 V data contains two censored data points, shown by the blue point on the graph. The PdAg data is presented in Figure 3.9. There is only data from 100 V and 50 V samples because the 25 V samples did not fail, the reason for this is not clear. Both bias voltages have censored data points represented in blue (one for each voltage).



3.7: 300°C thin film data

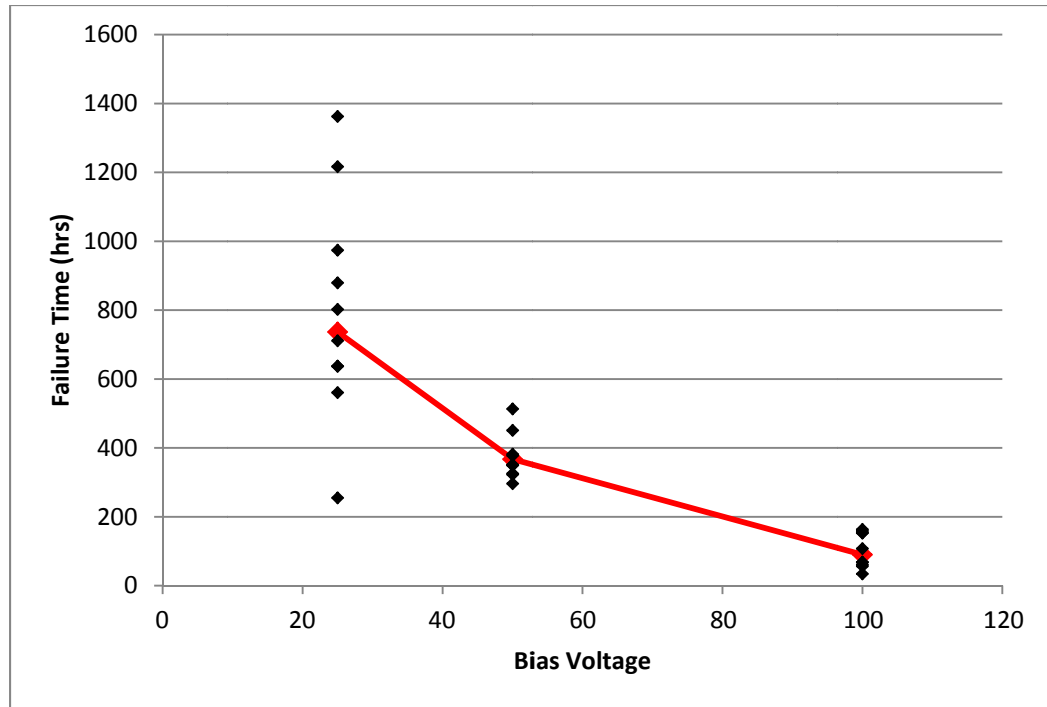


3.8: 300°C nano Ag data

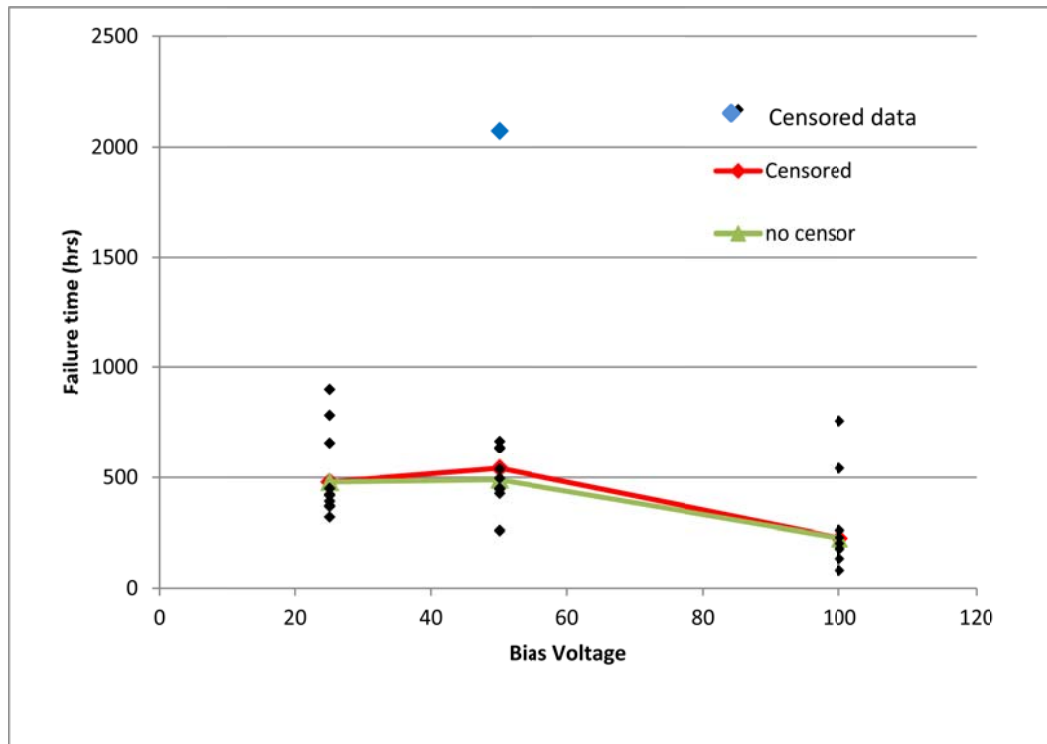


3.9: 300°C PdAg data

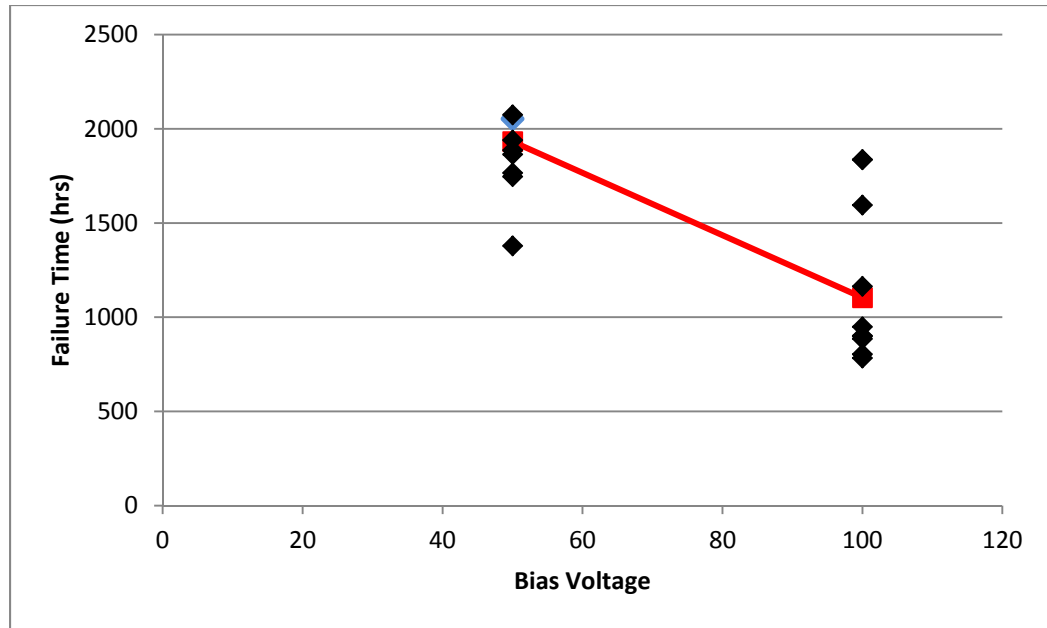
Figure 3.10 shows the 375°C thin film data. The same expected inverse relationship between bias voltage and failure time is shown here. There are no censored data points within this data set. Figure 3.11 show the 375°C Nano-Ag data. This data set shows a slight decrease in median time to failure between 25 V and 50 V tests. This is not the expected result and it is not clear why the samples failed in this manner. There is one censored sample at 50 V shown in blue on the graph. As with the 300°C thin data, the median time to failure was calculated with and without the censored data point because the censored point was over 1400 hours beyond the last failure it was ignored. Figure 3.12 shows the 375°C PdAg data. There are 3 censored data points at 50 V represented in blue but these are difficult to see because there is a failure very close to this censor point.



3.10: 375°C Thin Film Ag data



3.11: 375°C Nano Ag data



3.12: 375°C PdAg data

The median failure time are presented in Table 3.1 along with the 95% confidence intervals. The 300°C, 25 V thin film and 375°C, 50 V nano-Ag median time to failure values calculated without the censored values are used.

Table 3.1: Ag test condition and median values

Nano Silver				
Temperature	Bias Voltage	Median Failure Time(hrs)	Confidence Interval +/-	Failures/Total
300	25 V	2677.40	909.89	8/10
300	50 V	1928.10	87.34	10/10
300	100 V	579.34	21.49	10/10
375	25 V	479.00	50.72	10/10
375	50 V	489.20	44.62	9/9
375	100 V	225.99	43.82	10/10
Thin Film				
Temperature	Bias Voltage	Median Failure Time(hrs)	Confidence Interval +/-	Failures/Total
300	25 V	2812.56	273.30	6/10
300	50 V	1009.61	154.41	10/10
300	100 V	358.64	55.06	5/5
375	25 V	736.42	104.33	10/10
375	50 V	367.13	18.03	10/10
375	100 V	90.15	14.98	10/10
Palladium Silver				
Temperature	Bias Voltage	Median Failure Time(hrs)	Confidence Interval +/-	Failures/Total
300	50 V	2575.78	212.74	9/10
300	100 V	1715.37	297.38	9/10
375	50V	1932.17	112.125	7/10
375	100V	1103.90	101.73	10/10

### 3.3 Silver Migration Experimental Analysis

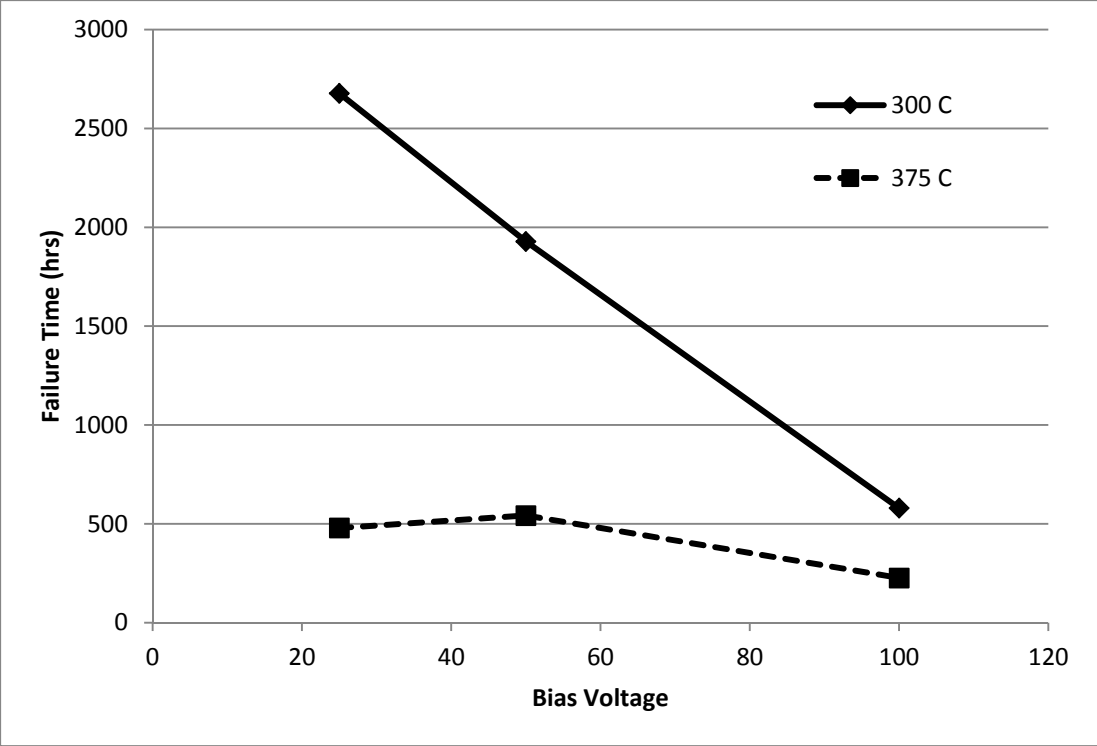
Hornung fit silver migration failure to an equation: Later Gagne rearranged that equation to solve for median time to failure. Equation 3.1 is Gagne's rearrangement of Hornung's equations. How these coefficients are determined will be discussed later, but when first looking at the data this equation will be used to highlights the trends that should be expected. Specifically there should be a direct inverse relationship between

median time to failure and bias voltage; also median failure time should have an exponential relation to temperature.

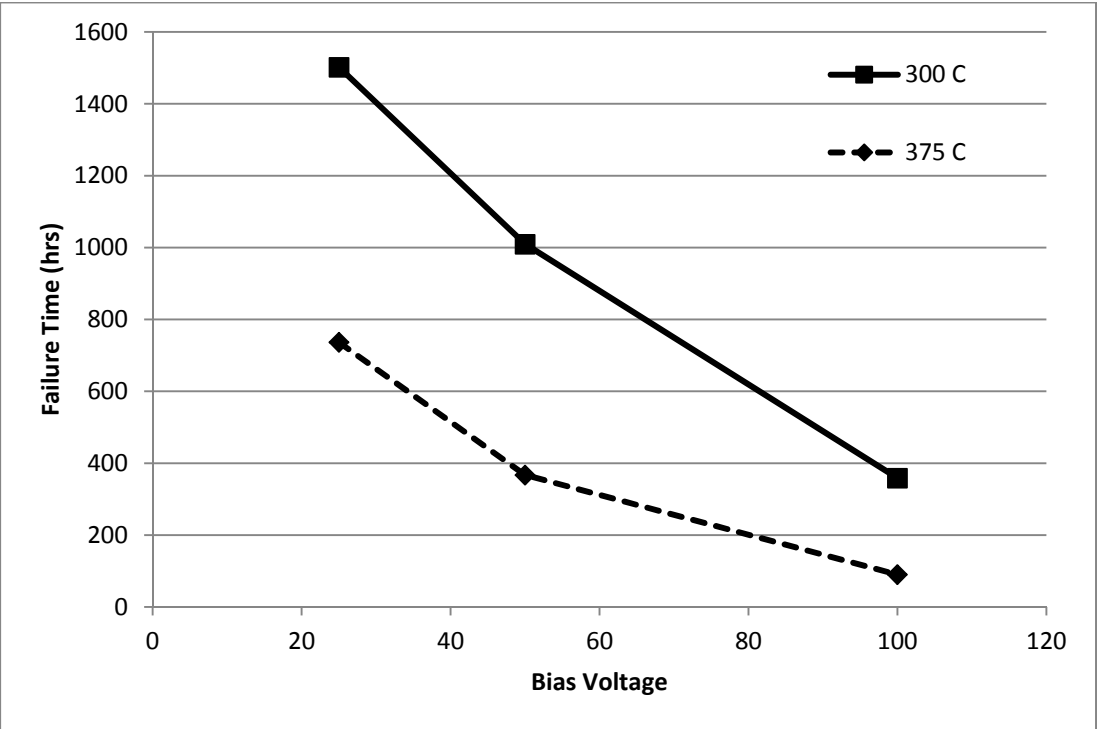
$$t_{50} = \frac{\alpha G}{V} \exp\left(\frac{\Delta H}{kT}\right) \quad [3.1]$$

$\alpha$  = proportionality constant  
 $V$  = applied voltage  
 $t_{50}$  = median time to failure  
 $G$  = gap distance between electrodes  
 $\Delta H$  = activation energy  
 $T$  = temperature in Kelvin  
 $k$  = Boltzmann's constant in eV

Figure 3.13 shows the median failure times for the nano Ag samples at each temperature. Although the exponential contribution of temperature cannot be proven, it is supported. It also can be seen that as bias voltage increases, the effect of temperature becomes much smaller. According to equation 3.1, when the natural log of bias voltage becomes larger than the activation energy over  $k \cdot T$ , the bias voltage effects will dominate over the temperature effects. The thin film data presented in Figure 3.14 also supports these conclusions showing the same trends as the nano Ag.



3.13 Comparison of 300°C and 375°C Data for Nano Ag.



3.14 Comparison of 300°C and 375°C Data for Thin Film Ag.



### 3.4 Statistical Analysis of Data

The data is not sufficient to produce a predictive model with any level of confidence, but the techniques are presented that should be followed to make that predictive model (all analysis is on the actual data). Gagne first rearranged Hornung's equation to solve for median time to failure, then taking the natural log of each side solved for the proportionality constant and activation energy using linear regression techniques. The regression was performed on the median lifetime of each voltage and temperature condition, for each material. The proportionality constant was described as a function of geometry and processing condition by Hornung, so it was solved for each material separately [17]. Equation 3.2 shows the fitted equation, this is the exact equation described used by Gagne [19].

$$\ln(t_{50}) = \ln(\alpha G) + \ln(V) + \frac{\Delta H}{kT} \quad [3.2]$$

Gagne was determining an acceleration factor based on the test voltage used to monitor the migration gaps, so he tested for a coefficient for V, but in our case we are only interested in the proportionality constant and the activation energy resulting from equation 3.3 which was used for the linear regression.

$$\mu - \ln\left(\frac{1}{V}\right) = B_0 + B_1\left(\frac{1}{T}\right) \quad [3.3]$$

$\mu = \ln(t_{50})$ ; which is the location term for the distribution

$B_0 = \ln(\alpha * G)$

$B_1 = \Delta H/k$

The calculated activation energies were expected to be within a confidence interval of each other since both materials are forms of pure silver, however this is not the case. The proportionality constants are further away but have confidence limits of 2.2 for nano Ag and 2.1 for thin film Ag so not much can be determined from these numbers.

Table 3.2: The regression results

Material	B0	B2	Adj. R2
Nano Silver	-0.498	6694.358	0.7859
Thin Film	1.67	5124.65	0.7305

$$t_{50 \text{ nano}} = 649.2 \frac{G}{V} \exp\left(\frac{0.57 \pm 0.12}{k * T}\right) \quad [3.4]$$

$$t_{50 \text{ thin}} = 5329 \frac{G}{V} \exp\left(\frac{0.44 \pm 0.11}{k * T}\right) \quad [3.5]$$

This data cannot be used for estimation of the variables in the equations. For the regression technique to be used there is an assumption of equal variance. This is assumption is not true for the data set presented.

## Chapter 4

### GOLD THERMOCOMPRESSIVE BONDING

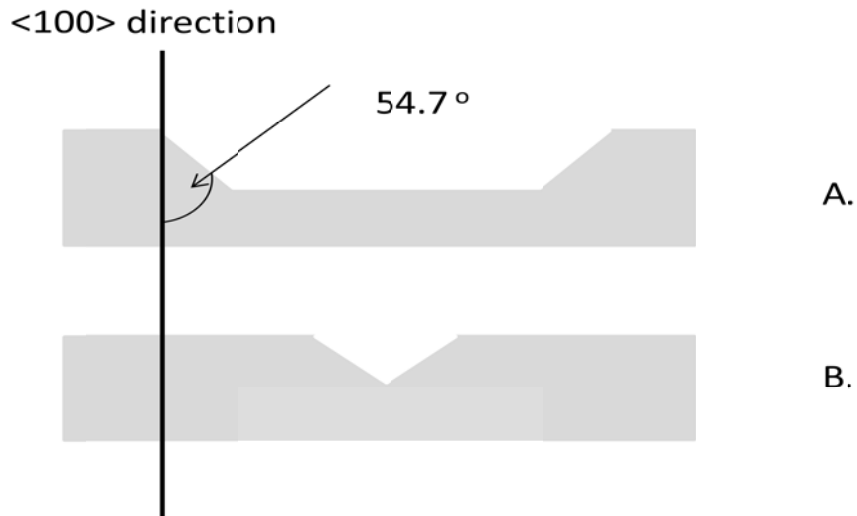
#### 4.1 Experiment set up

The goal of the experiment was to develop an Au based die attachment method using TC bonding. To achieve this, an Au plated die surface was patterned with 3  $\mu\text{m}$ , 4  $\mu\text{m}$ , 5  $\mu\text{m}$  or 6  $\mu\text{m}$  tall pyramids. The base of these pyramids were separated by a  $\sim 1\text{-}2$   $\mu\text{m}$  gap. A force between 20 kg and 40 kg was applied at temperatures between 350°C and 400°C to bond these die to an Au plated substrate. These pyramids will deform when they began to come in contact with the substrate dispersing the thin contamination layer and allowing bonding to occur. The high density of these pyramids provides a nearly uniform surface and therefore a uniform bond.

##### 4.1.1 Silicon imprint die

To produce this pyramid pattern, a silicon die was fabricated to be used as a stamp. The desired geometries were achieved using potassium hydroxide (KOH) etching of  $\langle 100 \rangle$  silicon (Si). KOH will etch  $\langle 100 \rangle$ ,  $\langle 110 \rangle$  and  $\langle 111 \rangle$  silicon at different rates; this means that anisotropic etching is possible with KOH. The actual etching rate is dependent on the concentration of KOH and can vary significantly, but generally the etching rate in the  $\langle 100 \rangle$  and  $\langle 110 \rangle$  direction is at least an order of magnitude faster than in the  $\langle 111 \rangle$  direction [45]. The  $\langle 100 \rangle$  plane is at a  $54.7^\circ$  angle to the  $\langle 111 \rangle$  plane and

90° to  $\langle 110 \rangle$ . What this means is when etching a  $\langle 100 \rangle$  Si wafer with KOH the Si will etch away until it gets to the  $\langle 111 \rangle$  plane, since this plane etches more slowly. This selective etching leaves a 54.7° flat plane. Figure 4.1 shows this, in A the etching will continue downwards until the intersection of two  $\langle 111 \rangle$  planes resulting in B, at this point etching will continue but much slower. KOH etches  $\text{SiO}_2$  and  $\text{Si}_3\text{N}_4$  much slower than any plane in Si so either of these materials can be used as an etching mask. These  $\langle 111 \rangle$  planes intersect at right angles from each other meaning they will form an inverse pyramid in Si if a small enough square opening is opened into the etching mask.

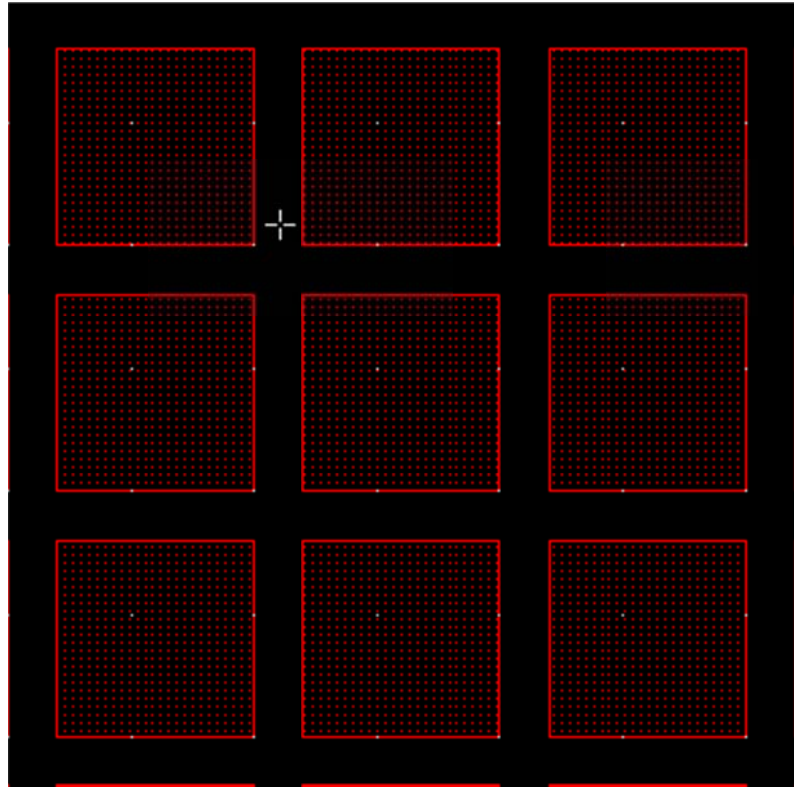


4.1 The geometry left by KOH etching.

Higher concentrations of KOH will produce faster etching rates, however these etches will be rougher. The addition of up to 5% IPA to the etching solution will help to smooth out the etched surface [46]. The concentration used in this work was approximately 30% KOH, 5% IPA and the rest  $\text{H}_2\text{O}$ .

To produce the 3  $\mu\text{m}$ , 4  $\mu\text{m}$ , 5  $\mu\text{m}$ , and 6  $\mu\text{m}$  tall pyramids that were used for testing, a photomask was designed using LASI that would produce 5 mm x 5 mm stamps of each height. Each stamp on the mask consisted of square openings 5  $\mu\text{m}$ , 7  $\mu\text{m}$ , 9  $\mu\text{m}$ ,

or 11  $\mu\text{m}$  wide placed 2  $\mu\text{m}$  apart. Figure 4.2 shows the close up of a section of one die mask.



4.2: The imprint die photomask.

Fabrication of these test die started with a  $\langle 100 \rangle$  Si wafer which was cleaned with a piranha clean (1 part 45%  $\text{H}_2\text{SO}_4$ : 2 parts 30%  $\text{H}_2\text{O}_2$ ) for 2 minutes then covered with 1  $\mu\text{m}$  of silicon nitride ( $\text{Si}_3\text{N}_4$ ) using LPCVD deposition. The wafer was then spin coated with AZ 5214 photoresist from AZ Electronic Materials at 3000 rpm for 30 second producing a photo resist thickness of  $\sim 1.5 \mu\text{m}$ . Using a Karl Suss mask aligner the photoresist was exposed to 350 W UV light for 6 sec and developed for 1 min using AZ 400 developer from AZ Electronic Materials diluted to 2:1 with water. Then the small  $\text{Si}_3\text{N}_4$  openings were etched away revealing the Si underneath. Using acetone then oxygen plasma, the photoresist was removed from the surface.

The wafer was first diced into 4 pieces because of the different heights of the pyramids. KOH etching was done in a 2 L beaker placed in a water bath heated to 65°C to control the solution temperature. The solution was made of 1330 ml of 45 wt. % KOH, 850 ml of H<sub>2</sub>O and 350 ml of IPA. The 5 μm and 6 μm die were etched for 25 minutes and the 3 μm and 4 μm die were etched for 15 minutes. After etching, the Si<sub>3</sub>N<sub>4</sub> mask was removed using a BOE etch leaving the etched Si wafer. The dies were then cut out using a dicing saw at 25000 RPM and a cutting rate of 100 mils/second.

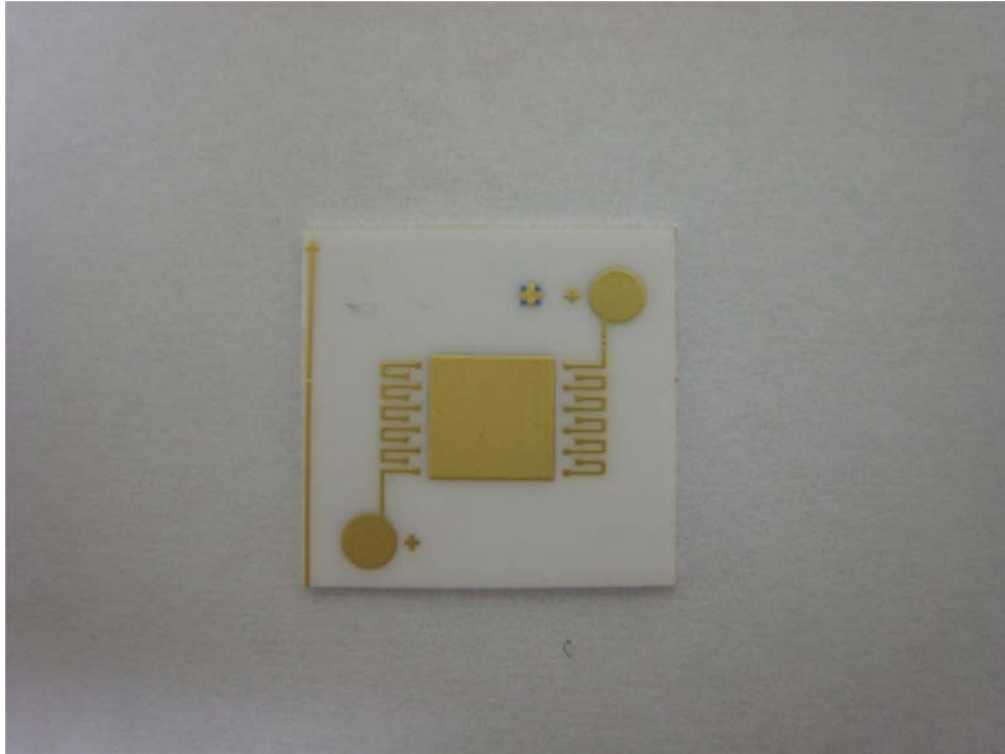
#### 4.1.2 Test die and substrate fabrication

Test die were fabricated from the polished surface of a silicon wafer. A four inch Si wafer was cleaned using a piranha clean for 5 min to remove any surface contaminates. Then 250 Å of Ti was e-beam deposited on the wafer to aid Au adhesion, the 500Å of Ti:W was sputtered to provide a diffusion barrier to the 1000Å of Au that was e-beamed deposited on top. Another 10 μm of Au was electroplated on the surface to provide a base to be imprinted with the aforementioned stamp. This wafer was then cut into 5 mm x 5 mm test die.

Also SiC test die were fabricated using a 3 in SiC wafer. This wafer was cleaned using 5 parts H<sub>2</sub>O: 1 part NH<sub>3</sub>OH: 1 part H<sub>2</sub>O<sub>2</sub> at 70°C for 20 min then rinsed in DI water for 1 min and dried with N<sub>2</sub> blown across the surface. The wafer was baked 120°C for 20 min right before metallization to dehydrate the wafer. The first layer metallization was 2000 Å e-beam deposited Cr, then 1000 Å sputtered NiCr and 1000 Å e-beam deposited Au. Au (10 μm) was electroplated for imprinting. This wafer was then cut into 3.4 mm x 3.4 mm die.

Test substrates were made from a 4 in <100> Si wafer and used the same process as the 5 mm by 5 mm Si test die, except the Au was plated to only 3  $\mu\text{m}$ . Unlike the die wafer, there were problems with the Au metallization peeling after plating, so the e-beamed Au was patterned with 4  $\mu\text{m}$  thick, 100  $\mu\text{m}$  wide lanes of photoresist between test substrates to relieve the stress induced by plating. The substrates were cut to 10 mm by 10 mm. The thin film substrates were assumed to be flat to within 2  $\mu\text{m}$  since only 3  $\mu\text{m}$  of Au was electroplated on them, so there was no extra preparation steps done to these surfaces.

Other test substrates were produced using screen printed thick film gold (Figure 4.3). Dupont 5771 ink was printed directly on the substrate then Dupont 5063 was printed on top of that. After each printing the substrate was dried at 150°C for 10 min then fired at 850°C using the profile in Figure 3.2. The 5771 ink was a Au alloy that adheres well to the substrate. The 5063 ink was a pure Au ink used to produce a pure gold bonding pad.



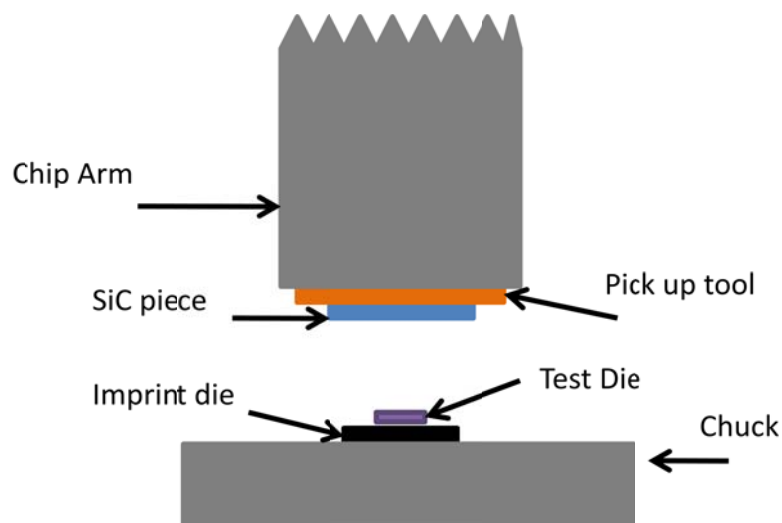
4.3: The test substrate for TC gold-gold bonding

#### 4.1.3 Gold Imprinting

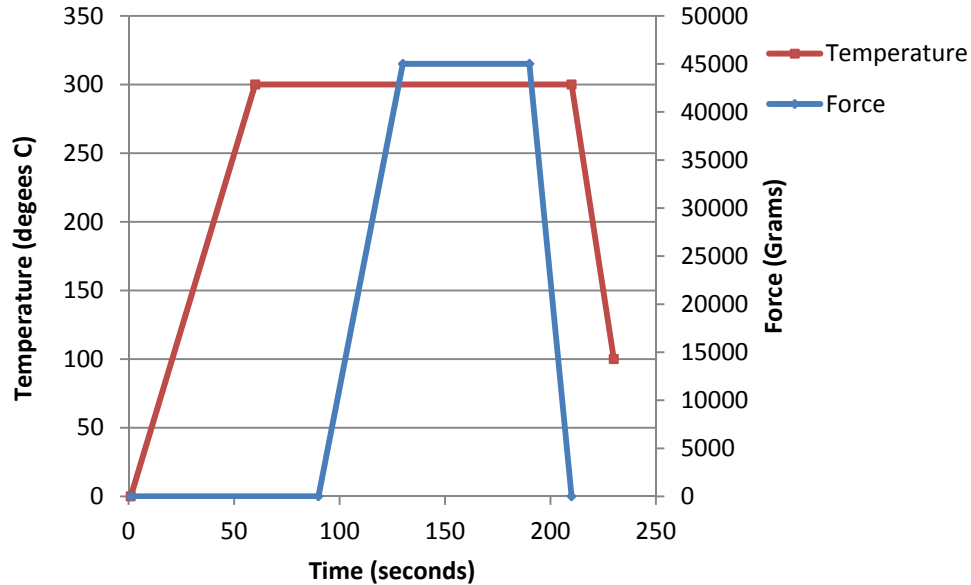
A Karl Suss FC 150 flip chip bonder was used to imprint the test die. The desired result was to transfer the pyramidal pattern of the Si stamp to the plated gold surface uniformly across the entire surface. However, producing a completely uniform surface was much more difficult than expected. Complete transfer of the pattern was never achieved, but some level of imprinting was achieved across the majority of the SiC test die. The FC 150 has a coplanarity feature to ensure parallelism between chip and substrate, however the electroplated surface of the test die did not produce a strong enough light reflection to use this feature, but bare SiC would produce a strong enough reflection (the details of this system are explained later). Therefore a piece of SiC was picked up by the chip arm and aligned with the imprint die that was placed on the chuck.



The test die was then placed on top of the imprint die and then compressed by the large piece of SiC (Figure 4.4). The time, temperature and force profile is shown in Figure 4.5. The maximum force and temperature was changed but the profile shapes were consistent. The rise and hold time used was selected to make sure both surfaces would reach the desired temperature before processing. Au will deform much easier when heated to near 50% its melting temperature, temperature were raised as high as possible [47]. Since the imprint die was Si this was limited to about 300°C.



4.4 Bonding set up on FC150



4.5: Force and temperature imprint profile

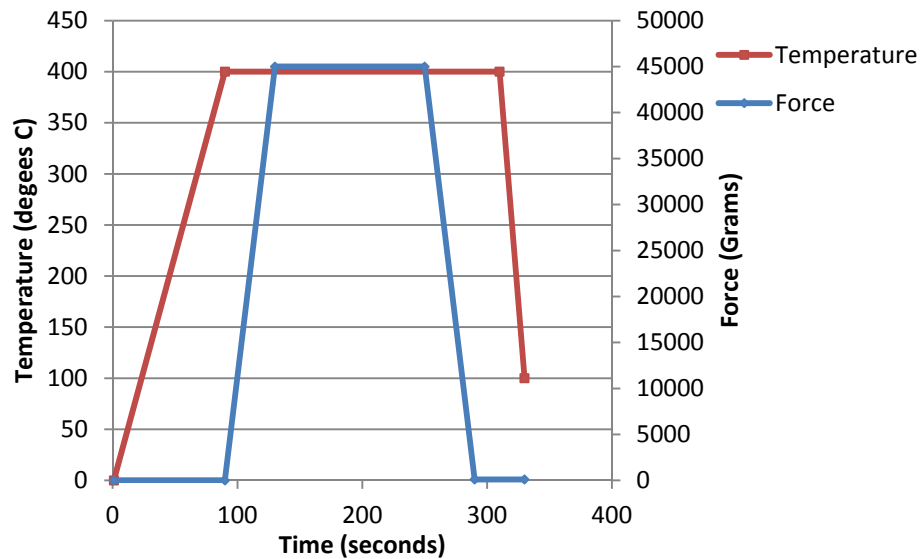
Imprinting was attempted on the Si die with varying success. An imprint could be seen on the entire perimeter of the die but not the center of the dies. It was thought possible slight bowing of the imprint or test die was the cause of this problem. Initially die were picked up directly by the chip arm using a small vacuum hole and it was thought this could be a source of the bowing. The previously described SiC piece was initially used to try to correct this bowing problem. This did improve the imprint transfer but the force of 40 kg required to imprint caused weakening of the die. This will be discussed in the results section of this chapter.

The thick film gold on the substrate produces a much rougher surface so before die attachment could be attempted the surface had to be prepared. This was done by first flattening the surface with a blank polished SiC die at 375 °C and 40 kg of force. Then the silicon stamp is imprinted on the flattened surface, the same difficulty with transfer of the pattern was experienced on the substrate as well and testing was done with and without the imprint pattern. Imprinting was also done on the screen printed ink, before

firing. This did slightly transfer the pattern; however it also caused bubbles to form between the first and second ink layers.

#### 4.1.4 Bonding

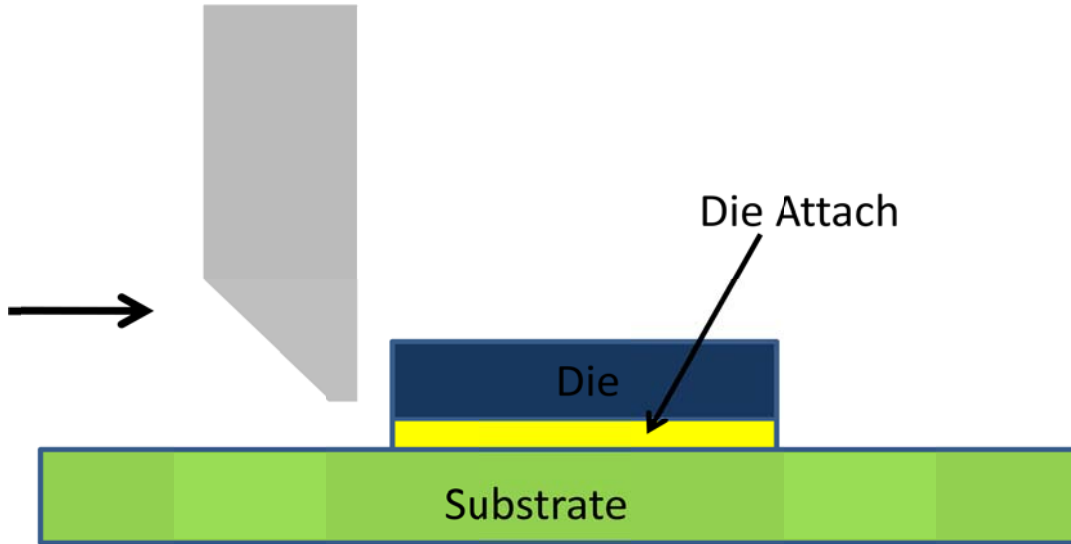
Bonding was performed with the same FC 150 flip chip bonder as mentioned before. The bonder was set up the same way as during die imprinting (Figure 4.4), except the imprint die was replaced with the substrate. Again parallelism was ensured between the large SiC plate and the substrate. Bonding forces of 20 kg, 30 kg, and 40 kg were tested at 350°C and 400°C. Figure 4.6 shows the bonding parameters except the maximum values change depending on the force and temperature used, but the shape was consistent.



4.6: Force and temperature bonding profile

Strength of the die attachment was analyzed by die shear testing using a Dage PC2400 die tester. Die shear testing is performed by pushing a flat edge attached to a load cell against one edge of a die. Force against the die is increased until the die fails.

Figure 4.7 shows a schematic of die shear testing. The height of the bottom of the testing wedge is adjustable. For these tests it was set at 2 mils.



4.7 Die shear testing schematic

## 4.2 Results

Table 4.1 shows the die shear results for Si samples on thick film Au on  $\text{Al}_2\text{O}_3$ . The analysis of data for this experiment is difficult to quantify because factors beyond just die shear strength must be considered. The major contributing factor to shear strength was the amount of die surface area that actually bonded to the substrate, however this seemed to be more dependent on the amount of die patterning success rather than the force used to bond the die and possibly the accuracy of ensuring parallelism between die and substrate, though this factor could not be quantitatively analyzed. This is believed because bonding was fairly consistent around the perimeter of the die, and this is the only area with good imprinting results. The die shear results can also be misleading because all of the Si die cracked during testing. Cracking of die introduces forces other than just shear forces, because of this, the force measured on the die shear

tester is not actually die shear force. This cracking is assumed to be caused by the stress experienced by the die in imprinting or bonding.

Table 4.1: Si die results

Si die on Al <sub>2</sub> O <sub>3</sub> substrates		
90 second at 375 C		
	Bond Force (kg)	
	30 kg	40 kg
1	19.59	43.40
2	31.79	22.31
120 seconds at 375 C		
	Bond Force	
	30 kg	
1	42.03	
90 second at 350 C		
	Bond Force	
	30 kg	
1	36.80	

These were the first group of tests and testing was not thorough because the shear strengths were much lower than desired. Since all the test die cracked in testing, SiC die were tried next. Also the screen printed substrates were not use after this because of the significant initial roughness.

The results for the second material are shown in table 4.2. Tests were performed at forces up to 40 kg however at 30kg and 40 kg the die had a problem with cracking. Every die except the first 40 kg sample showed evidence of metallization peeling.

Table 4.2 SiC die shear results

SiC die on Si substrate			
120 seconds at 400 C			
	Bond Force (kg)		
	20	30	40
1	48.78*	31.06*	>99.9
2	36.78*	22.80*	27.99*
3	40.58†	26.58*	29.30*
120 seconds at 350 C			
	Bond Force (kg)		
	20		
1	66.58†		
2	23.49*		
3	51.64*		

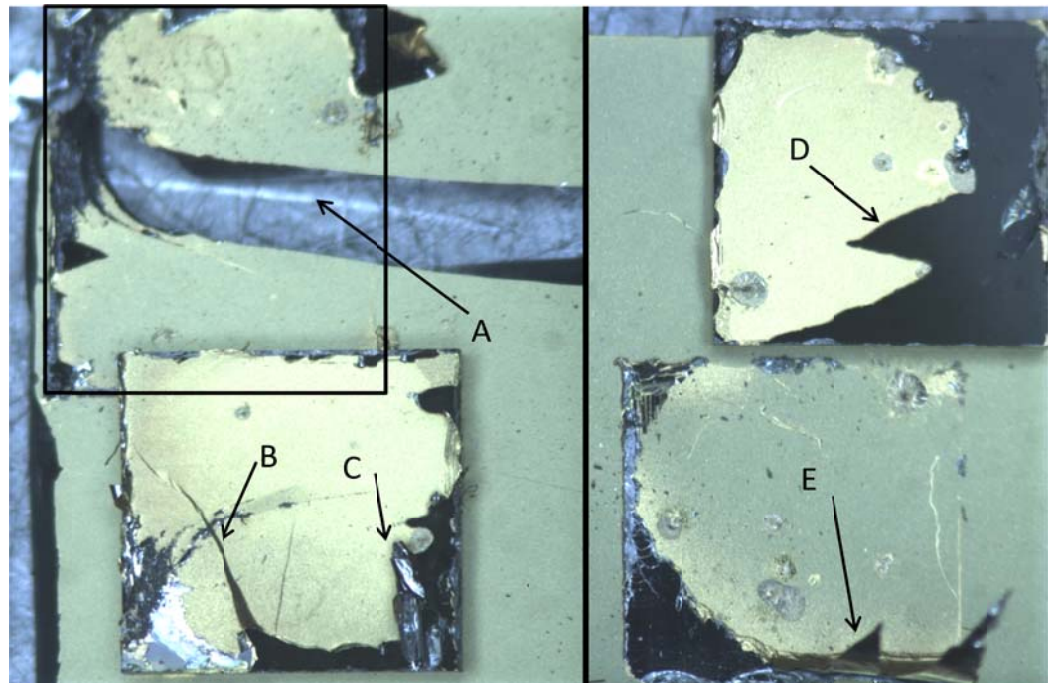
\* indicate cracked die

† indicates peeled metallization but no cracks

On initial examination, the 20 kg, 350° C samples seem to produce the best average results, the next best seems to be the 20 kg at 400° C. This is misleading; the >99 kg sample was the only 40 kg die that did not crack and all of the 30 kg samples cracked or peeled some amount of the metallization off of the SiC. Most likely the cracking was caused by the high stress put on the die during imprinting or bonding.

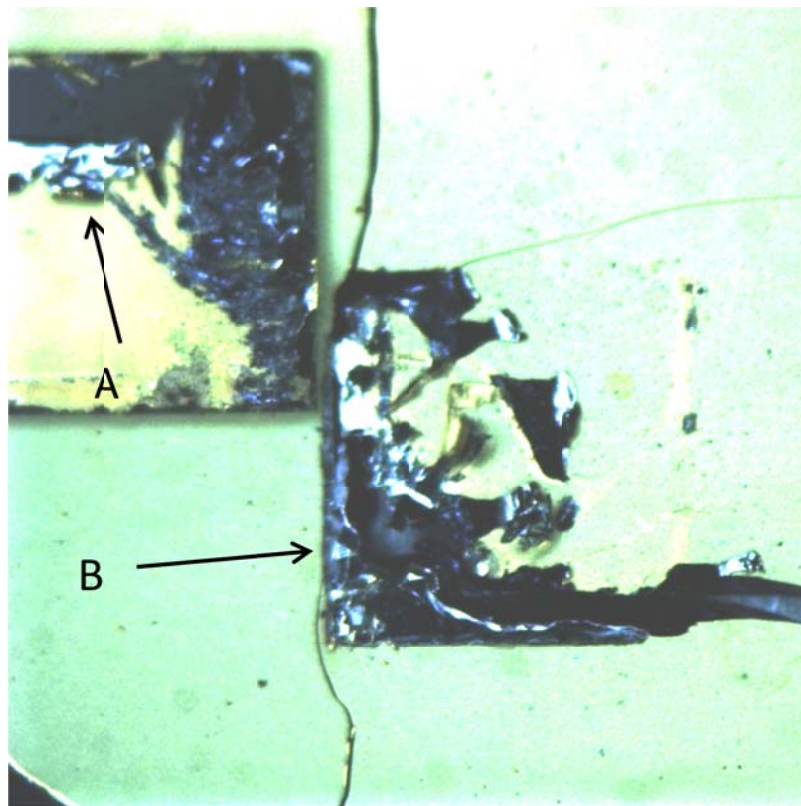
Figure 4.8 shows the surface of sample 1 (left) and sample 3 (right) from the 20 kg 400°C group. The square on sample 1 shows the outline of the die attach area on the substrate. Sample 1 had the highest shear strength and it highlights several possible additive failure mechanisms, though shear strength is incorrect because of cracking. First, (A) the substrate is cracked which occurred during testing and the crack is through the die attachment area which could cause stresses on the die other than shear stress. The second (B) source of weakening is the crack in the SiC. This crack runs out to the bottom left edge of the die, not through to the surface as expected, meaning this section of the die was sheared off and started to break free. The third (C) point is the peeling of the

metallization off of the die surface. This is not necessarily a problem, with such small bonding area there is very high stress on this section that did peel. This peeling is also the kind of failure expected even in a good die attachment, because that would mean the die attach is stronger than the die metallization. So this peeling could show that the sections that did bond bonded very strongly. A better example of peeling is given in Sample 3 (D and E). The black sections of the die show the metal peeled away on the die, but this is clearer on E which shows the peeled sections that were left. The strips left came off when separating the die after testing to get the picture. The edge was the only section pulled off during testing. A point also to note in both pictures is the large area of unaltered Au meaning only a small section of the die, mainly the edges, was attached. This is to be expected since the die imprint process used the same materials and the center of those die were not imprinted.



4.8: 20 kg bonding at 400°C samples 1 and 3

Figure 4.9 shows the failure of sample 1 from the 30 kg bonding samples. This substrate was pieced back together after testing for this picture. As with the previous Figure, A shows the peeling back of the die metallization, but B shows a section where the Si has been broken from the substrate. Again the majority of the surface is not bonded and all bonds seem to form along the edge of the die. The Si substrate shows significant cracking. The other two die from this set were cracked and it is assumed that is the cause of the lower shear strength.

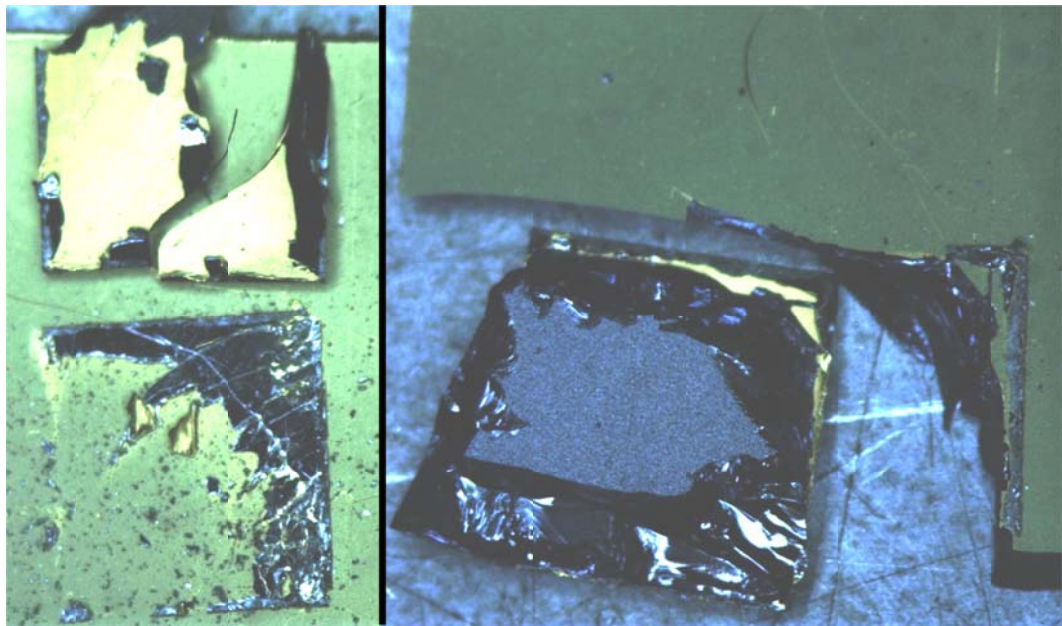


4.9: 30 kg bonding force at 400°C

Figure 4.10 shows sample 3 (left) and sample 1 (right) from the 40 kg bonding group. Sample 3 shows a die that failed completely and sample 2 failed in a similar manner. The most important feature of this die is the dark areas which is SiC from the die, this means the die was weak enough for a section of the die to break off. Again a



relatively large area of Au is not bonded. Unlike the previous samples, though there is much more bonded area and from the results of sample 1 it can be assumed that had the die not been weakened and cracked the shear strength would have been much higher. Sample 1 shows the die with a large section of Si still attached to the back. This substrate, though cracked, did not fail. It could be theorized that since the metallization peeled from some of the previous samples and not this one that a larger bonded surface area distributed the force on the die more evenly, keeping the metallization from peeling.

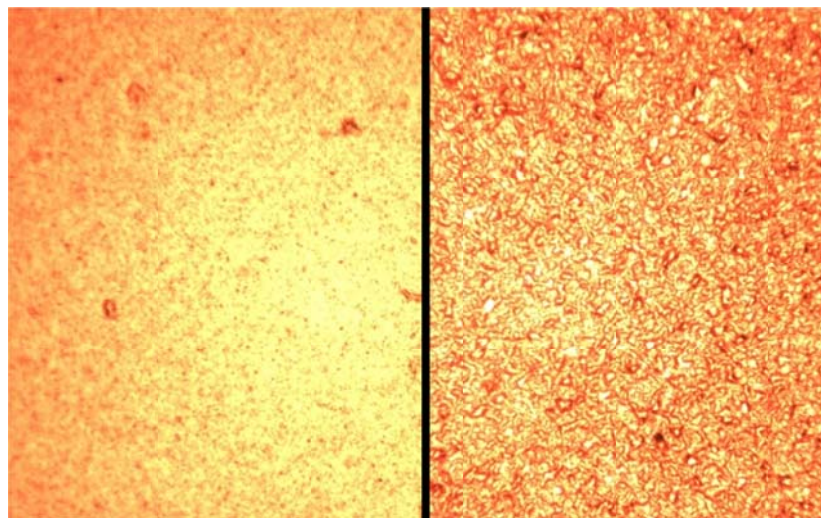


4.10: 40kg bonding force at 400°C

Since most of the die cracked, there can be no definitive analysis of the failures. The cracking of the die caused forces to act on the die, other than only shear. Though the cause of failure cannot be determined the low percentage of bonded area would have been a problem, even if the die had not cracked.

A contributing factor to the poor bonding and imprinting was the difficulty experienced when trying to ensure parallelism between the die and substrate or the die and imprint die. Though all sides of the dies bonded, there is definitely evidence of

preferential bonding to one side of the die. This was also seen in the imprinting of the die. The FC 150 coplanarity feature was mentioned previously, but here it will be explained. A beam of light illuminates a section of both the substrate and the chip arm. This light is reflected back to the microscope (this reflection is in the shape of a cross) and adjustments in the chip's planar orientation are made until the alignment images match up. Ideally to ensure parallelism between the chip arm and die, this would be done on 2-3 locations to verify planarity. Unfortunately 10  $\mu\text{m}$  of electroplated gold has a surface that is too rough for the coplanarity system and the leveling cross on this surface could not be seen. That is a main reason 3  $\mu\text{m}$  of gold was used on the substrates even though it gave less depth for deformation to occur. It is also the reason the bare SiC was required on the chip arm for leveling purposes. Figure 4.11 compares the surface of 3  $\mu\text{m}$  Au on polished Si (left) and 10  $\mu\text{m}$  Au on polished Si (right) at 40 times magnification. The bonder has a level accuracy of  $\pm 0.57^\circ$  which could be the main problem with this bonding approach, because with a 3.3 mm die there can be height accuracy from one edge to the other of  $\pm 33 \mu\text{m}$  [48].



4.11: 3  $\mu\text{m}$  and 10  $\mu\text{m}$  electroplated Au

The fact that this bonding method produced up to 66 kg bond with 20 kg of force is promising especially since not even half of the die was actually bonded. Unfortunately, there are many problems this process faces, some can be overcome easily, however it will prove difficult to find solutions to others. The problem of the SiC metallization peeling could be an isolated problem with this particular wafer metallization because this metallization on SiC die has been proven before [13] or just a result of the high forces experienced by the metallization. Work is currently being performed at Auburn University to improve the Au to SiC adhesion which could be used on future tests of this process. The problem of substrate cracking can also be solved with using a harder substrate material such as AlN or attaching the Si substrate to a ceramic substrate using high strength glue for shear testing. The problems associated with planarity may be able to be overcome with an additional feature of the FC 150 not available on the one used here. There is a laser leveling tool that can be added to the machine that may help. The difficulty in uniform imprinting is another problem without an obvious solution. One possibility is trying to fabricate imprint die out of a harder material that will not form a bond with Au so the imprinting temperature could be raised. This could be done with a gray scale mask to achieve the 3-D micromachining necessary, since KOH type etching is not possible on materials other than Si. A simpler solution may be simply to anneal the sample at 400°C for an hour or more to soften the gold and then try to imprint.

## Chapter 5

### CONCLUSIONS

Silver migration presents a significant concern when using silver based metallurgies in high temperature electronics. Since median time to failure has a directly inverse relationship to bias voltage, high voltage (>100V) applications present significant cause for concern even at moderate temperatures (200°C). With the exponential dependence on temperature, temperature quickly dominates the median time to failure; therefore using silver metallurgy in open air for devices that have extended operation conditions above 300°C would cause early device failures, not experienced with other metallurgies. If through packaging, the partial pressure of O<sub>2</sub> is lowered, Ag metallurgies may be useful.

Gold TC bonding has some very attractive properties for die attachment and it does not suffer the risk of migration in open air as Ag does, however successful die attachment using this method faces many challenges and more research is necessary to make this a viable technology.

## Chapter 6

### FUTURE WORK

#### **6.1 Silver-Indium testing**

The next step in the Ag migration testing would be to re-run the previous test with higher temperature and voltage conditions so failures will occur earlier and sufficient data should be obtained to calculate predictive model parameters. Also the addition of the Ag-In TLP bonding metallurgy mentioned in the literature review section would be very interesting to test. Lastly assembling some high voltage devices with the Ag metallurgies and observing the time it takes for the migration of silver to cause a failure would be interesting.

#### **6.2 Au TC bonding**

Another method of producing Au TC bonding test die has been initiated. This method will be to pattern a die surface with plated micro columns about 5  $\mu\text{m}$  tall and between 4  $\mu\text{m}$  and 10  $\mu\text{m}$  square separated by a small gap, between 2  $\mu\text{m}$  and 10  $\mu\text{m}$ . Again the goal of this is to deform the columns and fill some of the space between them, producing a uniform bonding surface, but unlike the previous work there will be no added stress on the die during an imprinting step.

Test die will be fabricated to produce an array of 5  $\mu\text{m}$  tall Au columns across the surface of the die. Each column is square or round with sides of equal length across the

entire surface of each die. The initial attempts to fabricate these die have been with 4  $\mu\text{m}$ , 6  $\mu\text{m}$ , 8  $\mu\text{m}$ , or 10  $\mu\text{m}$  sides each separated by 4  $\mu\text{m}$ .

These test die were fabricated on a 4 inch Si wafer that was processed just like the previous test die with Ti/Ti:W/Au metallization the same thicknesses as before. Also, another 250 Å of Ti was e-beam deposited on top of the last Au layer. The wafer was then spin coated with AZ 9245 photo resist at 2250 RPMs for 60 seconds resulting in a photoresist layer  $\sim$ 6  $\mu\text{m}$ . The photoresist was exposed using a Karl Suss photo mask aligner for 90 seconds at 350 W. The mask was developed for 120 seconds using AZ 400 developer by AZ electronic materials diluted to 3:1 with H<sub>2</sub>O for 3 minutes leaving the opening for the columns. A final 15 second O<sub>2</sub> plasma clean was done to remove any residual photoresist.

Photoresist has low adhesion strength on Au and since electroplating can produce relatively high forces on the photoresist in such small areas the Ti layer was deposited to increase the adhesion of the photoresist. To expose the gold surface for electroplating the Ti had to be etched off. Etching was done with SF<sub>6</sub> and O<sub>2</sub> ICP plasma at 700 W for four, one minute intervals to completely remove the Ti layer. Using 434 plating solution the Au was plated to a thickness of 5  $\mu\text{m}$ . After this the photoresist was striped using Acetone and O<sub>2</sub> plasma and the remaining Ti was removed using 10:1 HF etching solution.

These test die however have not been successfully electroplated at this time. The Ti layer is very difficult to distinguish from the Au layer and it is thought incomplete etching of the Ti is the reason from poor electroplating results. The incomplete etching

could either be from insufficient removal of the photo resist or insufficient etching time.

More testing will be needed to determine exactly what is needed.

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