# High Temperature Electronics Packaging Processes and Materials Development

by

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Abstract

Silicon carbide device technology is being developed for power electronics applications for use at high temperatures. In recent studies, SiC based electronics and sensors have also been demonstrated for extended operation at 500 and 600$^{o}$C, but the level of integration is at a very low level. Silicon on insulator (SOI) technology provides the ability to realize complex electronics functions. SOI rated for 250$^{o}$C is commercially available and 300$^{o}$C operation has been demonstrated. To build functional systems operating at high temperatures, packaging technology must be developed to interconnect the SOI and SiC based devices. Key elements of a high temperature packaging technology include the interconnection substrate, die attach and wire bonding. New developments in each of these areas for high temperature operation are discussed in this work.

A system-in-package (SiP) approach has been developed for SOI based devices, using thick film technology on $Si_3N_4$ ceramic substrates. Eutectic Au-Ge die attach was used with a Ti/Ti:W/Au backside die metallization for 300$^{o}$C operation. Results of die attach reliability based on shear strength are discussed after thermal storage and thermal cycling tests. Wire bonding is a cost-effective and flexible interconnect technology for HTE packaging. SOI die typically have Al wire bond pads that are not compatible with Au thermosonic wire bonding for high temperature applications. A plating process that provides a barrier layer (electroless Ni) and a wire bondable finish (electroless Pd plus immersion Au) over the Al wire bond pads has been

examined. Results of the investigation of Au wire bonding on substrate metallization and die surface metallization are also presented in this dissertation

For the SiC based devices applications at 500°C, this project examines off-eutectic Au-Sn as the die attach alloy in the Liquid Phase Transient (LPT) die attach process. Two different approaches that use thick foil Sn-Au-Sn preform and limited volume Au-Sn eutectic preform, have been investigated using. The substrate used in this project was PtAu thick film metallization on AlN substrates. A pure Au thick film layer was printed over the PtAu thick film layer. The SiC backside metallizations evaluated were Ti/TaSi/Pt/Au and Cr/NiCr/Au. Die shear tests were performed after aging at 500$^{o}$C and after thermal cycling. The shear test results and failure surface analysis are discussed

Hermetic sealing minimizes the intrusion of contamination and allow the circuit mounted inside the package to survive for a longer period of time. Two packaging approaches have been developed in this project: One path was an integrated package that uses a metalized AlN substrate as the package base. A machined AlN cavity lid was sealed to the AlN substrate to create a hermetic cavity for the die. For the second approach, a commercial off the shelf (COTS) $Al_2O_3$ package has been evaluated. In this case the metalized AlN substrate with the die attached and wire bonded could be hermetically sealed inside the ceramic package.

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# CHAPTER 1 INTRODUCTION

## 1.1High Temperature Electronics (HTE)

"High temperature electronics" (HTE), a term subject to various interpretations, is conventionally taken to mean electronics operation at temperatures beyond the MIL-STD-883 method 1011 range whose upper limit is 125°C. However, in various fields there are demands for electronics that must operate at much higher temperatures.

## 1.2 Applications and Benefits of High Temperature Electronics

Existing and envisioned needs for high temperature electronics derive from various industry and government programs. For example, applications for on-engine aircraft sensors can require operating temperatures in excess of 500$^{o}$C. Surface temperatures are 485$^{o}$C on Venus, electronics for probing and analyzing the surface of Venus must be capable of operating at such high temperatures for days or even months. The primary applications for HTE encompass automotive, aerospace, deep-well drilling, nuclear power generation and space. Table 1.1 lists a number of high-temperature applications and summarizes their temperature operating times, and other requirements [1].

Table 1.1 Applications area and Parameters for High Temperature Electronics. [1]

| Application | Temperature (°C) | Minimum Duration (hours, unless otherwise indicated | Duty | Other Environmental Factors |
|---|---|---|---|---|
| Well-logging-gas & oil (down-hole) instrumentation | 150 to 300 | Few hours-years | Intermittent/cyclical, or continuous | Temperature cycling, chemicals, pressure, mechanical stress, possibly radiation |
| Well-logging-geothermal | 150 to 400 | Few-100 | Intermittent/cyclical | Temperature cycling chemicals, pressure, mechanical stress |
| Aircraft systems-on engines & smart transducers | 300 to 500 | 1000 | Intermittent/cyclical | Temperature cycling, vibration, stress, fuel/oil/chemicals |
| Aircraft engine R & D | 500 to 600 | 100 | Intermittent/cyclical (one-shot acceptable) | Temperature cycling, shock/vibration |
| Automobiles | 150 to 250 (700) | 8000 operating, 10 years "shelf" | Intermittent/cyclical | Temperature cycling, vibration, fuel/oil/chemicals, rough handling |
| Fossil-fuel energy plants | 400 to 500 | Months-years | Continuous | Radiation |
| Nuclear reactors | 200 to 450 | Months-years | Continuous | Radiation |
| Space Exploration | 125 to 485 | Month - years | Intermittent/cyclical, or continuous | Temperature cycling chemicals, pressure, |

In HTE applications, the need for HTE arises from either "a high temperature environment" or "difficulties in disposing of the heat dissipation", sometimes both. Thermal protection systems such as dewars (vacuum-insulated vessel) and phase change materials may be used to protect conventional temperature range electronics operating in high temperature environments for limited periods of time. For longer duration applications, complex thermal management systems such as fluid cooling are used to maintain the electronics at lower temperatures. In both cases, this adds weight, bulk, cost, complexity, and maintenance issues while introducing additional failure points. These burdens may be less acceptable or less practical compared to using HTE electronics which can withstand the temperature of the environments. The ability to operate electronics at the ambient temperature will simplify the

electronics system and enable the use of electronics in some applications where it is not possible today. [2]

1.3 High-Temperature Electronics Technology and Material

Silicon and GaAs are two commonly used semiconductor materials, which have found many applications in modern electronics. However, both with relative low band-gap (the energy difference between the conduction band minimum and valence band maximum) are clearly outperformed by wide band-gap semiconductors, (SiC, GaN etc.) for use at high temperatures. SiC, which has the potential to operate above 500°C, is by far the most developed among all wide band-gap semiconductors due to the availability of high quality SiC substrates and the progress in epitaxial growth technologies. It has a wide variety of poly-types, but only 4H-SiC and 6H-SiC are commercially available. Recently, SiC has been recognized as a good candidate material for high temperature, radiation resistant, short wavelength optoelectronic and high-power/high-frequency electronic devices. Table1.2 shows the key properties of SiC in comparison to Si and GaAs [3].

Table 1.2 Key Physical & Electronic Properties of Semiconductor Materials [3]

| | 4H-SiC | 6H-SiC | GaAs | Si |
|---|---|---|---|---|
| Bandgap Energy (eV) | 3.26 | 3.03 | 1.43 | 1.12 |
| Breakdown Electric Field [V/cm (for 1000 V operation)] | 2.2E+06 | 2.4E+06 | 3.0E+05 | 2.5E+05 |
| Thermal Conductivity (W/cm · K @ RT) | 3.0-3.8 | 3.0-3.8 | 0.5 | 1.5 |
| Saturation Electron Drift Velocity [cm/sec (@ $E \geq 2 \times 10^5$ V/cm)] | 2.0E+07 | 2.0E+07 | 1.0E+07 | 1.0E+07 |

The properties that make SiC an attractive semiconductor material for these applications are [3,4,5]:

- Wide energy band-gap. Electronic devices formed in SiC can operate at extremely

high temperatures without suffering from intrinsic conduction effects because of the wide energy band-gap. Also, this property allows for unique optoelectronic applications, that include blue light emitting diodes and UV photo-detectors

- High thermal conductivity. Heat will flow more readily through SiC than other semiconductor materials. This property enables SiC devices to operate at extremely high power levels and still dissipate the large amounts of excess heat generated. Additionally, high thermal conductivity is also beneficial in maximum device packaging density.
- High breakdown electrical field. SiC can withstand a voltage gradient (or electric field) without undergoing avalanche breakdown. This property enables the fabrication of very high-voltage, high-power devices such as diodes, power transistors, power thyristors and surge suppressors, as well as high power microwave devices. High break down electric field also allows for increased isolation between devices and higher packing densities.
- High saturated drift velocity. Due to the high saturated electron drift velocity of SiC, SiC devices can operate at high frequencies (RF and microwave).

Silicon carbide device technology is being developed for power electronics applications for use at high temperatures [5, 6, 7]. In recent studies, SiC based electronics and sensors have also been demonstrated for extended operation at 500 and 600$^{o}$C.However, level of integration is at a very low level. In addition, for realization of high-power applications, SiC-based power switches are not yet commercially available [8, 9, 10, 11].

For efficient and effective integration of wide bandgap power devices into the power electronic modules, silicon on insulator (SOI) based integrated circuits are needed to interface

them with the control units. SOI technology provides the ability to realize complex electronics functions for high temperature applications. In high-temperature electronics, junction leakage is a major concern. Bulk complementary metal-oxide-semiconductor (CMOS) processes suffer from significant leakage current which contributes to higher junction temperature compared to the ambient. In SOI devices and circuits, the active device area is restricted to a Si layer of small thickness, perfectly isolated by the buried and field oxide. Buried insulator layer in SOI structure provides dielectric isolation, greatly reducing the leakage path associated with the drain and the source p-n junction diodes, which enables higher temperature operation. The threshold voltage variation with temperature is smaller in SOI devices than in bulk devices. SOI also provides improved latch-up immunity, which ultimately increases the reliability of the circuit operation at higher temperature [1, 12]. These make SOI-based circuits capable of operating successfully in the 200°C-300°C temperature range which is well above the range of conventional bulk silicon-based devices. It has been shown that the leakage current remains manageable in SOI until at 300°C [1, 12]. At elevated temperatures, SOI devices and circuits clearly outperform comparable bulk silicon. SOI rated for 250°C [13, 14] is commercially available and 300°C operation has been demonstrated [15, 16]. Power electronics for 200-300°C applications will combine SOI for control and SiC power devices [17]. SOI will be the primary technology for low power digital, mixed signal and analog electronics at temperature $\leq$ 300°C. To build functional systems operating at high temperatures, packaging technology must be developed to interconnect the SOI and SiC based devices.

## 1.4 High Temperature Electronics Packaging

Devices capable of functioning in high temperature environments need robust and reliable packaging to sustain operation throughout its entire designed lifetime cycle.

Additionally, to build any functional systems, multiple devices including passives must be interconnected. Without parallel developments in packaging technology, the advances in HTE technology will be hindered. Therefore, packaging and interconnections for these devices are important requirements for realizing any practical HTE systems. This work addresses packaging for the SOI electronic devices applications at 300°C and SiC devices applications up to 500°C.

### 1.4.1 Key Elements of HTE Packaging

The key elements in realizing HTE packaging technology are (1)substrate materials selection; (2) die and substrate metallization; (3)die attach; (4)wire bonding; and (5)hermetic sealing. Figure 1.1 is the illustration of key elements of a HTE package.

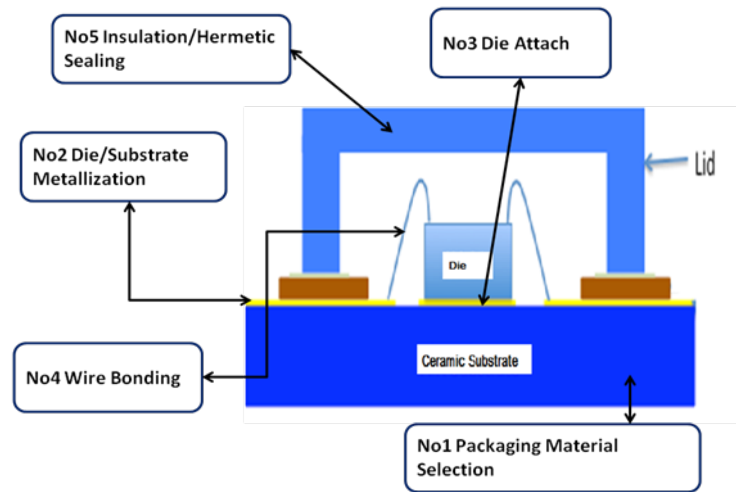



Figure 1.1 the Illustration of Key Elements of a Package

### 1.4.2 Substrate Selection

Unlike organic based packaging, metalized ceramic substrates have the potential for use at extreme high temperature. Aluminum oxide ($Al_2O_3$) is the most commonly used ceramic substrate and a wide variety of $Al_2O_3$ packages are commercially available. However, the coefficient of thermal expansion (CTE) of $Al_2O_3$ (CTE = 6.5ppm/$^o$C) is relatively high compared to that of SiC (CTE = 4.2ppm/$^o$C). With a potential thermal cycle range from room temperature

to 500$^o$C and this CTE mis-match, the strain on interfaces such as the die attach is significant and will limit the number of thermal cycles to failure. Aluminum nitride (AlN) has excellent high temperature stability, high thermal conductivity and a coefficient thermal expansion (CTE) (CTE=4.4 ppm/ $^o$C) closely matching that of SiC, which provides a ideal packaging platform for SiC based high temperature electronics. For Si die (CTE = 2.9ppm/$^o$C) [18], silicon nitride ($Si_3N_4$) provides the best CTE match. $Si_3N_4$ also has higher mechanical strength and fracture toughness than $Al_2O_3$ and AlN. For these reasons, AlN is being investigated for SiC device packaging and $Si_3N_4$ is being investigated for SOI device packaging in this research. The typical properties of these ceramics substrates are presented in Table 1.3[19]

Table 1.3 Typical Properties of Ceramic Substrates [19]

| | $Al_2O_3$ (96%) | AlN | $Si_3N_4$ |
|---|---|---|---|
| Flexural Strength (MPa) | 350 | 220 | 610 |
| Coefficient of Thermal Expansion 40-400$^o$C (x10$^{-6}$/$^o$C) | | 4.6 | 2.6 |
| Thermal Conductivity @ RT (W/m·K) | 24 | 150 | 20 |
| Volume Resistivity (W-cm)<br>20$^o$C<br>300$^o$C | <br>>$10^{14}$<br>$10^{10}$ | <br>>$10^{14}$<br>$10^{10}$ | <br>>$10^{14}$<br>$10^{12}$ |
| Dielectric Constant @ 1MHz | 9.4 | 9.6 | 8.6 |
| Dielectric loss angle @1MHz (x10$^{-4}$) | 4 | 19 | 3 |

### 1.4.3 Die and Substrate Metallization

A basic metallization scheme for a semiconductor die used in HTE technology consists a contacting layer (either Ohmic or Schottky contact), a diffusion barrier layer and a cap layer for interconnection [20]. For the die attach process success, the die backside metallization must have good adhesion and low contact resistance. The contacting layer must be made of a material that is thermodynamically stable in contact with the semiconductor/oxide, otherwise the electrically active interface thus formed cannot be stable; The barrier layer is a critical part of the

metallization and must have high resistance to oxidation and inter-diffusion because its function is to impart thermal stability to the system; The cap layer, in general, Au, must have good wettability with the die attach material in order to obtain a void-free bond joint [20]. In this dissertation, Ti/Ti:W/Au was evaluated as SOI backside die metallization for 300°C operation. For 500°C operation, the SiC backside metallization evaluated were Ti/TaSi/Pt/Au and Cr/NiCr/Au.

The ceramic substrate metallization provides a base for the die attachment and electrical interconnections for the systems. The substrate metallization intended for high temperature operation must resist surface oxidation and migration while maintaining good adhesion to the substrate [21, 22]. In this work, thick film technology is used to metalize the ceramics: Au and Pt/Au conductive metal pastes were deposited in patterns defined by screen printing onto a ceramic substrate and fired using a high temperature profile (peak temperature 850°C). During the firing process, the inorganic binder molecules in the metal paste migrate to the metal/substrate interface and form reactive binding chains.

### 1.4.4 Die Attach

Die attach is the process of attaching the chip to the substrate or the semiconductor package. It is a fundamental element of any packaging approach. Commonly, there are two common die attach processes, adhesive die attach and eutectic die attach. For high temperature applications, Au based alloys have been proposed as promising die attach materials for high-temperature device packaging because of their good compatibility with the die and substrate metallization, excellent electrical conductivity, thermal conductivity and corrosion resistance. In this dissertation, eutectic Au-Ge (88/12 wt%) preforms have been investigated as die attach material for SOI die packaging for 300°C operation, and a liquid transient phase die attach

bonding process using Au-Sn (80/20 wt%) preform or off eutectic Sn-Au-Sn thick foil were developed for SiC devices at 500$^{o}$C operation.

### 1.4.5 Wire Bonding

Wire bonding is an electrical interconnection technique using thin wires and a combination of heat, pressure and/or ultrasonic energy, where the two metallic materials (wire and pad surface) are brought into intimate contact. [23] It is generally considered the most cost-effective and flexible interconnect technology, and is used to assemble the vast majority of semiconductor packages [24]. Commonly aluminum or gold wires are used for wire bonding, but when the operation temperature is increased to more than 200 °C, Al becomes weak. On the other hand, Au possesses much higher strength at high temperature than Al. In addition, Al and Au are incompatible because Au reacts with Al, forming brittle intermetallics at high temperature. The reaction accelerates with increasing temperature and Kirkendall voids are created if gold-aluminum diffusion is excessive, which will lower the physical and mechanical properties of the bond [25, 26]. In this study, the bonding process was investigated and the suitable process parameters were identified for 1mil diameter Au wire and Al/Ni/Pd/Au die wire bond pads on SOI using thermo-sonic wire bonding for 320°C applications.

### 1.4.6 Hermetic Sealing

Hermetic sealing protects the electronic devices from mechanical damage and intrusion of the atmosphere contaminants. One of the hermetic packaging schemes that have received most use for high temperature is multilayer ceramic packages [27, 28].Two types of approaches were investigated in this project for hermetic sealing: LTCC (low temperature co-fired ceramic) AlN packages and commercially available 40pin hybrid $Al_2O_3$ packages with a metalized $Al_2O_3$ lid. Key features of the LTCC AlN packages construction evaluated in this project were metalized

AlN substrate, the LTCC frame, screen printed thick film Au seal ring and machined AlN cavity lid.

## 1.5 Research Outline

The goal of the project was to develop the assembly materials and processes for packaging SiC and SOI electronics, which will be used in high temperature environments. In Chapter 2, material properties and device technology related to HTE are briefly discussed. Key issues in packaging of HTE are reviewed in Chapter 2, including: substrates technologies, die thin film metallization, die attach materials and processing, wire bonding, and hermetic lid sealing.

Chapter 3 describes an investigation of eutectic Au-Ge die attach for the Silicon-on-insulator (SOI) die packaging for applications at 300°C, including substrates technology, die metallization, die attach bonding process. Results of die attach reliability based on shear strength are discussed after thermal storage and thermal cycling tests. Results of the investigation of Au wire bonding on substrate metallization and die metallization are also presented in chapter 3, including wire bonding parameters, bond-ability and reliability based on pull and shear strength tests. Failure analysis after reliability testing was also performed.

Chapter 4 presents details of the Au-Sn liquid transient phase (LTP) die attach technology for SiC packaging at 500°C operation, which includes die attach materials, suitable brazing processes, SiC die and AlN substrate metallization preparation. Chapter 4 also reports the mechanical strength and investigations of the braze joint during high temperature storage and thermal cycling tests. Failure analyses after reliability testing are presented.

Chapter 5 reports the details of hermetic lid sealing processes for HTE ceramic packages, including AlN substrate metallization, LTCC AlN package preparation, and lid sealing profiles. Results of the gross leak testing were also included.

# CHAPTER 2 BACKGROUND

This chapter presents the background information related to the topics that will be covered in this dissertation. Packaging considerations for HTE are reviewed. Key issues in HTE packaging will also be discussed in this chapter including: die thin film metallization, substrate technologies, die attach materials and processing, wire bonding, and hermetic lid sealing.

## 2.1 Packaging Considerations for HTE

In the selection of proper packaging and interconnection materials for high temperature applications, the critical issues that must be considered are [29,30, 31]:

A. Thermo-mechanical compatibility: Coefficient of Thermal Expansion (CTE) mismatches between the die and the substrate as well as between the different packaging components will cause stresses during assembly and during operation. With higher operating temperatures, the temperature span ($\Delta T$) associated with the thermal cycle increases, resulting in higher stress/strain on materials with mismatched CTEs. The higher stress/strain levels will lead to a lower number of thermal cycles to failure. Therefore, the thermal expansion mismatch between the die, the substrate, and other packaging components should be small at all temperatures to minimize thermal stresses.

B. Thermal conductivity: Poor thermal conductivities can mean poor ability to dissipate heat and cause excessive temperature differences between parts of the circuit. Therefore, substrate, metallization, and die attach thermal conductivity must be maximized. The fact that the thermal conductivity of packaging materials decreases with increasing

temperature must be considered, and thermal designs must be based on materials at the highest operating temperature expected for the system.

C. Electrical properties: With increasing operating temperature, the electrical conductivity of metal decreases, and the voltage blocking capability/insulation resistance of the dielectrics decreases as well. These factors must be considered in simulations of system performance at elevated temperatures.

D. Chemical compatibility: Inter-diffusion in metals can cause Kirkendall voiding due to the differential diffusion rates of one metal into another. Many metal couples can form inter-metallic compounds, which are often brittle and have different properties from those of the individual metal. Oxidation of metals will reduce material electrical conductivity. Moreover, excessive oxidation can lead to structural/mechanical failure. Therefore, die attach and wire bonding materials, as well as die and substrate metallization should have good oxidation resistance, minimum inter-diffusion and inter-metallic formation.

E. Hermeticity: Hermetic seal prevents gases and liquids from entering the package cavity where the die is mounted. For high temperature and harsh environment packaging, the package should have atmospheric integrity to protect the die from environmental elements.

## 2.2 Thin Film Die Metallization

Multilayer thin film metallization compatible with HTE packaging and interconnecting techniques (wire bonding and die attach) are commonly used for die metallization (The term "thin film" here refers more to the manner in which the film is deposited as opposed to the actual thickness of the films.). As it has been stated in the introduction chapter, the basic metallization scheme consists of three layers: (1) the bottom layer provides adhesion to the die and serves as

Ohmic or Schottky contact if required; (2) the middle layer acts as a diffusion barrier between the contact layer and the cap layer; and (3) the cap layer is the interconnection layer. An effective chip metallization should provide the following features [32]:

• Good adhesion to the wafer passivation and the contact (Ohmic or Schottky)

• Low contact resistance

• An effective diffusion barrier

• A metal stack that is compatible with wire bonding and braze metallurgy

• High temperature reliability

### 2.2.1 Evaporation and Sputtering

Thermal evaporation and sputtering are the two most important physical vapor deposition (PVD) methods employed for depositing multilayer metal thin films. The main principle is to convert the source material (target) into vapor by sputtering or evaporation. The vapor passes across a region of low pressure from its source to the substrate and subsequently condenses on substrate surfaces to form the thin films [33,34,35,36].

In thermal evaporation, the conversion into vapor phase is achieved by applying heat to the source material. High vacuum is required in the evaporation method to allow the atoms/molecules to evaporate freely in the chamber. There are two widely used evaporation technologies: electron-beam evaporation (E-beam) and resistive evaporation. In electron beam evaporation, a high kinetic energy beam of electrons is aimed at the target for evaporation. Upon impact, the high kinetic energy is converted into thermal energy, heating up and evaporating the target material. Resistive heating uses a big current passing through the resistor (the target material is put or attached to the resistor) to generate high temperature, converting the target material into vapor state. Traditionally the resistors are made by W($T_m$=3380℃),

Ta(Tm=2980°C) or Mo(Tm=2630°C) which have a high melting temperature. A schematic diagram of a typical system for e-beam evaporation [35] is shown in the Figure 2.1.

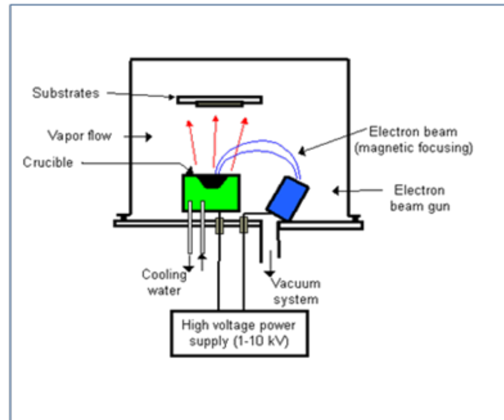
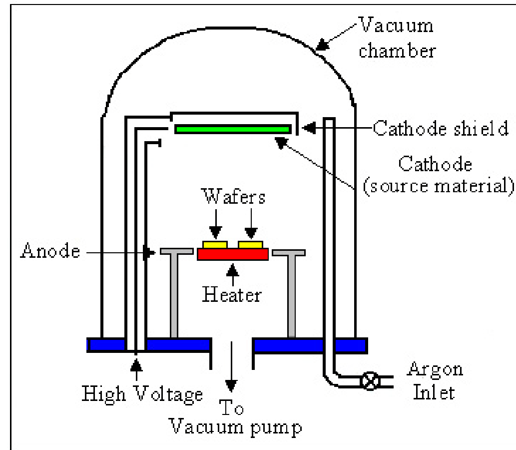



Figure 2.1 Typical system of e-beam evaporation of materials [35]

Sputtering is performed in a vacuum chamber filled with noble gas, commonly Argon. The source material to be deposited (target) is negatively charged as the cathode. By adding a high voltage DC or RF power source, the argon will enter a plasma state and $Ar^+$ will move toward the cathode with high speed. The high-energy impact of the ions induces atoms at the surface of the target to be ejected or sputtered. These sputtered atoms will then form a thin film coating on the substrate after condensing [35,37]. Since the source atoms are released by impinging high-energy ions, sputtering thin film metallization deposition uses much lower temperature than evaporation. Figure 2.2 is a schematic diagram of plasma sputtering deposition system [37]




2.2 Typical Plasma Sputtering System [37]

2.2.2 Gold Electroplating

Gold is the most common conductor material used in thin film metallization, because of the ease of wire and die bonding and the high resistance of the gold to oxidation and corrosion. In the thin film technology, it is a common practice to sputter a very thin layer of gold which is only a few hundred Å (or less) to a few thousand Å and to build up the thickness of gold film by electroplating. This is considerably more economical and results in much less target usage [34]. The details of gold electroplating process used in this research will be discussed in chapter 3 & 4.

2.3 Substrate Technology

Substrates provide electrical interconnection between various active and passive elements, mechanical supports for the components and a path for heat removal from the devices. Organic substrates due to their relatively low glass transition point ($T_g$) and decomposition temperatures are not suitable for temperature in excess of 250°C. Ceramics offer the greatest potential for high temperature packaging and interconnection technology. Commonly used substrate materials include aluminum oxide ($Al_2O_3$), aluminum nitride (AlN), and silicon nitride ($Si_3N_4$). The typical properties of these ceramics substrates are presented in Table 1.3 in the first Chapter, (section 1.4.2) Depending on the materials' properties, compatibility, and packaging

requirements, there are three basic technologies that can be used to form metallurgy on ceramic substrate: thick film technology; thin film technology, copper metallization technology.

Screen printing of thick film paste is among the earliest methods employed to form metallization on ceramic substrates. The metallization process sequentially consists of screen printing, drying and firing. Thick film paste materials are usually composed of (1) fine metal (such as gold) powder, (2) inorganic binder (such as metal oxides), and (3) organic vehicle (solvent and polymer). Screen printing is the first step in this technique: thick film paste is pushed through a patterned mesh screen onto the ceramics with thickness control [38]. During the following drying process ($2^{nd}$ step) at 150 °C, the solvent portion of the organic vehicle evaporates and the paste becomes a semi-solid phase mixture of metal powder, polymer and binder. In the following firing process the polymer decomposes, and the inorganic binder molecules migrate to the metal/substrate (e.g. Au/ceramic) interface and form reactive binding compounds. The binder may also be a glass that mechanically interlocks with the substrate. Precious metal thick-film metallization (on ceramic substrates) have been used for hybrid-packaging conventional (room temperature to 150 °C) electronics. In this project, Au and Pt based thick film materials, which are processed at high temperatures (850 °C), have been used to produce metalized ceramic substrate for high temperature operation [39].Screen printing is also used to deposit refractory metals, typically molybdenum or tungsten to ceramics. These require very high temperature firing in $H_2$. Gold and nickel can be post-plated on top of the refractory metal thick film to allow components mounting and wire bonding.

In thin film technology, multilayer thin film conductor materials are deposited by vacuum deposition (such as sputtering and evaporation as described in section 2.2.1), after which fine-line patterns can be produced on the ceramic substrate by photo-lithograph and etching, which is

suited for high density interconnection and high frequency application. But due to inter-diffusion at elevated temperatures, multilayer composite metallurgy leads to reliability issues. Effective diffusion barriers are a limiting factor in the use of thin films at high temperature [30, 34].

Thick and thin film technologies are limited in their ability to handle large currents. Copper metallization technologies provide considerable advantages when packaging high power circuits. There are three basic technologies available: direct bond copper (DBC), active metal braze (AMB), and various methods of plating copper directly to the ceramic [34].The thick layer of copper is capable of handling large currents without excessive voltage drops and heat generation, and also allows the heat to spread rapidly outwards from the devices.

## 2.4 Die Attach

### 2.4.1 General Considerations for HTE Die Attach

Die attach provides mechanical, electrical and thermal connection between the SiC die and the substrate. The ideal die attach materials for HTE packaging should have the following properties [21, 29,32]:

- Good adhesion to the die and the substrate.
- Good corrosion resistance.
- High thermal conductivity, so that heat dissipated from the devices and the thermal expansion difference between the die and the substrate can be minimized.
- An appropriate processing temperature and good thermal stability to fit into the die bonding process.
- Self-resilience to provide good stress relaxation behavior so that induced internal stress is reduced to low levels.

2.4.2 HTE Die Attach Options

Attachment of the die (chip) to the substrate with conductive polymeric adhesives is a commonly used method for conventional temperature ranges. These die attach materials have the advantages of low processing temperature and relatively low cost, however, they are not suitable for applications above 250°C due to their relative low decomposition temperature [30, 40]. Epoxies are typically limited to a maximum continuous operating temperature of 150°C-200°C. Silver-filled polyimide has been used long term to 250°C-275°C. Unfilled polyimide has much higher glass transition and decomposition temperature, but much lower thermal conductivity than metal-filled versions, which is important in dissipating heat from the die to keep junction temperature lower for high temperature electronic systems [41].

For higher operating temperature ranges, there are generally three options for HTE die attachment: soldering, brazing and transient liquid bonding. The selection of bonding materials and/or process will depend on the compatibility with the terminal metallization of the die and the operating temperature requirements.

Solders are conventionally metal alloys, coming in the form of either a solder paste amenable to screen printing or a preform (sheet) [30, 42, 43]. Soldering is a process in which die and substrate are bonded together by melting and flowing the solder alloy into the joint. Solders based on Au and Ag are often called “hard solder, whereas solders based on Pb, Sn and In are called “soft solder”. The terms soft and hard are taken to mean the mechanical behavior of the alloy. Hard materials have higher strength and lower elasticity than soft materials; they also exhibit less stress relaxation from thermal cycling to high temperatures. For instance, gold based alloys such as Au/Sn, Au/Ge, and Au/Si can offer high mechanical strength, but they do not provide good stress relief. Consequently, matching the CTE of the die and substrate becomes an

increasingly crucial design criterion as the die size and the operating temperature increase. There is no fundamental difference between brazing and soldering. According to the usual metallurgical definition, soldering and brazing are distinguished by the melting point of the filler metal. Typically, filler melting below 400C are considered solders and those above are considered brazes. To prevent oxidation, brazing is normally conducted in an inert gas or in a vacuum [30, 42,43]. The melting points of several high temperature solders and brazes are given in Table 2.1 [44,45,46].

Table 2.1 Melting Points of Common solder and Braze Alloy Materials [44,45,46]

| Alloy Composition (WT%) | Solidus (°C) | Liquidus (°C) |
|---|---|---|
| Sn 63, Pb 37 | 183 (eutectic) | |
| Sn 95, Pb 5 | 235 | 240 |
| Pb 92.5, Sn 5, Ag 2.5 | 280 (eutectic) | |
| Au 80, Sn 20 | 280 (eutectic) | |
| Pb 92, In 5, Ag 3 | 300 | 310 |
| Pb 95, Sn 5 | 310 | 314 |
| Au 88, Ge 12 | 361(eutectic) | |
| Au96.76, Si 3.24 | 363 (eutectic) | |
| Au 82, In 18 | 451 | 485 |
| Ag 45, Au 38, Ge 17 | 525 (eutectic) | |
| Ag 50, Cd 18, Zn 16.5, Cu 15.5 | 625 | 635 |
| Ag 78, Cu28 | 780 (eutectic) | |
| Au 82, Ni 18 | 950 (eutectic) | |

Liquid Transient Bonding (LTB) [30,47]

Transient-liquid-phase (TLP) bonding is a material joining process that can produce a high quality bond at the interface of the parts to be joined with no remnant of the bonding agent. The four discrete stages of the TLP bonding process are (1) heating, (2) dissolution and widening, (3) isothermal solidification, and (4) homogenization [48]. A schematic illustration of the process, shown in Figure 2.3 [49,50], indicates that by placing a thin interlayer of an alloying metal containing a melting point depressant (MPD) between the two pieces of parent metal to be

joined and heating the entire assembly, a liquid interlayer is formed. The liquid may form because the melting point of the interlayer has been exceeded, or because reaction with the parent metal results in a low melting liquid alloy. The liquid then fills voids formed by unevenness of the mating surfaces and can sometimes dissolve residual surface contamination. With time the MPD diffuses into the parent metal resulting in isothermal solidification. Upon cooling there remains no trace of the liquid phase, and ideally the joint becomes indistinguishable from other grain boundaries.

The interlayer rich in a melting point depressant can be provided by foils, electroplated, sputter coats, or any other process that deposits a thin film on the surfaces that need to be bonded. The two most important stages in terms of joint quality are the isothermal solidification and the homogenization stages; coincidently, it is also these stages that require the longest time for completion since they are controlled by solute diffusion in the solid. [51] In systems with a low solubility limit, the isothermal solidification stage becomes longer. Conversely, in some systems with a high solubility limit, the homogenization stage requires longer time for completion. The major advantage of TLP bonding is that it is an isothermal process, the thermal stresses formed between the die and substrate are minimal. When TLP is possible, it generally produce joints of excellent stength and high reliability.

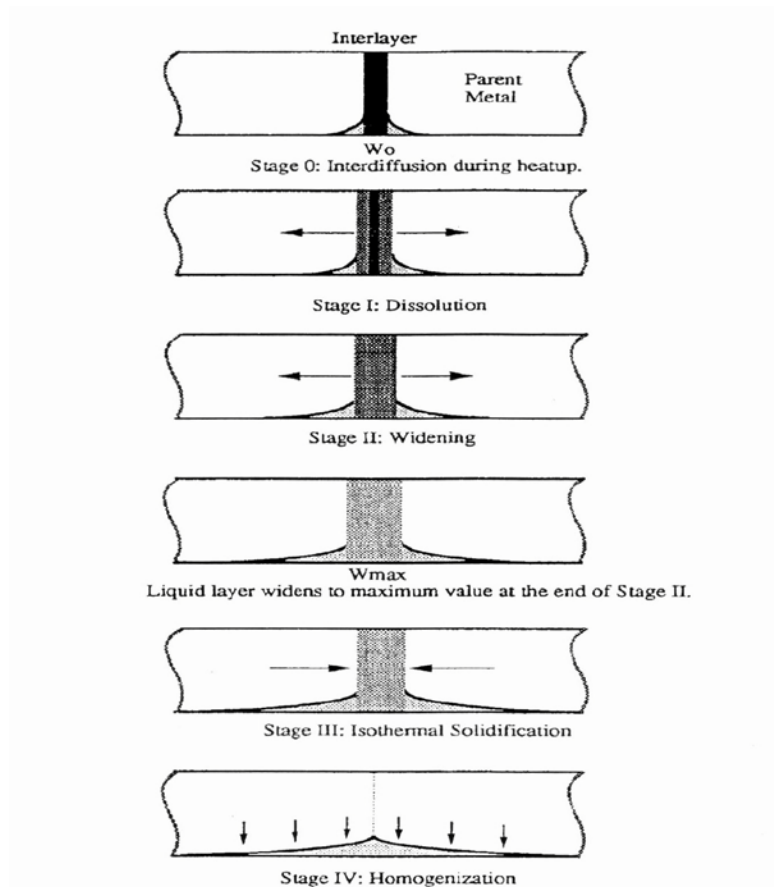



Figure 2.3 Schematic Illustration of TLP bonding process [49]

### 2.4.3 Die Shear Testing

Die shear testing is a widely used process to determine the strength of adhesion of a die to the substrate. The purpose of die shear testing is to assess quality of the die-attach process as well as the integrity of the bonding materials used in the process. A typical die shear tester consists of: (a) a mechanism that applies the correct load to the die, (b) a die contact tool which applies the force uniformly from one end of the edge to the other, (c) provisions to ensure that the die contact tool is perpendicular to the die attach plane, in the mean time, the die edge and contact tool are aligned in parallel to each other [36]. During testing, the shearing arm moves the contact tool horizontally against the die, subjecting the die to a stress that is parallel to the plane of die attach substrate, resulting in a shearing stress between: 1) the die-die attach material

interface; and 2) the die attach material-substrate interface. The force needed to shear a die off its pad, known as the die shear force, is then measured by the shear tester. A typical test set-up for die attach shear testing is shown in Figure 2.4[52].

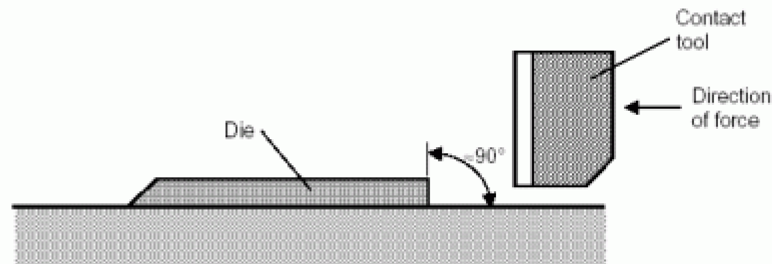



Figure 2.4 Test Set-up for Die Attach Shear Testing [52]

2.5 Wire Bonding

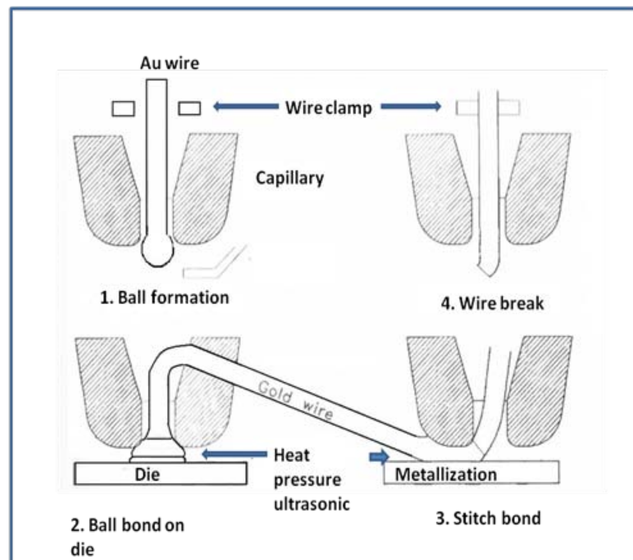
Wire bonding is a process used to make the electrical connections from the bond pads on the top surface of the die to the substrate or a lead frame, from package terminals to substrate, or from one point on the substrate to another. Wire pull test and bond (ball) shear test are the two most universally accepted methods for monitoring the quality of the wire bonding operation. A critical factor that must be considered when operating at elevated temperatures is the material interactions between the wire and the pad to which it is being bonded, because of the brittle inter-metallic phases that could form.

There are two basic forms of wire bonding: ball bond (Figure 2.5) and wedge bond (Figure 2.6). Depending on bonding agent (heat and ultrasonic energy), the bonding process can be defined to three major processes: thermo-compression bonding (T/C), ultrasonic bonding (U/S), and thermo-sonic bonding (T/S) [53].

2.5.1 Ball Bonding

During ball bonding, a free air ball (FAB) is first formed by melting a small portion of the wire extending beneath the capillary through an electric arc called electronic flame-off

(EFO). The FAB is then pressed to the bonding pad on the die, and adequate amounts of pressure, heat, and ultrasonic forces are applied to the ball for a specific amount of time, forming the initial metallurgical weld between the ball and the bond pad. The capillary is then raised and repositioned over the second bond site on the substrate; a precisely shaped wire connection called a wire loop is thus created. Deforming the wire against the bonding pad makes the second bond (stitch bond). Then the wire clamp closes, and the capillary ascends once again breaking the wire just above the wedge, an exact wire length is left for the EFO to form a new ball to begin bonding the next bonding cycle [53,54,55]. Ball bonding is generally used in thermo-compression (T/C) or thermo-sonic bonding (T/S) process and this technique is used extensively for Gold wire bonding. However, Ball bonding is not recommended for Aluminum wire because Al wire doesn't form a uniform FAB during flame-off unless an inert gas is used. Figure2.5 (a) shows the typical Au wire ball bonding sequence and (b) is schematic representations of the geometry of a ball bonding [34,56].




2.5 (a) Typical Au Wire Ball Bonding Sequence [34]

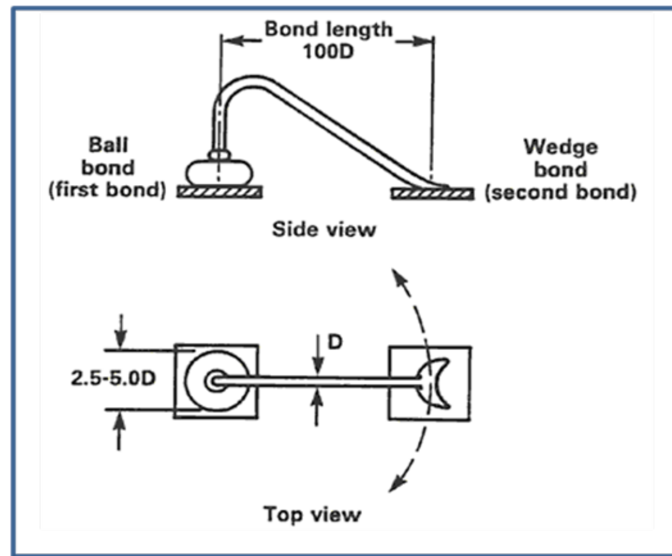
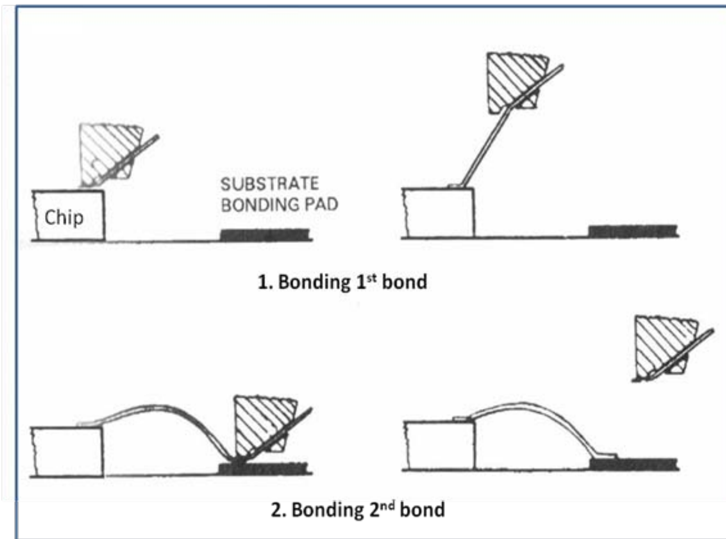



Figure 2.5 (b) Illustration of the Geometry of Ball Bonding [56]

2.5.2 Wedge Bonding

Wedge bonding is named based on the shape of its bonding tool. In this technique, the wire is fed at an angle usually 30-60$^{o}$ from the horizontal bonding surface through a hole in the back of a bonding wedge. By lowering the bonding wedge onto the bond pad, the wire is pinned against the pad surface and an U/S or T/S bond is performed. Next, the wedge rises and executes a motion to create a desired loop shape. At the second bond location, the wedge descends, making a second bond. The wire is then broken off by clamping and movement of the wire [54, 55, 56]. Wedge bonding technique can be used for both aluminum wire and gold wire bonding applications. The principle difference between the two processes is that the aluminum wire can be bonded in an ultrasonic bonding process at room temperature, whereas gold wire wedge bonding is performed through a thermo-sonic bonding process with heating up to at least 150$^{o}$C. Figure2.6 (a) shows the Al wire ultrasonic wedge bonding sequence and (b) is schematic representations of the geometry of ultrasonic wedge bonding [34, 56].




2.6 (a) Ultrasonic Wedge Bonding Sequence [34]

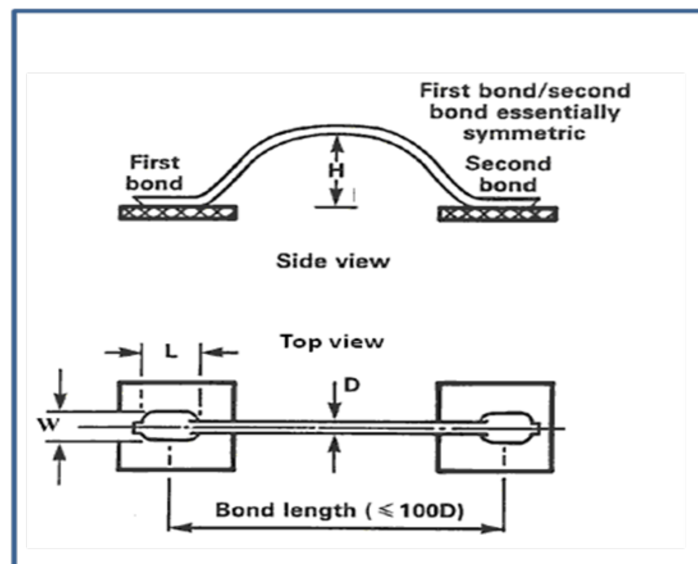



Figure 2.6 (b) Schematic Illustration of the Geometry of Wedge Bonding [57]

### 2.5.3 Wire Pull Testing and Bond Shear Testing

Wire pull testing requires special equipment commonly referred to as a wire pull tester (or bond pull tester), which consists of two major parts: 1) a mechanism for applying the upward pulling force on the wire using a tool known as a pull hook; and 2) a calibrated instrument for measuring the pulling force at which the wire eventually breaks. This breaking force is usually

recorded by wire pull tester in grams-force [36, 53, 55]. Aside from the bond strength reading, the operator must also record the bond failure mode. Failure mode in this context refers to one of the following: 1) first bond (ball bond) lifting; 2) neck break; 3) mid-span wire break; 4) heel break; and 5) second bond (wedge bond) lifting. First or second bond lifting is unacceptable and should prompt the process owner to investigate why such a failure mode occurred. Figure 2.7(a) shows the schematic illustration and pull test failure modes of a typical wire pull test.

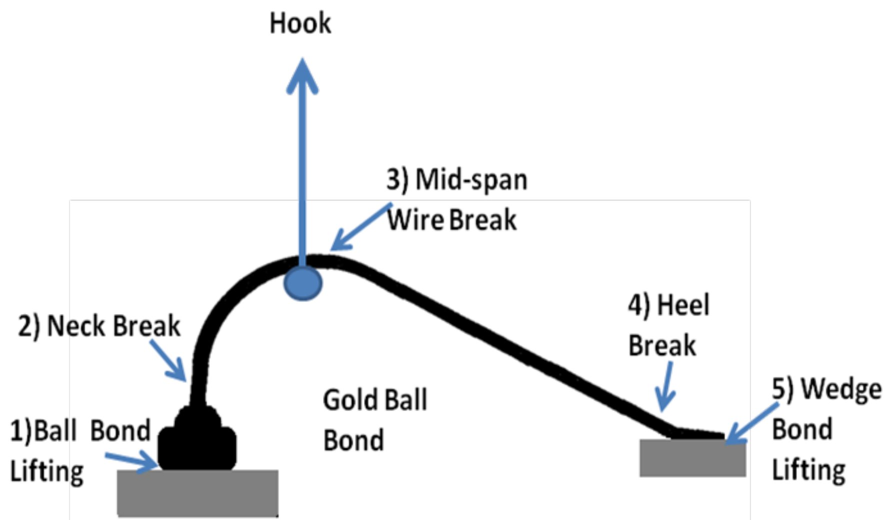



Figure 2.7 (a) Typical Geometrical Configuration and Pull Test Failure Modes for Wire Pull Test [54]

A bond shear tester is needed to perform the bond shear test [36,53]. This equipment consists of a sample holder, a shearing arm with a chisel-shaped tool at the end, and an instrument for measuring the shear strength of the bond. Initially, the shearing tool is positioned beside the ball bond to be tested. The shearing arm then moves the tool horizontally against the ball, in effect pushing the ball off its bond pad. The force needed to shear a ball off its pad, known as the bond shear force, is then measured by the ball shear tester. During bond shear testing, the shear height is an important variable, and it must be set high enough to avoid

dragging on the substrate surface but low enough to produce a shear load rather than a rolling force. The schematic illustration of bond shear test is shown in Figure 2.7 (b).

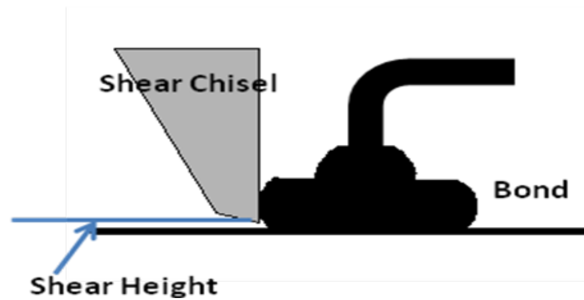



Figure 2.7 (b) Typical Geometrical Configuration and Position of Chisel for Bond Shear Test [54]

## 2.6 Hermetic Sealing

Hermetic sealing minimizes the intrusion of contamination and allow the circuit mounted inside the package to survive for a longer period of time. In practice, “hermetic” is defined not in the absolute sense of the word but rather in meeting a finite helium leak rate below a specified standard rate. For added reliability, a hermetic package is sealed in either a benign environment, generally nitrogen, or in vacuum [34, 41].

Ceramic packages and metal packages are two common types of hermetic packages[34,41]. Kovar® metal packages [58] which are fabricated primarily from F-15 alloy (known as Kovar® alloy) have glass to metal feed-throughs and are widely used to hermetically seal hybrid circuit with low I/O counts. They can provide a close match in CTE between glass and the F-15 alloy, but the CTE varies significantly as a function of temperature, which can cause high stress during cycling. Kovar® packages may be Au-plated or Ni-plated and sealed with similarly plated Kovar® lids [58]. Most ceramic packages used today are produced from co-fired alumina, either by HTCC (high temperature co-fired ceramic) or LTCC (low temperature

co-fired ceramic) [31,34,41]. Leads are then brazed to the package body. The metalized areas of the package are electroplated (usually nickel followed by gold). LTCC packages are gaining prominence because of the ability to co-fire with low resistivity Au, Ag and Cu at relatively low temperature, and the flexibility and ease with which packages integrated with substrates can be designed and fabricated [58]. Further benefit of LTCC packages includes that the CTEs can be tailored to closely match Si and GaAs devices. Ceramic packages can be sealed with a flat lid metalized around the periphery of the seal area by soldering, usually with Au-Sn (80/20 wt%) alloy (eutectic $T_m$=280$^o$C). For higher operating temperature, Au-Sn TLP sealing is an option [30,41]. Sealing with a low-melt-point glass is less expensive but this method is also less reliable because the glass seal is susceptible to mechanical and thermal stress; Welding can provide the highest temperature capability, but the technique requires a seal ring to be brazed to the ceramic. At temperature above 400$^o$C, it is challenging to find reliable materials for the brazes and a compatible seal ring [59].

# CHAPTER 3 PACKAGING FOR HIGH TEMPERTURE SILICON-ON-INSULATOR ELECTRONICS

## 3.1 Introduction

Silicon-on-insulator (SOI) integrated circuits have been demonstrated for use at temperatures up to 300$^{o}$C. However, to build functional electronics, multiple devices must be interconnected to provide the desired functionality. A system-in-package (SiP) approach has been developed using thick film technology on $Si_3N_4$ ceramic substrates in this project. Eutectic Au-Ge die attach was used with a Ti/Ti:W/Au backside die metallization for 300$^{o}$C operation. Results of die attach reliability based on shear strength are discussed after thermal storage and thermal cycling tests. Wire bonding is a cost-effective and flexible interconnect technology for HTE packaging [60]. SOI die typically have Al wire bond pads that are not compatible with Au thermosonic wire bonding for high temperature applications. A plating process that provides a barrier layer (electroless Ni) and a wire bondable finish (electroless Pd/immersion Au.) over the Al wire bond pads has been examined. Results of the investigation of Au wire bonding on substrate metallization and die surface metallization are also presented in this chapter.

## 3.2 Thick Film $Si_3N_4$ Substrates

Fabrication of a thick film module begins with the substrate. For Si die, silicon nitride ($Si_3N_4$) provides the best CTE match. $Si_3N_4$ also has a higher flexural strength than $Al_2O_3$ and AlN, which is important in measure-while-drilling (MWD) applications. For these reasons, $Si_3N_4$ is being investigated for SOI die packaging.

Thick film materials have not been developed specifically for $Si_3N_4$ ceramic substrates. An early attempt to use a standard thick film conductor material developed for AlN yielded poor adhesion of the thick film Au metallization to the $Si_3N_4$ substrate [61].

Sienna Technologies, Inc. (Woodinville, WA) has recently developed a first generation thick film Au for $Si_3N_4$ including paste chemistry control and surface engineering that yields excellent metallization adhesion. Figure 3.1 shows an Au metalized $Si_3N_4$ substrate. A cross section of the metalized substrate is shown in Figure 3.2. The glass adhesion layer (B) of the thick film conductor can be clearly seen. The engineered surface layer (C) on the surface of the $Si_3N_4$ substrate is seen below the thick film glass adhesion layer. Sienna Technologies, Inc. fabricated substrates for the die attach (high temperature aging and thermal cycling) and wire bond experiments.

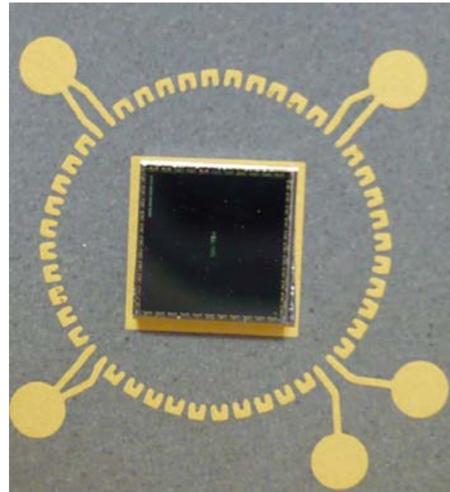


Figure 3.1(a)

Figure 3.1 (b)
Figure 3.1 Thick Film Metalized $Si_3N_4$ Substrate. (a) wire bond test pattern, (b) close-up of wire bond pad

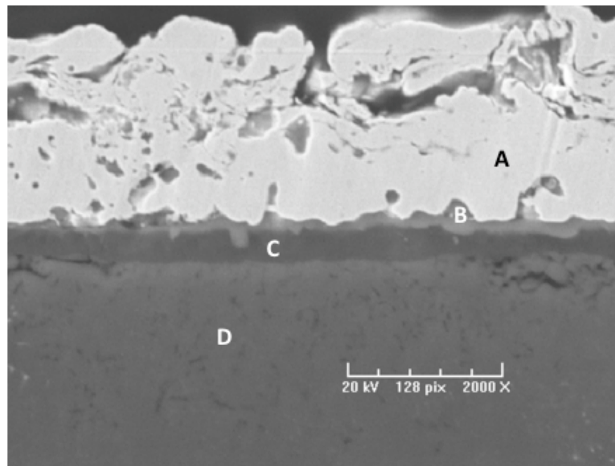



Figure 3.2 Cross Section of Fired Thick Film Au Conductor on $Si_3N_4$ Substrate,
A = Sintered Au, B = Thick Film Glass Adhesion Layer, C = Engineered Surface Layer,
D = Bulk $Si_3N_4$.

### 3.3 Si Die Backside Metallization

Au-Ge has been shown to be incompatible with Ni/Au plated on direct bond copper (DBC) for high temperature applications due to the formation of Ni-Ge intermetallics [62]. To avoid any potential issue with Ni-Ge intermetallics, the Si test die backside metallization used in this experiment was: Ti/Ti:W(10:90wt%)/Au. The deposited thin film layer thicknesses were:

100nm/200nm/100nm. After thin film deposition, additional Au was electroplated onto the backside of the die to produce a final thickness of 3μm. Figure 3.3 illustrates the standard gold plating setup. Gold HS 434, supplied by Technic Inc., was used as the gold electroplating solution. A multi-meter was connected with the circuit in series to monitor the current flowing through the HS 434 solution. A platinized cadmium mesh was used as the anode, with the electrolyte solution acting as the source of gold. When current was flowing through the solution containing the metallic ions, the positive ions were attracted to the cathode and the negative ions to the anode. By way of electrolysis the gold ions were removed from the solution and deposited on the surface of the wafer as a thin layer. The gold HS deposit 434 is 99.99+ % pure, with a deposit density of 18.5 g/cc and a contact resistance of 0.3 milliohms/$cm^2$ [63]. The details of the gold electroplating process were the following:

- Soak in TSC-1501 for 2 minutes at 65°C to remove light oils, fingerprints and handling residues.
- Rinse in DI water for at least 1 minute.
- Soak in 5% sulfuric acid, at room temperature for 2 minutes.
- Rinse in DI water for at least 1 minute.
- Electroplating with Technic gold HS 434 at 55°C-60°C under 2ASF for 30 minutes.
- Rinse in DI water and blow dry with $N_2$.

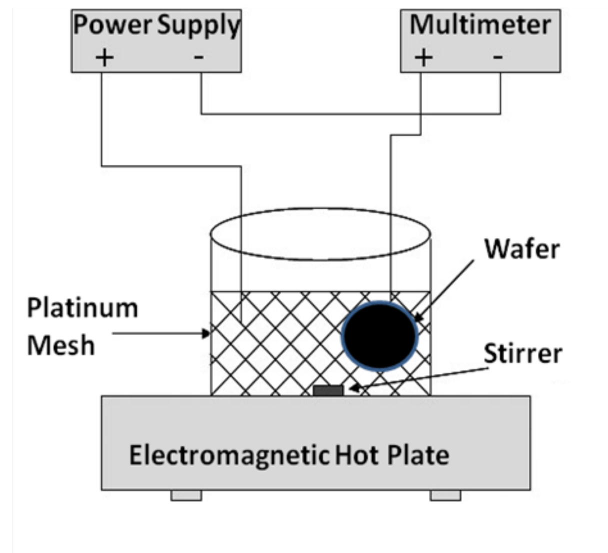



Figure 3.3 Schematics of Gold Electroplating Setup

## 3.4 Die Attach

### 3.4.1 Au-Ge Braze

Gold-germanium (Au-Ge) alloy is used in the microelectronics industry for attaching dies to substrates and substrates to carriers. In this research, 25.4μm thick eutectic Au-Ge (88/12 wt%) preform with a melting point of 356$^{o}$C manufactured by Williams Advanced Materials was selected for evaluation. Au-Ge does not form intermetallics with the thick film Au and has previously been demonstrated with thick film Au on AlN at 300$^{o}$C [62]. Figure 3.4 is the phase diagram for gold-germanium [64].

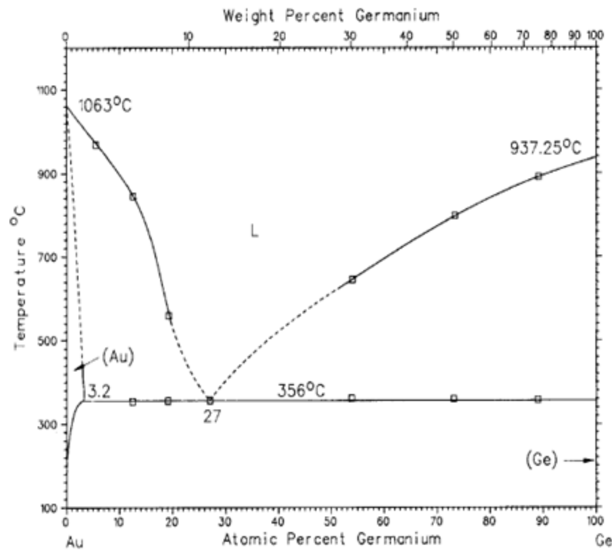



Figure 3.4 Gold-Germanium phase diagram [64]

3.4.2 Au-Ge Brazing Profile

Au-Ge preform was sandwiched between the Si die and substrate and a weight rod was placed on each assembly as the bonding force. The bonding process was run in the SST vacuum furnace and the bonding profile is shown in Figure 3.5. The profile peak temperature was 385°C and the bonding time at peak temperature was 3 minutes. Time at the peak temperature was critical to ensuring that there was good wetting but minimum gold dissolution.

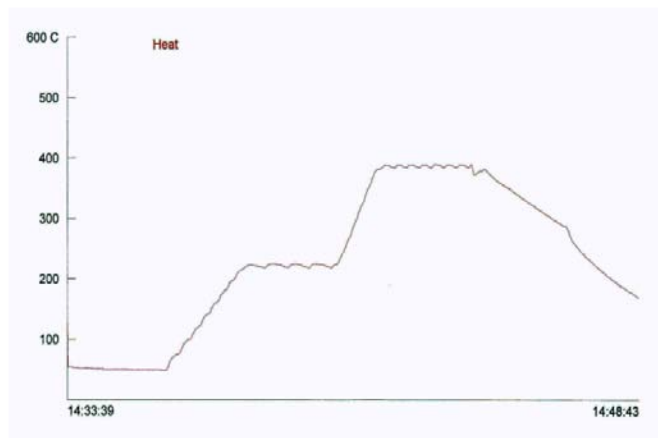



Figure 3.5 Au-Ge SST Bonding Profile

3.5 Die Attach Reliability Test

The die shear tests were performed to evaluate the bond reliability using a Dage 2400PC shear tester with a 100kg load cartridge. The shear tool height was set at 100µm above the substrate surface and the shear speed was 50µm/s.

3.5.1 High Temperature Thermal Aging Test

A high temperature thermal aging test was used to investigate the effect of time and temperature on the die shear strength. The apparatus used was a Blue-M burn in chamber maintained at 325°C over the entire 3000 hours aging period.

The 3.4mm x 3.4mm Si test die were assembled using 25.4µm thick Au-Ge preforms (size: 3.3mm x 3.3mm) in a SST vacuum furnace with a bonding force of 7 grams. Figure 3.6 plots the initial (as built) die shear strength test results. A range of shear strength values was observed. The data fall into two groups: high shear strength (sample 1, 5, 6, 8) and low shear strength (sample 2, 4, and 7). All shear strengths measured were significantly (>10X) higher than the minimum die shear strength specified in Mil-Std-883G, Method 2019.7.

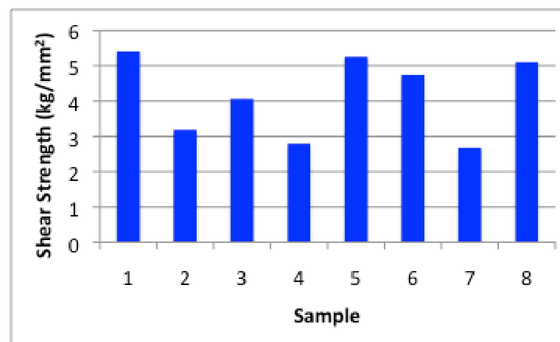



Figure 3.6. Distribution of Initial Die Shear Strengths

A cross section of an as-assembled die attach is shown in Figure 3.7. The cross section shows Ge crystals within the Au. Segregation of Ge crystals is expected as Au and Ge have very low mutual solubility in the solid state. The slow cooling in the vacuum furnace allows time for

some Ge segregation to occur. The cross section also shows Ge reaching the thick film conductor-substrate interface. Figure 3.8 is a cross section of a high shear strength substrate after die shear: the failure is between the engineered surface layer and the bulk $Si_3N_4$. The lower shear strength substrates had some areas with the failure interface between the engineered surface layer and the bulk $Si_3N_4$, but the majority of the failure interface area was between the thick film Au and the engineered surface layer (Figure 3.9). Surface analysis of the fracture surface of lower shear strength die revealed Ge present at the interface on the die side fracture surface. Thus, if during the die attach process, the Au-Ge is dissolving too much of the thick film Au layer (Ge reaching the substrate interface), the failure mode is at the thick film Au-to-engineered surface substrate interface and is lower in shear strength. If the Au-Ge does not reach the thick film Au-to-substrate interface, the thick film Au adhesion is higher and the ultimate failure mode is at the engineered surface layer-to-bulk $Si_3N_4$ interface with a high die shear value.

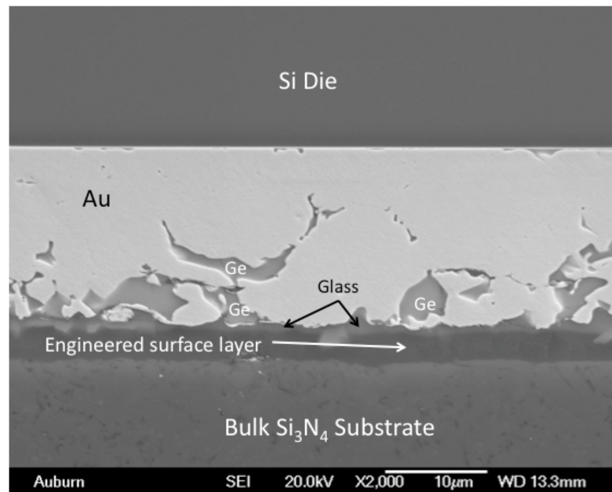



Figure 3.7 Cross Section of Die Attach As-Assembled.

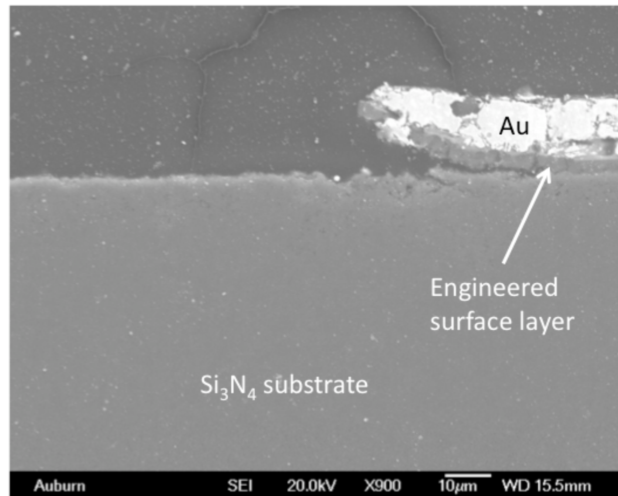



Figure 3.8 Cross Section of a High Die Shear Strength Substrate Showing Au Thick Film Remaining at the Edge of the Die Pad and Failure at the Engineered Surface Layer to $Si_3N_4$ Interface under the Die (to the left of Au)

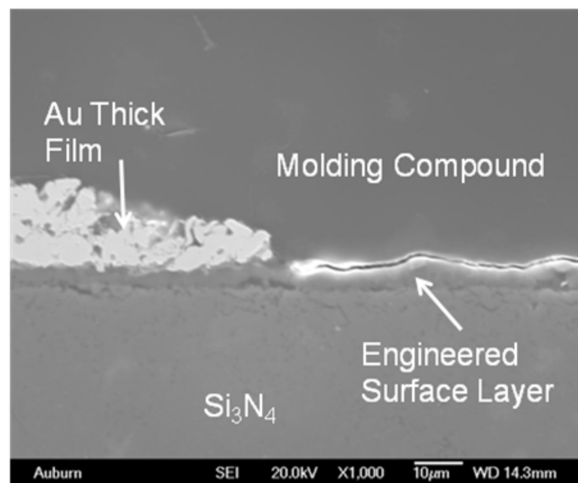
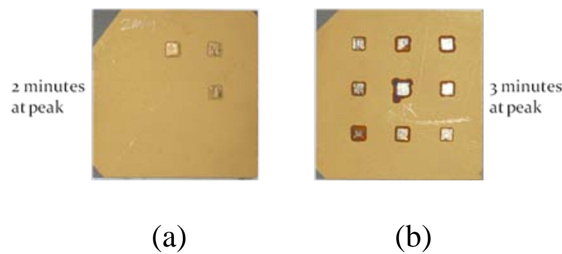



Figure 3.9 Cross Section of a Die Shear Strength Substrate Showing Failure at the Thick Film to Engineered Surface Layer Interface under the Die (to the right of the Au)

The test substrates (1.5" x 1.75") had a 3 x 3 array of die attach sites. Variations in the time-temperature profile at the different sites on the graphite heater in the vacuum furnace could result in variations in the extent to which the Au-Ge dissolved the Au thick film layer. To evaluate this hypothesis, a test was performed to evaluate the melting and wetting of the Au-Ge preform as a function of time at peak temperature. The profile peak temperature was 385$^{o}$C as

measured by the control thermocouple: not the actual substrate temperature. The time at peak was varied from 2 minutes to 3 minutes. At 2 minutes, the Au-Ge only wet at 3 of 9 sites (Figure 3.10 a). The time had to be increased to 3 minutes to get Au-Ge wetting at all 9 sites (Figure 3.10 b). A substrate processed with 3 minutes at peak temperature results in some sites being at peak temperature 1 minute longer than necessary to achieve wetting and thus excess dissolution of the thick film Au. The trend was for the die shear strength to decrease when the Au-Ge was in the molten state for a longer time. This supports the hypothesis and indicates the time-temperature profile is critical.




(a) (b)

Figure 3.10 Wetting of Nine AuGe Preforms to Substrate Metallization as a Function of Time at Peak Temperature. (a) 2 minutes at peak (b) 3 minutes at peak

The test samples used in the aging, thermal cycling and wire bonding tests were assembled prior to determination of the cause for the range of shear strength values. For the test samples used in these experiments, a profile with 3 minutes at peak temperature was used.

Parts were aged at 325$^{o}$C and the die shear test results are plotted in Figure 3.11.The mean shear strength decreased by ~16% after 3000 hours at 325$^{o}$C. Through 1500 hours, the failure mode was at the substrate interface. At 2000 and 3000 hours the failure mode was mixed: in the preform layer and at the backside of the die.

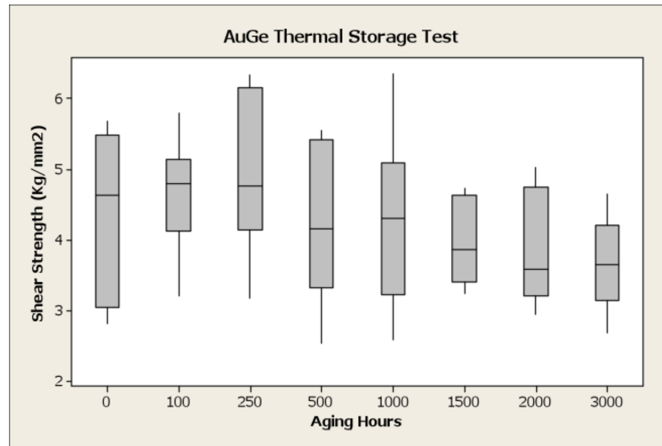



Figure 3.11 Die Shear as a Function of Storage Time at 325°C.

Figure 3.12 is a cross section of the die attach after 3000 hours at 325°C. A layer of Si is observed in the middle of the die attach layer and the interface between the Si die and the die attach is rough compared to the initial condition (Figure 3.7). The composition of the features in the micrograph was determined by energy dispersive x-ray analysis. Note that the Ge is now near the Si interface rather than at the substrate interface in the cross section of the as-assembled sample (Figure 3.7). The rough surface of the die attach-to-die interface supports the only plausible explanation that the source of the Si was from the die backside. Silicon was not observed in as-assembled die attach cross sections. This would indicate the Ti/Ti:W was not an effective barrier layer with time at 325°C. Au-Ge-Si forms a ternary eutectic (Figure 3.13) with a melting point of 326°C [65]. This is within the accuracy of the measured 325°C storage temperature. Thus, it is hypothesized that initial defects in the thin film Ti/Ti:W layer or defects created in the barrier layer by diffusion of the Ti and Ti:W allowed Au-Ge to contact Si and Au-Ge-Si eutectic then formed. The presence of this Si layer did not result in a significant decrease in mean die shear strength or a decrease in the lower limit of the data range, but the failure mode did change (Figure 3.14) and the upper range of the data decreased. Alternate backside metallization systems should be explored. Figure 3.15 shows a cross section of a wire bond test

die after 3000 hours of storage at 320°C. No Si is present in the die attach region. Thus, limiting the peak exposure temperature to below the ternary eutectic temperature eliminates the Si dissolution into the die attach layer.

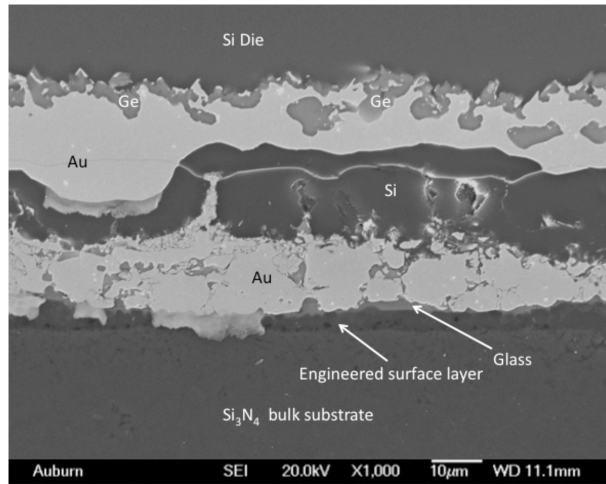



Figure 3.12 Cross Section Micrograph of Die Attach after 3000 Hours at 325°C.

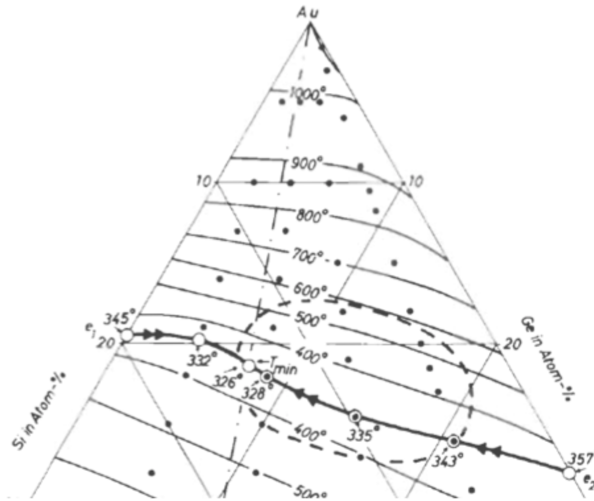



Figure 3.13 Au-rich Region of Au-Ge-Si Phase Diagram [65].

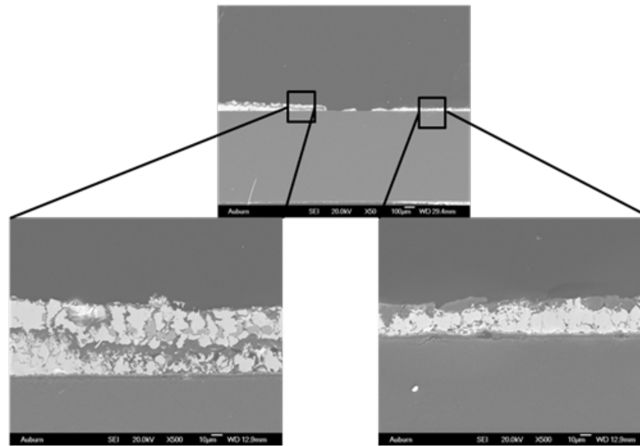


Figure 3.14 Cross Section of Substrate after Die Shear Test following 3000 Hours Storage at 325°C

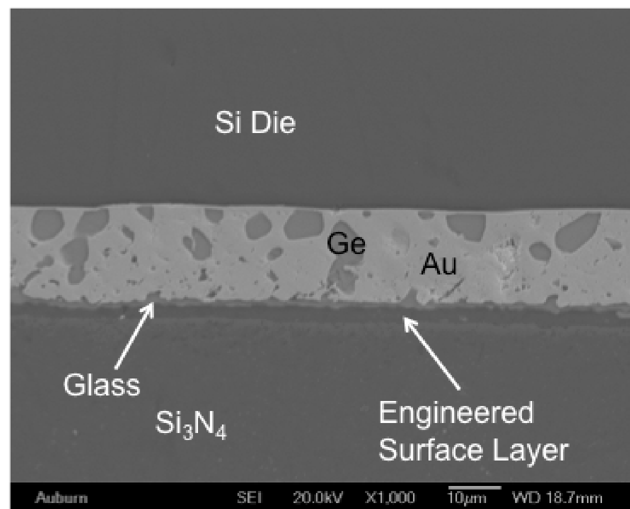



Figure 3.15 Cross Section of Wire Bond Test Die after 3000 Hours at 320°C

3.5.2 Thermal Cycle Test

The thermal cycle test was used to determine the ability of the pacakge to withstand the stress from cyclic exposure to high and low temperatures. The thermal cycle test samples were assembled with larger die (7.5mm x 7.5mm) and preform (7.45mm x 7.45mm). A larger die size was selected to increase the die attach stresses during thermal cycling. The thermal cycle was from 40°C to 325°C (Figure 3.16), which consisted of 25 minutes ramp from 40°C to 325°C, then soak for 5 minutes, followed by 35 minutes cool down from 325°C to 40°C. Die shear tests were

performed on test assemblies after 250 cycles, 500 cycle, 1000 cycles, 1500 cycles and 2000 cycles with a group sample size of 8.

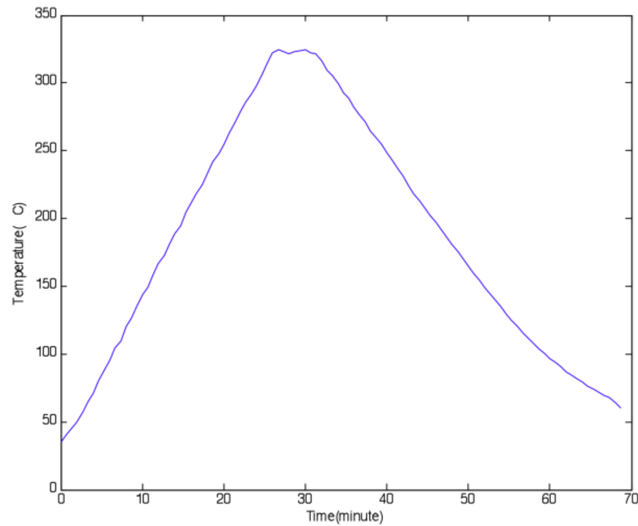



Figure 3.16 Thermal Cycle Profile

The die shear results are shown in Table 3.1 Shear strengths recorded as >1.78kg/mm$^2$ (100kg/56.25mm$^2$) indicates the die did not shear at the maximum shear force of the load cell (100kg). The die that did shear, failed at the thick film Au to engineered surface layer interface (Figure 3.17). This failure mode would correlate with the earlier described issue with temperature uniformity during the assembly operation: excess dissolution of Au thick film by molten AuGe. As with the smaller die for the aging test, most die had high shear strength (did not shear at 100kg) while a few had lower shear strength (sheared at <100kg). After thermal cycling, a crack (Figure 3.18) was observed on some substrates at the perimeter of the die attach region. These die subsequently sheared during the shear test. If no crack was observed, the die did not shear during the shear test. This would imply that the weaker initial assemblies developed cracks while the stronger initial assemblies did not develop cracks during thermal cycling.

Optimization of the assembly process should eliminate these lower shear strength failures as indicated by the majority of the samples that did not shear at 100kg after cycling

Table 3.1 Thermal Cycle Die Shear Results (Shear Strength in $kg/mm^2$)

| 0 cycles | 250 cycles | 500 cycles | 1000 cycles | 1500 cycles | 2000 cycles |
|---|---|---|---|---|---|
| >1.77 | >1.77 | >1.77 | >1.77 | >1.77 | >1.77 |
| >1.77 | >1.77 | >1.77 | >1.77 | >1.77 | >1.77 |
| >1.77 | >1.77 | >1.77 | >1.77 | >1.77 | >1.77 |
| >1.77 | >1.77 | >1.77 | >1.77 | >1.77 | >1.77 |
| >1.77 | >1.77 | >1.77 | >1.77 | >1.77 | >1.77 |
| >1.77 | >1.77 | >1.77 | 0.76 | >1.77 | >1.77 |
| 1.54 | >1.77 | >1.77 | 0.83 | 0.67 | 1.17 |
| 1.42 | 1.60 | 1.38 | 1.14 | 0.70 | |

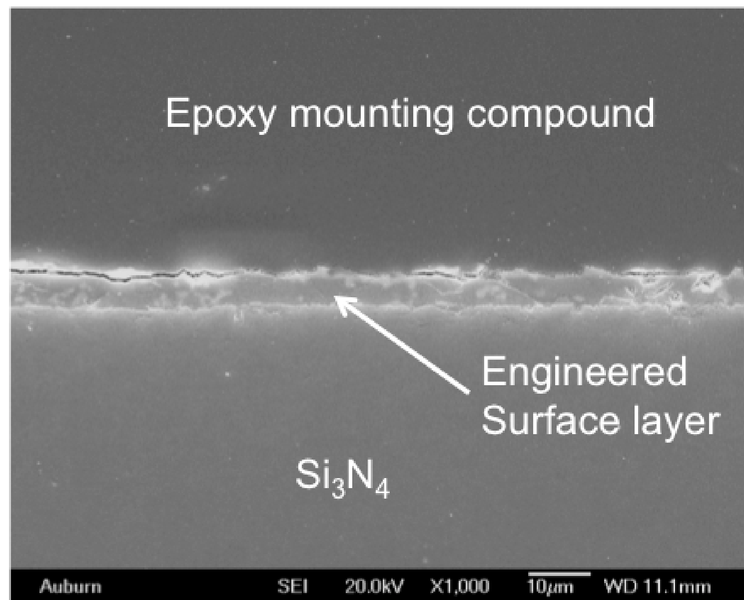



Figure 3.17 Cross Section of Substrate after Shear Test Following 1000 Thermal Cycles

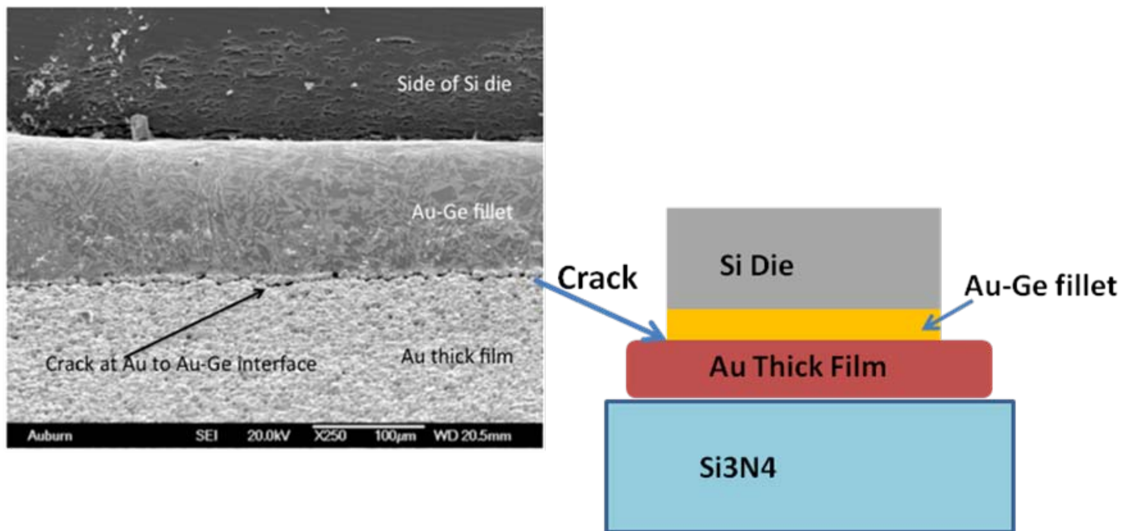



Figure 3.18 Micrograph (left side) of Crack at the Perimeter of the Thick Film Au and Au-Ge Interface After 1500 Thermal Cycles Prior to Die Shear. Schematic Side-view of Au-Ge Die Attach Assembly Shown on the Right Side

## 3.6 Wire Bonding Test

### 3.6.1 Wire Bond Pad Metallurgy

Aluminum wire bond pads are typically used on SOI devices. These are not compatible with Au wire bonds at 300°C due to intermetallic formation and Kirchendall voiding. Al wire bonding is one option, but moves the Al-Au interface to the thick film Au metallization where the same reliability issues would exist. A two-step Ni/Au plating approach (ElectrolessNi/immersion Au + electroless Au over Al) has been previously demonstrated as a reliable pad metallurgy for 300°C use. [66]. A simple process was evaluated in this work. The process was: zincate, electroless Ni, electroless Pd and immersion Au. The Ni provides a diffusion barrier. This process sequence eliminated the need for a separate electroless Au plating step. The plated pad is shown in Figure 3.19. Two plating thicknesses were deposited by PacTech (Santa Clara, CA) for evaluation:

1) 5.8μmNi/200nmPd/22nmAu; and

2) 5.8μmNi/400nmPd/19nmAu.

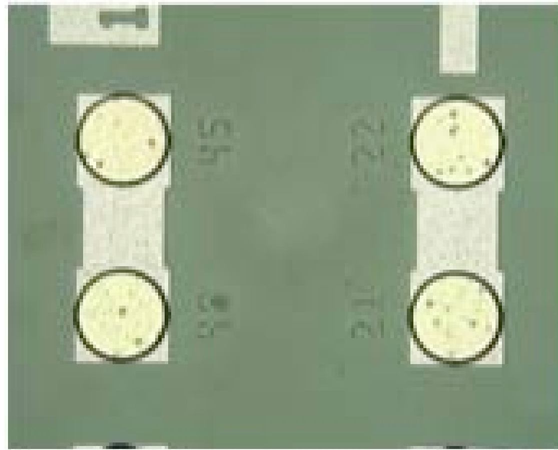


Figure 3.19 Electroless Ni/Electroless Pd/Immersion Au Wire Bond Pads.

The test die were backside metalized with Ti/Ti:W/Au (100nm/200nm/100nm) thin film metallization and electroplated Au to a final thickness of 3μm (same die backside metallization as described in section 3.2.3). Au-Ge eutectic die attach was used to attach the die to the thick film metalized $Si_3N_4$ substrates (Figure 3.1 a). A Palomar 2460 – V thermosonic wire bonder was used to bond the 25.4μm diameter Au wire to the die. The bonding parameters were optimized using pull force, ball shear force and failure mode as evaluation criteria. Wire bonded test vehicles were aged at 320$^{o}$C in the Fisher scientific isotemp programmable furnace.

3.6.2 Wire Bond Pull Force Test

The wire bond pull force test results as a function of aging time are plotted in Figures 3.20 and 3.21. For the 5.8μmNi/200nmPd/22nmAu die, 2 of 31 wire pulls at t=0 hours were second bond lifts (6.4g and 8.5g) from the thick film metallization. The remainder of the t=0 hour breaks were in the wire (mid-span (1 of 31) or in the neck above the ball (28 of 31)). For the 5.8μmNi/400nmPd/19nmAu die, 3 of 32 pulls were second bond lifts (9.8g, 8.3g and 7.3g) at t=0 hours. The remainder of the breaks at t=0 hours were wire breaks in the neck above the ball.

There were no ball lifts from the Ni/Pd/Au pads at t=0 hours. The pull force decreased as a function of time as expected due to the annealing of the Au wire. All failures with aging from 100 to 2000 hours were in the wire – no ball bond or second bond lifts. The wire breaks shifted from in the neck above the ball to mid-span as the wire annealed. After 3000 hours at 320$^{o}$C, ball bond lifts were observed (10% ball lifts for 5.8µmNi/200nmPd/22nmAu die and 6% for 5.8µmNi/400nmPd/22nmAu die). Figures 3.22 and 3.23 show the failure mode: cratering of the Si under the bond. Cratering of the Si under the bond pad occurs during the bonding process to 'hard' bond pad metallizations due to excess force and ultrasonic energy used in bonding. Ni/Pd/Au is a harder bond pad than Al or Ni with thick Au. It is hypothesized that the cratering defects were not detected in earlier pull tests due to the thickness of the Ni layer that provided sufficient mechanical strength compared to the wire strength. With thermal cycling (all of the test samples were removed from the oven at each test interval), the Ni weakened and the cratering was observed.

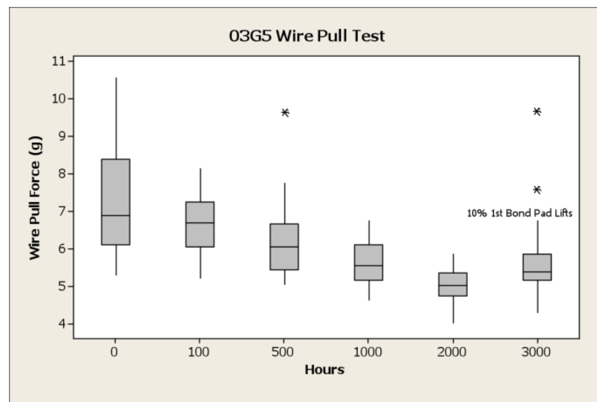



Figure 3.20 Pull Force as a Function of Aging Time at 320$^{o}$C for 5.8µmNi/200nmPd/22nmAu Die

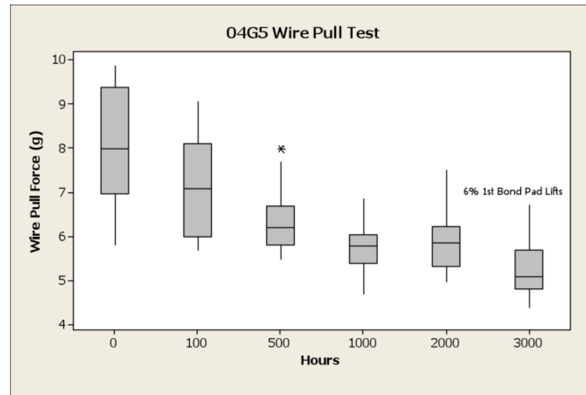



Figure 3.21 Pull Force as a Function of Aging Time at 320$^{o}$C for 5.8μmNi/400nmPd/19nmAu Die

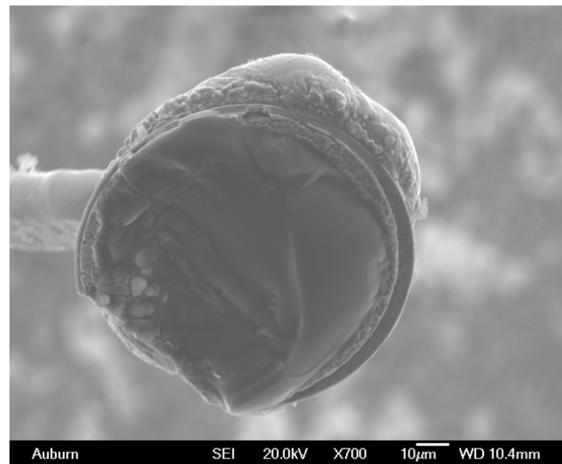



Figure 3.22 Scanning Electron Micrograph of Lifted Ball Bond Illustrating Cratering of the Si Pad after 3000 Hours of Aging at 320$^{o}$C

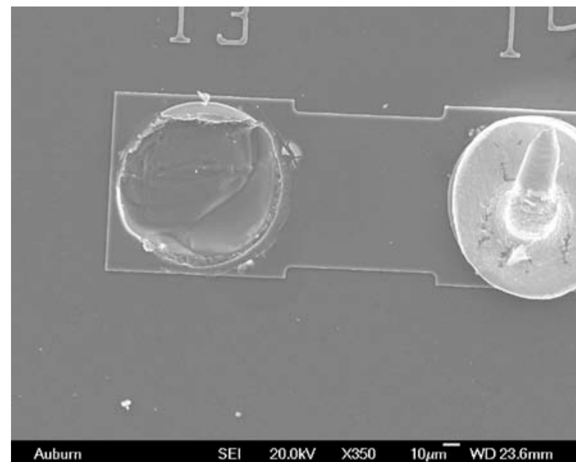



Figure 3.23 Scanning Electron Micrograph of Cratered Si Pad after 3000 Hours of Aging at 320$^{o}$C

3.6.3 Wire Bond Ball Shear Force Test

The ball shear force test results as a function of storage time at 320°C are plotted in Figures 3.24 and 3.25 The shear tool was set 10µm above the face of the die and the shear speed was 50µm/s. The initial shear force was higher for the die with thicker Pd. The shear force for the die with thinner Pd increased with aging time, while the shear force for the die with thicker Pd remained relatively constant. No cratering defects were observed.

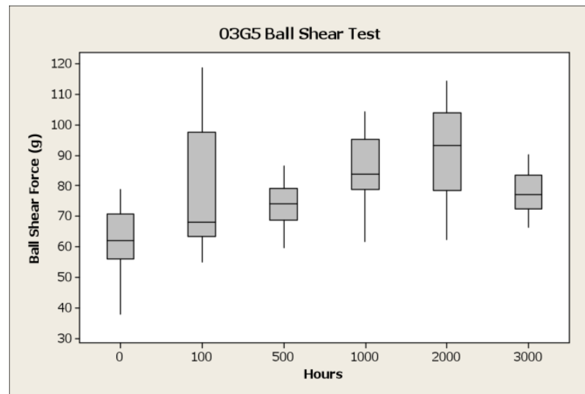



Figure 3.24 Ball Shear Force as a Function of Aging Time at 320°C for 5.8µmNi/200nmPd/22nmAu Die

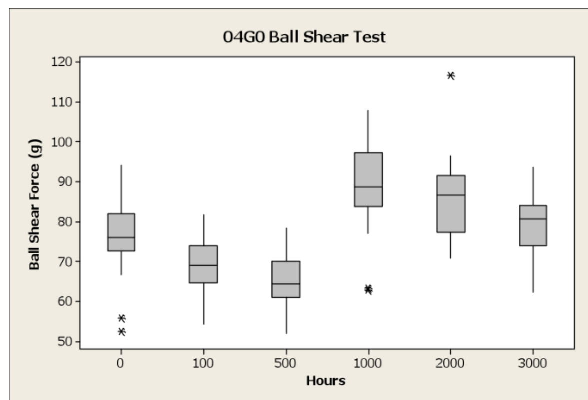



Figure 3.25 Ball Shear Force as a Function of Aging Time at 320°C for 5.8µmNi/400nmPd/19nmAu Die

### 3.6.4 Daisy Chain Electrical Resistance

Daisy chain electrical resistance was also measured. The daisy chain included 88 wires, the Al metallization on the die and the thick film Au on the $Si_3N_4$ substrate (Figure 3.1 a). The resistance as a function of aging time at 320°C is plotted in Figures 3.26 and 3.27. The resistance remained relatively constant (slight decrease with initial aging then a slight increase with further aging) through 2000 hours. After 3000 hours of 320°C storage, a significant increase in resistance was observed on some test die. Within those test die, the increase in resistance could be isolated to just a few wire bonds. The bonds were correlated by cross section to cratered wire bond pads. This correlates well with the previously discussed ball bond lifts observed in the wire pull tests.

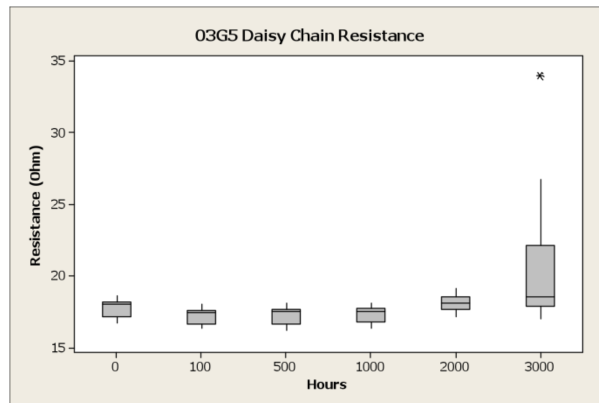



Figure 3.26 Daisy Chain Resistance as a Function of Aging Time at 320°C for 5.8µmNi/200nmPd/22nmAu Die

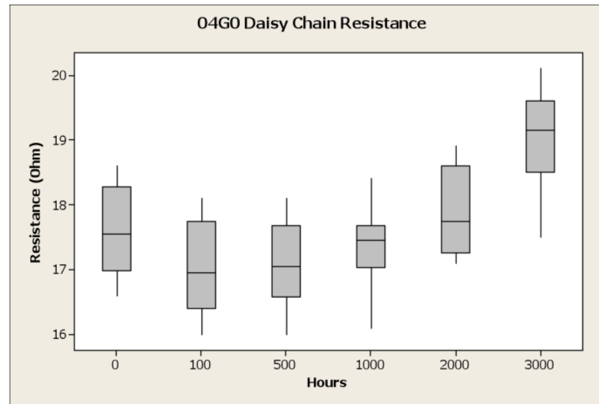



Figure 3.27 Daisy Chain Resistance as a Function of Aging Time at 320°C for 5.8µmNi/400nmPd/19nmAu Die

No intermetallic or voiding issues were observed with the Ni/Pd/Au wire bond pads after 3000 hours aging at 320°C. The mechanical failures (first bond lifts) were due to cratering and not separation within the bond pad metallurgical stack as would be expected if Kirchendall voiding were to occur. Also, the increase in wire bond electrical resistance was related to wire bond pads that cratered. For die and portions of die without cratering, the bond resistance was stable.

To eliminate cratering a series of bonding experiments were performed to optimize the bonding parameters. To evaluate cratering, wire bond samples were thermal cycled using the profile in Figure 3.16. Thermal cycling over this wide temperature range would quickly expose cratering due to the coefficient of thermal expansion mis-match between the Al/Ni/Pd/Au pad stack and the Si die. Pull tests were performed after 100 thermal cycles. No cratering was observed during the pull testing of 23 wire bonds. Table 3.2 compares the wire bonding parameters used in the original NiPdAu wire bond test and the 'crater' optimized bonding parameters. Increasing the stage temperature allowed the ultrasonic displacement and force to be lowered, eliminating craterin

Table 3.2 Wire Bonding Parameters

| Parameter | Original Experiment | Crater Optimized |
|---|---|---|
| Force | 55 grams | 45 grams |
| Time | 40 ms | 40 ms |
| Ultrasonic Amplitude | 1 μm | 0.75 μm |
| Stage Temperature | 150°C | 210°C |
| Capillary | Gaiser 1851-13-437GM 55(3.5X120D-8D-8)20D AB10X12 | Gaiser 1851-13-437GM 55(3.5X120D-8D-8)20D AB10X12 |
| Free Air Ball Diameter | 65 μm | 65 μm |

## 3.7 Summary

A first generation thick film Au including paste chemistry control and surface engineering for metalizing $Si_3N_4$ substrates has been demonstrated. Au-Ge is a feasible die attach material, but the use temperature should be limited to 300°C. Au-Si-Ge has a ternary eutectic with a melting point of 326°C. If the Si die is exposed to the Au-Ge at 326°C or above through defects in the barrier layers (Ti/Ti:W in this work), eutectic liquid can form. The defects in the barrier layer may be due to coverage issues over the rough (compared to the thickness of the thin film layers) surface topology of the Si backside or due to diffusion at the elevated temperature. In this work, a thick layer of Si formed in the center of the die attach layer after storage at ~325°C. However, the formation of this layer did not result in a dramatic decrease in shear force.

Control of the Au-Ge die attach process (time and temperature) is also critical. The initial shear results had a range of values. The lower shear strength assemblies were the result of significant dissolution of the thick film Au as the liquid Au-Ge die attach material reached the thick film-to-substrate interface. Tighter process control is required. Lower initial die shear

strength did not result in a further decrease in shear strength with aging, but did result in lower shear strength after thermal cycling.

Electroless Ni/electroless Pd/immersion Au over Al wire bond pads is a viable metallurgy for Au wire bonding for 300$^{o}$C applications; however, optimization of the wire bonding parameters to eliminate pad cratering is required.

# CHAPTER 4 PACKAGING FOR HIGH TEMPERTURE SILICON CARBIDE ELECTRONICS

## 4.1 Introduction

The challenges of packaging SiC based electronics for high temperature applications include their high operating temperatures, wide thermal cycle ranges, and sometimes high currents and high voltages. As a result, the selection of chip metallization, substrate metallization, and die attach are crucial to a successful package design. This chapter examines off-eutectic Au-Sn as the die attach alloy with a PtAu thick film metallization on AlN substrates. A pure Au thick film layer was printed over the PtAu thick film layer. The SiC backside metallizations evaluated were Ti/TaSi/Pt/Au and Cr/NiCr/Au. Die shear tests were performed after aging at 500$^{o}$C and after thermal cycling. The shear test results and failure surface analysis are discussed.

## 4.2 Aluminum Nitride Substrate Metallization Fabrication:

Aluminum nitride (AlN) has a CTE (4.5ppm/$^{o}$C) that provides a close match to SiC. It also has a high thermal conductivity. For these reasons AlN has been selected for investigation for SiC high temperature electronics packaging. Both refractory metalized and thick film metalized substrates were studied in this work.

The refractory metalized substrates were commercially purchased AlN substrates with refractory MoMn metallization and electroplated Ni (~5μm)/Au (1μm) from Stellar Industries.

An additional 4μm of Au was electroplated at Auburn University, using the same Au electroplating set up as described in Section 3.3.

For thick film processing, the AlN substrate was pretreated by firing using an 850°C – 10 minute peak temperature profile (Figure 4.1) to grow a thin oxide layer in order to enhance the thick film metallization adhesion. A PtAu thick film conductor paste, C6029 from Heraeus®, was printed onto the pretreated AlN substrate using a patterned 320 mesh screen, dried in air at 150°C for 15 minutes, and fired using the same 850°C peak profile.A pure Au paste (no binder), 5063D from Dupont, was then printed, dried and fired over the fired PtAu thick film using the same process. This pure Au layer was to provide additional Au for the off-eutectic Au-Sn die attach process to be described in a subsequent section.

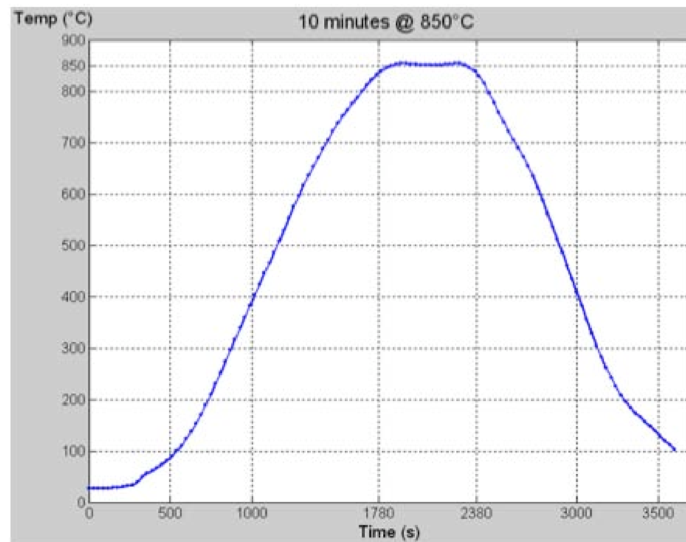



Figure 4.1 Belt Oven Firing Profile with Peak Temperature of 850°C

A pull test was designed to evaluate the adhesion of the thick film metallization aged at 500°C: AlN substrates with square PtAu/Au thick film conductor pads (5.5mm x 5.5mm) were diced into 16mm x 16mm squares and mounted on an alignment and clamping fixtures with aluminum pull studs (which had 2.7mm diameter heads with pre-coated epoxy) pressed against

the conductor pads (Figure 4.2-a). The epoxy was then cured in an oven at 150°C for 60 minutes, Figure 4.2-b shows a cured sample with an aluminum stud attached. The studs were then pulled perpendicular to the substrate and the force at failure was measured. Figure 4.3 illustrates the schematic setup for the stud pull test. For samples aged at 500$^{o}$C, the studs were attached after aging. The pull test results as a function of aging time are shown in Figure 4.4. In all cases, the failure was in the epoxy. The pull strength was recorded as the pull force(kg)/aluminum stud tip area(mm$^2$) and corresponds to the range of tensile strength reported by the supplier for the epoxy. No apparent degradation in thick film adhesion was observed.

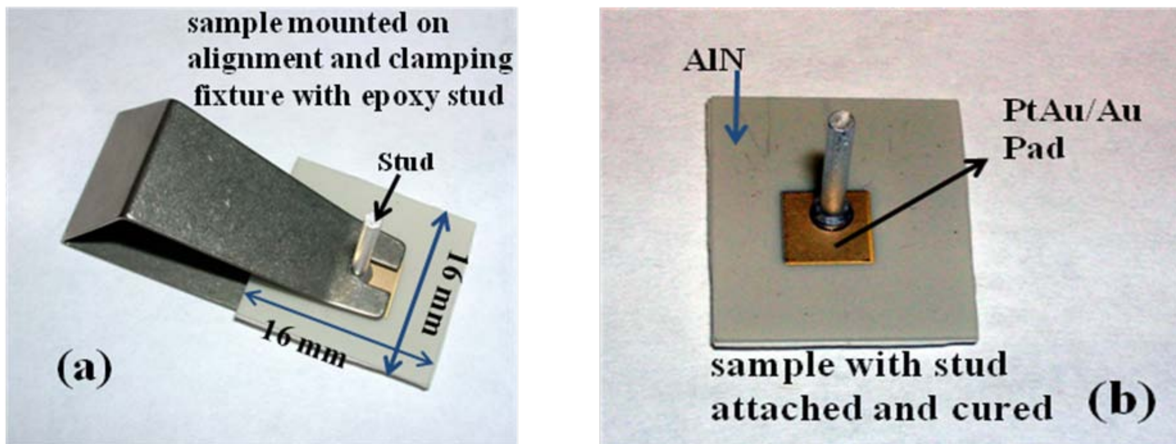
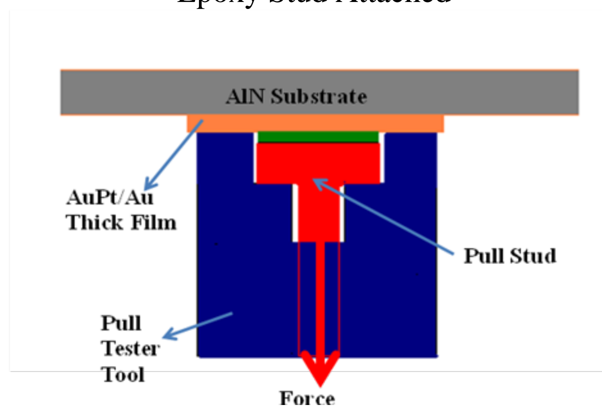



Figure 4.2 (a) Sample Mounted on an Alignment and Clamping Fixture and (b) Sample with an Epoxy Stud Attached




Dimensions Not Drawn to Scale

Figure 4.3 Schematic Side View of Stud Pull Test Setup

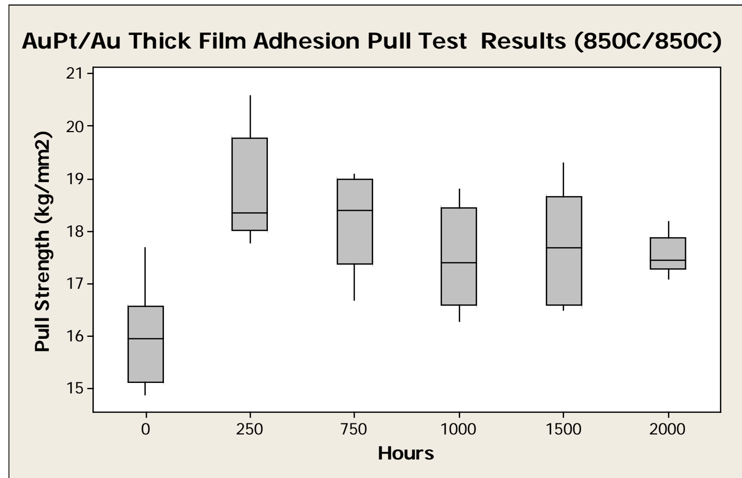



Figure4.4 PtAu/Au Thick Film Adhesion Pull Test Results ($kg/mm^2$) as a Function of Storage Time at 500°C: Both PtAu and Au Thick Film Fired Using 850°C Profile

For comparison purpose, an alternate process was evaluated to form PtAu/Au thick film metallization on AlN substrate. The only difference was, in this approach, the first layer of thick film PtAu paste (C6029 from Heraeus®) was fired using a 970°C-10minute peak temperature profile. The pull test results as a function of storage time at 500°C are plotted in Figure 4.5. Pull test results show the adhesion of the thick film metallization with two different PtAu/Au thick film processes (PtAu-850°C/Au-850°C and PtAu-970°C/Au-850°C) were similar after thermal storage at 500°C. In this project, all the AlN substrate used in die attach test were produced with PtAu-850°C/Au-850°C process.

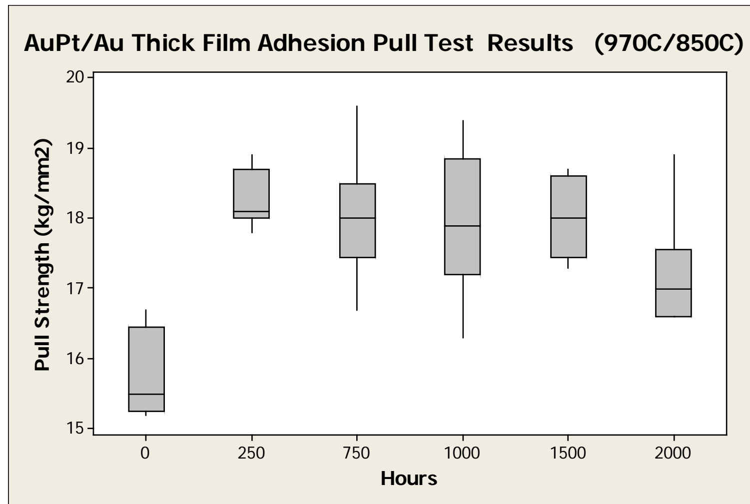



Figure4.5 PtAu/Au Thick Film Adhesion Pull Test Results (kg/mm$^2$) as a Function of Storage Time at 500°C : PtAu Fired Using 970°C Profile, Au Fired Using 850°C Profile

4.3 SiC Die Metallization

In this research, test vehicles were fabricated using SiC with two different backside metallization: Cr/Cr-Ni/Au and Ti/$TaSi_2$/Pt.

(1) Cr/Cr-Ni/Au: Prior to the die backside thin film stacks deposition, a RCA (Radio Corporation of America) pre-cleaning procedure was used to remove organic and inorganic contaminants on the SiC wafer. The SiC wafer was:

- immersed in a 5:1:1 (Vol. ratio) mixture of DI water: $NH_4OH$: $H_2O_2$ heated on hot plate to boil gently for 15 minutes.
- rinsed in DI water for ~1minute.
- immersed in a 6:1:1 (Vol. ratio) mixture of DI water: HCl: $H_2O_2$ heated on hot plate to boil gently for 15 minutes.
- rinsed in DI water for ~1 minute.
- blow dried with $N_2$ gas.
- baked in 120°C for ~20minutes

A three layer thin film stack composed of Cr/NiCr/Au with thin film layer thicknesses of

200nm/100nm/200nm was then deposited on the pre-clean SiC wafer. After thin film deposition, additional Au was electroplated onto the backside of die to produce a final thickness of 3μm using the same Au electroplating setup as described in section 3.3.

(2) Ti/$TaSi_2$/Pt: These die were fabricated at NASA Glenn Research Center with deposited Ti/$TaSi_2$/Pt thin film layer thicknesses of 100nm/400nm/200nm, annealed at 600$^oC$ for 30 minutes, and then 1000A of Au was e-beam deposited onto the three layer thin film metal stacks without annealing.

## 4.4 Off-eutectic Au-Sn Liquid Phase Transient (LPT) Die Attach:

### 4.4.1 Background

Off-eutectic Au-Sn liquid transient phase die attach for high temperature SiC power transistor attachment has been previously demonstrated [9]. In the original process, eutectic Au-Sn preforms were used with excess Au dissolved from either the backside of the die or the surface metallization of the substrate. As the wt% of Au in the die attach layer increases, the solidus point of the Au-Sn increases (Figure 4.4).

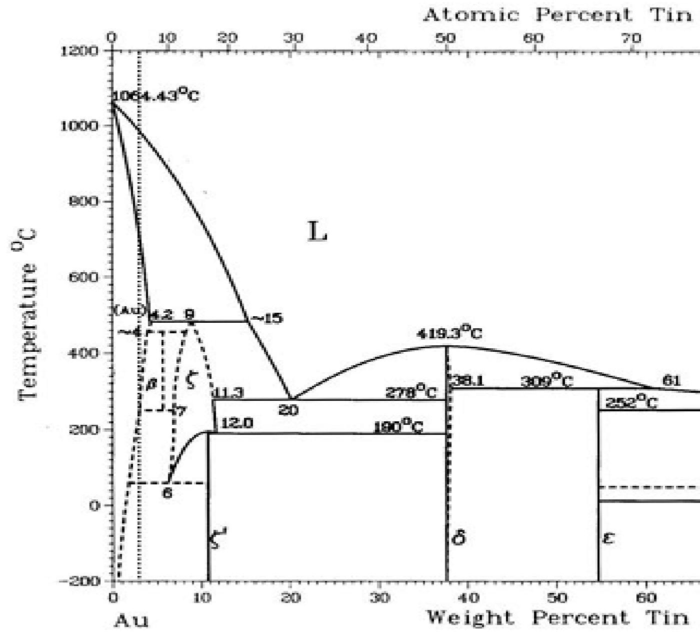
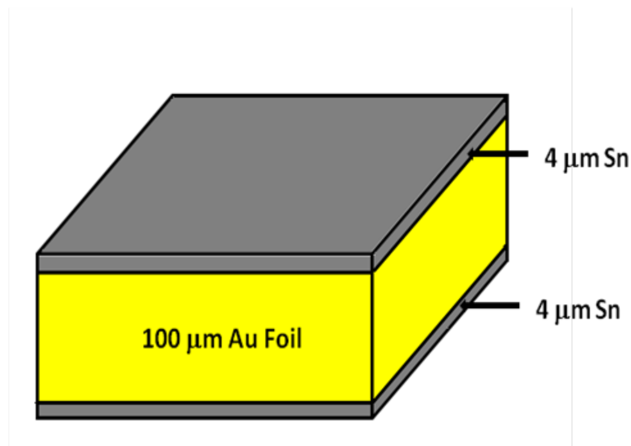



Figure 4.6 Au-Sn Phase Diagram [67]

4.4.2 Two TLP Die Attach Approaches:

1. To achieve the desired off-eutectic composition, a 100μm thick Au foil was electroplated with Sn on both surfaces (Figure 4.7) and cut to the same size of the die. To lower the concentration of Sn to 3wt%, the thickness of the Sn layer on both side of the Au foil was calculated from Equation (4.1) to be 4μm. With this thickness ratio, without any additional Au contribution from the SiC die or the substrate, the equilibrium preform concentration of Au would be ~97wt.%, and the resulting melting point would approach 700°C or higher as shown in the Au-Sn phase diagram. Dissolution of additional Au from the die or substrate would further increase the solidus temperature.




Dimensions not drawn to scale

Figure 4.7 Sn-Au-Sn Off-eutectic Thick Foil Sketch

$$\mathbf{W_{Sn}}\% = \frac{\rho_{Sn} * A * h_{Sn} * 2}{\rho_{Sn} * A * h_{Sn} * 2 + \rho_{Au} * A * h_{Au} * 2} \qquad \text{(eqn. 4.1)}$$

A: Surface bonded area

h: Thickness of Au or Sn

$\rho_{Sn}$: Density of Sn, 7.3g/cm$^3$

$\rho_{Au}$: Density of Au, 19.3 g/cm$^3$

Just prior to assembly, an argon plasma was used to sputter clean both the substrate and the die. An SST 3150 high vacuum furnace as used for the assembly. The bonding profile is shown in Figure 4.8. Process conditions and bonding parameters for assemblies were: peak temperature: 400$^o$C, bonding force: 500 grams, bonding time at peak temperature: 60 minutes. During the die attach process; the Sn layers liquefy, rapidly dissolving Au. As the Au dissolves, the melting point of the liquid increases. Once the liquid layers solidify, solid state Sn diffusion continues during the high temperature soak in the die attach thermal profile. The key to the die attach process is to allow sufficient soak time at temperature for the Sn to diffuse to a low enough concentration throughout the die attach layer, so that the solidus temperature exceeds the

maximum application temperature. The Sn will continue to diffuse toward the equilibrium concentration during the high temperature service life of the assembly.

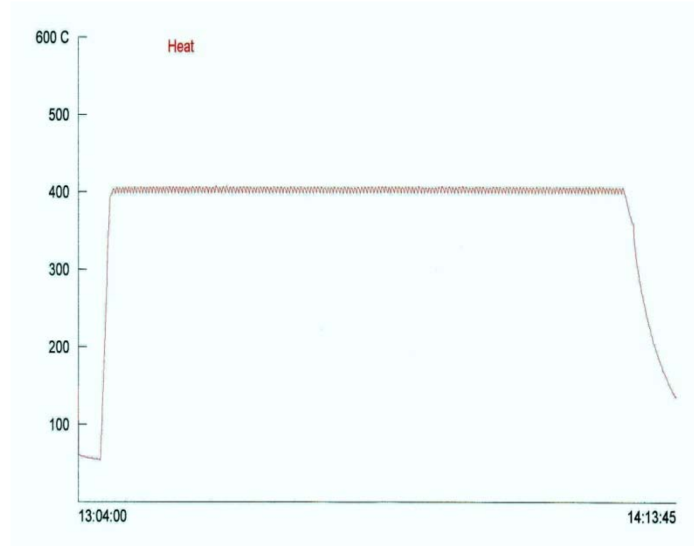



Figure 4.8 Off-eutectic Sn-Au-Sn SST Bonding Profile

2. The second approach used a 25.4μm thick eutectic Au-Sn (80:20wt%, with a melting point $T_m$= 280°C) preform that was only 33% the size of the die (limited volume eutectic Au-Sn). With proper bonding force during die attach process the preform will flow, filling the entire under-die area and creating a thinner layer of Au-Sn. The thick film Au on the AlN substrate provided a sink for Sn diffusion; lower the Sn concentration and raising the melting point. Theoretically, without considering any additional Au contribution from backside of die, assuming the "effective" Au-Sn preform to be the maximum thickness of 8.5μm (33% of the Au-Sn preform thickness before breezing), if 15μm Au in the thick film (17~20 μm thick) had been dissolved into the die attach, the maximum Sn concentration level in the "effective" die attach would be~5.8 wt%, and the corresponding solidus temperature was 498°C. However, in practice, the equilibrium Sn concentration in the die attach layer can be considerably smaller than 5.8%. That is because (1) during actual die attach process, Au-Sn preform spread beyond the die area,

resulting in the "effective" die attach thickness being smaller than 8.5 µm, (2) the electroplated Au on the backside of the die will be dissolved into the die attach, raising the Au concentration in the die attach, and (3) Sn will diffuse through Au thick film layer and form intermetallics with Pt in the metallization layer on the substrate, which also reduces the Sn level in attach. Therefore, for all the above reasons, there is enough Au (17~20µm) available in the Au/PtAu thick film layers to lower the Sn wt% in the die attach material and to raise the melting point of the die attach above 500$^{o}$C. The Actual Sn percentage in the die attach is shown in the following section 4.5. Figure 4.9 (a) and (b) show the sketch of package being assembled using limited volume Au-Sn die attach before and after Au-Sn was "squeezed" in brazing process.

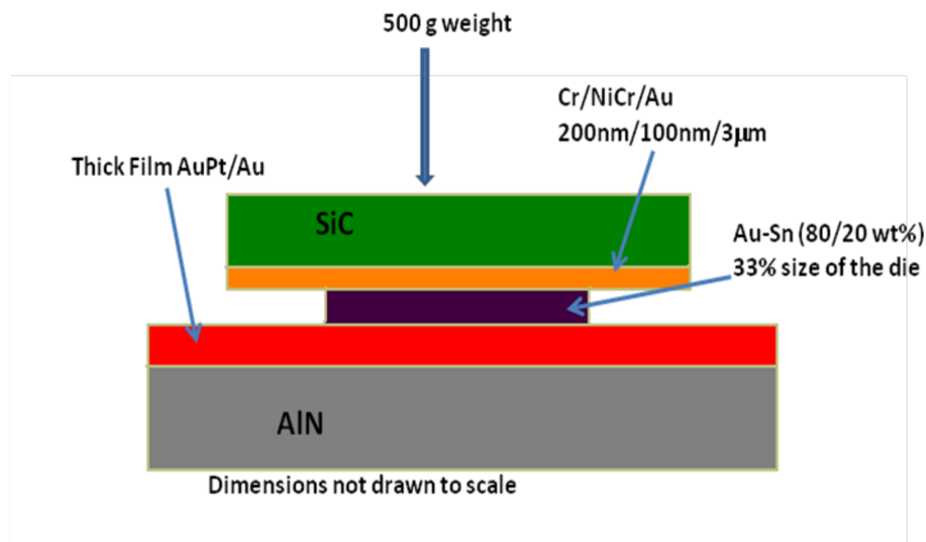



Figure 4.9 (a) Limited Volume Au-Sn Die Bonding Sketch before Brazing

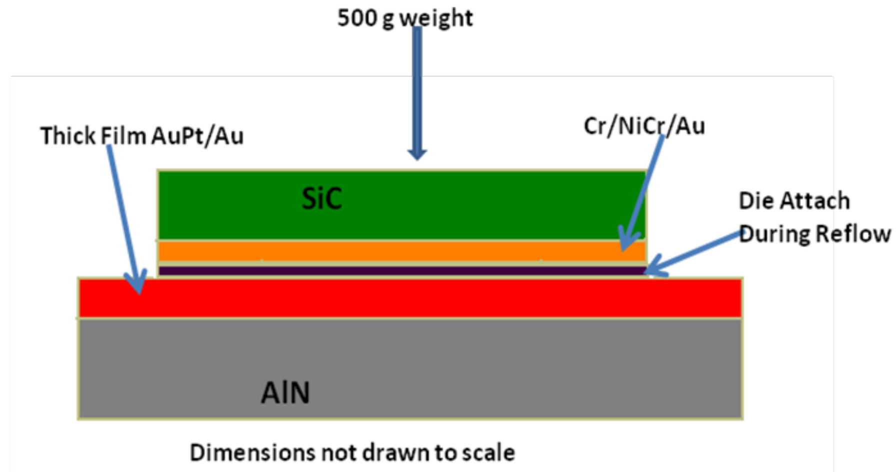



Figure 4.9 (b) Limited Volume Au-Sn Die Bonding Sketch During Reflow (The Au-Sn Was Squeezed to Create a Thinner Bond)

Just prior to assembly, an argon plasma was used to sputter clean both the substrate and the die. After the cleaning process, the 3.3mm x 3.3mm SiC die were assembled using a 2.85mm x 1.27mm x 25.4µm (thick) eutectic Au-Sn (80/20 wt%) preform in an SST high vacuum furnace. A 500 gram weight was used as the bonding force. The SST profile (Figure 4.10) for the eutectic Au-Sn limit volume die attach was: peak temperature 330°C for 5 minutes then a soak at 280°C for 30 minutes. The 30-minute soak time allowed Sn to diffuse into the thick film layers, lowering the Sn concentration throughout the die attach layer.

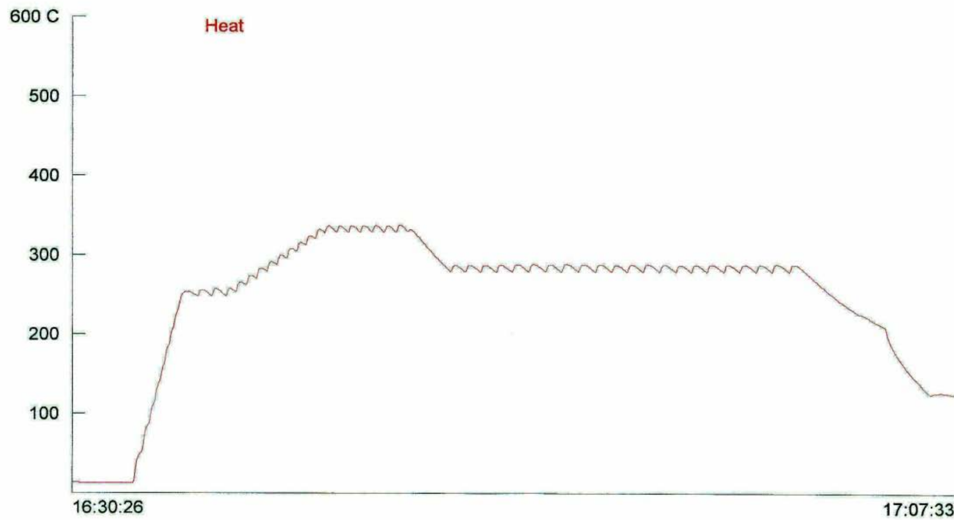



Figure 4.10 Limited Volume Eutectic Au-Sn (80/20 wt%) SST Bonding Profile

4.5 High Temperature Thermal Aging Test:

Test parts were assembled with three different combinations:

1. SiC die (3.3mm x 3.3mm) metalized with Ti/$TaSi_2$/Pt/Au were assembled on AlN metalized with Mo:Mn/Ni/Au using off-eutectic Sn-Au-Sn thick foil.

2. SiC die (3.3mm x 3.3mm) metalized with Cr/Ni-Cr/Au were assembled on PtAu/Au using off–eutectic Sn-Au-Sn thick foil.

3. SiC die (3.3mm x 3.3mm) metalized with Cr/Ni-Cr/Au were assembled on PtAu/Au using limited volume eutectic Au-Sn preform.

Note: The thin film deposition of Cr/NiCr/Au on test die used for off-eutectic Sn-Au-Sn and limited volume eutectic Au-Sn assemblies were fabricated with different thin film deposition runs.

Assembled parts were stored in Blue-MOV-10C high temperature chamber at 500ºC for long-term reliability tests and the die shear tests were performed at time intervals using a Dage 2400PC shear tester with a 100kg load cartridge. The die shear strength (kg of shear force

divided by the die area mm$^2$) as a function of storage time at 500$^o$C are shown in Figure 4.11, Figure 4.12 and Table 4.1. Shear strengths recorded as >9.18kg/mm$^2$ (100kg/10.89mm$^2$) in Table 4.1 indicates the die did not shear at the maximum shear force of the load cell (100kg).

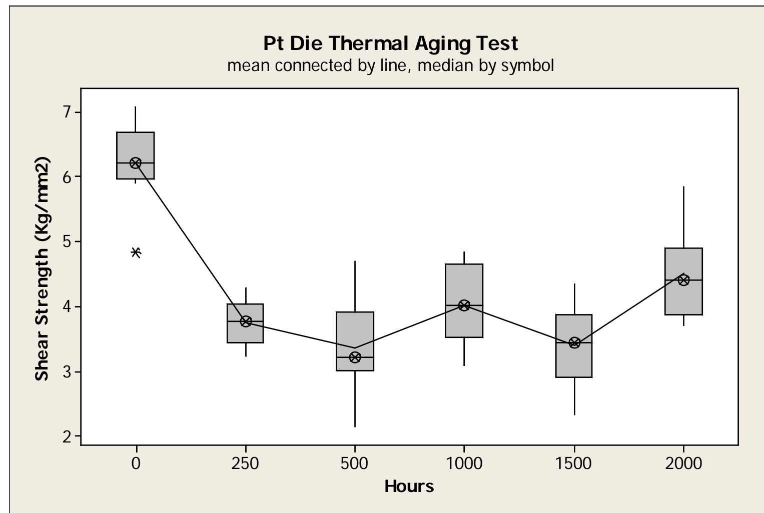



Figure 4.11 Ti/TaSi$_2$/Pt/Au Die Assembled with Off-Eutectic Sn-Au-Sn Shear Strength (kg/mm$^2$) as a Function of Storage Time at 500$^o$C

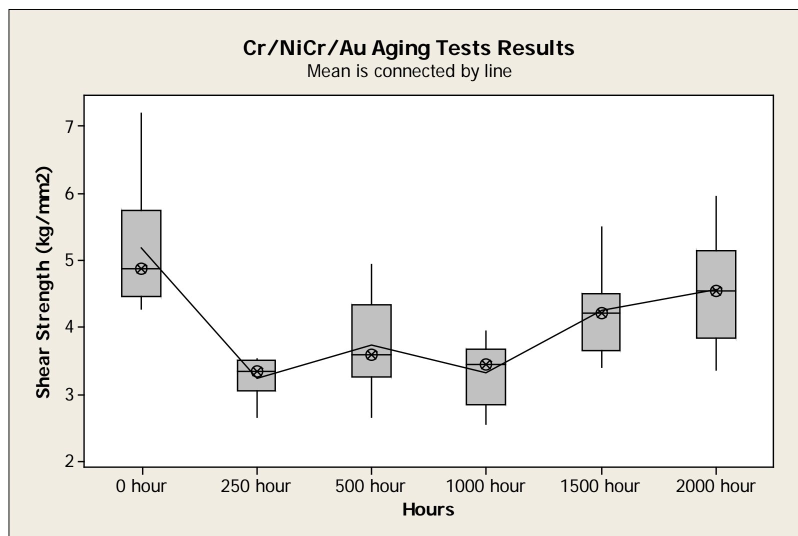



Figure 4.12 Cr/NiCr/Au Die Assembled with Off-Eutectic Sn-Au-Sn Shear Strength (kg/mm$^2$) as a Function of Storage Time at 500$^o$C

Table 4.1 Cr/NiCr/Au Die with Limited Volume AuSn Eutectic Die Attach Shear Strength ($kg/mm^2$) as a Function of Storage Time at $500^oC$

| Initial | 250 hour | 500 hour | 1200 hour | 1500 hour |
|---|---|---|---|---|
| >9.18 | >9.18 | >9.18 | >9.18 | >9.18 |
| >9.18 | >9.18 | >9.18 | >9.18 | 6.01 |
| >9.18 | >9.18 | >9.18 | >9.18 | 6.92 |
| >9.18 | 7.12 | >9.18 | >9.18 | 6.82 |
| 7.95 | 6.08 | 8.12 | 8.40 | 6.10 |
| 7.64 | 6.69 | 9.04 | 7.78 | 5.30 |
| 8.93 | 6.91 | 7.91 | 7.64 | 7.98 |
| 9.15 | 7.28 | 7.15 | 8.40 | 7.73 |

In both cases for assemblies with off-eutectic Sn-Au-Sn thick foil, die shear strength decrease during the first 250 hours then remain relatively stable through the remainder of the test. The initial failure mode for the Pt die assemblies was "failed inside the preform" and for Cr die assemblies the failure mode was mixed: "failed at the Cr to SiC interface" and "failed inside the preform". After 250 hours aging the shear strength stabilized and failure mode changed to "failed at the die". The failure interface for the Ti/TaSi/Pt/Au die was at the Pt layer, while for the Cr/NiCr/Au die, the failure was at the Cr layer. A depth profiling by Auger Electron Spectroscopy (AES) and Energy-dispersive X-ray spectroscopy (EDX) were used to analyze the Ti/$TaSi_2$/Pt/Au die fracture surface after 2000 hours thermal aging at $500^oC$. Results from both analyses show there was significant mixing of Pt and Sn at the predominate area of the Ti/$TaSi_2$/Pt/Au die fracture surface. Picture-(a) in Figure 4.13 (lower left) shows the scanning electron micrograph of Ti/$TaSi_2$/Pt/Au die fracture surface after 2000 hours storage at 500°C. Figure 4.13 (b) (upper left) is a close-up view of the frame in picture-(a), and Figure 4.13 (c) (right) is a close up view of the frame in Figure 4.13 (b) (left). EDX analysis shows at point 2 in Figure 4.13(c) there was mixing of Pt and Sn. Pt and Sn can form inter-metallic compounds. It is

believed that the diffusion of Sn into the Pt layer is the cause of the die shear strength decrease and the origin of the shift in failure mode.

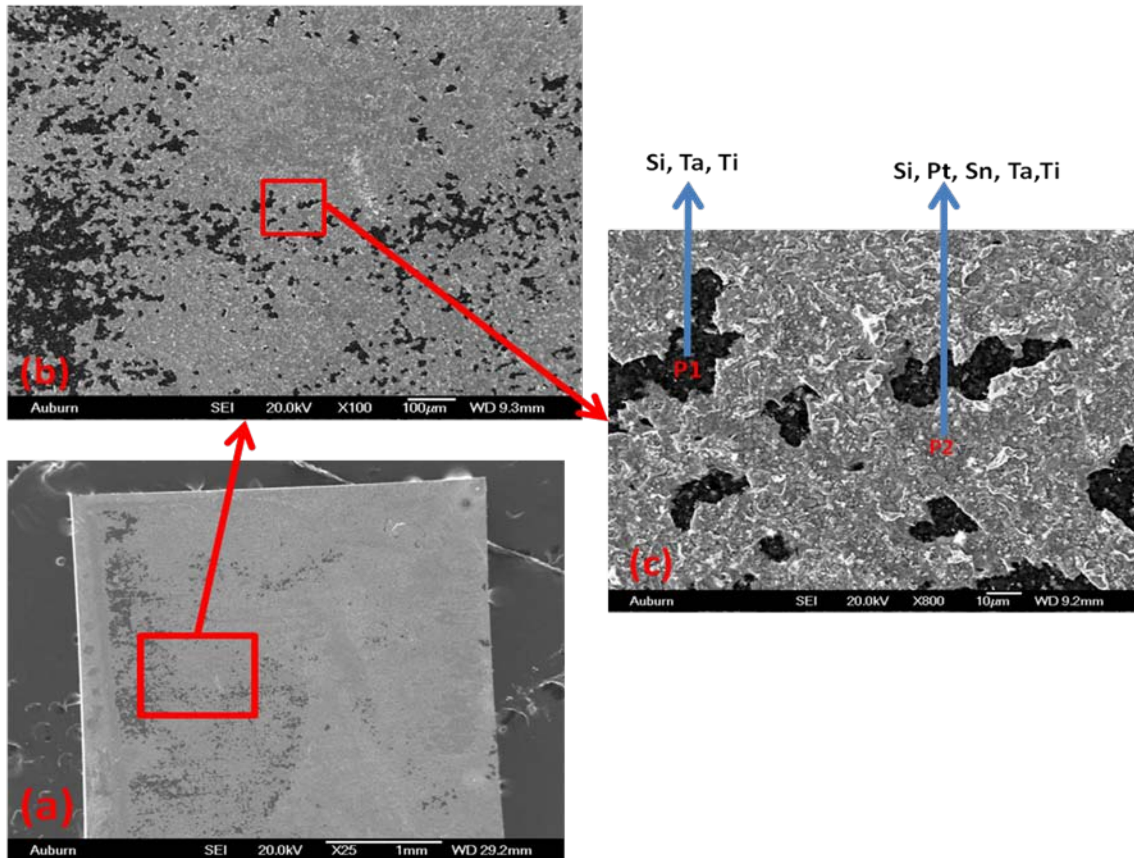



Figure 4.13 (a) Scanning Electron Micrograph of Pt Die Fracture Surface with Sn-Au-Sn Die Attach after 2000 Hours at 500°C, (b) Close-up View of the Frame in Figure (a), and (c) Close-up View of the Frame in Figure (b)

AES analysis on Cr/NiCr/Au die and PtAu thick film substrate fracture surfaces (Table 4.2-a) before aging show that only Au and Sn were present at the both fracture surface, which confirms the initial failures happened “inside preform”. The analysis on die and substrate fracture surface after 2000 hours aging show that Cr are present at the both fracture surfaces, which indicates Cr has diffused through NiCr and reached the Au and Sn die attach, this can be the cause of decease in shear strength.

Table 4.2(a) AES Analysis of Fracture Surface Element for Off-eutectic Au-Sn Die Attach

| Off Eutectic Sn-Au-Sn Die Attach | | | |
|---|---|---|---|
| Initial (before aging) | | 2000 hrs at 500℃ | |
| SFS | DFS | SFS | DFS |
| Au, Sn | Au, Sn | Cr, Sn | SiC, Cr |
| Note: SFS=substrate fracture surface, DFS=die fracture surface. | | | |

For the parts assembled using limited volume eutectic Au-Sn preform, the initial shear strength was high and 50% of the initial samples did not shear. The initial failure mode for the parts that did shear was "failed at die: thin film metal layers lifted from the SiC". After the first 1200 hours of aging, there was little decrease in die shear strength and the percentage of the assemblies that sheared remained constant. After 1500 hours aging, only one die did not shear, and the shear strength had decreased. However, the shear strength was still very high with respect to the minimum shear strength specified in Mil-Std-883. After aging the failure was at the Cr to SiC interface. AES and EDX were used to identify the elements presented on the die and substrate fracture surface before aging test and after 2000 hours aging at 500℃ (Table 4.2-b). Before aging the predominate area on the substrate fracture surface is Cr, and the die fracture surface is primarily SiC, so we can conclude that the limited number of initial failures are due to initial Cr adhesion. After 2000 hours aging, there is Au and Sn on the substrate surface, which indicates that Cr has diffused into the Au layer during the aging, Au and Sn have also diffused through Cr/Ni layer and reached to the fracture surface, the diffusion of Cr into Au layer can be the cause of decrease in adhesion of thin film stack to SiC.

Table 4.2(b) AES Analysis of Fracture Surface Element Limited Volume Au-Sn Die Attach

| | Limited Volume Au-Sn Die Attach | | | |
|---|---|---|---|---|
| | Initial (before aging) | | 2000 hrs at 500℃ | |
| | SFS | DFS | SFS | DFS |
| AES analyses | Cr | SiC | Au, Sn | SiC |
| Note: SFS=substrate fracture surface, DFS=die fracture surface. | | | | |

4.6 Thermal Cycling Test

A thermal cycle test was performed with the thermal cycle profile from 35$^{o}$C to 500$^{o}$C in air as shown in Figure 4.14, which consisted of 22 minutes ramp from 35$^{o}$C to 500$^{o}$C, then 4 minutes soak at 500$^{o}$C, followed by 30 minutes cool down from 500°C to 35°C. The test SiC die were 3.3mm x 3.3mm with backside metallizations of Ti/TaSi/Pt/Au (100nm/400nm/200nm/100nm) and Cr/NiCr/Au (200nm/100nm/3µm). The test substrates were AlN metalized with thick film PtAu/Au.

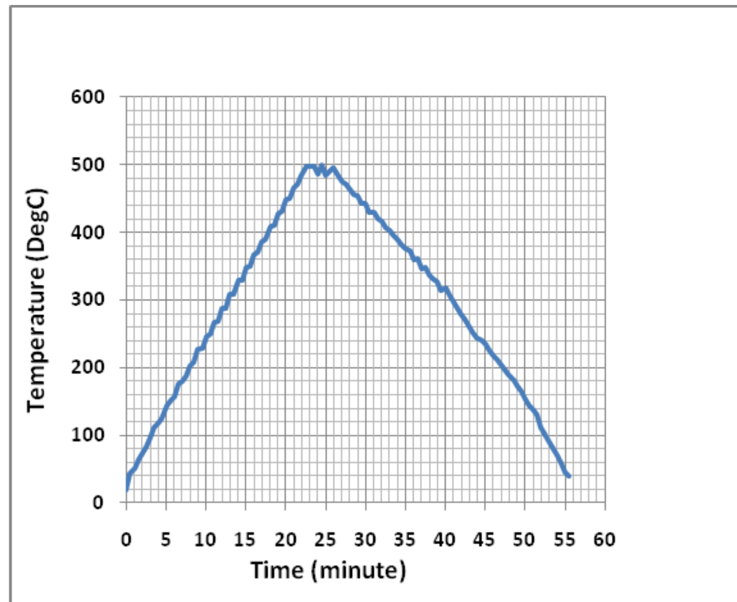



Figure 4.14 Thermal Cycle Profile

Test vehicles were assembled with three different combinations for comparison:

1. Ti/$TaSi_2$/Pt/Au SiC die were assembled on AlN using off-eutectic Sn-Au-Sn thick foil

2. Cr/Ni-Cr/Au SiC die were assembled using off-eutectic Sn-Au-Sn thick foil

3. Cr/Ni-Cr/Au SiC die were assembled using limited volume eutectic Au-Sn preforms

The die shear results for the Sn-Au-Sn assemblies are shown in Tables 4.3 and 4.4 Shear strengths recorded as >9.18kg/mm$^2$ indicates the die did not shear at the maximum shear force of the load cell (100kg). For off-eutectic Sn-Au-Sn die attach assemblies, thermal cycling test results for Ti/$TaSi_2$/Pt/Au and Cr/NiCr/Au test vehicles were similar: both had high initial average shear force and the initial failure mode was “failed inside the preform”. However, after 500 cycles, die shear strength dropped to average of 1.04-1.36kg/mm$^2$ and the die shear strength was 0.1-0.3kg/mm$^2$ after 1000 cycles

Table 4.3 Pt Die with Off-Eutectic Die Attach Thermal Cycle Shear Results

| 0 cycle (kg/mm$^2$) | 250 cycles (kg/mm$^2$) | 500 cycles (kg/mm$^2$) | 1000 cycles (kg/mm$^2$) |
|---|---|---|---|
| >9.18 | 2.05 | 0.97 | <0.18 |
| >9.18 | 1.45 | 0.66 | <0.18 |
| >9.18 | 1.53 | 1.80 | <0.18 |
| >9.18 | 1.95 | 0.82 | <0.18 |
| >9.18 | 1.90 | 1.43 | <0.18 |
| 7.67 | 1.35 | 0.60 | <0.18 |
| 7.14 | 1.43 | 0.94 | <0.18 |

Table 4.4 Cr/NiCr/Au Die with Off-Eutectic Sn-Au-Sn Die Attach
Thermal Cycle Shear Results

| 0 cycles ($kg/mm^2$) | 110 cycles ($kg/mm^2$) | 250 cycles ($kg/mm^2$) | 500 cycles ($kg/mm^2$) |
|---|---|---|---|
| >9.18 | 5.08 | 1.52 | 0.30 |
| >9.18 | 3.96 | 1.96 | 0.21 |
| >9.18 | 5.57 | 1.06 | 0.20 |
| >9.18 | 4.44 | 1.25 | 0.56 |
| 6.94 | 5.66 | 1.44 | 0.47 |
| 7.08 | 4.81 | 0.96 | 0.26 |
| 7.98 | 4.99 | | |
| 6.83 | 5.08 | | |

A cross section micrograph of a Ti/$TaSi_2$/Pt/Au assembly (Figure 4.15) after 300 cycles from 35°C to 500°C shows two cracks occurred at the periphery of SiC die propagating into the bond joint, separating the preform from both the die and the substrate. Figure 4.16 (a) is a cross section micrograph of a Cr/NiCr/Au assembly after 500 cycles from 35°C to 500°C. The die and the off-eutectic Sn-Au-Sn thick foil are still attached but separated from the substrate. A crack also occurred at the die to preform interface.

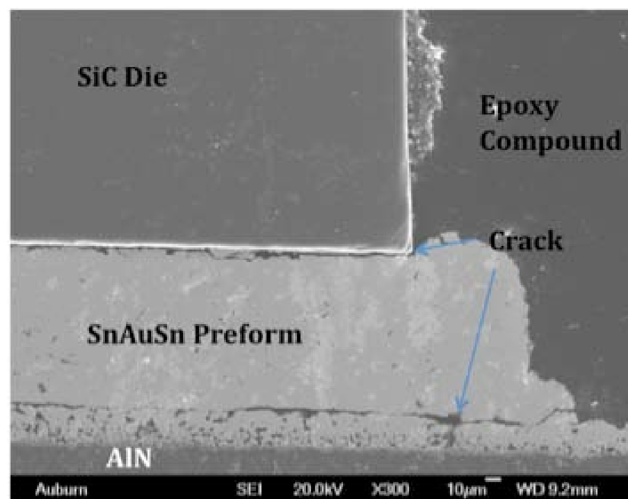



Figure 4.15 Cross Section Micrograph of a Pt Die with a Off-Eutectic Sn-Au-Sn Preform after 300 cycles from 35°C to 500°C

To determine the failure mechanism, EDX analysis was performed on cross sections of off-eutectic Sn-Au-Sn samples as-assembled and after aging for 25 hours to investigate the Sn distribution in the off-eutectic Sn-Au-Sn die attach and the thick film layers. The elemental profile across the die attach/thick film layers shows that as-assembled, the Sn percentage is higher at the die attach edge and lower in the middle, which indicates that original plated Sn in the Sn-Au-Sn preform did not diffuse very far during the initial assembly (Figure 4.17). This higher Sn concentration results in a more brittle region. During thermal cycling, stresses built up causing a crack to form within this brittle region. This would explain the two cracks (top and bottom of the preform) that developed in the Sn-Au-Sn assembled test vehicles during thermal cycling. Figure 4.16 (b) is a SEM picture of the sheared/detached AlN substrate fracture surface after 500 cycles from 35$^{o}$C to 500$^{o}$C, correlated with the die fracture in Figure 4.16-a. The periphery of the printed square PtAu thick film conductor pads has been lifted during shear test. The EDS analysis of point 1 on the AlN substrate fracture surface (labeled as P1 in Figure 4.16 (b)) shows there is a high Sn concentration on the substrate fracture surface, which confirms the theory that the insufficient Sn diffusion in the as–assembled assemblies should be the cause crack forming during cycling.

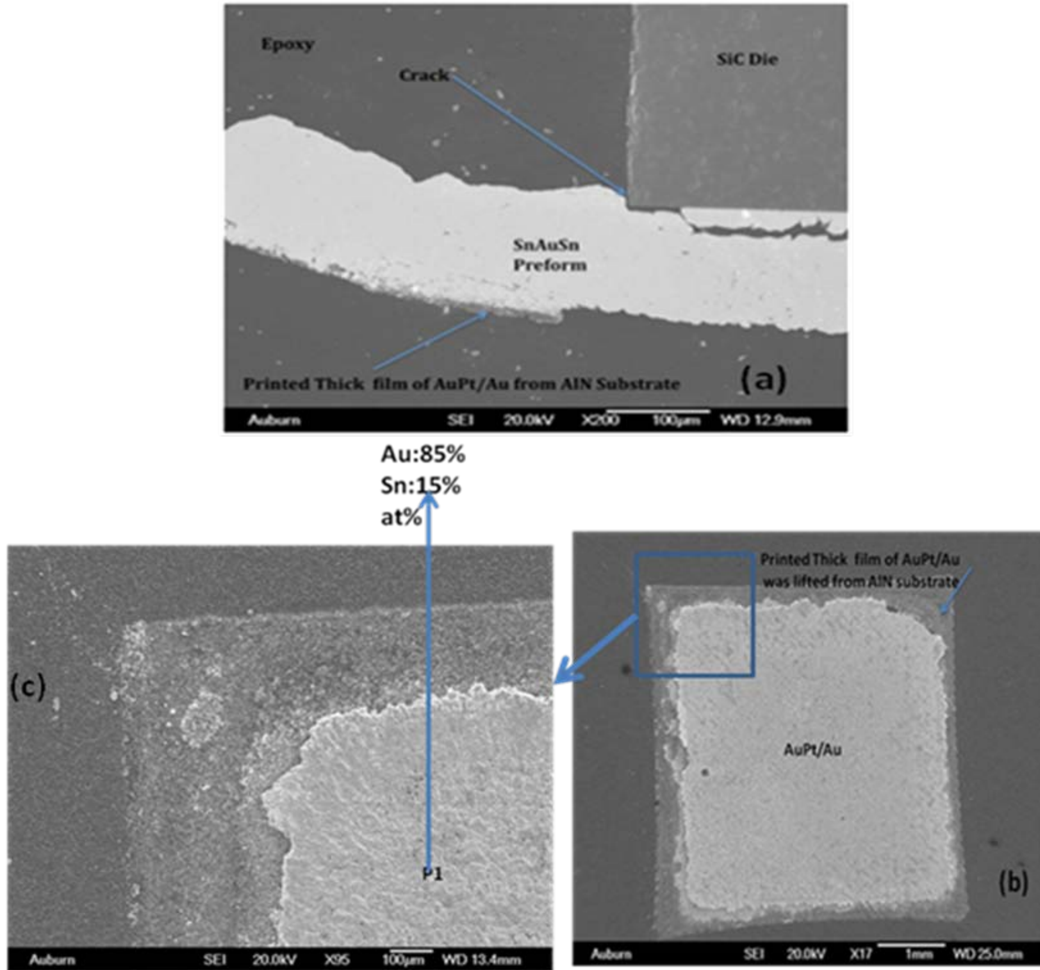
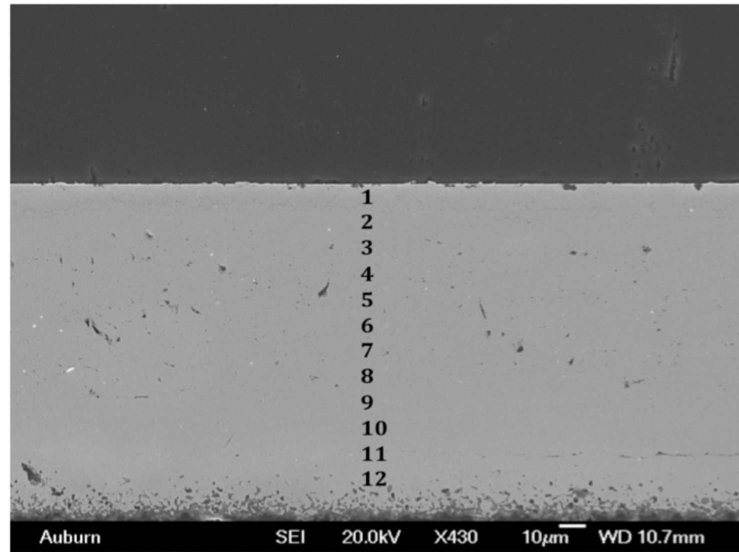



Figure 4.16 (a) Cross Section Micrograph of a Cr/NiCr/Au Die with a Off-Eutectic Sn-Au-Sn Preform after 500 Cycles From 35°C to 500°C, (b) SEM Picture of the Sheared AlN Substrate Fracture Surface after 500 cycles from 35°C to 500°C, and (c) Micrograph is a Close-up View of the Frame in Figure (b)

After 25 hours of storage at 500°C, the Sn has diffused further into the Au foil, and the Sn concentration is more evenly distributed (Figure 4.18). Longer high temperature diffusion time before thermal cycle testing, might improve thermal cycle performance. The peak in Sn concentration at the die side may help explain the initial decreases in die shear strength with aging observed for the Sn-Au-Sn preform. The exact mechanism requires further study. The peak in the Sn at the substrate surface with aging indicates reaction between the Sn and the Pt in the thick film PtAu layer.



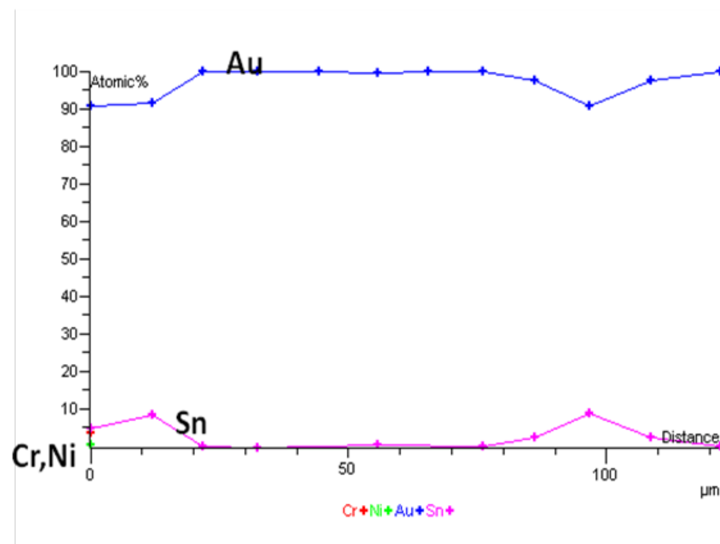
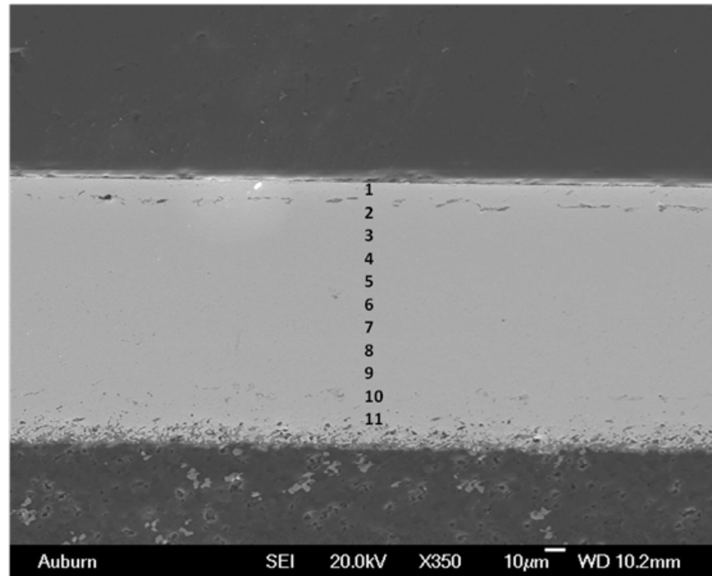




Figure 4.17 Elemental Analysis Across the Bond Layer of the As-assembled Cr/NiCr/Au Test Sample with Off-eutectic Sn-Au-Sn Die Attach

The die shear results for assemblies with limited volume eutectic AuSn are presented in Table 4.5. The die shear results are significantly better than for the off-eutectic Sn-Au-Sn preform assemblies. Figure 4.19 is a cross section after 500 thermal cycles. No cracks were observed. For limited volume eutectic AuSn die attach, EDX analysis of a cross section of the as-assembled die attach shows a low Sn concentration near the die (~5 at%, or 3 wt%), low Sn

concentration (~7.5 at%, or 4.6 wt%) through the braze, then a higher Sn concentration in the PtAu layer (Figure 4.20) because the Sn reacts with the Pt to form intermetallics, however, this does not appear to lead to failures.



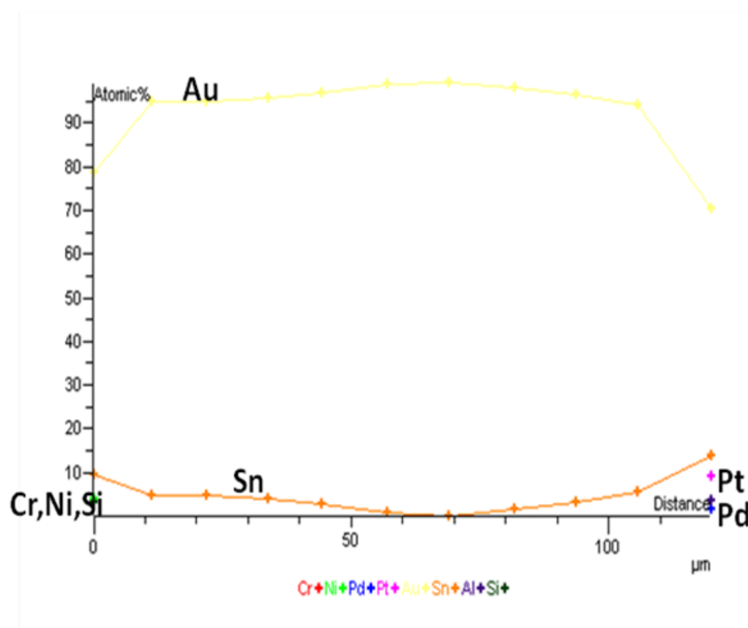




Figure 4.18 Line Profile of Cr/NiCr/Au Die with Off-Eutectic Sn-Au-Sn Die Attach after 25 Hours at 500$^{o}$C

Table 4.5 Cr/NiCr/Au Die with Limited Volume Eutectic Au-Sn
Thermal Cycle Shear Results

| 0 cycles ($kg/mm^2$) | 110 cycles ($kg/mm^2$) | 250 cycles ($kg/mm^2$) | 500 cycles ($kg/mm^2$) | 1000 cycles ($kg/mm^2$) |
|---|---|---|---|---|
| >9.18 | >9.18 | >9.18 | 8.82 | 6.96 |
| >9.18 | >9.18 | >9.18 | 7.96 | 7.99 |
| >9.18 | >9.18 | >9.18 | 9.09 | 7.0 |
| >9.18 | >9.18 | >9.18 | 8.01 | 8.27 |
| >9.18 | >9.18 | 7.30 | 6.37 | 7.87 |
| >9.18 | 9.07 | 7.06 | 7.60 | 8.36 |
| >9.18 | 7.79 | 6.39 | 7.0 | 7.26 |
| | 8.02 | 7.64 | | 7.36 |

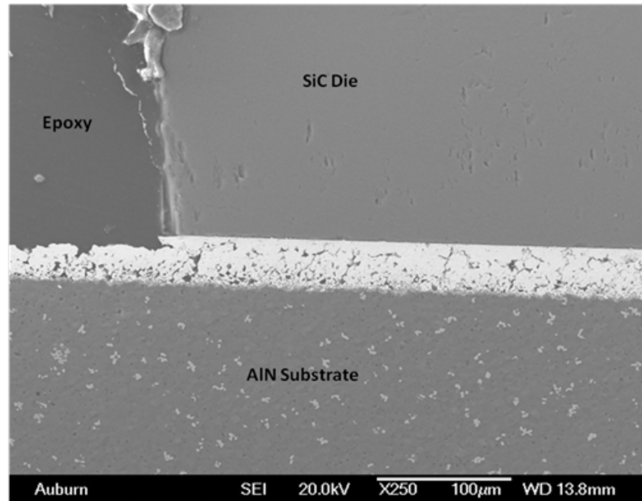
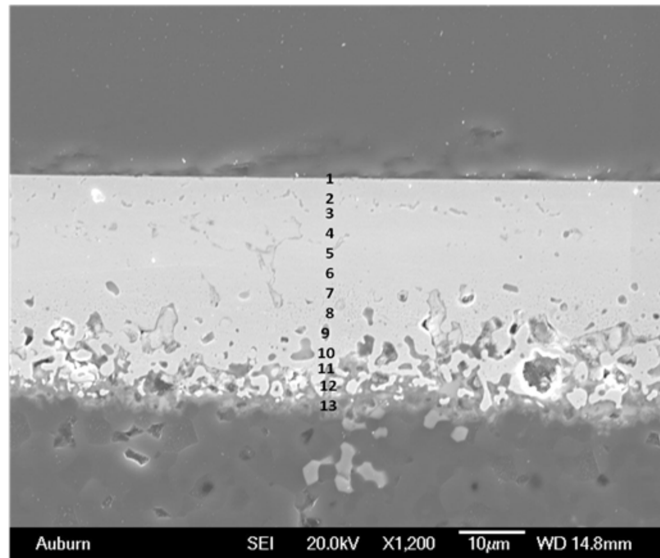



Figure 4.19 Cross Section Micrograph of the Cr/NiCr/Au Die with Limited Volume Eutectic AuSn Die Attach after 500 cycles from 35°C to 500°C



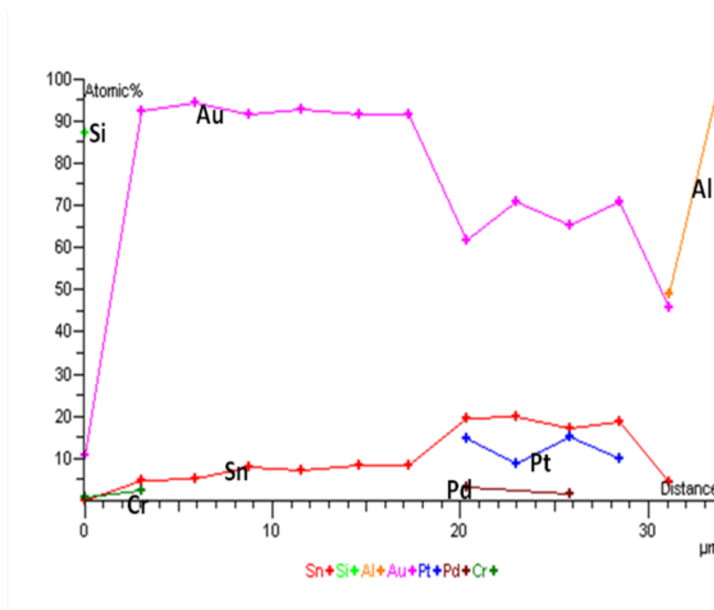




Figure 4.20 Elemental Analysis across the Bond Layer of the As-assembled Cr/NiCr/Au Test Sample with Limited Volume Eutectic Au-Sn Die Attach

## 4.7 Summary

Liquid phase transient bonding with Au-Sn provides a method to achieve die attach for applications up to 500°C. The test results indicate that using a limited volume eutectic Au-Sn preform with excess Au provided by the die or substrate metallization was superior to the thick

foil Sn-Au-Sn prefrom. The Sn-Au-Sn preform relies heavily on solid state diffusion that is slower than the liquid phase diffusion that occurs with the eutectic Au-Sn preform.

# CHAPTER 5 HERMETIC SEAL PACKAGES

A true hermetically sealed package can prevent intrusion of contaminations for an indefinite period of time. In practice, however, even in a perfectly sealed structure, diffusion will occur overtime, allowing the smaller molecules such as helium or water vapor to penetrate the barrier medium and ultimately reach equilibrium within the package interior [34]. A hermetic package is conventionally defined as one in which the finite leak rate of helium is below a specific rate with reference to Mil-Std-883, method 1014 [41]. Both metal and ceramic packages have been extensively employed to handle, test and seal off circuits from the environment. In hermetic packaging for HTE, a metal or ceramic cavity package encloses the assembled circuit; then a metal lid is either welded or soldered on. Ceramic lids metalized with seal ring may also be sealed directly to ceramic package bases [41].

Two packaging approaches have been developed in this project: One path was an integrated package that uses a metalized AlN substrate as the package base. A machined AlN cavity lid was sealed to the AlN substrate to create a hermetic cavity for the die. For the second approach, a commercial off the shelf (COTS) $Al_2O_3$ package has been evaluated. In this case the metalized AlN substrate with the die attached and wire bonded could be hermetically sealed inside the ceramic package.

5.1 Alumina 40 Pin Hybrid Hermetic Seal Package

5.1.1 Alumina 40 Pin Hybrid Package

The 40 lead hybrid package was purchased from Chelsea Technology Inc. Metal seal frame around the periphery of the cavity is 250μm thick Kovar® successively plated with 2.5 μm of Ni and 1.5 μm of Au. Figure 5.1 is a picture of COTS 40-lead hybrid package body and Figure 5.2 is the 40 pin hybrid package with a metalized AlN substrate attached inside, and a SiC die is attached to the AlN substrate.

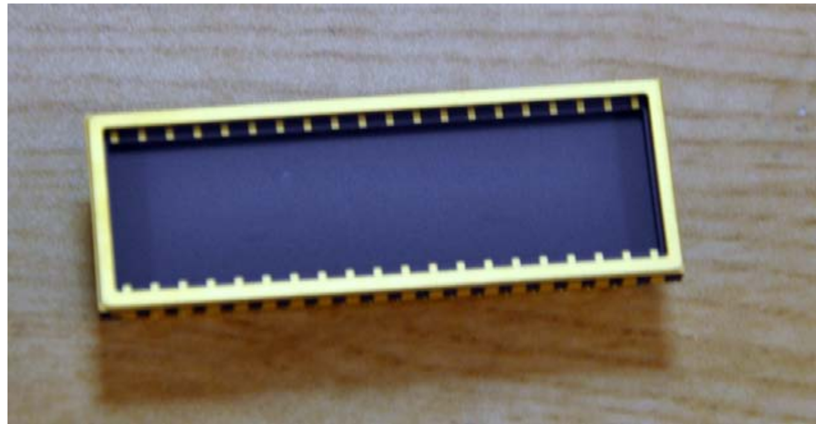


Figure 5.1 COTS Ceramic 40 Pin DIP Package

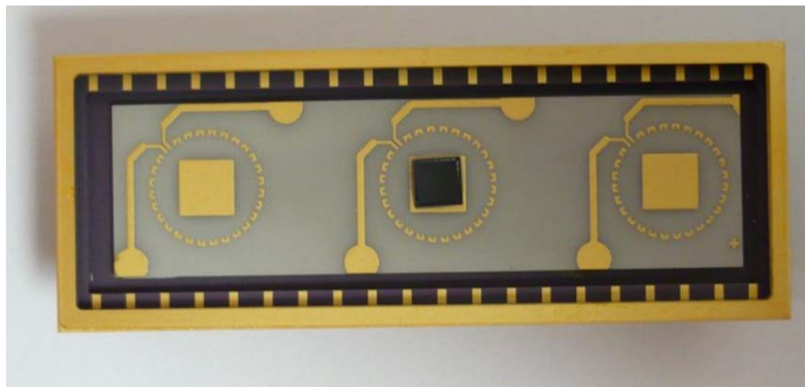


Figure 5.2 Metalized AlN Substrate Attached in COTS Ceramic 40 Pin Package, with One SiC Die Attached

5.1.2 Au-Sn Pre-Attach

The standard lid for the COTS 40 pin hybrid package is Kovar® lid. At temperature below 400ºC, the CTE of Kovar® (≈5 ppm/ ºC) approximately matches that of alumina. However, the CTE of Kovar® increases dramatically above 400ºC and may not be compatible with alumina and high temperature brazes for large area seal ring (Figure 5.3 shows the CTE of Kovar as a function of temperature ) [68, 30]. For these reasons, a 96% alumina flat lid (50.8mm x 19.56mm x 1.02mm, manufactured by Stellar Inc.), which was metalized with 0.3 µm refractory metal Mo-Mn, then successively plated with 2.5-7.5µm electroless Ni and 0.4µm electroless Au around the periphery of the sealing face (Figure 5.4), was used to hermetically seal the 40-pin ceramic packages by the TLP bonding method with off Sn-Au-Sn thick foil. To make the off-eutectic Sn-Au-Sn thick foil: a 100µm Au ring was electroplated with 4µm thick of Sn on both sides.

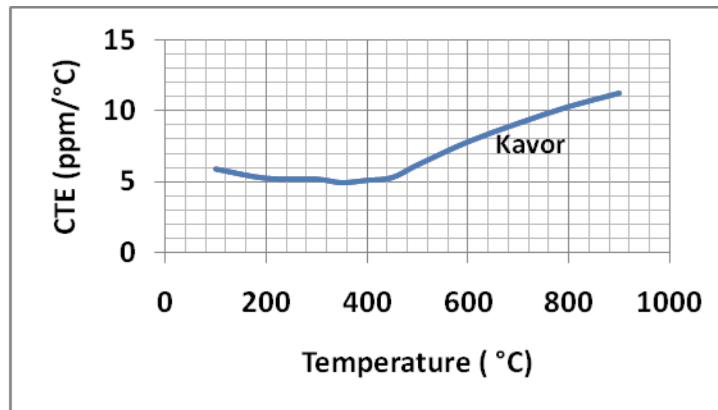



Figure 5.3 Coefficient of Thermal Expansion for Kovar® as a Function of Temperature

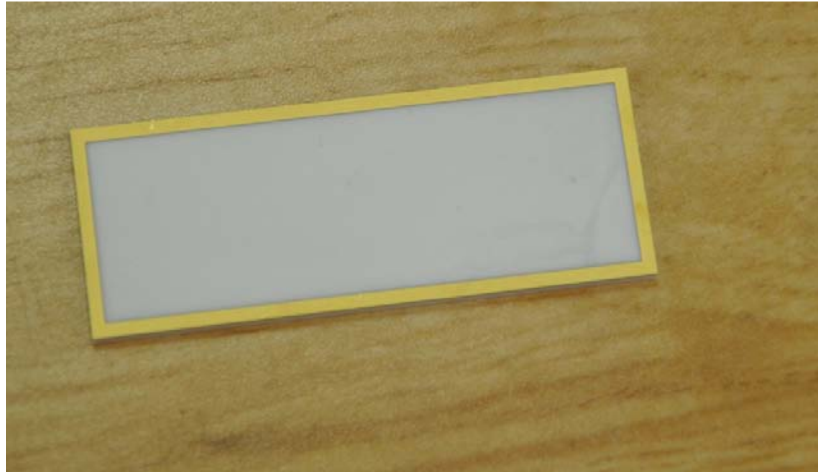


Figure 5.4 96% Alumina Flat Lid with Mo-Mn/Ni/Au Metallization

Prior to Sn-Au-Sn TLP bonding, two 25.4μm thick eutectic Au-Sn (80:20 wt%) preform rings were pre-attached separately to the outer perimeter of the flat lid and to the peripheral seal area of the 40 pin ceramic package. During the lid attach process, the 100μm thick Au foil in the Sn-Au-Sn preform acted as a sink for Sn diffusion. Unlike the eutectic AuSn preform, Sn-Au-Sn thick foil will not "flow" during the high temperature TLP bonding process, and because the seal areas on the flat lid and 40 pin package are not completely flat, there could be some small gaps between the flat lid and 40 pin package. This can cause possible voids in the seal area, which will later lead to leaking. The goal of the Au-Sn pre-attachment is to create enough liquid solder to wet the entire seal area and "fill the gap" during TLP bonding and to help produce a void free lid attach. There are two important factors that need to be taken into consideration when designing the pre-attachment process. (1) Because of the high surface tension and zero wetting angle Au-Sn does not flow easily on a horizontal surface, although it has excellent wettability [69], proper pressure is required to ensure good, void free bonding [69]. In this process, a 1850gram weight was added to the assembly as the bonding force and a frame shaped tool (same shape as the seal area) was designed to apply pressure only to the seal area. (2) The eutectic Au-Sn ring pre-attach

process was completed in the SST-vacuum furnace oven using a peak temperature of 320°C profile (Figure 5.5). The soak time at peak temperature is another important factor. It should be just enough time for preform ring to wet the seal area, but not too long otherwise Au-Sn will dissolve too much Au from the metallization on the lid and package. Soak time at peak temperature is 2 minutes in this ring pre-attach profile.

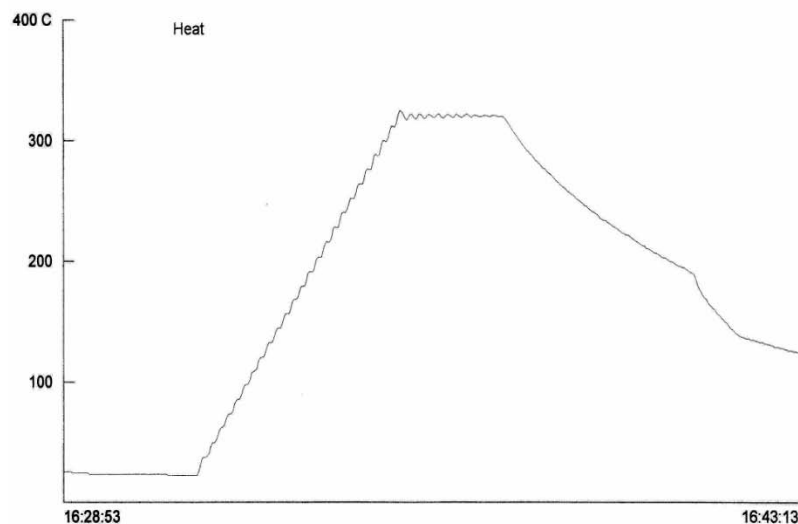
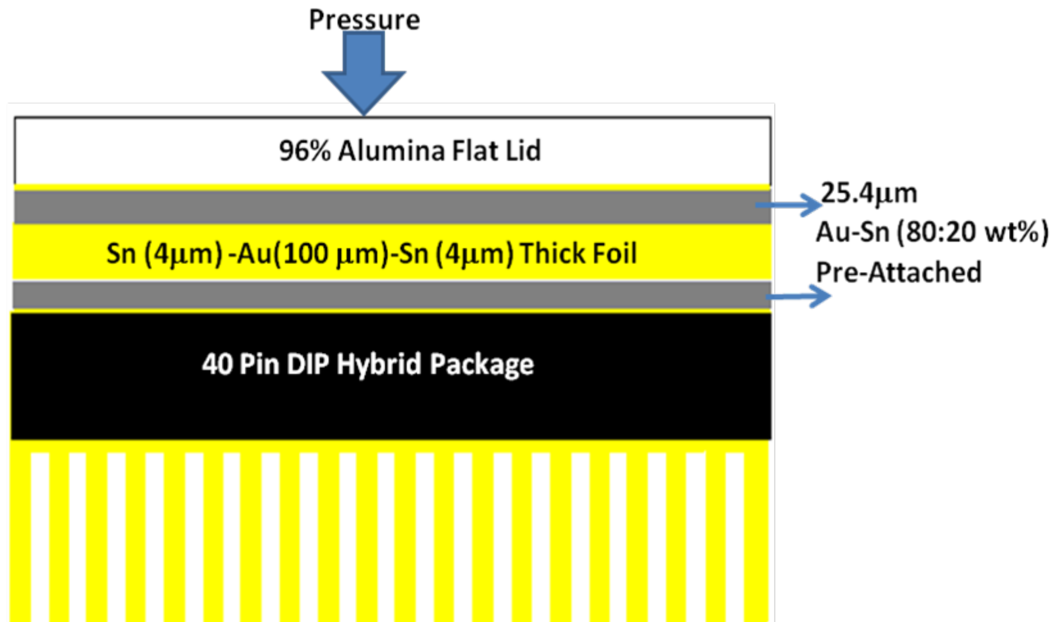



Figure 5.5 Eutectic AuSn Preform Ring Pre-Attach Profile

5.1.3 Off-Eutectic Sn-Au-Sn TLP Lid Seal Process

The TLP bonding process for hermetic sealing was performed in a SST 3150 high vacuum furnace and all components were placed within a specially designed graphite boat. The details of the sealing process are as follows: Just prior to the assembly, argon plasma was used to sputter clean the lid and the package. Off-eutectic Sn-Au-Sn foil was then inserted/sandwiched between the flat lid and the package (Figure 5.6), bonding force was 1850 grams and the same tool used in Au-Sn pre-attach (section 5.1.2) was used to apply force only to the seal area. The bonding profile is shown in Figure 5.7. The profile included a 10 minutes ramping form room temperature to 360 ºC (peak temperature), a 2 minutes soak at peak temperature followed by a soak at 280 ºC for 40 minutes. The

40-minuted soak at 280 ℃ was designed to give time for Sn to diffuse into the Au, raising the melting point of the lid attach. A picture of sealed package is shown in Figure 5.7.




Dimensions Not Drawn to Scale

Figure 5.6 Schematic Side view of 40 Pin Package Lid Attach

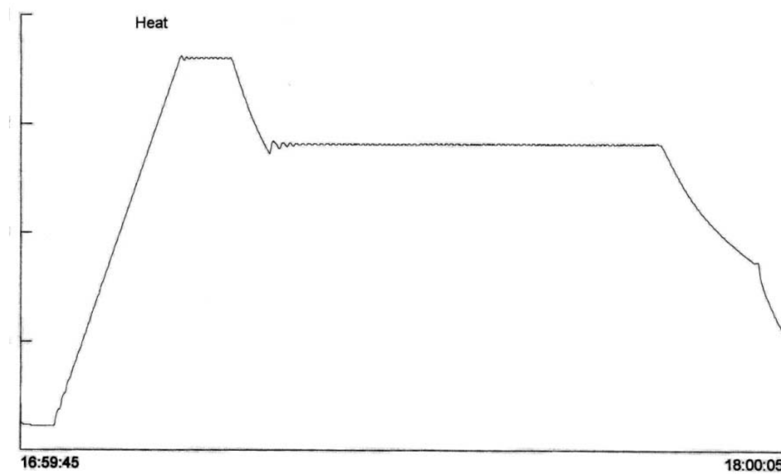



Figure 5.7 Off-Eutectic SnAuSn Thick Foil TLP Lid Sealing Profile
Ceramic DIP Package Sealed with Ceramic Flat Lid

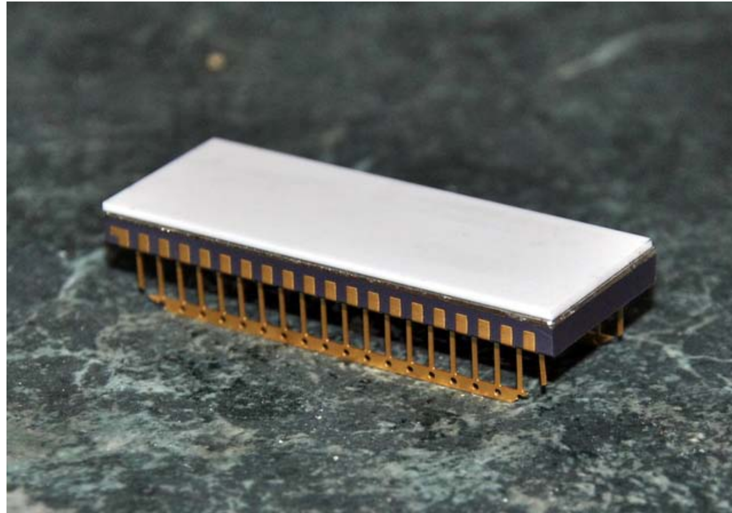


Figure 5.8 Picture of 40 Pin Hybrid Package Hermetically Sealed with Metalized Flat Lid

Without including the additional Au dissolved form the package and lid metallization into the lid attach, the equilibrium Sn weight percentage in the new lid attach (two eutectic AuSn preforms and 1 SnAuSn thick foil ) is ~7.5 wt%, which is calculated using the equation below; and at Sn weight percentage being 7.5%, the expected solidus tempersture as shown in the Au-Sn phase diagram (Figure 5.8) is ~498°C.

$$\text{Sn wt\%} = \frac{(14.5*2*0.2+2*4*7.3)*A}{(14.5*25*2+2*4*7.3+100*19.3)*A} * 100\% = 7.5\%$$

(1) Two pieces of eutectic Au:Sn (80:20 wt%) preform are used, each is 25 μm thick with density of 14.5g/cm$^3$; [68]

(2) The thick foil is SnAuSn with Sn4μm/Au100μm/Sn4μm;

(3) Au density: 19.3g/cm$^3$, Sn density: 7.3g/cm$^3$;

(4) A is the sealing surface area.

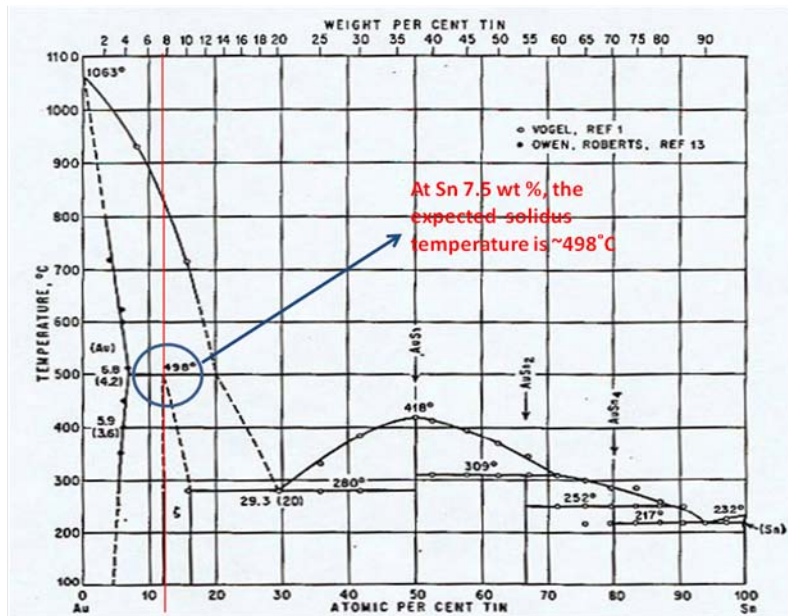



Figure 5.9 Au-Sn Phase Diagram [70]

### 5.1.4 Leak Testing

There are many different methods available for fine and gross leak testing. In this dissertation, a gross leak testing method, bubble test, was used to detect any leakage. During testing, the sealed package was immersed into perfluoropolyehter (which has a high boiling temperature than water) at a temperature above the boiling point of water ~110°C. When exposed to the high temperature, the air or vaporized moisture located within the cavity of the package expands, generating an elevated pressure inside the devise causing a bubble stream to emanate from the leak site. If no bubble stream is observed, the package passes the gross leak test. The 40 pin hybrid ceramic package hermetically sealed using the process (picture shown in Figure 5.7) in section 5.1 has successfully passed the gross leak test.

## 5.2 AlN Integrated Package Hermetic Seal

Because of the factors such as thermal conductivity and thermal expansion coefficients, as have been discussed in the previous chapters, AlN should provide better packaging platform than alumina for high temperature SiC electronics. Attempts at creating a hermetic, high

temperature AlN based package were made in this project, and the key elements of the packaging process described in this section are: (1) AlN package base: a thick film metalized AlN substrate was laminated with low temperature cofired ceramic tape frame, after lamination, the LTCC frame was metalized with Au thick film braze seal ring, (2) AlN cavity lid: a machined AlN cavity lid was metalized with AuPt/Au thick film seal ring, and (3) a two step off-eutectic Au-Sn LTP lid attach process (as described in section 5.12-5.13). Figure 5.10 illustrates the key elements in an AlN hermetic package.

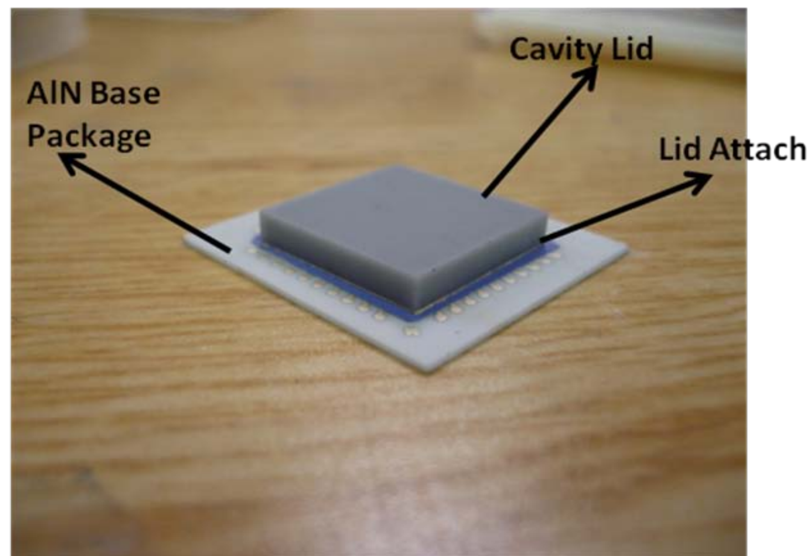



Figure 5.10 Key Elements in an AlN Integrated Package

5.2.1 AlN Cavity Lid Fabrication

The metallization process used for the AlN cavity lid is the following: First a layer of AuPtPd conductive paste (C6029 from Heraeus®) was printed on the perimeter of a machined AlN lid (shown in Figure 5.11 (a)) with a 280-mesh screen. The printed paste was then dried and fired using the same processes/profile as described in section 4.1. The thickness of the AuPt thick film after firing was 12-16μm. The second layer of Au (5063D from Dupont) paste was

then printed over the AuPt, dried and fired with the same profile. Figure 5.11(b) shows the finished AlN lid, the total thickness of finished thick film metallization was ~30-40μm.

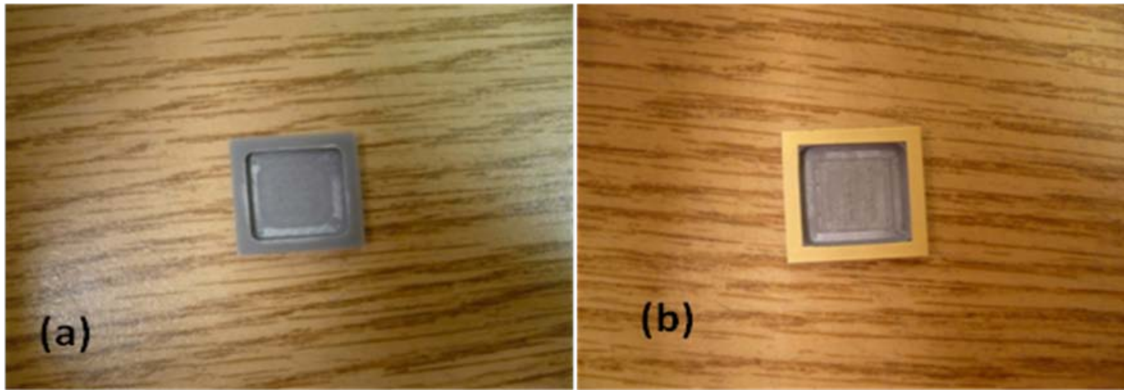



Figure 5.11 (a) Machined AlN Cavity Lid before Metallization and (b) Perimeter of the AlN Lid was Metalized with Thick Film PtAu/Au.

5.2.2 AlN Package Base Fabrication

AlN package base fabrication for the AlN integrated hermetic seal package approach was a process sequence that consisted of three major steps: 1) metalizing the AlN substrate with thick film metallization, 2) the metalized ALN substrate was laminated with LTCC (low temperature co-fired ceramic) tape for insulation, and 3) a Au seal ring was printed and fired onto the LTCC tape. The detailed process flow was:

(1) Thick film metallization of the AlN substrate: AlN substrate (51mm x 51mm x 0.56mm, purchased from Stellar Inc.) was metalized with two layers of thick film conductors: AuPt and Au (Au as the top layer) using the same process described in section 5.2.1. Figure 5.12 (a) is a picture of an AlN substrate with the AuPt thick film and Figure 5.12 (b) is a picture of the AlN substrate with Au over AuPt.

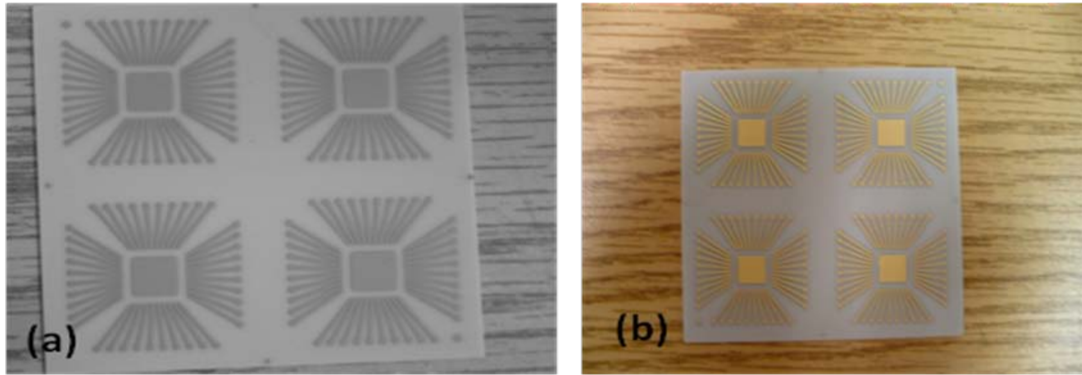
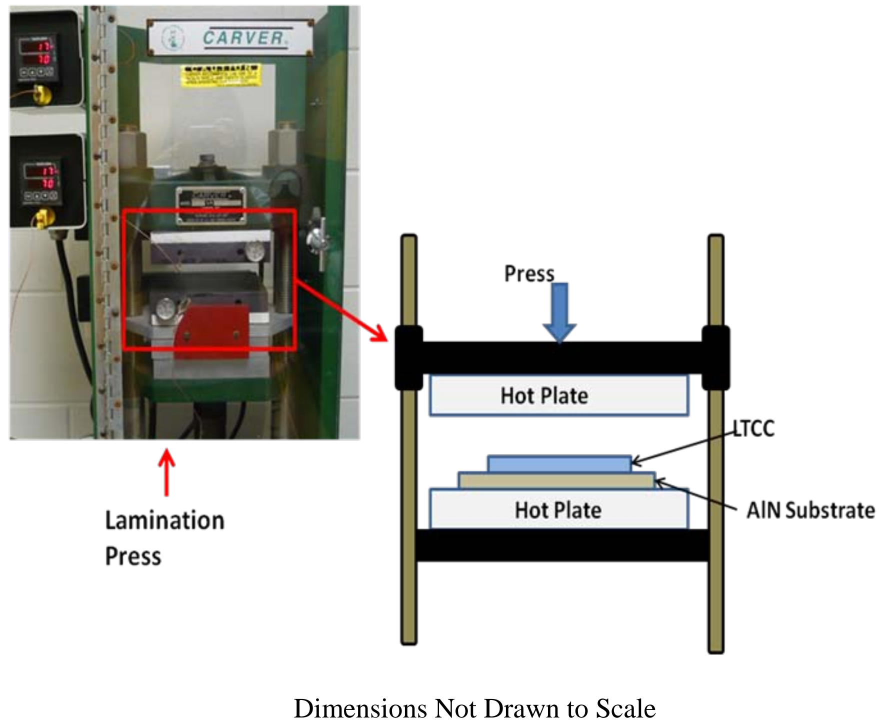



Figure 5.12 (a) AlN substrate metalized with AuPt thick film, (b) AlN with Au thick film over AuPt

(2) LTCC Tape processing:

(i) The LTCC tape (125μm thick CT800 by Heraeus®) was cut with a sharp blade to the desired shape; then align/place the tape onto the metalized AlN substrate. In our project, a heated press (Carver Model 2112, shown in Figure 5.13 ) was use to laminate the LTCC tapes at 3000 psi for at least 10 minutes at temperature of 70$^{o}$C. Figure 5.14 shows the LTCC tape laminated on the metalized AlN substrate before firing.




Dimensions Not Drawn to Scale

Figure 5.13 Figure Scheme of the Lamination Process for the LTCC tape

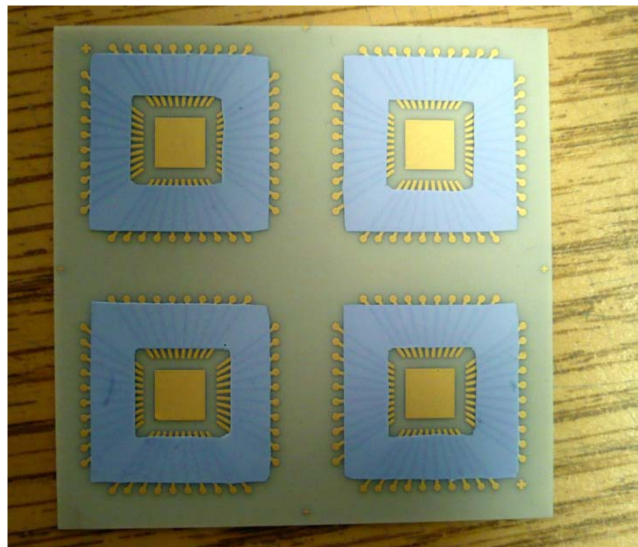


Figure 5.14 LTCC Frame Laminated on Metalized AlN Substrate Before Firing

(ii) After the lamination process, the LTCC tape laminated AlN substrate as shown in Figure 5.14 was fired using an 850$^{\circ}$C peak temperature profile. The firing process was performed in a Fisher-Scientific Isotemp® Programmable furnace

(model 750-126) and the firing profile is shown in Figure 5.15. The detailed heating schedule as programmed in the furnace was:

- From room temperature to 400°C at a ramping rate of 13°C/min
- Kept 400°C for 20 minutes, this 20 minutes soak at 400°C is needed to burn out the organic components in the LTCC tape.
- Ramp from 400°C to 850°C at 7.5°C/min
- Kept at 850°C for 30 minutes
- Turn the furnace off and let it cool to room temperature

Figure 5.16 is a picture of LTCC tape laminated on the metalized AlN substrate after firing process.

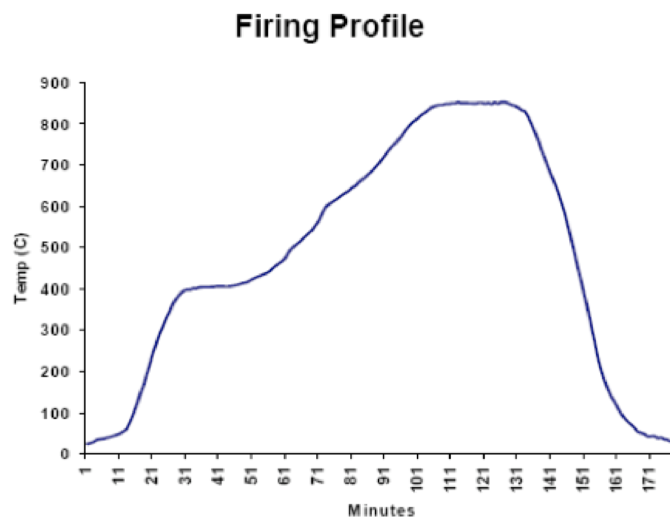



Figure 5.15 LTCC Tape Firing Profile

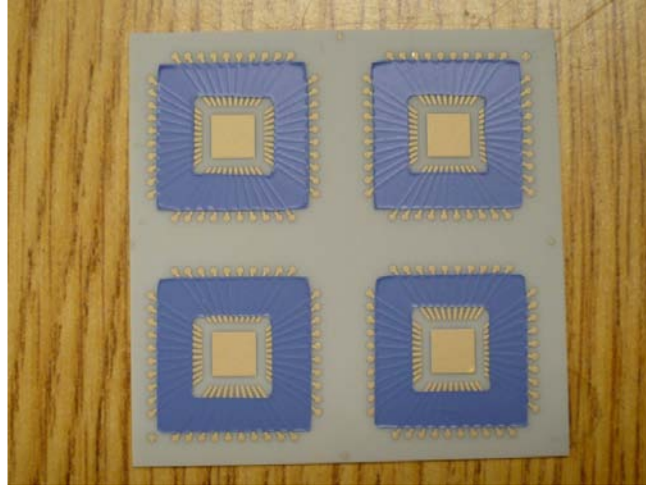


Figure 5.16 LTCC Tape Frame Laminated on Metalized AlN Substrate after firing process

(3) Seal Ring Metalliztion: Au thick film paste (AlN71 purchased from Dupont) was printed onto the laminated/fired LTCC tape, using the same type of screen and the same drying/firing process as was used for AlN substrate metallization. In order to provide enough Au for Au-Sn TLP lid attach, the same process was repeated to form a second layer of thick film Au ring (5063D from Dupont) to increase the seal ring thickness and the final thickness should be ~30-45μm. Figure 5.17 is a picture of the LTCC tape metalized with the Au thick film seal ring.

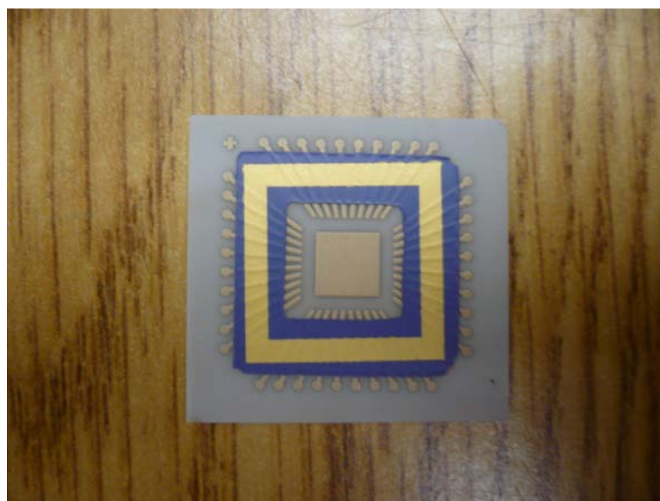


Figure 5.17 AlN Base Package with Au Seal Ring on LTCC Tape

### 5.2.3 Off-Eutectic TLP Lid Attach

The hermetic lid attach process used for AlN integrated package was the same as the lid attach process in section 5.1.3 (process profile shown in Figure 5.7). Eutectic AuSn 80:20 wt% was used as the lid attach material. Prior to the assembly, eutectic Au-Sn (80:20 wt%) performs were pre-attached to lid and package base separately using the preform pre-attach profile shown in Figure 5.5. The Sn-Au-Sn thick foil with same Au-Sn composite (4μm/100μm/4μm) was used as filler that provided excess Au in the TLP lid attach process. A picture of finished package is shown in Figure 5.10.

Unfortunately, the AlN package created using the process described in this section did not pass the gross leak test. A stream of tiny bubbles was observed during the leak testing.

## 5.3 Discussion

It is very important to have a flat/smooth seal ring area in order to ensure a hermetic seal and eliminate possible leak sites. There are a few options to improve the flatness of the seal area on the LTCC tape

(1) As it is shown in Figure 5.18, a thinner thick film pattern can help reduce “ridges” on the AlN substrate and create a smoother laminated LTCC tape surface. To reduce the thickness of the thick film pattern under the LTCC tape, instead of printing both AuPt and Au layers, only one layer of AuPt is needed on the area under the LTCC tape for electrically conductive purposes.

(2) Polish the laminated and fired LTCC tape: Polishing can help create a smoother LTCC tape surface to ensure a flatter Au seal ring for a hermetic lid sealing.

(3) The firing causes the LTCC tape to shrink and produces hard, rigid substrates. Theoretically, there is ~14% shrinkage in the $x$-$y$ plane and ~30% on the $z$ axis. The

curling of the LTCC tape from the shrinkage will also hurt the planarity of the seal ring. So when design the substrate structure, one need to leave enough real estate tolerance for curling of the LTCC tapes.

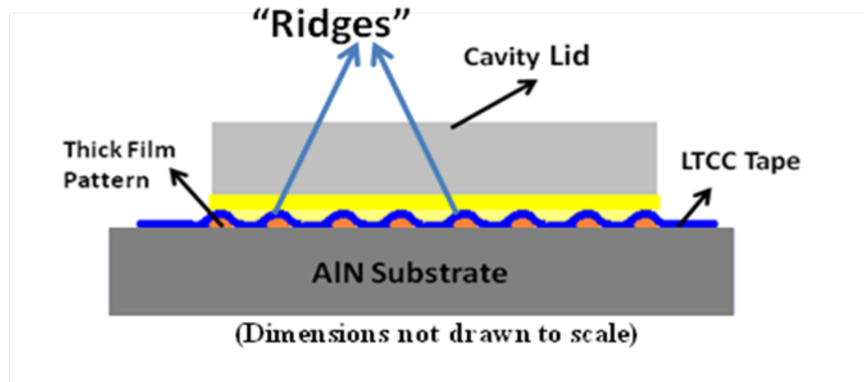



Figure 5.18 Schematic Side-view of AlN Integrated Package

## 5.4 Conclusion

Hermeticity was achieved when the commercial off the shelf (COTS) 40 pin $Al_2O_3$ package was sealed with metalized 96% alumina flat lid, using a two step TLP Au-Sn lid attach process. As for the AlN based hermetic packages, improvements have to be made to ensure the planarity of the seal ring on the laminated LTCC frame.

# CHAPTER 6 CONCLUSIONS AND FUTURE WORK RECOMMENDATION

## 6.1 Packaging for High Temperature SOI Devices

Au-Ge is a feasible die attach material, but the use temperature should be limited to ~300°C, because Au-Si-Ge has a ternary eutectic with a melting point of 326°C. If the Si die is exposed to the Au-Ge at 326°C or above through defects in the barrier layers (Ti/Ti:W in this work), eutectic liquid can form. However, the presence of this Si layer did not result in a significant decrease in mean die shear strength or a decrease in the lower limit of the data range, but the failure mode did change (Figure 3.14) and the upper range of the data decreased.

Control of the Au-Ge die attach process (time and temperature) is also critical. The initial shear results had a range of values. The lower shear strength assemblies were the result of significant dissolution of the thick film Au as the liquid Au-Ge die attach material reached the thick film-to-substrate interface. Tighter process control is required. Electroless Ni/electroless Pd/immersion Au over Al wire bond pads is a viable metallurgy for Au wire bonding for 300°C applications.

## 6.2 Packaging for High Temperature SiC Based Devices

Liquid phase transient bonding with Au-Sn provides a method to achieve die attach for applications up to 500°C. The test results indicate that using a limited volume eutectic Au-Sn preform with excess Au provided by the die or substrate metallization was superior to the thick foil Sn-Au-Sn prefrom. The die shear results for assemblies with limited volume eutectic AuSn are significantly better than for the off-eutectic Sn-Au-Sn preform assemblies. The Sn-Au-Sn

preform relies heavily on solid state diffusion that is slower than the liquid phase diffusion that occurs with the eutectic Au-Sn preform.

## 6.3 Off-Eutectic Sn-Au-Sn TLP Lid Seal Process for Hermetic Packaging

Hermetic package was achieved with commercial off the shelf (COTS) $Al_2O_3$ package and 96% alumina flat lid with Mo-Mn/Ni/Au metallization, using a two step TLP Au-Sn lid attach process : Au-Sn 80/20 wt% preform pre-attach, and thick foil Sn-Au-Sn off eutectic lid attach. The maximum possible calculated Sn weight percentage in the lid attach is 7.5% with the corresponding solidus temperature being ~498°C.

## 6.4 Recommendations for Future Work

Based on the results presented in this dissertation, some recommendations for future work are as follows:

- For SOI die, an alternate backside metallization system should be explored to effectively minimize Si diffusion into the Au-Ge and reduce the Au-Ge-Si eutectic formation.
- For high temperature SiC die attach process, when use thick foil Sn-Au-Sn as TLP die attach material, it is recommended to add the soak time at peak temperature to the brazing profile, which can provide enough time for Sn to diffuse thoroughly into the Au, creating Au-Sn homogeneousness in die attach. Also, a reliable diffusion barrier layer need be explored for Cr layer.
- For LTCC tape lamination process on AlN substrate, it is possible to use polish as the method to create a smooth LTCC tape surface. But the optimization for polishing parameters is required.

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