Flexible, Ultra-Thin, Embedded Die Packaging

by

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Abstract

As thin, flexible electronics solutions become more robust, their integration into everyday life becomes more likely. With possible applications in wearable electronics, biomedical sensors, or ‘peel and stick’ sensors, the reliability of these ultra-thin packages becomes paramount. Likewise, the density achievable with stacked packages benefits greatly from thinner die stacks. To this end, techniques previously developed have demonstrated packages with die thinned to approximately 20µm.

Covered in this work are methods for thinning and packaging silicon die, as well as information on common materials used in these processes. The author's contribution is a fabrication process for embedding ultra-thin (approximately 10µm) silicon die in polyimide substrates. This method is fully illustrated in Chapter 3 and enumerated in the Appendix as a quick reference.

Additionally, thermal cycle testing of passive daisy chain assemblies has shown promising reliability data. Packages were mounted in three alignments: flat, concave, and convex, and placed into thermal shock testing. Finally, the author discusses possible applications for this fabrication process, including the fabrication of multi-chip-modules.

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List of Abbreviations

IC	Integrated Circuit
CMP	Chemical Mechanical Polishing
DI	De-Ionized
RH	Relative Humidity
RIE	Reactive Ion Etching
DRIE	Deep Reactive Ion Etching
STS	Surface Technology Systems
ASE	Advanced Silicon Etcher
AOE	Advanced Oxide Etcher
BCB	Benzo-Cyclo-Butene
CTE	Coefficient of Thermal Expansion
HMDS	Hexamethyldisilazane
BGA	Ball Grid Array
CSP	Chip Scale Package
DIP	Dual Inline Package
PDIP	Plastic Dual Inline Package
TQFP	Thin Quad Flat Pack
TSSOP	Thin Shrink Small Outline Plastic Package
LCP	Liquid Crystal Polymer
PET	Polyethylene Terephthalate
AMNSTC	Alabama Micro/Nano Science and Technology Center

1. Introduction

Thinning of silicon wafers has become common practice in the packaging industry for use in stacked die packages and 3D wafer stacking [1-5]. As such, this technology can be used to build very thin, flexible electronics. When considering flexible electronic assemblies, the weight and density are of great importance. The integration of components directly into the substrate does much for increasing the density of the assembly. Furthermore, reducing the thickness of the embedded components will undoubtedly improve the overall weight of the package.

Applications include electronics that can be bonded to non-flat surfaces to produce conformal electronics or to fabrics to create wearable electronics, 'peel and stick' sensor packages, biomedical sensors and foldable membranes [6-11]. In addition, systems requiring electronics to fit into irregularly shaped cavities would benefit from this technology. Layers of flexible electronics can be stacked and interconnected to produce very thin, 3-D electronics assemblies with embedded active devices. Further decreasing the profile of these thinned circuits enables higher density 3D stack packages.

Current research in the area of flexible electronics has centered around three major assembly techniques, covered in Chapter 2. The fabrication method outlined in Chapter 3 of this work looks to improve upon these techniques, with increased flexibility

and density. The process is essentially comprised of three parts: die thinning, die-substrate attach, and interconnect formation. The test die in this work included a daisy chain pattern, which allows for a test signal to be run off die then back on repeatedly.

Thinning the die occurred in two steps: a chemical mechanical polish to roughly 50µm and a plasma etch to their final thickness around 10µm. A polyimide substrate was chosen for its flexible properties as well as its thermal coefficient close to that of silicon. In order to minimize the weight and thickness of the package, the substrate itself is no more than 12µm on each side of the embedded die. A Cu/Ni/Au metalization was chosen, as the metal layer needed to be solderable. The fabricated packages were put through thermal shock testing at a temperature range of -40°C to +120°C. Using a Weibull plot, thermal reliability for fully assembled packages was calculated to be 4841 cycles.

2. Review of Previous Research

Previous work in this area has focused on three major techniques for the fabrication of thin, flexible packages: thinned die flip-chip solder assembled on polyimide or LCP flex [12-16]; thinned die thermo compression laminated into LCP films [17-20]; thinned die embedded in polyimide flex [20-26]. Work in the area of thinned die in polyimide (PI) substrates has shown great promise with single layer packages including microcontrollers [24] and RF devices [22]. However, these processes have been developed for the packaging of CMP thinned silicon in the 20-50μm range, this work details the use of deep reactive ion etching (DRIE) to package die that are 8-10μm thick. With an eye toward more flexible packages and thinner 3D die stacks, packages have been manufactured with die thinned to approximately 10μm thick [26].

2.1. Wafer and Die Thinning

Development of low profile electronic packages is being motivated by the ongoing miniaturization of electronic products. For obvious reasons, smaller feature size packages and components provide advantages including smaller space requirements, lighter weight, and increased density. Therefore, very thin silicon is attractive for

developing thin IC assemblies. Figure 2.1 illustrates the trend of decreased die thickness in electronic packages [27].

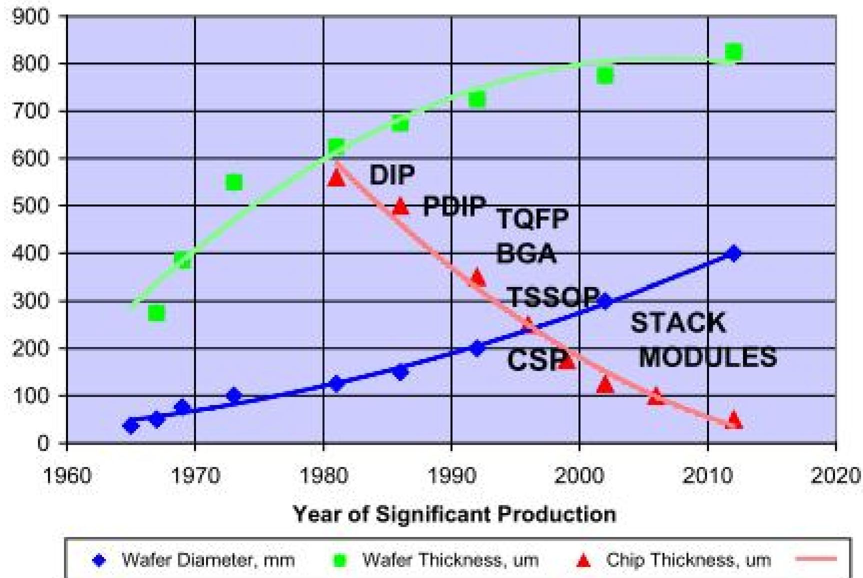

Figure 2.1: Trends for Wafer Thickness, Wafer Diameter and Die Thickness [27]

2.1.1. Backside Grinding

The most common practice for wafer thinning is backside grinding. 150mm wafers typically have variations between 1 and 3µm. During grinding, the wafer backside is abraded mechanically by 3 rotating wheels carrying embedded diamonds. Wafers are cooled by flushing with de-ionized (DI) water. A typical grinding process consists of two steps: rough grinding and subsequent fine grinding. The fast mechanical action causes a harsh removal rate of silicon: resulting in significant sub-surface damage on the wafer.

Common defects are die chipping, cracking, die scratching, die metallization smearing and die corrosion. Additionally, prolonged exposure of water during grinding may lead to copper corrosion. Therefore, the wafer must be protected by tape so that water does not come into contact with the metallization. However, too thick or too thin tape can lead to die metallization smearing. Backside stress can lead to warped silicon substrates and increases the risk of wafer breakage. This problem is overcome by adding a stress relief process after grinding. Suggested techniques are wet-chemical etching, chemical mechanical polishing (CMP) or plasma dry etching. In a CMP process, chemical slurry is used to polish the wafer. Silica based slurry is most common. Dry polishing utilizes the same principal as CMP except the medium is a polishing wheel—made of very fine diamond particles [28-30].

2.1.2. Die Release

Since standard dicing techniques produce a great deal of stress on the sidewalls of the die, dicing thinned silicon presents some major reliability concerns. Therefore, a technique referred to as "dicing by thinning" has become a standard practice in thin silicon technology. In this technique, trenches are diced into the wafer at a depth equal to the final thickness. In doing this, the die are released during the thinning process; thus eliminating a need for dicing the already thinned wafer. This process has several advantages including the parallel release of the die. Additionally, when the die are

released in this manner, the chip corners are slightly rounded, resulting in improved mechanical strength. These trenches can also be realized by patterning the wafer with photoresist and plasma etching, allowing for non-rectangular die layouts. Furthermore, the etching of trenches allows for narrower lanes, greatly increasing wafer chip density for small area die [31].

2.2. Substrate Materials

With substrate thickness below 100µm, conventional substrate materials: ceramics or epoxy-based fiber reinforced laminates are unable to provide the mechanical strength to support these devices. In contrast, polyesters, polyimides and liquid crystal polymers (LCP) maintain a high modulus and a high strength even when very thin. The average properties for these materials are listed in Table 2.1 [32]. However, it should be noted that there are many varieties of each substrate material that have their own distinct advantages and disadvantages.

Table 2.1: Properties of Flex Materials [32]

	Polyester	Polyimide	LCP
Melting point (°C)	243-260	-	277-254
Density (g/cm^3)	1.35-1.40	1.32-1.71	1.49-1.79
Tensile strength, yield (MPa)	$0.38\text{-}0.89 \times 10^2$	$0.32\text{-}0.87 \times 10^2$	$1.48\text{-}2.07 \times 10^2$
Tensile strength, break (MPa)	$0.48\text{-}0.73 \times 10^2$	$0.20\text{-}1.10 \times 10^2$	$0.62\text{-}2.07 \times 10^2$
Elongation, break	85.0-160.0%	0.5-10.0%	1.0-3.0%
Tensile modulus (GPa)	2.75-3.82	1.08-2.55	1.01-2.21
Flexural modulus (GPa)	0.88-1.76	0.59-1.93	0.94-1.60
Compression strength (MPa)	$0.96\text{-}1.26 \times 10^2$	$0.14\text{-}2.42 \times 10^2$	$0.45\text{-}0.80 \times 10^2$
Izod notched, R.T. (kg cm/cm)	1.6-22.7	1.4-19.7	3.8-16.7
Thermal conductivity (W/m-°K)	0.067-0.121	0.22-0.63	0.13-0.45
Linear thermal expansion (cm/cm-°C)	$14\text{-}90 \times 10^{-6}$	$13\text{-}52 \times 10^{-6}$	$2.0\text{-}27 \times 10^{-6}$
Deflection Temp. @ 264 psi (°C)	177-232	238-349	170-349
Continuous service temp. (°C)	166-193	249-288	-
Dielectric strength (V/mm)	$1.5\text{-}2.7 \times 10^4$	$0.8\text{-}2.7 \times 10^4$	$2.2\text{-}3.5 \times 10^4$
Dielectric constant @ 1MHz	2.9-3.2	3.0-5.2	3.1-4.3
Dissipation factor @ 1MHz	0.010-0.020	0.001-0.010	0.020-0.030
Water absorption, 24 hr	0.08-0.15%	0.27-0.97%	0.01-0.10%

Polyesters are thermoplastics made primarily from high molecular weight polyethylene terephthalate (PET) [33]**.** They posses good physical properties for flex such

as a high modulus of elasticity and good tensile strength. Additionally, they are optically transparent and can be a good low-cost solution for many thin-film applications. Unfortunately, they suffer from a relatively low service temperature (Table 2.1), which can pose a problem when package assembly requires eutectic solder. However, they can still be useful when low-temp cure adhesives can be used in place of solder.

Polyimides are found in the majority of flex applications due to their superior physical properties. They have excellent chemical resistance as well as the ability to operate at extremely high and low temperatures. Numerous variations of polyimide are produced for various applications. For example, HD Microsystems PI-2611 is manufactured with low stress, low CTE, high modulus, and high ductility [34]. This type of polyimide is particularly useful because its CTE (~3 ppm/°C) is closely matched to that of silicon (~2.6 ppm/°C), thus mitigating in-plane stress from potential CTE mismatches. The major disadvantage for polyimides comes from its high level of water absorption. It has been found that in humid environments (>80% RH), polyimides will experience high frequency losses, as well as dimensional instability. Therefore, in a majority of high frequency applications, LCP is used [35].

Compared with polyimide films, LCP films have very low moisture absorption (<0.1%) and low permeability to most common gases. Additionally, they have a low loss tangent, high temperature resistance, flame resistance, and good vibration absorption. This makes them an excellent choice for mm-wave applications such as RF cables,

antennas, and optical pickup boards [35]. LCP can be single or double copper clad and can form layers without the need for an adhesive. Like polyimide, its CTE can be controlled to match that of Si, Cu, or GaAs [36].

As demonstrated in the following sections, the assembly of thin and flex packages can be accomplished with solder, compression bonding, or adhesives. Probably the best adhesive for these applications is BCB (Benzo-Cyclo-Butene) from the Dow Chemical Company [37]. BCB is thermosetting, photosensitive, and forms strong bonds at relatively low temperatures, especially when compared to anodic or fusion bonding. BCB is characterized by its ability to cure with little to no solvent evolution. This is important as it mitigates the formation of voids between the die and substrate. Additionally, BCB has a high tolerance to non-uniform substrate surfaces, allowing for seals with feed-through lines. Furthermore, BCB is compatible with high temperature applications [38].

BCB has been used to form hermetic seals for MEMS device packaging, as a low-k dielectric material for multi-level packaging, and as a void-free material for adhesive bonding. Bonding has been accomplished at both the wafer and chip level [39]. BCB is typically cured in two stages: pausing first at a temperature between 125˚C and 150˚C for 10-15 minutes before climbing to the final setting temperature. A hard-cure is generally achieved with a soak at 250˚C for 45 minutes to an hour. The cure process is typically performed under a light load; either in an oven or on a hotplate. More recently, studies have successfully implemented laser-assisted bonding in as little as 10 seconds [38].

2.3. Flip-Chip on LCP or Polyimide Flex

Recent work with thin die flip-chip soldered onto copper-clad LCP or polyimide flex has shown to be highly flexible with excellent reliability [12, 17]. Thinning of the test die is performed on the wafer level. The wafer is temporarily attached on the front side to allow for thinning. Once thinned, the wafer is transferred to a backside support or "handle wafer" for increased stability and ease of handling during the fabrication process. Figure 2.2 [12] shows the curvature of thinned die without any support. Solder bumping was performed after thinning at the wafer level. This involved sputtering Cu/Cr before the thinning process, then patterning and electroplating eutectic Sn/Pb onto the die pads. The wafer was reflowed before the resist was stripped and then the wafer was diced into test die. The handle attached to each die allowed the thin chips to be processed with standard techniques and no further special processes, aside from the removal of the handle which was accomplished by soaking the device in acetone.

In this case, the flex substrate was 50μm Dupont Pyralux AP—a copper clad polyimide laminate. The copper was patterned, etched, and then electroless Ni plated to 4μm. A protective immersion Au layer of 0.25μm was also applied. Since the substrate itself was so thin, the flip-chip reflow process would cause the substrate to buckle. To correct this, a vacuum fixture with a flexible membrane was developed to hold the package in place during reflow. Reliability tests were performed with and without underfill, with the underfilled packages performing much better than their counterparts.

Due to the nature of the underfill, the handle die had to be removed prior to its application, since the underfill would creep around the sides of the die and make removal of the handle impossible [12]. Similar techniques have been demonstrated with additional substrate materials [17, 18].

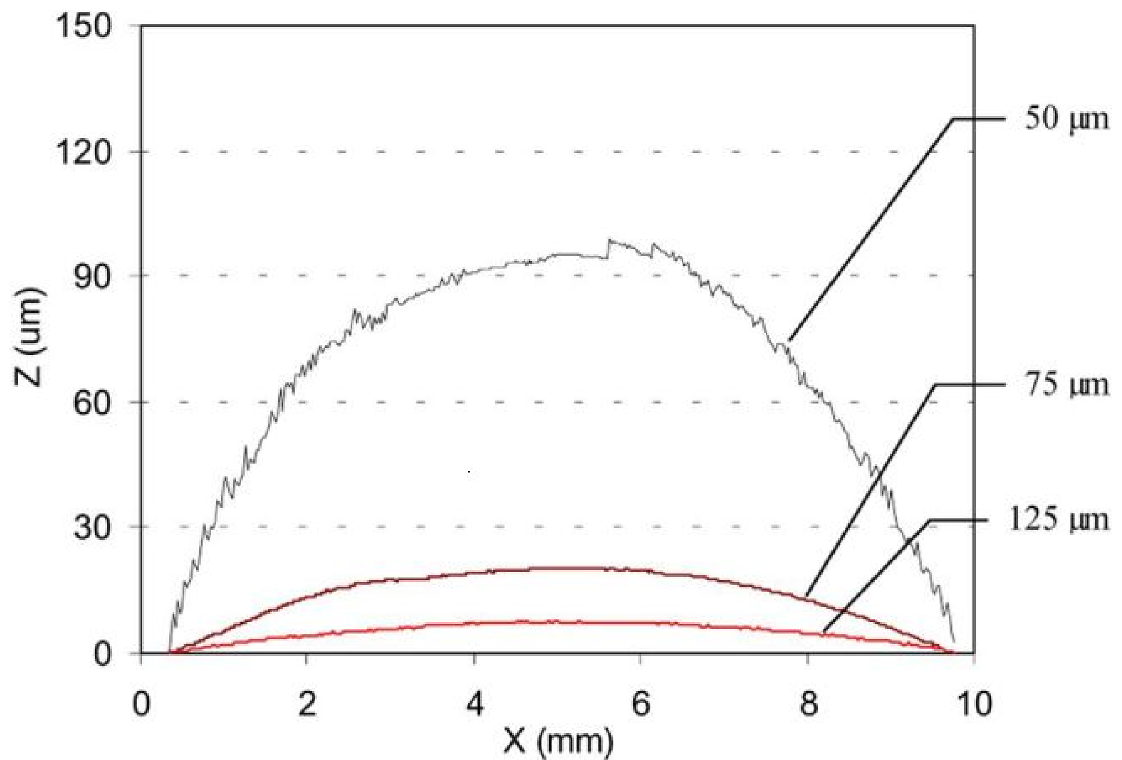

Figure 2.2: Thinned Die Curvature without Handle [12]

2.4. Thin Die Thermocompression Laminated on LCP Flex

Another technique for ultrathin package assembly is gold/gold thermo-compression bonding. This technique is similar to the one presented in Chapter 2.3, except that instead of reflow soldering the die to the substrate, the die are bonded with gold bumps through heat and pressure (Figure 2.3). Like the previous example, the thinned die require a handle for ease in handling and bonding. The LCP substrate utilized thicker gold layers as well (~2μm) in order to facilitate the Au/Au bonding. Also, like the previous technique, this flip-chip assembly process has shown good reliability data [17].

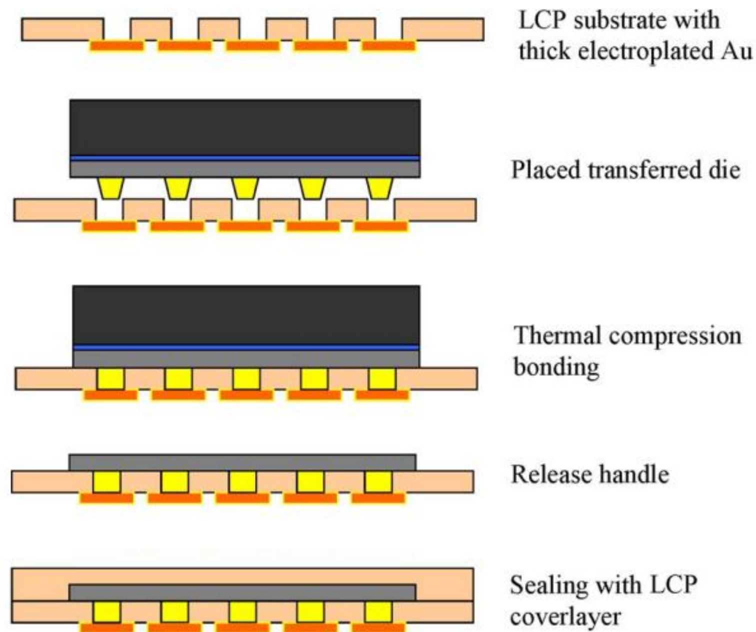

Figure 2.3: Thermocompression Process Flow [17]

2.5. Thin Die Embedded in Polyimide

The process of embedding a thin die into a polyimide substrate involves spinning layers of polyimide beneath and on top of a thinned die. Therefore, the thinned die must be bonded to the polyimide substrate through some form of adhesive. This has been attempted with various adhesives, including different polyimides [18, 21], but BCB (Chapter 2.2) appears to be the best material for silicon / polyimide bonding.

One such process involves spinning polyimide onto a glass substrate to form the base of the substrate. This is followed by the spinning on of a photo-imageable polyimide that is masked to create a cavity equal to the thickness of the die for the die to sit in. A tiny amount of BCB is then pipetted into the cavity and the die placed inside. Once cured, the entire package should be planar and is closed over with another layer of the initial polyimide. Contact holes are laser etched into the package allowing for the metalization of traces and contacts. The entire package is then released from the glass wafer [24].

This technique has been used to successfully fabricate packages utilizing die thinned to 20µm. Active devices such as microcontrollers and RF devices have been successfully integrated into flex substrates in this manner [22, 23]. Additionally, this process has been utilized to manufacture multi-chip modules [24]. Unfortunately, at this time, there appears to be no published reliability test data utilizing this particular fabrication method.

2.6. Author's Current Research Summary

Building on some of the concepts for embedded die packaging, the author has developed and tested a method for thinned die integration into thin-film polyimide. Previous works have shown promise in utilizing die thinned to as low as 8-10µm [18, 20, 26]. Additionally, this technique has been used to develop multi-chip modules both 2D and 3D in design. While initial thermal testing exposed some issues with the design, this work presents an improved fabrication process, as well as improved reliability data.

3. Fabrication Method

This chapter outlines the fabrication technique for ultra-thin die packaging. The entire process flow is outlined in Appendix A.

3.1. Die Thinning

In order to create extremely thin embedded die packages, the die themselves must be thinned as much as possible. A final die thickness of 10µm was chosen as it is thin enough for silicon to be flexible, and thick enough to support standard fabrication techniques. Wafers are pre-sawn to a depth of 75µm and then chemical-mechanically thinned to 50µm, resulting in individual die. The die are mounted face down onto handle die (500µm thick Si die diced to approximately the dimensions of the thinned die) using a thin adhesive layer. Using deep reactive ion etching, the 50µm die are then further thinned to 8-10µm. The handle die keeps the thinned die planar, protects the face during processing, and aids in handling.

3.1.1. Test Die

The Delphi Electronics PB (Perimeter Bump or Bond) series of test die (See Figure 3.1, Figure 3.2) is designed to simulate the I/O of CMOS-like devices at various pad pitches. These test vehicles form the basis of a useful die standard for the evaluation of flip chip applications as a function of various bump, materials, or assembly variables. The PB6 test chip is designed with I/O pads on 6 mil (152µm) pitch located on the peripheral of the die. The 0.2-inch by 0.2-inch PB6 die contains 112 pads giving 56 daisy chain pairs.

The PB6 wafers were 5-inches (125mm) in diameter and approximately 600µm thick. Each pad area was composed of Al/Cu/Si (98/1/1) with a thickness of 8900 angstroms. The wafer's nitride passivation was 8000 angstroms thick. Passivation openings were 105-µm square.

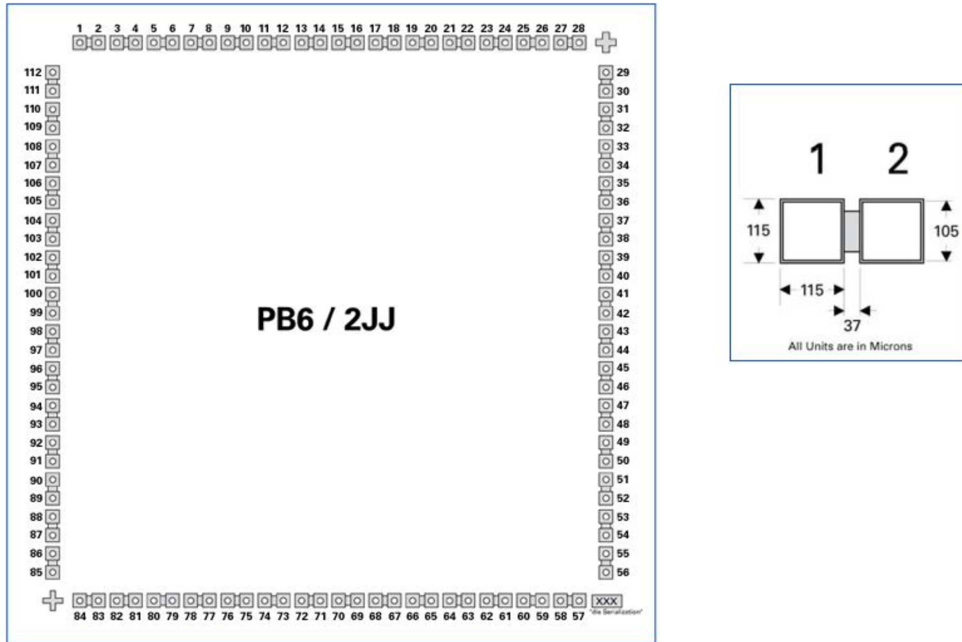

Figure 3.1: Schematic of Delphi Electronics PB6 Test Die [40]

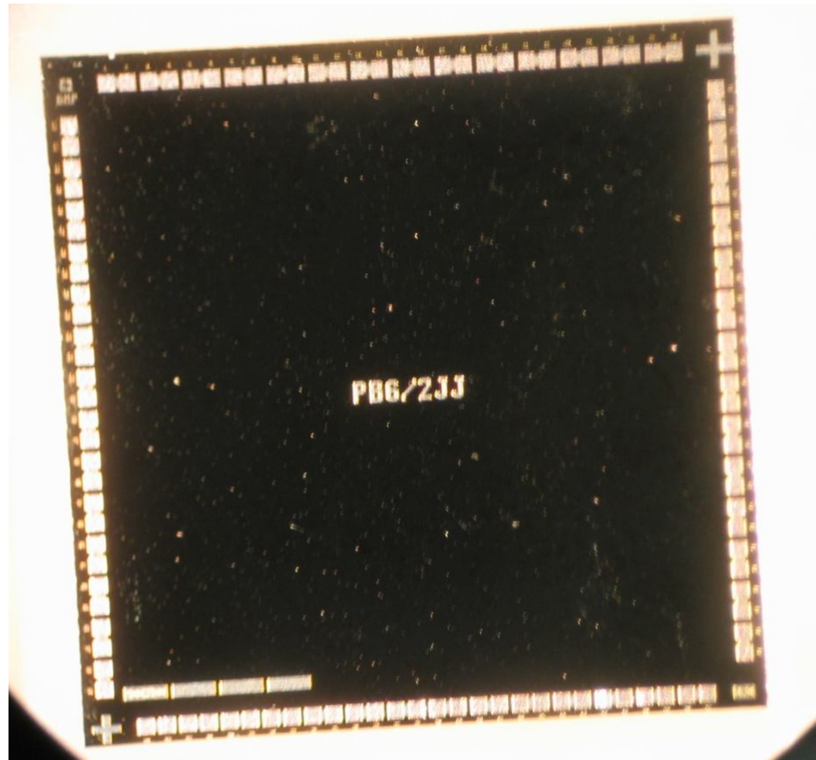

Figure 3.2: Photo of Delphi Electronics PB6 Test Die

3.1.2. Wafer Level Thinning

The first step in the fabrication process was to thin the wafer of PB6 die to individual 50µm thick individual die. Chemical-mechanical polishing (CMP) can be used to thin a wafer to 50µm. Since standard dicing techniques produce a great deal of stress on the sidewalls of the die, dicing thinned silicon presents some major reliability concerns (See Chapter 2.1 for more details). Therefore, a process was used that singulated the die during the thinning process. This process is illustrated in Figure 3.3. To

accomplish the die singulation, a 75-100μm deep trench was sawn into dicing streets around the die on the front side of the to-be-thinned wafer. The wafer was then sent to Aptek Industries [49] for standard chemical-mechanical polishing. At Aptek, the wafer was mounted on a grinding fixture with a temporary adhesive. Sequential grinding was used to remove the bulk silicon and to polish the backside of the die. When the thickness of the thinned die was less than the depth of the trenches, the trench grids were exposed and the thinned wafer was automatically turned into an array of thinned die. The thinning process continued until the thickness reached the target value of 50μm. After completion of the thinning process, the thinned die were released from the grinding fixture by dissolving the adhesive. The process had high yield with no damage to the die edges. The thinned die were then returned in waffle packs (Figure 3.4).

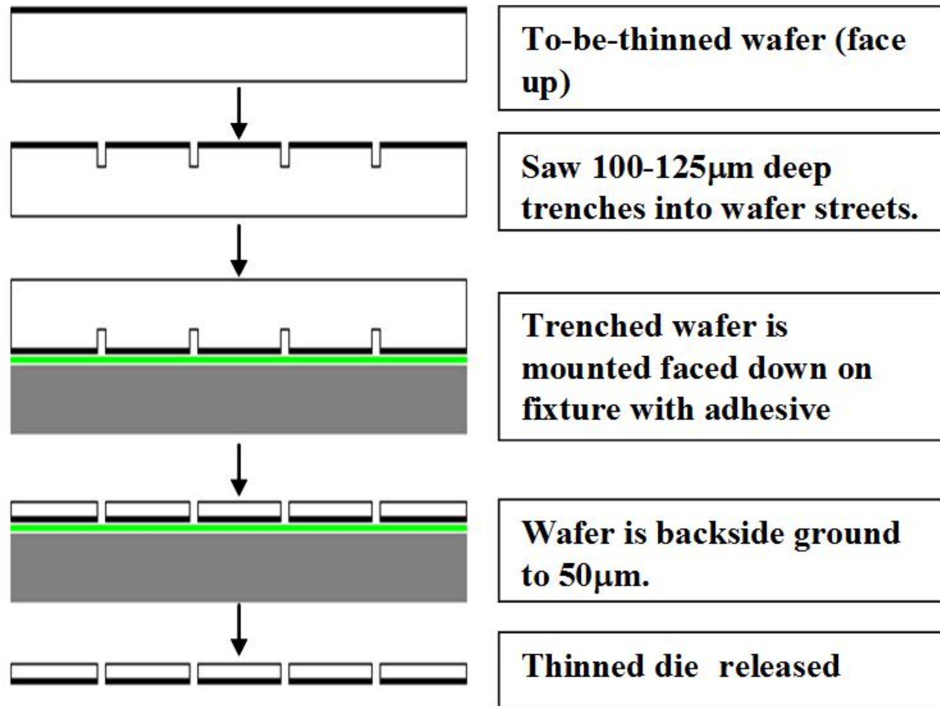

Figure 3.3: Flowchart of the Wafer Thinning Process [26]

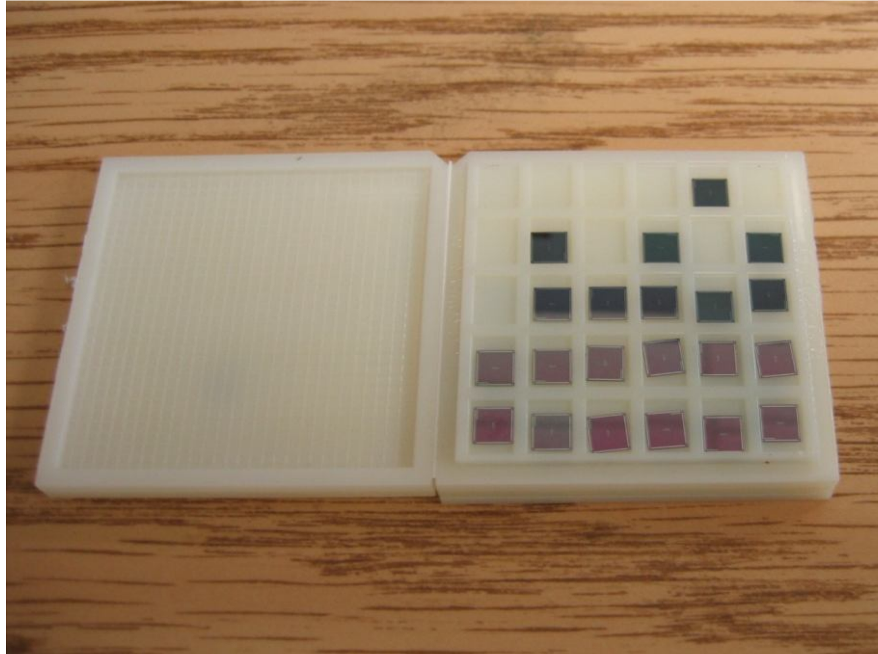

Figure 3.4: Thinned Die Returned from Aptek in Waffle Packs

3.1.3. Individual Die Thinning

Since the fabrication process utilizes silicon die thinned below 10µm, special precautions were made for handling the thinned die. In order to reduce damage from handling the ultra-thin die, each 50µm thick die was individually bonded to a "handle" die during the substrate fabrication process. Furthermore, the 50µm die were handled using a handheld vacuum tool to prevent chipping of the edges during processing.

The handle die were produced using a standard 100mm diameter, 500 µm thick silicon wafer polished on one side. For the adhesive, Humiseal 1B31 [41]; a fast air

drying, single component, acrylic coating was chosen. After spincoating the unpolished side of a silicon wafer, the Humiseal was cured in a 90˚C oven for 2 hours then diced into die approximately 0.05mm smaller than their PB6 counterparts. This size reduction was performed to mitigate an issue in the thinning process where excess adhesive would creep up the sides of the PB6 die, resulting in the formation of an un-etched "ridgeline" on the thinned die. Reducing the size of the handle die helped to keep the adhesive on the front side of the die, alleviating this issue. Once diced, the handle die were dehydrated in a vacuum oven for 2 hours at 120˚C.

Several Methods were used to bond the handle die to the 50µm thick PB6 die. The best results were produced using a KarlSuss FC150 Automated Device Bonder. The thinned die and handle were aligned face to face with the aid of the built in microscope. The process involved the heating of both die to 160˚C while squeezing with 200g of force for 90 seconds. The stack was cooled under pressure for an additional 90 seconds (Figure 3.5). While previous experiments required an additional 2 hour bake, this process was found to have sufficient planarity across the die stack [26]. This was most likely due to the KarlSuss having active cooling, which allowed the Humiseal to re-set while still under the load force.

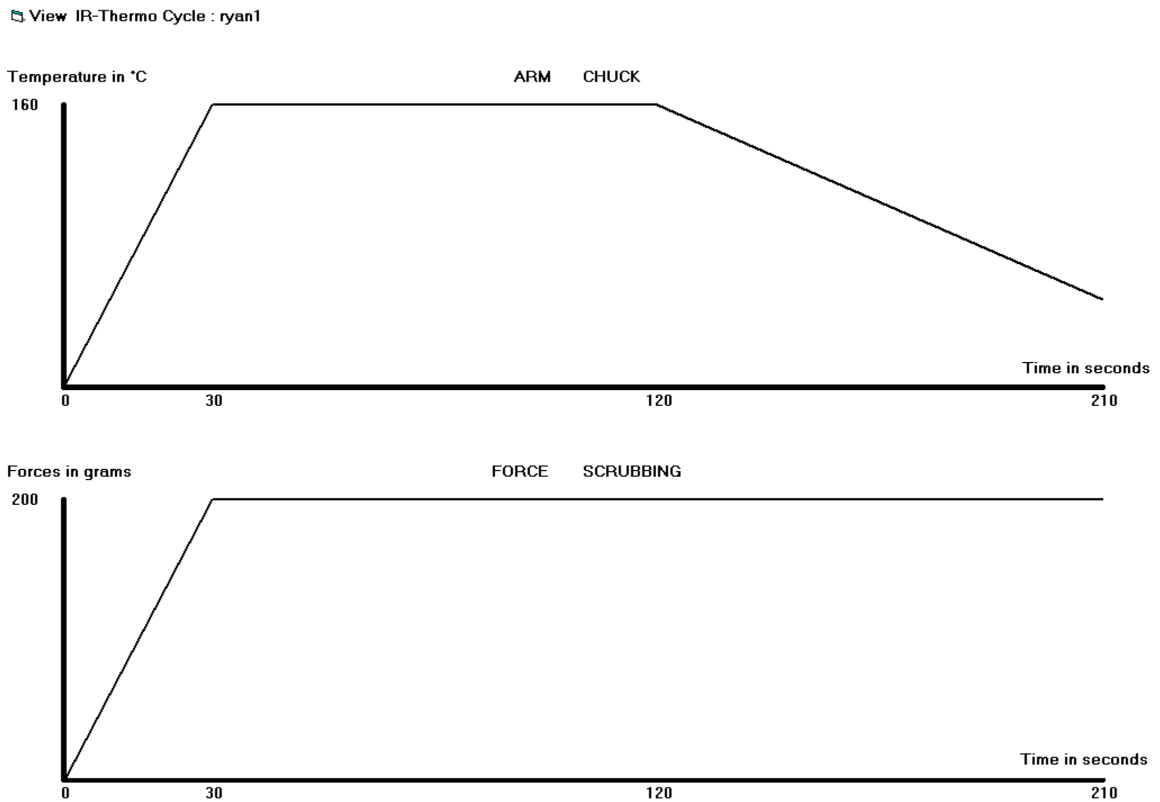

Figure 3.5: Die to Handle Bond Program

Once individual 50µm thick PB6 die were thoroughly bonded to handle die (Figure 3.6), they were mounted and cleaned in preparation for their final thinning. Using Dynatex International Wafer Grip [42], the die stacks were adhered to an oxidized Si wafer, handle die down. The backsides of the exposed PB6 die were then cleaned with acetone, methanol, and DI water. Following this step, the wafer was placed into a Matrix oxygen plasma asher for 30 seconds at 300W power. This step was important in ensuring

that the die thinned planar: as it was discovered that occasionally there would be residue from the Aptek thinning process or Humiseal on the backside of the die.

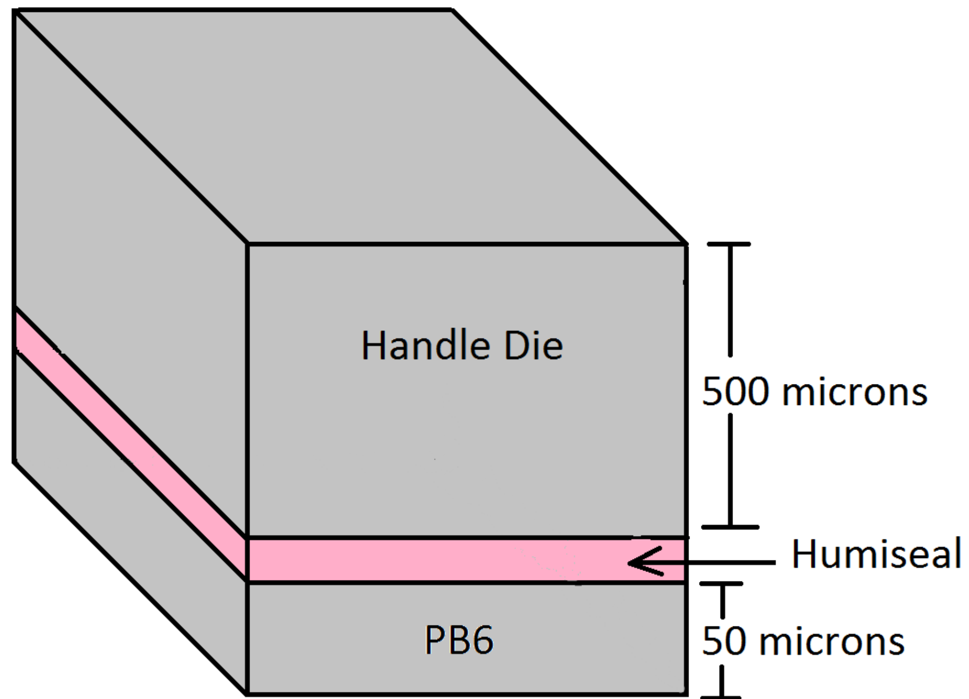

Figure 3.6: Bonded Die Stack

Once bonded to their handle die and cleaned, the 50μm thick die were thinned to their final thickness with Deep Reactive ion Etching (DRIE). A Surface Technology Systems (STS) Advanced Silicon Etcher (ASE) was used to plasma etch the PB6 die,

four at a time, from 50μm to their final thicknesses. The plasma was a mixture of SF_6 and O_2 with a C_4F_8 passivation step. The process is detailed in Table 3.1.

Table 3.1: Die Thinning Plasma Recipe (Represents on Full Cycle)

Step	**Time (sec)**	**O_2 Flow (sccm)**	**SF_6 Flow (sccm)**	C_4F_8 **Flow (sccm)**	**RF Power (watts)**	**Platen Power (watts)**
Etch	20	13	130	0	600	12
Passivate	7	0	0	85	600	0

The thinning process was characterized by etching the die in 5-10 cycle segments. After each run a drop gauge was used to measure the thickness of the die stack. Once the optimal number of cycles was determined, the process was reduced to a single run in the etcher. Due to variations in the cleanliness of the etcher, the total etch time varied between 20 and 21 cycles. Only after a thinned die was attached to the substrate and the handle removed could a profilometer be used to verify the thickness of the die.

3.1.4. Die Thinning and Handling Issues

As mentioned in Chapter 3.1.3, care was taken when processing the chips to prevent an issue where the backside of the etched die would have unetched ridges. A photograph of a ridgeline in the surface of a PB6 die is presented in Figure 3.7. The ridges varied from 6-12μm in height, an indication that some substance was concealing the etch area; thus causing an uneven etch.

The ridgline formation was directly linked to the cleanliness of the exposed backside of the PB6 die. By reducing the size of the handle die, Humiseal creep to the etch surface was mitigated. Furthermore, the O_2 plasma clean was able to remove any trace from the Aptek process, as well as any Humiseal that may have managed to reach the backside.

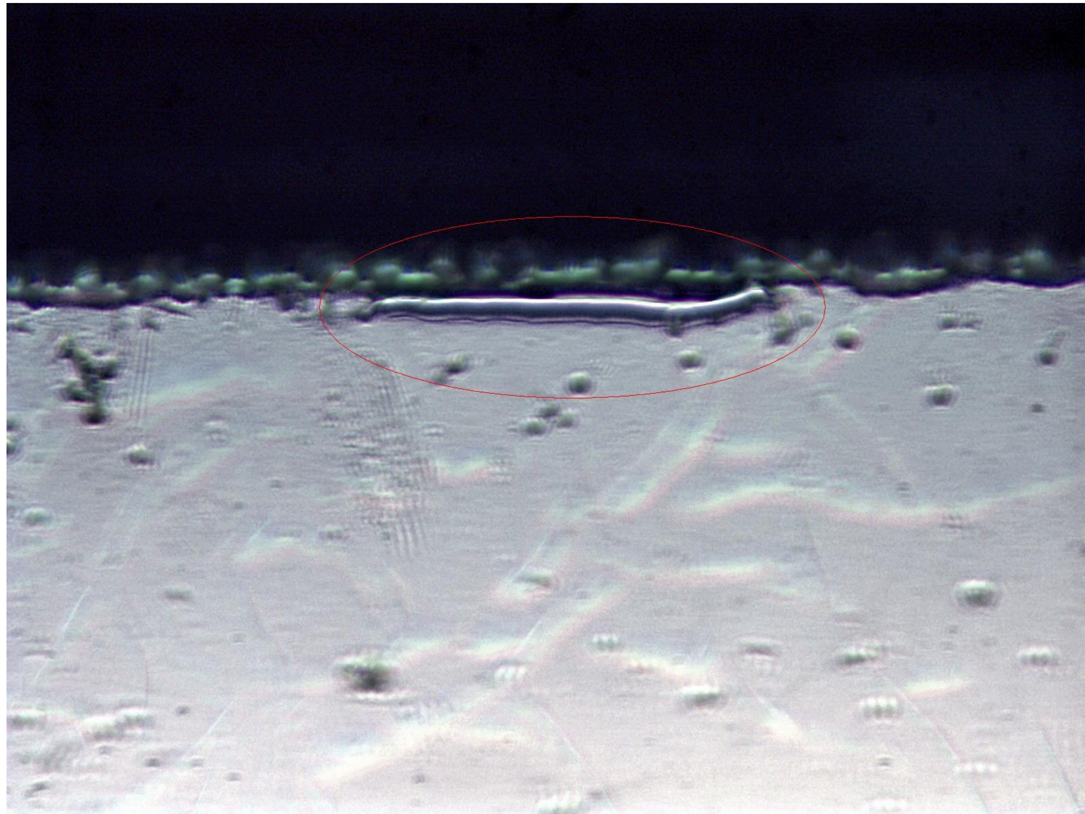

Figure 3.7: Ridge Formation on the Etched Die

3.2. Substrate Fabrication

Polyimide layers have been utilized in the realization of complex 3-D interconnect layers because the material can be deposited as thin insulating layers; it can be micromachined to realize very small vias; it adheres well to Si, deposited metal traces and previously deposited polyimide layers; and it has a high moisture resistance [43]. PI-

2611 polyimide was selected as the substrate material for this application due to its CTE match with silicon.

3.2.1. Polyimide Processing

The polyimide substrates in which the thinned die were embedded were fabricated on bare polished silicon wafers. In order for the process to be successful, the embedded die must release from the bare wafer after processing. Since polyimide does not adhere well to bare silicon, Dow Chemical AP3000 adhesion promoter [44] was only applied to the periphery of the wafer top side (Figure 3.8). To accomplish this, the substrate was spun at 500 rpm for 5 seconds while the AP3000 was poured onto the edge of the wafer. The rotation was then accelerated to 3000 rpm for 20 seconds. Then the wafer was soft-baked for 60 seconds at 120˚C. Once the adhesion promoter was in place, a layer of PI-2611 polyimide was spun on top of the wafer at 500 rpm for 10 seconds and 3000 rpm for 30 seconds [34]. Since PI-2611 is extremely viscous, the slower spin allowed for a more even distribution of the material. Additionally, a hand pipette was used to remove any bubbles from the polyimide before spinning. The wafer was then placed into a 120˚C oven for a 5 minute hard-bake prior to curing at 350˚C over a period of 9 hours. See Figure 3.9 for the complete curing information. Typically, the cured polyimide had a thickness of 5.5 to 6μm (Figure 3.10).

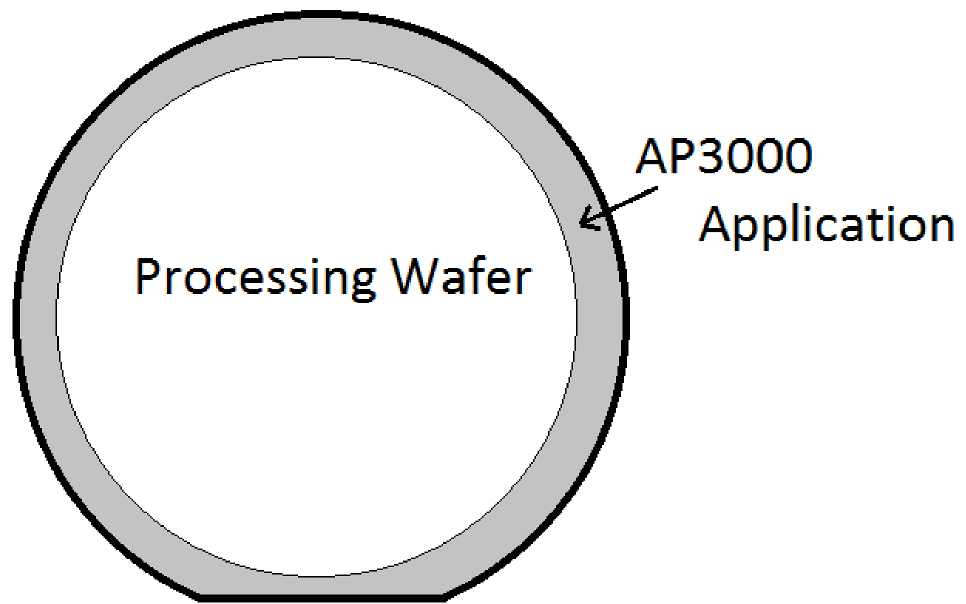

Figure 3.8: Attachment of Substrate to Processing Wafer

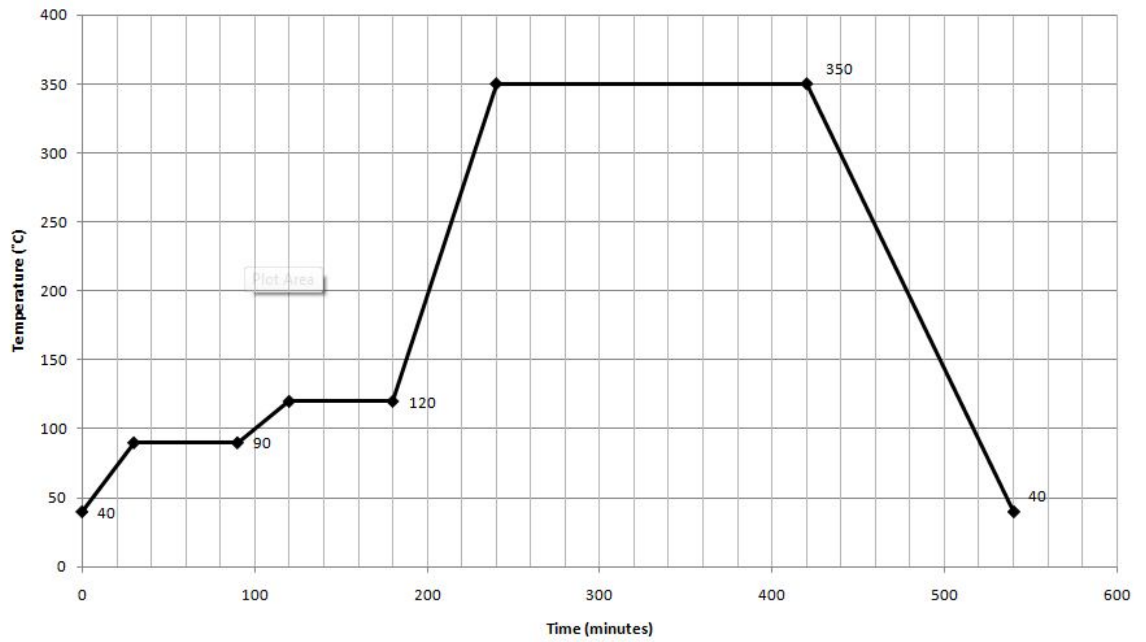

Figure 3.9: PI-2611 Hard-Cure Procedure

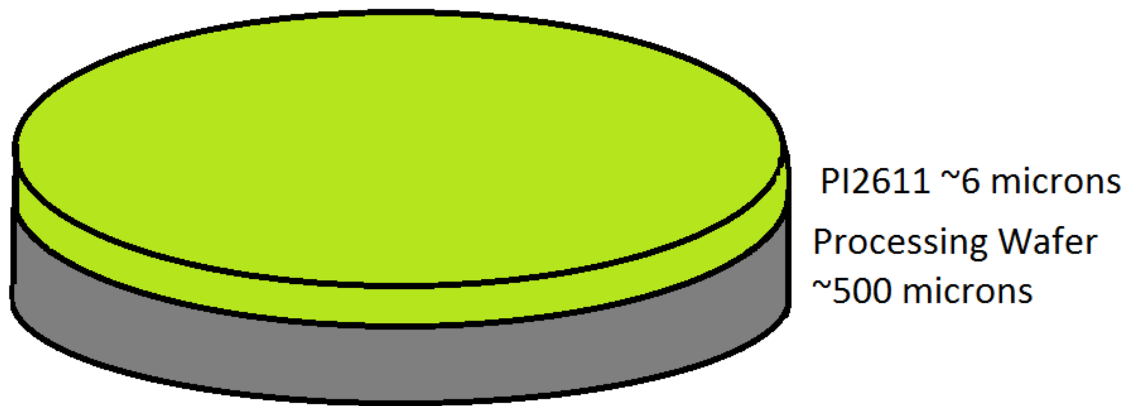

Figure 3.10: PI 2611 Substrate

3.2.2. Die Attach

The next challenge of the substrate fabrication process came in the selection of a proper material to adhere the fully thinned die to the polyimide. This adhesive layer had to be extremely thin, flexible, void free, and for the purpose of 3D stacked components, easily etched. For these reasons, Cyclotene 4024-40 Advanced Electronics Resin, a Benzocyclobutene (BCB), was chosen for the adhesive. This variety of BCB had the added advantage of being photo imageable: which may be beneficial for future applications. Although the BCB was excellent in achieving a void-free bond, its one drawback was its CTE mismatch with the other materials in the package. See Table 2.1 for more information.

Due to the fact that polyimide retains moisture, the substrate was baked in a vacuum oven for 2 hours at 200˚C. Completely dehydrating the polyimide substrate ensured that moisture would not escape during the BCB cure process, creating unwanted bubbles. Additionally, the wafer was placed in a Matrix oxygen plasma asher for 1-minute at 300W in order to roughen the polyimide surface. This step improved adhesion to the BCB and other polyimide layers, and prevented delamination issues. To further increase adhesion, AP3000 was spun on to the entire surface of the wafer at 3000 rpm for 20 seconds and soft-baked at 120˚C for 60 seconds.

Once properly prepared, the BCB was then spun onto the wafer at 500 rpm for 10 seconds, 3000 rpm for 30 seconds and then soft-baked at 90˚C for 90 seconds. A flood

exposure of UV light was then performed to fully crosslink the BCB. At this speed, the resulting BCB layers are approximately 3μm thick [37]. The thinned die, still attached to the handle die, were then placed onto the BCB layer and cured to the substrate using the standard "Hard Cure" outlined in Cyclotene's 4000 Series Processing Procedure [37]. The curing process was performed under a light load in an inert oven with a peak temperature of 250˚C (Figure 3.11). For a load, 30g brass plugs were used (Figure 3.12). The applied bonding pressure is important, as it decreases the amount of voids. However, too much bonding pressure can cause gaps from flatness nonuniformities [52]. Once the cure was completed, the die stacks were thoroughly bonded to the polyimide surface (Figure 3.13).

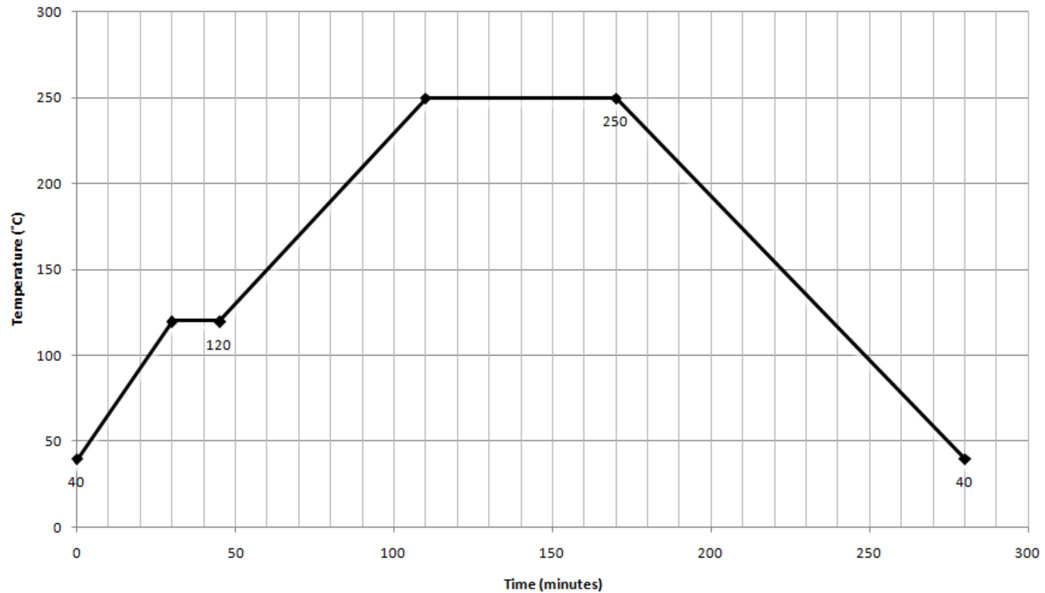

Figure 3.11: BCB Hard-Cure Procedure

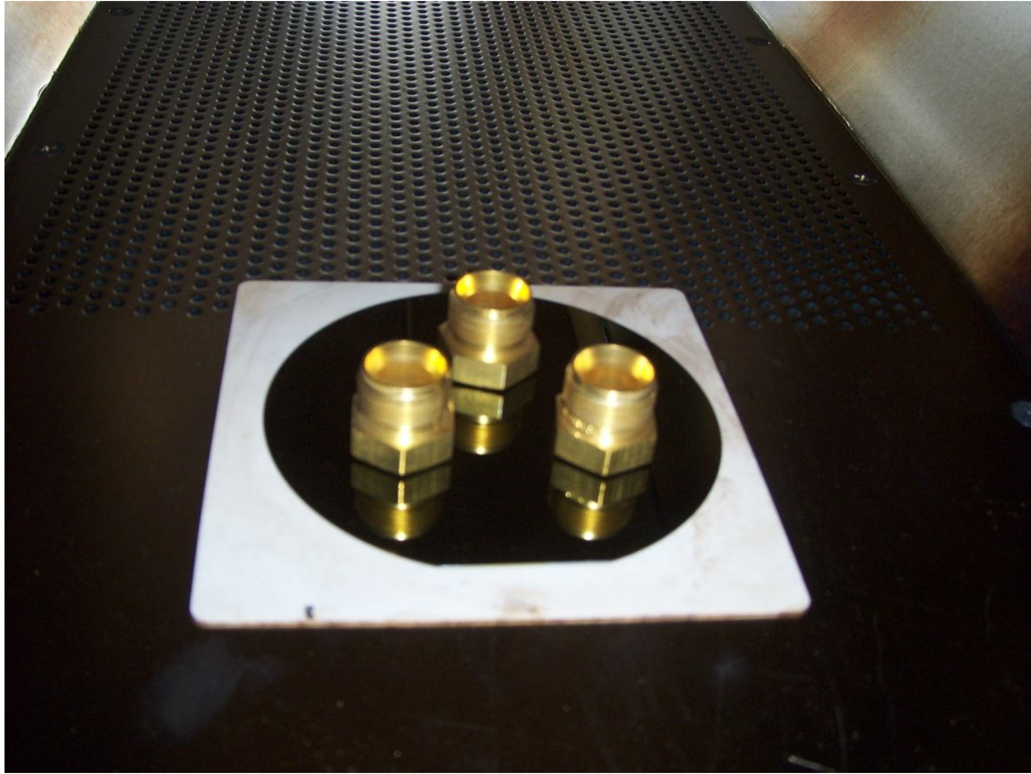

Figure 3.12: Wafer Ready for BCB Cure

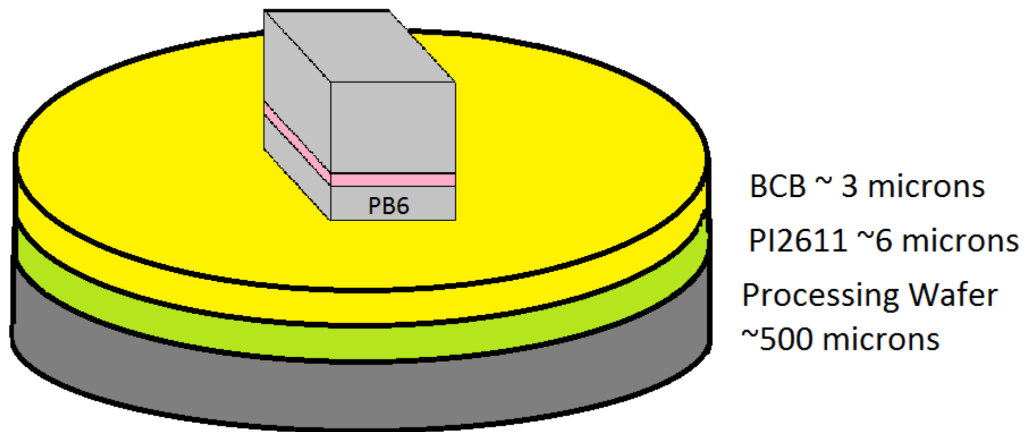

Figure 3.13: Thinned Die Stack Cured to Substrate

3.2.3. Handle Die Removal

With the thinned die successfully mounted to the substrate, the handle die had to be removed from the thinned PB6 die. The die stack adhesive was thermoplastic and softened when returned to a high temperature. Therefore heating the wafer to 145˚C for 5 minutes allowed the handle die to be sheared off the PB6 die (Figure 3.14). This was performed on a hotplate: allowing the Humiseal to soften and then carefully sliding the handle die off of the thinned die with a pair of tweezers. Once the handle die was removed, acetone was used to remove all remaining adhesive from the exposed surface of the PB6 die, and the substrate was again dehydrated.

3.2.4. Second PI Layer

AP3000 adhesion promoter was used to coat the topside of the thinned die and the exposed BCB before the second layer of polyimide was spun on (Figure 3.15). Again, PI-2611 was used for this layer in order to achieve a layer thickness of approximately 6μm. After another soft-bake, curing was performed with the same process as previously described.

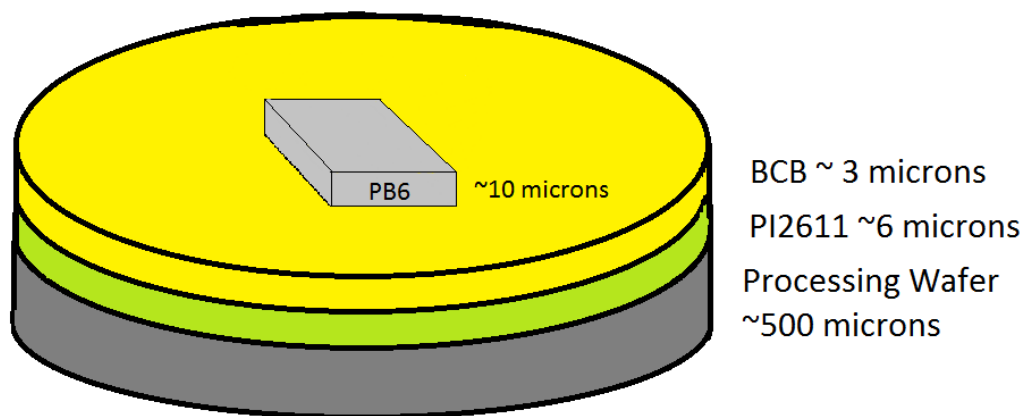

Figure 3.14: Released Thinned PB6 on Substrate

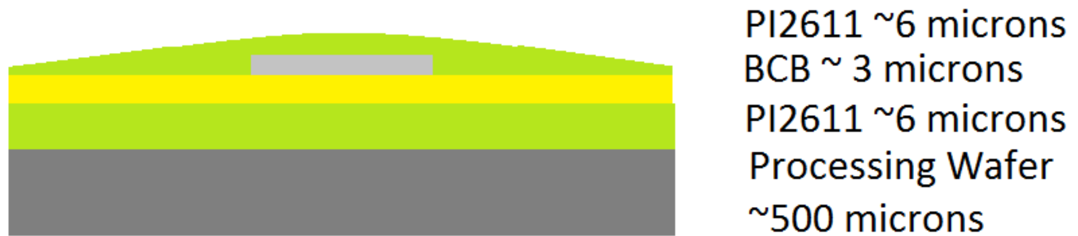

Figure 3.15: Fully Encapsulated Thinned Die

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3.2.5. Substrate Issues

Throughout the development of the fabrication process, several issues were encountered concerning the substrate and die attach. These issues and their solutions are described below.

The first issue came in the selection of the right adhesive material for die attach. The most important property of the material selected was its ability to cure void free. Different forms of polyimide were tried, including PI-2611 and PI-2556 (See Chapter 2.2 for details). Unfortunately, both of these polyimides evolved significant solvents during the curing process, which made their reliability concerns unacceptable (Figure 3.16). Eventually BCB was chosen, however it too was not without incident. Because of the polyimide's inclination to absorb moisture, anything less than the full dehydration of the

substrate before the BCB application would result in significant bubbling under the die (Figure 3.17).

Additionally there was the issue of polyimide-polyimide adhesion. Because polyimide cures so smooth it often has difficulty adhering to other materials, including itself. This can manifest itself as a delamination event, either in subsequent processing steps or during thermal testing (Figure 3.18). To mitigate this issue, nitrogen plasma (Table 3.2) was used to roughen the surface of the polyimide, greatly increasing adhesion.

Lastly, while it has been recommended to cure the BCB at the same temperature as the polyimide to prevent issues during the second polyimide cure [24], this was shown to be problematic with this particular process flow. This is due to the fact that the Humiseal used to hold the handle and test die together would overheat and burn at 350˚C: this was not an issue at 250˚C. Therefore, the BCB cure temperature was kept at 250˚C. While there were two subsequent polyimide cures performed at a peak temperature of 350˚C, no problems have been experienced from not heating the wafer to this temperature during the die attach.

Table 3.2: Nitrogen Plasma Recipe

Step	Time (sec)	Base Pressure (mTorr)	N_2 Flow (sccm)	RF Power (watts)	Platen Power (watts)
Etch	60	10	40	600	100

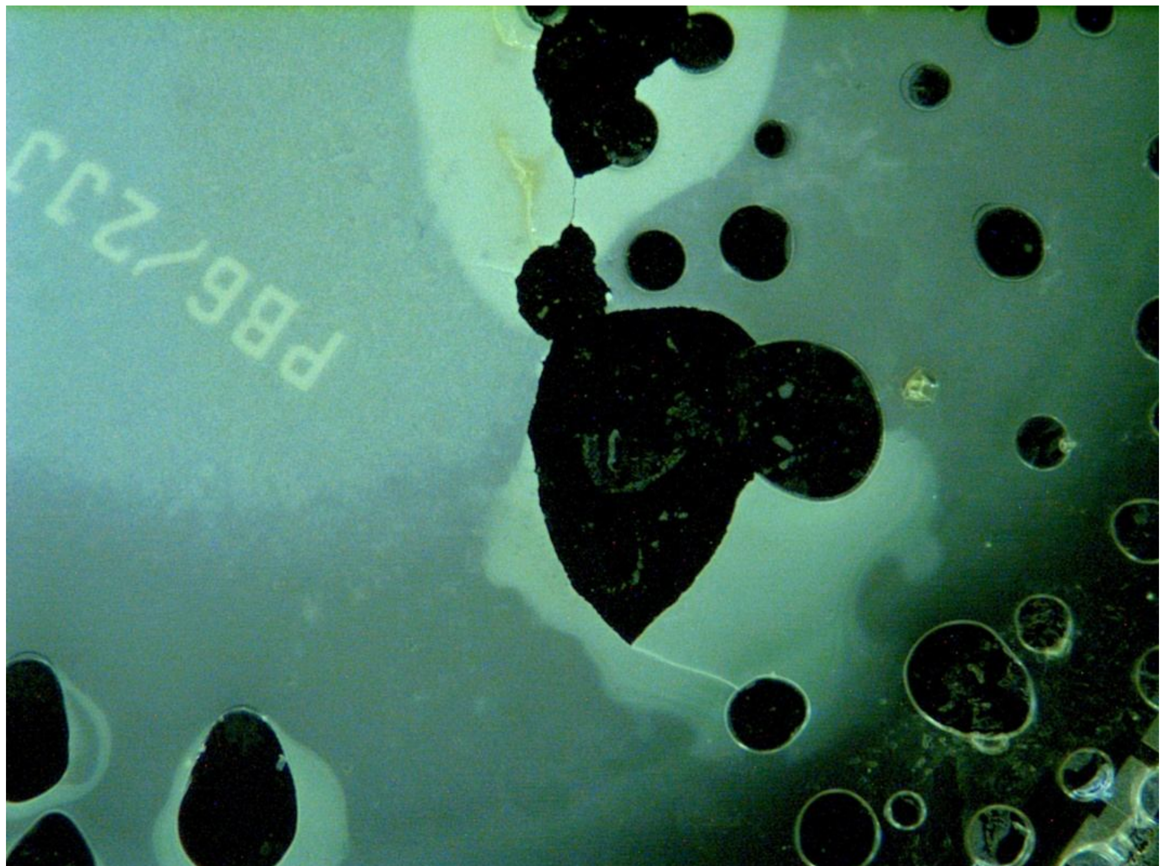

Figure 3.16: Pockets of Voiding Between the Die and Polyimide Substrate

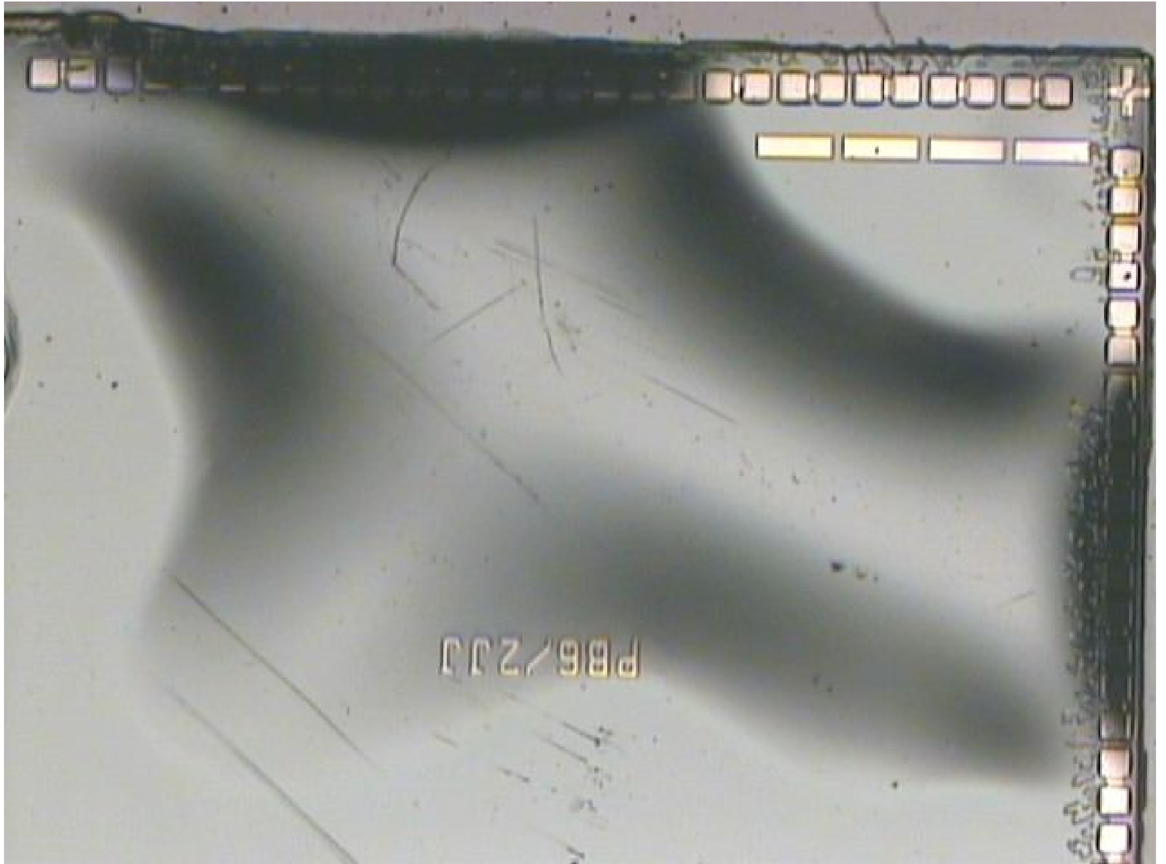

Figure 3.17: Bubbling Beneath the Attached Die

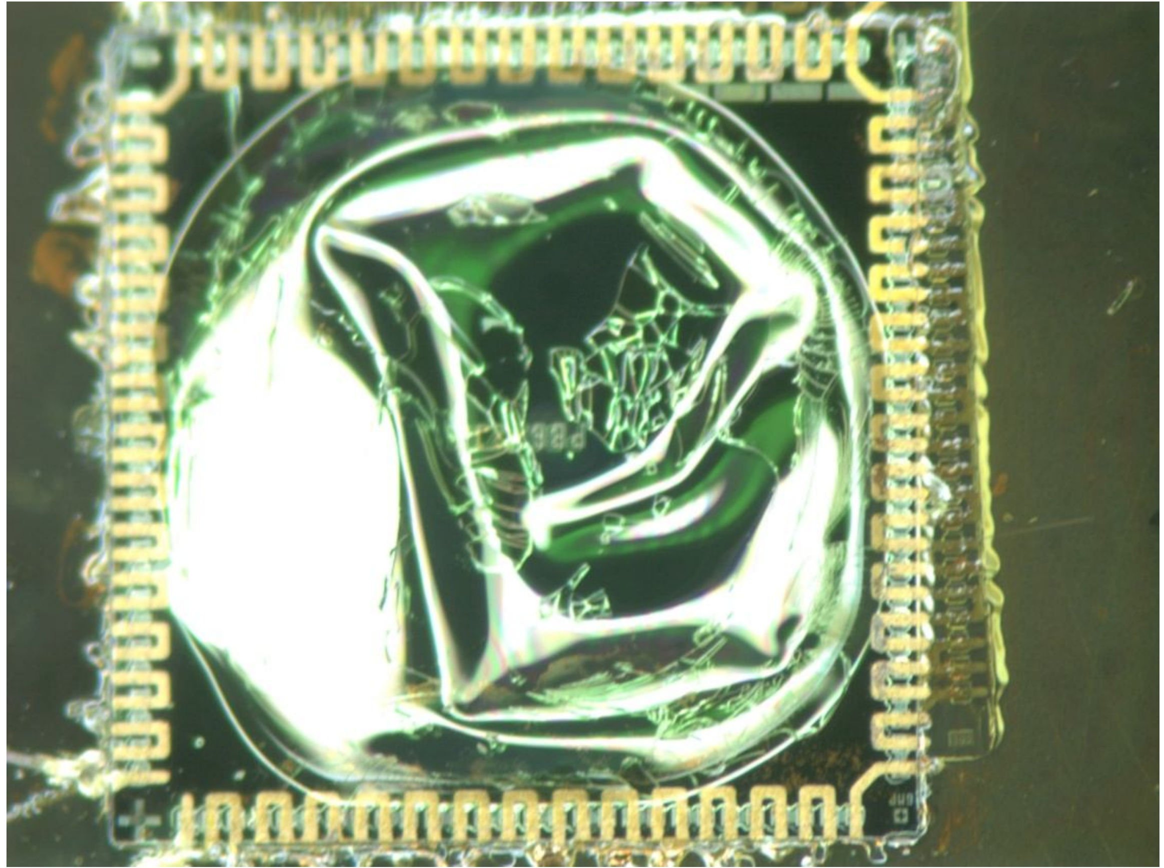

Figure 3.18: Polyimide-Polyimide Delamination Event

3.3. Interconnect Formation

The next step was the creation of contact hole vias through the top polyimide layer to the wirebond pads on the embedded die. This was accomplished using reactive ion etching (RIE). Following this, interconnects were formed using an electron beam deposited Ti/Cu seed layer and electroplating Cu/Ni/Au. The package was finished with a

third layer of PI-2611. Test pads were opened using the same RIE profile. Figure 3.19 outlines this process.

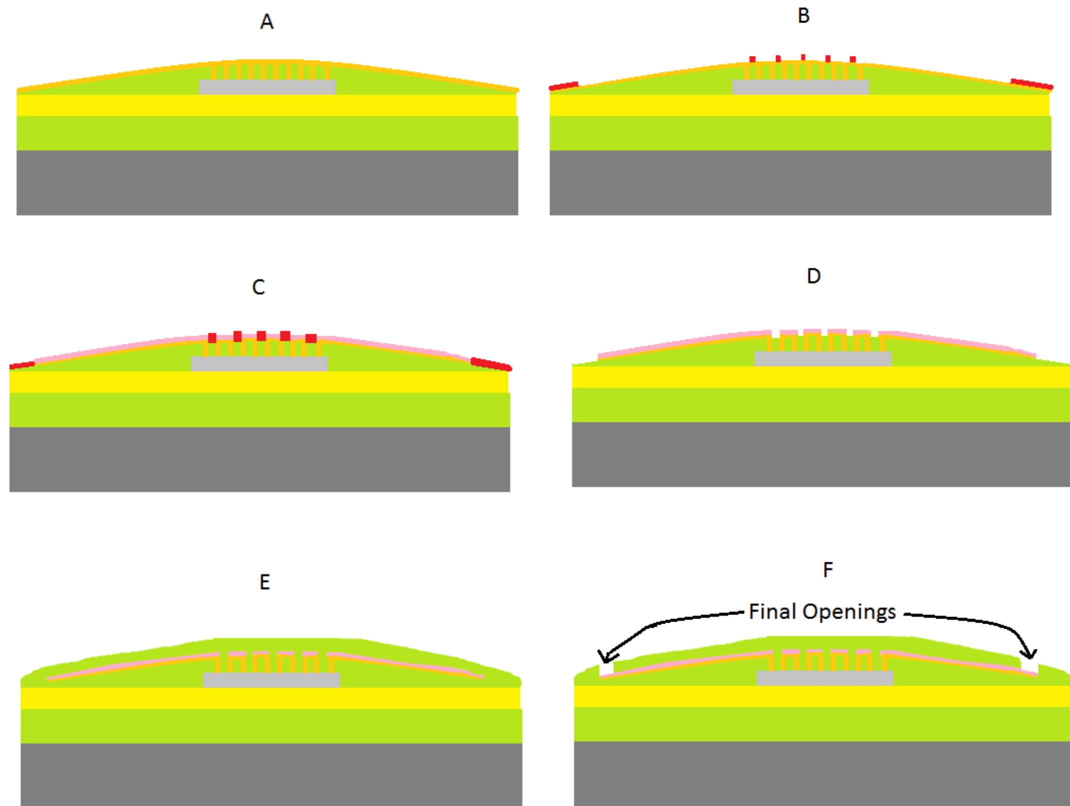

Figure 3.19: Interconnect Formation Process Flow

A: Seed Layer Deposition; B: Patterning of Seed Layer; C: Plating of Interconnects; D: Removal of Photoresist and Seed Layer; E: Third Polyimide Layer Deposition; F: Opening of Test Pads

3.3.1. Opening Contact Holes

The polyimide wafer was masked and the top polyimide layer was then oxygen plasma etched, using an STS AOE (Advanced Oxide Etcher), to open the vias. Due to the fact that the AMNSTC mircolab's AOE is tooled for 5-inch wafers and the processing wafers were only 4 inches in diameter, the processing wafers had to be temporarily attached to 5-inch dummy wafers. This was accomplished by heating a 5-inch wafer to 120˚C and applying a 4-inch diameter sheet of Dynatex International Wafer Grip. The Wafer Grip is thermoplastic and after 5 minutes the 4-inch wafer was pressed down onto the Wafer Grip and then alowed to cool. Since etching was performed with RIE oxygen plasma, a thick photoresist was required. For this process, AZ4620 positive photoresist was spun onto the wafer at 1500rpm for 30 seconds, resulting in a thickness of 12µm. The resist was then soft baked at 110˚C for 3 minutes and 30 seconds. This thickness was important since the etch process etched approximately 3µm of polyimide for every 5µm of photoresist. Once coated and soft-baked, the wafers were contact printed and UV exposed for three 30 second cycles. The wafers were then developed in 3:1 H_2O:AZ400K developer [45] and then exposed under UV light for an additional 20 seconds after descum to ensure that no bubbling would occur during etch.

Once properly masked, the wafers were placed in the STS AOE etcher for 8 minutes. The etch profile consisted of 80% O_2 and 20% CF_4 and utilized a 13.56MHz RF generator. See Table 3.3 for the full etch profile. Due to an issue with the wafers

overheating and causing the photoresist to bubble, the etching was performed in four two minute runs where the wafer was allowed to cool between runs. Once the contact holes were opened to the die aluminum pads (Figure 3.20), the remaining photoresist was stripped off in acetone. Once again, dehydrating the wafer after this step was extremely important.

Table 3.3: Polyimide Plasma Etch Recipe (1 Cycle)

Step	**Time (sec)**	**O_2 Flow (sccm)**	**CF_4 Flow (sccm)**	**Base Pressure (mTorr)**	**Coil Power (watts)**	**Platen Power (watts)**
Etch	120	40	10	90	500	300

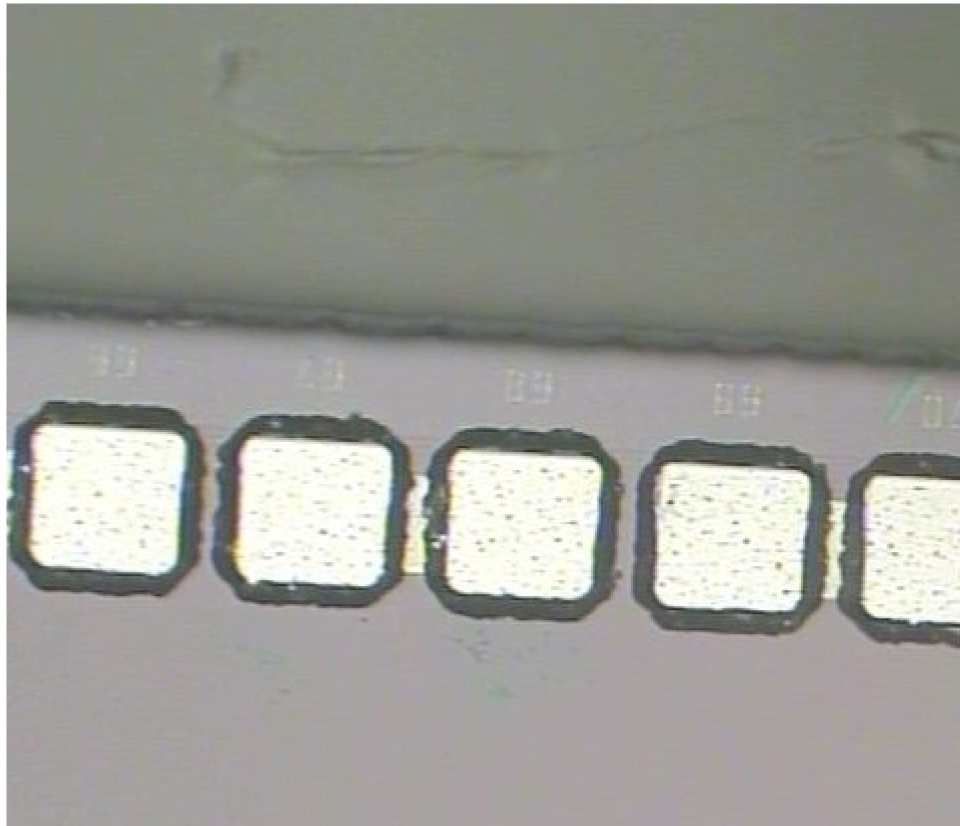

Figure 3.20: Open Vias for Interconnects

3.3.2. Interconnects

The daisy chain interconnect pattern for this test device was implemented using a standard Ti-Cu-Ni-Au process. A seed layer of 250Å Ti and 2000Å Cu was deposited over the entire wafer by electron beam evaporation for use as a plating seed layer. In order to improve metal/polyimide adhesion, a 1-minute oxygen plasma etch was performed on each wafer to roughen its surface.

Channels for realizing the interconnections were then patterned in approximately 4µm of AZ9245 photoresist. After a 5-minute HMDS application [46], AZ9245 was spun on at 3000 rpm for 30 seconds and soft-baked for 110˚C for 90 seconds. The mask pattern (Figure 3.21) was exposed for 60 seconds. Due to a need for positive photoresist, a dark-field mask was necessary. This would have made the alignment of the 40µm traces extremely difficult. Therefore, alignment fiducials were placed on either side of the die during the polyimide etch (Chapter 3.3.1). These were (relatively) large squares and were aligned to during the metalization photolithograhy with a cross. An example of the fiducial can be seen in Figure 3.27 at the end of this chapter. Again, wafers were developed in 3:1 H_2O:AZ400K for approximately 3 minutes. A 15-second oxygen plasma descum and 10 second UV exposure were also performed.

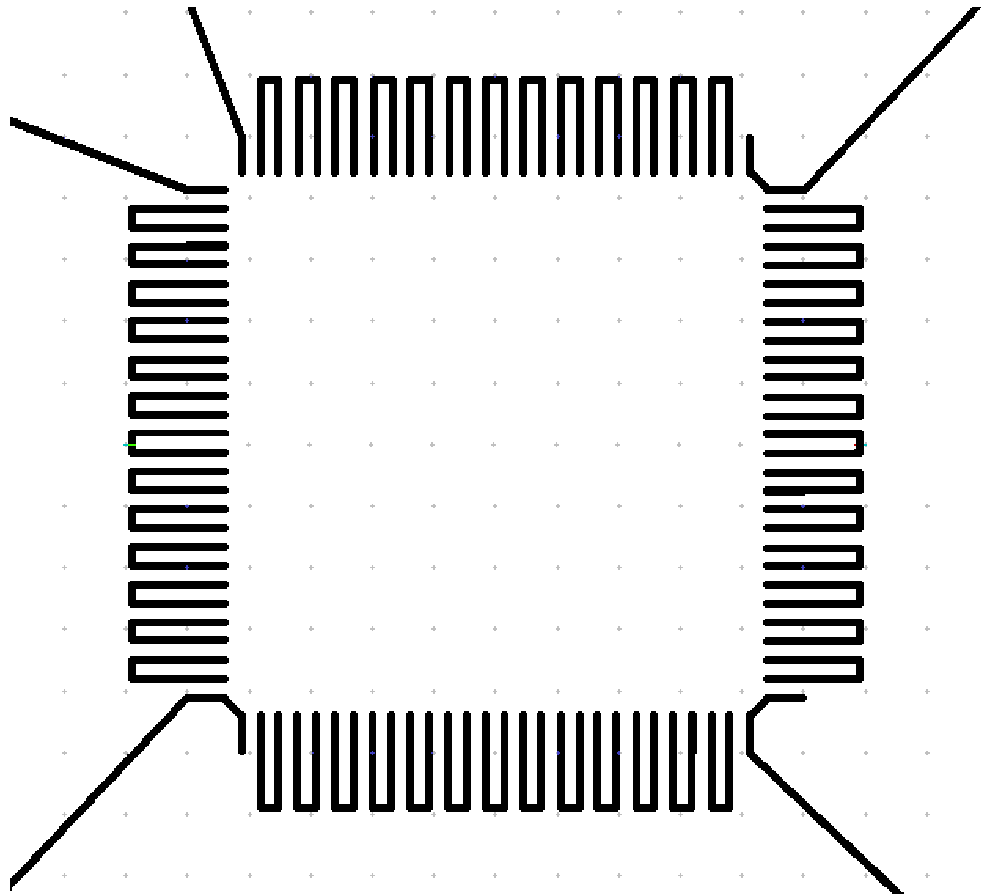

Figure 3.21: Interconnect Mask

Once properly masked, the exposed seed layer was ready for electro-plating. Plating was accomplished in 4 steps: Copper Solution, Nickel Solution, Gold Strike, and Gold Plating Solution. The composition of each solution is found in Table 3.4. Cu/Ni/Au was chosen for the simple fact that the test pads needed to be able to wet to solder. Since gold does not oxidize naturally, it makes an excellent material for the top layer. Additionally, due to the fact that copper will migrate into gold and form an unwanted

intermetallic, a nickel layer is commonly used as a barrier layer. Furthermore, it has been shown that copper will corrode over time when in contact with polyimide [47]. Therefore 1µm of Cu, 0.5µm of Ni, and 0.5µm of Au were used for interconnects and test pads.

Table 3.4: Electroplating Solutions

Table 3.4a: Copper Electroplating Solution	
Microfab SC Makeup	1 L
Microfab SC MD	8 mL / L
Microfab 10 70/30	2 mL / L

Table 3.4b: Nickel Electroplating Solution	
Nickel Sulfamate RTU	1 L
Nickel Stress Reducer	8 ml / L

Table 3.4c: Gold Electroplating Solutions	
Orostrike C	Pure
RTU HS434	Pure

For copper and nickel electroplating, the substrate (cathode) to be plated is wired to the negative terminal of a power source, while a block of copper or nickel (anode) is connected to the positive terminal. For each solution, the pair are immersed during the entirety of the plating time. As the current passes across the electrolyte, electrons are continuously supplied to the cathode, where positive ions combine with electrons and are transformed into neutral atoms that are deposited on the surface of the wafer. Atoms on the surface of the block are converted into positive ions at the anode, entering into the plating solution to compensate for the loss of positive ions due to the electron combination at the cathode.

Prior to placing the wafers into solution, they were dipped into a 5% HCl Solution for 20 seconds then briefly rinsed with DI water. This ensured that the surface was clear of any oxide that would prevent ions from attaching to the surface of the wafer. Copper was plated at 2mA per package on the wafer for 5 minutes and then 6mA per package for an additional 10 minutes. The reason for the low initial current was to fill in any gaps from the seed layer deposition and help the copper start up the sidewalls of the vias. After a rinse in DI water, nickel was plated at 6mA per package for 5 minutes. Additionally, the nickel solution was heated to 38˚C.

Gold electroplating was performed in two parts. First, the nickel plated wafer was placed directly into a pre-plating solution, Orostrike C, at 40°C. This gold pre-plating insured better adhesion of the gold to the nickel deposit. For this process, the substrate

was connected to the negative terminal of the power supply and a piece of platinum mesh was connected to the positive terminal. With current flowing, the pre-plating solution was ionized and positive Au ions from the solution moved toward the cathode, depositing on the plated nickel. The current was set to 1mA per package for 2 minutes. With a small amount of gold built up on the surface, the risk of oxidation was now alleviated. The wafer could now be rinsed well and then placed into a more pure gold solution. This solution was heated to 50˚C with a current of 1mA per package for 3 minutes.

Once plating was completed, the removal of the photoresist and seed layer was required. The wafer was rinsed in DI water, and then placed into acetone to remove the photoresist. Once the resist was thoroughly removed, the wafers were cleaned with methanol and DI water. The removal of the copper seed layer required a copper etchant, Cu 49-1 [48]. The etchant was heated to 40˚C and the wafer was submerged for approximately 2 minutes. As the bond pads on the die were aluminum, the removal of the titanium seed layer had to be performed using the STS AOE: since the titanium wet etchant will also etch aluminum. The time to etch 250Å of Ti was approximately 60 seconds. The process parameters are listed in Table 3.5. Figure 3.22 portrays the interconnects as they slope down into the contact holes. Likewise Figure 3.23 depicts the interconnects running off of the test die.

Table 3.5: Titanium Plasma Etch Recipe

Step	Time (sec)	O_2 Flow (sccm)	SF_6 Flow (sccm)	Base Pressure (mTorr)	Coil Power (watts)	Platen Power (watts)
Etch	60	8	40	30	700	0

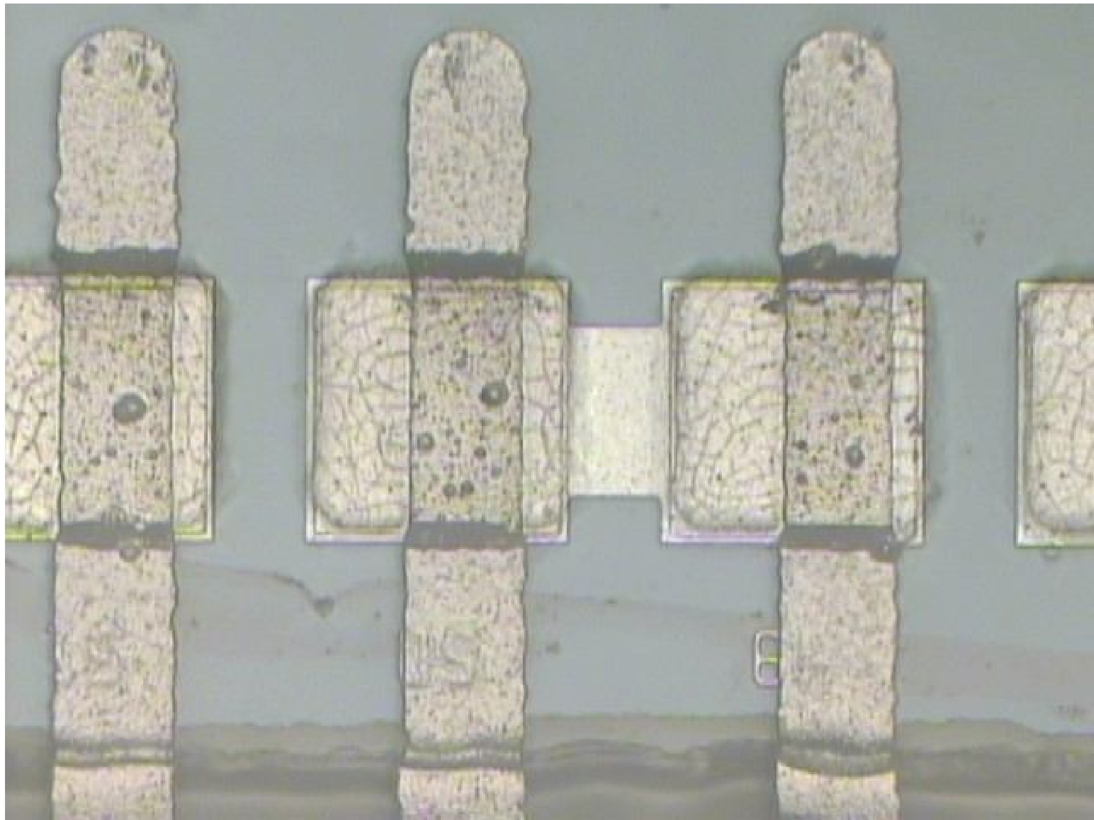

Figure 3.22: Interconnects Contacting the Die Pads

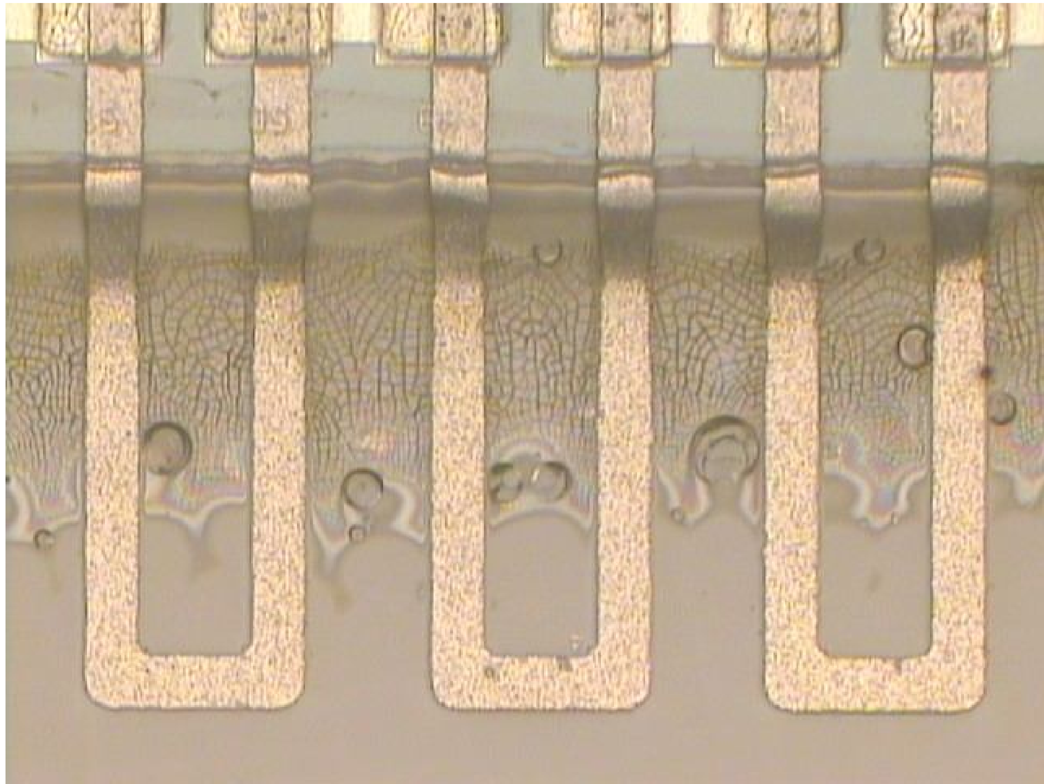

Figure 3.23: Interconnects Running Off Chip to Complete the Daisy Chain

3.3.3. Interconnect Formation Issues

There were, in fact, a few issues with the formation of interconnects. First, controlling the heat during the polyimide etch was of great importance. Due to the thickness of the photoresist (12μm) and the fact that the processing wafer had to be attached to a secondary 5-inch wafer for use in the STS AOE, the photoresist would tend to bubble or burn if the etch cycle was too long. To mitigate this, the 8 minutes of etch were spaced out into four 2-minute runs with adequate time for cooling in between.

Another issue was the choice of nickel plating solution. The sulfamate solution used above tends to be less corrosive and has a lower internal stress than other nickel plating solutions. One such other solution is the Watts Ni Plating Solution, outlined in Table 3.6. The Watts solution is inexpensive and more readily available. Unfortunately, the aluminum wirebond pads on the test die were too easily corroded by this mixture (Figure 3.24). Many attempts were made to make the solution work—low current plating, higher current plating, shorter exposure times—but none were successful.

Table 3.6: Watts Nickel Electroplating Solution

Nickel Sulfamate	200 g / L
Nickel Chloride	5 g / L
Boric Acid	25 g / L
Ferrous Sulfate	8 g / L
Saccharin	3 g /L

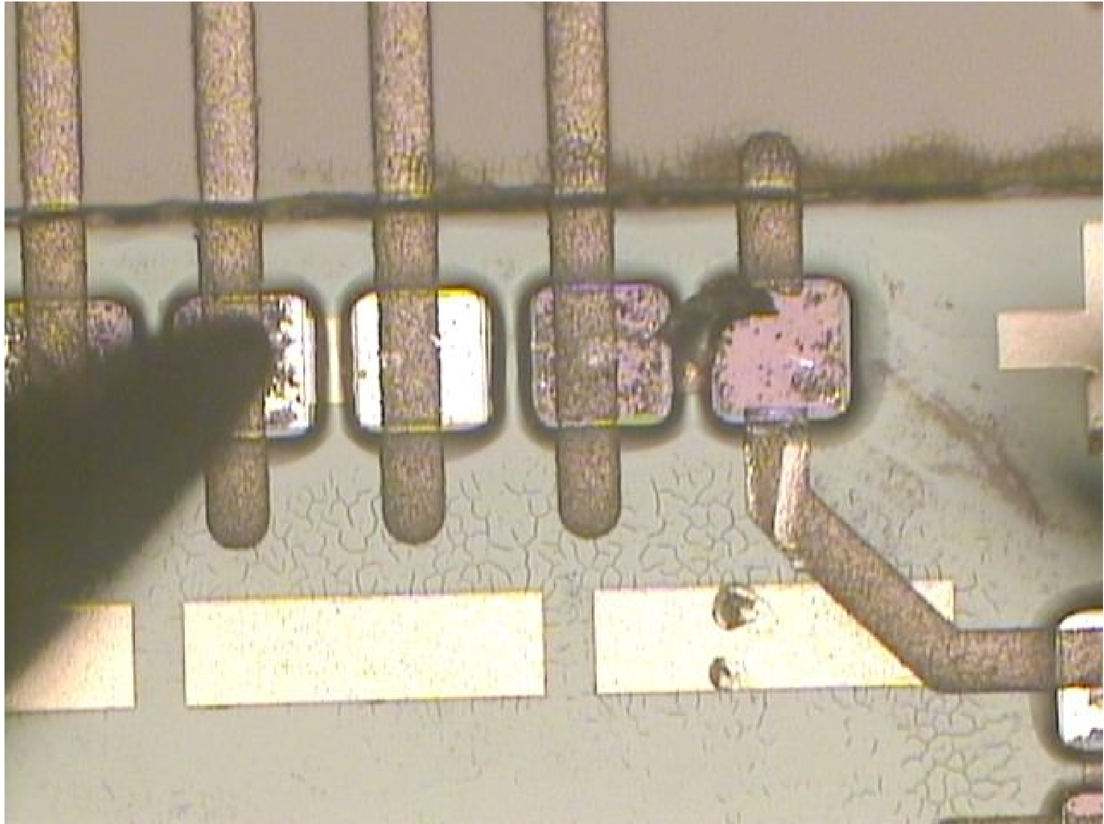

Figure 3.24: Corroded Aluminum Pads from Exposure to Watts Solution

Lastly, there was an issue with the size of the test pads. This design opted for 5mm diameter test pads for ease of solderability. An issue came up with the test pads delaminating from the substrate when they were etched open through the third polyimide layer (Chapter 3.3.4). This appears to be a result of the large area of the pad and high stress of the etching and / or polyimide cure. In order to compensate for this, the openings for the test pads were made to be only 4mm in diameter (Figure 3.25). This corrected the issue while still leaving a sizable area for soldering. Additionally, the final

polyimide cure was carried out at a maximum temperature of 250˚C to reduce the stress on the pads.

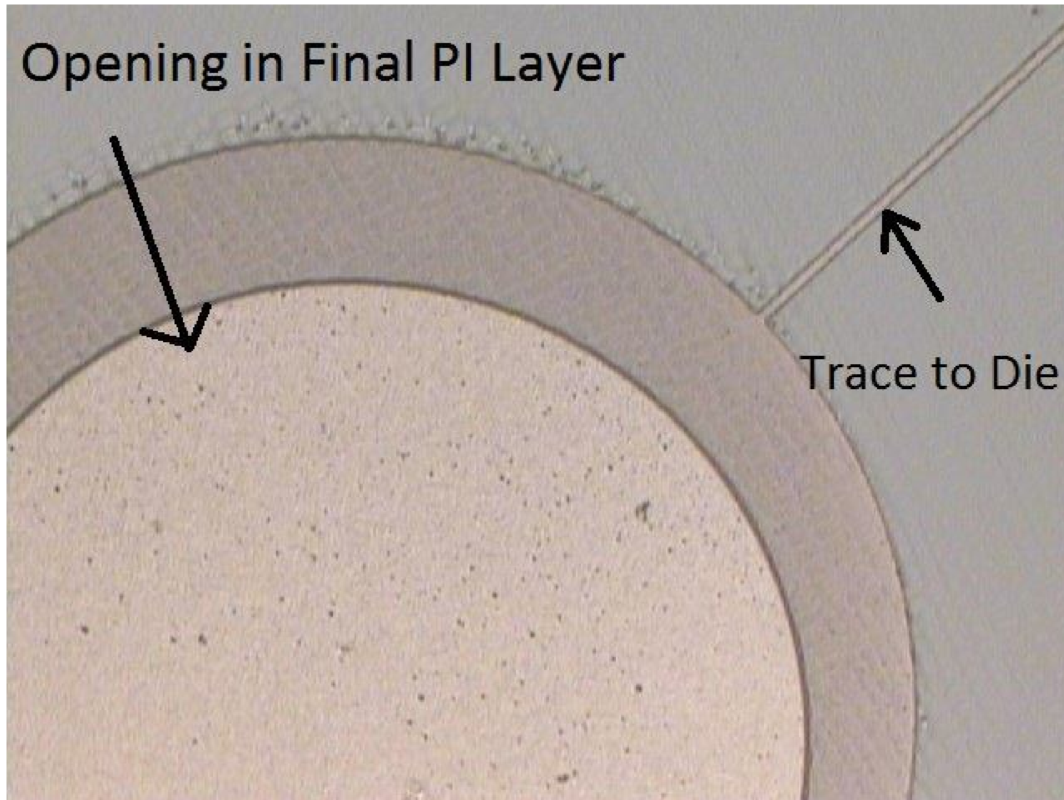

Figure 3.25: Finished Test Pad with Opening

3.3.4. Completing the Package

Before the final layer of polyimide was applied, another nitrogen plasma exposure was performed to improve the polyimide-polyimide adhesion. The entire wafer was again

dehydrated and the final layer of polyimide was spun on and cured, resulting in a layer thickness of approximately 6µm. The last step involved opening holes in the polyimide to access the test pads off the die. This step was performed in the exact manner as the via hole creation. There was one issue concerning the size of the pads—see Chapter 3.3.3 for details.

The fabricated device could then be peeled off of the processing wafer, yielding the completed package. Photographs of a fully packaged die are presented in Figures 3.26, 3.27 and 3.28. The final package was approximately 35µm thick. The package's 5 large test pads are solderable and used for thermal testing. Probes can be used to measure the resistance between pads.

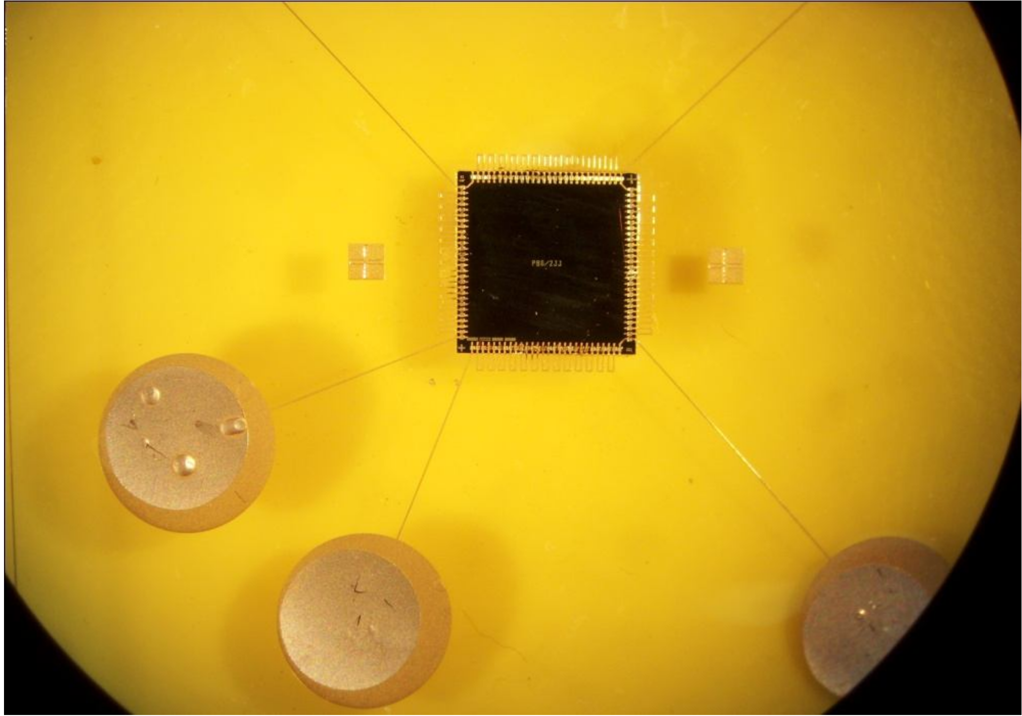

Figure 3.26: Completed Package

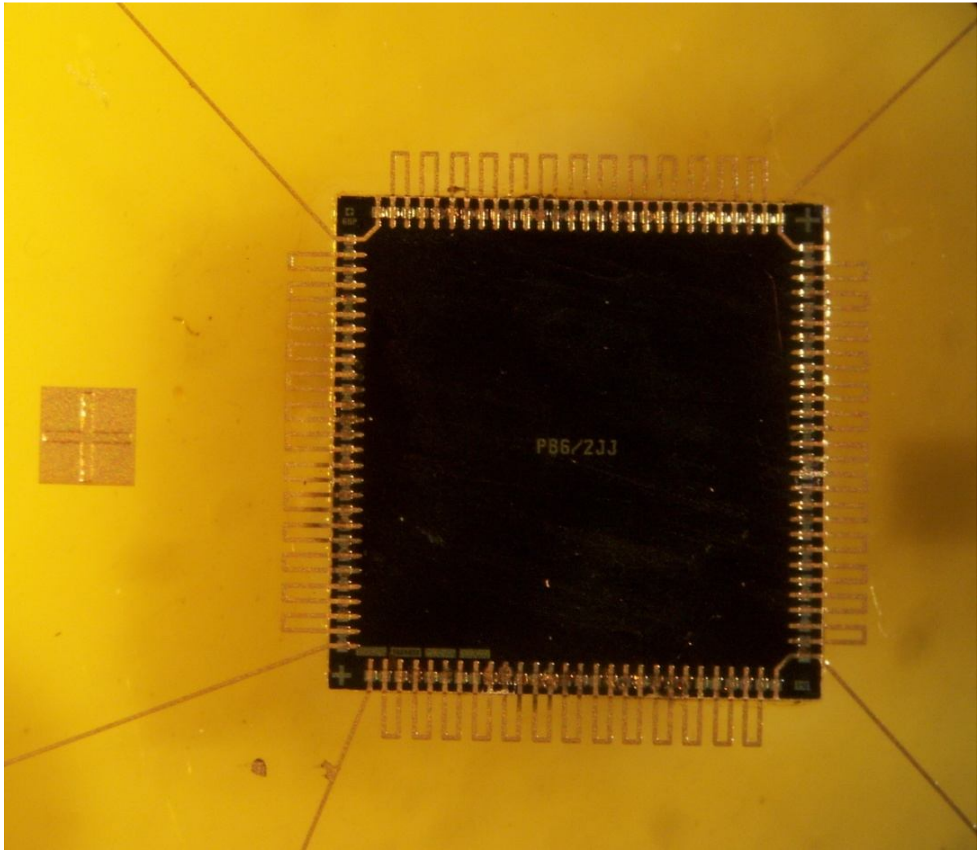

Figure 3.27: Released Package (Note the fiducial on the left)

Figure 3.28: Completed Assembly Flexed Around a Pen

4. Thermal Shock Testing

Thermal shock testing is performed to determine the resistance of a device to sudden changes in temperature. Parts are exposed to an extremely low (or high) temperature and shortly thereafter exposed to an extremely high (or low) temperature. This takes place in a RANSCO thermal cycling chamber (Figure 4.1). During this time, electrical testing of the samples is performed to detect electrical failures accelerated by the temperature cycle.

Failure acceleration due to thermal shock depends on three main factors: the difference between the high and low temperatures used; the transfer time between the two temperatures; and the dwell times at the extreme temperatures. Breakage during thermal testing is usually associated with CTE mismatches: different parts of the package expanding and contracting at different rates. Failure mechanisms accelerated by thermal shock include die cracking, delamination, wire / interconnect breaks, and bond lifting. For reliability testing or qualification of new devices, 1000 temp cycles are usually performed [50].

The particular specifications for thermal cycling used in this work are discussed in the following sections.

Figure 4.1: RANSCO Thermal Cycling Chamber

4.1. Thermal Shock Profile

The parameters for thermal shock testing were designed to *Mil*-Std-883 [51]. Cycling took place between +120°C to -40°C with a dwell of 10 minutes and a transition time of less than 1 minute (Figure 4.2). These particular temperatures were chosen because they serve as a good benchmark for in-service conditions (a car engine for example). Furthermore, the change is great enough that any significant manufacturing or design defects should manifest themselves.

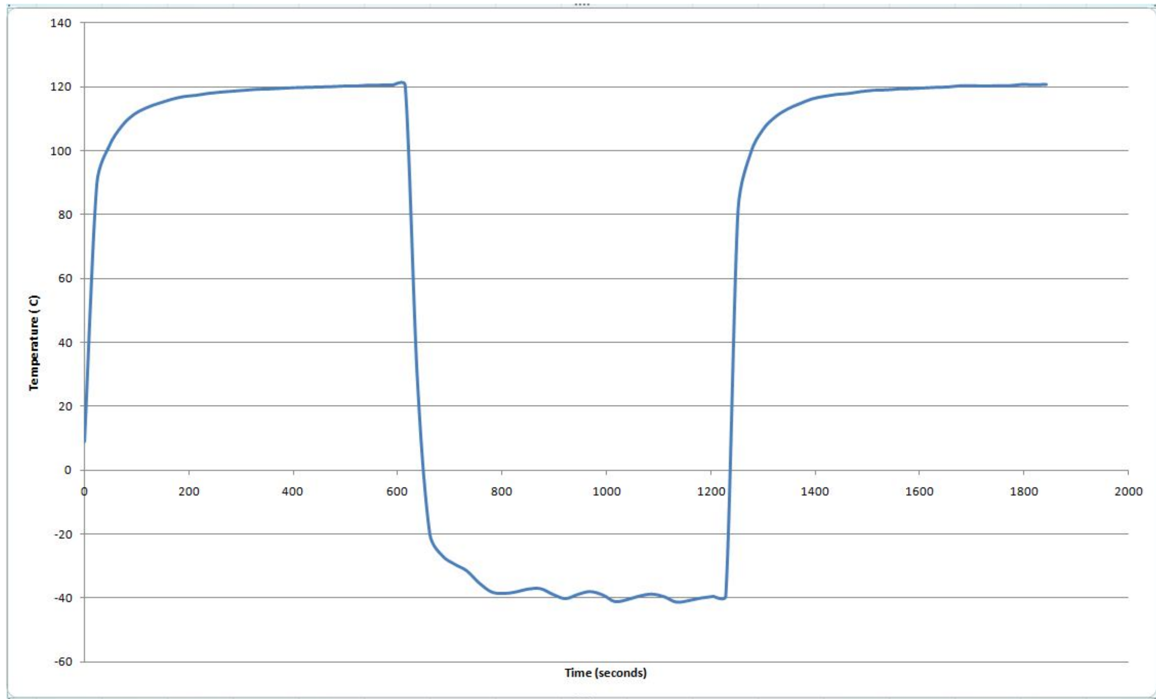

Figure 4.2: Thermal Shock Profile Captured from Thermocouple in Chamber

4.2. Test Setup

Fifteen daisy chain packages were separated into three groups and mounted to aluminum substrates. Each group held the packages in a different orientation: flat, convex, and concave. The flexed fixtures were semicircles with a radius of 3 inches. The packages were affixed to the aluminum with kapton tape. Figure 4.3 depicts two such groups.

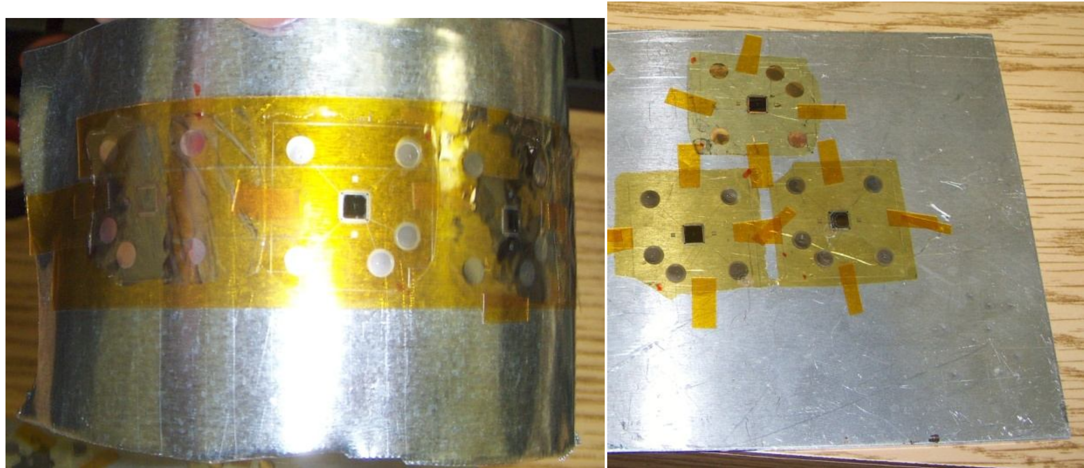

Figure 4.3: Convex and Flat Testing Orientations

Once securely fastened to the aluminum, 24AWG Teflon coated wire was used to connect the daisy chains to a computer running LabView data collection software. The wires were soldered to the large test pads on each package at the opposite ends of the daisy chain. Each wire was hand soldered and 66/44 Sn/Pb rosin core solder was used. These wires were run out of the oven and into an interface board (Figure 4.4). LabView passed an excitation current through the package and would monitor the voltage across two terminals at the beginning and end of the interconnect pattern. In this way the resistance between the two terminals on the daisy chain was monitored and would report a failure at over 100 ohms. Since the accuracy of the resistance under 100 ohms was not important, a basic 2-point resistance measurements was utilized.

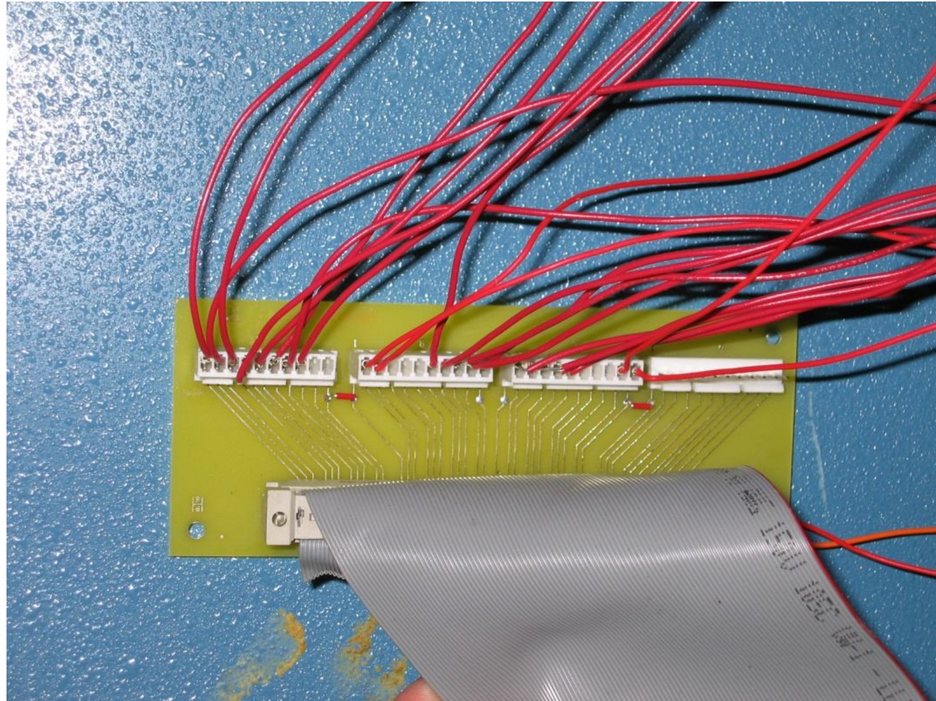

Figure 4.4: Fully Wired Interface Board

4.3. Thermal Shock Test Results

After 4000 thermal cycles, just over one half of the packages had experienced a failure. Since several units survived the entire test without failing, the data set included right censored data. This type of censoring is called "right censored" data since the times of failure to the right (i.e., larger than the test time) are missing. A Weibull plot (a flexible life distribution model) was used to analyze the data (Figure 4.5).

This analysis led to a shape parameter (or Weibull Slope) of 0.5033 and an estimated lifetime of 4841 cycles. Special Weibulll statistical analysis software was used to generate Figure 4.6--an extrapolated reliability vs. time graph. The correlation coefficient for this dataset is 0.9642, indicating that the Weibull plot is a good match for this data.

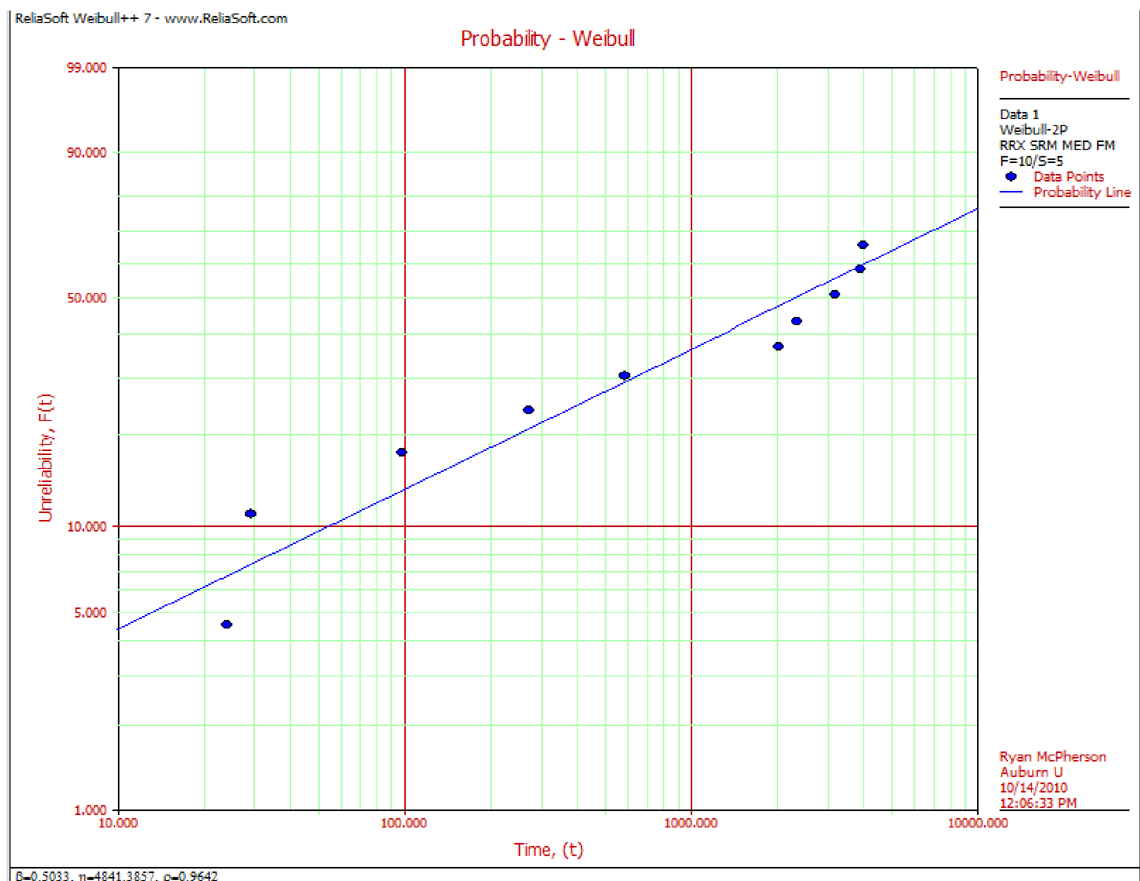

Figure 4.5: Weibull Plot of Thermal Test Data

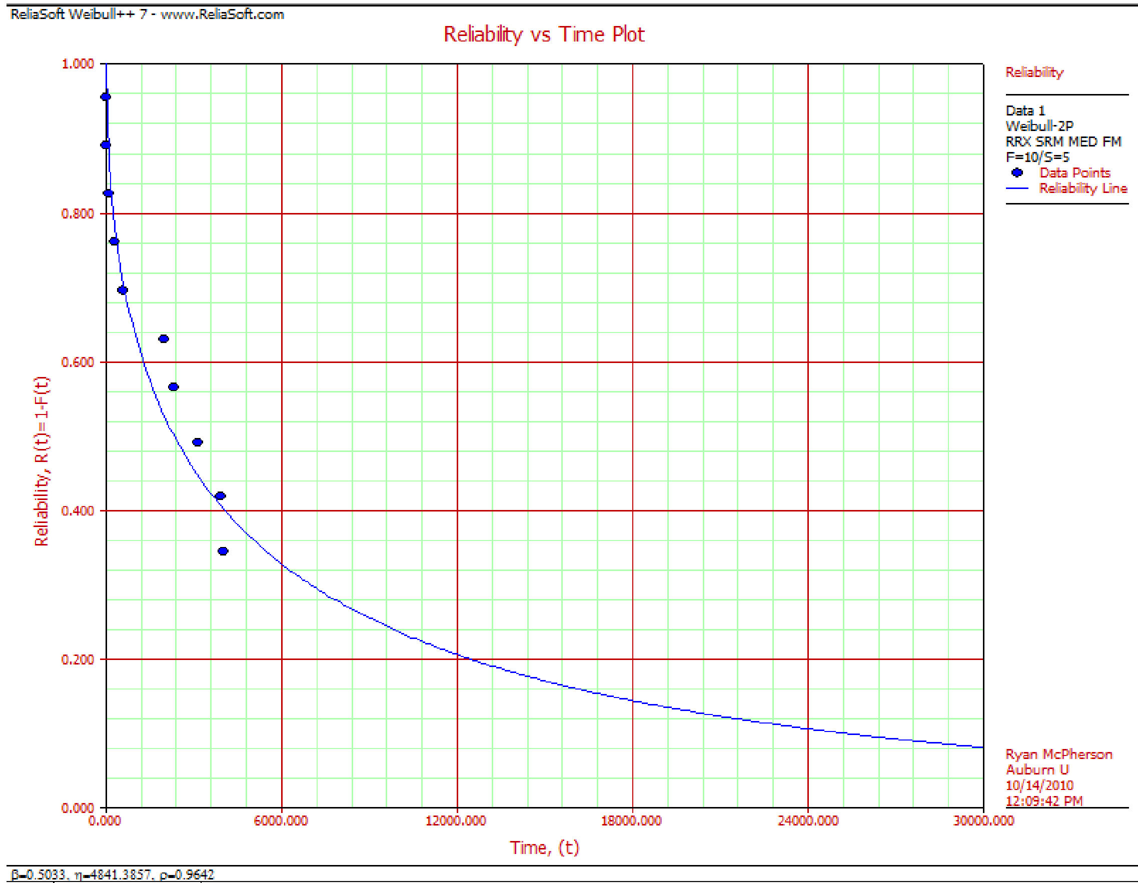

Figure 4.6: Reliability vs. Time Plot

After 2367 cycles, a majority of the failed parts were removed from the test oven for analysis. Using visual inspection, the most common source of failure was a delamination of the polyimide and die, causing the interconnects to break (Figure 4.7). Another issue is that of pad corrosion (Figure 4.8). At this time, the exact cause of the degradation of the Al bond pads is unknown. The pattern of corrosion appears almost

random in nature, and may be due to trapped chemicals from the fabrication process. Ni / Au plating of the bond pads may mitigate this issue.

Figure 4.7: Interconnect Breakage Due to Delamination Event

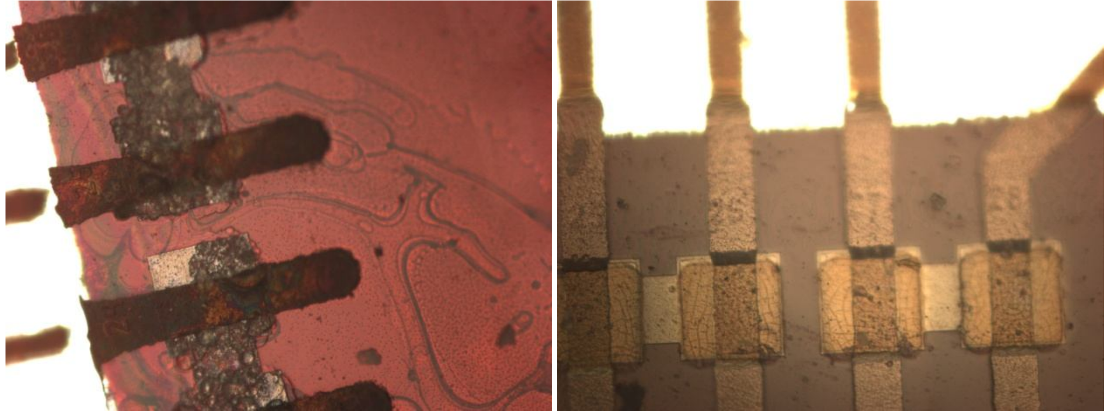

Figure 4.8: (Left) Significant Pad Corrosion; (Right) No Corrosion Present

5. Finite Element Analysis

A basic FEA simulation was performed to get an idea of the limits of the flexibility of the assembly. The simulation was done using Intellisense Intellisuite Mechanical Analysis Software. The ultimate strength of silicon in a 3-point flexural test varies between 200 and 400 MPa, while the ultimate strength for BCB is 87MPa [21,53].

The first analysis performed was to determine the maximum displacement of a 10µm die as opposed to a 50µm die in the flexural test. The maximum displacement for the 10µm thick die was 901µm (Figure 5.1), while the maximum displacement for the 50µm thick die was 183µm (Figure 5.2). It is interesting to note that the correlation of these two values is linear with respect to the die thickness. In each case, the stress was measured in plane—x-direction (Figure 5.3, 5.4).

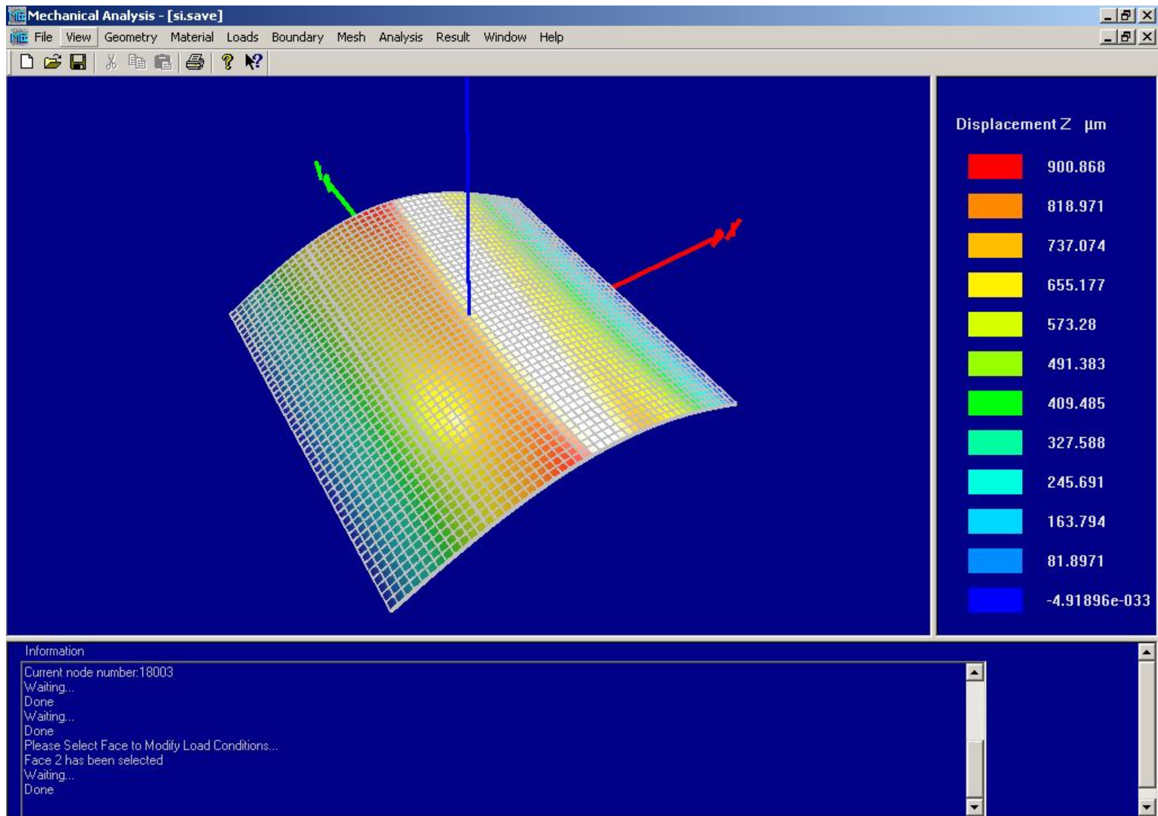

Figure 5.1: Simulated Maximum Displacement of 10µm Thick Silicon Die

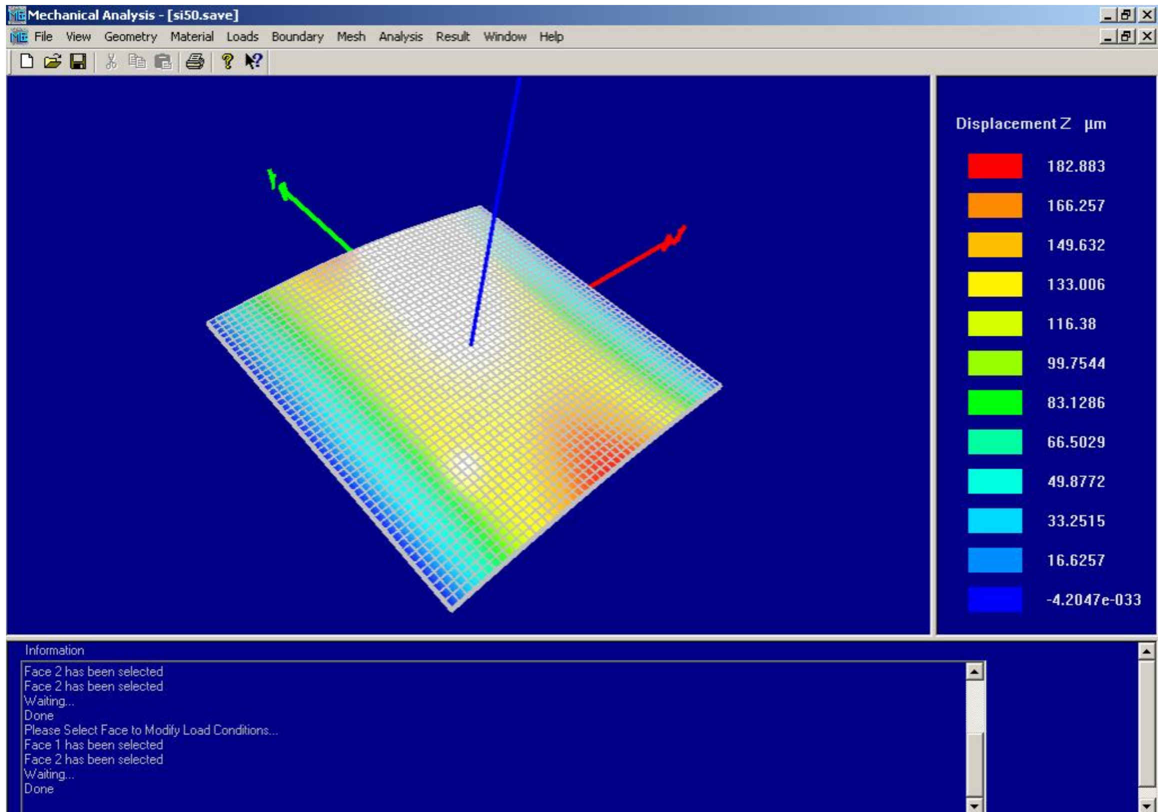

Figure 5.2: Simulated Maximum Displacement of 50µm Thick Silicon Die

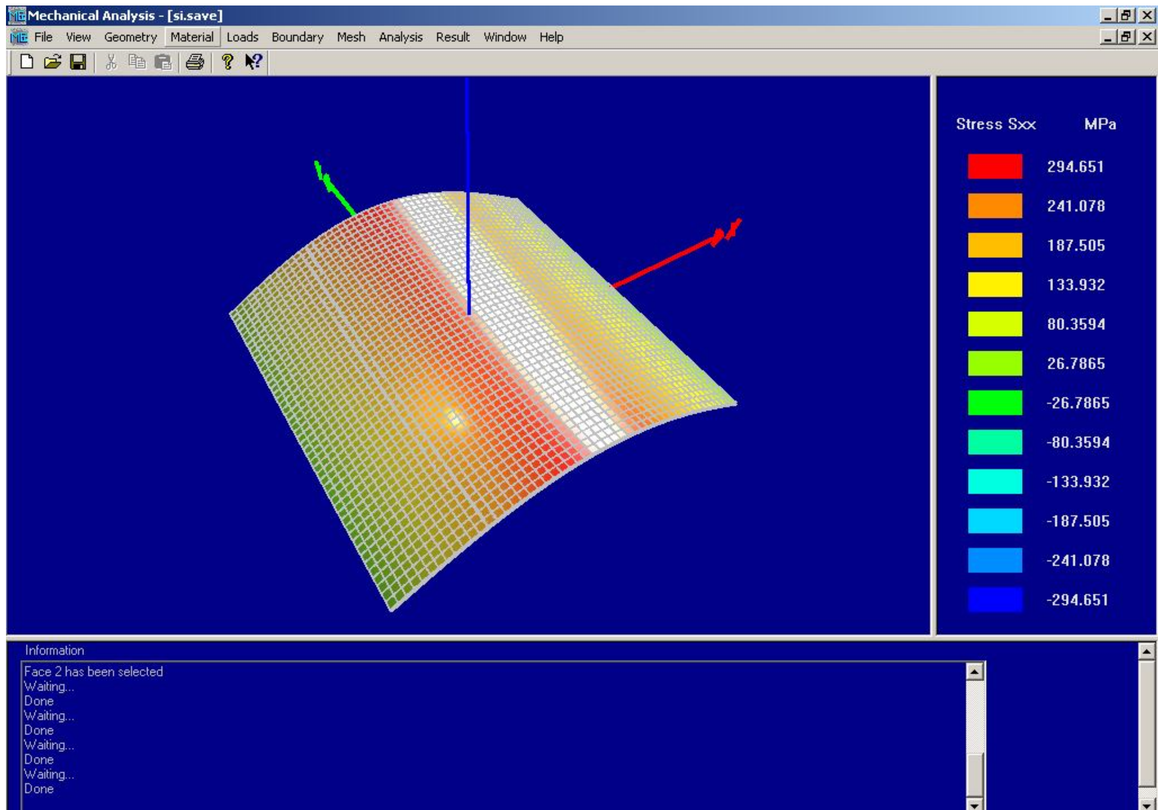

Figure 5.3: In Plane Stress of 10µm Thick Silicon Die

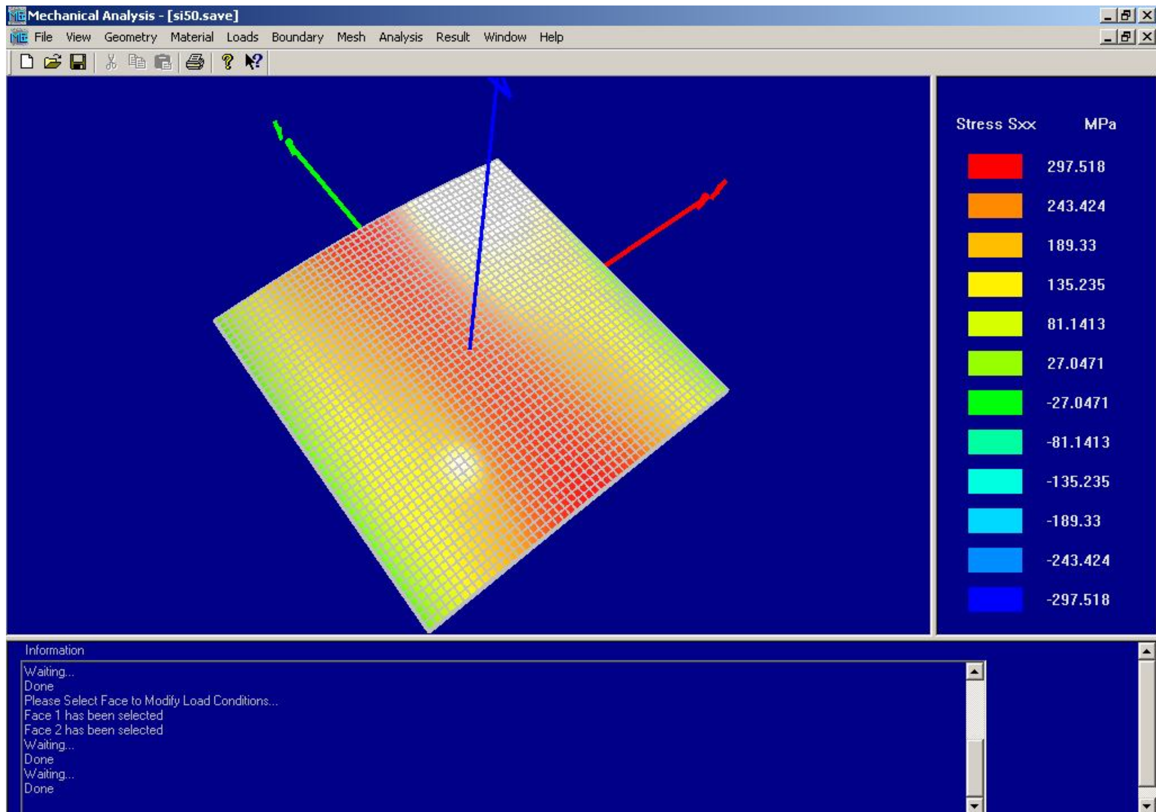

Figure 5.4: Simulated In Plane Stress of 50µm Thick Silicon Die

Next, a simulation was performed on a model of the chip package. The parameters for PI-2611, BCB, and silicon were entered into the model in an effort to determine the maximum displacement of the assembled package. Figure 5.5 depicts the maximum displacement at a stress of 300MPa. With a value of 947µm it is clear that the silicon is the limiting factor—which was to be expected. The stress on the BCB and silicon for this simulation confirm this as the BCB is under no more than 1MPa (Figure 5.6), while the Silicon is close to its failure point (Figure 5.7).

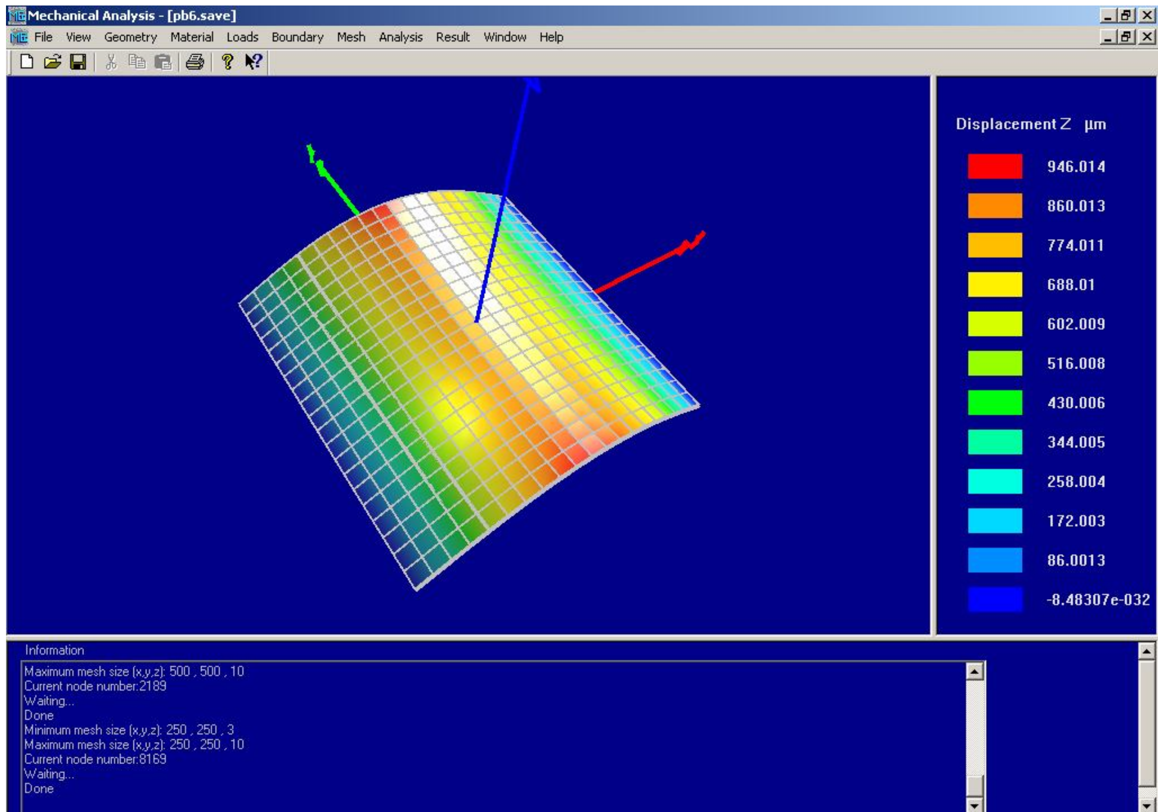

Figure 5.5: Simulated Maximum Displacement of Packaged Die

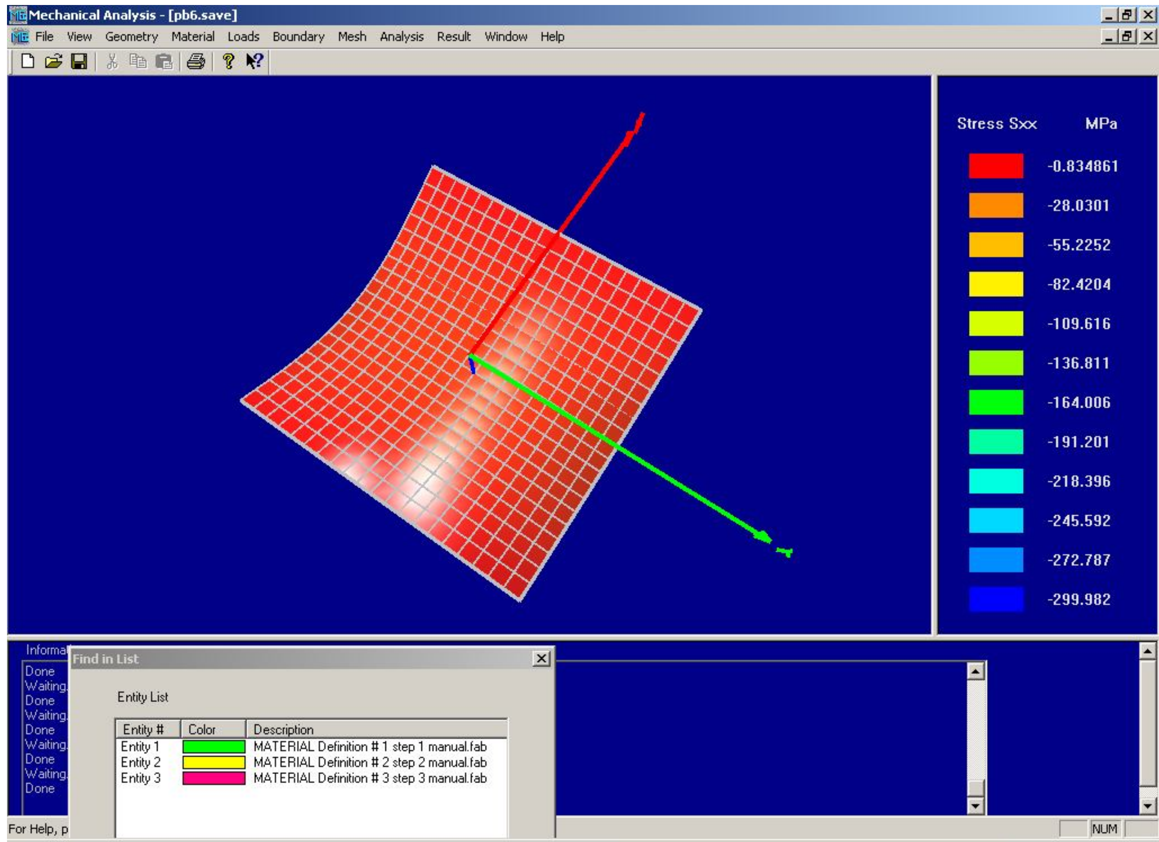

Figure 5.6: Simulated In Plane Stress on BCB in Assembled Package

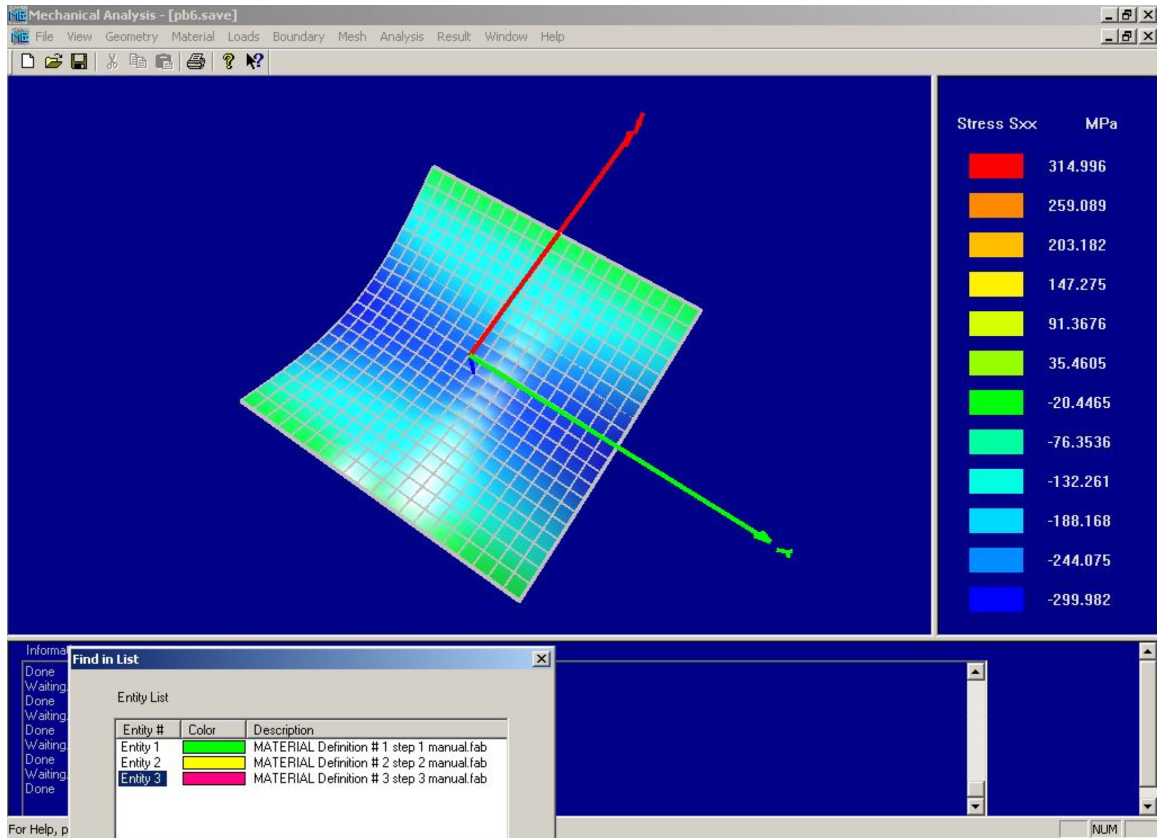

Figure 5.7: Simulated In Plane Stress on Si in Assembled Package

In examining this data, it is clear that the thinner silicon is more flexible, as it produces more displacement with the same amount of stress. Additional simulations were performed on the completed package model in an attempt to see a difference in stress or displacement in relation to the direction of bend; however, no correlation was found.

6. Multi-Chip-Modules

Additional work has been performed to realize multi-chip modules. Using a similar technique, coplanar and 3D daisy chain assemblies were fabricated and tested for electrical continuity. The coplanar assembly fabrication was accomplished in much the same manner as the single die. The major exception was the need to align two die on a plane before they were cured to the substrate. In order to accomplish this, a small aluminum fixture was created to align the die. A photograph of the fixture is presented in Figure 6.1. The fixture was manufactured from 20 mil (508µm) thick aluminum stock. A hole punch was used to create 6 mil (147µm) standoffs on the fixture to prevent the fixture from curing to the BCB. The die and fixture were carefully placed onto the BCB covered wafer by hand. Once properly aligned, the die were loaded and cured in the same manner as described in Chapter 3.2.2.

The remainder of the fabrication process was identical to that of the single die assembly. Photographs of a finished coplanar assembly are presented Figure 6.2.

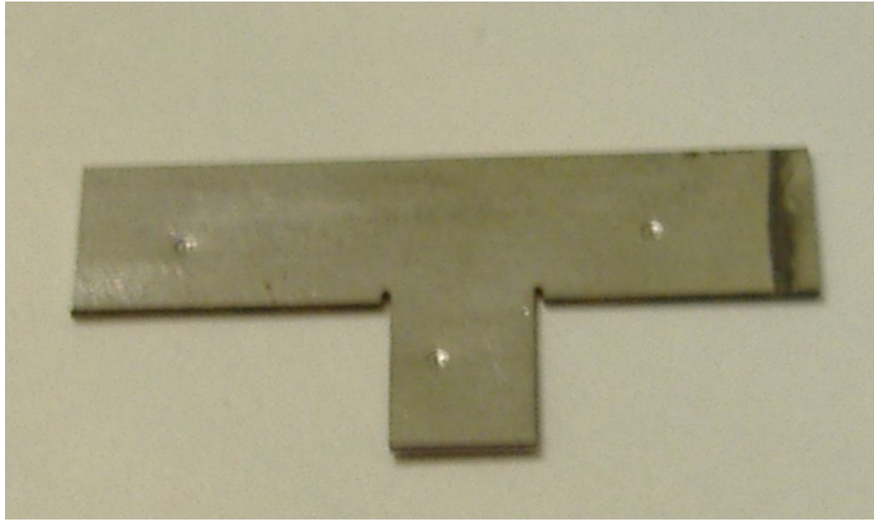

Figure 6.1: Coplanar Assembly Alignment Fixture

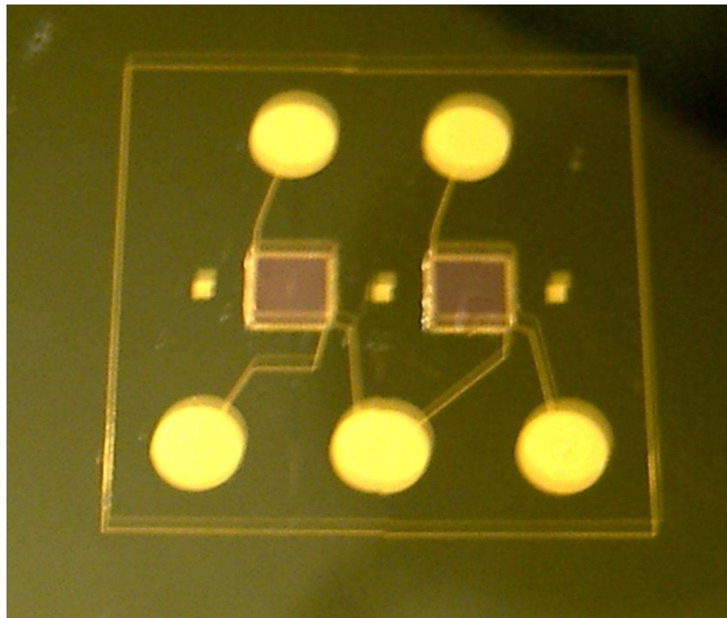

Figure 6.2: Completed Coplanar Assembly

The fabrication of 3D die stacks is merely an extension of the single die assembly. The only change occurred during electroplating where gold is unnecessary for intermediate layers, as Cu/Ni is sufficient to prevent trace corrosion. Once completed, the process was repeated: with the subsequent BCB layer and thinned die cured directly over the metal layer (Figure 6.3). Since the interconnect pattern included the same large test pads as previous assemblies, there was a good amount of leeway for aligning the top and bottom die. Obviously in a production environment this process would need to be more tightly controlled and would require some sort of fixture or automated alignment tool.

To avoid corrosion and improve sodlerability, the final metal layer was gold electroplated. Once the final polyimide layer is spun, cured, and contacts are etched, the completed 3D multichip circuit is released from the silicon wafer. A close-up photograph of a completed 3D assembly, with the top die cured off-center of the bottom die for enhanced viewing, is presented in Figure 6.4.

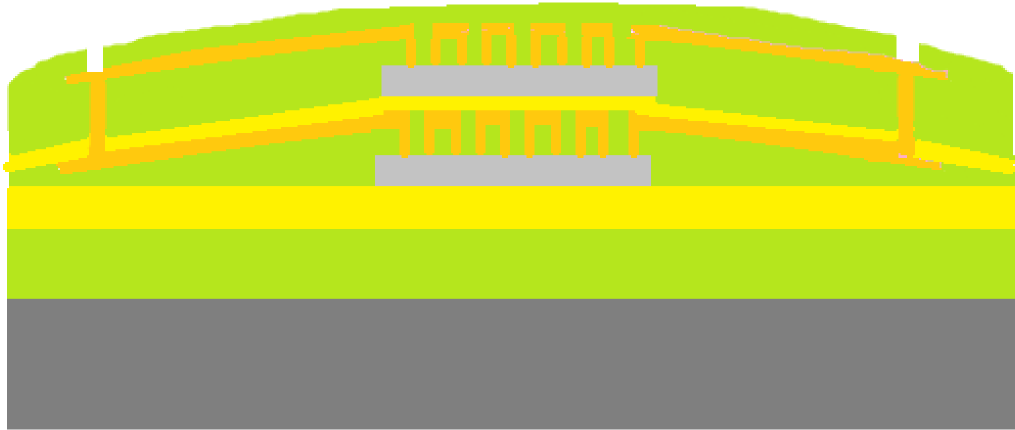

Figure 6.3: Diagram of a 3D Die Stack

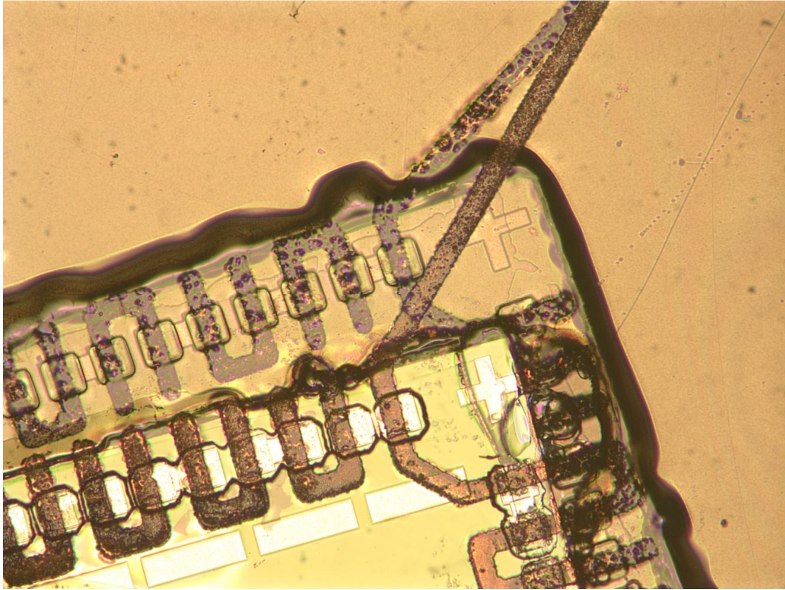

Figure 6.4: Misaligned 3D Die Stack

Testing was performed by testing electrical connectivity between each layer on a probe station. Current was passed through the lower die first, then passed to the upper die. The two die were connected at exactly one point to ensure that a failure at any point in the daisy chain would be detected.

7. Conclusions

As electronics packaging moves more toward 3D and flexible assemblies, thinner packages will continue to become more commonplace. The process for utilizing die thinned to a mere 10µm allows for packages with a total thickness of around 30µm. Furthermore, as electronics become smaller, board space is held at a premium. The ability to produce packages with thin 3D die stacks would greatly increase the density of electronics.

The work presented herein centers around three main concepts: die thinning, substrate fabrication, and metallization. Initial thinning was accomplished with "dicing by thinning" in order to alleviate stress on the die sidewalls. Die were taken to their final thickness with reactive ion etching. The use of a handle attached to each thinned die enabled the manipulation of the thinned die without a concern for chipping and cracking. The handle was also instrumental in keeping the die planar during the substrate bonding process.

A polyimide substrate was deemed best not only because of its flexibility and physical properties, but also because it could be applied in thin layers; here 6µm. PI-2611, in particular, was chosen for its CTE compatibility with silicon—hopefully resulting in improved thermal reliability. BCB was selected as the optimal material for

adhesive bonding due to its flexible film nature, void-free curing profile, and temperature compatibility with polyimide cures. The entire assembly process is compatible with standard fabrication techniques.

This research in the embedding ultra-thin die into polyimide substrates has been able to push the envelope in thin die packaging. Moreover, it has proven to have good flexibility and reliability to thermal shock. While promising, this technology can be further improved with future research.

8. Future Work

This dissertation presents a fabrication process for ultra-thin, flexible, silicon die packaging. The ideal applications for such products would be flexible sensors or RFID tags. Furthermore, this packaging technique could be utilized for 3D packages and other multi-chip-modules. 3D assemblies would benefit from the thinner die as interconnects between die are shorter. Early attempts in 3D assemblies were marred with reliability concerns [20]. The fact that the causes of failure in those assemblies (polyimide blistering, delamination, and corrosion) are shared by the devices that failed early in this study indicates that these failures may be more an issue of human error during the fabrication process and not necessarily a design flaw. There are, however, a few improvements that can be recommended at this time for both single die packaging, as well as future 3D endeavors.

Although the die are thinned to a mere 10µm, the current fabrication process still leaves the packages non-planar. Creating a polyimide cavity for the die to sit in, either through etching or photo-sensitive polyimides would help to mitigate this concern. This would be especially important in the assembly of 3D die stacks, where planarity may play a large role in reliability.

Additionally, a majority of the yield problems with this process centered around the Al bond pads on the test die. This led to the use of certain chemicals and processes that would not harm the die pads. The use of different metallurgy or Ni /Au bumping the pads would have eliminated a number of issues encountered throughout the fabrication process; as well as increase the available options for fabrication materials. Furthermore, this may eliminate the corrosion seen in Figure 4.8.

Moving from the test chips to an active device would be the next logical step for this research. By integrating an op-amp or microcontroller, electrical testing could be performed to see if the 10μm die are robust enough to handle flex and thermal testing. Furthermore, it would be interesting to observe the effects that bending these assemblies would have on electrical performance.

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Appendix

Preparation of Handle Die:

Clean Oxide Wafer	Acetone, Methanol, DI Water
Dehydrate Wafer	20 minutes 120˚C
Spin Humiseal onto unpolished side	1000 rpm 30sec 333 ramp
Hard-Bake	2 hours at 90˚C
Dice Wafer	Fwd speed 1000
Dehydrate Individual Die	2 hours at 120˚C (in vacuum)

Die Thinning:

Saw Trenches into Wafer	75 – 100µm depth
Chemical Mechanical Polishing	Performed at Aptek Industries – Die returned in waffle packs ~ 50µm
Bond Die Stacks with Flip-Chip Bonder	Heat: 200g force, 160˚C, 120 seconds
	Cool: 200g force, 50˚C, 90 seconds
Clean Oxide Wafer	Acetone, Methanol, Water
Dehydrate Wafer	20 minutes 120˚C
Mount Die Stacks to Oxide Wafer	WaferGrip - 120˚C
Clean Backside of Thinned Die	Acetone, Methanol, DI Water

Oxygen Plasma Clean	30 seconds, 300W
ASE Etch	20-21 cycles
	See Table 2.1 for recipe

Prepare Polyimide Substrate:

Clean Silicon Wafer	Acetone, Methanol, DI Water
Dehydrate Wafer	20 minutes 120˚C
Spincoat AP3000	3000 rpm 30sec 1000 ramp
Soft-Bake	60 seconds at120˚C
Spincoat PI-2611 (6 µm)	500 rpm 8 sec / 3000 rpm 30 sec 500 ramp
Hard-Bake	5 minutes in 120˚C oven
Cure Polyimide	YES OVEN Program 6
	See Figure 3.8

Adhesive Bond Die to Substrate:

***Dehydration Bake**	2 hours 150-200˚C
Roughen PI Surface	1 minute N_2 Plasma
Spincoat AP3000	3000 rpm 30sec 1000 ramp
Soft-Bake	60 seconds at120˚C
Spincoat BCB	500 rpm 8 sec / 3000 rpm 30 sec 500 ramp
Soft-Bake	90 seconds at 90˚C
Expose	60 seconds over 3 exposures
Place Die stacks onto Substrate	Lightly weight stack (30-40g)

Cure BCB	120˚C / 15 minutes; 250˚C / 60 minutes
	See Figure 3.9
Remove Handle Die	Heat Wafer to 140-160˚C
	Shear Handle off of wafer
Clean Humiseal Residue	Acetone, Methanol, DI Water

* Unnecessary if taken directly from curing oven

Encapsulation:

Dehydration Bake	2 hours 150-200˚C
Spincoat AP3000	3000 rpm 30sec 1000 ramp
Soft-Bake	60 seconds at120˚C
Spincoat PI-2611 (6 µm)	500 rpm 8 sec / 3000 rpm 30 sec 500 ramp
Hard-Bake	5 minutes in 120˚C oven
Cure Polyimide	YES OVEN Program 6
	See Figure 3.8

Open Contact Holes:

***Dehydration Bake**	2 hours 150-200˚C
****Attach to 5-inch wafer**	Wafer Grip, 120˚C
Spincoat AZ4620 Photoresist (12 µm)	500rpm 5sec / 1500 rpm 30sec 333 ramp
Soft-Bake	3:30 at110˚C

Pattern Wafer	Expose for 3 x 20 seconds
Develop 1:3 AZ400K:H_2O	Approx. 3 minutes
Post Develop Exposure	10 Seocnds
Descum	O_2 Plasma, 15 seconds
Etch Contact Holes	Approx 4 2-minute runs
	See Table 2.2 for recipe
Remove from 5-inch Wafer	120˚C
Strip PR	Acetone, Methanol, DI Water

* Unnecessary if taken directly from curing oven

** Needed for AMNSTC AOE

Metalize Contacts:

Dehydration Bake	2 hours 150-200˚C
Roughen PI Surface	1 minute O_2 Plasma
Electron Beam Deposition	250 Å Ti / 2000 Å Cu
HMDS Application	5 minutes
Spincoat AZ9245 Photoresist (4.5 µm)	1700rpm 5sec / 3000 rpm 30sec 500 ramp
Soft-Bake	90 seconds at110˚C
Pattern Wafer	Expose for 3 x 20 seconds
Develop 1:3 AZ400K:H_2O	Approx. 3 minutes
Post Develop Exposure	10 Seocnds
Descum	O_2 Plasma, 15 seconds

Electroplating:

Plate Copper (1 µm) - Room Temp	5% HCL Dip 20 seconds
	3 mA/cm^2 5 minutes
	9 mA/cm^2 10 minutes
Plate Nickel (0.5 µm) - 38˚C	5% HCL Dip 20 seconds
	9 mA/cm^2 5 minutes
Plate Gold (0.5 µm) - 50˚C	Orostrike – 1 mA/cm^2 2 minutes
	RTU - 1 mA/cm^2 3 minutes
Strip Photoresist	Acetone, Methanol, DI Water
Strip Cu Seed Layer	Cu etchant 49-1, 38˚C 2 minutes
Strip Ti Seed Layer	Plasma Etch 1 min
	See Table 2.4 for recipe

Final PI Layer:

Dehydration Bake	2 hours 150-200˚C
Roughen PI Surface	1 minute N_2 Plasma
Spincoat AP3000	3000 rpm 30sec 1000 ramp
Soft-Bake	60 seconds at 120˚C
Spincoat PI-2611 (6 µm)	500 rpm 8 sec / 3000 rpm 30 sec 500 ramp
Hard-Bake	5 minutes in 120˚C oven
Cure Polyimide	Low Stress Cure (250˚C)

Open Test Pads:

***Dehydration Bake**	2 hours 150-200˚C
****Attach to 5-inch wafer**	Wafer Grip, 120˚C
Spincoat AZ4620 Photoresist (12 µm)	500rpm 5sec / 1500 rpm 30sec 333 ramp
Soft-Bake	3:30 at110˚C
Pattern Wafer	Expose for 3 x 20 seconds
Develop 1:3 AZ400K:H_2O	Approx. 3 minutes
Post Develop Exposure	10 Seocnds
Descum	O_2 Plasma, 15 seconds
Etch Contact Holes	Approx 4 2-minute runs
	See Table 2.2 for recipe
Remove from 5-inch Wafer	120˚C
Strip PR	Acetone, Methanol, DI Water

* Unnecessary if taken directly from curing oven

** Needed for AMNSTC AOE