Thermal Cycling Reliability of Nickel added Solder Paste for Use in Surface Mount Manufacturing

by

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Abstract

With the ban on lead (Pb) by the European Union (EU), the electronics industry has sought alternatives to replace the long used Sn-Pb solder. Although Sn-Ag-Cu (SAC) alloys with Sn3Ag0.5Cu (SAC 305) have been considered as a replacement option, a clear understanding of the mechanical and reliability aspects of these alloys is very important. With the increasing use of mobile electronics, the reliability of SAC 305 alloys is under question due to its poor drop/shock performance. Even though suggestions to use less silver content to increase the alloy performance are shown in the literature, they suffer from increased failure rates when exposed to higher operational temperatures and thermal cycles.

A search for an optimized Sn-Ag-Cu (SAC) alloy with good drop performance (SAC 105) and a better thermal cycling reliability (SAC 305) is ongoing to increase reliability. Many lead-free solder pastes with additives such as Mn, Cu, Ni etc are being tested by numerous researchers to determine their drop/shock and thermal cycle reliability.

In this work Sn/0.7Cu/0.05Ni/Ge paste, manufactured by Nihon, was used to assembly various SMT packages and its assembly characteristics were studied. On a 60 mil thick board, land grid arrays (LGA), quad flatpack no lead (QFN) and resistors were assembled using SAC 305, SAC 105 and Nihon paste. Boards were also built using Sn-Pb paste to serve as a reference. Assembly characteristics of all the pastes were studied, identifying ideal parameters for successful surface mount technology (SMT) implementation.

The assembled boards where subjected to accelerated thermal cycle testing from -55^{o}C to 125^{o}C, with 10 minutes dwells at high temperature, 5 minutes dwells at low temperature and 30 minutes ramps. The total cycle time was 90 minutes. The thermal cycle results as a function of both alloy and the package type were studied.

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Chapter 1

Introduction

1.1 Electronic Packaging Definition

Electronic packaging deals with connecting various electrical and electro-mechanical components on a printed circuit board (PCB) to achieve the desired functionality of a system. It is an art of establishing interconnections between various levels of electronic components, modules and sub-systems. Electronic components consist of the both active components (integrated circuits (IC's), transistors, etc) and passive components (resistors, capacitors, etc). The components are interconnected to produce electronic products. The functions of electronic packaging include signal distribution, power distribution, heat dissipation and protection (mechanical, chemical and electromagnetic).

1.2 Surface Mount Technology

Surface mount technology (SMT) as a process is the practice of mounting surface mount electronic components on the surface of the printed circuit board. It provides a state of the art solution that decreases package size, increases functional density and increases the possible number of package connections. In a typical surface mount manufacturing process (refer to Figure 1.1) there are four sequential operations: 1. solder printing; 2. solder inspection; 3. pick and place; and 4. solder reflow.

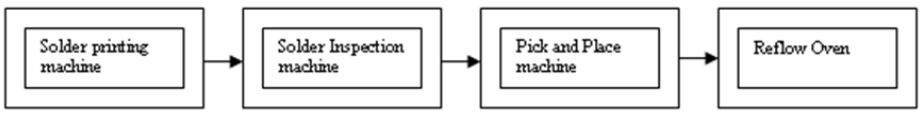


Figure 1.1: SMT Manufacturing Process Flow

The PCB is deposited with a sufficient amount of solder paste using a solder printing machine, and then the solder paste is inspected for any defects. A pick and place machine places the components on the PCB and finally a reflow oven is used to melt the solder to form a good solder joint between the component and the PCB board.

1.3 Surface Mount Devices

Surface mount devices/packages house active and passive components, and have termination along the body which are soldered to the PCB (refer to Figure 1.2). The main advantage of surface mount devices (SMD) is they provide greater packaging density because of their smaller size. Portable electronics has further driven the demand to decrease the package size and the widespread use of fine pitch and ultrafine pitch, ball grid arrays (BGA's) and chip scale packages (CSP's). Along with real estate savings these devices have many advantages like increased electrical performance, protection from environmental hazards, good heat removal, increased number of input/outputs (I/O's) and improved handling during assembly.

Even with the above mentioned advantages, SMD packages have their own share of disadvantages. With through-hole components, the solder joints are formed through the plated hole, which when compared to surface solder joints, are more reliable and robust. The surface mount packages are usually subjected to high temperatures during soldering which makes them prone to moisture related cracking. Due to various operational temperatures a package is subjected to while in operation, the mismatch in thermal expansion may lead to solder joint failure.

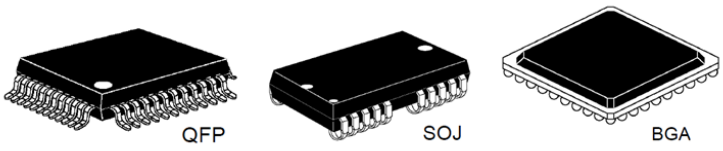


Figure 1.2: Comparison of Various SMT Devices [1]

1.4 Ban on Lead

Due to the increasing environmental concerns related to the use of lead, the electronics industry has pursued its elimination since 1990. The European Union (EU) passed a law to ban the use of lead in electronics on Feb 13, 2003 [2], which went into effect on July 1, 2006 [3]. To comply with environmental regulations and to avoid any product delay issues many companies and consortium's were formed to find alternatives to Sn-Pb solder paste.

The lead-free solders replacing tin-lead should have good mechanical properties both in soldering and while in service. For a successful transition one needs to find replacement solder alloys which have favorable characteristics comparable to Sn-Pb [4]. Table 1.1 shows some of the promising lead-free alloys proposed initially by the researchers for use in SMT manufacturing.

Lead Free Alloys
96.5Sn/3.5Ag
93.6Sn/4.7Ag/1.7Cu
95Sn/4.0Ag/1.0Cu
95.5Sn/4.0Ag/0.5Cu
95.5Sn/3.0 Ag/0.5Cu
93.1Sn/4.7Ag/1.7Cu/0.5Co
96.2Sn/2.5Ag/0.8Cu/0.5Sb
91.8Sn/4.6Ag/1.6Cu/1Sb/1Bi
92.4Sn/3.3Ag/1Cu/1.1Bi
91.9Sn/3.3Ag/4.8Bi
95Sn/3.5Ag/1.5In
95Sn/3.5Ag/0.5Cu/1Zn
99.3Sn/0.7Cu
98.3Sn/0.7Cu/1In

Table 1.1: Proposed Lead-Free Solder Alloys

The National Center for Manufacturing Sciences (NCMS), after a four year major research effort concluded that there are no "drop-in" replacements for eutectic Sn-Pb [5]. The International Tin Research Institute (ITRI) [6] and the National Electronics Manufacturing Initiative (NEMI) [7] have recommended SnAgCu-305 eutectic (or near eutectic 405) alloy

for reflow solder applications. Mechanical characteristics such as creep and thermal fatigue of SAC 305/405 alloys are reported to be comparable to the traditional Sn-Pb alloys [8, 9] and after preliminary studies of various tin based alloys, SAC 305/405 was accepted as the best alternative [10].

With the increasing use of portable electronics in the market and the lead-free transition, the reliability of SAC 305/405 alloys have come into question due to their low drop/shock reliability [11, 12]. Alternatives to increase the drop/shock reliability by reducing the silver content in SAC alloys has been reported in the literature [13, 14]. These low silver SAC alloys even though having superior drop/shock reliability suffer from decreased high temperature cycling reliability, limiting their use in many applications [15].

Sn-0.7Cu was one replacement alloy suggested by the industry consortium at the beginning for use in wave soldering to replace Sn-Pb [16]. But due its poor solder joint fillet formation and the higher reflow temperatures needed (10^oC more than SAC 305) it did not gain popularity for use in SMT manufacturing [17]. However, it was discovered that adding smaller amounts of nickel would considerably increase the solderability and microstructure properties of Sn-Cu alloys [18, 19]. This has expanded the possibility for wider usage of these alloys. An alloy based on the Sn-Cu-Ni system with the addition of Ge is currently used successfully in lead-free wave soldering. This has prompted studies for using this alloy composition for SMT applications.

1.5 Product Qualification

Electronic assemblies are subjected to various stress and temperature ranges while in operation, and their reliability should be evaluated to avoid early failures on the field. Test standards set by industrial organizations such as JEDEC and IPC, should be used to analyze the performance of the assembly in various operational environments. Thermal cycling and drop/shock testing are an important part of reliability testing in which failures are accelerated on the PCB's to understand their life expectancy.

Thermal Cycle Testing: Thermal cycle tests are performed to understand if the part can withstand the extreme high and low temperature dwells, and its ability to function properly under cyclic stresses. A wide variety of dwell and ramp temperatures can be achieved inside an environmental chamber and devices are monitored for the failures to calculate their life expectancy. Laboratory thermal cycle testing provides an accelerated test that can be related to the expected product lifetime in the field where the thermal cycle conditions are less severe. Figure 1.3 shows a temperature cycle profile with dwell times and ramp rates identified. While testing, the profile starts at room temperature, ramps to the high temperature, dwells at the high temperature, then ramps down to low temperature, dwells at low temperature, and finally ramps upto the high temperature. This cycle is continuously repeated and the reliability of a part is given in terms of number of cycles to failure.

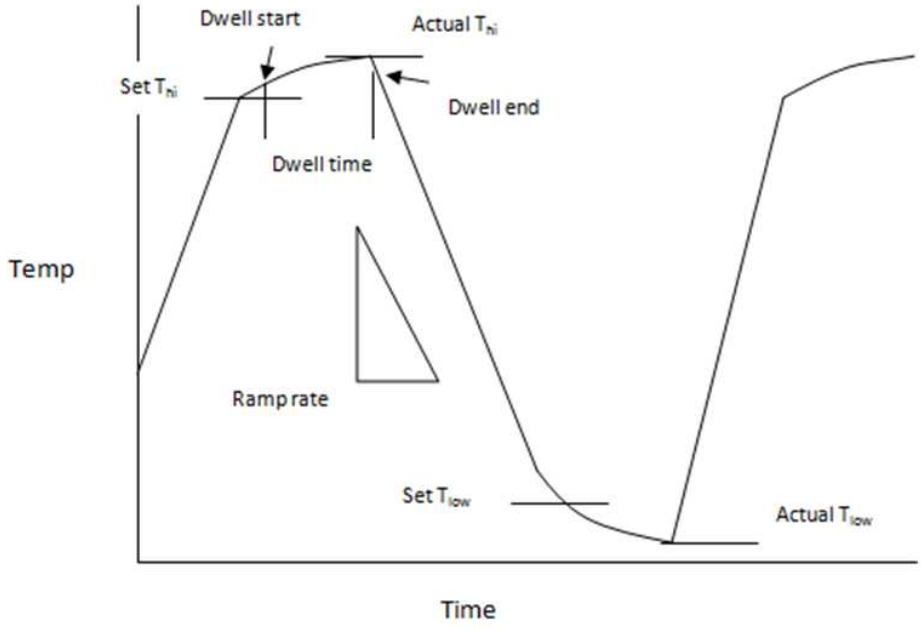


Figure 1.3: Thermal Cycling Profile

Two standards currently govern the thermal cycle testing and they are: JEDEC-JESD22-A104 and Mil-Std-883. In these standards, temperature excursions at high temperatures upto 300^{o}C, and at low temperatures down to -55^{o}C, are performed and the parts are classified according to their reliability. Even though dwell/ramp times and temperature ranges are

given as an exact number in thermal profiles, tolerances of +/- 5^{o}C can be considered as per the (IPC 9701-A table 4.1) [20, 21].

Drop/Shock Testing: With the widespread usage of portable electronics, drop/shock testing is currently performed on the PCB's to understand it's various failure modes. According to JEDEC-JESD22-B111 [22], "Drop shock tests are used to evaluate surface mount electronic component failures due to excessive flexure in circuit boards when dropped". In a drop/shock testing, boards are bolted to a surface, and then raised to a specified height and dropped on to the strike surface while measuring the acceleration value, pulse value and pulse shape. An example drop/shock profile is shown in Figure 1.4. Finally the reliability of the components are given by number of drops to failure.

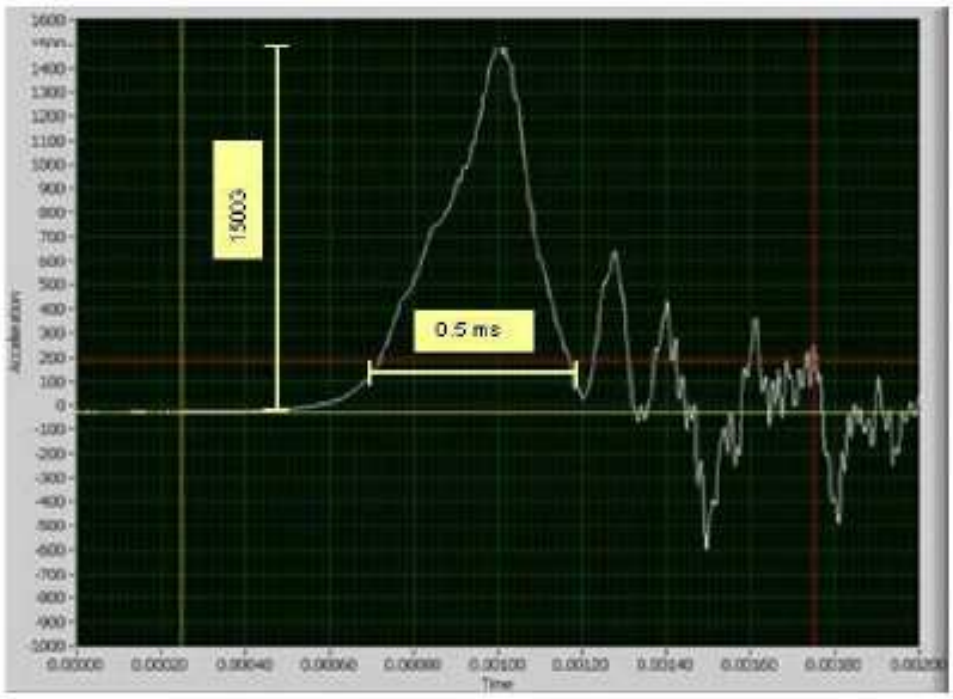


Figure 1.4: Drop/Shock Profile [22]

Failures while drop/shock testing due to material properties of bulk solder alloys and intermetallic compounds (IMC), with failures by crack initiation and propagation along the pad/package interface are shown in the literature [23, 24].

1.6 Thesis Organization

Chapter 2 provides a literature review of alloys performance with respect to thermal cycle and drop/shock testing. In Chapter 3 experimental details about PCB design, fabrication, SMT assembly characteristics and thermal cycle profile parameters used are discussed. In Chapter 4 experimental results are discussed. Conclusions and recommendations for future work are presented in Chapter 5.

Chapter 2

Literature Review

2.1 Thermal Cycling Performance of SAC Alloys

Due to the mismatch in coefficient of thermal expansion (CTE) between the component and the board, when subjected to high/low temperature excursions, solder joints experience stress and strains resulting in solder cracking after repeated cycles. Example solder joint failures are shown in Figure 2.1.

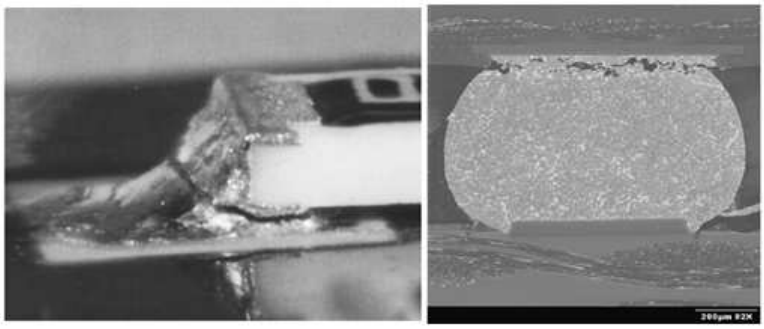


Figure 2.1: Thermal Cycle Fatigue Failures [1]

The major causes of failures during thermal cycle testing are due to both fatigue and creep in solder joints. Fatigue is defined as failures in the components due to repeated or cyclic stress application. While temperature cycling, cyclic stresses are generated on the whole assembly and with the inheritant mismatch in coefficient of thermal expansion (CTE), solder joints experience a large amount of stress and strains resulting in solder cracking.

Along with this, a solder joint exhibits a viso-plastic material behavior where creep deformation plays an important role in its reliability [25]. Creep is a failure mechanism in materials which are subjected to a constant stress over a period of time [26]. This applied stress even being less than the yield strength, causes stress accumulation in the material

thus slowly deforming it and finally leading to failure. Creep is a major deformation phenomenon in metals which have a very high homologous temperature (T_h) [26]. Homologous temperature is defined as the ratio of current temperature (T) to the material melting temperature (T_m). The T_h of eutectic 63Sn-37Pb is $0.65T_m$ at room temperature ($T_m = 183^oC$), while the T_h of SAC 305 alloy is $0.61T_m$ at room temperature ($T_m = 217^oC$). Both of these homologous temperatures are well above the $0.5T_m$ acceptable range, and these alloys are considered to creep even at room temperature. Electronic components cycled over extreme temperature ranges (-55^{o}C to 125^{o}C) using a eutectic Sn-Pb solder have a $T_h = 0.51\text{-}0.87T_m$, while SAC 305 solder have a $T_h = 0.48\text{-}0.81T_m$. These high homologous temperatures suggest creep dependence of solders at high temperature dwells with failures due to strain energy accumulation and crack propagation while reliability testing.

There has been significant research on the strength, microstructure and reliability of SAC 305 alloys [27, 28, 29], and a lot of studies have reported the temperature dependent properties of creep, shear strengths, etc [30, 31, 32, 33, 34]

During thermal cycling, it is reported that microstructural coarsening and thermal fatigue reliability of SAC alloys is dependent on the distribution and morphology of Ag_3Sn intermetallic compounds within the solder [35, 36]. It was reported that with the increase in silver content, SAC alloy reliability increases (Figure 2.2). This behavior was due to the higher Ag content, which inhibits microstructural coarsening and increases solder fatigue life [15].

A number of studies have shown crack propagation in the solder near the pad/package-to-solder interface as the main cause of failure mode during thermal cycle testing. The crack initiates at the corner of the solder joint and propagates through the entire diameter of the solder ball (Figure 2.1) [37, 38].

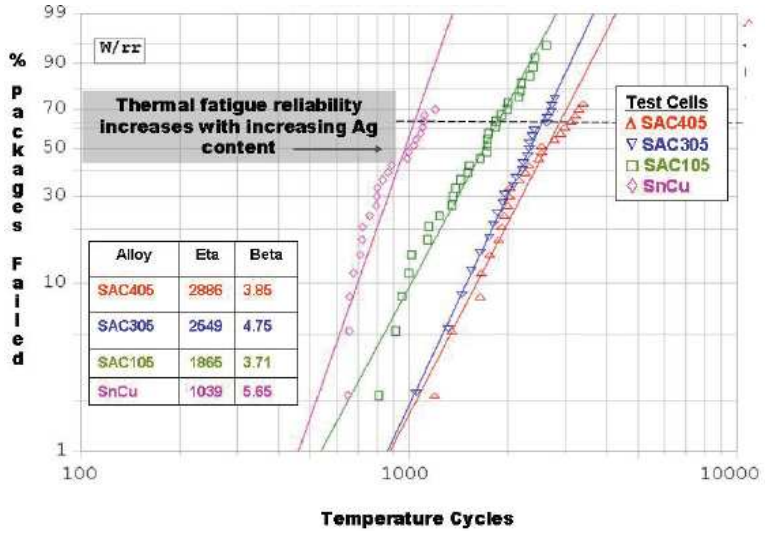


Figure 2.2: Weibull Plot Showing Thermal Cycling Reliabilty Dependence on Silver(Ag) Content for 2512 Chip Resistors [37]

2.2 Effect of Thermal Cycle Parameters

The effect of ramp and dwell times on acceleration factor during thermal cycle testing has been discussed in the literature [39, 40, 41]. Xuejun et al. [42] have studied the effect of dwell times and ramp rates on acceleration factor during thermal cycle testing. A BGA package built with SnAgCu 305 alloy was used and thermal cycle testing from -55^{o}C to 125^{o}C was performed. It was reported that with the increase in duration of dwell time, solder joint creep accumulation increases leading to earlier failure. It was reported that the solder joint life decreased significantly as the dwell times increased from 15 minutes, to 30 minutes, until 90 minutes with the same failure modes. It was reported that faster ramp rates impose more solder joint failures when compared to slower ramp rates with the larger temperature range (ΔT) causing more strain accumulation. It was reported that in between dwell times at high and low temperature, low temperature has more effect on solder failure. This was attributed due to the stress relaxation in the solder at the high temperature dwell.

Syed [29] has performed thermal cycle testing on various BGA packages assembled on a PCB with OSP surface finish. Three thermal cycling conditions were tested, and it was reported that -55^{o}C to 125^{o}C profile had the highest amount of failures. It was suggested

that the higher temperature range (ΔT) caused larger solder deformation when compared to lower temperature range (ΔT) during thermal cycle testing. When comparing alloys, the thermal cycling reliability of SAC 305/405 alloys was greater than Sn-Pb for all thermal cycle testing conditions. It was suggested that although joint reliability increased for SAC alloys, the degree of improvement is package and environment dependent.

With 2512 chip resistors (stiffer components), for a lower temperature thermal cycle testing range it was reported that SAC alloys outperform Sn-Pb, but as the temperature range increased Sn-Pb out performed SAC alloys. This behavior has been reported by others in the literature [38, 43, 44]. Due to the strong creep dependence of SAC alloys at relatively low stress levels corresponding to smaller temperature range, the SAC alloy will creep less than the Sn-Pb solders, but this trend may reverse as the applied stress (temperature range) increases. It is reported in the literature that the creep strain rate is proportional to the applied stress (MPa) raised to the power of n. For Sn-Pb, n is 2 [45], and for SAC alloys its between 11 and 18 [46].

Osterman et al. [47] have reported that at lower stress levels (1MPa) SAC alloys are more creep resistant than Sn-Pb alloys, where creep is primarily diffusion driven. But at higher stress levels the creep deformation is dislocation driven, which partly explains the higher acceleration factor in SAC alloys. It was reported that the cyclic life of SAC alloys is greater than Sn-Pb when the cyclic strain range is lower than the critical value (Figure 2.3). Performing thermal cycling reliability test with two different temperature ranges and different dwell times, it was concluded that with a 0-100^{o}C temperature range SAC was superior and in the 25-125^{o}C temperature range Sn-Pb was superior supporting the alloy creep dependence to the temperatures used. Components used were ceramic leadless chip carrier (CLCC) - stiffer components soldered to FR-4 board.

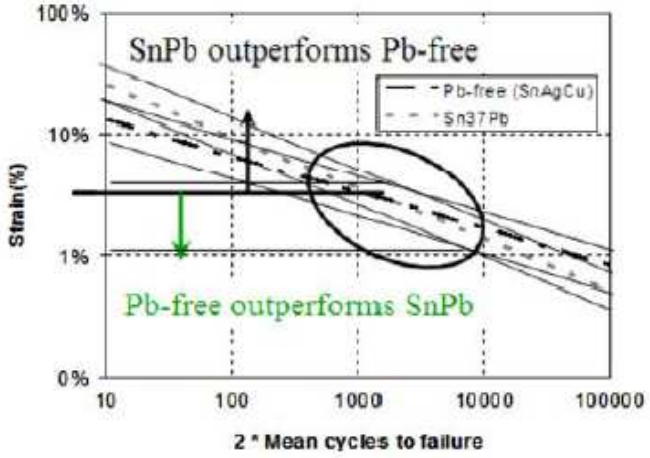


Figure 2.3: Cycles to Failure Vs Strain Rate [47]

2.3 Second Generation Lead-Free Alloys

With the widespread usage of portable electronics, the search for alloys that have both thermal cycle reliability and drop/shock reliability is important. Currently, a number of studies have been performed on second generation lead free solder alloys with additives like Bi, Ni, Cr, Ge etc. [17, 23, 48, 49, 50] which have shown both promising thermal fatigue life and drop/shock resistance.

Arnold et al. [51] have performed thermal cycle reliability test on Ni added solder paste for chip scale packages (CSP), thin small outline pack (TSOP) and chip resistors. Four different thermal profiles were used in this study. It was reported that using temperature cycles from -40^{o}C to 125^{o}C caused a greater amount of solder joint degradation when compared to the other profiles. It was shown that the acceleration factor of a nickel added solder paste is between that of SAC 305 and Sn-Pb with indications that this alloy was more effective at the higher temperature dwells. It was reported for the -40^{o}C to 125^{o}C thermal cycling condition the component failure follow this order: 2512 resistors ($N_{63\%}$ 628), CSP ($_{63\%}$ 867), and TSOP ($_{63\%}$ 1071). From the same study, by ranking the alloy performance for a given package type, it was shown that for the TSOP, the characteristic lives for all of the alloys

were the same. For CSP's, it was reported that SAC and Sn-Pb alloys have almost the same characteristic life with the nickel added paste outperforming both of them.

2.4 Drop/Shock Performance of SAC Alloys

As reported in the literature, SAC 305/405 alloys have lower performance in drop/shock testing when compared to SAC 105 alloys [11, 12]. The root cause of this performance is due to two factors.

The high Sn content and upto 4% Ag and 1% Cu, SAC 305/405 alloys have relatively higher strength and modulus and lower acoustic impedance (refer to Figure 2.4), and therefore under drop/shock they more readily transfer stress to the solder-substrate interface. The second factor is the growth of intermetallics. The intermetallic compounds (IMC) formed during soldering are of low ductility and it is this interface that exhibits brittle failure during testing (left image in Figure 2.5) [48]. Sometimes due to high strength of solder joints, during drop/shock testing the forces are transfered to the PCB resulting in cracking in the PCB (right image in Figure 2.5).

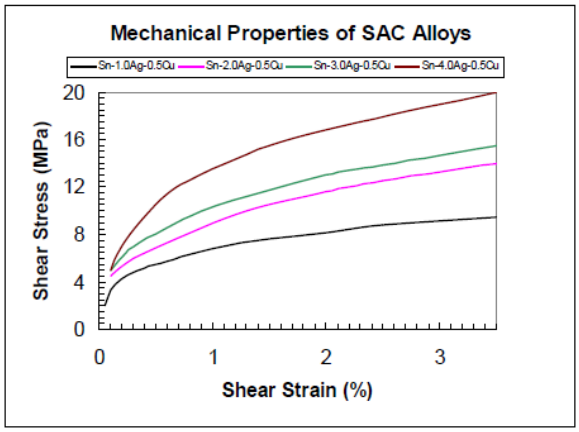


Figure 2.4: Mechanical Properties of Various SAC Alloys [52]

An approach to reduce the silver content in SAC alloys to make them more compliant, thus reducing stress transferred to weak interface (IMC) during drop/shock testing has been reported in the literature (refer to Figure 2.6) [23, 48]. Lowering the Ag content reduces the

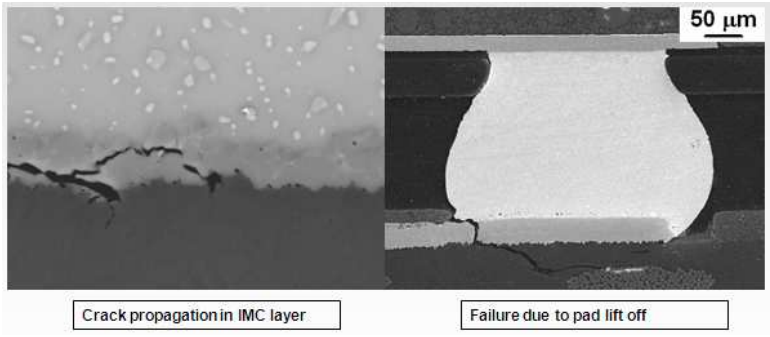


Figure 2.5: Failures During Drop/Shock Testing [53, 54]

formation of Ag_3Sn intermetallics in bulk solder which makes them more ductile and more drop/shock resistant.

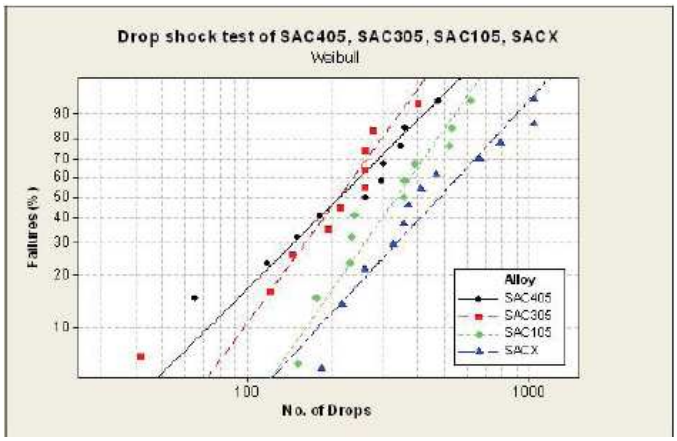


Figure 2.6: Weibull Plot Showing Drop/Shock Reliability Dependace on Silver(Ag) Content for BGA Packages [48]

Usage of various pad surface finish materials which promote reduction in IMC thickness are reported in the literature [55]. On a bare copper pad, intermetallic compounds Cu_6Sn_5 and Cu_3Sn are formed at the pad/package interface when using SAC alloys. It was reported in the literature that Cu_3Sn has a detrimental effect on drop/shock performance due to its brittle nature [48]. Intermetallic growth for various pad finishes using Sn-Pb and SAC alloys are shown in Table 2.1. Micro-structure view of intermetallic compounds as per Table 2.1 are shown in Figure 2.7.

ENIG - electroless nickel immersion gold, OSP - organic solder preservative

Paste	Bulk Solder	Bare Cu pad	ENIG pad	OSP pad
Sn-Pb	Cu_6Sn_5	Cu_6Sn_5, and Cu_3Sn due to high temperature	Ni_3Sn_4 and Ni_3P	Cu_6Sn_5 and Cu_3Sn
SAC	Ag_3Sn and Cu_6Sn_5	Kirkendall voids along Cu_3Sn	Ni_3Sn_4, $(Cu,Ni)_3Sn_4$ and $(Cu,Ni)_6Sn_5$	Ag_3Sn and Cu_6Sn_5

Table 2.1: IMC Growth For Various Pad Finishes [56, 57, 58]

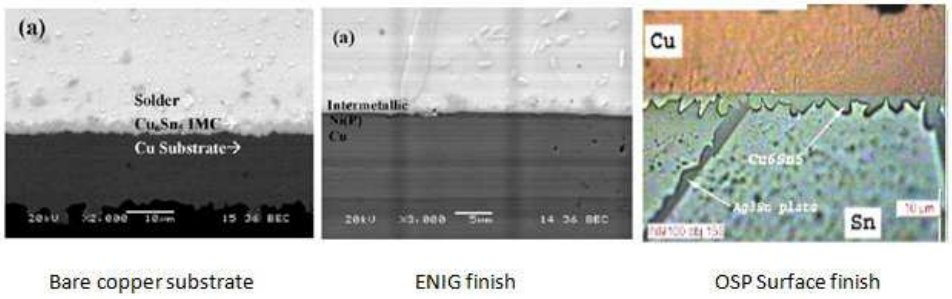


Figure 2.7: IMC Growth for Various Pad Finishes using SAC Alloys [59]

Currently, many studies have used dopant's like Mn, Ni, Ce, Ti which are reported to increase the drop shock reliability of low silver SAC alloys considerably [50].

2.5 Summary

The literature survey has shown the performance of various SAC alloys during thermal cycle and drop/shock testing. The effect of dwell time and ramp rates in thermal cycle tests on the reliability of SAC alloys has been discussed. It can be seen that the majority of the failures are in the bulk solder due to fatigue and creep. Due to the CTE mismatch between the components and the board, solder joint cracking was observed. This crack propagates through the entire ball diameter leading to failure. SAC 305 alloy performance in thermal cycle testing is package and environment dependent. In some cases Sn-Pb is superior in performance. The effect of adding Ni to Sn-0.7Cu alloy on its thermal cycle reliability has been discussed.

The thermal cycling behavior of nickel added paste for use with various SMT components is not fully documented in the literature. Very few topics related to whether the Ge-enhanced, Ni-modified Sn-0.7Cu solder, offers any advantage over SAC 305 in high temperature cycling are currently available. This work discusses these issues in detail.

Chapter 3

Experimental Test Setup

3.1 Introduction

The objective of this work was to conduct accelerated thermal cycle (ATC) testing using a test vehicle to compare the performance of SAC 305, SAC 105, eutectic Sn-Pb and Nihon Sn/0.7Cu/0.05Ni/Ge (Sn100C) alloys. The test vehicle was assembled with land grid arrays (LGA), quad flat no leads (QFN) and 2512 chip resistors. The above components were chosen to represent different solder joint configurations and stress levels during thermal cycling.

3.2 Component Design

3.2.1 Resistors

For this experiment 2512 chip resistors as shown in the Figure 3.1 were used.

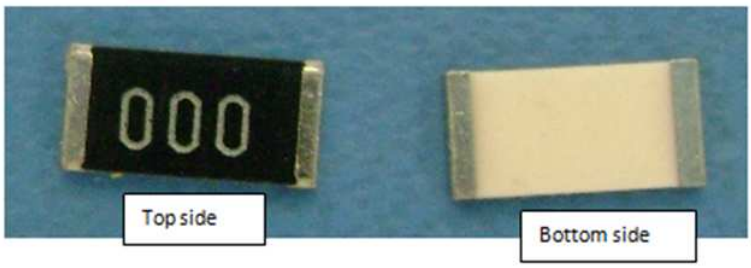
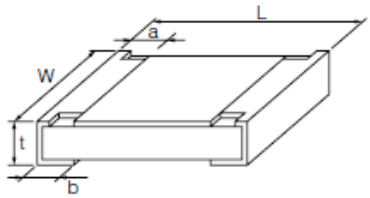


Figure 3.1: Resistor Top and Bottom View

Resistor package dimensions are shown in Figure 3.2 [60].



Length L (mm)	Width W (mm)	I. electrode a (mm)	O. electrode b (mm)	Thickness t (mm)
6.40 +/- 0.20	3.20 +/- 0.20	0.65 +/- 0.20	0.60 +/- 0.20	0.60 +/- 0.10

Figure 3.2: Resistor Dimensions

Using Orcad Layout, a 2512 chip resistor footprint was generated (refer to Figure 3.3) [60, 61, 62, 63]. Length, width and spacing as shown in Table 3.1 were used to create pad footprints.

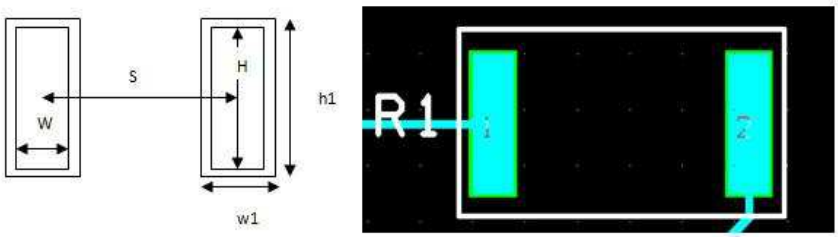


Figure 3.3: Chip Resistor Pad Dimension Notation (left), Resistor Footprint on PCB (right)

NSMD: non-solder mask defined (refer to Figure 3.4)

Height H in mm	Width W in mm	Pitch S in mm	Solder mask w1 in mm	Solder mask h1 in mm
3.2 (126 mils)	1 (39 mils)	6.2 (244 mils)	1.17 (46 mils) NSMD Pad	3.37 (133 mils) NSMD pad

Table 3.1: Resistor Pad Dimensions

The width of the trace was 4 mils, less than 1/2 times the pad dimension as recommended [64].

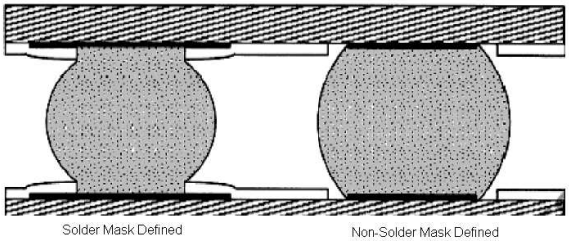


Figure 3.4: SMD Pads Vs NSMD Pads [65]

3.2.2 Land Grid Arrays (LGA)

For this experiment a CTBGA (12X12 mm 228) package as shown in Figure 3.5 was used. This package is a low profile plastic land grid array (without solder balls), with three perimeter row pads having an electroless nickel/ immersion gold (ENIG) surface finish. LGA's were used for this experiment due to the inability to obtain BGA's with Nihon alloy solder balls.

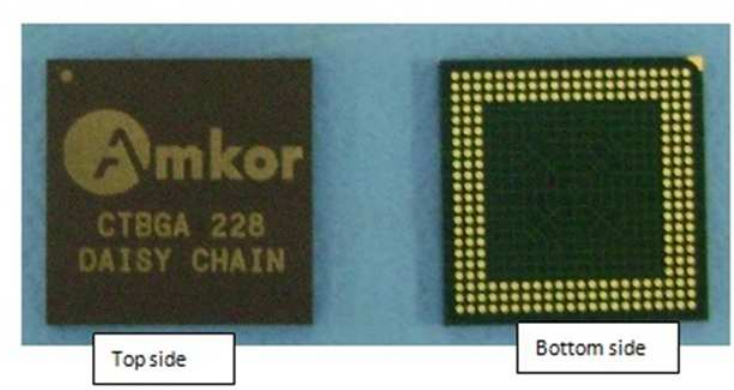


Figure 3.5: CTBGA Front and Back View

LGA package dimensions are shown in Figure 3.6 and Table 3.2.

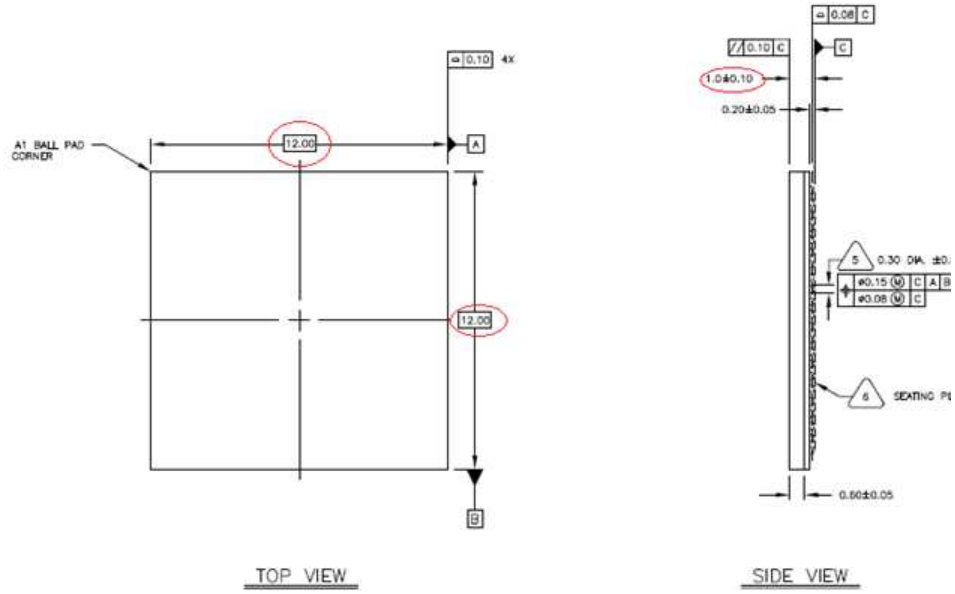


Figure 3.6: CTBGA Package Dimensions

Package length in mm	Package width in mm	Package thickness in mm
12 (473 mils)	12 (473 mils)	1 (40 mils)

Table 3.2: CTBGA Package Dimensions

Using Layout, a LGA footprint was created (refer to Figure 3.7) from the dimensions as shown in Table 3.3. After placing the footprint on the PCB, the daisy chain pattern as shown in the Figure 3.8 was created for continuous resistance monitoring purposes.

Pitch in mm	Diameter in mm	Solder mask NSMD	Pad to package end in mm
0.5 (20 mils)	0.3 (12 mils)	0.1 (4 mils)	0.75 (30 mils)

Table 3.3: CTBGA Pad Dimensions

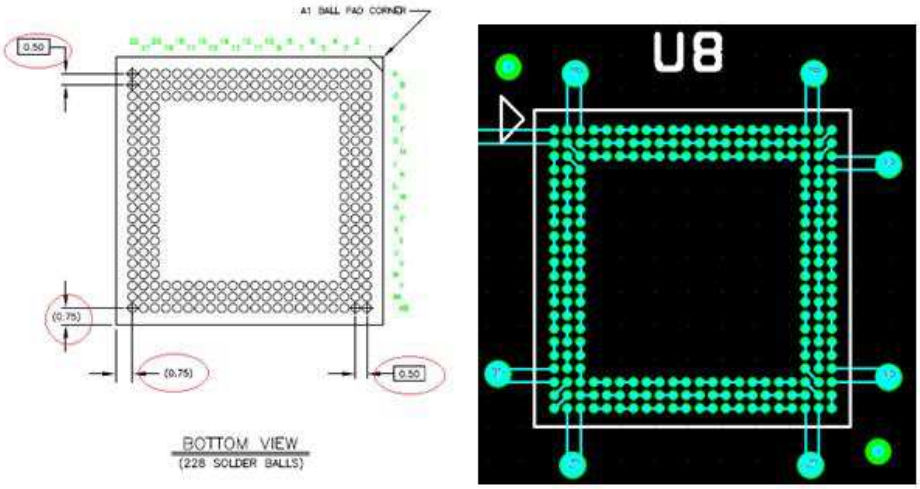


Figure 3.7: Pad Dimensions (left), CTBGA on PCB with Daisy Chain Pattern (right)

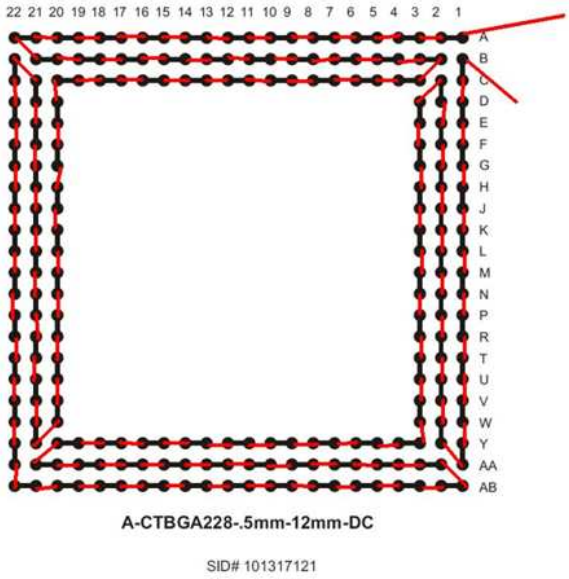


Figure 3.8: CTBGA Daisy Chain Pattern

The width of the trace was 4 mils, less than 1/2 times the pad diameter as recommended [64].

3.2.3 Quad Flat No Leads (QFN)

A QFN (MLF 8X8 mm 56) package with tin (Sn) surface finish as shown in the Figure 3.9 was used.

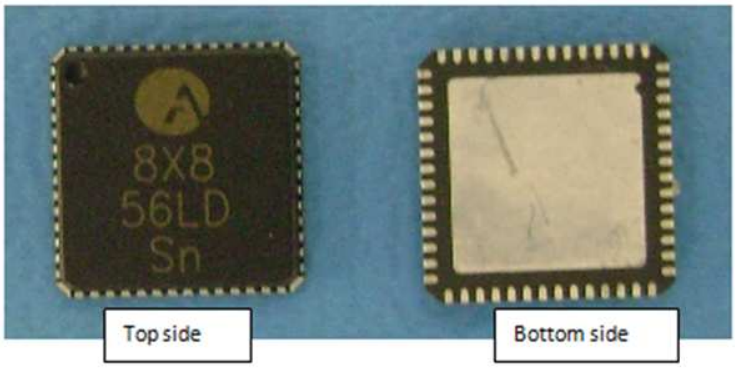


Figure 3.9: QFN Front and Back View

QFN package dimensions are shown in Figure 3.10 and Table 3.4.

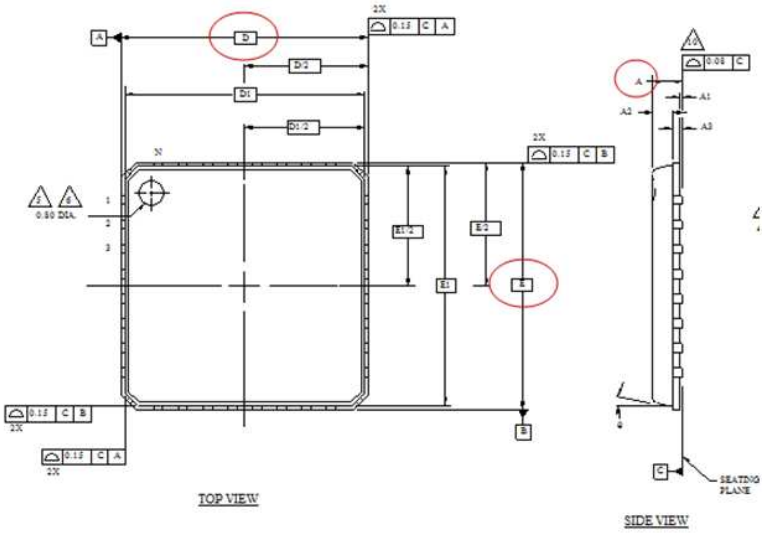


Figure 3.10: QFN Package Dimension Notation

Package length (D) in mm	Package width (E) in mm	Package total thickness (A) in mm
8 (320 mils)	8 (320 mils)	0.85 (34 mils)

Table 3.4: QFN Package Dimensions

In QFN packages, the die pad and the I/O pads are made from a planar copper lead-frame. The corresponding lands on the PCB should be designed accurately to fit the package I/O pads. Along with this, the exposed die pad, called a thermal pad, needs to be soldered to the PCB. This provides a direct path for heat removal from the die [66].

The length of the QFN pads on the PCB should be 0.2 mm longer than the package I/O pads. As per the specification it was 0.49 mm, adding 0.2 mm tolerance makes the final pad length to be 0.69 mm [67, 68, 69]. The pad width on the PCB should match the package I/O pad width. As per the specification it was 0.28 mm. The thermal pad should match with the exposed die pad. Based on the width and length of I/O pads, thermal pad dimension were calculated using geometry based on the Figure 3.10. These dimensions may not match with that of datasheet values.

While designing a non-solder mask design (NSMD) pad, for the solder mask to stick, it's minimum width or length should be 120 to 150 μm, and a design clearance of 60 to 75 μm between the copper pad and the solder mask should be maintained, A 140 μm thick solder-mask was designed giving a clearance between pads of 80 μm [67, 68, 69]. For packages which have thermal pad dimensions near the maximum available, a SMD type of thermal land is preferred. The mask opening should be approximately 100 μm smaller than the thermal land on all four sides to increase the distance between the thermal pad and the I/O lands. Using Orcad Layout, QFN footprints were generated as shown in Figure 3.11. The final pad dimensions used for the design are given in Table 3.5

Pitch e in mm	Width b in mm	Length l in mm	Thermal pad D2 and E2 in mm	Solder mask overall width in mm
0.5 (20 mils)	0.28 (11.2 mils)	0.69 (27.6 mils)	5.54, 5.54 (221.6 mils)	0.140 (5.6 mils)

Table 3.5: QFN Pad Dimensions

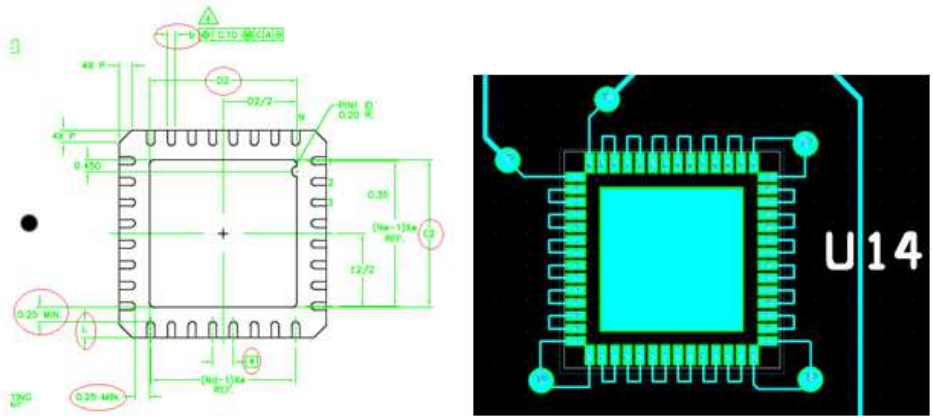


Figure 3.11: Pad Dimensions (left), QFN Package on PCB with Daisy Chain Pattern (right)

Rectangle pads were chosen for the land pattern design after discussions with the board manufacturer and part supplier (refer to right image in Figure 3.11). The width of the trace was 4 mils, less than 1/2 times the pad width as recommended [64].

3.2.4 Other Components

Connector

All of the components on the PCB were connected to the connector holes located on the ends of the board. Later these connector holes were connected to a resistance monitoring system during the thermal cycling experiment. A connector available with the standard Orcad library was used, and its dimensions were modified to suit the given purpose. The final dimensions used for designing the footprint are given in Table 3.6. The pad footprints are shown in Figure 3.12.

Hole dia in mm	Annular ring clearance	Ground/power clearance	Solder mask mm	Pitch in mm
1.01 (40 mils)	0.5 (20 mils)	1.01 (40 mils)	0.178 (7 mils)	2.54 (100 mils)

Table 3.6: Connector Pad Dimensions

Annular ring clearance was 20 mils on the top and bottom surfaces [64]. So, the hole diameter on the top and bottom surfaces was 40+20=60 mils. Ground and power planes

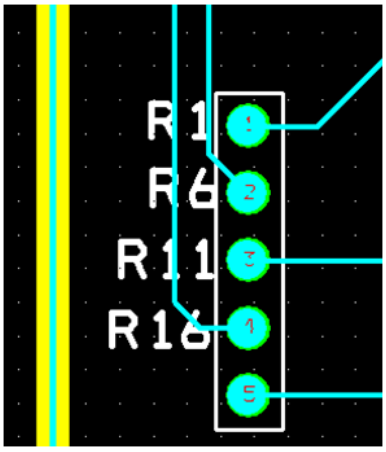


Figure 3.12: Component Connector Holes Located on Board Sides

should have an annular ring clearance+20 mils [64]. So, total diameter on the ground and power planes was 80 mils. The width of the trace was 4 mils.

Fiducials

During component assembly, fiducials serve as a reference point and help in aligning the PCB with the machine axis. They also serve as the board origin in CAD data files, with component locations calculated from them. In addition to global fiducials, local fiducials are used for fine pitch components to improve placement accuracy with their locations at the corners of the packages [61]. Three global fiducials to identify the board and 16 local fiducials to identify the 8 LGA packages were used. Fiducial footprints are shown in Figure 3.13 and the pad dimensions used are given in Table 3.7.

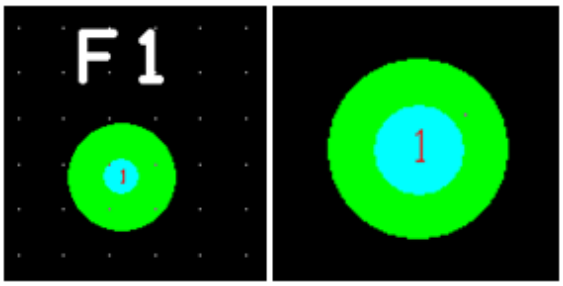


Figure 3.13: Global Fiducials for Identifying Board (left), Local Fiducials for Identifying LGA Package (right)(image enlarged)

Global Fiducials		Local Fiducials	
Diameter in mm	Solder mask (mm)	Diameter in mm	Solder mask (mm)
1.106 (40 mils)	3.04 (120 mils)	0.5 (20 mils)	1.106 (40 mils)

Table 3.7: Fiducial Pad Dimensions

Solder mask clearance for global fiducials was 80 mils, making the entire fiducial diameter 120 mils [61, 64]. Solder mask clearance for local fiducials was 20 mils, making the entire fiducial diameter 40 mils.

Test Points

Test points are placed for each component of the PCB to measure its continuity after board assembly (refer to Figure 3.14). Solder mask clearance used was 5 mils, making the entire test point pad diameter 42 mils (refer to Table 3.8).

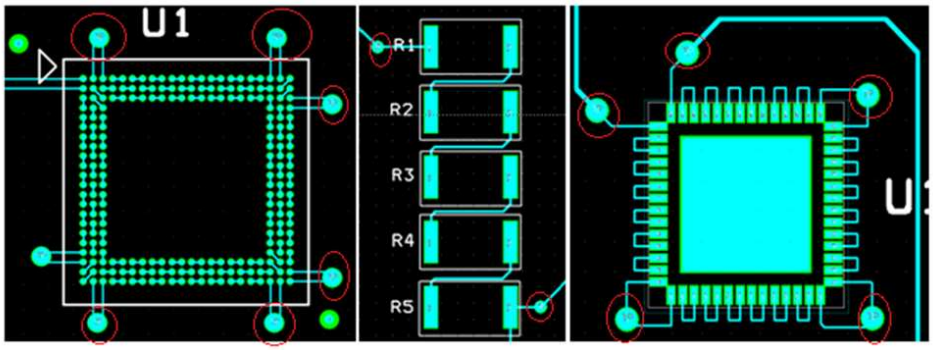


Figure 3.14: LGA with Test Points (left), Resistor Chain with Test Points (center), QFN with Test Points (right)

Diameter in mm	Solder mask mm
1 (37 mils)	1.5 (42 mils)

Table 3.8: Test Point Pad Dimensions

3.3 Board Design

3.3.1 Orcad Layout

Cadence ORCAD Layout software was used to design the test vehicle. Layout is a CAD based software used to design the physical representation of circuits on the PCB. Package footprints are placed inside the board outline and are connected using netlists. Netlists are converted into traces and the total board gerber data was generated using post-processing options. Along with the CAD functionality, layout acts like a frontend CAM software by generating various design (gerber) files which help in manufacturing a physical PCB.

3.3.2 Test Vehicle Description

A four layer board with total thickness of 60 mils was designed and manufactured for the purpose of this experiment. 2512 resistors, QFN and LGA components were assembled on the board (refer to Table 3.9 for quantities used). Every pad on the PCB is a non-solder mask defined (NSMD) pad with an OSP surface finish (refer to Figure 3.4). The test vehicle was 8.75 inch long and 5 inch wide (refer to the Figure 3.15 for complete board dimensioning).

Component name	Total Quantity used per board
LGA	8
QFN	4
2512	20

Table 3.9: Packages Used and their Quantity per Board

LGA and QFN packages were supplied internally daisy chained by the manufacturer. By creating a corresponding pattern on the PCB, a complete electrical path was created and the resistance could be monitored during thermal cycling.

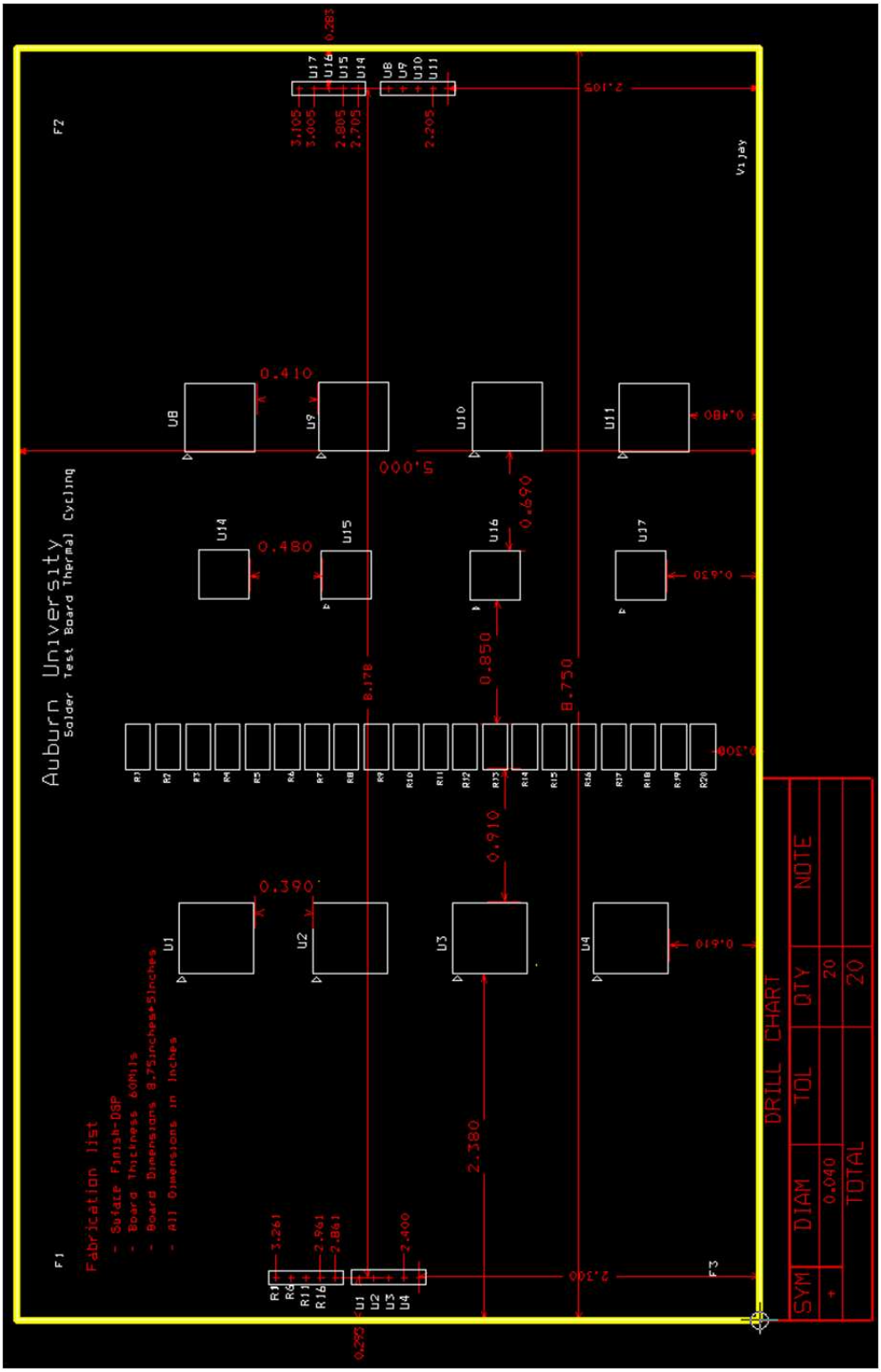


Figure 3.15: Solder Test Vehicle with Complete Dimensions

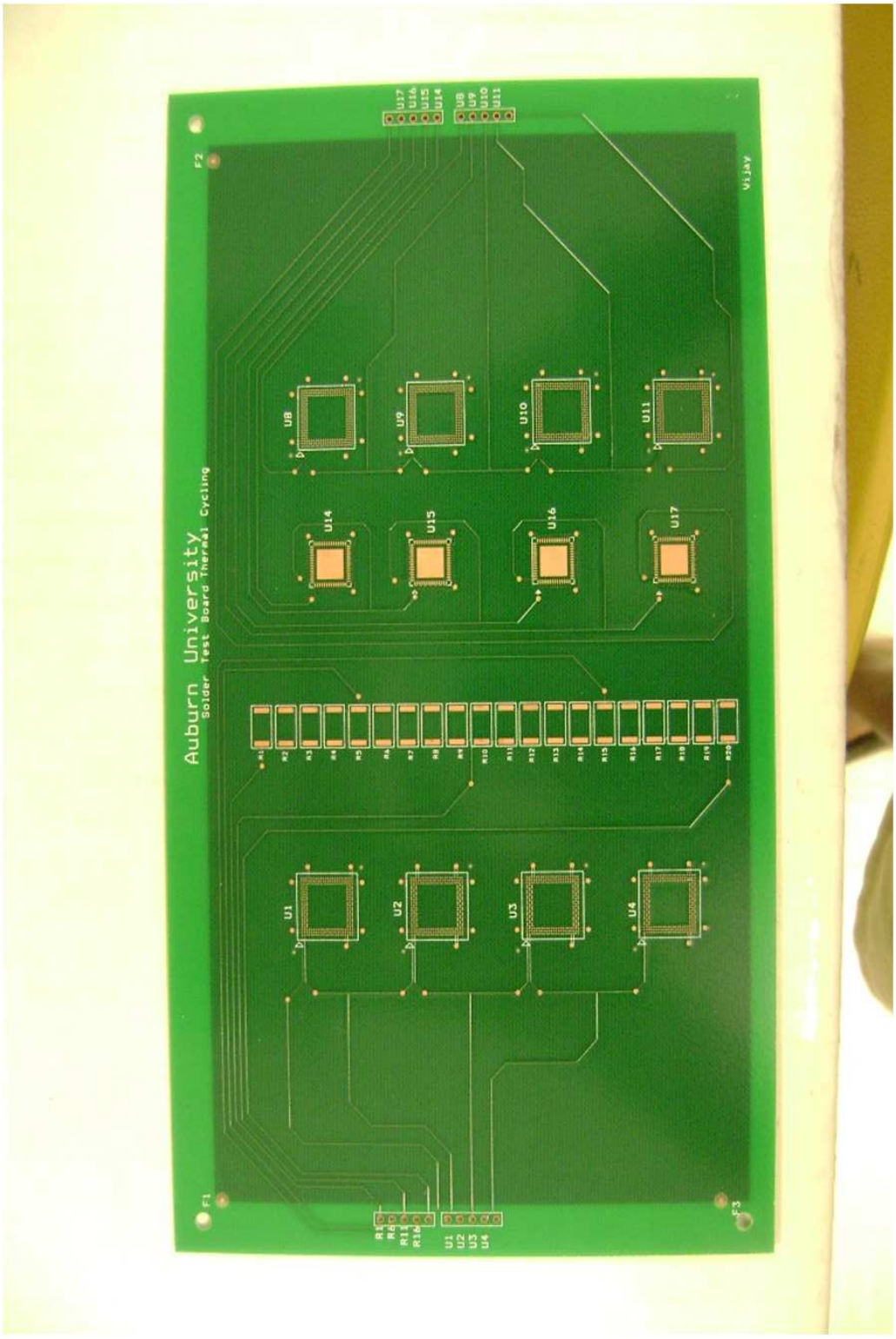


Figure 3.16: Test Vehicle PCB

3.4 Stencil Design

Stencils have openings to match the land patterns on the PCB where solder needs to be deposited. Using a printing machine and stencil, solder paste is applied to the PCB.

3.4.1 QFN Stencil Design Guidelines

The reflow solder joints on the perimeter pads should have a standoff height of about 2 mils to 3 mils [69]. The ratio of stencil aperture size to land size should be typically a 1:1 ratio. It is suggested that when using a finer pitch package (0.4 mm or less) the thickness of the stencil should be reduced to prevent solder bridging.

The thermal pad should be sectioned into smaller areas to reduce void formation, and to provide an uniform stencil pressure at all points on the package lands [66, 70]. A larger opening in thermal pad region allows for scooping to occur during screen printing thus leading an uneven paste deposit. The segmentation should be in such a way that the entire area of solder paste on the pad is between 50 to 80% of the pad area.

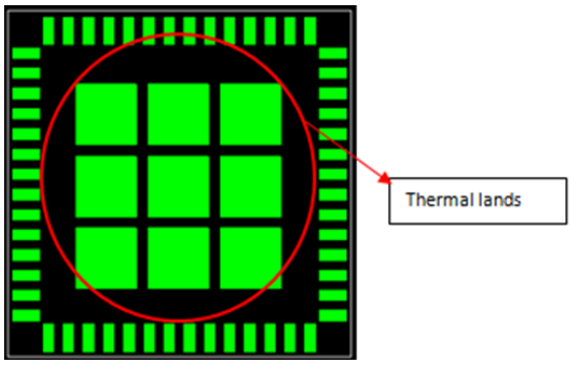


Figure 3.17: QFN Package Thermal Land on the Stencil

Studies have show that spacing between segments on the stencil should be 0.15 mm or more [68]. For the experiment it was designed at 0.35 mm. Narrower spacings between the segments can become a manufacturing issue and should be avoided. It was suggested to use a separation gap of 0.75 mm between I/O pads and the thermal pads on all sides to reduce the incidences of bridging [66].

3.4.2 Stencil Type and Thickness

A laser cut, stainless steel stencil with electro-polished trapezoidal walls was recommended [69]. Electro-polishing reduces the surface friction and helps in good paste release. Using a trapezoidal sectional aperture promotes a brick like solder paste release that assists in a firm component placement. A stencil thickness between 0.15 mm (6 mils) to 0.2 mm (8 mils) for packages with pitch greater than 0.5 mm is recommended [69]. Freescale [68] recommends a 5 mils thick stencil for 0.5 mm pitch packages and a 6 mil thick stencil for 0.65 mm pitch packages. Since there are various components on the PCB with different sizes and pitches, stencil thickness should always be calculated based on the overall area and aspect ratios of each component.

Area ratio is the ratio between the pad area to the stencil wall area and aspect ratio is the ratio of the aperture opening to the stencil thickness. These values should always be greater than 0.6 and 1.5, respectively for all the components on the board for a successful paste deposition. Figure 3.18 shows the area and aspect ratio values for all the components and stencil type used.

For this experiment a laser cut, stainless steel stencil with electro-polish finish was used. The stencil thickness was 5 mils.

- For LGA's, the stencil opening was that of its pad diameter (0.3 mm)
- For QFN's, the stencil opening was that of its pad dimensions (0.28 mm X 0.69 mm)
- The thermal land on QFN was segmented into 9 squares, each 1.52 mm X 1.52 mm. Separation of 0.35 mm between two squares on all sides was used.
- The resistor stencil opening was that of its land dimensions (3.2 mm X 1 mm)
- Using bare test-points during the assembly process would result in degradation so, solder was deposited on them. The opening in the stencil for these were 1 mm in diameter

L= length of the pad opening, W= width of the pad opening, T= thickness of the stencil, D= Diameter of the pad (circular pads for LGA).

Stencil Thickness	LGA Top		LGA Bottom		2512 Resistors		QFN Vertical oriented pads		QFN horizontal oriented pads	
	Area	Aspect	Area	Aspect	Area	Aspect	Area	Aspect	Area	Aspect
	D/4T	W/T	D/4T	W/T	(L*W)/ 2*T*(L+W)	W/T	(L*W)/ 2*T*(L+W)	W/T	(L*W)/ 2*T*(L+W)	W/T
5 Mils	0.6	2.4	0.5	2	2.97	2	0.78	7.8	0.78	5.4
6 Mils	0.5	2	0.4166	1.66	2.48	1.66	0.65	6.5	0.65	4.5

Figure 3.18: Area and Aspect Ratio Comparison for the Components

It can be seen from the Figure 3.18 that a 6 mil stencil violates the area ratio for the LGA packages.

3.5 PCB Fabrication Process Capability Study

The quality of the manufactured board is an important factor for its proper functionality and overall system reliability. Good quality boards increase the performance of the system and contribute toward an increased life expectancy. Process capability is the measure of how well a given process has performed and is measured statistically from the process outputs. In terms of board manufacturing, process capability is the measure of how well the manufactured board meets all the required limits and tolerances.

On the current test vehicle, there are 3 different pad dimensions with 3 different spacing's and all these dimensions were measured to check for the board process capability. Two boards were selected and 50 readings per board, for a given dimension, were measured with a microscope. A process capability study using Minitab was conducted. The manufacturing tolerances taken for this study were +/- 0.5 mils and a process variation was measured by 6 standard deviations (+/- 3 Sigma on each side of the mean).

2512 Resistors

Figures (3.20 - 3.22) present the process deviation for the 2512 resistor pads. Measured units on the graph are in mils and the values were rounded to the nearest number. The pads were designed to be 126 mils wide and 39 mils in length (refer to Figure 3.19), with a spacing between them of 204 mils. The process did not meet the required tolerances. The pad length and width were below the lower specification limit (LSL). Correspondingly, the pad-to-pad spacing was above the upper specification limit (USL).

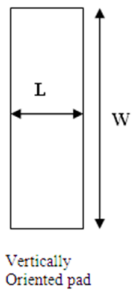


Figure 3.19: Pad Dimensioning Notation on 2512 Resistor

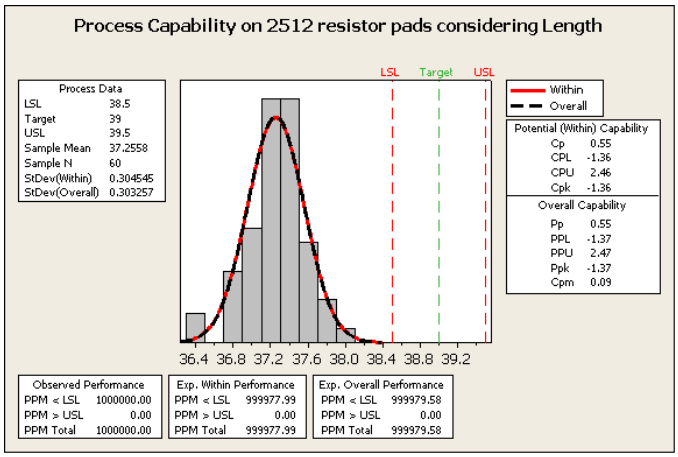


Figure 3.20: Process Capability on 2512 Resistor Pads Considering Length

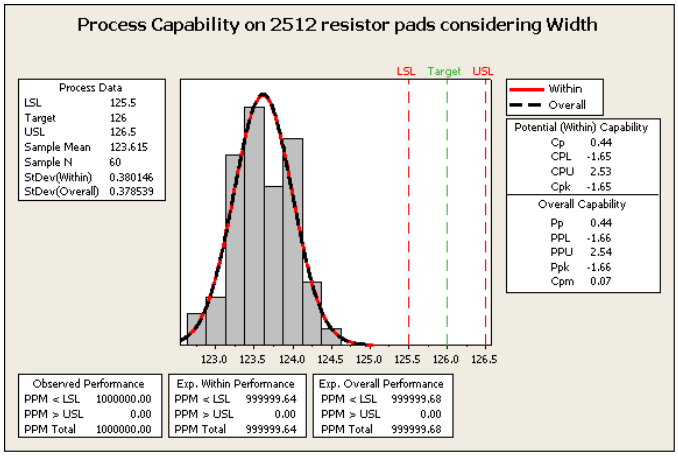


Figure 3.21: Process Capability on 2512 Resistor Pads Considering Width

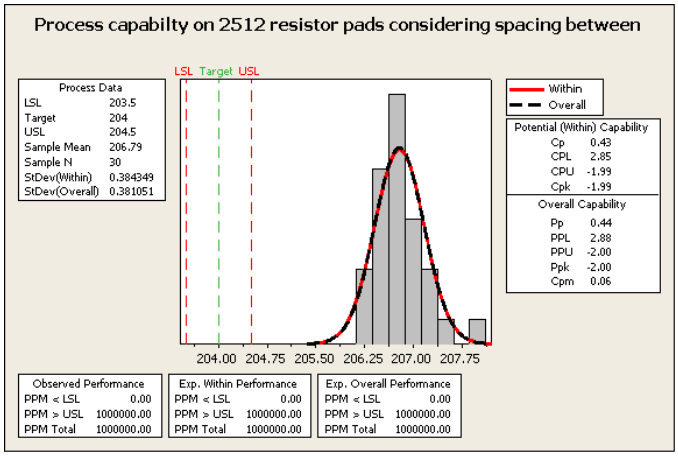


Figure 3.22: Process Capability on 2512 Resistor Pads Considering Spacing

QFN

Figures (3.24 - 3.29) plot the process variation of the QFN pads. The package consists of horizontal and vertical pads. In its horizontal orientation, the designed length of the pad was 27 mils and the width was 11 mils. In its vertical orientation, the designed length of the pads was 11 mils and the width was 27 mils (refer to the Figure 3.23). The spacing in between the two pads (not the pitch) was 8.66 mils.

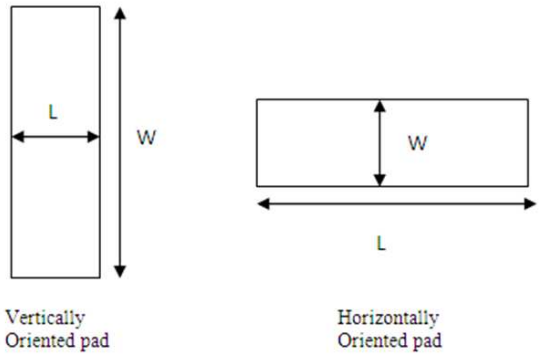


Figure 3.23: Pad Dimensioning Notation on QFN

The pad lengths and widths were below the lower specification limit (LSL) and the spacing was greater than the upper specification limit (USL). The manufacturing process didn't meet the required process tolerances.

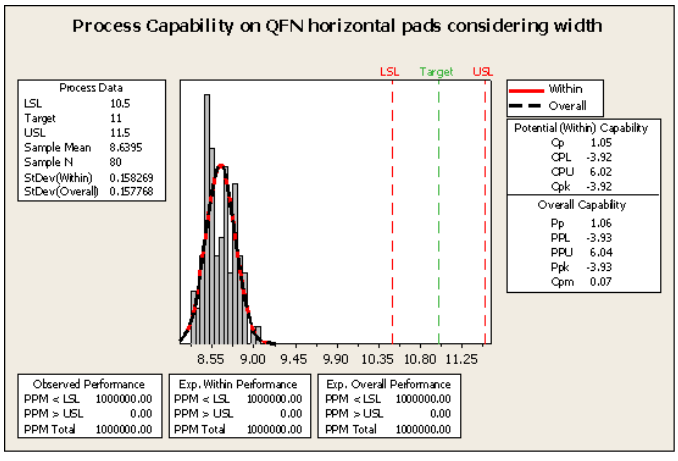


Figure 3.24: Process Capability on QFN Horizontal Pads Considering Width

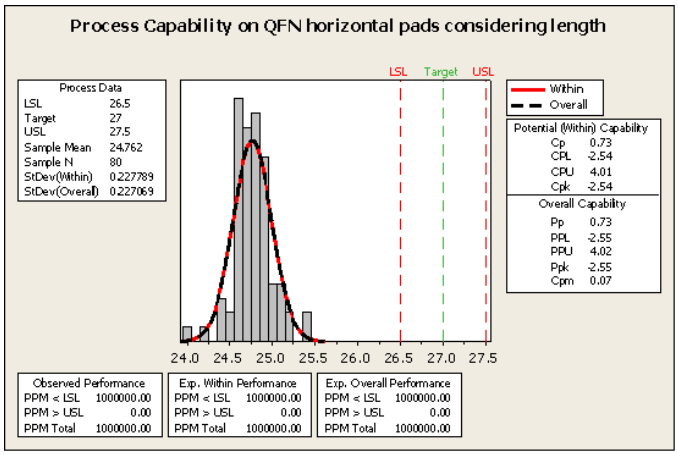


Figure 3.25: Process Capability on QFN Horizontal Pads Considering Length

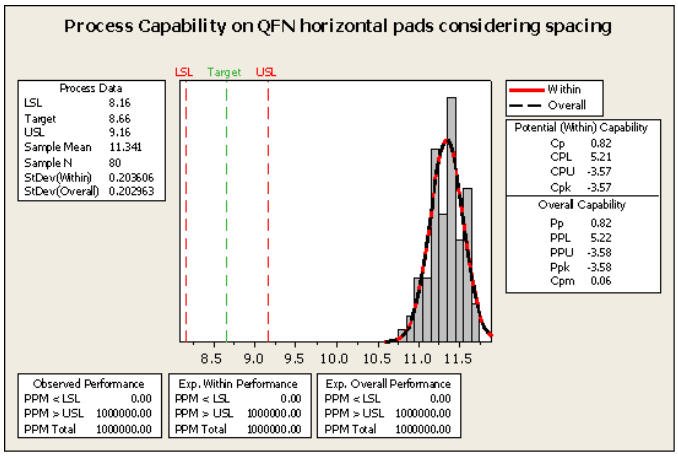


Figure 3.26: Process Capability on QFN Horizontal Pads Considering Spacing

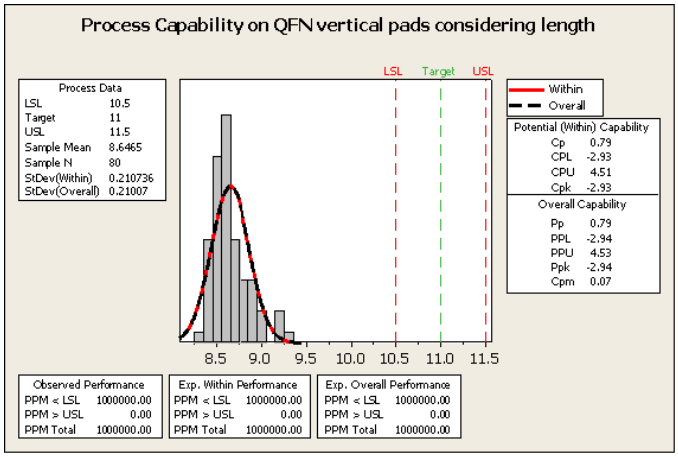


Figure 3.27: Process Capability on QFN Vertical Pads Considering Length

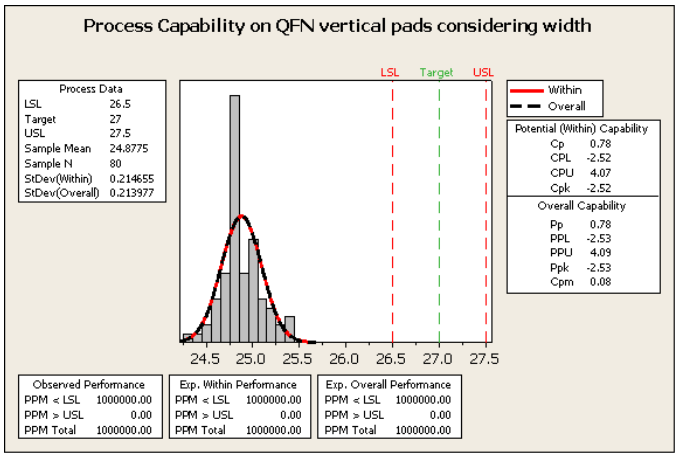


Figure 3.28: Process Capability on QFN Vertical Pads Considering Width

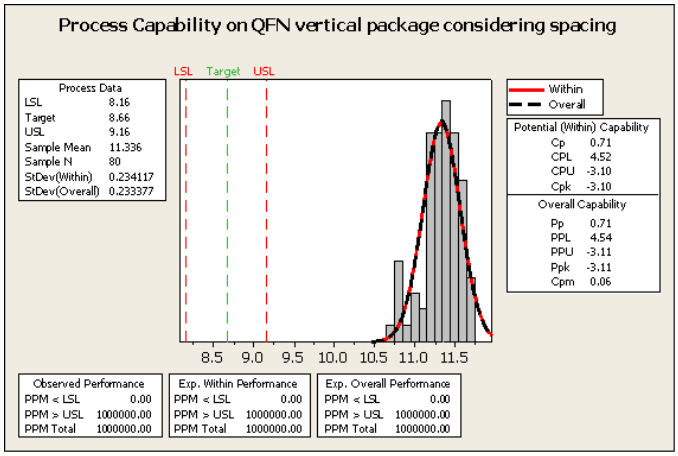


Figure 3.29: Process Capability on QFN Vertical Pads Considering Spacing

LGA

Figure 3.30 shows the process variation for the LGA pads. This package consists of circular pads with a diameter of 12 mils. The measured pad dimensions were below its lower specification limits (LSL).

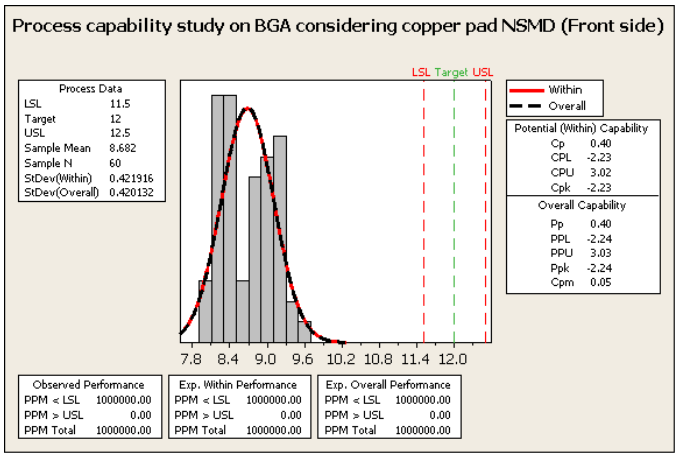


Figure 3.30: Process Capability on LGA Pads Considering Diameter of Pad

Conclusions

From all the process capability plots, the process for the pad sizes was not centered on the target, most of the pads are smaller than the target and the whole normal distribution was shifted below the lower specification limits (LSL). Nominally all of the pads were smaller by 2 to 4 mils than their target. The spacing was too not centered on the target. Most of the spacing measurements are larger than the target, and the whole normal distribution was greater than the upper specification limits (USL). For both the pads and spacing measurements, the Cpk values are less than 1 indicating the process capability did not meet the required specifications.

3.6 Component Assembly

In a typical surface mount manufacturing process, the PCB is deposited with sufficient solder paste using a solder printing machine, and then the solder paste is inspected for any deficiencies. A pick and place machine places the components on the PCB and finally a reflow oven is used to melt the solder, making a good joint between the component and PCB board.

3.6.1 Solder Paste Inspection Data Analysis

After solder paste printing, boards are measured for solder paste area and volume using an inspection machine. Using laser technology, solder inspection machines give solder joint area, volume and height as outputs. Understanding the amount of paste on a particular pad is very important as it serves to reduce the total number of defect going into an assembly process.

For this analysis solder paste volume, area and height were taken as response variables and box plots were constructed to see the spread of each parameter over 8 boards. Figure 3.31 shows solder height on 2512 resistor pads for 8 boards build using the Nihon paste. The measured solder height on the resistor pads was well within the required pass/fail thresholds.

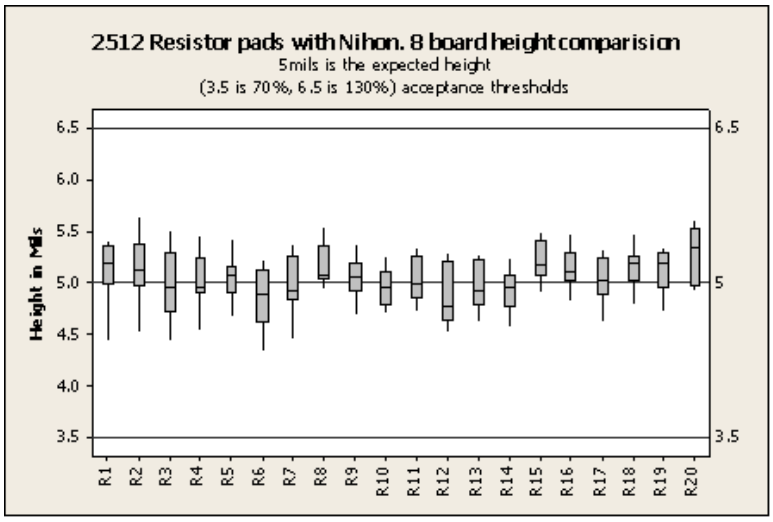


Figure 3.31: Resistor with Nihon. 8 Board Height Comparisons

Figure 3.32 shows solder area on resistor pads for 8 boards build using the Nihon paste. Expected area with 100% stencil opening was 4914 Sq mils. The measured solder area on the resistor pads was well within the required pass/fail thresholds.

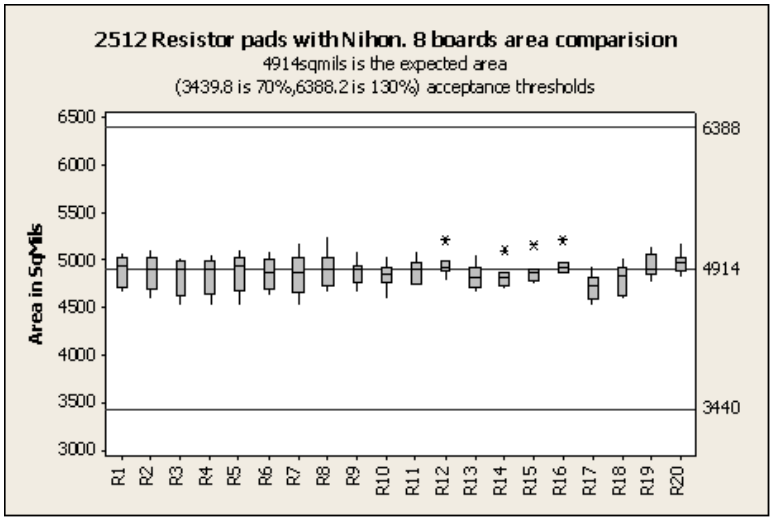


Figure 3.32: Resistor with Nihon. 8 Board Area Comparisons

Figure 3.33 shows solder volume on resistor pads for 8 boards build using the Nihon paste. Expected paste volume was 1485 cubic mils. The measured solder volume on the resistor pads is well within the required pass/fail thresholds.

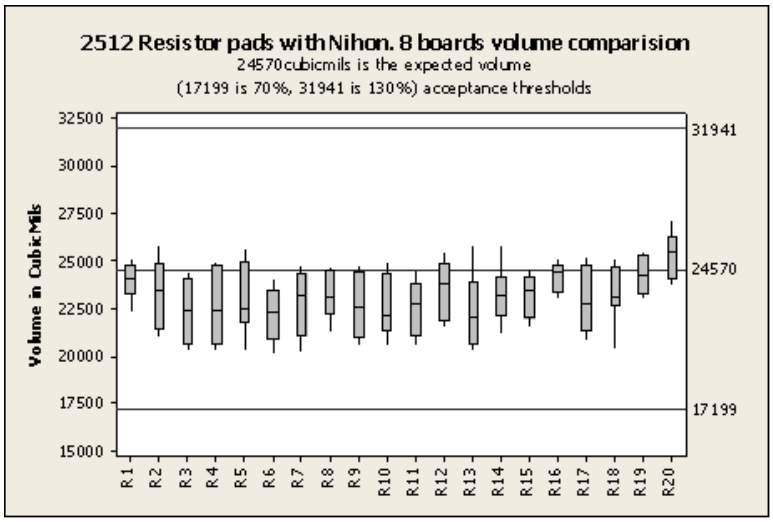


Figure 3.33: Resistor with Nihon. 8 Board Volume Comparisons

3.6.2 Board Reflow Parameters

Reflow profiles are paste dependent and should be designed keeping in mind the paste alloy and rheological properties. A typical reflow profile is divided into four zones: A preheat zone to dry off the volatiles from the paste, a soak zone to bring the temperature of board uniformly to below reflow temperatures, a reflow zone to melt the solder and finally a cool down for solidification of the newly formed solder joint. The process variables shown in the Figures 3.34, 3.36, 3.38, 3.40 were used to generate reflow profiles for the respective solder pastes.

Sn-pb process variables [71, 72, 73]

Paste name: Kester Sn-Pb	Low Limit	High Limit	Units
Maximum rising slope (target 1.0) calculate slope over 20 seconds	0.0	2.0	degrees/second
Slope 1 (target 1.0) Between 150 to 215 (calculate slope over 50 seconds	0.0	2.0	degrees/second
Max falling slope (calculate slope over 20 seconds)	-6.0	-1.0	degrees/second
Soak time 100-150C	60	120	seconds
Time above reflow 183C	60	90	seconds
Peak temperature	210	220	degrees Celsius
Total time above 210C	10	20	seconds

Figure 3.34: Sn-Pb Paste Reflow Parameters

Sn-Pb Reflow Profile

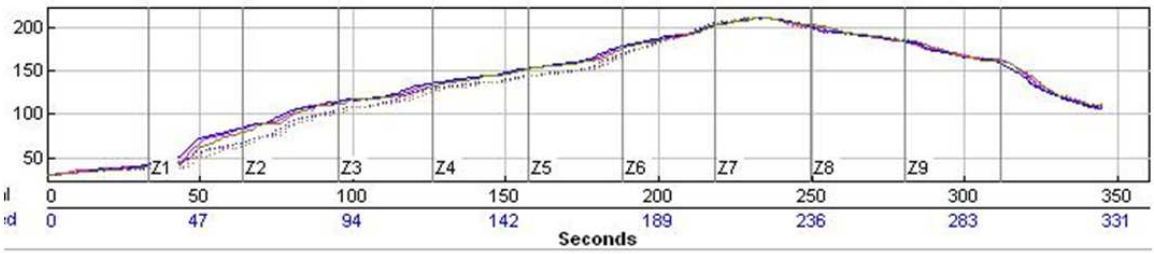


Figure 3.35: Sn-Pb Paste Reflow Profile

SAC 305 process variable [74, 73]

During reflow an inert environment (Nitrogen gas) was used for this paste.

Paste name: Heraeus SAC 305	Low Limit	High Limit	Units
Maximum rising slope (target 1.0) calculate slope over 20 seconds	0.0	2.0	degrees/second
Slope 1 (target 1.0) Between 150 to 240 (calculate slope over 50 seconds	0.0	2.0	degrees/second
Max falling slope (calculate slope over 20 seconds)	-6.0	-1.0	degrees/second
Soak time 130-165C	60	120	seconds
Time above reflow 217C	30	50	seconds
Peak temperature	230	255	degrees Celsius
Total time above 235C	10	20	seconds

Figure 3.36: SAC 305 Paste Reflow Parameters

SAC 305 Reflow Profile

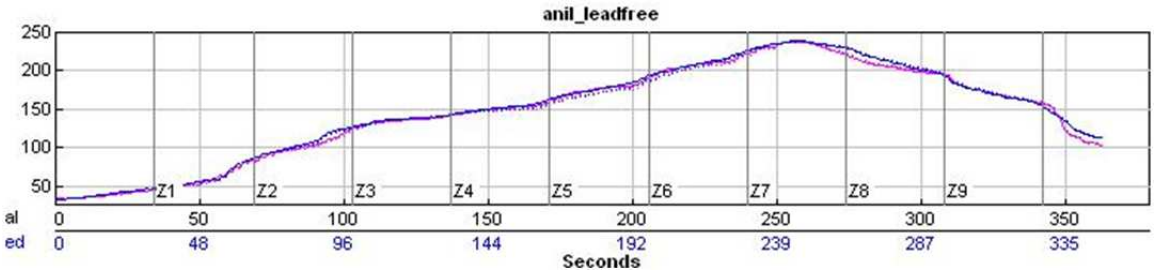


Figure 3.37: SAC 305 Paste Reflow Profile

SN100C Nihon Process variables [75]

Paste name: Nihon SN100C	Low Limit	High Limit	Units
Maximum rising slope (target 1.8) calculate slope over 20 seconds	1.5	2.0	degrees/second
Slope 1 (target 1.8) Between 25 to 227 (calculate slope over 50 seconds	1.5	2.0	degrees/second
Max falling slope (calculate slope over 20 seconds)	-3.0	-1.0	degrees/second
Time above reflow 227C	40	60	seconds
Peak temperature	235	245	degrees Celsius
Total time above 235C	10	30	seconds

Figure 3.38: SN100C Paste Reflow Parameters

SN100C Reflow Profile

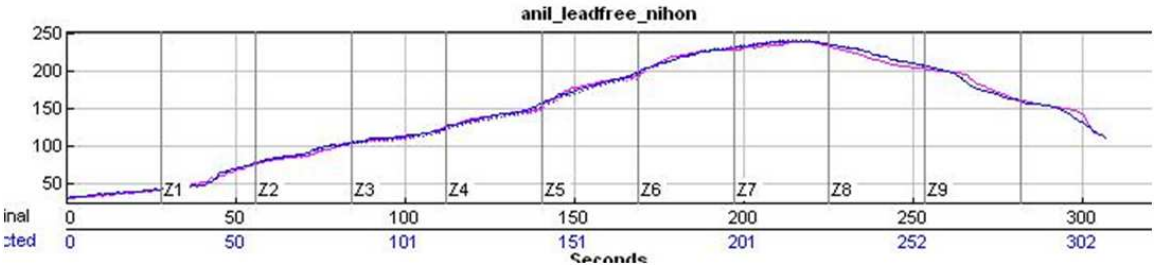


Figure 3.39: SN100C Paste Reflow Profile

SAC 105 process variables [76, 77]

During reflow an inert environment (Nitrogen gas) was used for this paste.

Paste name: Heraeus SAC 105	Low Limit	High Limit	Units
Maximum rising slope (target 1.8) calculate slope over 20 seconds	1.5	2.0	degrees/second
Slope 1 (target 1.8) Between 25 to 227 (calculate slope over 50 seconds	1.5	2.0	degrees/second
Max falling slope (calculate slope over 20 seconds)	-3.0	-1.0	degrees/second
Time above reflow 227C	60	100	seconds
Peak temperature	230	250	degrees Celsius
Total time above 235C	10	30	seconds

Figure 3.40: SAC 105 Paste Reflow Parameters

SAC 105 Reflow Profile

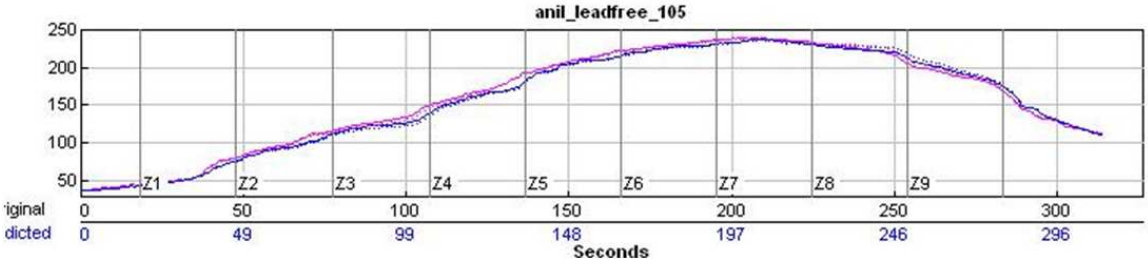


Figure 3.41: SAC 105 Paste Reflow Profile

Figure 3.42 shows the final assembled board after the reflow process. The electrical continuity of the attached components was verified by hand probing the test points with an ohmmeter.

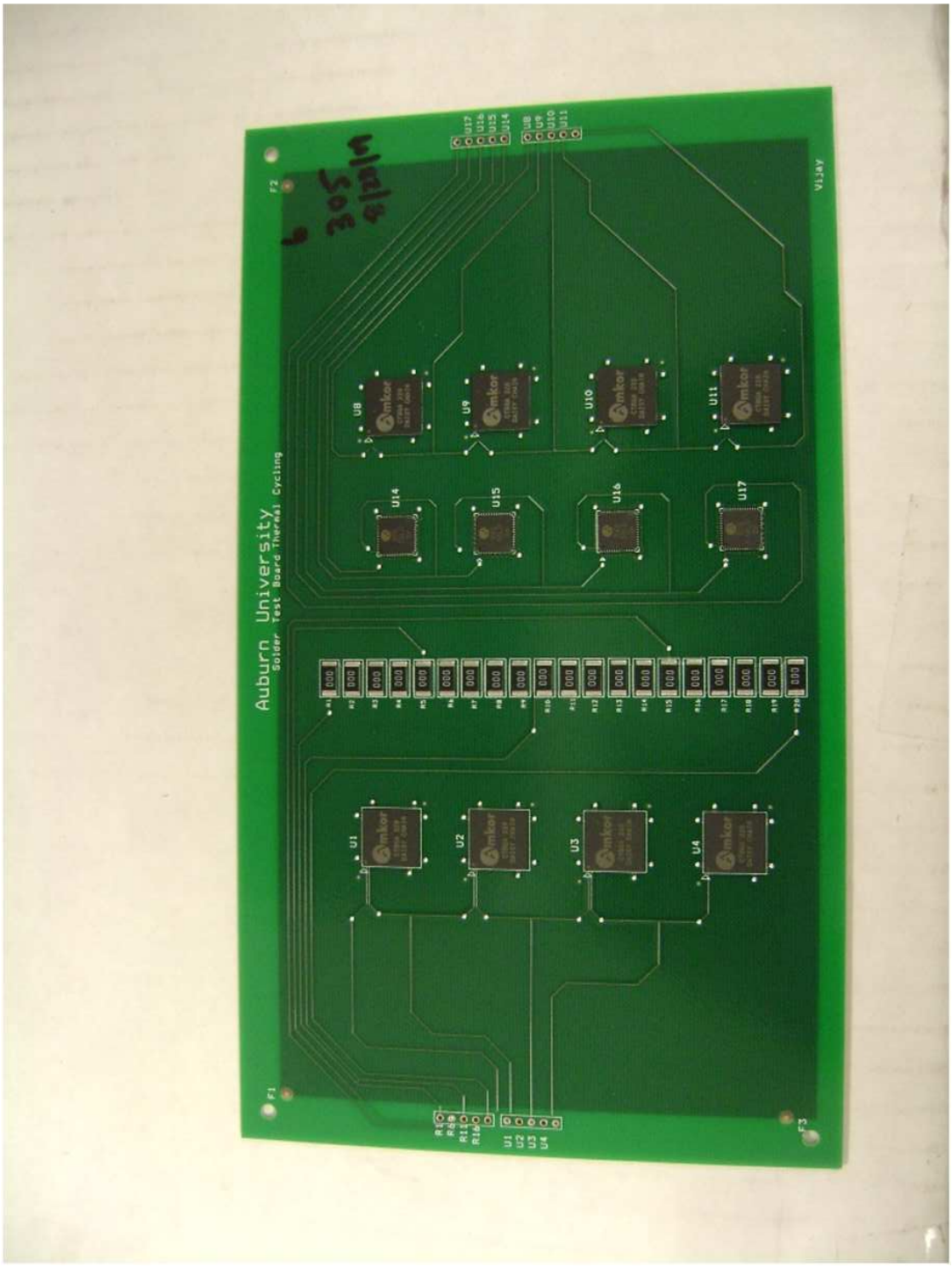


Figure 3.42: Solder Test Vehicle with Components Assembled

3.7 X-ray Analysis

The assembled board was viewed under X-ray to study the solder joint formation. Figure 3.43 shows solder joint formation between the PCB and the chip resistor.

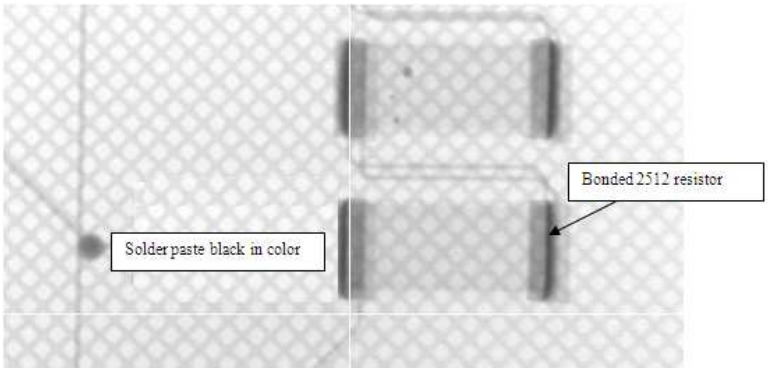


Figure 3.43: 2512 Resistor X-ray Image

Figure 3.44 shows solder joint formation between PCB and QFN chip. A few voids were observed in the thermal pad area.

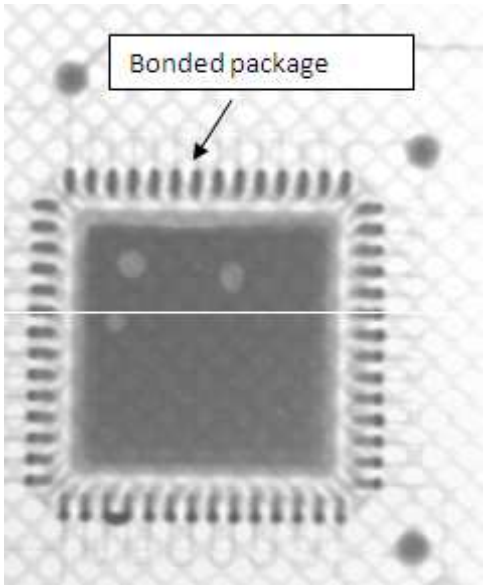


Figure 3.44: QFN X-ray Image

Figure 3.45 shows solder joint formation between PCB and LGA. Good alignment and no solder bridging was observed.

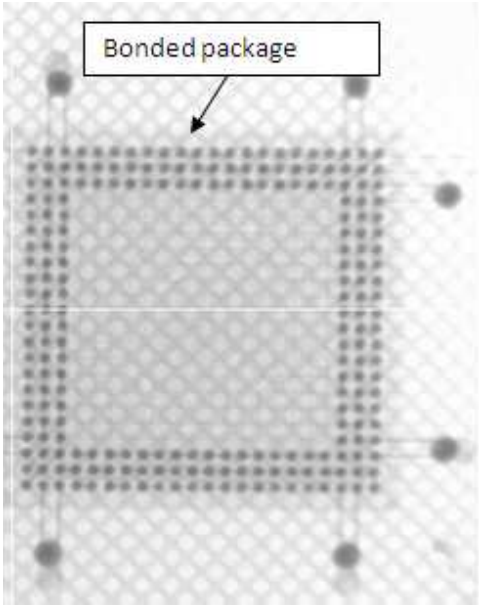


Figure 3.45: LGA X-ray Image

3.8 Accelerated Thermal Cycling

For this experiment thermal cycling condition: -55^{o}C to 125^{o}C, 10 minutes dwells at high temperature, 5 minutes dwells at low temperature, and 30 minutes ramp times were used. The total cycle time was 90 minutes. Thermal profiles are load dependent and should be designed for the particular board to be cycled. A sample PCB board was placed at the center of the chamber with three thermocouples attached to it. With the thermocouples connected to a data acquisition device, a temperature vs time plot (refer to Figure 3.46) was generated to determine if the board reached the set temperature limits.

Soak at 125^{o}C (Sec)	Soak at -55^{o}C(Sec)
1457 to 2015 = 648	4643 to 5075 = 432
6802 to 7504 = 702	10042 to 10420 = 378
12201 to 12903 = 702	15441 to 15873 = 432
17654 to 18302 = 648	20840 to 21272 = 432
23053 to 23647 = 594	

Table 3.10: Dwell Times at Both Low and High Temperatures

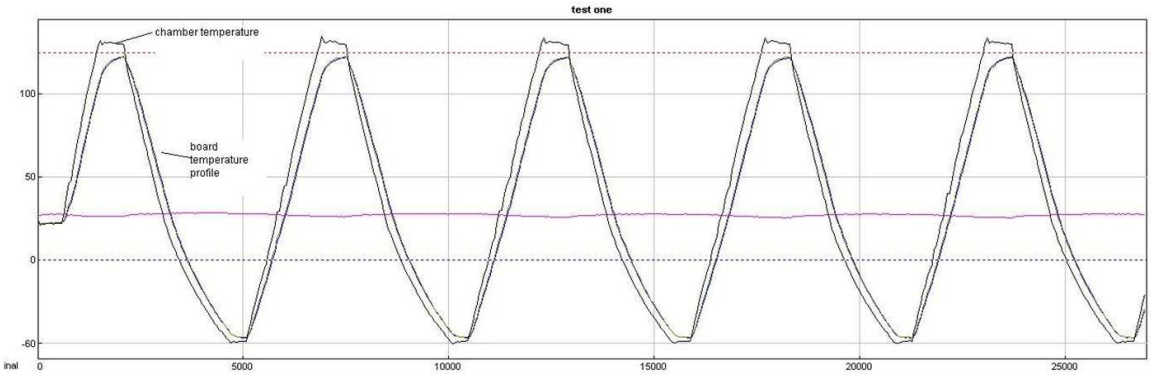


Figure 3.46: Solder Test Vehicle Thermal Cycling Profile

It can be seen from Table 3.10 that the test vehicle stayed at 125^{o}C for a period of 10 minutes, and stayed for a period of 5 minutes at the low temperature of -55^{o}C.

Chapter 4

Results and Discussions

Test vehicles were subjected to the thermal cycling condition defined in the previous chapter. Figure 4.1 plots the Weibull distribution of cycles to failure for the 2512 resistors.

2512 Resistors

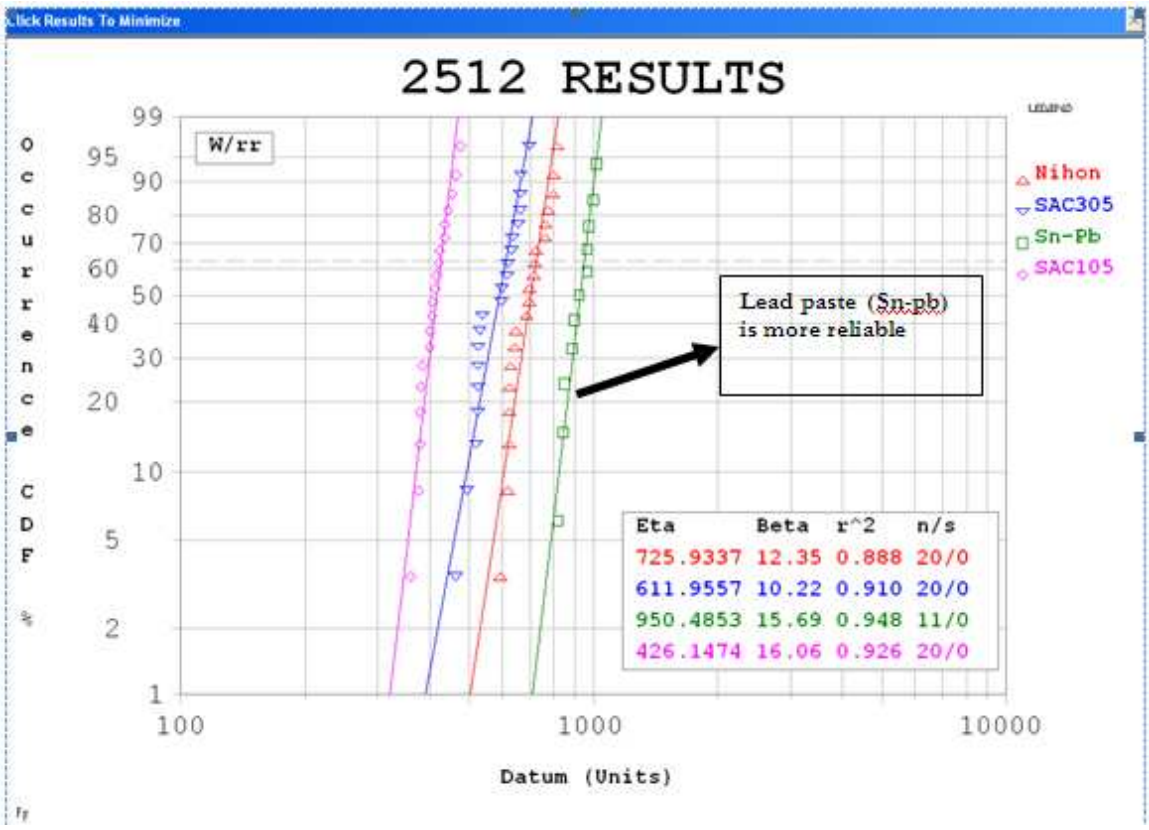


Figure 4.1: Resistor Component Weibull Distribution Plots

Cycles to first failure, cycles to 10% failure and cycles to 63.2% failure are extracted from Figure 4.1 and are tabulated in Table 4.1.

Paste	First Failure (N1)	Cycles to 10% failure (N10%)	Cycles to 63.2% failures (N63.2%)	Weibull Shape parameter
Nihon	593	605.0906	725.9337	12.359
SAC305	463	491.0361	611.9557	10.22
SAC105	360	370.5342	426.1474	16.06
Sn-Pb	820	823.484	950.4853	15.69

Table 4.1: Cycles to Failure Data on 2512 resistors

Data from Table 4.1 was plotted on a 3-dimensional plots to provide a comparison among different solder alloys. It can be seen that Sn-Pb has the highest reliability and SAC 105 has the lowest reliability.

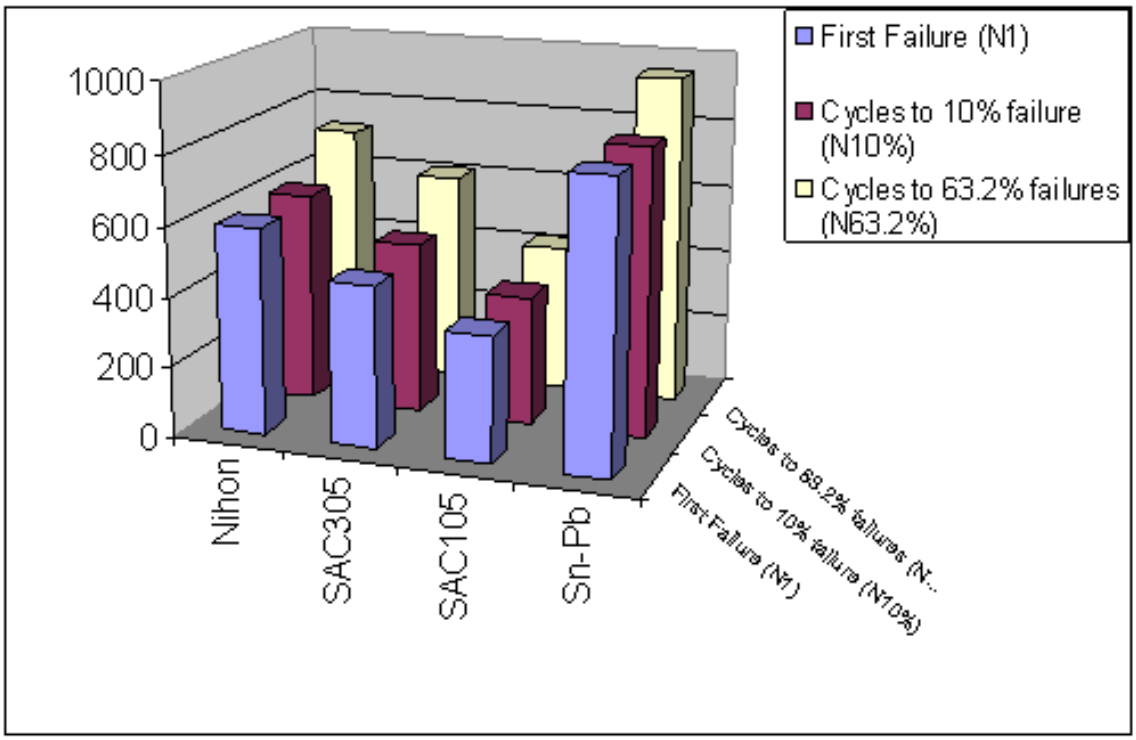


Figure 4.2: 3D Plot Comparing Cycles to Failure on 2512 resistors

The reported Weibull plots and graphs are in agreement with the literature data [38, 41, 43, 44, 47].

LGA

Figure 4.3 plots the Weibull failure distribution for the land grid arrays.

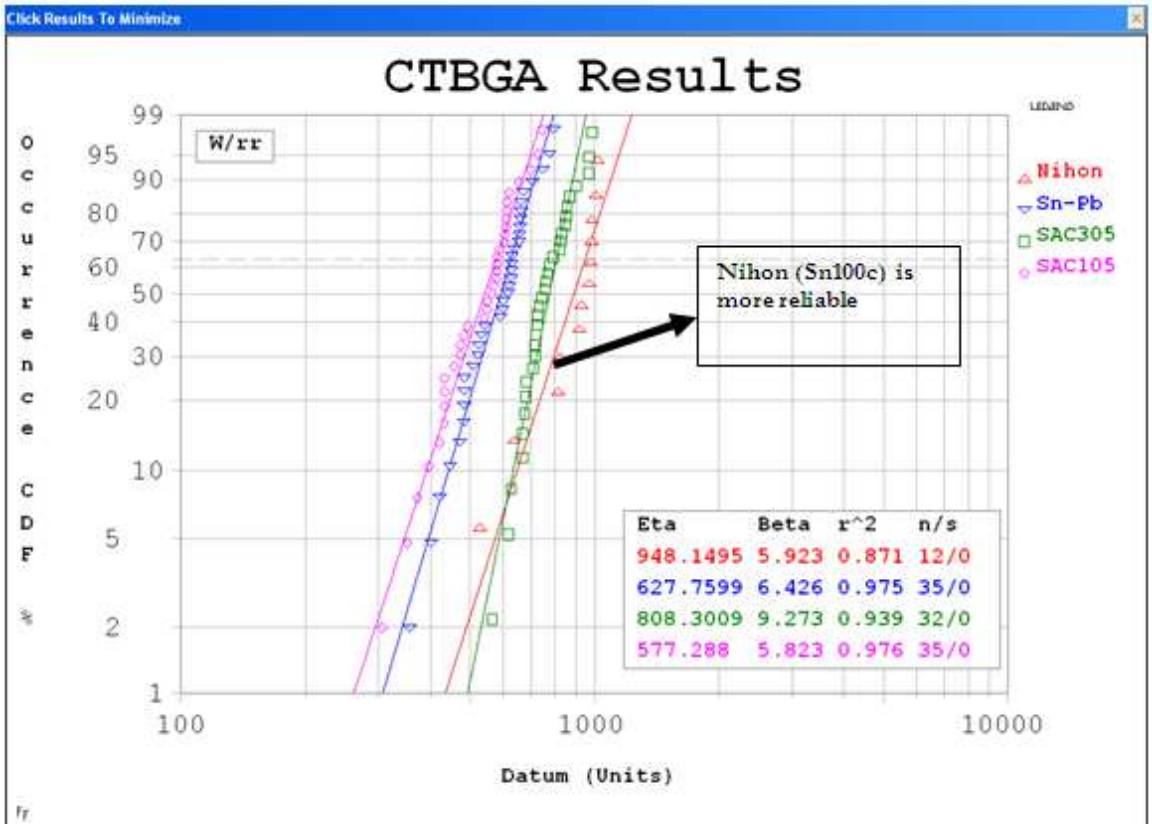


Figure 4.3: CTBGA Weibull Distribution Plots

Cycles to first failure, cycles to 10% failure and cycles to 63.2% failure are extracted from Figure 4.3 and are tabulated Table 4.2.

Paste	First Failure (N1)	Cycles to 10% failure (N10%)	Cycles to 63.2% failures (N63.2%)	Weibull Shape parameter
Nihon	527.5	648.4626	948.1495	5.923
SAC305	565	634.1372	808.3009	9.273
SAC105	306	392.2331	577.288	5.823
Sn-Pb	356	442.2806	627.7599	6.426

Table 4.2: Cycles to Failure Data on CTBGA Package

Data from Table 4.2 was plotted on a 3-dimensional plots to provide a comparison among different solder alloys. It can be seen that the Nihon alloy has marginally higher reliability than SAC 305, and SAC105 has the lowest reliability.

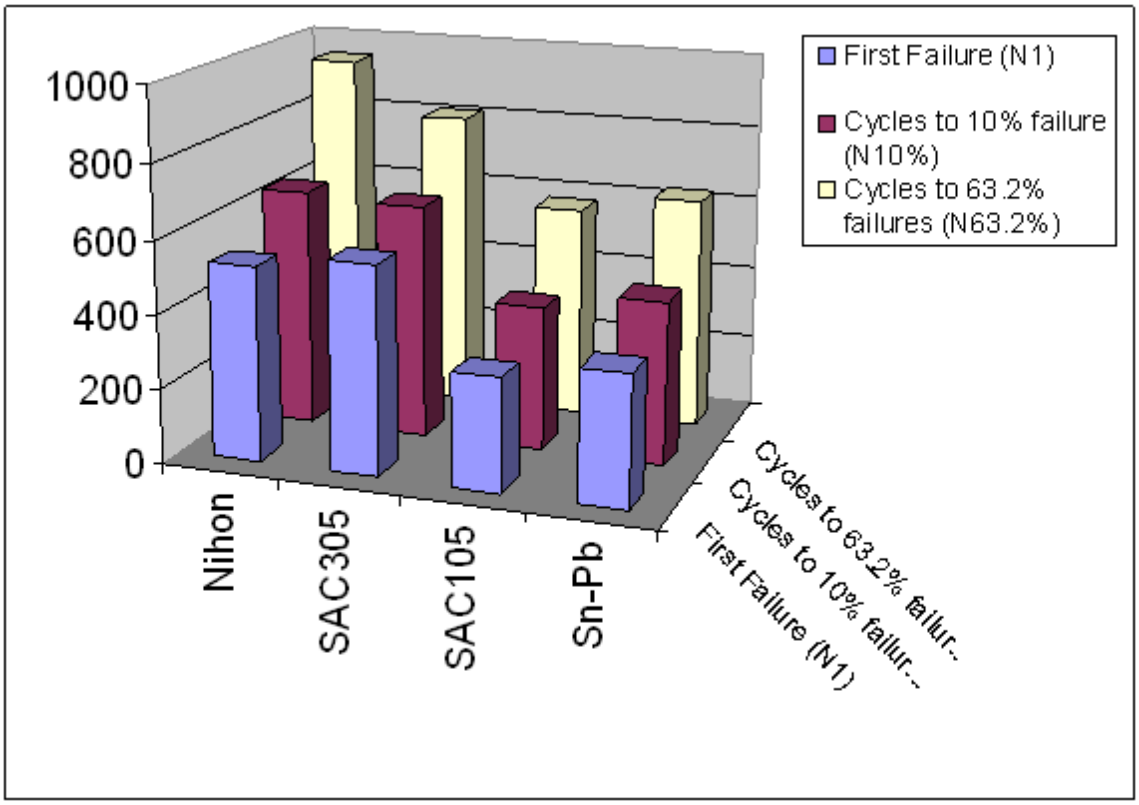


Figure 4.4: 3D Plot Comparing Cycles to Failure on CTBGA

QFN packages

As of Oct 26 2010, the test vehicle was subjected to a total of 1800 cycles and only a few failures have occurred for this package type. Weibull analysis cannot be performed at this point of time due to insufficient data.

Chapter 5

Conclusions and Future Work

5.1 Conclusions

The thermal cycling reliability of LGA, QFN and 2512 chip resistors assembled on a test vehicle using SAC 305, SAC 105 and Sn/0.7Cu/0.05Ni/Ge (Nihon) solder alloys have been studied. Boards were build using Sn-Pb solder alloy for reference purposes. A thermal cycling condition: -55^{o}C to 125^{o}C, 10 minutes dwells at high temperature, 5 minutes dwells at low temperature, and 30 minutes ramps were used. Total cycle time was 90 minutes.

Testing results include: Sn-Pb solder alloy was considered to be superior for use with 2512 chip resistors, and Sn/0.7Cu/0.05ni/Ge (Nihon) solder alloy was considered to be superior for use with LGA packages. These findings are in agreement with the published literature.

5.2 Future Work

The next step in thermal cycling study would be to complete the QFN cycling and to study the failure locations. Further work to analyze the reliability of Sn/0.7Cu/0.05Ni/Ge (Nihon) solder alloy by performing vibration and drop/shock testing is needed.

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