Design of Reconfigurable Baseband Filter

by

Xin Jin

A thesis submitted to the Graduate Faculty of
Auburn University
in partial fulfillment of the
requirements for the Degree of
Master of Science

Auburn, Alabama
December 13, 2010

Keywords: analog filter, reconfigurable, gm-C, lowpass filter

Approved by

Fa Foster Dai, Chair, Professor of Electrical and Computer Engineering
Guofu Niu, Professor of Electrical and Computer Engineering
Bogdan M. Wilamowski, Professor of Electrical and Computer Engineering

Abstract

With the rapid development of worldwide wireless communication networks, mobile terminal devices compatible for multi-standard and various applications are needed. Software defined radio is a suitable answer to those demand. Baseband filter is one of the key building blocks in this device. And the baseband filter designed with tunable cutoff frequency gains a lot of popularity in recent years.

A linear, reconfigurable fully differential CMOS transconductance-C filter is presented in this paper. The filter is implemented in 0.13um CMOS technology. It provides inverse-Chebyshev response and the cutoff frequency tuning range of the filter is from 4MHz to 40MHz. The transconductor adopts a folded-cascode structure and using gain boosting technique in the output stage to provide high output impedance. The input stage uses cross-coupled differential pair with bias offset to achieve high linearity. To be able to achieve the tuning capability of the filter, a floating voltage source with tunable value is employed. Cutoff frequency can be tuned by varying the floating voltage.

Acknowledgments

I would like to express my deep gratitude to my thesis supervisor, Dr. Foster Dai for his continuous guidance and support during this work. His understanding and patience have been a constant source of encouragement for me to finalize the project. I would also like to thank other committee member Dr. Guofu Niu and Dr. Bogdan M. Wilamowski for their enlightening discussion.

Table of Contents

List of Figures

List of Abbreviations

SDR	Software Defined Radio
OPAMP	Operational Amplifier
OTA	Operational Transconductance Amplifier
GBW	Gain Bandwidth
LHP	Left Half Plane
RHP	Right Half Plane
LP	Lowpass

Chapter 1

Introduction

1.1 Background and motivation

With the rapid development of worldwide wireless communication networks, mobile terminal devices compatible for multi-standard and various applications are ne key building blocks in those devices. It is a continuous-time lowpass filter located before the analog teeded. Software defined radio is a suitable answer to those demand. And the baseband filter designed with tunable cutoff frequency gains a lot of popularity in recent years. Baseband filter is one of tho digital converter to provide anti-aliasing action by attenuating high frequency components.

Analog filters composed of resistors, capacitors and inductors are referred to as passive filters. Active devices, such as operational amplifiers and operational transconductance amplifiers, can also be employed in filter design. Filters making use of active devices are referred to as active filters [1]. Compared to passive filters, which require large inductors result in large area in general LC ladder structure [2], active filters have the advantage of less area consumption and lower cost and it becomes the dominant architecture in filter design.

In this work, a reconfigurable continuous-time lowpass filter is designed with an operating frequency from 4MHz to 40MHz. Filter types and topologies are chosen to best meet the requirement.

1.2 Organization of the thesis

The thesis has been organized to provide design architectures as well as techniques for

reconfigurable filters. Chapter 2 of the paper analyzes previously reported different filter architectures and techniques to improve those architectures. Chapter 3 describes the design of the filter architectures and linear transconductors, simulation results are given with explanation. Chapter 4 draws conclusions and future work.

Chapter 2

Previous Work on Filter Architecture

2.1 Active-RC filters

In filter design, the most popular building blocks are the Operational Amplifier (OPAMP) and Operational Transconductance Amplifer (OTA). Different architectures have been reported by using those building blocks, such as switched-capacitor filters, active-RC filters, OTA-C filters. Recently other types of filters are proposed, such as gm-OPAMP-C [3] and active-gm-C [4] [12].

Active-RC filters are composed of resistors, capacitors and OPAMPS. It is well known that these types of filters have good linearity due to the using of OPAMP to form feedback loop. The high linearity can be maintained as long as the gain of the filter is large. Filter needs to provide transition band with enough sharpness to reject out-of-band signals. In many applications, high-order filter is needed to meet this demand. High-order filter can be built from cascading several biquads together. One of the main advantages of cascade filters is that they are easy to tune because each biquad is only responsible for one pole and zero pair. Another advantage is that cascade design is easy and transparent because in designing such a filter we can only focus on the low-order sections rather than implement the whole high-order filter. Two commonly used active-RC biquads are Tow-Thomas biquad and Sallen-Key biquad. Tow-Thomas biquad is shown in Figure 2.1.

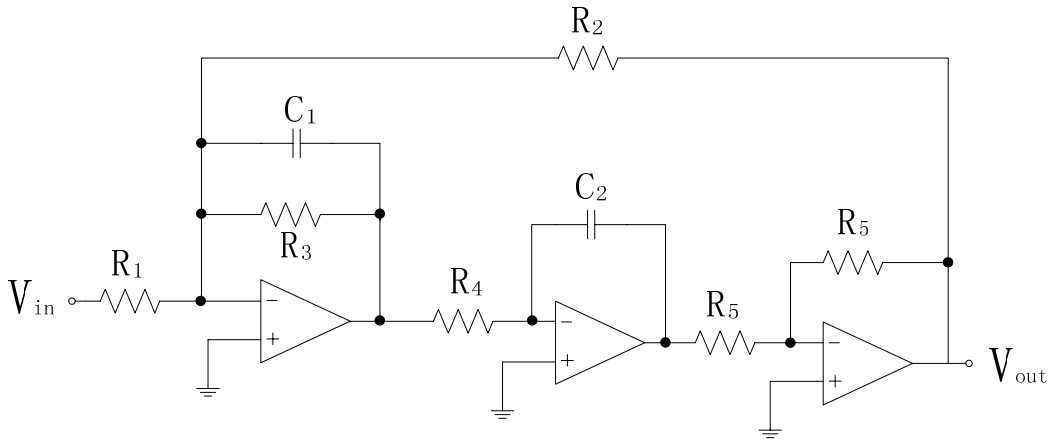

Figure 2.1 Tow-Thomas biquad

The lowpass transfer function and filter parameters of the Tow-Thomas biquad is

$$H(s) = -\frac{1/(R_1R_4C_1C_2)}{s^2+s/(R_3C_1)+1/(R_2R_4C_1C_2)} \tag{2.1}$$

$$\omega_0^2 = \frac{1}{R_2R_4C_1C_2} \tag{2.2}$$

$$Q = \frac{R_3}{\sqrt{R_2R_4}}\sqrt{\frac{C_1}{C_2}} \tag{2.3}$$

$$H = \frac{R_2}{R_1} \tag{2.4}$$

As we can observe in the above equations, the biquad circuit can be tuned *orthogonally*. It means all the parameters can be tuned independently without affecting other parameters. This is always preferred in filter design.

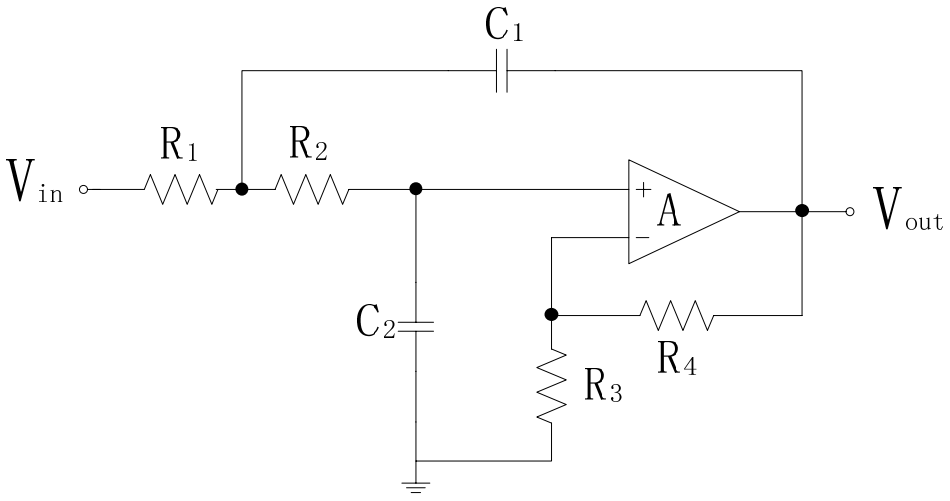

Figure 2.2 Sallen-Key biquad

Figure 2.2 shows the architecture of Sallen-Key biquad. The lowpass transfer function of

Sallen-Key biquad can be represented as

$$H(s) = -\frac{K/(R_1R_2)}{s^2C_1C_2+s[C_2(1/R_1+1/R_2+C_1(1-K)/R_2]+1/(R_1R_2)} \quad (2.5)$$

Where $K = 1 + R_4/R_3$

$$\omega_0^2 = \frac{1}{R_1R_2C_1C_2} \quad (2.6)$$

$$Q = \frac{1}{\sqrt{R_1R_2}}\frac{1}{1/R_1+1/R_2(2-K)} \quad (2.7)$$

$$H = K \quad (2.8)$$

It can be observed that the Sallen-Key biquad consumes less power compared to Tow-Thomas biquad simply because it just uses one OPAMP. However, the Sallen-Key biquad has larger sensitivity on PVT variation and more susceptible to parasitic capacitance. It also has large sensitivity of *Q* to *K*. When designing a lowpass filter with Q=10, it can be proved that 1% error in amplifier gain *K* will result in approximately 30% error in quality factor Q [1].

An important limitation on active-RC filter is that the bandwidth of the filter cannot exceed the bandwidth of the OPAMP. And the linearity of active-RC filter will also degrade as frequency is higher than a limit [5]. The reason for this is the OPAMP lose its gain at high frequency and beyond this frequency the filter will not function correctly. Generally, it is not recommended that the active-RC circuits to be operated at frequencies higher than 5 or 10% of the OPAMP's cutoff frequency. In our design, the desired filter tuning range is from 4MHz to 40MHz. Which means the OPAMP's bandwidth should be at least 400MHz or 800MHz. Another potential problem of active-RC filter is the Q enhancement and this problem becomes severe when filter designed with high order is needed. It has been shown that in a Tow-Thomas two-integrator loops, the actual quality factor Q is enhanced by roughly a factor of 1/(1-2Q*ω/GBW) [1]. For example, for a 4MHz 8th Chebyshev filter, to keep the increase of the Q smaller than 5%, the GBW must at least be 280 (Q=7) times larger than the cutoff frequency

of 4MHz [6]. So the GBW of the OPAMP should not be less than 1.12GHz. For a filter (with similar order) with tuning range from 4MHz to 40MHz, the required GBW is so large that the power consumption might be unreasonably large.

To illustrate the problem more intuitively, a prototype of 7th order inverse-Chebyshev filter is build based on active-RC architecture. The 7th order prototype is built by cascasding three Tow-Thomas biquads with a 1st order lowpass filter. Figure 2.3 shows the Q enhancement problem in 7th order inverse-Chebyshev prototype. As we can see from the figure, the filter cutoff frequency is about 15MHz but the GBW needed to be larger than 2Grad/s to keep the ripple less than 0.5dB. It is also observed that when the GBW of OPAMP is only ten times larger than the cutoff frequency (200MHz in this case), the attenuation response in the transition band is far away from desired. Thus when filters are designed for high frequency application, large GBW OPAMP is inevitable. It is predictable that in this case the OPAMP will consume unacceptable large power when conventional Miller compensation is employed.

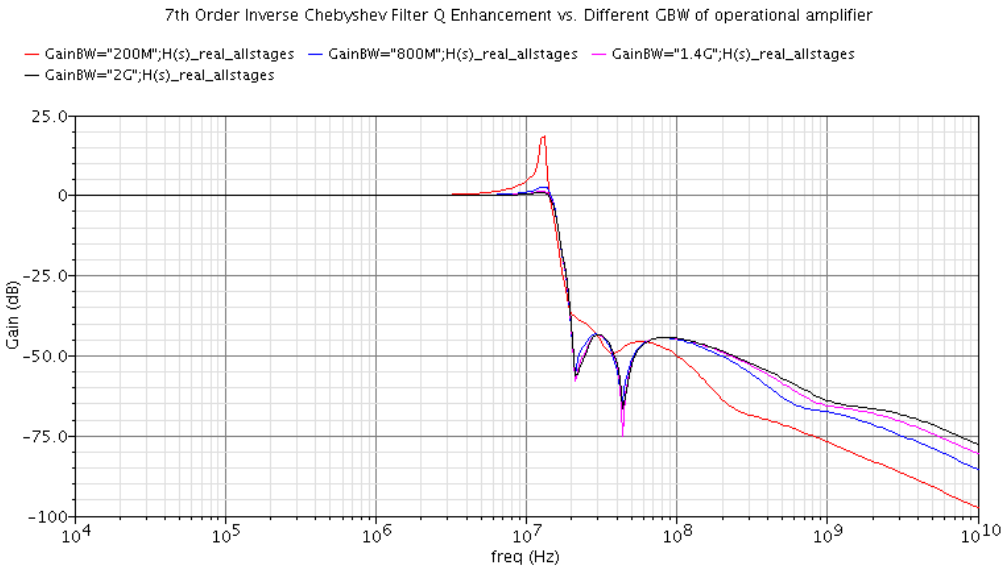

Figure 2.3 Q enhancement problem

2.2 Techniques to improve the performance of active-RC filters

Many techniques have been proposed to improve the performance of active-RC filter in high-frequency application.

The conventional two-stage OPAMP employing miller compensation has many design limitations when high gain and wide bandwidth is needed. Efforts have been done to improve the active-RC filter performance by designing the OPAMP without using miller compensation. To be able to expand the GBW of OPAMP without sacrificing gain and consuming more power, a three-stage OPAMP with Nested Miller frequency compensation can be used to boost the GBW the concept is shown in Figure 2.4 [7].

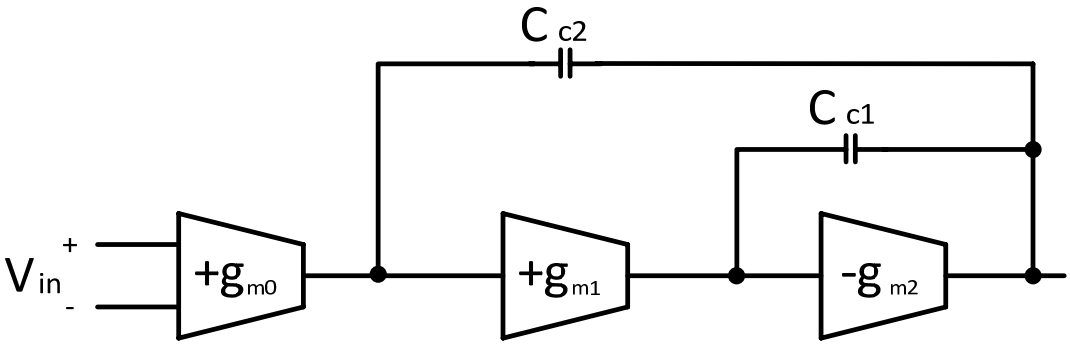

Figure 2.4 Three-stage opamp with nested miller compensation

Another technique proposed to mitigate Q enhancement problem is by adding extra resistors in series with Miller capacitor to create a zero that cancels the effect of the limited amplifier's GBW [1] [8]. The proposed method using this technique is shown in Figure 2.5.

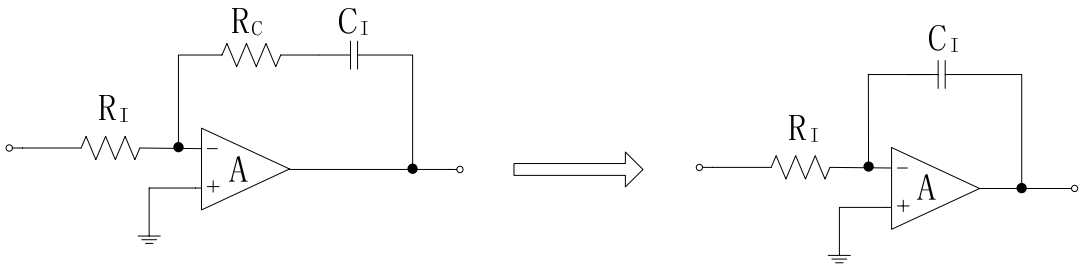

Figure 2.5 Alleviate Q enhancement problem by inserting a series resistor

Analysis shows the transfer function of the modified integrator is

$$H(s) = -\frac{1}{sC_I R_I}\frac{1+sC_I R_C}{1+1/(\omega_t R_I C_I)+s/\omega_t(1+R_C/R_I)} \quad (2.8)$$

where ω_t is parasitic pole of the original integrator

Thus by choosing

$$R_C = 1/(\omega_t * C_I) \quad (2.9)$$

We can have an ideal integrator

$$H(s) = -\frac{1}{sC_I R_I}\frac{1}{1+1/(\omega_t R_I C_I)} \approx -\frac{1}{sC_I R_I} \quad (2.10)$$

To be able to make R_C track $1/(\omega_t * C_I)$. Extra Q tuning circuit is necessary which increases the complexity of the filter design.

A more elegant way to accomplish this compensation is propose in [9]. Noticed that ω_t is largely determined by g_m/C_c, where C_c is the miller compensation capacitor of OPAMP. If C_c and C_I can match well, R_C only need to track g_m which turns the problem into constant-g_m biasing. Using this approach, the GBW of OPAMP requirement is greatly relaxed which results in less power consumption.

Alternatively, a required Q can be predesigned in filter which is referred as predistortion. By predistorting the Q, the filter will enhance the Q to the desired value Q_r. This technique can only be employed under the assumption that the GBW of OPAMP is known. In practice, extra tuning circuit is needed to fine tune the Q.

Another approach is using a conventional two-stage OPAMP but employing new compensation technique [10]. In the two-stage OPAMP, besides the classic conventional miller compensation, another compensation capacitor is added and across connected to the outputs of the first and second stages of the amplifier. The added capacitor helps to keep phase response away from -180° when frequency goes beyond the unity gain frequency. By employing this approach, the OPAMP can gain more bandwidth and without severely degrading stability of the

OPAMP [10].

A different compensation scheme for multistage amplifiers with no Miller capacitors is shown in Figure 2.6 [11]. By creating a feedforward path using gm2, this scheme produces a LHP zero to compensate the negative phase shift of the poles. However, the transient response might be degraded severely by the pole-zero doublets.

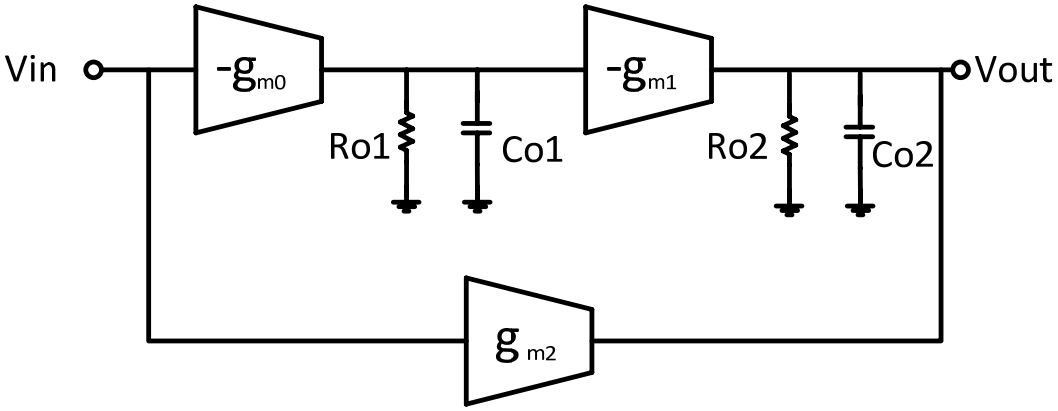

Figure 2.6 Opamp compensation using feedforward

Usually, the cutoff frequency tuning of active-RC filter is achieved by constructing resistor and capacitor array. Thus, the cutoff frequency can only be tuned at discrete intervals. The tuning resolution is determined by the unit resistor and capacitor.

To be able to achieve continuously frequency tuning, a continuously tunable resistor is proposed shown in Figure 2.7 [7]. The resistor value can be tuned by diverting current through the MOS transistor. However, carefully design need to be performed because Cp affects its frequency response, so the transistor needs to be sized to achieve ω_t larger than the interested frequency band.

Although the techniques mentioned above can improve the active-RC filter performance in high frequency operation, their operating frequency is generally limited below 20MHz.

2.3 Transconductance-C filters

As mentioned, generally it is not recommended that the active-RC circuits be operated at

frequencies higher than 5 or 10% of ω_t. For high frequency operation, transconductance-C (gm-C) filter becomes the dominant circuit in these applications [1]. Similar to active-RC filters, gm-C filters can be constructed based on cascading biquads.

The basic building blocks for gm-C filters were shown in Figure 2.7 to Figure 2.9 [13].

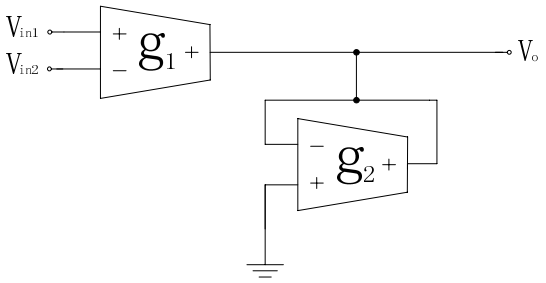

Figure 2.7 Amplifier

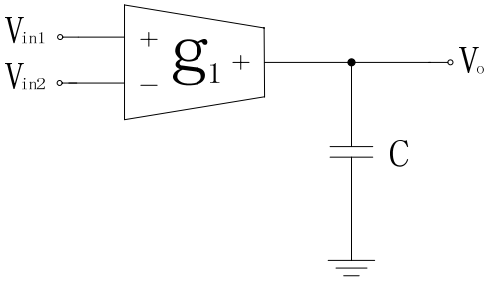

Figure 2.8 Ideal Integrator

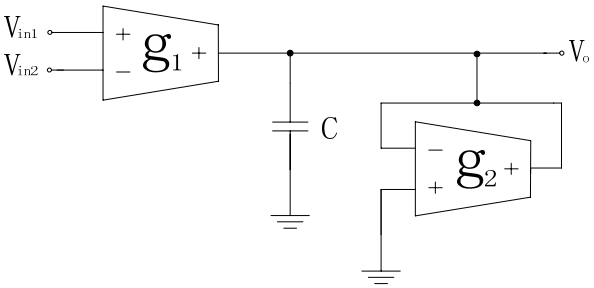

Figure 2.9 Lossy integrator

The gm-C biquad architecture is shown in Figure 2.10. This gm-C biquad is an equivalent of Tow-Thomas (TT) active-RC biquad.

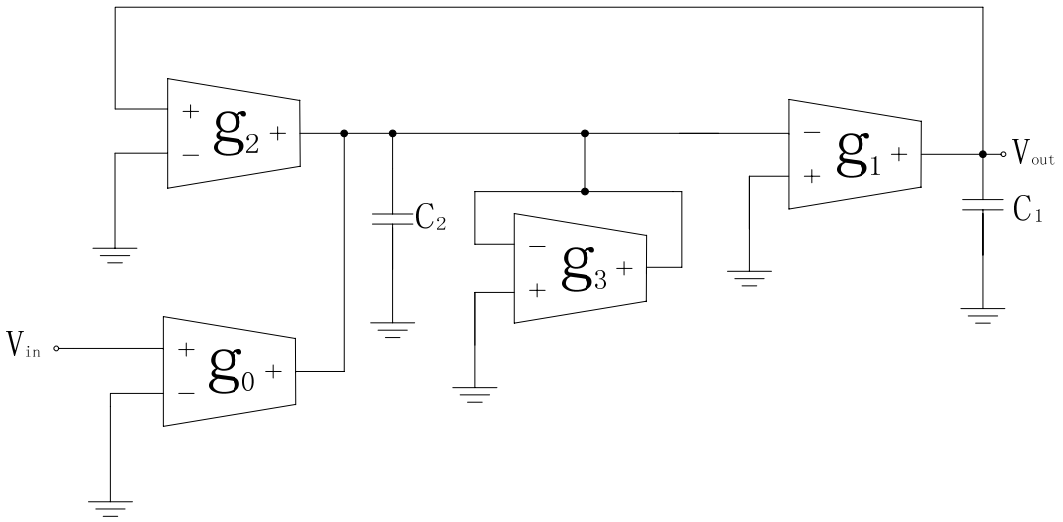

Figure 2.10 Gm-C Biquad

The transfer function of lowpass output is given by the equation below

$$H_{LP}(s) = \frac{V_{out}}{V_{in}} = \frac{-g_0 g_1}{s^2 C_1 C_2 + s g_3 C_1 + g_1 g_2} = \frac{-K_{LP}\omega_0^2}{s^2 + s(\omega_0/Q) + \omega_0^2} \quad (2.11)$$

$$\omega_0 = \sqrt{\frac{g_1 g_2}{C_1 C_2}} \quad (2.12)$$

$$Q = \frac{1}{g_3}\sqrt{\frac{g_1 g_2 C_2}{C_1}} \quad (2.13)$$

$$K_{LP} = \frac{g_0}{g_2} \quad (2.14)$$

The equations above show that the filter gain can be tuned independently of the quality factor Q and frequency ω_0 and the quality factor Q can be tuned independently of frequency ω_0.Then orthogonal tuning can be achieved for equal capacitors [13].

2.4 Techniques to improve the performance of transconductance-C filters

A general problem of gm-C filters is that they suffer from low linearity performance. This is due to the open-loop operation of this type of filter. Therefore, the linearity of gm cell directly affects the linearity performance of the filter. Many techniques have been proposed to improve the linearity of the gm, such as attenuation, nonlinear terms cancellation and source degeneration.

For attenuation approach, the input of the transconductance is an attenuated version of the input signal. Therefore, the transconductance gain must be increased by the same factor to

maintain the overall gain unchanged, which increased both power consumption and silicon area [14].

A more elegant technique to linearize transconductors is using the cross-coupled connection to cancel the nonlinear term which will produce an ideally linear transconductor [15]. The general concept of this technique is shown in Figure 2.11.

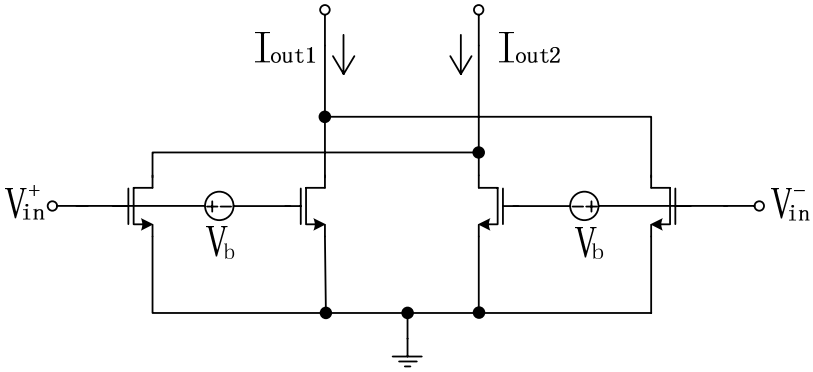

Figure 2.11 General concept of circuit structure employ nonlinear term cancelling [15]

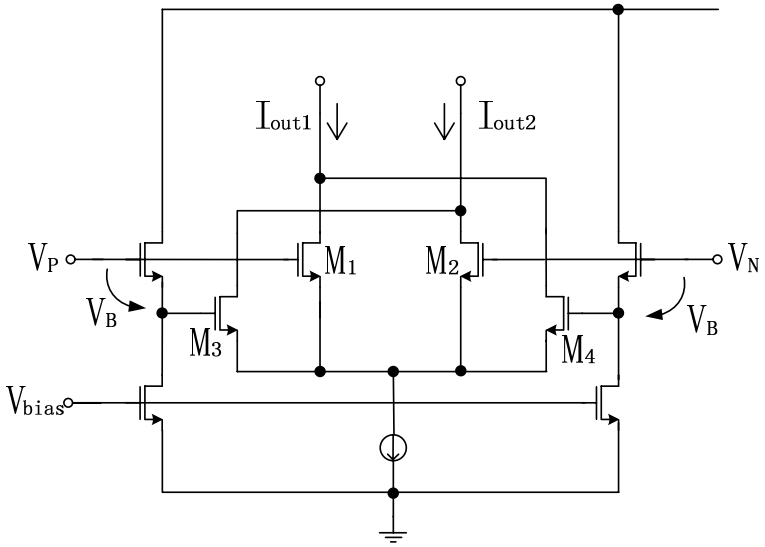

Figure 2.12 Circuits realized the concept in Figure 2.11 [15]

From Figure 2.12, we can derive the equations below

$$I_1 = I_{d1} + I_{d4} = K(V_P - V_T)^2 + K(V_N - V_B - V_T)^2 \tag{2.15}$$

$$I_2 = I_{d2} + I_{d3} = K(V_N - V_T)^2 + K(V_P - V_B - V_T)^2 \tag{2.16}$$

where $K = (\frac{\mu C_{ox} W}{L})/2$ and V_T is the threshold voltage.

The differential output current is calculated as

$$I_o = I_1 - I_2 = 2KV_B(V_P - V_N) \tag{2.17}$$

Equation (2.17) shows the transconductance is simply $G_m = 2KV_B$, which is linearly controllable by the voltage V_B. The techniques based on non-linearity cancellation require accurate matching of MOS transistors, and they are sensitive to second-order effects (e.g., bulk effect, channel-length modulation, and short-channel effects).

Another popular linearization technique employs source degeneration which is shown in Figure 2.13. Usually, R is realized by using transistors operated in triode region shown in Figure 2.14.

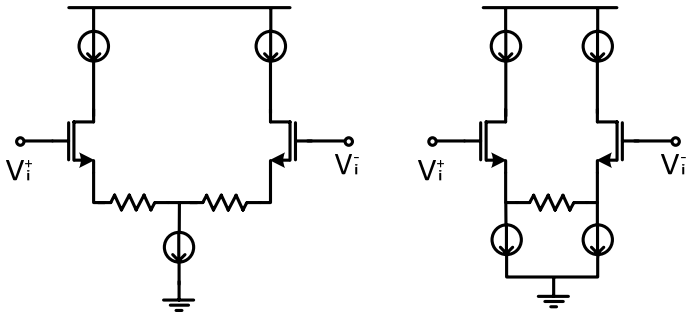

Figure 2.13 Concepts of gm linearization using source degeneration [14]

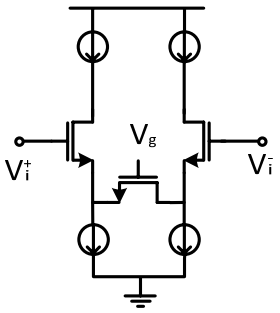

Figure 2.14 Gm linearization by using source degeneration (transistor in triode region)[14]

The topologies in Figure 2.13 exhibit different properties. Noticed Figure 2.13 (left) has smaller common-mode input swing than Figure 2.13 (right). Noise contribution from the current source in Figure 2.13 (left) appears as common-mode noise, but in Figure 2.13 (right) the noise contribution from current source appears as differential-mode noise.

A recently proposed method to increase the linearity of transconductor is by making use of nonlinear source degeneration technique [18]. The circuit implementation is shown in Figure

2.15. The operation of this type of linearization technique can be explained as follows. For a differential pair with source resistor (let's assume the value of the resistor is a) degeneration, it exhibits its own gm curve versus differential mode input. If we change the resistor value from a to b, we can get another gm curve versus differential mode input voltage. If we plot the gm curve with different resistor value, we can get different gm curves. For a linear transconductor, the gm value should be constant over a wide differential mode input range. Thus, if it is possible to jump from one curve to another curve when input swing changes we can acquire a linear transconductor. Also notice that as the input voltage increases, the transconductance drops. However if the degeneration resistor decreases as the input voltage increase a perfect linear transconductor achieved.

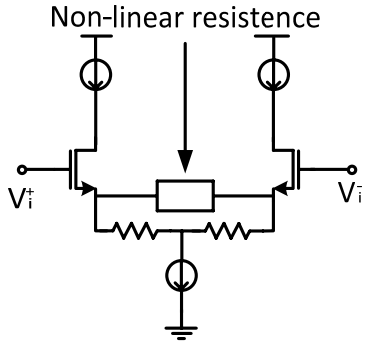

Figure 2.15 Gm linearization by using nonlinear resistance [18]

In practice, a perfect nonlinearity cancellation cannot be achieved due to PVT. So an extra linearity tuning circuit is needed in this approach.

It is well known that the active-RC filter can provide good linearity because their closed-loop operation. A proposed Gm-C filter by making use of this approach is reported in [19]. The concept of this approach is shown in Figure 2.16.

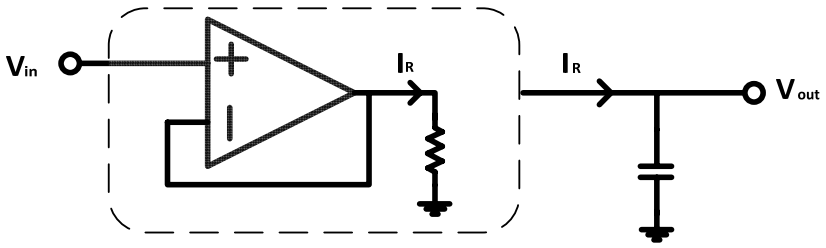

Figure 2.16 Concept of gm linearization by using unity-gain buffer

The main advantage of the approach compared to conventional active-RC filter is by making use of unity-gain feedback to realize maximum bandwidth usage. Circuit employing this technique does show good linearity over a wide range of Vid. However, it has narrow tuning range issue due to mobility degradation, which limits its application when wide-tuning is needed [19].

Another consideration in designing transconductor is how to realize large output impedance. For ideal transconductor, we should have infinite output impedance. Practical transconductor, however, just have finite output impedance. A technique employing negative resistance is proposed [16]. The basic concept of the transcondutor is shown in Figure 2.17.

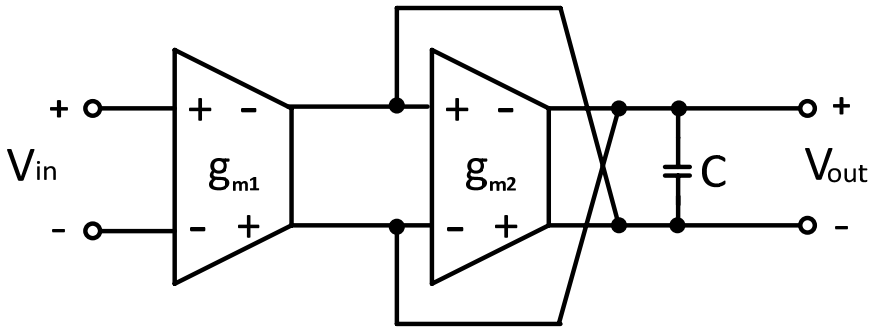

Figure 2.17 Conceptual block diagram of transconductor with high output impedance

The open-circuit voltage transfer function of the figure 2.17 is given by

$$\frac{V_{out}}{V_{in}} = -\frac{G_m}{sC - G_{m2} + 1/R_{out}}$$

G_{m2} acts as a negative resistor, infinite output impedance can be achieved by choosing G_{m2} equal to $1/R_{out}$. This results in a $\mathrm{G_m - C}$ integrator circuit with infinite dc gain. $\mathrm{G_{m2}}$ needs to be larger than $1/R_{out}$ because if we choose $1/R_{out} < \mathrm{G_{m2}}$ a RHP will be introduced

which leads to instability issue. To maintain the circuit operating in stable condition, $G_{m2} \leq 1/R_{out}$ must be maintained, this results in a lossy gm-C integrator.

Classic cascode structure can also be used to increase the output impedance. A technique proposed by combining bias offset and folded cascode is reported in [17]. However, as low power application becomes more popular today, this approach does consume too much headroom.

The high-order filter can be constructed by cascading several biquads together. It is easy to design using approach because each biquad only responsible for one zero and pole pair. So designers just need to focus on low order biquad filter not the whole high order filter. Although it is simple to design and tune a cascaded filter, this method suffers from high sensitivity to component variations [1]. It is well known that doubly terminated LC ladders have very low sensitivity in passband. To achieve this low sensitivity, gm-C filters are designed by simulating the operation of the ladder.

In our design, the operation range is from 4MHz to 40MHz, it is more suitable to use Gm-C filter rather than Active-RC filter because the former one is more suitable for high frequency operation. And the filter is designed by simulating the operation of ladder for the reason discussed above.

Chapter 3

Design of Reconfigurable Baseband Filter

3.1 Filter Topology

Based on the advantages mentioned above, we decide to build a filter using Gm-C architecture to simulate the operation of ladder. For the filter response consideration, in order to have sharp transition band with relative low order and zero ripple in passband, inverse-Chebyshev filter response is selected. The attenuation for Butterworth and Chebyshev I filters of lowpass type approaches infinity for high frequencies. Therefore, in pole efficiency perspective, the filters have a much larger attenuation in the stopband than necessary. However, the attenuation of inverse-Chebyshev filter is monotonically increasing in the passband and has equirriple stopband attenuation. In passband, the filter has no ripple which resembles a Butterworth filter. The difference between them is the inverse-Chebyshev filter has zeros located on imaginary axis. And those zeros provide a smaller transition band than a Butterworth filter of the same order. Generally it is considered that Butterworth filter have less group delay compared to inverse-Chebyshev filter and also provide sharp transition band when filter order is high enough. However, for the same sharpness of transition band the inverse-Chebyshev filter requires lower order compared to Butterworth filter, and high order filter will result in large group delay, thus it is possible that the inverse-Chebyshev filter have lower group delay compared to Butterworth filter to meet the same demand. The ladder prototype of a 5^{th} order Inverse-Chebyshev filter is shown in Figure 3.1.

To simulate the operation of this ladder, we use the signal-flow-graph (SFG) method to

establish the signal flow equations. Use Thevenin equivalent circuit on the left most resistor and redraw the ladder we have the equivalent circuit shown in Figure 3.2.

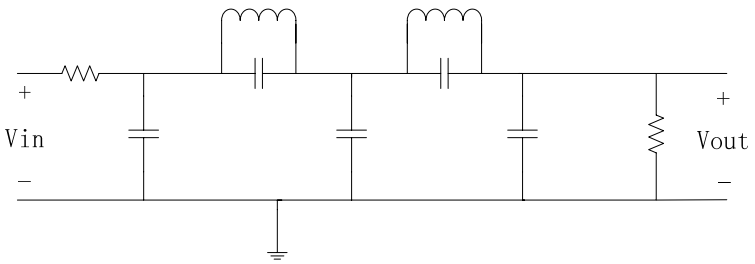

Figure 3.1 The ladder prototype of 5th order inverse-Chebyshev filter

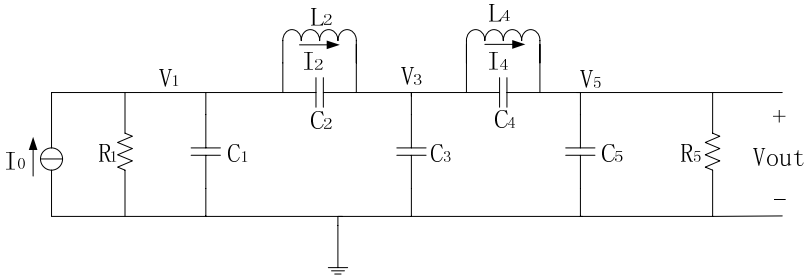

Figure 3.2 The ladder prototype of 5th order inverse-Chebyshev filter with current source

It is more conveniently to treat the ladder with general impedance. The filter prototype with general impedance is shown in Figure 3.2. This ladder is described by the equations presented below

$$V_1 = Z_1[(I_0 - I_2) - Y_{21}(V_1 - V_3)] \tag{3.1}$$

$$I_2 = Y_{22}(V_1 - V_3)] \tag{3.2}$$

$$V_3 = Z_3[(I_2 - I_4) + [Y_{21}(V_1 - V_3) - Y_{41}(V_3 - V_5)]] \tag{3.3}$$

$$I_4 = Y_{42}(V_3 - V_5)] \tag{3.4}$$

$$V_5 = Z_5[I_4 + Y_{41}(V_3 - V_5)] \tag{3.5}$$

Where

$$Z_1 = \frac{1}{sC_1 + 1/R_1} \tag{3.6}$$

$$Y_{21} = sL_2 \tag{3.7}$$

$$Y_{22} = sL_2 \tag{3.8}$$

$$Z_3 = \frac{1}{sC_3} \tag{3.9}$$

$$Y_{41} = sC_4 \tag{3.10}$$

$$Y_{42} = sL_4 \tag{3.11}$$

$$Z_5 = \frac{1}{sC_5+1/R_5} \tag{3.12}$$

The ladder prototype with general impedance is shown in Figure 3.3.

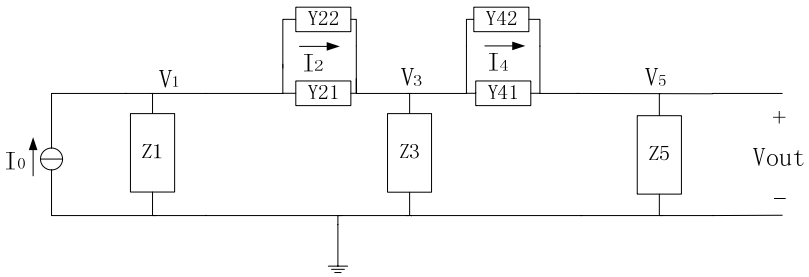

Figure 3.3 General impedance graph of the ladder prototype

Signal-flow graph method requires the all node signals are indicated by voltage, we scale the ladder equations to treat the current as voltage signal. The resulting equations are shown below

$$V_1 = Z_1 g[(V_0' - V_2') - Y_{21}/g(V_1 - V_3)] \tag{3.13}$$

$$V_2' = Y_{22}/g(V_1 - V_3)] \tag{3.14}$$

$$V_3 = Z_3 g[(V_2' - V_4') + Y_{21}/g(V_1 - V_3) - Y_{41}/g(V_3 - V_5)] \tag{3.15}$$

$$V_4' = Y_{42}/g(V_3 - V_5)] \tag{3.16}$$

$$V_5 = Z_5 g[V_4' + Y_{41}/g(V_3 - V_5)] \tag{3.17}$$

Next, we ratio the general impedance to acquire more freedom when design the ladder using operational simulation. The general impedance becomes

$$Z_1' = \frac{Z_1 g}{g_1} \tag{3.18}$$

$$Y_{21}^{'} = \frac{Y_{21}g_1}{g} = \frac{Y_{21}g_3}{g} \tag{3.19}$$

$$Z_2 = \frac{Y_{22}}{g_2 g} \tag{3.20}$$

$$Z_3^{'} = \frac{Z_3 g}{g_3} \tag{3.21}$$

$$Y_{41}^{'} = \frac{Y_{41}g_3}{g} = \frac{Y_{41}g_5}{g} \tag{3.22}$$

$$Z_4 = \frac{Y_{42}}{g_4 g} \tag{3.23}$$

$$Z_5^{'} = \frac{Z_5 g}{g_5} \tag{3.24}$$

From the equations (3.19) (3.22), we find that it is necessary to keep $g_1 = g_3 = g_5$. To be able to use Gm-C basic building block to build the ladder architecture based on the equations above, substitute equations (3.6) – (3.12) into equations (3.18) – (3.24) we have

$$Z_1^{'} = \frac{1}{sC_1^{'}+g_1^{'}}, \text{ where } C_1^{'} = \frac{C_1 g_1}{g}, \; g_1^{'} = \frac{g_1}{R_1 g} \tag{3.25}$$

$$Y_{21}^{'} = sC_2^{"}, \text{ where } C_2^{"} = \frac{C_2 g_1}{g} = \frac{C_2 g_3}{g} \tag{3.26}$$

$$Z_2 = \frac{1}{sC_2^{'}}, \text{ where } C_2^{'} = L_2 g g_2 \tag{3.27}$$

$$Z_3^{'} = \frac{1}{sC_3^{'}}, \text{ where } C_3^{'} = C_3 g_3 / g \tag{3.28}$$

$$Y_{41}^{'} = sC_4^{"}, \text{ where } C_4^{"} = \frac{C_4 g_3}{g} = \frac{C_4 g_5}{g} \tag{3.29}$$

$$Z_4 = \frac{1}{sC_4^{'}}, \text{ where } C_4^{'} = L_4 g g_4 \tag{3.30}$$

$$Z_5^{'} = \frac{1}{sC_5^{'}+g_5^{'}}, \text{ where } C_5^{'} = \frac{C_5 g_5}{g}, \; g_5^{'} = \frac{g_5}{R_5 g} \tag{3.31}$$

Again, it is worthwhile to mention that we need $g_1 = g_3 = g_5$ to make the equations above are valid. Using the basic building blocks, we can have the active realization of ladder architecture as shown in Figure 3.4. The above figure shown in Figure 3.4 is its single-end version, its modified version is shown in the below figure in Figure 3.4.

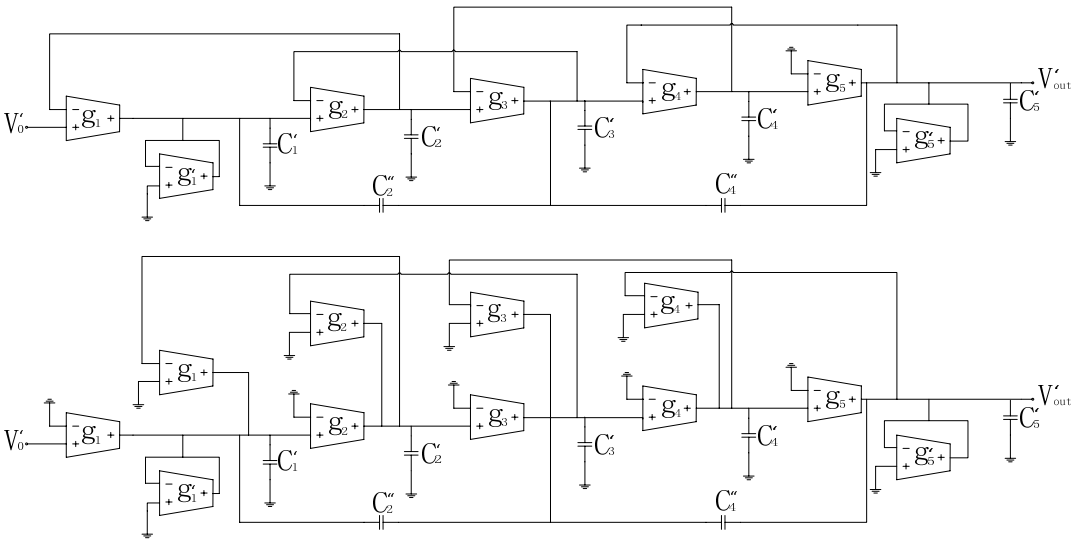

Figure 3.4 Gm-C realization of the ladder prototype

It is well known that fully differential architecture have less common noise compared to single-end architecture, especially when digital circuits are integrated in the same chip. Therefore, fully differential architecture is preferred in design because of its better noise performance. A fully differential architecture version converted from Figure 3.4 is shown in Figure 3.5. Two inputs were connected together to compensate the 6dB gain loss of the ladder prototype.

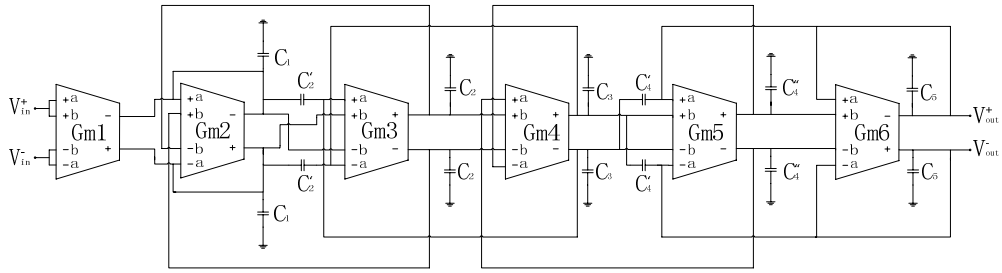

Figure 3.5 Fully differential Gm-C realization of ladder filter

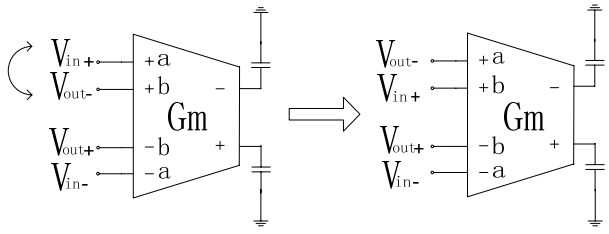

Figure 3.6 Conventional Gm-C integrator (left) and modified version with input-swap (right)

A modified biquadratic filter topology reported in [20] can provide inherently more linear performance than conventional one. This technique can also be used for ladder filter architecture. Noted in Figure 3.5, each OTA cell contains two input pairs and one output pair. We examine one gm-C integrator and its signal connection in Fig. 3.6. The current flow out of the conventional OTA can be represented as

$$I_{out} = G_{ma}(V_{in+} - V_{in-}) + G_{mb}(V_{out-} - V_{out+}) \tag{3.32}$$

From equation (3.32), it can be observed that each OTA (G_{ma} and G_{mb}) has differential input signal swing to a full scale. Assume G_{ma} and G_{mb} have the same value for the entire input signal swing and they matches well, equation (3.32) can be rearranged as

$$I_{out} = G_{ma}(V_{out-} - V_{in-}) + G_{mb}(V_{in+} - V_{out+}) \tag{3.33}$$

It can be observed that after the rearrangement the output current of the OTA remains the same. Therefore, the integrator has the same transfer function. The advantage of this arrangement is the input signal swing is much smaller than the conventional one, which alleviates the linearity problem for large swing input signal of the OTA. Accordingly, the swing of all the internal nodes of the filter is less than that of the conventional one. In the filter topology, this rearrangement can be simply realized by swapping the input of V_{a+} and V_{b+}. The complete modified filter topology is shown in Fig.3.7.

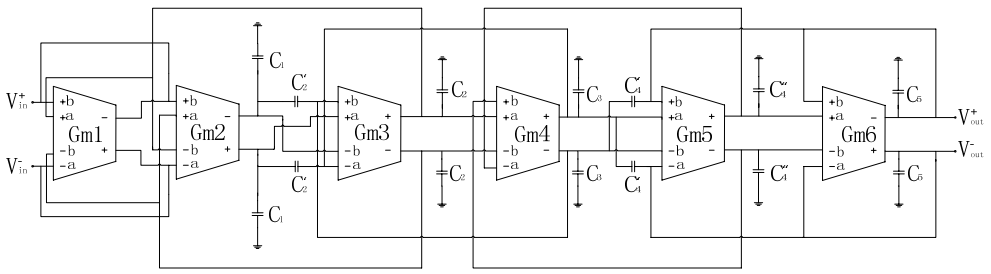

Figure 3.7 Modified circuit by swapping the input of each OTA

The tuning range of the filter should start from 4MHz to 40MHz. The tuning ability is

accomplished by adjusting the Gm value in each transconductor. Based on the prototype shown in Figure 3.7, we built a behavior model of the filter prototype in Cadence, the simulation result is shown in Figure 3.8.

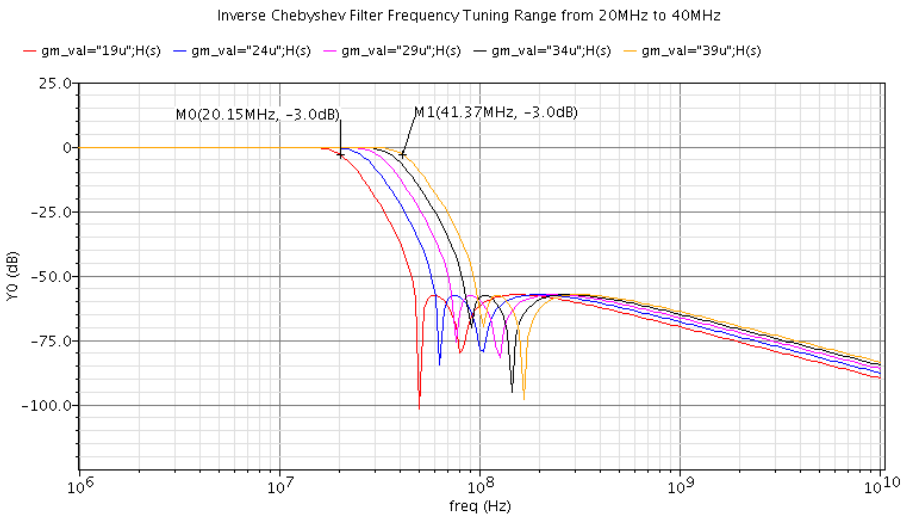

Figure 3.8 Example of 5th order inverse-Chebyshev filter tuning process

As shown in Figure 3.8, the cutoff frequency can be tuned from 20MHz to 40MHz by adjusting the Gm value in transconductor. The phase response and group delay of the filter prototype are shown in Figure 3.9 and Figure 3.10. Wider cutoff frequency tuning range can be achieved if we have larger gm tuning range. In this work, the cutoff frequency of the lowpass filter can be tuned from 4MHz to 40MHz.

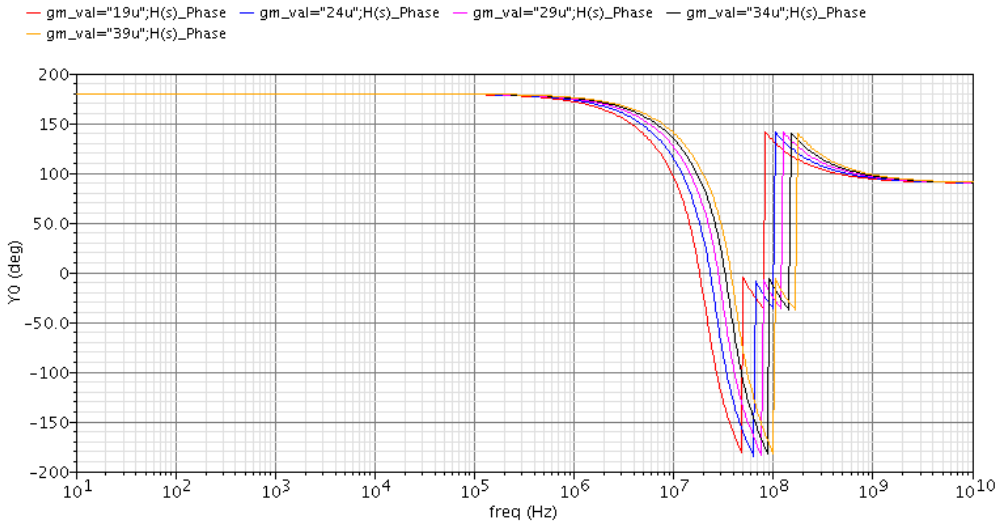

Figure 3.9 5th order inverse-Chebyshev filter phase response

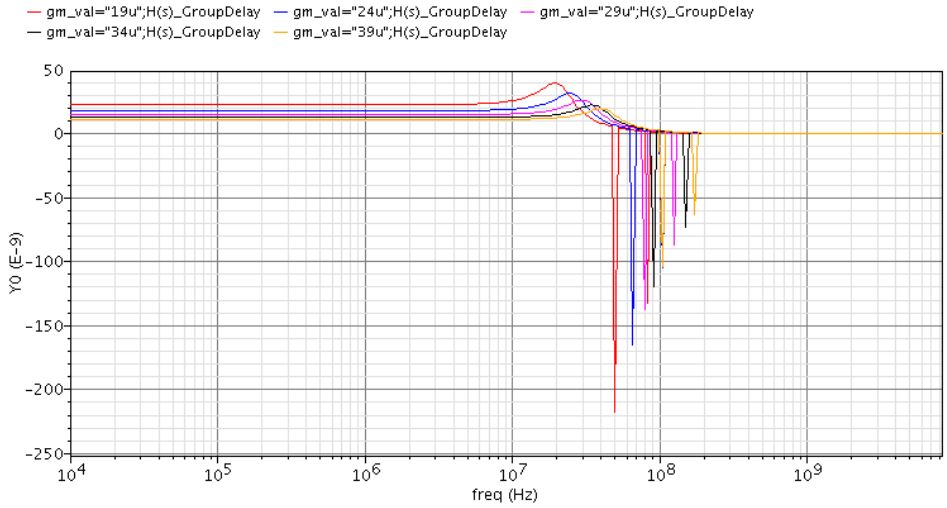

Figure 3.10 5th order inverse-Chebyshev filter group delay

3.2 The design of operational transconductance amplifier (OTA) circuit

The key challenge behind this filter is the operational transconductance amplifier design. OTA with a loaded capacitor forms an integrator. The integrator is the main building block in active filters. One of major problem in high-frequency applications is the phase error of the integrator. To keep the phase as close as possible to -90°, a wideband OTA with sufficiently high DC gain is needed. Otherwise Q-tuning circuit is needed to attenuate the Q enhancement effect. In order to avoid the use extra Q tuning circuit, high-performance OTAs are required. The technique employed in this project combine the cross-coupled input stage with the gain

boosting folded cascode output stage

The schematic of the input stage of OTA is shown in Figure 3.11. The schematic of output stage of OTA is shown in Figure 3.12.

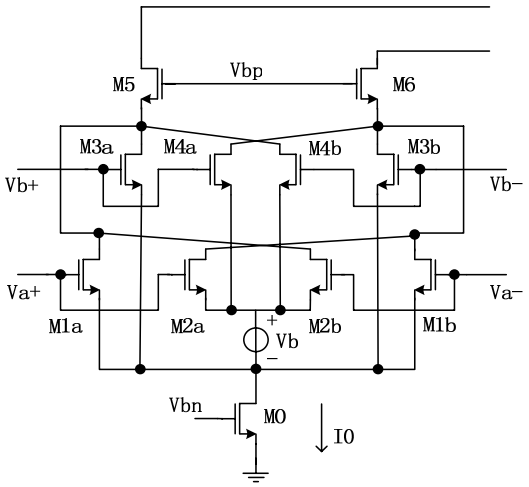

Figure 3.11 Input stage of OTA cell

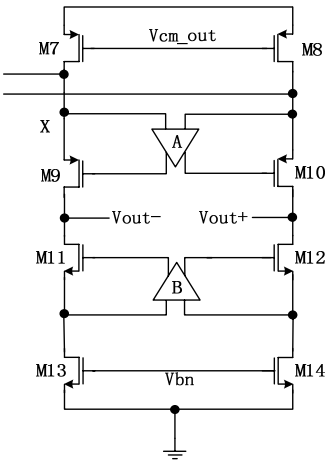

Figure 3.12 Output stage of OTA cell

The output stage shown in Figure 3.12 employs gain boosting cascode circuit, it consists of M7 to M14 and boosting amplifier A and B. Noted that the impedance seen from the node X is low because of M7 is in parallel with the output impedance of the input stage. In order to maintain the high impedance seen from node X, large device length is needed in M1a to M4b (shown in Figure 3.11) which results in a large parasitic capacitance. M5 and M6 is added to alleviate this problem, it can provide higher impedance as well as less capacitance seen from the

node X.

The output current of the transconductor can be expressed as:

$$I_1 = I_0 + \frac{I_{out}}{2} = I_{d1} + I_{d4} = K(V_P - V_T)^2 + K(V_N - V_B - V_T)^2 \quad (3.34)$$

$$I_2 = I_0 - \frac{I_{out}}{2} = I_{d2} + I_{d3} = K(V_N - V_T)^2 + K(V_P - V_B - V_T)^2 \quad (3.35)$$

Where $(I_{d1} + I_{d2}) + (I_{d3} + I_{d4}) = 2I_0,\ K = \frac{\mu_n C_{ox}}{2}\frac{W}{L},\ V_P = V_{a+}\ or\ V_{b+},\ V_N = V_{a-}\ or\ V_{b-}$

(3.37)

Therefore, if we make M1a to M4b have the same size which means they have the same K, the output current of the transconductor can be calculated as

$$I_{out} = I_1 - I_2 = 2\,KV_B \quad (3.38)$$

Noticed theoretically, all non-linear terms were cancelled which left a perfectly linear transfer function. And this transconductor is tunable by varying the floating DC voltage source V_B. If $r_{out} \neq 0$, it can be shown that the linear transfer function becomes nonlinear as

$$I_{out} = 2\,K[V_B + r_{outB}(I_{d3} + I_{d4})]V_{id} \quad (3.39)$$

Thus the resistance of the floating voltage source should be made as small as possible. The floating voltage source can be realized using a MOSFET operated in triode region. In order to lower the resistance of the voltage source, a large W/L ratio is preferred in implementation. For M1a to M4b to operate in saturation the linear range of V_{id} is limited by [16]

$$|V_{id}| \leq \sqrt{I_0/K - 3V_B^2/4} - V_B/2 \quad (3.40)$$

Differential output requires a common-mode feedback circuit to stabilize the operating point. As shown in Figure 3.12, V_{cm_out} is the common-mode feedback voltage generated by a common-mode feedback circuit, it stabilizes the common-mode output of the transconductor to a desired operating point. The common-mode feedback circuit is shown is Figure 3.13.

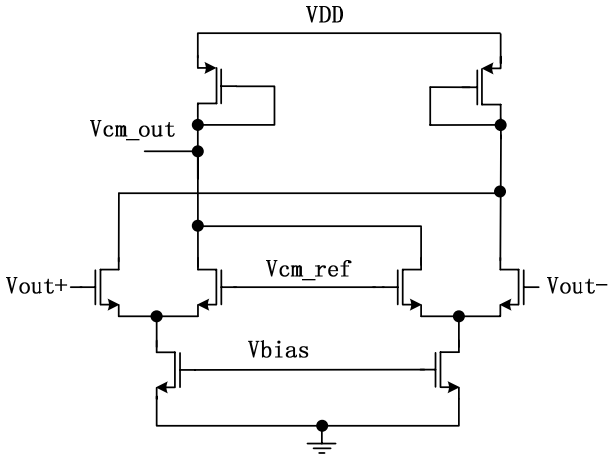

Figure 3.13 The schematic of transconductor cell

In Figure 3.12, amplifiers A and B are added to enhance the output impedance of the OTA, thus the gain of the transconductor can be also increased. This is desired because ideal OTA has infinite input and output impedance. The gain of the OTA amplifier is the product of transconductance and the output impedance, large output impedance will lead a large DC gain. Amplifiers A and B are differential input and differential output folded-cascode amplifier. The schematic of amplifier A and B together with their common-mode feedback are shown in Figure 3.14, the amplifier A is a folded-cascode amplifier with NFET input stage which is not shown.

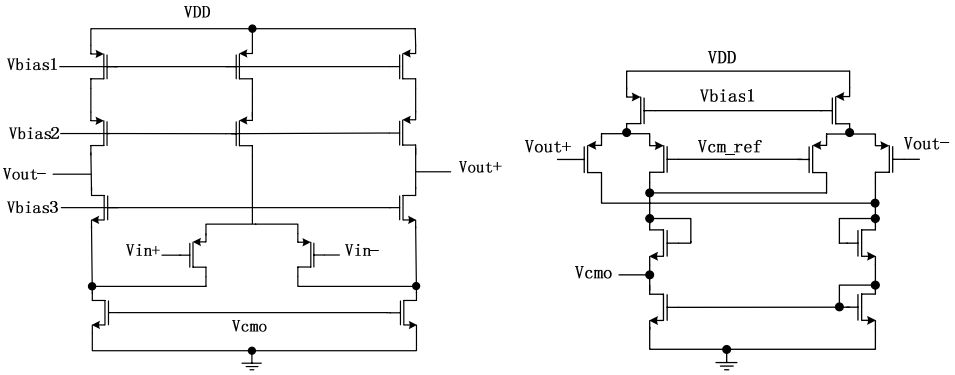

Figure 3.14 The schematic of amplifer B and its common-mode feedback circuit

In order to make the OTA with tunable transconductance, a controllable floating voltage source V_B is needed to provide bias offset of the circuit. The schematic of the floating voltage source is shown in Figure 3.15.

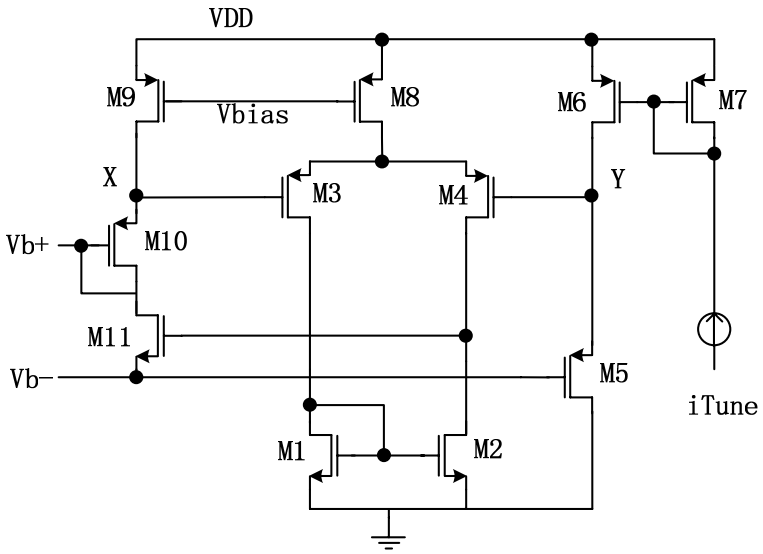

Figure 3.15 Floating voltage source V_B

The current mirror M1 – M4 and M8 force the voltage at node X and Y almost the same. The floating voltage source V_B is the voltage drop across M11 which can be approximately represented as (assuming node X and Y have the same voltage)

$$V_B = V_{b+} - V_{b-} = V_{sg5} - V_{sg10} \tag{3.41}$$

The source-gate voltage of M5 can be controlled by tuning iTune. And the tuning process is monotonously as long as the iTune is larger the current flowing through M9.

The transfer function of the filter depends on the pole and zero position. For gm-C filter, accurate frequency response requires the accurate value of transconductances and capacitances. This is hardly achieved in practice due to PVT variation. Thus, tuning circuit is needed to automatically tune the cutoff frequency to a desired value.

The tuning circuit designed in this work employs a commonly used master-slave tuning scheme. In this scheme, the tuning circuit (usually implemented by a simple phase locked loop) tunes the cutoff frequency of the master filter to a desired value by controlling the current flowing into the floating voltage source. And meanwhile, this control signal is feed into the slave filter which is the 5th order inverse-Chebyshev filter. Thus, the tuning accuracy is determined by the match between the master filter and slave filter.

Before we start to design the tuning circuit, we can examine the property of gm-C biquad. The master filter is a biquad using the same transconductance of the main filter. We redraw the gm-C biquad in Figure 3.16.

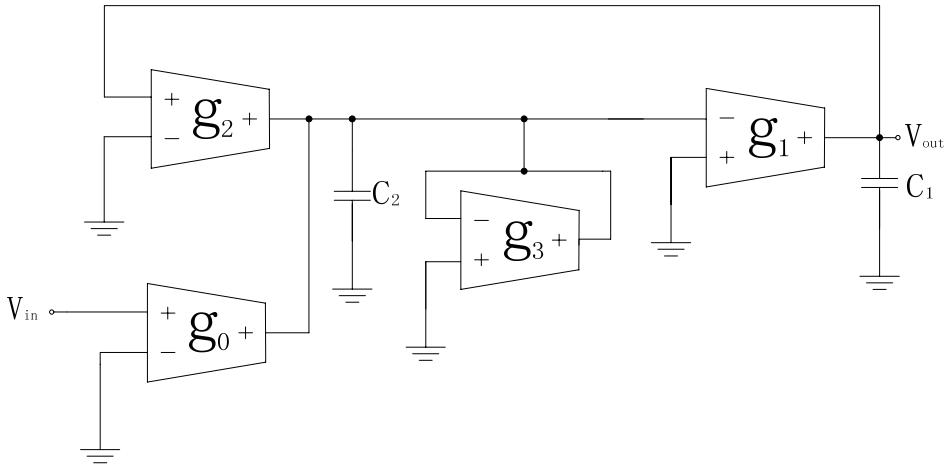

Figure 3.16 Gm-C biquad

The lowpass output transfer function of the biquad is shown below

$$H_{LP}(s) = \frac{V_{out}}{V_{in}} = \frac{-g_0 g_1}{s^2 C_1 C_2 + s g_3 C_1 + g_1 g_2} = \frac{-K_{LP}\omega_0^2}{s^2 + s(\omega_0/Q) + \omega_0^2} \quad (3.42)$$

When $s = j\omega_0$, equation (3.42) becomes

$$H_{LP}(s) = \frac{-K_{LP}\omega_0^2}{-\omega_0^2 + j\omega_0(\omega_0/Q) + \omega_0^2} = \frac{-K_{LP}Q}{j} = jK_{LP}Q \quad (3.43)$$

Thus when the input signal frequency is ω_0, the output signal in quadrature to its input. The tuning circuit can be built based on this property. The conceptual circuit of the tuning circuit is shown in Figure 3.17. The concept of the phase detector is shown in Figure 3.18.

In this work, the transconductance of the transonductor can be tuned by varying the voltage of the floating voltage source. And the voltage can be tuned by controlling the current feed into the voltage source.

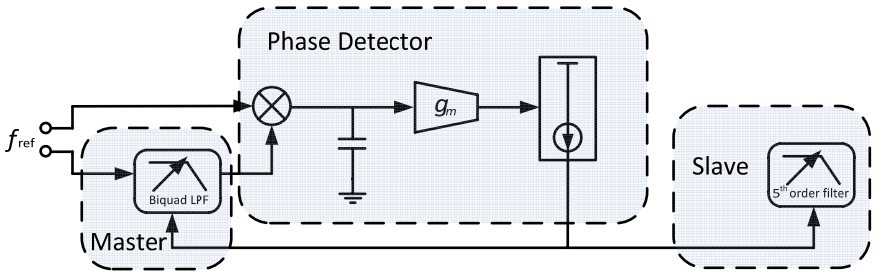

Figure 3.17 Concept of tuning circuit

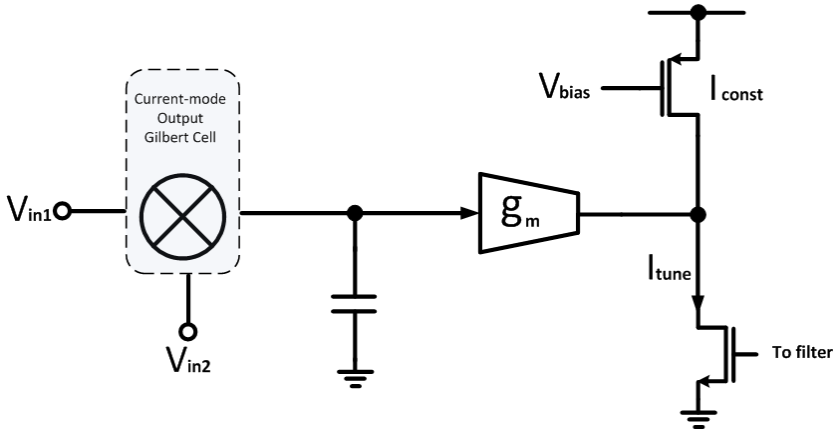

Figure 3.18 Concept of phase detector

In Figure 3.17 the current is generated from a controllable current source. The tuning process can be explained as follows.

One of two reference signals with frequency f_{ref} is directly feed into the mixer, the other reference signal is feed into the master biquad. The output of the biquad is then feed into the mixer. A capacitor is connected at the output of the mixer to convert the current into voltage as it acts like an integrator. This voltage signal is then feed into gm cell to convert voltage into current which feed into the biquad to control the cutoff frequency of the biquad. When the two inputs of the mixer are in quadrature, the output current of the mixer is zero. Then the voltage at the gm cell input is constant which produces a constant control current. Therefore, after the tuning process is over, the output of the biquad is locked in quadrature to its input.

The tuning range of the tuning circuit is determined by the bias current in gm cell. As shown in Figure 3.18, when the gm cell sinks all its bias current, iTune is the sum of Iconst and Ibias of gm. The ω_0 of biquad reaches its maximum value and the cutoff frequency of the biquad

reaches its maximum value. In contrast, when the gm cell damps all its bias current, iTune is the difference of Iconst and Ibias of gm. The ω_0 of biquad reaches its minimum value and the cutoff frequency of the biquad reaches its minimum value.

3.3 Simulation Results

The simulation result of the floating voltage source is shown in Figure 3.19. V_B can be tuned from 5mV to 112mV by varying itune from 10uA to 30uA. We just need a small value for V_B because we choose large W/L ratio for input stage which will result in large gm value, the gm value can be tuned by changing V_B and the simulation result will be shown next.

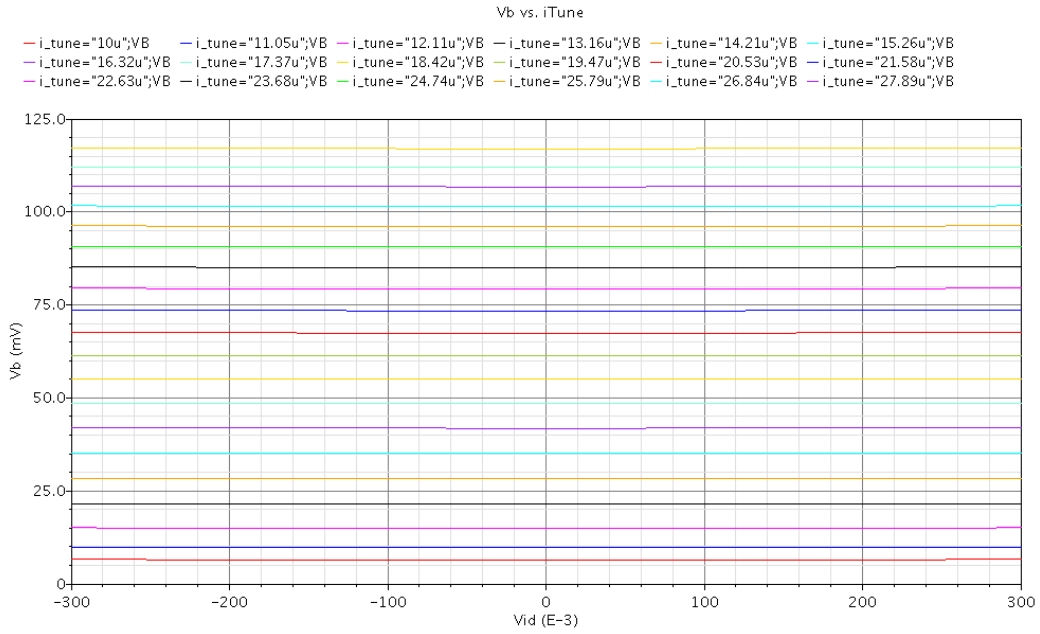

Figure 3.19 The tuning process of V_B

From Figure 3.19, we can see that Vb is almost linear over a large differential mode input swing. This is because the output impedance of the floating voltage source is small and the voltage drop caused by current flow through it can be considered constant.

With the tunable V_B, the transconductance of the gm cell can be tuned which makes the cutoff frequency of the filter to be reconfigurable. The tuning simulation of transconductance is

shown in Figure 3.20.

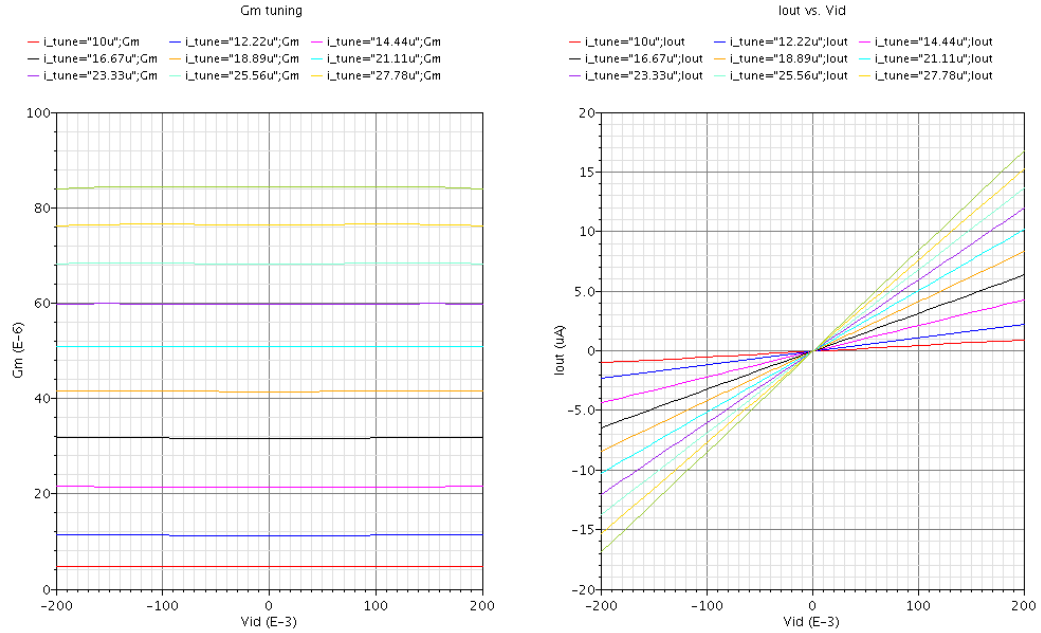

Figure 3.20 The tuning of G_m

As we can see in the Figure 3.20, Gm can be tuned from 5uS to 90uS. Each curve in the left figure represents different gm value versus differential mode input voltage. The curves shown in the right figure is the output current versus differential mode input voltage, the slope of each curve is the transconductancer which can be tuned by current. Generally, it exhibits good linearity over a wide range of differential input.

The frequency response of the OTA is important because it strongly affects the filter performance. The magnitude response and phase response over frequency of the OTA with gain enhancement is shown is Figure 3.21. The power supply of the OTA is 3.3V, it has a load capacitor equals to 700fF. The DC gain of the OTA increases as itune increases, this is because the transconductance increases as itune increases which produce a larger $g_m * r_{out}$. The large DC gain is the result of gain boosting amplifier employed in the output stage.

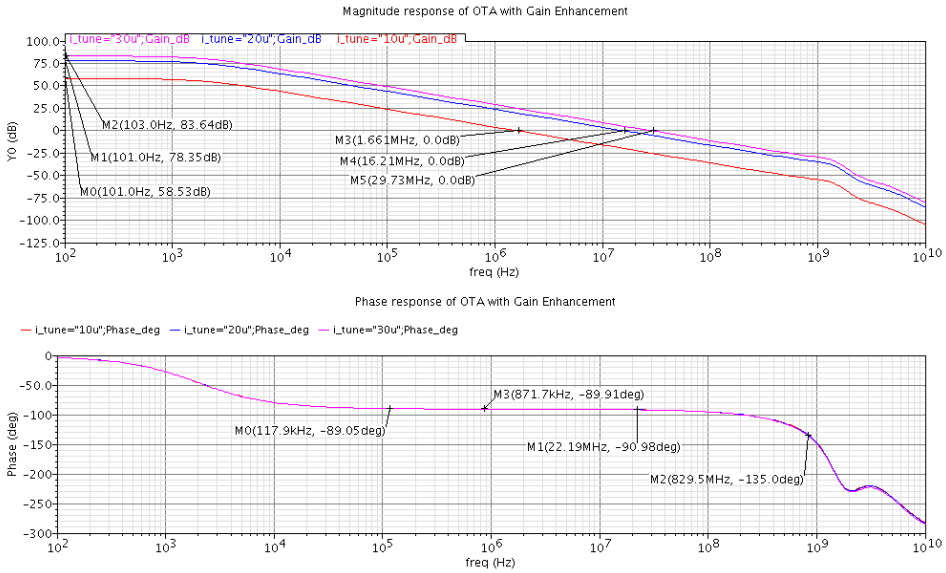

Figure 3.21 Frequency response of the OTA with gain enhancement

It is obvious that the phase response of the OTA is almost -90 degree over a wide frequency range. This is desired because the ideal integrator should have constant phase response of -90 degree in all frequency. The figure shows the transconductor with its capacitive load can be considered as an ideal integrator within a wide frequency range.

The frequency response of amplifier A and B are shown in Figure 3.22 and Figure 3.23. They were design to have large phase margin to push the second pole higher than the OTA second pole. Also the cutoff frequency of these two amplifiers needs to be assigned within a safe range.

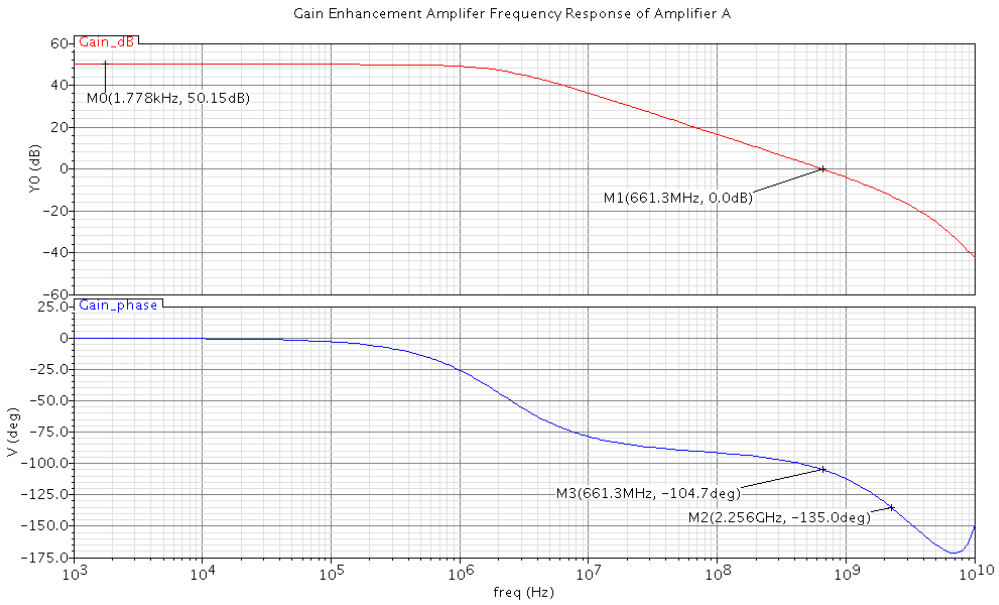

Figure 3.22 Frequnecy response of amplifier A

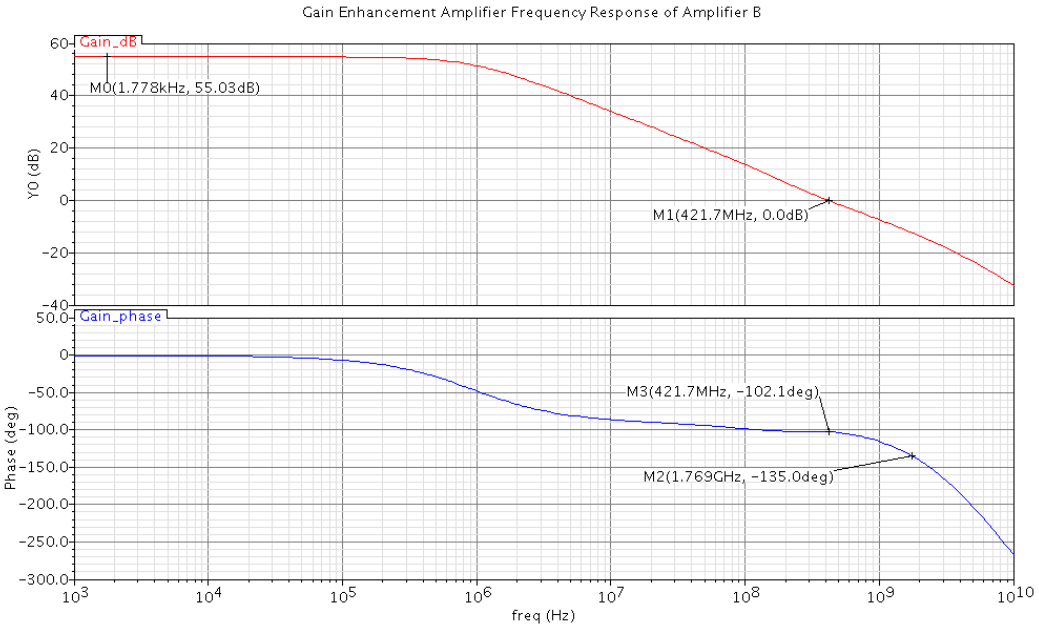

Figure 3.23 Frequnecy response of amplifier B

The cutoff frequency of the filter can be tuned from 4MHz to 40MHz. Two types of filter were simulated to show the performance of the tunable transconductor. The simulation result of the cutoff tuning process of inverse-Chebyshev type is shown in figure 3.24. The simulation of elliptic type is shown in figure 3.25.

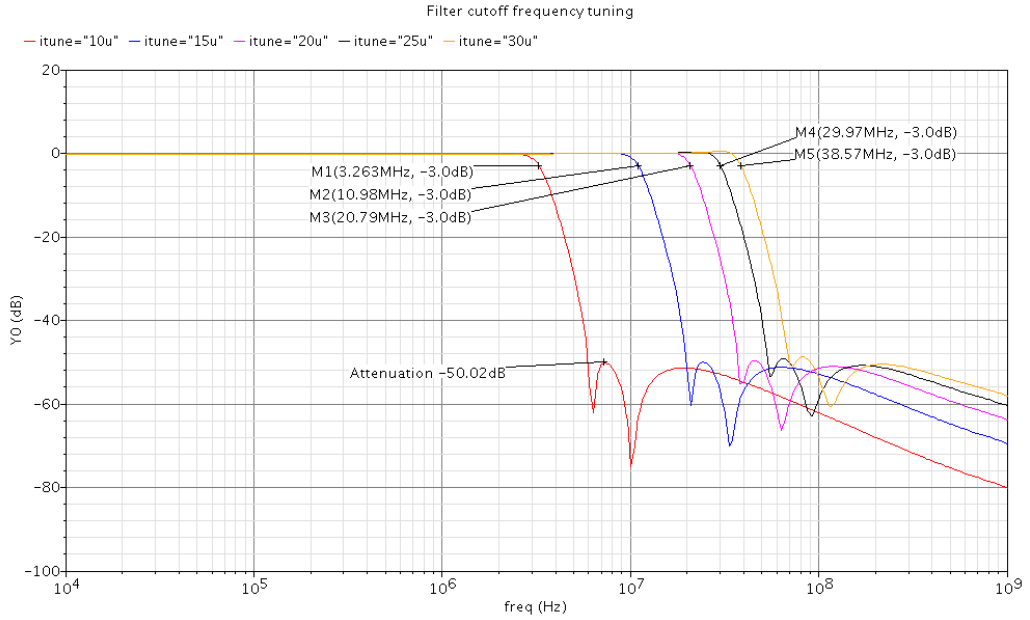

Figure 3.24 The cutoff frequency tuning of inverse-Chebyshev filter

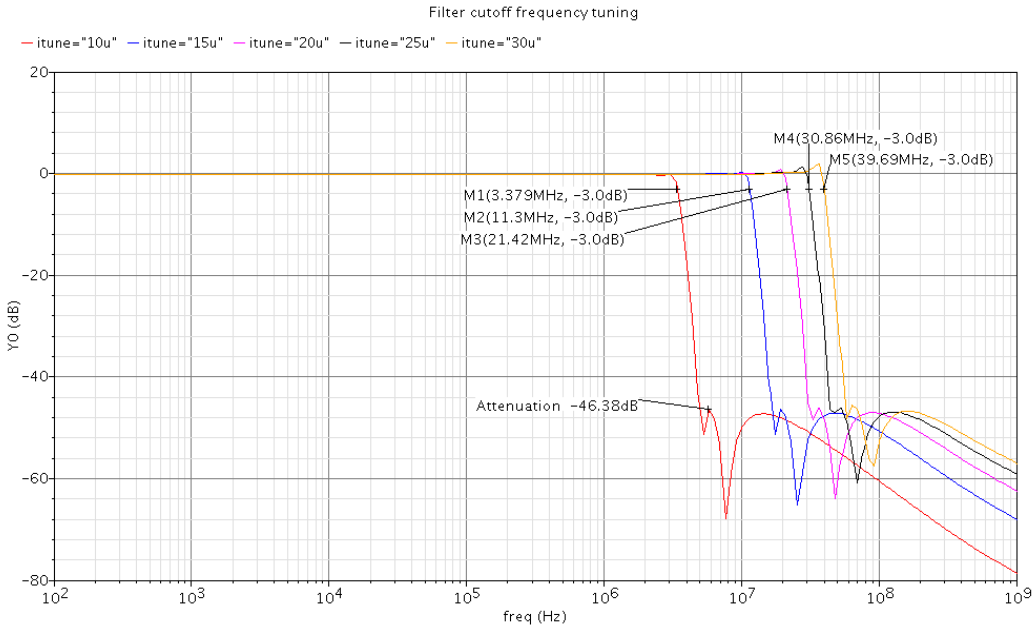

Figure 3.25 The cutoff frequency tuning of elliptic filter

Due to PVT variations, the cutoff frequency of the filter cannot be maintained to a desired value under all conditions. A tuning circuit is needed to compensate the PVT variations. The transient simulation result of the tuning circuit is shown in Figure 3.26.

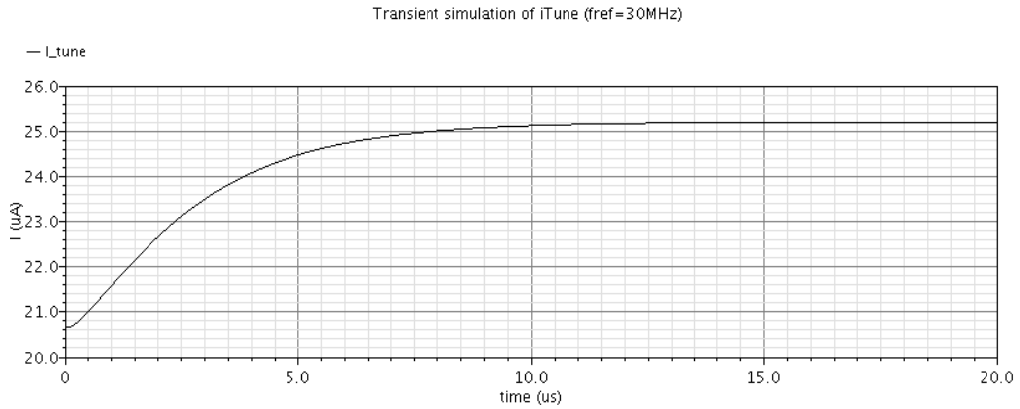

Figure 3.26 Transient simulation of iTune over temperature

Before the tuning starts, the iTune value is the constant current from the top current source shown in Figure 3.26. The input signal frequency is set to 30MHz, and at the beginning the output of the biquad is not in quadrature to the input of the biquad. This condition is shown in Figure 3.27.

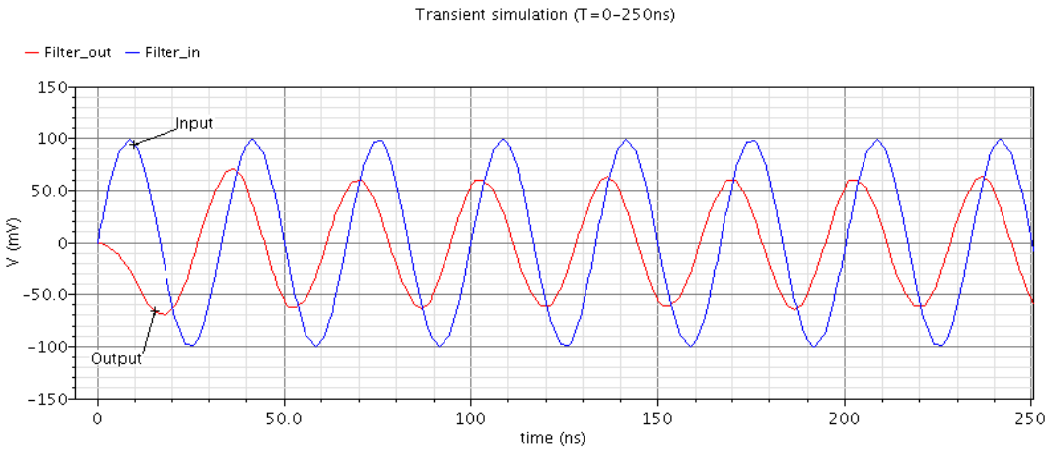

Figure 3.27 Transient simulation of input and output of biquad before tuning

For a 30MHz input signal, iTune needs to be larger than the constant bias from the current source. The feedback loop of the tuning circuit will force the output signal of biquad approaches quadrature position to its input signal. After the tuning process complete, the output signal and input signal of the biquad are in quadrature. The transient simulation result is shown in Figure 3.28.

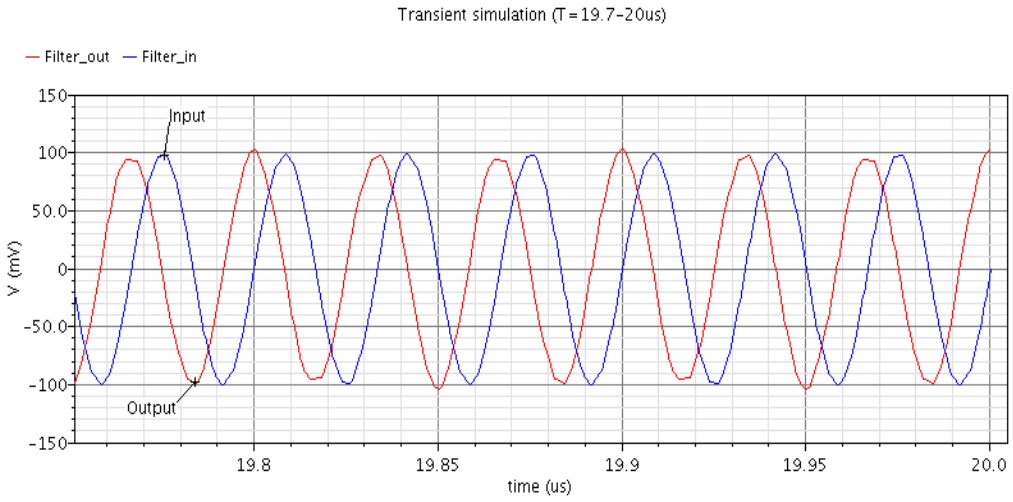

Figure 3.28 Transient simulation of input and output of biquad after tuning

As shown in Figure 3.28, the output and input signal of biquad are in quadrature after tuning is complete.

Another important property introduced by tuning circuit is it should compensate the PVT variations. The transient simulation of the iTune from the tuning circuit over temperature is shown in Figure 3.29.

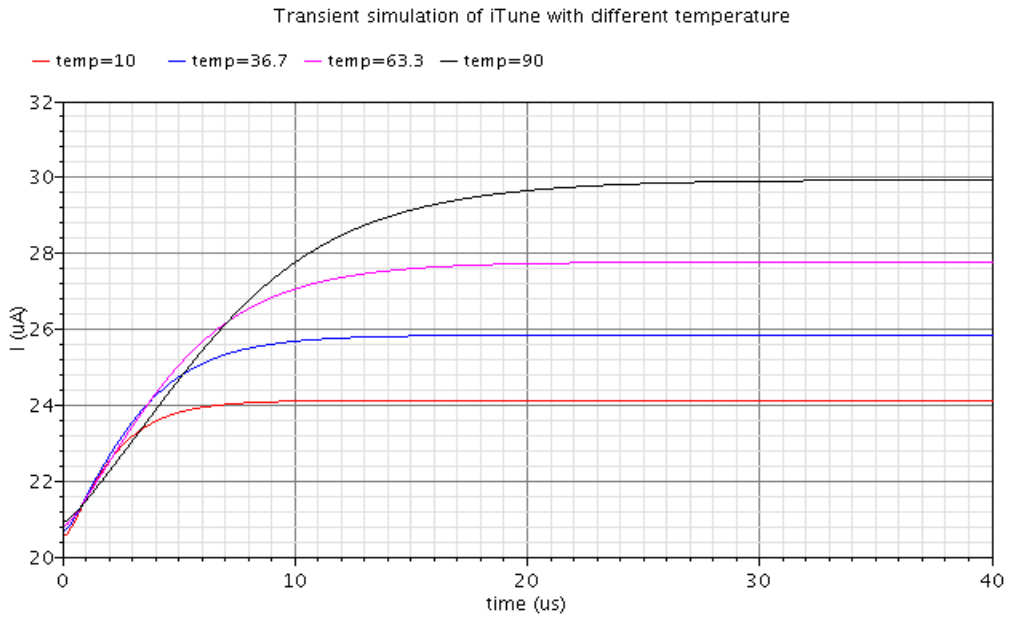

Figure 3.29 Transient simulation of iTune over temperature

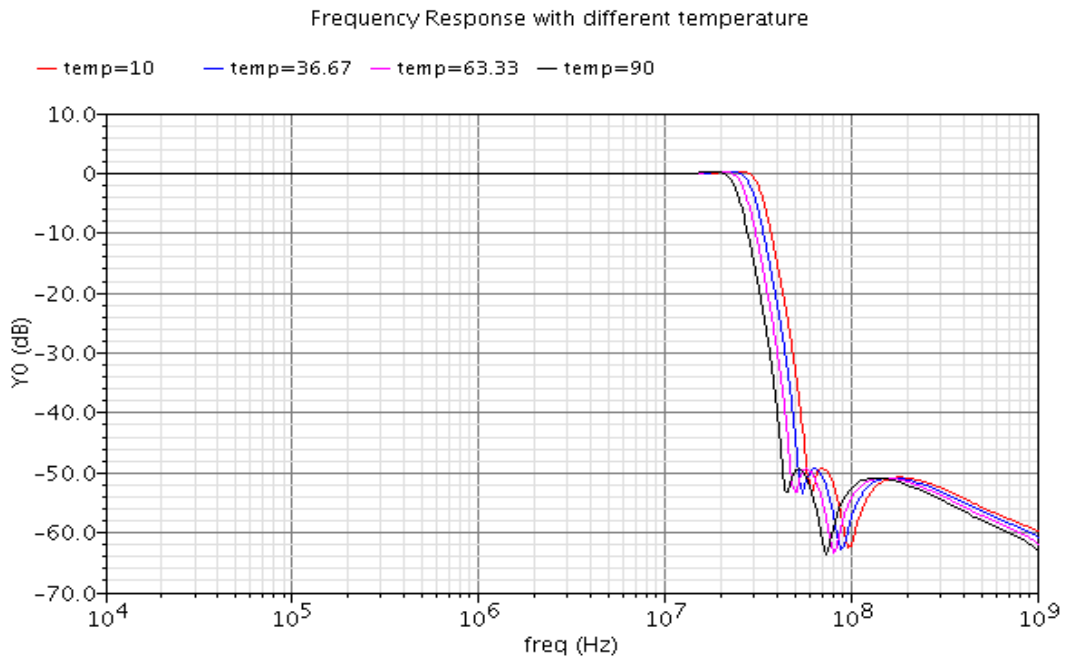

Figure 3.30 Cutoff frequency of the filter over temperature without tuning circuit

Figure 3.30 shows the simulation result of cutoff frequency over temperature without tuning circuit, it can be seen that the cutoff frequency varies with temperature. When the temperature varies from 10℃ to 90 ℃, the variations of cutoff frequency is about 10MHz. This large cutoff frequency variation is intolerable in many applications. With the tuning circuit, the cutoff frequency can be locked to a desired value. The simulation result of cutoff frequency over temperature with tuning circuit is shown in Figure 3.31.

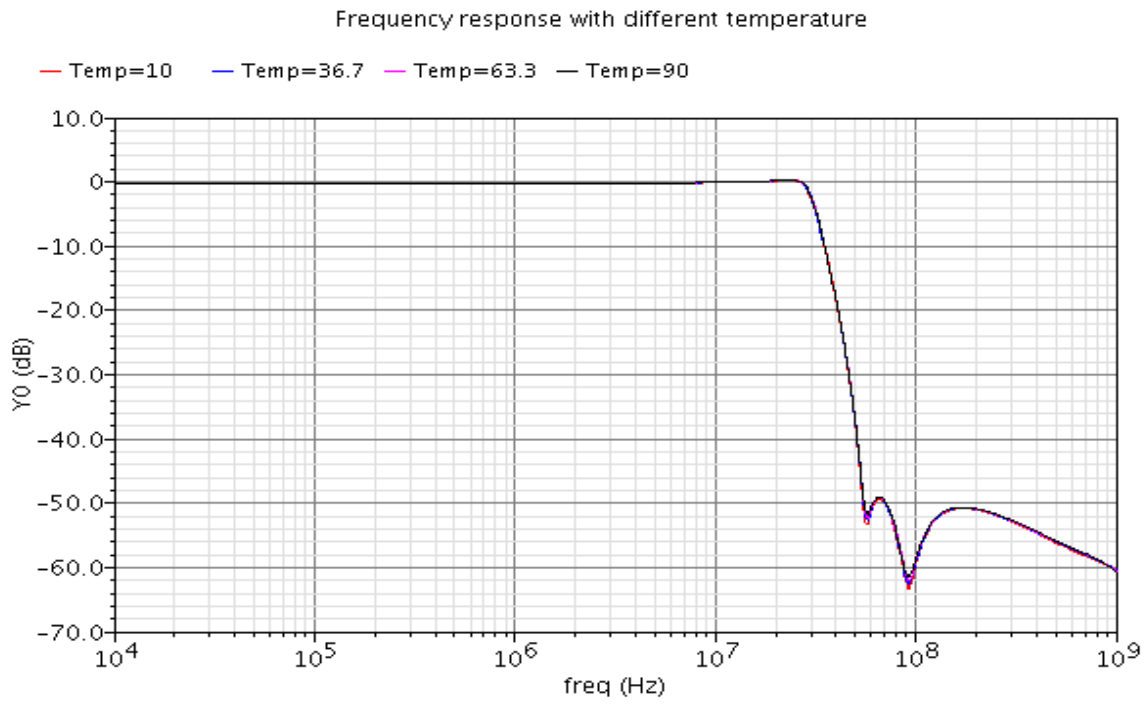

Figure 3.31 Cutoff frequency of the filter over temperature with tuning circuit

3.4 Bandgap circuit

A bandgap circuit is designed to provide the reference voltage to the filter. The schematic of the bandgap circuit is shown in Figure 3.32.

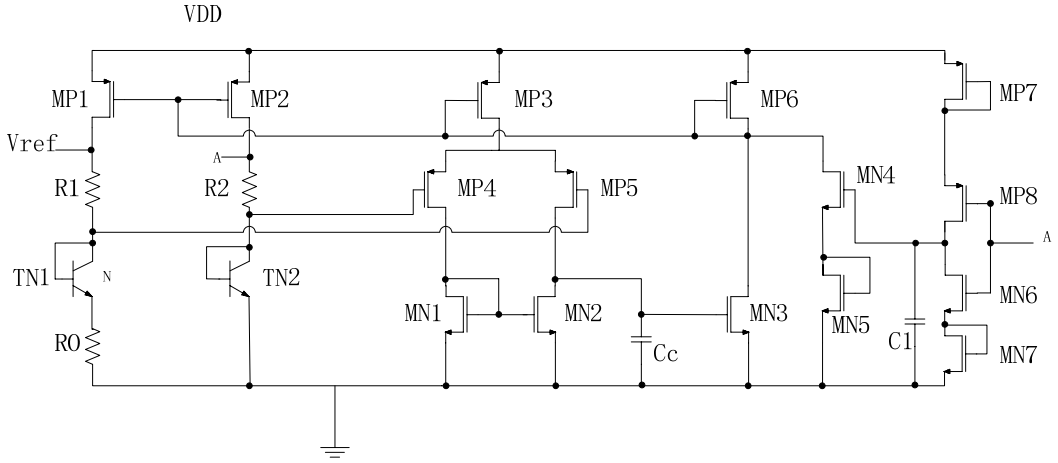

Figure 3.32 Bandgap Circuit schematic

The emitter area of TN1 is N times larger than TN2. MP3-MP6 and MN1-MN2 forms an operational amplifier which provides negative feedback to force the collector voltage of TN1 and TN2 the same.

ΔV_{BE} is extracted on R0 and voltage across R0 is PTAT (proportional to absolute temperature) voltage. Correspondingly, the current flow through R0 is PTAT. The voltage drop across R1 is (ΔV_{BE}/R0)*R1 which is also a PTAT voltage. The voltage at the collector of TN1 is V_{BE} which is a CTAT (complementary to absolute temperature) voltage. Therefore the DC value of V_{ref} can be expressed as

$$V_{ref} = V_{BETN2} + (R_1/R_0)V_t lnN \tag{3.44}$$

By properly ratio the R_1 *and* R_0, we can have V_{ref} with zero temperature coefficient at desired temperature.

In order to acquire more insight to improve PSR of this circuit, it is necessary to analyze the small signal model of this circuit. The small signal model of the bandgap is shown in Figure 3.33.

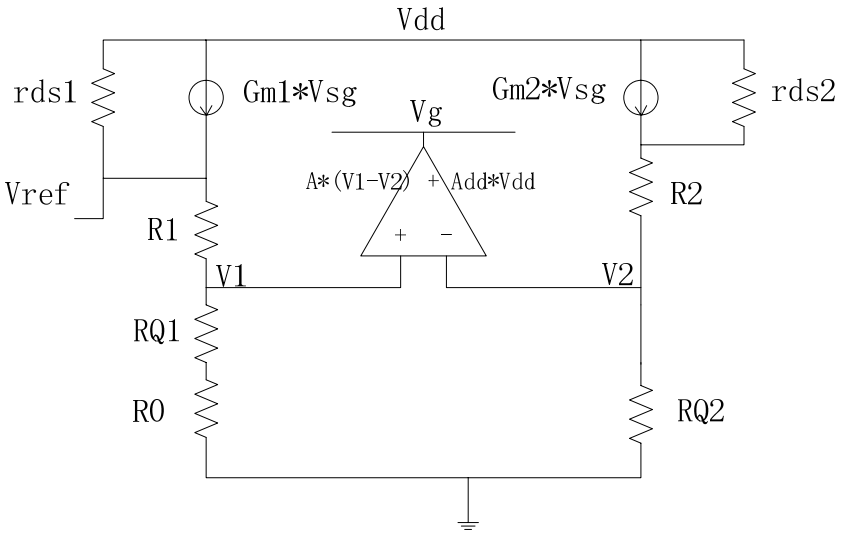

Figure 3.33 Bandgap small signal circuit

Based on the small signal model shown above, we can have the following equations

$$V_g = A(V_1 - V_2) + A_{dd}V_{dd} \tag{3.45}$$

$$V_1 = g_{m1}(V_{dd} - V_g)(R_{Q1} + R_0) \tag{3.46}$$

$$V_2 = g_{m2}(V_{dd} - V_g)R_{Q2} \tag{3.47}$$

where A is the differential gain of the operational amplifier, A_{dd} is gain from V_{dd} to the

output of the operational amplifier. R_{Q1} and R_{Q2} are the output impedance of two NPN transistors TN1 and TN2 respectively.

Substitute equation (3.45) (3.46) into (3.47), we have

$$V_g = A[g_{m1}(V_{dd} - V_g)(R_{Q1} + R_0) - g_{m2}(V_{dd} - V_g)R_{Q2}] + A_{dd}V_{dd} \quad (3.48)$$

Rearrange equation (3.48), V_g can be expressed as

$$V_g = [V_{dd} - \frac{V_{ref}}{g_{m1}(R_1+R_0+R_{Q1})}] \quad (3.49)$$

Replace V_g in equation (3.49) and rearrange gives

$$\frac{V_{ref}}{V_{dd}} = \frac{(R_{Q2}+R_2)g_{m1,2}(1-A_{dd})}{1+A*g_{m1,2}(R_{Q1}+R_0-R_{Q2})} \approx \frac{(R_{Q2}+R_2)(1-A_{dd})}{A*(R_0-R_{Q2})} \quad (3.50)$$

Based on the equation above, it is obvious that a large gain of operational amplifier will result in better PSR. Also noted that when $A_{dd} = 1$, the PSR will be ideally infinite. Thus to acquire a better PSR without adding more complexity of the circuit, we can just tie the output of opamp directly to the gate of its current source, and as shown in Figure 3.33, the gate of PMOS current mirror in bandgap core is also the output of the opamp.

Another way to examine the circuit is by observing MP6 and MN3 forms a subtractor, it directly feed the noise from VDD to the output of the opamp. This leads to a low PSR of opamp which is exactly what we needed to improve bandgap PSR. The PSR of the opamp can be approximated as

$$A_{dd} = \frac{V_{out,opamp}}{V_{dd}} = \frac{R_{o,MN3}}{1/g_{m,MP6}+R_{o,MN3}} \quad (3.51)$$

Usually $R_{o,MN3}$ dominated which gives the above equation approximated equals to 1, this matches the analysis of PSR improvement of bandgap circuit.

The compensation of the opamp is done by connecting C_C between the drain of MN2 to ground. Miller compensation is not employed here because the second stage gain of the opamp is very small. Thus miller capacitor will not be amplified very much and plus there is a right half

plane zero (RHZ) introduced in the circuit which requires a series resistor to perform zero cancellation. The connection shown in Figure 3.33 provides reasonable PSR of bandgap circuit (typical value 98dB) and consumes little power (<0.36mW). The PSR simulation result is shown in Figure 3.39. The closed-loop phase margin simulation result is shown in Figure 3.42.

Noise analysis can be performed by examining the small-signal model of the bandgap. The small-signal model is shown in Figure 3.34 below. The noise simulation result is shown in Figure 3.50.

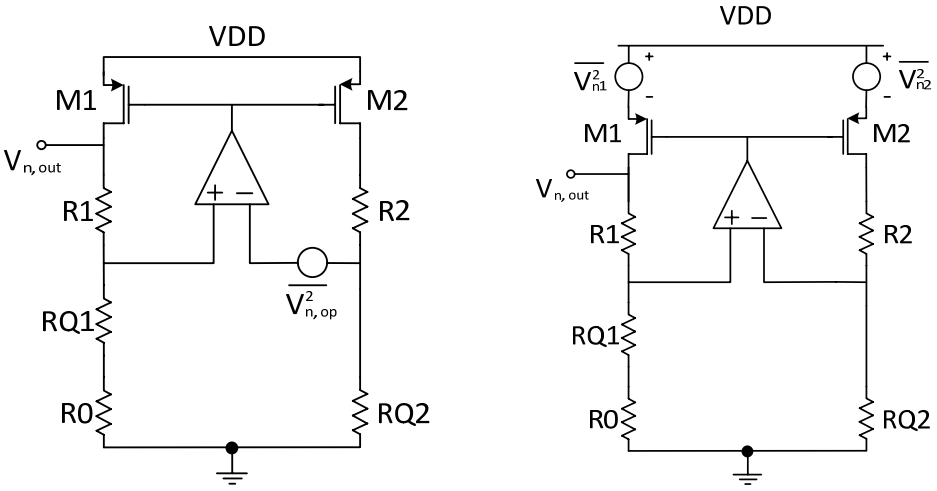

Figure 3.34 Small signal model for noise analysis

The impact of noise from the operational amplifier is analyzed first, based on the small-signal model shown in Figure 3.34, we have

$$I_{d1} = I_{d2} = \frac{V_{n,out}}{R_1+R_{Q1}+R_0} \tag{3.52}$$

$$V_{sg1} = V_{sg2} = \frac{1}{g_{mp}} \frac{V_{n,out}}{R_1+R_{Q1}+R_0} \tag{3.53}$$

The differential input of operational amplifier is

$$V_{diff,op} = \frac{1}{g_{mp}} \frac{1}{A_0} \frac{V_{n,out}}{R_1+R_{Q1}+R_0} \tag{3.54}$$

Where A_0 is the gain of the opamp.

$$V_{n,out} = \frac{V_{n,out}*R_1}{R_1+R_{Q1}+R_0} + \frac{1}{g_{mp}} * \frac{1}{A_0} * \frac{V_{n,out}}{R_1+R_{Q1}+R_0} + V_{n,op} + \frac{V_{n,out}*R_{Q2}}{R_1+R_{Q1}+R_0} \tag{3.55}$$

Rearrange gives

$$V_{n,out} = V_{n,op}/(1 - \frac{R_1+R_{Q2}}{R_1+R_{Q1}+R_0} - \frac{1}{g_{mp}} * \frac{1}{A_0} * \frac{1}{R_1+R_{Q1}+R_0}) \approx V_{n,op} \tag{3.56}$$

Thus, the noise from operational amplifier directly appears at the output. The noise from

the PMOS current mirror is analyzed as follows, we consider M1 first,

$$I_{d1} = \frac{V_{n,out}}{R_1+R_{Q1}+R_0} \tag{3.57}$$

$$V_{sg1} = \frac{1}{g_{mp}} * \frac{V_{n,out}}{R_1+R_{Q1}+R_0} \tag{3.58}$$

$$V_{diff,op} = (\frac{1}{g_{mp}} \frac{V_{n,out}}{R_1+R_{Q1}+R_0} + V_{n1})/A_0 \tag{3.59}$$

$$I_{d2} = (V_{n,out} - \frac{V_{n,out}*R_1}{R_1+R_{Q1}+R_0} - \frac{\frac{1}{g_{mp}} \frac{V_{n,out}}{R_1+R_{Q1}+R_0}+V_{n1}}{A_0})/R_{Q2} \tag{3.60}$$

$$V_{sg2} = \frac{1}{g_{mp}} * (V_{n,out} - \frac{V_{n,out}*R_1}{R_1+R_{Q1}+R_0} - \frac{\frac{1}{g_{mp}} \frac{V_{n,out}}{R_1+R_{Q1}+R_0}+V_{n1}}{A_0})/R_{Q2} \tag{3.61}$$

$$V_{n1} + V_{sg1} = V_{sg2} \tag{3.62}$$

Thus we have the output noise contribution from the M1,

$$V_{n,out} = \frac{-V_{n1}(1+\frac{1}{g_{mp}R_{Q2}A_0})}{\frac{1}{g_{mp}*(R_1+R_{Q1}+R_0)} - [\frac{R_{Q2}+R_0}{R_1+R_{Q1}+R_0} - \frac{1}{A_0(R_1+R_{Q1}+R_0)}]\frac{R_{Q2}}{g_{mp}}} \tag{3.63}$$

Next we consider the noise from M2,

$$I_{d1} = \frac{V_{n,out}}{R_1+R_{Q1}+R_0} \tag{3.64}$$

$$V_{sg1} = \frac{1}{g_{mp}} * \frac{V_{n,out}}{R_1+R_{Q1}+R_0} \tag{3.65}$$

$$V_{diff,op} = (\frac{1}{g_{mp}} * \frac{V_{n,out}}{R_1+R_{Q1}+R_0})/A_0 \tag{3.66}$$

$$I_{d2} = (V_{n,out} - \frac{V_{n,out}}{R_1+R_{Q1}+R_0} * R_1 - \frac{\frac{1}{g_{mp}}*\frac{V_{n,out}}{R_1+R_{Q1}+R_0}}{A_0})/ R_{Q2} \tag{3.67}$$

$$V_{sg1} = V_{sg2} + V_{n2} \tag{3.68}$$

$$\frac{1}{g_{mp}} * \frac{V_{n,out}}{R_1+R_{Q1}+R_0} = \frac{V_{n,out} - \frac{V_{n,out}}{R_1+R_{Q1}+R_0}*R_1 - \frac{\frac{1}{g_{mp}}*\frac{V_{n,out}}{R_1+R_{Q1}+R_0}}{A_0}}{R_{Q2}} * \frac{1}{g_{mp}} + V_{n2} \tag{3.69}$$

Thus the output noise due to V_{n2} is calculated as follows

$$V_{n,out} = V_{n2}/(\frac{1}{g_{mp}} * \frac{1}{R_1+R_{Q1}+R_0} - \frac{1}{R_{Q2}*g_{mp}} + \frac{1}{R_1+R_{Q1}+R_0} * R_1 * \frac{1}{R_{Q2}*g_{mp}} + \frac{\frac{1}{g_{mp}}*\frac{1}{R_1+R_{Q1}+R_0}}{A_0} * \frac{1}{R_{Q2}*g_{mp}}) \tag{3.70}$$

Where $V_{n1} = V_{n2} = \sqrt{\frac{8kT}{3g_{mp}} + \frac{k_x}{WLC_{ox}*f}}$

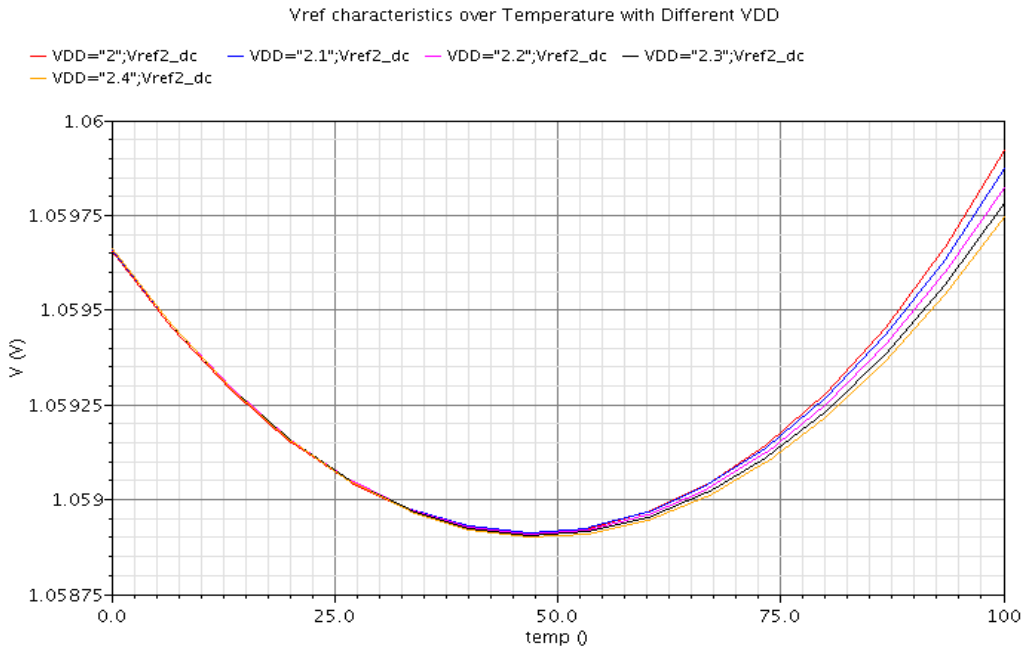

Figure 3.35 Vref vs. Temperature with VDD sweep

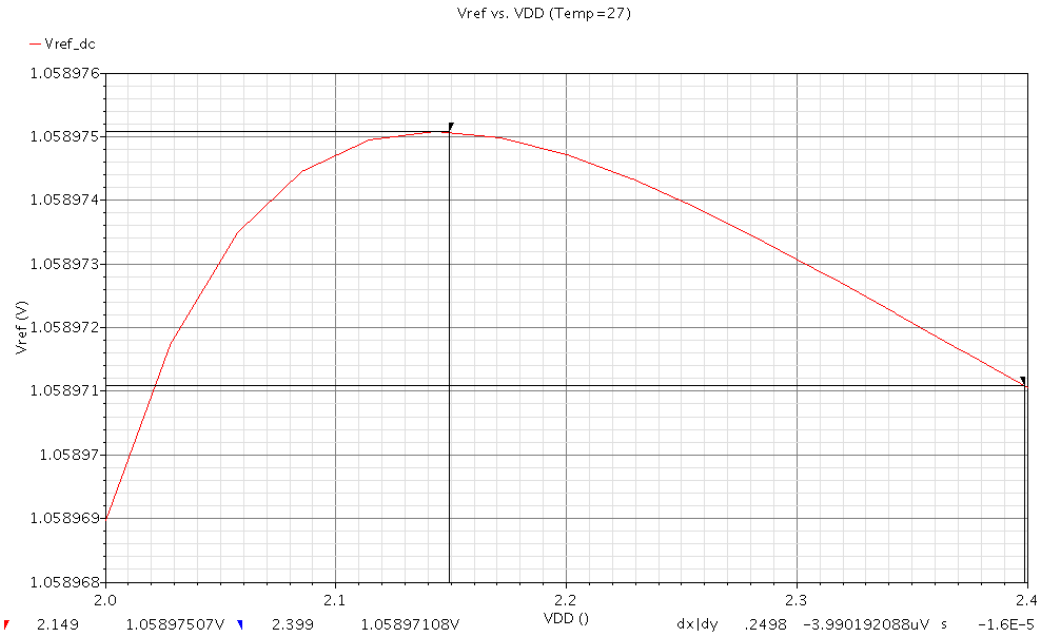

Figure 3.36 Vref vs. VDD (Temperature = 27℃)

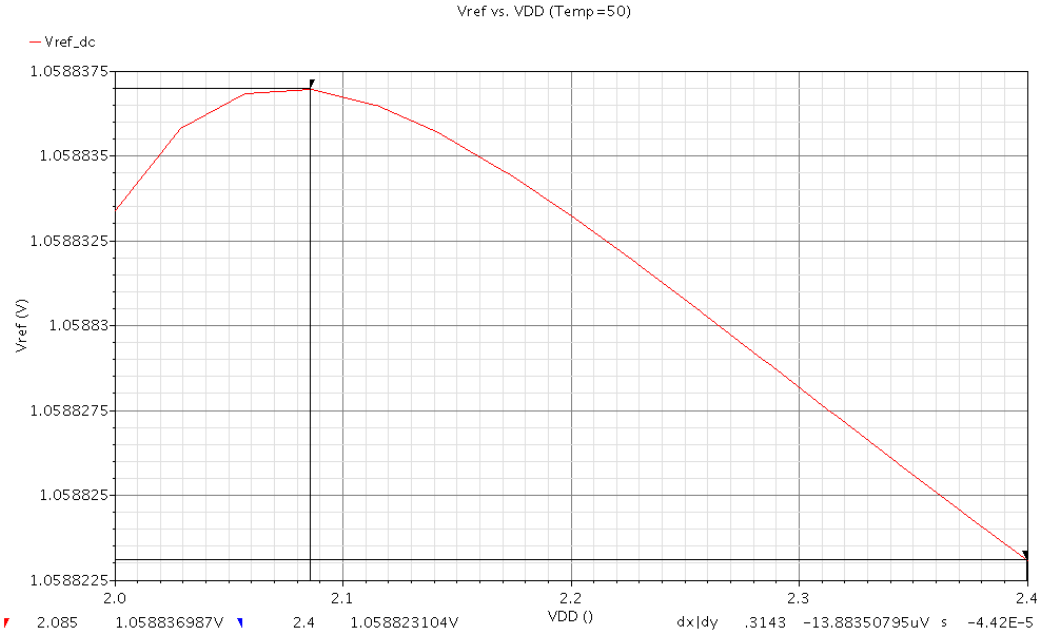

Figure 3.37 Vref vs. Temperature with VDD sweep Vref vs. VDD (Temperature = 50℃)

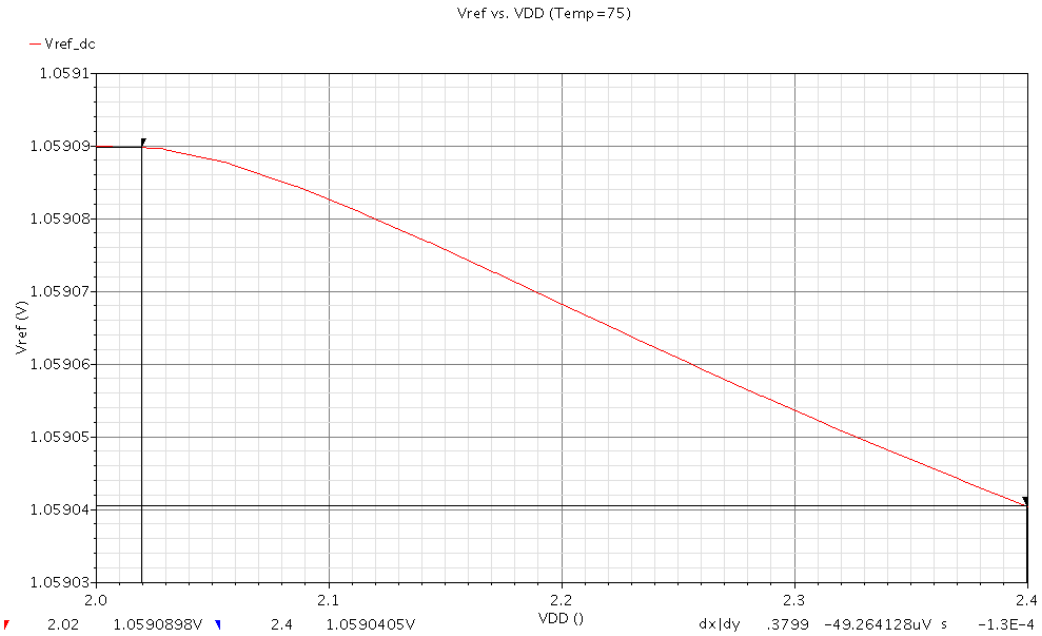

Figure 3.38 Vref vs. VDD (Temperature = 75℃)

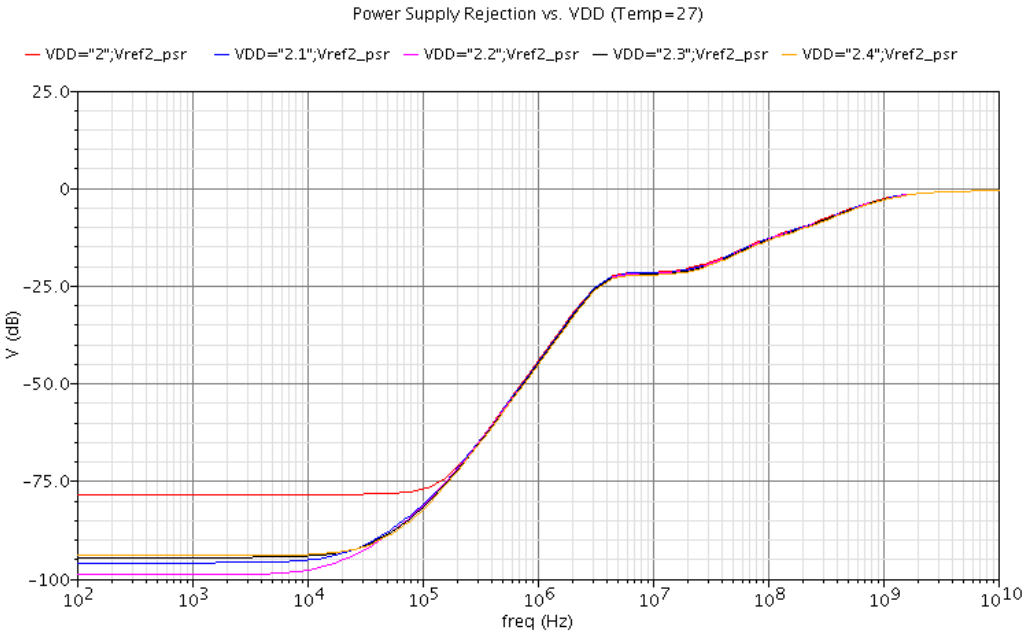

Figure 3.39 PSR vs. VDD (Temperature = 27℃)

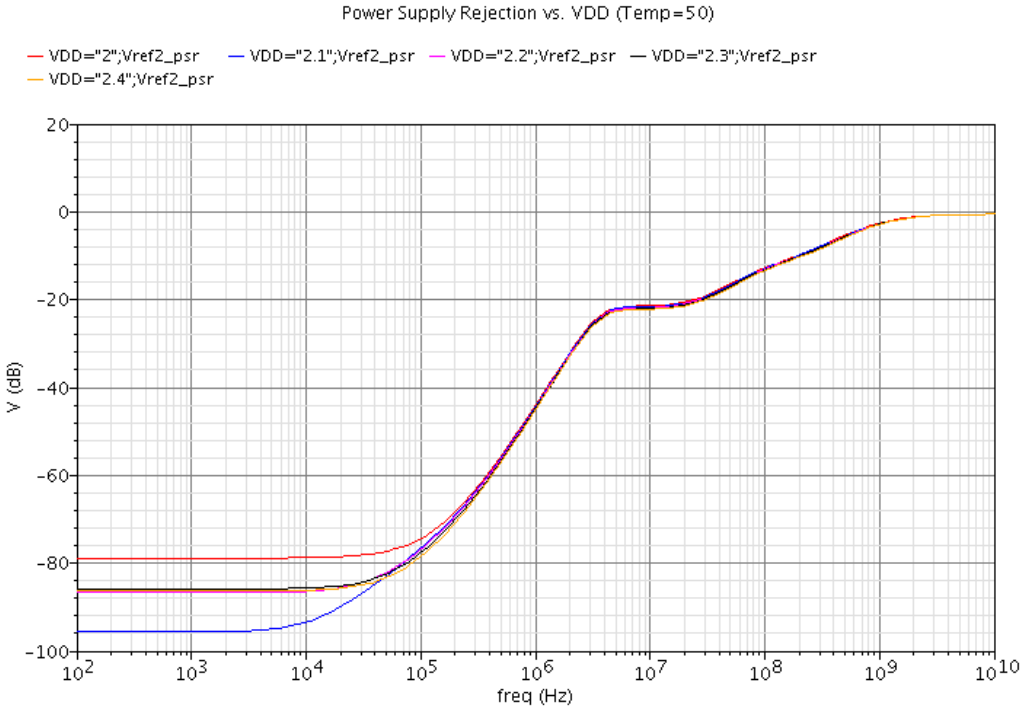

Figure 3.40 PSR vs. VDD (Temperature = 50℃)

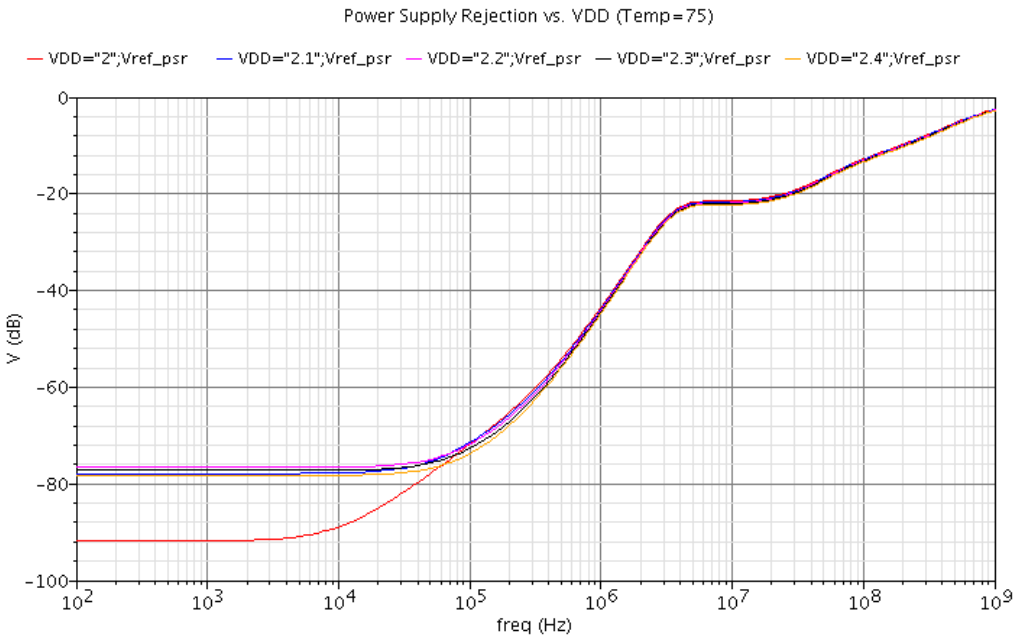

Figure 3.41 PSR vs. VDD (Temperature = 70℃)

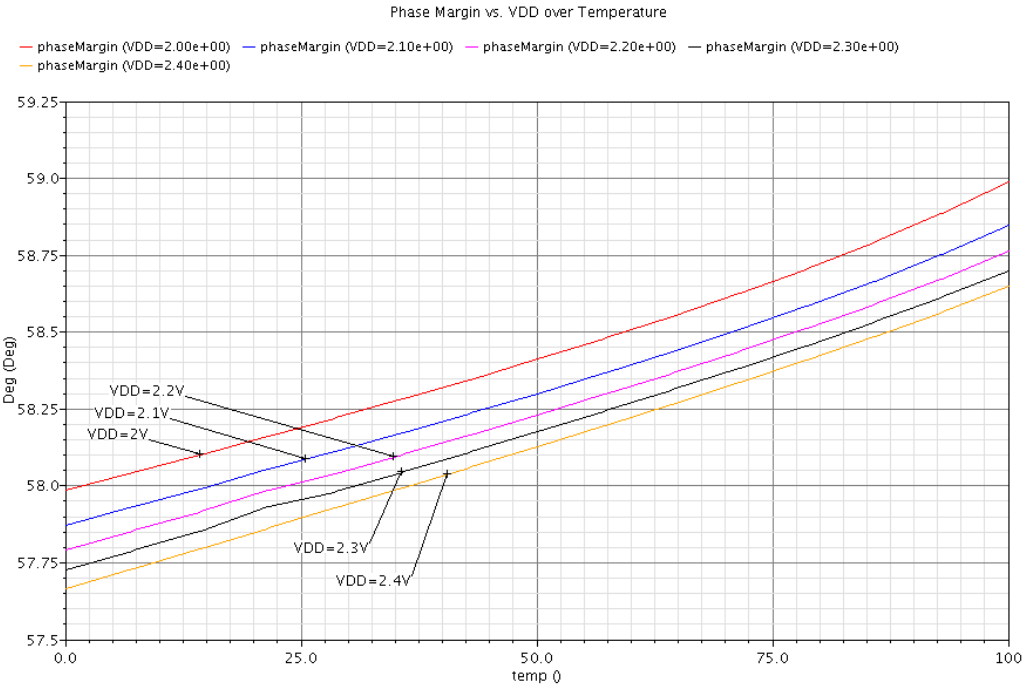

Figure 3.42 Closed-Loop Phase Margin vs. VDD over Temperature

To be able to make the circuit function properly when power up, a start-up circuit is needed to move the circuit to its correct operating point. The start-up circuit should not affect the main circuit when start up finished. Transistor MN4-7 and MP7-8 consists the start-up circuit. At

the very first when power up, the voltage at A is low, this drives the inverter (MN6-7, MP7-8) output to a high voltage which increase the gate voltage of MN4. Thus MN4 turns on, pull down the gate voltage of all the current sources and start the main circuit. Then the voltage A will increase to its typical voltage (equals to Vref) which turns the output of the inverter to a low voltage which turns off MN4. This disconnected the start-up circuit from the main circuit. Transistor MN5, MN7 and MP7 are used to provide enough threshold voltage to make the startup circuit working properly. The transient simulation result with and without start-up circuit is shown in Figure 17. Transient simulation including ramp up VDD very quick (1ns) and slow (3us), this simulation also cover three typical operating temperature (27℃, 50℃, 75℃). Typical Vref = 1.059V.

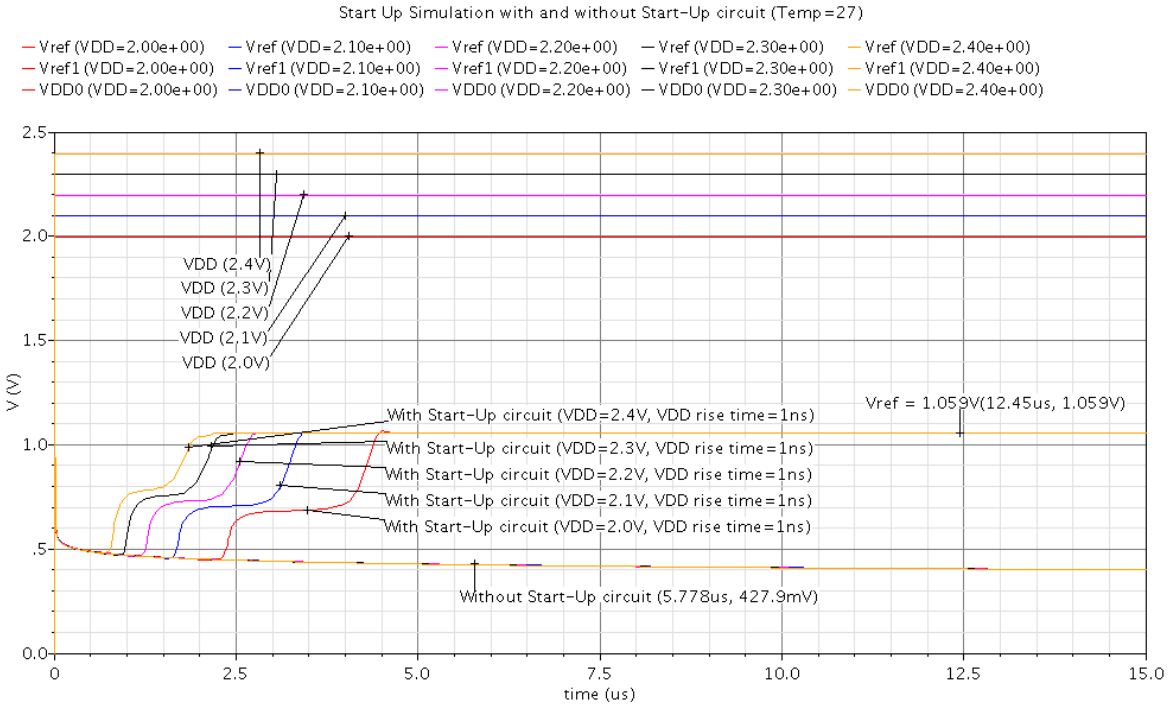

Figure 3.43 Transient simulation (VDD rise time=1ns, Temp = 27℃)

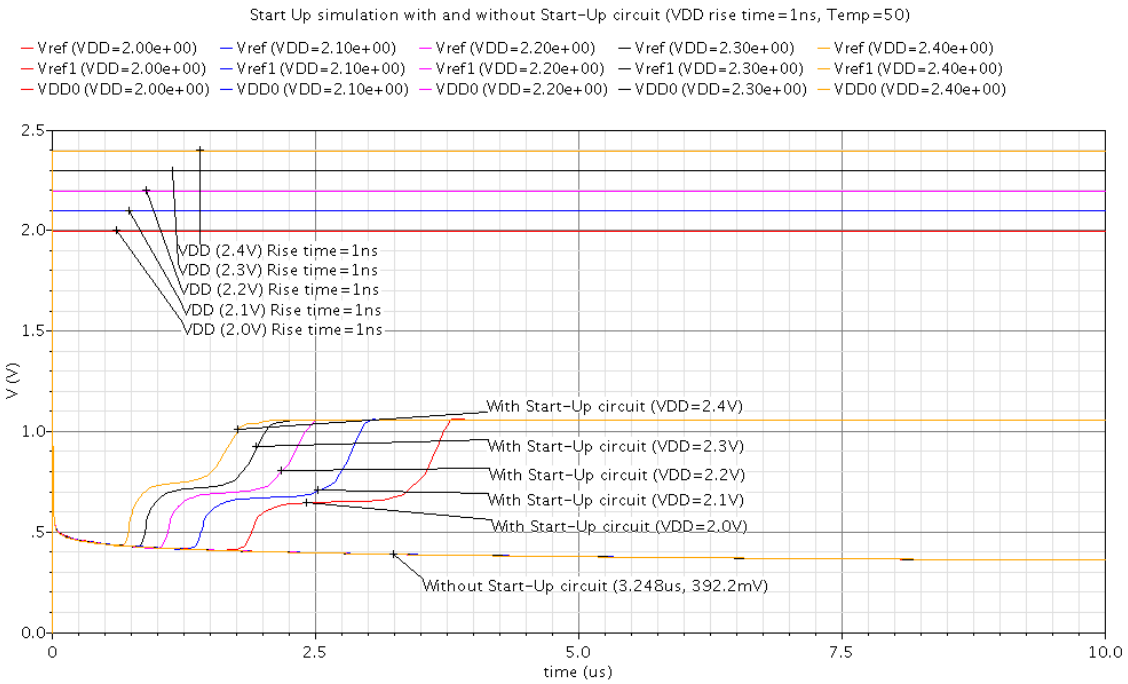

Figure 3.44 Transient simulation (VDD rise time=1ns, Temp = 50℃)

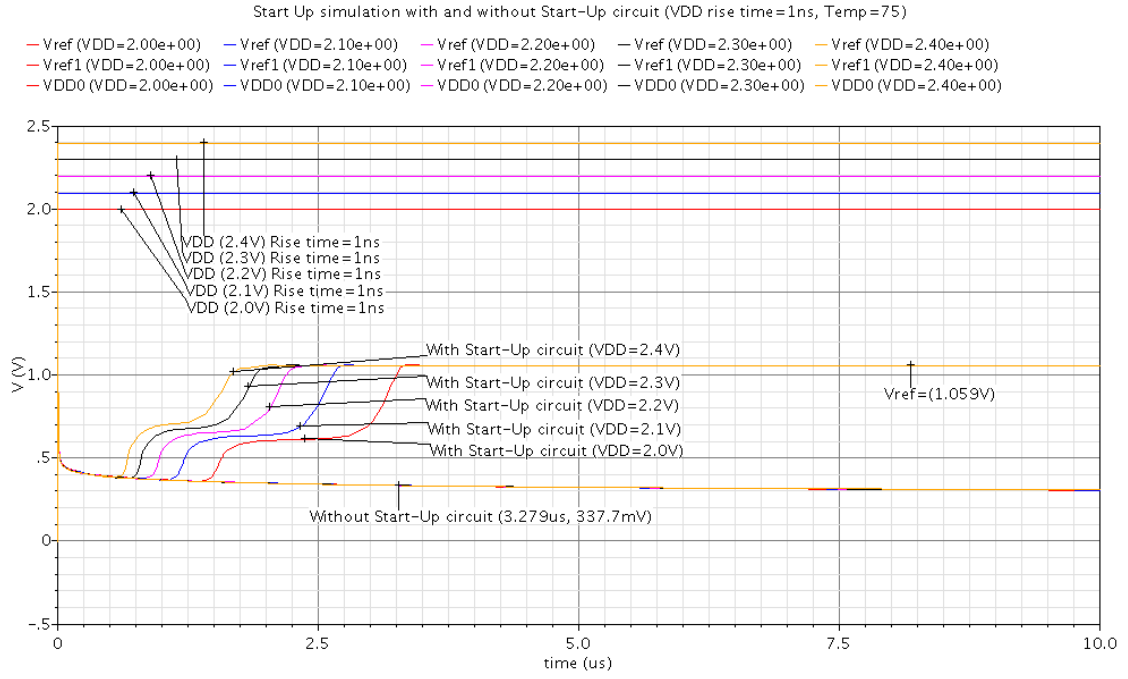

Figure 3.45 Transient simulation (VDD rise time=1ns, Temp = 75℃)

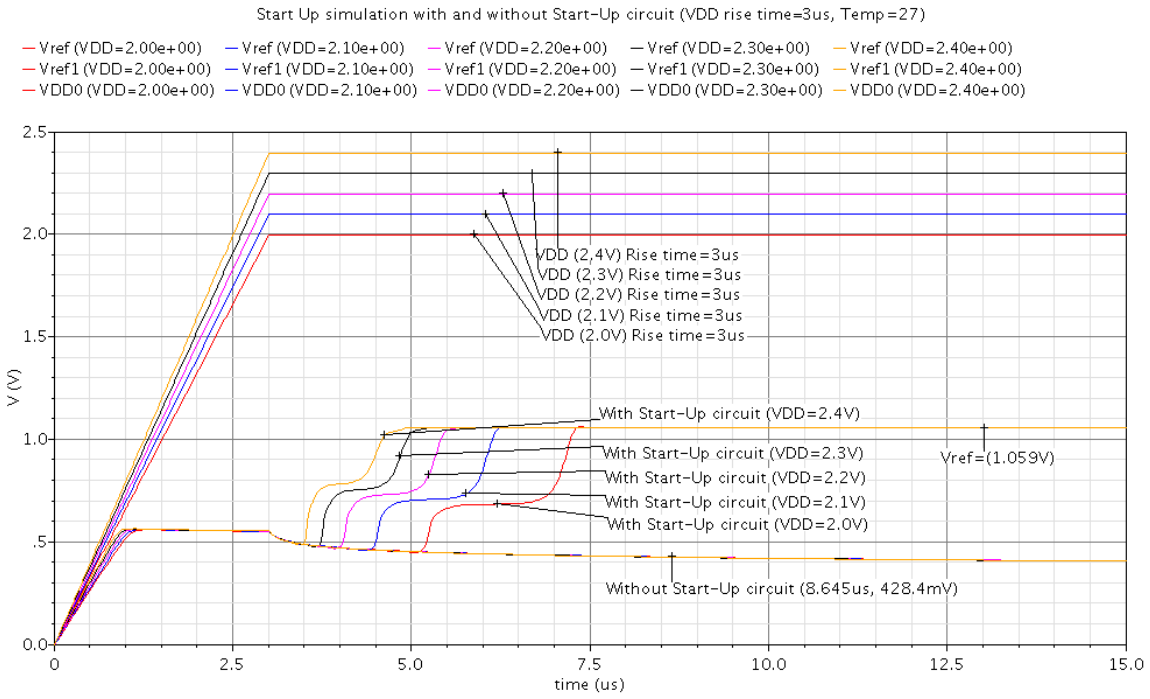

Figure 3.46 Transient simulation (VDD rise time=3us, Temp = 27℃)

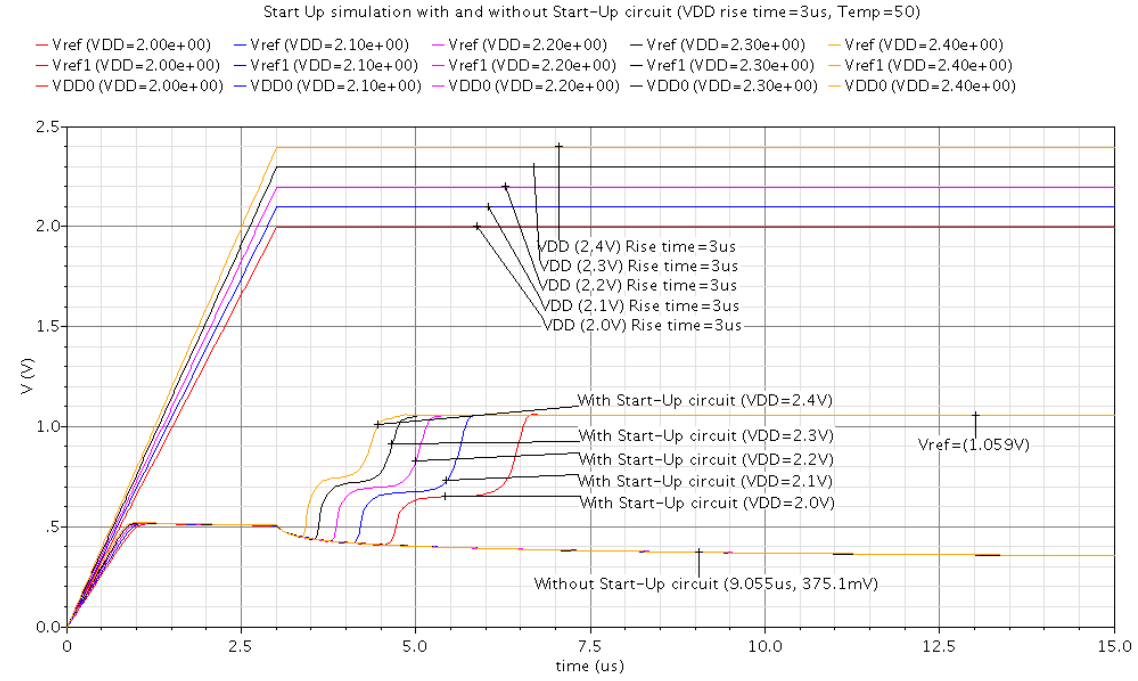

Figure 3.47 Transient simulation (VDD rise time=3us, Temp = 50℃)

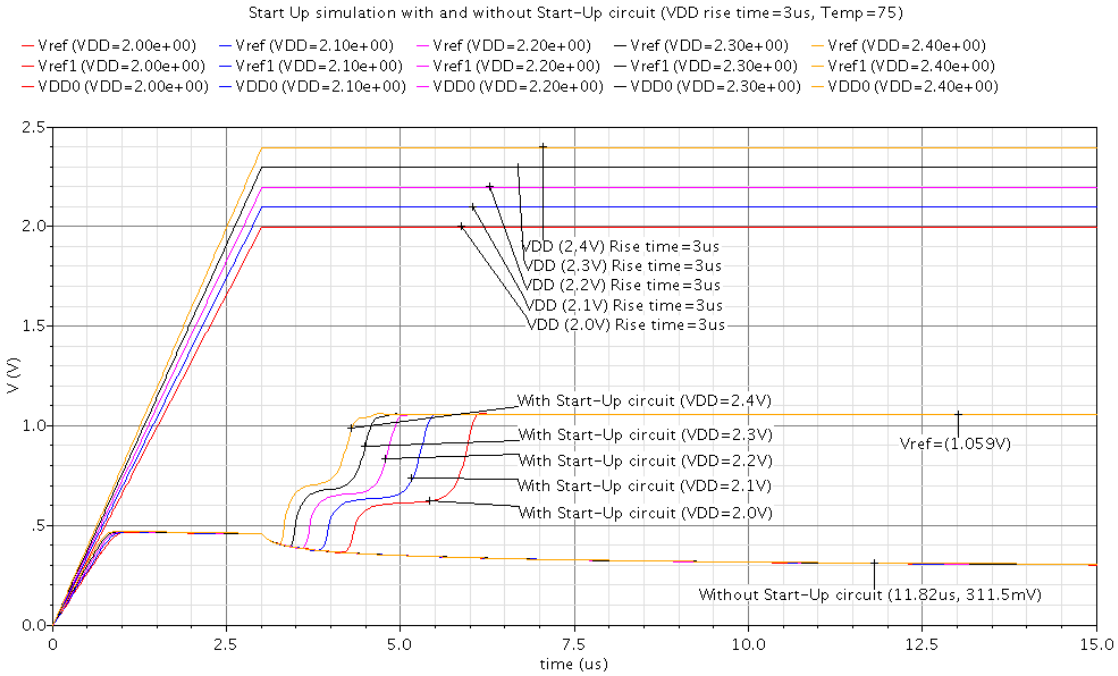

Figure 3.48 Transient simulation (VDD rise time=3us, Temp = 75℃)

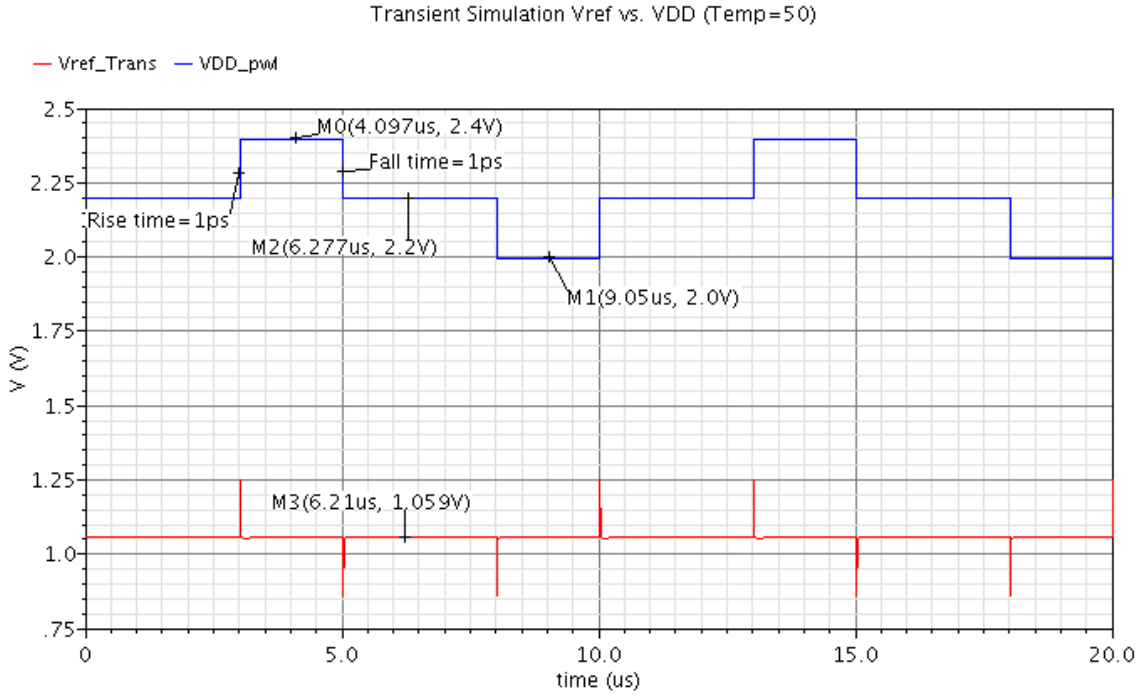

Figure 3.49 Transient simulation with VDD 200mV variation (Temp = 50℃)

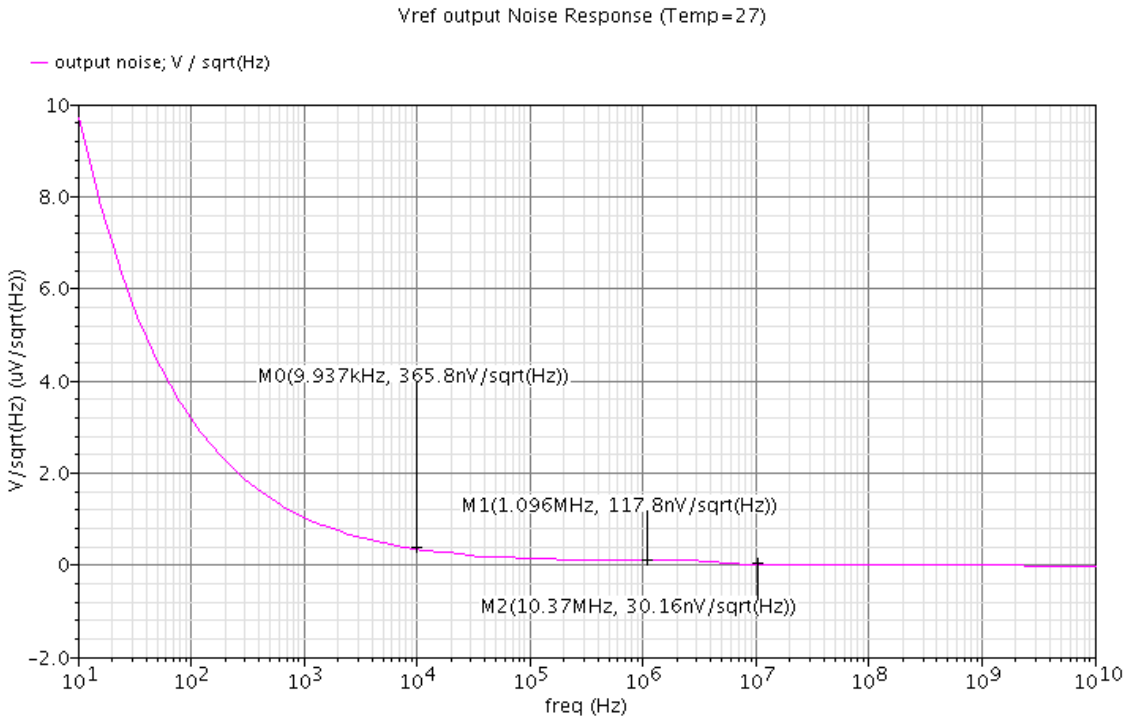

Figure 3.50 Bandgap voltage reference noise response (Temp=27℃)

Chapter 4

Conclusions and Future Work

4.1 Conclusions

A continuous-time reconfigurable transconductance-C is designed to meet the requirement of SDR. The filter provides 5^{th} order inverse-Chebyshev response with a tuning range from 4MHz to 40MHz. Cross-coupled pair with bias offset is employed to enhance the linearity of the transconductor. Gain boosting output stage of the OTA is employed to increase the output impedance. The simulation results show the THD is -44.34dB with an input of 400mV V_{p-p} and -54.6dB with an input of 200mV V_{p-p}. The filter consumes 23mW from a 3.3V power supply.

4.2 Future work

Baseband filter is an important building block in transceiver architecture. Continuous effort has been made to improve the performance of the filter. Filters designed with high linearity and low power consumption with a wide tuning range will always be a challenge task in the future. The techniques presented this work are only part of the work for SDR and can be optimized to meet future application.

References

[1] R. Schaumann, H. Xiao and M. E. V. Valkenburg, *Design of Analog Filters*. Oxford: Oxford University Press, 2010.

[2] J. J. Friend, C.A. Harris and D. Hilberman, "STAR: an active biquadratic filter section," IEEE Trans. Circuits Syst., vol. CAS-22, no. 2, pp 115-121, 1975.

[3] V. Gopinathan, M. Tarsia, and D. Choi, "Design considerations and implementation of a programmable high-frequency continuous-time filter and variable-gain amplifier in submicrometer CMOS." IEEE J. Solid-State Circuits, vol. 34, no. 12, pp. 1698-1707, 1999.

[4] S. D'Amico, A. Baschirotto, "Active-Gm-RC continuous-time biquadratic cells." Analog Integrated Circuits and Signal Processing, 45, 281-294, 2005.

[5] Y. P. Tsividis, "Integrated Continuous-Time Filter Design – An Overview," IEEE J. Solid-State Circuits, vol. 29, no. 3, pp. 166-176, Mar. 1994.

[6] H. Ma, F. Yuan, S. Liu, Y. Shi, "A low power baseband chain for CMMB application," IEEE Communication Systems, ICCS 2008, Pp. 1466-1470, Jan. 2009.

[7] H. Amir-Aslanzadeh, E. J. Pankratz, E. Sanchez-Sinencio, "A 1-V +31 dBm IIP3, Reconfigurable, Continuously Tunable, Power-Adjustable Active-RC LPF," IEEE J. Solid-State Circuits, vol. 44, no.2, Feb. 2009.

[8] S. Kousai, M. Hamada, R. Ito, T. Itakura, "A 19.7MHz, fifth-order active-RC Chebyshev LPF for draft IEEE 802.11n with automatic quality-factor tuning scheme," IEEE J. Solid-State Circuits, vol. 43, pp 2326-2337, Nov. 2007.

[9] P. Wan, Y. Chiu, P. Lin, "A 5.8mW, 20MHz, 4th-order programmable elliptic filter achieving over -80dB IM3," IEEE Custom Integrated Circuit Conference, 2010.

[10] A. Vasilopoulos, G. Vitzilaios, G. Theodoratos, Y. Papananos, "A low-power wideband reconfigurable integrated active-RC filter with 73 dB SFDR," IEEE J. Solid-State Circuits, Vol. 41, pp 1997-2008, Sep. 2006.

[11] B. K. Thandri, J. Silva-Martinez, "A Robust Feedforward Compensation Scheme for Multistage Operational Transconductance Amplifiers with No Miller Capacitors," IEEE J. Solid-State Circuits, vol. 38, pp 237-243, Feb. 2003.

[12] S. D'Amico, V. Giannini, and A. Baschirotto, "A 4^{th}-order active-Gm-RC reconfigurable (UMTS/WLAN) filter," IEEE J. Solid-State Circuits, vol. 41, no. 7, pp1630-1637, Jul. 2006.

[13] Yichuang Sun, "Design of High Frequency Integrated Analogue Filters," The Institution of Engineering and Technology, London, 2002

[14] E. Sanchez-Sinencio and J. Silva-Martinez, "CMOS transconductance amplifiers, architectures and active filters: A tutorial," Proc. Inst. Elect. Eng. – Circuits Devices Syst., vol. 147, no. 1, pp. 3-12, Feb. 2000.

[15] Z. Wang and W. Guggenbuhl, "A voltage-controllable linear MOS transconductor using bias offset technique," IEEE J. Solid-State Circuit, vol. 25, pp. 315-317, Feb. 1990.

[16] S. Szcepanski, J. Jakusz and R. Schaumann, "A linear Fully Balanced CMOS OTA for VHF Filtering Applications", IEEE Transactions on Circuits and Systems, Vol. 44, No. 3, Mar.

1997.
[17] J. Glinianowicz, J. Jakusz, S.Szcepanski and Y. Sun, “High-frequency two-input CMOS OTA for continuous-time filter applications”, IEE Proc. –Circuits Devices Syst., Vol. 147, No.1, Feb. 2000.
[18] A. J. Lewinski and J. Silva-Martinez, “A 30 MHz fifth-order elliptic low-pass CMOS filter with 65-dB spurious-free dynamic range,” IEEE Transactions on Circuits and Systems – I, Vol. 54, No. 3, Mar. 2007.
[19] L. Acosta, M. Jimenez, R. G. Carvajal, A. J. Lopez-Martin, J. Ramirez-Angulo, “Highly linear tunable CMOS Gm-C low-pass filter,” IEEE Trans. Circuits Syst., Vol. 56, No. 10, pp. 2415-2158, Oct. 2009.
[20] Tajalli, A., and Leblebici, Y, “Linearity improvement in biquadratic transconductor-C filters”, Electron Lett., 2007, 43, (24), pp. 1360 – 1362.