Reactive Power Compensation Device Design with Utilization of an Integrated Circuit Controller

by

John Graham Kirkpatrick

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Approved by

Mark Halpin, Chair, Professor of Electrical and Computer Engineering
Mark Nelms, Professor of Electrical and Computer Engineering
Charles Gross, Professor Emeritus of Electrical and Computer Engineering

Abstract

Reactive power compensation is necessary to increase the efficiency of current and future global electrical infrastructure. There are many methods for the design and implementation of reactive power compensators. This thesis will focus on the design, implementation, and study of a reactive power compensation device utilizing an integrated circuit controller, gating circuits, and dynamically switched shunt capacitor banks with special attention being given to the integrated circuit controller, gating circuit, and its switching scheme.

The compensation device controller will be constructed of discrete integrated circuit chips with a primary focus on the use of an analog-to-digital converter for data capture and a microcontroller for data manipulation. The goal of the controller is to capture and process reactive power data and then select and send the appropriate switching signals to capacitor banks which will dynamically adjust the reactive power levels on a three phase system. Transient free switching of the shunt capacitor banks will be performed by IGBTs that are controlled by a proposed gating circuit.

In this work, the reactive power compensation device with integrated circuit controller is discussed, implemented, and analyzed. It is concluded that the designed reactive power compensator performs as expected and correctly compensates reactive power demand from a three phase load, thus decreasing the reactive power demand seen by the electrical grid.

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Table of Contents

List of Tables

List of Figures

Chapter 1

Introduction

With continued societal and political pressure to produce more efficient electrical grids in nations across the world, utility companies have become more sharply focused on the development of strategies to reduce energy losses in their respective electric grids. One strategy to reduce these losses is to reduce the amount of reactive power delivered along transmission and distributions lines to customers. The more reactive demand the utilities must serve, the less efficient their grids become. Electric utilities, like Con Edison of New York, are beginning to introduce new reactive power charges to those commercial customers who, for example, do not maintain a power factor greater than 95 percent [1]. This creates new incentives for end users to find ways to efficiently and economically reduce their use of grid delivered reactive power, yet meet their reactive power needs. Several solutions are available.

Reactive power can be supplied in several ways. Reactive demand can be met by using synchronous condensers which can provide varied levels of reactive power based on varying the condenser excitation. This method was the dominant form of dynamic reactive power compensation until the 1960s, and in many cases reactive power control was gained just by decoupling older generators from their turbines to avoid new investment costs [2]. Today synchronous condensers still are an excellent source of large

quantities of reactive power, however the high level of maintenance required to maintain these electric machines has been a key reason why their use has dropped off as a source of localized reactive power for the end user. With continued advancements in power electronics, the use of dynamically switched capacitors to provide reactive power compensation to transmission and distribution networks as well as end user facilities has dramatically increased. These systems can be accurately controlled to provide safe and reliable compensation for utilities or the end user.

In the past, many reactive power compensation controllers utilized bulkier and more expensive, PC based, embedded systems boards like the PC-104 architecture that contained a multitude of external data acquisition peripherals to perform the task of calculating reactive power demand and make the required logic decisions to perform compensation [3]. With advances in integrated circuit technology, microcontroller units (MCUs) now have higher processing speeds as well as greater quantities of onboard ROM and RAM which combine to increase the newer MCUs computational capabilities of complex algorithms and signal processing routines. These advancements can be taken advantage of to produce a more streamlined and efficient, yet cost effective, controller for reactive power compensation. Many newer MCUs have multiple onboard analog-to-digital converters (ADCs) with 12-bit resolution for data input capture. But the majority of these devices utilize only unipolar coding of the analog inputs. Fortunately, the integrated circuit industry has designed higher bit capacity bipolar coding ADCs which can be taken advantage of to easily perform data conversion of sinusoidal signals.

Reactive power compensation devices utilizing shunt capacitors have been around for decades. Originally shunt capacitors were primarily used to control the steady state

system voltages [2], but advancements in the power electronics industry have opened a new door for dynamic, real time switching of the capacitor banks which provide focused and more load specific compensation. The power electronics must be managed to safely switch in the capacitor banks, otherwise damaging inrush current transients can harm the capacitors. Gating circuits that utilize switching schemes can be configured to appropriately switch in capacitors to avoid damage and will be used in such a manner in this work.

The purpose of this thesis will be to take advantage of recent technological advancements in the integrated circuit (IC) and power electronics markets to design, implement, and analyze the effectiveness of a reactive power compensation device that utilizes an IC platform controller along with gating circuits for the transient free switching of shunt capacitor banks.

Chapter 2

System Background

Special attention is given to the the development of a new platform controller for a reactive power compensator in later portions of this work, but first a type of reactive power compensator must be selected, designed, and built in order for the IC controller to be inserted and implemented. The reactive power compensation device that the proposed controller platform will operate will be a member of the family of reactive power compensators known as static var generators (SVG), which utilize capacitors or inductors to compensate for the reactive load of a system. In the following pages the development of this device will be summarized to provide background to the system in which the controller proposed later in this work is intended to operate.

Two different switching devices can usually be considered when building the well known form of reactive power compensator called a static var generator. The first consideration utilizes switching devices typically used in the development of SVGs called thyristors which are still widely used today for their high current capabilities. The second consideration takes advantage of recent advancements in the power electronics field which has introduced a new solid state device called an insulated gate bipolar transistor, or IGBT. IGBTs have turn-on and turn-off times on the order of a microsecond and are available as modules in ratings as large as 3.3 kV and 1200 A. [4].

An important difference between the thyristor and the IGBT is found in the manner in which the devices are turned on. The thyristor is turned on via a current pulse and stays on until the current passes through the zero point while the IGBT is turned on by applying a positive voltage to the gate and is turned off when the voltage is removed [3]. Another difference between the two power electronic devices is in the power levels where the devices are used. Thyristors find much of their use in utility applications at power levels beyond a few MWs where IGBTs are used in applications up to a few MWs [4]. And since this work is considering device application at industrial power ratings, the IGBT will be used as the switching device. A basic schematic of the compensation device can be found in Fig. 2.1.

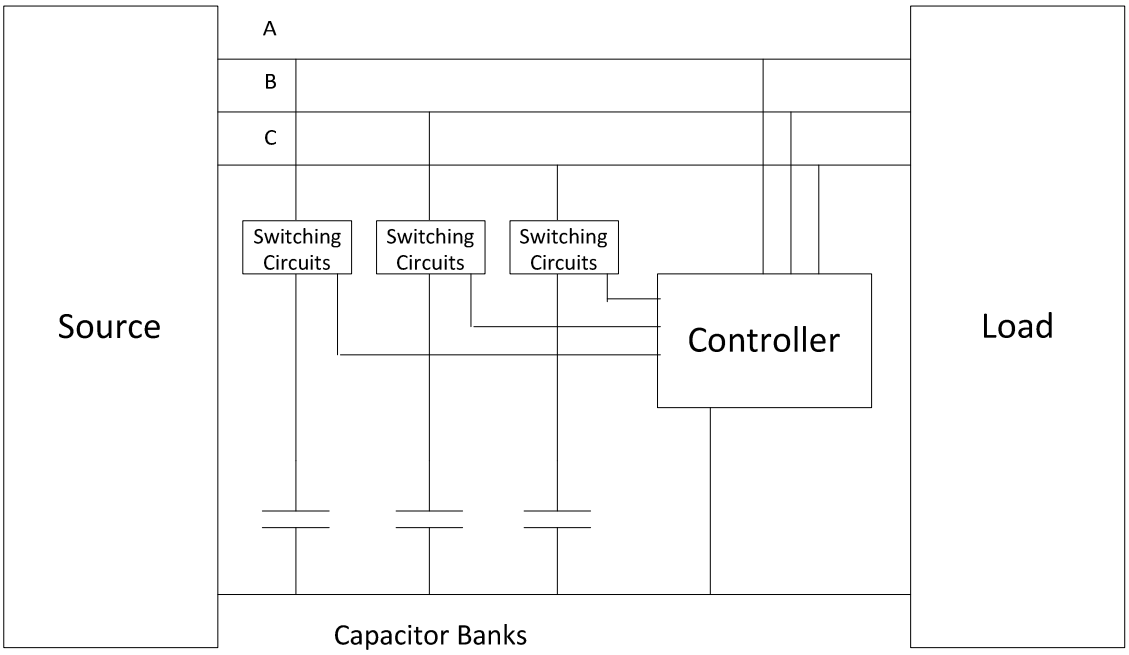

Figure 2.1: General compensation system schematic

2.1 Corrective Reactive Power Source

The system is designed to operate at customer side voltages and power ratings with capabilities to deliver large total reactive generation in small steps. The three phase system generates reactive power via capacitors banks placed on each phase. The available reactive power generation on each phase is subdivided into four levels or banks. The capacitor combinations are configured as binary multiples to allow for 2^n compensation steps per phase, where n equals the number of compensation levels [3]. This would minimize the number of capacitors. A full scale compensation system for industrial applications would typically call for capacitor banks sized at 10, 20, 40, and 80 kvar which would allow for maximum reactive power generation of 150 kvar per phase with a step size of 10 kvar.

2.2 Switching

Switching in the capacitors to provide the necessary reactive power is an important aspect of the control system. It is important to avoid any switching transients as they could damage the capacitor banks or the switching devices should such transients occur. A switching method that relies on a single IGBT module to perform transient free switching is a simple possibility that has been utilized in past systems [3]. The module, as seen in Figure 2.2, is composed of a single IGBT and anti-parallel diode.

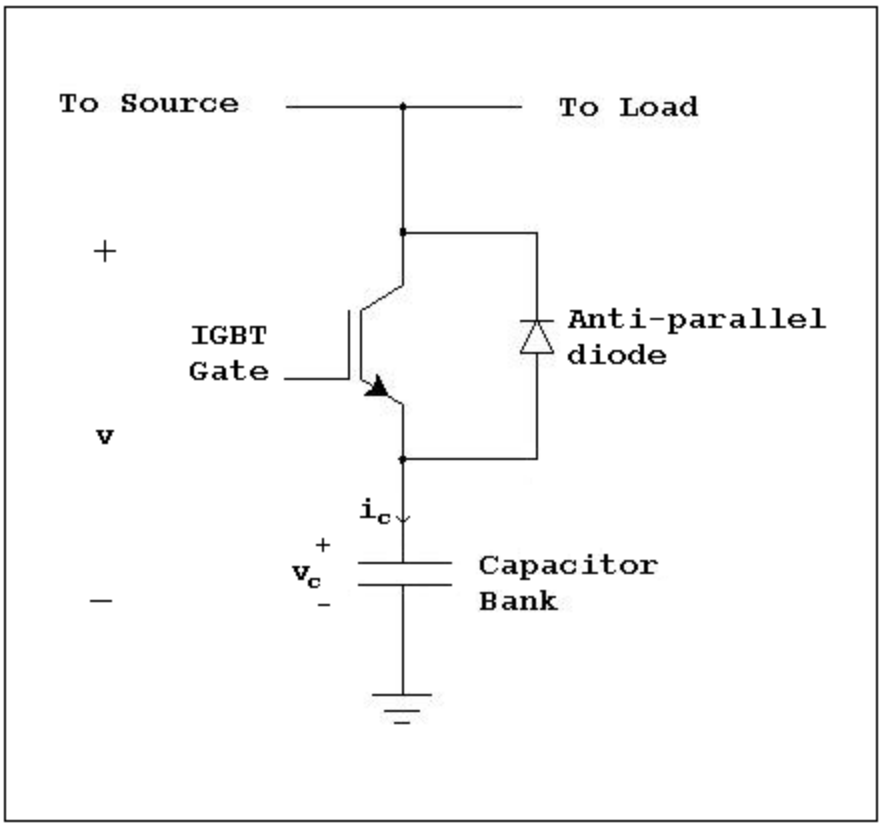

Figure 2.2: Single IGBT module including anti-parallel diode and compensating capacitor bank

The transient free switching is accomplished by making sure the capacitors are only switched in when the capacitor voltage is equal to the applied system voltage which makes the difference between the two voltages zero, as seen in Equation 2.1. If the capacitor is switched in at any other point, a large current transient will result as can be seen by Equation 2.2.

$$v - v_c = 0 \tag{2.1}$$

$$i_c = C\frac{dv_c}{dt} \tag{2.2}$$

If a single IGBT module is used it would certainly switch in the capacitor safely but the anti-parallel diode could allow for inrush currents to be seen during startup in the device, possibly damaging the capacitors.

An alternate switching method utilizing a bidirectional switch composed of two IGBT modules can be implemented to avoid both initial startup transients and switching transients. If the bidirectional switch is utilized and formed as seen in Figure 2.3 then the initial startup transients can be avoided by blocking all current flow while both IGBT modules are off. To avoid switching transients the two gates, G1 and G2 as seen in Figure 2.3, must be gated in a particular manner. If G1 is limited to gating at the negative peaks of the applied source voltage and G2 is limited to gating at the positive peaks of the applied voltage, then transient free switching of the capacitors can be achieved regardless of the capacitor voltage at any point in time. This is assuming that

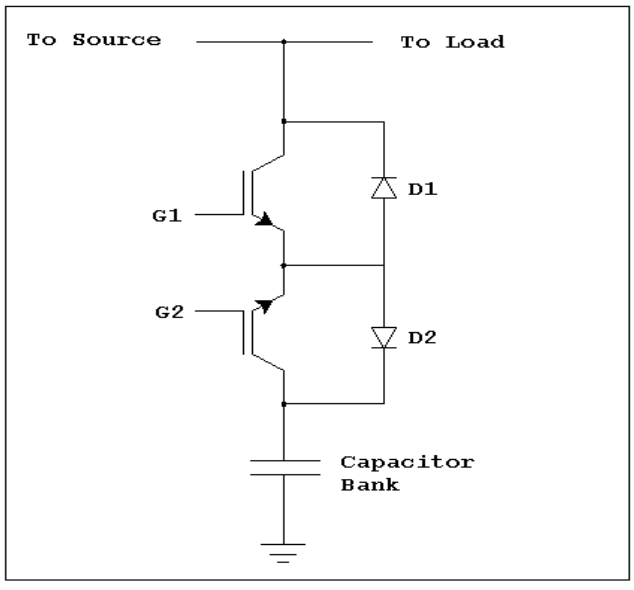

Figure 2.3 Bidirectional IGBT switch with capacitor

the voltage across the capacitor will always be greater than or equal to the initial applied voltage. This concept can be easily seen through an example scenario and can be seen in Figure 2.4.

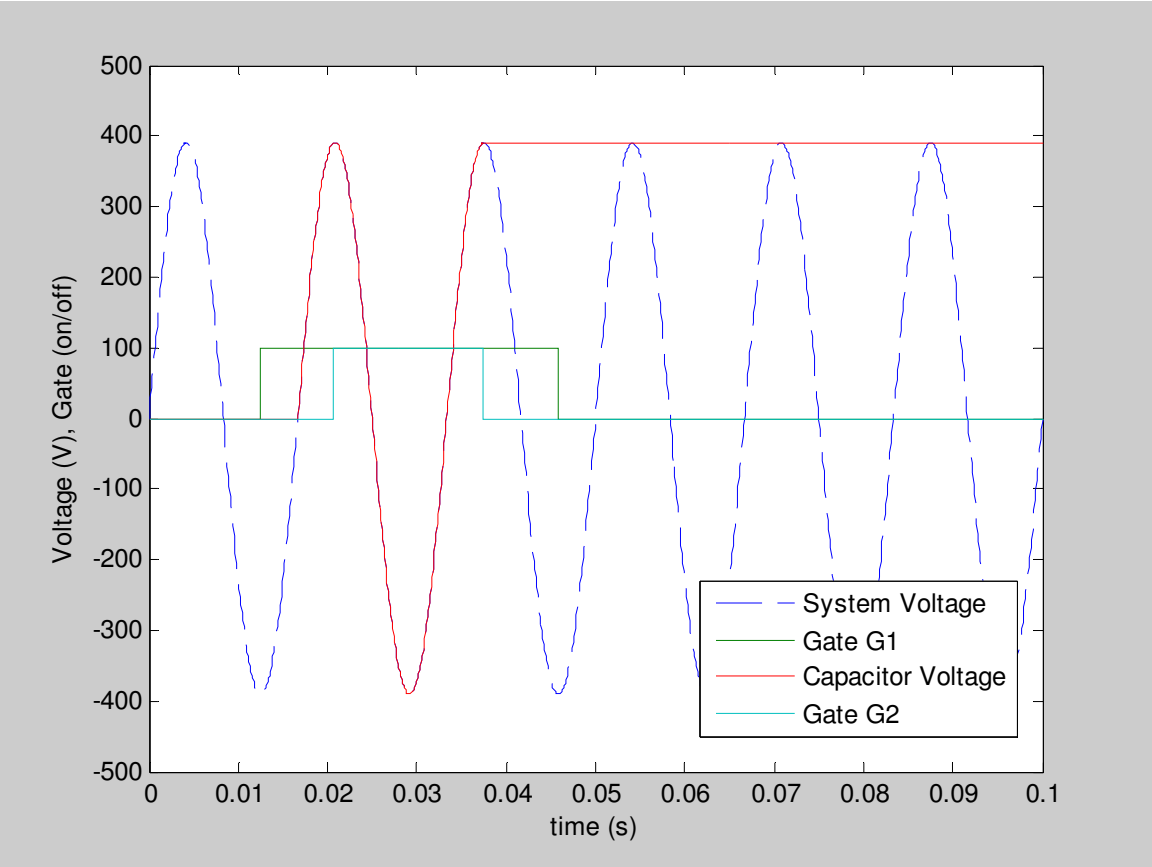

Figure 2.4: System voltage, capacitor voltage, and gate signals for the bidirectional switch process with zero initial voltage across the capacitor.

For instance, consider the case where there is initially zero voltage across the capacitor. If gate G1 associated with the first IGBT module turns on at the negative voltage peak of the applied voltage, the series connected diode D2 associated with the second IGBT module is reversed biased and will not conduct current and therefore no current transient will exist. As soon as the applied voltage waveform passes through the next consecutive

zero point the diode D2 associated with the second IGBT module will become forward biased and begin to conduct current in one direction causing a positive voltage to grow across the capacitor. When the voltage waveform reaches its maximum peak voltage, gate G2 can be turned on and the switch will be able to conduct current in both directions. Switching the gates on at the voltage peaks coordinates with the zero crossing of the current waveform. This is why there is no switching transient seen when gate G2 is turned on. Since the current is at the zero crossing point when the voltage is at its peaks, this is also the appropriate time for gate signal removal, which will occur in a similar successive manner as when they were turned on.

Now consider that the switch has been fully turned on and has been conducting current in both directions for some length of time. Depending on which gate signal is called to be removed first there will be either a positive or a negative voltage left across the capacitor. For instance if the gate G1 signal is called to be removed first, this removal must occur at a negative voltage peak. When the negative voltage peak is reached, the current will be zero and G1 is turned off. Since the diode D1which is associated with the first IGBT module will be reversed biased when the voltage begins to turn positive after it crosses the next consecutive zero point, there will be a negative voltage left on the capacitor. Gate G2 will be safely turned off at the next positive voltage peak, again where the current is now at the zero crossing. The negative voltage remaining across the capacitor will begin to dissipate with time due to ANSI and IEEE requirements that capacitors bleed a certain amount of charge off in a specified amount of time. For example ANSI and IEEE standards require that a 600V rated capacitor must discharge its charge to less than 50V within a 60 second period [5]. This will leave a

varying amount of voltage across the capacitor terminals. But as long as the switching scheme is adhered to the transient free operation will continue. Again the example can be continued for the case when a voltage remains across the capacitor terminals and can be seen in Figure 2.5.

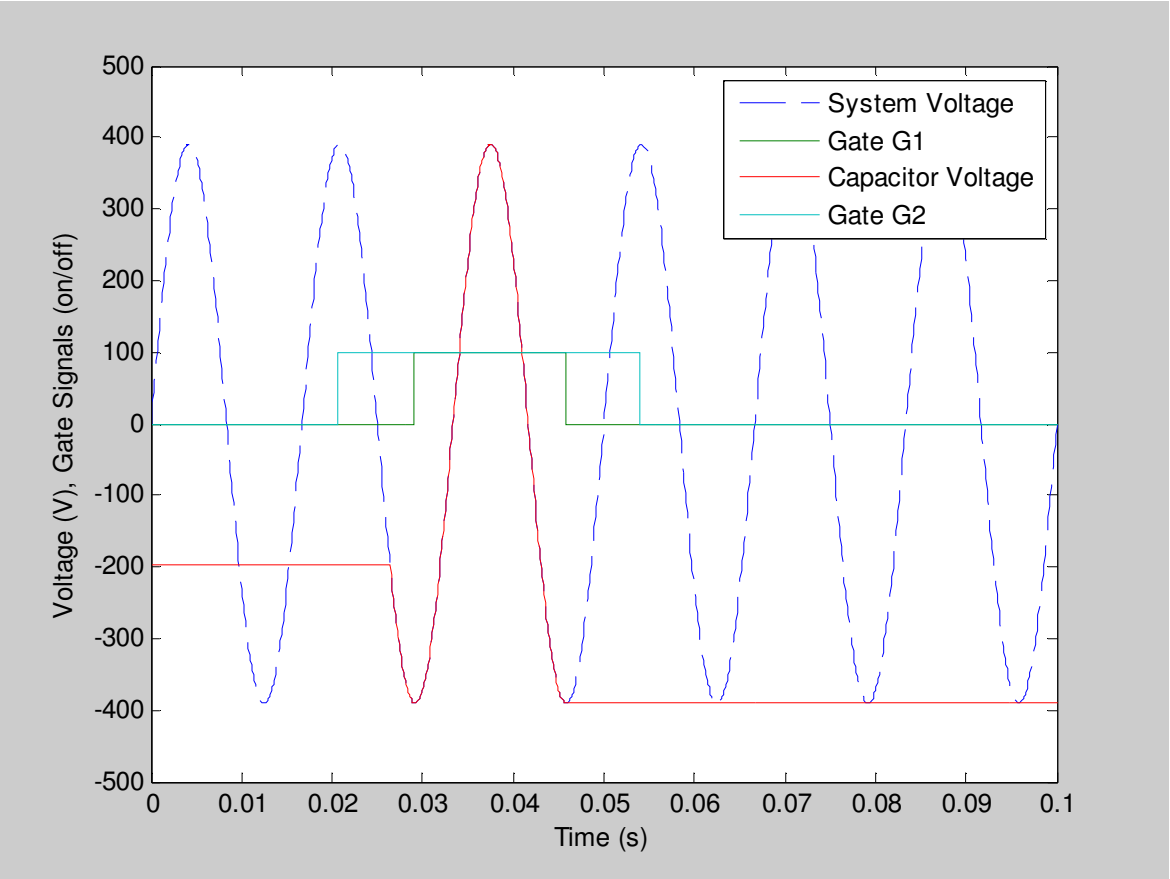

Figure 2.5: System voltage, capacitor voltage, and gate signals for the bidirectional switch process with a negative initial voltage across the capacitor.

Now assuming, for example, that the voltage across the capacitor terminals has dropped to 50 percent of its peak value, gate G2 can be switched in at the positive voltage peak where it is found that the diode D1 associated with the first IGBT module is again reversed biased and not allowing current to conduct. As the voltage crosses the zero point and enters into the negative half cycle the diode D1 becomes forward biased and

begins to conduct current allowing a negative voltage to build across the capacitor. Since the voltage across the capacitor is initially greater than the applied voltage there is no transient appearance and the applied voltage will then "catch up" to the capacitor voltage and surpass it, recharging the capacitor to the maximum negative voltage. However, at the time the negative peak is reached, gate G1 can be turned on to complete the transient free switching process and the switch will again be conducting in both directions until the gate signals are removed in the reverse order as they were turned on.

If the IGBT modules are placed in the circuit to form the bidirectional switch as seen in Figure 2.3, and the previous switching scheme followed, transient free switching can certainly be obtained. However, a problem can arise that could hinder timely compensation of reactive power. Since the switching scheme calls for gate G1 to be turned on or off at the negative peak and gate G2 to be turned on or off at the positive peak, a scenario can arise in which charges of 180˚ polarity difference are left on differing banks of capacitors depending on when switching signals are sent to turn on or off the varying capacitor banks. Without a modification, different capacitor banks could be called to switch in together at a particular instant and one bank with a negative trapped charge would come on 180˚ out of step with a bank that had a positive trapped charge. To prevent this detrimental occurrence, gate G2 associated with each capacitor bank, which is initially off at device startup and switches on and off only at the positive voltage peak, must be allowed to turn on during the first initial capacitor bank compensation switch-in request as specified in the previously explained switching scheme, but must remain on thereafter. By leaving gate G2 on, this will perpetually leave a maximum negative charge across the capacitor terminals, effectively changing the bidirectional

switch back into a single module switch. This will allow capacitor switching only once per cycle when the system voltage is equal to the capacitor voltage, which in this perpetual case, will always be the maximum negative voltage. Here the current waveform will be crossing the zero point and will, as stated before, allow for transient free switching. This method will maintain the ability to stop initial startup and switching transients and will also allow for correct synchronization of the capacitor banks should any combination, or all of them, be called to switch in together at one particular instant.

2.3 Gating Circuit

Since it is important to maintain the proper switching scheme of the IGBT gates, a gating circuit is implemented in this compensation system. As stated earlier in the discussion of the switching scheme, in order to provide transient free switching, it was determined that gate G1 would need to be initiated at the negative voltage peak of the applied voltage and that gate G2 would need to be initiated once during device start up at the positive voltage peak and remain on thereafter. This will be accomplished utilizing the gating circuit seen in Figure 2.6. The role of this circuit upon receipt of a capacitor turn on signal, or switching signal, from the controller is to coordinate and initiate the proper gate turn on sequence.

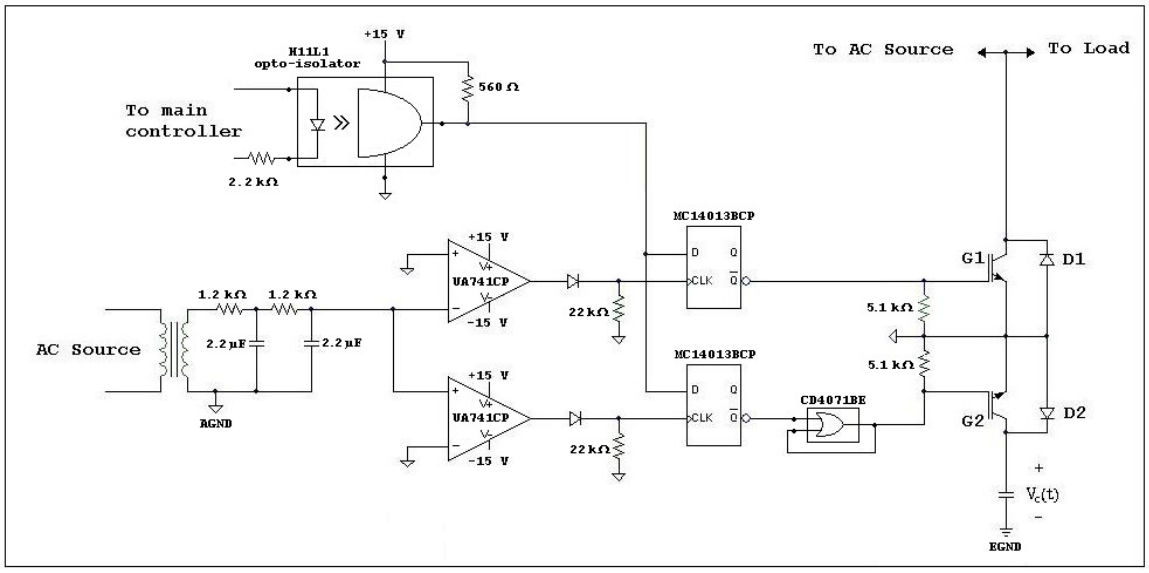

Figure 2.6: Gate control circuit including bidirectional switch and compensating capacitor

The gate circuit, seen in Figure 2.6, monitors the system voltage by first utilizing a transformer to reduce the system voltage down to around 8 V. This isolated voltage waveform maintains the same frequency and phase as the original system voltage waveform, however in order to create switching signals that will turn on the gates at the system voltage peaks, the phase of the new isolated voltage waveform must be shifted by 90˚. This is accomplished by a pair of RC low pass filters with resistor values of 1.2 kΩ and capacitor values of 2.2 μF. The voltage waveform that exits the pair of RC low pass filters is now shifted from its original form and is sent to op-amps which have their respective negative and positive voltage supply rails supplied by a corresponding negative and positive 15 V from an AC to DC voltage converter. The signal entering the op-amps overdrives the op-amps creating a square wave clock signal. The op-amp associated with gate G1 is configured so the rising edge of the clock signal corresponds to the negative voltage peak of the system voltage. Similarly the op-amp associated with

gate G2 is configured so the rising edge of the clock signal corresponds to the positive voltage peak of the system voltage. These clock signals are sent to the clock inputs of D flip-flop logic devices powered by the same 120 V AC to 15 V DC voltage converter that powers the rest of the gate circuit chips. However the logic devices will not accept negative voltage values so the clock signals are sent first through diodes, which are reversed biased in the negative half cycle, to remove the negative portion of the clock signal waveform. A 22 kΩ resistor is connected between each of the logic device's clock inputs and circuit reference to provide discharge paths for any charge buildup at the D flip-flop input. The control signal received from the main controller is also attached to the D input of each of the D flip-flops. The logic devices latch the received control signals from the controller on the low to high transition of the clock signal and then hold the control signal until the next such change.

An issue surfaces when attaching the D flip-flop outputs to the gate inputs of the bidirectional switch. The emitter voltage of the bidirectional switch will fluctuate depending on which IGBT is switched in and each IGBT requires a gate-to-emitter voltage of +15 V in order to switch on the device. This will require that the reference to the entire gating circuit be tied to the emitter voltage of the IGBTs forming the bidirectional switch if the D flip-flop is going to be able to provide the necessary +15 V to the gates relative to the emitter voltage for proper IGBT operation. A 5.1 kΩ resistor is placed between the gate of each IGBT and the gating circuit reference to provide for accumulated capacitive charge across the IGBT gate to emitter to dissipate.

The method of allowing gate G2 to turn on only once during the initial compensation request is accomplished by using a simple set latch [6]. A set latch is

formed by using a two input OR logic gate with its output tied to one of the gate's inputs to produce a feedback path as seen in Figure 2.7. At the introduction of power, the two logic inputs and the output are equal to zero as seen in Figure 2.7a. When the input not associated with the feedback path changes to logic one for the first time, the output changes to logic one and henceforth, so does the input connected to the output, as seen in Figure 2.7b. When the unconnected input returns to the zero logic state, the feedback connected input remains at logic one, as seen in Figure 2.7c.

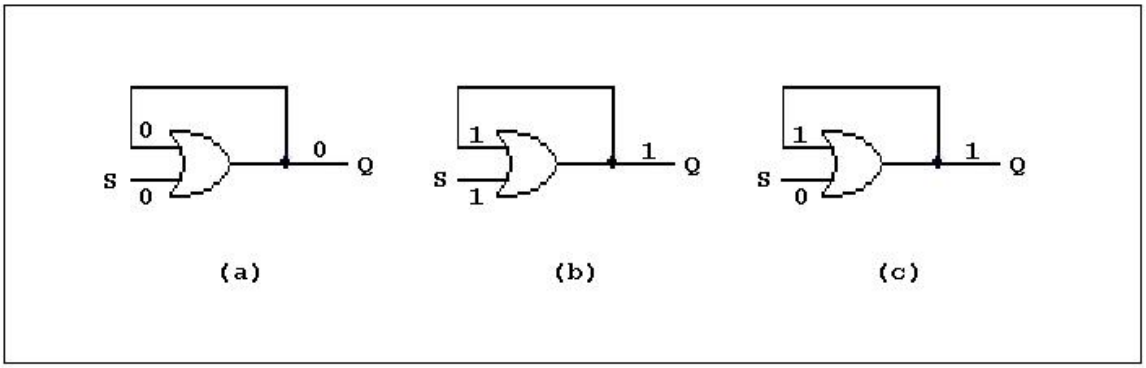

Figure 2.7: Set latch. (a) Initial state. (b) Output set to one. (c) Output permanently set.

The feedback connected input will permanently remain at logic one until power is removed from the chip, which at that point all inputs and outputs will return to zero. This is an important point of note. Should the compensation device lose power for any reason, the capacitors will maintain their immunity to startup transients due to the fact that the set latch will reset to zero upon power down. Upon restart, the gating circuit will again wait for the first compensation request and will, at that time, for one iteration, allow the switching device composed of the two IGBT modules to act as a bidirectional switch to block inrush currents to the capacitors during initial startup. From that point, the set latch

will again be permanently in the logic one state and gate G2 will remain on as designed to leave the capacitor banks negatively charged.

One further note on the gating circuit before moving forward; the floating reference of the gating circuit creates the possibility for potentially high voltages seen in reference to ground. For this reason an opto-isolator is placed between the main controller and the gating circuit to provide up to 7.5 kV of isolation. The controller will send control signals to this opto-isolator whose output will become the input to the D flip-flop logic device. However the opto-isolator uses negative logic. To compensate for this, the output from the D flip-flop which will be used to supply the gating signals to the IGBT gates will come from the logic device's negative Q output.

2.4 Reactive Power Calculation Algorithm and Measurement Scheme

Correct measurement of the reactive power is imperative and since the selected compensation device will be operating in continuous time, a key component for the controller will be to formulate reactive power calculations based on real time voltage and current measurements. In previous work in this area, methods for calculating the reactive power have been discussed and reviewed. One method proposed for such a device utilizes a zero crossing algorithm based on three consecutive operations: calculation of the rms voltages and currents, a phase lock loop filter, and the measurement of the reactive current at the zero voltage crossings [3]. This method was found to have a high immunity to harmonic content of input signals but has also been found to produce too much error in reactive power calculations caused by a slow response to changes in current magnitude, especially during circumstances associated

with small or no changes in phase. An alternate method utilizes a least squares approach and allows for the direct estimation of the current and voltage magnitudes and angles needed to perform reactive power calculations [3]. This method was found to be not as efficient in filtering out harmonic content of the signals but was more effective in its ability to minimize reactive power calculation errors. This method will be utilized in the implementation of the proposed controller platform and is summarized below.

The reactive power formula seen below in equation 2.3 utilizes the sine of the difference between the voltage and current angles. Phase angles are an inherent property of phasor voltages and currents and not a property of instantaneous signals [7].

$$Q = V_{rms} I_{rms} \sin(\theta_v - \theta_i) \tag{2.3}$$

As stated the least squares method can be used to estimate the voltage and current magnitudes as well as the needed phase angles with as little as three samples. The method takes advantage of the fact that any sinusoidal signal can be broken down into its real and imaginary components as seen in Equation 2.4.

$$y(t) = Y_r \cos(\omega t) + Y_i \sin(\omega t) \tag{2.4}$$

By making the assumption that the most recent sample is represented solely by the real portion of y(t) the fundamental frequency angle(ϕ) can be determined. The fundamental frequency angle in Equation 2.5 is the sampling period multiplied by the signal frequency

and is used in defining the relationship between the samples and the estimated signal values.

$$\phi = \Delta t * \omega \tag{2.5}$$

The relation as seen in Equation 2.6 uses three samples which allows for the formation of an overly defined set of linear equations. A slight buffer for signal discrepancies is added by over defining the relationship. The relation is solved for the real and imaginary components as seen in Equations 2.7, 2.8, and 2.9.

$$\begin{bmatrix} Y_{k-2} \\ Y_{k-1} \\ Y_k \end{bmatrix} = \begin{bmatrix} \cos(2\phi) & \sin(2\phi) \\ \cos(\phi) & \sin(\phi) \\ 1 & 0 \end{bmatrix} \begin{bmatrix} Y_r \\ Y_i \end{bmatrix} \tag{2.6}$$

$$[A]^T[A] \begin{bmatrix} Y_r \\ Y_i \end{bmatrix} = [A]^T \begin{bmatrix} Y_{k-2} \\ Y_{k-1} \\ Y_k \end{bmatrix} \tag{2.7}$$

$$\begin{bmatrix} Y_r \\ Y_i \end{bmatrix} = \{[A]^T[A]\}^{-1}[A]^T \begin{bmatrix} Y_{k-2} \\ Y_{k-1} \\ Y_k \end{bmatrix} \tag{2.8}$$

After these component values are found then the signal magnitudes and angles can be found via Equations 2.9 and 2.10.

$$|Y| = \sqrt{(Y_r)^2 + (Y_i)^2} \tag{2.9}$$

$$\theta_Y = \tan^{-1}\left[\frac{Y_i}{Y_r}\right] \tag{2.10}$$

Following the estimation of the magnitudes and phase angles for the current and voltage, these values can then be inserted into Equation 2.3 to calculate reactive power.

Measurement accuracy could be affected by the introduction of harmonics. Unfiltered harmonics added to the measured signal and if inserted into the least squares algorithm will directly result in errors in the reactive power calculation. Therefore the sampled data will be pre-filtered by a 4th order Butterworth filter with a cutoff frequency of 120 Hz before entering the least squares algorithm. This will attenuate the higher harmonics while effectively passing the 60 Hz signal unaffected through the filter. Errors in the least squares algorithm output appear as 120 Hz ripples or higher in the output. To correct this, a low pass filter will be implemented following the least squares algorithm.

2.5 Sampling Frequency

Sampling frequency selection plays an important role in the function of the controller. Recalling from the previous section that the sampling period is a component of the fundamental frequency angle calculation in Equation 2.5, and that a 4th order Butterworth filter will be used to filter the incoming algorithm data, it can be seen that adjustments to the sampling rate can have a noticeable effect on the functionality of the compensator. Too low of a sampling rate will be counterproductive since this will spread samples out and dampen the algorithms ability to quickly detect changes in the incoming signals. A low sampling rate will also cause problems in using the filters. The sampling rate must stay above the lowest time constant of the two filters. Decreasing the sampling

rate below the filter's time constants will cause stability and accuracy problems to occur since the time constant is a measure of signals ability to track changes in the signals [3]. However, if a sampling rate is chosen that is too high, the MCU will not be able to execute the program code quickly enough to keep up with the data being sampled. Therefore careful consideration must be taken in the selection of the sampling frequency.

Chapter 3

Controller Design Requirements

Now that the design of the switching apparatus and control algorithm of the reactive power compensation device has been properly summarized, the design requirements of the control platform can be discussed.

From a high level design perspective, the device controller will need to receive voltage and current data and then quickly and effectively calculate the reactive power demand drawn by the load. Based on the calculated value the controller will select and send switching signals to external capacitor switching circuits to dynamically switch in the appropriate capacitor banks for the proper amount of reactive power compensation.

The components that are necessary to meet the basic needs of this high level design perspective are a MCU and an ADC. Each of these IC devices will need to meet specific design requirements of their own.

3.1 Microcontroller Requirements

3.1.1 Processing Speed

Processing speed is one of the most critical design requirements as cycle to cycle control of compensation is desired for the system. The ability to provide this cycle to cycle control is dominated by the capacitor switching scheme which is controlled by the

capacitor gating circuit. The gating circuit was described in detail in Chapter 2, but it can be recalled that the bidirectional switch only operates as such for the first switch-in request of capacitor bank and then operates as a single IGBT module switch thereafter. This means that the highest frequency of operation for the IGBT switch is 60 Hz. This sets a minimum frequency that the controller should be able to perform compensation decisions. This in itself does not place too heavy a burden on performance. However, utilization of the least squares algorithm and the implementation of digital filters place a heavier computational burden on an MCU. Filter implementations, in particular, can be timely and computationally intensive processes. The chosen sampling rate will also have an effect on the ability of the MCU to efficiently execute calculations. Recalling from the previous chapter, in order to maintain accuracy and numerical stability of the reactive power calculations the sampling rate should not go lower than the smallest time constant of the digital filters used. However, care must be taken not to sample at such a high rate that the processor cannot complete the calculations in real time. Therefore a sufficiently fast processing speed in the megahertz range is a priority in the selection of a MCU.

3.1.2 Programming Language Capabilities

A widely known and accepted higher level programming language is desired for ease of programming of the controller. An MCU with capabilities of using a high level language such as the C programming language would be more preferable as opposed to assembly language programming which can become tedious and difficult for non-computer engineers to implement.

3.1.3 Communication Peripherals

The controller must maintain quick and effective communications between the MCU and ADC to reduce processing time of the measured data. An efficient communications protocol is required. For the proposed controller a serial peripheral interface (SPI) is desired due to the established protocol's ease of software configuration and high data transfer capabilities.

3.1.4 Input/Output Peripherals

Based upon reactive power calculations and compensation decisions, the controller will be sending capacitor switching signals to a maximum of twelve capacitor switching circuits representing the four different levels of compensation available to each of the three phases of the power system. Therefore an MCU with a minimum of twelve general input/output pins is required. Also the development of any type of simple human-machine interface (HMI) that could assist end users with the compensator's device operation would more than likely need access to several extra I/O ports. This additional consideration will be taken into account during device selection.

3.1.5 On Chip Memory

Prior versions of controllers utilized hard disk drives containing necessary operating systems such as Windows or Linux to perform execution of the control programs. Although hard drives exhibit large data storage capabilities, the necessity of such large storage quantities is not required for a modest control algorithm or program. It is necessary that the desired MCU be capable of storing the control algorithm on board the device in memory. Since one of the main purposes of the new controller design is to take advantage of recent technological advances in the IC market, the ability of the MCU

to hold its own control program is an area of great opportunity. Companies like Microchip, Inc are manufacturing MCUs with on-chip storage capacity nearing the megabyte range [8]. This on-chip storage ability provides for more efficient program execution by removing the process of retrieving programs from an external memory source. This retrieval of an external program has its own execution code and can create an opportunity for valuable program execution time to be lost. This will be negated by obtaining an IC capable of placing the program code directly on the chip

3.2 Analog-to-Digital Converter Requirements

The most pertinent ADC requirements are found in the following list.

- **Bipolar Input Capability -** Measurements of sinusoidal signals will be taken and therefore it is mandatory that the ADC have the capability to sample signals in a bipolar range.
- **High resolution ADC -** To maintain high fidelity in the reactive power calculations, it is desired that the proposed controller take advantage of a higher resolution ADC. A 16-bit converter is advantageous and desired.
- **Controllable Sampling Rate -** To meet the target of cycle to cycle compensation, avoid the introduction of aliasing, and to allow for proper and accurate algorithm processing time an adjustable sampling rate is desired.
- **Simultaneous Sampling -** The ability to measure current and voltage on each of the three phases is required. Therefore the selected ADC will be required to have a minimum of six input channels with the capability to

simultaneously sample the inputs. Simultaneous sampling of the inputs is required to assure that no additive phase shift is inserted into the calculations by delayed sample capture.

- **Fast Conversion -** The analog to digital conversion of the inputs is an important computational overhead parameter that must be considered. The proposed controller will require quick conversion to assist in the overall reduction of algorithm execution time.

Chapter 4

Device Selection

Based upon the design requirements a Microchip PIC32MX695F512H (PIC32) MCU and an Analog Devices AD7606-6 ADC were selected as the core components of the controller.

4.1 PIC32MX695F512H Microcontroller Features [9]

The PIC32 MCU was chosen since it had a combination of features that met the required needs of the controller design. The PIC32 MCU utilized a high performance 32-bit RISC CPU with a maximum operating frequency of 80 MHz that would allow for quick execution of code. There was also a prefetch cache module to speed execution from the onboard 512 K flash memory. The PIC32 MCU also had three SPI modules for serial data communications as well as 53 input/output pins for use in sending out the necessary capacitor switching signals and other I/O applications. For ease of programming the PIC32 MCU allowed for code development in C.

4.2 Important AD7606-6 ADC Features [10]

The AD7606-6 ADC was also chosen for its combination of features. The ADC had six inputs capable of simultaneous sampling as well as a true bipolar analog input

range with settings of ±10 V, or ± 5 V. The resolution of the AD7606-6 was 16 bits with data transfer capabilities of up to 200 kS/s on all channels. The chip also was SPI compatible which provided the necessary communication protocol to easily connect to the MCU.

Each of the selected chips was manufactured in a 64-lead Thin Quad Flat Package (TQFP) with dimensions of 10 mm by 10 mm by 1 mm. This packaging was designed for soldered chip placement onto a printed circuit board. Therefore, for device development, the chips were soldered onto 64 pin breakout boards which could be inserted into a breadboard for easy access to each of the 64 pins.

Chapter 5

Device Implementation

Now that the core components of the new IC platform controller have been selected, an explanation of how the IC devices must be configured is important. Much of the operation of the controller relies on the effective and correct configuration of each of the chips. Incorrect attention to the detailed steps of device setup can not only cause a malfunction in the device but could also allow for valuable processing time and efficiency to be lost. It is also important to note that the device manufacturers create chips to be as versatile as possible in their configurations to allow for end users to optimize each chip for a specific operation. Therefore a discussion of how each of these chips will be configured as well as the software configuration of the combined system is warranted.

5.1 Hardware Configuration

5.1.1 PIC Microcontroller Hardware Setup

The MCU has many different peripherals and configurations for external interfacing that need to be selected and set up for reactive power control. For reference, a schematic of the PIC microcontroller is presented in Figure 5.1.

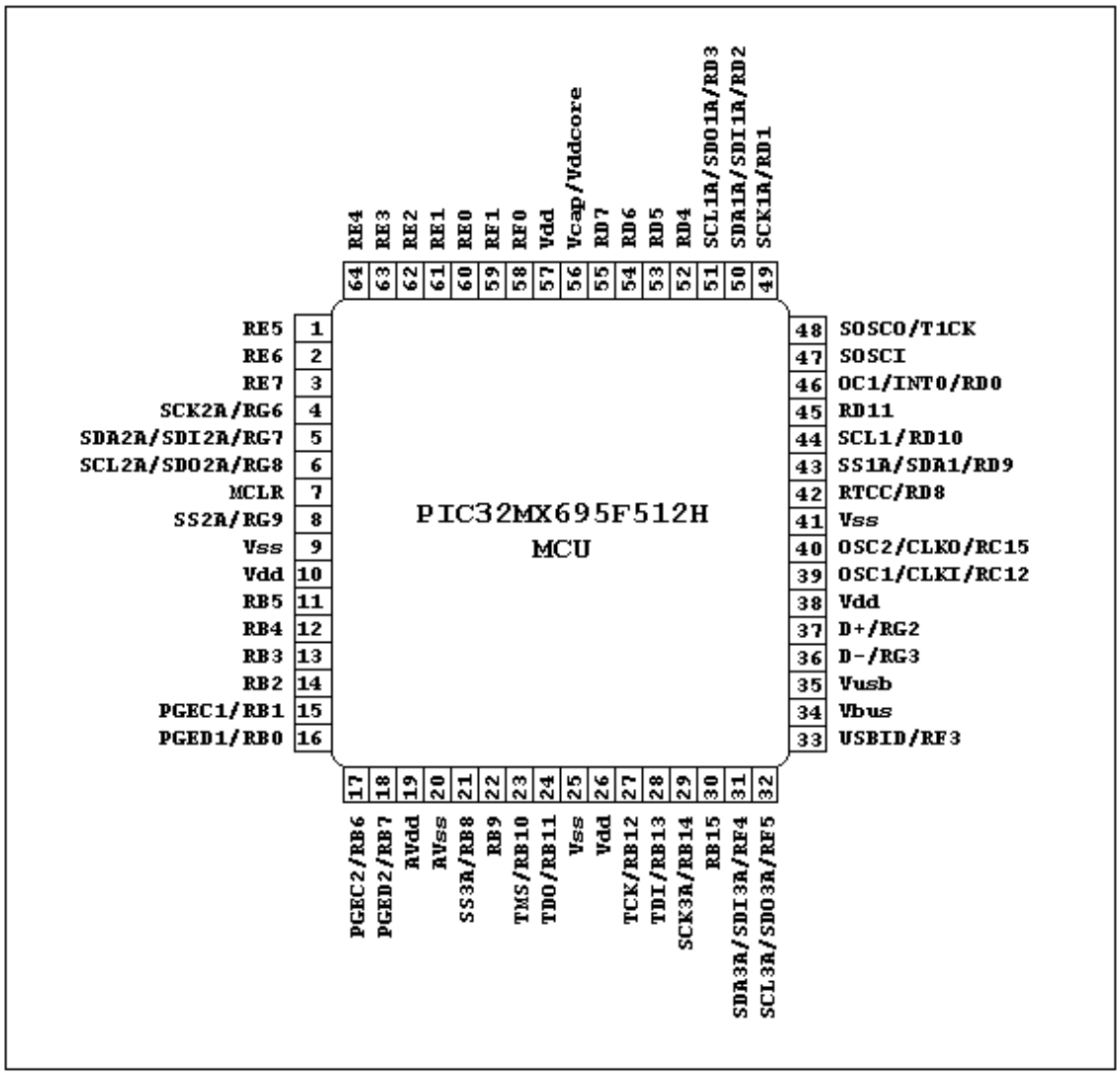

Figure 5.1: PIC32MX695F512H MCU pinout diagram

(Note: All of the following pin designations, unless otherwise stated, refer to PIC32MX695F512H MCU pins.)

The MCU has an operating voltage of 3.3V DC. A 5V to 3.3V voltage regulator is necessary to provide the appropriate supply voltage to the chip. This supply voltage is applied to pins 10, 19, 26, 38, and 57. To maintain the fidelity of the power supply, parallel 0.1 μF ceramic capacitors are connected between the power supply pins and

analog ground (AGND). The AGND reference for the MCU is connected to pins 9, 20, 25, and 41. Also, for stability of power supply voltage, a parallel 10 μF capacitor should be placed between the supply voltage and AGND at the board voltage source [9]. A simple schematic showing the basic decoupling capacitor connections is seen in Figure 5.2.

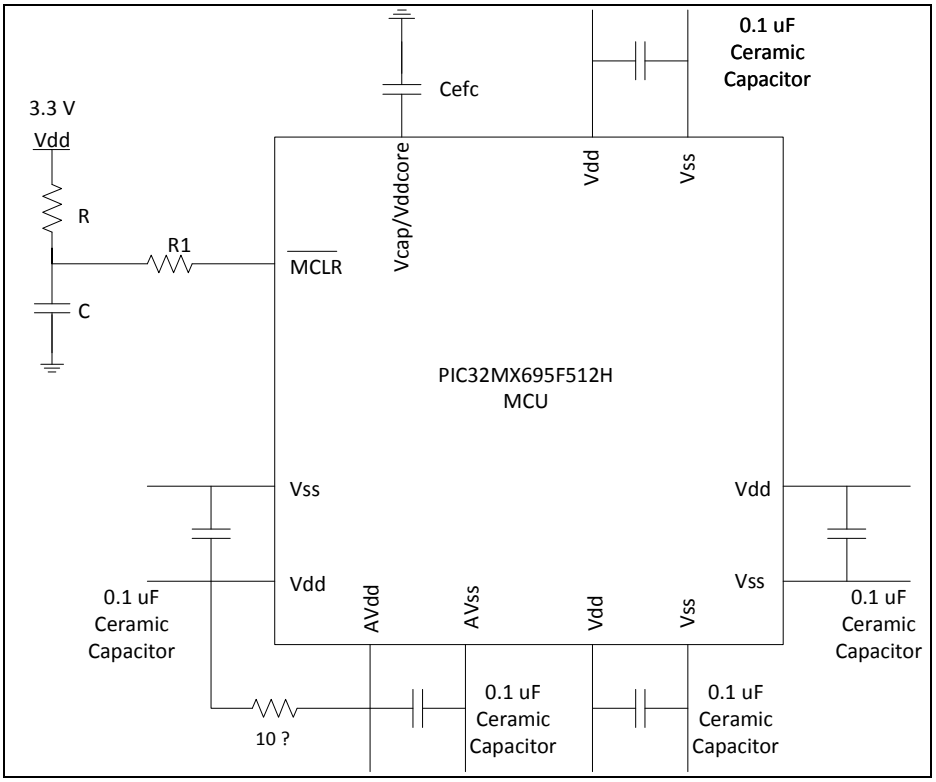

Figure 5.2: Basic power supply pin decoupling capacitors connections

The MCU has an internal voltage regulator, and its output is stabilized by connecting a 10 μF capacitor from pin 56 to AGND.

An external 8 MHz crystal oscillator is used to provide the MCU system clock. A 1.5 kΩ resistor is inserted in series between the crystal and MCU external oscillator pin

to prevent the crystal from being overdriven. The 8 MHz clock signal will be increased, or gained, internally by the MCU to achieve a maximum system clock frequency of 80 MHz.

Output signals to the capacitor switching circuits will be sent through the MCUs 16 bit PORTB register. PORTB bits 0 and 1 are used for in-circuit programming and debugging, but only 12 bits are necessary to cover all switching logic signals. So PORTB bits 4-15 will be utilized for the switching signals. Connections are made from these pins to the switching circuits. Specifically, MCU pins 27, 28, 29, and 30 are connected to Phase A switching circuits. Pins 21, 22, 23, and 24 are connected to Phase B switching circuits, and pins 11, 12, 17, and 18 are connected to Phase C switching circuits.

Communication between the MCU and the ADC is performed using one of the three MCU SPI modules. The serial clock, pin 49, is connected to its ADC SPI counterpart. The serial data input, pin 50, is connected to the ADC serial data output. It is not necessary to connect the MCUs serial data output pin since the MCU SPI module will only be used in receive mode for the proposed controller [11]. Also, bit 5 of PORTE, MCU pin 1, is an output bit that is used as the chip select pin for the framing of SPI communication between the MCU and ADC. Other input/output connections are:

- Pin 2- PORTE bit 6 used as an output to provide ADC chip reset.
- Pin 64- PORTE bit 4 used as an output to control ADC conversion.
- Pin 63- PORTE bit 3 used as an input to receive ADC conversion busy signal while analog-to-digital conversion is taking place.
- Pin 62- PORTE bit 2 used as an input to receive ADC first data signal

5.1.2 ADC Hardware Setup

The AD7606-6 ADC has several different configurations and can be utilized in different sampling modes such as simultaneous sampling of all inputs or batched sampling of groups of inputs depending on the end users needs [10]. Since configuration of the chip is user specific, and proper data measurement is imperative, a detailed description of the ADC setup is given. A pinout schematic is presented for referencing in Figure 5.3.

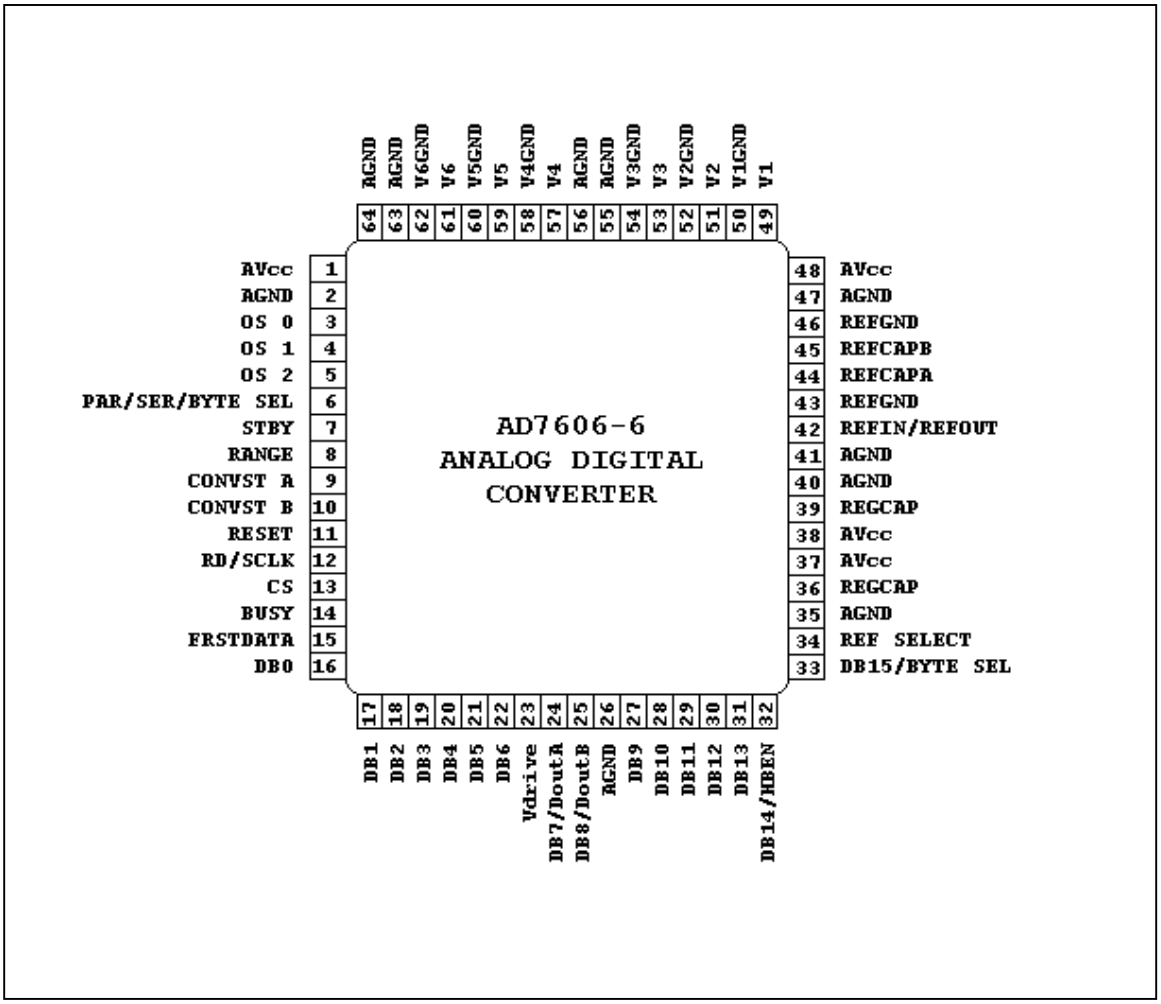

Figure 5.3: AD7606-6 ADC pinout diagram

(Note: All of the following pin designations, unless otherwise stated, refer to AD7606-6 ADC pins.)

The AD7606-6 ADC has an operating voltage of 5 V DC. The supply voltage is applied to pins 1, 37, 38, and 48 with each pin being decoupled to AGND with a 0.1 μF parallel capacitor for voltage stability and a 10 pF parallel capacitor to reduce the introduction of high frequency noise to the chip. The logic power supply input is to be the same voltage with which the MCU operates, 3.3 V. The voltage is to be connected to pin 23 and is used as the logic high input for the ADC. The pin is decoupled with the same value capacitors as the device power supply pins to reduce noise interference. Pins 2, 26, 35, 40, 41, and 47 are ground connections and are connected to AGND.

The ADC has an on-chip 2.5 V reference available on the device and will be configured to be utilized for this controller. To configure the chip to utilize the internal reference the internal/external reference selection input pin, pin 34, must be set to logic high. Therefore the pin will be hardwired to the logic high voltage.

The reference ground pins, pins 43 and 46, should be connected to AGND. The reference buffer output force/sense pins, pins 44 and 45, should also be connected to AGND but done so by connecting them together and then decoupling them to AGND by using a 10 μF capacitor. Other decoupling capacitors are required for proper chip operation, and are as follows: A 1 μF capacitor should be placed from the "decoupling capacitor pin for voltage output from internal regulator" pins, pins 36 and 39, to AGND. Also, a 10 μF capacitor should be applied from the reference input/reference output pin, pin 42, to AGND.

Oversampling of the input signals is available on the ADC but will not be used as this will increase the time needed for data conversion and will therefore increase overall execution time for the reactive power calculation algorithm. So these pins will be connected to the logic low signal, AGND, to disable the oversampling mode.

Setting the analog input signal range is performed by first determining the largest input expected to be received. From an input range perspective, the largest of the measured data will be the three phase voltages. The phase voltages that will be input to the ADC will be passed through a 100:1 voltage divider and since the compensation system will be placed at the service entrance of industrial loads the expected system voltages will be 480 V. Therefore the ADC Range pin, pin 8, will be hardwired to the logic low voltage to achieve a bipolar input range of ± 5 V for all input channels. Phase A voltage and current inputs will be placed on pins 49 and 51, respectively. Phase B voltage and current will be placed on pins 53 and 57, respectively. Phase C voltage and current will be placed on pins 59 and 61, respectively. Analog input ground pins are pins 50, 52, 54, 58, 60, and 62. They are connected to AGND.

The ADC data conversion process is controlled and managed by the conversion start input pins A and B. These pins are coupled together for simultaneous sampling and are connected to the PORTE bit 4 pin of the MCU.

The SPI module is controlled by several pins on the ADC. Several forms of communication are available on the ADC and the SPI mode is selected by placing a logic high signal on the parallel/serial/byte interface selection input pin, pin 6, and by placing a logic low signal on the parallel byte mode select pin, pin 33. These pins will be hardwired to the logic high voltage and AGND respectively to achieve the serial

communications mode. The serial clock input, pin 12, receives the serial clock signal from the MCU while pin 13 is the chip select (CS) pin and also receives its signal from the MCU to frame the SPI data exchange. The data is transferred from the serial interface data output pin, pin 24. Each of these ADC SPI pins is connected to their respective SPI counterparts on the MCU. The digital outputs "busy" and FRSTDATA are SPI process indicator pins and are connected to PORTE bits 3 and 2, respectively, of the MCU. Other ADC pin connections are:

- Reset input, pin 11-connected to MCU PORTE bit 6 for ADC system reset.
- Standby mode input, pin 7- hardwired to logic high voltage to keep chip turned on.
- Parallel output data bits, pins14, 16 to 22, and 27 to 31- unused, connected to AGND.

5.2 Software Configuration and Programming

Programming of the software was accomplished utilizing the Microchip, Inc. PIC32 development software, MPLab. Proper software configuration and setup is paramount to achieve an efficient and functional reactive power compensator. A simple flow chart outlining the major sections of the control program can be found in Figure 5.4.

The control program will execute in the following manner. The MCU will first be set up using the microcontroller's configuration bits to run the processor at the maximum processing speed of 80 MHz, run the peripherals at 40MHz, enable interrupts, and configure the SPI module to transmit 16 bit frames of data. Global variables that will be

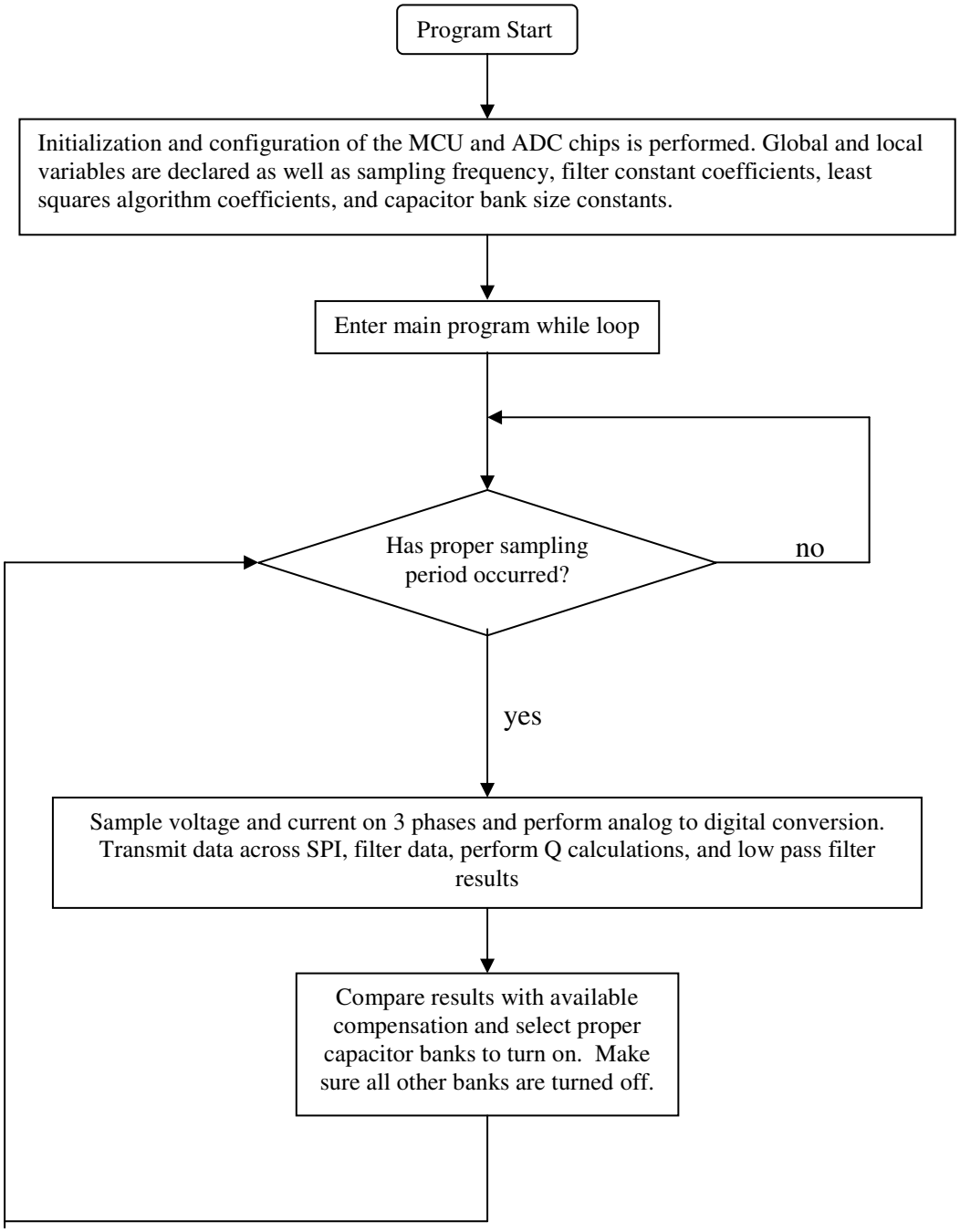

Figure 5.4: Flow chart describing function of the reactive power compensation program

used across the entire program are then initialized and declared before entering the main program. Upon entering the main program, local variables and arrays that will be used for six channel sampling, filtering, reactive power calculations, and data collection will be initialized and declared. Next, constants containing the capacitor bank sizes for each phase will be declared. Since there are four banks of capacitors used in compensation of each phase of the system, there will be four declared constants. These constant values will then be adjusted downward by ½ the smallest capacitor bank value to ensure that the compensated values of reactive power end up as +/- half the smallest capacitor bank size when the constants are used in comparisons for bank selection. Next the program will setup the least squares algorithm constant coefficients, the constant coefficients for the 4^{th} order Butterworth filter for the filtering of sampled data, and the constant coefficients for the low pass filter used in filtering the reactive power calculations. Following all the variable and coefficient initializations, the program will run a series of optimization functions designed to ensure maximum processing speed of the MCU and its peripherals. The code will then execute function calls to enable interrupts and configure the general input/output ports. The desired sampling rate is then stated in the code and this information is used to setup and configure the timer modules to ensure that the proper sampling frequency is maintained during program execution. At this point of the main program the MCU will send a reset signal to the ADC to ensure that the ADC has been initialized correctly and will perform accurate sampling. Following this reset signal, the Timer 1 module will be reset to zero and the program will enter into the main while loop that will run the program continually. The program uses a variable, GO, that when set to

1 will allow the control program to execute, but when set to zero will hold the execution of the program until the correct number of timer cycles has elapsed to ensure the proper sampling frequency is being maintained. Once the correct amount of time has elapsed an interrupt is triggered to set the GO variable to 1, which will resume the program execution. Upon "GO = 1," the program sends a conversion signal to the ADC and it simultaneously samples the six input signals, namely the voltage and current measurements of the three phases, and performs the data conversion. Following the data conversion, the MCU resets GO to zero to make sure sampling doesn't occur again until the correct sampling period has elapsed. The SPI module then sends the converted data in 16-bit packets to the MCU where the data is then filtered using the 4^{th} order Butterworth filter to remove any high frequency harmonics. This filtered data is then used by the least squares algorithm to estimate the current and voltage magnitudes of each phase and their corresponding phase angles. This data is then used to calculate the reactive power of each phase of the three phase system. Once these calculations are made the output data is then filtered by the low pass filter to remove any lower order harmonics. With the reactive power of each phase known, the controller then uses this information to select the proper amount of compensation by comparing the calculated amount of reactive power to the amount of reactive power available from each capacitor bank on each phase. In reality the program is comparing the calculated reactive power value to the capacitor bank constants that were created earlier in the code. The program begins its comparisons with values calculated for phase A and then proceeds sequentially to phases B and C. Upon entering the capacitor switching portion of the code, the program will first check to see if the calculated reactive power value that it obtained from

the control algorithm for phase A is larger than half the value of reactive power available from the smallest capacitor bank, which is called the step size. If the calculated reactive power value is not larger than the step size, then the program will bypass all the switching logic for phase A, turn off any switching signals that had been previously sent to phase A banks in prior switching iterations, and move on to compare reactive power values in the next phase. However, if the calculated reactive power value is larger than the step size, the controller will enter into the switching logic and compare the calculated reactive power with the largest capacitor bank constant first. If the calculated reactive power value is not larger than the largest capacitor bank constant, the program will turn off any previous "turn on" signal for the largest bank and will proceed to compare the calculated reactive power value with the next largest capacitor bank constant. However, if the calculated reactive power value is larger than the amount of reactive power available from the largest capacitor bank, the controller sends a signal to the switching circuit to switch this bank of capacitors into the circuit. The controller will then subtract the amount of reactive power switched in by this capacitor bank from the calculated reactive power value and then proceed to compare this newly adjusted calculated reactive power value with the next largest capacitor bank constant. This procedure will continue down through each level of possible compensation and through each phase of the system, turning banks on or off as necessary for accurate compensation. Once the program has been fully executed, the program will return to the head of the main while loop and wait for the timer interrupt to trigger and start the program execution over again in conjunction with the proper sampling frequency.

Chapter 6

Experimental Setup and Analysis

In order to test the functionality of the designed system with its proposed controller, a full three phase reactive power compensator must be prototyped and built. However, the full scale compensator is designed to operate at industrial power ratings. Testing a three phase prototype version of the compensator at industrial power ratings would not only be more expensive but could also pose safety concerns in the experimental stage. Therefore a scaled down version of the compensation device was constructed to use during testing. The device that was prototyped for testing utilized a line-to-line operating voltage of 208 V and provided compensation only to one phase with gating circuits and IGBT switches only being utilized on the one phase. A single phase device was decided upon under the theory that if the controller could successfully control and compensate one phase of a three phase system while continuing to perform calculations and make switching decisions on all three phases, then when the gating circuits and switches were implemented on the other two phases, compensation could successfully be performed in the full three phase version of the compensator. Using this method required fewer parts and saved time and money in the construction of individual gate circuits.

Since the experimental setup and testing is performed in the lab on a small scale replica of the compensation device, the full scale capacitor banks that would provide

reactive power correction of 10, 20, 40, and 80 kvar at 277 V are not used. Instead, the experimental prototype model developed for this work implements capacitors that will provide total reactive power compensation in the range of a few hundred var. Capacitor values of 10, 20, 40, and 80 μF are used to produce the 16 levels of compensation found in Table 6.1. The shaded values in Table 6.1 represent the four different capacitors that can be switched in for compensation, while the unshaded values represent compensation values formed by varying combinations of the four capacitors.

Level	Compensation (var)
1	0
2	54.29
3	108.57
4	162.86
5	217.15
6	271.44
7	325.73
8	380.02
9	434.31
10	488.6
11	542.89
12	597.18
13	651.47
14	705.76
15	760.05
16	814.34

Table 6.1: Compensation levels for the model reactive power compensation device

The compensation device's experimental model consisted of the proposed controller mounted on two printed circuit breakout boards to allow for breadboard insertion of the 64 pin TQFP MCU and ADC chips, four prototyped gate circuits that were used to provide the correct transient free switching of the capacitor banks, eight IGBT modules for switching (two per bank), four banks of capacitors, a ¾ horsepower

three phase induction motor which served as the reactive power sink, and a laptop computer. A schematic diagramming the experimental setup can be seen in Figure 6.1.

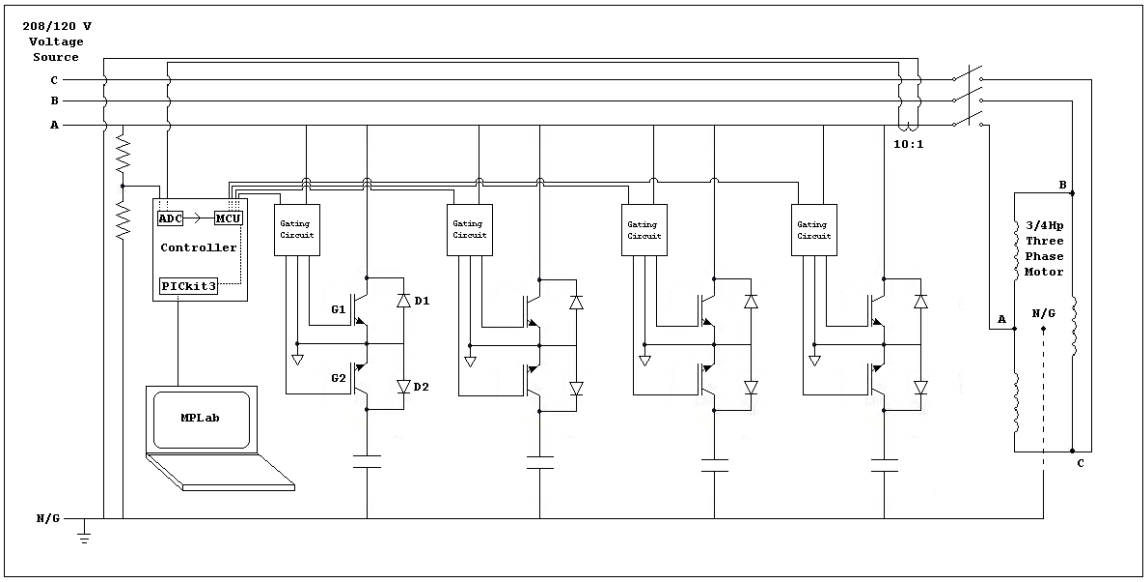

Figure 6.1: Experimental setup schematic for compensation of one phase of a three phase load

The hardware and software were setup for the controller as described in Chapter 5. However, it was previously stated in Chapter 2 that selection of the sampling frequency should be done in regard to the smallest time constant of the two filters being implemented. It was found that the smallest time constant of the two filters was in the Butterworth filter used in filtering the incoming data to the least squares algorithm [3]. The time constant of this filter was found to be 1.434 ms, which means that the minimum sampling rate allowed for the ADC has to be above 700 Hz. Through testing it was found that the MCU processor could correctly execute the program when utilizing an upward sampling frequency threshold of 1800 Hz.

The gate circuits were constructed as shown in Figure 2.4 of Chapter 2 and controlled the IGBTs which were placed in the circuit to create the bidirectional switch seen in Figure 2.3. The capacitors with values stated in Table 6.1 were inserted into the

circuit. A 208 V, ¾ Hp, three phase induction motor was chosen as the reactive load and inserted into the circuit. Testing showed that the motor required around 400 var per phase during its steady state operation and required upwards of 900 var per phase during starting. This was determined to be a suitable load for the model compensation system.

The final component of the experimental model was a computer running the MCU development software MPLab, tethered to the compensator controller via an in-circuit programmer/debugger module from Microchip, Inc., namely the PICkit 3. This will allow operation of the compensator and controller to be managed during testing from inside MPLab. From MPLab the compensator controller can be initiated, stopped, or reset at various stages to facilitate different testing scenarios. Managing the controller with MPLab and the PICkit 3 also allows for quick adjustment of the sampling frequency between experimental runs.

Data collection was performed using an oscilloscope with data storage capabilities and by utilizing the inputs on the ADC itself. Since the scenario of compensating reactive power on only one of the three phases was adopted, this allowed for the inputs on the ADC that were reserved for phases B and C to be used for measuring reactive power at other locations in the system. The input ports that were to be utilized for phase B voltage and current measurements were adopted for measuring the reactive power at the source of phase A, while the phase A ADC inputs were utilized in measuring the reactive power seen by the load on phase A. The controller was still performing reactive power calculations for all three phases, but in this case, “phase B” inputs were being used to measure the phase A reactive power seen at the source, and “phase C” inputs were connected to ground. It is important to note that the three phase software control program

was not altered even though the phase B and C inputs were not collecting phase B and C voltage and current data. The control program was still sampling the six inputs, filtering the samples collected on the inputs, performing reactive power calculations with the values it was collecting on each input, filtering of the reactive power results of each "phase", and then making switching decisions for the three "phases" based on the reactive power calculations the controller determined. It was just the case that in this experimental setup, there were no physical connections to any switching circuits or capacitors on phases B and C and therefore allowed for the advantage of using the controller to collect reactive power measurements at the source of phase A instead of reactive power measurements for phase B. This clarification is provided to make it clear that the controller was making all its normal calculations and switching decisions and also that there were no MCU timing alterations made to the three phase controller during the single phase compensation scenario.

Arrays were created to store data measurements on the MCU's onboard memory. The PIC32 device chosen for the experiment had ample onboard memory storage for testing needs and the chip's development software, MPLab, gave easy access to all variables and data arrays.

Testing and analysis began by first verifying that all components of the controller were functioning correctly and accurately. Signals of known value were placed on each input to the ADC and were correctly verified. The serial peripheral interface between the ADC and the MCU was tested and verified as operating correctly. Reactive power calculations obtained from the least squares algorithm were tested and positively verified by implementing the code in MATLAB and placing known data into the algorithm and

comparing the reactive power calculations obtained by the algorithm with the expected reactive power values. Upon successful testing of the controller and its components, testing of the experimental prototype began.

Of particular interest during testing was the compensator's reaction to the transient state of the motor during startup as well as the steady state. The compensator was designed to quickly begin reduction of the reactive power demand served by the source during system transients and then maintain the level of compensation throughout load operation. Monitoring the effectiveness of the compensator through the motor startup transient and into the steady state operation of the motor would give the appropriate data needed to verify correct device operation. Analysis of this state was accomplished by placing a three pole, single throw switch in series with the compensation device and the motor as seen in Figure 6.1. The compensator was turned on, and with its monitoring routine operating, the three pole switch was closed and the motor entered startup. During each experimental run, the following data from phase A and the MCU were collected for use in analysis:

1. Voltage
2. Load current
3. Source current
4. Calculated load reactive power
5. Calculated source reactive power
6. Capacitor switching signals sent from the MCU

Plots of the experimental results utilizing sampling rates of 1750 Hz, 1200 Hz, and 750 Hz are seen in Figures 6.2-6.4 respectively.

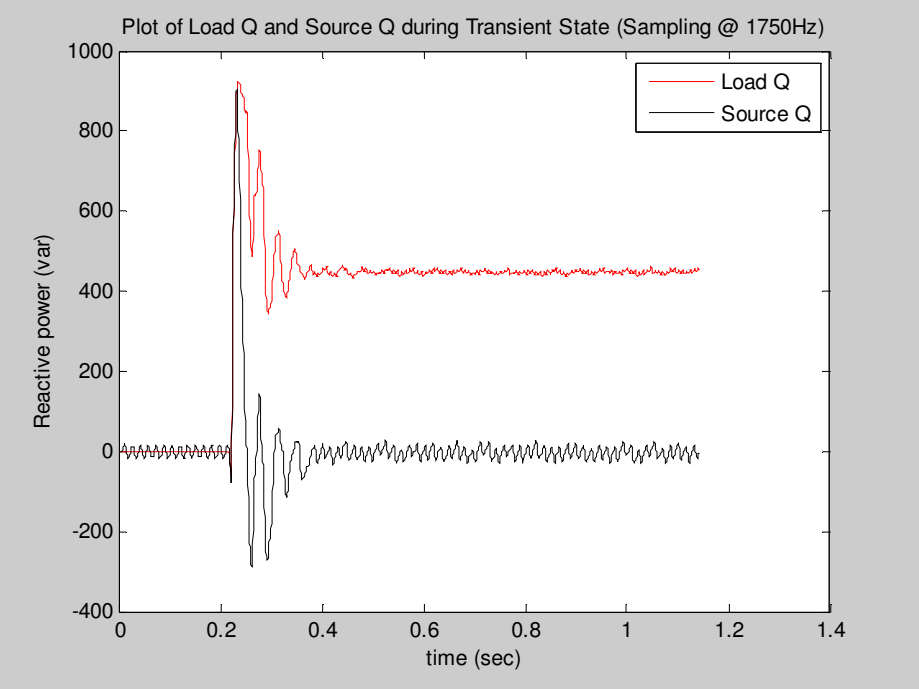

Figure 6.2: Plot of load Q and source Q during motor startup. Sampling performed at 1750 Hz.

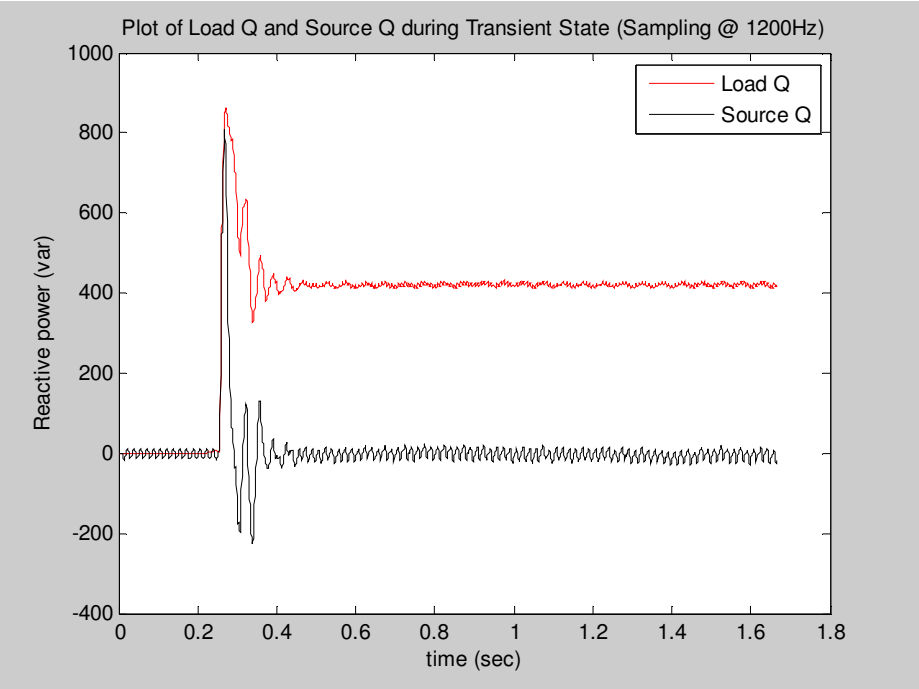

Figure 6.3: Plot of load Q and source Q during motor startup. Sampling performed at 1200 Hz.

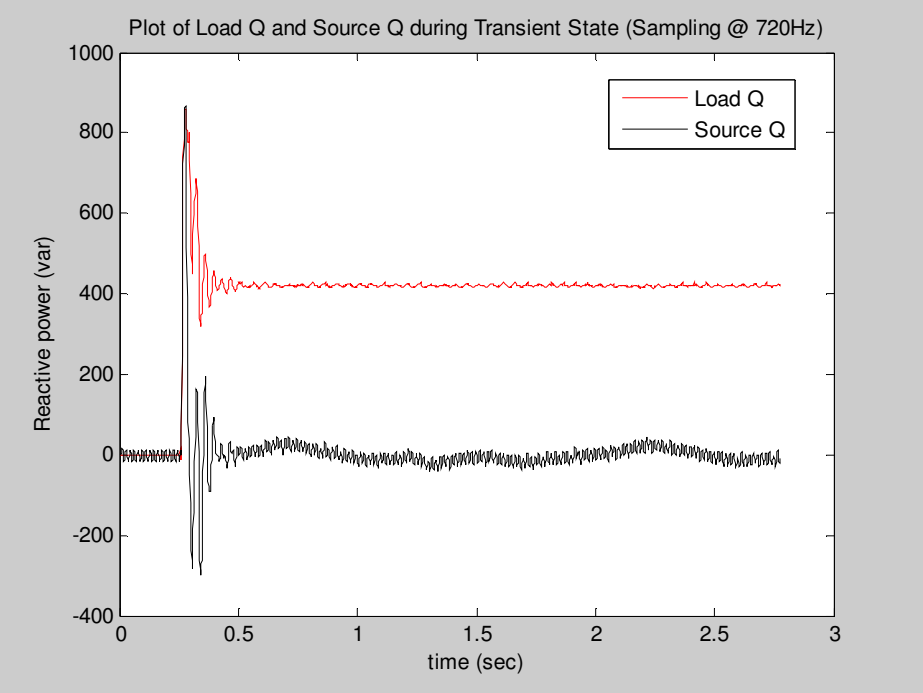

Figure 6.4: Plot of load Q and source Q during motor startup. Sampling performed at 720 Hz.

In Figures 6.2-6.4, it can be seen that the motor is drawing close to 900 var per phase during startup and around 400 var per phase when the motor settles out into the steady state. At motor start, the source initially provides the necessary reactive power but the compensator quickly recognizes the amount of reactive power demanded by the load and begins to perform the switching of the capacitors to locally provide the reactive power. The compensation system maintains proper correction into the steady state of motor operation which relieves the amount of reactive power delivered by the source and thus confirms correct system operation as expected.

One key observation was noted during analysis. There was oscillation of the reactive power seen at the source during the motor startup period which requires an explanation. A close-up view of this oscillation can be viewed in Figure 6.5.

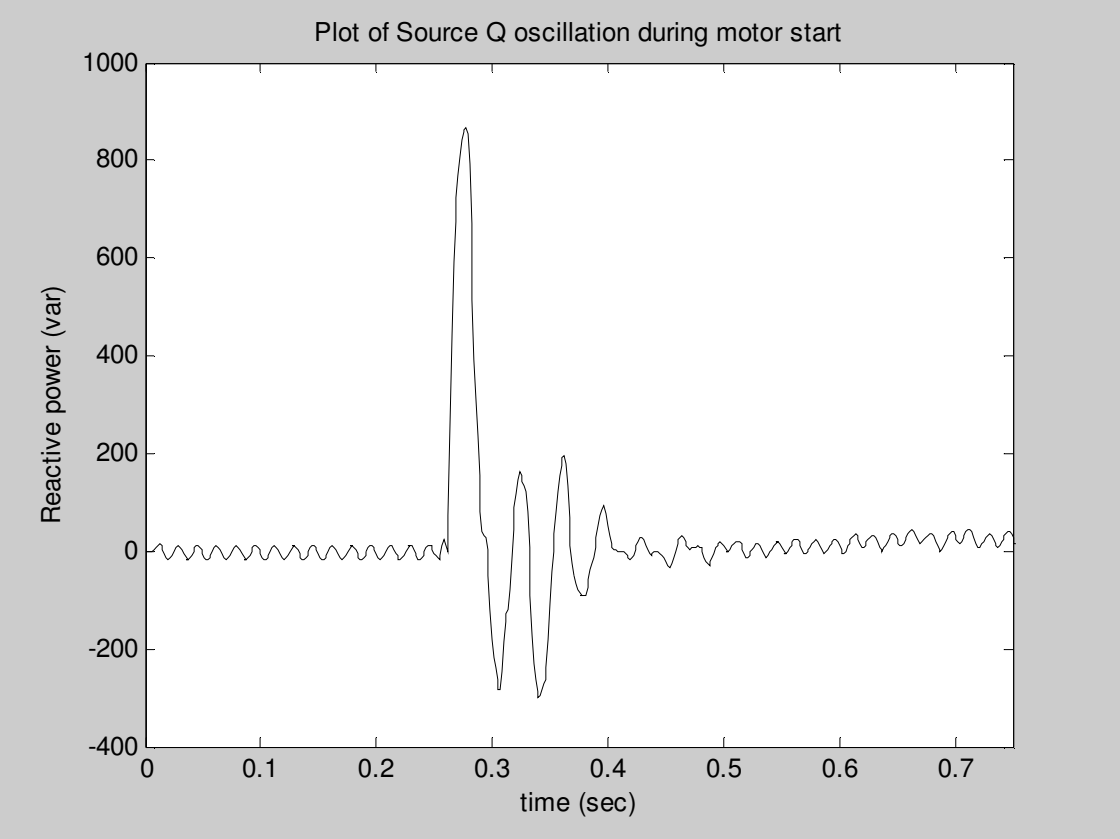

Figure 6.5: Plot of source Q oscillation during motor start.

This reactive power oscillation can be attributed to the nature of the load that was utilized during analysis of the system. The three phase induction motor was being operated under no load. Under this condition the reactive power demanded by the load was found to have an oscillatory nature which was magnified during motor startup. The controller was performing as expected and tracking the reactive power demanded by the load, but due to the oscillatory nature of the reactive power demanded by the motor, an oscillation in the source reactive power occurs.

Since the three phase motor produced oscillation in the reactive power, it was determined that analysis of a non-oscillatory reactive load was necessary to corroborate the assumptions made regarding three phase motor. For this purpose a simple circular

saw was utilized. The circular saw required a measurable amount of reactive power and since the blade was attached there was some appreciable physical loading to the saw which would help to smooth out the reactive power demand. A plot of the experimental results utilizing the saw as the load is found in Figure 6.6.

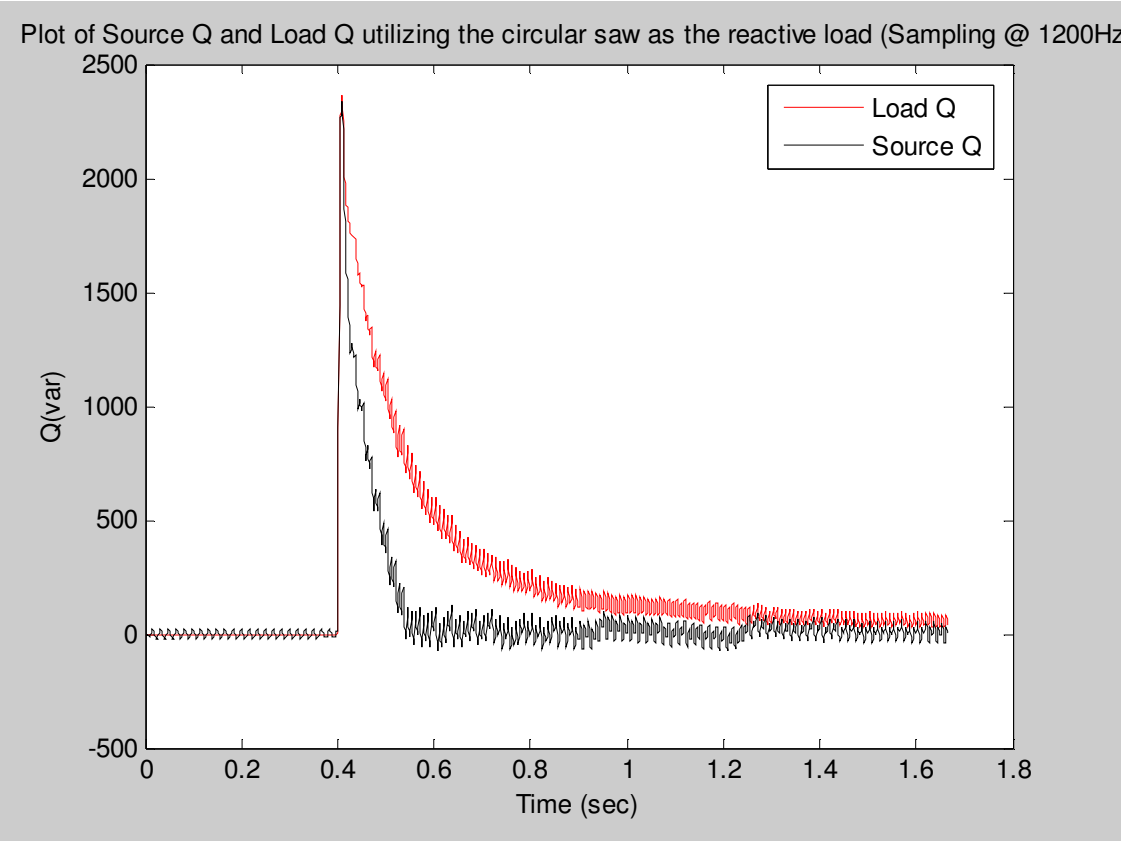

Figure 6.6: Plot of source Q and load Q utilizing the circular saw as the reactive load.

In Figure 6.6, it can be seen that the amount of reactive power drawn by the single phase circular saw during startup is much larger than the amount of reactive power drawn by a single phase of the three phase induction motor which is seen in Figures 6.2-6.4. Since the reactive power drawn by the saw is much larger the amount of reactive power compensation capabilities of the capacitors, it takes some time for the reactive power seen at the source to be reduced to near zero. More importantly, it can be seen in Figure

6.6 that the compensation controller closely tracks the reactive power demand drawn by the circular saw in a manner that does not cause an oscillation in the amount of corrective compensation, thus verifying the assumptions made in regards to the oscillation witnessed during the tests performed on the single phase of the three phase induction motor that the reactive power oscillation was due to the nature of the specific load in use.

Chapter 7

Conclusion

As demand for electricity continues to increase, the demand for grid delivered reactive power will also increase. This work was an attempt to develop an effective reactive power compensation system utilizing an IC controller that would be implemented at industrial power ratings to lower the reactive power demand drawn by industrial loads on the electrical grid. The reactive power compensation system utilized recent advances in the integrated circuit market as well as the power electronics market to provide an updated compensator model. A controller was proposed, constructed, and tested utilizing a PIC32 MCU and a multi-input, simultaneous sampling ADC. A software program utilizing a least squares algorithm to estimate signal magnitudes and phase angles was discussed and implemented to calculate reactive power demanded by a specified load and provide for proper corrective capacitor bank selection. A method to perform safe, reliable and transient free switching of capacitor banks via gate control circuitry and the use of a bidirectional switches constructed with IGBT modules was discussed and implemented.

These system components were constructed to form a model reactive power controller that was tested and proven to be reliable and effective. Although a full scale device was not implemented and only experimental testing was performed on a prototype

version of the compensator, the theory and design of the controller and compensator were proven to be effective on the scale in which it was tested and a reasonable assumption can be made towards the functionality of the same device built to industrial power ratings.

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