Energy Efficiency and Process Variation Tolerance of 45 nm Bulk and High-k CMOS Devices

by

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Abstract

With transistor sizes being reduced to sub 45nm ranges, we have seen an improvement in speed, better performance, and deeper integration of digital circuits. However, there has been a corresponding increase in power consumption, along with greater energy dissipation. The reason is because of increased leakage current in the channel. A proposed solution is a shift towards high-k materials and metal gate from poly-silicon gate of yesteryear. Reduced feature sizes also suffer from greater parametric process variations during lithography and cause identical circuits to behave differently.

With high-k technology overshadowing bulk technology ever since transistor sizes hit 45nm, a greater understanding of how the properties of high-k technology will affect digital devices especially their speed, power consumption, and energy dissipated upon voltage scaling is needed. Also, a better estimation of effects of parametric variations on circuits designed in high-k technology can provide valuable information which can be used to improve current designs.

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Chapter 1

Introduction

Gordon Moore, co-founder of Intel, famously stated in 1965 “The amount of transistors which can be inexpensively placed on an Integrated Circuit doubles every 18 months.” This statement has been dubbed as Moore’s law and scaling down of transistors has been the trend of the industry ever since [45]. We have come a long way since 1971 when the semiconductor manufacturing process was 10 μm, now we are adopting 32nm technology and research is being done to implement 22nm technology and beyond. Evolving nanometer CMOS technologies provide better functionality, higher performance and greater levels of integration but suffer from increased subthreshold leakage and excessive process variation. With the industry and market emphasizing on ”performance per watt” and ”performance per joule”, there is a growing need for new power and energy saving techniques for the increased power and energy dissipation caused due to scaling down of transistors.

This thesis work examines the 45 nm bulk and high-k metal gate technologies. Aggressive voltage scaling techniques described in previous research [18, 19, 41, 54, 60] was used to evaluate how a chosen circuit’s (32-bit ripple carry adder) power and energy consumption varies with a change in supply voltage (V_{dd}). After obtaining the optimum V_{dd} at which the minimum energy per cycle occurs, the results were compared the for both processes. The performance of a 32-bit ripple-carry adder circuit was evaluated for the entire range of supply voltages over which it displays a correct functionality. Lowering voltage increases delay, reducing the maximum clock frequency. We use the maximum permissible clock rate and the energy per cycle at that clock rate as two performance criteria.

The same 32-bit ripple carry adder circuit was designed in both 45 nm bulk and high-k technologies in order to compare which technology is better suited for a low power and higher energy efficient design. The minimum energy per cycle operation occurs at a subthreshold voltage for both designs. For minimum energy, the bulk technology has a very low performance ($\sim$ 7 MHz). However, high-k technology works at a much higher 250 MHz clock. Faster clock rate reduces the leakage energy making high-k almost twice as energy efficient compared to bulk.

This thesis also examines the relationship between energy per cycle versus supply voltage and how the minimum energy point behaves against speed and energy deviations due to process related parametric variations for different technologies provides a stable equilibrium. These deviations can be expected to be lower for high-k technology compared to those circuits designed in bulk technology that are commonly in use. These deviations are also lower compared to those at higher supply voltages that are commonly in use. Monte Carlo simulations for various parameters like threshold parameter (vth0), oxide thickness (t_{ox}), and mobility (u_0) of the technology model files [5] were conducted, and the variations were compared with the ideal scenario (no process variations) to see how total power and energy varied with the ideal number.

We conclude that there is a significant improvement in performance when the process is changed from bulk to high-k technology. The circuit modeled in high-k showed an operating frequency of 250 MHz which is a significant jump from bulk CMOS technology while retaining the advantage of low energy consumption. Furthermore, from the nature of the energy versus V_{dd} graph, we hypothesize that the operation at subthreshold V_{dd} is more resilient to process variation than that at the normal V_{dd} for both high-k and bulk technologies.

This thesis is divided further into five more chapters. Chapter two is the background chapter, and it gives a brief summary of all the important work done in the area of this thesis, and work that has been an inspiration to pursue this research.

This chapter has a section which explains about technology scaling, and why there has been a shift from bulk to high-k technology. In the next section, it gives a background about different voltage scaling techniques used in this thesis research. The last section talks about various kinds of process variation, and how each one can affect the threshold voltage and current of a digital circuit.

Chapter three talks about various tools and techniques used to conduct the experiments of this thesis. The working of various design tools like Leonardo Spectrum [4], Design Architect [1], HSPICE [3] etc. is explained, and how voltage scaling and process variation techniques are applied in this particular experiment is elaborated. Chapter four elaborates the methods by which the various tools and techniques discussed in the previous chapter are used to conduct the simulation of the circuit. It explains how the experiment was conducted, and gives a step by step procedure so as to provide the reader an easy guide to repeat the experiment if necessary.

Chapter five discusses the results of the experiment conducted using the methods mentioned in the previous chapter. Using the literature review as reference, this section validates the obtained results and explains the meaning of the data obtained from the experiment. Finally, Chapter six concludes the thesis by summarizing all the previous chapters, discusses the practical applications of this thesis, and gives an overview about the future direction this research could lead to.

Chapter 2

Background

In the 1980s, there was a switch to CMOS logic from other forms like TTL, NMOS logic etc. CMOS had a lot of advantages like high noise immunity, ability to integrate higher logic functions on a chip, and low power consumption [65]. The total power (P_{total}) dissipated in a CMOS logic gate consists of static power (P_{static}) and dynamic power ($P_{dynamic}$). In a typical CMOS circuit, most of the power dissipated is dynamic power while static power makes up a small part of the total power dissipated. Scaling down of transistors every two years [45] showed a reduction in total power dissipation because of a reduction in dynamic power as the transistors switched faster.

In 1971, Meindl and Swanson concluded that CMOS circuits offered an advantage of 10 to 1000 times in power-speed product when compared to a bi-polar junction transistor (BJT) [43]. They expanded on the work done by Keyes [30] and derived that "fundamental limits on power-speed performance are imposed by the uncertainty energy, the thermal energy, and the minimum high speed switching power." They identified the advantages of CMOS over BJT transistors like zero standby power drain, reduced load capacitance, and lower supply voltage of a CMOS digital circuit. All this was achieved without permitting degradation of fan-in and fan-out, and introducing noise immunity to a logic gate. They also showed the relation between the delay in a logical state and various circuit design parameters as shown below:

$$T_d \approx 10 \frac{L}{W} \frac{t_{ox}}{\varepsilon_{ox}} \frac{1}{\mu_n} \frac{C_L}{V_{dd}} \tag{2.1}$$

where

T_d = Delay per logical state

L = Channel length

W = Channel width

t_{ox} = Oxide thickness

ε_{ox} = Oxide permittivity

μ_n = Electron surface mobility

C_L = Load capacitance

V_{dd} = Supply voltage

However, when transistor sizes shrunk to 90 nm and below, two new trends began to emerge. The first one was that the industry literally "ran out of atoms" to insulate the transistor gate [13]. Basically, because of continuous scaling down of transistors following Moore's law [45], the SiO_2 layer insulating the gate had become only a few atoms thick and any further scaling would have caused a breakdown of the transistor because of the heat due to high power dissipation. The scientists at Intel came up with an innovative solution to counter this problem. They used materials with high dielectrics (high-k) like metal and metal oxides to build the transistor gates [2]. Other researchers were also researching into high-k transistor designs to achieve greater power and energy savings [11, 36, 44, 48]. Kim et al. [35] highlighted two components of leakage current. One is the sub-threshold leakage current (I_{sub}), which is a weak inversion current in the device, and the other is gate leakage current (I_{ox}) which is a tunneling current through the gate oxide insulation.

2.1 Technology Shift

Chandrakasan et al. [22] derived equations on how the leakage current components (I_{sub} and I_{ox}) depend on various parameters like threshold voltage, supply

voltage, and oxide thickness. Sub-threshold current (I_{sub}) is defined as:

$$I_{sub} = K_1 W e^{\frac{-V_{th}}{nV_\theta}} \left(1 - e^{\frac{-V_{dd}}{V_\theta}}\right) \tag{2.2}$$

where

W = Gate width

V_θ = Thermal voltage

V_{th} = Threshold voltage

V_{dd} = Supply voltage

K_1 and n are experimentally derived parameters

Roy et al. [50] said that the subthreshold conduction is dominated by the diffusion current caused due to weak inversion. This weak inversion current defines the off state leakage because of low V_{th}. The authors in [50] defined a characteristic called subthreshold slope which indicates how effectively a transistor can be turned off when V_{dd} is below V_{th} and is defined as:

$$S_t = 2.3\frac{kT}{q}\left(1 + \frac{C_{dm}}{C_{ox}}\right) \tag{2.3}$$

where

C_{dm} = Depletion layer capacitance

C_{ox} = Gate oxide capacitance

Ideally, the value of the slope in equation 2.3 should be as low as possible. With a shift towards high-k technology, due to the increase in gate oxide capacitance because of the use of high-k dielectric materials, transistors when operated in the subthreshold region switch faster due to a larger gate oxide capacitance resulting in a faster rate of decrease of I_{off}.

Another component of subthreshold current is the Drain Induced Barrier Lowering (DIBL) current. In a short channel device, the threshold voltage and subthreshold

current varies with the drain bias. It occurs when the energy barrier at the surface between the source and drain preventing electrons from flowing to the drain reduces, causing an increase in subthreshold current due to the lowering of the threshold voltage. Roy et al. showed that DIBL does not change the subthreshold slope but only affects the threshold voltage [50].

From equation 2.2, we can see there are two ways to reduce subthreshold current. The first one is to reduce the supply voltage hereby, reducing the exponential term in the equation and hence reducing the current. The other technique is to increase the threshold voltage (V_{th}), because it appears as a negative exponent, and hence can cause a dramatic change in current even in small changes. However, since the frequency of the circuit depends on the operating voltage and threshold voltage:

$$f \propto \frac{(V - V_{th})^{\alpha}}{V} \tag{2.4}$$

where

f = Frequency

α = Activity factor

An increase in V_{th} would cause a decrease in performance of the circuit which is undesirable.

The second equation derived by Chandraksan et al. [22] which illustrates the factors affecting gate-oxide leakage current is:

$$I_{ox} = K_2 W \left(\frac{V}{T_{ox}}\right)^2 e^{-\alpha T_{ox}/V} \tag{2.5}$$

where

W = Channel Width

T_{ox} = Oxide Thickness

K_2 and α are experimentally determined.

It is seen clearly that a reduction in the oxide thickness will cause an increase in the field across the gate-oxide. The high electric field along with a low oxide thickness caused the electrons to tunnel through the oxide layer resulting in gate oxide leakage current. There are two mechanisms of tunneling through the gate oxide: Fowler-Nordheim (FN) tunneling, and direct tunneling [50]. The authors showed that the tunneling probabilities are different in these two cases leading to two different types of gate leakages.

In FN tunneling, electrons tunnel into the conduction band of the oxide layer. In [50], Roy et al. derive that the FN current represents the tunneling through the triangular potential barrier and is only valid for $V_{ox} > \phi_{ox}$, where V_{ox} is the voltage drop across the oxide, and ϕ_{ox} is the barrier height for electrons in the conduction band. The authors noted that the measured value of FN tunneling is very small, and can be easily neglected when the device is in normal operating mode.

In direct tunneling, electrons tunnel directly to the gate through the forbidden energy gap of the oxide layer. This phenomena occurs in very thin oxide layers, namely on the order of 3-4 nm. Direct tunneling occurs when $V_{ox} < \phi_{ox}$ as electrons tunnel through the trapezoidal potential barrier instead of the triangular barrier [50]. Direct tunneling has three mechanisms: electron tunneling from conduction band (ECB), electron tunneling from valence band (EVB), and hole tunneling from valence band (HVB) [20]. In NMOS devices, ECB controls the gate to channel tunneling current, while EVB controls gate to body tunneling in depletion-inversion, and ECB controls it in accumulation. In PMOS devices, HVB controls the gate to channel tunneling, while gate to body leakage is controlled by EVB in depletion-inversion, and ECB in accumulation [20, 50]. The authors in [50] showed that tunneling associated with HVB is much less than tunneling associated with ECB, leading to lower leakage current in PMOS compared to NMOS.

As high-k gates can be thicker when compared to “bulk” or SiO_2 gates, gate leakage was reduced hence causing the devices to run cooler. These new transistors worked so well that Intel has started incorporating them in their new microprocessor designs starting from the Penryn chip lineup [13].

However, the shift in transistor design did not completely solve the primary problem faced by chip makers which was increased power and energy dissipation due to leakage at sub 90 nm technologies. With a reduction in transistor size, it was seen that although scaling caused a reduction in dynamic energy per cycle due to reduced capacitances in the circuit, there was an increase in leakage current of the circuit due to scaling down of the threshold voltage causing a significant increase in the static power dissipation [15]. Hence, there is a high interest in developing design techniques for power and energy efficient circuits using high leakage nanometer technologies.

2.2 Voltage Scaling

The speed of digital circuits is currently limited by the energy density. Shrinking feature sizes will continue to have the advantage of higher degree of integration, resulting in lower cost, provided energy density can be kept in control. Another characteristic that will assume increasing significance is tolerance to larger process variation of smaller features. The supply voltage has the strongest influence on all components of power and energy of a digital CMOS circuit.

Meindl and Swanson mathematically showed that to obtain the greatest power saving and the least power-speed product, the circuit must be operated at the lowest supply voltage practically possible by the design technology [57]. Their calculations showed that CMOS transistors did not abruptly turn off below the threshold voltage but acted as weak inversion devices. They determined that the smallest theoretical supply voltages at which circuits could function is approximately $8kT/q \approx 0.2V$ at $T = 300$ Kelvin, where k is the Boltzmann constant, T is absolute temperature, and

q is the electron charge. They also experimentally noticed that reduced operating temperatures permitted lower supply voltages theorized by [30]. One technique highlighted in their paper was ion implantation of boron for adjusting the turn-on voltages for both p and n transistors, achieving an operation close to their derived theoretical limit. However, because of very low performance for technologies in use at that time such low voltage operation was not adopted in practical systems.

Another approach has been to examine the energy minimization for circuits operating in the sub-threshold region. Studies have shown subthreshold operations have a number of advantages, namely, improved gain, noise margin, and greater energy efficiency at lower frequencies than the standard CMOS [54]. The authors simulated a chain of inverter gates forming a ring oscillator and noticed the following:

- The power consumption is linearly dependent with the operating frequency at higher frequencies due to the dominance of dynamic power component.
- The power consumption becomes independent of operating frequency at lower frequencies as static power is more dominant.
- Subthreshold circuits consume less power than strong inversion circuits at the same operating frequency.

The authors in [54] also simulated subthreshold pseudo-NMOS circuits and compared the results with its CMOS counterpart. They found that pseudo-NMOS has comparable in its power dissipation and robustness with CMOS but with less area, capacitance, and has an improved performance. However, very careful sizing of PMOS to NMOS ratio is needed in order to ensure the proper functioning of the circuit.

Calhoun and Chandrakasan further examine solutions for optimum supply voltage (V_{dd}) and threshold voltage (V_{th}) to minimize energy in subthreshold operations of digital circuits [19]. The authors identified that there is a maximum achievable frequency for a given circuit operating in the subthreshold region. They observed

that any work done on strong inversion optimization did not account for gate leakage even though it is a significant contributing factor in deep submicron technologies. Their calculations showed that parameters like gate current, gate-induced drain leakage (GIDL), and pn junction leakage are negligible when compared to sub-threshold current because they roll off much faster with V_{dd}. Their paper highlights the dependence of minimum energy point on technology, design characteristics of the circuit, and operating conditions like temperature, duty cycle, workload etc. They showed that in sub-threshold region, the optimum V_{dd} changes by several hundred milli volts when the above parameters are changed leading us to infer that circuits are very sensitive to process variations in subthreshold voltage operations. They also conclude that the current standard cell libraries also show reduced energy per operation for a minimum sized device.

In a follow up paper, Calhoun and Chandrakasan successfully showed test chips fabricated in 90nm technology operating at 330 mV supply voltage while obtaining energy savings on the order of 9X compared to other reduced performance scenarios [18]. They proposed a technique called "Ultra-dynamic voltage scaling" where the circuit will work at normal operating voltage when speed of circuit or performance is the primary criteria and at sub-threshold voltage when energy conservation is the main motive. This technique made sense as for a majority of circuits, sub-threshold operations was only needed when a major section of the chip was in "OFF" mode, and needed to "wake up" or if the entire circuits were in sub-threshold region (e.g. microsensor mode). This gave the users flexibility to operate the circuits either in an energy efficient mode or performance mode depending upon their need.

Kwong and Chandrakasan highlight two major challenges faced by sub-threshold voltage designs and can potentially impact circuit functionality [41]. The first one was that the drive-current (I_{on}) is lower in sub-threshold region when compared to strong inversion. Hence, the ratio of active to idle leakage current (I_{on}/I_{off}) is lower. This

means that idle leakage may counter the active current and the output of the device may not pull completely to V_{dd} or ground. Another problem faced by sub-threshold voltage operations highlighted by [41] was process variations. Global variations can affect the entire circuit and its operations throughout the voltage scale. In sub-threshold regions, it is seen at skewed P/N corners with either strong PMOS/weak NMOS or vice versa. However, local fluctuations mainly, random dopant fluctuations (RDF) cause random shifts in threshold voltage (V_{th}). These shifts can cause the shifting of the minimum energy operating point and hence should be accounted in circuit modeling as well. The authors also concluded that optimum V_{dd} need not occur at the lowest voltage at which the circuit functions correctly. This result was quite significant as it disproved the conclusion drawn by Meindl and Swanson [43]. The reason was the increased leakage of the sub-micron devices.

Zhai et al. highlighted the challenges of subthreshold voltage operation in SRAM designs [63]. They highlighted three key challenges. First was a reduced I_{on}/I_{off} current ratio which led to a difficulty in distinguishing between the read current of an accessed cell and the leakage current in the unaccessed cell. Another key problem highlighted by [63] was the change in gate sizing requirements in low voltage operations. The read and write stability of any conventional SRAM are heavily dependent upon the pull-up, pull-down, and pass transistors whose strengths can be drastically affected due to skewed PMOS to NMOS V_{th} ratios. The most important challenge to low voltage SRAM designs is the increased sensitivity to process variations. Even small variations have known to cause mismatches hence causing functional failure [63]. The authors presented a novel 6 transistor SRAM design in 0.13 μm capable of overcoming these challenges and successfully operating at subthreshold voltages. Their results showed that the proposed design works successfully between 1.2 V to 193 mV while providing a 36% improvement in energy over other SRAM proposed

designs with less area overhead. Hanson et al. have also designed a processor capable of working in the subthreshold voltage region of transistors [25]. Their design was used for sensor applications and showed correct operations at 350 mV operating voltage while consuming only 3.5pJ of energy per cycle.

Dual voltage design in the subthreshold voltage range has recently been studied and shown to have energy and speed advantages [33, 34]. In [34], Kim and Agrawal obtained a point which they call the "true minimum" by using dual sub-threshold voltage supplies. Using these dual supplies, the authors were able to lower the energy per cycle to a point below the known minimum energy energy point. They avoided the use of level converters which are usually needed in any dual level voltage design by implementing mixed integer linear programs (MILP) hereby negating the disadvantages of level converters such as delay insertion and power consumption. The authors were successfully able to achieve a saving of 23% for a 16 bit ripple carry adder and 5% for a 4×4 multiplier which was a worst case scenario in their case. In their follow up paper [33], they achieved an energy savings of $\sim 25\%$ for various ISCAS'85 benchmark circuits.

Subthreshold voltage operation may also have an advantage in extending the battery lifetime in portable and mobile electronics [40]. In this paper, Kulkarni and Agrawal examined the energy consumption of a circuit and observed the impact of the efficiency of the battery. They observed the need for controlling the power consumption in order to control the size of the battery. They demonstrated that for most circuits, the efficiency of the battery reduces for higher currents and operating the battery at sub-threshold voltages (0.3 V in their case) vastly improved the battery lifetime, which is critical for today's portable electronic devices.

Abouzeid et al. developed a 45nm CMOS cell library which was optimized for ultra-low power applications. They developed a decoder circuit, which operated at a speed of 457 kHz when operated at 0.35 V [6]. That point was the minimum energy

point and they achieved a total energy consumption of 3.9 fJ per cycle [6]. Tran and Baas designed a 32 bit fast adder which functioned successfully at subthreshold voltage regions. They showed that their design performed successfully while being most energy efficient at 0.37 V with a frequency of 100 MHz [58]. However, their circuit was designed in PTM 45nm bulk technology. Since, the shift towards high-k, a study is needed to see how the shift towards high-k would affect circuit performance in terms of speed and energy efficiency.

2.3 Process Variation

Till now, we have seen a lot of mentions of the term "process variation". It is the natural variation occurring in the parameters of transistors (like threshold parameter, oxide thickness, channel width and length, mobility etc.) during the fabrication of integrated circuits. William Shockley first discovered random variation in semiconductor devices during his analysis of random fluctuations in junction breakdown [53]. He theorized that the effects of spatial fluctuations of donor and acceptor ions are randomly distributed according to a Poisson distribution. Keyes expanded on Shockley's work by studying the effect of randomness of impurity atoms on the electrical characteristics of a MOSFET [31]. From his models, he concluded that threshold voltages are normally distributed in a square transistor.

In 1974, Schemmert and Zimmer used the conclusion drawn by Bauer et al. [12] that threshold voltage (V_{th}) depends upon the depth of penetration of ions during ion implantation, among other parameters and introduced a procedure for minimizing threshold-voltage sensitivity of ion-implanted MOSFETs due to different process parameters [51]. Their results showed a maximum deviation of $\pm 10\%$ for t_{ox}. A Monte Carlo analysis on a small MOSFET conducted by Alvarez and Akers in 1981 showed

that controlling the process variation parameters to ±10% yielded a threshold voltage variation of ±15% [8]. They also noticed that the distribution was normal, and almost 95% of the variance was around ±100 mV about the mean threshold voltage.

Agrawal and Nassif further classify process variation into two sub-categories: random variation and systematic variations [7]. They further classify systematic variations into across-field and layout dependent variations. The authors in [7] explain that across-field variations can cause identical devices at different locations of the reticle to behave differently. They classify the sources of error are caused due to photolithographic and etching sources (dose, focus, expose variations etc.), lens aberrations, mask errors, and variations in etch loading [16, 17, 27, 62]. The authors characterize layout dependent variations as the one causing different layouts of the same same device to have different characteristics even when they are close to each other. They note that these variations are predictable and can be modeled according to different deterministic factors such as layout structure and topological environment surrounding the device layout.

Agrawal and Nassif [7] characterize random variation as unpredictable random uncertainties in the fabrication process like fluctuations in the number and location of dopant atoms, and poly-silicon gate line-edge roughness. According to authors in [9, 23, 24, 32], line-edge roughness and line-width roughness can cause an increase in sub-threshold current and a degradation in the threshold voltage.

Random variations can cause device mismatch of identical and adjacent devices and the deviation of threshold voltage caused due to these variations is represented by an equation derived by Stolk et al. [55]:

$$\sigma_{V_t} = \left(\frac{\sqrt[4]{4q^3\epsilon_{Si}\phi_B}}{2}\right).\frac{T_{ox}}{\epsilon_{ox}}.\frac{\sqrt[4]{N}}{\sqrt{W_{eff}L_{eff}}} \tag{2.6}$$

where

T_{ox} = Gate oxide thickness

N = Channel Dopant concentration

W_{eff} and L_{eff} = Effective channel width and length

$\epsilon_{Si} and \epsilon_{ox}$ = Permittivity of silicon and oxide

$\phi_B = 2k_BT\ln(N/n_i)$ (with k_B Boltzmann's constant, T the absolute temperature, and n_i the intrinsic carrier concentration)

The above equation illustrates that mismatch reduces with a decrease in doping (N) and gate oxide thickness (T_{ox}) and increases when effective length and width decreases.

Kuhn et al. from the Technology and Manufacturing Group at Intel cited that high-k metal gates are also subject to variations in oxide thickness, fixed charge, and interference traps [39]. They note that these physical changes result in parametric variations in drive current, gate tunneling current, or threshold voltage. Studies show that intrinsic threshold voltage fluctuations induced by local oxide thickness variations become comparable to voltage fluctuations introduced by Random Dopant Fluctuations (RDF) in deep submicron MOSFETs [10]. By evaluating gate-tunneling leakage current theoretically and experimentally for 1.2 - 2.8 nm SiO_2 gate oxides in MOSFETs, Koh et al. showed that when the gate oxide tunnel resistance becomes comparable to the gate poly-Si resistance, the statistical distribution of gate-tunnel leakage current causes large fluctuations in V_{th} [37]. Kaushik et al. studied the effects of fixed charge in the high-k layer and concluded that mobility and uniformity of threshold voltages were affected by variations in the fixed charge [29].

Another concern highlighted by [39] is mobility degradation and V_{th} instability due to fast transient charging (FTC) in electron traps. Investigation of effects of FTC by studying the impacts metal gate electrodes on mobility degradation suggest that the increase in FTC can be attributed to the higher densities of the oxygen atom

vacancies in the dielectric caused due to dielectric induced scavenging processes [61]. Various optimization techniques have been shown to reduce the charge trapping process [38, 49].

Management of process variation is playing a greater important role in technology scaling and CMOS literature has always shown process variation as a critical element in semiconductor fabrication. Until better fabrication and post-lithography techniques are designed to minimize process variations, it must be considered in all circuit and design simulations in order to accurately guess how a real world model would actually function.

Chapter 3

Tools and Techniques

This section gives an introduction to the various tools and techniques used to conduct the experiments of this thesis. There are different tools for circuit modeling, netlist generation, simulation, process variation, and result analysis. Also, there are different techniques to estimate the minimum energy operating point, and simulation of circuit by varying different process parameters.

3.1 Test Circuit

The first step to performing any experiment is to choose a test circuit. After a specific test circuit is chosen, the decided tools will be used to apply the appropriate technique for conducting the experiment. Usually, a simple replicable circuit or a benchmark circuit where performance and working can be easily monitored is chosen. For this thesis, a 32-bit ripple carry adder was chosen for its simple design yet it has a sufficient logic depth for the proper utilization of the design technique.

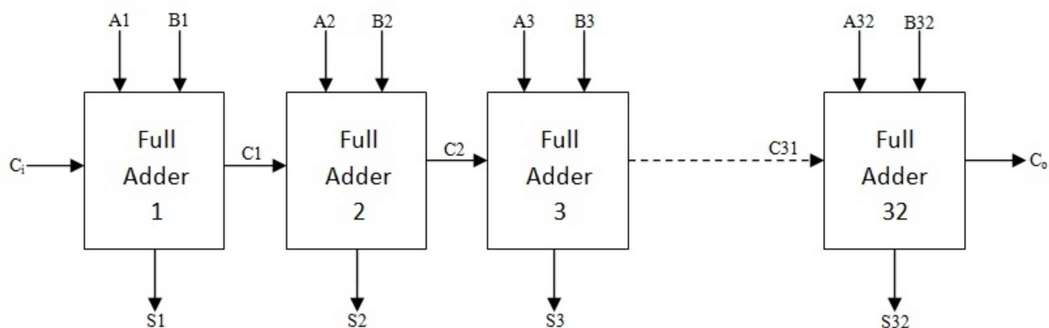


Figure 3.1: Schematic of a 32-bit ripple carry adder.

Figure 3.1 shows the basic schematic of a 32-bit ripple carry adder. A[1:32] and B[1:32] are two 32-bit inputs to the adder, C_i is the carry in to the first adder, C_o is the carry out from the last adder, and S[1:32] are the sum outputs of each full adder cell.

A ripple carry adder consists of a chain of full adders where the carry output of the least significant bit (LSB) adder goes into the next adder. This way, the carry signal "ripples" through the chain of adders hence the term, ripple carry adder. In a 32-bit ripple carry adder, the carry signal must propagate through 32 iterations of 1 bit full adders before the next set of input vectors can be applied. Thus, the critical path delay of the adder is defined as total path delay between the carry in (C_i) signal given to the first adder and the carry out (C_o) of the last adder.

3.2 IC Design and Simulation Tools

This section discusses the various tools used for designing and simulating the test circuit.

3.2.1 Leonardo Spectrum

Leonardo Spectrum [4] is a logic synthesis tool from Mentor Graphics Corp. Logic synthesis is the process of translating a Hardware Description Language (HDL) into a technology specific gate-level description. Leonardo Spectrum [4] offers design capture, VHDL and Verilog entry, register transfer level debugging for logic synthesis, constraint based optimization, timing analysis, encapsulated place-and-route, and schematic viewing for Complex Programmable Logic Devices (CPLD, Field Programmable Gate Arrays (FPGAs), and Application Specific Integrated Circuits (ASICs).

3.2.2 Design Architect

Design Architect [1] is a scalable design definition environment provided by Mentor Graphics Corp. Since, it can interface easily with Leonardo Spectrum, this tool can import the netlist generated by Leonardo Spectrum, and display the Register level or transistor level design of the desired circuit. It can model digital, analog or mixed-signal blocks, and can quickly simulate the entire hierarchal design.

3.2.3 HSPICE

Simulation Program with Integrated Circuit Emphasis (SPICE) is a general purpose electronic circuit simulator used to check the integrity of circuit design and predict circuit behavior [47]. HSPICE is a circuit simulator tool derived from SPICE and designed by Synopsys Inc. in order to predict the timing, functionality, power consumption, and yield of their designs. HSPICE takes a text netlist describing the circuit elements like transistors, resistors, capacitors etc. and their connections, and translate this description into solvable equations, and produce the final result. It is common to use SPICE simulators to simulate Monte Carlo Simulations to document the effect of process variations on any circuit, hence providing an accurate approximation of the yield of the circuit when fabricated.

3.3 Circuit Design and Simulation Techniques

This section explains how the circuit was modeled using a HDL before being optimized by the tools explained in the previous section. It also explains how process variation for various design parameters was modeled using Monte Carlo simulations in SPICE.

3.3.1 VHDL

A popular high level description language for system and circuit design is VHDL. The language has various levels of abstraction and supports behavioral, structural, and dataflow descriptions. Although behavioral statements are executed sequentially, the structural and dataflow descriptions in VHDL display a concurrent behavior i.e, all statements written in that format are executed concurrently. Hence, the order of the statements are not important.

3.3.2 Monte Carlo Analysis

Monte Carlo experiments can be defined as a collection of computational algorithms that compute results by repeated random sampling. This method is most often used when it is impractical or impossible to compute an exact result because of reliance on random numbers. Monte Carlo simulations are particularly useful in studying process variations, more specifically, how variations in process parameters (like vth0, mobility, oxide thickness etc.) of transistors can affect the various functional parameters (like delay, drive current, threshold voltage, power dissipation, energy etc.) of the circuit. Designers use this method to correctly estimate 3 sigma corners and optimize their circuits to get the best yields.

3.4 Predictive Technology Model

Predictive Technology Models are customizable and predictive model files for transistor and interconnect technologies. They are compatible with SPICE, easily scalable for a wide range of process variations, and provide accurate models from 180 nm to sub-45 nm technologies [5]. In today's fast paced scaling of MOSFET technology, research and circuit design must begin before a future generation of MOSFET technology is fully implemented [21]. Challenges like process variations, leakage current, and reliability must be properly addressed for each technology before being

embraced fully [64]. Hence, it is important for researchers to work with fully customizable and accurate transistor models for each technology. Almost all semiconductor companies guard their models closely, and do not disclose the data of their models in order to prevent industrial espionage. Hence, it is critical for researchers to use models which are not only available in open source but also provide accurate results when compared to benchmark circuits designed using industrial models.

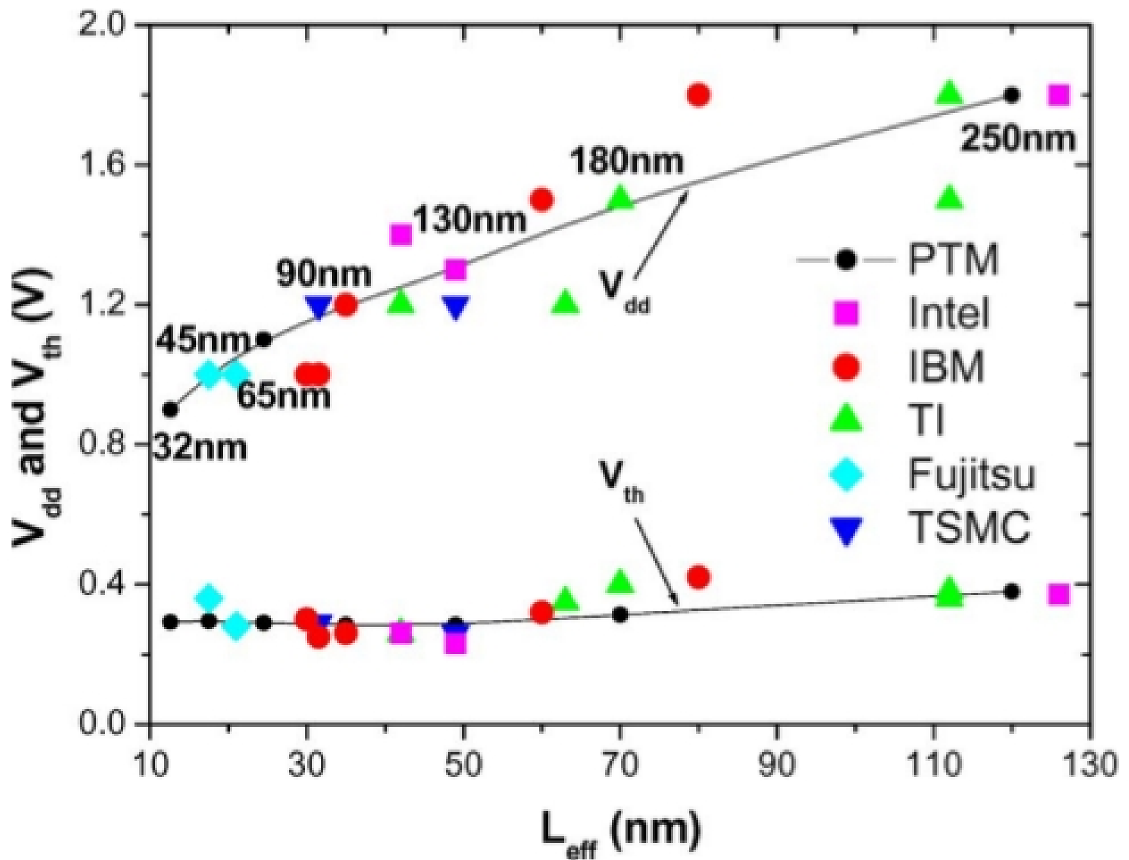


Figure 3.2: Comparison of PTM and industry's technology model for V_{dd} and V_{th} scaling vs. effective length (L_{eff}) for for a range of technology nodes [64].

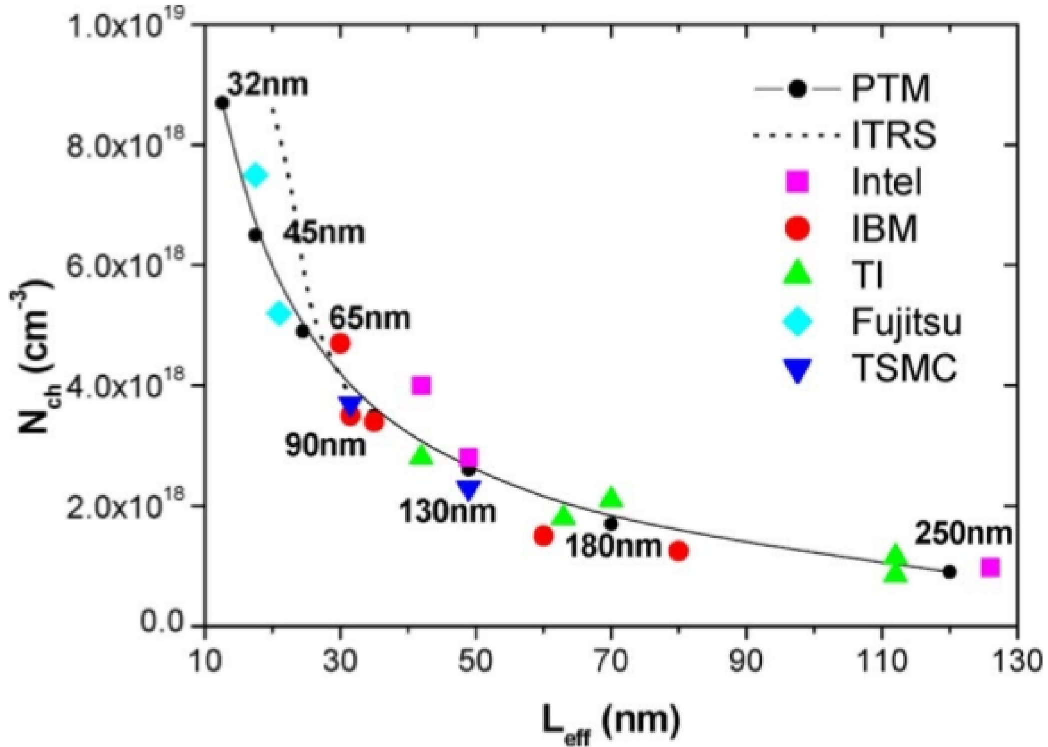


Figure 3.3: Comparison of PTM and industry's technology model for channel doping concentration N_{ch} vs. effective length (L_{eff}) for for a range of technology nodes [64].

The authors in [64] have successfully developed technology models for a range of 130nm to sub-45nm. By analyzing Figures 3.2 and 3.3 which were drawn from their paper, the conclusion shows that results obtained from their model matches closely with data obtained from the industry. PTM has especially shown excellent predictions for 45 nm technology node, along with better scalability for a wide range of process and design conditions. Hence, it is highly preferable to use PTM models for use in modeling and simulation of circuits when industrial models are not available.

Chapter 4

Methodology

4.1 Test Circuit Modeling

The 32-bit ripple carry adder circuit was first designed using VHDL. The VHDL model was then imported into Leonardo Spectrum tool [4], which can create a simulatable netlist for the VHDL model. A circuit netlist can be created for any technology. For this thesis, the circuit was modeled in TSMC 0.18 micron technology. Leonardo Spectrum generated a verilog file which contained the properly synthesized netlist. This synthesized verilog file was then imported into the Design Architect tool [1], which gave the schematic of the 32-bit ripple carry adder using the standard TSMC cell libraries.

The Design Architect tool has an internal SPICE simulator which can internally generate a SPICE netlist. This SPICE netlist was further modified by changing the width of all transistors from 0.18μm to 45 nm while preserving the width over length (W/L) ratio. Instead of using the TSMC libraries as used by the Design Architect, we used the Predictive Technology Model (PTM) for both 45 nm bulk and high-k technologies [5]. This was done because Design Architect did not provide 45 nm libraries, and the research required us to simulate circuits in the latest transistor technologies.

4.2 Minimum Energy Point Estimation

To calculate the voltage at which the circuit operates at minimum energy, we use a technique called "Dynamic Voltage Scaling" used by Calhoun and Chandrakasan

[19]. This technique consists of changing the operating voltage step by step, measuring the critical path delay, and power dissipated by the circuit at each voltage step, and calculating the energy dissipated by multiplying the power and the delay.

$$E_{avg} = P_{avg} \times t \tag{4.1}$$

$$P_{avg} = V_{dd} \times I_{avg} \tag{4.2}$$

where

E_{avg} = Average dissipated energy

t = Critical path delay

P_{avg} = Average dissipated power

V_{dd} = Operating voltage

I_{avg} = Average current drawn by the circuit

At each voltage step, there is a change in path delay as well as drawn current. In other words, when voltage is decreased, there is an decrease in drawn current but an increase in critical path delay. Hence, to find the minimum energy dissipated by the circuit, the delay and current at each voltage step needs to be measured.

To calculate the delay at each voltage, the critical path needs to be activated. Therefore, the following vectors were applied. First, all the inputs (A, B, and C_i) were initialized to 0. This sets all the sum outputs and the carryout to value 0. In the second vector, all A inputs (A[1:32]) were set to 1, while keeping all B inputs (B[1:32]) to 0. All sum outputs thus became 1, but there was no change in the carry signal and there was no rippling of bits through the carry signals. A third vector then set at C_i at 1 to activate the critical path. As a carry was propagated through all 32 full adders, two critical paths were simultaneously activated. While the carry bits in all the 32 full adders changed to 1, sum outputs were simultaneously brought back to 0. The time delay between the initializing of the 3rd test vector, and changing of

the output signals of the final adder was measured.

$$t_1 = t_{C_o} - t_{C_i} \tag{4.3}$$

$$t_2 = t_{S32} - t_{C_i} \tag{4.4}$$

where

t_1 and t_2 = Path delays

t_{C_i} = Time when C_i switched from 0 to 1

t_{C_o} = Time when C_o switched from 0 to 1

t_{C_i} = Time when S32 switched from 1 to 0

The largest time delay out of t_1 and t_2 is deemed the critical path delay. The critical path determines the frequency of test vector application. This frequency changes for each voltage point and needs to be measured each time there is a voltage step change.

After finding the frequency, 100 random vectors were applied to the inputs of the 32-bit ripple carry adder at the maximum operating frequency at that voltage point. On conducting the SPICE simulations using HSPICE [3], the average current consumed by the circuit was measured. It was then multiplied by voltage to give the average power dissipated by the test circuit as given in equation 4.2. To determine the average Energy per cycle, the average power was multiplied with the delay of the circuit as shown in equation 4.1. The average energy per cycle for each voltage step was calculated, tabulated and graphed.

4.3 Process Variation

The results obtained using the above described technique is only applicable for an ideal circuit. However, in real life, process variations can cause changes in various transistor parameters like threshold parameter, mobility, oxide thickness etc. Hence,

it is important to investigate how a circuit's characteristics like threshold current, delay etc. changes with process variation.

We use Monte Carlo analysis to model process variations in the circuit. For this circuit, we perform three types of variations. In the first one, we change the threshold parameter (vth0) by 16%. In the second one, the oxide thickness (t_{ox}) is varied by a factor of 20%. The last one consists of a variance of both vth0 and t_{ox}, and then calculating the mean and sigma values of all three cases. We compare two cases to test the effect of process variations on the circuit.

First, we compare the operation of the circuit at 0.3 V for both bulk and high-k technologies. More specifically, the critical path delays are measured under the effect of process variation, and then the mean value is used to run the adder circuit to measure the average current drawn. The average power dissipated, and energy per cycle are calculated using equations 4.1 and 4.2, and the means are compared with the ideal scenario. The second case consists of comparing the operation of circuit designed in high k technology at 0.9 V and 0.3 V. We calculate how process variations affect the critical path delays and energy per cycle for both voltage points, and compare the means.

Chapter 5

Results

5.1 Inverter Simulation

Current flowing in a circuit has two components: static current and dynamic current. Furthermore, static (or leakage) current has two major components: sub-threshold leakage and gate oxide leakage. Due to reduced feature size of the gate oxide in bulk MOSFET designs, there is an increase in gate oxide leakage which can affect the delay of a circuit because of electron tunneling through the oxide layer. This issue was addressed by a switch to high-k designs. However, with high-k, due to the presence of a larger dielectric, the oxide capacitance increases leading to larger dynamic current flowing through the circuit. Secondly, high-k designs have a thicker oxide layer compared to bulk designs which led to a greater sub-threshold current flowing through the transistor.

Hence, it is evident that high-k designs will have more dynamic and leakage current flowing through the circuit. However, because of greater gate oxide leakage in bulk designs, the delays of circuits designed in bulk technology will be significantly larger compared to high-k designs. Therefore, we expect the energy per cycle for high-k designs to be lower compared to bulk designs inspite of high-k having a higher current flow because of the tremendous gain in speed.

Before we performed SPICE simulations on the 32-bit ripple carry adder, we simulated a single inverter designed in both 45nm bulk and high-k technologies to understand how current, delay, and energy varies with a switch in technology. We operated the inverter for 10 clock cycles at 0.4 V. Within those 10 cycles, there were 2 transitions occurring 0→1, and a 1→0 transition. The other 8 cycles were idle

cycles i.e no transitions were occurring. During idle periods, the only current flowing through the circuit will be leakage current which will lead to static power dissipation. During the transition cycles, both leakage and drive current will be flowing, hence the power consumed in that period would be the sum of both static and dynamic power. To calculate dynamic current, we can subtract the static current flowing during idle periods the current flowing during the transition cycles.

Table 5.1 shows the values of dynamic current, static current, average current over 10 clock cycles, and clock period (gate delay) for both technologies.

Table 5.1: Comparison of various currents and clock period of a CMOS inverter operating at 0.4 V for 45nm bulk and high-k technologies.

Technology	Static Current $\times 10^{-7}$ (A)	Dynamic Current $\times 10^{-5}$ (A)	Average Current $\times 10^{-6}$ (A)	Clock Period $\times 10^{-12}$ (s)	Energy per cycle $\times 10^{-18}$ (J)
45nm bulk	0.11	0.82	0.83	25.9	8.59
45nm high-k	3.02	5.48	5.72	3.63	8.30

From Table 5.1, it is clearly seen that energy per cycle for high-k designs is lower compared to bulk design even though there is a greater current flowing through the inverter designed in high-k. For circuits with greater critical path delay, we expect the gap between the energy per cycles to further increase as increased gate oxide leakage would cause larger circuits to run much slower.

5.2 Minimum Energy Point Estimation

From the Tables 5.2 and 5.3, it is evident that when there is a decrease in operating voltage, there is a simultaneous decrease in average drive current and an increase in critical path delay. However, it is seen that with a drop in voltage, the decrease in current is greater than the increase in delay. Hence, there is a gradual reduction in energy per cycle with every voltage drop. We also see that, at a particular voltage (0.3 V), the energy dissipated per cycle is minimum for the circuit, and

for voltages below that point, the energy starts to increase. The reason for this is because, as voltage decreases further below that point, the savings in current cannot compensate the huge increase in delay which causes the energy per cycle to increase.

Also, the circuit works faster when designed in high-k technology rather than in bulk technology. From Tables 5.2 and 5.3, we find the frequency of operation at the optimum energy (minimum energy/cycle) point is 250 MHz (critical path delay is 4 ns) for high-k technology while for bulk technology the corresponding frequency for minimum energy/cycle operation is just above 7 MHz (critical path delay is 137 ns). The reason is because there is more drive current flowing through the circuit, hence causing the transistors to switch faster, and the critical path delay is reduced due to reduced gate current leakage in high-k.

Notably, it is seen that circuits modeled in high-k technology has the advantage of greater energy efficiency as seen in Figure 5.1. In high-k technology, the minimum energy obtained is lower at the same voltage than that for the bulk technology. Comparing the minimum energy operations for the two technologies, we find that for high-k energy per cycle is 40% lower compared to that for the bulk technology. The minimum energy point occurs at 0.3 V for both high-k and bulk technologies. Again, the reason is because although there is a higher drive current in the circuit designed in high-k technology, the improvement in delay is more than enough to accommodate the increase in the drive current, hence causing energy savings.

Table 5.2: Simulated performance of 32-bit ripple carry adder designed in 45nm bulk technology.

Operating Voltage (V)	Average Current $\times 10^{-5}$ (A)	Average Power $\times 10^{-6}$ (W)	Critical path delay $\times 10^{-9}$ (s)	Average energy/cycle $\times 10^{-14}$ (J)
1	18.6	186	0.939	17.5
0.9	12.7	114	1.11	12.7
0.8	8.97	71.7	1.38	9.89
0.7	5.63	39.4	1.88	7.41
0.6	2.96	17.8	3.01	5.36
0.5	1.15	5.74	6.52	3.74
0.4	2.76	1.1	23.4	2.58
0.35	0.119	0.416	54.3	2.26
⋆0.3	0.053	0.16	137	2.19
0.2	0.017	0.035	923	3.19

Table 5.3: Simulated performance of 32-bit ripple carry adder designed in 45nm high-k technology.

Operating Voltage (V)	Average Current $\times 10^{-5}$ (A)	Average Power $\times 10^{-6}$ (W)	Critical path delay $\times 10^{-9}$ (s)	Average energy/cycle $\times 10^{-14}$ (J)
1	34.9	349	0.45	15.6
0.9	25.7	231	0.47	10.9
0.8	20	152	0.51	8.10
0.7	15.5	109	0.57	6.16
0.6	10.5	62.9	0.67	4.19
0.5	6.38	31.9	0.87	2.78
0.4	3.20	12.8	1.42	1.82
0.35	1.84	6.42	2.12	1.36
⋆0.3	1.09	3.28	3.71	1.22
0.2	0.382	0.764	18.7	1.43

⋆ Highlighted row indicates minimum energy voltage point

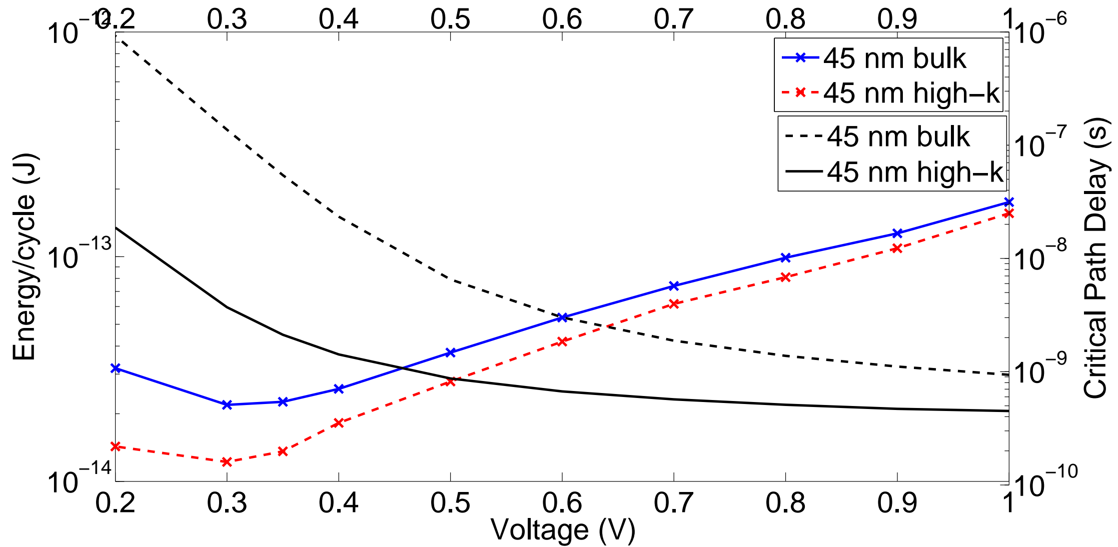


Figure 5.1: Energy per cycle vs. V_{dd} for 32-bit ripple carry adder simulated in 45nm bulk and high-k CMOS.

5.3 Process Variation

All circuits suffer from process variation in the real world. Hence, it is important to understand how process variation will affect voltage scaling or more specifically, the minimum energy point with the nominal operating point. On analyzing the graphs in Figure 5.1, we infer that circuits designed in 45nm high-k technology should be more resilient to process variations because the energy-delay curve is lower when compared to circuits designed in 45nm bulk technology and that minor changes would not cause any drastic effect on efficiency or performance. Two parameters, threshold parameter (vth0) and oxide thickness (t_{ox}) are varied separately, and then together. vth0 is varied by a factor of 16% because that is the deviation cited by the ITRS roadmap [26]. Oxide thickness is varied by a factor of 20% as calculated by the authors in [46].

The delay was measured after performing a Monte Carlo analysis of a 1000 samples of the circuit for the voltage points of 0.9 V and 0.3 V in high-k technology, and for the point of 0.3 V designed in bulk technology. The delays obtained by the analysis of the 1000 samples was compared with the delays obtained by the analysis

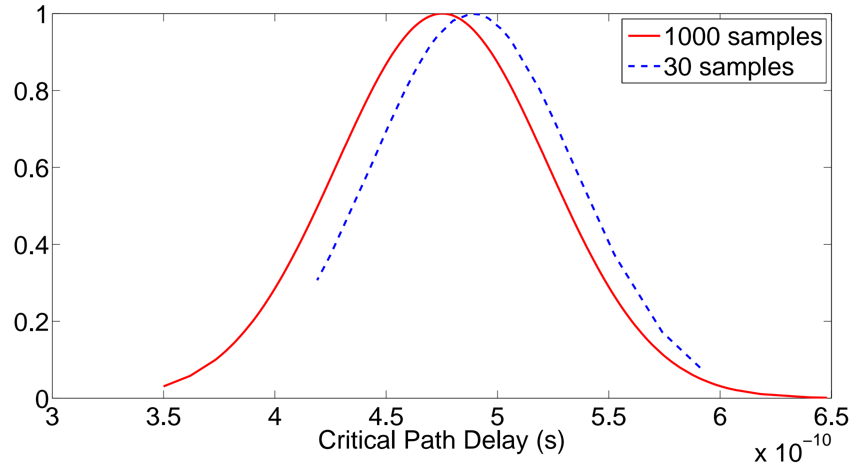
of 30 random samples. Critical path delay was measured for each sample through HSPICE [3] simulation using a vector pair that activated the critical path.

The means (t_m) and standard deviations (σ) of the critical path delay for circuits operating at 0.3 V designed in 45nm bulk and high-k technologies, and 0.9 V at high-k technology are tabulated in Table 5.4. It is seen that the means and standard deviations are closely comparable for the 30 and 1000 random samples establishing the fact that 30 random samples can be used to model process variations.

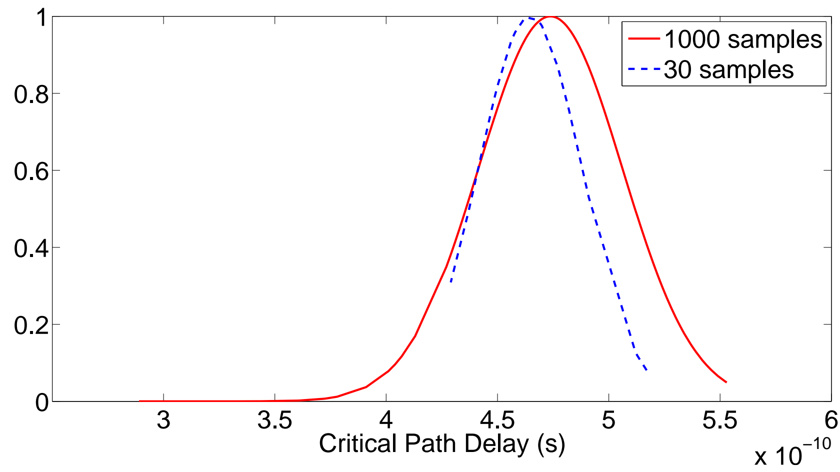
Table 5.4: Comparison of mean and standard deviation of critical path delays for 30 and 1000 random samples.

Operating Voltage	Process Variations	30 samples		1000 samples	
		Mean (t_m) $\times 10^{-9}$ s	Standard Deviation (σ) $\times 10^{-9}$ s	Mean (t_m) $\times 10^{-9}$ s	Standard Deviation (σ) $\times 10^{-9}$ s
0.9 V high-k	vth0	0.488	0.045	0.475	0.048
	t_{ox}	0.465	0.023	0.474	0.032
	Both	0.477	0.055	0.48	0.062
0.3 V high-k	vth0	6.36	4.45	6.29	8.57
	t_{ox}	4.61	1.52	4.23	1.65
	Both	6.15	4.95	6.85	9.25
0.3 V bulk	vth0	274.4	210.32	225.7	207.32
	t_{ox}	279.6	171.7	204.6	237.4
	Both	192.3	202.03	241.1	238.65

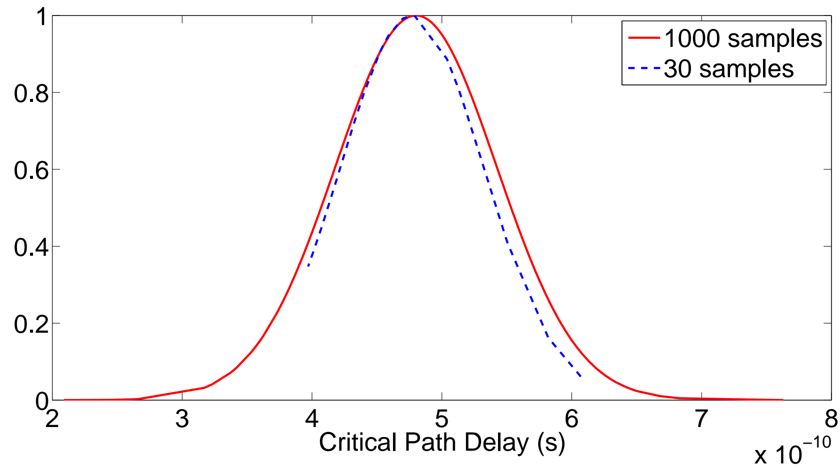
The following figures (Figures 5.2 - 5.4) compare the histograms of the delays for the 30 and 1000 random samples. It can be clearly seen that the two histograms overlap closely meaning that simulations done using 30 random samples is equivalent to simulations done using 1000 random samples. This experiment was done to establish the above stated fact since all the following results were done using 30 random samples. Experiments using 1000 random samples were unfeasible because calculating the energy can take a duration of almost 3 days for one voltage point, and secondly, there was not enough memory in the computer to store the output from the SPICE file.



(a) Variation of vth0 by 16%

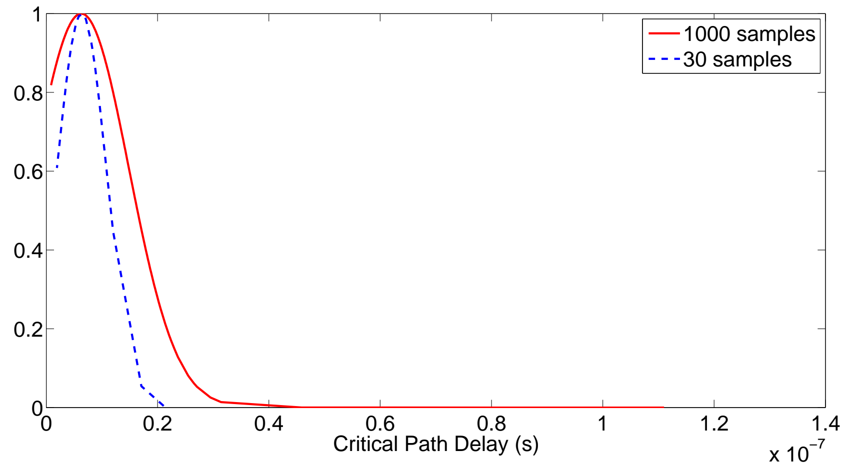


(b) Variation of t_{ox} by 20%

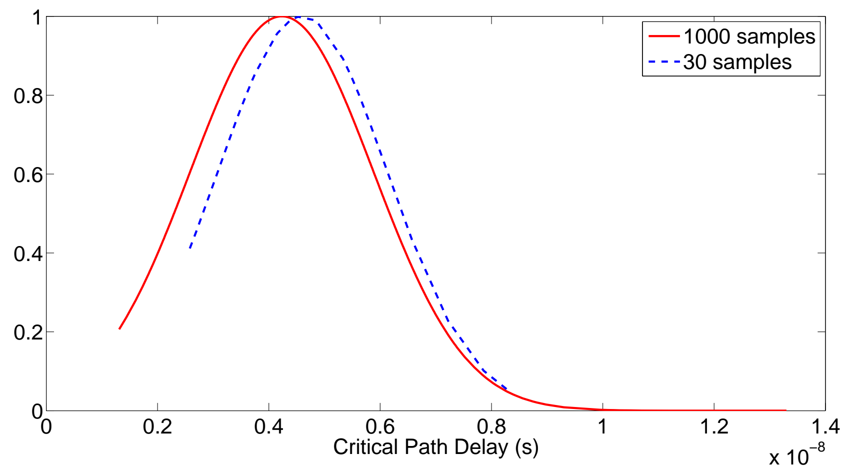


(c) Variation of both vth0 and t_{ox}

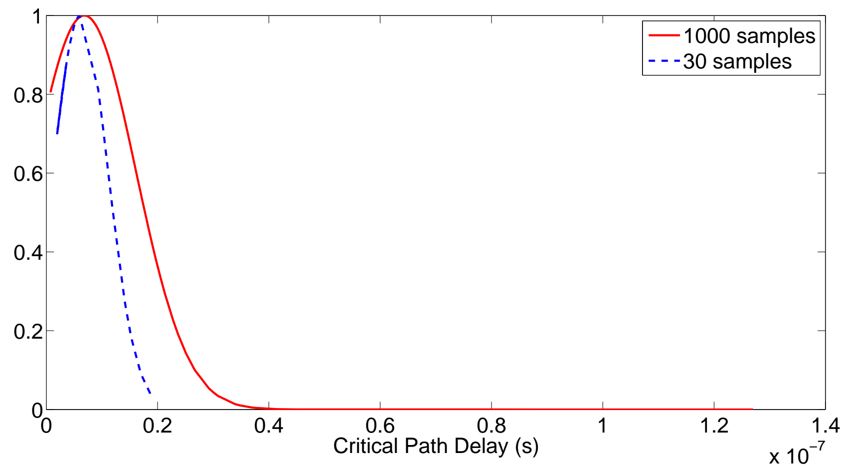
Figure 5.2: Effect of Process variation on critical path delay for adder operating at 0.9 V designed in 45nm high-k technology.



(a) Variation of vth0 by 16%

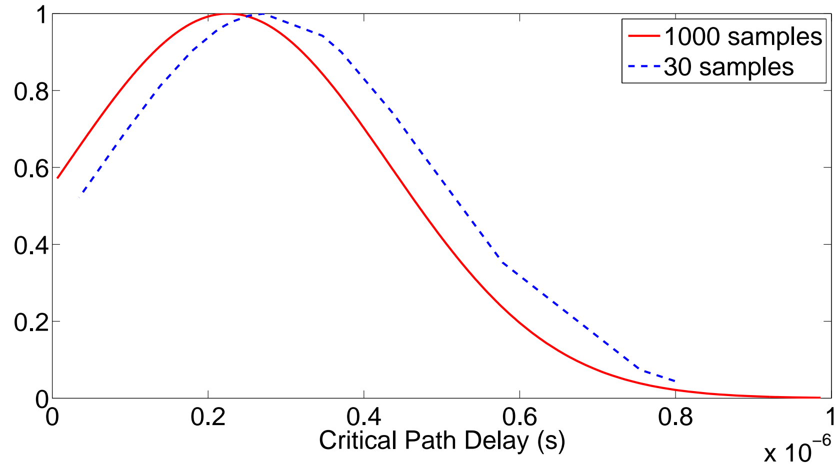


(b) Variation of t_{ox} by 20%

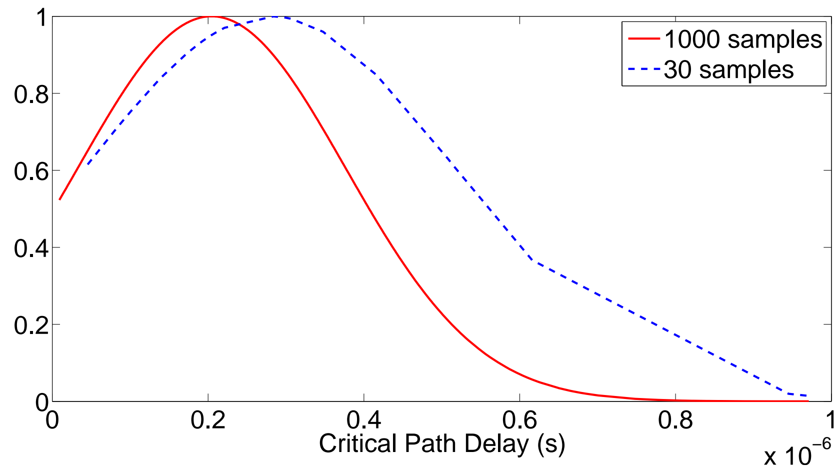


(c) Variation of both vth0 and t_{ox}

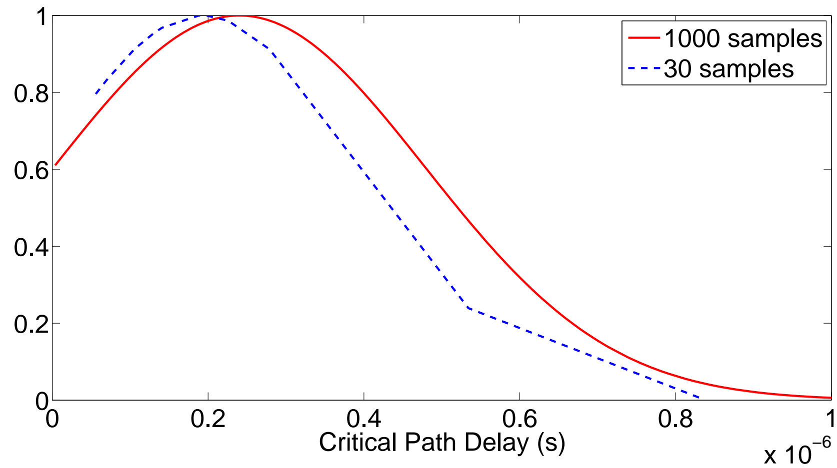
Figure 5.3: Effect of Process variation on critical path delay for adder operating at 0.3 V designed in 45nm high-k technology.



(a) Variation of vth0 by 16%



(b) Variation of t_{ox} by 20%



(c) Variation of both vth0 and t_{ox}

Figure 5.4: Effect of Process variation on critical path delay for adder operating at 0.3 V designed in 45nm bulk technology.

Table 5.5: Yield of circuit designed in 45nm bulk and high-k technologies when affected by process variations.

Operating Voltage (V)	Process Variations	Yield (%)
0.9 V high-k	vth0	100%
	t_{ox}	98.9%
	Both	99%
0.3 V high-k	vth0	99.6 %
	t_{ox}	98.9%
	Both	99.7%
0.3 V bulk	vth0	90.7%
	t_{ox}	97.5%
	Both	79.8%

Table 5.5 tells us how many samples out of 1000 function correctly after being affected by process variation, i.e yield of the circuit. It is seen that circuits designed in high-k technology are more resilient to process variations, has a very low failure rate. Bulk technology, on the other hand, is seen to have a lower yield, and when both parameters undergo process variation at the same time, the yield drops drastically to less than 80% unlike high-k, which still maintains an almost 100% yield. Hence, it could be hypothesized that as more parametric parameters undergo process variation, the yield will be affected as well.

The corresponding sum of mean and 3σ gives the worst case delay for a circuit operating at 0.3 V for each technology. This worst case delay was used as clock period to feed 100 random vectors to 30 random Monte Carlo samples of the 32 bit adder circuit and the current drawn from V_{dd} for each sample was measured. The average current of a circuit sample was multiplied by the current operating voltage to obtain the power, which when multiplied by the clock period gave us the energy/cycle for each random sample.

Table 5.6 compares the average values of energy/cycle and the clock period with and without process variations for various technologies and operating voltages. Although the clock period almost doubles due to process variations for subthreshold

Table 5.6: Comparison of average energy/cycle and clock period with and without process variations for a 32-bit ripple carry adder.

Operating Voltage (V)	Process Variations	Clock Period $\times 10^{-9}$ (s)	Energy/cycle $\times 10^{-14}$ (J)
0.9 V high-k	No Variation	0.47	10.9
	vth0 (16%)	0.619	12.4
	t_{ox} (20%)	0.57	120
	Both	0.666	87
0.3 V high-k	No Variation	3.71	1.22
	vth0 (16%)	32	8.15
	t_{ox} (20%)	9.18	24
	Both	36.4	43.2
0.3 V bulk	No Variation	137	2.19
	vth0 (16%)	847.66	19.6
	t_{ox} (20%)	916.8	50.4
	Both	957.05	62.7

voltages, it is clearly seen that the circuit's energy consumption is not that far from the nominal energy/cycle. Since we assumed all samples to have a clock period corresponding to the worst (3σ) delay, it is possible that some circuits may be able to run faster and, for those cases, their individual energy/cycle may come closer to the nominal values or even perform better than that. The graphs in Figures 5.5 - 5.7 highlight the variations in energy/cycle for the circuit operating at 0.3 V and 0.9 V designed in both bulk and high-k technologies. From the table and graphs, it is evident that a combinational circuit designed in high-k technology is more resilient to process variation, has a smaller critical path delay and a lower energy/cycle.

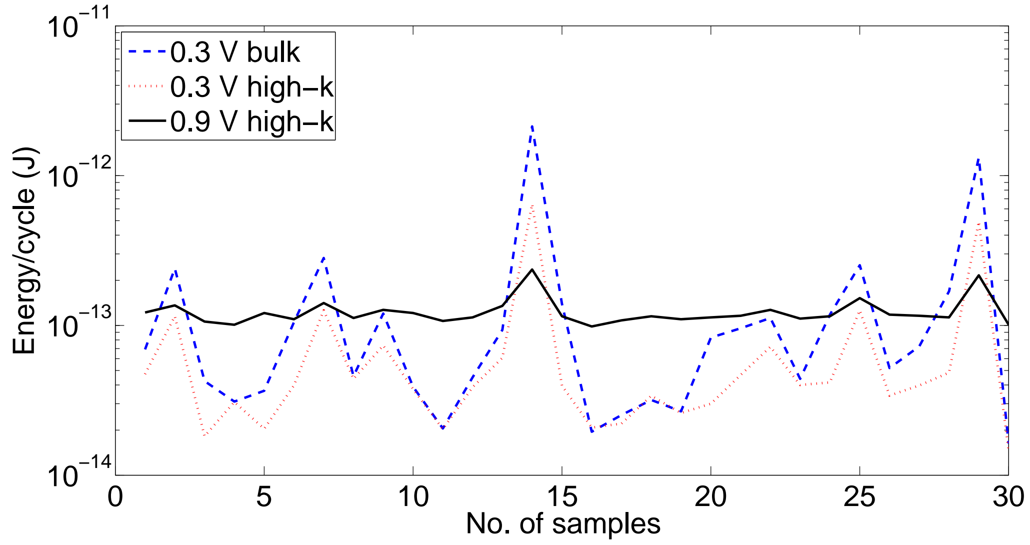


Figure 5.5: Comparison of energy/cycle for different adder circuit operations when threshold parameter (vth0) undergoes process variation.

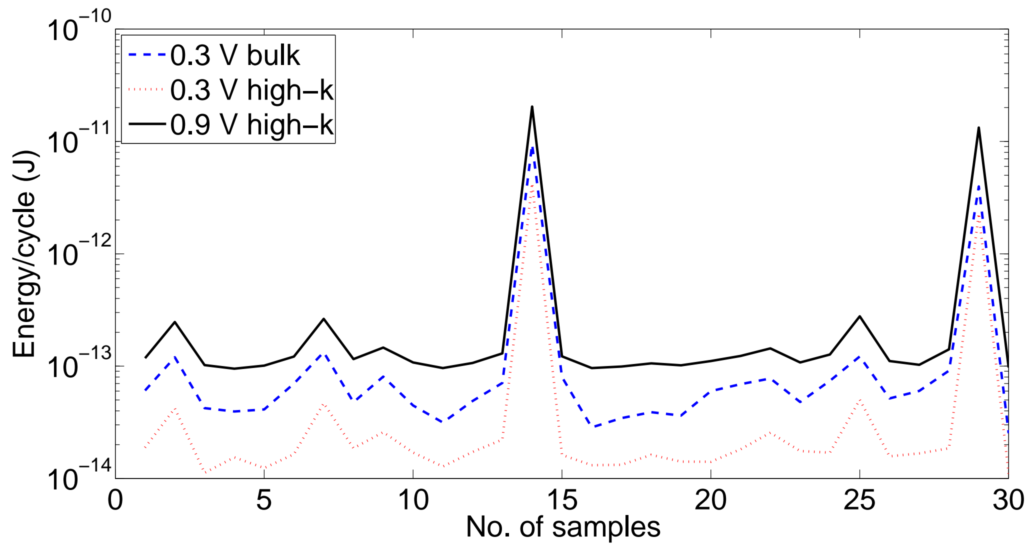


Figure 5.6: Comparison of energy/cycle for different adder circuit operations when oxide thickness (t_{ox}) undergoes process variation.

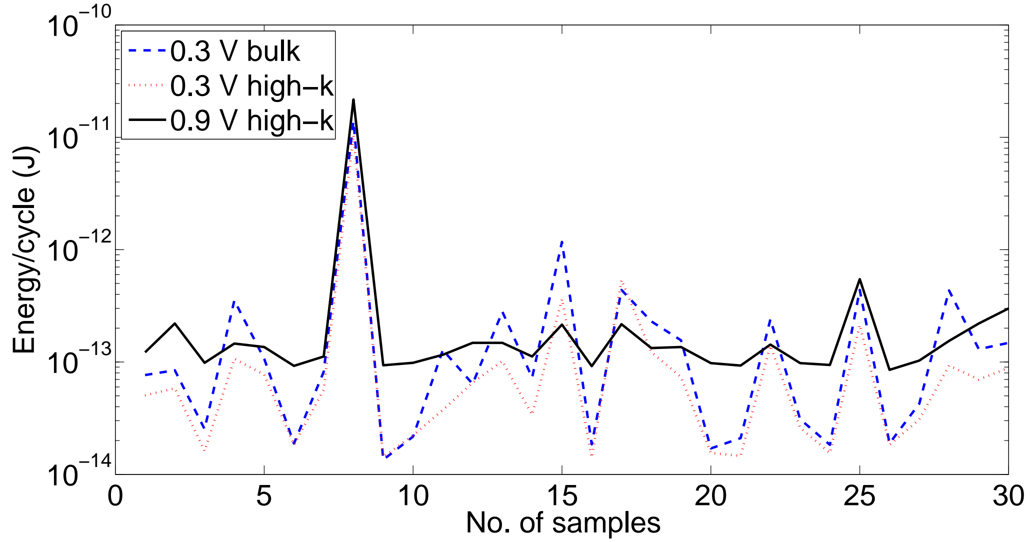


Figure 5.7: Comparison of energy/cycle for different adder circuit operations when both vth0 and t_{ox} undergo process variation.

A deviation in the process parameters causes a change in the drive current and critical path delay. This change usually causes the energy/cycle to increase as current and delay are not exactly inversely proportional to each other. However, there are rare instances (in high-k) where their relationship has caused the energy/cycle to decrease from the nominal value resulting in a circuit that runs faster. By analyzing the graphs in Figures 5.5 - 5.7, it is clearly seen that even with process variations, circuits operating at 0.3 V are considerably more energy efficient than circuits operating at 0.9 V.

Chapter 6

Conclusion

The results presented in this thesis are believed to be accurate and portray a picture of how a device will behave when fabricated in these technologies as the PTM models have shown a trend of closely following the actual fabrication trends. They have also shown better physical scalability over a wide range of process and design conditions [64].

Results indicate that the average power dissipated by the circuit decreases steadily with voltage scaling. This is true for both bulk and high-k designs. Simultaneously, it is also seen that the critical path delay increases or in other words, the speed of the circuit decreases. However, due to a greater drop in power compared to speed, the average energy per cycle of the circuit for both designs also decreases steadily. It is seen that the circuit has a minimum energy at an operating point of 0.3 V below which, the circuit started to dissipate more energy compared to higher voltages. The reason for this was that the drop in power dissipated was not enough to compensate the increase in delay of the circuit leading it to take more energy per cycle to run successfully.

Similar work was done by Tran and Baas, and their results showed their fast adder circuit functioning properly at 0.37 V while consuming 34 fJ per cycle [58]. Their design was based on 45 nm bulk PTM model, and since our 45 nm bulk model design also got similar results, [58] validates our results and affirms the conclusions drawn in this thesis.

Results also show that high-k technology runs faster, and more energy efficiently when compared to bulk technology. Although, the minimum energy point occurs at

the same voltage for both bulk and high-k, the value of average energy per cycle is 40% lower for high-k when compared to bulk. Also, high-k design operated at 250 MHz while bulk design operated at just above 7 MHz showing that high-k designs are faster at sub-threshold voltages as well.

Figure 6.1 explains why high-k technology is better than bulk technology. High-k technology has a thicker gate oxide when compared to bulk leading to lower current leakage through the gate oxide via tunneling. Secondly, presence of a metal gate instead of a polysilicon gate allows a better flow of charge in the channel, leading to a larger drive current and hence causing circuits designed in high-k to run faster.

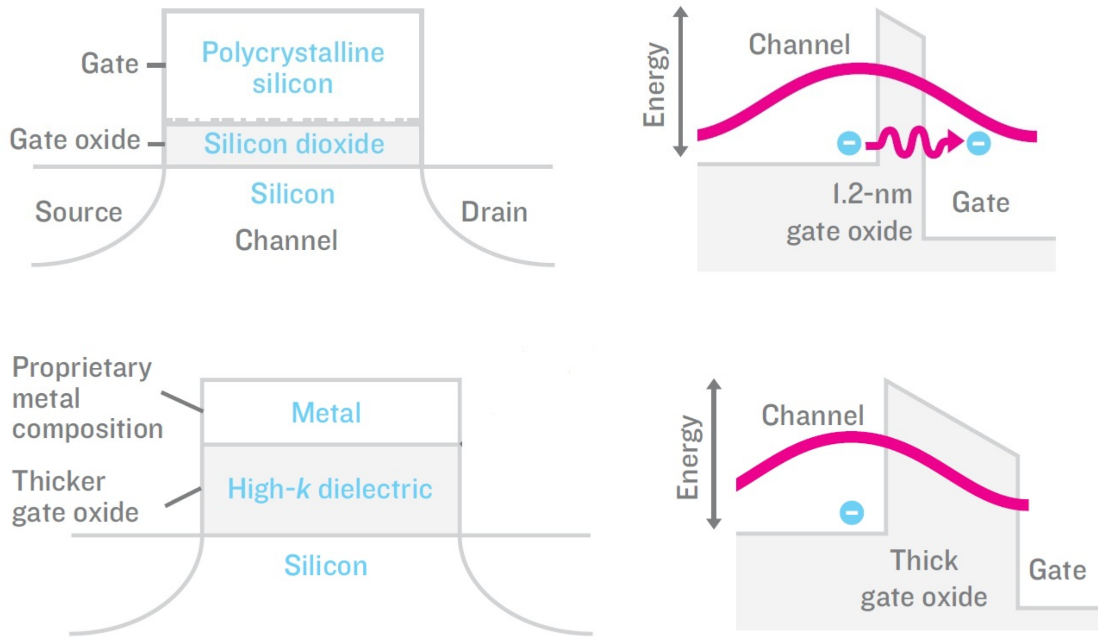


Figure 6.1: Comparison of gate oxide and gate design between a bulk MOSFET (top), and high-k MOSFET (bottom) [13].

Recent research has shown that process variation can greatly affect the functionality of logic gates [56]. It can also bring in uncertainties in the circuit logic. Shifts in the threshold voltage V_{th} can drastically affect the I_{on} and I_{off} in sub-threshold regions causing an exponential shift in the minimum energy point [41]. By analyzing the data from our results, we theorize that high-k technology designs at the minimum

energy point will be more resilient to process variations when compared to bulk technology because high-k technologies provide a higher drive current in the sub-threshold region along with a reduction in gate oxide leakage for the same drive current when compared to the bulk technology [13, 52].

It is seen that process variation has a large effect on the yield of the circuit designed in bulk technology compared to high-k technology. Changes in threshold parameter (vth0) and oxide thickness (t_{ox}) caused the yield of the circuit designed in 45nm bulk technology to drop to less than 80%. However, high-k designs showed more resilience and the yield was almost 100% for both normal operating voltages and sub-threshold voltages.

Parametric variations also have an effect on the speed and average energy dissipated of the circuit. On performing 1000 Monte Carlo simulations, and comparing its histogram with 30 samples, it is seen that the mean delays are very close to each other. Hence, the conclusions drawn from 30 samples would be the same as the ones drawn from analyzing a 1000 samples although, 1000 samples may provide more accurate figures and comparisons .

SPICE simulations have shown that even with process variations, circuits operating at 0.3 V (sub-threshold voltages) remain more energy efficient than at 0.9 V (normal operating voltages). Hence, it is more energy efficient to operate the circuits at sub-threshold voltages rather than at normal supply voltages. Also, it is seen that high-k designs are more resilient than bulk designs not only in terms of yield, but they are faster and more energy efficient compared to bulk designs.

Studies have shown that the voltage at which the minimum energy point occurs reduces with change in technology, reached a minimum at 90 nm and then starts increasing with every technology advance [14]. Although we expect the clock rate to further improve and energy per cycle to reduce for 32 nm and finer technologies, some projections by [14] indicate that energy per cycle could increase with a move

towards finer technologies. Hence, for lower technologies, the voltage at which the minimum energy point occurs should increase. However, as these studies have been done only for bulk technologies, it is hard to predict how high-k models will behave. Simulations need to be done to check how the minimum energy point moves from 45 nm high-k technology to finer high-k technologies.

Hence, future research could probably look into the movement of the minimum energy point when transistors designed in high-k technology are scaled down. It is still unknown how sequential circuits will behave when affected by parametric variations for finer high-k technologies. Research could be done to understand the effect of process variations on timing, energy dissipation and yield for sub-threshold operations of sequential circuits.

The ultimate minimum energy any circuit can achieve is bounded by the Landauer limit, which is given by $kTln2$, where k is the Bolzmann constant and T is the absolute temperature in Kelvin. Current studies have shown that the lower bound on the energy to process one bit is about 36,000 times higher than the absolute Landauer limit [28, 42]. A shift towards high-k technology is only a small step towards achieving energy values close to that limit. However, more research and supporting experiments need to be done to find the limits of high-k technology so that it can lead to actual implementations of digital systems like microprocessors, graphics processors, and digital signal processors.

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