Built-in Self-Test and Calibration of Mixed-signal Devices

by

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Abstract

Wide adoption of deep sub-micron and nanoscale technologies in the modern semiconductor industry is resulted in very large complex mixed-signal devices. It has then become more difficult to estimate and control device parameters, which are now increasingly vulnerable to fabrication process variations. Conventional design-for-test (DFT) methods have been already well studied for digital circuitry to ensure verification of its functionality and fault coverage. Built-in self-test (BIST) approaches have been developed for design automation of digital ICs. However, such DFT techniques cannot be applied to analog and mixed-signal circuits directly. Therefore, new techniques must be employed to detect faults in analog components and to provide certain level of calibration capability to dynamically adjust the parameters of an analog device for better yield of chips. The most important analog devices in a mixed-signal system-on-chip (SoC) are analog-to-digital converter (ADC) and digital-to-analog converter (DAC). Such converters transfer data between digital and analog circuits and convert analog signals to digital bits or vice versa. In this research, novel digital signal processor (DSP)-based post-fabrication process-independent BIST approaches and variation tolerant design technique for ADC and DAC are studied. We use a sigma-delta modulation technique for measurement and a polynomial fitting algorithm for device calibration. In the proposed technique, a digital signal processor is programmed and used as test pattern generator (TPG), output response analyzer (ORA) and test control unit. The polynomial fitting algorithm characterizes the nonlinearity errors and the polynomial is used to generate compensating signals to reduce nonlinearity errors to ± 0.5LSB. This

technique can be applied to other digitally-controllable mixed-signal devices and a general test-characterization-calibration approach modeled after this work can be developed to detect, measure, and compensate nonlinearity errors caused by device parameter deviations.

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Table of Contents

List of Figures

List of Tables

Chapter 1

Introduction

Digital test technology has been developing for nearly 40 years and has evolved into hardware and software based testing techniques. In early years, a test bench had to be designed and constructed for each circuit. Later, automatic test equipment (ATE) provided a general test solution for all digital devices. During the ATE period, the complexity and density of digital circuits increased dramatically while at the same time better quality and reliability were required by the market and consumers. Many VLSI test issues are especially challenging in high-performance and high-reliability designs. This trend is making the validation of VLSI circuits more and more difficult. Both external ATE machines, which are used in the IC production stage, and embedded test solutions, which are required for chip diagnosis and test are necessary in the design of modern electronic systems. The need to adopt or establish automated testing standards has been recognized by most manufacturing companies as essential for higher yield and lower cost.

However, no such automatic process exists for mixed-signal circuits where the interface between digital and analog components, in most case, digital-to-analog and analog-to-digital converters (DAC and ADC), may be impossible to be directly accessed by the test circuit and equipment.

Often, test circuitry must be embedded to overcome the problem of testing and allow both digital and analog components in a system to be accessed and tested independently. Usually such kind of testing techniques involve the use of additional pins, chip area and

design time. With the increased complexity of mixed-signal circuits and reduced access to internal nodes and paths, proper and efficient testing of such devices is becoming a major bottleneck during design and testing phases. Additionally, the current tendency to integrate both analog and digital circuits onto a single die leads to new testing problems, generally the analog part the root cause of major testing problems. Mixed-signal components, at the interface between digital and analog parts of a single chip, play a critical role in the overall performance of the whole chip.

In this thesis, a novel DSP-based post-fabrication process variation tolerant design technique for mixed-signal devices is discussed and a general test-characterization-calibration approach is developed to compensate for parameter deviations in those devices.

1.1 Overview

In recent decades, rapid advances in IC industry have led design functionality and complexity to unprecedented level motivated by deep sub-micron technology and nanoscale technology (65nm and beyond).

As the chip feature size keeps shrinking, more components can be integrated onto a single device. While the performance of such a device has been improving, power consumption is reducing and manufacturing cost is dropping. Figure 1.1 demonstrates the rapid growth of IC sales for 20 years between 1982 and 2002.

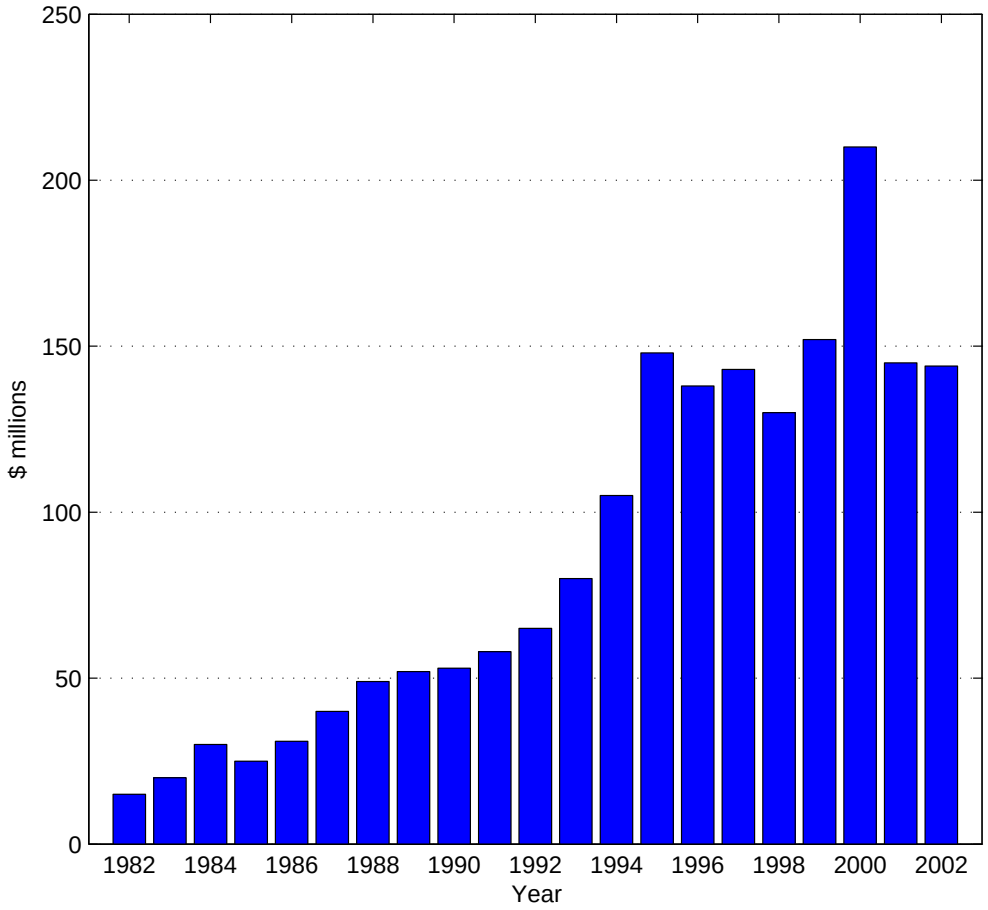

Figure 1.1: World semiconductor sales, 1982-2002 [1].

1.1.1 Digital Testing Techniques

Design-for-test (DFT) techniques have been used for digital ICs to achieve such objectives as test circuit insertion, test pattern generation, fault detection, and fault coverage analysis.

Purely digital circuits are usually tested using the stuck-at fault model, which considers all faults in a digital IC as either tied up to logic 1 or down to logic 0. All digital faults can be categorized into either stuck-at-0 or stuck-at-1 faults and can assume that every node can have either one of these two possible faults. For any given combinational circuit,

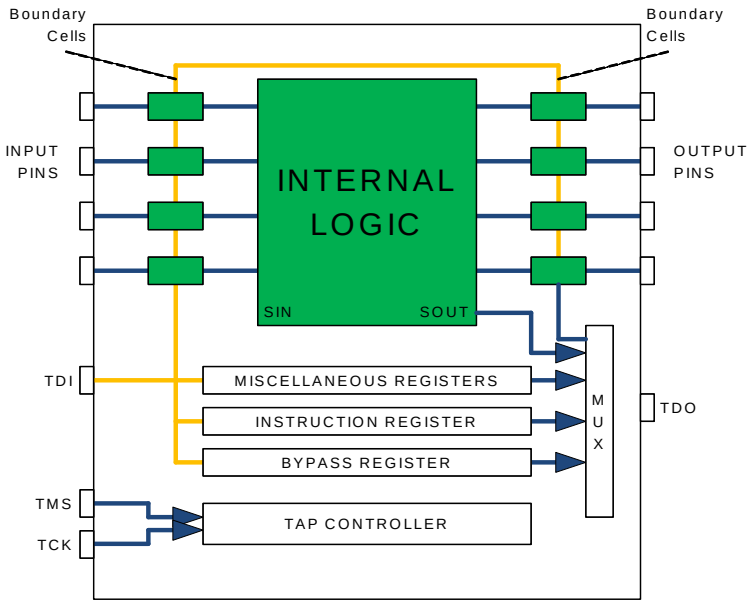

Figure 1.2: IEEE 1149.1 architecture.

a truth-table can be generated by simulation of all possible inputs. For a certain single-fault existing in the circuit-under-test (CUT), it is called a detectable fault if a different truth-table is generated by the simulation of all possible inputs. For a test sequence, the ratio of detectable faults to all possible faults of a digital circuit is called fault coverage. The input values that can detect at least one fault are considered test patterns. Thus, test patterns are generated to detect faults in a digital device and the testability of the given device can be measured by fault coverage. A path sensitization technique is used to find proper test patterns for any given detectable fault. Finally, fault collapsing techniques are used to remove many stuck-at faults and to reduce the total number of test patterns.

Over the years, three major methods have been widely adopted by integrated circuit (IC) industry to address the digital testing issues: boundary scan, scan chain and BIST.

Boundary scan is a method for testing wire interconnections between individual ICs of a circuit board as defined by the IEEE Std.1149.1 [6]. A basic IC architecture of IEEE 1149.1 is shown in Figure 1.2. Boundary scan can be used to isolate an IC chip from other

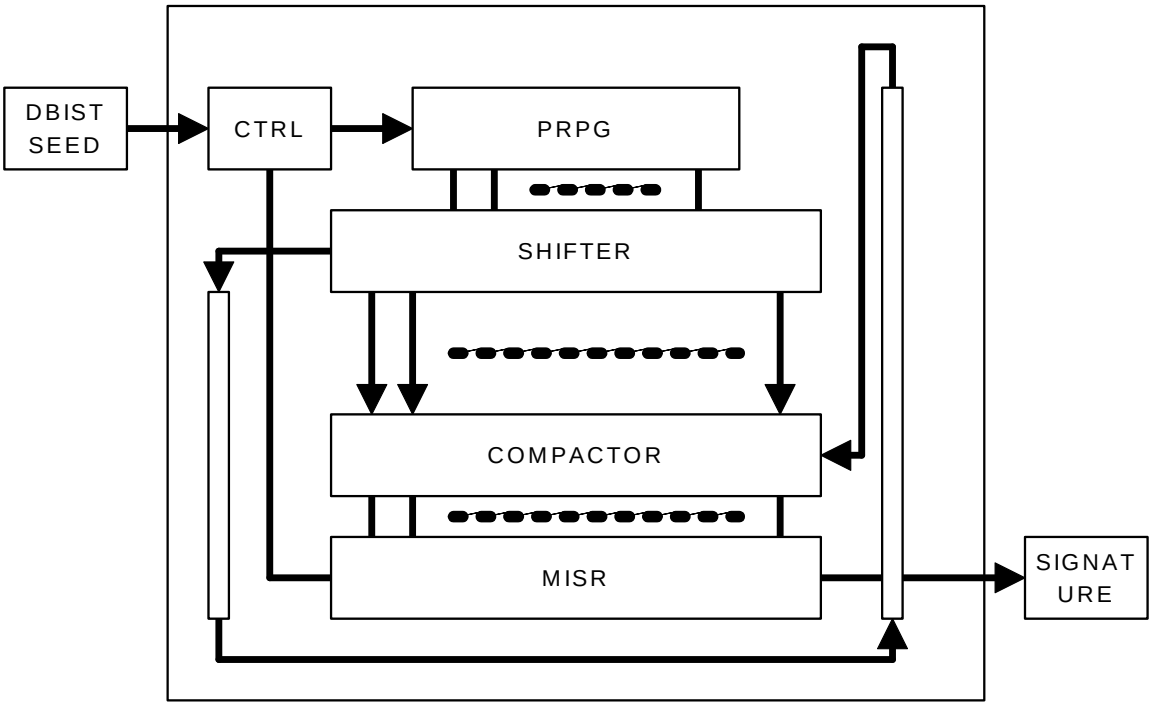

Figure 1.3: A typical boundary scan architecture.

chips on the board, supply desired test patterns as input and obtain output from the IC for analysis, as shown in Figure 1.3.

Scan chain is a method to set and observe every flip-flop inside a digital IC chip by replacing all regular D flip-flops (DFF) with scan DFFs and two additional input pins, test enable (TE) and test input (TI). All SDFFs are in a chain which is connected through TI pin and Q pin. When TE pin is enabled (shift mode), the scan chain can be accessed by standard JTAG I/O [7] pins to read and set all SDFFs. After all SDFFs are settled into a desired state, TE pin is disabled (capture mode) and output of combinational logic can be captured in SDFFs. Then TE pin is enabled again to shift out the Q pin of SDFFs bit by bit through the scan chain and at the same time a new pattern is shifted in to set all SDFFs to the next desired state. Scan chain makes it possible to assign an arbitrary internal state to a digital IC and thus may achieve higher test coverage with fewer test patterns.

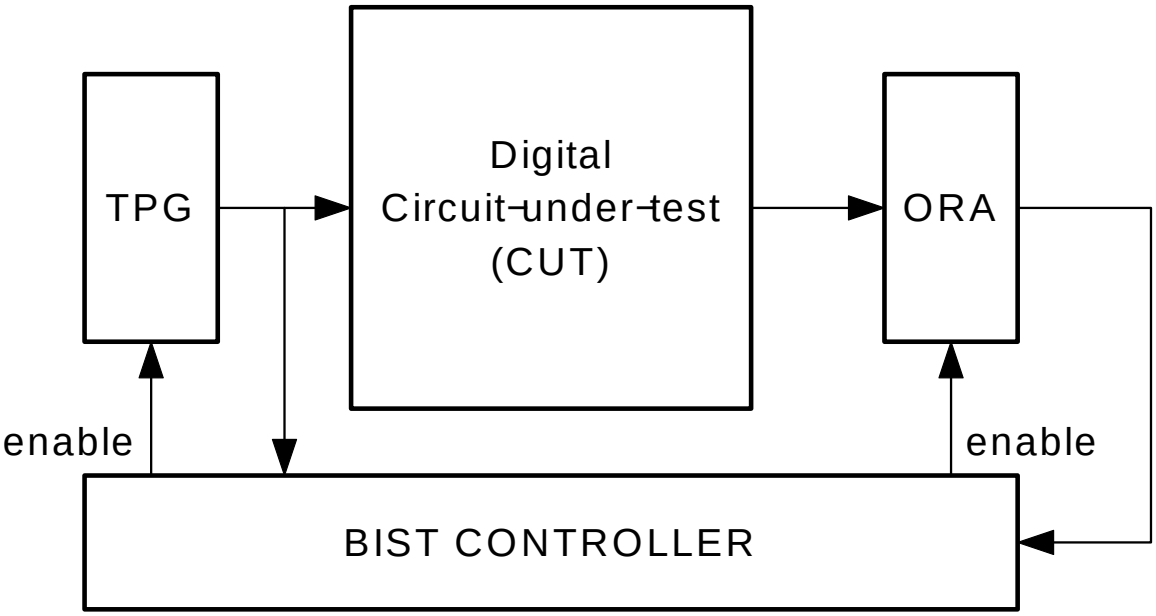

Figure 1.4: The basic BIST architecture.

Built-in self-test (BIST), as shown in Figure 1.4 is an advanced method for testing digital IC because this method requires no external equipment for test application and testing can be performed not only at the manufacturing stage but also at every power-up or even during normal operation. BIST techniques permit IC chips to test themselves by embedding both test pattern generator (TPG) and output response analyzer (ORA) inside the chip. At the cost of approximate by 20% – 30% overhead in the chip area and a small penalty in performance due to additional BIST hardware [8], the IC chip can now perform testing through internal scan chains without an external automatic testing equipment (ATE). In general, BIST techniques make testing of a digital IC chip easier, faster, more efficient and less costly.

1.1.2 Mixed-Signal Devices

A mixed-signal device integrates both digital and analog components and is capable of processing both digital and analog signals. Typical mixed-signal devices include

converters (digital-to-analog and analog-to-digital), amplifiers, transceivers, etc. With the development of new deep sub-micron CMOS technologies, such mixed-signal devices provide much more functionality than traditional digital or analog devices and hence, they are widely deployed in various applications. According to a recent report [9], global shipments of analog and mixed-signal ICs amounted to $31.7 billion in 2005, increased to $37 billion in 2006, and may hit $67.8 billion by 2011. The increasing demand for mixed-signal integrated circuits implementing both digital and analog functions on a single semiconductor die is pushing for increasing higher levels of integration as the fabrication technology advances.

However, scaling down of the chip feature size and integration of nanoscale digital and analog components brings new problems in manufacturing and testing of such mixed-signal devices. With scaling down of the feature size, device parameter deviations become a critical factor affecting fault occurrence, die yield, reliability, performance, and eventually the manufacturing cost. More severe the device parameter deviations become, lower is die yield and higher the final. The deep sub-micron process makes it possible to build complicated and highly integrated mixed-signal System-on-Chip (SoC) with both digital and analog components, but also leads to difficulties in the test of such components resulting in prolonged test time and rising test costs. While the area of analog/mixed-signal devices is important for designers and developers, testing of such devices is becoming a dominant factor of test costs associated with SoC validation [10]. As downscaling in CMOS technologies continues to 22nm, one of the difficult challenges in the near-term will be to deal with fluctuations and statistical process variation affecting the sub-11nm gate length MOSFET [11]. When the feature size of the mixed-signal devices approaches the physical limits,

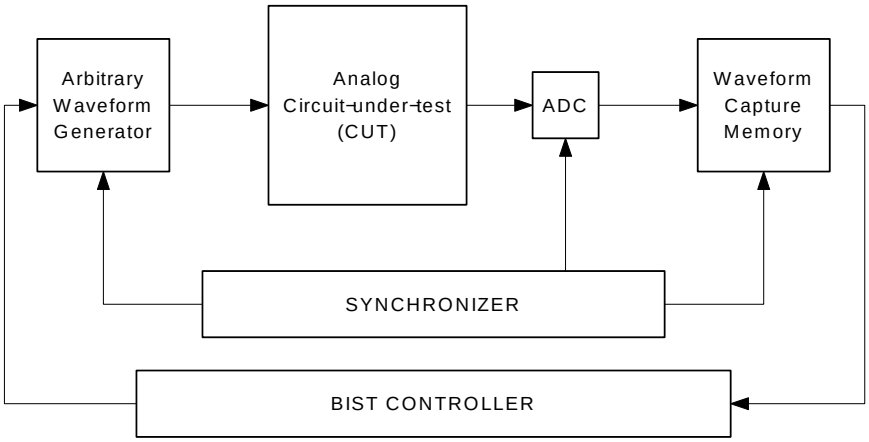

Figure 1.5: A basic analog tester scheme.

the device parameters will become more difficult to estimate and control. These difficulties may limit further feature size reduction, performance improvement and cost reduction.

Standards have been proposed for mixed-signal system-on-chip (SoC) test, e.g., IEEE 1149.4 [12]. These standards solve the testability problem of mixed-signal devices and improve the controllability of analog circuits. However, the area overhead and test time for using such standards are too high to deploy them for many mixed-signal devices. The hardware overhead of design for testability (DFT) is especially high for analog devices. Such standards need long test time and limit the analog test signal bandwidth as well.

Thus, particular solutions for fast and reliable test are still necessary for mixed-signal devices and components. Many of such proposals are based on digital signal processors (DSP), which is often available on a typical mixed-signal SoC for measurements on analog signals from ADC, processing base-band digital data, and generating analog signals using DAC. The same DSP can also be employed as test controller for BIST of mixed-signal SoCs [13, 14]. A basic analog tester is shown in Figure 1.5 [14]. It includes a digital controller, a waveform generator, a waveform capture memory, a synchronizer between generator and capturer, and an ADC to measure analog CUT outputs [15].

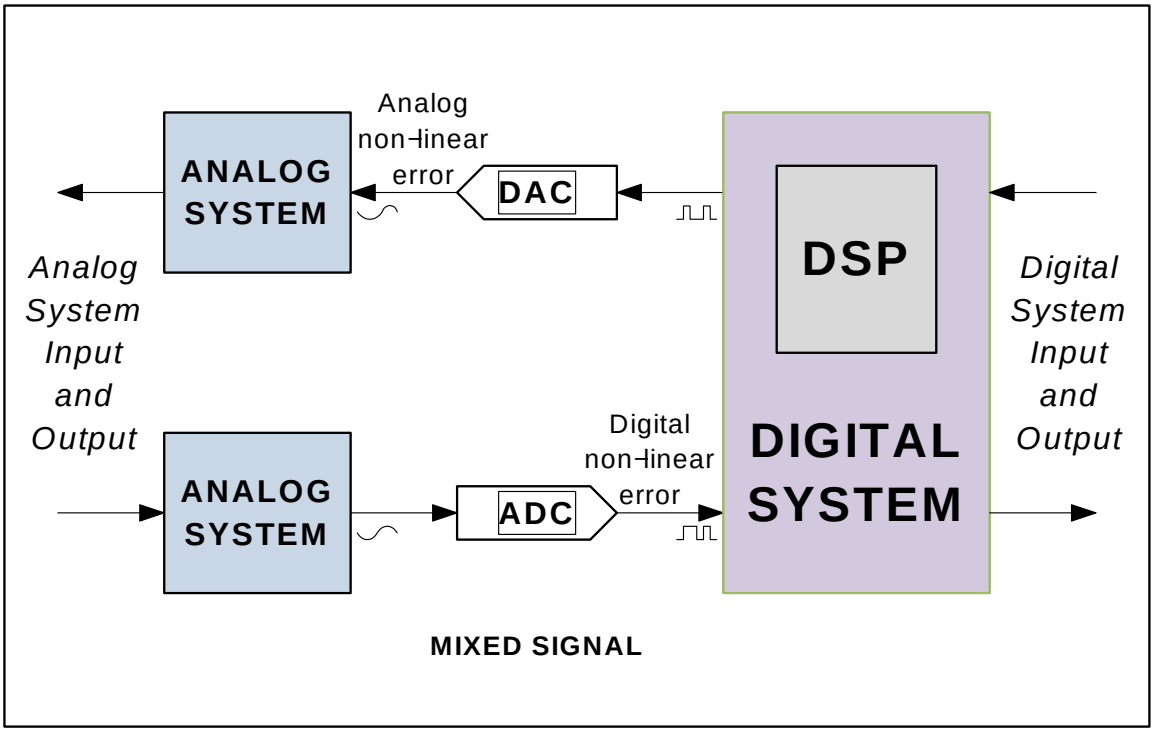

Figure 1.6: A typical architecture of mixed-signal system-on-chip (SoC), consisting of digital circuitry, ADC/DAC, and analog circuitry.

In this thesis, mixed-signal components, particularly ADC/DAC, are considered and special DFT techniques to characterize and calibrate such components are studied.

1.1.3 ADC and DAC

Many modern mixed-signal integrated circuit (IC) systems include built-in digital-to-analog converters (DAC) or analog-to-digital converters (ADC). They are two major components of any mixed-signal SoC and their typical test procedure is shown in Figure 1.6. Because the whole system relies on ADC and DAC to transfer signals between analog waveforms and digital bit-streams, the overall performance of the mixed-signal SoC depends upon the characteristics of those converters.

The test of high-speed and high-resolution ADC/DAC is a challenging and costly issue for designers and engineers. It has a large impact on fabrication and manufacturing

costs. Linearity and resolution are critical measurements for DACs and ADCs of a mixed-signal system-on-chip (SoC). They determine overall performance of the device. With increasing requirements for high resolution DAC/ADC set by high speed DSP processors and digital circuitry it becomes more challenging to test the on-chip converters, especially for system-on-chips (SoC). It also becomes more expensive and difficult to test the high performance converters using external automated testing equipment (ATE). The digital implementation of analog functions in such mixed-signal devices requires high resolution and better linearity for on-chip ADC and DAC, especially for communication transmitters and receivers [16].

1.1.4 Process Variation

The most important factor to affect parameter deviation of mixed-signal devices is fabrication process variations. Nanoscale technologies have given rise to new problems of increased parameter variation [11], higher leakage, and time-dependent degradation, all of which are active research areas.

For deep sub-micron technologies, a combination of physical feature of the process, dependency on die location, effects of optical proximity and etching and deposition may all lead to heterogeneous and non-monotonic relationship among the process parameters. The resulting process variation might be considered completely random effect without detailed understanding of individual contributions of each factor.

According to Boning and Chung [2], process variation appears at a number of different scales, as shown in Figure 1.7 [17]. Parametric faults, or soft faults, means that device parameters exceed beyond specified tolerance limits and mixed-signal devices are more

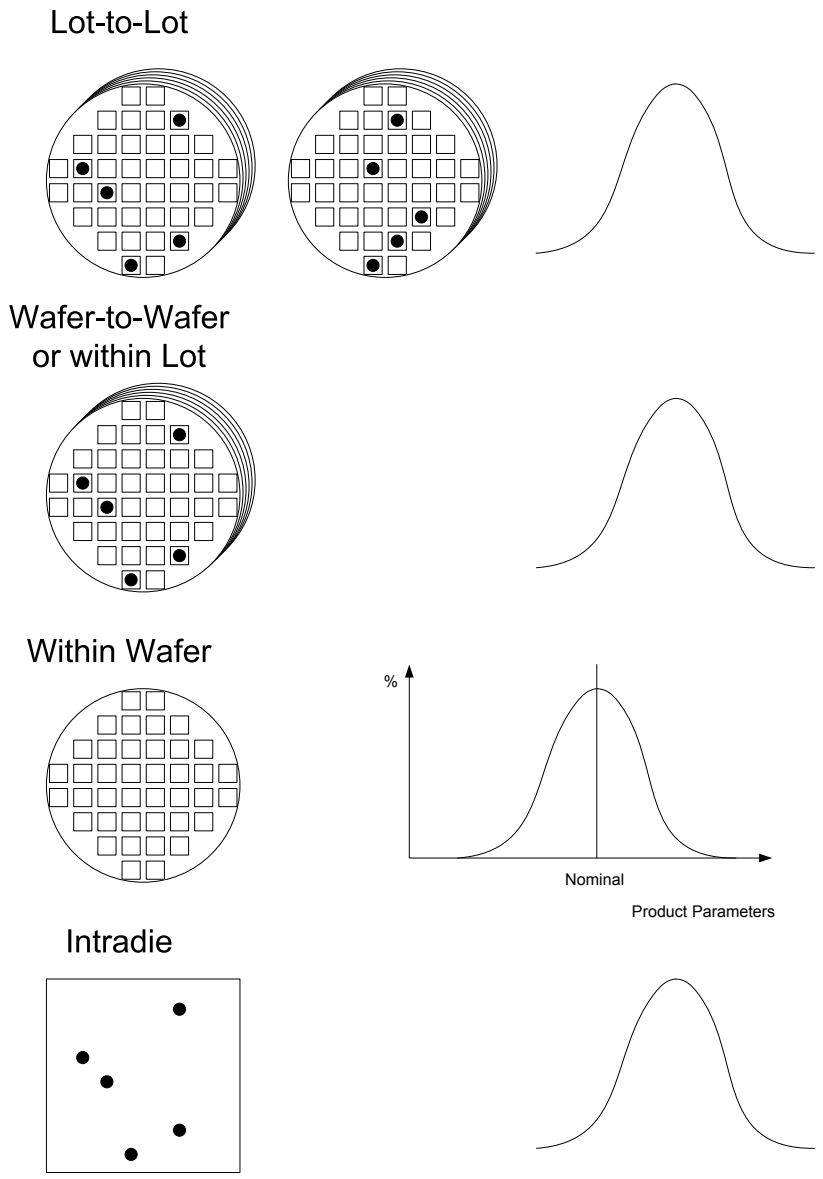

Figure 1.7: Different scales of process variation [2].

susceptible to such parametric faults than digital circuitry. So far there is few convincing fault models to describe the parametric faults and they are difficult to be identified until devices are characterized and device parameters are extracted. Known range of acceptable parameter values must be specified so that fault-free device s can be determined. Process

variations may seriously degrade overall mixed-signal system performance when parametric faults exist. Thus unlike catastrophic faults (hard faults) that need defect-oriented structural test approach, a specification-oriented functional test shall be employed for test of parametric faults.

In nanoscale devices, parameters may change (degrade) with time and with operating conditions. One such phenomenon that has received attention is the *negative bias temperature instability* (NBTI) [18]. The parameter changes will require that any calibration and compensation procedure should be able to adopt. In this research, we propose a polynomial error fitting type of nonlinearity compensation where the degree of the polynomial is self-adaptable. Thus, the system can recalibrate the the compensation parameters either the idle times or the restart of the system.

However, such integration also brings unprecedented challenges to present testing techniques, especially under nanoscale process. Scaling down feature size to nanoscale increases difficulties in manufacturing and testing of mixed-signal devices, and furthermore process variation of nanoscale device parameters during fabrication and packaging becomes a even more critical factors to faults, die yield and eventually unit cost of SoC. As downscaling in CMOS technologies continues, 22nm is a near-term challenge. Parameter fluctuations and statistical process variation in sub-11nm gate-length will also continue as one of the long-term challenges [11].

In a mixed-signal SoC, the challenges of nanoscale technologies [11] more difficult to deal with. Digital components may require built-in redundancy and reconfiguration, but analog and mixed-signal components may be correctable through measurement, calibration and correction schemes [19].

1.2 Motivation and Objectives

To deal with the issues in mixed-signal devices mentioned above, especially critical issues of ADC and DAC as they are the interface between digital and analog circuits inside the mixed-signal IC chip and therefore the most critical mixed-signal components in such IC chip, a novel on-chip DSP-based BIST approach for mixed-signal SoC is presented. The propose BIST approach is digitalized post-fabrication scheme with capability of self-test and self-calibration for mixed-signal components, in particular ADC and DAC converters.

Digital BIST techniques have been already widely studied and employed in decades and a systematic methodology has been developed for testing of digital circuitry. Therefore it is guaranteed for the digital circuitry used in ADC test to be fault-free and only ADC-under-test could be faulty. Discussion of design and implementation of BIST architecture for digital circuits and DSP is beyond the topic of this thesis, and in the rest of the thesis we can safely assume the all digital components and circuits for BIST of mixed-signal device are fault-free. If any fault is found in digital circuitry, the chip under test will be marked as faulty and BIST for mixed-signal device will not performed after all.

The principle of digital BIST for on-chip ADC and DAC is shown in Figure 1.8 [20]. For ADC testing, the transition voltage is generated by a counter. A signal circuit compares the ADC output with the previous one. The transition voltage can be used if the result of the comparison is positive and therefore this voltage is used instead of ideal transition voltage in the nonlinearity test.

The two general methods for testing mixed-signal devices are the servo and histogram. These techniques requires logical controlling unit, an independent input voltage and a complete analog test circuitry [21].

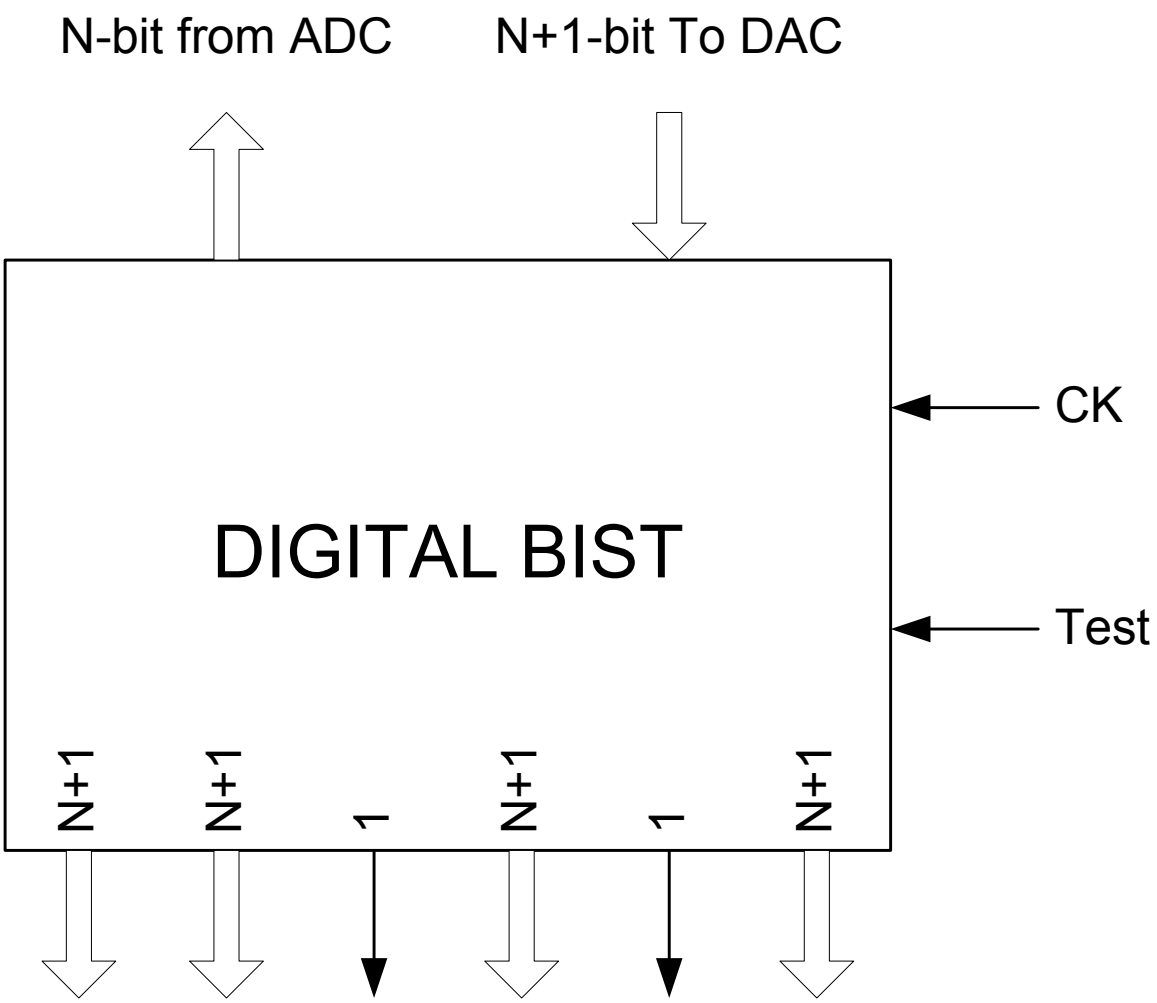

Figure 1.8: Digital BIST with inputs and outputs.

The other methods for on-chip generation of analog waveforms as test signals for ADC is to filter a periodically reproduced bit-stream previously encoded via a sigma-delta modulation by a low-pass filter (LPF) [22]. The principle of such analog test signals from digital test pattern generation filtered by low-pass filtering periodically bit-stream is shown in Figure 1.9.

In both servo-loop and histogram methods, the first step is the self-diagnosis of testing circuitry to make sure that testing results are correct before any BIST procedures and measurement performed on on-chip ADC and DAC. A self-diagnosis includes that self-test of analog waveform generator, waveform capture unit, and interconnections between these

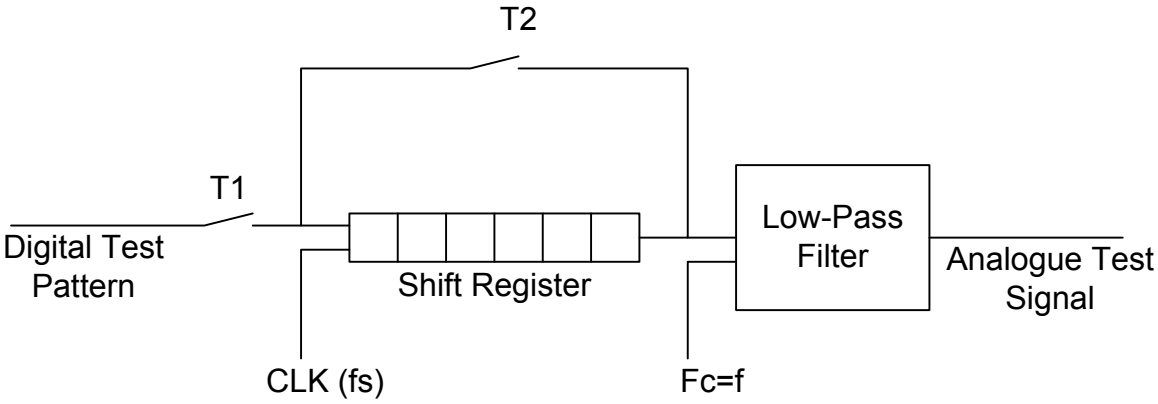

Figure 1.9: Techniques of analog test signal using periodical bit-stream and low-pass filter (LPF) [3].

testing circuitry to DSP which is responsible for measurements collection, data analysis and determining test results of the whole chip.

Generating test signals by filtering digital outputs, the proposed testing approach is able to extract both static and dynamic responses from ADC and to determine whether ADC is faulty. Should on-chip ADC pass test and prove to be fault-free, it can be used later in DAC testing to measure DAC outputs. Due to filtering digital outputs, the high frequency noise figure of the digitally generated test stimuli are much higher than analog test signals generated by on-chip DAC in conventional BIST approaches. A low-pass filter must be used to remove as much as noise from test signals and measured ADC outputs must be processed to reduce the negative effects of those digital noises. This approach is best suited for high-linearity ADCs, especially ADC based on sigma-delta modulation technique, for which noises in digital outputs can be filtered by higher order of sigma-delta modulator or greater oversampling ratio (OSR).

1.3 Contributions

Chapter 1 gives an overview of methods for testing mixed-sign devices, especially for ADC and DAC converters which are the most important mixed-signal components in such devices. ADC and DAC are the interface between digital and analog circuits and their characteristics determine the overall performance of a mixed-signal SoC.

Chapter 2 will give necessary background information on the details of the characteristics for ADC/DAC and other mixed-signal devices. The measurement and analysis of such converters are presented with different factors, including noise, SNR, gain, offset, harmonic distortion and nonlinearity errors. Among these characteristics, nonlinearity errors are the major issue for testing of ADC/DAC since nonlinearities of a give ADC or DAC are the direct results of the process variation and the greatly affected by different factors. Nonlinearity errors determine the accuracy of conversion from digital vectors to analog signals (DAC) or vice versa (ADC). Chapter 2 also shows the differences between static and dynamic test methods. These two methods require different testing methodology and different designs for TPG and ORA.

In Chapter 3, the details of the proposed testing architectures for mixed-signal devices are proposed. The major components of testing architectures are designed and analyzed, including measuring ADC, dithering DAC, and ramp/sinusoid testing signal generator. Measuring ADC is used for output measurement of on-chip DAC, which generate analog signals from digital patterns given by DSP. Usually the digital patterns are ramp vectors for static test of DAC to obtain nonlinearity and other characteristic. Ramp signal generator is used for analog testing signal generation to test on-chip ADC. Ramp signals can be linear,

triangle, or saw-tooth signals, all of which is suitable for static test of ADC. Sinusoid waveforms may also be used for dynamic test of ADC which requires low-frequency sine/cosine signals.

DSP plays the core role in the testing procedures because digital pattern generation, measurement analysis, device parameter extraction, device characterization and calibration are all programmed with the embedded DSP. DSP is also responsible for self-diagnosis of all testing circuitry since only digital circuits are guaranteed to be fault-free before any test of mixed-signal circuitry can be performed. DSP can also monitor the status of mixed-signal device during normal operation by performing characterization of ADC/DAC and other analog circuits when DSP is idle from other tasks. If drastic change of calculated parameters of ADC/ADC is detected by DSP, a new calibration procedure can be executed to re-calibrate the ADC/DAC to ensure the performance of mixed-signal device. This continuous detection and calibration can be programmed as a time-based routine that periodically executed to keep ADC/DAC calibrated.

In Chapter 4, Sigma-Delta modulation and measuring ADC are discussed. The benefit of Sigma-Delta modulation is the high-linearity and accuracy achieved by using oversampling and noise-shaping techniques. Oversampling technique distributes in-band quantization noise into a much wider frequency range and noise-shaping technique further moves in-band noise to higher-frequency. Combination of these two techniques pushes much of the quantization noise out-of-band into the higher frequency which can be easily removed through a low-pass filter. The resolution of Sigma-Delta ADC is determined by the oversampling ratio, the order of feedback loops and the number of effective bits of quantizer (usually a simple DAC), and the ADC in feedback loop. Although Sigma-Delta ADC is

considerably slower than any other type of ADC, the proposed mixed-signal BIST architecture will not take big impact since the Sigma-Delta ADC is only activated during BIST phase before any normal operation is executed. Thus the slow conversion rate of Sigma-Delta ADC will not slow down the normal operation of the mixed-signal devices.

Chapter 5 gives details of a polynomial fitting algorithm proposed by Sunter and Nagi [23]. An implementation of that algorithm was presented by Roy *et al.* [24]. Polynomial fitting algorithms are used for both characterization of on-chip ADC and DAC, and the coefficients of the polynomial determined by the algorithm are used for calibration of on-chip DAC. A low-resolution dithering DAC is driven by a polynomial computation unit to generate calibrating signals for each input digital code of on-chip DAC. Thus the final output of calibrated DAC is the combination of both outputs from on-chip DAC and dithering DAC which removes detected nonlinearity errors from on-chip DAC outputs. Various orders of polynomial fitting are discussed, from linear, third-order or even higher order fitting algorithms. An adaptive determination of a proper order of the polynomial fitting is proposed for various applications and situations. A lower order fitting algorithm is simpler to design and implement with less overhead in terms of the chip size. A higher order fitting algorithm gives better fitting for nonlinearities of DAC so that higher-linearity and more accuracy may be achieved at the cost of more overhead and performance penalty. In most cases, third-order polynomial fitting appears best for most applications for balancing the design complexity and calibration accuracy.

In Chapter 6, details of fault detection and calibration process are presented. A fault in a mixed-signal circuit is different from that of a digital circuit and therefore the stuck-at

fault model widely used in digital testing techniques cannot be used in testing of mixed-signal devices. Fault models for ADC/DAC and further generic mixed-signal circuits are presented. In fact, the faults in mixed-signal circuits are not the simple on-off types as in digital circuits. The faults in a mixed-signal circuit are determined by the allowable range of each parameter which is characterized during mixed-signal testing and measuring phases. If any parameter exceeds its allowable range (either high-side watermark or low-side one), the mixed-signal circuits will be considered faulty. A mixed-signal circuit is fault-free only if all obtained parameters are within their respective ranges. Therefore, calibration of a given mixed-signal circuit, particularly ADC/DAC, uses additional hardware to alter output signals of the ADC/DAC to make all obtained parameters within the allowable ranges.

Portions of the work reported in this dissertation have appeared in three recent papers [25, 26, 27].

Chapter 2

Background

Many analog testing methods tend to be specification-oriented as opposed to defect-oriented approaches typically used for testing digital circuitry. A defect-oriented approach applies the fault model to circuits to find out all possible faults existing in the circuit-under-test (CUT). One of such widely employed approaches is the stuck-at fault model, which assume that every net interconnection could be faulty as if stuck at either 1 or 0. A specification-oriented approach consists of a set of specifications that define the valid boundary for each measurable characteristic of CUT. When a certain characteristic value exceeds the defined limited, it will be considered as a fault. This difference partially comes from the fact that analog circuitry processes analog signals with a given value range instead of deterministic 0 or 1 found in digital circuitry. The parameters of analog circuitry are also affected by component tolerances, environmental variations (e.g., temperature and supply voltage) and noise.

Testing the analog porting of mixed-signal integrated circuits and systems has been identified as one the major challenges for the future, and BIST has been identified as a potential solution to this testing challenge [10, 11].

2.1 Analysis and Test of ADC and DAC

This section gives details on test and measurement of various performance characteristics of ADC/DAC under test, including noise figure and signal-to-noise ratio (SNR).

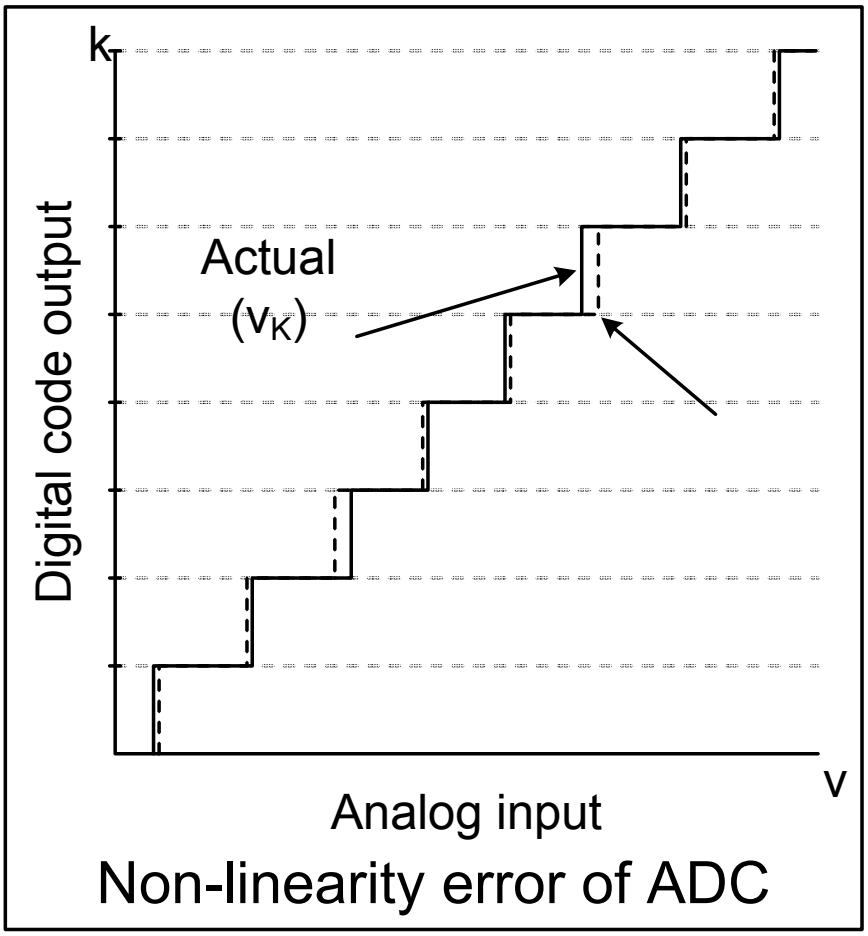

Figure 2.1: Non-linearity error in ADC.

2.1.1 Resolution and Non-Linearity Errors

The performance of an analog-to-digital converter (ADC) or a digital-to-analog converter (DAC) can be determined by static and dynamic responses. The static response specifies ADC's input-output function at low frequency input stimuli. Linearity tests typically measure static responses of ADC for determination of differential nonlinearity (DNL), integral nonlinearity (INL), gain and offset error. The most important characteristics of ADC and DAC are nonlinearity errors as shown in Figures 2.1 and 2.2.

Because differences between these two kinds of converters, the detail definitions of nonlinearity errors of the two converters are slightly different, although the principal ideas

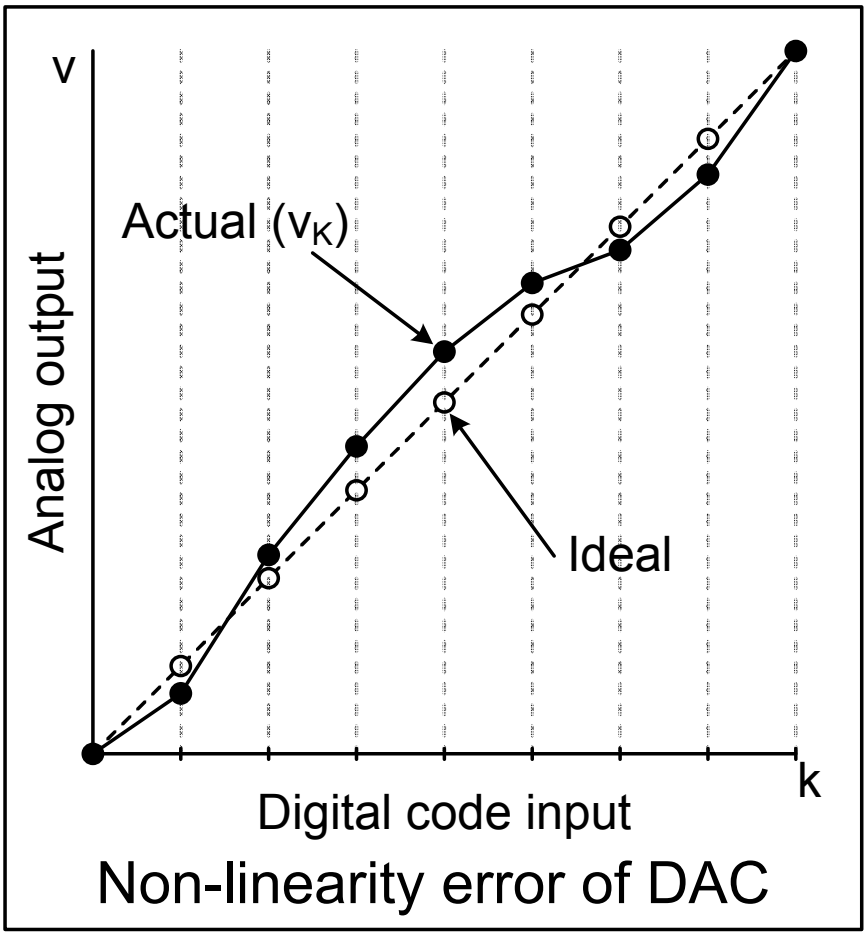

Figure 2.2: Non-linearity error in DAC.

behind them are similar. The nonlinearity errors of a particular ADC or DAC give the information about how different the ADC/DAC outputs are from those of ideal devices under perfect condition. More nonlinearity errors imply lower quality for ADC/DAC. The nonlinearity errors vary from chip to chip, die to die, even wafer to wafer, and may also change with the temperature of working environment. All these factors affect the characteristics of ADC/DAC and eventually the overall performance of the whole mixed-signal device.

Least significant bit (LSB) is the minimal voltage difference between consecutive codes of an ideal ADC or DAC. The LSB is defined as:

$$LSB = \frac{V}{2^N} \tag{2.1}$$

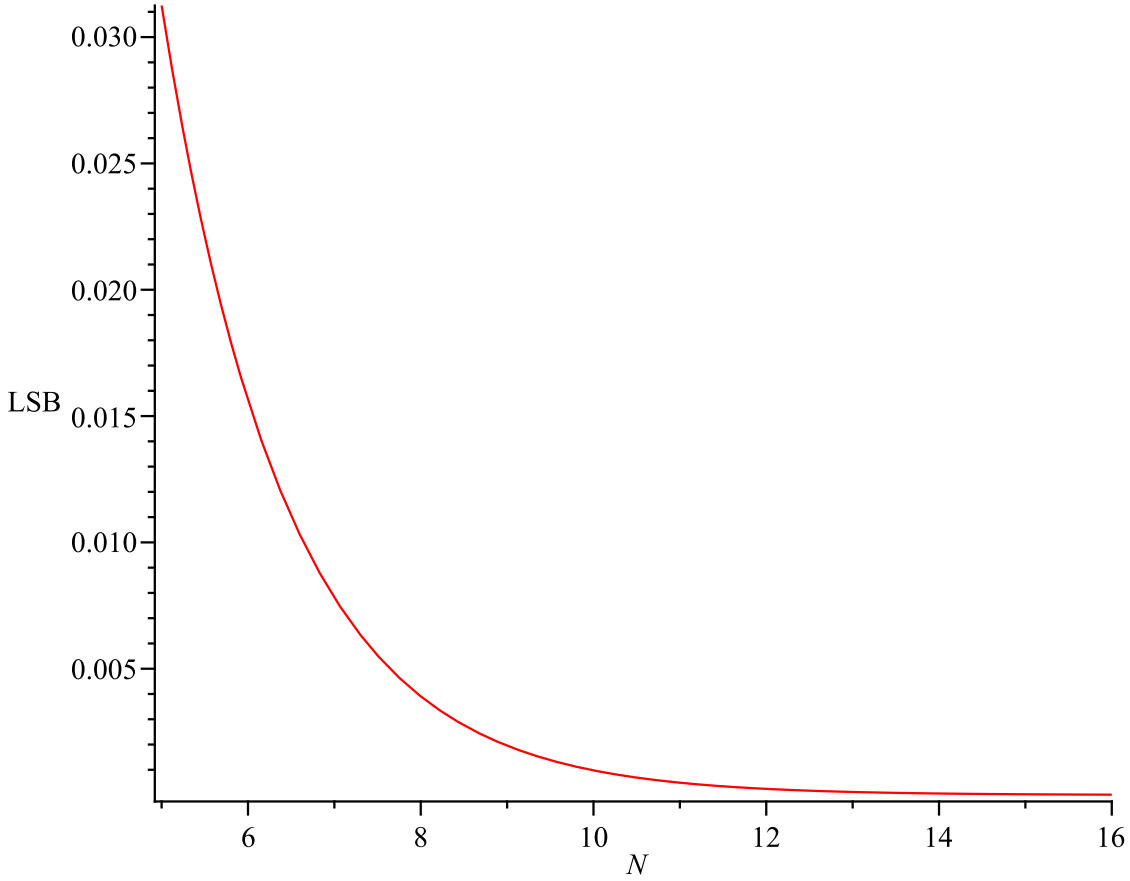

Figure 2.3: Resolution and the least significant bit (LSB) of converters.

where V is the full range of the converter with N-bit resolution.

For DAC, assuming input analog signal v_k corresponding to output digital code k, DNL and INL can be defined as,

$$DNL_k = \frac{v_k - v_{k-1}}{LSB} - 1 \tag{2.2}$$

$$INL_k = \sum_{i=0}^{k} DNL_i \tag{2.3}$$

$$= \frac{v_k - v_0}{LSB} - k \tag{2.4}$$

where LSB is the minimum measurement of the least significant bit of DAC. Therefore, each code corresponds to a particular analog signal level and nonlinearity errors can be calculated by comparing the measured levels with the expected ideal ones.

Unlike DAC, each code measured by an ADC has two transition edges corresponding to the lower and upper analog signal levels between which ADC outputs the code. Each transition edge represents change of consecutive ADC output codes. Let $\hat{V}_k$ and $\hat{V}_{k+1}$ be lower and upper transition edges of code k, respectively. Thus, $\hat{V}_k$ is the transition edge between code $k-1$ and k. An ideal ADC shall output code k for input analog signal level $v_k = k \cdot LSB$ and therefore the transition edges must be $0.5LSB$ away from v_k so that $\hat{V}_k = vk - 0.5LSB$, $\hat{V}_{k+1} = vk + 0.5LSB$, and

$$v_k = \frac{\hat{V}_k + \hat{V}_{k+1}}{2} \tag{2.5}$$

Equation (2.5) can also be applied to non-ideal ADC to calculate center signal level corresponding to each measured code because the transition edges are easy to detect and measure. Differential nonlinearity (DNL) and integral nonlinearity (INL) errors can be calculated, respectively, as:

$$\begin{aligned} DNL_k &= \frac{\hat{V}_{k+1} + \hat{V}_{k+2}}{2} - \frac{\hat{V}_k + \hat{V}_{k+1}}{2} - LSB \\ &= \frac{\hat{V}_{k+2} - \hat{V}_k}{2} - LSB \end{aligned} \tag{2.6}$$

$$\begin{aligned} INL_k &= \sum_{i=0}^{k-1} DNL_k \\ &= \frac{\hat{V}_k + \hat{V}_{k+1}}{2} - v_k \end{aligned} \tag{2.7}$$

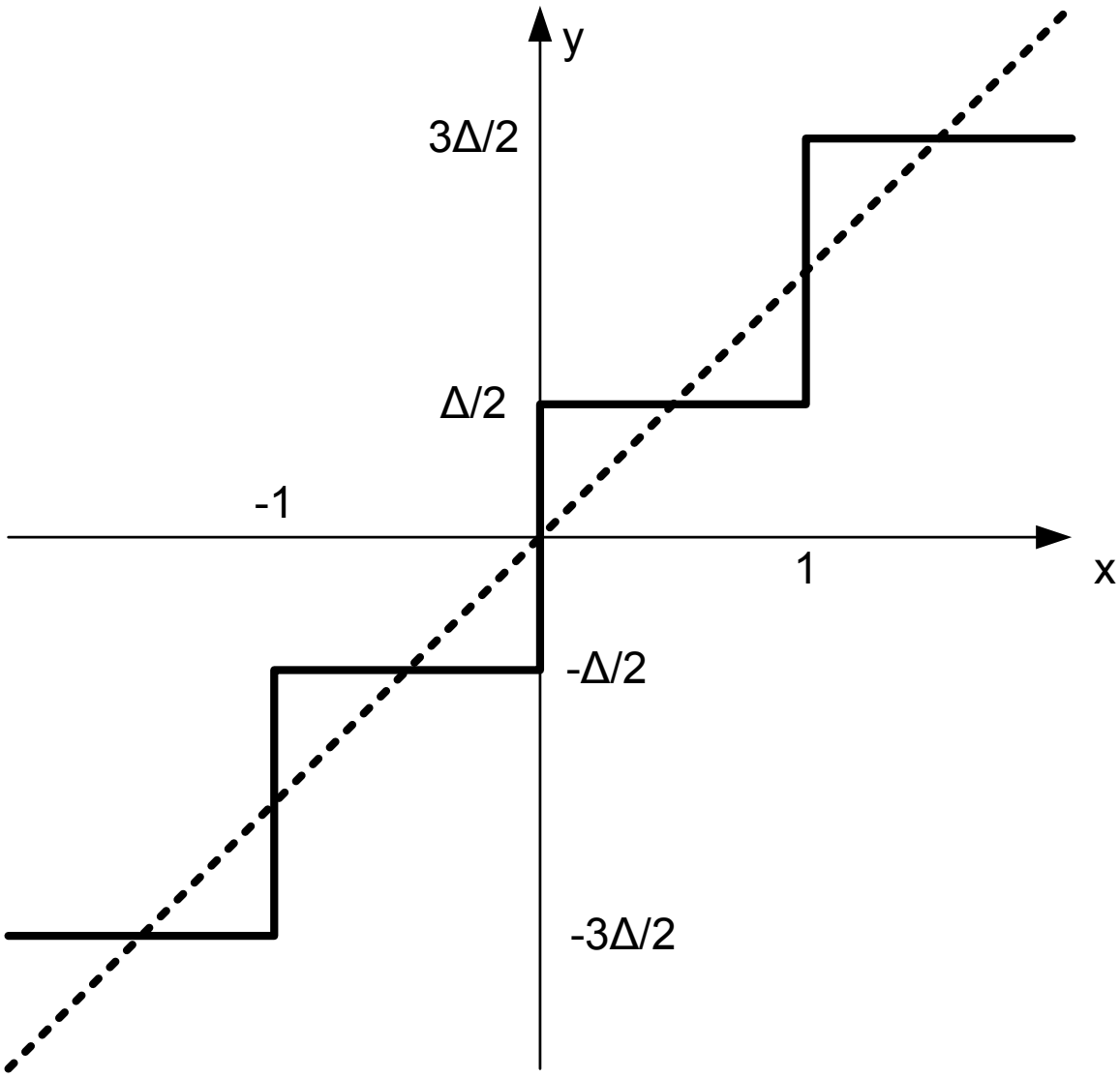

Figure 2.4: Transfer function of a quantizer.

ADC codes 0 and $2^N - 1$ are special as code 0 does not have the lower transition edge and code $2^N - 1$ does not have an upper edge, so the analog signal level corresponding to these two codes cannot be calculated by (2.5).

2.1.2 Noise

Quantization noise is a major source of nonlinearity errors in converters and needs to be carefully analyzed. A quantizer (either ADC or DAC) converts continuous analog signals to discrete digital codes, or vice versa. Since continuous analog signals may not match the exact values of the corresponding discrete digital codes. Unless the signal happens to be an integer multiple of LSB, or quantizer step value Δ, there will always be a quantization error in the output, as depicted in Figure 2.4. The error e is in range of one quantization level:

$$-\frac{\Delta}{2} \leq e \leq \frac{\Delta}{2} \tag{2.8}$$

Thus, the quantized signal y can be represented by a linear function as:

$$y = Gx + e \tag{2.9}$$

where gain G is the slope of the broken line in Figure 2.4.

The quantization error for a random signal, which is uniformly distributed in the band, can be considered as additive white noise and the error can be located anywhere in the range of one quantization level. Thus, it has the probability density:

$$p(e) = \begin{cases} \frac{1}{\Delta} & -\frac{\Delta}{2} \leq e \leq \frac{\Delta}{2} \\ 0 & otherwise \end{cases} \tag{2.10}$$

A normalization factor is required to guarantee that the sum of all probabilities equals 1. The mean square *rms* error voltage e_{ems} can be found by integrating square of error voltage:

$$\begin{aligned} e_{rms}^2 &= \int_{-\infty}^{+\infty} p(e)e^2\,de \\ &= \frac{1}{\Delta}\int_{-\frac{\Delta}{2}}^{+\frac{\Delta}{2}} e^2\,de \\ &= \frac{\Delta^2}{12} \end{aligned} \tag{2.11}$$

Therefore we can obtain the quantization error of an ADC/DAC given its LSB, the quantization step.

2.1.3 Signal-to-Noise Ratio

For an ADC/DAC the signal-to-noise ratio is the ratio of effective signal power to noise power. Assuming a sinusoidal signal applied to an N-bit ideal converter with white uniformly-distributed quantization noise and maximum peak-to-peak amplitude $(2^N-1)\cdot\Delta$, we can get noise power as shown in (2.11). The signal power is:

$$\begin{aligned} P_{signal} &= \int_0^1 \left(\frac{2^N-1}{2}\cdot\Delta\cdot\sin(2\pi\cdot x)\right)^2 dx \\ &= \frac{1}{8}\left(2^N-1\right)^2\cdot\Delta^2 \end{aligned} \tag{2.12}$$

Thus, SNR can be calculated as the quantization noise power that falls into the signal band:

$$\begin{aligned} SNR &= 10\log\left(\frac{P_{signal}}{P_{noise}}\right) \\ &= 10\log\left(\frac{P_{signal}}{e_{rms}^2}\right) \\ &= 10\log\left(\frac{\frac{1}{8}\left(2^N-1\right)^2\cdot\Delta^2}{\frac{\Delta^2}{12}}\right) \\ &= 10\log\left(\frac{3\cdot\left(2^N-1\right)^2}{2}\right) \\ &\approx 10\log\left(\frac{3\cdot 2^{2N}}{2}\right) \end{aligned} \tag{2.13}$$

Noting that $\log_{10}(x) = \log_{10} 2 \cdot \log_2 x$ and so the preceding expression leads to:

$$SNR \approx 6.02 \cdot N + 1.76 \tag{2.14}$$

We observe that SNR may be improved by 6 dB for every extra bit added to the quantizer. Given a known resolution for a certain converter, the maximum possible SNR can be calculated from (2.14). For example, a 10-bit converter has SNR of up to 61.96 dB. Figure 2.5 shows the relation between converter resolution and its SNR.

2.1.4 SNDR and ENOB

Dynamic characteristics can be measured using signal-to-noise-and-distortion ratio (SNDR, also called SINAD), total harmonic distortion (THD), effective number of bits (ENOB), dynamic range (DR), etc. A dynamic test strategy generally uses fast Fourier transform (FFT) analysis of ADC outputs corresponding to single-tone or multi-tone analog test input stimuli.

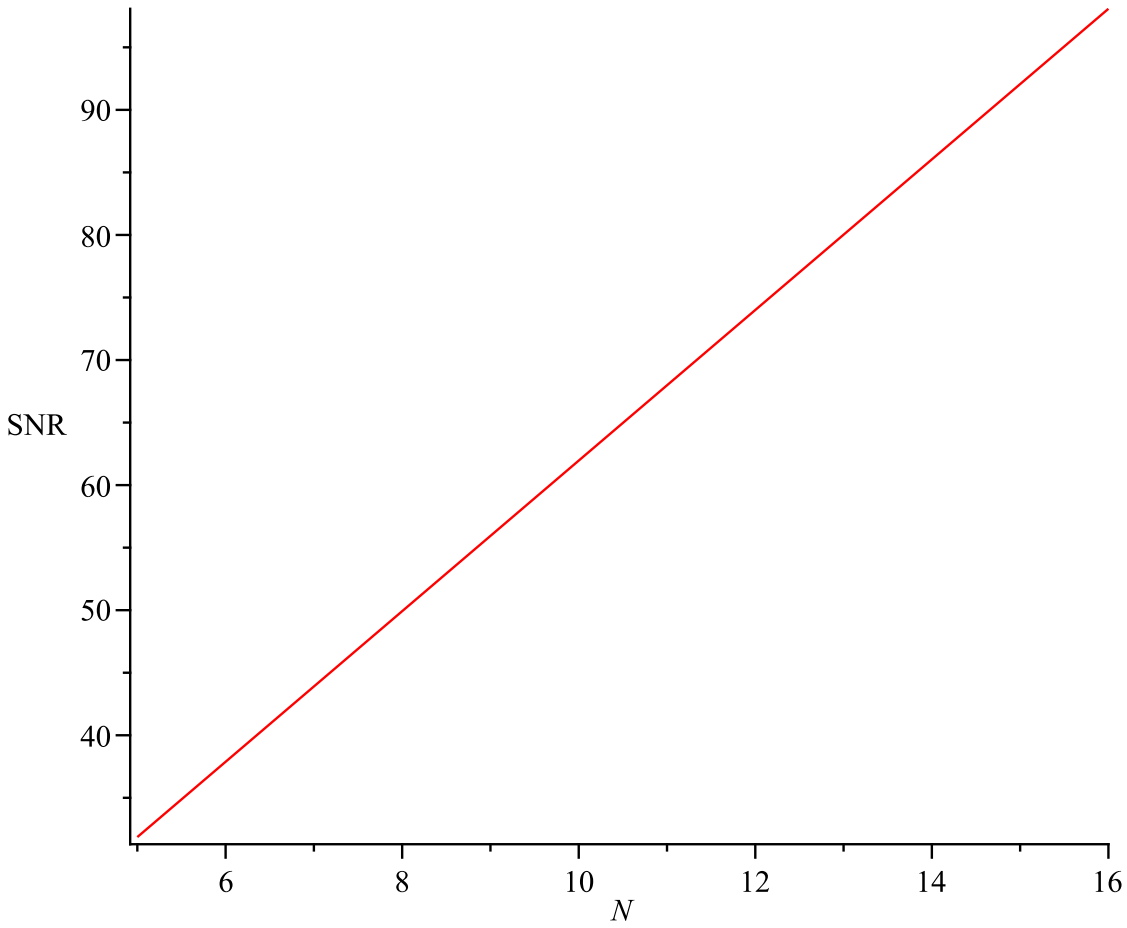

Figure 2.5: Resolution vs SNR of converters.

For ideal converters, SNR is determined by its resolution, i.e., number of bits. However, in reality harmonic distortion also affects the performance of converters, due to non-linearity errors found in output data. Signal-to-noise-and-distortion ratio (SNDR), the ratio of signal power to total power of quantization noise and harmonic distortions (THD), is defined as:

$$SNDR = \frac{P_{signal}}{P_{noise} + P_{distortion}} \tag{2.15}$$

SNDR considers not only the quantization noise but also harmonic distortions, so it can be used to determine the effective number of bits (ENOB) of a certain converter. Similar to SNR and resolution, ENOB and SNDR can be calculated from each other using the

following equation:

$$SNDR = 6.02 \cdot ENOB + 1.76 \tag{2.16}$$

2.2 Summary

In this chapter, some fundamental characteristics that measure the performance of ADC and DAC are discussed and the background for mixed-signal testing is given. Although mixed-signal IC and SoC usually consist of fewer components as compared to digital circuits, testing mixed-signal devices is more complex because here one adopts a specification-oriented approach instead of the defect-oriented approach used by digital testing techniques. Due to their complexity, most of the well-studied digital testing techniques cannot be directly applied to mixed-signal testing and their relevant characteristics must be understood to find ways to test the mixed-signal circuitry.

Chapter 3

BIST Architecture for Mixed-Signal Devices

In this chapter, a newly proposed fully digital ADC self-test approach is discussed and compared with the conventional ADC test methods. This complete digital test flow takes advantage of test signals from a digital signal processor (DSP), which can be programmed to generate various test patterns, e.g., maximum/minimum, ramp, triangle, single-tone sinusoid, or multi-tone sinusoidal codes. Different test patterns can be used for static or dynamic response analysis to measure the ADC performance.

3.1 Test of Mixed-Signal Devices

3.1.1 ADC/DAC Test Methods

To characterize high-resolution ADC/DAC, accurate stimuli must be generated to measure both static and dynamic performances. Most conventional test methods for on-chip ADC in mixed-signal SoC fall into two types. Some production test approaches employing analog or mixed-signal automatic test equipment (ATE), which generates high-precision analog test signals externally. While providing good quality test signals, such external test equipment is expensive, offers only off line application and usually requires a relatively long test time.

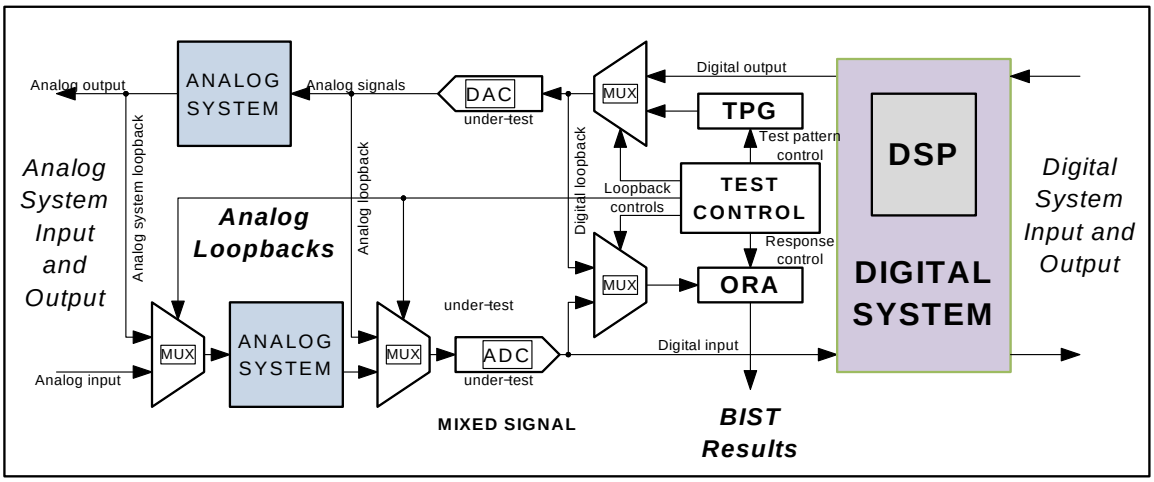

Figure 3.1: Typical servo-loop testing methods for ADC in a mixed-signal system with a local analog feedback loop [4].

3.1.2 Available Test Methods

There were many well-studied BIST approaches proposed for mixed-signal circuits. Some approaches introduce built-in self-test (BIST) techniques that use on-chip DAC to generate analog test signals [25]. A test pattern generator (TPG) and a output result analyzer (ORA) have to be integrated into the mixed-signal system as well as DAC/ADC to generate digital patterns, which will be later converted into analog waveform by DAC, and to measure and analyze ADC outputs through an analog feedback loop established only during test as shown in Figure 3.1 [4]. Presuming on-chip DAC and other mixed-signal components to be fault free, such internal approaches give shorter testing time and on-line characteristics for on-chip ADC with only a few performance penalties in terms of hardware overhead and conversion speed. However, it is difficult to make the above presumption in reality and the mixed-signal components used to test on-chip ADC must be tested in advance. Otherwise, the measurements of ADC outputs are distorted and become useless. These situation demonstrate a dilemma for built-in test approaches because testing

of either DAC or ADC requires the other part to be fault free as well as a working analog loopback connection [28].

In some situations, this on-chip DAC may need additional high-resolution ADC to test [29]. A recent paper [26] has proposed a self-calibration approach to make fixes to ADC and DAC outputs to achieve better linear outputs, requiring both on-chip ADC and DAC. Additional self-test of measuring ADC must be done prior to test and calibration of other on-chip components, otherwise the extracted parameters are not precise and compensating signals cannot be correctly generated. If a DAC is not present on the target mixed-signal SoC, noise could be used as test signal for BIST of ADC [30], requiring significant power consumption by digital circuitry. In another method [31], digital control logic is used to generate voltage oscillation for full-range ramp test of ADC without DAC. This method can be used for DNL, INL and gain error testing. However, the measured performances heavily rely on the linearity of the current source and capacitance which generate ramp signals.

3.1.3 Servo-Loop Testing Method

Conventional built-in ADC test approaches, as shown in Figure 3.1, require test circuitry including test pattern generator (TPG), output results analyzer (ORA), a built in (presumed fault-free) DAC and a local feedback loop link established between DAC and ADC during BIST. Such approaches are called servo-loop methods and usually perform a full-scale histogram test on ADC-under-test to measure linearity responses of the ADC. To properly test on-chip ADC, the DAC required by conventional ADC test methods must

be of same or higher resolution than that of the ADC. TPG can also be used to generate various forms of test signals for dynamic response tests.

A three-step testing procedure must be performed in order to complete servo-loop test on ADC-under-test.

- Perform BIST on digital circuitry at first
- Establish a digital link between TPG and ORA, and perform a digital test on TPG/ORA directly
- Establish an analog link between DAC and ADC, and perform an mixed-signal test on ADC

It is obvious that the servo-loop approach is complex and slow, requires an on-chip high-resolution DAC, and multiple loopback links have to be established/disconnected during different steps of test. The DAC is the most critical part in the approach because low-resolution DAC cannot satisfy the minimum requirements of ADC. DAC with lower resolution is easier to manufacture and control, and generally has lower cost, however, such low-resolution DAC is unable to cover full-scale of ADC-under-test and majority of the codes cannot be tested. On the other hand, high-resolution DAC may be sufficient to test ADC but it is more expensive to design and manufacture, and it is more difficult to control its linearity and noise figure.

The test performance relies on the design of a presumed fault-free DAC; otherwise it may result in incorrect measurements and wrong characteristics. For static response test, ideal digital test patterns generated by TPG will no longer be ideal after they are converted into analog signals by DAC. Any nonlinearity errors in either DAC or ADC will

be measured but considered only as nonlinearity errors of ADC. For dynamic response test, transfer function of DAC will distort ideal test patterns and inject additional noise into the single-tone or multiple-tone sinusoidal signals. Thus, the usage of a DAC should be removed from ADC test procedures to avoid such unexpected nonlinearity errors, noise and distortions caused by the DAC to correctly measure and characterize the ADC-under-test.

3.1.4 Sigma-Delta Testing Method

A sigma-delta modulation based BIST scheme has been presented for mixed-signal circuits [32]. Oversampling sigma-delta modulation was employed for both stimulus generation and response analysis to achieve high-quality stimuli and measurement without stringent hardware requirement. This approach also requires higher-resolution stimuli generator and multi-bit digital streams to measure the function (approximately, 6dB per bit). A software based multi-bit sigma-delta encoder is used to compensate for DAC imperfections. The approach depends on software to complete the BIST and provide compensation and its performance is a concern. The existence of multiple sigma-delta modulators in this approach is another concern, which may increase the design complexity and overhead of the BIST circuit.

Lee *et al.* [33] proposed a sigma-delta modulation based BIST scheme to concurrently generate analog sinusoidal test stimuli and digital sinusoidal reference signals. CUT is supplied the analog stimuli and then four key parameters of ADC, namely, *offset error, gain error, integral nonlinearity error* and *differential nonlinearity error,* are measured against digital reference based on sinusoidal histogram of ADC output. This approach can provide

high accuracy and low chip area overhead for 8-bit ADCs. But for testing higher-resolution ADC, it may be difficult to produce analog and digital signals simultaneously and sigma-delta modulator would require more clock cycles leading to a reduce overall performance. The histogram method used in the scheme also requires much larger overhead for additional memory space for storing data. Ong *et al.* [34] give a second-order delta-sigma modulator based mixed-signal BIST architecture capable of testing/characterizing itself using all digital stimulus. Test time of the architecture is shorter than the static linear ramp testing. However, it heavily depends on DSP processor for generating digital stimulus, filtering the results from delta-sigma modulator, performing fast Fourier transform (FFT) and characterizing the modulator.

There are other similar solutions using Sigma-Delta techniques [35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48].

3.1.5 Histogram Testing Method

Histogram methods are often used in BIST schemes for DAC/ADC. Wang *et al.* [49] present a low-cost BIST based on linear histogram for testing on-chip ADC with parallel time decomposition technique to minimize area overhead and test time. Several authors [29, 50] use dithering techniques to obtain precise analog signals for high quality stimuli generation. However, it is difficult to apply the histogram testing method to high-resolution ADC because of the large amount of samples to be collected and the long test time that leads to. The method also needs a very slow-slope ramp signal or low-frequency sinusoidal test signals. In BIST, these requirements either are impractical to design or cause high overhead.

Histogram testing method is widely used for determination of nonlinearity errors of ADC as an alternative of servo-loop method. The excitation signals for ADC under test can be either a low-slope ramp signal or a low-frequency sinusoidal wave, but usually a ramp signal is used because histogram test with ramp signals (or equivalent triangular signals) is significantly faster than that with sinusoidal signals. When noise figure is comparable to ADC measurement accuracy and all conversion codes need to be tested, ramp histogram testing method is faster than servo-loop testing method and also has lower overhead and testing costs.

The histogram testing method requires an accurate and highly linear ramp signal to correctly test ADC under test. Any non-ideal factors in ramp testing signals, e.g., quantization errors, device parameter variances, or unbalanced elements, will influence the measured ADC output codes and therefore have an impact on the transfer function of ADC. For example, to test a 16-bit ADC to 1/8LSB accuracy requires a ramp with 19 bits of resolution and overall linearity error of better than 2 ppm. A histogram ramp testing of ADC has been proposed [51] for imperfect ramp signals by measuring more samples per code. In a typical case, 14 samples are needed for each code and 10,000 codes in total would then be about 140,000 samples, which require about 140ms to perform the full range testing of an ADC with conversion speed of 1μs.

However, the histogram ramp testing method of this type cannot be easily applied to high-resolution ADCs because of the large amount of possible measured code by such ADCs. Considering in the same typical case, 14 samples are needed for an ADC with 16-bit resolution which has 65,536 possible codes in total and then required testing time is close

to 1s. Furthermore, generally a high-resolution ADC is significantly slower than a lower-resolution ADC and thus the required testing time would be much longer if conventional histogram ramp testing method is used.

Assuming an N-bit ADC with converting speed of S samples per second and average K samples per code for a reduced error margin, the total testing time for such an ADC using the histogram method is:

$$T = \frac{K2^N}{S} \tag{3.1}$$

Very low-slope ramp testing signals are also required to measure each possible code by ADC under test. Ramp signal generator typically consists of a current source (I) and a capacitance (C), and the open loop output voltage is $V = I \cdot t/C$. Further, assuming that the ADC measuring range is V volts, the ramp slope and current are:

$$\begin{aligned} \Delta V &= \frac{V}{T} = \frac{VS}{K2^N} \\ I &= \frac{CV}{T} = \frac{VSC}{K2^N} \end{aligned} \tag{3.2}$$

Suppose, $V = 3.3$V and $C = 47$pF for a typical design with reasonable testing hardware overhead, the calculated current source is only about 0.15nA from (3.2), which is comparable to the background noise and hence impractical for real designs. Thus, both situations are unacceptable in most applications.

The errors introduced during a histogram test method are classified into two categories: deterministic errors for inaccuracy and random errors for uncertainty of measured results. The ADC output is a combination of these two kinds of errors. In characterizing

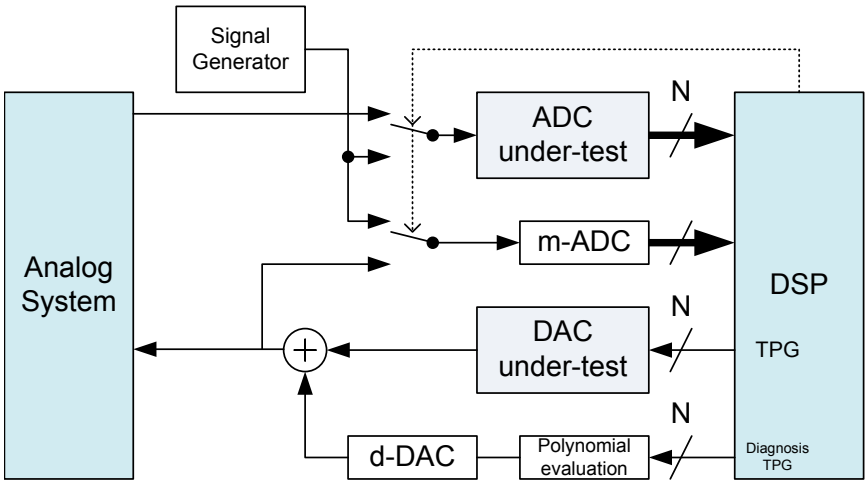

Figure 3.2: The proposed mixed-signal BIST architecture for testing both ADC and DAC.

ADC by measured results, the deterministic errors can be obtained by calculated coefficients because random errors will be greatly reduced by accumulation of measurements. Therefore, a minimal number of measurements must be determined.

3.2 Proposed Approaches

There are several papers that discuss mixed-signal testing techniques for ADC and DAC [16, 52]. In this dissertation, a post-fabrication mixed-signal BIST architecture is proposed for testing ADC/DAC and analog circuitry. Before the mixed-signal BIST starts, the proposed method requires that digital circuitry, including DSP and other peripheral digital logic, must have passed digital BIST and therefore we can assume that digital circuitry is fault-free and able to generate desired digital signals without any error.

After digital circuitry is tested and verified to be fault free by digital BIST architecture, for example, logic BIST, memory BIST, scan chains, etc., the mixed-signal BIST will start for testing of DAC/ADC and then for testing of analog circuitry. The proposed mixed-signal BIST architecture, as shown in Figure 3.2, includes three additional major parts for

testing ADC and DAC. These parts include an analog signal generator, a high-resolution measuring ADC and a low-resolution dithering DAC.

3.3 Testing Steps of BIST Architecture

The proposed mixed-signal BIST architecture includes four major steps to complete full-range self-test and calibration for on-chip ADC and DAC. Prior to the mixed-signal BIST, all digital circuitry must have passed digital test procedures, which has been already well studied and beyond the discussion topic in this thesis. The most widely employed digital test techniques that can be used for digital part of the mixed-signal system include logic BIST, scan chain, and cell/chip-level boundary scan. After digital circuitry passes its own digital testing procedure, it can be considered fault-free so that it will generate desired and correct digital data which in turn will be used for following mixed-signal testing procedures proposed in this thesis.

First step of the proposed BIST architecture is diagnosis of newly added testing hardware for on-chip ADC and DAC, as shown in Figure 3.3. A loopback connection may be established between analog signal generator and measuring ADC so that DSP can measure analog testing signals by measuring ADC. The results that DSP gets from measuring ADC shall be a rising consecutive codes and a simple histogram may be constructed to evaluate linearity of analog signal generator. A second loopback connection then can be established between dithering DAC and measuring ADC to measure dither DAC outputs. DSP will generate rising consecutive codes, which is converted into analog ramp signals by dithering DAC and then back into digital codes in turn by measuring ADC. During this test, DSP

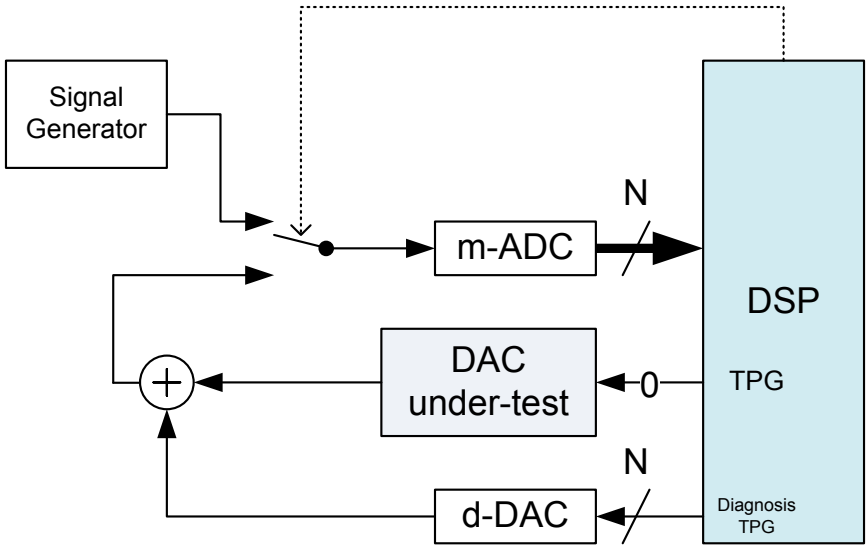

Figure 3.3: Diagnosis of testing hardware, including an analog signal generator, a high-resolution measuring ADC and a low-resolution dithering DAC.

shall drive on-chip DAC with zero so its outputs will not affect the measurements of m-DAC. Then DSP will be able to compare the measured digital codes from measuring ADC to its own generated codes to determine the linearity errors of dithering DAC. Three new added parts will be diagnosed in this step. Measuring ADC itself can be considered fault-free because any faults in the circuits and components of the measuring ADC will cause it malfunction and output wrong data for both analog signal generator and dithering DAC. Both of the linearity of analog testing signals and dither DAC can be measured by measuring ADC. The only chance that this self-diagnosis step fails to detect faults in the testing hardware for on-chip ADC and DAC is that the analog signal generator and dithering DAC has the exactly same output errors which happen to compensate errors of measuring ADC so that DSP obtains desired measurements from it. It is obvious that the possibility that this worst scenario happens is very rare.

Second step is testing of on-chip ADC using analog signal generator with either linear ramp testing signals for static test or sinusoidal testing signals for dynamic test. On-chip

ADC will measure generated analog signals and DSP will analyze the measurement for characterizing the ADC-under-test. It shall be noted that the analog signal generator must have been reset to zero before performing this step to make sure the results is not affected by its current status due to the previous step. DSP is occupied during the test and cannot run other tasks.

Third step is testing of on-chip DAC using DSP as both test pattern generator and output data analyzer which takes the output data from measuring ADC and characterizes the DAC-under-test. Digital test patterns generated by DSP can be of any form, however, in most cases ramp signal and sinusoidal signal are used for static and dynamic tests respectively. Multiple-tone sinusoidal signals can also be used to measure the third-order intermodulation (IM3), and linearity measured using third-order intercept point (IP3) [53]. DSP is occupied during the step too because it generate test patterns and analyze results.

The last step is calibration of on-chip DAC using dithering DAC that will generate negative compensating analog signals for every analog outputs of DAC-under-test so that the nonlinearity errors can be reduced, if not removed completely, from the final output of on-chip DAC. The compensation signals are calculated from characteristics of the DAC-under-test measured by measuring ADC. Dithering DAC can be driven with compensating values from either DSP directly or a hardware implementation which takes digital output codes.

In summary, testing steps for the proposed mixed-signal BIST architecture are:

1. Diagnosis of newly added testing hardware;

2. Testing of on-chip ADC using analog testing signals;

3. Testing of on-chip DAC using embedded DSP and measuring ADC;

4. Calibration of on-chip DAC using dithering DAC.

5. Validation of calibrated DAC using on-chip ADC

3.4 Components of BIST Architecture

3.4.1 Analog Signal Generator

An analog signal generator, usually linear ramp signal generator with very low gain to cover the full-scale of ADC input range, is used to generate analog testing signals for on-chip ADC. A sinusoidal signal generator can also be used in the place to generate very low frequency sine waves for testing on-chip ADC. ADC-under-test will measure the testing signals from the signal generator and samples will be picked up by DSP for analysis and characterization of the ADC.

If linear ramp testing signals are used, DSP will perform a static testing procedure, which is useful to obtain characteristics of ADC like nonlinearity errors, gain, offset and other harmonic distortions. If sine wave testing signals are used instead, DSP will perform a dynamic testing procedure to analyze the frequency response of the ADC, dynamic range, and other distortions. One of these two analog signal generator have to be chosen for a certain chip based on its application and working environment.

A linear ramp signal generator is easy to design and generates small footprint in die so the hardware overhead is lower. A sinusoidal signal generator is complex comparing to ramp generator, but it is capable of performing much more testing and measurements for different frequency. Single-tone sine wave signal can be used for analysis of frequency responses of a wide range so that more accurate characteristics, such as gain, offset and harmonic distortions can be acquired. Multiple-tone sine wave can also be used for analysis

of intermodulation distortions between two frequencies to obtain nonlinear characteristics, usually third-order intermodulation of two frequencies.

Here we will discuss the design of a linear ramp signal generator which is implemented for my thesis research.

Usually a ramp signal generator is designed using a cascaded current mirror so that the output ramp signals are linear and stable. W/L ratio of each transistor has to be carefully calculated to get desired scaling-down factor to achieve low-slope gain. Some special considerations must be taken because the load transistor in the output branch of current mirror may have a voltage drop so that the output voltage range may not cover full-scale of operational range of ADC-under-test.

A typical design of a highly linear ramp signal generator based on MOSFET current mirror is shown in Figure 3.4 [5, 52]. The slope of the generated ramp signal is slow enough and very linear to allow the static characterization of the entire dynamic range of an ADC under test.

To avoid leakage current which is not negligible with extra discharge current through the load, a buffer must be added to the output terminal at the cost of some linear range sacrificed. A switch between output terminal and ground in parallel with ramp capacitor will reset ramp generator to zero and initialize a rising ramp signals for ADC to measure.

All transistors in Figure 3.4 are working in saturation region and W/L ratio of each MOSFET is carefully assigned for low ramp gains. It is known that saturation current I_{ds} can be calculated by W/L ratio and V_{gs}:

$$I_{ds} = \frac{K}{2} \cdot \frac{W}{L} \cdot (V_{gs} - V_{th})^2 \tag{3.3}$$

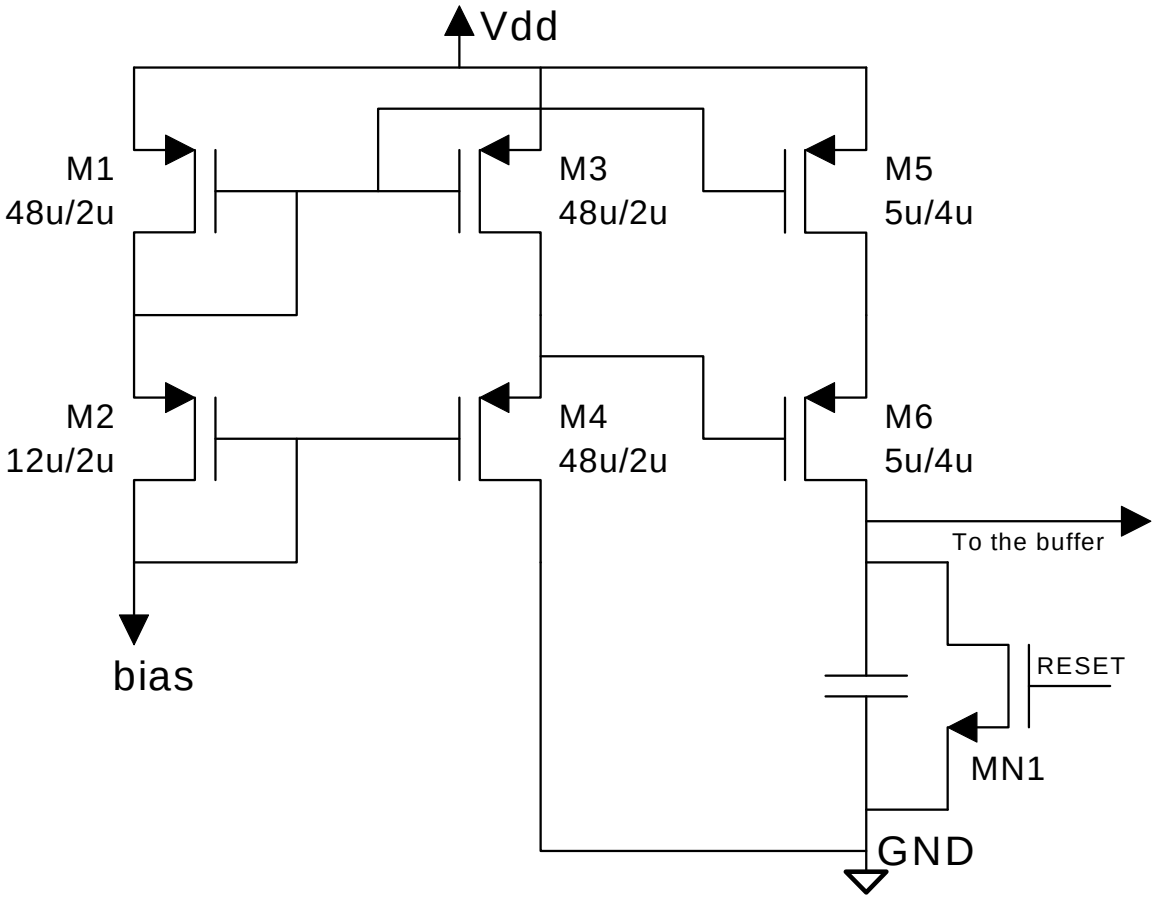

Figure 3.4: Design of ramp testing signal generator [5].

From (3.3), we can find that for every quadruple of W/L ratio or double of $V_{gs}-V_{th}$ value, the saturation current becomes quadruple. It also means that for the same saturation current in a single branch with two transistors, quadruple of W/L ratio of a certain transistor reduce $V_{gs}-V_{th}$ value by half.

Let us assume ΔV is $V_{gs}-V_{th}$ of M1. Supposed that bias current is I through M1 and M2, and voltage drop over M1 is $\Delta V+V_{th}$ due to the bias current, the mirror current in the branch through M3/M4 is also I because V_{gs} of M3 is same as M1. W/L ratio of M2 is one fourth of M1 but M1 and M2 have the same saturation current, so voltage drop of M2 is double of M1, that is $2\cdot\Delta V+V_{th}$. Thus, we can find that voltage drop from V_{DD} to gate terminal of M2/M4 is $3\cdot\Delta V+2\cdot V_{th}$.

The mirror current in the branch through M3/M4 is I, same as M1/M2, and M3 and M4 have the same W/L ratio, so V_{gs} of M3/M4 is same as M1 according to (3.3). Thus the voltage drop of M3 can be obtained,

$$V_{ds,M3} = V_{d,M4} - V_{ds,M4} \tag{3.4}$$

$$= (3 \cdot \Delta V + 2 \cdot V_{th}) - (\Delta V + V_{th}) \tag{3.5}$$

$$= 2 \cdot \Delta V + \cdot V_{th} \tag{3.6}$$

Transistor M5 has same V_{ds} as M1, but a much smaller W/L ratio, then the current in this branch is drastically reduced by nearly 20 times while voltage drop between gate-source terminals of M5/M6 is same as M1, which is $\Delta V + V_{th}$. In addition, because gate terminal of M6 connects to source terminal of M4 as shown in Figure 3.4, we can get that the voltage drop of M5 is exactly ΔV by subtracting V_{gs} of M6 from voltage drop of M3 in (3.6),

$$V_{ds,M5} = V_{ds,M3} - V_{gs,M5} \tag{3.7}$$

$$= (2 \cdot \Delta V + \cdot V_{th}) - (\Delta V + V_{th}) \tag{3.8}$$

$$= \Delta V \tag{3.9}$$

By carefully adjusting the bias current in the source current branch in order to make voltage drop of M1 small enough to be close to zero, the generated linear ramp signal, which is in the range of 0 though $V_{DD} - \Delta V$, will be able to cover nearly full-scale of operational range of on-chip ADC.

3.4.2 Measuring-ADC

A high-resolution measuring ADC is used for testing on-chip DAC by measuring DAC outputs and converting analog voltage levels from DAC output to digital codes. DSP then will compare measured digital results from this high-resolution ADC to generated test patterns for any possible difference.

In order to undergo fine analysis and to obtain results with more accuracy, effective resolution of the measuring ADC must be higher than that of DAC-under-test. If the measuring ADC cannot meet such resolution requirements, the values of its digital output codes are not sufficient to determine the errors existing in the DAC-under-test.

Since usually on-chip DAC get digital input codes directly from DSP, the DSP can act like a test patter generator for the DAC-under-test for both static and dynamic tests. If DSP generate ramp codes for on-chip DAC, a static test can be performed to obtain characteristics of ADC like nonlinearity errors, gain, offset and other harmonic distortions. In the other hand, if DSP generate approximate sinusoidal codes in sine/cosine wave forms, then a dynamic test can be done using measured results from measuring ADC to analyze its frequency response, dynamic range, and other distortions.

Conversion speed, which is a important characteristics for converters in general, is not a critical issue here for measuring ADC at all. Since such measurements of analog output signals from on-chip DAC by measuring ADC only be sampled during mixed-signal testing period, the performance of normal DAC operations after mixed-signal BIST is not affected by the conversion time of the measuring ADC. Therefore, in order to get more precise analysis characteristics of DAC-under-test, we can choose as high resolution ADC design and implementation for the measuring ADC as possible. The only requirement for the

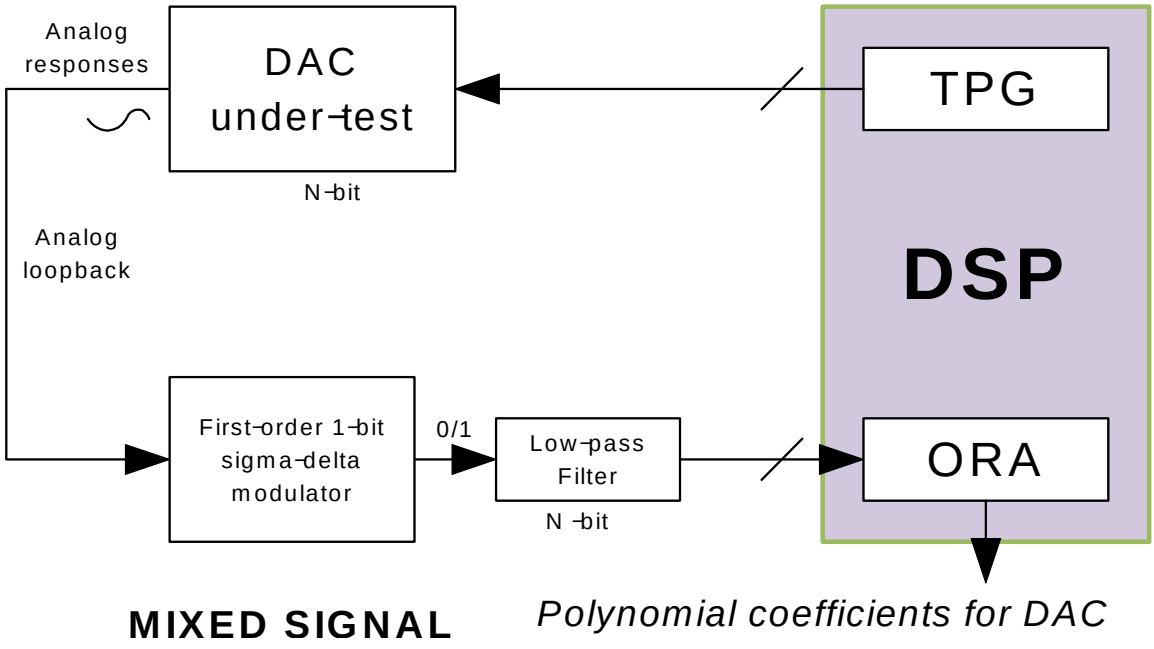

Figure 3.5: Test on-chip DAC by DSP and measuring ADC.

measuring ADC is that its design shall be simple enough so that it will not put a significant hardware overhead in the mixed-signal chip.

A Sigma-Delta modulation-based ADC is well suitable for the measuring ADC because Sigma-Delta modulation is able to achieve very high resolution easily by employing oversampling technique [54, 55]. The design of Sigma-Delta modulator is also easy to implement due to its simple structure and only a high-speed digital clock, which is used by digital quantizer within Sigma-Delta modulator, is required for the modulator to work properly.

A Sigma-Delta modulator-based measuring ADC (m-ADC) is employed to measure DUT outputs, as shown in Figure. 3.5. This m-ADC consists of a first-order 1-bit sigma-delta modulator and a digital low-pass filter (LPF). The measurements will compare to corresponding ramp test codes to obtain nonlinearity errors for polynomial fitting. Required

minimal resolution of the Sigma-Delta modulator depends on the resolution of DUT and d-DAC as well as fault-tolerance factor.

The minimal effective number of bits (ENOB) of Sigma-Delta modulator can be obtained by

$$\begin{aligned}\hat{N} &= \log_2 \frac{V_{ref}}{LSB_{d-DAC}} \\ &= N + N' - \alpha - 1 \end{aligned} \tag{3.10}$$

where d-DAC is the dithering DAC and α is the fault-tolerance factor, which will be discussed later. The signal-to-noise ratio (SNR) of m-ADC can be estimated as

$$\begin{aligned}SNR_{dB} &= 10\log\left(\frac{RMS_{signal}}{RMS_{noise}}\right) \\ &= 6.02\hat{N} + 1.76 \end{aligned} \tag{3.11}$$

The relationship between SNR and oversampling ratio (OSR) of first-order Sigma-Delta modulator is [4]

$$OSR = \frac{f_s/2}{f_0} = \frac{f_s}{2f_0} \tag{3.12}$$

$$SNR = \frac{3}{8\pi^2} OSR^3 \tag{3.13}$$

$$\begin{aligned}SNR_{dB} &= 10\log_{10} SNR \\ &= 30\log_{10} OSR - 14.2 \end{aligned} \tag{3.14}$$

where f_0 is maximum frequency of measured analog signals and f_s is sampling clock frequency of Sigma-Delta modulator.

Thus OSR of Sigma-Delta modulator can also be determined from (3.10) (3.11) and (3.14)

$$OSR = 10^{\frac{SNR_{dB}+14.2}{30}} \tag{3.15}$$

$$= 10^{\frac{6.02N+N'-\alpha+10}{30}} \tag{3.16}$$

For a given 14-bit on-chip DAC and 6-bit d-DAC, assuming fault-tolerance factor is 3, minimal OSR can be calculated using (3.16)

$$OSR = 10^{\frac{6.0214+6-3+10}{30}} = 2195$$

3.4.3 Dithering-DAC

A low-resolution dithering DAC, which generates dithering analog signals to compensate nonlinearity errors of on-chip DAC, is placed along with the DAC-under-test to reduce its nonlinearity errors and make it more linear and less deviation from ideal DAC. After raw analog output signals DAC-under-test are sampled and measured by the high-resolution measuring ADC, DSP will use the raw data to characterize on-chip DAC by comparing the measured data to generate test patterns. Thus the difference between measured digital data and generated test pattern for each code can be obtained and the detailed nonlinearity errors of DAC-under-test are obtained on its full-scale working range. DSP then can apply a compensating phase-inverted analog signal with the same magnitude of such nonlinearity error to output port of DAC-under-test by supply the same digital code to bother DAC-under-test and dithering DAC, so that the nonlinearity error of each digital code for DAC-under-test can be reduced, if not removed by the dithering DAC.

Since what dithering DAC is designed to remove are nonlinearity errors of on-chip DAC, which is much smaller analog value than DAC output values themselves, the dithering DAC is not necessary to be a high resolution one. Output analog values from dithering DAC must be scaled down to the magnitude of LSB of on-chip DAC, in order to compensate such nonlinearities of DAC-under-test. The exact required resolution of this dithering DAC depends on testing accuracy and tolerance of nonlinearity errors specified by on-chip DAC.

Usually dithering DAC with higher resolution is useful to gives better compensating results and larger range of nonlinearity tolerance so that both output signals quality and fixable errors are improved in theory. However, higher resolution design of DAC also means the complexity of dithering DAC increases dramatically and dithering DAC itself may be found more nonlinearity errors which would affect the final output signal quality of on-chip DAC in practice. Given a mixed-signal BIST application with certain on-chip DAC and measuring ADC, we have to make trade-off between testing accuracy and tolerance of nonlinearity errors by choosing proper resolution of dithering DAC and scaling-down factor of compensating signals for its outputs signals.

After the order and polynomials of best matching fitting polynomial are determined, they will be compared to pre-defined values. INL errors of DUT are correctable only if the polynomial coefficients are within the specified range; otherwise DUT will be marked as faulty by DSP. For correctable DUT, the fitting polynomial and its coefficients will be saved into memory cells and retrieved by polynomial evaluation circuit to generate correcting codes.

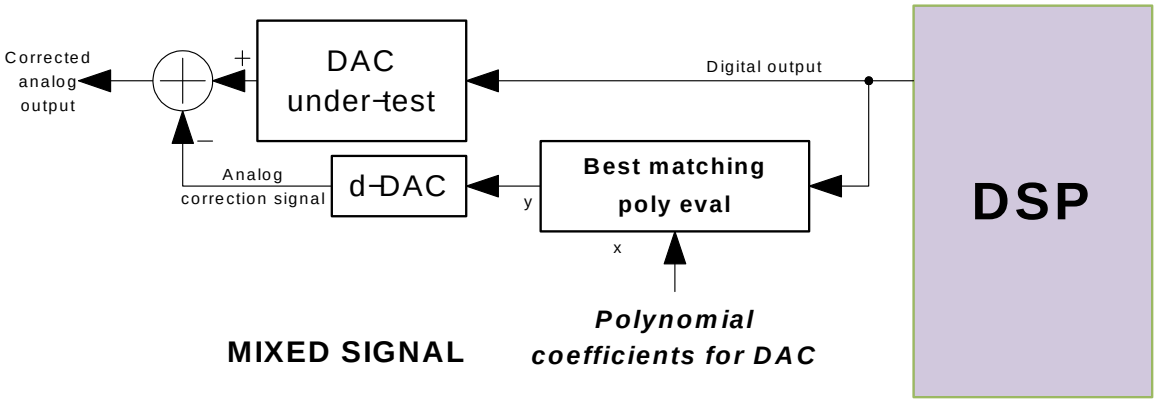

Figure 3.6: DUT calibration by dithering DAC (d-DAC) and best matching polynomial.

A low-resolution low-cost dithering DAC (d-DAC) will convert such correcting codes into correcting analog signals to remove nonlinearity errors from DUT output, as shown in Figure 3.6. Low-resolution d-DAC is simple to design and manufacture cost if low while converting speed is high. Higher-resolution d-DAC may generate more accurate correcting signals if total delay of polynomial evaluation circuit and d-DAC is less than converting time of DUT and such hardware overhead is acceptable. The reference voltage of d-DAC is defined by the resolution of DUT and fault-tolerance factor.

$$\begin{aligned} V_{ref,d-DAC} &= \pm\frac{2^{\alpha}}{2}\cdot LSB \\ &= \pm\frac{2^{\alpha}}{2}\cdot\frac{2V_{ref}}{2^{N}} = \pm 2^{\alpha-N}\cdot V_{ref} \end{aligned} \tag{3.17}$$

$$\begin{aligned} LSB_{d-DAC} &= \frac{2V_{ref,d-DAC}}{2^{N'}} \\ &= 2^{1+\alpha-N-N'}\cdot V_{ref} \end{aligned} \tag{3.18}$$

for N-bit DAC-under-test with reference voltage V_{ref},N'-bit d-DAC, and fault-tolerance factor α.

In most case, it is sufficient to choose α equal to 3 and to use 6-bit d-DAC for DUT correction. Thus for given 14-bit DAC-under-test, the reference voltage and LSB of d-DAC

are

$$V_{ref,d-DAC} = \pm\frac{V_{ref}}{2^{11}} \tag{3.19}$$

$$LSB_{d-DAC} = \frac{V_{ref}}{2^{16}} \tag{3.20}$$

3.4.4 Digital Test Pattern Generator

Instead of analog circuitry for testing signal generator, an alternative method for testing of on-chip ADC is construct test pattern generator by digital circuitry to generate digital test patterns as input vectors of ADC-under-test. Due to design flexibility of digital signal processing techniques, the generated test patterns can be of any forms to fit for various applications and test requirements. When a static test is required for characterizing ADC-under-test with parameters like nonlinearity errors, gain, offset and harmonic distortions, a low-slope low-gain linear ramp waveform (or equivalent triangle waveform) will be usually used to cover the full-scale of input signal range of the converters. In the other hand, a sinusoidal waveform will be used for dynamic test of ADC-under-test with parameters like frequency response, dynamic range and other distortions. Other forms of digital test patterns can also be used with little hardware or software overhead.

The digital test pattern generator (TPG) can be either implemented in hardware or in software. Hardware implementation of DTPG provides fast generation speed and requires no extra software to run and to occupy DSP running time to generate these test patterns. And software implementation of DTPG gives very flexible solution to generate any forms for digital test patterns by updating firmware running at DSP and occupies no extra die size to increase hardware overhead of the testing scheme.

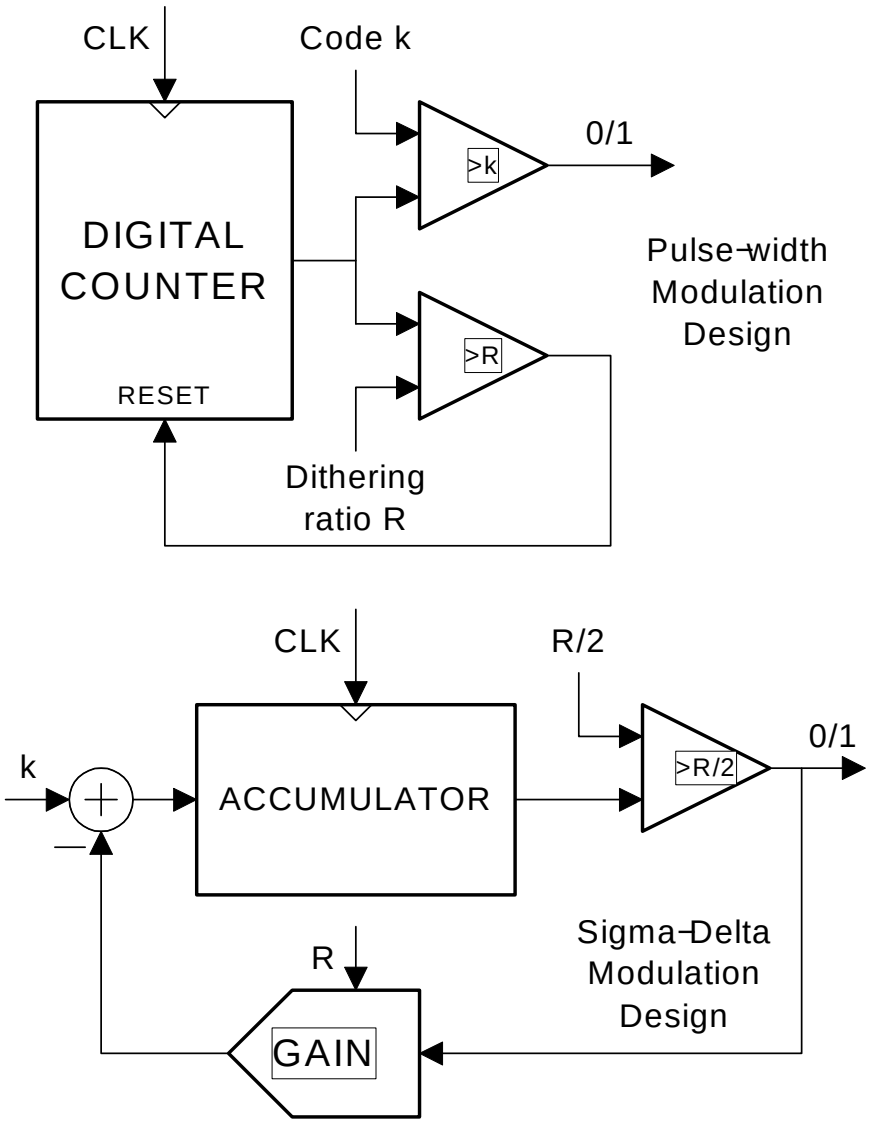

Figure 3.7: Schematics of digital test pattern generator (DTPG).

DTPG takes *N*-bit digital input code *k* and generate a series of 1-bit stream of which ratio of number of 1s and 0s reflects *k*. DTPG can be implemented as either hardware components or software running by DSP, but the process behind the implementations are essentially same. Figure 3.7 shows two schematics of typical digital test pattern generators.

The simplest design of DTPG is use of pulse-width modulation (PWM), of which duty cycle of signal representing ratio of 1s to total unit bits reflects input signal. DTPG will generate a bit-stream with unit length of dithering ratio *R*, a serial of 1s with length of

n_1 is output at first, then a serial of 0s with length of n_0. It is obvious that $R = n_1 + n_0$ and duty cycle is n_1/R. PWM is easy to implement but suffers serious drawback due to the imbalance of 1s and 0s in its waveform. So the dithering noise of PWM is widely distributed and difficult to completely remove because some of the noise is very close to lower signal band. To separate in-band signals from dithering noise, test pattern frequency cannot be very high to avoid be interfered by noise. Therefore PWM design of DTPG is only suitable for applications with low conversion rate ADC.

The other design of DTPG is similar to Sigma-Delta modulation. An accumulator (as Sigma component in Sigma-Delta modulation) and a comparator (shown as a triangular component) is used to process input code k. The feedback loop consists of a differential component and a multiplying factor F (equal to 2^N or 0). F depends on the DTPG output, 2^N if output is 1, 0 otherwise. $k - F$ is added into the accumulator. DTPG outputs 1 if accumulator is larger than 2^{N-1}, 0 otherwise. With this design, 1s and 0s of bit-stream from DTPG output is more likely distributed. If k is minimum value 0, DTPG outputs bit-stream of 0s; if k is maximum value $2^N - 1$, DTPG outputs bit-stream of 1s. If k is other intermediate value, DTPG will output appropriate number of 1s and 0s so that the ratio of number of 1s to R is equal to $k/2^N$. For example $k = 2^{N-1}$, DTPG will output bit-stream like $010101010101\cdots$.

Figure 3.8 demonstrate a typical 4-bit ramp pattern and bit-stream for the ramp, of which digital code k goes from 0 to 2^4 =16. For N-bit ADC, a total number of 2^N ramp patterns are required for full range static response test so that every code that ADC can measure is generated. We may observe that quantization noise is distributed in signal band and after dithering digital ramp patterns into bit-stream, a high-frequency dithering noise

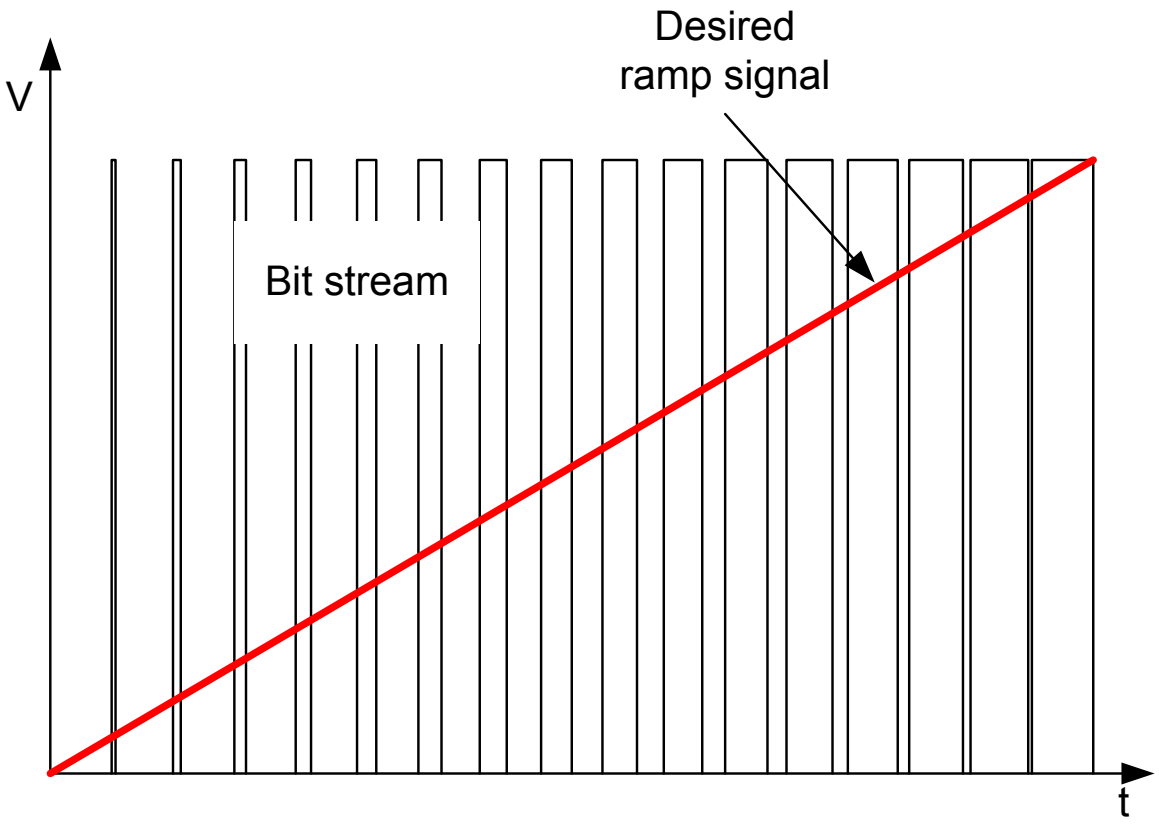

Figure 3.8: Typical analog ramp signals from DTPG patterns.

is introduced at sampling frequency f_s. Low-pass filter will remove dithering noise from analog test signals, and high dithering ratio is necessary to remove digital quantization noise. High dithering ratio R means long period of test patterns, so low digital signal frequency is required for static response test for on-chip ADC to obtain stable and precise measurements. The drawback of high dithering ratio is long testing time.

$$T = R \cdot 2^N \cdot t_s = \frac{R \cdot 2^N}{f_s} \tag{3.21}$$

In most cases, dithering ration must be equal to or larger than number of codes (2^N), so testing time for static response is at least 2^{2N} times sampling period. For example, 10-bit on-chip ADC needs 100ms for static response test with 100 MHz digital clock.

A typical single-tone sinusoidal full-range pattern for 10-bit ADC and its dithering bit-stream can be used for dynamic test. The full-range pattern is generated by DSP and can be used for dynamic response test at specific digital signal frequency. In fact DSP may generate arbitrary form of test patterns for various applications. Beside single-tone test pattern, multiple-tone test patterns can also be used to measure inter-modulation between two frequencies by ADC-under-test.

Assuming analog signal frequency of single-tone sinusoidal pattern is f_0 and digital signal frequency is f_d, where f_d must be at least twice f_0 according to Nyquist-Shannon sampling theorem so that DSP may recover sinusoidal pattern from ADC outputs. From (4.1), given digital clock frequency f_s, the maximum analog signal frequency f_0 for single-tone sinusoidal pattern is $f_s/2R$. However, all digital codes have to be covered to perform a full-range ADC test, thus the ratio of analog signal to digital signal frequency must be more than $2R$.

Therefore, the sampling clock ratio of f_s to f_0 must be larger than $2R \cdot 2^N$, and the practical maximum sinusoidal pattern frequency for full-range dynamic test is

$$f_0 = \frac{f_s}{2R \cdot 2^N} \tag{3.22}$$

where R must be equal to or larger than 2^N for N-bit ADC. Similar to (3.21) for static response test, the minimum test time required for one dynamic response test can be calculated as,

$$T = 2R \cdot 2^N \cdot t_s = \frac{2R \cdot 2^N}{f_s} \tag{3.23}$$

The low-pass filter will remove dithering noise and quantization noise of sinusoidal pattern as for ramp pattern.

3.5 Testing of On-chip Converters

In this section, we will discuss the detailed steps of testing of each component in the mixed-signal BIST architecture. Before any testing steps of on-chip converters, logic BIST of digital circuitry must have been successfully tested and passed so that the digital part of the mixed-signal system can be considered fault-free. The testing components, including analog signal generator and measuring ADC, have to be tested in the first place in order to guarantee minimal noise and errors existing in the output data of generated analog testing signals and measuring results. Then on-chip ADC and DAC under test may undergo mixed-signal testing procedures respectively. Since both tests require DSP as digital test pattern generator or digital result analyzer so these two test procedures cannot be performed simultaneously. After both tests of on-chip ADC and DAC finish, we can tell the testing results from characteristics calculated by DSP and if values of all characteristics are within the allowed limits, the chip then can be considered as fault-free in mixed-signal circuitry. Furthermore, if values of some characteristics exceed the allowed limit ranges but can be calibrated by calibration circuits, which will be discussed later. The on-chip ADC/DAC would be considered as faulty only if any value of obtained characteristics exceeds calibration range to that it cannot be fixed by the propose post-layout calibration process.

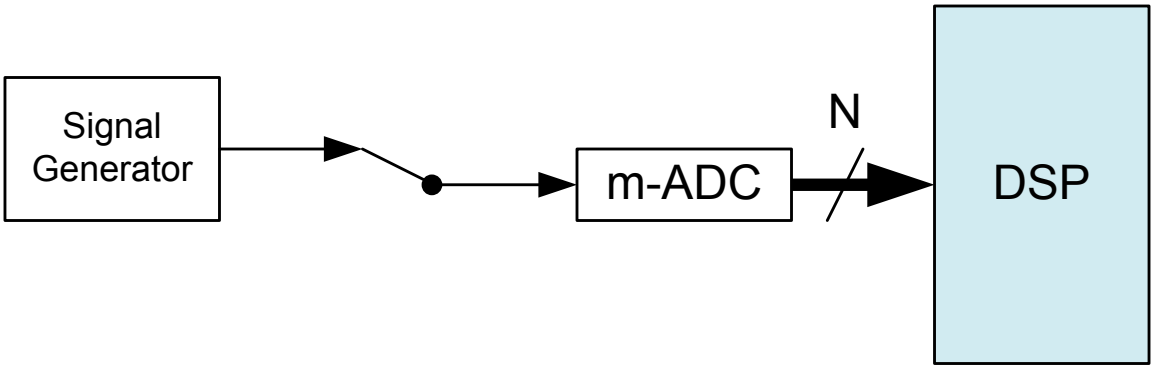

Figure 3.9: Diagnosis of analog signal generator and measuring ADC.

3.5.1 Diagnosis of Testing Components

To diagnose new-added testing components, including an analog signal generator, a high-resolution measuring ADC and a low-resolution dithering DAC, two sub-steps have to be taken for two pairs of analog-digital data sets. One pair is analog signal generator and measuring ADC; the other pair is dithering DAC and measuring ADC.

Figure 3.9 shows the diagram for analog testing signal generator and measuring ADC. The analog testing signal generator has been initialized to zero before measurements and it stops as soon as the measuring ADC outputs the maximum digital code for DSP to analyze.

Since the analog testing signal is in fact intended for testing of on-chip ADC, the effective resolution of measuring ADC can be set to be same as that of on-chip ADC. Provided the resolution of on-chip ADC is N-bit, and measuring ADC is a first-order single-bit Sigma-Delta ADC, the minimum SNDR required for both ADC are:

$$SNR = 6.02 \cdot N + 1.76 \tag{3.24}$$

$$SNR = 10 \cdot \log_{10}\left(\frac{3}{8\pi^2} OSR^3\right) \tag{3.25}$$

$$= -14.2 + 30 \log_{10} OSR \tag{3.26}$$

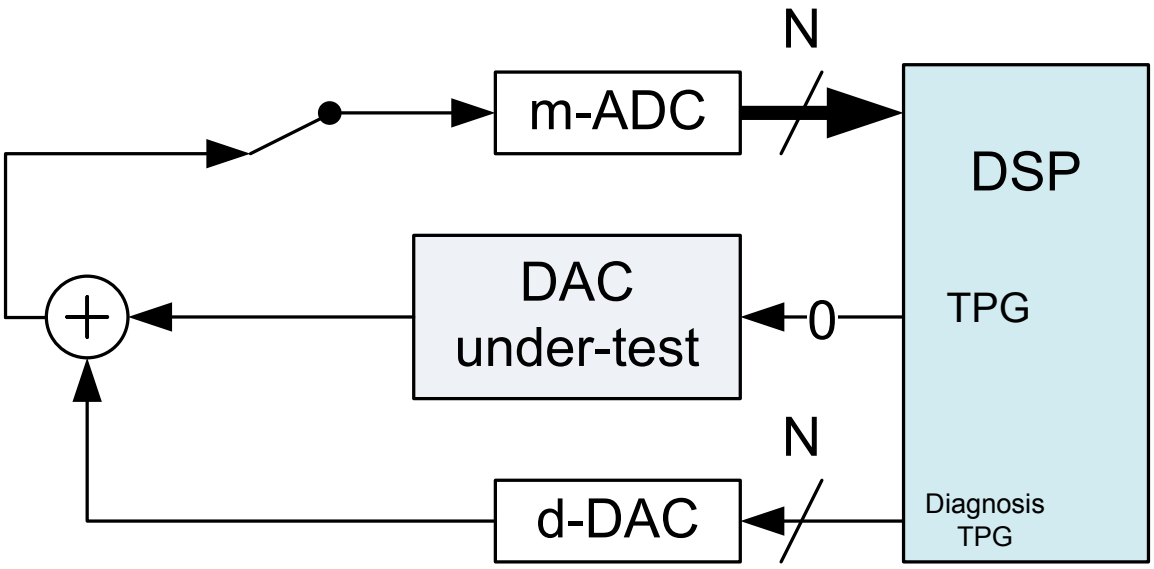

Figure 3.10: Diagnosis of dithering DAC and measuring ADC.

Equation (3.24) is for on-chip ADC and (3.26) for measuring Sigma-Delta ADC. Next, we get:

$$OSR = 10^{\frac{6.02 \cdot N + 1.76 + 14.2}{30}} \tag{3.27}$$

Assuming that the resolution of on-chip ADC is 14 bits, and by (3.27), we can conclude that the required minimum oversampling ratio (OSR) to sample the analog testing signal generator is about 2194 to fully test the generator.

Figure 3.10 shows the diagram for dithering DAC and measuring ADC. DSP will act as both test pattern generator (TPG) to drive dithering DAC and output result analyzer (ORA) to collect measurements for analysis. During this test, DSP must drive on-chip DAC to a constant value, usually zero, to make sure that on-chip DAC will not affect diagnosis process of the dithering DAC. Since dithering DAC is a low-resolution DAC, the measuring ADC will not working at as high oversampling ratio as that for analog testing signal generator. Because DSP knows both test patterns and output results, it is simple to

detect any inconsistence between these two digital values and find possible errors in the dithering DAC.

Assuming that the resolution of the dithering DAC is only 6 bits, apply it to the same equation (3.27), then we can get the minimum OSR for this case is 55. Therefore the diagnosis of dithering DAC is much faster than that of analog signal generator.

If both self-diagnoses pass the test by demonstrating desired form of digital signals, for example, rising digital consecutive codes for linear ramp signals, we can consider the newly-added testing hardware without fault. There could be only one exceptional case that existing fault cannot be detected, which happens when analog testing signals and dithering DAC has the exactly same nonlinearity errors and those errors can exactly compensate those of measuring ADC. It is obvious that such chance is very rare and it is nearly impossible for all three components match the condition at the same time.

3.5.2 Test of On-Chip ADC

The proposed approach is shown in Figure 3.11 [27]. Similar to a histogram testing method [56], this ADC BIST architecture also consists of three major components, a test signal generator, the on-chip ADC under test and a digital signal processor (DSP) for measured data processing and analysis.

Linear ramp testing signals are used to stimulate the ADC under test for simple implementation and short test time. Let the linear ramp signals sampled by the on-chip ADC be,

$$f(k) = a \cdot T \cdot k + b \tag{3.28}$$

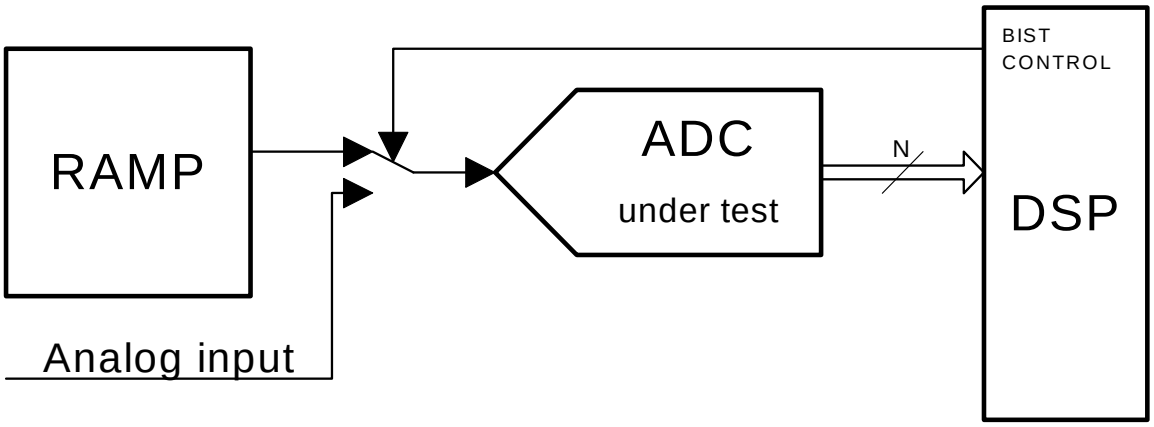

Figure 3.11: The proposed ADC BIST architecture.

where T is interval time between samples, a and b are coefficients of the linear function ($a > 0$), and k is the variable of samples.

Initially, b is presumed to be close enough to zero so that the measurements always begin with code 0. This condition can be satisfied by the implementation to always reset ramp signal generator to output signal close to zero. If the next sample is still measured as 0 then the previous sample is discarded until a non-zero output code is measured. On subsequent samples the output ascends until the measurement of K-th sample output $f(K)$ reaches $2^N - 1$ which is the maximum possible output code of N-bit ADC. Thus, we have following assumptions for the measured outputs of the ADC under test,

$$M(k)|_{k=0..K} = \begin{cases} 0 & k = 0 \\ M_{ADC}(f(k)) & k = 1..K-1 \\ 2^N - 1 & k = K \end{cases} \tag{3.29}$$

For an ideal ADC there is no nonlinearity error and the ramp testing signals may be reconstructed using,

$$f(k) \approx M(k) \cdot LSB + e_q \tag{3.30}$$

However, it must be noted that quantization errors (e_q) still exists in the reconstructed ramp signal function though the effect of these errors may be reduced by accumulation of a large number of samples as shown below.

Because $M(0)$ and $M(K)$ are the lower and upper bounds for all measurements and their corresponding signals $f(0)$ and $f(K)$ might fall outside ADC measurement range, these two measurement must not be considered during the characterization of the ADC. All other measurements, $M(1)$ through $M(K-1)$, are divided into two equally-sized parts and then accumulated into two sums so that we may get the time-domain functions of ramp testing signals from (3.30),

$$\begin{aligned} s_0 &= \sum_{k=1}^{K/2} M(k) = \frac{1}{LSB} \cdot \sum_{k=1}^{K/2} f(k) \\ &= \frac{1}{LSB} \cdot \left(\frac{1}{8} K (K+2) aT + \frac{1}{2} Kb \right) \end{aligned} \tag{3.31}$$

$$\begin{aligned} s_1 &= \sum_{k=K/2}^{K-1} M(k) = \frac{1}{LSB} \cdot \sum_{k=K/2}^{K-1} f(k) \\ &= \frac{1}{LSB} \cdot \left(\frac{1}{8} K (3K-2) aT + \frac{1}{2} Kb \right) \end{aligned} \tag{3.32}$$

Then, two syndromes can be obtained from the two sums using following equations,

$$S_0 = s_1 - s_0 \tag{3.33}$$

$$S_1 = -s_1 + 3 \cdot s_0 \tag{3.34}$$

Applying (3.31) and (3.32) to (3.33) and (3.34), respectively, we get

$$S_0 = \frac{1}{LSB} \cdot \left(\frac{1}{4} K (K-2) aT \right) \tag{3.35}$$

$$S_1 = \frac{1}{LSB} \cdot (K (aT + b)) \tag{3.36}$$

From these two equations, the coefficients of the ramp signal function can be found as,

$$a = LSB \cdot \frac{4S_0}{K (K-2)} \cdot \frac{1}{T} \tag{3.37}$$

$$b = LSB \cdot \left(\frac{S_1 K - 2S_1 - 4S_0}{K (K-2)} \right) \tag{3.38}$$

Finally, the two coefficients of time-domain ramp function (3.28) can be recovered from two sums by applying (3.33) and (3.34). Thus,

$$a = LSB \cdot \frac{4 (s1 - s0)}{K (K-2)} \cdot \frac{1}{T} \tag{3.39}$$

$$b = LSB \cdot \frac{(3s_0 - s_1) K - 2(s_0 + s_1)}{K (K-2)} \tag{3.40}$$

A DSP block, presumed to be available on the mixed-signal SoC, is used to accomplish all computations shown above. The on-chip ADC measures test signals and the DSP reads and processes the ADC output codes. It uses (3.39) and (3.40) to approximately reconstruct the original ramp test signal function. The DSP then compares each ADC measurement to the expected code from the reconstructed test signal function to get INL errors of the ADC under test. The two coefficients can also be used to determine offset errors of the ADC under test.

The principal steps of the proposed BIST approach for on-chip ADC can be described as follows [27]:

1. Reset testing signal generator to output ramp signals.

2. Detect first non-zero output from ADC; all previous samples are discarded.

3. Measure all subsequent samples and record ADC output codes until the maximum possible code are detected.

4. Accumulate measured samples in two equally divided parts and get two sums.

5. Using (3.39) and (3.40) obtain approximate coefficients for the signal function.

6. Calculate expected code for each sample using the obtained signal function and compare it to the measured code to get INL errors.

The two coefficients of the test signal function can also be used for a preliminary estimation of INL error of the ADC under test. The absolute value of magnitude of coefficient b indicates overall offset error of ADC and the value of a indicates ramp slope of testing signals. The coefficient b should be around zero because $\|b\| < 0.5LSB$, and a should be close to the design specification of ramp signal generator for ADC under test to pass BIST. If the preliminary conditions are not satisfied, there will be a high probability that that ADC under test is faulty.

The same idea can also be applied when using low-frequency sinusoidal test signals for nonlinearity test of an ADC under test. Let a sinusoidal test signal be in the form shown below:

$$f(k) = A\left[1 + \sin\left(\omega T \cdot k - \frac{pi}{2}\right)\right] \tag{3.41}$$

where $\omega = 2\pi F$ is the frequency of sinusoidal test signal generated, and T is unit time interval of samples. Assuming $f(0)$ is measured zero, $f(1)$ is measured non-zero, and $f(K)$ is the first measured highest possible code, we get $f(K) = A$ and thus, we can get the maximum time interval of sampling given a required minimal number of total samples:

$$T = \frac{\pi}{\omega K} = \frac{1}{2FK} \tag{3.42}$$

However, the design of such a sine-wave signal generator for ADC is more complicated than that of ramp signal generator because the former requires a stable low-frequency oscillator to generate test signals, a voltage shifter and a low-noise amplifier to move signal voltages to the working range of the ADC.

3.5.3 Test of On-Chip DAC

This section describes details of the proposed BIST scheme to generate digital stimulus, to measure DAC outputs and to calculate parameters that determine the performance of DAC and control the dithering DAC for calibration. To test on-chip DAC, as shown in Figure 3.12, BIST control unit generates a series of consecutive digital codes (corresponding analog voltage v_k) from the lowest value (v_0) to the highest value (v_{n-1}) and uses sigma-delta modulator to sample the output of DAC as ($\hat{v}_k$):

$$\hat{v}_k = v_k + q_k + \hat{q}_k \tag{3.43}$$

where q_k is the quantization error of the on-chip DAC and $\hat{q}_k$ that of sigma-delta ADC. $\hat{k}$ is captured at the output of the sampling sigma-delta ADC for each input code k. For an

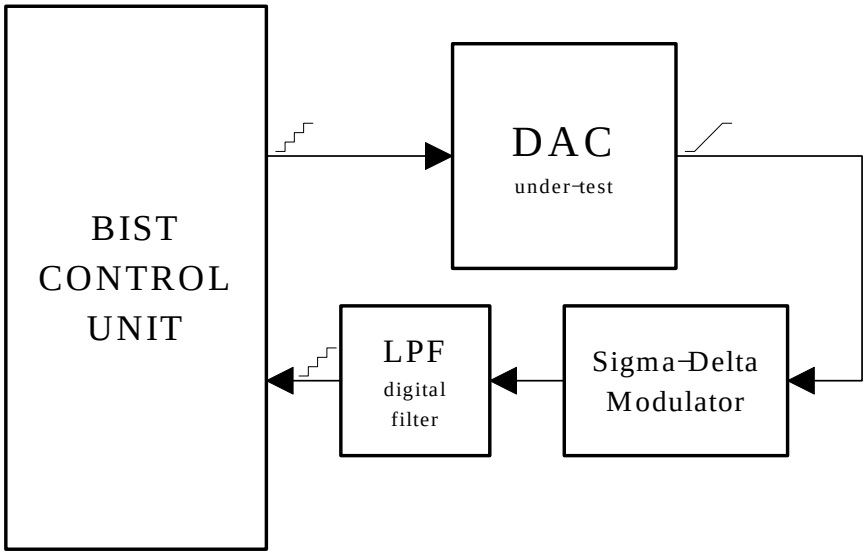

Figure 3.12: Test circuitry of DAC.

accurate measurement, $\hat{k}$ must contain more effective number of bits (ENOB) than that in k. The ENOB of $\hat{k}$ is determined by the oversampling ratio K, and requires higher K to obtain larger ENOB and better resolution. Thus, the total quantization error for each code k is,

$$\varepsilon_k = \hat{v}_k - v_k = q_k + \hat{q}_k \tag{3.44}$$

$\hat{q}_k$ is small enough to be ignored with high oversampling ratio K and thus the quantization error is mainly from the on-chip DAC. The dithering DAC will then eliminate ε_k from the DAC output for normal operation and output linearity can be further improved by employing a dynamic element mismatching (DEM) technique. Because of large number of ε_k for each code k, (2^N in total for N-bit DAC), it requires a huge amount of memory to store the compensation data for every code, thus the 3^{rd}-order best fit algorithm shown above is used to reduce memory consumption. On the other hand, the quantization error ε_k for each code k also satisfies the requirements for the polynomial fitting algorithm. Applying

the fitting algorithm to INL error ε_k, rather than result $\hat{v}_k$ obtained from sigma-delta modulator as [23] proposed, will make it easier for dithering DAC to generate compensation signals. The consecutive codes from v_0 to v_{n-1} are divided into four equal-size segments and quantization errors ε_k in each segment are summed up to get four fundamental sum values:

$$S_0 = \sum_{k=0}^{n/4-1} \varepsilon_k = \sum_{k=0}^{n/4-1} (\hat{v}_k - v_k) \tag{3.45}$$

$$S_1 = \sum_{k=n/4}^{n/2-1} \varepsilon_k = \sum_{k=n/4}^{n/2-1} (\hat{v}_k - v_k) \tag{3.46}$$

$$S_2 = \sum_{k=n/2}^{3n/4-1} \varepsilon_k = \sum_{k=n/2}^{3n/4-1} (\hat{v}_k - v_k) \tag{3.47}$$

$$S_3 = \sum_{k=3n/4}^{n-1} \varepsilon_k = \sum_{k=3n/4}^{n-1} (\hat{v}_k - v_k) \tag{3.48}$$

where $n = 2^N$ is the total value range for the N-bit on-chip DAC.

Being mathematically equivalent to the least-square fit it can produce the best unbiased (linear) estimates for the coefficients by feeding converter with a linear ramp test stimulus covering the full range of conversion. The converter may work at full speed to traverse the ramp stimulus and the output results are sampled by a measuring device. The full range of conversion is divided into four equal interval segments, as shown in Figure 5.1. The samples at each segment are accumulated and the four sums are S_0, S_1, S_2, and S_3. The general third-order polynomial equation to fit converters is

$$y = b_0 + b_1 x + b_2 x^2 + b_3 x^3 \tag{3.49}$$

The input x is assumed to be a cosine waveform to relate the four coefficients to harmonic distortion,

$$x = A \cdot \cos(\omega t) \tag{3.50}$$

$$y = c_0 + c_1 \cos(\omega t) + c_2 \cos(2\omega t) + c_3 \cos(3\omega t) \tag{3.51}$$

where c_0, c_1, c_2, and c_3 represent DC offset, gain, and 2^{nd} and 3^{rd} harmonic distortions, respectively.

We assume the following four syndromes from combination of sums:

$$B_0 = S_3 + S_2 + S_1 + S_0 \tag{3.52}$$

$$B_1 = S_3 + S_2 - S_1 - S_0 \tag{3.53}$$

$$B_2 = S_3 - S_2 - S_1 + S_0 \tag{3.54}$$

$$B_3 = S_3 - 3S_2 + 3S_1 - S_0 \tag{3.55}$$

One can derive [23] four coefficients for the best fit polynomial from the syndromes:

$$b_0 = \frac{1}{N}\left(B_0 - \frac{4}{3}B_2\right) \tag{3.56}$$

$$b_1 = \frac{4}{N \cdot n}\left(B_1 - \frac{4}{3}B_3\right) \tag{3.57}$$

$$b_2 = \frac{16}{N \cdot n^2} \cdot B_2 \tag{3.58}$$

$$b_3 = \frac{128}{3 \cdot N \cdot n^3} \cdot B_3 \tag{3.59}$$

The characteristics of converters are derived from the syndromes as well:

$$c_0 \approx \frac{B_0}{n} \qquad \text{Offset} \tag{3.60}$$

$$c_1 \approx \frac{4B_1}{N \cdot n} \qquad \text{Gain} \tag{3.61}$$

$$c_2 \approx \frac{B_2}{B_1} \qquad 2^{nd}\text{harmonic} \tag{3.62}$$

$$c_3 \approx \frac{2B_3}{3B_1} \qquad 3^{rd}\text{harmonic} \tag{3.63}$$

where N is the total number of samples and n is the range of the converter ($A = n/2$, $n = 2^N$). The approximated equations are accurate if the number of samples is large enough (typically greater than 1000, i.e., equals or exceeds 10 bits).

The syndromes and coefficients of the best fit polynomial for ramp signal are calculate from these four sum values using (3.52) through (3.55) and (3.56) through (3.59), respectively.

With these coefficients, representing offset, gain, and 2^{nd} and 3^{rd}-order harmonic distortions by calculating quantization error, we can construct a best fitting curve that has least square error. We use (3.49) and (3.51) to replace the actual quantization errors by both DAC and sigma-delta ADC. To achieve even higher linearity of ε_k, the ENOB of sigma-delta ADC shall be larger than number of bits in the DAC, usually at least 3 more effective bits, though test time would be slightly longer. The reference voltage of the dithering DAC can be the maximum *INL* error for the on-chip DAC in theory and usually 3 LSB is used for this dithering range to guarantee the full compensation for a low quality on-chip DAC. Because of spurious factor introduced by the dithering DAC to the final result of on-chip DAC, a low-pass filter must be used to filter out any high frequency noise.

3.5.4 Calibration of On-Chip ADC/DAC

After coefficients of the fitting polynomial are obtained from syndromes, the polynomial can be used to recover static INL error for each code and therefore can be used to drive dithering-DAC to generate compensating signals to fix nonlinear quantization outputs of on-chip DAC.

To calibrate on-chip DAC, the quantization error of DAC can be calculated by two output values,

$$\Delta v_k = v_k - \hat{v}_k \tag{3.64}$$

for each test stimulus code k, where v_k is the ideal DAC output and $\hat{v}_k$ is the actual output of DAC-under-test. Four coefficients of a 3^{rd}-order polynomial function are calculated from the sums obtained from four equally-divided segments. Δk is the N'-bit code of calculated voltage value Δv_k by N-bit code k and $\hat{N}$-bit code $\hat{k}$. Δk will be used by digital BIST control unit for actual calculation to obtain coefficients. These four coefficients will be used to recover N'-bit code Δk, to generate compensation signal for DAC output during ADC BIST in next step, and in the normal operation until the power is finally turned off.

An N'-bit dithering DAC using a dynamic element matching (DEM) technique is used for accurate compensation with high-tolerance mismatches among the current sources of the DAC. Assuming DEM iteration factor p, meaning N'-bit dithering DAC generates p outputs for each input code Δk, we get DEM elements distance factor q so that $p \cdot q = 2^{N'}$. After eliminating spurious data by an LPF, the performance of dithering DEM DAC is comparable to an ideal DAC with $N' + \log_2 p$ ENOB as discussed in a previous paper [57]. A typical implementation of dithering DEM DAC contains $2^{N'}$ current sources which are

divided into p segments with element distance of q. For any code k, k consecutive current sources from $(d-1)q+1$ through $(d-1)q+k$ are turned on at d^{th} iteration ($1 \leq p$).

The implementation of BIST circuitry and algorithm to test ADC-under-test is quite similar to the techniques used for DAC-under-test. BIST control unit generates exactly the same consecutive codes as digital test stimuli for the on-chip DAC, which then outputs an analog ramp signal. BIST reads the digital conversion output of ADC-under-test whose input is the ramp signal. Since testing and calibration of DAC has been completed in the previous step and the resolution and linearity is improved, the quantization error of DAC may be ignored now.

Four coefficients of a third-order best-fitting polynomial function are obtained from the output of ADC in a similar fashion as was done for the Sigma-Delta modulator in the previous step. The calibration of on-chip ADC is simple,

$$k = k' + \Delta k \tag{3.65}$$

where k' is N'-bit ADC output, Δk is calculated from polynomial function, and k is calibrated result. We should point out that this procedure only makes limited compensation to the linearity and does not improve the resolution of ADC-under-test.

The proposed test and calibration approach is verified by simulation in Matlab for 14-bit on-chip DAC and ADC model on various quantization noise levels. A 6-bit low-cost dithering DAC model is used in the simulation to generate compensating analog signal for DAC calibration. The reference voltage for the dithering DAC is 3 LSB of on-chip

DAC considering fault tolerance of its resolution. However, this is enough to calibrate the on-chip DAC with 3 more ENOB.

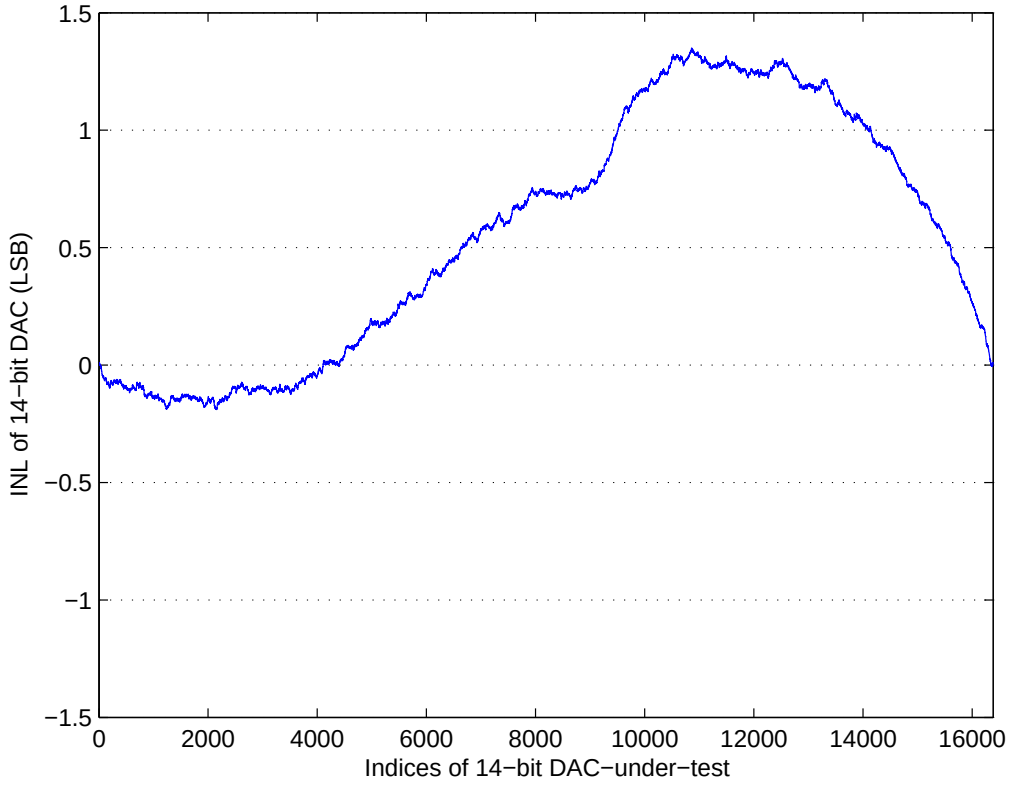

Figure 3.13: INL of simulated 14-bit DAC-under-test.

Figure 3.13 depicts INL of a 14-bit DAC with maximum 1.4 LSB quantization error from a Matlab simulation in which random noise was introduced. The maximum INL magnitude is within a pre-defined range, e.g., 3 LSB in this case, so that this on-chip DAC could be calibrated. If INL_k for any code k falls outside the specified range, the on-chip DAC would fail the test. Under ideal condition the negative values of these INL data could be used as calibrating signals for DAC outputs to obtain perfect linear results. However, it is impractical to store such huge amount of INL data for every input code, especially with high resolution DACs.

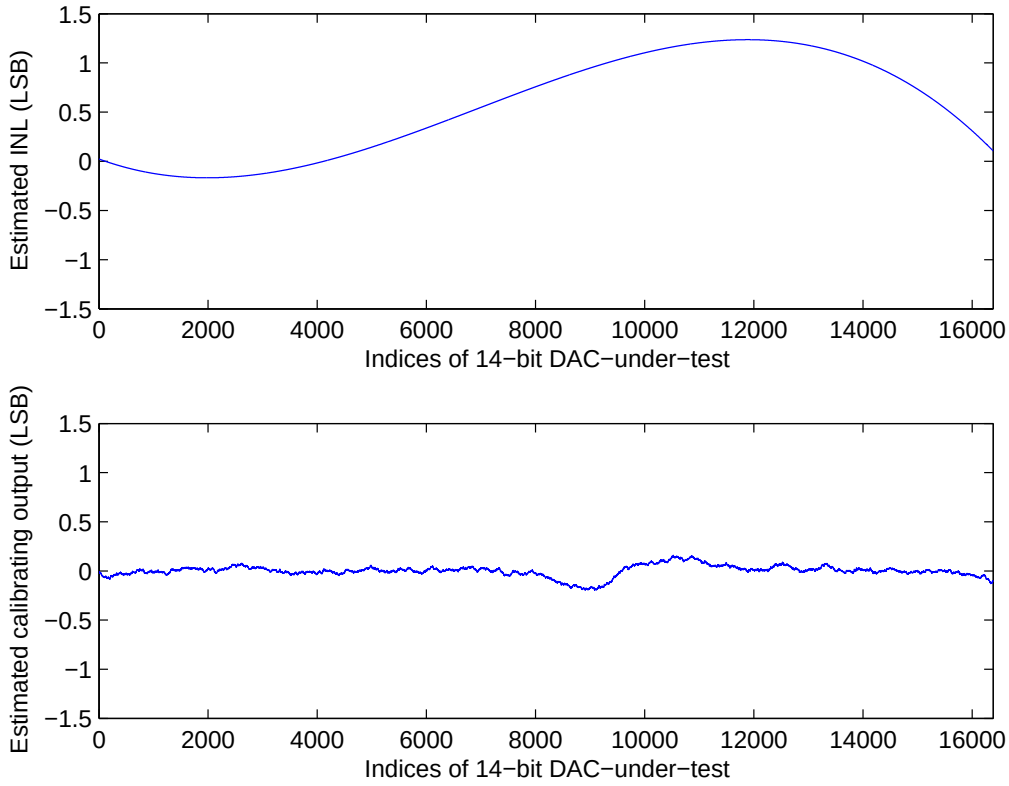

Figure 3.14: Least mean-square fit third-order polynomial (top) and estimation error (bottom) for DAC-under-test INL data of Figure 3.13.

The polynomial fit algorithm, which will be further described in Chapter 5 in details, will dramatically reduce the required data to only four coefficients of a 3^{rd}-order polynomial. By dividing the INL data of Figure 3.13 into four equal code segments, we get sums S_0, S_1, S_2 and S_3, syndromes B_0, B_1, B_2, and B_4, and polynomial fit coefficients b_0, b_1, b_2, and b_3 shown in Table 3.1. These were obtained by the method of [24, 23]. Figure 3.14 shows the best mean-square third-order polynomial fit and the estimation error by the fitting algorithm. The average error is about $-39.3dB$.

Similar results for a low-quality 6-bit dithering DAC are shown in Figure 3.15. This dithering DAC will generate analog calibrating signals for DAC output by four fit coefficients (b_0, b_1, b_2, and b_3) calculated above. The reference voltage of the DAC is typically

Table 3.1: Third-order polynomial fit for INL of Figure 3.13.

i	Sum, S_i	Syndrome, B_i	Coefficient, b_i
0	$2.5437E3$	$-0.1959E4$	0.93
1	$1.9997E3$	$-1.1045E4$	$9.2746E5$
2	$-3.3732E3$	$-2.8564E3$	$-1.0391E8$
3	$3.1289E3$	$-2.3792E3$	$-1.4088E12$

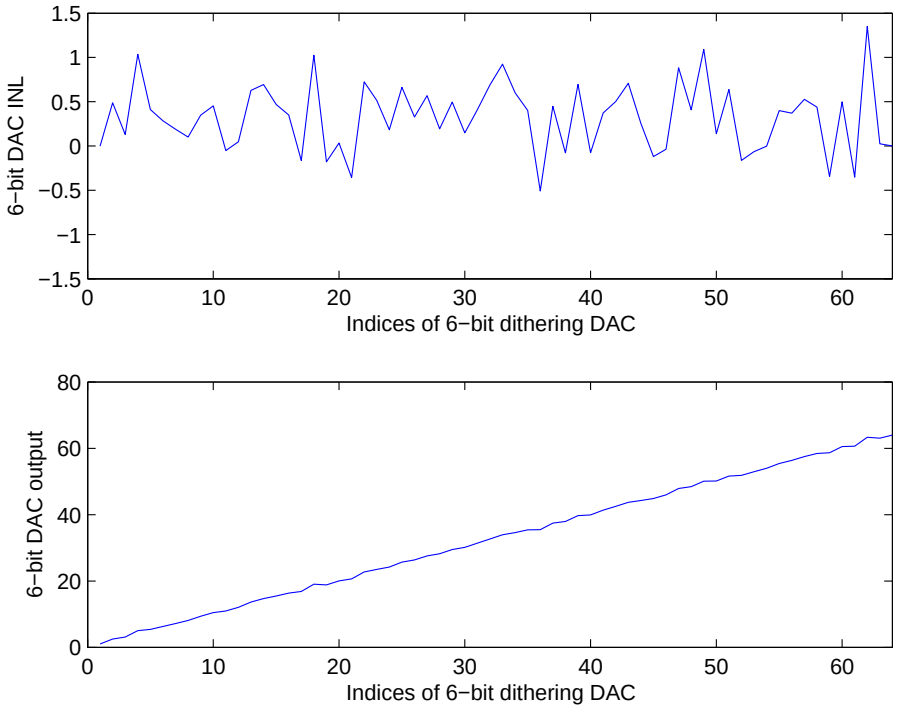

Figure 3.15: INL (top) of simulated 6-bit dithering DAC, and DAC outputs (bottom).

3 LSBs of the DAC-under-test. Using a reference voltage higher than 3 LSB will provide a larger range of calibration and hence better fault-tolerance but will lower the calibrating precision and worsen linearity. On the other hand, using less than 3 LSB will provide better calibration precision and linear outputs but worsen fault-tolerance feature of the DAC.

The final calibrating output of the 14-bit DAC-under-test using the 6-bit dithering DAC is shown in Figure 3.16. By subtracting the outputs of the 6-bit dithering DAC from that of DAC-under-test as shown in Figure 3.13, the linearity of DAC will be significantly improved. Due to the quantization error of low-resolution dithering DAC, the calibrating

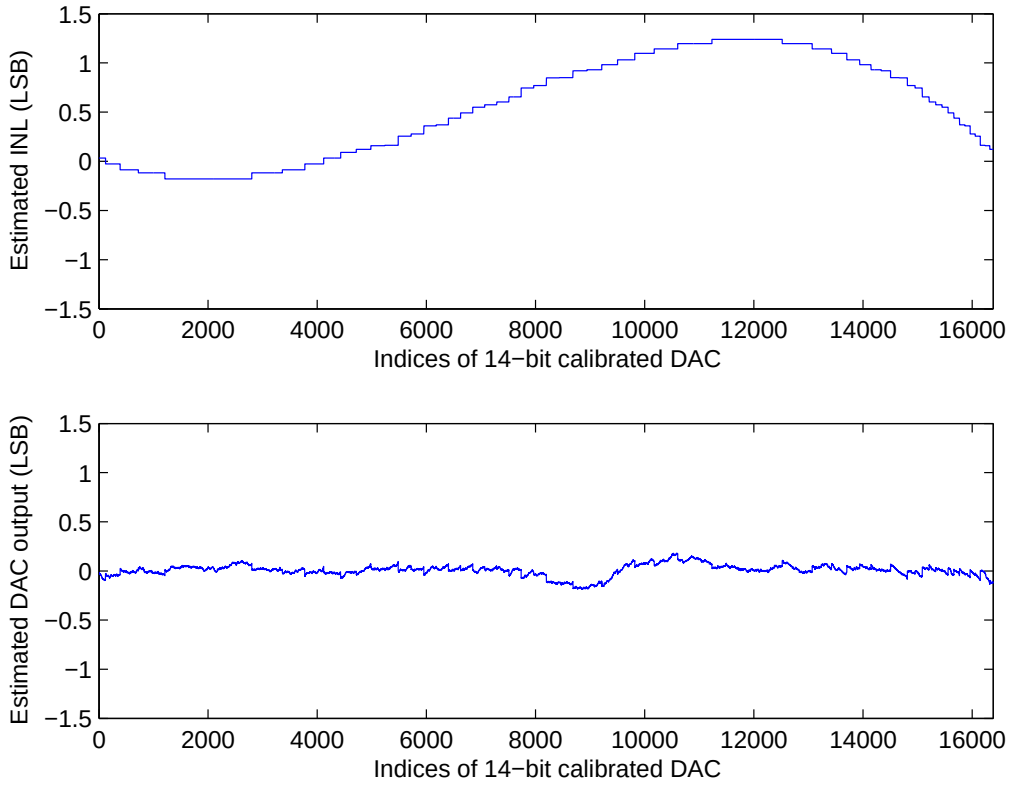

Figure 3.16: INL (top) of calibrated 14-bit DAC-under-test using third-order polynomial fit and 6-bit dithering DAC, and corresponding estimated INL error (bottom).

data is not exactly as good as shown in Figure 3.14. The average estimation INL error of calibrated DAC output is about $-38.0dB$, still acceptable in this case. Figure 3.14 also shows that the INL of the calibrated DAC is not greater than 0.25 LSB, which is comparable to the ideal DAC with 16-bit resolution. So the on-chip DAC is improved by 2-bits of resolution in this case.

3.5.5 Verification of ADC/DAC Test Results

After both on-chip DAC and ADC are tested by the proposed approach, two converters-under-test are characterized and calibrated separately, the real output of the compensated

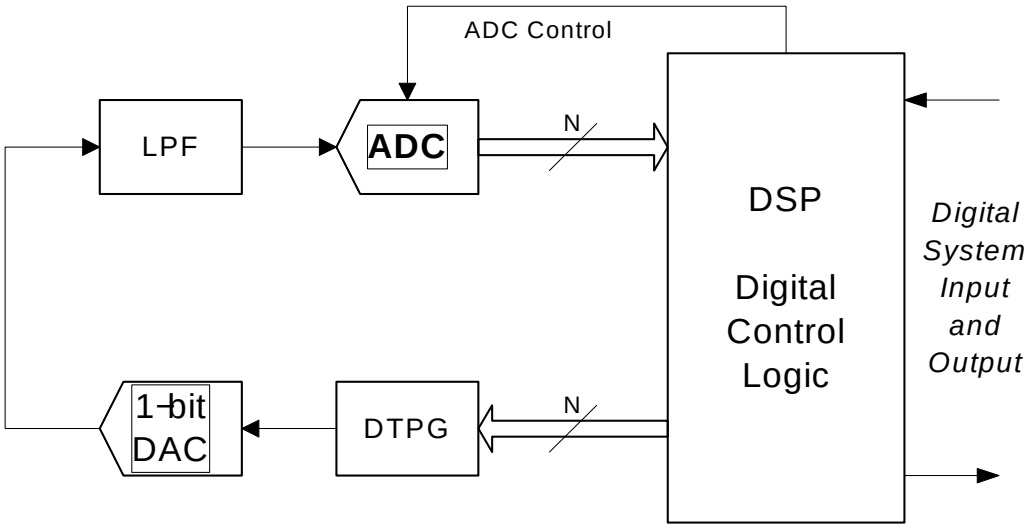

Figure 3.17: Proposed digital ADC self-test architecture.

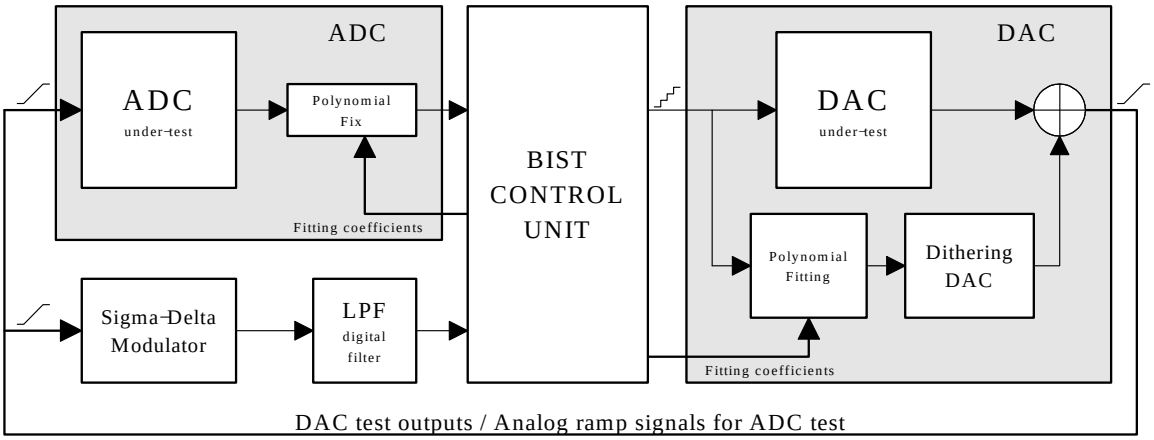

Figure 3.18: Test of DAC with loopback connection between DAC output and ADC/m-ADC input ports.

converters must be verified with each other to guarantee that INL errors are within the allowable range. A local analog signal loop will be established for verification by connecting output pin of on-chip DAC to input pin of on-chip ADC. The block diagram of verification scheme is shown in Figure 3.17 which consists of a digital signal processor (DSP) to generate test patterns for DAC inputs and to acquire ADC output results, and a feedback loop connecting DSP output to ADC input.

During the verification of ADC/DAC testing results, DSP will be able to generate any desired test patterns, same as test for on-chip DAC, to perform static of dynamic test on DAC-ADC loop. Then DSP can collect measured outputs from on-chip ADC and compare the results against generated test patterns to obtain INL and DNL errors for static test, and frequency response, dynamic range, harmonic distortions, etc., for dynamic test. Usually a static test with a ramp code will be used for nonlinearity errors since INL is most concerned in this thesis.

After the local analog signal loop connection is established between DAC and ADC, DSP generates consecutive codes from minimum value to maximum one to drive on-chip DAC and dithering DAC. The input codes to on-chip DAC will generate analog outputs in its output, just as it has been tested during the test for DAC. The same codes to dithering DAC will be used by the polynomial evaluation unit (PEU) to generate the compensating analog signals to reduce the nonlinearity errors of on-chip DAC output values. Four coefficients, which are obtained using polynomial fitting algorithm will be stored and applied to the PEU to generate proper compensating signals,

$$\tilde{v}_k = c_0 + c_1 \cdot k + c_2 \cdot k^2 + c_3 \cdot k^3 \tag{3.66}$$

The calibrated outputs of on-chip DAC will then be,

$$v_k = \hat{v}_k - \tilde{v}_k \tag{3.67}$$

The combined analog signals of on-chip DAC and dithering DAC then will be measured by on-chip ADC and subsequently retrieved by DSP for comparison against the corresponding generated test patterns. If the verification step confirms that nonlinearity errors between generated test patterns and measured samples are within 0.5LSB, it means that both on-chip DAC and ADC are both operating normal after calibration because in the previous steps they are independently tested and calibrated. Otherwise, either one of on-chip DAC or ADC may be faulty if in the verification steps any nonlinearity error is found exceed 0.5LSB.

3.5.6 Minimal Number of Samples

Since measurements by ADC always contain quantization errors owing to its nature to convert continuous analog wave into discrete digital code, a minimal number of samples must be taken to ensure that such quantization errors are negligible in the process. Let us first consider an ideal ADC. The quantization errors of the ideal ADC can be anywhere between $\pm\frac{LSB}{2}$, and as more samples ADC measures less quantization errors remain after accumulating all measurements. A histogram approach can be considered as the extreme situation of the requirements, which needs multiple samples for each code to make sure that the quantization error is essentially removed from statistical distribution of codes.

However, for a non-ideal ADC under test, there are two possibilities that must be taken into consideration. It is always possible that some codes with greater nonlinearity errors are not measured during BIST, and also it is possible that a measured nonlinearity error introduces distortion to the reconstructed transfer function of ramp signals.

Generally, the first problem will be non-existent if every code is measured at least once, and the second problem will be effectively eliminated with large number of samples because such nonlinearity errors will be attenuated to make little impact on the calculation. In practice, we found that at least 2^{N-2} samples should be measured to perform this BIST procedure on an N-bit ADC to avoid these two issues and ensure that ramp signals are reconstructed properly.

3.5.7 Delay of Polynomial Evaluation

The other issue is the miscorrelation between delay times of DAC-under-test and polynomial evaluation unit. Since polynomial evaluation involves large amount polynomial calculation, which is mostly digital circuits, it will impose additional delay from DSP to dithering-DAC. Hence a potential issue arises to the calibrated DAC outputs because the output analog signals could be divided into two sections. In the first section, on-chip DAC generates output signals which possibly contain nonlinearity errors larger than 0.5LSB. In the second section, dither-DAC generates compensating signals to fix corresponding nonlinearity DAC outputs by removing portion of nonlinearities. However, due to the differences in delay between these two timing paths, these two signals may not arrive at DAC output simultaneously and therefore cause additional unexpected error to the analog system. To diminish such delay effects, the combined delay of polynomial calculation circuitry and low-resolution dithering-DAC must be less or equal to the conversion time of on-chip DAC.

Thus, the delay of polynomial evaluation unit must be taken into consideration in the late verification step. After DSP drive on-chip DSP and dithering-DSP with certain

test pattern, it will expect a measured data from on-chip ADC outputs. If DSP observes miscorrelation in the measurements, even the final measurements being correct and within the 0.5LSB limit, the verification must show a failure.

3.6 Summary

In this chapter, the proposed built-in self-test and calibration scheme for analog-to-digital and digital-to-analog converters is described in details. On-chip ADC is tested using ramp signals from analog signal generator, and its outputs are collected by DSP. On the other side, On-chip DAC is tested by digital ramp test patterns generated by DSP, and measured by a high-linearity measuring-ADC, which is based on Sigma-Delta modulation. Both data from ADC and DAC are finally processed by DSP using polynomial fitting algorithm to obtain four polynomial coefficients which can be used to estimate characterizations of converters, such as offset, gain, and high order distortions. The four polynomial coefficients then will be used by polynomial evaluation unit during result verification and normal operations. In the final result verification step, DSP will generate another set of test patterns, usually ramp patterns, to drive both on-chip DAC and dithering DAC (through polynomial evaluation unit to calibrate DAC) to make DAC outputs with reduced nonlinearity errors. On-chip ADC will measure the combined DAC outputs after calibration to verify that nonlinearity errors of both DAC and ADC are within 0.5LSB. Otherwise, it means that either the on-chip ADC or DAC is faulty.

Chapter 4

Sigma-Delta ADC

4.1 First-order 1-bit Sigma-Delta Modulation

For ADC based on Sigma-Delta modulation, typically as shown in Figure 4.1, over-sampling technique is used to distribute quantization noise over a wider frequency range (up to sampling frequency f_s) than the digital signal frequency (f_d). Thus, the in-band noise is reduced and SNDR is improved [58, 59]. Oversampling ratio (OSR) is defined as [60]:

$$OSR = \frac{f_s}{2 \cdot f_d} \tag{4.1}$$

SNDR of Sigma-Delta ADC is revised from (2.16) to consider oversampling ratio:

$$SNDR = 6.02 \cdot ENOB + 1.76 + 3 \cdot log_2 OSR \tag{4.2}$$

From (4.2) we may observe that SNDR of an ADC based on first-order 1-bit Sigma-Delta modulation will increase by 6 dB for each additional bit in conversion resolution, and 3dB for doubling sampling frequency.

A typical Sigma-Delta ADC in Figure 4.1 consists of a Delta modulator and integrator ($H(s)$) in a negative feedback loop. Quantization noise ($E(s)$) is introduced into the system

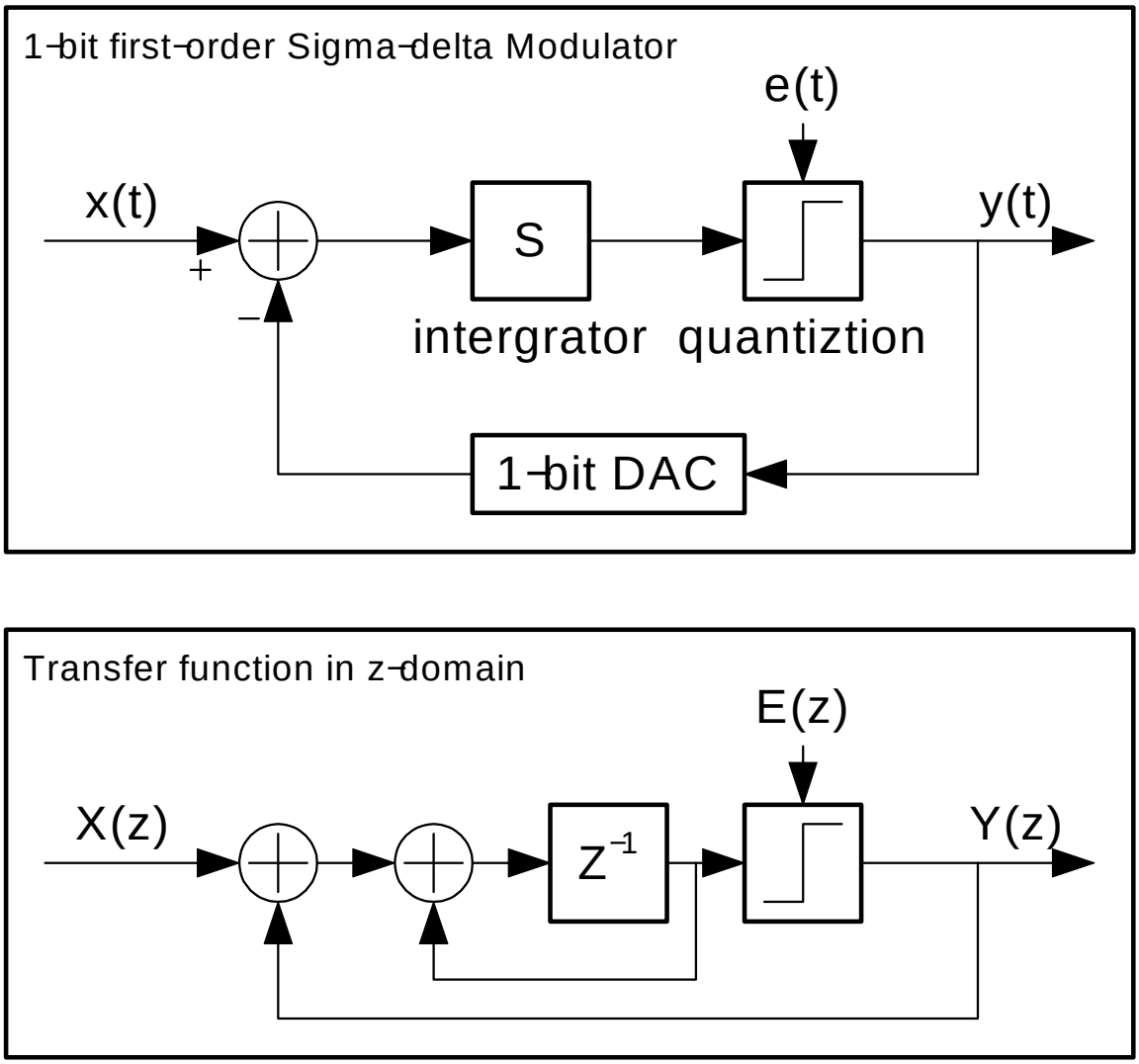

Figure 4.1: Schematic of an typical ADC based on first-order 1-bit Sigma-Delta modulation and its transfer function in z-domain.

by the quantizer (1-bit ADC) and a 1-bit DAC. The transfer function of close loop of Sigma-Delta modulator can shape the quantization noise by pushing the noise further up to out-band of input signal, so that a low-pass filter (typically digital filter, e.g., accumulator) will be able to remove the most of noise. Let input and output signals of the Sigma-Delta ADC in s-domain be $X(s)$ and $Y(s)$, respectively.

$$Y(s) = X(s) \cdot \frac{H(s)}{1+H(s)} + E(s) \cdot \frac{1}{1+H(s)} \tag{4.3}$$

It can be observed that the close loop acts like a low-pass filter for input signal ($X(s)$) and high-pass filter for quantization noise ($E(s)$). Due to 1-bit ADC and DAC used in the negative feedback loop, nonlinearity error in these analog components can be ignored. Therefor with oversampling and noise shaping techniques, Sigma-Delta ADC is able to achieve both high resolution and high linearity with large number of OSR.

However, according to the Nyquist-Shannon sampling theorem, given a specific sampling frequency, large OSR will effectively reduce bandwidth of input signal and also extent the conversion time. Conversion time is also a critical measurement of ADC performance, especially for high speed applications which require fast converting rate for high frequency input analog signals.

The digital BIST circuitry cannot process the analog ramp signals directly, so we employ a first-order 1-bit Sigma-Delta modulator to sample DAC output and to convert each analog signal k to corresponding digital code $\hat{k}$.

The proposed Sigma-Delta modulator includes an integrator, an 1-bit quantizer, and an 1-bit DAC. With oversampling and noise-shaping techniques Sigma-Delta DAC is simple to design and implement for achieving high linearity without strict requirements for high quality components. By oversampling the quantization noise of Sigma-Delta ADC is uniformly distributed over a wider band up to half of sampling frequency (Nyquist frequency) and therefore the overall noise figure is reduced. Because the signal to noise ratio (SNR) of simple oversampling increases by 3dB for each doubled sampling rate, the oversampling rate (OSR) must be quadrupled for each ENOB of resolution gain. The feedback loop (consisting of a quantizer and a 1-bit DAC) acts as a low-pass filter for input analog signals and high-pass filter for internal quantization error. So the quantization noise is removed

from the lower band and is concentrated in the high-frequency end of the Nyquist band. Therefore, the noise is shaped to higher band than input signals.

More than one integration and loop stages could be used to build high-order Sigma-Delta modulators for better quantization noise-shaping and ENOB gain for a given OSR. However, a high-order Sigma-Delta modulator is not as stable and linear as a first-order modulator [61], which is our choice in this application. Testing time of the first-order 1-bit Sigma-Delta modulator is not an issue since the testing and calibration procedure is executed only during chip powering up and therefore modulator will not affect the performance of the normal operation.

Figure 4.1 shows a typical design of first-order 1-bit Sigma-Delta modulator. The transfer function of the modulator is

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})E(z) \tag{4.4}$$

where $E(z)$ is the quantization error introduced by the Sigma-Delta modulator.

Assuming oversampling rate of a Sigma-Delta modulator is M, each analog signal output by DAC-under-test for code k must have M samples by the modulator. The SNR of Sigma-Delta modulator with an oversampling rate M is

$$M = \frac{f_s}{f_0} \tag{4.5}$$

$$n_0 = e_{rms}\frac{\pi}{\sqrt{3}}\left(\frac{1}{M}\right)^{3/2} \tag{4.6}$$

$$SNR = \frac{1}{n_0 \cdot 2\sqrt{2}} \tag{4.7}$$

$$\approx \frac{\sqrt{3}M^{3/2}}{2\sqrt{2}\pi^2} \tag{4.8}$$

where f_s is the sampling frequency of Sigma-Delta modulator and f_0 is the operational frequency of the DAC.

Assuming $e_{rms} = 1$, the input signal RMS value is $1/2\sqrt{2}$ and SNR for the first-order Sigma-Delta modulator can be obtained. Generally, we can get higher SNR using larger oversampling rate at the cost of longer measuring time for each code, but this would apply only to BIST stage and does not affect DAC/ADC performance during normal operations.

The reference voltage of the modulator must be same as that for the DAC-under-test in order to make sure that the conversion result is precise and any difference between results and stimuli is only the quantization error introduced by the DUT itself.

The accuracy of modulator must be higher than that of DUT, which means that the resolution of the modulator is higher than that of DUT, in order to measure the DUT outputs. Furthermore, delta-sigma modulator may have to be accurate enough to calibrate DUT for several more bits of resolution. We estimate the required number of bits of the modulator from the following equation:

$$ENOB_{\Sigma\Delta} = N_{DUT} + N'_{d-DAC} - \log_2 \alpha \tag{4.9}$$

where we have N-bit resolution for DAC-under-test, N'-bit resolution for dithering DAC, and α as a scaling factor for INL range of fault tolerance.

Taking a large value for α, the scheme becomes more capable of fixing the nonlinearity error of DUT but the final calibrated resolution becomes lower. On the other hand, a small α can be used for better calibration result with a reduced range of nonlinearity error tolerance. Suppose, we choose $\alpha = 8$, giving 3 LSB range of fault tolerance. The ENOB

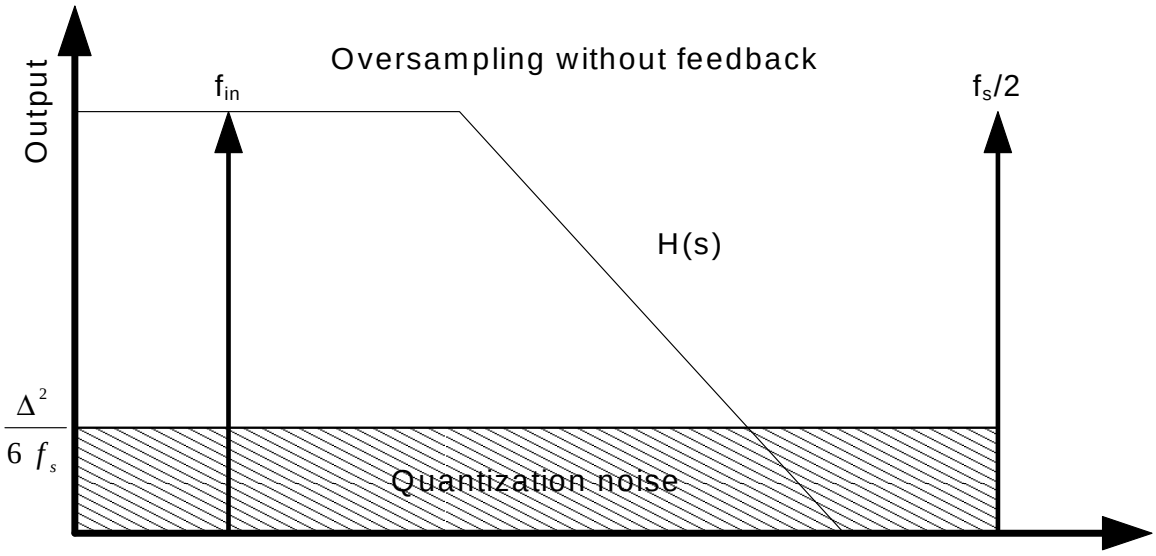

Figure 4.2: Oversampling system without noise-shaping feedback.

of the modulator must be larger than $\hat{N} = N + N' - 3$ for the desired INL voltage range. Thus, the SNR of the Sigma-Delta modulator is [62]

$$SNR = 6.02\hat{N} + 1.76 \tag{4.10}$$

where $\hat{N}$ is ENOB of the modulator calculated above for given DUT and dithering DAC.

4.1.1 Oversampling and Noise Shaping Techniques

From (4.2), we can find that the SNR improves by 6 dB for every bit added to the quantizer. For the same amount of total quantization noise power, every doubling of the sampling frequency reduces the in-band quantization noise by 3 dB, as shown in Figure 4.2. Thus RMS (root mean square) value of the in-band quantization noise is reduced by the oversampling technique since the total noise is spread across the entire sampling bandwidth [4]. Hence, every doubling the oversampling ratio (OSR) is equivalent to increasing the quantizer levels by a half-bit for concerned quantization noise.

Oversampling technique allows the use of a lower-resolution converter without sacrificing noise performance and the trade-off between measuring time and accuracy. Doubling the oversampling rate, meaning longer conversion time and lower converting signal frequency at the same sampling frequency, gives two times number of correlated signal samples and the signal power is increased by 6 dB. In other words, the signal samples are correlated while the noise samples are not. Thus the SNR improvement of 3 dB is obtained corresponding to a half-bit resolution improvement.

The benefit of oversampling technique is that the requirements on analog antialiasing filter for A/D converters or *deglitching* filters for D/A converters is lower due to wider transition bands from oversampling and therefore only low-order filter are needed. The disadvantage of oversampling technique is the requirements on high oversampling ratio to achieve high resolution, that is, much higher sampling rates than ordinary A/D and higher clock speed for digital circuits. It also means that the signal bandwidth sampled using oversampling technique has to be much lower than sampling rate.

While oversampling technique is able to reduce the random quantization by averaging such noise over a much wider sampling bandwidth due to high oversampling ratio, another useful scheme for quantization noise reduction is noise shaping using negative feedback. Considering the transfer function of first-order Sigma-Delta modulator (Figure 4.1) in (4.4), a negative feedback is added to stabilize the system containing an integrator.

For in-band signal $X(z)$, the system acts as a low-pass filter and the signal transfer function is nearly unity at low frequencies. Similarly noise signal $E(z)$ is approximately zero for low frequencies due to its noise transfer function is like a high-pass filter. Thus for the Sigma-Delta modulator, it is designed to have high gain for in-band signal in low

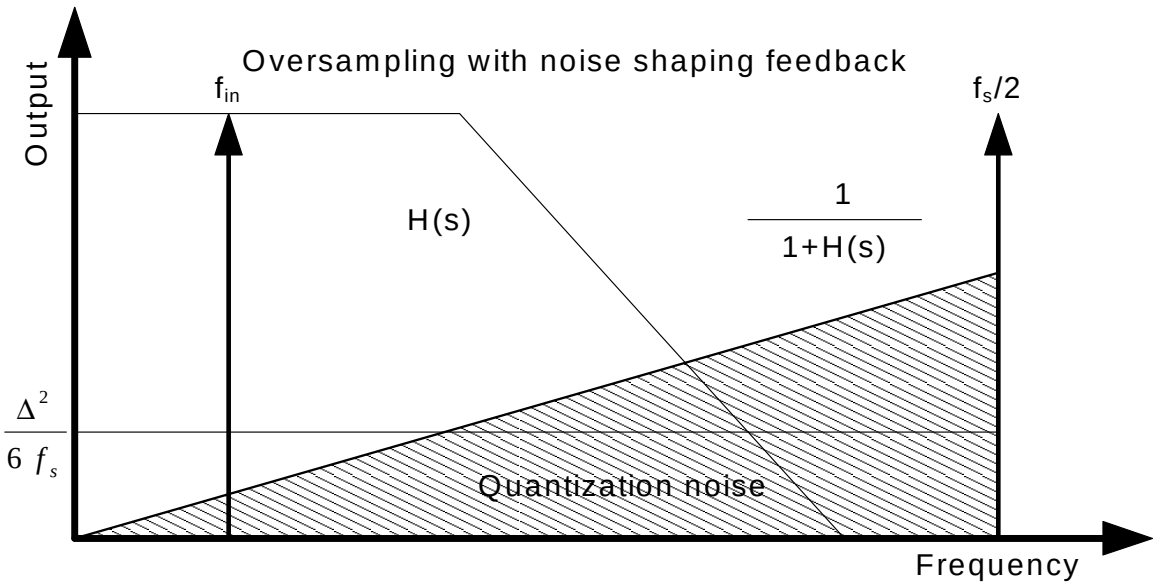

Figure 4.3: Oversampling system with noise-shaping feedback.

frequency band and for quantization noise in high frequency bands. It is apparent the output quantization noise is reduced in signal band, or *moved* into higher frequency bands as shown in Figure 4.3. The most troublesome noise is the close-in quantization noise since it is hard to remove using a low-pass filter. In an open-loop system without nose-shaping feedback as shown in Figure 4.2, the quantization noise is a white noise uniformly distributed from $0 \leq f \leq f_s/2$. With noise shaping technique in a close-loop system, the in-band quantization noise is high pass-shaped by the feedback loop, leading to lower in-band noise. Noting that the total quantization noise energy for both open-loop and negative close-loop system are same ($\Delta^2/12$), the noise distribution is changed as the quantization noise in Figure 4.3 is shifted to the higher frequency band and can be easily filtered.

Oversampling and noise-shaping techniques are related. While oversampling refers to sampling beyond Nyquist rate, noise shaping refers to shaping the noise spectrum to higher frequencies and thus lowers the noise in the signal band. Sigma-Delta modulation greatly enhances the oversampling effect by using feedback systems. The oversampling system

with Sigma-Delta modulation is often called a high-order oversampling system since the conventional oversampling system without Sigma-Delta modulation is, in fact, a zero-order feedback system [4].

4.2 Digital Filter

The output of Sigma-Delta modulator is a bit stream of '0' or '1' which contains high-frequency noise and cannot be directly processed by BIST control unit. A low-pass digital filter (LPF) is required to filter out the noise. We use a simple integrator at the output of Sigma-Delta modulator as LPF. It has been shown [33] that the z-domain transfer function of a modulator and integrator is given by,

$$Y(z) = \frac{z^{-1}}{1-z^{-1}}X(z) + E(z) \tag{4.11}$$

where $X(z)$ is Sigma-Delta input, $Y(z)$ is the integrator output and $E(z)$ is quantization error. Thus, the input signal is recovered and quantization error is not accumulated, improving the overall SNR. The final LPF output is then converted to usual digital code $\hat{k}$, corresponding to input stimulus k plus quantization error from both DAC-under-test and Sigma-Delta modulator.

Since the reference voltage is only about 3 LSB of DAC-under-test, the quantization error of Sigma-Delta modulator is much less than that of DAC-under-test and therefore can be ignored.

Since the oversampling technique distributes the overall quantization noise from bandwidth of f_0 to $f_s/2$ by the oversampling ratio f_s/f_0 and noise-shaping acts as a high-pass

filter for the quantization noise most which fall outside the signal pass band, the digital filter is actually a low-pass filter that eliminates the high frequency noise and keeps the low frequency signals.

One simple method to implement the low-pass filter to extract signals is to use an accumulator that sums up the output bit-stream of the sigma-delta modulator. This accumulator acts like a $1^{st} - order$ low-pass filter with a z-domain transfer function:

$$Y(z) = \frac{1}{1-z^{-1}} Y(z) \tag{4.12}$$

$$= \frac{z^{-1}}{1-z^{-1}} U(z) + E(z) \tag{4.13}$$

Examining (4.13), we find that the signals in the bit-stream are extracted by the accumulator and the high frequency noise shaped by sigma-delta modulator is very low in the band of interest and therefore almost eliminated. The remaining noise in the accumulator output is only due to the 1-bit quantization error (1 LSB) while the signal is reinforced during accumulation to achieve much higher SNR.

The bit-stream generated by the sigma-delta modulator requires a smoothing process called *decimation* that eliminates redundant output data by down-sampling the bit-stream to reconstruct the input signal without distortion. A down-sampling reduction ratio M means that the sampling rate of the bit-stream is reduced by a factor M, equivalent to picking up one of every M samples from the stream to reconstruct the input signal and discard the rest of the samples. No signal information will be lost during the down-sampling process provided that decimation data rate is more than twice the signal band width f_0. Digital filter using decimation will minimize the requirements for a high speed parallel multiplier and a large memory to store every bit of the lengthy stream. A common implementation

of such decimation is comb filter, or sometimes called *sinc* filter that will also eliminate the unnecessary high frequency portions of the bit-stream. Ong *et al.* [34] give an efficient implementation of a comb filter by cascading K stages of accumulators operating at the sampling rate of the sigma-delta modulator, followed by K stages of cascaded differentiators operating at the down-sampled rate. The transfer function of the sinc filter with K stages and a down-sample ratio M has the form:

$$H(z) = \left(\frac{1}{M} \frac{1 - z^{-M}}{1 - z^{-1}} \right)^K \tag{4.14}$$

with a frequency response:

$$\left| H\left(e^{j\omega}\right) \right| = \left(\frac{1}{M} \frac{\sin(\omega M/2)}{\sin(\omega/2)} \right)^K \tag{4.15}$$

The desired frequency components should be contained within the first peak of the frequency response. We also observe that larger K yields larger attenuation to frequency response and larger M yields more and thinner peaks so proper K and M should be chosen carefully to filter the desired frequency components to reconstruct the signal.

4.3 Summary

In this chapter, a first-order 1-bit Sigma-Delta modulation is described and the oversampling and noise-shaping techniques are introduced. Because of its simple architecture and high linearity, the Sigma-Delta modulator-based ADC is chosen as the best candidate for measuring-ADC, which requires low hardware overhead and higher linearity than DAC-under-test. With oversampling technique, the measuring-ADC can achieve higher

resolution by using greater oversampling ratio (OSR), which sacrificing conversion time for higher SNR and therefore higher resolution. Since measuring-ADC is only employed only once during testing steps and will be turned off after BIST and calibration steps finish, the conversion time is not a critical factor because it will not greatly impact overall performance of the mixed-signal system.

Chapter 5

Polynomial Fitting Algorithm

5.1 Overview

As our research has shown [25, 26, 27], a simplified polynomial-fitting algorithm [23, 24] can be employed for characterizing DAC/ADC by four coefficients that form a best fit 3^{rd}-order polynomial curve for the transfer function of the converters. The input code range of the DAC is divided into four equal segments as illustrated in Figure 5.1. For these segments, S_0, S_1, S_2 and S_3 are the sums of outputs corresponding the included codes. Syndromes, B_0, B_1, B_2 and B_3, are then obtained as specific linear combinations of the sums, and these allow the computation of four coefficients, b_0, b_1, b_2 and b_3, for a least mean-square fit of a third-order polynomial:

$$y(x) = b_0 + b_1 x + b_2 x^2 + b_3 x^3 \tag{5.1}$$

where x is the input code and $y(x)$ is the analog output of DAC.

5.2 Fitting Algorithm

This algorithm [23, 24] eliminates the requirement for massive amount memory to store individual sampled data as some schemes using histogram algorithms do. We apply this kind of third-order mean-square fit to the integral nonlinearity (INL) calculated as the

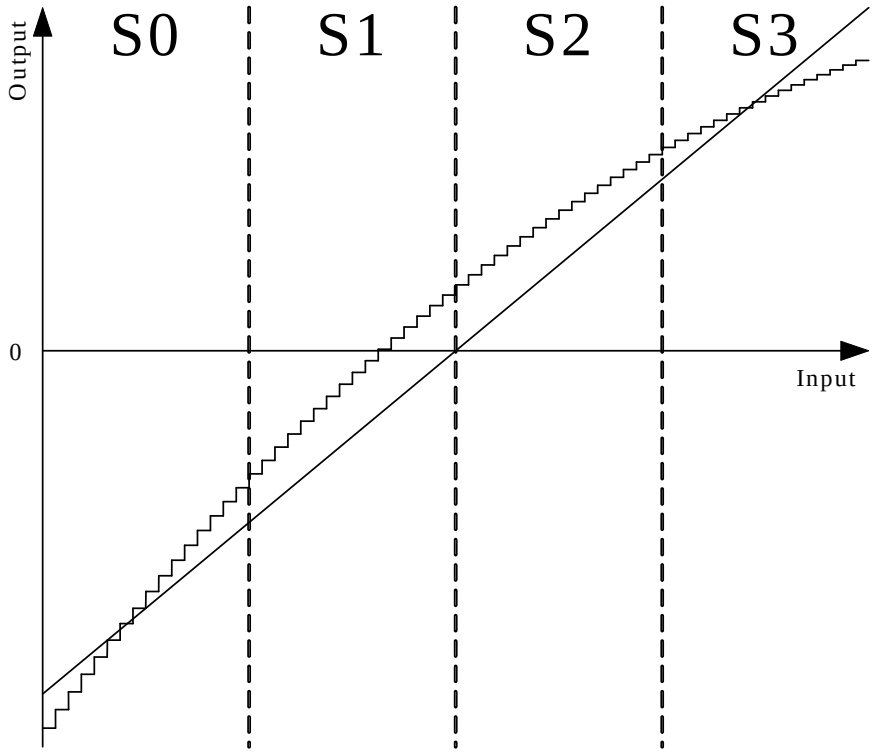

Figure 5.1: Polynomial fitting algorithm of DAC/ADC.

difference between the actual DAC output and the ideal output for all input codes. The proposed best fit polynomial algorithm is then used to check the functionality of DAC, as well as to control the dithering DAC to produce proper analog compensation signal for each code. However, it is also possible to apply the similar polynomial fitting algorithm to other order instead of three.

Zero-Order Polynomial

First of all, Zero-order polynomial will be tried, which is just mean value of all non-linearity errors of N-bit DAC in fact.

$$y = b_0 \tag{5.2}$$

$$b_0 = \frac{1}{2^N}\int_{-2^{N-1}}^{2^{N-1}} v_k dk = \frac{1}{n}\int_{-n/2}^{n/2} v_k dk \tag{5.3}$$

where $n = 2^N$ is the total number of input codes for N-bit DAC-under-test.

This polynomial is actually a constant value fitting for every input code. It has the least hardware overhead and delay for polynomial evaluation but may have the most fitting error.

5.2.1 Linear Fitting

The responses for input ramp codes is divided into two equal-length sections and two sums of these two sections can be obtained by

$$S_0 = \int_{-2^{N-1}}^{0} v_k dk = \int_{-n/2}^{0} v_k dk = \frac{n}{2} b_0 - \frac{n^2}{8} b_1 \tag{5.4}$$

$$S_1 = \int_{0}^{2^{N-1}} v_k dk = \int_{0}^{n/2} v_k dk = \frac{n}{2} b_0 + \frac{n^2}{8} b_1 \tag{5.5}$$

Then we define two syndromes for the first-order polynomial

$$B_0 = S_1 + S_0 = n b_0 \tag{5.6}$$

$$B_1 = S_1 - S_0 = \frac{n^2}{4} b_1 \tag{5.7}$$

Therefore, the first-order polynomial and two coefficients can be obtained by

$$y = b_0 + b_1 \cdot x \tag{5.8}$$

$$b_0 = \frac{1}{n} B_0 \tag{5.9}$$

$$b_1 = \frac{4}{n^2} B_1 \tag{5.10}$$

The two coefficients are proportional to offset and gain of the transfer function. Using linear fitting, high order harmonic distortions are discarded and so fitting error is large for DAC measurements. However, it is suitable for fitting ADC measurements because DSP can only get ADC outputs in the unit of LSB so high order distortions are already lost.

5.2.2 Second-Order Fitting and Third-Order Fitting

The responses are divided into three equal-length sections for second-order polynomial. Each of three sections are accumulated up to obtain three sums

$$S_0 = \int_{-n/2}^{-n/6} v_k dk = \frac{n}{3} b_0 - \frac{n^2}{9} b_1 + \frac{13n^3}{324} b_2 \tag{5.11}$$

$$S_1 = \int_{-n/6}^{n/6} v_k dk = \frac{n}{3} b_0 + \frac{n^3}{324} b_2 \tag{5.12}$$

$$S_2 = \int_{n/6}^{n/2} v_k dk = \frac{n}{3} b_0 + \frac{n^2}{9} b_1 + \frac{13n^3}{324} b_2 \tag{5.13}$$

We then define three syndromes for the second-order polynomial

$$B_0 = S_2 - 26S_1 + S_0 = -8nb_0 \tag{5.14}$$

$$B_1 = S_2 - S_0 = \frac{2n^2}{9} b_1 \tag{5.15}$$

$$B_2 = S_2 - 2S_1 + S_0 = \frac{2n^3}{27} b_2 \tag{5.16}$$

Therefore, the second-order polynomial and three coefficients can be obtained by

$$y = b_0 + b_1 \cdot x + b_2 \cdot x^2 \tag{5.17}$$

$$b_0 = -\frac{1}{8n} B_0 \tag{5.18}$$

$$b_1 = \frac{9}{2n^2} B_1 \tag{5.19}$$

$$b_2 = \frac{27}{2n^3} B_2 \tag{5.20}$$

The response is divided into four equal-length sections for third-order polynomial, as discussed in [23, 24]. The sum of each section is

$$S_0 = \int_{-n/2}^{-n/4} v_k dk = \frac{n}{4} b_0 - \frac{3n^2}{32} b_1 + \frac{7n^3}{192} b_2 - \frac{15n^4}{1024} b_3 \tag{5.21}$$

$$S_1 = \int_{-n/4}^{0} v_k dk = \frac{n}{4} b_0 - \frac{n^2}{32} b_1 + \frac{n^3}{192} b_2 - \frac{n^4}{1024} b_3 \tag{5.22}$$

$$S_2 = \int_{0}^{n/4} v_k dk = \frac{n}{4} b_0 + \frac{n^2}{32} b_1 + \frac{n^3}{192} b_2 + \frac{n^4}{1024} b_3 \tag{5.23}$$

$$S_2 = \int_{n/4}^{n/2} v_k dk = \frac{n}{4} b_0 + \frac{3n^2}{32} b_1 + \frac{7n^3}{192} b_2 + \frac{15n^4}{1024} b_3 \tag{5.24}$$

We can now define four syndromes as below (also same as in [23])

$$B_0 = S_3 + S_2 + S_1 + S_0 = n b_0 + \frac{n^3}{12} b_2 \tag{5.25}$$

$$B_1 = S_3 + S_2 - S_1 - S_0 = \frac{n^2}{4} b_1 + \frac{n^4}{32} b_3 \tag{5.26}$$

$$B_2 = S_3 - S_2 - S_1 + S_0 = \frac{n^3}{16} b_2 \tag{5.27}$$

$$B_3 = S_3 - 3S_2 + 3S_1 - S_0 = \frac{3n^4}{128} b_3 \tag{5.28}$$

Therefore, the third-order polynomial and four coefficients can be obtained by

$$y = b_0 + b_1 \cdot x + b_2 \cdot x^2 + b_3 \cdot x^3 \tag{5.29}$$

$$b_0 = \frac{1}{n}(B_0 - \frac{4}{3}B_2) \tag{5.30}$$

$$b_1 = \frac{4}{n^2}(B_1 - \frac{4}{3}B_3) \tag{5.31}$$

$$b_2 = \frac{16}{n^3}B_2 \tag{5.32}$$

$$b_3 = \frac{128}{3n^4}B_3 \tag{5.33}$$

These two polynomial fitting algorithms are used for DAC output fitting since the nonlinearities caused by process variation in DAC are of second or third order type in most case. So, employing a second or third order polynomial fitting algorithm may yield best results.

5.2.3 Higher-Order Fitting

Repeat the procedure above and we can obtain $N+1$ syndromes by dividing output responses into $N+1$ equal-length sections. And then $N+1$ coefficients for N^{th}-order polynomial can be calculated from these syndromes. In theory high-order polynomial may result in better fitting results. However, higher-order polynomial may have much greater penalty upon hardware overhead and delay, especially for high-order multiplies computation. We observed that N=3 is sufficient in most cases so there is no need to explore higher-order polynomial fitting equations.

5.3 Adaptive Fitting

We assume that the DSP and other digital circuitry have been tested and is fault-free. Before actual testing of on-chip DAC under test, a loopback as shown in Figure 3.18 is established. The DSP sends a series of random numbers through its output port and checks the input port for response. This step will detect any interconnect faults at DSP input/output.

If the inconsistency among test code and ADC responses is smaller than the fault-tolerance factor, the on-chip DAC-under-test (DUT) is considered fixable. Such inconsistencies between test code (k) and m-DAC response ($\hat{k}$) is actually the digitized and combined integral nonlinearity (INL) errors of both DUT and m-DAC.

$$INL_k = \frac{v_k - v_0}{LSB} - k = \hat{k} - k \tag{5.34}$$

where v_k is N-bit DUT output and the least significant bit (LSB) is the minimal unit voltage value for the DUT. For example, given reference voltage V_{ref}, LSB of 14-bit DAC is

$$V_{LSB} = \frac{V_{ref}}{2^{14}} \tag{5.35}$$

Because m-ADC is based on Sigma-Delta modulator and has high linearity with large OSR, the INL error of m-ADC can be ignored and thus $\hat{k} - k$ can be considered as the INL error of sole DUT for given code k. An adaptive polynomial fitting algorithm is employed to fit the nonlinearity errors (INL_k for each code k) of DUT to obtain the best-matching minimum degree polynomial for nonlinearity characteristics of DUT outputs.

Consider an order-p fitting polynomial:

$$y = b_0 + b_1 \cdot x + b_2 \cdot x^2 + \cdots + (p-1) \cdot x^{p-1} + p \cdot x^p \tag{5.36}$$

where b_0, b_1, b_2, ..., b_{p-1}, b_p are polynomial coefficients. Best-matching polynomial gives minimum mean-square error. To obtain the best-matching polynomial, we apply fitting to data for successively increasing degrees of polynomials. Although a higher order polynomial may have better fitting and lower error, it takes more time to calculate the coefficients, will require more memory to store and will need more complex digital circuitry for calculation. Thus, a higher order polynomial will require more gates and delay than a lower order one. Too high an order also brings meta-stability to system and negatively affects product reliability. Therefore, make trade-off between fitting accuracy and fitting time/hardware overhead. To make at-speed DAC correction possible, the maximum path delay of digital polynomial calculation circuitry must not exceed DAC conversion delay. So for given process and DAC design, maximum available order of polynomial shall be specified as well as fault-tolerance factor.

Accuracy of matching polynomial can be determined as the root mean square (RMS) error between measured INL errors and the polynomial values:

$$\Delta v_k = v_k - (v_0 + k \cdot LSB) \tag{5.37}$$

$$y_{rms} = \sqrt{\frac{1}{2^N} \sum_{k=0}^{2^N-1} (\Delta v_k - y(k))^2} \tag{5.38}$$

for N-bit DAC-under-test. In the proposed BIST procedure, a low-order polynomial fitting algorithm is used at first and then high-order ones, until the RMS errors drops below a specified threshold. For each polynomial, two steps are executed: coefficients extraction and polynomial evaluation. In coefficients extraction step, a series of consecutive ramp codes are generated as test patterns to DUT, then the Sigma-Delta modulator will measure DUT responses and DSP will collect both test patterns and DUT responses to calculate current polynomial coefficients for INL errors. In polynomial evaluation step, another series of consecutive ramp codes will be generated to evaluate the polynomial with calculated coefficients and obtain its RMS value for ramp codes. Thus the fitting accuracy of current polynomial to INL errors of DUT outputs can be defined as the RMS value. In real implementation, polynomial evaluation step of previous polynomial may be combined with coefficients extraction of next polynomial because these two steps will be using different hardware at the same time with possible race issue. The coefficients may also indicate if DUT is correctable by comparing to pre-defined values.

We use Matlab to simulate the proposed adaptive self-calibration approach. INL errors of a 14-bit DAC-under-test is shown in Figure 5.2 and we try various order polynomials to fit the INL errors, as shown in Tables 5.1, 5.2, 5.3 and 5.4.

Figure 5.3 compares fitting curves of those three polynomials and RMS errors of each order polynomials can also be calculated: 1.5188 for zero-order, 0.9643 for first-order, 0.8407 for second-order, and 0.0907 for third-order. It can be observed that third-order polynomial is the best match polynomial to fitting on-chip DAC in this case. It is possible that fourth-order polynomial may have better matching results but due to significant

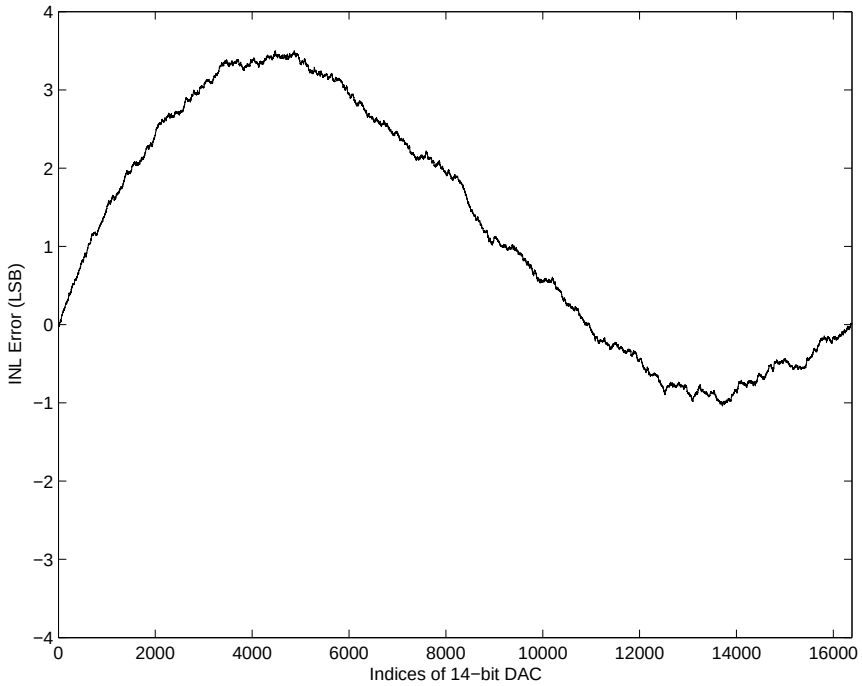

Figure 5.2: INL errors of a 14-bit on-chip DAC-under-test.

increase on hardware overhead and delay, fourth-order polynomial is not suitable in this case.

The d-DAC correcting outputs is shown in Figure 5.4 and final corrected INL error is shown in Figure 5.5. INL error is significantly reduced by our adaptive self-calibration technique, from $\pm 4LSB$ down to only $\pm 0.4LSB$.

Table 5.1: Zero-order polynomial fit for *INL* of Figure 5.2.

Sums	Syndromes	Coefficients
$S_0 = 1.9901 \times 10^4$	N/A	$b_0 = 1.2147$

Table 5.2: First-order polynomial fit for *INL* of Figure 5.2.

Sums	Syndromes	Coefficients
$S_0 = 2.054 \times 10^4$	$B_0 = 1.9901 \times 10^4$	$b_0 = 1.2147$
$S_1 = -645.4238$	$B_1 = -2.1192 \times 10^4$	$b_1 = -3.1578 \times 10^{-4}$

Table 5.3: Second-order polynomial fit for *INL* of Figure 5.2.

Sums	Syndromes	Coefficients
$S_0 = 1.3676 \times 10^4$	$B_0 = -2.2853 \times 10^5$	$b_0 = 1.7435$
$S_1 = 9.2011 \times 10^3$	$B_1 = -1.6649 \times 10^4$	$b_1 = -2.7910 \times 10^{-4}$
$S_2 = -2.9731 \times 10^3$	$B_2 = -7.6993 \times 10^3$	$b_2 = -2.3633 \times 10^{-8}$

Table 5.4: Third-order polynomial fit for *INL* of Figure 5.2.

Sums	Syndromes	Coefficients
$S_0 = 9.0857 \times 10^3$	$B_0 = 1.9901 \times 10^4$	$b_0 = 1.7672$
$S_1 = 1.1461 \times 10^4$	$B_1 = -2.1192 \times 10^4$	$b_1 = -6.5577 \times 10^{-4}$
$S_2 = 1.8845 \times 10^3$	$B_2 = -6.7893 \times 10^3$	$b_2 = -2.4699 \times 10^{-8}$
$S_3 = -2.5300 \times 10^3$	$B_3 = 1.7112 \times 10^3$	$b_3 = 1.0132 \times 10^{-11}$

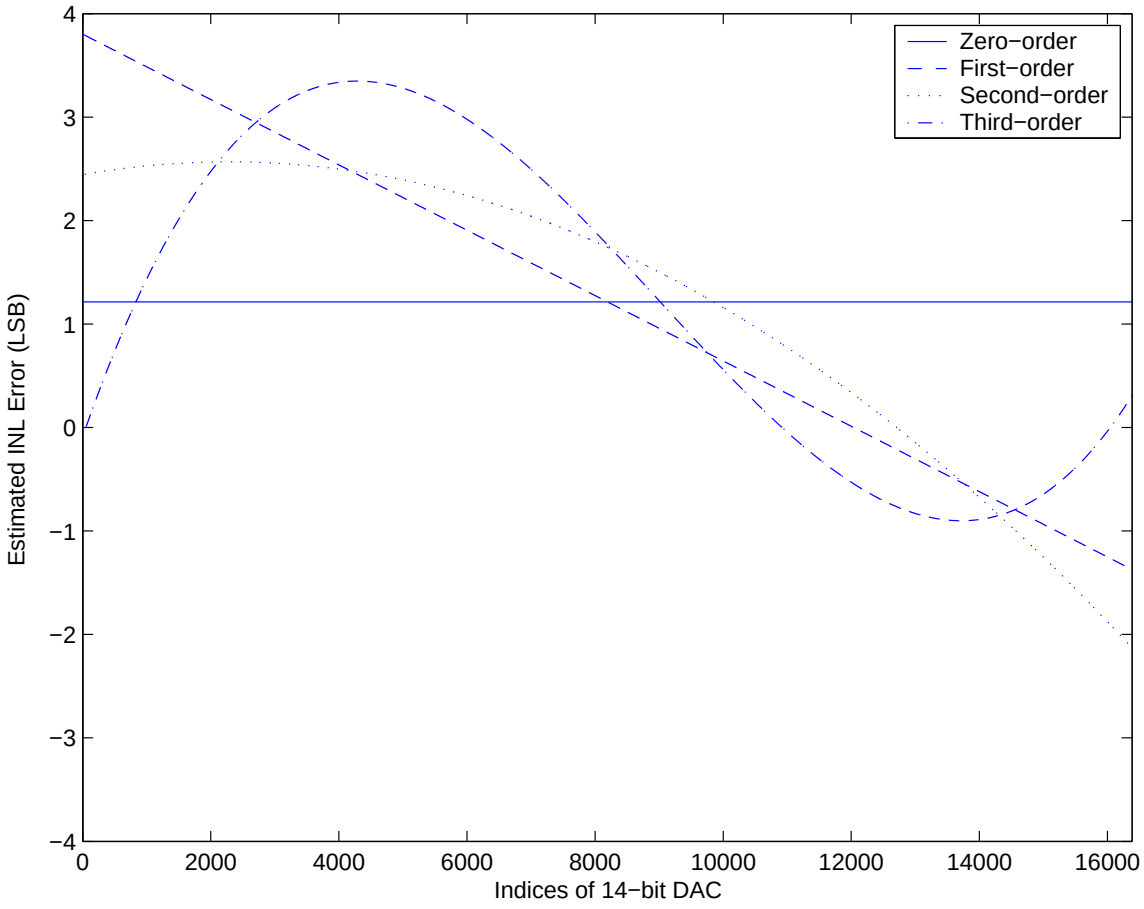

Figure 5.3: Fitting results from different order polynomials.

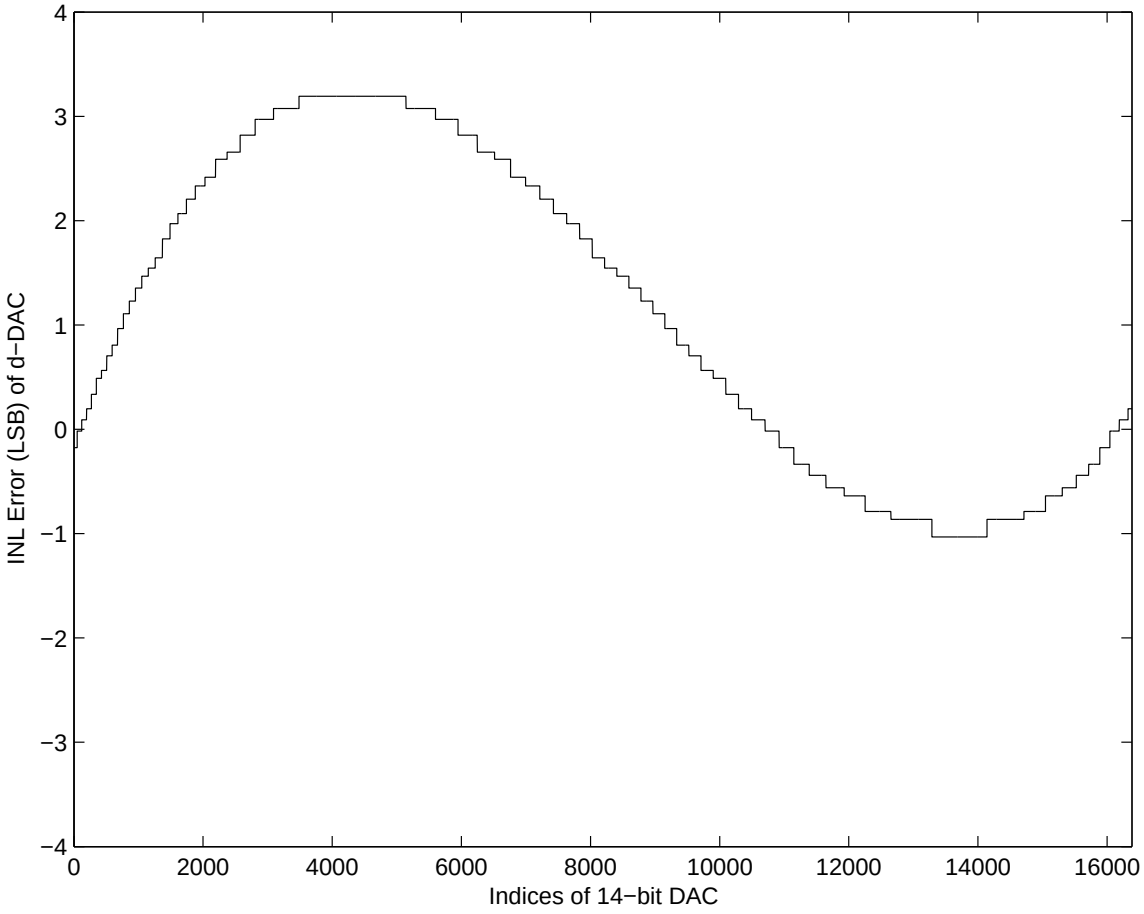

Figure 5.4: Correcting signals converted by a 6-bit d-DAC using third-order fitting polynomial.

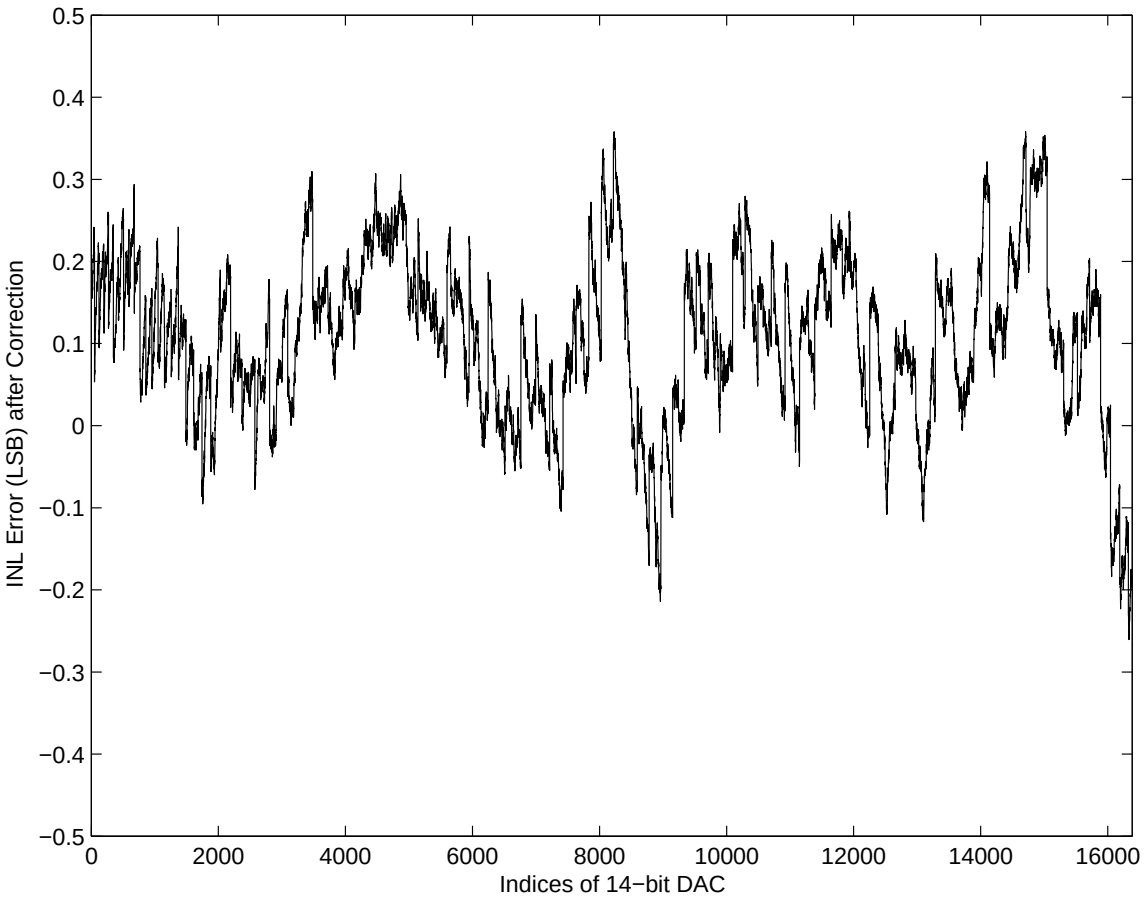

Figure 5.5: INL errors of 14-bit on-chip DAC corrected using 6-bit d-DAC.

Chapter 6

Conclusion

The proposed BIST and calibration approach is verified, simulated and implemented using tools such as Matlab, and Design Compiler. Matlab and SimuLink models are used to build a systematic simulation environment to test the feasibility of the proposed approach. Design Compiler is used to synthesize an implementation of polynomial evaluation unit since this single unit occupies most area overhead due to multiply-accumulate operation required by polynomial computation.

6.1 Truncation Error

Fix-point multiply-accumulate operation is used in the implementation because design of an IEEE-compatible float-point computation unit is too complicated and will take much larger silicon area. However, using fixed-point calculation brings another problem in addition to the existing nonlinearity errors that is truncation error. Given the fixed length of data word, the precision is limited and the rest will be discarded. Assuming N-bit word length, the range of the fixed-point number which a word may represent is,

$$-2^{N-1} \leq n < 2^{N-1} - 1 \tag{6.1}$$

For example, the range for a 10-bit word is -1024 to 1023.

Table 6.1: Truncation Error for 10-bit DAC. (All unit in LSB)

Word Length	Linear	Second-Order	Third-Order	Higher-Order
4-bit	64.296	77.474	84.6201	77.622
8-bit	3.2427	5.0105	5.8187	6.2390
12-bit	0	0.28352	0.37217	0.40544
16-bit	0	0.010821	0.023578	0.025812

Table 6.2: Truncation Error for 12-bit DAC. (All unit in LSB)

Word Length	Linear	Second-Order	Third-Order	Higher-Order
4-bit	255.30	309.60	337.97	354.91
8-bit	15.251	20.358	23.170	25.054
12-bit	0	1.2515	1.4993	1.6491
16-bit	0	0.070815	0.094711	0.10523

Table 6.3: Truncation Error for 16-bit DAC. (All unit in LSB)

Word Length	Linear	Second-Order	Third-Order	Higher-Order
4-bit	1023.3	1237.9	1351.3	1419.5
8-bit	63.252	81.181	92.521	100.141
12-bit	3.2405	5.1244	5.9794	6.5742
16-bit	0	0.31280	0.37720	0.42131
20-bit	0	0.017700	0.023781	0.026617
24-bit	0	0.00067559	0.0014819	0.026617

The truncation may affect the calibration results because it adds additional quantization noise into the DAC outputs that may exceed 0.5LSB limit. Longer word length is, fewer truncation error will be injected into the calibrated DAC outputs but at the heavy cost of hardware overhead. To get the optimal word length of polynomial evaluation unit, we simulate different cases with various DAC resolutions.

We can observe that while 12-bit fixed-point algorithm may be well fit for calibration of a 10-bit DAC (Table. 6.1), calibration of a 12-bit DAC (Table. 6.2 may need 16-bit fixed-point algorithm. For a 14-bit DAC, 16-bit fixed-point algorithm may be risky because the truncation error itself may bring about 0.37LSB into nonlinearity error of the final calibrated DAC output data, thus it could be better to use a 17-bit fixed-point algorithm.

Table 6.4: Hardware overhead of polynomial evaluation unit (in equivelant NAND gates and D flip-flops, respectively).

Word Length	Linear		Second-Order		Third-Order		Higher-Order	
4-bit	216	38	495	87	866	153	1329	235
8-bit	357	63	863	152	155	275	2334	430
12-bit	520	92	1281	226	2322	410	3642	643
16-bit	658	116	1646	291	3009	531	4743	837
20-bit	820	145	2064	364	3775	666	7218	1274
24-bit	959	169	2432	429	4464	788	8580	1514

6.2 Overhead

The hardware overhead of the proposed testing and calibration approach includes an analog signal generator (ramp signal generator), a measuring ADC (m-ADC, first-order single-bit Sigma-Delta ADC), a dithering DAC (d-DAC, low resolution low speed DAC) and a polynomial evaluation unit (PEU).

Among these components, PEU occupies the largest area due to its multiply-accumulate operation core. The ramp signal generator consists of only a few MOSFET gates and a capacitor, the Sigma-Delta ADC is first-order and contains only 1-bit DAC for quantization, and the dithering DAC is a low resolution low speed DAC which can be just a simple binary-weighted DAC with one resistor and current source for each bit. All other hardware overhead is ignorable comparing to the implementation of PEU.

A reference implementation is synthesized in TSMC 0.18un library using Synopsys Design Compiler, as shown in Table. 6.4. It clearly shows that 12-bit and 16-bit of word length suitable for implementation of third-order polynomial evaluation unit due to trade off between hardware overhead and truncation error.

6.3 Test Time

Although testing time of the proposed approach is not as critical as other factors like nonlinearity error, truncation error and hardware overhead, it is still worth estimation. The testing steps employed by the proposed approach only happens during chip power-up and they run only to characterize on-chip ADC and DAC, extract coefficients of fitting polynomials, verify the calibrated DAC and ADC. Thus the normal operation of ADC/DAC and other analog/digital circuitry in SoC system will not be affected by the testing time after test accomplishes.

Assuming on-chip ADC/DAC under-test is of N-bit resolution and their sampling and conversion time is T, oversampling ratio of m-ADC (first-order single-bit Sigma-Delta ADC) is M and d-DAC resolution is N', we get

$$T_{d1} = 2^N \cdot M \cdot T \tag{6.2}$$

$$T_{d2} = 2^N \cdot M \cdot T \tag{6.3}$$

$$T_{ad} = 2^N \cdot T \tag{6.4}$$

$$T_{da} = 2^N \cdot M \cdot T \tag{6.5}$$

$$T_v = 2^{N'} \cdot M \cdot T \tag{6.6}$$

where T_{d1} is the diagnosis time for analog signal generator and m-ADC, T_{d2} is the diagnosis time for d-DAC and m-ADC, T_{ad} is the testing time of on-chip ADC, T_{da} is the testing time of on-chip DAC, and T_v is the testing time for verification of calibrated ADC/DAC.

Thus the total testing time is:

$$T_{total} = 2^{N+1} \cdot T \cdot (M+1) + 2^{N} \cdot T \cdot M \tag{6.7}$$

To consider a typical case, let on-chip ADC/DAC resolution be 14 bits with a 10ns conversion time, OSR of m-ADC be 2000 and assume a 6-bit resolution for the d-DAC used for calibrating the DAC. Then, the total test time is 657ms.

6.4 Summary

A DSP-based adaptive self-calibration BIST scheme is proposed to test and diagnose on-chip DAC with best-matching polynomial fitting algorithm. A Sigma-Delta modulator-based measuring ADC is used to measure on-chip DAC outputs. The native nonlinearity errors of Sigma-Delta modulator are ignored by selecting sufficient oversampling ratio (OSR). The order and coefficients of best-matching polynomial can be calculated to retrieve nonlinearity errors as output correcting code. A low-resolution dither DAC is employed to convert digital correcting code to analog correcting signals for DAC output. This BIST scheme will be executed every time when SoC starts up to get up-to-date characteristics of on-chip DAC. The adaptive self-calibration approach has been verified by simulation and shows significant improvement of linearity for noisy on-chip DAC output.

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Appendices

Appendix A

Abbreviations

ADC	Analog-to-Digital Converter
ATE	Automatic Test Equipment
BIST	Built-In Self-Test
CUT	Circuit Under Test
d-DAC	Dithering DAC
DAC	Digital-to-Analog Converter
DFF	D Flip-Flop
DFT	Design For Test
DNL	Differential Non-Linearity
DR	Dynamic Range
DSP	Digital Signal Processor
DUT	Design Under Test
ENOB	Effective Number of Bits
FFT	Fast Fourier Transform
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
IM3	Third-Order Intermodulation
INL	Integral Non-Linearity
IP3	Third-order Intercept Point
ITRS	International Technology Roadmap for Semiconductors
JTAG	Joint Test Action Group
LPF	Low-Pass Filter
LSB	Lease Significant Bit
m-ADC	Measuring ADC
MATLAB	A high-level technical computing language from MathWorks
MOS	Metal-Oxide Semiconductor
MOSFET	MOS Field Effect Transistor
NBTI	Negative Bias Temperature Instability
ORA	Output Response Analyzer
OSR	Oversampling Ratio
PEU	Polynomial Evaluation Unit
PWM	Pulse-Width Modulation
RMS	Root Mean Square

SDFF	Scan D Flip-Flop
Simulink	A MATLAB simulation and design system from MathWorks
SINAD	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
SNDR	Signal-to-Noise-and-Distortion Ratio
SoC	System-on-Chip
THD	Total Harmonic Distortion
TPG	Test Pattern Generator

Appendix B

OSR and SNR of Sigma-Delta Modulation

Assuming a sufficiently high over sampling rate (OSR) such that $f_s^2 \gg f_0^2$, the rms noise magnitude in the signal band of a first-order Sigma-Delta modulator is,

$$n_0 = e_{rms}\frac{\pi}{\sqrt{3}}(OSR)^{-3/2} \tag{B.1}$$

The rms noise magnitude in the signal band of a second-order Sigma-Delta modulator is,

$$n_0 = e_{rms}\frac{\pi^2}{\sqrt{5}}(OSR)^{-5/2} \tag{B.2}$$

The rms noise magnitude in the signal band of a higher-order Sigma-Delta modulator is,

$$n_0 = e_{rms}\frac{\pi^n}{\sqrt{2n+1}}(OSR)^{-(2n+1)/2} \tag{B.3}$$

The SNR with oversampling and noise shaping can be found. The rms noise magnitude in the signal band of second-order Sigma-Delta modulator is,

$$SNR = 10\log\left[\frac{\frac{1}{8}\left(2^N-1\right)^2\Delta^2}{\frac{\Delta^2}{12}\frac{\pi^{2n}}{2n+1}OSR^{-(2n+1)}}\right] \tag{B.4}$$

$$= 10\log\left[\frac{3}{2}\cdot 2^{2N}\cdot SNR^{2n+1}\cdot\left(\frac{\pi^{2n}}{2n+1}\right)^{-1}\right] \tag{B.5}$$

where N is the resolution of quantizer and n is the order of the modulator. If we consider single-bit Sigma-Delta modulator then the expression of SNR can be simplified as,

$$SNR = 10\log\left(\frac{2n+1}{8\pi^{2n}}OSR^{2n+1}\right) \tag{B.6}$$

Further manipulation of the above expressions yields,

$$SNR = 6.02N + 1.6 + 3(2n+1)\log_2 OSR - 10\log_{10}\left(\frac{\pi^{2n}}{2n+1}\right) \tag{B.7}$$

The effective number of bits (ENOB) of a Sigma-Delta modulator with lowered quantization noise due to oversampling and noise shaping can be found as,

$$N_{ENOB} \approx N + \frac{2n+1}{2}\log_2 OSR - 1.66\cdot\log_{10}\left(\frac{\pi^{2n}}{2n+1}\right) \tag{B.8}$$