Reliability of Solder Attachment Options with Lead Free for 0.4 mm Micro BGA Packages

by

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Abstract

Electronic Modules have become an integral part in Automobiles. User friendly applications in Automobiles require high reliable electronic components to perform in harsh temperature ranges of -40 C to 165 C. Micro-electronic devices are often manufactured with operating conditions as a priority which is termed as “Design for Reliability”. This exponential rise in use of electronics results in dramatic increase in the use of electronics modules which fosters the development of use of materials that is very hazardous to human body and environment.

Solder joints in electronic packages give mechanical, electrical and thermal support to the overlying integrated circuits. Hence its reliability is also a major concern for the performance of electronic module. BGA (Ball Grid Array) are very common type of surface mount technology packages on electronic modules. In BGA packages, Solder balls are arranged in particular grid patterns which form the interconnection between chip and board resulting in High density Interconnections (HDI). Thus solder attachment reliability is a big concern to the functioning of whole electronic system.

Tin-Lead solders were initially used in the electronic industry, but later lead in the solders resulted in Lead poisoning, which was toxic to the human body. “Green Electronics” is gaining greater attention by the consumers and Environmental Protection Agency (EPA) whi ch includes the elimination of use of lead for soldering but many researchers believe this

transition into lead free electronics will take a long time for high reliability applications.

Successful performance of an electronic module is functions of reliabilities of all other components like solder material, resistors, and metal inter connections etc which perform at different temperature levels. Solder attachment reliability is defined as the ability of solder joints to survive planned design life of a given product. This research looks in to reliability of the solder attachment option in the test vehicles which are subjected to 4300 thermal cycles tracing a particular temperature profile and resistance is used a monitoring parameter for failure of components. This test is done with different Solder pastes and surface finishes which thus will have different solder attachment options and tested in thermal cycling conditions which relate to the actual scenario and will characterize its reliability.

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List of Abbreviations

OSP	Organic Solder ability Preservative
HDI	High Density Interconnections
HASL	Hot Air Solder Leveling
QFP	Quad Flat Packs
SnPb	Tin Lead
PBGA	Plastic Ball Grid Array
PCB	Printed Circuit Board
ImSn	Immersion tin

Chapter 1
Introduction

Moore's Law states that, "The numbers of transistors incorporated in a chip will approximately double every 24 months". This law characterizes the exact growth rate of electronic industry to the extent of Nano-electronics. The Figure 1 shows that trend predicted by Gordon Moore.

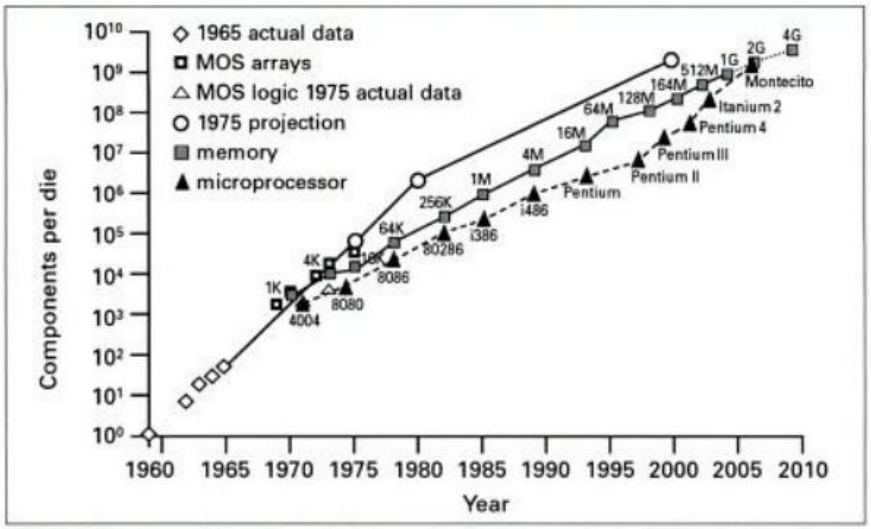


Figure 1 Integrated circuits complexity [52]

Thus there is a great demand for ultra fast and ultra portable electronic chips which will have superior functionality; this need has created a benchmark for electronic packaging industry for future generations. [43]. New materials, routing methods and process have contributed to Moore's predictions. Higher I/O connections and superior thermal dissipation are design hurdles for future packages and will affect performance of any electronic component; it has been targeted by packaging industry

for potential breakthroughs. An interesting co-relation has been noted many experts, with increasing transistor density the size of components is going down as shown in Figure 2.

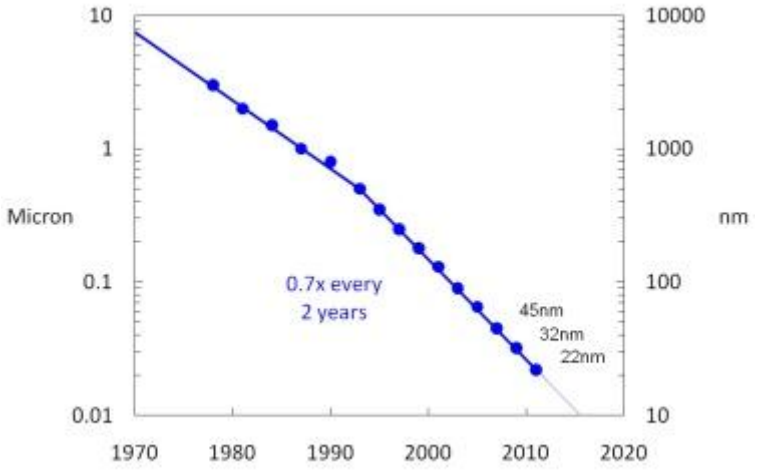


Figure 2 Decrease in Size of transistors [43]

Electronic content in automobiles has always been in an increasing trend. In the year 1977, the automobile had electronic content worth $110 and it is predicted in the year 2013 to have twenty-fold increase in terms of cost. The primary reason for this increase in electronic content is due to regulation of fuel economy and emission control by government.[51]. Modern automotive technologies like drive-by-wire, etc also require more high power electronic systems. This is need of high power in electronics demands better reliability in electronics.

1.1 Electronic Packages

The chip carrier holds the silicon chip inside it is termed as an electronic package. The chip carrier protects the silicon chip from humidity, assembly handling, isolation from shock and vibration and provides interconnection of the circuits on the chip. The chip carrier has pins, leads or pads on the under side which serve as solder joints.

Thus package design is very important as it affects chip performance and functionality.

Electronic Packages are primarily classified as through hole and surface mount packages. Through hole chip carriers have leads inserted into holes in the circuit board. After insertion, the leads are bent inwards and cut. Thus the solder joints are formed which mechanically support the package to the circuit. Then, solder joints are wave soldered to make a permanent connection.

Main difference between these two types of chip carriers is in the type of leads used for I/O connection from the carrier. Surface mount type can be further classified into three types, J leaded, leadless and Ball Grid Array (BGA). There are also many other types of Surface mount packages with specific advantages and disadvantages as described in the table 1

Characteristic	QFP	BGA	CSP	Wafer-level CSP	Flip-Chip
I/O density	-	-	+	+	++
I/O pitch (mm)	1.27-0.4	2.5-0.8	0.8-0.5	0.8-0.5	0.5-0.070
Size	– –	–	+	++	++
Electrical and thermal behaviour	– –	– –	+	++	++
Underfill	no	no*	no*	no*	yes
Re-workability	++	++	+	+	– –
Reliability	++	+	+	+	++
Die protection	++	++	++	+/-	+
Handling	++	++	+	-	-
Electrical testing	++	++	+	+	-
Commercial availability	++	+	+/–	+/–	–
Cost	+	-	– –	+	+
Compatibility with IC design	++	++	+/–	+/–	–
Compatibility with standard reflow	++	+++	+	+	– –

Table 1 Comparison of different Surface mount type packages [48]

1.2 Solder Interconnections

The connections from the chip carrier are termed as first level of solder inter connects. [7]. Considerable number of chips are placed on circuit boards and connected together (Second level of solder interconnects). Several Printed Circuit boards (PCB) are stacked together to form a panel and the connection between each PCB is termed as third level of solder interconnects.

Solder joints are metallic solder connections that is formed between the semiconductor package and a substrate board. This can be achieved by wires or solder balls .Thus solder balls, solder bumps etc are termed as solder joints. Ball grid arrays (BGA) have solder balls on the bottom surface to provide metal interconnections.

BGA ‘s provide a substantial advantages in assembly process due to its larger pitch, compatibility with existing standard surface mount PCB assembly equipment etc in contrast to fine pitch BGA assembly.[20] Solder joints also give mechanical strength to support the overlying chip, electrical transmission to substrate and give heat dissipation.

Lau describes the various loads that act on a solder joint alone or in combination include:

- Cyclic differential thermal expansion
  - Differences in Co-efficient of thermal expansions between the substrate and board results in shearing of solder balls
- Vibration
  - Transportation and mobile use

- Thermal Shock
  - Rapid temperature changes every time electronic modules go through one operating cycle.
- Mechanical Shock
  - Extreme temperature conditions and accidents

Thus solder joint reliability and durability is the biggest concern for electronic packaging industry. Some of major advantages in BGA's include have a very good I/O count, better yields can be achieved during manufacturing process, no co planarity problems etc. A Ball grid array with a flip chip (Chip Scale Package) will great enhance heat dissipation.[7]

Solder joint fatigue is one of the most common failure mechanisms in electronic packages when exposed to thermal cycling tests. Co-efficient of thermal expansion (CTE) values also forms a major part in fatigue failure mechanisms in electronic packages. Therefore, solder ball reliability become one of major aspects of research interest in electronic industry.

1.3 Lead free solder and its characteristics

Eutectic Sn 63% Pb 37% has been the most widely used solder material since the advent of electronics due to its cost, availability, ease of use and its solder characteristics like low melting temperature and sustainability in reflow ovens and wave soldering processes.(43).

Environment Protection Agency (EPA) has ruled out lead as one of the most harmful elements to human body. Most electronic wastes (e-wastes) are not treated

properly and end up in landfills which destroy our natural ecosystem. European Union (WEEE) is one of the major supporters for lead free electronics.

Lead free solders have different physical and chemical properties in contrast to conventional Sn-Pb based solder. Thus they pose certain criteria which they have to satisfy in order to be implemented in industries. Dr. Shangguan's systematic and holistic approach to lead free soldering is as shown in Figure 3.

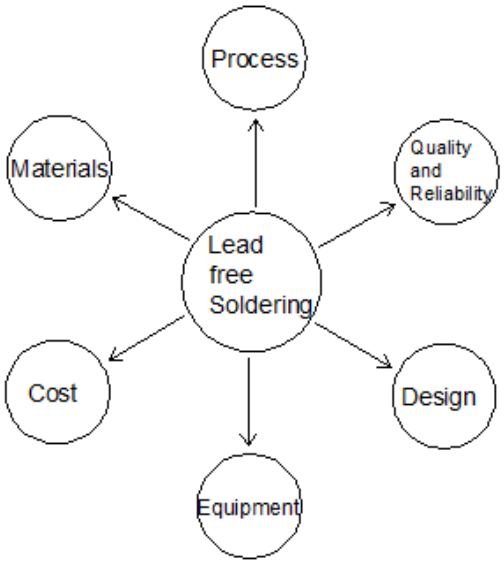


Figure 3 Lead free soldering – a holistic approach[45]

We know that design and construction of boards affects solder joint reliability but assembly process also has it effects on solder joint reliability [46]. Solder pastes on exposure to air for a prolonged period to time losses its tackiness. Hence assembly process has to modify according to this requirement. Similarly, Flux holds the solder joints before reflow process and hence its exposure will result in tackiness problems. Shangguan believes that all the above considerations shown in the Figure 3 has to be satisfied by the alternative lead free alloy and it is critical to successful business

implementation.

There have been numerous replacements materials for tin-lead solder which include Sn-Cu, Sn-Ag-Cu, Sn-Bi, Sn-Bi-Zn. The table 2 below shows various lead free alloys classified on its purpose

Wave soldering	Sn-Ag family
	Sn-3.5 Ag
	Sn-(3-3.9) Ag- (0.5-0.8) Cu
	Sn-Cu family
	With some additions of Ag,Au,Ni,Ge etc
Reflow Soldering	Sn-Ag family
(Higher Temperature)	Sn-3.5 Ag
	Sn-(3-3.9) Ag- (0.5-0.8) Cu
	Sn-(2-4)Ag-(1-6) Bi
	With 1%- 3% In
Intermediate Temperature	Sn-Zn family
	Sn-9Zn, Sn-7Zn-Al
	Sn-8Zn-3Bi

Table 2 Different Lead free alloys [45]

Eutectic Sn-Ag alloys has many disadvantages but addition of copper to Tin-Silver solder will remove certain limitations and yield results like (Suganuma)

- Lowering of the melting point
- Better wettability performance
- Thermo mechanical performance improvements

Sn-Ag-Cu (SAC) leads as an effective replacement solder material due to its ability to produces highly reliable solder materials in accordance to the above disadvantages.[fujiunchi]

Yi et al discuss manufacturing difficulties of SAC in contrast to conventional

Sn-Pb alloy. They compare both these alloys in terms of wet ability and printability performance that resulted due to manufacturing process. In order assess SAC's wettability and printability performance, Yi analyzed test vehicles of different combinations of Surface finishes and Solder pastes. Test vehicles included Quad flat packages (QFP) with 0.3mm, 0.4mm and 0.5mm pitch and Chip Scale Packages (CSP) with 0.4 mm, 0.5mm and 0.6 mm pitch. On measuring different solder spreads and wetting angles on solder balls in every combination using X-ray, Visual Inspection methods etc, Yi et al concluded that SAC will sustain as an effective replacement for Sn-Pb solder with minor changes in process parameters. It was also been found that reflow process windows was narrower for SAC in comparison to Sn-Pb.

1.4 Chip Scale Packages

As electronic industry is going towards High Density Interconnections (HDI), Chip Scale packaging technology is gathering attention over conventional area array packages. Chip scale packages is said to be no larger than 1.2 times the size of the die.[43].

Chip scale packages have ease handling, test, assembly and rework. Chip Scale Packages are smaller than BGA. Chip scales packages have higher I/O ratios, it is mainly due to BGA pattern on the underside.

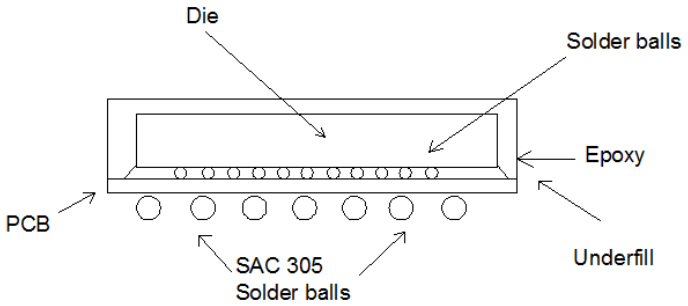


Figure 4 Chip Scale Packages [7]

The above Figure 4 shows a wire bonded chip scale package. The molds (plastic encapsulation) give mechanical protection to the wires and die. The die is attached on the interposer board. The die can even be attached with solder bumps instead of wires. Solder balls are attached to bottom side of interposer board as a final step. MicroBGA is a good example for Chip Scale packages as chip size is directly related to packages size.

There are four different types of Chip Scale Packages[58]

- Rigid Interposer
- Flex Interposer
- Lead Frame Interposer
- Wafer level Assembly/Wafer Scale

CSP packages are very small; this helps in a lot of ways to improve overall reliability of the package. Smaller packages means thinner substrates, hence the CTE mismatches would not be huge problem. Also under fill between BGA balls and substrate absorbs CTE mismatches, which would improve overall reliability.

Reliability affects cost; a bad product would incur costs interms of rework and

repair to keep it sustainable over its product life. Also, if solder joint cracks or fails, component related to it will not function, thus reliability of the entire system is questioned. Thus production of reliable electronic equipment requires excellence in many aspects like designing against failure, and Process variability of manufacturing process. To design against failure, correct materials, correct techniques, design for thermal management and packaging rigidity against environmental impacts have to be considered. Solder joint fatigue is one of the major factors affecting reliability.

There exist different methodologies like Area of the Spread test, Surface tension balance test etc for testing solder joint reliability depending on the characteristics being evaluated. Accelerated Thermal Tests mimic actual service life of an electronic component thereby it is useful to evaluate its effective functionality. It exposes the electronic package to different temperature ranges. Data exists for conventional SnPb solder on thermal cycling and its effect on solder joint reliability as it has been in use for the last twenty years. SnAgCu(SAC) solder has different characteristics in comparison to conventional tin-lead solder and with development new process techniques, its reliability has to be characterized.

Chapter 2
Literature Review

Research and development in the field of micro electronic devices is fueled by the desire to make them smaller and faster [27]. These two attributes leads to high electrical power consumption which results in increased temperature levels resulting increased stress levels in the electronic modules. In higher temperatures, solder ball interconnections in BGA packages are subjected to high thermal stresses which thereby affect the performance of the electronic module

Electronic components can fail due to multiple reasons like product design issues, differences in thermal expansion co-efficient, working environments and its related stresses that can lead the cause.

The main element that differentiates harsh environment electronics from consumer electronics is the operating environment in which they perform. The table 3 below shows the thermal operating environments for various electronics in different fields

Electronics	Operating Temperature
Consumer	0 C to + 70 C
Industry	-40 C to 85 C
Automotive	-40 C to +125 C
Military	-55 C to +125 C

Table 3 Thermal operating Environments [49]

These elevated operating temperatures pose thermal management problems for electronic devices which could be have catastrophic results. Electronic devices in Automobiles operate in a very harsh environment due to engine vibration, dirt, chemicals, petroleum vapors etc with addition of thermal management problems that arise due to under the hood air flow. Thus reliability and durability of electronic products are main concern for Automotive Manufacturers.

2.1 Lead free solder

Environmental Protection Agency has concluded lead as one of the top 17 chemical posing the greatest threat to human life and environment. Lead free soldering is going through a major change from research and development to actual implementation in products owing to the fact that it had gained appreciation from consumers and major support from electronic industries in Japan and Europe. Over the years, electronics industry had tried to find a suitable replacement and many materials like Bismuth, Silver had been suggested as a replacement material. The replacement material should satisfy all important physical properties like Mechanical

loading, Electrical Conductivity, Melting temperature, Thermal Conductivity, Co-efficient of thermal expansion and Elastic modulus [3][5] and other important characteristics like Cost[6], Toxicity, Manufacturability, Design flexibility and availability of new solder material etc. Co-efficient of thermal expansion is a big concern for “Under the Hood” transportation applications as metals expand in heat, giving rise to unequal stressed areas which can cause failure in metal connections of solder balls [8]. Melting temperature of solder should be higher than operating range of the equipment in order to prevent metal liquefaction. Electrical and Thermal Conductivity are directly related to the performance of electronic module.

Suraski and Seeling [6] point out on Cost and Reliability of the new solder material as a major problem to implement lead free soldering in all industries as lead is the least expensive material in the world and different combination of materials achieved certain properties like lower creep strength [9] but lack certain properties like Mechanical Strength, Higher elastic modulus [6][9], it was not at all possible to find the one suitable replacement material to lead in tin-lead solder because of its excellent properties. [4][7].

Tin-Lead Soldering has been practiced by micro-electronic industry for a long time hence Suraski and Seeling [6] believe lead free soldering changes will take a long time to come into effect as lot of analysis has be done on lead free solders before implementing this major change.

Solder wetting dynamics is a crucial parameter as it determines the solder joint performance Solder wetting is a function of various phenomenon like surface tension

imbalance, viscous dissipation, molecular kinetic motion, chemical reactions and diffusion[13]. Kang et al empirically formulated that wetting dynamics is a function of temperature, solder material and substrate metallization. Temperature has a drastic effect on solder joint formation i.e. a low reflow temperature will lead to incomplete melting of the solder sphere and have deteriorating effect on solder joint reliability and a higher reflow temperature will lead to brittle solder joint.

Solder Pastes are homogeneous mixture of solder powder and flux. Lau describes that solder pastes involve several scientific disciplines like metallurgy and particle technology, Chemistry and physics, rheology. Solder pastes are the connecting medium for most surface mount technologies. Solder pastes are generally deposited using stencil printing process [28]. They are usually composed of solder powder, flux, viscosity control agents and a solvent system. Stencil printing of solder pastes is a very important and critical stage as only precise placement would bring permanent metal connection during reflow conditions. A big proportion of all SMA defects are attributed to the stencil printing process.

New legislations of lead free solder are going to pose a challenge to stencil printing process as solder paste medium density changes from leaded to lead free. Nguty believe that most defects occur after reflow and defect rates can be controlling process parameters i.e within the process windows.

An experiment was conducted by Nguty with different lead free solder pastes, stencil pitch and printing process parameters to study their various interactions. To examine the effects of these parameters, solder paste height was determined to be the

statistical process control parameter. It was found that lower the metal content in solder paste, shorter was the solder ball and tighter will be the process window. Thus solder paste selection will greatly influence stencil printing process parameters which in turn affect reliability.

SAC 305 contains 96.5 % tin 3% and 0.5% of copper. Reliability of a solder joint is combined result of Aging, mechanical and thermal stress withstanding capacity. [31]. Svecova et al claim that both lead and lead free solder pastes have similar mechanical and electrical properties. Even though they have similar properties, effective functioning of lead free solder in real world is still being researched. An experiment was conducted to test reliability of SAC 305 with variable base metal thickness and different surfacing methods. Test boards were thermal cycled between 0 C to 100 C. From the test results they found that Immersion tin had the least reliable surface fitting. Copper oxide formation on pad surface had caused reliability issues.

2.2 FR 4 laminate

FR 4 is a laminate is a composite mixture of epoxy resin with woven fiberglass reinforcement and widely used printed circuit board (PCB) material. The woven fiberglass particles give mechanical support to laminate and resins are used as a cementing material. Peak temperatures of lead free solders during reflow conditions are higher compared to conventional tin-lead solders. Sanapala[32] et al believe that this peaking in reflow condition for lead free alloys will affect the material properties of FR-4 laminates and hence affects reliability.

The laminates manufactured for this experiment were classified on the basis of

glass transition temperature. Glass transition temperature is the temperature at which solid glass particles transform into compliant state. The boards are classified as high T_g (T_g < 165 C), mid T_g (140 C < T_g < 165 C) and low T_g (T_g < 140 C). Every classified group had subgroups which had different grouping agents, fillers and flame retardants. All these boards were exposed to three different reflow profiles with different reflow ageing rates.

All laminates have a more or less similar glass transition temperature in spite of different curing materials, fillers and flame retardants. It was also proved that material with higher glass transition temperature had lower CTE which may be a result of high cross-linking density in the epoxy resin. Filler materials have lower CTE values when compared to without filler material. Thus reflow profile does affect certain mechanical properties of FR 4 laminates and this study has given a scientific way to choose the correct substrates.

2.3 BGA Reliability

BGA packages were developed to satisfy certain major requirements like High I/O numbers, high density and high robustness [7]. BGA packages possess solder balls on the entire bottom of chip and form the metal contact between the chip and substrate [7]. With need of having circuit boards smaller, underside of BGA packages should also be made smaller. This need has lead advancements of BGA technology over the years, as shown in table 4.

BGA	2001	2003	2006
Max. lead count	900	1000	1200
Max. # rows	14	15	16
Min. lead pitch (mm)	0.75	0.75	0.5
Min. ball diameter (mm)	0.4-0	0.4-0	0.3
Max. body size (mm)	35	38	42
Max. seated height (mm)	2.0	1.5	1.3
Co-planarity (μm)	100	80	80
Cost (Euroct/pin)	0.9	0.8	0.6

Table 4 Improvements in BGA Packages [48]

As integrated circuits become smaller and smaller, their reliability is questioned due to factors like electrical power consumption, heat dissipation etc. Material properties would have a greater impact on the solder attachment option and reliability function of the electronic module.[9].

Syed[24] formulated a design of experiment and numerical analysis approach to predict the effect of design parameters and their interactions on thermal fatigue on solder balls in an automotive 'under the hood' applications. The design parameters are substrate thickness, pitch, solder pad size and the type of array used. Thermal cycling Tests were done with three different profiles with extreme temperatures in the range of -40 C and 125 C and with three BGA configurations: standard, perimeter and thicker substrate board.

The standard BGA had a solder ball array of 15 x 15 at 1.5 mm pitch and with substrate thickness of 0.36 mm. Thicker Substrate board is same as that of standard BGA but with a increased substrate thickness of 0.76 mm. All of these BGA's are solder masked defined and were assembled on a 1.575 mm thick FR 4 PCB.

Thermal test results proved that perimeter type and thicker substrate board had better solder ball fatigue life. CTE gradients are reduced significantly due the thicker substrate boards and also the boards directly under the die are subjected more shear stress than the solder balls on perimeter. A design of experiment model was formulated to study individual contribution and their interactions. From the results it had been found that substrate thickness is the main effect and will have twice the fatigue reliability with improvement in substrate thickness [24][25]. Also larger pad sizes on the package side and smaller ball pitch improve the load bearing area and the solder joint fatigue reliability by 5 times.

2.4 Flip Chip

Flip technology has been favored by the electronic industry due to its miniaturization capabilities when compared to conventional ball grid arrays. With miniaturization, CTE mismatches, Excessive Intermetallic compound formations, thermal dissipation problems etc arise. Mass production of Flip chips faces the biggest problem of the need to develop a low cost bumping process.

Many researches [34] [35] [36] have conducted various experiments to improve the overall reliability of Flip chips through various improvements in substrate technologies and under fill properties. Braun et al focus their paper on failures that occur due to CTE changes and due to effects of interconnection technology advancements in thermal cycles. Material properties change with temperature, precisely speaking this minute change in material properties could contribute to cause of failure.

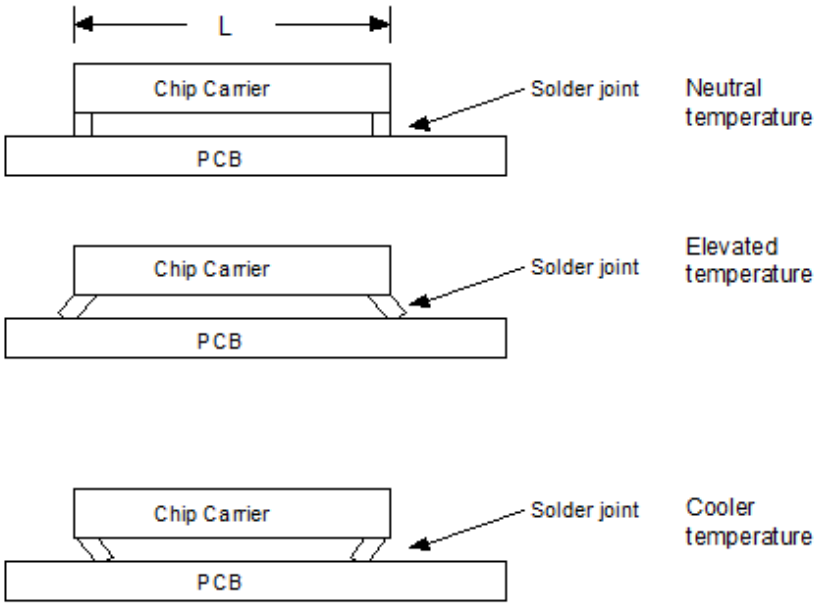


Figure 5 Effects of temperature on solder joints

The bending effect of package as shown above in Figure 5 is caused to very high CTE differences between board and substrate. Thus shear stresses act on the solder balls leading to war page and leading to crack formation at solder interface, thus leading to failure..

Developing lead free solder bump cannot be quantified as similar process to eutectic tin-lead solder. Also reliability prediction of lead free is more complex than tin lead alloys.[33] Zhao et al conducted a study to analyze failure mechanisms in lead free and eutectic tin lead solder for flip chip assemblies with optimization of material and process as prime requirements. Three different types of solder bumps were formed on the same die and the same package to study effects of solder alloy, process and under the bump metallurgy on failure mechanisms. Three types of solder balls are 63Pb/37Sn screen printed bump with UBM composition of Al/NiV/Cu,

63Pb/37Sn electroplated bump with UBM composition of Ti/Cu/Ni, Sn/Ag4/Cu0.5 screen printed bump with UBM composition of Al/NiV/Cu.

The bump pad pitch was 200 micrometer and a final pad diameter was 120 micrometer. The dimensions of the test chip were 15mm x 15 mm x 1.7mm thick fcBGA and the BGA substrate was a 4 layer laminate with 196 solder balls. All solder pads were coated with Organic solder ability preservative.

All the boards were high temperature aged to accelerate intermetallic growth in the interface region. To analyze the failure mechanisms, they are thermal cycled between 55 C to 125C with 2 cycles per hour. Most literature claim that eutectic tin lead solder performace would better than SAC alloys. Thermal cycling test also proved that electroplated SnPb bump had the best performance and printed tin lead bump was better that screen printed SAC. Cross section analysis on SAC alloys relieved that crack formation at Intermetallic surface is the primary failure mechanism.

2.5 Solder joint Reliability

Solder joint reliability is a function of many factors. Surface finish is one of the factors that have direct effect on solder joint reliability as solder joint interfacial reaction changes with different options. Electronic packaging industry is leading the change from tin lead to lead free alloys and hence it is very important to characterize effects of surface finish on lead free alloys. Need for good surface finish for lead free alloys has been an important requirement since it has been found Hot Air Solder leveling(HASL) has smoothness issues**.**[Shangguan]. Zheng[37] et al studied effect

of surface finish on solder joint reliability for SAC 305 alloy by isothermal aging four different surface finished boards at 125 C. Electroless Nickel and Immersion gold(ENIG),Organic Solderability Preservative, Immersion Silver and Immersion tin were the four different surface finishes that were analyzed. Intermetallic compound formation surface morphology was analyzed using SEM to study microstructure changes.

Quad flat packs (QFP) of 100 pins with 0.5 mm pitch, resistors and SAC solder balls with different solder finishes were used to study different solder joints during isothermal aging. From the test results, there has a development of cobble like Cu6Sn5 layer on OSP, ImAg and ImSn and this layer thickness increases with isothermal aging. Various other test like low speed full test and high speed shear strength of solder balls were conducted to analyze tensile and shear strengths of solder balls.

Manock [38] et al studies the effect of thermal cycle parameters on the SAC solder joint reliability. Mancock et al study the effect of dwell time on SAC solder joints with a 35x35mm PBGA package with 1.0 mm solder ball pitch. All boards were thermal cycled from 0°C to 100°C with10 minute ramp between extreme temperature0, 30, or 60 minute dwells at each temperature extreme or -40°C to 125°C with 15 minute ramp and 15 minute dwell.

Thermal test cycles show that SAC performance is better than tin-lead solders at short dwell time but its performance gradually decreases with increased dwell time. The primary reason of failure is CTE mismatches between PBGA and substrate,

resulting shear stress on solder balls.CTE mismatches are function of temperature and hence dwell times indeed affect solder joint reliability

Sattiraju et al conducted an analysis to find the relation between wetting dynamics and surface finish. The experiment was conducted with five different surface finishes like immersion Sn, organic solderable preservative (OS€'). electroless Ni/immersion Gold, immersion Ag and electroless Pd. All these surface finished boards were analyzed for wetting forces when subjected to solder baths. The joint between molten alloy and board finish occurs with various forces like buoyancy force of solder and downward surface tension forces interacting with each other. It was found the immersion tin had a highest wetting force (highest tendency to wet) and OSP had the lowest recorded wetting forces. It was also included that reflowing in Nitrogen does not affect the wetting behavior much.

Micro-vias are defined by IPC-2315 and IPC-6012A standards, as a blind and buried vias that are equal to or less than 6 mils (152 microns) in diameter and have a target pad equal to or less than 14 mils (356 microns).[20] IRTS also estimates that micro via diameter will reach the order of 18 microns by the year 2010. Microvias play a major role in high density interconnections. As the size of micro via gets smaller and smaller effects of plastic strain will be predominant because the wall thickness correspondingly reduces in size which will increase the strain effects that hinders its reliability. It is not only the size of the microvia but also the wall angles that greatly impact reliability. [50].

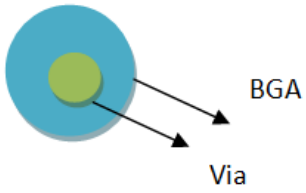


Figure 6 Microvia in pad design

High Density Interconnections requirements are primarily fueled mass-miniaturization in the field of electronics. Mircovia-in pad technology greatly improves in providing electrical connection in ultra small components. Micro via in-pad design indirectly affects the reliability characteristics of electronic package. Many researchers have found that microvia-in pad design often produces solder joint voids due to entrapment of air/gas during reflow [21]. If the entrapment of gas is large enough, would hinder reliability because of void formations. There are also other contributing factors like board thickness, board finishes, filling material etc which also affect solder joint void formation. [20]. Copper filled microvias has been found to be giving the least voiding effect than any other material [21] and also believed to have a positive effect on CTE co-efficient, thus providing thermal relief [23].

Unfilled microvia's are known many assembly issues as they deplete above lying solder resulting in a improper joint[23].Also probability of void formation greatly increases in the case of unfilled microvias due to large entrapment of gas below.

2.6 Intermetallic growth effects on Solder joint reliability

During reflow soldering process, intermetallics are formed between solders and substrate. Formation of intermetallic compounds between solders and substrate

ensures good metallurgical connection i.e proper wetting has taken place. Intermetallic growth occurs as a result of diffusion of atoms in to another through crystal spaces that have been created by voids, oxidized layers etc. The growth of intermetallic layer is affected by factors like peak reflow temperature; service conditions etc and will greatly influence the solder joint reliability [15]. Intermetallic compounds are brittle in nature and hence if they occupy a greater part of a solder joint, failure can be the result. Many researchers(16) believe that surface finishes that prevent oxidation also function as a diffusion barrier resulting to form a proper bond. Salam et al conclude that solder joint size does affect intermetallic growth rates.

Surface condition of copper pads greatly influence the wetting behavior of BGA's , thereby affecting their reliability characteristics. Tin oxide formations are usually formed on copper pads during Reflow process and this oxide layer formation poses a threat to intermetallic compound formation thereby affecting wetting phenomenon

Often, Fluxes are used to clean the pad surface. Flux deposition or Fluxing is a vital step in fixing the solder balls to the substrate. Flux chemistry helps in Solder ball robustness, to remove any oxidation layers on the solder pad and Inter connection performance. Since solder balls are responsible for metal interconnection this is an important and precision required step. Flux is applied with the intention to clean the pad surface which then promotes the wetting phenomenon and thus solder balls have a secured positional alignment as intended. [12].

Flux also performs the function to activating pad surfaces. Hetschel et al believe

that this chemical active surface might poses degradable effects to solder ball if flux systems are strong enough. Thus a balance has to be achieve between cleaning quality of copper pad and long term reliability effects due to degradation.(Hetschel)

Reflow profile has a consequential effect on solder joint reliability as it influences wetting and interfacial metallurgy of the solder joint. Pan [41] et al studied the effect of reflow profile on solder joint reliability. There investigation specifically investigated the effect of peak reflow temperature on solder joints by comparing effects of nine different reflow profiles on both tin lead and SAC 305 solders.

Intermetallic layer thickness is a vital factor that affects solder joint reliability. Reflow profile has a direct impact on intermetallic layer thickness; more reflow aging would result in thicker intermetallic layer. Thicker intermetallic layers are the brittle parts in solder joint and hence would reduce solder joint reliability.

A design of analysis experiment with peak temperature and time above liquids as input factors was constructed to study effect of peak reflow temperature on solder joint strength. The test boards were a 3.875 by 5.375 inch with FR 4 material. After thermal cycling the components, two failure types were observed: Solder joint failure and component failure. Shear force is a measure of shear strength of solder joint times the joint contact area. From DOE experiment, it has found that shear force of SnPb solder joints is higher than that to SAC 305. The only possible reason why SnPb solders have higher shear force than SAC 305 is that SnPb solder have more contact area. Thus wetting differences between SAC 305 and SnPb alloys are proved with their shear force measures

Melton[42] conducted a similar experiment to quantify the effects of Reflow parameters, atmosphere, peak reflow temperature, time above liquidus and metallization on wettability. The reflow profiles used the following reflow parameters; a 99 C/ minute ramp to 20 C with soak of one minute at that temperature, 65 C/minute ramp to peak reflow temperature. Solder balls of 96.5% Sn/3.5% Ag and 58% Bi/42% Sn solder alloy were used in this experiment.

A Design of Experiment problem was formulated to reveal that Metallization and Solder alloy and their interaction were found highly significant with respect to solder spread. All other results like time to wet etc proved that conventional SnPb alloys were the best solder next tin-lead-bismuth alloy.

Chapter 3
Research Methodology

3.1 TV 8 Test board design

The boards used in this experiment has a high temperature glass epoxy laminate(FR-4) substrate with OSP or ImSn surface finishes. These boards were designed by CAVE and were manufactured in Continental. The FR 4 substrate is 42 mil thick. Initally, Solder ball pitch was designed to be 0.4 mm, which increases the chance of short during reflow process. The boards were aimed with miniaturization in mind i.e. size, weight and space requirements. The components are solder mask defined. All solder balls were made using SAC 305 alloy. These boards were initially built as double sided, but yielded very poor results when went through the reflow oven for the second time. This test boards were specifically manufactured to study the reliability effects of different plating finishes, standard array with perimeter array of solder balls, filled with unfilled microvias and among various manufacturing process. This thickness in the board helps in reducing the co-efficient of thermal expansion gradient between board and substrate, thereby increasing its reliability characteristics.

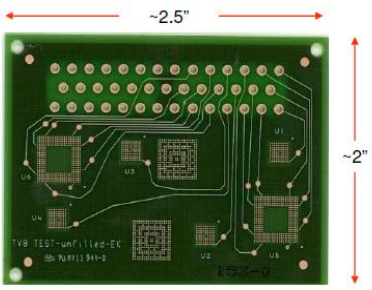
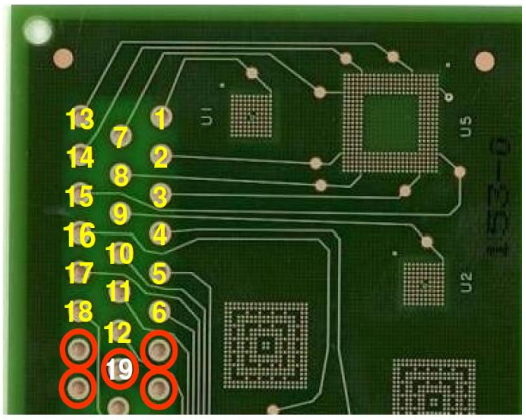


Figure 7 TV 8 board

The boards' dimensions are 2.5 by 2 inches and 42 mil thick. In each board there are six components: Two BGA 360 and four BGA 97. The boards are designed to have connector holes that are surface finished and connected to individual components. There are 41 connector holes, in which 5 are ground, 18 connector holes which are mapped to the test points of components.



1	**U1**	**8**	**U5**	**15**	**U5**
2	**U5**	**9**	**U2**	**16**	**U3**
3	**U5**	**10**	**U6**	**17**	**U6**
4	**U4**	**11**	**U6**	**18**	**U6**
5	**U6**	**12**	**U6**	**19**	**Gr**
6	**U6**	**13**	**U5**		
7	**U5**	**14**	**U5**		

Figure 8 TV 8 component leads
Table 5 Lead Description

The ground for each component traces back to the common ground and the common ground is connected to five ground connecter holes marked red as shown above in red. Wires from connector holes are attached to monitoring system that notes resistance value after every cycle.

TV 8 boards are solder mask defined. The important function of solder masks is to control placement of solder during an automated soldering process. TV 8 board substrates are formed first chemically etching the layout on to PCB boards.

There are twenty different combinations of boards that are used in this test which are as listed in the table 6.

S.no	Solder Paste	Type of Surface finish	Filled/Unfilled
1	Heraus	OSP	Filled
2			Unfilled
3		Immersion tin	Filled
4			Unfilled
5	Senju	OSP	Filled
6			Unfilled
7		Immersion tin	Filled
8			Unfilled
9	Kester	OSP	Filled
10			Unfilled
11		Immersion tin	Filled
12			Unfilled
13	Henkel	OSP	Filled
14			Unfilled
15		Immersion tin	Filled
16			Unfilled
17	Inventec	OSP	Filled
18			Unfilled
19		Immersion tin	Filled
20			Unfilled

Table 6 Different types of Boards used

3.2 Micro Vias

Microvias are very small holes on the surface pad that are generally created using non mechanical forces to connect two adjacent layers in a circuit board. Institute of Interconnection and Packaging electronic circuits (IPC) defines microvia's as equal to or less than 150 µm in diameter. Interconnection density is increased with help of these microvia's which results in increased routing area. During reflow process, the solder ball collapses and merges with the micro via, resulting in a permanent interconnection. If microvias are unfilled, the entrapped gases will result in void formation in solder balls as shown in the Figure 9 below. It has been known that voids greatly affect solder joint reliability. Also this void formation will result in increasing the diameter of collapsed solder ball which will lead to shorts due to less proximity between them.

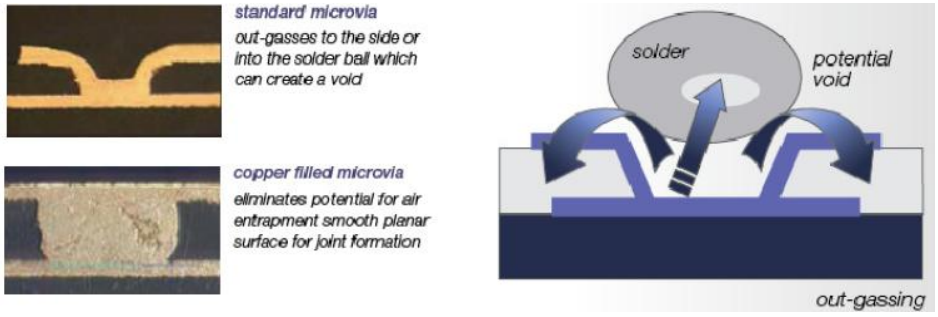


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Figure 9 Unfilled micro via void mechanism

Advantages of Micro via [56]

- It requires smaller pad, thus we have board size and weight independence
- Presence of Microvia's improve electrical performance due to short pathway distance.

- Low cost manufacturing.
- Increase in wire density by a factor of 4.
- 33% reduction in layer counts
- Fabrication capability on Rigid, Flex or rigid/Flex Substrates

3.3 Mouting Pad design

3.3.1 Microvia-in Pad design

Need of High density interconnection has lead the packaging industry to Microvia-in pad technologies [21]. The capability of forming micro via in copper pads gives flexibility to the designer in denser areas. The rings in Microvia for TV 8 were fabricated using laser beam. There are other types of micro via in pad designs like Offset –Center, Partial etc. A typical micro via-in pad is shown in Figure 10.

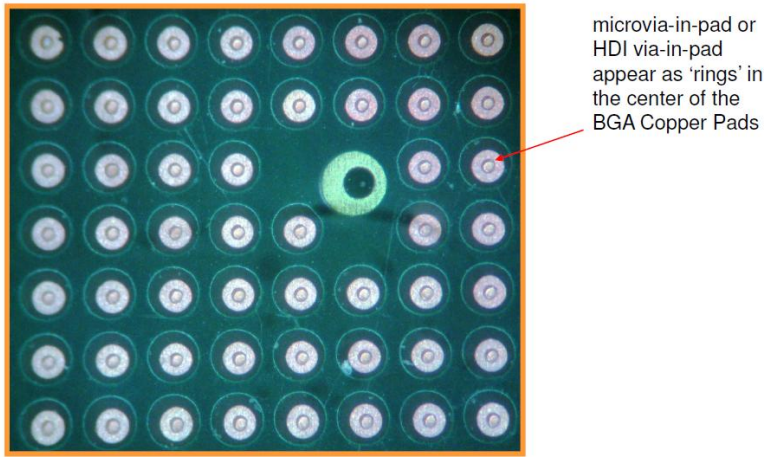

Figure 10 Microvia-in pad technology

Microvia-In pad designs are not much popular compared to dog-bone structure due to its low yields and cost involved in the process, [46]

Advantages of Using Via-in pad design [43]

- Reduced Pad resistance, Inductance and Capacitance
- High pin counts.
- Shorten signal routing

Challenges in Building Via-In-Pad design

- Void Formation Concern
- Limited Routing Space for Inner layers
- Fine ball pich versus trace width considerations.

3.3.2 Dog bone design

Via's perform the function of interconnecting solder balls to printed circuit board. Dog bone structure as shown in Figure 11 something has pad surface at an offset distance and it is connected to via with a trace. Thus it routes more than via-in pad configuration. This configuration can either by Solder mask defined or non solder mask defined. [46]

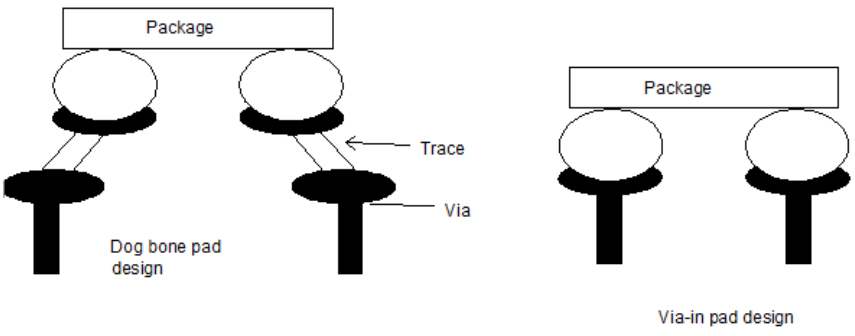

Figure 11 Surface pad designs[43]

Dog-bone structure takes up more space when compared to micro-via in pad design due to trace, but it also has the added advantage of changing distance any two consecutive routing lines.

Solder ball pitch for TV 8 boards is 0.4mm. There is very little distance between solder balls to design routing lines. Hence microvia-in-pad systems are the better choice.

3.4 Component Description: Ball Grid Array Packages

There are two types of BGA's: Ceramic BGA (CBGA) and Plastic BGA (PBGA)

Ceramic Ball Grid Packages (CBGA) have very big disadvantage with CTE mismatches as ceramic has very low CTE co-efficient when compared to FR 4 substrate. This CTE mismatch will aid crack propagation to occur faster. Generally, under fills are used to reduce CTE differences.

On the contrary, Plastic Ball Grid Array (PBGA) packages have a very good CTE match with all materials of PCB. PBGA's will absorb moisture when in storage and during reflow moisture in the package expands, results in a popcorn failure.

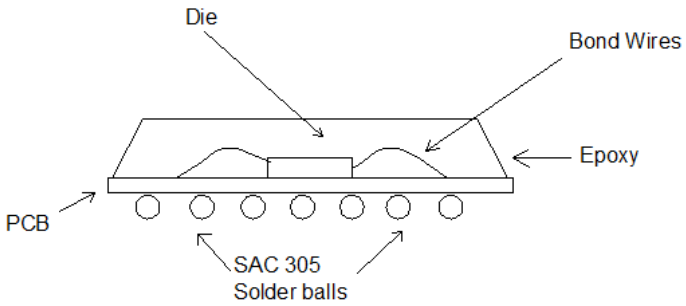

Figure 12 BGA Package[

BGA packages advantages include high real estate efficiency; design flexibility, enhanced performance and its ability of self align if there is misalignment by placing machine. Repairing of BGA packages is very hard and cannot be done using conventional systems, could only be done in rework stations equipped with spilit vision systems, a placement head and forced convection heating to the top and bottom of PCB. [7].BGA packages have big disadvantage in terms of reliability when compared to QFP packages in high temperature environments. But there are lots of improvement methodologies in BGA that make it more reliable in harsh environment conditions

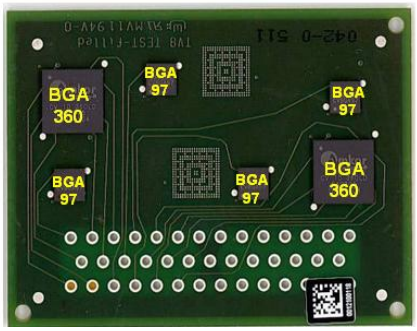

Figure 13 TV 8 Board with component locations

Each board has five components which are surface mounted. BGA 97 is a 5 mm x 5 mm package with standard array pattern and BGA 360 is a 10 mm x 10 mm has a perimeter array pattern. BGA 360 packages also have the same pattern similar to standard pattern, but solder balls directly under the die are removed. BGA 97 as the name suggest has 97 solder balls and BGA 360 has 360 solder balls.

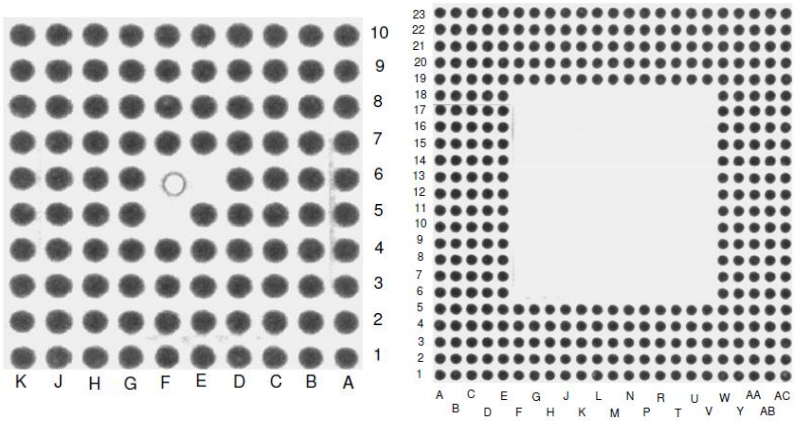

Figure 14 BGA 97(Standard pattern) and BGA 360(Partial Pattern)

Both BGA 97 and BGA 360 have daisy chain scheme to its solder balls. Daisy chain is a very popular wiring scheme in electrical engineering. As in the picture below in Figure 15, let us say, if a & b, b & c etc are in a loop then a & f are also in that loop, this forms the basic functioning of a daisy chain. Pros include less wiring needed to connect all components to circuit and only power is need to connect them. One of the biggest downsides includes circuit opens even if only one component fails.

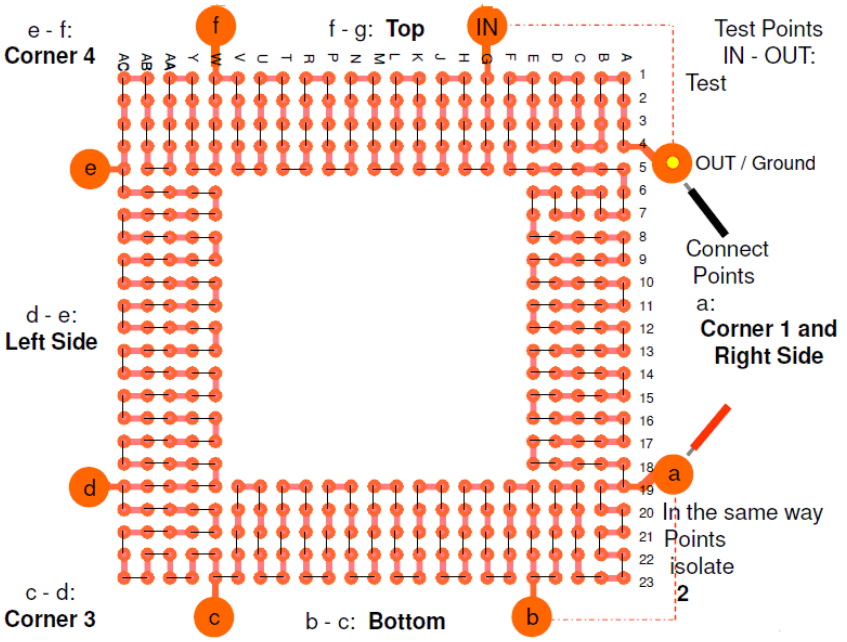

Figure 15 Daisy chain schemas for BGA 97 Packages

3.5 Surface finish

Surface finishes are basically used to enhance the solder ability property of any contact surfaces i.e. notable increase in wetting phenomenon in solder balls. The reliability of solder ball contact between SAC and terminal finish is important as any metallurgical conflict might results in brittle solder joints.[22] .If the intermettalic layers reaches the uppermost surface, it form oxides in the presence of atmospheric oxygen which will lead to areas of poor solder ability. Also many researchers have found surface finish greatly affects Intermetallic growth formation and this growth greatly helps in creating a permanent solder joint. [22]. two types of surface finishes: Immersion tin and Organic Solder ability Preservative were used in TV 8 test boards. Immersion Tin process requires deposition of pure tin on the copper pads thereby prevents the oxidation of copper to copper oxide which reduces the solder ability in the solder joint junction.

Organic Solder ability Preservatives is composed organo-metallic polymers with certain quantity of fatty acids and azole derivatives. [5].It possesses a unique property of bonding only with copper and thus serves the aim to prevent oxidation with other compounds in copper which reduces the wetting phenomenon resulting in bad solder joint. OSP's are protective coatings that must be removed before the soldering process with fluxing agents. This experiment includes analysis on 20 different boards that comprises combination of different types of surface finishes and different solder pastes to test for their reliability.

3.6 Properties of Solder Pastes and Fluxes

TV 8 boards used different solder material and fluxes in order to characterize its reliability in -40 to 85 C temperatures.

Fluxes

Kester

It is a No clean paste flux manufactured to work with lead free solder. It is compatible with SnAg, SnCu, SnAgCu and SnAgBi. Kester has peak reflow temperature up to 270 C. It has very aggressive action on various finishes like OSP-Cu, Immersion tin, Silver and ENIG. It has very low corrosion property[61].

Henkel

It is blue tacky flux material with 80% metal content and a tack life of 24 hrs. It is suitable of reflows in Nitrogen or air and is best suited with SAC alloys. Blue dye in Henkel material can be easily viewed under imaging systems to ascertain flux existence. Peak reflow temperatures are in the range of 230 -235 C [62].

Solder pastes

Senju

Senju ECO M31-GRN360-KV solder paste was primarily developed for lead free soldering applications. This paste retains its good viscosity properties for a over a period of long time. It has over 24 hour tack time. Suggest reflow profile for solder paste is as give below with peak temperature in the range of 230 -250 C[60].

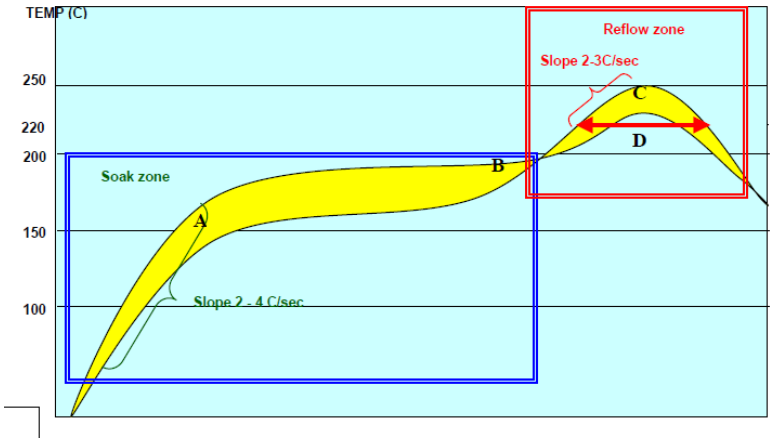

Figure 16 Suggested reflow profile for Senju pastes[60]

Hearus

Hearus F 640 solder paste was used in the screen printing process and stencils were used to produce solder balls. This solder paste has 89% metal content. Reflow can be done in either nitrogen or air. Peak Reflow temperature that would achieve the best results is 15 -20 C above the melting temperature of SAC 305. It has an 8 hour tack and work life. Best working conditions for this kind of solder paste would be between 20 and 32 C [63].

Inventec Material

Inventec Ecorel Pop 10 has SAC 305 alloy which was primarily developed for solder dipping process. As recommended, the boards were reflowed in a Nitrogen atmosphere. It has 80% metal content with melting temperature of 217 C[64].

3.7 Test Board manufacturing process – Solder paste and flux application methods

3.7.1 Screen Printing

Screen printing techniques translates solder paste onto the solder pads. It involves the process of using a fine mesh (stencils), usually made up of steel with very minute

holes. Meshes or screens are placed on the component and solder paste is forced through it with a squeegee tool. Type 3 solder paste is used in screen printing process. Manufacturing process in Continental (Board Manufacturer) had the highest capability of using type 3 pastes. The minute holes on the mesh are in perfect alignment with surface pads below. Thus the volume of the solder ball is directly controlled by the mesh. Density of conventional tin-lead solder paste is different to SAC 305, hence process parameters has to be changed accordingly to achieve the desired results. A Pick and place robot with a solder dispenser syringe can be used to replicate the screen printing process and thus mass production is easily achieved.

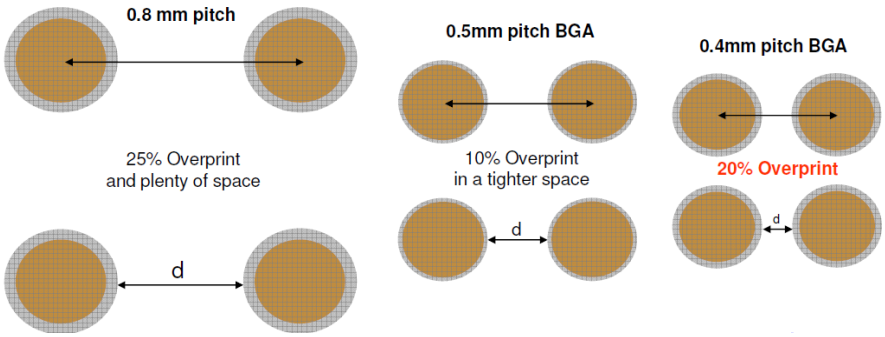

Figure 17 Effects of decreasing pitch on solder shorts

From the figure 17, we can notice that grey area (solder ball) is bigger than brown area (surface pad), this increases the risk of shorts. Initially, TV 8 boards were designed for 0.4 mm pitch. Screen printing 0.4mm pitch solder balls yielded very poor results. Figure 17 shows presence of shorts due to bridging of solder after reflow process.

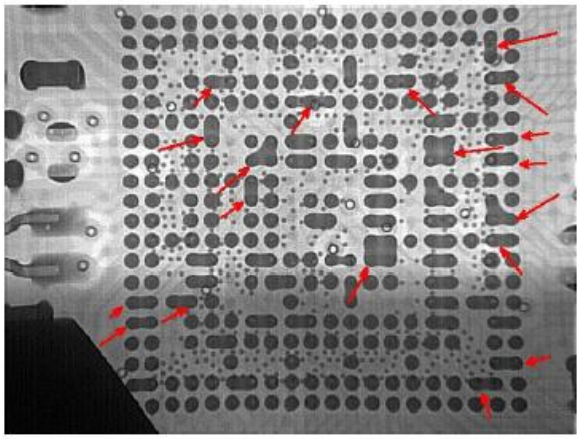

Figure 18 Solder shorts in TV 8 0.4mm pitch boards

In 0.4 mm solder ball pitch component, there less than 2 mils (<75 mils) space between two adjacent solder deposits. 300um diameter aperture stencil was used in this process to screen print solder balls. It is believed that 300um diameter is the smallest practical diameter for a type 3 solder paste.

All screen print TV 8 boards were x-rayed to note presence of solder shorts as shown in the diagram 19 below.

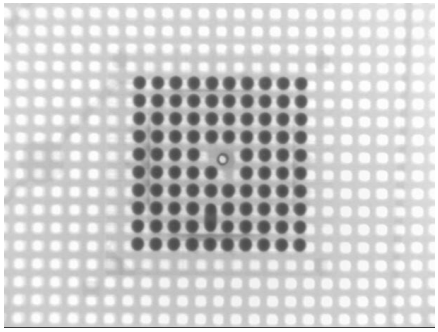

Figure 19 Xray analysis of BGA 97

3.7.2 Dip flux and Dip paste

Solder balls in TV 8 boards are 11.8 mils in diameter with 0.4 mm pitch. In visual inspection tests, few solder balls which did not pass initial inspection tests. Cross section analysis clearly shows a visible distance between solder ball and surface pad after reflow process. An explanation to this phenomenon would be there was no enough solder in the solder ball to melt and form a connection with surface pad below during the reflow process.

Screen printing these solder balls required 5 mil thick stencil with 10 mil aperture diameter on stencil. By using 10 mil aperture diameter proper solder balls were not achieved as solder paste was sticking along the edges. They (Continental –Board Manufacturer) used a 15 mil aperture diameter stencil to achieve this. Using a stencil thinner than 5 mil, would result in solder skips and thicker stencil would definitely result in solder bridging.

A solution to this problem would be dipping the solder balls in paste medium. Thus dipping in a paste medium would increase the solder balls diameter marginally and may be enough to form a metal interconnection. In Dip paste method, BGA package is dipped in a paste –flux medium rather than only paste as OSP coatings have to be removed before reflow in order to make a conductive medium. Fluxes perform this function. Dip flux method involves dipping the entire BGA package in flux and then it sent into reflow soldering.

3.8 Reflow Soldering

No single reflow profile can be used to all electronic boards. Different solder

pastes, board design, substrate board thickness etc have the effect of reflow profile on them which might induce failures. Reflow profiles have definitive effect on solder joint reliability as reflow aging increases brittle intermetallic compound thickness which affect wettability. Reflow can be done in Nitrogen or Air. Typically reflowing air would be sufficient but when using flux instead of a solder paste, it becomes important to reflow it in nitrogen inorder to produce reliable solder joints. (Shangguan) .After the screen printing process, solder balls temporarily connect electronic components to surface pads. Reflow soldering involves the process of melting the solder ball to form a permanent contact with surface pad. The electronic boards are sent in to oven with different temperature zones to result in a permanent connection. Different zones are

Preheat Zone

Lau suggests this zone should have the slowest ramp rate as the solvent evaporates. Also this layer reduces thermal shock in boards as it is exposed higher temperatures in next zones.

Thermal soak Zone

Activation of fluxes takes place in this zone. Flux activation cleans the surface pad, so that solder joint has good reliability. If the temperature is too low, flux activation would not started and if temperature is too high, flux gets used up and oxidation of paste takes place. Wetting does not occur.

Reflow Zone

Temperature in this zone reaches the highest in the range of 20 C -30 C more than

liquidus. Peak temperature is one of the key parameters in the reflow process. In this zone, solder paste goes to the liquidus state (reflows) and forms a permanent metal bond with surface pad below.(Shangguan) Intermetallic growth formation can be seen in this stage between the liquidus solder ball and surface pad when soaked more in liquidus state of solder ball.

Cooling Zone

It is the very last zone and process in the reflow process. All reflowed boards are cooled here and solder joints get solidified.

Chapter 4
Testing Methodology

Main objective of this thesis is to analyze the reliability effects of various aspects like filled and unfilled microvia- in pad design, OSP and Immersion tin surface finishes, Reflow atmosphere Nitrogen and Air and manufacturing methods like dip paste, dip flux and screen printing process on solder joints.

The Figure 20 below shows the testing methodology used for completing this thesis report. The manufactured boards are well inspected for wetting problems, surface finish problems etc before they are actually put into thermal testing. It was made sure that every solder joint in thermal shock was good as reliability characterization cannot be quantified with bad solder joints.

After thermal testing cycles, failed boards were cross sectioned for failure analysis. Also reliability is characterized with the failure data.

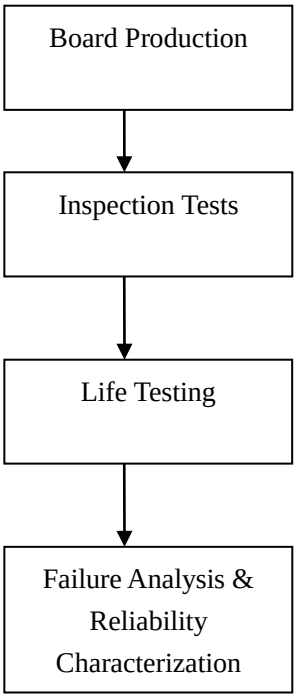

Figure 20 Testing methodology

4.1 Inspection Tests

4.1.1 Electrical Probing

BGA 97 has one test point and BGA 360 has seven test points. All these test points were electrically probed with a multimeter. Electrical Probing is performed to check openness of circuit. If solder joints are good and they provide a good connection between BGA package and substrate board, an internal resistance would be a result due to closed circuit. If solder joints are cracked, a high resistance would result in a circuit. As shown in the Figure 21, wetting problems in solder balls will make a circuit open. This open circuit when probed will result in a very high resistance value.

4.1.2 X ray inspection

During first production of TV 8 boards, solder balls pitch was 0.4 mm. But the yield was very poor as a result of many shorts due to proximity in solder balls. After

evaluating all x-ray images, it was concluded that BGA packages are good for thermal shock tests.

4.1.3 Cross section Analysis

After electrical probing, Solder balls which failed were analyzed to find the root cause of failure. Exact failure daisy chain was determined and components were dissected from the board. The examination is aimed at reveal cracks or crack progressions, voids, wetting performance etc all of which might be cause of failure. It is well known that voids often reduce solder joint strength and hence affecting reliability. Plastic moulds were prepared with epoxy resins and hardeners. The components are placed down in these plastic moulds and were polished using various grid papers to achieve proper finishing. Some of examined cross-sections are shown in Figures 21 and 22.

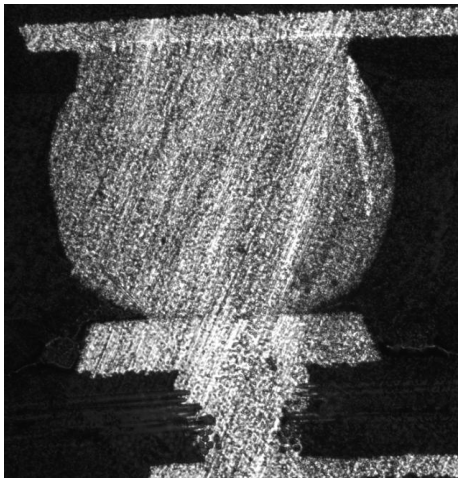

Figure 21 Wetting problems in Kester-OSP-Filled, BGA 97 – U1

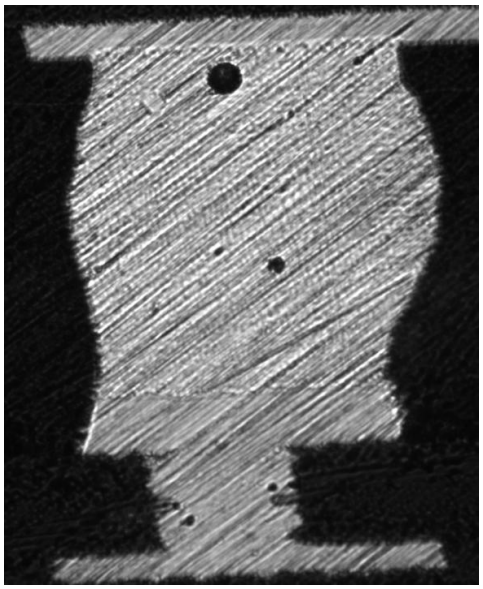

Figure 22 Presence of Voids in Inventec-Sn-filled

4.2 Surface Science Analysis

Copper oxide formation on surface pads during immersion tin process will affect solder joint wet ability. Hence Auger electronic spectroscopy is used to study these pad surfaces.

AES is a true surface technique, allowing detection of all elements of the period table (except H) located within the first 50 Å of the material surface to a sensitivity of ~ 0.01 atom %.

Methodology

The specimens were removed from the shipping packages and a through-hole portion with a pad surface was identified, cut away from the PCB and mounted into the surface system with no additional pretreatment or special handling.Surface analysis on the pad surface was then performed, followed by Ar sputter cleaning. The sputter cleaning step for each specimen lasted 5 (10) minutes, corresponding to removal of ~ 125 (250) Å of the specimen surface.

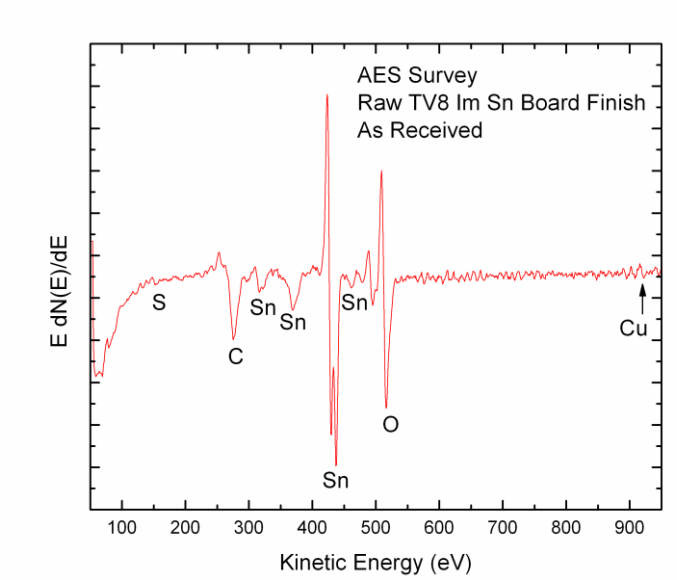

Figure 23 AES Spectra- TV 8 immersion tin board finishes before wetting on raw board

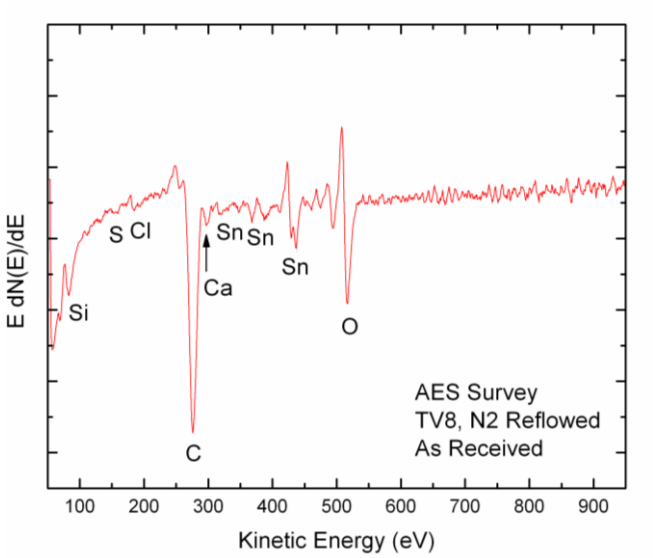

Figure 24 AES Spectra- TV 8 immersion tin board finishes after one reflow cycle in Nitrogen on raw board

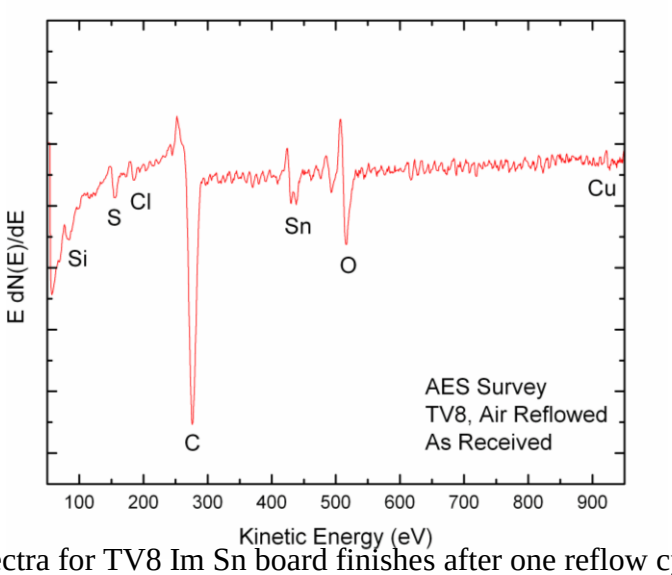

Fig. 25 AES spectra for TV8 Im Sn board finishes after one reflow cycle in air on raw board

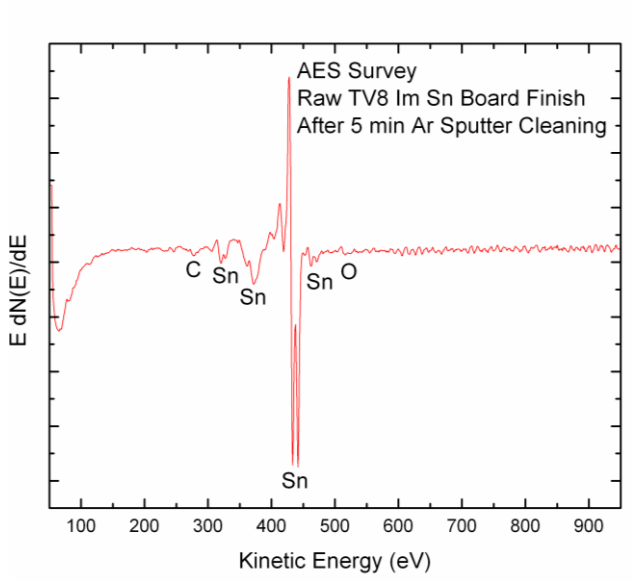

Fig. 26 AES spectra for TV8 Im Sn board finishes after one cycle of sputter cleaning on raw board

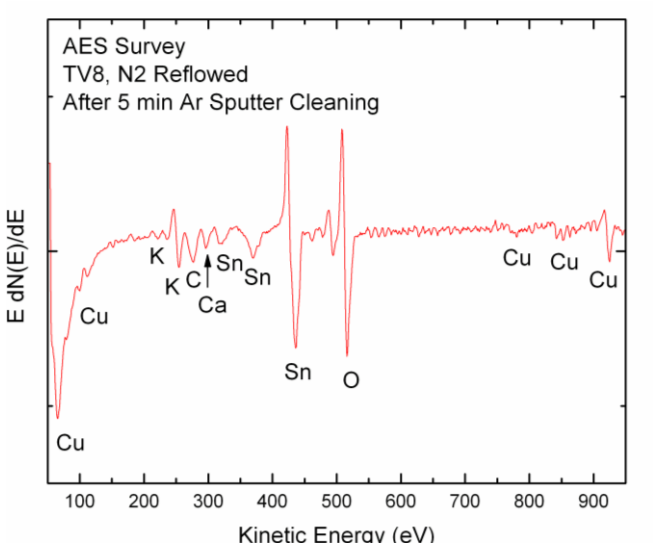

Fig. 27 AES spectra for TV8 Im Sn board finishes after one cycle of sputter cleaning afterone reflow cycle in Nitrogen

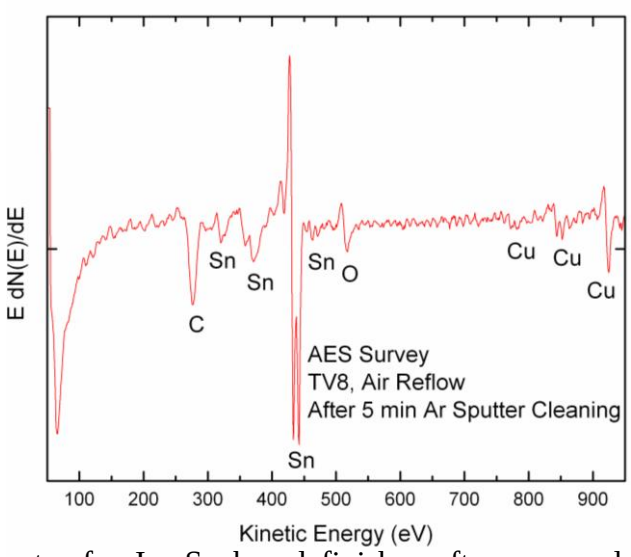

Fig. 28 AES spectra for Im Sn board finishes after one cycle (5 min) of sputter cleaning. And reflow cycle in air

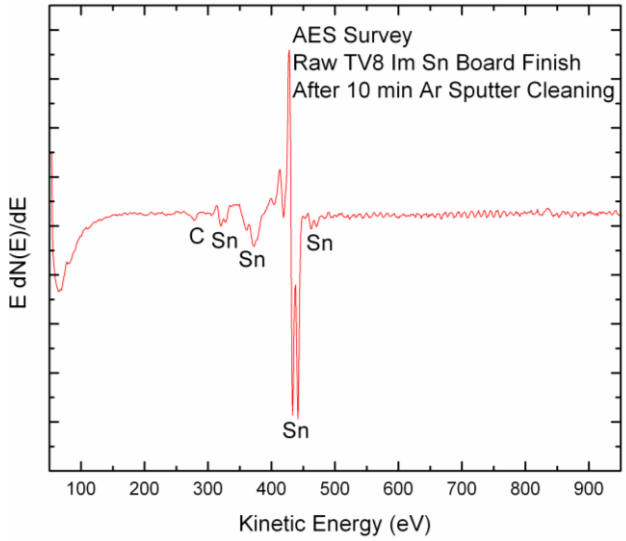

Fig. 29 AES spectra for Im Sn board finishes after two cycles (10 min) of sputter cleaning.) oner one reflow cycle in air on raw board

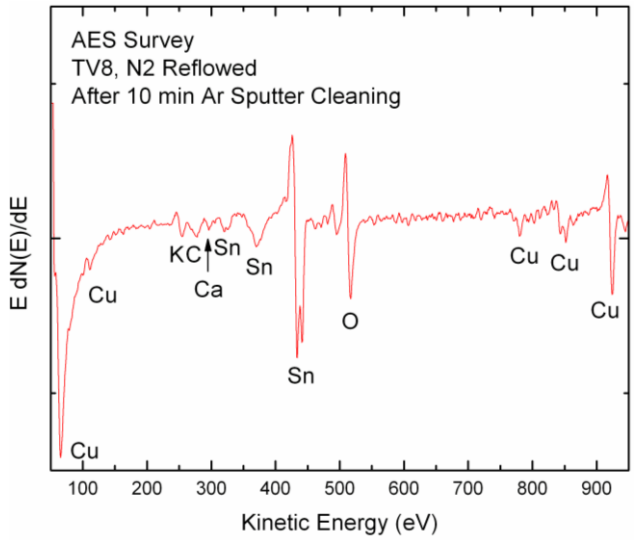

Fig. 30 AES spectra for Im Sn board finishes after two cycles (10 min) of sputter cleaning.) after one reflow cycle in Nitrogen

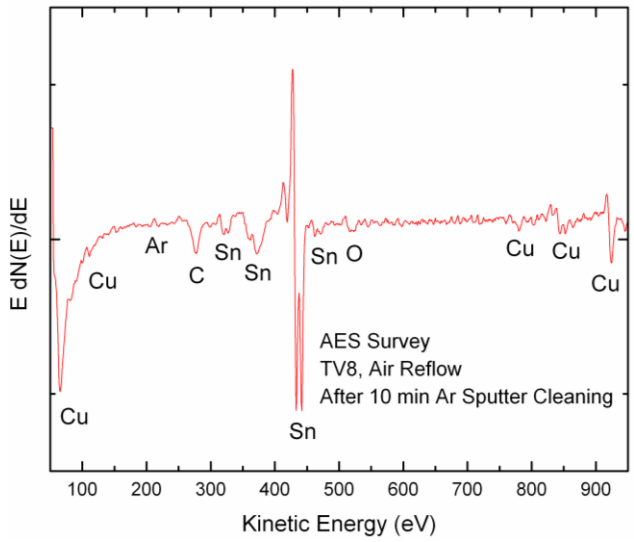

Fig. 31 AES spectra for Im Sn board finishes after two cycles (10 min) of sputter cleaning after one reflow cycle in air.

Findings.

- TV 8 Sn board finish surface is good with usual amount of sulphur, carbon and oxygen on surfaces exposed to air. But supper cleaning of board finish removes all these elements as show in the Figure. 26
- From Figures 21 and 22, we can observe a large carbon signal. Both air and nitrogen reflow atmospheres have added carbon to surface. .
- Despite the similar amounts of starting C found on after reflowed specimens, the N2-reflowed specimen “cleaned up” faster during the sputter process with respect to C. This is seen by comparing Figs. 27 and 28 After both 1 and 2 cycles of sputter cleaning, the N2-reflowed surface shows less surface C than the air-reflowed surface; however, it is interesting that the N2-reflowed surface shows more O on the board finish surface which persists during sputter cleaning
- Finally, it looks like the Cu observed in the reflowed specimens is due to Sn-Cu interdiffusion at temperature. This is because we do not see Cu on the raw board

finish surface both before and after sputter cleaning but it is present on both reflowed board finishes

4.3 Failure Testing

A lot of different methods exist for finding various failure mechanisms; it all depends on the characteristic that has to be studied. Some of the most common methodologies are

4.3.1 Thermal cycling

When in operation, most electronic equipment undergoes thermal temperature cycles. Co-efficient of thermal expansion mismatches occur, induce strain on the system. This induced strain exceeds the elastic stress of solder balls, resulting in cracks. The actual testing environments vary with different fields like Space, Marine, under the hood automotive etc.

4.3.2 Vibration

Vibration is a vital factor that is encountered is most harsh automotive environments and military electronic hardware. Care should be taken in proper clamping of the test boards. Vibration test are conducted to test mechanical withstanding capability of electronic packages. Electronic packages vibrate in high frequency in resonance conditions and mostly will fail in this condition.

4.3.3 Mechanical shock (Drop Test)

Every product has the probability of getting dropped accidently over its product life. Thus a certain amount of damage resistance has to build as a product reliability characteristic. Products are dropped using the drop test machine from certain height

with desired force. The failure criterion in this kind of test would be no visible damage to the product. (Lau)

4.3.4 Accelerated Life testing – Thermal Shock

Differentiating thermal shock and thermal cycling, we can formulate that testing conditions are the important factors. Due to wide range application of electronic products at various temperatures, thermal shock procedures are used to expose it to large temperature gradients. Also thermal shock tests have a normal operating range of -40 C and 125 C which is not the case with thermal cycling.

One of the most important performance characteristic of electronic packages are its performance at different temperature levels i.e. Reliability. The most common method of finding out failure rates is through accelerated testing conditions. An accelerated testing stress produces more than that actual service life of components and hence it is one of the most widely used methods of evaluating long term reliability of solder joints. The results from this test will enable the engineer to extrapolate it to practical environments. However, Tong [44] believes that Thermal shock testing would be a bad test, if tested boards have similar Co-efficient of Thermal Expansion Values. All these tests are primarily used as qualification stages for electronic products. The boards in this experiment are subjected to a 30 min cycle which includes a 15 sec transit time at -40 C to 85 C and will result in alternate contraction and expansion stress on solder joints.

The boards were subjected to very high temperature extremes in a very short

period of time i.e. Thermal shock. Thermal shock testing can be Air to Air or Liquid to Liquid. All TV 8 boards were Air Shocked in a dual chamber with hot and cold sides. In dual chamber, the boards were placed in a basket that moves up and down between -40 C cold chambers and 85 C hot chambers and a rubber sealing exists between these two chambers. Cracking, crazing, and delimitation are common types of failure mechanisms associated with thermal shock.

The boards were subjected to a total of 4300 thermal shock cycles before stopping the test. This temperature cycling of boards affects co-efficient of thermal expansion between different components resulting in inducing of stresses that will lead to crack propagation, resulting in complete failure. Thermal shocks test mechanical strength of solder joints and components. Induced thermal stresses are directly related to geometrical properties and material properties of individual components. There are number of parameters influencing reliability which include filled/unfilled via, solder paste, surface finish, CTE differences, Specific Heat etc. The test profile used for this experiment is a shown in Figure 32.

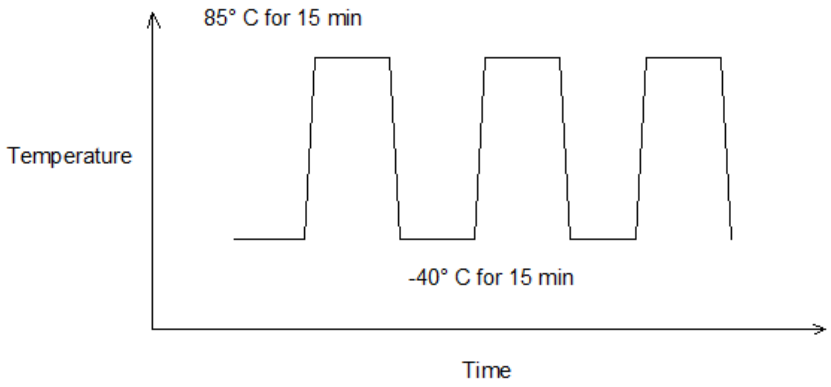

Figure 32 Thermal shock test profile

The boards were thermal shocked for 4300 cycles and were monitored with resistance as a failure parameter. Solder joints effects were monitored. A resistance temperature detector was used to log in number of cycles. After each thermal cycle data is logged on to database using LABVIEW software

Chapter 5
Analysis and Results

5.1 Reliability Curve – 'Bathtub'

Bath tub curves are primarily used to represent component reliability (failure rate) over time. [54]. Bath tub curves looks at cumulative number of failures over a period of time. Reliability of electronic systems is directly affected by applied stress. Many studies have shown that the height of the curve is directly proportional to applied stress. A bath tub curve is a composite curve that has three regions: Infant mortality, Normal life and Wear out regions.

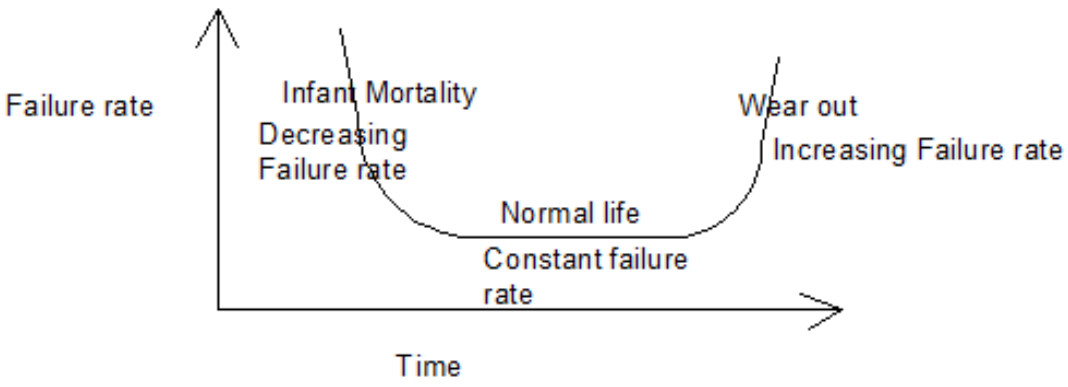

Figure 33 Bathtub Curve

- Infant Mortality
    - Infant mortality failures occur during first stages of testing. These

failures are results of manufacturing defects which do not expose themselves during initial testing procedures like Electrical probing, x ray inspection. Thus thermal shock testing of these components will result in very early failure. These failures could result in total system failure when found in large number.

- One other method of testing for infant mortalities is Burn in process. In this process, electrical and thermal stresses are applied to chip which are equivalent to its product life but will be of higher amplitude. Thus defects are detected and will not be shipped. [53].
- Solder joints in TV 8 boards were inspected before putting into actual thermal shock test. All combination of boards yielded no infant mortality problems.

- Normal Life
  - Random failures caused by effect of stresses on failure mechanisms over a prolonged period of time.
  - Most boards have survived over 1700 cycles and first recorded failure was at 1795 thermal shock cycles
- Wear out
  - Failure rate increases drastically as products have crossed their useful life use operation is beyond what the component was designed to do.

5.2 Reliability Characterization

Tv 8 boards were thermal shocked for 4300 cycles and obtained data is as

given below. From the data we can infer that there is no particular pattern in which any one combination board fails. A total of 350 components of different combinations were put into test. From the failure data, we can calculate that there is 3% overall failure. This 3%failure reveals that all combinations of finishes, BGA pattern, and reflow atmosphere had very less significant effect on solder joint reliability.

S.no	Component Type	Component Name	Board Combination	Failure Cycles
1	BGA 360	U3	Senju-filled-ImSn	1795
2	BGA 360	U6	Senju-filled-ImSn	1826
3	BGA 360	U5	Hera-Unfilled-OSP	1870
4	BGA 360	U5	Inventec-Unfilled-ImSn	1925
5	BGA 360	U6	Henkel-filled-OSP	2235
6	BGA 360	U6	Senju-filled-OSP	2365
7	BGA 360	U5	Kester-filled-ImSn	2502
8	BGA 360	U2	Inventec-filled-ImSn	3274
9	BGA 360	U4	Inventec-filled-ImSn	3284
10	BGA 97	U1	Inventec-filled-ImSn	3314
11	BGA 360	U3	Inventec-filled-ImSn	3314
12	BGA 360	U6	Kester-Unfilled-OSP	4265

Table 7 Failed Components after 4300 cycles

Test boards which failed during the 4300 cycle test were cross-sectioned for failure analysis. The cross section would determine the failure mechanisms for BGA Packages. Thermal shock involves exposing the test board to extreme temperatures. When exposed to hot temperature, metal expands resulting stresses

as shown in Figure34 . Same is the case during cold side, this cyclic occurrence of stresses will result in crack propagation and ultimately failure. Figure 34 a representation of failure mechanism in solder joints. Most cracking has occurred in the region between solder ball and copper i.e. around intermetallic compound and is in a parallel direction to copper pad. This would be result of a weak intermetallic region. A considerable number of cracks were also seen in the top region of solder pads and solder ball interface. As Tv 8 boards are solder mask defined, shear stress may be high in this region. These cracks are caused by stresses which are resulted due CTE mismatches between board and substrate. The cracks shown in the Figures 35 and 36 have travelled the entire area of intermetallic region.

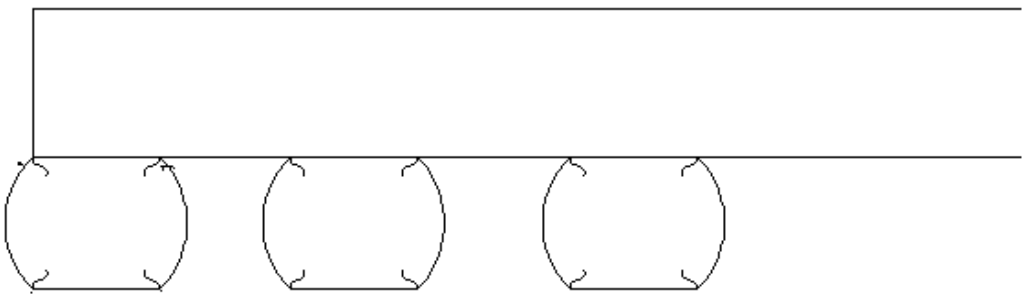

Figure 34 Combined effect of hot and cold temperatures on solder balls.

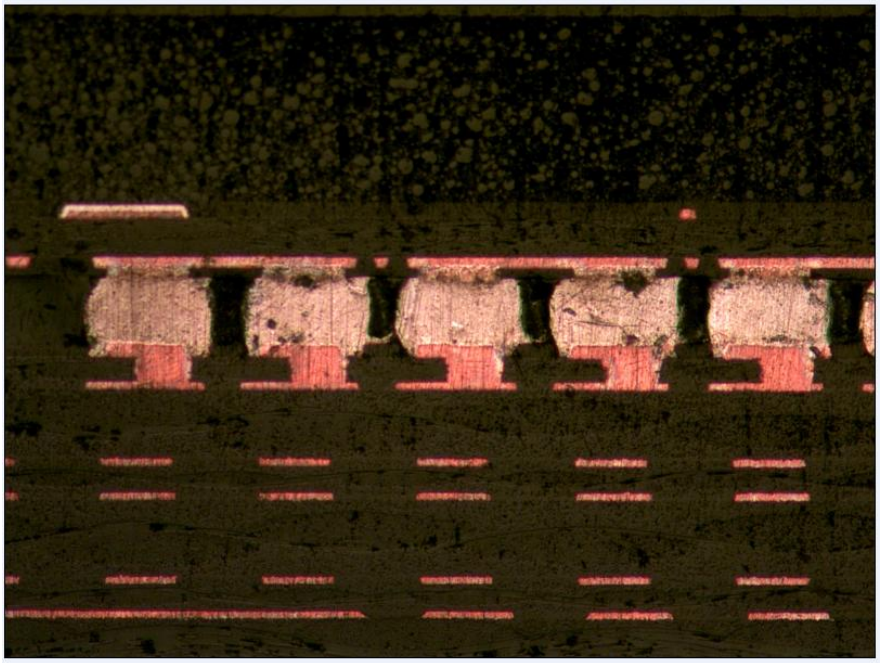

Figure 35 Cracks at Intermetallic region and top surface.

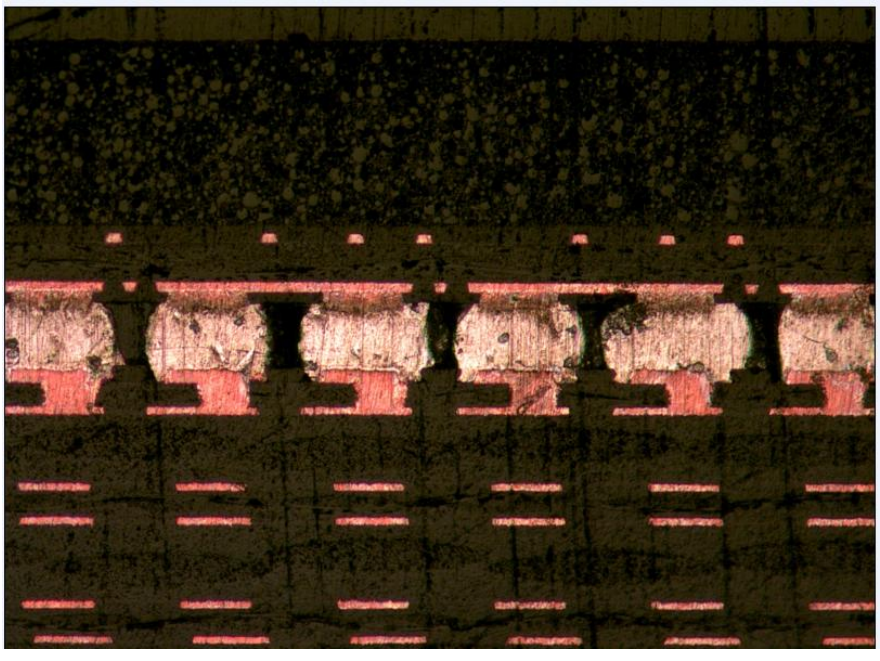

Figure 36 Cracks at Intermetallic region and top surface.

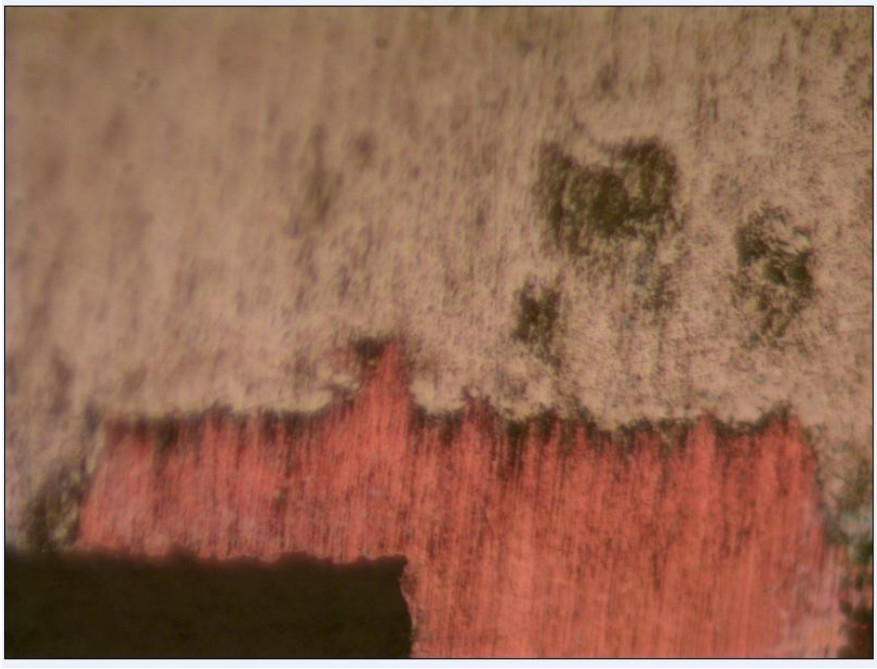

Figure 37 Presence of Crack Propagation

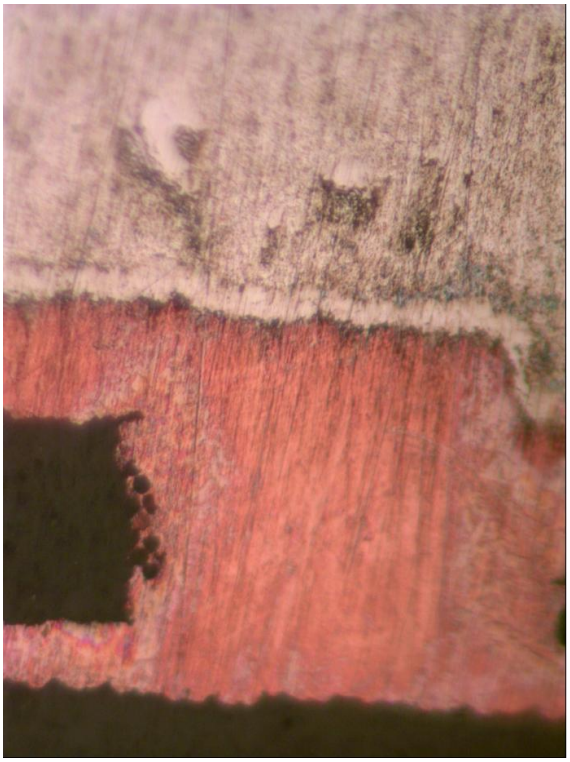

Figure 38 Crack propagation parallel to intermetallic region

Chapter 6
Conclusion

Due to ever increasing demand for smaller and faster BGA packages, various new technologies have emerged. It is very important to characterize its failure modes and mechanisms and characterize its reliability. Reliability of solder joints which forms the metal connection between package and substrate are very important parameters during design stage of electronics as interfacial metallurgy defines wetting characteristics. Solder materials, manufacturing processes, reflow atmosphere etc will have its affect on solder joint reliability. This thesis conducts a similar research on a very fine pitch BGA packages with various improvements like microvia-in pad design, different plating finishes etc.

Cracks propagation was observed in cross section analysis. These cracks are located very close to intermtallic region and propagated through the entire volume of solder ball. CTE mismatches are the primary cause for this cracking to occur. Both BGA packages have survived 4300 cycles with less than 5% failures.

With this 5% failure in a temperature range of -40 C to 85 C we can conclude that there is no significant difference in effects of different plating finishes, use of different solder pastes and microvia structure to overall reliability of solder joints during these 4300 cycles.

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