PBGA RELIABILITY OF LEAD FREE SOLDER BALLS ASSEMBLED WITH TIN LEAD SOLDER PASTE FOR HARSH ENVIRONMENT ELECTRONICS

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Charles Clayton Mitchell

Certificate of Approval:

Saeed Maghsoodloo Professor Industrial and Systems Engineering	John L. Evans, Chair Associate Professor Industrial and Systems Engineering
Michael J. Bozack Professor Physics	Lewis N. Payton Research Assistant Professor Industrial and Systems Engineering

Stephen L. McFarland
Acting Dean
Graduate School

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Charles Clayton Mitchell

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PBGA RELIABILITY OF LEAD FREE SOLDER BALLS ASSEMBLED WITH TIN LEAD SOLDER PASTE FOR HARSH ENVIRONMENT ELECTRONICS

Charles Clayton Mitchell

Signature of Author

Date of Graduation

VITA

Charles Clayton Mitchell, son of Nancy and Paul Mitchell, was born on July 18th, 1981, in Greenville, Alabama. He graduated high school from Fort Dale Academy as Salutatorian in May 2000. After high school, he attended Auburn University located in Auburn, Alabama in the fall of 2000. In the spring of 2004, he graduated magna cum laude with a Bachelor of Science degree in Industrial and Systems Engineering. After graduation, he remained at Auburn University and entered the graduate program as a research assistant in the field of automotive electronic reliability. While a graduate student at Auburn University, he was selected as one of Auburn's ten most outstanding graduate students. In the summer of 2006, he will obtain his degree in Masters of Science concentrated in Industrial and Systems Engineering.

THESIS ABSTRACT

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Charles Clayton Mitchell

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The demand for high-temperature electronics is growing rapidly in the automotive industry. This stems directly from the fact that these electronics are being transferred from their passive environments to under-the-hood locations, specifically on the engine or transmission. The electronics not only have to withstand high temperatures in excess of 150ºC but also maintain superior levels of reliability at no added cost. To meet this criterion, the plastic ball grid array (PBGA) electronic packages have been successfully integrated into the design of under-the-hood controllers.

Until recently, the research and design of the PBGA packages have incorporated the traditional tin lead solder balls assembled on tin lead solder paste. But lead free regulations set forth in Europe, Japan, and China has put pressure on the Unites States electronics industry to convert to lead free manufacturing. Due to different timetables between the electronic component supplier and the manufacture, direct conversion to lead free manufacturing is not feasible. For PBGA packages, hybrid interactions between the solder balls and solder paste will exist. The primary focus of this research was to evaluate the reliability of the hybrid combination, namely lead free PBGA packages assembled on tin lead solder paste.

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CHAPTER 1: INTRODUCTION

As automobiles have become more sophisticated, their electronics have increased in both complexity and functionality. These enhancements have expanded the percentage of manufacturing costs dedicated for electronics. In 1977, the average automobile contained $110 worth of electronics. By 2003, this number was increased to $1,510 and by 2013 the estimated value of electronics within the car is expected reach to $2,285 [1].

In automotive electronics, there is a continuing trend to reduce the size of electronic packages due to space requirements and material costs. While this trend is occurring, automotive electronics are currently being shifted to under-the-hood locations, specifically the engine or transmission. By integrating controllers on the engine and the transmission modules, the electronic packages are exposed to high temperature operating conditions. As defined by the Toyota Motor Corporation, Table 1 portrays the operating temperatures for automotive electronic systems.

Location	Operating Temperature
Under Dash Board	-30ºC to 85ºC
ECU Box	-30ºC to 105ºC
Underhood	-30ºC to 125-150ºC
Connected to Engine	-30ºC to > 175ºC

Table 1: Toyota's Electronic Automotive Environment

Considering the miniaturization of electronic packages and their high temperature operating conditions, the automotive industry is constantly under pressure to maintain expected levels of reliability while still lowering cost. As a result, the automotive industry has embraced plastic ball grid array (PBGA) packages. PBGA packages deliver small footprints and great electrical conductivity while still maintaining low levels of cost for high volume manufacturing [2].

To ensure that the PBGA electronic packages can withstand the automotive under-the-hood operating conditions, accelerated life testing is performed. Accelerated life testing (ALT) attempts to overstress the electronic package and reduce the mean life to failure. Solder joint reliability requirements, cited by [1, 3, 4], for under-the-hood automotive electronics, requires temperature cycling between -40ºC to 125ºC with no failures up to 2,000 cycles or less than 1% failure after 2,500 cycles.

For the past 10 years, research studies have determined that altering PBGA design parameters can positively or negatively affect its reliability. However, this research was based upon a tin lead system (interaction between tin lead solder balls and tin lead solder paste). Because of the recent lead-free regulations, the demand for lead-free products has been increasing.

The motivating forces behind the transitioning to lead-free manufacturing can be attributed to the Japanese manufactures, European governmental regulations, and Chinese governmental regulations. Since 1998, the Japanese manufactures have been using lead-free soldering in many of their popular consumer products [5]. As of January 2006, most Japanese manufactures have converted to lead-free manufacturing. In Europe there are two lead-free directives/laws that directly affect their electronics industry. The Waste Electrical and Electronic Equipment (WEEE) limits the amount of lead disposed in the environment which became effective on August 13, 2005. The Restriction of the Use of Hazardous Substances (RoHS) eliminates lead in electrical and electronic equipment and takes effect in July 1, 2006. The Chinese government approved their version of RoHS that removes lead in electronic products that will take effect in March 1, 2007.

Through globalization, the United States electronics manufacturing industry frequently imports electronic devices from China, Europe, and especially Japan. Figure 1 shows the end-of-year money spent by US companies on imports (semiconductors & related devices) from Japan, China, and Europe [6].

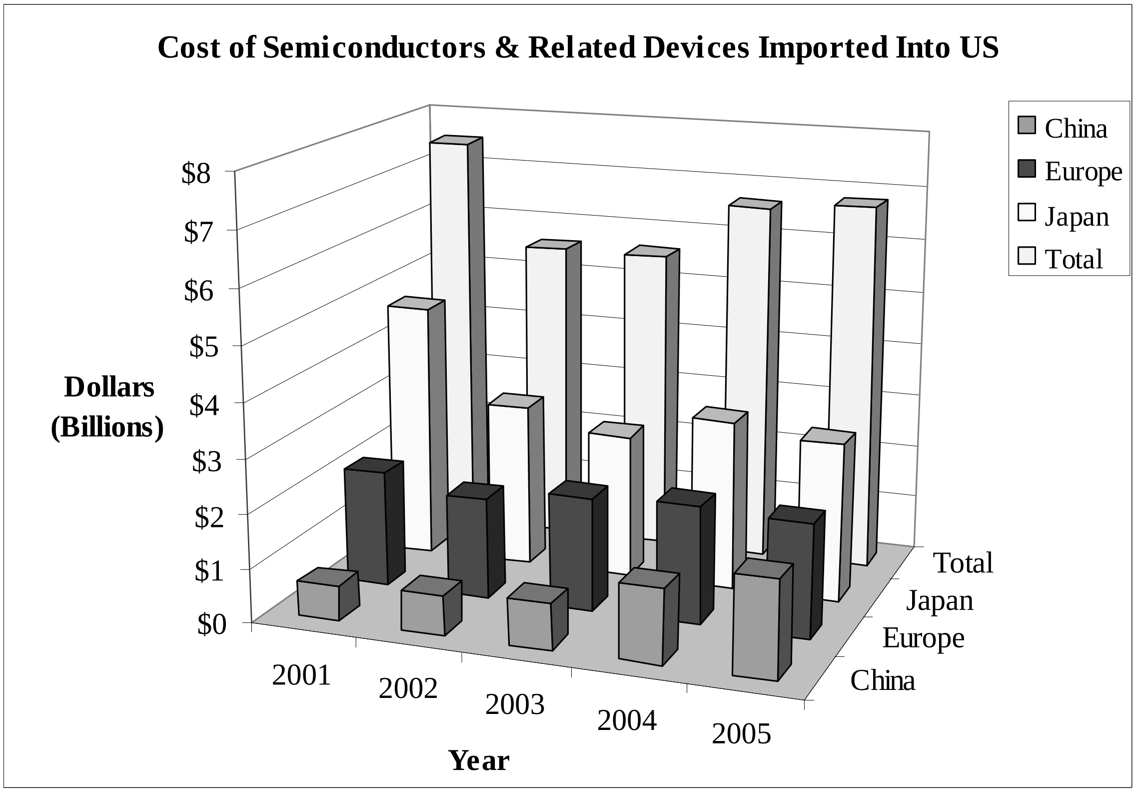


Figure 1: US Cost - Import Semiconductors

In 2006 and 2007 the electronic components imported from these regions will be lead-free. Thus, the US electronics industry has to prepare to convert to lead-free manufacturing.

The feasibility of the US electronics industry converting directly from the traditional tin-lead system to the lead-free system is doubtful. Hybrid systems will emerge since the component suppliers and the assembly manufacturers are not on the same lead-free timetable. Figure 2 represents the three routes that will be taken in the transition to lead-free manufacturing [7].

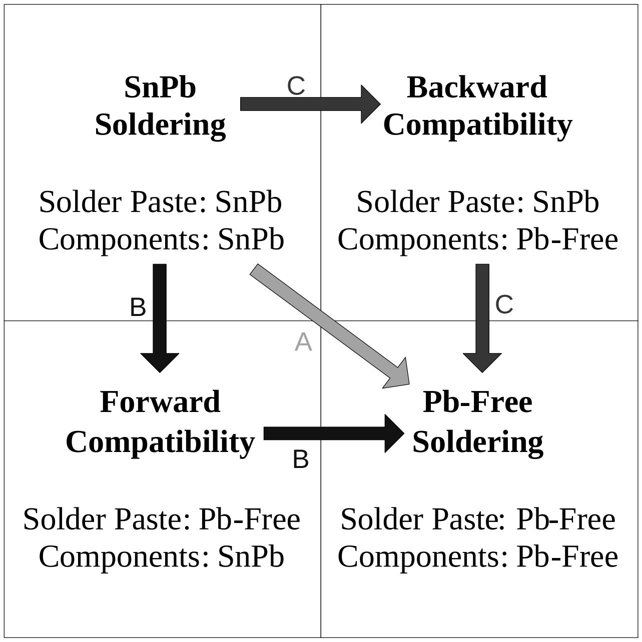


Figure 2: Lead Free Roadmap

The reliability of these hybrid systems must be evaluated to determine if they are suitable for automotive under-the-hood electronics. With respect to harsh environmental testing (-40ºC to 125ºC), limited research has been performed on the reliability of these hybrid systems, namely Backward Compatibility and Forward Compatibility.

This thesis focused on quantifying the reliability of lead free PBGA packages assembled with SnPb solder paste (i.e. Backward Compatibility). All of the testing and analysis were performed at the Center for Advanced Vehicle Electronics (CAVE) located in Auburn University, Alabama. CAVE is a research consortium dedicated to working with industry in developing and implementing new technologies for the packaging and manufacturing of electronics.

To evaluate the “backward” system a test vehicle was designed. The design of the test vehicle, TV3D, was a mutual effort between Siemens VDO Automotive located in Huntsville, Alabama and CAVE. Based upon the electronic packages assembled onto the test vehicle, two different configurations were developed.

The first configuration, TV3D_C1, was air-to-air thermally cycled between -40ºC to 125ºC with a cycle time of 90 minutes. This design compared the SnPb solder joint against the “backward” solder joint via 17mm and 27mm PBGA packages. The TV3D_C1 design also evaluated the reliability impact among three different types of surface finishes. The three surface finishes evaluated were HASL (Hot Air Solder Level), ImSn (Immersion Tin), and OSP (Organic Soldering Preservative).

The second configuration, TV3D_C2, was liquid-to-liquid thermally shocked between -40ºC to 125ºC with a cycle time of 14 minutes. Using 17mm PBGA packages, the SnPb, “backward” and Pb-free solder joints were evaluated. TV3D_C2 used one type of surface finish, ImAg (Immersion Silver).

The results from this thesis will add valuable information to the limited research performed on hybrid systems exposed to harsh environmental testing. It will also provide insight for the risks involved in mixing Pb-free solder balls with SnPb paste.

CHAPTER 2: LITERATURE REVIEW

This literature review is divided into three sections. The first section, "Background of Electronics Packaging", discusses surface mount technology trends and includes pertinent information regarding passive and active electronic devices. It also addresses the current movement to miniaturize the design footprint of electronic packages while maintaining superior levels of reliability. The second section, "Harsh Automotive Environment", discusses the reliability issues and concerns of electronic packages when they are exposed to extreme conditions (e.g. automotive under-the-hood). Finally, the "Lead-free" portion provides an in-depth review on the current issues surrounding the conversion to lead-free manufacturing.

2.1 Background of Electronics Packaging

The increased density, complexity, functionality, and miniaturization of electronic products in the late 20th century initiated the transition from through-hole to surface mount technology. Through-hole technology is when the components' pins are inserted through the printed circuit board (PCB), while surface mount technology allows for direct mounting onto the PCB. The following advantages were incurred by changing from through-hole to surface mount technology: (1) smaller and lighter electronic components, (2) increased component density through double sided assembly, (3) increased manufacturability because surface tension from the molten solder pulls the component into alignment with the solder pads, (4) enhanced performance because of lower lead resistance and inductance, and (5) improved mechanical performance under shake and vibration conditions [8].

Division of surface mounted electronic packages can be separated into passive and active electrical devices. Passive devices are capable of operating without an external power source and contribute no power increase within a circuit [9]. Resistors and capacitors form the core group of passive devices. Active devices require a power source to operate and have the capability to control voltages and currents within a circuit [9]. Examples of active devices include transistors, integrated circuits (ICs), and microprocessors. To this end, the discussion will focus on active devices.

Depending upon their complexity, active devices can take the shape of a wide spectrum of electronic packages. Active electronic packages can be separated into categories based upon how they are mounted onto the PCB. The majority of the active electronic packages are mounted via J-leads, gull wings, and solder balls [8]. Another mounting terminal includes grooved-shaped terminations called castellations. Castellations are used as terminations for leadless surface mount packages. Each termination type is represented in Figure 3.

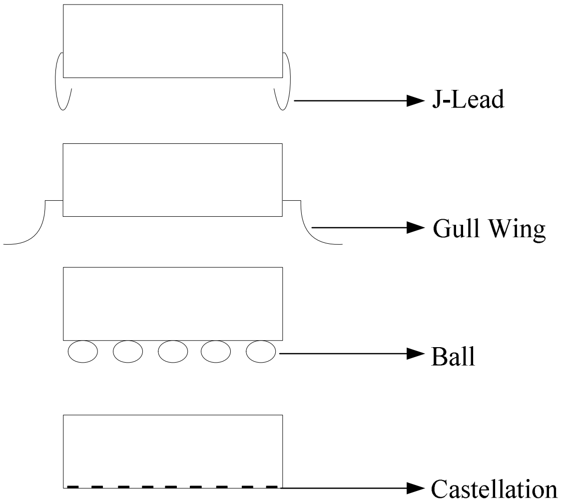


Figure 3: Types of Terminations

Table 2 shows the names, acronyms, termination types, and pictures (Courtesy of National Semiconductor) of commonly used active electronic packages.

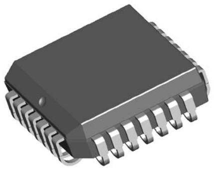
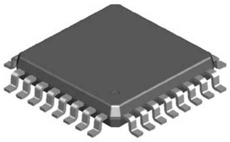
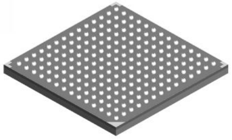
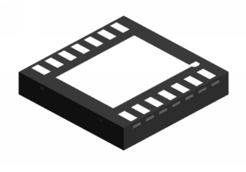
Package Name	Package Acronym	Termination Type	Picture
Plastic Leaded Chip Carrier	PLCC	J-Lead	
Quad Flat Pack	QFP	Gull Wing	
Ball Grid Array	BGA	Ball	
Quad Flat No-lead	QFN	Castellation	

Table 2: Electronic Package Examples

There are tradeoffs between the commonly used “leaded” termination types. J-lead packages are known for their stability because they can withstand the effects of shipping and handling. “J-lead packages have been the real work horse of the surface mount technology [8].” But, J-leads can not be used when the pin count increases above 84 pins [8]. Gull wings are more space efficient than J-leaded packages. Gull wings packages are most commonly used when the pin count increases above 84 pins [8]. The main disadvantage of the gull wing packages is the fragility of their leads which can result in unreliable solder joints. The ball grid arrays (BGA) packages are superior when the pin count is greater than 160 pins [3, 4]. Since the fragile leads are replaced with robust balls, the issue of bent leads becomes obsolete. Due to the reduced signal path, electrical performance increases. The BGA package also has superior ability to self align during the manufacturing process. Since the BGA solder joints are hidden, inspection and rework become troublesome [8]. Table 3, summarizes the key attributes of the previously discussed configurations [8].

Characteristics	**Shape of Terminal**		
	Gull Wing	**J Lead**	**BGA**
Compatibility With High Pin Package Trend	Very Good	Good	Excellent
Package Thickness	Very Good	Good	Excellent
Lead Rigidity	Poor	Very Good	Excellent
Repair/Rework	Good	Very Good	Poor
Ability To Self-Align During Reflow	Good	Good	Excellent
Solder Joint Inspection	Good	Very Good	Poor
Ease of Cleaning	Poor	Excellent	Excellent
Real Estate Efficiency	Poor	Very Good	Excellent

Table 3: Comparison of Terminations

The trend in electronics packaging continually drives to miniaturize electronic devices while increasing their functionality. This trend began at the start of the 1990's and has continued to push onward. In the early 1990's the electronic package of choice for application specific integrated circuits (ASIC) was the quad flat pack (QFP). As the functionality and complexity of the electronic circuits increased, the need for higher I/O (Input/Output) grew. In order for the QFP to satisfy the growing technology trend, the numbers of leads were increased while still maintaining its same footprint. To accommodate the increase in lead count, the lead pitch (distance from the midpoint of two adjacent leads/balls) and lead size were reduced. The reduction in lead size resulted in manufacturing problems that included lead frailty and coplanarity (positioned on the same planar surface) issues. The reduction in lead pitch also tightened the manufacturing process window. If the QFP design was not precise and the manufacturing process was not firmly controlled, higher costs from low product yields would result. Low product yields are detrimental to the high volume manufactures.

With the advent of BGA packages in the mid 1990's, achieving increased functionality while decreasing package form can be realized. Since the balls are populated underneath the package, the BGA package can accommodate high I/O (varying from 16 to 2,400 [8]) within a small footprint. A package size comparison between a QFP and BGA is shown in Figure 4 (Courtesy of Motorola).

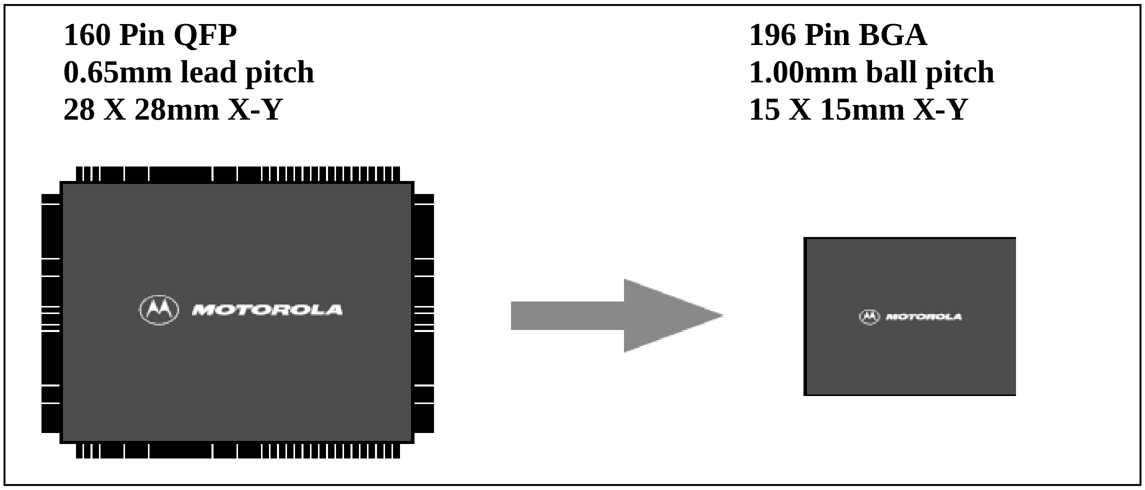


Figure 4: QFP versus BGA

The manufacturing of BGAs creates a higher process yield than QFPs. The higher process yield is directly related to the following factors [8]: (1) BGA packages are compatible with standard surface mount processes, (2) the solder balls are robust and do not bend or break during manufacturing, (3) self alignment can occur when the BGA packages are misplaced by 50%, and (4) relaxed process manufacturing window because of increased pitch between the solder balls/leads.

BGA packages do have drawbacks [8]. Since the solder joints are formed underneath the package, rework and inspection become difficult. The BGA packages are susceptible to moisture absorption that can result in package cracking (i.e. popcorn effect) during the reflow process [8]. Also, under high temperature environments the BGA packages are not as reliable as QFPs. QFPs have more compliant leads that absorb stresses during high temperature applications [2]. Improvements for BGA reliability exists and will be discussed in following sections.

2.2 Harsh Automotive Environment

This section of the literature review investigates the previous research conducted on the reliability of PBGA packages in harsh automotive environments, mainly under-the-hood conditions. Two baseline conditions have to be determined before the PBGA reliability results are presented. These conditions include the definition and reliability requirements for automotive under-the-hood electronics.

2.2.1 Definition & Reliability Requirements

As automobiles have become more advanced, their electronics have evolved. In 1977 the average automobile contained \$110 worth of electronics. By 2003 this number was increased to \$1,510 and by 2013 the estimated value of electronics within the car will reach \$2,285 [1]. In an automobile there are five major electronic systems. These include the engine & power train, chassis & safety, comfort & convenience, displays & audio, and signal communications & wiring harnesses [1]. All of these electronic systems are exposed to a variety of different operating conditions. Table 4 reproduced from [1], summarizes the electronic operating conditions defined by General Motors and Delphi Delco Electronic Systems.

Location	Operating Temperature
Driver Interior	-40ºC to 85ºC
Underhood	-40ºC to 125ºC
On-engine	-40ºC to 150ºC
In the Exhaust & Combustion Areas	-40ºC to 200-600ºC

Table 4: GM & Delphi's Electronic Automotive Environment

To qualify under-the-hood solder joints, reliability standards have been specified. These standards require no failures up to 2,000 cycles or less than 1% failure after 2,500 cycles for temperature cycling between -40ºC to 125ºC [1, 3, 4].

In automotive electronics, there is a continuing trend to reduce the size of electronic packages due to space requirements and material costs. While this trend is occurring, automotive electronics are currently being shifted to under-the-hood locations, specifically the engine or transmission. By integrating controllers on the engine and the transmission modules, the electronic packages will be exposed to high temperature operating conditions. With these factors in consideration, the automotive industry is constantly under pressure to maintain expected levels of reliability while still lowering cost. As a result, the automotive industry has embraced plastic ball grid array (PBGA) packages. PBGA packages deliver small footprints while still maintaining low levels of cost for high volume manufacturing [2].

Unfortunately, trends in electronics packaging are driven by computer and portable devices. The electronic packages in computers and portable devices are not designed to meet harsh environment applications (-40ºC to 125ºC). Therefore, designers and engineers have had to develop innovative ways to extend the life of electronic packages without incurring increased cost to the overall product.

2.2.2 Plastic Ball Grid Array (PBGA) Reliability

The coefficient of thermal expansion (CTE) is defined as the increase in length per unit rise in temperature that can be expressed as 10^{-6}/ºC or ppm/ºC [10]. The key failure mode of PBGA packages originates from the coefficient of thermal expansion mismatch between the silicon die and PBGA substrate [2-4, 11-14]. The CTE mismatches are represented below in the cross section of a PBGA package (Figure 5). The CTE measurements were referenced from [15].

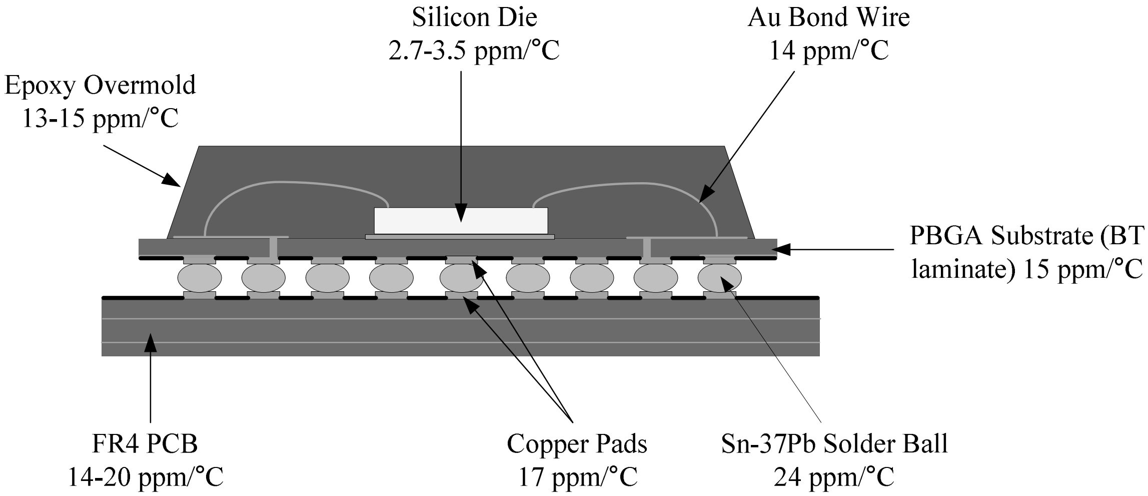


Figure 5: PBGA Cross Section - CTE Measurements

The CTE mismatch is directly absorbed by the solder balls which results in failure from thermal fatigue after repeated cycling. Historically, solder ball failures occur directly underneath the corners of the silicon die [2, 4]. Designers have attempted to increase the reliability of the PBGA by reducing the CTE mismatch between the silicon die and the PBGA substrate.

Different research studies have demonstrated that the reliability of PBGA packages can be affected by altering its design parameters. Altering the design parameters of the PBGA package is an feasible method to improve its reliability [3, 11]. The following design parameters are commonly altered: solder ball stand-off height, solder ball diameter, pitch, solder mask, solder pad diameter, solder ball layout, substrate thickness, silicon die size, encapsulation type, and body size [2, 16]. The majority of the design parameters are interrelated. For example, the solder ball diameter, solder mask, and pad diameter directly affect the stand-off height of the solder ball. Figure 6 shows a cross section of a PBGA package with design parameters that are commonly altered.

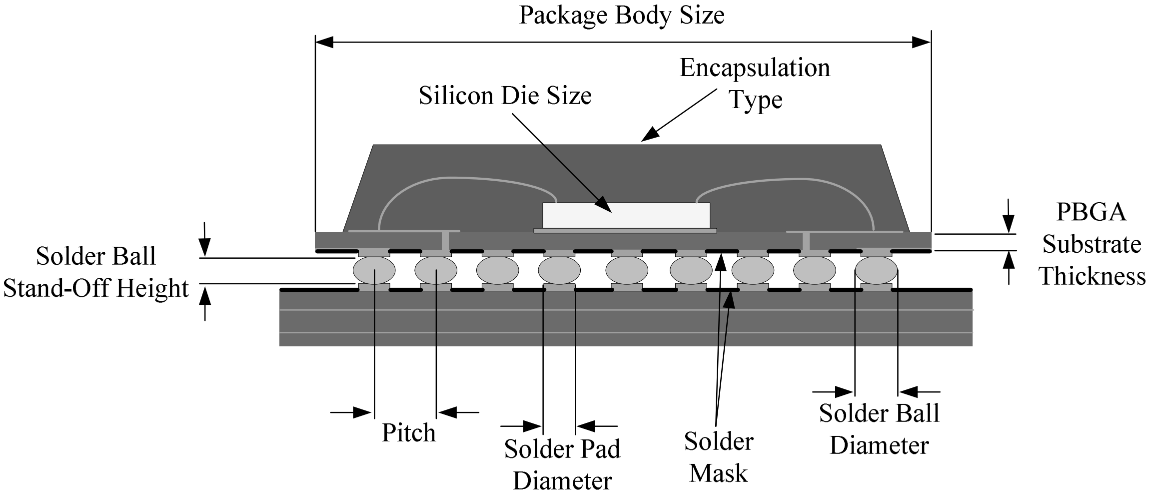


Figure 6: PBGA Cross Section - Altered Design Parameters

The solder pad diameter can be in reference for both the PBGA package and the printed circuit board. There are two types of commonly used solder masks, solder mask defined (SMD) and non solder mask defined (NSMD). Both the SMD and the NSMD pads can be at the PBGA and PCB level. Examples of these two types of solder mask pads are in Figure 7.

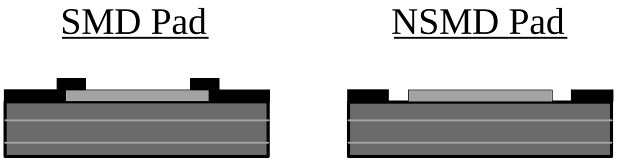
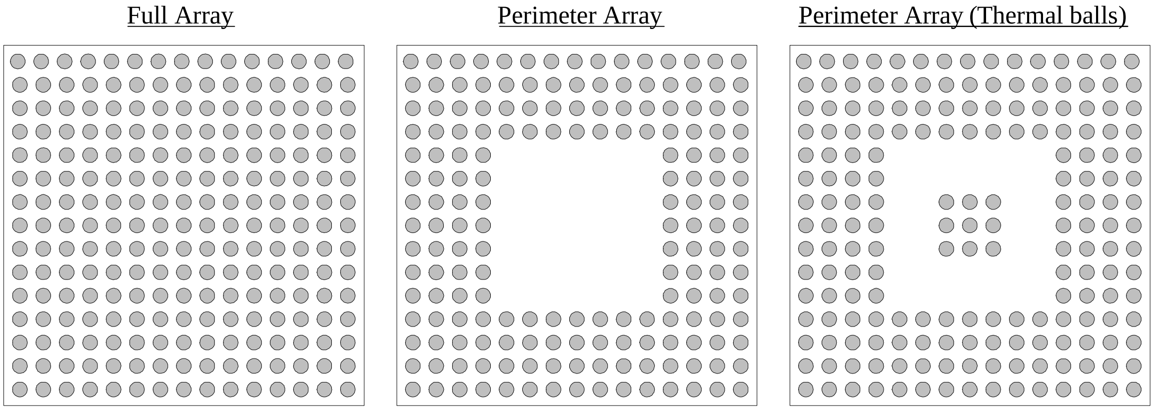


Figure 7: Solder Mask Defined Vs Non Solder Mask Defined

Solder ball placement underneath the PBGA substrate also impacts its reliability. There are three commonly used configurations. The "full array" configuration completely populates the PBGA substrate, while the "perimeter array" populates the outer portions of the substrate. The third combination utilizes the perimeter array but also includes thermal balls. Figure 8 shows the typical solder ball layouts for plastic ball grid array packages.


Full Array

Perimeter Array

Perimeter Array (Thermal balls)

Figure 8: PBGA Solder Ball Layouts

Following is the recent literature on how the above design parameters affect the PBGA reliability.

Mawer et al. [3] invested the reliability of 1.0 and 1.27mm pitch PBGAs for under-the-hood applications. All the PBGA packages used in this research were perimeter arrayed with/without thermal balls. This study incorporated different PBGA combinations including: (1) Body size – 17x17mm, 23x23mm, 27x27mm, & 31x31mm, (2) Pitch – 1.00mm & 1.27mm, (3) Encapsulation type – molded & glob-top, (4) BGA substrate thickness - .36mm & .56mm, (5) Die size & thickness and (6) Solder mask type on the component side. The packages were mounted on a FR4-06 substrate with a HASL (Hot Air Solder Level) surface finish and NSMD pads. The PBGAs were thermally cycled in two types of harsh environments. In the “typical” thermal cycle profile, the temperature extremes ranged from -40ºC to 125ºC with 15 minutes dwells and 15 minute transition times. The more stringent profile had temperature ranges from -50ºC to 150ºC with 15 minutes dwells and 24 minute transition times. While cycling, the PBGA packages were continuously monitored for failure.

Under typical temperature cycling (-40ºC to 125ºC) the NSMD pads on the component increased the life of the 27x27mm packages twofold. When comparing the glob-top and the molded encapsulation type, the glob-top encapsulation significantly decreased the reliability of the 27x27mm package. The reliability of 27x27mm packages with 1.27mm pitch were deemed appropriate for automotive applications. Because the 27x27mm packages consisted of a perimeter array of solder balls, the high concentration of stress underneath the silicon die did not impact the reliability. The 17x17mm package with 1.00mm pitch scarcely met the automotive specifications. The decrease in package size brought the edge of the die closer to the inner row of the perimeter solder balls. In the harsher temperature cycling -50ºC to 150ºC all of the packages failed earlier and could be questionable for automotive applications if requirements became more stringent.

Suhling et al [4] evaluated the under-the-hood reliability of small PBGA packages with increased substrate thickness, NSMD pads for the component, and underfill. Different sized PBGA components were included in this study. These included 15x15mm, 17x17mm, and 27x27mm packages. Both the 15mm and 17mm packages had 1.0mm pitch while the 27mm package had 1.27mm pitch. For each of the packages, the PBGA substrate thickness (.38mm & .56mm) and pad type (SMD & NSMD) were varied. The test board was a 4 layer FR-406 with a HASL surface finish and NSMD pads. The test procedure was a thermal cycling chamber with a temperature range of -40ºC to 125ºC. The cycle time was 90 minutes which included 20 minute dwells at each temperature extreme. The packages were continuously monitored for failure and after 6,000 cycles, the test was terminated.

Suhling et al [4] determined that the reliability of the package without underfill was mainly dependent on package size. The reliability increased as the body size of the PBGA increased. In comparing the 15mm and 17mm PBGAs, the thicker BT substrate significantly increased the reliability. However, without underfill, the smaller sized BGA packages were not suitable for under-the-hood applications. No comparison was drawn between the SMD and NSMD defined pads (component side) because manufacturing issues induced early failures for the SMD pads. With underfill, the reliability of both the 15mm and 17mm PBGA packages increased fourfold and qualified for automotive applications. The underfill acts as a dampening mechanism that absorbs stresses during thermal cycling. Underfill improves the survival life of the smaller BGA components, but at a cost in the manufacturing process: Capital expense, additional manufacturing processes, and increase in cycle times due to the additional process steps which include underfill dispense, underfill flow, and cure [12].

Adams et al. [17] compared the reliability of PBGA packages against the traditional, more reliable gull winged devices, PLCCs and QFPs. At the component side, the pads were SMD. The test matrix is shown below in Table 5

Type	I/O	Body Size (mm)	Pitch (mm)	Solder Ball Layout
PBGA	225	27x27	1.50	Full Array
PBGA	256	27x27	1.27	Perimeter Array
PBGA	361	25x25	1.27	Full Array
PLCC	68	24x24	1.27	N/A
QFP	160	28x28	0.65	N/A

Table 5: Test Matrix – PBGAs, PLCCs, QFPs

The test board was a 4 layer FR-402 with a HASL surface finish and NSMD pads. The electronic packages were thermally cycled with a temperature range of -40ºC to125ºC. The cycle time was one hour, which included 15 minute dwells at each temperature extreme. The packages were continuously monitored for failure and after 11,000 cycles, the test was terminated. The reliability of the 256 BGA, with the perimeter array of solder balls, was comparative with the PLCC and QFP. The reliability of the other BGA packages was 50% less than the gull winged devices. The degradation in reliability of both the 225 and 361 BGA packages can be attributed to the full array solder ball layout. The CTE mismatch between the silicon die and the PBGA substrate prompted early failures located underneath the silicon die.

Evans et al [11] investigated methods to increase the longevity of the PBGA packages for under the hood applications and determine if the reliability of PBGAs could be comparable to PLCCs and PQFPs. The PBGA package tested was a 352 lead, 27x27mm package with a full array solder ball layout. The initial testing (thermal cycling from -40ºC to 125ºC with 10 minute dwell at both temperature extremes & 20 minute transients) indicated that the BGAs were not as reliable as the standard PLCC and PQFP packages. Evans et al [11] concluded the reliability of PBGAs was design dependent and the main cause of failure was the thermal expansion mismatch between the silicon die and the PBGA substrate. The solder balls directly underneath the silicon device corners were the first to fail. To increase the reliability of the PBGA, two improvements were made. First, the PBGA substrate was increased from .36mm to .56mm. Next, the center solder balls were removed and rerouted to the two outer rows of the PBGA. The identical thermal cycle conditions were repeated, and the life of the PBGA increased by 100% making it equivalent with both the PLCC and PQFP packages.

Syed [14] also researched the reliability of a PBGA package when the package substrate thickness was increased and the solder ball array configuration was changed. The testing matrix involved three BGA configurations. The standard configuration had a full array of solder balls, 1.5mm pitch, and BT substrate thickness of 0.36mm. The design alterations stemmed from the standard configuration. The second configuration consisted of a perimeter array instead of the full array, and the third configuration increased the BT substrate thickness to 0.76mm. For all three configurations, the packages had SMD pads. The PBGAs were mounted on a FR-4 with NSMD pads and thermally cycled from -40ºC to 125ºC. The cycle time was approximately one hour, with a 20 minute transition/ramp time and 10 minute dwells. In comparing the number of cycles to first failure, the thicker BT substrate and the perimeter array configurations resulted in an increased life of 82% and 43% respectively over the standard configuration.

Mawer and Cho [18] analyzed the effect of PBGA reliability when the solder pad geometry is altered. The four pad geometry designs that were included are shown below in Figure 9.

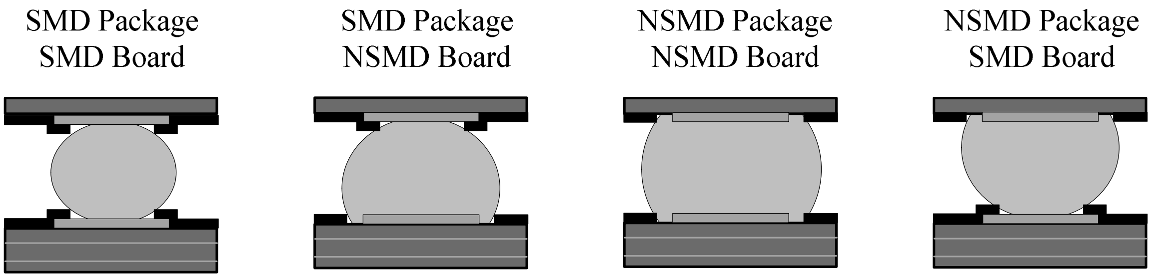


Figure 9: Solder Mask Geometry

For each of the four configurations, the diameter of the board level solder pad was altered. For the NSMD pad, the diameters ranged from 15.5mm to 23mm. For the SMD pad, the diameters ranged from 15.5mm to 23mm. The PBGAs were mounted on a four layer board with a HASL surface finish and thermally cycled from 0ºC to 100ºC with 5 minute dwells and 10 minute transition times. The SMD pads at the package level exhibited significantly lower levels of reliability in comparison with the NSMD pads. In fact, after 15,000 cycles no failures were exhibited on the NSMD package pad with the NSMD board pad. The reason for this improvement was thought to be a solder stress reduction in the NSMD pads. With the NSMD pads, the solder ball was able to "wrap around" the copper pad, thus providing more surface area to absorb the thermal stresses.

In summary, the previous research studies demonstrated that the reliability of the PBGA package is design dependent. There were a variety of specifications altered to increase or decrease the reliability of the PBGA package. Generally, the following factors increased the reliability of the PBGA package: (1) increased PBGA substrate thickness, (2) perimeter arrayed solder ball layout, (3) NSMD pads on the component and board level, (4) underfill, and (5) increased pitch between the solder balls as a result of larger package dimensions. But, all of the research was based upon a tin lead system (interaction between the tin lead solder ball and solder paste). Because of lead-free regulations, the demand for lead-free products is overwhelming.

Following is an evaluation of the lead-free system to determine its impact on reliability of the PBGA packages.

2.3 The Lead-Free System

This section is divided into two segments. The first segment discusses the motivating force for a lead-free system, and the roadmap that will be taken by the United States electronics industry to convert to lead-free manufacturing. The second segment reviews the current reliability of hybrid and lead-free systems for PBGA packages.

2.3.1 Motivating Force & Roadmap

The motivating forces behind the transitioning to lead-free manufacturing can be attributed to the Japanese manufactures, European governmental regulations, and Chinese governmental regulations. Since 1998, Japanese manufactures have been using lead-free soldering in many of their popular consumer products [5]. These products include personal computers, laptops, MiniDisc players, mobile phones, VCRs, and TVs. With the positive results that were recognized in their consumer lead-free products and the adverse environmental effects of lead, the Japanese Electronics Information Technology Industries Association (JEITA) developed a lead-free roadmap. By January 1, 2006, the lead-free conversion for the Japanese electronics industry was expected to be completed. Although most of the Japanese manufactures have converted to a lead-free process, others may be two years behind the 2006 deadline. In Europe there are two lead-free directives/laws that directly affect their electronics industry. The Waste Electrical and Electronic Equipment (WEEE) limits the amount of lead disposed in the environment and became effective on August 13, 2005. The Restriction of the Use of Hazardous Substances (RoHS) eliminates lead in electrical and electronic equipment which takes effect in July 1, 2006. After the RoHS law passed in Europe, the Chinese government approved their version of RoHS that removes lead in electronic products. China's version of RoHS will take effect in March 1, 2007.

Through globalization, the United States electronics manufacturing industry frequently imports electronic devices from China, Europe, and especially Japan. Table 6 shows the end-of-year money spent by US companies on imports (semiconductors & related devices) from Japan, China, and Europe [6].

Cost of Semiconductors & Related Devices Imported Into US (In Billions)					
Location	**2001**	**2002**	**2003**	**2004**	**2005**
Japan	4.72	3.01	2.65	3.13	2.94
China	0.65	0.73	0.85	1.36	1.78
Europe	2.13	1.86	2.10	2.17	2.09
Total	7.50	5.60	5.60	6.66	6.81

Table 6: US Cost – Import Semiconductors

In 2006 and 2007 the electronic components imported from these regions will be lead-free. Thus, the US electronics industry has to prepare to convert to lead-free manufacturing.

The feasibility of the US electronics industry converting directly from the traditional tin-lead system (63Sn-37Pb) to the lead-free system is doubtful. Hybrid systems will emerge since the component suppliers and the assembly manufacturers are not on the same lead-free timetable. See Figure 10 to distinguish the interactions between the supplier and manufacturer for a PBGA package.

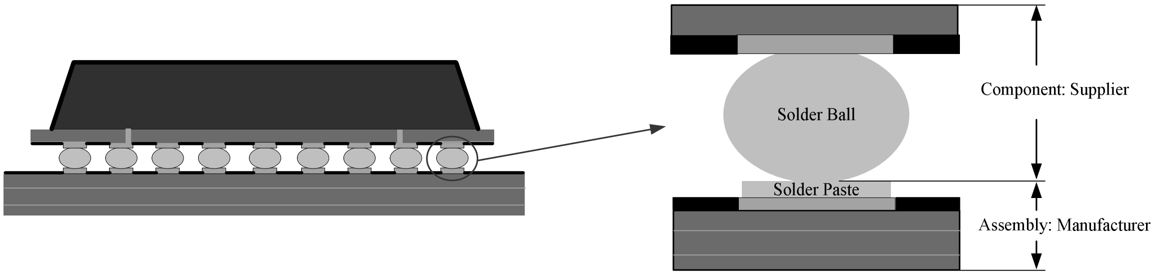


Figure 10: PBGA Supplier & Manufacturer Interactions

Forward and backward compatibility are the two hybrid systems that will emerge [7]. Forward compatibility occurs when the manufacturing assembly process has been converted to lead-free technology (Lead-free solder paste & high reflow temperatures - 260ºC), but the component suppliers are still supplying lead in their terminations/balls. Backward compatibility occurs when the manufacturing assembly process is still using SnPb technology (SnPb solder paste & low reflow temperatures - 220ºC), but the suppliers are distributing lead-free components. Figure 11 shows the four interactions between the solder ball and solder paste that will exist during the conversion to lead-free manufacturing.

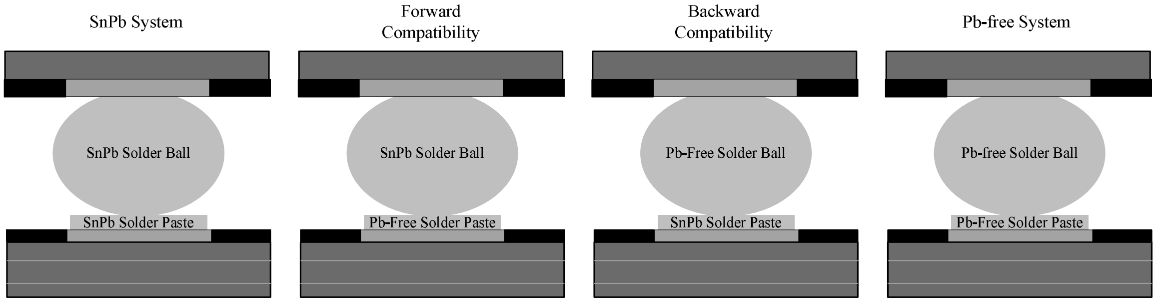


Figure 11: PBGA Interactions

In surface mount technology, the process of converting from the SnPb to the lead-free system can take three separate routes [7, 19]. For a visual representation of the three routes refer to Figure 2 in Chapter 1. Route "A" directly converts SnPb soldering to lead-free soldering. Route "B" transitions from forward compatibility (SnPb terminations/ball with lead-free solder paste) to lead-free soldering, while route “C” transfers from backward compatibility (Pb-free terminations/balls with SnPb paste) to lead-free soldering.

Concerns arise for the Pb-free system and both mixed assemblies. In the Pb-free and forward compatibility system, the Pb-free reflow profile demands high temperatures up to 260ºC because the melting point of Pb-free alloys range from 217ºC to 230ºC. The increase of reflow temperatures directly affects the printed circuit board (laminate) and the plastic surface mounted components. Due to the low T_g of the PCB, the high reflow temperature causes the laminate to become soft and rubbery during reflow. This can cause some components to have poor solder bonds and also permanently warp the PCB [7]. Plastic surface mounted components are susceptible to absorb moisture. The increased reflow temperature intensifys the rate at which the moisture is evaporated out of the components resulting in premature failure due to electronic package cracking/delamination [22]. In the backward compatibility system, the peak temperature for the reflow profile ranges from 215ºC to 220ºC because the melting point of SnPb is 183ºC. Since the reflow temperatures are not high enough to completely melt the Pb-free solder ball, adequate melting of the solder ball is unlikely. Figure 12 depicts the discrepancy between the SnPb and the lead-free reflow profiles.

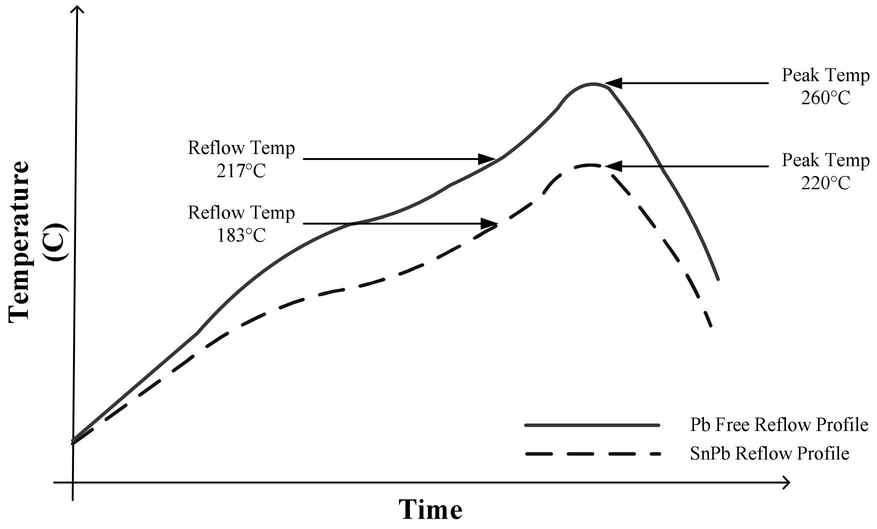


Figure 12: SnPb Vs Pb-free Reflow Profile

In the change to a lead-free system, the National Electronics Manufacturing Initiative (NEMI) was formed in 1999 with the intent to help the electronics industry in North America develop the capacity to produce lead-free products [20]. Their first task was to select a primary Pb-free alloy for reflow applications. NEMI used the following selection criteria to evaluate each lead-free alloy (1) ternary Alloys or less, (2) the alloy should be near eutectic, and (3) not use a patented alloy so industry freedom can be assured. In order to down select the possible number of Pb-free alloys, NEMI evaluated a three year study previously performed by the National Center for Manufacturing Sciences (NCMS). In the NCMS study, 79 lead-free solder alloys were evaluated. After reviewing the study, NEMI selected six alloys for further investigation: Sn-58Bi, Sn-8Zn-3Bi, Sn-3.4Ag-4.8Bi, Sn-3.9Ag-0.6Cu, Sn-3.5Ag, and Sn-0.7Cu.

After the investigation, NEMI concluded that the Bismuth containing alloys were unacceptable for reflow soldering because of the cost and availability of Bismuth. Also, alloys that included Bismuth would result in a decreased melting point when exposed to SnPb coated components and boards. This damaging reaction would result in the reliability degradation of the manufacturing process. Next, Sn-3.9Ag-0.6Cu, Sn-3.5Ag, and Sn-0.7Cu were compared. Sn-3.5Ag and Sn-0.7Cu were eliminated because they exhibited high melting temperatures of 221ºC and 227ºC respectively. Finally, Sn-3.9Ag-0.6Cu (+/- 0.2) was deemed as an appropriate alloy for reflow soldering because of its lower melting point of 217ºC, availability, and comparable, yet limited, reliability results with SnPb solder [20].

Clech [21] stated "Much work remains to be done for the industry know-how on SAC reliability to come up to par with the established SnPb reliability knowledge base." Once NEMI chose their primary candidate for lead-free soldering, the reliability studies of hybrid and lead-free systems ignited.

The reliability issues that are related for the hybrid and Pb-free systems are addressed in the following section.

2.3.2 PBGA Reliability for Lead-Free and Mixed Assemblies

Swan et al [22] tested electronic packages to determine if the increased reflow temperatures would result in manufacturing problems. A lead-free reflow profile with a peak temperature of 260ºC was used to evaluate a variety of electronic components for delamination. These packages included varying sizes of QFPs, BGAs, SOT (Small Outline Transistors), and SOIC (Small Outline Integrated Circuits). After testing, Swan et al [22] concluded that no significant delamination/cracking occurred and these electrical devices are suitable for Pb-free manufacturing.

Syed [23] researched the reliability of a SnPb alloy system versus nine different Pb-Free alloy systems. In this study two different types of BGA packages were used. The packages were 27x27mm PBGA and a 12x12mm FlexBGA packages. The PBGA had 256 I/O, 0.75mm ball size, 1.27mm pitch, and a die size of 10x10mm. The FlexBGA had 144 I/O, 0.45mm ball size, 0.8mm pitch, and a die size of 6.4x6.4mm. The components were mounted on a FR-4 substrate with an OSP (Organic Solderability Preservative) substrate and NSMD pads. Depending on the alloy system, the appropriate reflow profile was used. The SnPb profile had a peak temperature of 220ºC and the Pb-free peak temperatures ranged from 240ºC to 260ºC. Three types of thermal cycling regiments were used: (1) Temperature range from -40ºC to 125ºC with 15 minutes ramps and dwells (2) temperature range from -55 ºC to 125 ºC with 2 minute ramps and 13 minute dwells (3) temperature range from 0 to 100ºC with 10 minute ramps and 5 minute dwells. The components were monitored for failures while they were cycled. Syed [23] concluded that for all three types of ATC test the Pb-free alloys preformed better than the SnPb alloy.

Creep is defined as plastic deformation that occurs at high temperatures under a constant load for an extended period of time [24]. In creep, "high" temperature is defined when the temperature of the material is greater than one-third of its melting point [24]. Because the Pb-free alloys had higher melting temperatures and finer microstructures, the effects of creep during the extreme temperature dwells were minimized. Since creep was minimized, the life was extended for the Pb-free solder joints.

Lee et al [25] assessed the reliability of SnPb and Pb-free PBGA assemblies via thermal cycling, bending, and vibration. In this experiment two types of solder mask defined PBGA packages were used. The 316 I/O plastic ball grid array package had a body diameter of 27x27mm, pitch of 1.27mm, perimeter array layout, 7x7mm die size, and a ball diameter of .762mm. The 313 I/O plastic ball grid array package had a body diameter of 35x35mm, pitch of 1.27mm, staggered full grid array layout, 10x10mm die size, and a ball diameter of .762mm. Depending on the type of assembly, the solder balls were either Sn-37Pb or Sn-3.9Ag-0.6Cu. In this experiment two different types of lead free solder paste were evaluated, Sn-3.9Ag-0.6Cu and Sn-2.5Ag-0.5Cu-1.0Bi. For the tin-lead assembly, the Sn-37Pb solder balls and paste were built with a peak reflow temperature of 220ºC. For the Pb-free assemblies, 240ºC and 260ºC were the peak reflow temperatures. The packages were mounted on a six-layered FR-402 substrate with an ENIG surface finish and NSMD pads. Table 7 shows the assembly matrix for the PBGA packages.

Solder Ball	Solder Paste	Peak Reflow Temperature
Sn-37Pb	Sn-37Pb	220°C
Sn-3.9Ag-0.6Cu	Sn-3.9Ag-0.6Cu	240°C
Sn-3.9Ag-0.6Cu	Sn-2.5Ag-0.5Cu-1.0Bi	240°C
Sn-3.9Ag-0.6Cu	Sn-3.9Ag-0.6Cu	260°C
Sn-3.9Ag-0.6Cu	Sn-2.5Ag-0.5Cu-1.0Bi	260°C

Table 7: PBGA Assembly Matrix

Once the packages were assembled, they were subjected to thermal cycling, bending, and vibration. The air-air thermal cycling had a temperature range of -40ºC to 125ºC with 15 minute dwells and transition times. In the three-point bend test, the two end supports were 100mm apart and the loading stroke applied was 0.025 mm/s. The vibration testing was conducted for six hours with frequencies ranging from 20 – 2,000 Hertz. For all three tests, the PBGA packages were monitored for failures.

After the tests were completed, Lee et al [25] summarized the results accordingly. In the thermal cycling test the following results were extracted (1) regardless of solder alloy and reflow temperature, the solder joint fatigue life of the smaller package (27x27mm) was longer than the larger package (35x35mm). This can be attributed to the perimeter array design of the solder balls and (2) the reliability of the lead-free solder joints were significantly better than the SnPb solder joints. This was independent of solder materials, package size, and peak reflow temperature. In the 3-point bend test, the SnPb assembly and the Pb-free assemblies with peak reflow temperature of 260ºC were equivalent. In the vibration testing of six hours, no failures occurred across the matrix.

Handwerker et al [26] compared the reliability and the microstructures of the mixed (Forward compatibility), Pb-free, and SnPb solder joints for six electronic packages. These six packages included a 48 I/O thin small outline package (TSOP) with Ni-Pd and Sn-10Pb finishes, 2512 resistors with pure Sn and SnPb finishes, 169 I/O & 208 I/O chip scale packages (CSP), 256 I/O PBGA, and a 256 I/O ceramic ball grid array package (CBGA). The CSPs had a pitch of 0.8mm, while the BGAs had a pitch of 1.27mm. The CSP and BGA packages had Sn-4Ag-0.5Cu and Sn-37Pb solder balls. The solder paste used in this experiment was Sn-37Pb and Sn-3.9Ag-0.7Cu. The components were populated onto an eight layered FR-4 substrate with an immersion silver surface finish. The mixed and Pb-free solder joints used a Pb-free profile, while the SnPb solder joints used a SnPb profile. Two accelerated thermal cycling profiles were used. The two temperature profiles, -40ºC to 125ºC and 0ºC to 100ºC, incorporated five minute dwells at each temperature extreme. The components were monitored for failures while they were cycled.

Once the tests were terminated, the reliability of the three solder joint combinations was determined. Using 95% confident bounds on the characteristic life, the mixed and the lead-free solder joints were compared to the SnPb solder joint where (0) was equivalent, (+) was superior, and (-) was inferior. Table 8, recreated from [26], shows the reliability of the mixed (forward compatibility) and Pb-free system in comparison with the SnPb system.

Component	**-40°C to 125°C**			**0°C to 100°C**		
	SnPb	Forward	Pb-Free	SnPb	Forward	Pb-Free
48 TSOP	0	-	0	Not Tested		
2512 Resistor	0	0	0	Not Tested		
169 CSP	0	+	+	0	0	+
208 CSP	0	0	+	0	+	+
256 PBGA	0	0	0	0	0	0
256 CBGA	Not Tested			0	-	+

Table 8: Reliability Comparison – Forward & Pb-free Vs SnPb

The lead free system solder joints were equivalent to the SnPb system, but the "forward" system was unclear about its reliability [26]. In comparing the PBGA package, no significant difference existed in the characteristic life between all three combinations. There were no pronounced differences in the solder joint geometry among the three combinations, and the failure mechanism was the same for all three solder combinations. The common failure mechanism included cracks propagating across the solder ball on the component side.

Nurmi and Ristolainen [27] evaluated the reliability of mixed (Forward compatibility), Pb-free, and SnPb solder joints using a solder mask defined 151 I/O PBGA package. The PBGA package had a 1.0mm pitch with a ball diameter of 0.30mm. The solder balls were either Sn-36Pb-2Ag or Sn-3.8Ag-0.7Cu. The solder paste used in this experiment was Sn-37Pb and Sn-3.8Ag-0.7Cu. The PBGA packages were populated onto a solder mask defined FR-4 substrate with both OSP and ENIG (electroless nickel immersion gold) surface finishes. The two profiles used were dependent upon the type of solder paste used. For both the mixed (forward) and Pb-free system a Pb-free reflow profile was used. The lead-free profile included a max temperature of 251ºC and 47 seconds above the liquidus temperature of 217ºC. The SnPb assembly used the typical SnPb profile with a max temperature of 227ºC and 89 seconds above the liquidus temperature of 183ºC. The PBGA packages were thermally cycled in an air to air chamber with a temperature range from -40ºC to 125ºC. The cycle time was 30 minutes with 14 minute dwells at both temperature extremes and 1 minute transition times. The components were monitored for failures while they were cycled. After 2,500 cycles, complete failure occurred throughout the different assemblies. The components were removed from test and the reliability results were summarized. Nurmi and Ristolainen [27] established that the reliability of the mixed and Pb-free systems were comparable with the SnPb assembly. In fact, on the OSP surface finish, the reliability of the mixed assembly out-performed both the SnPb and Pb-free systems. In conclusion, the authors stated that “it can be assumed that the tin-lead BGA component soldered with lead-free solder paste withstands the temperature cycling stress as well as pure tin-lead systems” [27].

Bath et al [28] used PBGA packages to compare the reliability of a Pb-free system with a “backward” system. The PBGA packages were subjected to air-air thermal cycling and a four point monotonic bend test. The 676 I/O PBGA package had the following characteristics: 27x27mm body size, 1.0mm pitch, full grid array of solder balls, 0.6mm ball diameter, 17x17mm die size, and SMD pads. The solder balls consisted of Sn-4Ag-0.5Cu. The types of solder paste included were Sn-3.9Ag-0.6Cu and Sn-37Pb. The test board was NSMD with nine layers and had an OSP surface finish. For the "backward" system, two types of reflow profiles were applied. Table 9 represents the assembly matrix for this research endeavor.

Type	Assemby	Peak Reflow Temperature	Time Above Liquidus
A	Backward	205°C	65 sec above 183°C
B	Backward	214°C	76 sec above 183°C
C	Pb-Free	237°C	59 sec above 217°C

Table 9: Assembly Matrix

After assembly, the boards were placed in two different thermal cycling profiles which ranged from 0°C to 100°C. The first profile was 40 minutes with 10 minute dwells and 10 minute transition times. The second profile was 90 minutes with a 60 minute dwell on the hot side, 10 minute dwell on the cold side, and 10 minute transition times. Types "B" and "C" were cycled in both ATC profiles, while Type "A" was only cycled in a 40 minute ATC profile. The components were continuously monitored for failure. After 6,000 cycles, both ATC tests were terminated. Types "B" and "C" were also used in the 4 point monotonic bend test.

For both the long and short dwells, failure cracking initiated near the component side of the solder joint close to the intermetallic. This was consistent with the lead-free and "backward" assemblies. Also, the failure locations for the PBGA package appeared to be near the edges of the die. In the short dwell testing, the reliability of both mixed samples was significantly worse than the Pb-free system. The reduced fatigue life can be attributed to poor solder joint mixing during reflow. The peak temperatures of both reflow assemblies never reached the melting point of the Pb-free solder ball. But in the long dwell testing, the Pb-free system (Type "C") and the "backward" assembly (Type "B") showed no statistical difference. When the dwell times are compared, the longer dwell time decreased the characteristic life of both types of assemblies. This is a direct result of creep damage that is incurred by a longer dwell time. In conclusion, the ATC reliability results for the two mixed combinations were worse than the lead-free combination [28]. In the bend testing, the most prominent failure was circuit trace lifting from the copper pad. Bath et al [28] stated the failure mode and fracture strength characteristics were essentially identical between the lead-free system and "backward" system.

Hau et al [29] evaluated the reliability of a fine pitch PBGA package with "backward" technology by changing the assembly parameters. The 9.0x7.7mm BGA package had 40 I/O, 0.5mm pitch, and a ball diameter of .30mm. The solder balls were Sn-4Ag-0.5Cu and the solder paste was Sn-37Pb. The packages were mounted onto a six layer FR-4 board (NSMD pads) with OSP and NiAu surface finishes. The assembly process was altered by changing the reflow profile, peak temperature, and the time above liquidus (TAL). The soak and ramp profile where the types of reflow profiles used. In soak profile, the temperature was ramped to a predetermined point. The board was then soaked at this temperature to equilibrate the temperature across the board and burn off solder paste impurities. A ramp profile did not include soaking the board and was mainly used to increase throughput. The two peak temperatures selected where 208ºC and 222ºC, and the TAL included 60-90 seconds and 90-120 seconds. In this context, the time above liquidus was referring to the SnPb melting point of 183ºC.

Once assembled, the boards were thermally cycled from -40ºC to 125ºC. The cycle time was 30 minutes which included a 2 minute transition time between temperature zones. The test goal was less than 5% failure at 800 cycles. The results of the test were represented as to whether the components passed/failed after 800 cycles. The summary of the results is in Table 10.

Surface Finish	Profile Type	Peak Temp	TAL (Sec)	Pass/Fail
NiAu	Ramp	208°C	60-90	Fail
		222°C	60-90	Pass
			90-120	Pass
	Soak	208°C	60-90	Fail
		222°C	90-120	Pass
OSP	Ramp	208°C	60-90	Fail
		222°C	60-90	Pass
	Soak	208°C	60-90	Pass
		222°C	90-120	Pass

Table 10: Summary of Results

As seen in the above table, the peak temperature and time above liquidus directly impacted the reliability of the BGA. The authors noted that the reliability degradation is directly related to the lack of solder mixing in the joint. Hau et al [29] stated that if the Pb-free ball completely mixes with the SnPb paste then the reliability goals can be met. But, one of the peak temperatures of 208ºC located on the OSP surface finish passed the reliability criteria. This data could be misleading because the full statistical description of this combination was not presented. It could be possible that after the 800th cycle this combination readily failed. The same argument can be made in predicting the life of all of the BGA combinations because the full statistical description was not given.

In a follow-up study Hua et al [30] furthered the research of backward compatibility. The packages used in this study were a 196 I/O PBGA and a 544 I/O

PBGA. The 196 I/O PBGA had a body size of 15x15mm with a 1.0mm pitch. The 544 I/O PBGA had a body size of 35x35mm with a 1.27mm pitch. Both of the PBGA components had SMD pads. The ball diameters for the 544 I/O and the 196 I/O PBGA packages were .40mm and .60mm respectively. The packages were assembled onto an eight layer FR-4 substrate (NSMD pads) with OSP and HASL surface finishes. Once again, the assembly process was altered by changing the reflow profile, peak temperature, and the time above liquidus. The same reflow profiles and peak temperatures were used, but the TAL was changed to 30-40 seconds and 60-90 seconds. As a control, a SnPb system was also built. The boards were thermally cycled from -40ºC to 125ºC with the same cycle time of 30 minutes. The components were continuously monitored for failure. As in the previous study, the reliability degradation of both packages could be attributed to the lower reflow temperatures that resulted in insufficient mixing of the "backward" solder joint. But, the incomplete mixing was more prevalent for the 35x35mm packages. When the peak reflow temperature was increased the reliability results for the "backward" assembly became comparable with SnPb system because complete mixing of the solder joint occurred.

Finally, a comprehensive study was performed by Mawer and Levis [13] that compared all four alloy systems. In this research a 324 I/O PBGA package was evaluated. The characteristics for this PBGA package are as follows: 23x23mm body size, 1.0mm pitch, perimeter arrayed solder balls, .60mm ball diameter, 10x10mm die size, .56mm substrate thickness, and solder mask defined pads. The solder balls were either Sn-36Pb-2Ag or Sn-3.5Ag. The solder paste used was Sn3.8-Ag-0.7Cu or Sn-37Pb. The package was assembled on a four layered FR-406 substrate (NSMD pads) with an ENIG surface finish. For the SnPb alloy system, the max reflow temperature was 215ºC. For the Pb-free, “forward”, and “backward” systems the max reflow temperature was 236ºC. Once assembled, the boards were air-air thermally cycled in two different types of environments. The first thermal environment had a temperature range from -40ºC to 125ºC with a 60 minute cycle time. The cycle time included 15 minute dwells and transition times. The second thermal environment had a temperature range of -50ºC to 150ºC with a 78 minute cycle time. The cycle time included 15 minutes dwells and 24 minute transition times. The PBGA packages were continuously measured for failure during the thermal cycling.

For both ATC testing conditions the same failure trends were exhibited. The first two combinations that failed were the SnPb and the “forward” systems. There was no significant difference of characteristic life between the two previously mentioned combinations. In both tests, the characteristic life of Pb-free system was doubled in comparison with the SnPb and the “forward” systems. Interestingly, the “backward” system was the best performer. After 5,619 cycles in the -50ºC to 150ºC thermal environment, the “backward” system had exhibited no solder joint failures, and after 9,187 cycles in -40ºC to 125ºC thermal environment, only one failure (7,555 cycles) had occurred.

Using a dye penetration test, Mawer and Levis [13] concluded that the majority of the solder ball failures occurred in the outermost perimeter row next to the corners. This reflects an increased distance from the neutral point (DNP) due to the CTE mismatch between the BGA substrate and the PCB substrate [13]. The increased survival life of the Pb-free and the “backward” systems can be attributed to the creep resistance exhibited by their alloy system. Also the grain structures of these two systems were finely distributed which inhibited crack growth through the solder ball.

From this extensive literature review some general conclusions can be drawn about previous research work that has been performed on the mixed and lead free systems. These conclusions are as follows: (1) the PCB and the electronic components were able to withstand the higher reflow temperatures that are associated with Pb-free alloys, (2) the lead-free solder system is superior in comparison with the SnPb system, (3) the “forward” system was comparable to the SnPb system, and (4) the reliability of the “backward” system was dependent upon the assembly parameter, mainly the peak reflow temperature. If the reflow temperature is below the melting point of the Pb-free solder ball, poor reliability results will occur. When the peak temperature is above the melting point of the Pb-free solder ball, the reliability is superior in comparison with the SnPb solder joint.

CHAPTER 3: RESEARCH METHODOLOGY

This chapter discusses the research methodology applied to evaluate the reliability of Pb-free PBGAs assembled on SnPb solder paste. The research methodology includes a description of the test vehicles, electronic packages, assembly processes, and testing methods.

3.1 Test Vehicle Design (TV3D)

The design of the test vehicle, TV3D, was a mutual effort between Siemens VDO Automotive located in Huntsville, AL. and the Center for Advanced Vehicle Electronics (CAVE) located in Auburn University, AL. The test vehicle was an FR-406 glass epoxy laminate with a glass transition temperature (T_g) of 170ºC and measured 152.4 x 101.6mm with a thickness of 0.775mm. The substrate was four-layered with NSMD pads. The copper pads were surface finished with HASL, OSP, Immersion Tin (ImSn), or Immersion Silver (ImAg). A common ground for all the packages was incorporated into the design of TV3D. To monitor the electronic packages during testing, copper traces routed the signals to the edge of the PCB. Figure 13 shows the unpopulated TV3D test vehicle.

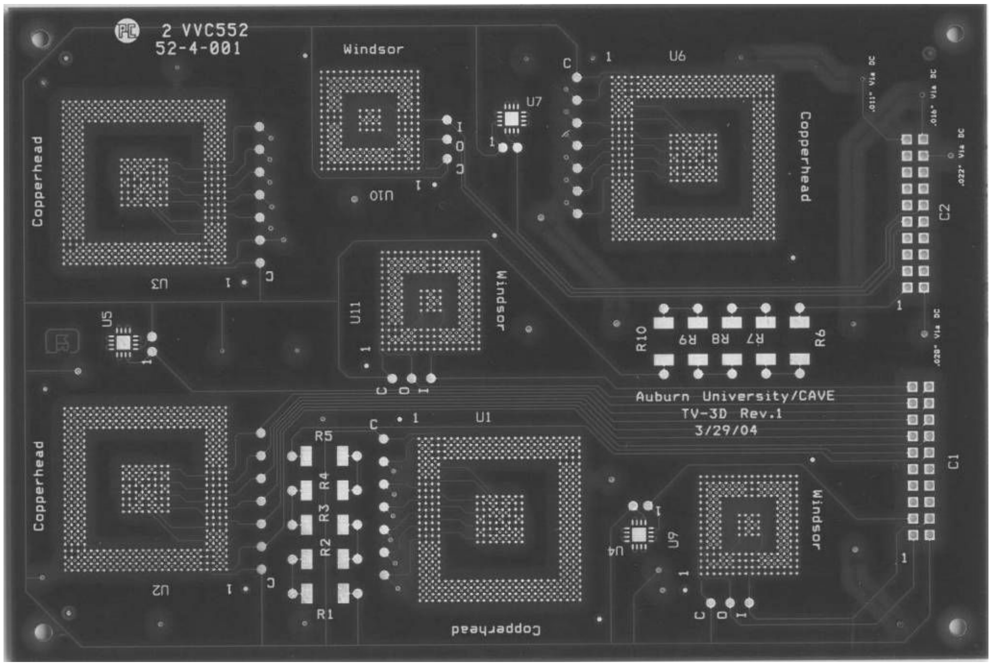


Figure 13: Unpopulated TV3D Test Vehicle

From this test vehicle, two different combinations were constructed dependent upon the types of electronic packages populated onto the substrate. To distinguish between the two test vehicles, they were named TV3D Configuration 1 (TV3D_C1) and TV3D Configuration 2 (TV3D_C2).

3.1.1 TV3D Configuration 1 Design

TV3D_C1 was populated with both active and passive devices. The active components included QFNs and a mixture of different sized SnPb and Pb-free PBGA packages. The QFNs measured 4x4x0.75mm (LxWxH) and had a termination alloy of Sn-15Pb. The smaller PBGA packages measured 17x17mm with a height of 1.80mm and had either Sn-36Pb-2Ag or Sn-3.8Ag-0.7Cu solder balls. The larger PBGA packages measured 27x27mm with a height of 2.25mm and had either Sn-36Pb-2Ag or Sn-3.8Ag-

0.7Cu solder balls. The resistors (passive devices) measured 6.3x3.2x0.71mm and had a termination alloy of Sn-10Pb. The industry standard naming convention for resistor sizes describes the length and width of its body in hundredths of an inch. To this end, the resistors used in this research will be referred to as 2512 resistors (i.e. the resistor measured 0.25"x0.12"). The 2512 resistors were mounted in banks that consisted of five resistors placed in series. Hence, if one 2512 resistor failed, then the bank failed. The 2512 resistors were incorporated for control purposes to ensure that their reliability data matched previous testing at CAVE.

OSP, HASL, and ImSn were the three different surface finishes incorporated into this test vehicle. The components were assembled onto the PCB with Sn-37Pb solder paste. To ensure that the Pb-free BGA packages would properly wet during assembly, an aggressive SnPb profile was used. The TV3D_C1 design compared the SnPb system against the "backward" system with different types of surface finishes. Due to the limited availability of PBGA packages with lead free solder balls, the Pb-free solder joint combination was excluded. Table 11 and Figure 14 show a summary of the component matrix and populated test vehicle.

Package Type	Body Size (LxWxH)	Termination Alloy	QTY
PBGA	27x27x2.25mm	Sn-36Pb-2Ag	2
PBGA	27x27x2.25mm	Sn-3.8Ag-0.7Cu	2
PBGA	17x17x1.80mm	Sn-36Pb-2Ag	2
PBGA	17x17x1.80mm	Sn-3.8Ag-0.7Cu	1
QFN	4x4x0.75mm	Sn-15Pb	3
2512 Resistor	6.3x3.2x0.71mm	Sn-10Pb	10

Table 11: TV3D_C1 Component Matrix

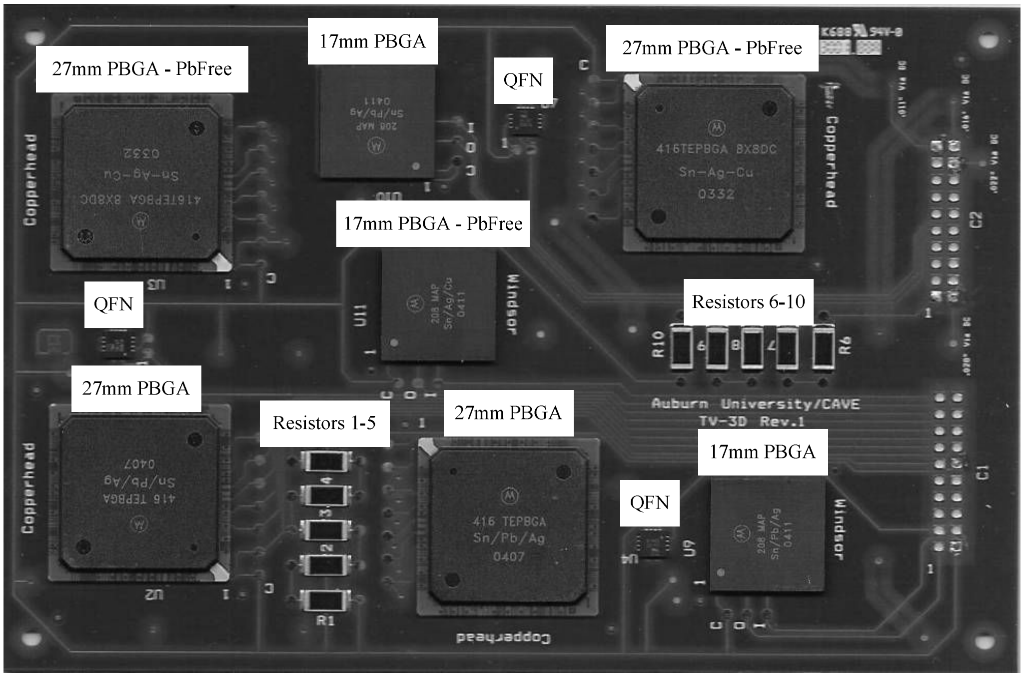


Figure 14: TV3D_C1 Test Vehicle

3.1.2 TV3D Configuration 2 Design

TV3D_C2 was populated with two 2512 resistors banks and two identical 17mm PBGA packages. These electronic packages were identical to the ones used in TV3D_C1 except the resistors were terminated with pure Sn instead of Sn-10Pb. Both 17mm PBGA packages mounted onto the board had either Sn-36Pb-2Ag or Sn-3.8Ag-0.7Cu solder balls. Immersion Silver (ImAg) was the only surface finish evaluated in this test vehicle. Depending upon the solder paste and reflow profile, five different variations of TV3D_C2 were constructed to match the five different PBGA assemblies. Table 12 summarizes the five combinations of PBGA assembly.

Combination	Technology Type	Solder Balls	Solder Paste	Reflow Profile Type
1	Lead Free	Sn-3.8Ag-0.7Cu	Sn-3.0Ag-0.5Cu	Pb-Free
2	Backward Compatibility	Sn-3.8Ag-0.7Cu	Sn-37Pb	Pb-Free
3	Backward Compatibility	Sn-3.8Ag-0.7Cu	Sn-37Pb	SnPb
4	Traditional (SnPb)	Sn-36Pb-2Ag	Sn-37Pb	SnPb
5	Traditional (SnPb)	Sn-36Pb-2Ag	Sn-37Pb	Pb-Free

Table 12: TV3D_C2 PBGA Assemblies

The design of TV3D_C2 was able to compare a SnPb system, lead-free system, and a "backward" system (with SnPb and Pb-free profile) of 17mm PBGA packages. Figure 15 shows the populated test vehicle.

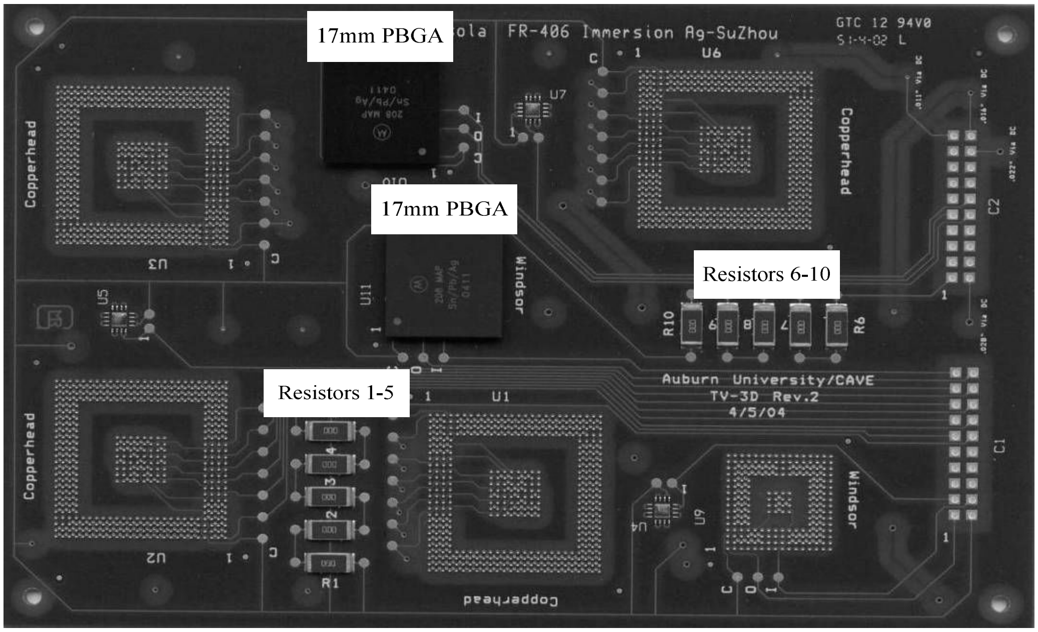


Figure 15: TV3D_C2 Test Vehicle

3.2 Electronic Package Descriptions

As stated earlier, there were two types of PBGA packages with either Sn-36Pb-2Ag or Sn-3.8Ag-0.7Cu solder balls. Both PBGA packages had a Bismaleimide Triazine (BT) substrate. The 17mm PBGA packages had the BT substrate completely encased by the epoxy overmolding, while the 27mm PBGA packages left the edges of the BT substrate exposed. In both PBGA packages the silicon die was attached with silver adhesive. Gold wire bonds connected the die to the solder balls through copper plated holes called vias. Table 13 distinguishes the characteristics between the two PBGA packages.

Characteristics	17mm PBGA	27mm PBGA
Body Size (LxWxH)	17x17x1.80mm	27x27x2.25mm
Ball/Lead Count	208	416
Pitch	1.0mm	1.0mm
Solder Ball Diameter	0.6mm	0.6mm
Copper Pad Diameter	0.5mm	0.5mm
Pad Geometry	SMD	SMD
BT Substrate Thickness	0.32mm	0.56mm
Silicon Die Size (LxWxH)	7.2x6.8x0.36mm	7.8x7.8x0.36mm

Table 13: 17mm & 27mm PBGA Design Characteristics

Even though the body sizes for the PBGA packages were significantly different, their pitch, solder ball diameter, copper pad size, and pad geometry were identical. Figure 16 shows the cross sections of both PBGA packages.

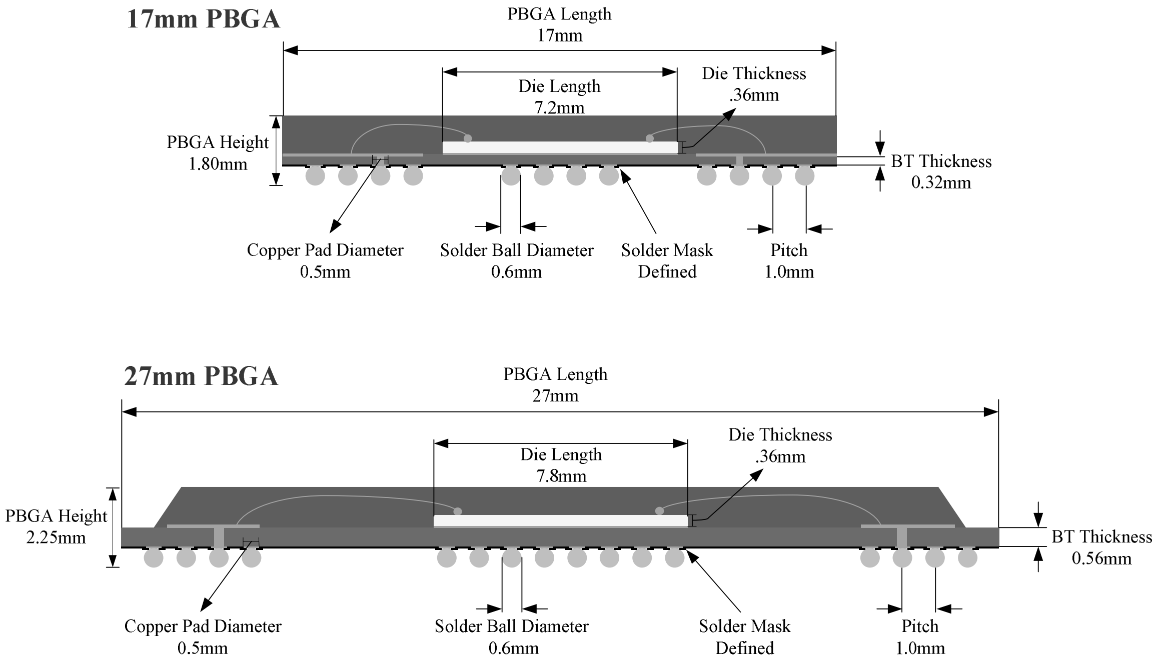


Figure 16: 17mm & 27mm PBGA Cross Sections

Both packages had a perimeter array solder ball layout with thermal solder balls. The 17mm PBGA had a 16x16 perimeter array of solder balls four rows deep and a 4x4 array of thermal solder balls. The 27mm PBGA had a 26x26 perimeter array of solder balls four rows deep and an 8x8 array of thermal solder balls. Figure 17 presents the solder ball layouts and the silicon die outline for both PBGA packages.

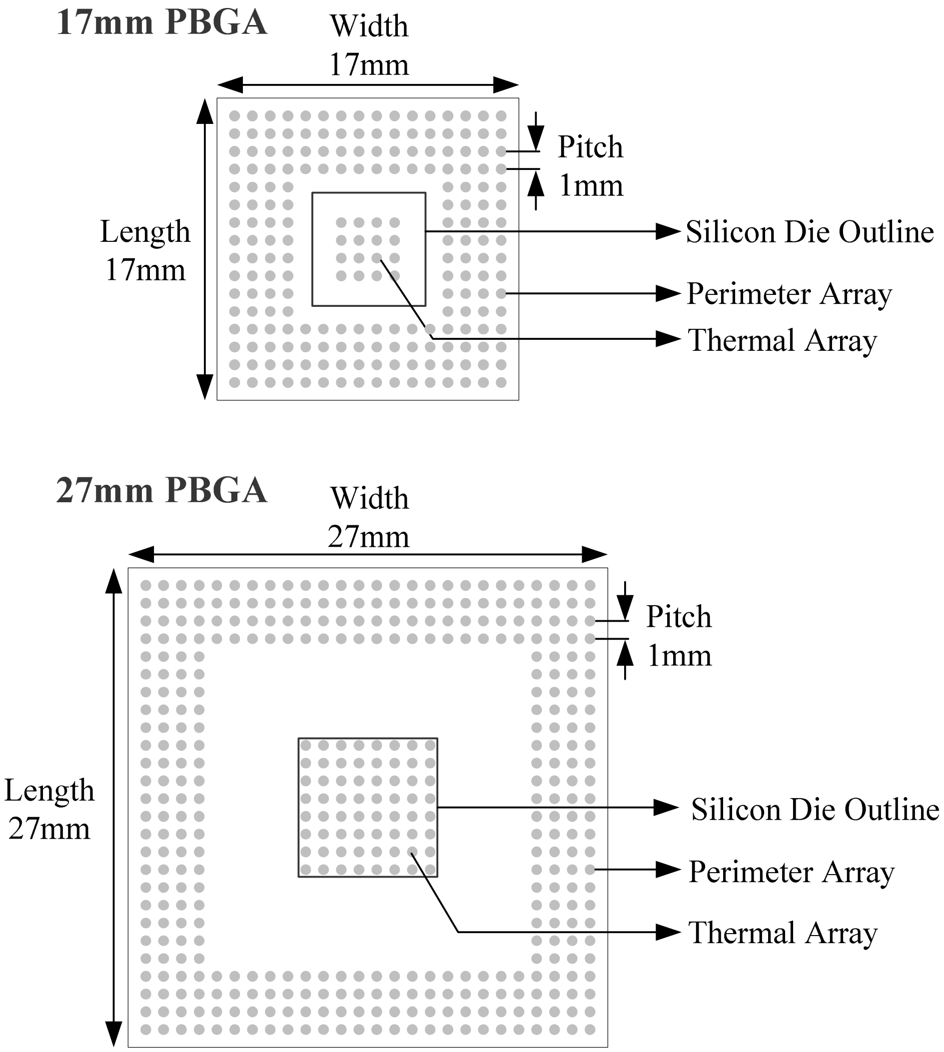


Figure 17: 17mm & 27mm PBGA Solder Ball Layout

The four perimeter rows of both the 17mm and 27mm PBGA were daisy-chained (i.e. if one of the solder balls within the four perimeter rows failed then the package failed) The inner rows (thermal balls) were structured with the same functionality.

The quad flat no-lead (QFN) package was the other active device used in this research. The QFN package was included into the test matrix based upon there rising popularity because of their small footprint and thermal performance. The QFNs measured 4x4mm with a height of 0.75mm. Unlike the BGA design, the QFN packages were leadless. These packages had copper lands plated with Sn-15Pb. The QFN had 16 total lands (4 per side) with a pitch of 0.65mm. Like the BGA, the copper lands were daisy chained. (Reference Figure 18 for side view of the QFN).

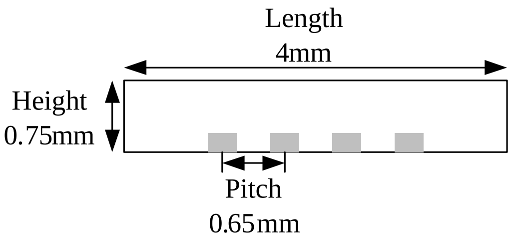


Figure 18: QFN Dimensions (Side View)

Since the QFN did not have leads/balls, its stand-off height in relation to the PCB was minimal. The reduced stand-off height caused increased internal heating. To aid in reducing the internal temperature of the package, the silicon die was mounted directly onto a copper thermal slug. The copper slug provided a heat sink to dissipate the heat away from the QFN. The silicon die measured 1.45x1.45x0.20mm and was wire bonded to the copper lands and the thermal slug. (Reference Figure 19 for the cross section of the QFN).

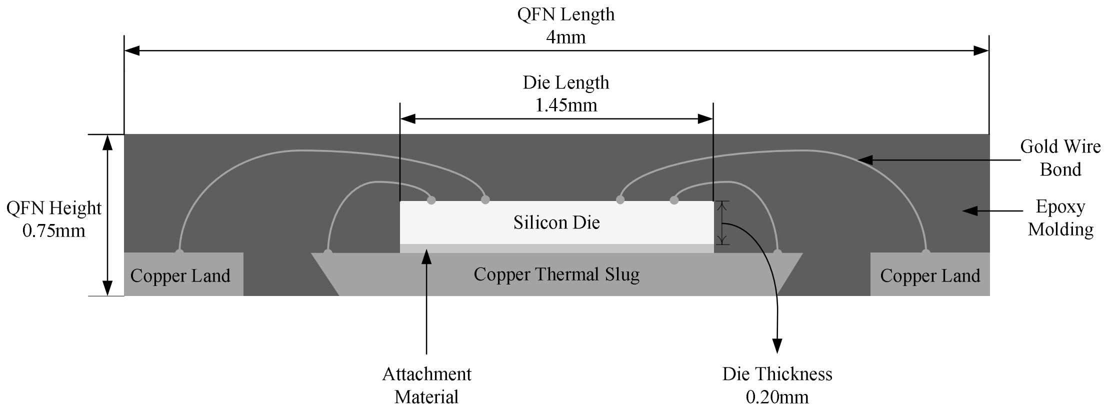


Figure 19: QFN Cross Section

For an additional reference, Figure 20 provides the underside/bottom view to illustrate the geometry of the copper lands and copper slug.

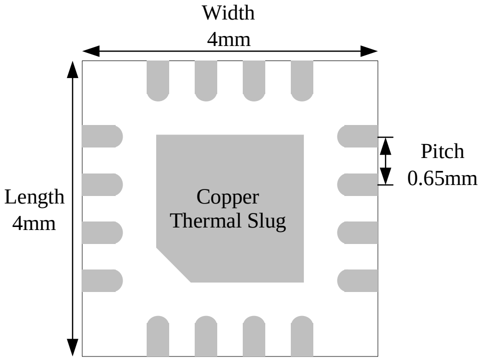


Figure 20: QFN Underside View

The thick film 2512 resistors were the only passive devices tested. The thick film resistors consisted of a resistive element (Ruthenium Dioxide) mounted onto a ceramic substrate composed of high purity alumina [8]. To protect the resistive element, the resistor was covered with a protective coating (glass passivation). The resistance value of the 2512 resistor was zero ohms with a tolerance of +5%. The 2512 resistor measured 6.3x3.2mm with a height of 0.71mm. The termination alloy was either Sn-10Pb or pure tin depending on the test vehicle configuration. Figure 21 is an isometric view of the 2512 resistor while Figure 22 shows the cross section of the resistor.

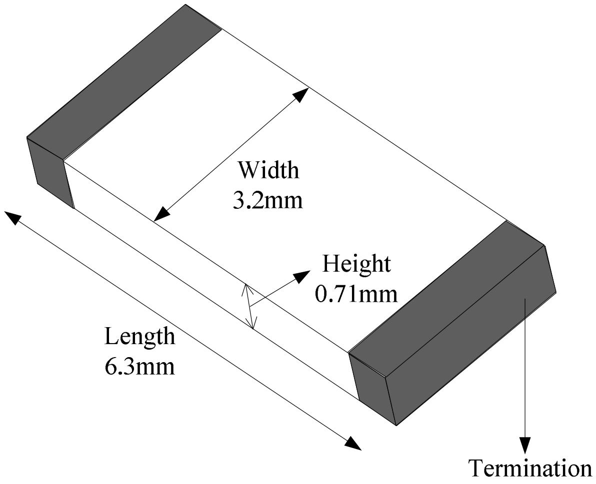


Figure 21: 2512 Resistor Isometric View

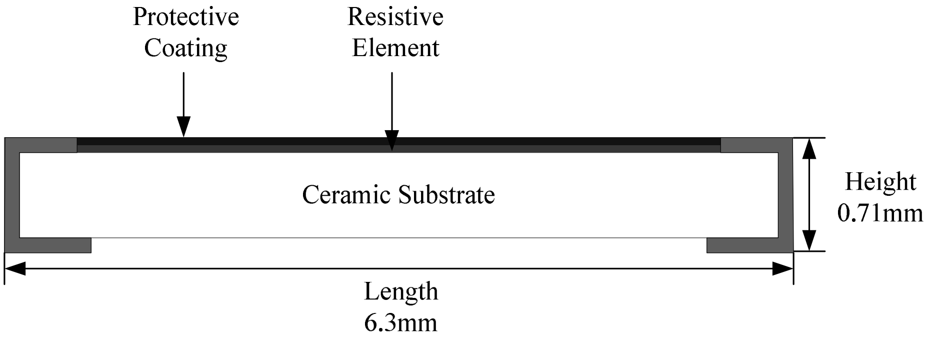


Figure 22: 2512 Resistor Cross Section

Regarding the electronic components, Table 14 provides a summary of all the pertinent design specifications previously discussed.

Package Type	Body Size (LxWxH)	Termination Alloy	Silicon Die Size (LxWxH)	Lead Count	Pitch
PBGA	27x27x2.25mm	Sn-36Pb-2Ag Sn-3.8Ag-0.7Cu	7.8x7.8x0.36mm	416	1.0mm
PBGA	17x17x1.80mm	Sn-36Pb-2Ag Sn-3.8Ag-0.7Cu	7.2x6.8x0.36mm	208	1.0mm
QFN	4x4x0.75mm	Sn-15Pb	1.45x1.45x0.20mm	16	0.65mm
2512 Resistor	6.3x3.2x0.71mm	Sn-10Pb 100Sn	N/A	2	N/A

Table 14: Electronic Package Summary

3.3 Assembly Processes

Both test vehicles, TV3D_C1 and TV3D_C2, were fabricated in CAVE's surface mount assembly lab via a MPM screen printer, ACM placement machine, and a Heller 1800 EXL reflow oven. Because this research was a joint effort with Siemens VDO Automotive, the electronic packages and the printed circuit boards were supplied by Siemens. Siemens also provided CAVE with ACM placement algorithms and approved the reflow profiles used in the test vehicle fabrication.

The following discussion describes the generic surface mount assembly process for both test vehicles.

Twelve hours before assembly, the PBGA packages were "baked out" in an oven at 150ºC to remove moisture and prevent a popcorn effect during the reflow process. The popcorn effect is caused by moisture rapidly expanding during reflow and can often encourage package cracking. After bake out, the first step in fabrication was to print solder paste on the PCB boards with the MPM screen printer. This was achieved by using a 0.15mm thick laser-cut stencil that precisely matched the pad footprints on the test vehicle. Once the stencil and the PCB were positioned in the screen printer, the solder paste was pressed through the stencil with a rubber squeegee. The board was then removed from the screen printer and inspected to ensure that the alignment of the solder paste was properly centered on PCB pad sites. If the volume and solder paste alignment were acceptable the PCB was fed into an automated ACM placement machine.

The ACM placement machine picked the electronic components and placed them on the PCB. The PBGA packages were picked from a matrix tray feeder, while the resistors and the QFNs were picked from a "tape and reel" feeder. Once the board was fed into the machine, the programmed algorithm (provided by Siemens VDO Automotive) began and all of the electronic components were systematically picked and placed onto the test vehicle. The test vehicle was again inspected for abnormalities such as skewed package placement.

Finally, the fully populated test vehicle was sent through the Heller 1800 EXL reflow oven. The reflow oven had eight temperature zones and used convection heating to bake the packages onto the board. The board was inspected again under an X-ray microscope to detect the voids, shorts, opens, and placement defects in the solder joints.

The following sections will provide the build matrix and the reflow profiles used in the Heller oven for both test vehicles.

3.3.1 TV3D Configuration 1 Assembly

Twenty-four (24) TV3D_C1 test vehicles were assembled. The assembly was broken into the type of surface finish plated on the test vehicle. The breakdown follows:

- Eight (8) boards with a HASL surface finish
- Eight (8) boards with a OSP surface finish
- Eight (8) boards with a ImSn surface finish

One board from each surface finish was cross sectioned after assembly to confirm solder joint integrity for the PBGA packages. Each board was populated with the following electronic packages (Table 15).

Package Type	Termination Alloy	QTY
27x27mm PBGA	Sn-36Pb-2Ag	2
27x27mm PBGA	Sn-3.8Ag-0.7Cu	2
17x17mm PBGA	Sn-36Pb-2Ag	2
17x17mm PBGA	Sn-3.8Ag-0.7Cu	1
QFN	Sn-15Pb	3
2512 Resistor Bank	Sn-10Pb	2

Table 15: Components Assembled on TV3D_C1

As mentioned earlier, the components were manufactured with Sn-37 solder paste (Kester - Easy Profile 256) using an aggressive SnPb profile. With the Sn-37Pb solder paste, Kester set forth recommendations in order to achieve an optimum reflow profile. These parameters included a soak zone between 150ºC to 183ºC with an interval time of 60-90 seconds (120 seconds max), a reflow zone greater than 183ºC with an interval time of 30-60 seconds (90 seconds max), and a peak temperature between 210ºC to 225ºC [31]. Figure 23 graphically represents Kester's reflow suggestions for an optimum SnPb profile.

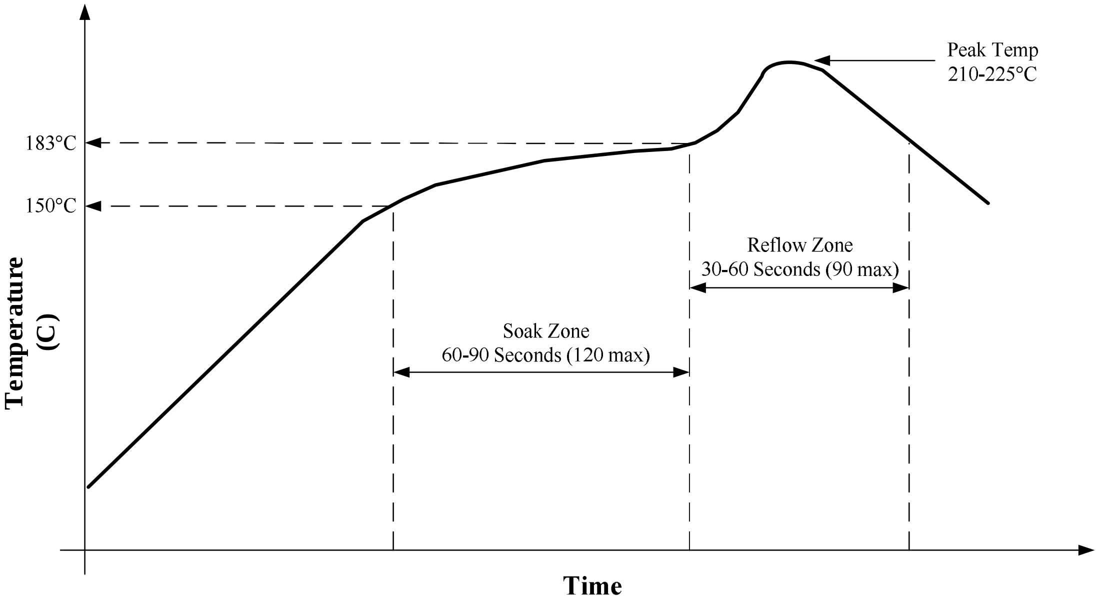


Figure 23: Kester's Suggested SnPb Reflow Profile

The soak zone serves two purposes. The soak zone brings the entire board up to a uniform temperature and begins to activate the flux within the solder paste. The reflow zone finishes the flux activation so that uniform melting of the solder joints will occur.

To adequately melt the Pb-free solder balls and ensure proper mixing with the SnPb solder paste, the recommended SnPb profile was modified. The modified SnPb profile increased the soak and reflow times near their maximum limit and increased the peak temperature above 225ºC. To achieve the desired reflow profile within the eight-zoned Heller oven, the Slim-Kic profiling system was used.

The Slim-Kic profiling system consisted of the following items: (1) transmitter, (2) receiver, (3) thermocouples, and (4) monitoring software. Underneath the electronic package, the ends of the thermocouples were taped onto the PCB. The thermocouples (TCs) were placed in strategic locations on the PCB to monitor uniform board heating during the reflow process (Figure 24).

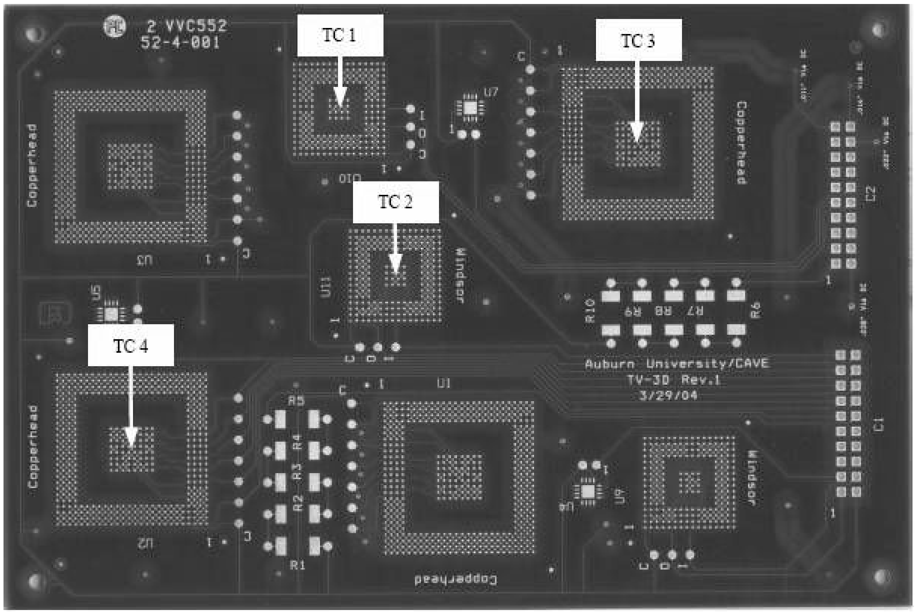
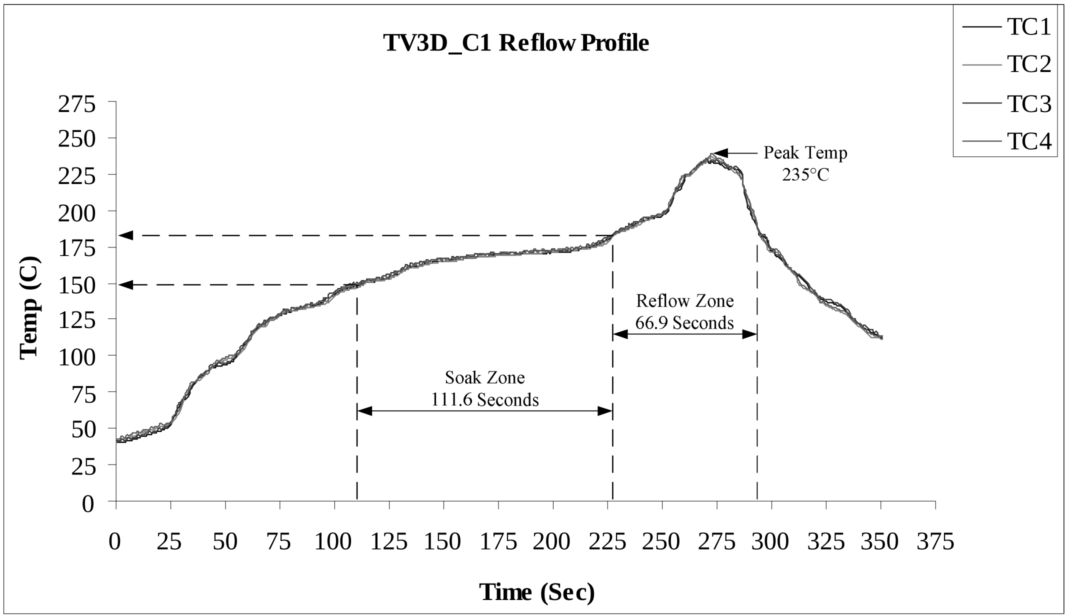


Figure 24: TV3D_C1 Thermocouple Locations

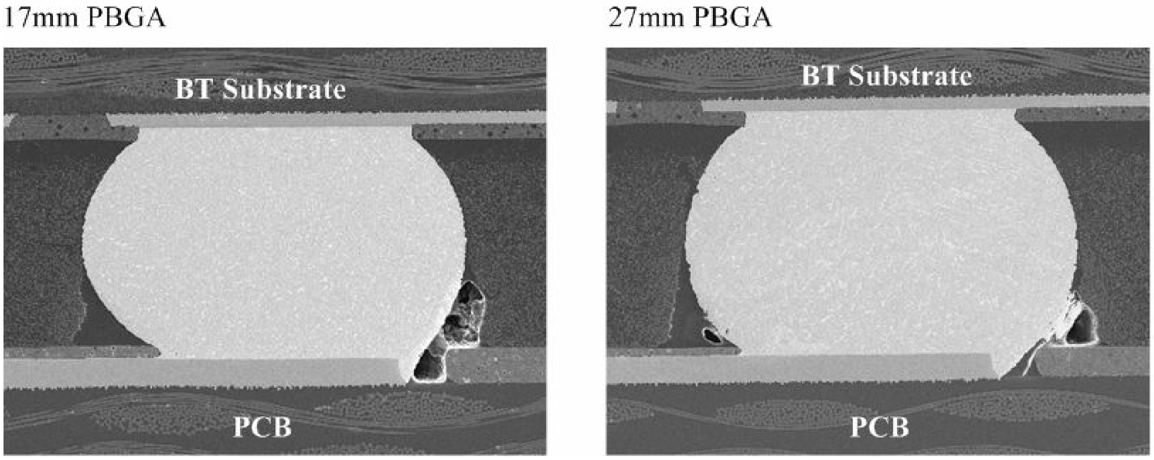
The corresponding ends of the thermocouples were then plugged into the receiver. The receiver was mounted on a carrier that was designed to travel on the conveyor belt behind the PCB through the reflow oven. Next, the initial belt speed and temperatures for the eight zones were set for the Heller reflow oven. As the board and the transmitter traveled through the reflow oven, the transmitter sent time and temperature data to the receiver. The receiver then supplied this information to the Slim-Kic software program. Based upon the reflow profile specifications entered into the program, the software recommend modifying the zone temperatures and adjusting the belt speed. After several iterations, the desired profile was achieved. The profile and its corresponding performance metrics are shown below in Figure 25.



Thermocouple	Soak Time (Sec) 150-183°C	Reflow Time (Sec) >183°C	Peak Temp
TC 1	111.2	66.9	233.2°C
TC 2	111.3	66.6	236.4°C
TC 3	112.0	67.1	234.8°C
TC 4	111.8	66.9	235.6°C
AVG	111.6	66.9	235.0°C

Figure 25: TV3D_C1 Reflow Profile & Metrics

To verify that this extreme SnPb profile caused no damaging effects (voids, open, shorts), the solder joints were x-rayed. Upon review, no opens or shorts existed and all the solder joints exhibited minimal voiding. Voids in the solder joint were caused by the inability of flux gases to escape during reflow. Appendix A shows representative voiding photos for each type of solder joint. The 17mm PBGA package showed the highest volume of voiding up to 10%. However, research conducted by Banks et al [32] concluded that voiding less than 24% in PBGA packages was not detrimental to its reliability during environmental testing. In some cases, the reliability of PBGA packages with significant voiding was extended because the voids acted as stress relievers and crack arrest [32]. For all three surface finishes, the PBGA packages with the Pb-free solder balls completely mixed with the SnPb solder paste and experienced full ball collapse (Figure 26)


17mm PBGA

27mm PBGA

Figure 26: TV3D_C1 Full Solder Ball Collapse

3.3.2 TV3D Configuration 2 Assembly

Forty (40) TV3D_C2 test vehicles were assembled. Each board was assembled with the two 17mm BGAs of the same solder ball composition and two 2512 resistor banks. The assembly was broken into 5 different combinations based upon the interaction among the PBGA solder ball, solder paste, and reflow profile. Once again, one board from each combination was sacrificed to ensure solder joint integrity. Nomenclature was developed to easily identity the five different combinations. The nomenclature was separated into three elements ➔(Solder ball composition) - (Solder Paste) - (Reflow Profile). Depending on the content of the element, it was either designated as LF (Lead Free) or L (Lead). Table 16 shows the build matrix for TV3D_C2.

Nomenclature	Solder Balls	Solder Paste	Reflow Profile	Num Boards
LF-LF-LF	Sn-3.8Ag-0.7Cu	Sn-3.0Ag-0.5Cu	Pb-Free	8
LF-L-LF	Sn-3.8Ag-0.7Cu	Sn-37Pb	Pb-Free	8
LF-L-L	Sn-3.8Ag-0.7Cu	Sn-37Pb	SnPb	8
L-L-L	Sn-36Pb-2Ag	Sn-37Pb	SnPb	8
L-L-LF	Sn-36Pb-2Ag	Sn-37Pb	Pb-Free	8

Table 16: TV3D_C2 Build Matrix

While there were five combinations of PBGA packages, only three combinations of 2512 resistor banks existed. The 2512 resistor banks were subject to different interactions between the solder paste and the reflow profile. These interactions included the resistors mounted on Sn-3.0Ag-0.5Cu paste with a Pb-Free profile, and the resistors assembled with Sn-37 solder paste subjected to either a SnPb or Pb-free reflow profile.

The SnPb solder paste was the same Kester – “Easy Profile 256” used in the TV3D_C1 build. The Pb-Free solder paste was Sn-3.0Ag-0.5Cu (Kester – EnviroMark

907). With the Sn-3.0Ag-0.5Cu solder paste, Kester set forth recommendations in order to achieve an optimum reflow profile. These parameters included a soaking zone between 150ºC to 217ºC with an interval time of 60-90 seconds (120 seconds max), a reflow zone greater than 217ºC with an interval time of 60-75 seconds (90 seconds max), and a peak temperature between 235ºC - 255ºC [33]. Figure 27 graphically represents Kester's reflow suggestions for an optimum Pb-Free profile.

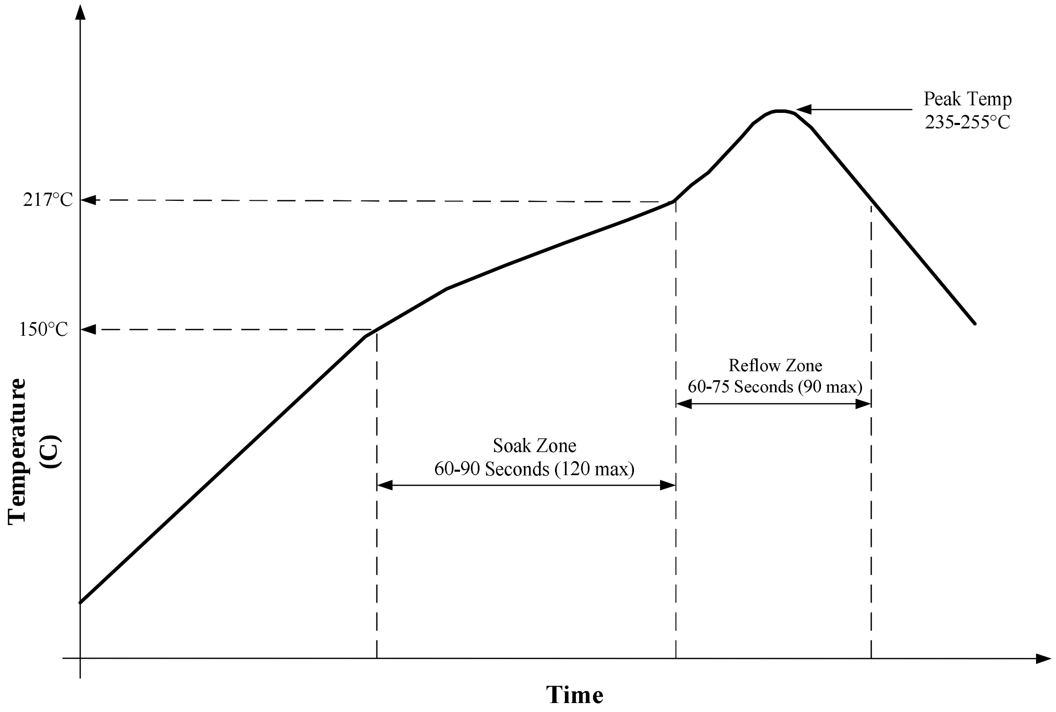


Figure 27: Kester's Suggested Lead Free Reflow Profile

As in the TV3D_C1 build, the Slim-Kic system was used to profile the Heller reflow oven to ensure that both the SnPb and the Pb-free profiles met the recommendations set forth by Kester. Figure 28 shows the locations of the thermocouples on the PCB.

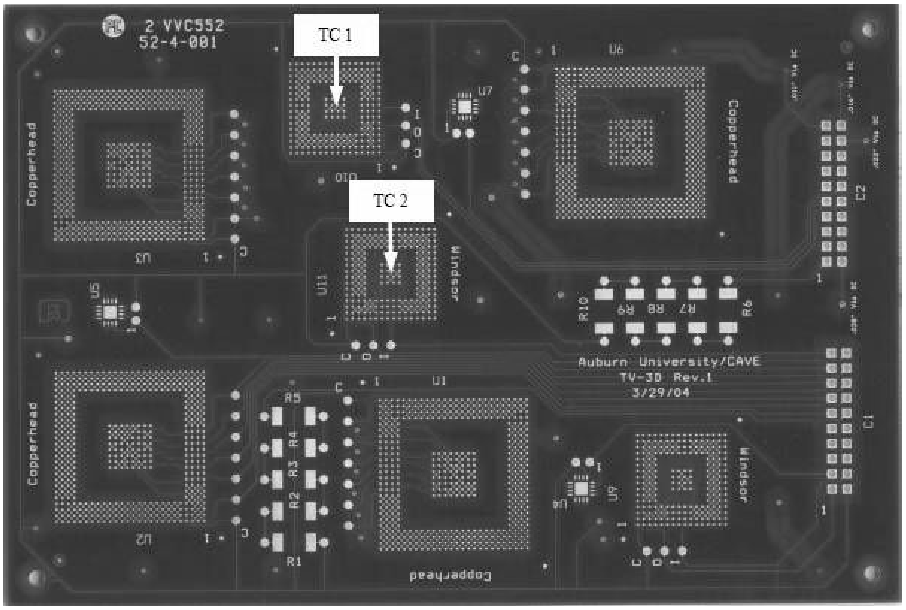
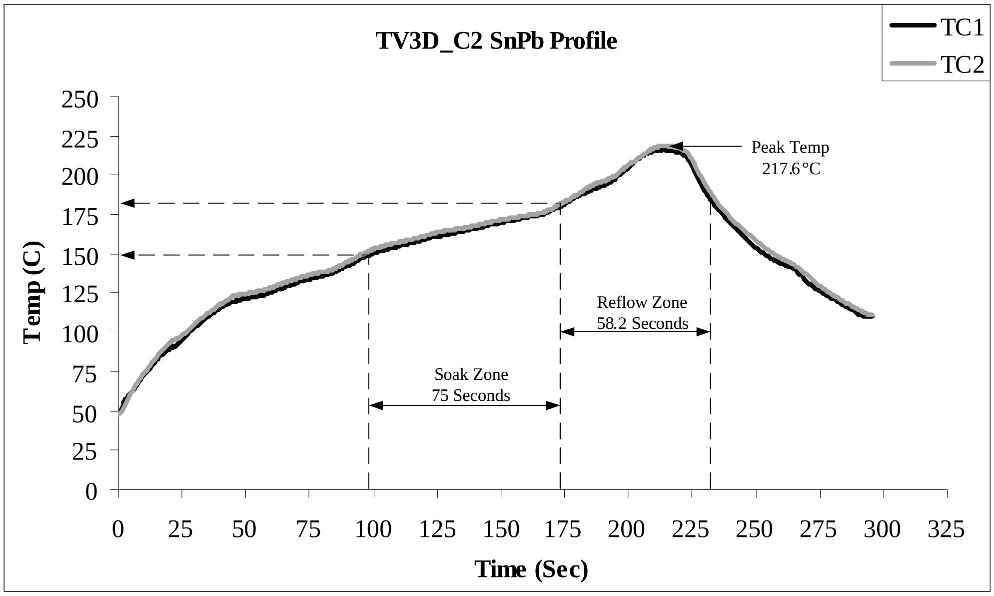


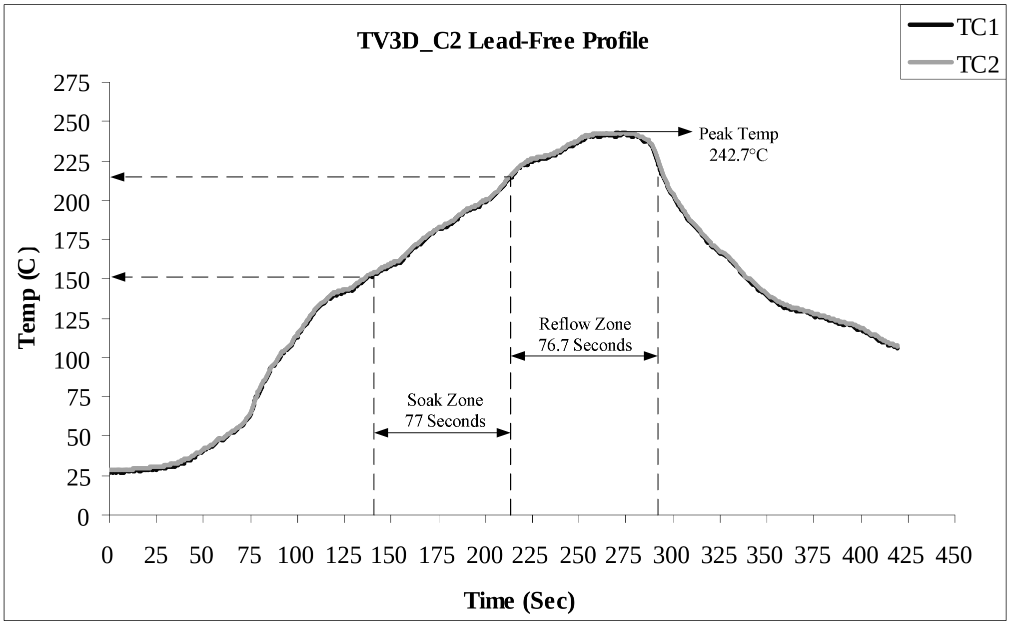
Figure 28: TV3D_C2 Thermocouple Locations

Figures 29 and 30 represent the completed SnPb and Pb-Free reflow profiles along with their corresponding performance metrics.



Thermocouple	Soak Time (Sec) 150-183°C	Reflow Time (Sec) >183°C	Peak Temp
TC 1	74.2	56.7	216.3°C
TC 2	75.8	59.7	218.9°C
AVG	75.0	58.2	217.6°C

Figure 29: TV3D_C2 SnPb Reflow Profile & Metrics



Thermocouple	Soak Time (Sec) 150-217°C	Reflow Time (Sec) >217°C	Peak Temp
TC 1	75.9	73.5	241.7°C
TC 2	78.0	79.9	243.0°C
AVG	77.0	76.7	242.7°C

Figure 30: TV3D_C2 Pb-Free Reflow Profile & Metrics

To verify that the two profiles caused no damaging effects (voids, open, shorts), the solder joints were X-rayed. Upon review, no opens or shorts existed and all the solder joints exhibited minimal voiding. Appendix B shows representative voiding photos of the solder joints for each of the five assembly combinations. Except for LF-L-L, solder ball wetting and collapse were consistent throughout the combinations. In LF-L-L, the SnPb reflow profile could not completely melt the solder ball and full solder ball collapse was not demonstrated.

3.4 Testing Methods

To determine the true reliability of electronic packages, testing schemes must mimic realistic environmental conditions. But, mimicking the exact environmental conditions is unrealistic due to the large amount of time and monetary investment required to fail the electronic component. Thus, accelerated life testing (ALT) attempts to overstress the electronic package and reduce the mean life to failure. Through accelerated life testing, the results can be extrapolated and feasible interpretations about the environment of interest can be deduced. For this research endeavor, thermal shock and thermal cycle testing were the two types of commonly accepted ALT mechanisms used to imitate automotive conditions.

The accelerated life testing methods, thermal shock and thermal cycle, exhibit different testing characteristics. Thermal shock testing rapidly cycles the boards between two temperature extremes through steep heating/cooling rates and quick dwell/soak times. On the other hand, thermal cycle testing moderately cycles the boards between the temperature extremes with extended dwell/soak times. Figure 31 demonstrates the difference between the two testing methods.

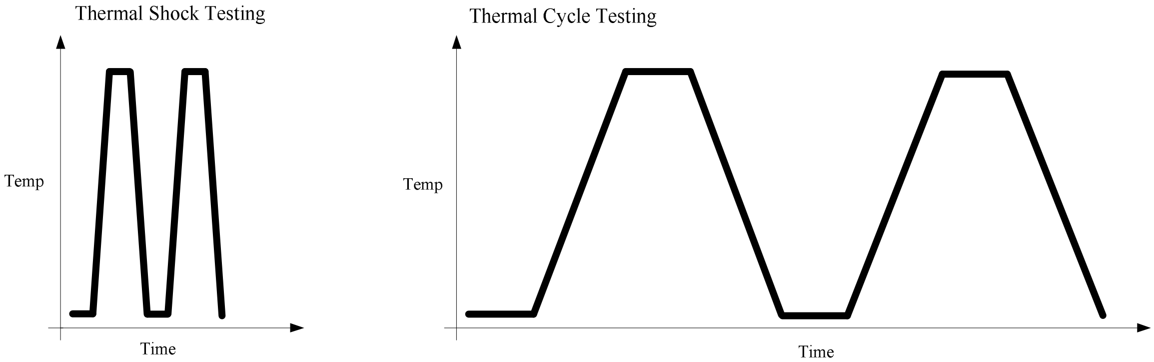


Figure 31: Environmental Testing Methods

The cycling of the electronic package causes solder joint failure through a combination of fatigue and creep. Fatigue is the weakening or breakdown of a material subjected to prolonged or repeated stress below its tensile strength [34]. Creep is the plastic deformation of a material subjected to a constant stress when the material is at a high homologous temperature (measured in Kelvin). Homologous temperature refers to the ratio of the material's temperature to its melting temperature and must be greater than 0.40 for the creep process to initiate [34].

Thermal shock testing fails the solder joint through solder fatigue. As the electronic package is repeatedly cycled, stresses act upon the solder joint. The steep ramp rates brutally pronounce the CTE mismatch between solder joint and the surrounding materials. Therefore, the different rate of expansions between the solder joint and the materials produces shear stresses along the solder joint interfaces. To relieve the stresses, the solder joint has to strain. The rapid dwell time on the hot temperature does not allow for substantial strain to counteract the shear stresses. Without stress relief, the solder joints fatigue and fail.

Thermal cycling testing is more conducive to the automotive under-the-hood environment (i.e. controllers are mounted directly onto the engine/transmission) where the solder joint is exposed to long temperature dwells. In thermal cycling, solder joint failure is attributed to the interaction between fatigue and creep. During the heating and cooling cycle, shear stresses act upon the solder joint. The long dwell time ignites the creep process which strains the solder. Even though the stress is relieved by the strain during the hot temperature dwell, plastic deformation occurs. As the cycling process continues, the plastic deformation will limit the amount of stress that can be relived and the solder joint will eventually fail.

3.4.1 TV3D Configuration 1 Testing

The TV3D_C1 test vehicles were thermally cycled in a Blue M air-air environmental chamber that used convection heating/cooling techniques. The TV3D_C1 test vehicles were exposed to a 90 minute cycle between -40ºC to 125ºC. At each temperature extreme the boards were soaked for fifteen minutes. The ramp rate from the hot to cold was 5ºC/minute (~33 minutes). The ramp rate from the cold to hot was 6ºC/minute (~27 minutes). Figure 32 represents the temperature cycling profile of the TV3D_C1 boards.

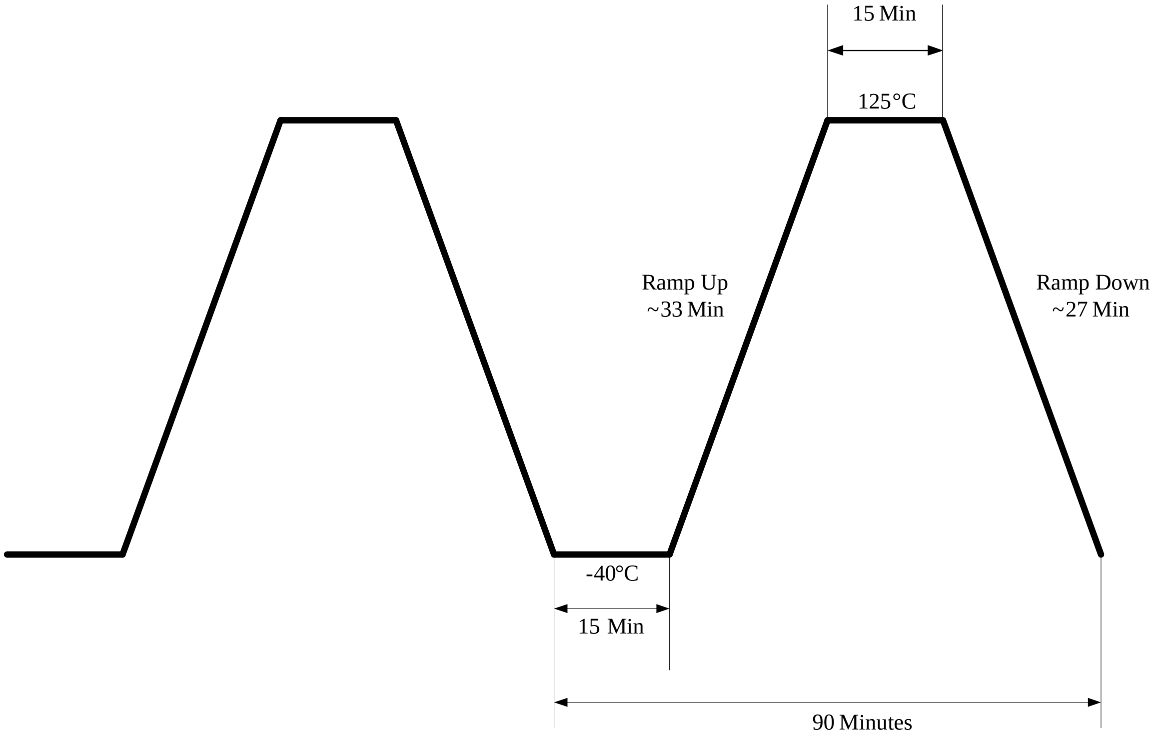


Figure 32: Air-to-Air Thermal Cycling Profile

As stated earlier, eight boards from three surface finishes (HASL, ImSn, and OSP) were assembled. One board from each type of surface finish was sacrificed to verify solder joint integrity. Thus, seven boards from each surface finish (total of 21 boards) were air-air thermally tested.

During temperature cycling, the resistance of the electronic components was monitored. The boards were placed in vertical racks within the chamber. To measure resistance, wires were routed from the edge of the test board to interface connectors. The interface connectors were linked to a monitoring system. The monitoring system consisted of a digital multimeter, switchboxes, and Labview software. The Labview software program, MarkDano, controlled the monitoring system and recorded the resistance of the electronic packages (MarkDano is proprietary monitoring software developed by CAVE). The resistance of the component was measured approximately three times per minute. The packages were deemed to have failed when the resistance of packages exceeded the threshold value five consecutive times. For TV3D_C1, the failure threshold for the electronic packages was 12 ohms. The MarkDano software recorded at which cycle number the package failed.

3.4.2 TV3D Configuration 2 Testing

The TV3D_C2 test vehicles were thermally shocked in a CSZ liquid-liquid environmental chamber that used two liquid bathes (hot and cold) to soak the boards. Perfluoropolyether fluid was used to withstand the extreme hot/cold conditions because it does not freeze or evaporate. The boards were secured in a metal basket attached to a mechanical arm. The mechanical arm transferred the basket between the liquid bathes. The boards were completely submerged under the liquid in each bath. CAVE has documented that when the boards are completely submerged in the liquid, they reach the soak equilibrium temperature almost instantaneously. The TV3D_C2 test vehicles were exposed to a 14 minute cycle between -40ºC to 125ºC. At each temperature extreme, the boards were soaked in the liquid for five minutes. Between each dwell, the mechanical arm was lifted into a neutral position for two minutes. After the two minutes expired, the basket was then plunged back into the liquid bath. Thus, the ramp rate from hot to cold and cold to hot was 82.50ºC/minute (~2 minutes). Figure 33 represents the temperature cycling profile of the TV3D_C2 boards.

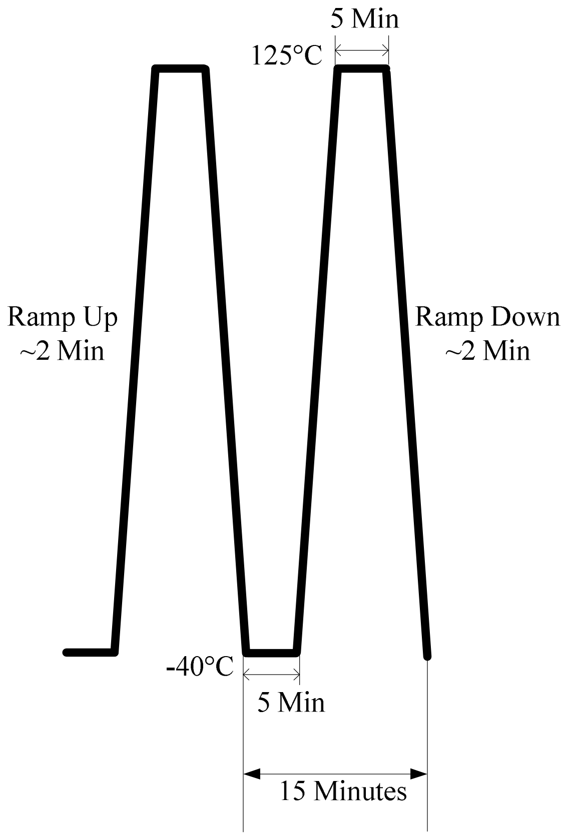


Figure 33: Liquid-to-Liquid Thermal Shock Profile

As stated earlier, eight boards from each of the five different combinations were assembled. One board from each combination was sacrificed to verify solder joint integrity. Thus, seven boards from each combination type (35 total boards) were liquid-liquid thermally shocked.

The resistance of the electronic components was monitored during temperature cycling. As described in the previous section, the same monitoring system was used. The packages were deemed to have failed when the resistance of packages exceeded the threshold value five consecutive times. For TV3D_C2 the failure threshold for the electronic packages was 12 ohms, and the MarkDano software recorded the cycle number at which the electronic package failed.

CHAPTER 4: ANALYSIS TECHNIQUES

This chapter discusses the techniques used to quantify and analyze the failure behavior exhibited by the electronic packages. It contains two sections that discuss the procedures used to evaluate the reliability and surface science characteristics of the electronic packages.

4.1 Reliability Evaluation

The foremost technique to characterize solder joint failure reliability is with the Weibull distribution [2]. The Weibull distribution graphically presents failure modes with three distinguishing parameters. These three parameters include the location parameter, the characteristic life (η), and the slope (β). The location parameter is defined as the minimum life of any entity/unit under test. In the electronics industry, all electronic packages are assumed to have a minimum life of zero because instantaneous failures can occur. Setting the minimum life to zero is a standard practice and widely accepted for electronic components [2]. Because the minimum life is set to zero, the failure life of electronic packages is characterized with a 2-parameter (η, β) Weibull distribution. The characteristic life (η) is the point (i.e. number of cycles) at which 63.21% of the population is expected to fail. The slope (β) of the Weibull distribution distinguishes different classes of failure modes. According to Abernethy [35], the slope of Weibull distribution can be separated into four distinct groups (1) $\beta < 1$ indicates infant mortality which is usually a result of a manufacturing process or defective parts, (2) $\beta = 1$ represents random failures independent of time, (3) $1 < \beta < 4$ implies early wear out failures, and (4) $\beta > 4$ signify old age, rapid wear out failures.

There are two methods to estimate the characteristic life and the slope of the Weibull distribution. These two methods are least squares estimators (LSEs) and maximum likelihood estimators (MLEs). Both methods are commonly accepted for estimating the two parameters of the Weibull distribution. Abernethy [35] conducted simulation studies that suggested, for sample sizes less than 100, the LSEs were less biased in comparison with the MLEs. Dodson [36] also compared LSEs and MLEs through simulated studies and suggested that LSEs should be used to estimate the 2-paramter Weibull for small sample sizes. Due to availability reasons, the sample sizes in this research were small. Therefore, the LSE technique was used to calculate the characteristic life and the slope.

Using the LSE technique, the software program, "WinSMITH Weibull" calculated and displayed the 2-parmater Weibull distribution. This software also calculated the r^2 value. The r^2 value indicates how well the data fit the estimated parameters of the Weibull distribution. An r^2 value of 1.0 indicates a perfect fit, but usually r^2 values greater than 0.85 are considered adequate. To confirm that "WinSMITH Weibull" was accurate, the results were verified with the statistical software Minitab (Version 14).

With Minitab, hypothesis testing on two data sets was conducted for the characteristic life (η) and the slope (β) to determine if these parameters were statistically different. The null hypothesis for η assumed equality between the two data sets ($\eta_1 = \eta_2$).

The null hypothesis for β also assumed equality between the two data sets ($\beta_1 = \beta_2$). For hypothesis testing, Minitab reported the p-values. If the p-value was greater than the desired level of significance (α), then the null hypothesis was accepted and no significant difference existed between the parameters. The level of significance of this research was set at the 5% level.

Another critical measure of electronic failures is the value $N_{1\%}$. $N_{1\%}$ corresponds to the number of cycles required for the sample to reach 1% cumulative failures. For the automotive under-the-hood environment, this number is critical to establish appropriate engine and transmission warranties. For this research, the sample size resolution to obtain $N_{1\%}$ was not sufficient. As a result, the cycle number to first failure was reported.

4.2 Surface Science Evaluation

For this research, surface science techniques were used to analyze the characteristics of the solder joint after an allotted number of completed thermal/shock cycles. After the electronic package had reached the desired level of completed cycles, the test vehicle was removed. Once removed, the electronic package was cross-sectioned from the test vehicle, mounted, polished, and gold coated. (Reference Appendix C and D for the cross sectioning and gold coating procedures)

After the samples were prepared, the following techniques were used to analyze the microstructures of the solder joint: (1) scanning electron microscopy (SEM), (2) cross-sectional SEM analysis, and (3) energy dispersive X-ray spectroscopy (EDX).

“EDX is a materials technique used in combination with SEM that analyzes the top 2-3 microns of a surface. Conventional EDX (the type used here) is capable of detecting all elements of the periodic table with the exception of first and second rows elements (H – Ne). Omission of these elements was due to a protective Be window over the LN_2 cooled X-ray detector that blocks the low energy X-rays emitted from these elements. For the analysis, this was not an impediment due to the high Z elements expected in the analysis. The limit of detection in a typical EDX analysis is 0.1 at %.” (As described by Dr. Michael Bozack, the director of Auburn University’s Surface Science Laboratory). A series of SEM photographs of representative cross-sections were taken.

CHAPTER 5: TV3D_C1 RELIABILITY & FAILURE ANALYSIS

This chapter presents and discusses the failure modes of the electronic packages located on the TV3D_C1 test vehicle. The first section reviews the reliability data, while the second section discusses the failure mechanisms.

5.1 TV3D Configuration 1 Reliability Analysis

The TV3D_C1 test vehicles were air-air thermally cycled between -40ºC to 125ºC with a 90 minute cycle time. Seven boards from the three surface finishes (21 total boards) were tested. Table 17 shows the electronic packages that were tested per board.

Package Type	Termination Alloy	QTY
2512 Resistor Bank	Sn-10Pb	2
27mm PBGA	Sn-36Pb-2Ag	2
27mm PBGA	Sn-3.8Ag-0.7Cu	2
17mm PBGA	Sn-36Pb-2Ag	2
17mm PBGA	Sn-3.8Ag-0.7Cu	1
QFN	Sn-15Pb	3

Table 17: Components Tested on TV3D_C1

The PBGA packages with the termination alloy of Sn-3.8Ag-0.7Cu will also be referenced as Pb-free PBGAs. The thermal solder balls were monitored on the 27mm PBGA packages. However, in most practical applications, the thermal solder balls dissipate heat from the PBGA package and provide no electrical connection [15]. Since the failure reliability of the thermal solder balls provides limited intrinsic value, they were omitted from the analysis.

To determine if the cycles to failure of identical electronic packages assembled on the same board were independent of location, two statistical tests were performed. These included the Paired t-Test and the Wilcoxon Signed Ranks Test (See Appendix E for further discussion between the two statistical tests). The QFNs were excluded from the statistical tests because of insufficient failures. Both statistical tests concluded that the cycles to failure for the components, regardless of surface finish, were independent of board location. (See Appendix F for the results). Table 18 represents the sample size of the components for each surface finish.

Electronic Package	Sample Size		
	HASL	ImSn	OSP
2512 Resistor Banks	14	14	14
27mm PBGA	14	14	14
27mm PBGA (Pb-Free)	14	14	14
17mm PBGA	14	14	14
17mm PBGA (Pb-Free)	7	7	7
QFN	21	21	21

Table 18: TV3D_C1 Sample Sizes

The air-air thermal cycle chamber completed 4,816 cycles before the test was terminated. Table 19 provides a summary of the percentage failure that occurred once the test ended.

Electronic Package	Surface Finish		
	HASL	ImSn	OSP
2512 Resistor Banks	100%	100%	100%
27mm PBGA	100%	100%	100%
27mm PBGA (Pb-Free)	86%	79%	64%
17mm PBGA	100%	100%	100%
17mm PBGA (Pb-Free)	29%	29%	0%
QFN	10%	14%	14%

Table 19: TV3D_C1 Failure Percentages

This table provides an initial indicator that the PBGA packages with Pb-free solder balls outperformed the PBGA packages with SnPbAg solder balls.

The following sections will discuss the reliability data for the electronic packages assembled on TV3D_C1. The results of the hypothesis testing between data sets, on both η and β, are located in Appendix G. The r^2 values for the data sets indicated excellent fits with the Weibull distribution.

5.1.1 2512 Resistors

As described earlier the 2512 resistor banks consisted of five resistors placed in series. When one resistor failed, the other four resistors became censored data points. Software programs, WinSMITH Weibull and Minitab, easily accommodated censored data. Figure 34 provides the Weibull plot of the 2512 resistors for all three types of surface finishes.

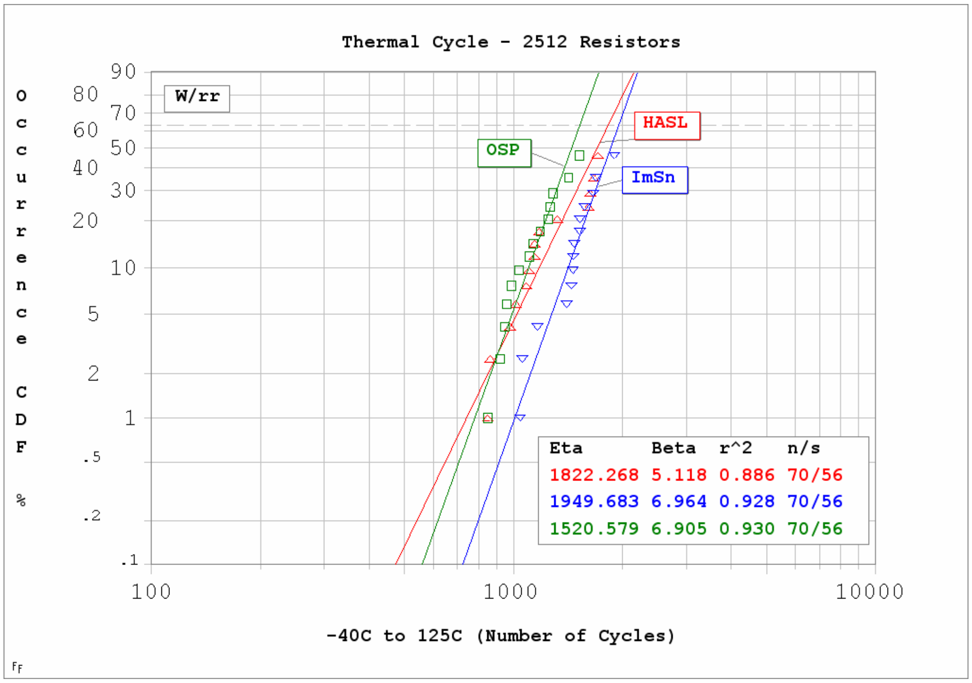


Figure 34: TV3D_C1 Weibull Plot - 2512 Resistors

The resistor failures were similar in relation with previous reliability testing at CAVE. This signifies no abnormalities existed in the assembly and testing of the TV3D_C1 test vehicles. The next step compared the etas and betas among the three data sets. In comparing the slopes of all three data sets, no statistical differences were observed. With respect to η, the resistor banks on both the HASL and ImSn surface finish performed equally. Conversely, the resistors mounted on the OSP board finish experienced the lowest characteristic life.

5.1.2 27mm PBGA

Figure 35 shows the Weibull plot of the 27mm PBGA packages.

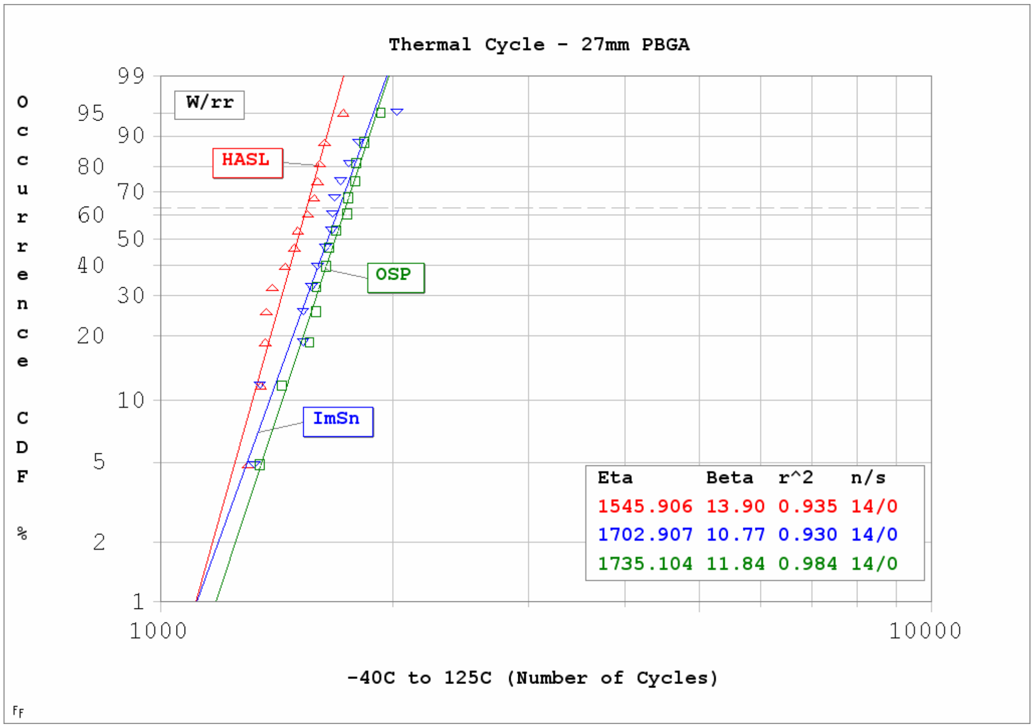


Figure 35: TV3D_C1 Weibull Plot - 27mm PBGA

Once again, no differences existed among the three β's for the 27mm PBGA packages. The 27mm PBGAs mounted on HASL had the lowest characteristic life of ~1,546 cycles.

This characteristic life (η) was statistically worse than the 27mm PBGAs mounted on both the ImSn and OSP surface finishes. On the other hand, η, for the 27mm PBGAs mounted on ImSn and OSP were statistically equal.

5.1.3 27mm PBGA (Pb-Free)

Figure 36 shows the Weibull plot of the 27mm (Pb-Free) PBGA packages.

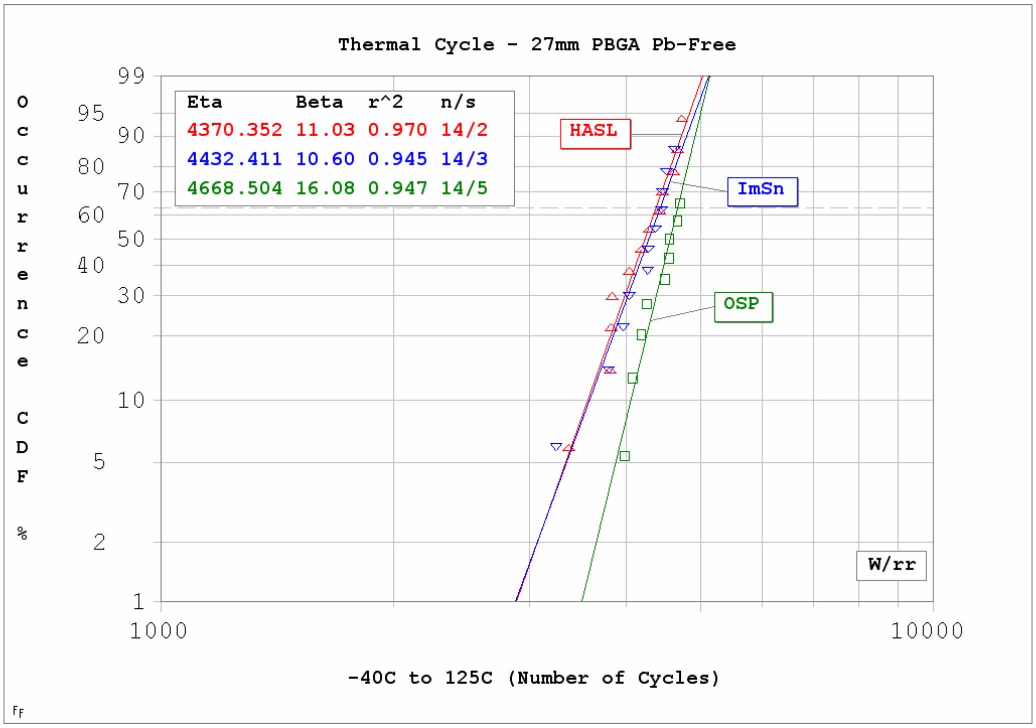


Figure 36: TV3D_C1 Weibull Plot - 27mm PBGA (Pb-Free)

The slopes of all three data sets were statistically equal. Also, the characteristic life between the HASL & ImSn and the ImSn & OSP board finishes were statistically equal. But, when η was compared between the HASL and OSP finishes, a statistical difference was observed. The 27mm PBGA (Pb-free) packages mounted on OSP had a significantly larger characteristic life than the packages mounted on HASL.

5.1.4 17mm PBGA

Figure 37 shows the Weibull plot of the 17mm PBGA packages.

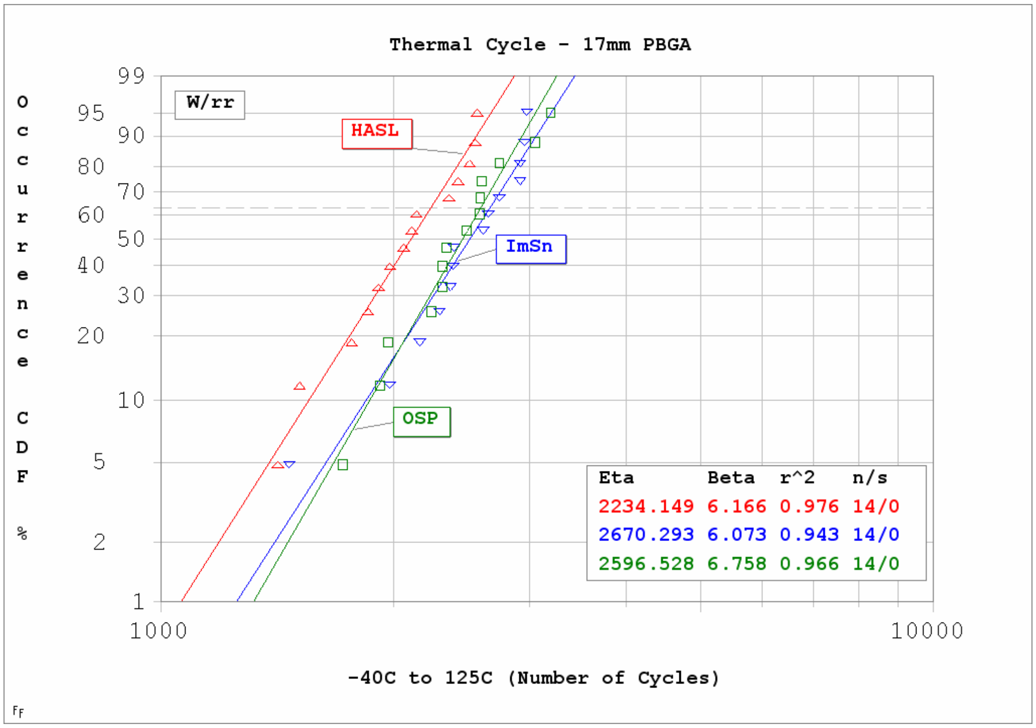


Figure 37: TV3D_C1 Weibull Plot - 17mm PBGA

Once more, no statistical differences existed between the three β's. The 17mm PBGA mounted on HASL had the lowest characteristic life of ~2,234 cycles. This characteristic life of the 17mm PBGA mounted on HASL was significantly lower than the 17mm PBGAs mounted on ImSn and OSP. On the other hand, the η for the 17mm PBGAs mounted on ImSn and OSP were statistically equal.

5.1.5 17mm PBGA (Pb-Free)

After 4,816 cycles, four total failures throughout the surface finishes occurred. The failure cycle, separated by board finish, are listed below:

- HASL: 4,619 ▪ 4,787
- ImSn: 4,394 ▪ 4,698
- OSP: None

Considering the lack of failures, rough parameter estimates of the Weibull distribution were drawn from the HASL and ImSn surface finishes (Table 20).

17mm PBGA (Pb-Free)		
Surface Finish	**Char. Life (η)**	**Slope (β)**
HASL	5,001.25	26.57
ImSn	5,099.40	14.19
OSP	n/a	

Table 20: 17mm PBGA (Pb-Free) Weibull Estimates

Due to the small number of failures, no comparisons were conducted among the surface finishes.

5.1.6 QFN

After 4,816 cycles, eight total failures throughout the surface finishes occurred. The failure cycle, separated by board finish, are listed below:

- HASL: 3,881 ▪ 4,365
- ImSn: 4,015.5 ▪ 4,318.5 ▪ 4,604
- OSP: 4,291 ▪ 4,431 ▪ 4,649

Considering the lack of failures, rough parameter estimates of the Weibull distribution were drawn from the three board finishes (Table 21).

QFN		
Surface Finish	**Char. Life (η)**	**Slope (β)**
HASL	5,938.95	7.51
ImSn	5,471.04	10.22
OSP	5,067.64	18.75

Table 21: QFN Weibull Estimates

The deficiency of failures allowed for no comparisons between surface finishes.

5.1.7 17mm Vs 27mm PBGA

Figures 38 through 40 show Weibull plots separated by surface finish, comparing the cycles to failure between the 17mm and the 27mm SnPbAg PBGA packages.

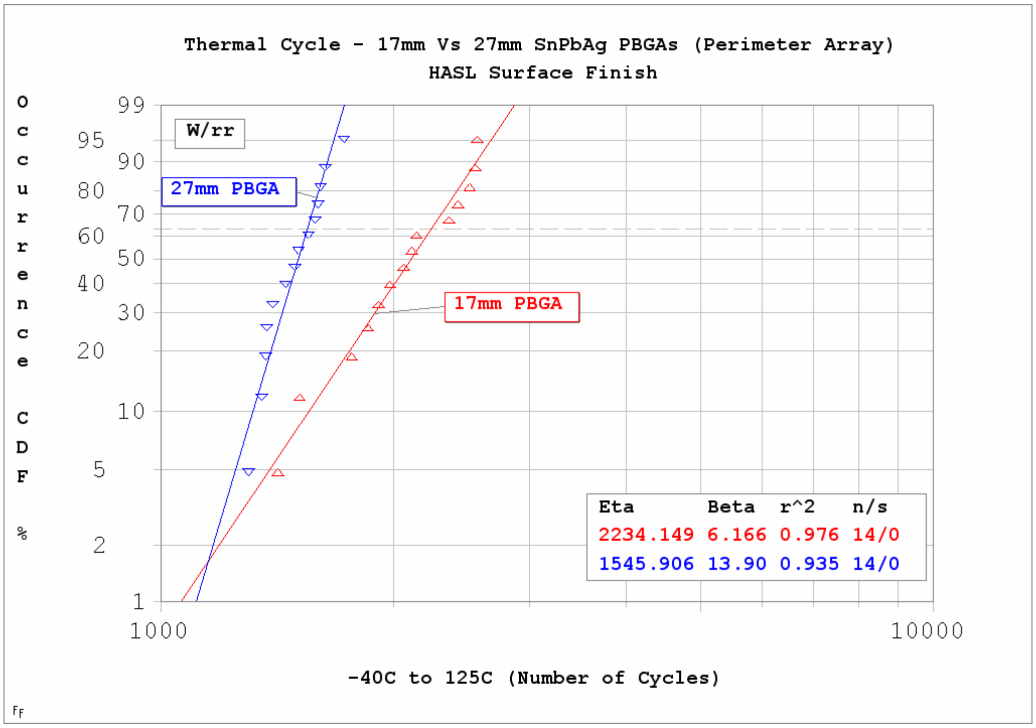


Figure 38: TV3D_C1 Weibull Plot - 17mm Vs 27mm SnPbAg PBGA (HASL)

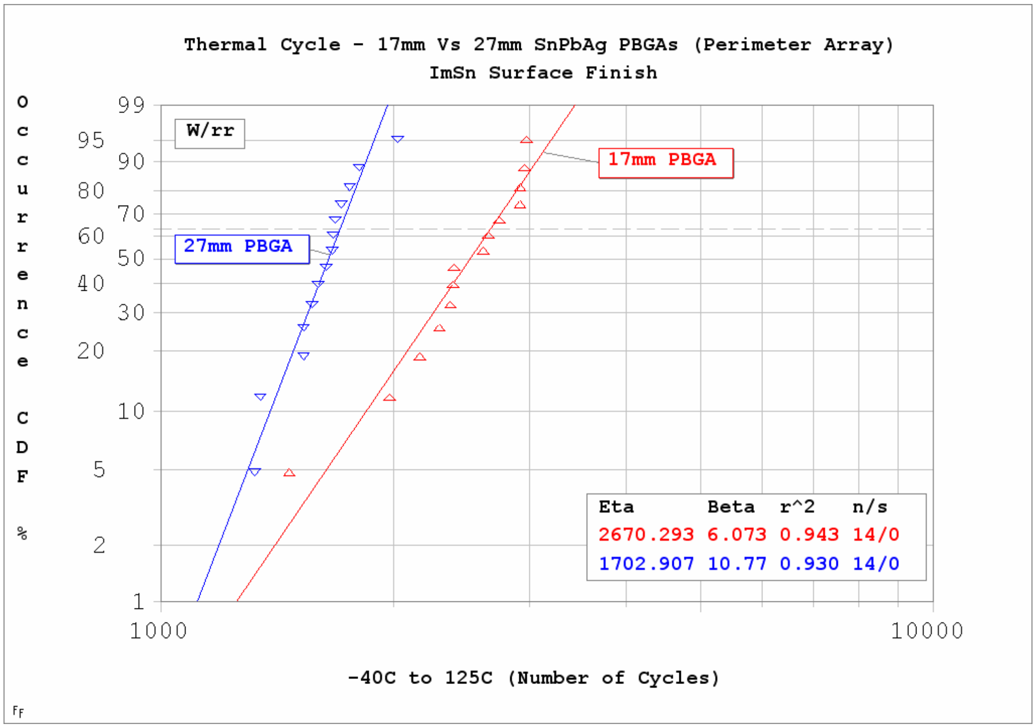


Figure 39: TV3D_C1 Weibull Plot - 17mm Vs 27mm SnPbAg PBGA (ImSn)

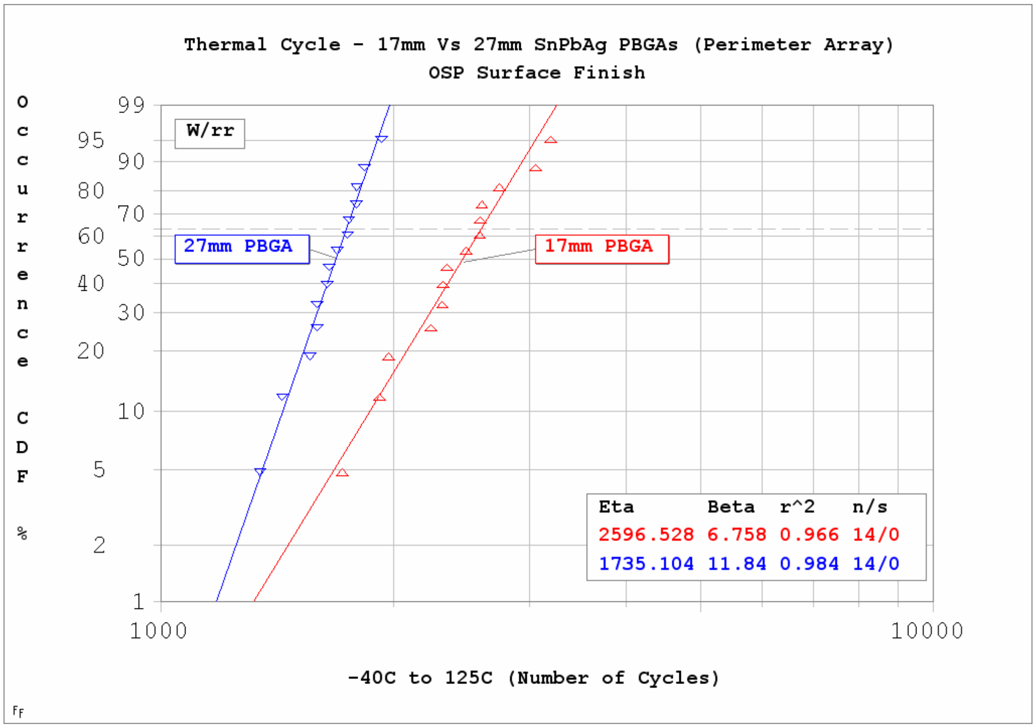


Figure 40: TV3D_C1 Weibull Plot - 17mm Vs 27mm SnPbAg PBGA (OSP)

Independent of surface finish, the characteristic life was statistically greater for the 17mm PBGA packages. The data also suggested that the slopes of the two PBGA packages were different.

5.1.8 Backward Vs SnPb Solder Joint

Figures 41 through 43 show Weibull plots, separated by surface finish, comparing the cycles to failure between the "backward" solder joint versus the SnPb solder joint for the 27mm PBGA packages.

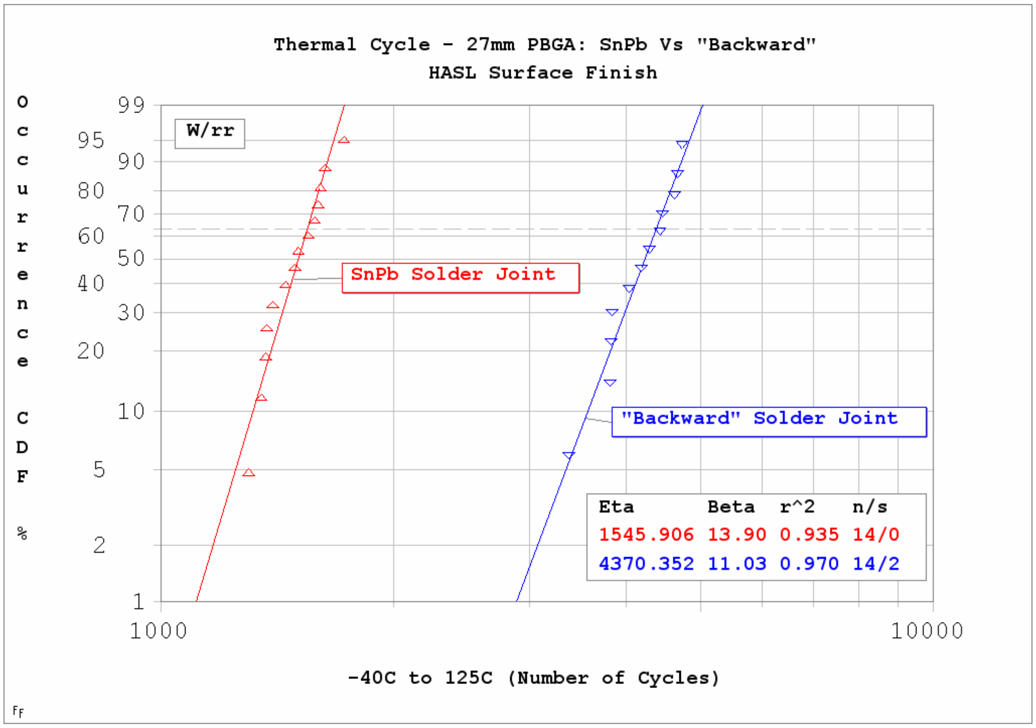


Figure 41: TV3D_C1 Weibull Plot – "Backward" Vs SnPb for 27mm PBGA (HASL)

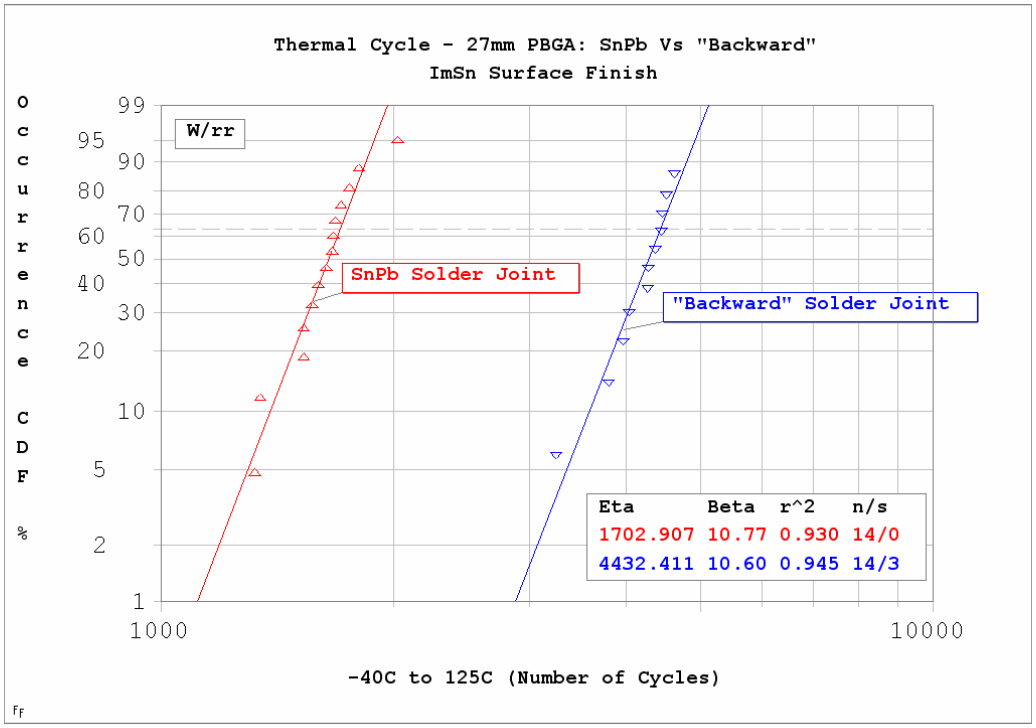


Figure 42: TV3D_C1 Weibull Plot - “Backward” Vs SnPb for 27mm PBGA (ImSn)

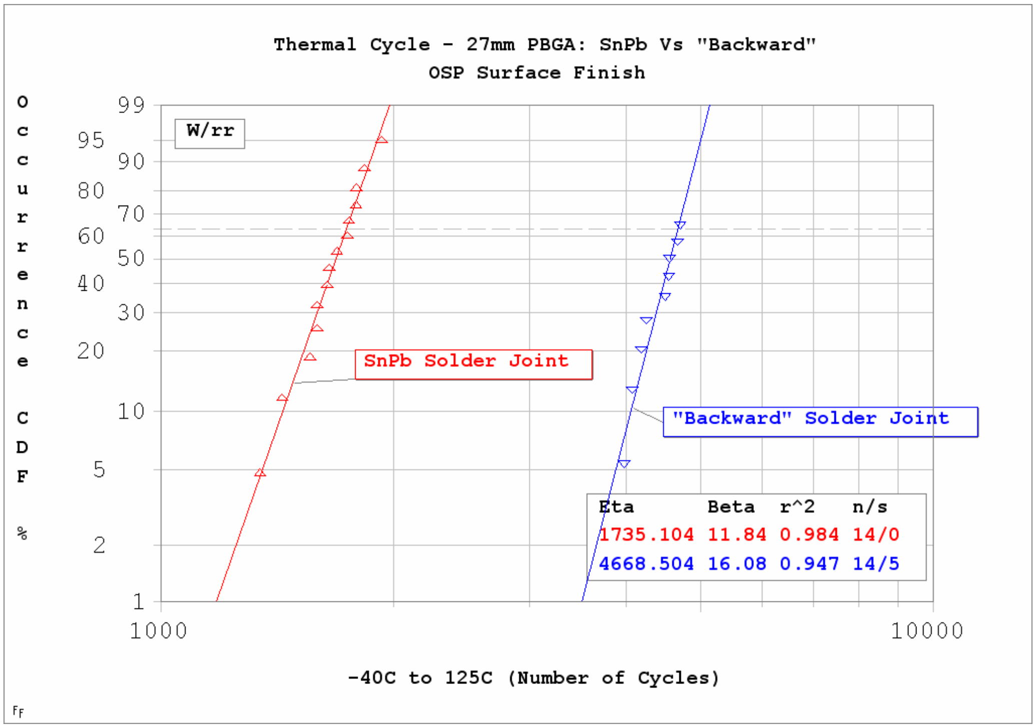


Figure 43: TV3D_C1 Weibull Plot - “Backward” Vs SnPb for 27mm PBGA (OSP)

Independent of surface finish, the characteristic life was significantly greater for the Pb-free packages. Also, the slopes (βs) were statistically equal for both the Pb-free and SnPbAg packages.

5.1.9 Summary

From the previous reliability data, the following can be concluded:

1) The surface finish had no impact on the slope (β) for all of the electronic packages (i.e. the failure modes remained similar).
2) The characteristic lives for all the packages were directly influenced by surface finish. Table 22 shows the comparison among the surface finishes for each type of electronic package. The "=" sign indicates that the characteristic lives were statistically equal. When the name of the surface finish appears in a cell, it statistically exhibited the larger characteristic life.

Characteristic Life (η) Comparison			
Package Type	**HASL Vs ImSn**	**HASL Vs OSP**	**ImSn Vs OSP**
2512 Resistor Banks	=	HASL	ImSn
27mm PBGA	ImSn	OSP	=
27mm PBGA (Pb-Free)	=	OSP	=
17mm PBGA	ImSn	OSP	=
17mm PBGA (Pb-Free)	n/a		
QFN	n/a		

Table 22: TV3D_C1 Surface Finish Comparison

In terms of providing an increased characteristic life for the electronic packages, the ImSn surface finish was statistically equal or better than the other two finishes. Except for the 2512 resistors, the packages assembled on HASL exhibited the lowest characteristic lives.

3) Independent of surface finish, the 17mm PBGAs significantly outperformed the 27mm PBGAs.
4) Independent of surface finish, the lead-free PBGAs assembled on SnPb paste significantly outperformed the SnPbAg PBGAs mounted on SnPb paste. In other words, the “backward” system increased the reliability of the PBGA packages in comparison with the traditional SnPb system.
5) The Pb-free 17mm PBGAs, the Pb-free 27mm PBGAs, and the QFNs met the automotive reliability requirements for thermal cycling. No failures for these packages occurred before 2,500 cycles.

A summary table (Table 23) was constructed for the packages tested on TV3D_C1. For each electronic package, the cycle to fail first, the characteristic life, and the slope were given. To be complete, the confident intervals for both η and β were calculated. The width of the confident intervals was dependent on the number of failures that occurred. Fewer failures increased the error of estimation for the Weibull parameters and consequently enlarged the CI width.

Electronic Package	1st Failure	Char. Life (η)	Slope (β)	95% CI on η	95% CI on β
Resistor Banks					
HASL	849	1,822.27	5.12	$1,630.92 \le \eta \le 2,036.08$	$3.60 \le \beta \le 7.28$
ImSn	1,042	1,949.68	6.96	$1,755.66 \le \eta \le 2,165.15$	$4.56 \le \beta \le 10.63$
OSP	851	1,520.58	6.91	$1,399.64 \le \eta \le 1,651.96$	$4.90 \le \beta \le 9.73$
27mm PBGA					
HASL	1,298	1,545.91	13.90	$1,485.26 \le \eta \le 1,609.03$	$9.55 \le \beta \le 20.24$
ImSn	1,321	1,702.91	10.77	$1,616.77 \le \eta \le 1,793.63$	$7.85 \le \beta \le 14.79$
OSP	1,342	1,735.10	11.84	$1,656.07 \le \eta \le 1,817.91$	$7.47 \le \beta \le 18.77$
27mm PBGA (Pb-Free)					
HASL	3,370	4,370.35	11.03	$4,141.82 \le \eta \le 4,611.49$	$6.36 \le \beta \le 19.15$
ImSn	3,247	4,432.41	10.60	$4,185.63 \le \eta \le 4,693.74$	$5.83 \le \beta \le 19.29$
OSP	3,979	4,668.50	16.08	$4,495.25 \le \eta \le 4,848.41$	$9.82 \le \beta \le 26.35$
17mm PBGA					
HASL	1,415	2,234.15	6.17	$2,043.09 \le \eta \le 2,443.07$	$3.77 \le \beta \le 10.10$
ImSn	1,465	2,670.29	6.07	$2,437.16 \le \eta \le 2,925.72$	$3.26 \le \beta \le 11.30$
OSP	1,717	2,596.53	6.76	$2,391.83 \le \eta \le 2,818.74$	$4.59 \le \beta \le 9.95$
17mm PBGA (Pb-Free)					
HASL	4,619	5,001.25	26.57	$4,230.05 \le \eta \le 5,913.05$	$0.68 \le \beta \le 103.26$
ImSn	4,394	5,099.40	14.19	$4,402.91 \le \eta \le 5,906.07$	$2.08 \le \beta \le 97.06$
OSP	>4816	n/a	n/a	n/a	n/a
QFN					
HASL	3,881	5,938.95	7.51	$4,610.13 \le \eta \le 7,650.77$	$2.03 \le \beta \le 27.79$
ImSn	4,016	5,471.04	10.22	$4,746.82 \le \eta \le 6,305.76$	$3.57 \le \beta \le 29.22$
OSP	4,291	5,067.64	18.75	$4,834.76 \le \eta \le 5,311.75$	$7.57 \le \beta \le 46.45$

Table 23: TV3D_C1 Reliability Summary

5.2 TV3D Configuration 1 Failure Analysis

This section will address the failure mechanism of the electronic packages mounted on the TV3D_C1 test vehicle. The primary focus of discussion will be the reasoning behind the reliability increase of the “backward” solder joint over the traditional SnPb solder joint. Secondary, the impact of surface finish and the effect of PBGA body size will be addressed. Before these topics are covered, the failure mechanics of the thermally cycled PBGA packages are described below.

During thermal cycling testing, the solder joint failure of the PBGAs was attributed to the interaction between fatigue and creep. During the heating and cooling cycle, shear stresses act upon the solder joint creating tension and compression forces.

These shear stresses were a direct result of the CTE mismatches among the silicon die, PBGA substrate, and the printed circuit board. For the PBGA packages used in TV3D_C1, the main concentration of stress occurred at the solder mask defined (SMD) interface on the PBGA side of the solder joint (Figure 44).

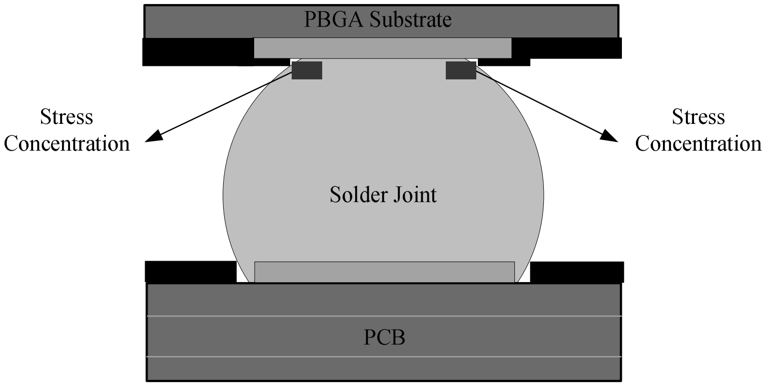


Figure 44: PBGA Solder Joint Stress Concentration

The high concentration of stress was a direct result of limited contact area available to help absorb stresses during temperature cycling.

In order to relieve the shear stress, the solder joint strained. The long dwell time started the creep process which strained the solder. Even though the stress was relieved by the strain during the hot temperature dwell, plastic deformation occurred. Eventually cracks began to initiate at the high stress concentrated areas of the solder ball. As the cycling process continued, plastic deformation limited the amount of stress relieved. The cracks then propagated through the solder ball resulting in electrical failure (Figure 45).

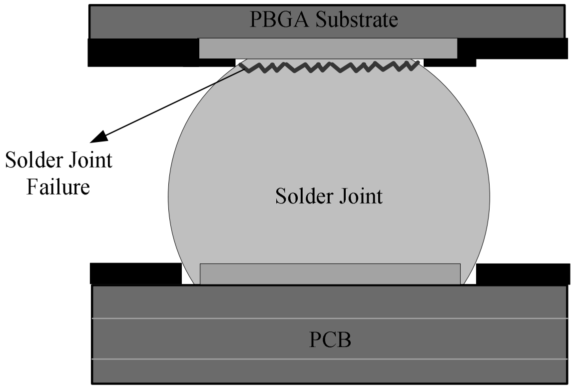


Figure 45: PBGA Solder Joint Failure

5.2.1 Backward Vs SnPb System

The Pb-free solder balls mounted on SnPb solder paste doubled the reliability of SnPbAg balls mounted on SnPb solder paste. The increase of reliability occurred for the "backward" system because of the following reasons: (1) "aggressive" SnPb profile, and (2) superior creep resistance [38, 39].

Because of the higher melting point of the Pb-Free solder balls (~217ºC), a "aggressive" SnPb profile was used in the assembly process. The aggressive profile included a higher reflow temperature (235ºC) and increased times within the soak and reflow zones. This reflow profile allowed for sufficient mixing between the Pb-free solder balls and the SnPb paste (Figure 46). The sufficient mixing of the solder joint was fundamental for the "backward" system to perform adequately when subjected to accelerated life testing.

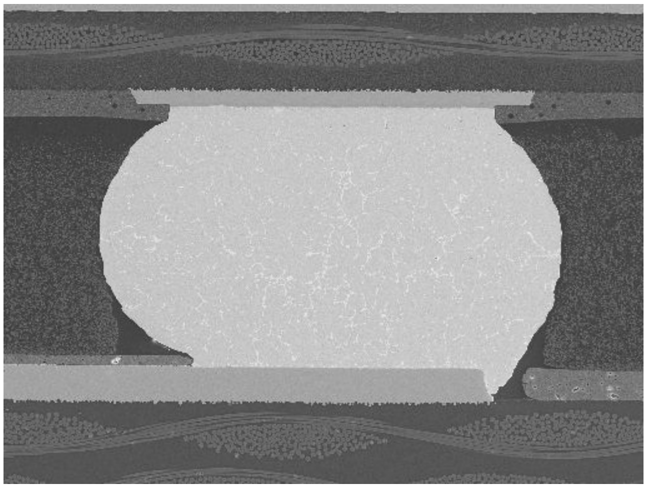


Figure 46: Completely Mixed Solder Joint

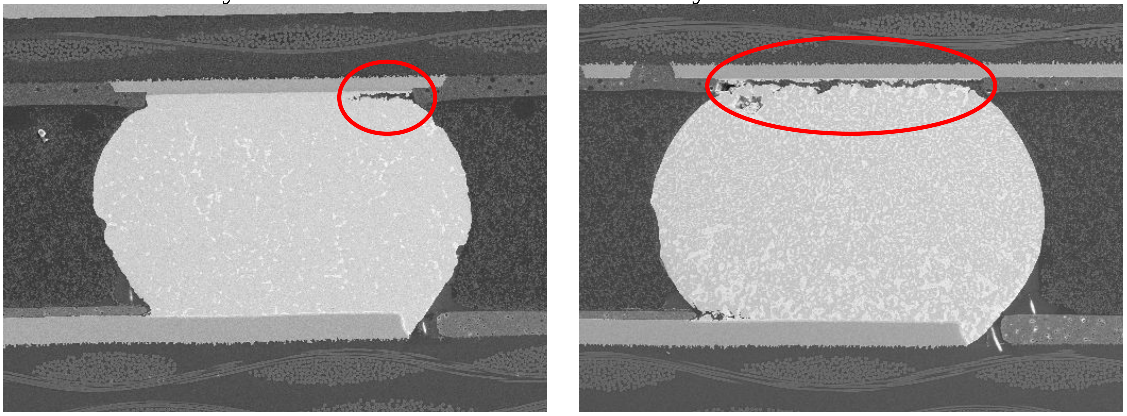
This solder joint was composed of 95.5%Sn-3.8%Ag-0.7% solder ball with 63%-37% solder paste. Taking into account the volumetric area of the solder ball and the solder paste, a rough calculation was performed to determine the percent contribution of each element for the solder joint (The calculations and equations are located in Appendix H). The results are shown below in Table 24.

% of Solder Joint	
Sn	90.95%
Ag	3.27%
Cu	0.60%
Pb	5.18%

Table 24: Solder Joint Element Percentages

Based upon recent literature [37-40], Pb-free solder joints have exhibited greater creep resistance abilities when compared to SnPb solder. The resilience against creeping for the Pb-free solder joint is directly related to its finely distributed microstructures. Wiese et al [40] and Kang et al [41] conducted research that concluded that high Sn content will produce β-Sn crystals. The β-Sn crystals are body-centered tetragonal (BCT) in which their restricted symmetry limit plastic deformation [41].

In the “backwards” solder joint, the Sn content was estimated at 91%. Therefore, the mixed solder joint experienced similar characteristics with a lead-free solder joint. Since, the “resistance to creep” attribute was exhibited during thermal cycling, the plastic deformation during the hot temperature dwell was minimal. The reduction of plastic deformation prevented cracks from initiating through the “high stress” concentrated areas and prolonged the life of the mixed solder joint. Similar results were demonstrated with the research conducted by Mawer and Levis [13]. Shown below (Figure 47) are representative SEM photos of crack propagation for the “backward” and SnPb systems after 3,142 thermal cycles.



“Backward” System

SnPb System

Figure 47: Backward Vs SnPb Solder Joint

5.2.2 Effect of PBGA Size

The 17mm PBGAs displayed superior reliability than the 27mm PBGAs. Both PBGA packages had identical characteristics. These included: pitch (1.0mm), solder ball diameter (0.6mm), copper pad diameter (0.5mm), pad geometry (SMD). Because of the previous attributes, the solder ball collapse/height between the two PBGA packages was approximately equal. Other than body size, no pronounced differences existed between the critical design parameters that affect PBGA reliability. The discrepancy in reliability data can be explained by the "distance from neutral point (DNP)" phenomenon.

DNP is the distance from the neutral point (i.e. center) of the BGA to the outside solder ball. Refer to Figure 48 for the DNP approximations for both types of PBGA packages.

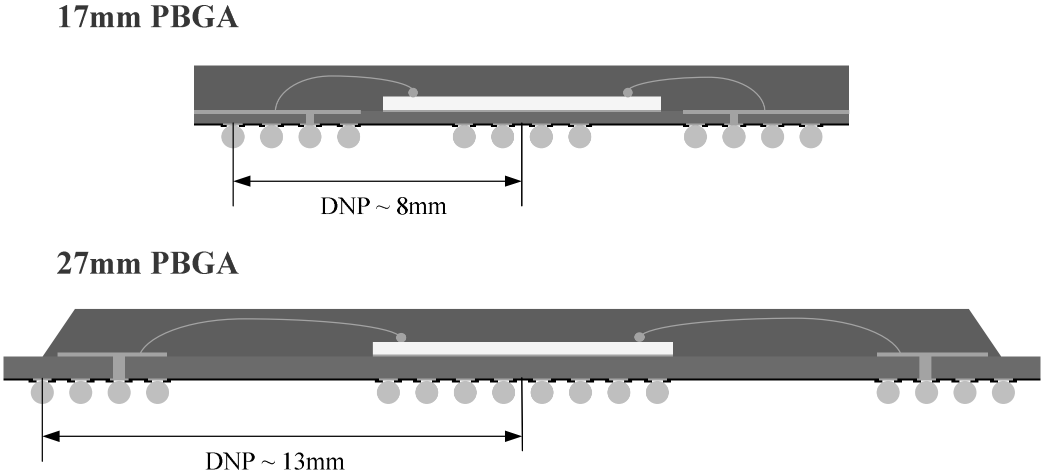


Figure 48: Distance From Neutral Point (DNP)

Different researches [42-44] have shown that maximum stress and strain is experienced at the free edge of the solder joint. In other words, the solder ball farthest away from the center experienced the highest degradation of reliability. This evidence coincides with the reliability results incurred in this research. The DNP for the 27mm PBGA was greater than the 17mm PBGA. Thus, the outer row of solder balls for the 27mm PBGAs was more susceptible to failure. The DNP theory explains why earlier failures were encountered for the 27mm PBGA packages.

5.2.3 Impact of Surface Finish

In terms of providing an increased characteristic life for the electronic packages, the ImSn surface finish was statistically equal or better than the other two finishes. Except for the 2512 resistors, the packages assembled on HASL statistically exhibited the lowest characteristic lives. The discrepancy of reliability between HASL and ImSn can be attributed to surface finish planarity (i.e. flatness). The surface thickness for HASL has extremely high variability. In one study by Prasad [45], the variations for HASL's thickness ranged from 0.8μm to 38μm. In contrast, Vianco [46] documented the variation of ImSn finishes to range from 7.6μm to 13μm. The ImSn provides a flatter surface finish on the test vehicle.

A study by Ormerod [47] concluded that surface finish planarity can reduce the variance of solder joint volume up to 50%. Without planarity, some solder joints in the PBGA package could be fragile due to reduced solder volume. With the reduction of solder joint volume, the shear stresses and strains induced by thermal cycling will decrease the life of the electronic package. The lack of solder joint volume for the PBGAs mounted on HASL could explain the reason for their early failures.

CHAPTER 6: TV3D_C2 RELIABILITY & FAILURE ANALYSIS

This chapter presents and discusses the failure modes of the electronic packages mounted on the TV3D_C2 test vehicle. The first section reviews the reliability data, while the second section discusses the failure mechanisms.

6.1 TV3D Configuration 2 Reliability Analysis

The TV3D_C2 test vehicles were liquid-liquid thermally shocked between -40ºC to 125ºC with a 14 minute cycle time. Seven boards from the five different combinations (35 total boards) were tested. All of the boards had Immersion Silver (ImAg) surface finish. As a reminder, the five different combinations were named from the interaction of the solder ball, solder paste, and the reflow profile of the PBGA. The nomenclature developed was (solder ball composition – solder paste – reflow profile) where “LF” designated lead-Free and “L” designated lead. Each test vehicle included two identical 17mm PBGA packages and two resistor banks. Table 25 shows the test matrix used for TV3D_C2 testing.

Nomenclature	Solder Balls	Solder Paste	Reflow Profile	Num Boards
LF-LF-LF	Sn-3.8Ag-0.7Cu	Sn-3.0Ag-0.5Cu	Pb-Free	7
LF-L-LF	Sn-3.8Ag-0.7Cu	Sn-37Pb	Pb-Free	7
LF-L-L	Sn-3.8Ag-0.7Cu	Sn-37Pb	SnPb	7
L-L-L	Sn-36Pb-2Ag	Sn-37Pb	SnPb	7
L-L-LF	Sn-36Pb-2Ag	Sn-37Pb	Pb-Free	7

Table 25: TV3D_C2 Test Matrix

Only the perimeter array of 17mm PBGA solder balls was monitored during testing. As stated earlier, three combinations of the 2512 resistor banks existed. The resistors were subject to three different interactions between the solder paste and the reflow profile. These interactions included the resistors assembled on Sn-3.0Ag-0.5Cu paste with a Pb-free profile, and assembled on Sn-37 solder paste subjected to either a SnPb or Pb-free reflow profile.

To determine if the cycles to failure of identical electronic packages assembled on the same board were independent of location, the Paired t-Test and the Wilcoxon Signed Ranks were performed. Both statistical tests concluded that the cycles to failure of the 2512 resistor banks and 17mm PBGA packages were independent of board location. (See Appendix I for results). Table 26 represents the sample sizes for the 17mm PBGAs and the 2512 resistor banks.

17mm PBGA	Sample Size
LF-LF-LF	14
LF-L-LF	14
LF-L-L	14
L-L-L	14
L-L-LF	14

2512 Resistor Banks	Sample Size
Pb-Free Paste / PbFree Profile	14
SnPb Paste / SnPb Profile	28
SnPb Paste / PbFree Profile	28

Table 26: TV3D_C2 Sample Sizes

After 1,000 and 2,000 cycles, predetermined boards were removed from the test for cross sectioning and surface science analysis. The liquid-liquid shock chamber completed 3,000 cycles before the test was terminated. All of the electronic packages exhibited complete failure after 3,000 cycles.

The following sections will discuss pertinent reliability data for the electronic packages assembled on the TV3D_C2. The results for the hypothesis testing between data sets, on both η and β, are located in Appendix J. The r^2 values for all the data sets were greater than 0.85 which indicated the data sets fit the Weibull distribution well.

6.1.1 2512 Resistors

Figure 49 shows the Weibull plot for the three combinations of resistors.

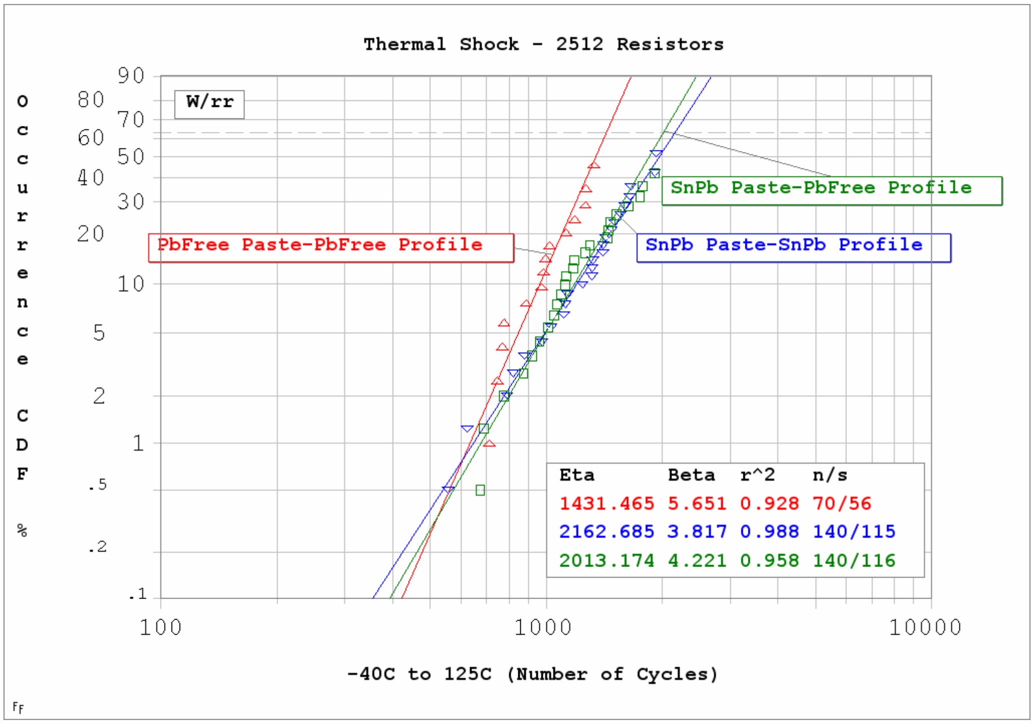


Figure 49: TV3D_C2 Weibull Plot - 2512 Resistors

Statistically, no differences were observed in the slope (β) among the three resistor combinations. No statistical difference in η was observed between the resistors with SnPb paste / Pb-free Profile and SnPb Paste / SnPb Profile. The resistor combination, Pb-free paste / Pb-free Profile, had a characteristic life (η) of 1,431 cycles which was statistically lower than the other two combinations.

6.1.2 Backward Compatibility (Different Reflow Profiles)

Figure 50 shows the Weibull plot comparing the “backward” systems with different reflow profiles for the 17mm PBGA package.

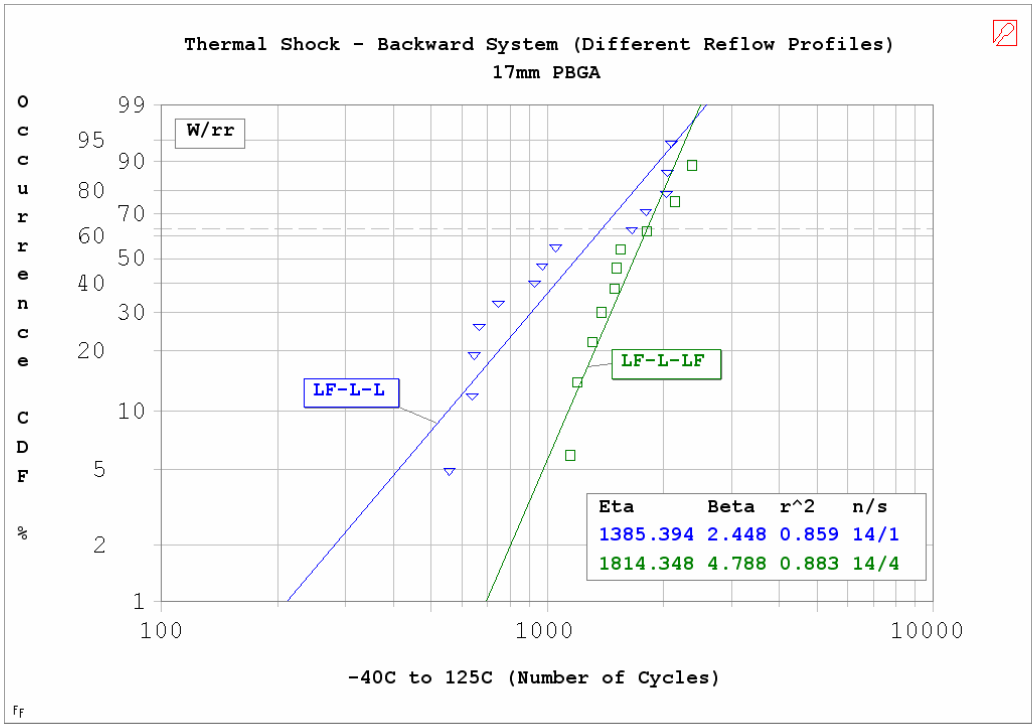


Figure 50: TV3D_C2 Weibull Plot - Backward Solder Joint (Reflow Profiles)

Statistically, differences were observed between the slope (β) and the characteristic life (η). The “backward” combination with the SnPb profile had a lower characteristic life.

6.1.3 SnPb Vs Pb-free Vs Backward Systems

Figure 51 shows the Weibull plot that compares all three solder joint combinations for the 17mm PBGA package.

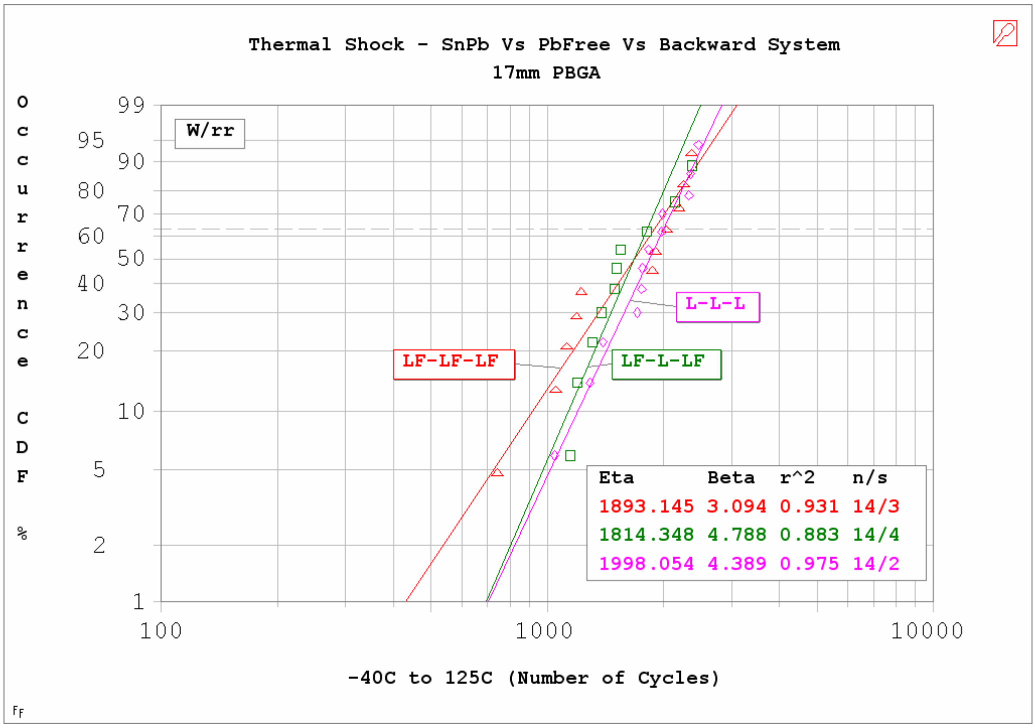


Figure 51: TV3D_C2 Weibull Plot - SnPb Vs Pb-Free Vs Backward Systems

In comparing the characteristic life and the slope among all three data, no statistical differences were observed among the three different assemblies.

6.1.4 Summary

From the previous reliability data, the following can be concluded:

1) The resistors that were assembled with Pb-free paste and Pb-free profile demonstrated a lower characteristic life in comparison with the other two combinations.

2) In comparing the “backward” systems with two different profiles, the SnPb profile significantly decreased the reliability of the package.

3) In comparing the SnPb, Pb-free, “backward” assemblies, no statistical differences existed between their slopes and characteristic lives. As in the case of the TV3D_C1 design, the vast improvement in reliability of the “backward” system was not realized.

A summary table (Table 27) was constructed for the packages tested on TV3D_C2. For each electronic package, the cycles to first failure, the characteristic life, and the slope were given. To be complete, the confident intervals for both η and β were calculated.

Electronic Package	1st Failure	Char. Life (η)	Slope (β)	95% CI on η	95% CI on β
Resistor Banks					
Pb-Free Paste / Pb-Free Profile	712.0	1,431.47	5.65	$1,270.15 \le \eta \le 1,613.27$	$3.76 \le \beta \le 8.50$
SnPb Paste / SnPb Profile	556.0	2,162.69	3.82	$1,838.42 \le \eta \le 2,544.19$	$2.71 \le \beta \le 5.38$
SnPb Paste / Pb-Free Profile	673.5	2,013.17	4.22	$1,818.48 \le \eta \le 2,228.73$	$3.29 \le \beta \le 5.42$
17mm PBGA					
LF-LF-LF	741.0	1,893.15	3.09	$1,560.38 \le \eta \le 2,296.86$	$1.74 \le \beta \le 5.49$
LF-L-L	557.0	1,385.39	2.45	$1,098.18 \le \eta \le 1,747.72$	$1.65 \le \beta \le 3.64$
LF-L-LF	1148.0	1,814.35	4.79	$1,595.56 \le \eta \le 2,063.13$	$3.18 \le \beta \le 7.21$
L-L-L	1044.0	1,998.05	4.39	$1746.09 \le \eta \le 2286.38$	$2.54 \le \beta \le 7.60$
L-L-LF	1718.0	2,272.71	10.63	$2139.8 \le \eta \le 2414.36$	$5.73 \le \beta \le 19.72$

Table 27: TV3D_C2 Reliability Summary

6.2 TV3D Configuration 2 Failure Analysis

This section will discuss the failure mechanics of the electronic packages mounted on the TV3D_C2 test vehicle. The primary focus will discuss the reliability among the SnPb, Pb-free, and “backward” systems. Other items that will be addressed include the following: (1) degradation of reliability for the resistors assembled with Pb-free paste and (2) impact of the SnPb reflow profile for “backward” assembly. Before these topics are covered, the failure mechanics of the thermally shocked PBGA packages are described below.

In comparing the thermal shock and thermal cycle test, the thermal shock test significantly decreased the life of the electronic packages. In the shock test, the ramp rate from hot to cold and cold to hot was approximately 82.50ºC/minute. The intense ramp rates exaggerated the CTE mismatch among the solder joint and its surrounding materials. The heightened CTE mismatch caused brutal shear stresses to act upon the solder joint. Through repeated cycling, the extreme shear stresses fatigued the solder joint to failure.

6.2.1 PBGA Failures for SnPb Vs Pb-free Vs Backward Systems

The SnPb, Pb-free, and the “backward” solder joints, with respect to β and η, performed equally. These results were surprising because the same failure trend that occurred for the thermally cycled 17mm PBGAs (i.e. the Pb-free PBGAs significantly outperform the SnPbAg PBGAs) was expected. Also, previous research studies, [13, 25], concluded that Pb-free and “backward” systems exhibited increased reliability in comparison with the SnPb solder joints. However, this research was conducted in a thermal cycling environment with slow ramp rates and long dwell times. Slow ramp rate and long dwell times created an environment with moderate shear stress levels and high rates of creep. Due to their high resistively of creep, the Pb-free and “backward” solder joints were better suited for thermal cycling.

Shock testing substantially increased the shear stresses applied to the solder joint. The increase of shear stress was due to the increased strain rates from the surrounding materials. Thus, the reliability of the solder joint was directly related to its ability to accommodate the added stress without fracturing (i.e. fracture toughness). Fracture toughness can be defined as the resistance to crack initiation and growth. In a study by Siow and Manoharan [48], the fracture toughness of SnPb (Sn-37Pb) and Pb-free (Sn-3.5Ag) were determined by applying two types of stresses, tensile and shear. Siow and Manoharan concluded that the SnPb solder joint had higher fracture toughness. Also, Liang et al [49] determined that "at higher stress-strain levels, the Sn-Pb eutectic solder has superior fatigue resistance to Pb-free alloys".

The toughness of the solder joint is dependent upon its modulus of elasticity, ultimate tensile strength, and ductility. In reviewing the previous literature [50-53] that compared the characteristics between SnPb and lead-free solders the following was concluded: (1) The ultimate tensile strength was greater for Pb-free solders, (2) the modulus of elasticity was greater for Pb-free solder, and (3) the ductility was greater for the SnPb solders.

During the thermal shock test, the SnPb solder joints were able to compensate for their lack of tensile strength and modulus of elasticity through increased ductility. In other words, the SnPb solder joints were able to plastically deform without fracturing. On the other hand, the Pb-free and "backward" solder joints were able to compensate for their low ductility through increased tensile strength and higher modulus of elasticity. The tradeoffs that were encountered during the shock testing equalized the reliability among the SnPb, Pb-free, and "backward" systems.

6.2.2 Lead Free 2512 Resistors

The resistors assembled with Pb-free paste demonstrated a lower characteristic life in comparison with the other two types of resistors solders with SnPb paste. Once again, this can be contributed to the inherent mechanical properties that existed between the SnPb and Pb-Free solders. The failure was caused from the CTE mismatch between the ceramic resistor (4-5 ppm/ºC) and the printed circuit board (14-20 ppm/ºC) [54]. The brittle Pb-free solder paste was not able to sufficiently accommodate the severe stresses and strains during the the thermal shock testing.

6.2.3 Reflow Profile Impact on Backward Assembly

For the Pb-free PBGA packages mounted on SnPb solder paste, the SnPb profile significantly decreased the reliability of the package. This result was consistent with previous research studies [29]. The SnPb reflow profile was not sufficient at melting the Pb-free solder ball.

As calculated earlier, the solder ball consumed approximately 86% of the total solder joint volume. The Pb-free solder ball had a melting point of 217ºC and the maximum temperature that the SnPb reflow profile reached was ~218ºC. Since the time above liquidus (TAL) was almost negligible, the Pb-free solder did not properly melt and mix with the SnPb solder paste. But, this does not fully explain the failure distribution of the “backward” solder joint with the SnPb reflow profile.

Figure 52 below shows the Weibull distribution for the “backward” solder joint assembled with the SnPb reflow profile.

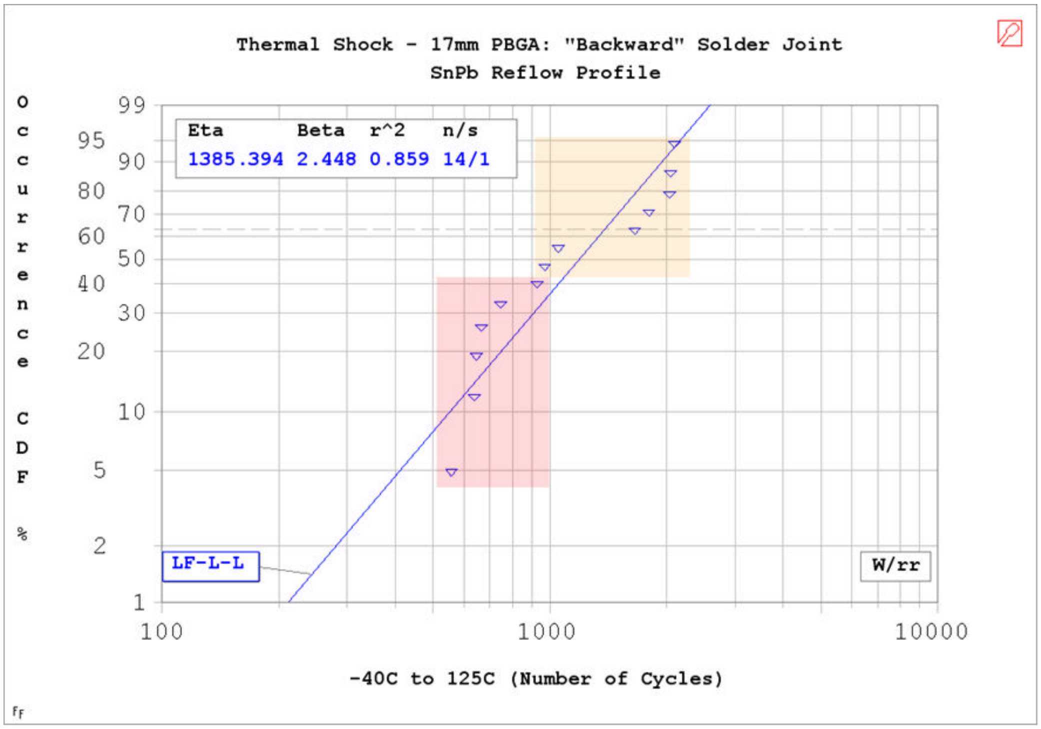
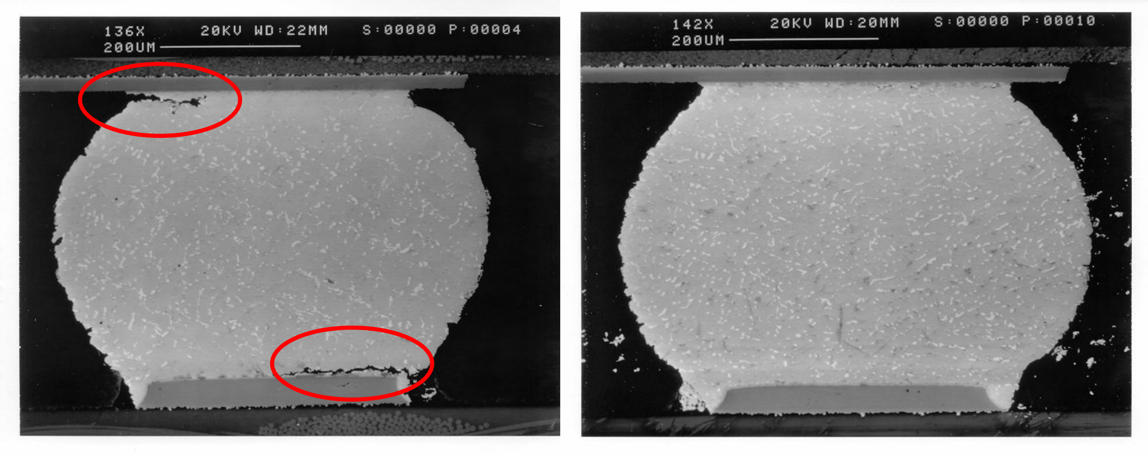


Figure 52: LF-L-L Bimodal Distribution

The LF-L-L combination appeared to demonstrate a bimodal distribution (shaded areas). The bimodal distribution could have resulted from solder ball collapse differences among the solder joint locations throughout the 17mm PBGA.

Different failure modes existed between the "backward" solder joints with different reflow profiles. For the "backward" solder joint, the stresses during the thermal cycle were heavily concentrated on the board side interface. In fact, more than half of the solder joints cross-sectioned had cracking concentrated on the PCB side interface. On the other hand, the "backward" solder joints (lead free profile) exhibited cracking primarily on the component interface. Figure 53 shows the crack propagation (after 3000 cycles) for the "backward" solder joint with a SnPb profile versus a Pb-free profile.


“Backward” Solder Joint – SnPb Profile

“Backward” Solder Joint – SAC Profile

Figure 53: Backward Solder Joint Failures

CHAPTER 7: CONCLUSIONS & FUTURE WORK

7.1 Conclusions

This thesis focused on quantifying the reliability of lead free PBGA packages assembled with SnPb solder paste (i.e. Backward Compatibility). Two test vehicles were designed to accommodate PBGA packages with body sizes of 17x17mm and 27x27mm. Each test vehicle was subjected to a different type of accelerated testing method.

The first test vehicle (TV3D_C1) was populated with both 17mm and 27mm PBGAs with SnPb and “backward” solder joints. An aggressive SnPb profile was used to ensure proper melting and mixing of the Pb-free solder ball. The test vehicles were then subjected to air-to-air thermal cycling with a temperature range from -40ºC to 125ºC. The cycle time was 90 minutes with 15 minutes dwells at each temperature extreme and ramp rates of approximately 5-6ºC/minute. From this type of testing environment, the following was concluded: (1) The reliability for both Pb-free PBGAs assembled with SnPb paste was twice that of the SnPb PBGAs assembled with SnPb, (2) The Pb-free 17mm and 27mm PBGA packages qualify for under-the-hood electronics, (3) The increase of reliability for the Pb-free PBGA packages was directly related to their resistively to creep, (4) The 17mm and 27mm PBGA packages mounted on the ImSn surface finish significantly outperformed the packages mounted on the HASL surface finish, and (5) Independent of surface finish, the 17mm PBGA packages had a significantly greater reliability than the 27mm PBGA packages.

The second test vehicle (TV3D_C2) was populated with 17mm PBGAs with SnPb, Pb-free, and “backward” solder joints. These test vehicles were subjected to liquid-to-liquid thermal cycling with a temperature range from -40ºC to 125ºC. The cycle time was 15 minutes with 5 minutes dwells at each temperature extreme and ramp rates of approximately 82.50ºC/minute. From this type of testing environment the following was concluded: (1) All three types of PBGA assemblies (i.e. SnPb, Pb-free, “backward” – Pb-free reflow profile) performed equally, (2) The reliability of the solder PBGA joints was directly related to their fracture toughness. Fracture toughness of the solder joint was a function of its modulus of elasticity, tensile strength, and ductility. The tradeoffs that were encountered during the shock testing equalized the reliability among the SnPb, Pb-free, and “backward” systems. (3) The reliability of “backward” solder joints was heavily dependent on the reflow profile. The reflow profile must have an adequate time above liquidus to properly melt the Pb-free solder ball so it can mix with the SnPb solder paste. But, a bimodal distribution was detected for the “backward” assembly with a SnPb reflow profile. This indicated that solder joints did not experience uniform ball collapse and mixing.

In conclusion, the reliability of Pb-free PBGA packages assembled with lead-free solder paste was dependent upon the accelerated life testing environments. For environments with slow ramp rates and long dwells the “backward” assembly will significantly outperform the SnPb solder joints. On the other hand, for environments with severe ramp rates the “backward” solder joints will perform equally with SnPb solder joints. If the reflow profile can sufficiently melt the Pb-free solder ball, no degradation of reliability, in comparison with SnPb solder joints, will be realized when Pb-free PBGAs are assembled with SnPb paste.

7.2 Future Work

To expand upon this research, future work can be conducted. Suggestions to further this research are the following: (1) air-to-air cycle the TV3D_C2 boards to determine if the results for the 17mm PBGAs are similar to the 17mm PBGA tested on TV3D_C1, (2) Experimentally determine the toughness (i.e. Area under the stress-strain curve) through tensile/shear testing of the SnPb solder joints and “backward” solder joints. Construct test specimens to properly account for the percentage contribution of each element by determining the volumetric ratios of the solder ball and solder paste. (3) Experimentally determine the strain rates of the different materials on the test vehicle that occurred in the air-to-air thermal chamber and liquid-to-liquid thermal chamber (4) Perform additional cross sectioning on the TV3D_C2 test vehicles for the “backward” solder joints assembled with the SnPb reflow profile. The PBGA packages cross sectioned should correspond to the PBGA packages that experienced early failures. Analysis should be performed to determine the microstructural differences among the solder joint locations under the 17mm PBGA.

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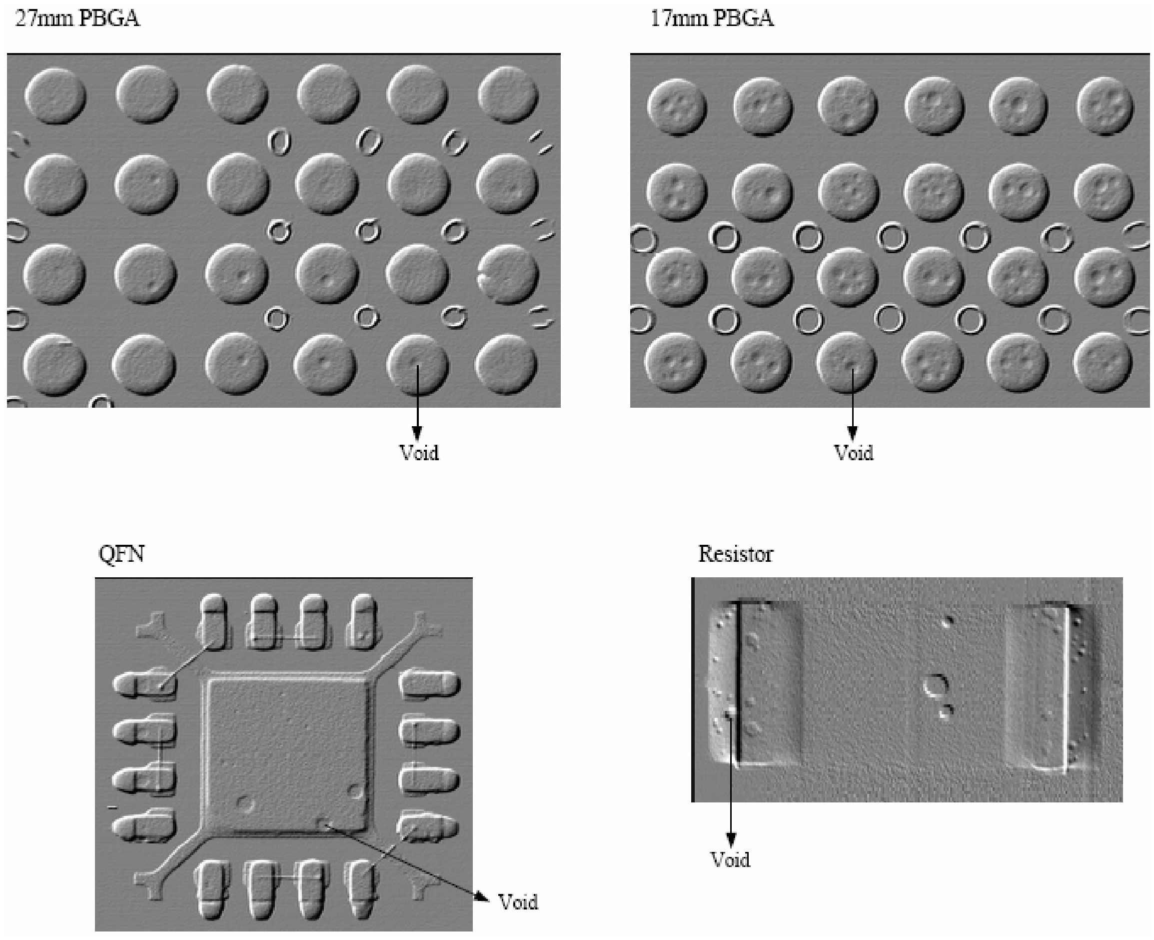
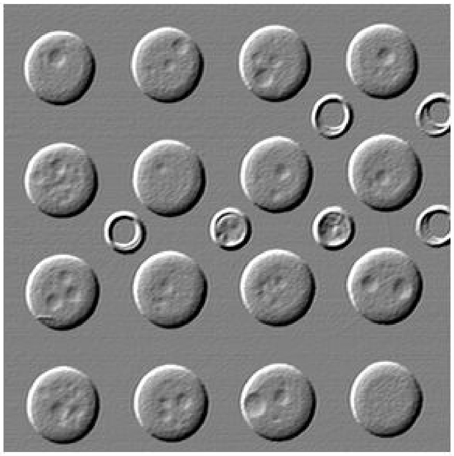
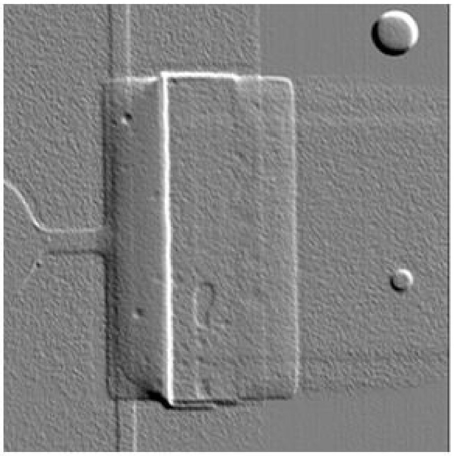
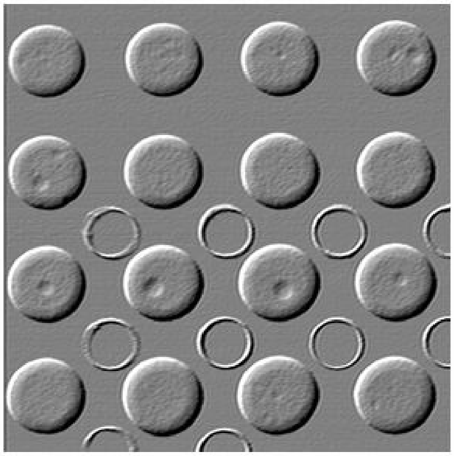
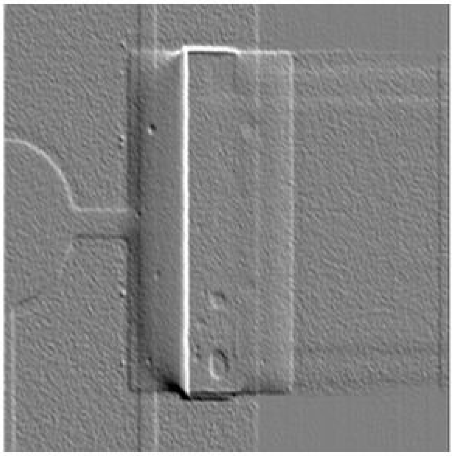
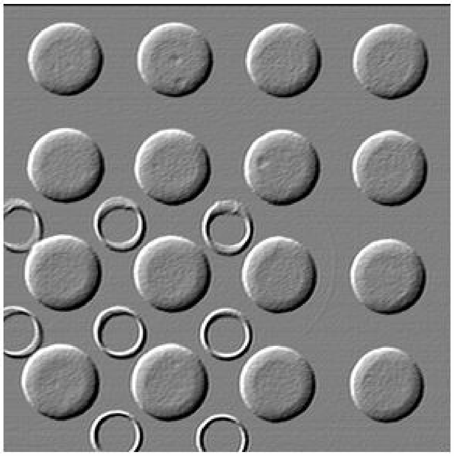
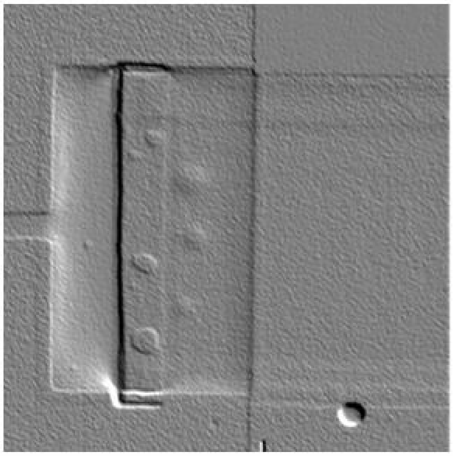
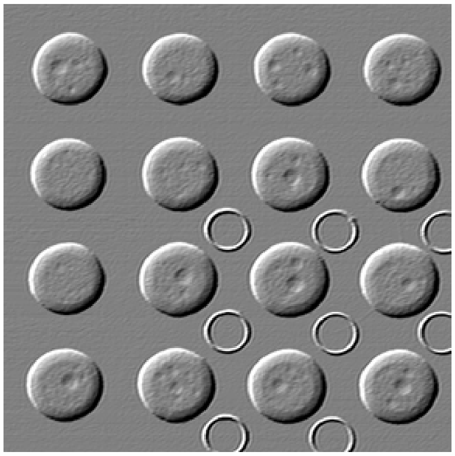
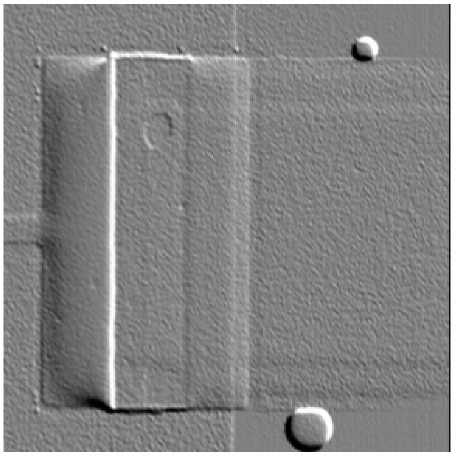
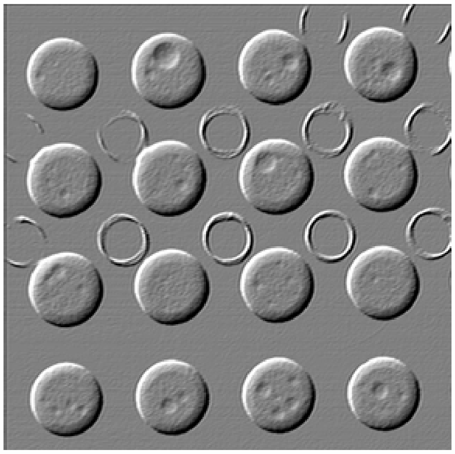
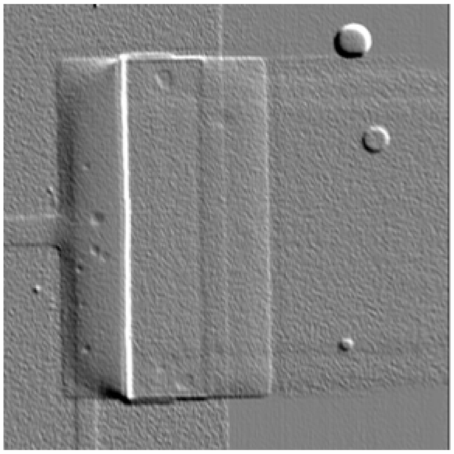
APPENDIX A: TV3D Configuration 1 Voiding Pictures



APPENDIX B: TV3D Configuration 2 Voiding Pictures

	17mm PBGA	Resistor
LF-LF-LF		
LF-L-LF		
LF-L-L		

	17mm PBGA	Resistor
L-L-L		
L-L-LF		

APPENDIX C: Cross Section Procedure

Step I: Underfill the Electronic Package

1. Retrieve the underfill and allow 30 minutes for the underfill to thaw out.
2. Retrieve a hot plate and heat it to 110ºC. For accuracy, use a thermocouple to ensure that the hot plate is 110ºC.
3. Place the board on the hotplate.
4. Using a suitable syringe tip, dispense the underfill on the sides of the desired electronic component.
5. Bake the board at 165ºC for 20-25 minutes.

Step II: Coating the Plastic Holders

1. Retrieve the red/blue plastic holders.
2. Retrieve the silicone release agent (Buehler Release Agent).
3. Apply the silicone agent liberally to the inside of the plastic holders.
4. Let the silicone agent dry (5 minutes), and then reapply.
5. Label all of the holders so that each cross section can be easily identified.

Step III: Cutting the Electronic Package

1. Using a fine tipped permanent marker, mark the area of interest of the electronic package.
2. The Isomet 1000 wet saw is used to make the cuts.
3. If the coolant is clean, continue, otherwise replace solution:
    a. 1 part coolant with 9 parts water (ratio 1:9).
    b. Cover the bottom of the saw with 3/8” of the solution.

4. Dress the cutting blade at 250 rpm - 2 passes.
5. Develop a cutting scheme for the electronic package.
6. Cutting speed at ~ 200 rpm.
7. Cut “proud” of the electronic package.
8. When finished, empty and replace the solution.

Step IV: Pouring Epoxy Resin

1. Retrieve the Sampl-Klips.
2. Put these clips on all of the samples.
3. With the use of tweezers, put the area of interest down (flush) in the holder.
4. Using the appropriate ratio, mix the epoxy resin & hardener in a Dixie cup.
5. Mix the resin and hardener by scooping with a tongue depressor from the bottom while tipping the cup at the angle. The mixture should turn clear when completely mixed.
6. Lay down aluminum for all of the plastic holders to be placed on.
7. Pour the epoxy on the sample. Start the pouring directly on the samples. The mold is completed when the epoxy resin completely covers the sample.
8. Allow 24 hours at room temperature for hardening.

Step V: Polishing Part 1

1. While the sample is still in the mold, etch onto the top of the mold the details of the sample so that they can be distinguished.
2. Push the sample out of the plastic holder
3. The surface grinder/polisher is the Ecomet 6.

4. Turn the main water valve on.
5. Take the metal clamp off of the wheel and put on the 250 grit paper.
6. Once the paper is secured on the wheel, turn on the water and make sure the stream of water hits the middle of the wheel.
7. Turn the wheel On ➔ 150 – 200 rpm.
8. Wet the sample.
9. With moderate pressure, place the sample on the spinning wheel. Move the sample back & forth for 3-5 seconds. Lift the sample up, rotate 90º, and place it back on the spinning wheel. (~3 minutes)
10. When the solder ball/termination is noticeable, switch to the 750 grit paper and apply the same routine a mentioned before. (~3 minutes)
11. Put the 1,200 grit paper on the polisher and apply the same routine. (~3 minutes)

Step VI: Polishing Part 2 – Masterprep

1. Replace the 1,200 grit paper and replace it with a magnetic black cover (Chemomet).
2. Turn the water on to dampen the black cover.
3. Shake the white masterprep solution.
4. Wet the sample.
5. Turn the wheel on ➔ 200 rpm.
6. While the wheel is spinning add a couple drops of the masterprep solution every 5-6 seconds.

7. With moderate pressure, place the sample on the spinning wheel. Move the sample back & forth for 3-5 seconds. Lift the sample up, rotate 90º, and place it back on the spinning wheel.
8. To check the progress, clean the sample and look under the microscope. The scratches in the sample should be disappeared and everything should be clear.
9. This process takes approximately 5-7 minutes.
10. When finished, turn the water off and squeegee the solvent out. To dry the black surface, increase the wheel speed to 300 rpm and let it spin for 5 minutes.
11. Wash off and dry the samples with compressed air.

APPENDIX D: Gold Coating Procedure

1. Put gloves on to prevent contamination.
2. Open the black (On top of the argon cylinder) knob. Make sure the pressure does not falls below 500 psi.
3. Open the green knob on the outside of the machine.
4. Put the samples in the holder and make sure that the surface to be coated is face up.
5. Encase the samples and make sure there is a good seal without pinching the tubing.
6. Before the key is inserted into the machine, the initial settings should be the following:
    a. Discharge Current = 0
    b. Timer (Minutes) = 0
    c. Timer setting = Manuel
    d. Bottom Left Knob Setting = Plate DC
    e. Pulse switch = Off
    f. Gas switch = Off
    g. Voltage at ZERO and turned off
7. Put the key into the machine and turn the machine ON.
8. Watch the vacuum pressure, and start the process when the pressure stops at 20/40 milli-torr. (~5 minutes)
9. Turn the gas switch ON. The pressure will rise back up to 80 and fall back to 60 milli-torr. When the pressure stops at 60, begin. (~10-15 minutes)

10. The SEM works best with 3.5 minutes of gold coating. But, the longest time to coat the sample should be no longer than 2 minutes. So, perform 2 minutes of coating followed by 1.5 additional minutes.
11. Turn the voltage switch ON.
12. Set timer = Auto.
13. Set timer for 2 minutes.
14. Then turn the voltage knob until 15 milliamps is established. The voltage might have to be continually adjusted to maintain the 15 milliamps. (The 15 milliamps usually requires 5-8 volts).
15. The voltage is automatically stopped when the timer is up.
16. Turn the voltage back to zero.
17. Reset the timer for one more iteration
18. Turn Voltage back to Zero.
19. Voltage switch = Off.
20. Timer = Manuel.
21. Gas = Off.
22. Power = Off.
23. Remove the samples.
24. Turn green and black valves off.
25. Wipe the glass jar to remove gold residue.
26. Turn key to the off position and remove from machine.

APPENDIX E: Paired t-Test Vs Wilcoxon Signed Ranks Test

The Paired t and the Wilcoxon signed ranks tests were used to determine if the cycles to failure of the same electronic packages were independent of location on the test vehicle. For example, TV3D_C1 was populated with two 17mm PBGA packages with Sn-36Pb-2Ag solder balls. The differences between their cycles to failure were calculated (See Table 28)

17mm PBGA (OSP Surface Finish)		
Brd Num	**Reference Location**	**Cycles to Failure**
1	U10	2601
2	U10	2588.5
3	U10	2483
4	U10	2314
5	U10	1716.5
6	U10	3193.5
7	U10	2235
1	U9	2739
2	U9	2342
3	U9	2585
4	U9	1918
5	U9	1967.5
6	U9	3050.5
7	U9	2312

Brd Num	D (U10 - U9)
1	-138
2	246.5
3	-102
4	396
5	-251
6	143
7	-77

D = 2,235 - 2,312

Table 28: Cycle to Failure Differences

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The paired t-Test assumes that the differences were normality distributed [55]. This assumption was tested with the Anderson Darling normality test. In the Anderson Darling normality test, high p-values (greater than 0.05), indicated that the differences (D) could be assumed normally distributed. Since the sample sizes were small, the normality assumption was weak. Thus, the Wilcoxon signed ranks test was also applied because it assumed no underlying distribution for the differences [56].

The paired t-test was a much more powerful test than the Wilcoxon signed ranks test. The paired t-test accounted for the magnitude/spread of differences, while the Wilcoxon signed ranked test did not. The Wilcoxon signed ranked test only evaluated whether the differences were positive or negative. Used together, both statistical tests provided great insight into determining if board location altered the cycles to failure for two identical electronic packages. For both tests, a high p-value (> 0.05) indicated that the cycles to failure were not dependent on board location.

APPENDIX F: TV3D Configuration 1 Electronic Package Independence

P-value: Anderson Darling Normality Test			
Electronic Package	**HASL**	**ImSn**	**OSP**
17mm PBGA	0.408	0.425	0.479
17mm PBGA (Pb-Free)	n/a		
27mm PBGA	0.067	0.875	0.378
27mm PBGA (Pb-Free)	0.800	0.093	0.477
Resistor Banks	0.532	0.248	0.497
QFN	n/a		

P-value: Paired t-Test			
Electronic Package	**HASL**	**ImSn**	**OSP**
17mm PBGA	0.992	0.731	0.734
17mm PBGA (Pb-Free)	n/a		
27mm PBGA	0.634	0.423	0.284
27mm PBGA (Pb-Free)	0.887	0.290	0.127
Resistor Banks	0.939	0.377	0.141
QFN	n/a		

P-value: Wilcoxon Signed Rank Test			
Electronic Package	**HASL**	**ImSn**	**OSP**
17mm PBGA	0.933	0.933	0.800
17mm PBGA (Pb-Free)	n/a		
27mm PBGA	0.353	0.554	0.272
27mm PBGA (Pb-Free)	0.998	0.529	0.151
Resistor Banks	0.800	0.447	0.151
QFN	n/a		

APPENDIX G: TV3D Configuration 1 Hypothesis Testing

Null Hypothesis for η on Surface Finishes			
	P-Values		
Electronic Package	$\eta_{HASL} = \eta_{ImSn}$	$\eta_{HASL} = \eta_{OSP}$	$\eta_{ImSn} = \eta_{OSP}$
2512 Resistors	0.385	0.010	< .001
27mm PBGA	0.004	< .001	0.599
27mm PBGA (Pb-Free)	0.725	0.049	0.138
17mm PBGA	0.006	0.015	0.655
17mm PBGA (Pb-Free)	n/a	n/a	n/a
QFN	n/a	n/a	n/a

Null Hypothesis for β on Surface Finishes			
	P-Values		
Electronic Package	$\beta_{HASL} = \beta_{ImSn}$	$\beta_{HASL} = \beta_{OSP}$	$\beta_{ImSn} = \beta_{OSP}$
2512 Resistors	0.273	0.232	0.975
27mm PBGA	0.309	0.596	0.741
27mm PBGA (Pb-Free)	0.924	0.318	0.292
17mm PBGA	0.970	0.774	0.775
17mm PBGA (Pb-Free)	n/a	n/a	n/a
QFN	n/a	n/a	n/a

Null Hypothesis for SnPbAg PBGA Body Sizes		
	P-values	
Surface Finish	$\eta_{17mm} = \eta_{27mm}$	$\beta_{17mm} = \beta_{27mm}$
HASL	< .001	0.010
ImSn	< .001	0.107
OSP	< .001	0.068

Null Hypothesis for 27mm PBGA Solder Balls		
	P-values	
Surface Finish	$\eta_{PbFree} = \eta_{SnPbAg}$	$\beta_{PbFree} = \beta_{SnPbAg}$
HASL	< .001	0.497
ImSn	< .001	0.964
OSP	< .001	0.373

APPENDIX H: Solder Joint Element Percentage Calculations

The solder joint of the PBGA package was broken into two sections, namely the solder ball and the solder paste printed onto the circular pad. The volume of each section was calculated. First, the volume of the solder ball was calculated by using the volume equation for a sphere [57]:

$$V_{Sphere} = \frac{4}{3} * \pi * r^3$$

Since the radius of the solder ball was 0.3mm, the volume of the solder ball was estimated to be:

$$V_{Solder\ Ball} = 0.1131$$

Next, the volume of the solder paste printed on the board's circular pad was calculated using the volume equation for a circular cylinder [57]:

$$V_{Sphere} = \pi * r^2 * h$$

Assuming there was a 1:1 match between the hole in the stencil and the circular pad, the radius was 0.2mm. The height (i.e. thickness of the stencil) was 0.15mm. The calculation for the volume of the solder paste printed was:

$$V_{Solder\ Paste} = 0.0189$$

Thus, the percentage of volume for each section was approximately:

Percent Volume (Solder Ball) $\approx$ 86%

Percent Volume (Solder Paste) $\approx$ 14%

With the percent weight between the solder ball and the solder paste, the proportion of each element in the solder joint was calculated. The solder ball was 95.5%Sn – 3.8%Ag – 0.7%Cu and the paste was 63%Sn-37%Pb. The calculations were as follows:

Percentage Sn: (0.86*0.955) + (0.14*0.63) ≈ 90.95%

Percentage Ag: (0.86*0.038) ≈ 3.27%

Percentage Cu: (0.86*0.007) ≈ 0.60%

Percentage Pb: (0.14*0.37) ≈ 5.18%

APPENDIX I: TV3D Configuration 2 Electronic Package Independence

17mm PBGA

Anderson Darling Normality Test	
17mm PBGA	**P-value**
LF-LF-LF	0.388
LF-L-LF	0.561
LF-L-L	0.559
L-L-L	0.006
L-L-LF	0.628

Paired t-Test	
17mm PBGA	**P-value**
LF-LF-LF	0.366
LF-L-LF	0.783
LF-L-L	0.778
L-L-L	0.119
L-L-LF	0.341

Wilcoxon Signed Rank Test	
17mm PBGA	**P-value**
LF-LF-LF	0.295
LF-L-LF	0.999
LF-L-L	0.933
L-L-L	0.208
L-L-LF	0.418

2512 Resistor Bank

Anderson Darling Normality Test	
2512 Resistor Banks	**P-value**
Pb-Free Paste / PbFree Profile	0.023
SnPb Paste / SnPb Profile	0.294
SnPb Paste / PbFree Profile	0.465

Paired t-Test	
2512 Resistor Banks	**P-value**
Pb-Free Paste / PbFree Profile	0.452
SnPb Paste / SnPb Profile	0.263
SnPb Paste / PbFree Profile	0.393

Wilcoxon Signed Rank Test	
2512 Resistor Banks	**P-value**
Pb-Free Paste / PbFree Profile	0.800
SnPb Paste / SnPb Profile	0.184
SnPb Paste / PbFree Profile	0.675

APPENDIX J: TV3D Configuration 2 Hypothesis Testing

Hypothesis Test on η For 2512 Resistors

Null Hypothesis:	P-Value
$\eta_{\text{PbFree Paste / PbFree Profile}} = \eta_{\text{SnPb Paste / SnPb Profile}}$	< .001
$\eta_{\text{PbFree Paste / PbFree Profile}} = \eta_{\text{SnPb Paste / PbFree Profile}}$	< .001
$\eta_{\text{SnPb Paste / SnPb Profile}} = \eta_{\text{SnPb Paste / PbFree Profile}}$	0.464

Hypothesis Test on β For 2512 Resistors

Null Hypothesis:	P-Value
$\beta_{\text{PbFree Paste / PbFree Profile}} = \beta_{\text{SnPb Paste / SnPb Profile}}$	0.149
$\beta_{\text{PbFree Paste / PbFree Profile}} = \beta_{\text{SnPb Paste / PbFree Profile}}$	0.233
$\beta_{\text{SnPb Paste / SnPb Profile}} = \beta_{\text{SnPb Paste / PbFree Profile}}$	0.642

Hypothesis Test on η For 17mm PBGAs

Null Hypothesis:	P-Value
$\eta_{\text{LF-L-LF}} = \eta_{\text{LF-L-L}}$	0.046
$\eta_{\text{L-L-L}} = \eta_{\text{LF-LF-LF}}$	0.654
$\eta_{\text{L-L-L}} = \eta_{\text{LF-L-LF}}$	0.310
$\eta_{\text{LF-LF-LF}} = \eta_{\text{LF-L-LF}}$	0.720
$\eta_{\text{L-L-L}} = \eta_{\text{L-L-LF}}$	0.087

Hypothesis Test on β For 17mm PBGAs

Null Hypothesis:	P-Value
$\beta_{\text{LF-L-LF}} = \beta_{\text{LF-L-L}}$	0.021
$\beta_{\text{L-L-L}} = \beta_{\text{LF-LF-LF}}$	0.388
$\beta_{\text{L-L-L}} = \beta_{\text{LF-L-LF}}$	0.803
$\beta_{\text{LF-LF-LF}} = \beta_{\text{LF-L-LF}}$	0.224
$\beta_{\text{L-L-L}} = \beta_{\text{L-L-LF}}$	0.036

APPENDIX K: TV3D Configuration 1 Representative SEM Pictures

SJ ➔ Solder Joint
Bkw ➔ “Backwards”

HASL Surface Finish Pictures

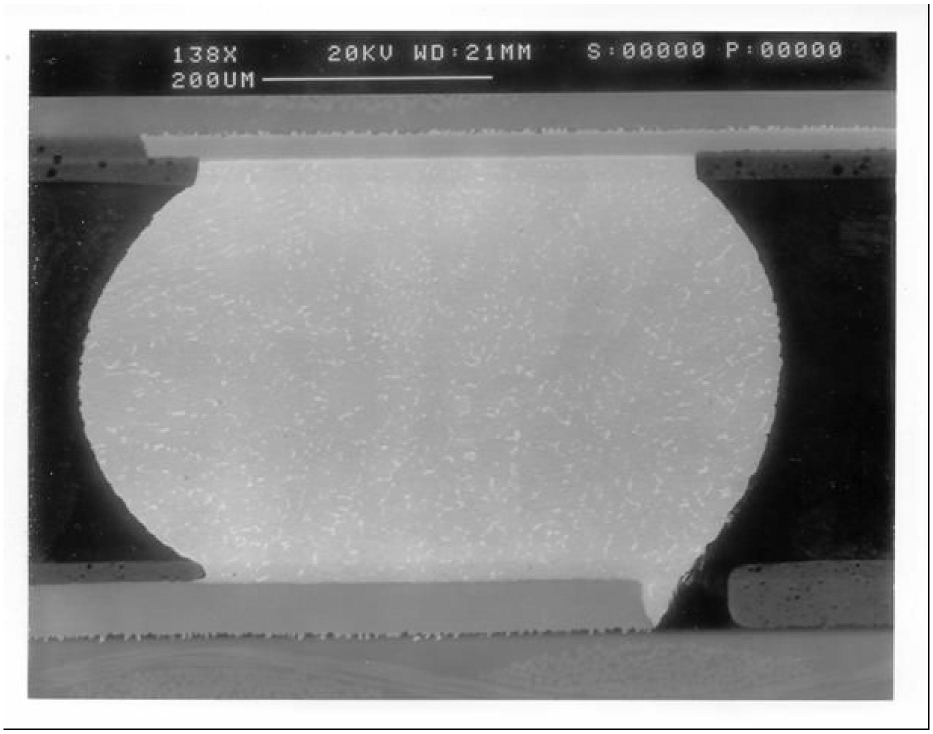

Figure K1: 27mm PBGA “Bkw” SJ – 0 Cycles (HASL)

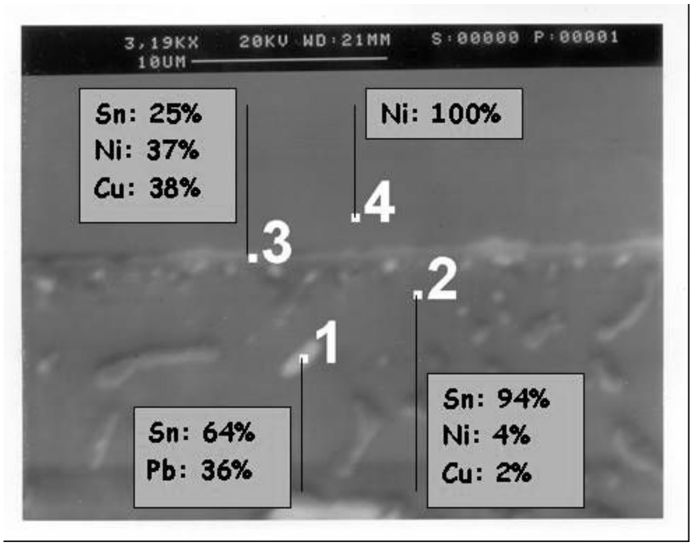

Figure K2: 27mm PBGA “Bkw” SJ Component Interface – 0 Cycles (HASL)

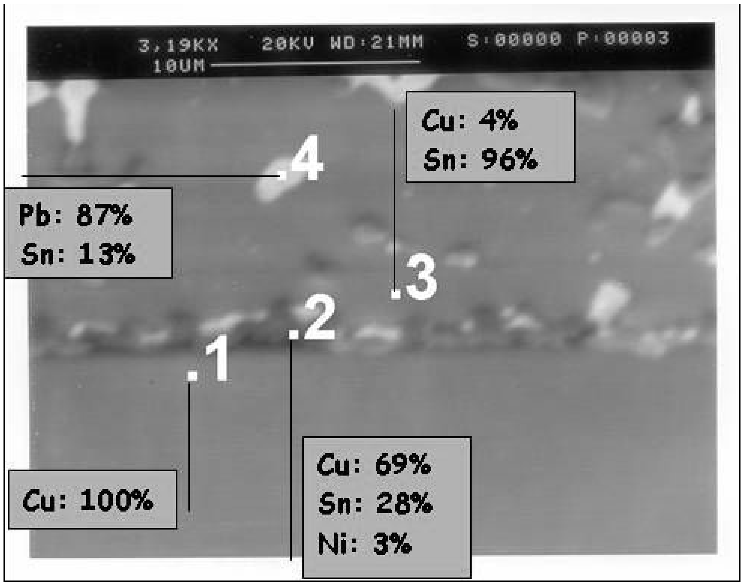

Figure K3: 27mm PBGA “Bkw” SJ PCB Interface – 0 Cycles (HASL)

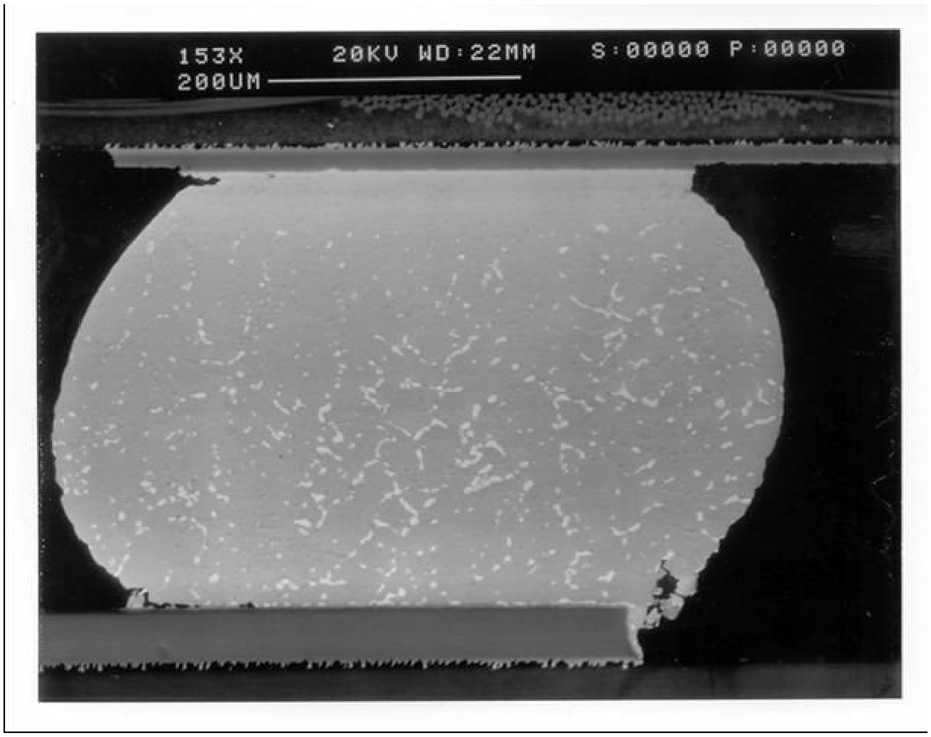

Figure K4: 27mm PBGA “Bkw” SJ – 3,142 Cycles (HASL)

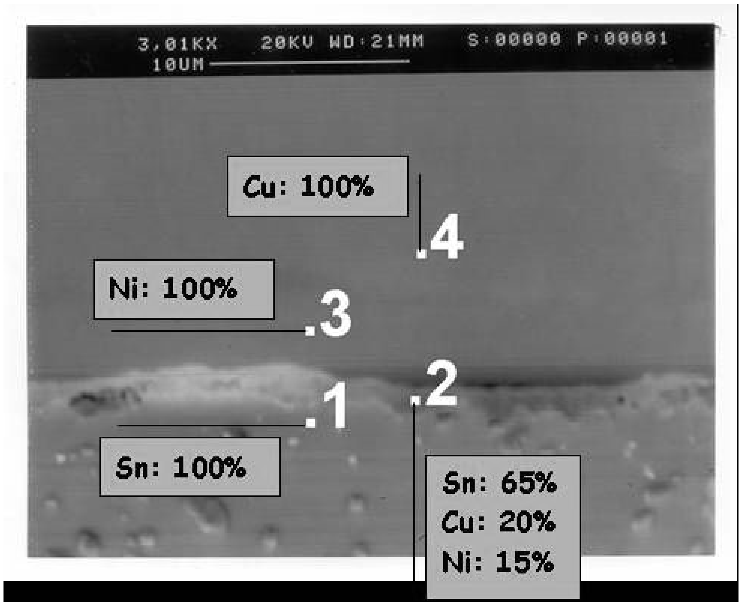

Figure K5: 27mm PBGA “Bkw” SJ Component Interface – 3,142 Cycles (HASL)

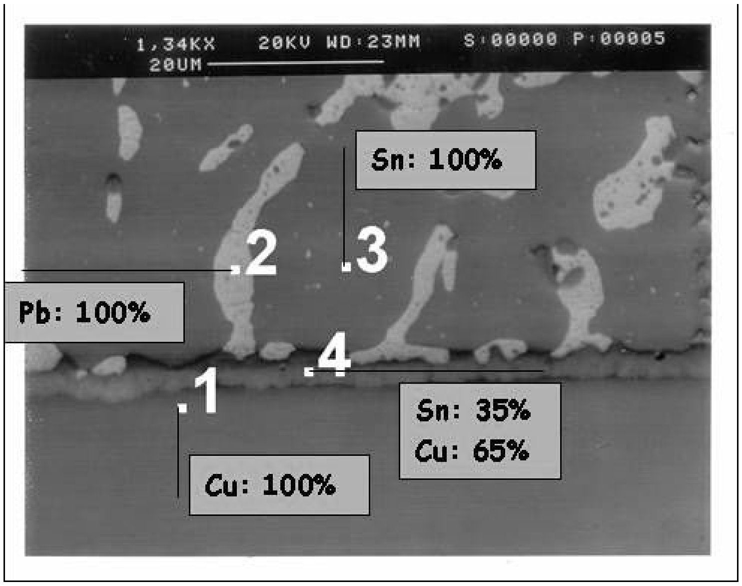

Figure K6: 27mm PBGA “Bkw” SJ PCB Interface – 3,142 Cycles (HASL)

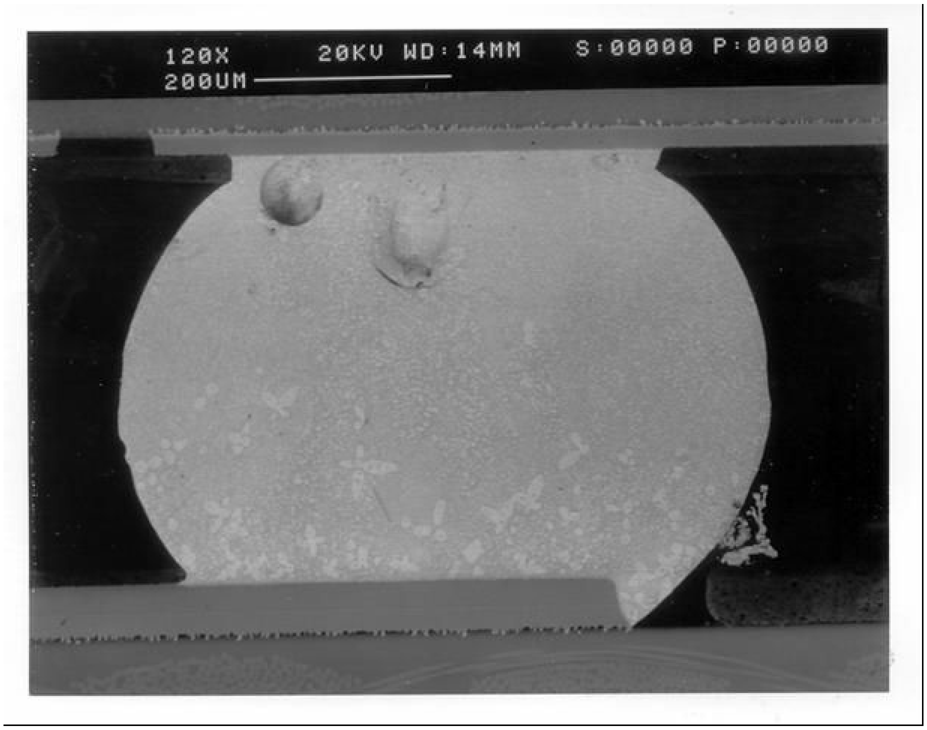

Figure K7: 17mm PBGA SnPb SJ – 0 Cycles (HASL)

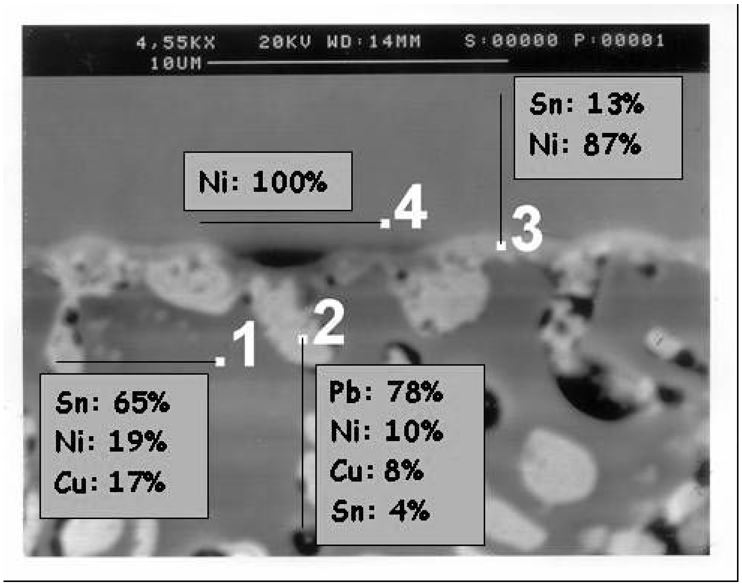

Figure K8: 17mm PBGA SnPb SJ Component Interface – 0 Cycles (HASL)

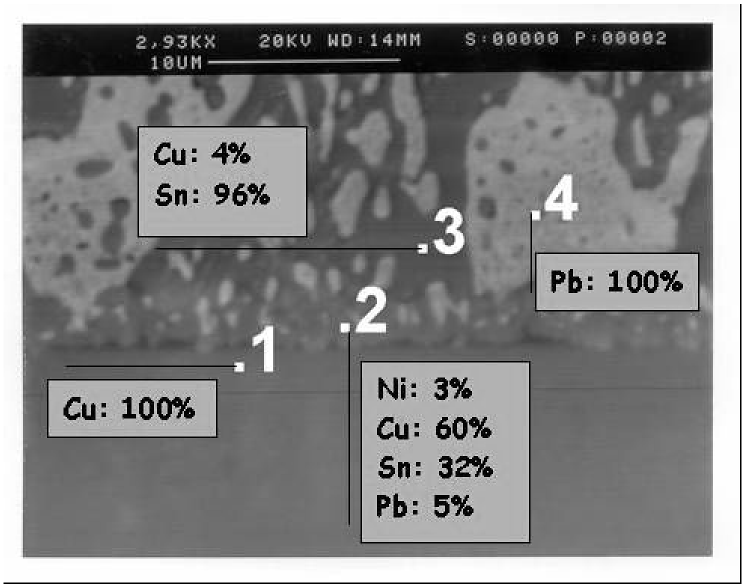

Figure K9: 17mm PBGA SnPb SJ PCB Interface – 0 Cycles (HASL)

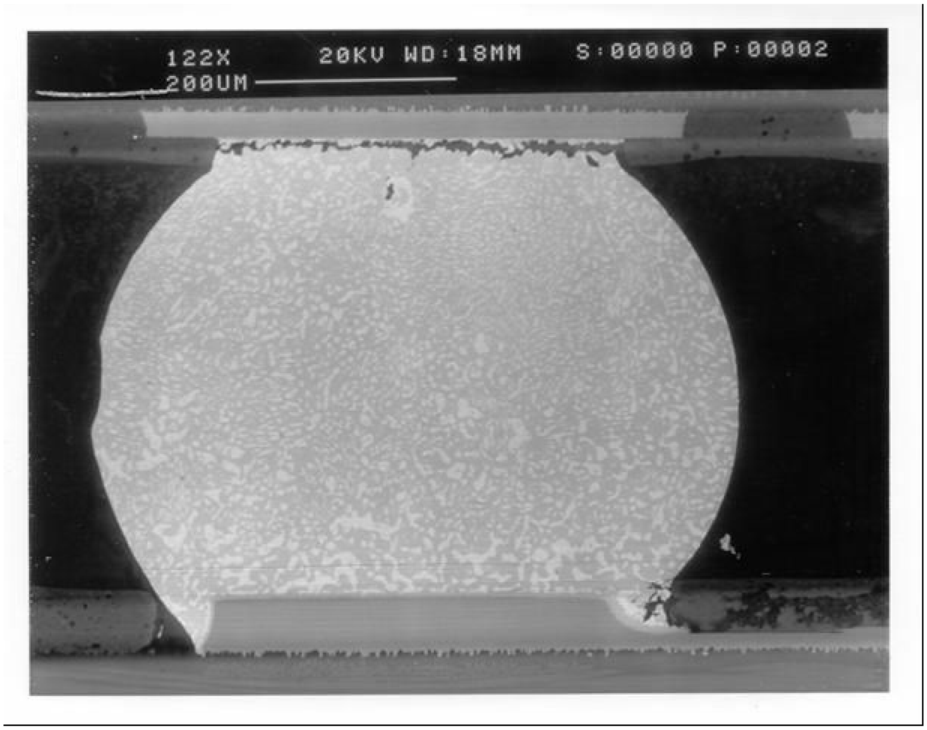

Figure K10: 17mm PBGA SnPb SJ – 3,142 Cycles (HASL)

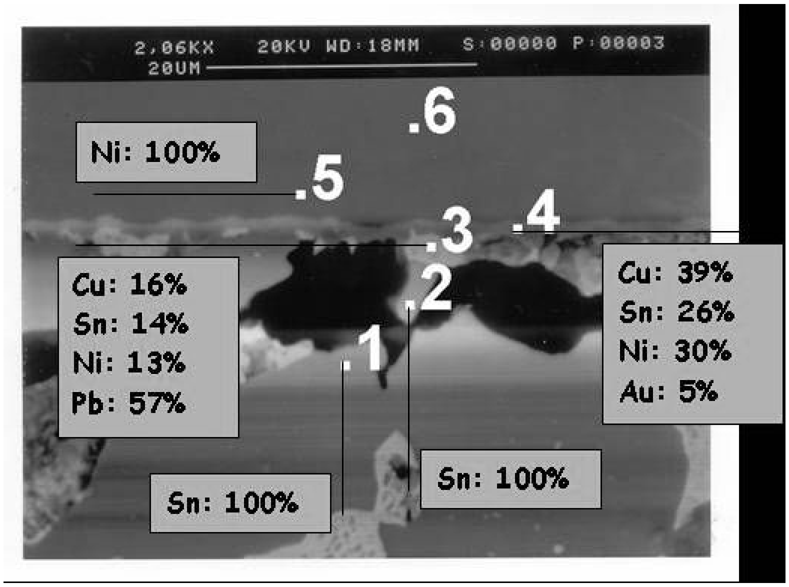

Figure K11: 17mm PBGA SnPb SJ Component Interface – 3,142 Cycles (HASL)

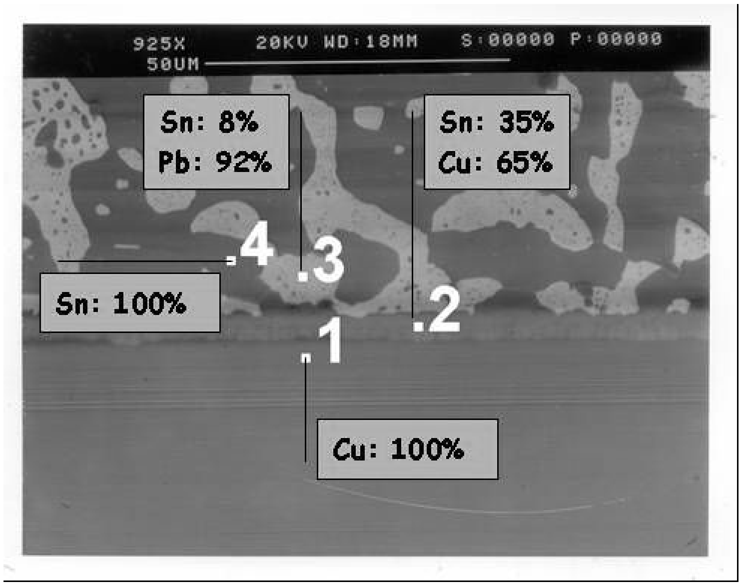

Figure K12: 17mm PBGA SnPb SJ PCB Interface – 3,142 Cycles (HASL)

ImSn Surface Finish Pictures

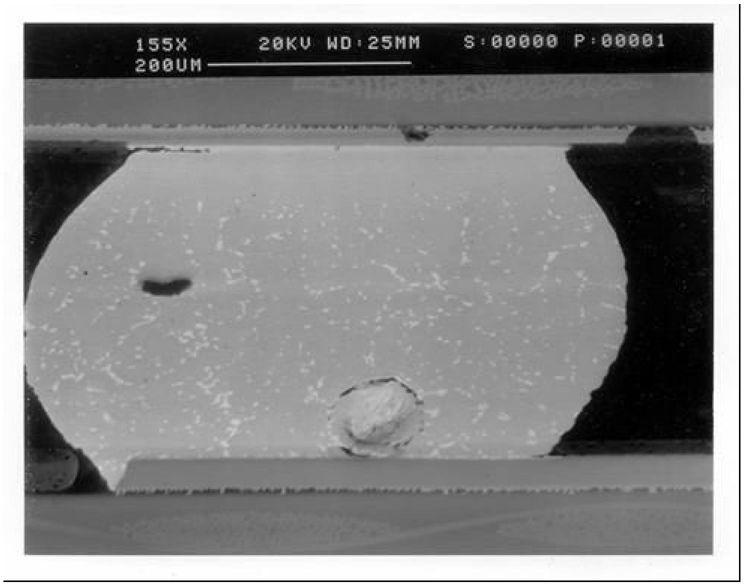

Figure K13: 27mm PBGA "Bkw" SJ – 3,142 Cycles (ImSn)

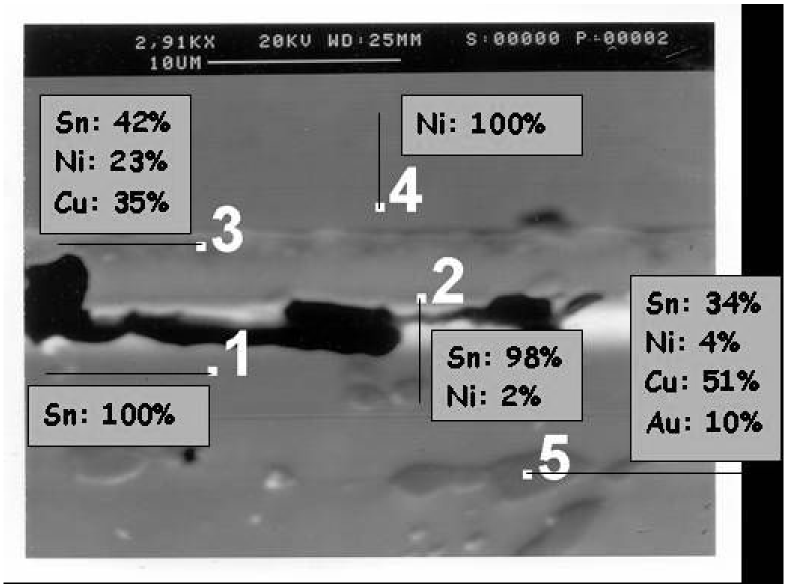

Figure K14: 27mm PBGA "Bkw" SJ Component Interface – 3,142 Cycles (ImSn)

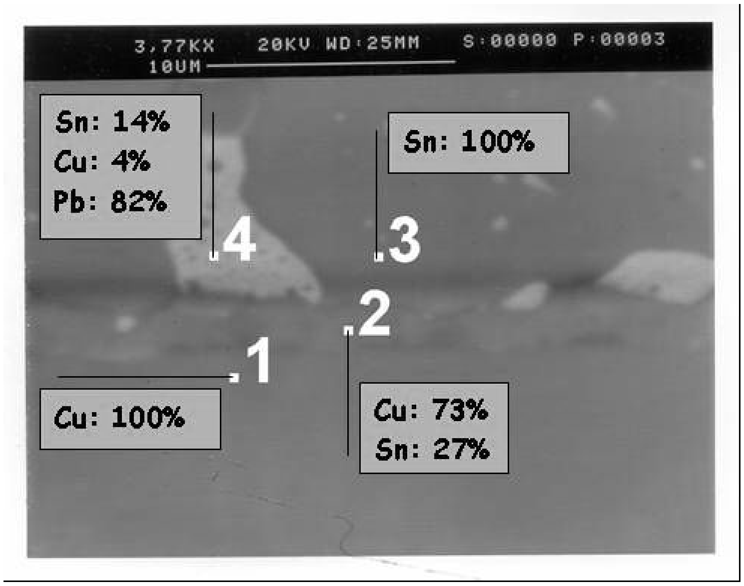

Figure K15: 27mm PBGA “Bkw” SJ PCB Interface – 3,142 Cycles (ImSn)

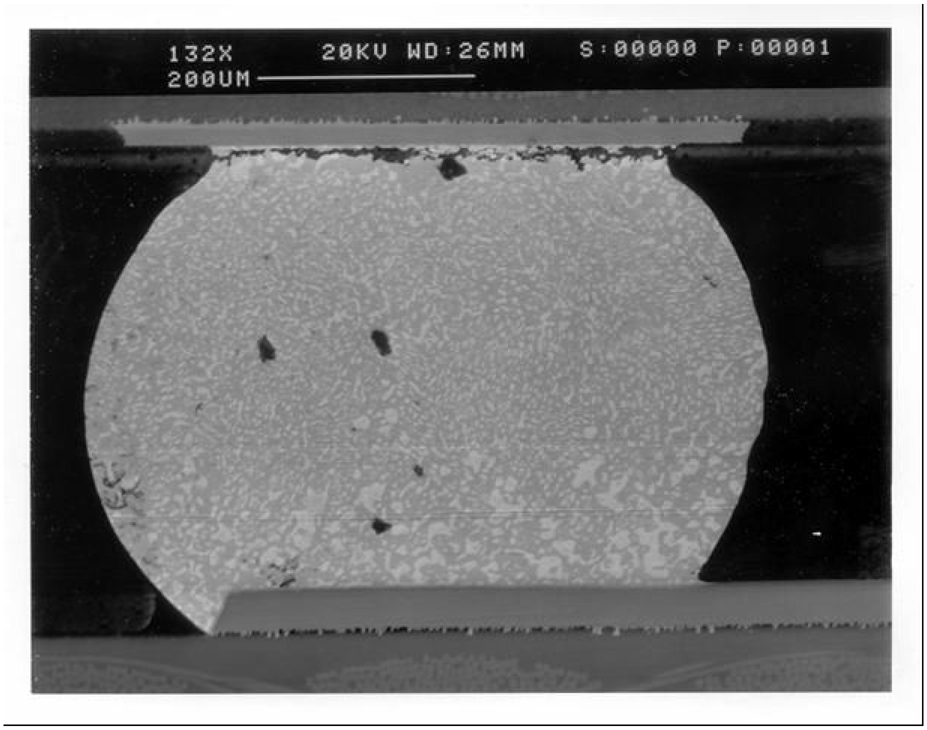

Figure K16: 17mm PBGA SnPb SJ – 3,142 Cycles (ImSn)

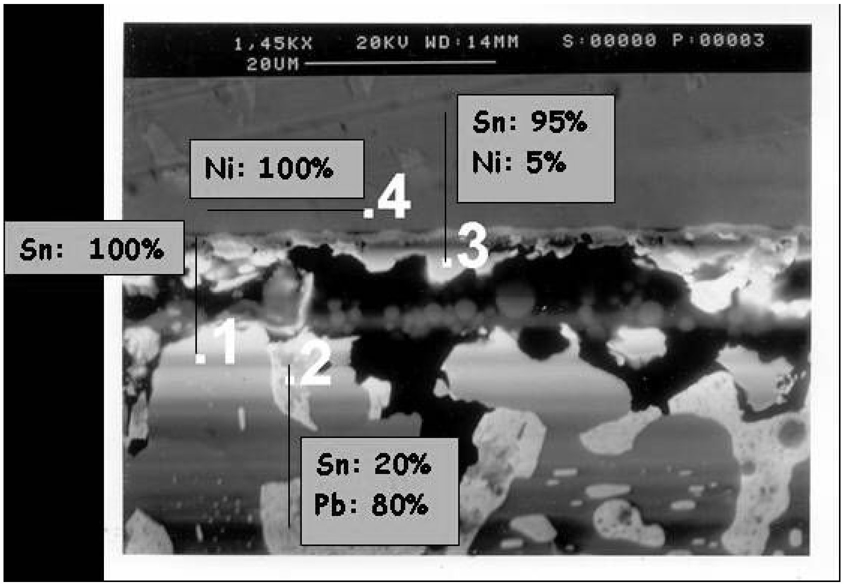

Figure K17: 17mm PBGA SnPb SJ Component Interface – 3,142 Cycles (ImSn)

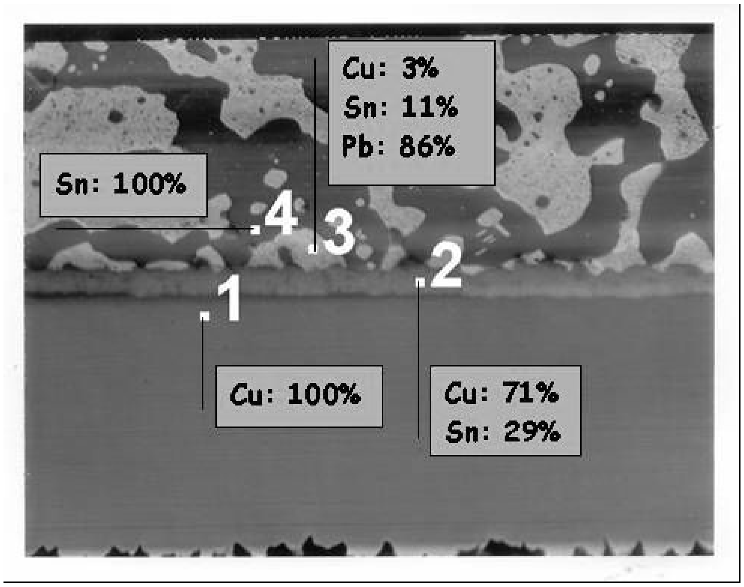

Figure K18: 17mm PBGA SnPb SJ PCB Interface – 3,142 Cycles (ImSn)

OSP Surface Finish Pictures

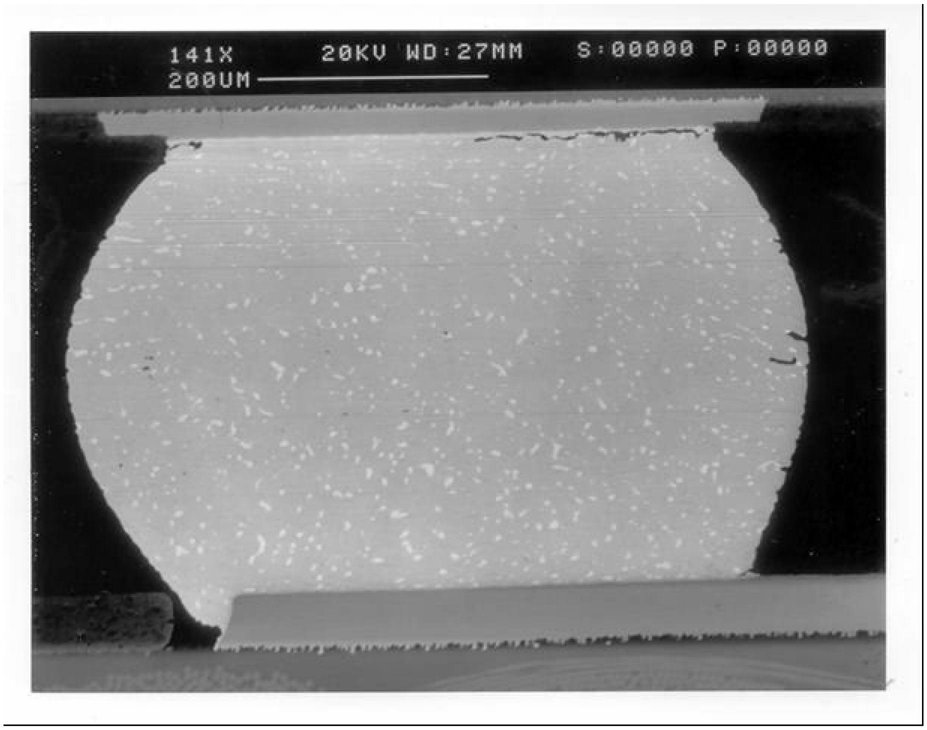

Figure K19: 27mm PBGA “Bkw” SJ – 3,142 Cycles (OSP)

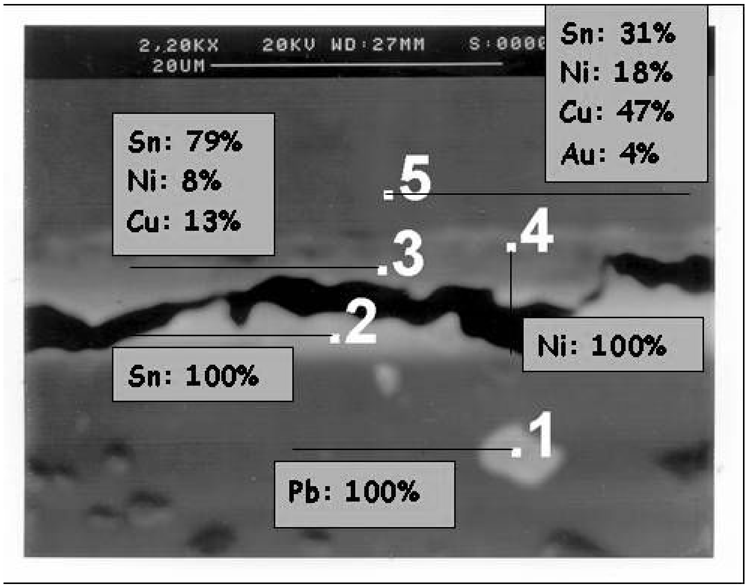

Figure K20: 27mm PBGA “Bkw” SJ Component Interface – 3,142 Cycles (OSP)

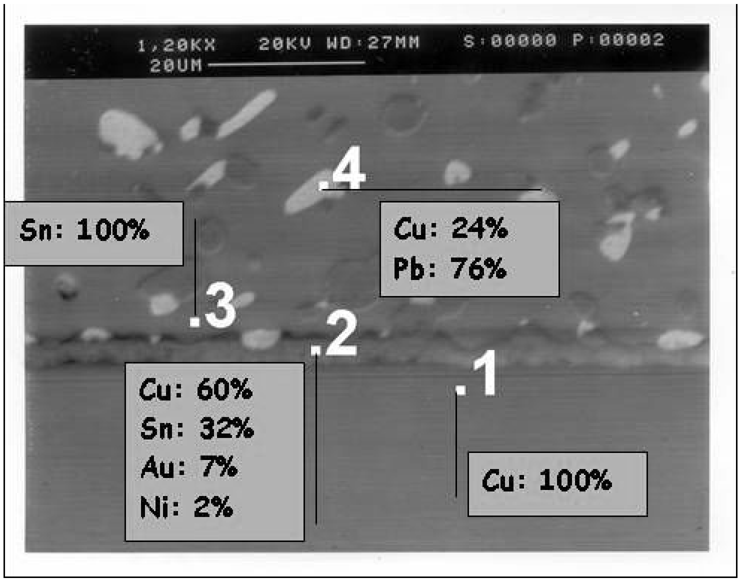

Figure K21: 27mm PBGA "Bkw" SJ PCB Interface – 3,142 Cycles (OSP)

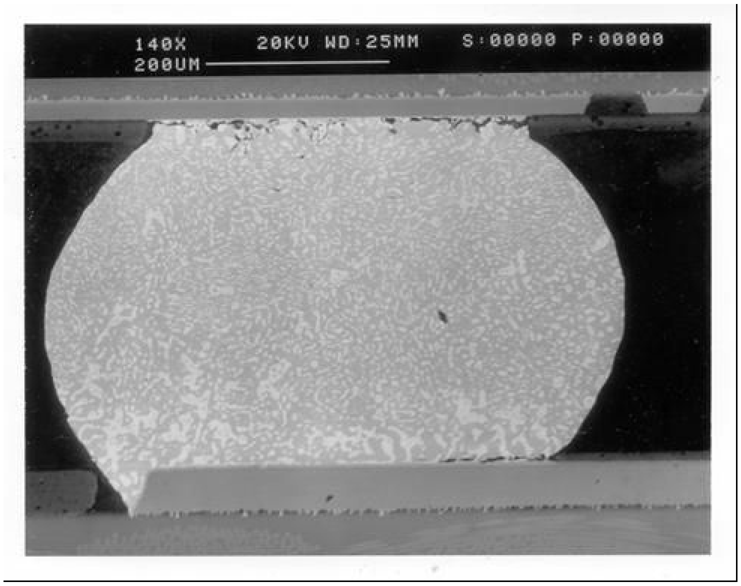

Figure K22: 17mm PBGASnPb SJ – 3,142 Cycles (OSP)

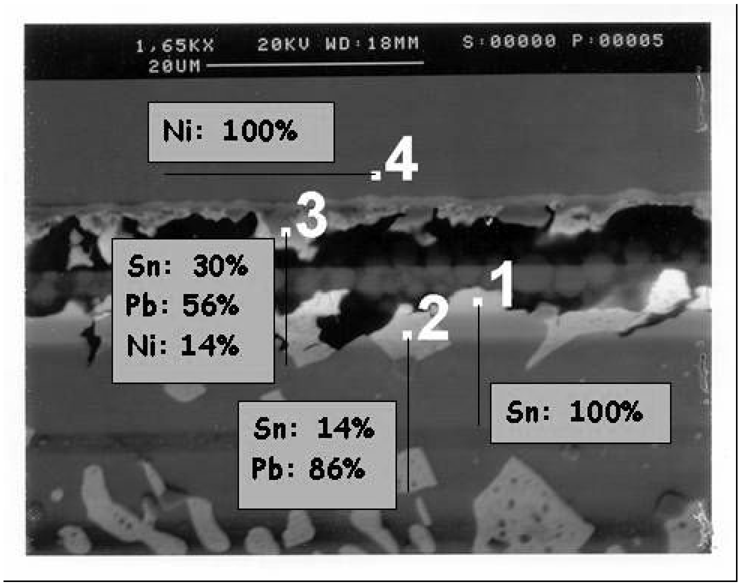

Figure K23: 17mm PBGA SnPb SJ Component Interface – 3,142 Cycles (OSP)

APPENDIX L: TV3D Configuration 2 Representative SEM Pictures

LF-LF-LF Pictures:

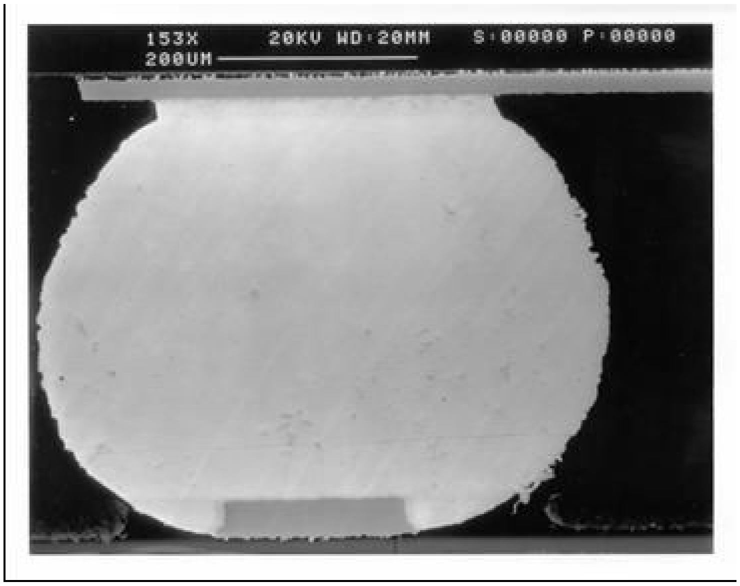

Figure L54: LF-LF-LF 0 Cycles

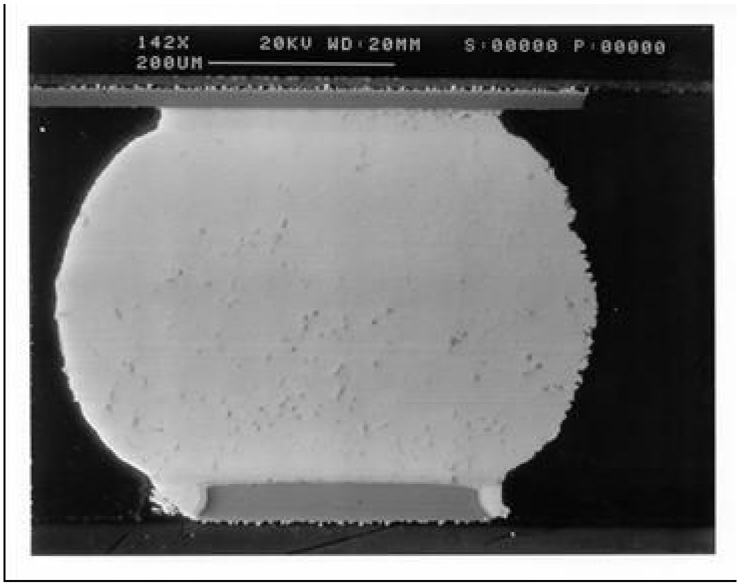

Figure L2: LF-LF-LF 1,000 Cycles

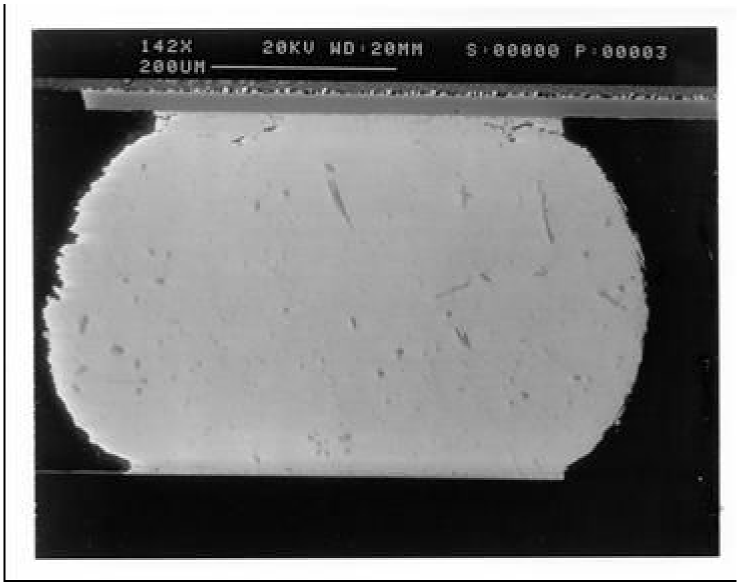

Figure L3: LF-LF-LF 2,000 Cycles

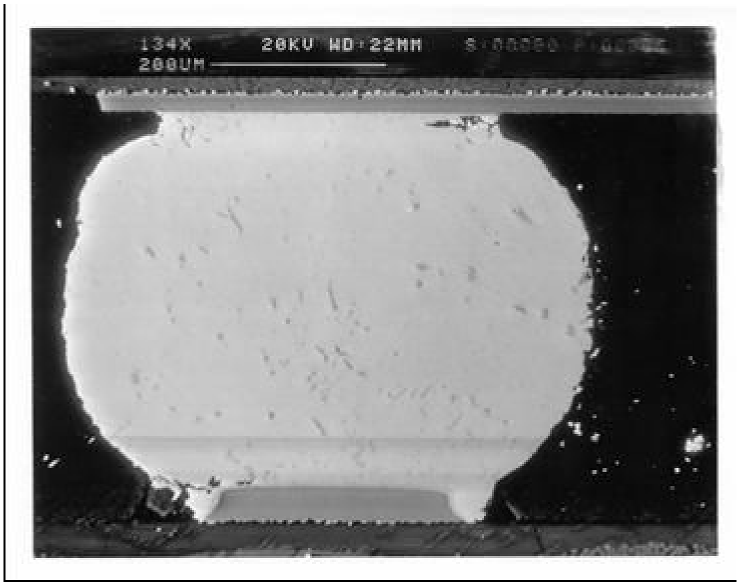

Figure L4: LF-LF-LF 3,000 Cycles

LF-L-LF Pictures:

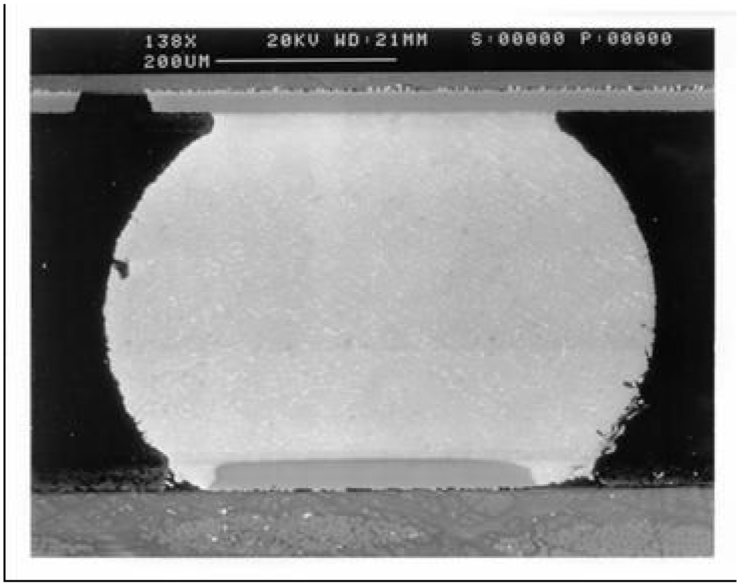

Figure L5: LF-L-LF 0 Cycles

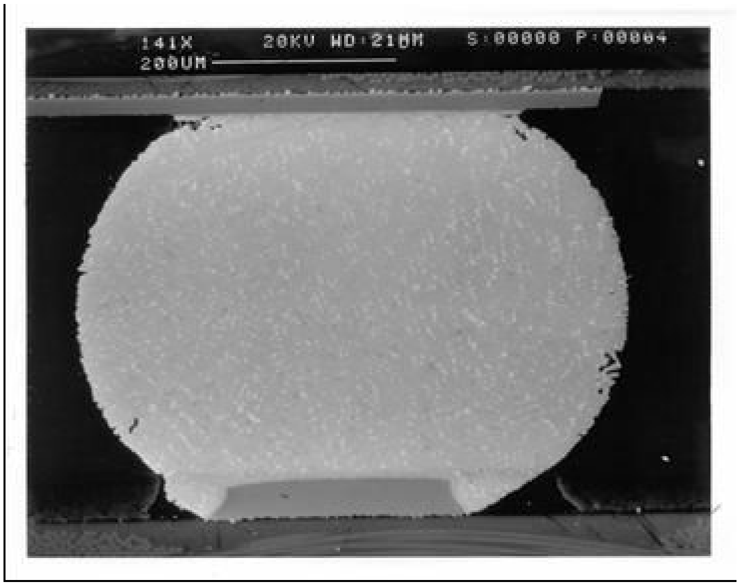

Figure L6: LF-L-LF 1,000 Cycles

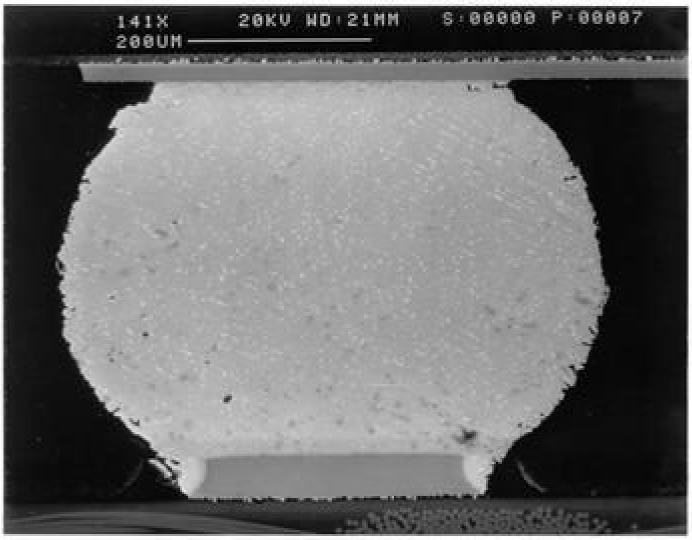

Figure L7: LF-L-LF 2,000 Cycles

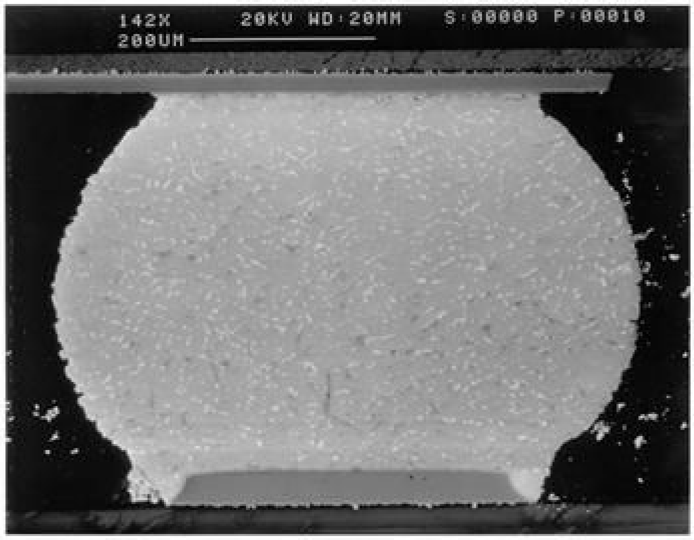

Figure L8: LF-L-LF 3,000 Cycles

LF-L-L Pictures:

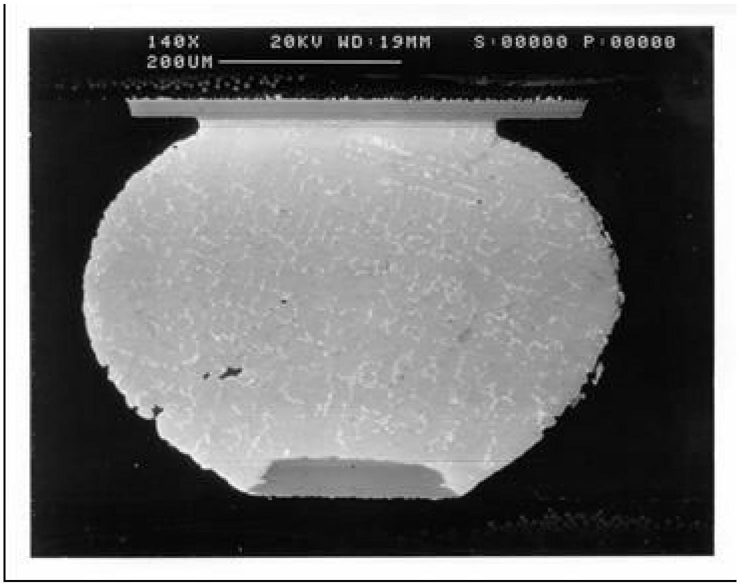

Figure L9: LF-L-L 0 Cycles

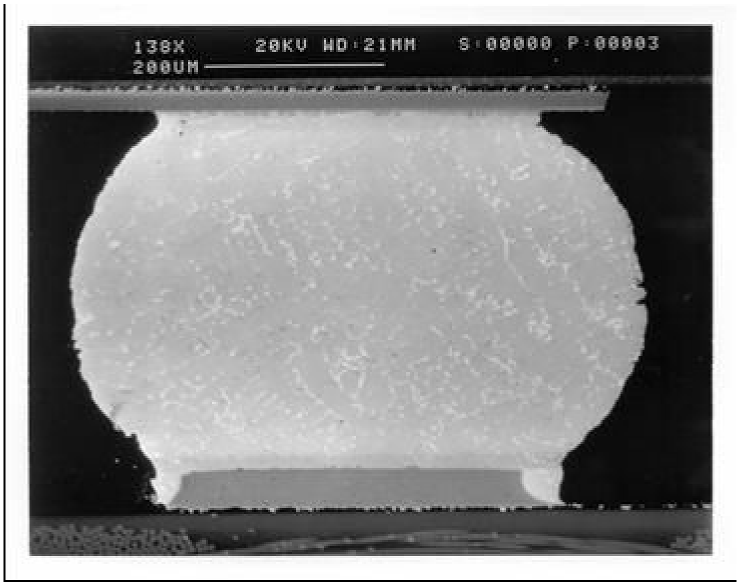

Figure L10: LF-L-L 1,000 Cycles

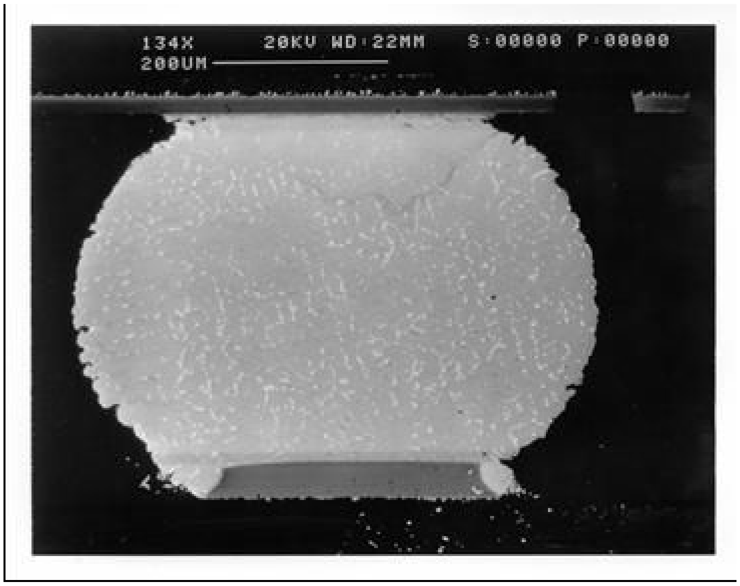

Figure L11: LF-L-L 2,000 Cycles

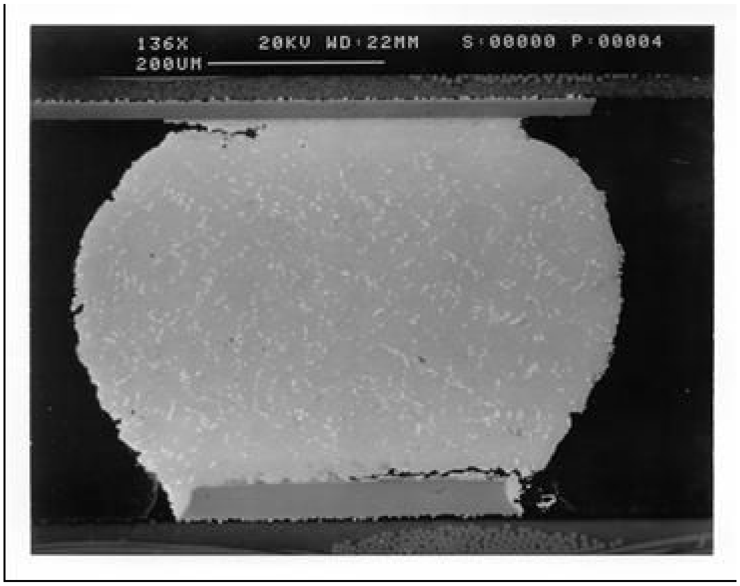

Figure L12: LF-L-L 3,000 Cycles

L-L-L Pictures:

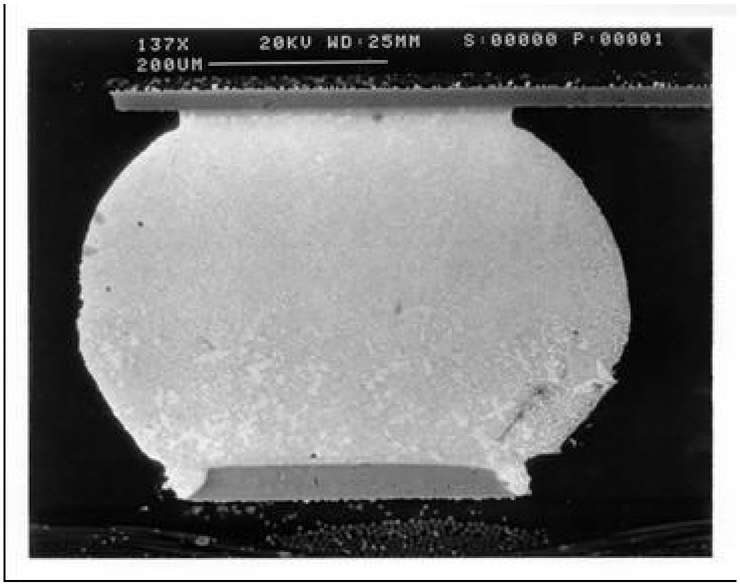

Figure L13: L-L-L 0 Cycles

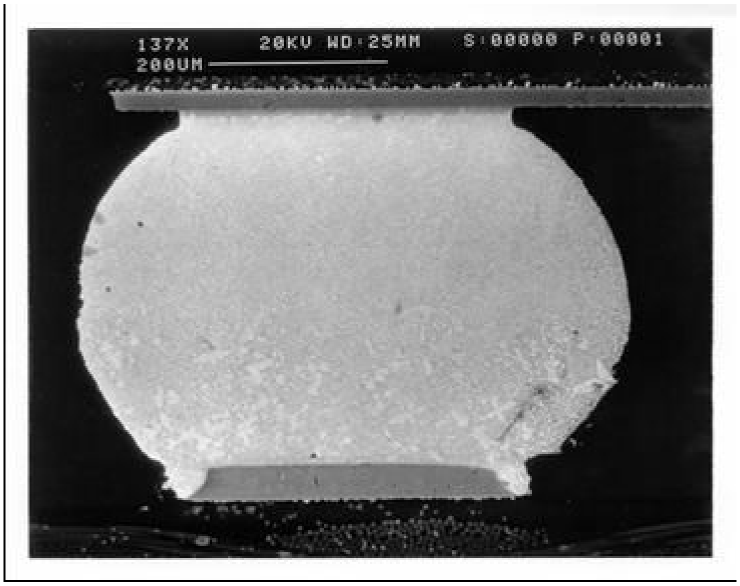

Figure L14: L-L-L 1,000 Cycles

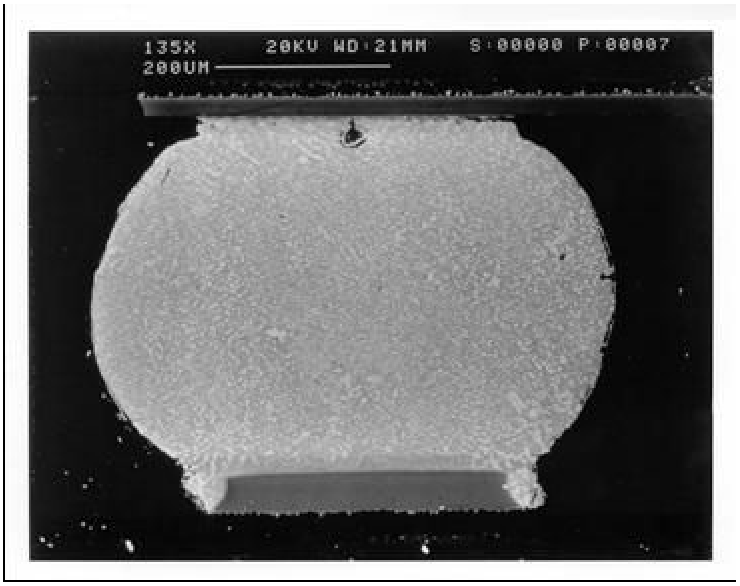

Figure L15: L-L-L 2,000 Cycles

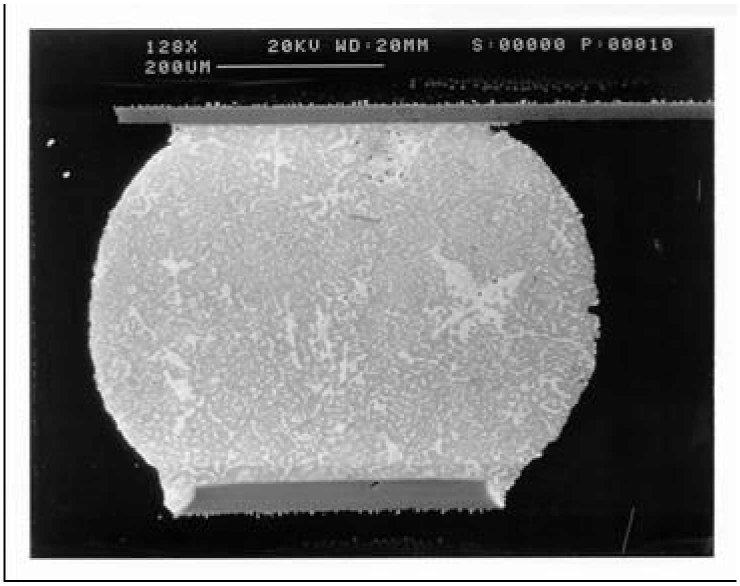

Figure L16: L-L-L 3,000 Cycles

L-L-LF Pictures:

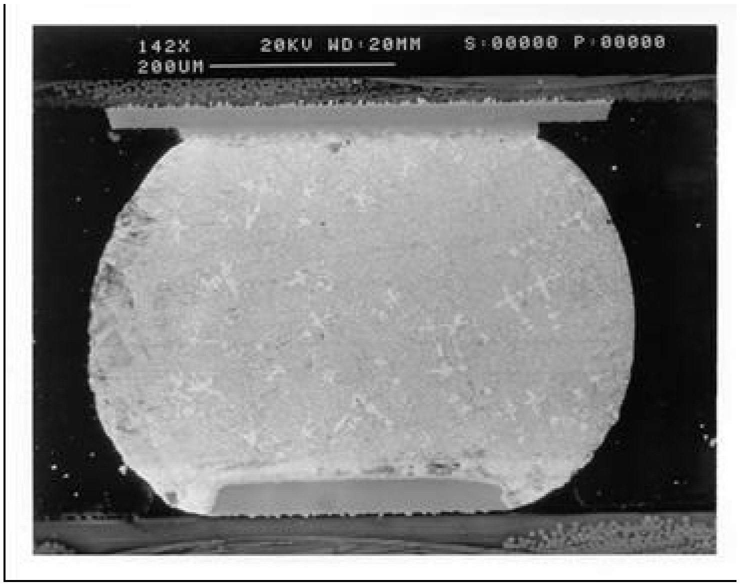

Figure L17: L-L-LF 0 Cycles

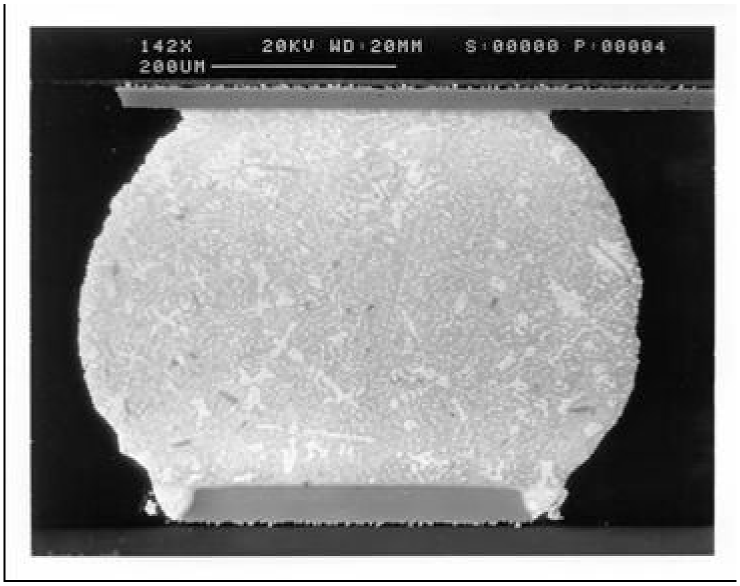

Figure L18: L-L-LF 1,000 Cycles

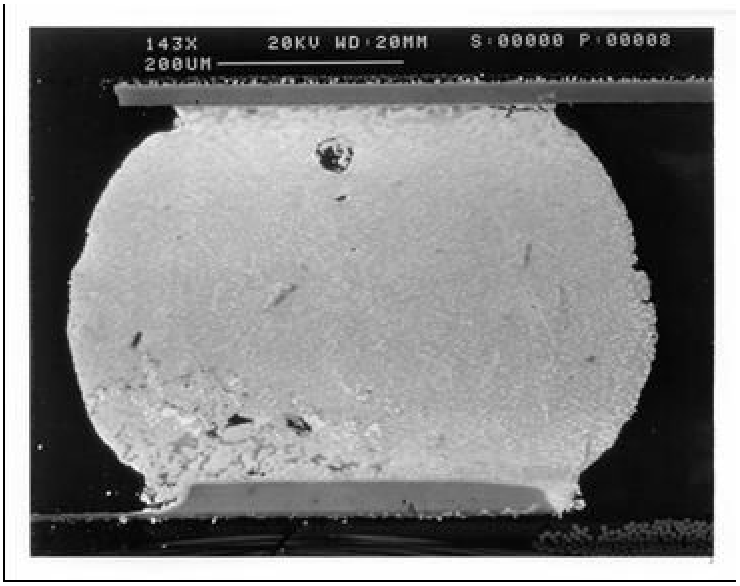

Figure L19: L-L-LF 2,000 Cycles

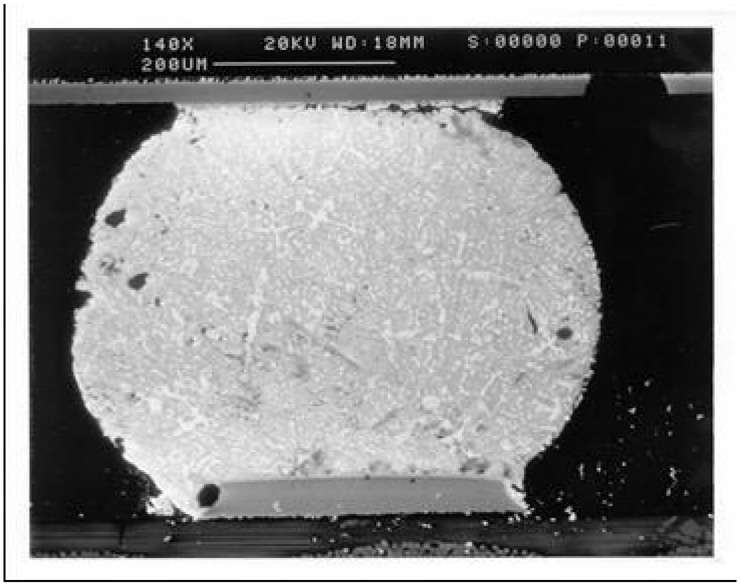

Figure L20: L-L-LF 3,000 Cycles

APPENDIX M: TV3D Configuration 1 Data

Surface Finish	Brd #	Electronic Package	Brd Locational Reference	F/C	Cycle # Failure
HASL	1	17mm PBGA - Perimeter Array	U9	F	1414.5
HASL	1	17mm PBGA - Perimeter Array	U10	F	1909.5
HASL	1	17mm PBGA (Pb-Free) - Perimeter Array	U11	C	3142
HASL	1	27mm PBGA - Perimeter Array	U2o	F	1364.5
HASL	1	27mm PBGA - Perimeter Array	U1o	F	1393
HASL	1	27mm PBGA - Thermal Array	U1i	F	1409
HASL	1	27mm PBGA - Thermal Array	U2i	F	1787.5
HASL	1	27mm PBGA (Pb-Free) - Perimeter Array	U3o	C	3142
HASL	1	27mm PBGA (Pb-Free) - Perimeter Array	U6o	C	3142
HASL	1	27mm PBGA (Pb-Free) - Thermal Array	U6i	C	3142
HASL	1	QFN	U4	C	3142
HASL	1	QFN	U5	C	3142
HASL	1	QFN	U7	C	3142
HASL	1	Resistor Bank	R1-5	F	979
HASL	1	Resistor Bank	R6-10	F	1665.5
HASL	2	17mm PBGA - Perimeter Array	U10	F	1977
HASL	2	17mm PBGA - Perimeter Array	U9	F	2061
HASL	2	17mm PBGA (Pb-Free) - Perimeter Array	U11	F	4619
HASL	2	27mm PBGA - Perimeter Array	U1o	F	1504.5
HASL	2	27mm PBGA - Perimeter Array	U2o	F	1550.5
HASL	2	27mm PBGA - Thermal Array	U1i	F	1723.5
HASL	2	27mm PBGA - Thermal Array	U2i	F	1873
HASL	2	27mm PBGA (Pb-Free) - Perimeter Array	U3o	F	3813
HASL	2	27mm PBGA (Pb-Free) - Perimeter Array	U6o	F	3825.5
HASL	2	27mm PBGA (Pb-Free) - Thermal Array	U6i	C	4816
HASL	2	QFN	U5	F	3881
HASL	2	QFN	U4	C	4816
HASL	2	QFN	U7	C	4816
HASL	2	Resistor Bank	R6-10	F	1102.5
HASL	2	Resistor Bank	R1-5	F	1175
HASL	3	17mm PBGA - Perimeter Array	U10	F	1510
HASL	3	17mm PBGA - Perimeter Array	U9	F	2139
HASL	3	17mm PBGA (Pb-Free) - Perimeter Array	U11	C	4816
HASL	3	27mm PBGA - Perimeter Array	U1o	F	1490
HASL	3	27mm PBGA - Perimeter Array	U2o	F	1596.5
HASL	3	27mm PBGA - Thermal Array	U2i	F	1782
HASL	3	27mm PBGA - Thermal Array	U1i	F	1880
HASL	3	27mm PBGA (Pb-Free) - Perimeter Array	U3o	F	3369.5
HASL	3	27mm PBGA (Pb-Free) - Perimeter Array	U6o	F	4286.5
HASL	3	27mm PBGA (Pb-Free) - Thermal Array	U6i	C	4816
HASL	3	QFN	U4	C	4816
HASL	3	QFN	U5	C	4816
HASL	3	QFN	U7	C	4816
HASL	3	Resistor Bank	R6-10	F	1142
HASL	3	Resistor Bank	R1-5	F	1143.5

HASL	4	17mm PBGA - Perimeter Array	U10	F	2356
HASL	4	17mm PBGA - Perimeter Array	U9	F	2507.5
HASL	4	17mm PBGA (Pb-Free) - Perimeter Array	U11	C	4816
HASL	4	27mm PBGA - Perimeter Array	U1o	F	1368
HASL	4	27mm PBGA - Perimeter Array	U2o	F	1579.5
HASL	4	27mm PBGA - Thermal Array	U1i	F	1725
HASL	4	27mm PBGA - Thermal Array	U2i	F	1908
HASL	4	27mm PBGA (Pb-Free) - Perimeter Array	U3o	F	4038.5
HASL	4	27mm PBGA (Pb-Free) - Perimeter Array	U6o	F	4425.5
HASL	4	27mm PBGA (Pb-Free) - Thermal Array	U6i	C	4816
HASL	4	QFN	U4	C	4816
HASL	4	QFN	U5	C	4816
HASL	4	QFN	U7	C	4816
HASL	4	Resistor Bank	R6-10	F	863
HASL	4	Resistor Bank	R1-5	F	1610
HASL	5	17mm PBGA - Perimeter Array	U9	F	2108.5
HASL	5	17mm PBGA - Perimeter Array	U10	F	2549
HASL	5	17mm PBGA (Pb-Free) - Perimeter Array	U11	F	4787
HASL	5	27mm PBGA - Perimeter Array	U1o	F	1347
HASL	5	27mm PBGA - Perimeter Array	U2o	F	1447.5
HASL	5	27mm PBGA - Thermal Array	U2i	F	1671.5
HASL	5	27mm PBGA - Thermal Array	U1i	F	1736
HASL	5	27mm PBGA (Pb-Free) - Perimeter Array	U6o	F	3839
HASL	5	27mm PBGA (Pb-Free) - Perimeter Array	U3o	F	4456.5
HASL	5	27mm PBGA (Pb-Free) - Thermal Array	U6i	C	4816
HASL	5	QFN	U7	F	4365
HASL	5	QFN	U4	C	4816
HASL	5	QFN	U5	C	4816
HASL	5	Resistor Bank	R6-10	F	1085.5
HASL	5	Resistor Bank	R1-5	F	1626.5
HASL	6	17mm PBGA - Perimeter Array	U9	F	1764
HASL	6	17mm PBGA - Perimeter Array	U10	F	2422.5
HASL	6	17mm PBGA (Pb-Free) - Perimeter Array	U11	C	4816
HASL	6	27mm PBGA - Perimeter Array	U2o	F	1297.5
HASL	6	27mm PBGA - Perimeter Array	U1o	F	1607
HASL	6	27mm PBGA - Thermal Array	U1i	F	1762.5
HASL	6	27mm PBGA - Thermal Array	U2i	F	1984.5
HASL	6	27mm PBGA (Pb-Free) - Perimeter Array	U6o	F	4665.5
HASL	6	27mm PBGA (Pb-Free) - Perimeter Array	U3o	F	4725.5
HASL	6	27mm PBGA (Pb-Free) - Thermal Array	U6i	C	4816
HASL	6	QFN	U4	C	4816
HASL	6	QFN	U5	C	4816
HASL	6	QFN	U7	C	4816
HASL	6	Resistor Bank	R1-5	F	849
HASL	6	Resistor Bank	R6-10	F	1708
HASL	7	17mm PBGA - Perimeter Array	U10	F	1852
HASL	7	17mm PBGA - Perimeter Array	U9	F	2567
HASL	7	17mm PBGA (Pb-Free) - Perimeter Array	U11	C	4816
HASL	7	27mm PBGA - Perimeter Array	U1o	F	1628
HASL	7	27mm PBGA - Perimeter Array	U2o	F	1723
HASL	7	27mm PBGA - Thermal Array	U2i	F	1731
HASL	7	27mm PBGA - Thermal Array	U1i	F	2076.5
HASL	7	27mm PBGA (Pb-Free) - Perimeter Array	U6o	F	4181.5
HASL	7	27mm PBGA (Pb-Free) - Perimeter Array	U3o	F	4616.5
HASL	7	27mm PBGA (Pb-Free) - Thermal Array	U6i	C	4816
HASL	7	QFN	U4	C	4816
HASL	7	QFN	U5	C	4816
HASL	7	QFN	U7	C	4816
HASL	7	Resistor Bank	R6-10	F	1012.5
HASL	7	Resistor Bank	R1-5	F	1322

Surface Finish	Brd #	Electronic Package	Brd Locational Reference	F/C	Cycle # Failure
ImSn	1	17mm PBGA - Perimeter Array	U9	F	2652
ImSn	1	17mm PBGA - Perimeter Array	U10	F	2974.5
ImSn	1	17mm PBGA (Pb-Free) - Perimeter Array	U11	C	4816
ImSn	1	27mm PBGA - Perimeter Array	U2o	F	1342.5
ImSn	1	27mm PBGA - Perimeter Array	U1o	F	1528
ImSn	1	27mm PBGA - Thermal Array	U1i	F	1843
ImSn	1	27mm PBGA - Thermal Array	U2i	F	1843.5
ImSn	1	27mm PBGA (Pb-Free) - Perimeter Array	U3o	F	4266
ImSn	1	27mm PBGA (Pb-Free) - Perimeter Array	U6o	F	4446
ImSn	1	27mm PBGA (Pb-Free) - Thermal Array	U6i	F	4115
ImSn	1	QFN	U7	F	4015.5
ImSn	1	QFN	U5	F	4604
ImSn	1	QFN	U4	C	4816
ImSn	1	Resistor Bank	R6-10	F	1458
ImSn	1	Resistor Bank	R1-5	F	1568.5
ImSn	2	17mm PBGA - Perimeter Array	U9	F	1974
ImSn	2	17mm PBGA - Perimeter Array	U10	F	2159.5
ImSn	2	17mm PBGA (Pb-Free) - Perimeter Array	U11	F	4394
ImSn	2	27mm PBGA - Perimeter Array	U2o	F	1321
ImSn	2	27mm PBGA - Perimeter Array	U1o	F	1635
ImSn	2	27mm PBGA - Thermal Array	U2i	F	1816
ImSn	2	27mm PBGA - Thermal Array	U1i	F	2151
ImSn	2	27mm PBGA (Pb-Free) - Perimeter Array	U6o	F	3246.5
ImSn	2	27mm PBGA (Pb-Free) - Perimeter Array	U3o	F	4621
ImSn	2	27mm PBGA (Pb-Free) - Thermal Array	U6i	F	3690
ImSn	2	QFN	U4	C	4816
ImSn	2	QFN	U5	C	4816
ImSn	2	QFN	U7	C	4816
ImSn	2	Resistor Bank	R1-5	F	1525.5
ImSn	2	Resistor Bank	R6-10	F	1658
ImSn	3	17mm PBGA - Perimeter Array	U10	F	2291.5
ImSn	3	17mm PBGA - Perimeter Array	U9	F	2610
ImSn	3	17mm PBGA (Pb-Free) - Perimeter Array	U11	F	4698
ImSn	3	27mm PBGA - Perimeter Array	U1o	F	1566
ImSn	3	27mm PBGA - Perimeter Array	U2o	F	1665
ImSn	3	27mm PBGA - Thermal Array	U2i	F	1868
ImSn	3	27mm PBGA - Thermal Array	U1i	F	2014
ImSn	3	27mm PBGA (Pb-Free) - Perimeter Array	U6o	F	4275.5
ImSn	3	27mm PBGA (Pb-Free) - Perimeter Array	U3o	F	4455
ImSn	3	27mm PBGA (Pb-Free) - Thermal Array	U6i	C	4816
ImSn	3	QFN	U5	F	4318.5
ImSn	3	QFN	U4	C	4816
ImSn	3	QFN	U7	C	4816
ImSn	3	Resistor Bank	R6-10	F	1059
ImSn	3	Resistor Bank	R1-5	F	1401

ImSn	4	17mm PBGA - Perimeter Array	U9	F	2386
ImSn	4	17mm PBGA - Perimeter Array	U10	F	2914
ImSn	4	17mm PBGA (Pb-Free) - Perimeter Array	U11	C	4816
ImSn	4	27mm PBGA - Perimeter Array	U2o	F	1596.5
ImSn	4	27mm PBGA - Perimeter Array	U1o	F	1678.5
ImSn	4	27mm PBGA - Thermal Array	U1i	F	1935
ImSn	4	27mm PBGA - Thermal Array	U2i	F	2064
ImSn	4	27mm PBGA (Pb-Free) - Perimeter Array	U3o	F	4364
ImSn	4	27mm PBGA (Pb-Free) - Perimeter Array	U6o	F	4515
ImSn	4	27mm PBGA (Pb-Free) - Thermal Array	U6i	C	4816
ImSn	4	QFN	U4	C	4816
ImSn	4	QFN	U5	C	4816
ImSn	4	QFN	U7	C	4816
ImSn	4	Resistor Bank	R1-5	F	1041.5
ImSn	4	Resistor Bank	R6-10	F	1526
ImSn	5	17mm PBGA - Perimeter Array	U9	F	2738
ImSn	5	17mm PBGA - Perimeter Array	U10	F	2951.5
ImSn	5	17mm PBGA (Pb-Free) - Perimeter Array	U11	C	4816
ImSn	5	27mm PBGA - Perimeter Array	U1o	F	1668
ImSn	5	27mm PBGA - Perimeter Array	U2o	F	1708
ImSn	5	27mm PBGA - Thermal Array	U2i	F	1687.5
ImSn	5	27mm PBGA - Thermal Array	U1i	F	2056
ImSn	5	27mm PBGA (Pb-Free) - Perimeter Array	U6o	F	4035.5
ImSn	5	27mm PBGA (Pb-Free) - Perimeter Array	U3o	C	4816
ImSn	5	27mm PBGA (Pb-Free) - Thermal Array	U6i	C	4816
ImSn	5	QFN	U4	C	4816
ImSn	5	QFN	U5	C	4816
ImSn	5	QFN	U7	C	4816
ImSn	5	Resistor Bank	R6-10	F	1463
ImSn	5	Resistor Bank	R1-5	F	1691.5
ImSn	6	17mm PBGA - Perimeter Array	U10	F	2393
ImSn	6	17mm PBGA - Perimeter Array	U9	F	2914.5
ImSn	6	17mm PBGA (Pb-Free) - Perimeter Array	U11	C	4816
ImSn	6	27mm PBGA - Perimeter Array	U2o	F	1802
ImSn	6	27mm PBGA - Perimeter Array	U1o	F	2022.5
ImSn	6	27mm PBGA - Thermal Array	U1i	F	2173.5
ImSn	6	27mm PBGA - Thermal Array	U2i	F	2226
ImSn	6	27mm PBGA (Pb-Free) - Perimeter Array	U3o	F	3796
ImSn	6	27mm PBGA (Pb-Free) - Perimeter Array	U6o	F	3968
ImSn	6	27mm PBGA (Pb-Free) - Thermal Array	U6i	C	4816
ImSn	6	QFN	U4	C	4816
ImSn	6	QFN	U5	C	4816
ImSn	6	QFN	U7	C	4816
ImSn	6	Resistor Bank	R6-10	F	1164.5
ImSn	6	Resistor Bank	R1-5	F	1469
ImSn	7	17mm PBGA - Perimeter Array	U10	F	1464
ImSn	7	17mm PBGA - Perimeter Array	U9	F	2368
ImSn	7	17mm PBGA (Pb-Free) - Perimeter Array	U11	C	3142
ImSn	7	27mm PBGA - Perimeter Array	U1o	F	1528
ImSn	7	27mm PBGA - Perimeter Array	U2o	F	1753
ImSn	7	27mm PBGA - Thermal Array	U1i	F	1752
ImSn	7	27mm PBGA - Thermal Array	U2i	F	2011
ImSn	7	27mm PBGA (Pb-Free) - Perimeter Array	U3o	C	3142
ImSn	7	27mm PBGA (Pb-Free) - Perimeter Array	U6o	C	3142
ImSn	7	27mm PBGA (Pb-Free) - Thermal Array	U6i	C	3142
ImSn	7	QFN	U4	C	3142
ImSn	7	QFN	U5	C	3142
ImSn	7	QFN	U7	C	3142
ImSn	7	Resistor Bank	R6-10	F	1445.5
ImSn	7	Resistor Bank	R1-5	F	1899

Surface Finish	Brd #	Electronic Package	Brd Locational Reference	F/C	Cycle # Failure
OSP	1	17mm PBGA - Perimeter Array	U10	F	2601
OSP	1	17mm PBGA - Perimeter Array	U9	F	2739
OSP	1	17mm PBGA (Pb-Free) - Perimeter Array	U11	C	4816
OSP	1	27mm PBGA - Perimeter Array	U1o	F	1638.5
OSP	1	27mm PBGA - Perimeter Array	U2o	F	1790
OSP	1	27mm PBGA - Thermal Array	U2i	F	1839.5
OSP	1	27mm PBGA - Thermal Array	U1i	F	1951
OSP	1	27mm PBGA (Pb-Free) - Perimeter Array	U6o	F	3979
OSP	1	27mm PBGA (Pb-Free) - Perimeter Array	U3o	C	4816
OSP	1	27mm PBGA (Pb-Free) - Thermal Array	U6i	C	4816
OSP	1	QFN	U4	C	4816
OSP	1	QFN	U5	C	4816
OSP	1	QFN	U7	C	4816
OSP	1	Resistor Bank	R6-10	F	916.5
OSP	1	Resistor Bank	R1-5	F	1519.5
OSP	2	17mm PBGA - Perimeter Array	U9	F	2342
OSP	2	17mm PBGA - Perimeter Array	U10	F	2588.5
OSP	2	17mm PBGA (Pb-Free) - Perimeter Array	U11	C	4816
OSP	2	27mm PBGA - Perimeter Array	U2o	F	1687.5
OSP	2	27mm PBGA - Perimeter Array	U1o	F	1928.5
OSP	2	27mm PBGA - Thermal Array	U1i	F	2086
OSP	2	27mm PBGA - Thermal Array	U2i	F	2364.5
OSP	2	27mm PBGA (Pb-Free) - Perimeter Array	U3o	F	4183.5
OSP	2	27mm PBGA (Pb-Free) - Perimeter Array	U6o	F	4251
OSP	2	27mm PBGA (Pb-Free) - Thermal Array	U6i	C	4816
OSP	2	QFN	U4	C	4816
OSP	2	QFN	U5	C	4816
OSP	2	QFN	U7	C	4816
OSP	2	Resistor Bank	R6-10	F	945
OSP	2	Resistor Bank	R1-5	F	1247
OSP	3	17mm PBGA - Perimeter Array	U10	F	2483
OSP	3	17mm PBGA - Perimeter Array	U9	F	2585
OSP	3	17mm PBGA (Pb-Free) - Perimeter Array	U11	C	4816
OSP	3	27mm PBGA - Perimeter Array	U2o	F	1650
OSP	3	27mm PBGA - Perimeter Array	U1o	F	1833
OSP	3	27mm PBGA - Thermal Array	U1i	F	2000
OSP	3	27mm PBGA - Thermal Array	U2i	F	2062.5
OSP	3	27mm PBGA (Pb-Free) - Perimeter Array	U3o	F	4543
OSP	3	27mm PBGA (Pb-Free) - Perimeter Array	U6o	C	4816
OSP	3	27mm PBGA (Pb-Free) - Thermal Array	U6i	C	4816
OSP	3	QFN	U4	C	4816
OSP	3	QFN	U5	C	4816
OSP	3	QFN	U7	C	4816
OSP	3	Resistor Bank	R6-10	F	1104
OSP	3	Resistor Bank	R1-5	F	1285.5

OSP	4	17mm PBGA - Perimeter Array	U9	F	1918
OSP	4	17mm PBGA - Perimeter Array	U10	F	2314
OSP	4	17mm PBGA (Pb-Free) - Perimeter Array	U11	C	4816
OSP	4	27mm PBGA - Perimeter Array	U1o	F	1557.5
OSP	4	27mm PBGA - Perimeter Array	U2o	F	1591
OSP	4	27mm PBGA - Thermal Array	U2i	F	1864.5
OSP	4	27mm PBGA - Thermal Array	U1i	F	1966.5
OSP	4	27mm PBGA (Pb-Free) - Perimeter Array	U6o	F	4663
OSP	4	27mm PBGA (Pb-Free) - Perimeter Array	U3o	C	4816
OSP	4	27mm PBGA (Pb-Free) - Thermal Array	U6i	C	4816
OSP	4	QFN	U4	C	4816
OSP	4	QFN	U5	C	4816
OSP	4	QFN	U7	C	4816
OSP	4	Resistor Bank	R1-5	F	1037
OSP	4	Resistor Bank	R6-10	F	1265
OSP	5	17mm PBGA - Perimeter Array	U10	F	1716.5
OSP	5	17mm PBGA - Perimeter Array	U9	F	1967.5
OSP	5	17mm PBGA (Pb-Free) - Perimeter Array	U11	C	3142
OSP	5	27mm PBGA - Perimeter Array	U2o	F	1342
OSP	5	27mm PBGA - Perimeter Array	U1o	F	1433.5
OSP	5	27mm PBGA - Thermal Array	U2i	F	1814
OSP	5	27mm PBGA - Thermal Array	U1i	F	1941.5
OSP	5	27mm PBGA (Pb-Free) - Perimeter Array	U6o	C	3142
OSP	5	27mm PBGA (Pb-Free) - Perimeter Array	U3o	F	4699
OSP	5	27mm PBGA (Pb-Free) - Thermal Array	U6i	C	3142
OSP	5	QFN	U5	C	3142
OSP	5	QFN	U7	C	3142
OSP	5	QFN	U4	F	4431
OSP	5	Resistor Bank	R6-10	F	959.5
OSP	5	Resistor Bank	R1-5	F	1419
OSP	6	17mm PBGA - Perimeter Array	U9	F	3050.5
OSP	6	17mm PBGA - Perimeter Array	U10	F	3193.5
OSP	6	17mm PBGA (Pb-Free) - Perimeter Array	U11	C	4816
OSP	6	27mm PBGA - Perimeter Array	U2o	F	1590
OSP	6	27mm PBGA - Perimeter Array	U1o	F	1749
OSP	6	27mm PBGA - Thermal Array	U1i	F	2070.5
OSP	6	27mm PBGA - Thermal Array	U2i	F	2254.5
OSP	6	27mm PBGA (Pb-Free) - Perimeter Array	U6o	F	4551
OSP	6	27mm PBGA (Pb-Free) - Perimeter Array	U3o	C	4816
OSP	6	27mm PBGA (Pb-Free) - Thermal Array	U6i	C	4816
OSP	6	QFN	U4	F	4291
OSP	6	QFN	U5	C	4816
OSP	6	QFN	U7	C	4816
OSP	6	Resistor Bank	R6-10	F	851
OSP	6	Resistor Bank	R1-5	F	1134.5
OSP	7	17mm PBGA - Perimeter Array	U10	F	2235
OSP	7	17mm PBGA - Perimeter Array	U9	F	2312
OSP	7	17mm PBGA (Pb-Free) - Perimeter Array	U11	C	4816
OSP	7	27mm PBGA - Perimeter Array	U1o	F	1742.5
OSP	7	27mm PBGA - Perimeter Array	U2o	F	1786.5
OSP	7	27mm PBGA - Thermal Array	U1i	F	1922
OSP	7	27mm PBGA - Thermal Array	U2i	F	2080.5
OSP	7	27mm PBGA (Pb-Free) - Perimeter Array	U6o	F	4076.5
OSP	7	27mm PBGA (Pb-Free) - Perimeter Array	U3o	F	4492
OSP	7	27mm PBGA (Pb-Free) - Thermal Array	U6i	C	4816
OSP	7	QFN	U7	F	4649
OSP	7	QFN	U4	C	4816
OSP	7	QFN	U5	C	4816
OSP	7	Resistor Bank	R1-5	F	988
OSP	7	Resistor Bank	R6-10	F	1186

APPENDIX N: TV3D Configuration 2 Data

Name	**Brd #**	**Electronic Package**	**Brd Locational Reference**	**F/C**	**Cycle # Failure**
LF-LF-LF	1	17mm PBGA	U10	C	1000
LF-LF-LF	1	17mm PBGA	U11	C	1000
LF-LF-LF	1	Resistor Bank	R6-10	F	745.5
LF-LF-LF	1	Resistor Bank	R1-5	F	972
LF-LF-LF	2	17mm PBGA	U11	F	1224
LF-LF-LF	2	17mm PBGA	U10	C	2000
LF-LF-LF	2	Resistor Bank	R6-10	F	995.5
LF-LF-LF	2	Resistor Bank	R1-5	F	1265
LF-LF-LF	3	17mm PBGA	U11	F	1868
LF-LF-LF	3	17mm PBGA	U10	F	2256
LF-LF-LF	3	Resistor Bank	R6-10	F	767.5
LF-LF-LF	3	Resistor Bank	R1-5	F	1022
LF-LF-LF	4	17mm PBGA	U10	F	1903
LF-LF-LF	4	17mm PBGA	U11	F	2364
LF-LF-LF	4	Resistor Bank	R6-10	F	886.5
LF-LF-LF	4	Resistor Bank	R1-5	F	1263.5
LF-LF-LF	5	17mm PBGA	U10	F	741
LF-LF-LF	5	17mm PBGA	U11	F	1190
LF-LF-LF	5	Resistor Bank	R1-5	F	776.5
LF-LF-LF	5	Resistor Bank	R6-10	F	1187
LF-LF-LF	6	17mm PBGA	U10	F	1051
LF-LF-LF	6	17mm PBGA	U11	F	2036
LF-LF-LF	6	Resistor Bank	R6-10	F	1126
LF-LF-LF	6	Resistor Bank	R1-5	F	1328
LF-LF-LF	7	17mm PBGA	U10	F	1121
LF-LF-LF	7	17mm PBGA	U11	F	2196
LF-LF-LF	7	Resistor Bank	R1-5	F	712
LF-LF-LF	7	Resistor Bank	R6-10	F	984.5

Name	Brd #	Electronic Package	Brd Locational Reference	F/C	Cycle # Failure
LF-L-L	1	17mm PBGA	U10	F	927
LF-L-L	1	17mm PBGA	U11	C	1000
LF-L-L	1	Resistor Bank	R1-5	C	1000
LF-L-L	1	Resistor Bank	R6-10	C	1000
LF-L-L	2	17mm PBGA	U10	F	745
LF-L-L	2	17mm PBGA	U11	F	969
LF-L-L	2	Resistor Bank	R1-5	F	790
LF-L-L	2	Resistor Bank	R6-10	F	1312
LF-L-L	3	17mm PBGA	U10	F	637
LF-L-L	3	17mm PBGA	U11	F	2096
LF-L-L	3	Resistor Bank	R6-10	F	1424.5
LF-L-L	3	Resistor Bank	R1-5	F	1911
LF-L-L	4	17mm PBGA	U11	F	557
LF-L-L	4	17mm PBGA	U10	F	2037.5
LF-L-L	4	Resistor Bank	R1-5	F	1109
LF-L-L	4	Resistor Bank	R6-10	F	1502.5
LF-L-L	5	17mm PBGA	U11	F	646
LF-L-L	5	17mm PBGA	U10	F	1800
LF-L-L	5	Resistor Bank	R1-5	F	1029
LF-L-L	5	Resistor Bank	R6-10	F	1655
LF-L-L	6	17mm PBGA	U11	F	665.5
LF-L-L	6	17mm PBGA	U10	F	1655
LF-L-L	6	Resistor Bank	R1-5	F	556
LF-L-L	6	Resistor Bank	R6-10	F	1135.5
LF-L-L	7	17mm PBGA	U10	F	1052.5
LF-L-L	7	17mm PBGA	U11	F	2043
LF-L-L	7	Resistor Bank	R1-5	F	1650.5
LF-L-L	7	Resistor Bank	R6-10	F	1930.5

Name	Brd #	Electronic Package	Brd Locational Reference	F/C	Cycle # Failure
LF-L-LF	1	17mm PBGA	U10	C	1000
LF-L-LF	1	17mm PBGA	U11	C	1000
LF-L-LF	1	Resistor Bank	R1-5	F	775
LF-L-LF	1	Resistor Bank	R6-10	C	1000
LF-L-LF	2	17mm PBGA	U10	C	2000
LF-L-LF	2	17mm PBGA	U11	C	2000
LF-L-LF	2	Resistor Bank	R6-10	F	1180.5
LF-L-LF	2	Resistor Bank	R1-5	F	1438
LF-L-LF	3	17mm PBGA	U11	F	1198
LF-L-LF	3	17mm PBGA	U10	F	1497
LF-L-LF	3	Resistor Bank	R1-5	F	1012
LF-L-LF	3	Resistor Bank	R6-10	F	1752.5
LF-L-LF	4	17mm PBGA	U11	F	1308
LF-L-LF	4	17mm PBGA	U10	F	1382
LF-L-LF	4	Resistor Bank	R1-5	F	1091.5
LF-L-LF	4	Resistor Bank	R6-10	F	1908.5
LF-L-LF	5	17mm PBGA	U11	F	1148
LF-L-LF	5	17mm PBGA	U10	F	1813
LF-L-LF	5	Resistor Bank	R6-10	F	1446.5
LF-L-LF	5	Resistor Bank	R1-5	F	1469.5
LF-L-LF	6	17mm PBGA	U10	F	1551.5
LF-L-LF	6	17mm PBGA	U11	F	2372
LF-L-LF	6	Resistor Bank	R6-10	F	918.5
LF-L-LF	6	Resistor Bank	R1-5	F	1262
LF-L-LF	7	17mm PBGA	U10	F	1513.5
LF-L-LF	7	17mm PBGA	U11	F	2144
LF-L-LF	7	Resistor Bank	R6-10	F	1067.5
LF-L-LF	7	Resistor Bank	R1-5	F	1125.5

Name	Brd #	Electronic Package	Brd Locational Reference	F/C	Cycle # Failure
L-L-L	1	17mm PBGA	U10	C	1000
L-L-L	1	17mm PBGA	U11	C	1000
L-L-L	1	Resistor Bank	R6-10	F	974.5
L-L-L	1	Resistor Bank	R1-5	C	1000
L-L-L	2	17mm PBGA	U11	F	1395
L-L-L	2	17mm PBGA	U10	F	1987
L-L-L	2	Resistor Bank	R1-5	F	1120
L-L-L	2	Resistor Bank	R6-10	F	1405.5
L-L-L	3	17mm PBGA	U10	F	1044
L-L-L	3	17mm PBGA	U11	F	1765
L-L-L	3	Resistor Bank	R6-10	F	1476.5
L-L-L	3	Resistor Bank	R1-5	F	1558.5
L-L-L	4	17mm PBGA	U10	F	1978
L-L-L	4	17mm PBGA	U11	F	2462
L-L-L	4	Resistor Bank	R1-5	F	1315.5
L-L-L	4	Resistor Bank	R6-10	F	1601
L-L-L	5	17mm PBGA	U10	F	1826.5
L-L-L	5	17mm PBGA	U11	F	2328
L-L-L	5	Resistor Bank	R6-10	F	623.5
L-L-L	5	Resistor Bank	R1-5	F	1402
L-L-L	6	17mm PBGA	U10	F	1710
L-L-L	6	17mm PBGA	U11	F	2350.5
L-L-L	6	Resistor Bank	R1-5	F	1240
L-L-L	6	Resistor Bank	R6-10	F	1322.5
L-L-L	7	17mm PBGA	U10	F	1289
L-L-L	7	17mm PBGA	U11	F	1756
L-L-L	7	Resistor Bank	R1-5	F	819
L-L-L	7	Resistor Bank	R6-10	F	877.5

Name	Brd #	Electronic Package	Brd Locational Reference	F/C	Cycle # Failure
L-L-LF	1	17mm PBGA	U10	C	1000
L-L-LF	1	17mm PBGA	U11	C	1000
L-L-LF	1	Resistor Bank	R1-5	C	1000
L-L-LF	1	Resistor Bank	R6-10	C	1000
L-L-LF	2	17mm PBGA	U10	C	2000
L-L-LF	2	17mm PBGA	U11	C	2000
L-L-LF	2	Resistor Bank	R1-5	F	673.5
L-L-LF	2	Resistor Bank	R6-10	C	2000
L-L-LF	3	17mm PBGA	U10	F	1718
L-L-LF	3	17mm PBGA	U11	F	1812
L-L-LF	3	Resistor Bank	R1-5	F	1296.5
L-L-LF	3	Resistor Bank	R6-10	F	1523
L-L-LF	4	17mm PBGA	U10	F	2214
L-L-LF	4	17mm PBGA	U11	F	2270
L-L-LF	4	Resistor Bank	R6-10	F	689
L-L-LF	4	Resistor Bank	R1-5	F	961
L-L-LF	5	17mm PBGA	U11	F	2100
L-L-LF	5	17mm PBGA	U10	F	2257.5
L-L-LF	5	Resistor Bank	R1-5	F	1173
L-L-LF	5	Resistor Bank	R6-10	F	1634.5
L-L-LF	6	17mm PBGA	U11	F	2271
L-L-LF	6	17mm PBGA	U10	F	2515
L-L-LF	6	Resistor Bank	R6-10	F	872.5
L-L-LF	6	Resistor Bank	R1-5	F	1776.5
L-L-LF	7	17mm PBGA	U11	F	2177.5
L-L-LF	7	17mm PBGA	U10	F	2270
L-L-LF	7	Resistor Bank	R6-10	F	1047.5
L-L-LF	7	Resistor Bank	R1-5	F	1117.5

APPENDIX O: ACRONYMS/NOMENCLATURE

Ag → Silver
Backward System → Lead free solder balls assembled on tin-lead solder paste
BCT → Body-centered tetragonal
BGA → Ball grid array
Bkw → Backwards
BT → Bismaleimide Triazine
C → Censored
CAVE → Center for Advanced Vehicle Electronics
CTE → Coefficient of Thermal Expansion
Cu → Copper
DNP → Distance from Neutral Point
EDX → Energy Dispersive X-ray
F → Failed
Forward System → Tin-lead solder balls assembled on lead free solder paste
HASL → Hot Air Solder Level
ImAg → Immersion Silver
ImSn → Immersion Tin
LF-LF-LF → Lead free solder balls - lead free solder paste - lead free reflow profile
LF-L-L → Lead free solder balls - lead containing solder paste - tin-lead reflow profile
LF-L-LF → Lead free solder balls - lead containing solder paste - lead free reflow profile
L-L-L → Lead containing solder balls - lead containing solder paste - tin-lead reflow profile
L-L-LF → Lead containing solder balls - lead containing solder paste - lead free reflow profile
LSEs → Least Squares Estimators
MLEs → Maximum Likelihood Estimators
mm → millimeter
NSMD → Non Solder Mask Defined
OSP → Organic Solder Preservative
Pb → Lead
Pb-Free → Lead Free
PBGA → Plastic Ball Grid Array
PCB → Printed Circuit Board
QFN → Quad Flat No-lead
QFP → Quad Flat Pack
SEM → Scanning Electron Microscope
SJ → Solder Joints
SMD → Solder Mask Defined
Sn → Tin
SnPb → Tin Lead
SnPbAg → Tin Lead Silver
TAL → Time Above Liquidus
TV3D_C1 → TV3D Configuration 1
TV3D_C2 → TV3D Configuration 2
β → Beta (Weibull Slope)
η → Nu (Weibull Characteristic Life)