A Novel Through-Silicon-Via (TSV) Fabrication Method

by

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Abstract

The Through Silicon Via (TSV) is expected to be the future of 3-D chip stacking technology for electronic devices. The structure of the TSV interconnect is developed by first etching deep vias into the surface of a wafer, and later filling those vias with a desired metal. Currently, copper based TSVs are the most cost effective mass producible TSVs. Vias filled with copper provide the interconnect “through” the wafer, once both the top and the bottom of the vias are exposed. This provides a solid robust interconnect isolated and protected by the wafer. It also provides the interconnect using much less volume, while reducing the need for a majority of the packaging associated with modern microelectronic packages. Copper based TSVs were produced in this work using two methods, the ADE method and the blind-via method. The ADE method introduces a unique process that is potentially compatible with post-microelectronic manufacturing. The fabricated TSVs from both methods were cross-sectioned for analysis, which revealed successful formation of solid copper TSVs.

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List of Abbreviations

AU	Auburn University
TSV	Through-Silicon-Via
MEMS	Microelectromechanical Systems
DRIE	Deep Reactive Ion Etching
HMDS	Hexamethyldisilazane
DI	De-Ionized
CMP	Chemical Mechanical Polishing
DRIE	Deep Reactive Ion Etching
STS	Surface Technology Systems
ASE	Advanced Silicon Etcher
CTE	Coefficient of Thermal Expansion
AMNSTC	Alabama Micro/Nano Science and Technology Center
PR	Photoresist
PVA	Polyvinyl Alcohol

Chapter 1: Introduction

As the package size of modern microelectronics rapidly shrinks, Moore's law begins to accurately describe the limitation on the amount of technology that can fit on an integrated circuit. The development of single electron transistors such as the SketchSET; however, have given us a glimpse towards the end of transistor scaling [1]. As the end of Moore's law approaches, a more recent approach emerges, called "More than Moore". This new trend attempts to improve systems by reducing the package size of devices. This ultimately delivers a higher component density. This transitions the electronic world from a classical multichip module, in which multiple chips were used for different functions, to a system on chip (SOC) model which integrates everything into a single chip. Production of such a chip, however, can be difficult with current conventional approaches.

One of the main limiting factors in package size comes from a chip's interconnects. Modern technology heavily uses wire bonds, which may take little material volume but as a result of their use they waste much more 3-D space. This is because nothing can come in contact with them, forcing them to be spatially separated from the chip and each other. Additionally, they have to be electrically isolated using more material. The leading alternative to wire bonds is the utilization of Through-Silicon-Vias (TSVs). TSVs are interconnects that pass through a wafer or chip allowing for an electrical connection through the substrate. This technology is beginning to be commercially utilized in many different devices, and it shows a promising future in many prospective applications including cameras [2], video cameras [3], and DRAM [4].

As TSVs ease their way into modern devices, the number of potential benefits and the effectiveness of these interconnects are surfacing. The benefits TSVs introduce are numerous. To begin with, a TSV can be customized to fit many different design specifications from dimensions

to materials to the location of the TSVs. They drastically reduce the routing length in comparison with wire bonds. A TSV's reduced length can increase speed and improve the performance of a circuit. Their mechanical robustness and isolation within the wafer make them ideal long term interconnects for a wide variety of applications.

With the demand for TSVs growing, this research is intended to propose a detailed procedure for an existing TSV development method as well as introduce a new method. A detailed description of those methods, along with experimental results, will be discussed. Problems that arose during the fabrication and how they were handled will also be analyzed.

Chapter 2: Literature Review

This chapter will focus on different methods that have been used to develop TSVs. It will discuss different materials, processes and technologies that can be utilized during the TSV microfabrication process. It will also review previous published work related to TSVs

2.1 Wafers

There are many different types of semiconductor wafers, including silicon, gallium arsenide, and gallium phosphide [5]. Silicon wafers are heavily used in industry since they are readily available and relatively inexpensive compared to Gallium based wafers. The leading alternative is gallium arsenide (GaAs), which is far more expensive but more ideally suited for microelectronic processing, and is considered toxic due to the presence of Arsenic. Although GaAs circuits can operate much faster due to GaAs's intrinsic electrical properties[6], the cost and possible safety concerns removed it from consideration for this project. Thus, in this paper, wafers are assumed to be made of silicon.

2.2 Cleaning

In any micro fabrication process, maintaining a clean wafer is essential. According to some sources, over fifty percent of IC yield losses are a direct result of micro-contamination [7]. This section will describe different methods that can be used throughout the fabrication process to maintain a clean wafer.

2.3 Wet Etching

Piranha etch is solution mixture of sulfuric acid (H_2SO_4, 98%) and hydrogen peroxide (H_2O_2, 30%) and is used to remove organics from a wafer. One ratio that can be used is 4:1 (H_2O_2:H_2SO_4) [7]. An HF (hydrofluoric acid) etch will etch through silicon dioxide as the acidity will form silanol bonds with the oxide on the wafer surface. The fluorine will form SiF_4

gas which is soluble in water yielding H_2SiF_6 [8]. This removes all oxides on the wafer surface making it hydrophobic. Nitric acid can be added to HF in order to enhance the etching properties [9]. Another method is known as the RCA Standard Clean. It is composed of two separate bath solutions. The first, known as RCA standard clean 1 (or SC-1) is a mixture of 5:1:1 H_2O : H_2O_2 : NH_4OH and is carried out for 10 minutes at 75-80°C. The second solution is known as the RCA standard clean 2 (or SC-2), which is used for the same duration and temperature as SC-1 but is composed of 6:1:1 H_2O : H_2O_2 : HCl. The solution is formulated not to aggressively attack Si or SiO_2 [10]. Tetramethyl ammonium hydroxide (TMAH, $(CH_3)_4NOH$) has been introduced as a silicon etch [**11**]. Although, the TMAH solution requires many other solutions including surfactants, pH regulators and complexing agents. Of all the different types of etching solutions listed here, the RCA standard clean's trusted method along with the HF's effective cleaning were the deciding factors in integrating them into the blank wafer cleaning process for this research.

2.4 Primer

A primer is used as an adhesion promoter so that the PR may adhere well to the silicon wafer's surface. There are different primer materials and methods of application.

2.4.1 Primer Materials

There are many choices for wafer primer. For silicon, the main three choices are: $(CH_3)_3SiNHSi(CH_3)_3$ 1,1,1,3,3,3-hexamethyldisilizane (HMDS), $C_6H_5SiCl_3$ Phenyltrichlorosilane or trichlorophenylsilane (TCPS), and $(CH_3)_3SiNCH_3COSi(CH_3)_3$ bistrimethylsilylacetamide (BSA). In the case of gallium arsenide (GaAs) wafers, Monazoline C, Trichlorobenzene, and Xylene are more desirable primers due to GaAs wafer's polar surface. For the purpose of this research, we will focus on the silicon wafer primers. Of the three silicon primers, it can be seen from the chemical equation that TCPS contains chlorine which is toxic

and corrosive; this primer also requires a hard bake of 200°C for 30 minutes [12]. BSA had little material resources available. The Hazardous Materials Identification System (HMIS® ranking chemicals from 0 minimal hazard to 4 severe hazard) rating on the HMDS sheets were used to compare safety [13], [14], [15]. TCPS and BSA were ranked a 3, and HMDS was ranked a 2. HMDS was chosen as the PR primer due to TCPS and BSA's health concern, the TCPS requiring a long hard bake, and the BSA resources being difficult to obtain.

2.4.2 Primer Application Methods

There are two main methods for HMDS priming. The first is called spin priming, and is performed by dripping a small amount of primer on the wafer and spinning the wafer to propel excess primer of the surface and to evaporate any remaining solution. This can only be done one wafer at a time. The second method is Vapor priming, and can be performed on multiple wafers at the same time while yielding good uniformity. Thus, being the preferred method for industry, it was chosen as the selected method for primer application for this project.

2.5 Photoresist (PR)

There are many different types of resist that can be used to mask a wafer. There are photosensitive liquid resists that are poured onto a spinning wafer, which removes excess resist and thins the resist down to a desired thickness. This process gives the user good control over formation of the resist on the wafer's surface. Dry film PRs are also becoming popular as they boast advantages such as protection of vias, wafer back-side protection, high etching selectivity (100:1), and also allowing the chemical processing for copper traces and vias.[16]. In comparison to spin-on liquids, they do not exhibit an edge-bead deformity which is the collection of PR on ridges or the edge of the wafer. Although there are some added benefits to the dry film

approach, its added benefit has no profound effect on TSV processing. The AMNSTC's experience using spin-on resists made it a more controlled variable in process development.

2.6 Etching

The etching process forms the via in any TSV procedure. There are three critical parameters that are used to analyze an etching process. The first parameter is feature size, which can be considered the width of the via since it is the smallest feature of the etch. The second parameter is an expansion of feature size, which is the aspect ratio of the etch. This gives us a comparison of the vertical sidewall height to the width of the etch. The last parameter is the sidewall surface roughness which needs to be smooth in order to allow for a better TSV.

2.6.1 Mechanical Drilling

Mechanical drilling is the same for micro scale as it is in macro scale. It uses a bit which is smaller than the hole being drilled, and is made from a strong enough material to withstand the forces associated with drilling (i.e. cemented carbide)[17]. Mechanical drilling can have an aspect ratio >10, although the feature size must be greater than 300μm, and the roughness is considered "average" [18]. The average sidewall roughness is due to the drill bit's non-uniformity and possibly micro-deformations developed due to drilling forces/abrasion. Although, the aspect ratio and roughness may be workable into a TSV procedure, the feature size is too large to be commercially viable.

2.6.2 Chemical Etching

Chemical Etching is a slight improvement over mechanical drilling for feature size. It allows for a reduced minimum feature size of 150 μm, but it is limited by an aspect ratio of roughly 1. The sidewall roughness is more uniform than mechanical drilling [18]. Wet etching is usually cheap, fast, and has limited damaging effects on the wafer; however, it is very isotropic

and would be very difficult to control in making high aspect ratio and high quality through silicon vias[19]. Thus, even with the improvements workable into a TSV procedure, the feature size needs to be competitive with wire bond technology in order for there to be enough benefit to use it in a TSV procedure.

2.6.3 Electrical Discharge Machining

Although Electrical Discharge Machining is a technology generally used to cut metals, it has recently been tested on silicon. Since the silicon is softer than most metals, the speed of machining silicon is faster, while exposing the electrode to less wear [20]. This technology is a further improvement in both aspect ratio (roughly 15) and minimum feature size (>50µm).The sidewall roughness is poorer than chemical etching, but roughly equal with mechanical drilling [18]. However, the minimum feature size and aspect ratios are big enough improvements over mechanical drilling and chemical etching to make it a better choice

2.6.4 Powder Blasting

Powder Blasting is another approach for etching wafers. It uses a photosensitive elastomer as a protection layer around the via. Then using 9-29µm diameter Al_2O_3 particles bombarding the silicon wafer at 90m/s, it begins to etch the silicon through the mask. The minimum feature size that can be obtained is roughly equal to electrical discharge machining (>50µm), but yields a poorer aspect ratio (~3-5) than mechanical drilling and electrical discharge machining. The sidewall roughness is the poorest of all etching discussed in this article [18]. The poor sidewall characteristics and aspect ratio make this an undesirable etching process for TSVs.

2.6.5 Laser Cutting and Ablation

Both laser processes were maskless but required a PVA layer on the wafer surface to prevent the ejected material from contaminating the wafer. Laser cutting was experimented with

in the same comparison study using an ND:YAG laser whose wavelength of 1064nm. It was pulsed for a duration of 0.2ms on a spot size ranging from 30-100µm. A high-pressure gas flow removed the molten silicon. This produced a better minimum feature size (>30µm), but not as good surface characterization as laser ablation [18].

Laser ablation was experimented with in the same comparison study using an ND:YAG laser whose wavelength of 355nm and pulsed for a duration of 30ns on a spot size ranging from 10-30µm. This yielded a high power density beam (108~1010 W/cm2), which evaporated the silicon instead of melting it. The results yielded a better aspect ratio (>20) and minimum feature size (>10µm) than the previously described techniques. The sidewall characterization was the same as mechanical drilling and electrical discharge machining [18]. The sidewall characterization and lack of equipment prevented this research from pursuing this option. Although, it should be mentioned that laser methods can be significantly faster than DRIE (roughly 25 times according to some research)[21]. This may soon compete with the Deep Reactive Ion Etching in that it is much faster and can also be used to dice a substrate. However, it should also be noted that laser etching is performed one via at a time, and if there are many vias, this process may actually take longer.

2.6.6 Deep Reactive Ion Etching

DRIE was also compared in the same study using SF_6/O_2 chemistry, using PECVD oxide as the masking layer. The result of the DRIE yielded the best aspect ratio (>20), minimum feature size (>5µm), and acceptable roughness [18]. This direct comparison proved that DRIE was still the best process for making vias. In addition to the standard BOSCH process for DRIE, a newer and higher aspect ratio method called the S.H.A.R.P. process has emerged from Alcatel

for the DRIE [22]. The BOSCH and S.H.A.R.P. processes made DRIE the most functional technology for etching silicon.

2.7 Seed Layer Deposition

Most research has been employing the standard E-beam/CVD approach for depositing a copper seed layer for TSVs [23][24][25]. DC sputtering was another approach used to line vias with a copper seed layer [26]. Those who used the E-beam and sputtering mechanisms also tended to taper the via's sidewalls before deposition. This was performed in order to obtain proper coating on the via's sidewalls. One research group worked with Metalorganic Chemical Vapor Deposition (MOCVD) and had a very conformal seed deposition on high aspect ratio (16:1) vias. This MOCVD approach allowed for sidewalls perpendicular to the surface while depositing a very conformal thin layer of copper [27].

2.8 Fill Material

Many fill materials can be used to fill TSVs. The need will come from the wide range of devices used in a wide variety of conditions. One study showed a detailed look at the stresses caused by CTE differences at extreme temperatures, and showed a more pronounced effect on device lifespan as TSV size increases. In addition, the study commented on the idea that the standard fill material being used today (copper) does not have a suitable coefficient of thermal expansion match with silicon. [28] Further investigation found that there are many conductors that can be used for this purpose. Cost, resistivity and wafer compatibility were the main considerations. Wafer compatibility referred to the volumetric coefficient of expansion, β. This aspect of the materials should be taken into long-term consideration, since over time, the expansion and contraction of the plated metal may have detrimental effects on the lifetime of the device. Finding a material to fill the vias that best matches the volumetric coefficient of

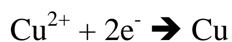
expansion of silicon may produce a higher yield for long-term, extreme temperature, and high current density devices. For the context of this paper, the low resistivity and cost of copper, as well as its use in commercial devices, were the deciding factors in pursuing copper as the fill material. A variety of possible plating materials are listed and compared in Table 1.

Table 1: Resistivity, Cost, and Volumetric Coefficients for TSV Fill Candidates

Material	Resistivity Ω·cm at 20°C [29]	Cost ($/lb) [30]	Volumetric Coefficient of Expansion [31]
Copper	1.68×10^{-8}	3.99	5.1×10^{-5}
Silver	1.59×10^{-8}	561.16	5.4×10^{-5}
Gold	2.44×10^{-8}	21,746.66	4.2×10^{-5}
Tungsten	5.6×10^{-8}	15.00	1.35×10^{-5}
Silicon			$.9 \times 10^{-5}$

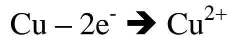
2.9 Electroplating

There are several methods for electroplating. The base of all the mechanisms involves a circuit connection connecting the cathode target to the negative terminal of the power supply and the anode to the positive terminal of the power supply and connecting the two in series through a solution. The solution is generally a copper sulfate based solution. The solution is composed of sulfuric acid and copper sulfate, which may contain traces of metal impurities. The sulfuric acid has three main functions. The first is to prevent the hydrolysis of water found in the solution. The second function is to decrease resistivity. This reduces the overall power required for the plating as well as reduces the formation of rough deposits when higher currents are obtained. It also decreases copper ion concentration, but it doesn't inhibit the supply of copper ions. The cathode (negative, or target wafer) uses the simple reaction:



$Cu^{2+} + 2e^{-} \rightarrow Cu$

to take the aqueous copper and form solid copper with the acceptance of two electrons. The reverse occurs at the anode (positive, or source) in order to continually replenish the solution with copper ions:

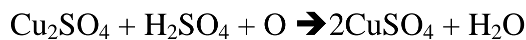


$$Cu - 2e^{-} \rightarrow Cu^{2+}$$

Ideally the sulfuric acid is not needed; however, since copper can be either Cu2+ or Cu+, the copper anode may give off Cu+ ions via the following reaction:

$$Cu - e^{-} \rightarrow Cu^{+}$$

The Cu+ ions would ideally plate the target with less current, but it tends to oxidize via oxygen found in solution from exposure to air or through non-degassed DI water through the following reaction:



$$Cu_2SO_4 + H_2SO_4 + O \rightarrow 2CuSO_4 + H_2O$$

Summarized:

$$2Cu^{+} + 2H^{+} + O \rightarrow 2Cu^{2+} + H_2O$$

The Cu+ ions also tend to form a solid Cu sludge residue on the source copper's surface as well as expelling it into solution through the reaction:

$$Cu_2SO_4 \rightarrow CuSO_4 + Cu$$

Summarized:

$$2Cu^{+} = Cu^{2+} + Cu$$

There are three ways to avoid these problems. The first is periodic solution preplacement with water and sulfuric acid to maintain balance. The second approach includes using nodes containing small amounts of lead. Or finally, the solution can completely be replaced [32].

Two common problems with electroplating blind-via TSVs include voids, seams, and platting overburden. To combat these two causes for error, many researchers have employed

different techniques, but most use a variety of chemical additives. The first additive in combating voids is the addition of an accelerator. This chemical accelerates the copper deposition rate. If only this were used, then void formation would still not be inhibited since the rapid copper deposition would cause the via to neck off (or bottle off) much faster. Thus, a leveler is added to deactivate the accelerated plating along the neck of the via. This inhibits the void from sealing off. If only these two chemicals were used then the vias would fill conformally but would have excessive overburden on the surface of the wafer. Thus another additive that can be used is what is called suppressor, which inhibits the copper deposition. It is a long polymer that tends to coat the wide open surfaces to create a "blocking" layer to inhibit copper overburden on the surface [33].

In addition to chemistry issues, one study showed the negative side effects of directional fluid flow over TSVs during plating [34]. This need for even solution flow over the wafer's surface has been met in several different ways. Some researchers employ a shower head jet nozzle spraying towards the wafer in solution in order to achieve coating in the depths of vias [35]. The use of a ShearPlate™ mixer (by Nexx Systems) has also been proven to be very beneficial in achieving conformal copper coating. In addition the same research has proven that smoother denser plating can be achieved by using a reduced current [36].

2.10 TSV Applications

TSVs boast a wide range of benefits including: low power consumption, short connections, higher density, better heat dissipation, reduced RC delays, and low impedance [37]. The application of these benefits yields the much desired effects in the products we use every day. The following is a discussion on TSV applications.

There has been much research in recent years in regard to TSVs. Modest capacitance reduction can be achieved with the replacement of long wires or wire bonds with shorter TSVs. This greatly enhances performance and power efficiency of devices. While Through Silicon Stacking (TSS) produces reduced form factor (allowing miniaturization), reducing the overall volume of the device. This reduction has been experienced by different sources [38] [39], A side-effect of miniaturization is the difficulty associated with routing, thus copper redistribution layers can be plated in order to connect TSVs on different parts of a wafer. This allows TSVs to have an x-y dimension routing capability. [40]. Hermetic sealing is at times an industry requirement for some applications such as MEMS accelerometers and gyroscopes. TSVs are compatible with these hermetically sealed packages [41]. TSVs can also be coaxial if necessary, and do not need to be simple copper (or other fill material). Analysis and modeling has been performed on this type of structure [42]. One of the key applications and research has been its effective use in stacked devices such as memory and RAM. A 3-D solid state drive has been designed, employing TSVs to show significant improvement [43]. Another research group developed a DDR3 DRAM with copper TSVs. They were able to reduce standby power by 50% and the active power by 25% when compared with QDP packages. Additionally, the TSV design increased the I/O speeds to 1.5Gb/s. [44].

In addition to this research, many companies are implementing TSVs in different RAM modules. Elpida Memory, Inc., for example, has recently begun sample shipments of its 1GB DDR3 SDRAM (x32) based TSV technology consuming very low power [45]. Samsung, however, tops this with its 8GB advanced Green DDR3 DRAM module. Samsung is able to reduce power by nearly 40% with this technology. They state that even with the 30% reduction in memory slots for next generation servers, TSV technology will overcome this by increasing

density by more than 50%. [4]. The excessively high density bandwidth of TSVs was also used as an advantage in TSV research carried out by Georgia Tech in order to improve memory fetch times, which merely stacking main memory on processors could not achieve [46].

Toshiba took the TSV technology into cameras by applying them down to the pixel level by attaching each pixel directly to a dedicated application specific integrated circuit (ASIC) through a TSV. ST Microelectronics has also utilized TSVs in ultra-small 2 megapixel system on chip image sensors with a built-in image signal processor [47]. This was used in an image sensor that was developed for mobile phones. [48][2]. Medigus also made the world's smallest medical video camera, only 0.99mm in diameter. [3].

Micron is also using this technology in what they call Osmium™ Packaging Technology. It takes advantage of TSVs (which they call TWIs or Through Wafer Interconnects) as the interconnect for this new technology in order to eliminate wire bonds from hindering the device's electrical performance. [49]. Tessera Technologies had one of the first Through-Silicon-Via solutions it called SHELLCASE MVP wafer-level chip-scale packaging (WLCSP), which now licenses for others to utilize TSVs in developing thinner, faster, and what it claims cheaper devices [50]. Silex Microsystems also offers its own version of Through Silicon Vias called Sil-Via®, but interestingly offers what it calls Met-Cap™ which is a Metal Via Wafer Level packaging that actually contains a cavity up to the surface of the wafer. It says it can be used as a capping feature in addition to being used to store passive devices [51]. This is a small variety of the many TSV manufacturers.

As industry pushes TSV manufacturing into the mainstream, software companies such as Cadence have jumped on board to develop technology allowing for the easy testing of TSV implemented 3D stacked ICs [52]. Mentor Graphics Corporation is also beginning to follow up

with its Calibre physical verification/extraction tool and its Tessent IC test solution to allow for TSV compatible test and verifications [53].

With the advantages of TSVs, it is apparent why so many companies are flocking toward TSV implementation.

Chapter 3: Materials, Equipment and Processes

The following sections describe in detail the materials, equipment and processes used throughout the research in this document. In addition to research, all the materials, equipment, and processes used in this research were located the Alabama Micro Nano Science and Technology Center (AMNSTC) facilities. The facilities contain a 4000 square foot Class-100 clean room in addition to several auxiliary laboratories. The laboratory is fully equipped with standard microelectronic fabrication equipment.

3.1 Materials and Chemicals

This section describes in detail the materials and chemicals used in this research.

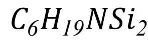
3.1.1 Silicon Wafers

Silicon wafers (to be called wafers) are the first design decision of any device. There are many different orientations that can be chosen. The processes described in this work are orientation independent and thus any orientation is compatible. Thus, arbitrary (100) and (111) (for backing wafers) orientations were chosen.

3.1.2 HMDS

Photolithography is a critical process during microfabrication. PR's adhesion to the wafer's surface is a critical step in this process. In order to assure quality PR adhesion to a wafer's surface, a primer, such as HMDS, must be coated on the wafer surface prior to PR application. This is necessary because even with the oxide strip during the RCA clean, the silicon wafer naturally develops a thin layer of oxide when exposed to atmosphere. In addition to the PR not adhering well to oxide, the oxide adsorbs water from the air through hydrogen bonds. Thus water may be absorbed by the oxide if a primer is not used, and the presence of water prior to PR application makes it difficult for the PR to adhere to the silicon wafer's surface.

The primer chosen for this research was Hexamethyldisilizane (HMDS). It works by exploiting the presence of silicon dioxide, on which it will chemically bond with the oxide and leave a surface which is readily adhesive to PR. This can be seen by closer examination of the HMDS structure. The chemical formula for HMDS is:



$$C_6H_{19}NSi_2$$

The chemical structure is shown Figure 1 below.

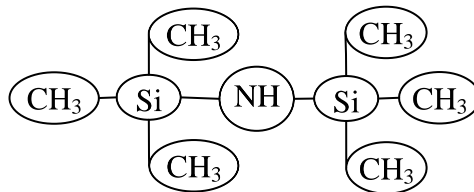
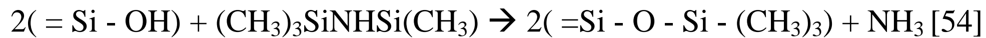


Figure 1: HMDS Chemical Structure

The chemical reaction is:



$$2(= Si - OH) + (CH_3)_3SiNHSi(CH_3) \rightarrow 2(=Si - O - Si - (CH_3)_3) + NH_3 \text{ [54]}$$

Using the equation, the following 3 images show how HMDS interacts with the oxidized silicon surface in order to bind to it and leave binding sites for the PR. First the NH from within the HMDS structure approaches the silicon wafer as shown in Figure 2.

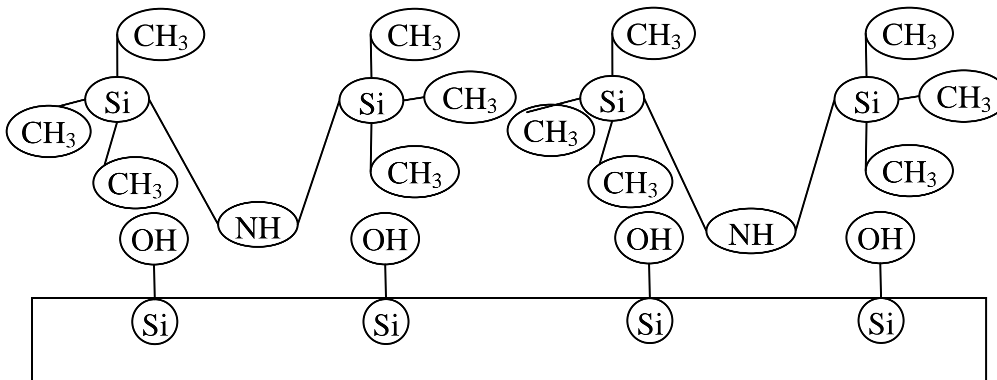


Figure 2: HMDS Coming Into Contact With An Oxidized Silicon Surface

The HMDS then chemically bonds with the oxidized surface by stripping the oxygen atoms of hydrogen and forming NH_3 (ammonia).

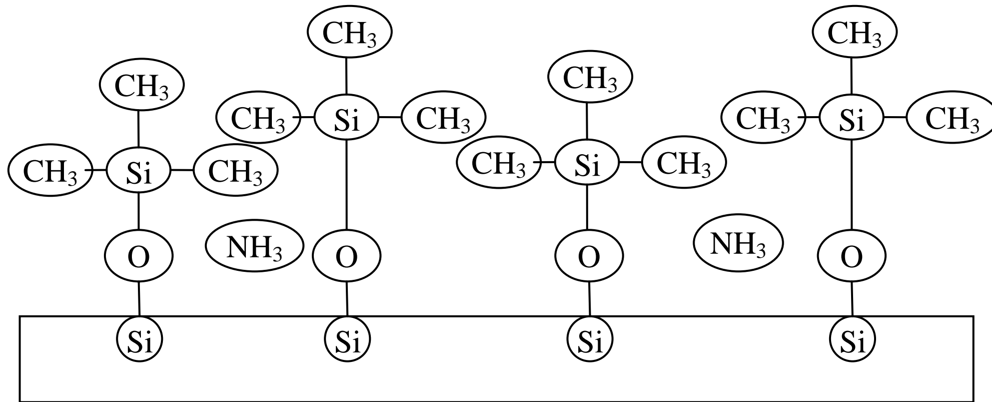


Figure 3: HMDS Chemically Bonding With the Oxidized Silicon Surface

The ammonia gas is then released as byproducts leaving the HMDS chemically bonded with oxide bonded on the Silicon's surface (Figure 4). PR will now readily adhere to the primer applied surface.

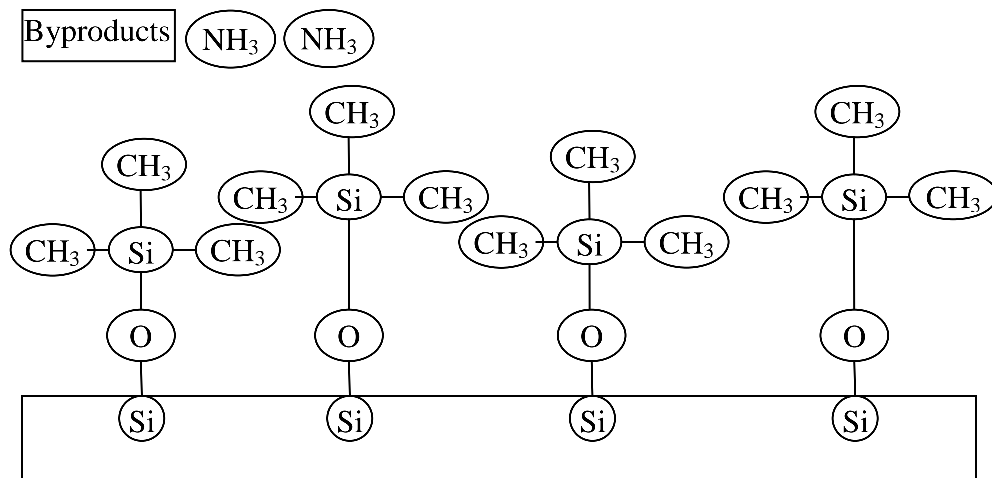


Figure 4: HMDS Bonding Complete

3.1.3 Photoresist

Two different photoresists were used in this research. The first was photoresist AZ P4620, which was chosen for its approximately 70:1 etching selectivity with Si when used in a DRIE. In

addition to this, it was chosen for its maximum spin on thickness of up to 24µm, which allowed for wafer etching down to any depth in the wafer. It is a positive photoresist which means areas exposed to UV radiation will be developed away. The second photoresist, AZ 9245, was chosen for its ability to brush up deformities in the photolithography process of the AZ P4620 and also used for temporary wafer to wafer bonding for full wafer etching. If a wafer was not backed with another wafer, there would be a gas up leak once the DRIE etching penetrated the entire depth of the wafer. These photoresists will be referred to as "PR" along with their name (AZ P4620 and AZ 9245).

3.1.4 Photolithography Masks

The photolithography mask used in this work (referred to as "mask") was made from chrome on glass. The mask is shown in Figure 5. The eight squares in the center of the mask contain 100µm circle diameters along their perimeters. The four sets of grids on the left and right of the squares are 10x10 grids of circles containing via dimension of 60, 70, 80, and 100µm.

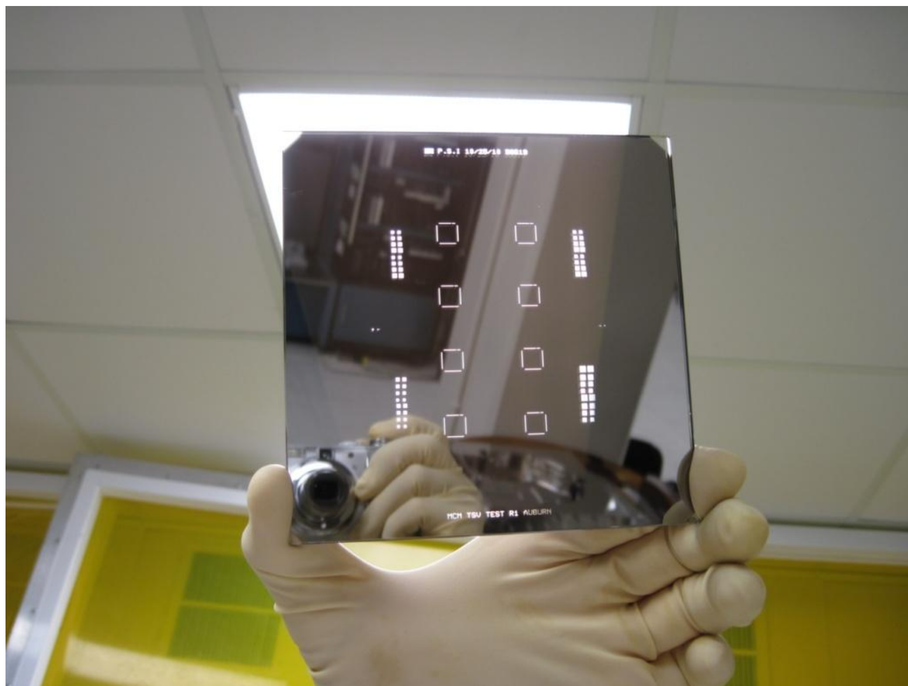


Figure 5: Photolithography Mask

3.1.5 Photoresist Developer

Once a PR coated wafer is exposed through a mask, it is developed in a developer solution. In this research, the only developer used was AZ 400K, which is a clear colorless solution. It is a potassium based buffered developer, is said to produce high contrast on thick film photoresists such as AZ P4620 and AZ 9245 photoresists. The developer was used in a 2:1 mixture of DI water (200mL) and AZ 400K (100mL). The wafers were developed for 1 minute, and then rinsed with DI water and N_2 air dried by hand.

3.1.6 Electroplating Chemicals

There were 2 types of solution chemistries for the electroplating in this research. The first solution was used for the ADE process and the second was used for the blind-via process.

The ADE process chemistry consisted of a solution from Enthone Chemicals known as "Part A", because of its general use with multiple additives for blind-via chemistries. In the ADE process, only part A was used because we did not need the additives for suppression (detailed in the blind-via portion of this section). The details of part A can be found in Table 2, and was the sole ingredient.

Table 2: Electroplating Chemistry for ADE Process

PART	Manufacturer	Manufacturer Part Number	Technical description	Use	Ratio	%
A	Enthone, Inc	Microfab DVF-200 TSV Sulfate Make Up	Copper Sulfate Solution	Copper source	3.5L	100%

The electroplating chemistry for the blind-via TSV was also from Enthone Chemicals. The chemistry contained four solutions, each with its own added benefit to the plating process.

Part A is a majority of the solution (98.519%) and is used as the source for copper ions in solution. These positive cations will neutralize on the negative copper wafer's surface, neutralizing the ions into solid, stable metal. Gradually this will plate the TSV on any copper surface. Since some TSVs can be very deep, a solution called "part B" is added to be 0.495% of the solution. This is known as the accelerator, since it accelerates the ions/solution into the bottoms of the TSVs. This allows for the solution to continually circulate into the depths of the TSV, allowing all copper surfaces to be plated. Another problem associated with plating is the overburden of plating on the wafer's planar surface. For this problem, a solution referred to as "part C" or the primary suppressor (referred to as the suppressor) is added as 0.617% of the solution. It is a solution containing larger molecules with position themselves on open easily accessible areas such as the wafer surface, suppressing excess plating. The final concern addressed with the chemistry is the ready availability of negative charge along the perimeter of the TSV opening the wafer, which has a tendency to result in excess plating around the "neck" of the via. This "necking off" leads to the sudden sealing of the via's opening, and results in voids within the center of the TSV. This problem requires the introduction of a new solution called "part D" or the secondary suppressor solution (to be called the leveler). It is added as 0.369% of the solution. It is a polar chemical that prevents the excessively charged wafer surface and the higher charged via openings from plating too quickly. It slows any plating in these areas by removing any plated copper. Since the rate of deposition is faster than the removal, only limited plating occurs (but no degradation). A summary of the plating chemistry can be found in Table 3.

Table 3: TSV Plating Chemical Summary

PART	Manufacturer	Manufacturer Part Number	Technical description	Use	Ratio	%
A	Enthone, Inc	Microfab DVF-200 TSV Sulfate Make Up	Copper Sulfate Solution	Copper source	3.5L	98.519%
B	Enthone, Inc	MICROFAB DVF 200-B Sulfuric acid	Accelerator	Accelerator	17.6mL	0.495%
C	Enthone, Inc	COMPOUND C94510 MICROFAB DVF 200-C 1,2-Ethanediol	Primary Suppressor	Suppressor	21.9mL	0.617%
D	Enthone, Inc	MICROFAB DVF 200-D	Secondary Suppressor	Leveler	13.1mL	0.369%

3.2 Equipment

In this section, the detailed descriptions of each piece of equipment used in order to undertake this research are presesnted. A short reference name/descriptor is given for each tool to be referred to throughout this document.

3.2.1 Spin Rinse Dryer – STI Semitool ST 240 Wafer Spin Rinse Dryer

The STI Semitool ST 240 Wafer Spin Rinse Dryer (Figure 6) is used throughout the fabrication process to keep a clean wafer surface. The spin rinse dryer contains a wafer boat used to hold 4in wafers, which are locked into place before the spin rinse dry begins. There are two phases: a spin-rinse phase and a spin-dry phase. During the spin-rinse phase, the wafers begin to spin while DI water is sprayed on the surfaces of the wafers. The DI water removes any debris and contamination while the rotation propels the debris-collected water off the wafer's surfaces to a drain. This spin-rinse phase has adjustable time and rotation parameters. For this research, the time was fixed to 90 seconds and the rotation speed was fixed to 500 rpm. The drying phase immediately follows. In this phase, the wafers spin while heated nitrogen air is blown to dry the

wafers. The force of the nitrogen gas removes larger droplets of water from the surface while the heat from the nitrogen gas dries the wafers on a micro-scale. This step also has the same adjustable time and rotation parameters. For this research, the time was fixed to 120 seconds and the rotation speed was fixed to 2500 rpm. Together these two steps ensure a streak-free, clean wafer surface. This procedure will be referred to as a "spin-rinse-dry".

Figure 6: Spin Rinse Dryer – STI Semitool ST 240 Wafer Spin Rinse Dryer

3.2.2 Ultrasonic Cleaner: Branson 5510 Tabletop Ultrasonic Cleaner

The 2.5 gallon tank is filled to the operating level with water. The sample to be cleaned is then placed in a pyrex bowl and the bowl is filled with a cleaning solution (acetone, IPA, etc…). The machine is turned on and the 40kHz ultrasonic frequency vibrates the sample through the solutions. This is used for a variety of tasks including vibrating away any debris from deep vias or simply quick removal of photoresist from a wafer's surface. This will be referred to as an "ultrasonic clean".

Figure 7: Ultrasonic Cleaner: Branson 5510 Tabletop Ultrasonic Cleaner

3.2.3 HMDS Coating Chamber

The HMDS chamber (Figure 8) is used to coat/bond HMDS, an adhesion promoter for photoresist, to a wafer's surface. The wafers are placed face-up in a wafer boat, which is placed in the chamber with a small quantity of HMDS poured into the basin. The wafers are placed face up in order to avoid contact with the surface of the wafer's edges. The volatile HMDS then fills the chamber and bonds to the wafer's oxidized surface, allowing future photoresist to adhere well to the wafer's surface. This will be referred to as an "HMDS coat".

Figure 8: HMDS Coating Chamber

3.2.4 Photoresist Spinner

A photoresist spinner (Figure 9), manufactured by Cost Effective Equipment, ensured proper PR coating on the wafer's surface. It was capable of coating 4-6 inch wafers. It allowed precise and accurate control of the PR's thickness as well even uniformity. This was accomplished by controlling the parameters listed in Table 4. The spin speed (0 to 6000rpm) controlled the thickness of the PR, with shorter spin time coating a thicker PR. The time (0 to 999sec) and to a lesser extent ramp acceleration (0~30,000rpm/sec) controlled the uniformity of the PR coat. Longer time and slower ramp acceleration providing the best uniformity. This will be referred to as a "PR spin" and the parameters will be listed as "a spin speed of A rpm and a ramp acceleration of B rpm/s for C seconds".

Table 4: Photoresist Spinner Parameters

Parameter	Control	Effect
SPIN SPEED	The top speed (in rpm) desired for the given "TIME".	Thickness
RAMP ACCELERATION	Rate increase from 0 to "SPIN SPEED" in rpm/s.	Uniformity
TIME	Total time of the spinning in seconds.	Uniformity

Figure 9: Photoresist Spinner

3.2.5 Hotplate

Following a PR application, a wafer is heated on a hotplate (Figure 10), this is called a softbake, to remove solvents and gases trapped in the PR. For AZ9245 photoresist, the softbake schedule is shown in Table 5. As for AZ P4620, the softbake schedule is shown in Table 6.

Figure 10: Hotplate

Table 5: Softbake Schedule AZ 9245

Duration (seconds)	Temperature (°C)	Wafer separation from hotplate surface (cm)
30	110	1.5
150	110	0

Table 6: Softbake Schedule AZ P4620

Duration (seconds)	Temperature (°C)	Wafer separation from hotplate surface (cm)
150	110	0

3.2.6 Karl Suss MA/BA6 Contact Aligner

The Karl Suss MA/BA6 Contact Aligner (Figure 11) brings a PR coated wafer into contact with a photolithography mask, and exposes UV light through the mask onto the wafer. The UV light comes from a mercury lamp. The machine is capable of processing wafers from 50mm to 150mm in diameter. It has three contact modes: Proximity, Soft and Hard. For this

work, the “hard” option was used in order to ensure maximum resolution. This means the mask will be in direct contact with the wafer, minimizing spacing and maximizing resolution. The optical resolution of the exposure device is 0.4μm, and the wavelength range of the lamp is 350-450nm. This will be referred to as the “exposure” procedure.

Figure 11: Karl Suss MA/BA6 Contact Aligner

3.2.7 Matrix Oxygen Plasma Asher

The Matrix Oxygen Plasma Asher (Figure 12) is used to remove organic/PR residue. The asher uses oxygen plasma, a heated chuck (0-190°C), high pressure (3-5 torr), and high RF power (0-500W) to remove any PR whether it is hardened by etching or simply difficult to remove. The oxygen plasma reacts with any organics (including PR) to form an ash that is

vacuum pumped from the system (hence “plasma asher”). For the purposes of this research, the chuck was not heated. The machine accepts both 4 and 5 inch wafers for processing. The tool effectively removes PR, but may also oxidize any exposed metal. It can also be used to descum (partially etch thin layers) of PR; however, a short time duration is desired. In this work, the asher was used to descum wafers immediately prior to etching, since the PR used for etching has a 70:1 etching ratio, even a small amount of PR residue could change the depth of vias containing PR residue. It was also used to completely remove any remaining PR or residue before wafers were copper coated in the E-beam system. The asher program used is called “PR_STRIP”. The only modified parameter was time of exposure which was 14 seconds for descum and 5 minutes for wafer cleaning. This was performed using 300W RF at a 4~5 Torr pressure with oxygen flowing at 31% of the rated 100sccm flow. The wafer was not heated since it had PR on it. The two processes will be referred to as descum and wafer clean.

Figure 12: Matrix Oxygen Plasma Asher

3.2.8 Inductively Coupled Plasma (ICP) Deep Reactive Ion Etcher (DRIE)

The Advanced Silicon Etcher manufactured by Surface Technologies Systems, Inc. shown in Figure 13 is an Inductively Coupled Plasma Deep Reactive Ion Etcher (to be referred to as DRIE). It utilizes the Bosch process using multiple, alternating cycles of passivation using C_4F_8 plasma and etching using SF_6/O_2. The machine has an RF induction coil which forms the plasma. This machine utilizes the BOSCH process to develop a nearly straight vertical anisotropic etch. There were three programs used on this machine that allowed for all the etching required in this work. They will be referred to as the "Via Low Power Etch" APPENDIX D, "Via High Power Etch" APPENDIX E, "Via Widen Etch Step 1" APPENDIX F and "Via Widen Etch Step 2" APPENDIX G. The difference between the low and high power via etch is the platen power (power applied to the plate that holds the wafer while processing).

Figure 13: ICP DRIE

3.2.9 Horizontal Oxidation and Diffusion Furnace

The oxidation furnace (Figure 14) is used to grow oxide in a controlled manner. It does this by controlling the temperature within the furnace as well as the flow of gases: nitrogen, oxygen, and hydrogen. The nitrogen flow is used to keep the furnace dry as well as clean (purging other gases). The oxygen is used to grow pure silicon dioxide (SiO_2), this is called dry oxidation. The introduction of hydrogen allows for more rapid, thicker silicon dioxide growth, but it is lower quality. This is called wet oxidation. The oxidation in this TSV research was performed via wet oxidation. The oxidation schedule used is shown in Appendix I .

Figure 14: Oxidation Furnace

3.2.10 Electron Beam Evaporation and Sputtering System

The Mark 50 electron beam chamber (Figure 15) made by CHA is used to deposit metals in thin layers. It can deposit the metal layers very precisely with high accuracy. It does so by

rotating the wafers to be deposited on a hemisphere carousel facing down towards the metal source. The metal source is in a crucible which is targeted with an electron beam guided toward the crucible with a magnetic field. The entire system is under high vacuum while the process is running. A three minute argon ion cleaning of the samples was performed prior to any deposition. The machine was used to deposit three metals for the various TSV processes: chrome, titanium, and copper. It will be referred to as "E-beam deposition of" a given metal at a given thickness in angstroms (Å).

Figure 15: Electron Beam Evaporation and Sputtering System

3.2.11 Profilometer: Tencor Alpha Step 200 Profilometer

The profilometer is a non-destructive way to take step measurements. It is accomplsihed using contact measurement of a diamond-tipped stylus. The tip is attached to an arm which moves the tip along the surface of the measured material. The profilometer measures the surface topology by measuring the arm's vertical deflection as the tip moves along the surface. It has a vertical range of ±160μm with a 5nm resolution. It can be used to measure step heights, etch depths, coating thicknesses, and surface roughness.

Figure 16: Profilometer: Tencor Alpha Step 200 Profilometer

3.2.12 Scanning Electron Microscope

A scanning electron microscope (Figure 17) was used in this research to analyze sidewall surface roughness. The machine works by emitting an electron beam from a tungsten coil filament that acts as a cathode. The sample is placed in a holder (anode) which is grounded to attract the electrons, which accelerate toward the sample in the holder. As the electrons approach the sample, they pass through a magnetic field which guides the beam through apertures to focus it on the sample. As the electrons hit the sample's surface, many deflections occur including cathodoluminescence, auger electrons, primary backscattered electrons, secondary electrons and x-rays. The SEM used in this research measures secondary electron deflections to produce the high quality images. Horizontal lines in the images from the SEM are a result of charging and are not actually present in the sample. This will be used to determine sidewall smoothness.

Figure 17: Scanning Electron Microscope

3.2.13 Pre-Wet System and Vacuum Pump

The chamber shown in (Figure 18) is the pre-wet system used to pre-wet the vias prior to electroplating. Since the electroplating process is a wet chemical process, it requires proper pre-wetting, which is the introduction of fluid into the vias before plating. This ensures that the entire via will plate in solution. The pre-wet is accomplished by placing the wafer to be plated in an empty petri dish. From here the wafers were pre-wet in two ways. In the first method, the petri-dish was filled with IPA and the vacuum pump was turned on. In the second method, the vacuum pump was turned on first before the dish was filled with IPA (without breaking the vacuum seal through a valve in the top of the chamber). The second method was more effective, as it removes all the air from the chamber and the insides of the vias instead of attempting to force the air out of the vias through the IPA in the petri dish. IPA was selected since it has a low surface tension. Therefore the low surface tension IPA rushes to fill the voids within the vias when air is evacuated. A rubber mallet was used to agitate the solution using mechanical shocks through the chamber. This entire process will be referred to as a "pre-wet" (either IPA first or vacuum first).

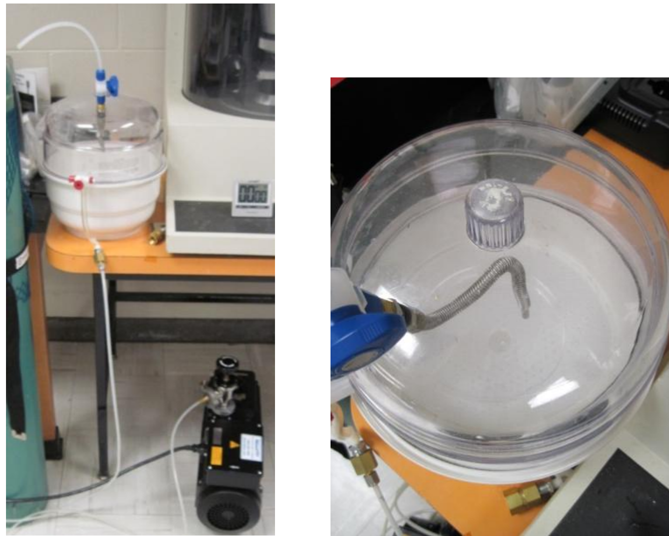


Figure 18: Pre-Wet System and Vacuum Pump

3.2.14 Beaker Copper Electroplating Bath

Initially plating was completed in a beaker set up as shown in Figure 19. The setup consisted of a current source to control and measure the applied current between the copper source and the tape assembly. The beaker is filled with Enthone Chemical's Microfab DVF-200 TSV Sulfate Solution to fully submerse the target and copper source. A magnetic spinner is used to stir the solution during plating.

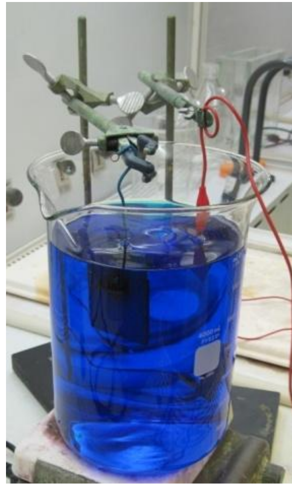


Figure 19: Beaker Copper Electroplating Bath

3.2.15 Custom Copper Electroplating Bath

The copper plating bath (Figure 20) is a custom designed copper electroplating bath. The problems with the beaker electroplating bath (such as non-uniformity and via necking off) prompted the design this custom bath. This bath was design for plating blind vias.

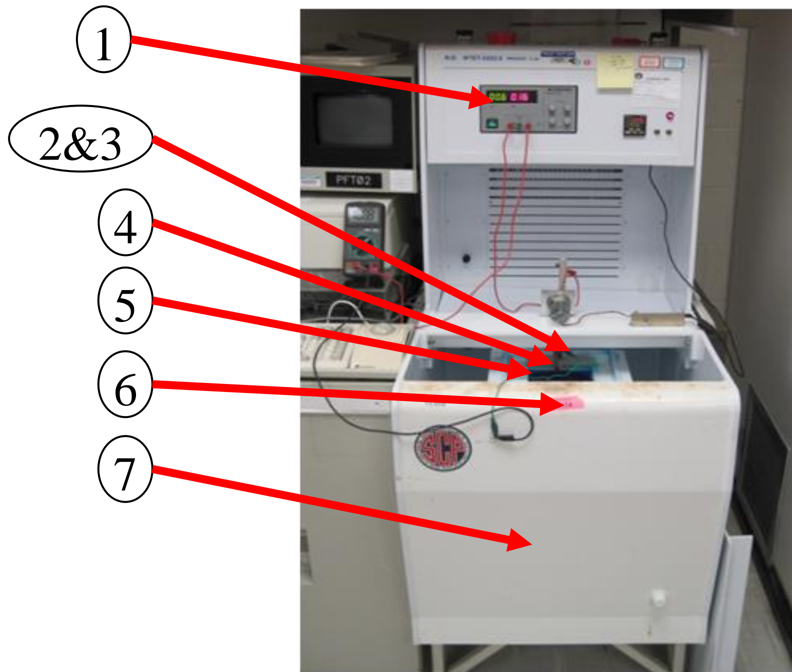


Figure 20: Copper Plating Bath

The main components of the copper plating bath include:

1. The Adjustable Current Source – steadily supplying a set current.

2. The plating target (cathode, wafer with Ti/Cu surface).

3. A wafer fixture to hold the copper coated face of the wafer pointing towards the copper source. The fixture has a water proof seal to protect the connectors used to connect to the anode’s surface.

4. A Sheer-Plate-Mixer (SPM) for moving waves of the plating chemistry on the wafer’s surface constantly (refreshing it). The SPM moves up and down at 6 Hz. There are laterally cut sections that allow fluid to freely flow through the SPM.

Figure 21: Sheer Plate Mixer

5. The metal source (Cu anode), which has vertical cuts to allow fluid flow from the pump through the source.

Figure 22: Pure Copper Source

6. The plating chemistry described earlier.

7. The filter/pump which pumps/filters the solution continuously.

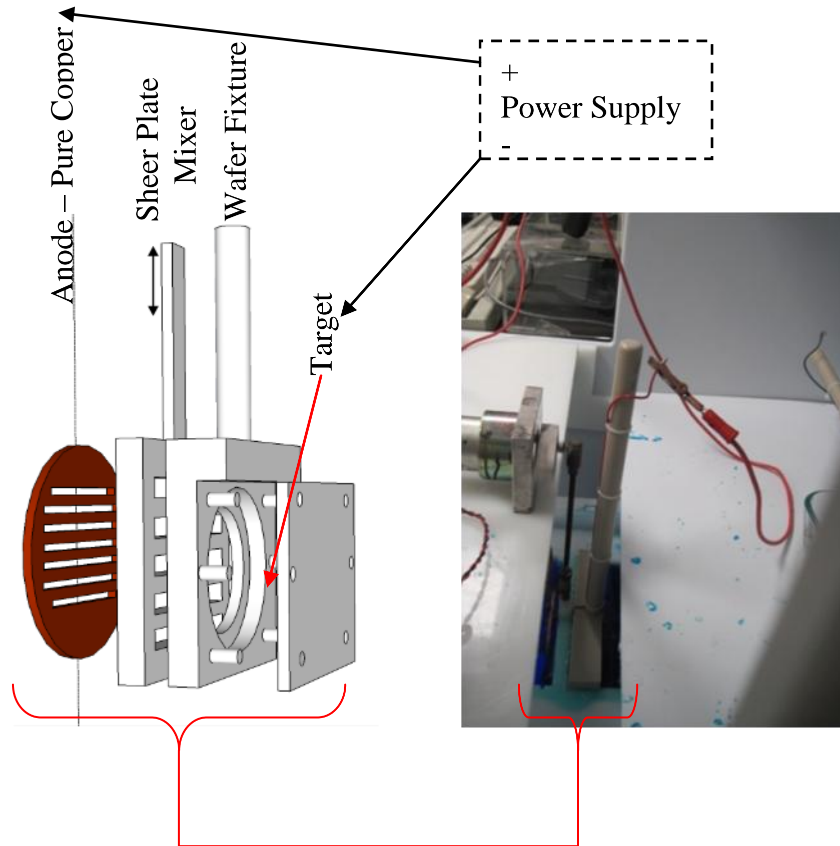


Figure 23: SPM Assembly Side View

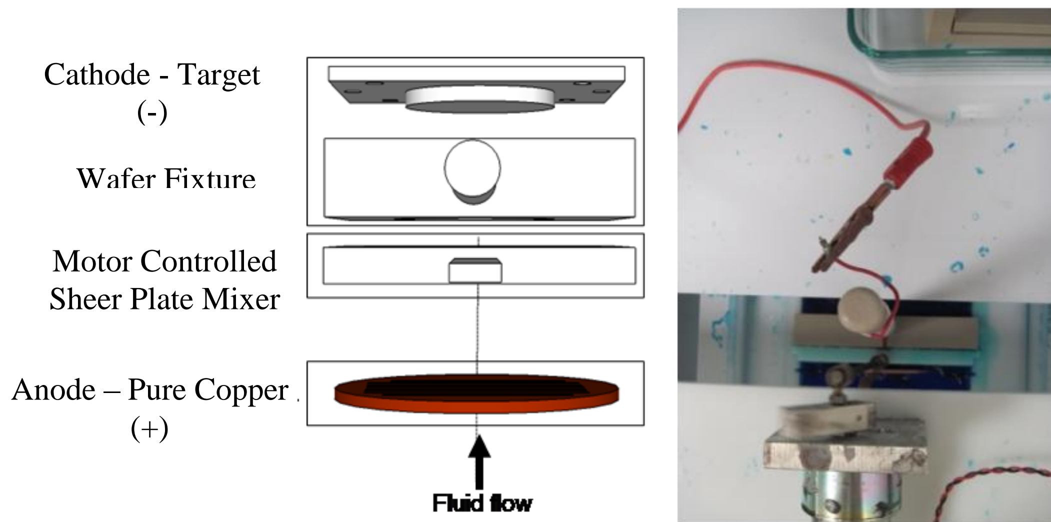


Figure 24: SPM Assembly Top View

Once the wafers are placed in the assembly and connected in the solution, the current supply is turned on and the current is ramped to the desired level to allow conformal plating/filling. This will be referred to as electroplating.

Since the ADE process is not a blind via process, the setup was slightly modified for electroplating using this process. The modification came in the form of a conductive wafer clip attached to the end of a conductive copper rod to connect to the tape used in the ADE process (Figure 25).

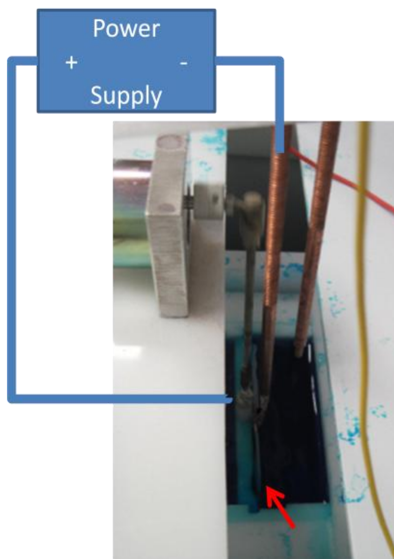


Figure 25: ADE Process Bath Set-Up

3.2.16 Dicing Saw: Disco Automatic Dicing Saw (DAD 3220)

This compact dicing saw was used to dice wafers into sections before using them for electroplating. It was also used to cut through the center of structures and obtain smooth sidewalls. This was done in order to produce high quality side profile images, as well as test for voids in the TSVs.

Figure 26: Dicing Saw: Disco Automatic Dicing Saw (DAD 3220)

Chapter 4: ADE Process Design, Fabrication, and Results

Two Methods were used to develop the TSVs. The first was the ADE process and is detailed in this section. The section begins with a more theoretical design, followed by the actual fabrication used, and finally a discussion of the results.

4.1 ADE Process

The ADE (Adhesive, DRIE, Electroplated) Process is a process that utilizes UV dicing tape to seal a wafer assembly. This sealed wafer assembly allows for copper plating from a backing wafer's seed layer through the vias of the TSV wafer. The detailed design and fabrication of this wafer is described in this section.

4.2 ADE Process Design

The wafer design consisted of 3 main parts (Figure 27). The first two parts are the fabrication and preparation of the TSV and Backing wafers. These two wafers can be processed in parallel. The two are then sealed into one assembly, using UV removable adhesive tape, and copper plated to fill the vias. The next three sections describe these parts in more detail.

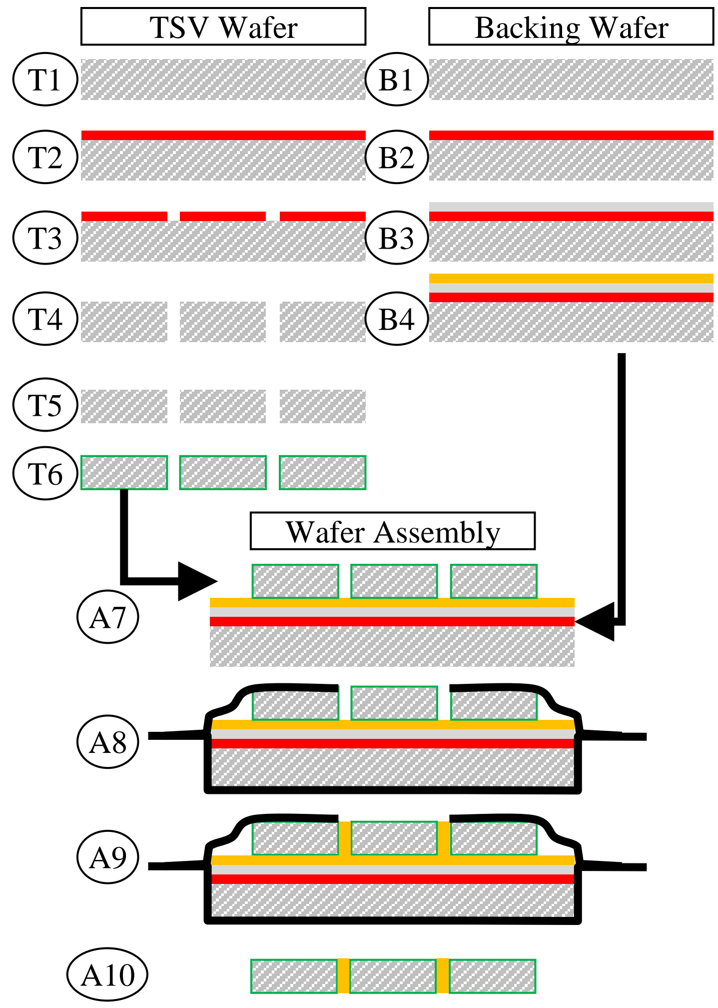


Figure 27: Detailed Design Using The ADE Process

4.2.1 TSV Wafer Design

The first part of the design consisted of fabricating the TSV wafer; a diagram of the process is shown in Figure 28. The first step was selecting a wafer. Any wafer thickness could have been used but the application called for using 100mm diameter, 350µm thick silicon wafers (Figure 28-T1). The wafers were then cleaned and deposited with PR (Figure 28-T2). This PR was then exposed and developed to reveal the TSV pattern (varying grids of 10x10 circles maximum 100µm diameter, 30µm spacing edge to edge) (Figure 28-T3). The DRIE was then used to etch the vias down through the entire depth (350µm) of the wafer (Figure 28-T4). The

wafers were then thinned using a backgrind and polish (Figure 28-T5). The backgrind and polish (CMP) step is not necessary in all applications, but this application required the thinning down of the wafer to 225µm. The wafer was then oxidized in order to prevent any electrical shorting between TSVs through the substrate (Figure 28-T6).

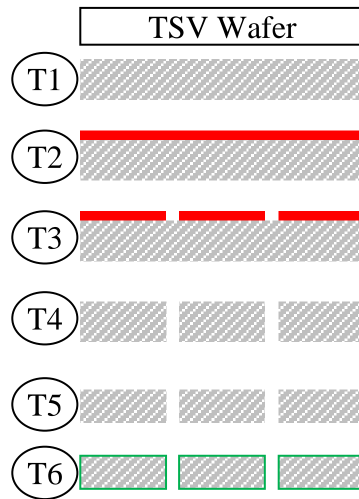


Figure 28: TSV Wafer Design

4.2.2 Backing Wafer Design

The backing wafer was the second part of the assembly. The fabrication process began the same way as the TSV wafer, by cleaning a blank wafer (Figure 29-B1) and preparing/spinning on of PR (Figure 29-B2); however, the PR was not exposed or developed. The seed layer deposition was performed using an electron beam evaporation system. 250Å of chromium (Figure 29-B3) and 2,500Å of copper (Figure 29-B4), which were sequentially deposited without breaking vacuum. This completed the backing wafer's preparation. The backing wafer, along with the TSV wafer, was then ready to be joined in the assembly.

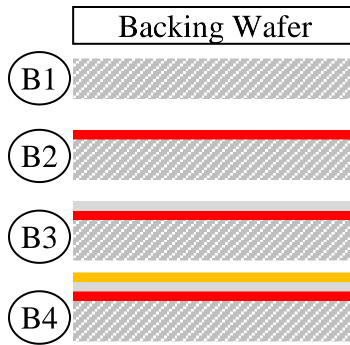


Figure 29: Backing Wafer Design

4.2.3 Wafer Assembly Design

The assembly began by stacking the TSV wafer on top of the copper surface of the backing wafer. A strip of electrically conductive adhesive copper foil tape was used to form an electrical connection from the backing wafer's copper layer through the tape assembly (Figure 30-A7). This way an electrode could be connected to it while it remained isolated in the plating solution. The assembly was then sealed using clear UV-removable adhesive tape. Openings were cut into the clear tape in order to expose the vias with copper at the base (Figure 30-A8). The wafers were then plated in a copper sulfate based TSV solution, with no added organics (Figure 30-A9). Once plating was completed, the UV tape was exposed to UV light and removed, leaving the plated wafer attached to the backing wafer through the PR. The remaining assembly was dipped in acetone to release the TSV wafer from the backing wafer by removing the sacrificial PR layer.

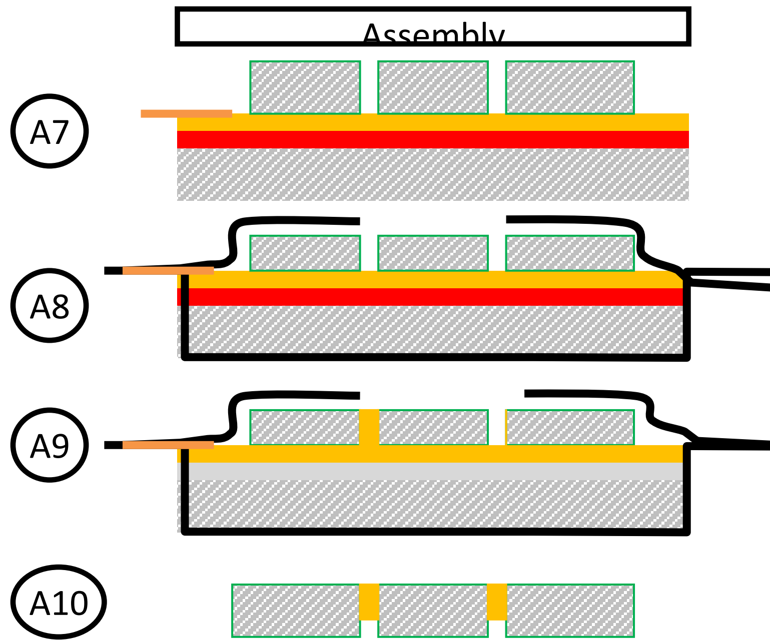


Figure 30: Wafer Assembly Design

4.3 ADE Process Fabrication

The procedure described in the design was followed as a guideline throughout the ADE process fabrication. Wafers were also quartered in order to get more trial results from a single wafer which would have very similar features since they were from the same wafer.

4.3.1 TSV Wafer Fabrication

The cleaning of these wafers was essential. The cleaning was performed using the RCA cleaning process to remove any organic, oxide, and metal contaminants. A spin-rinse dry was the final step in preparing the wafers for photolithography (Figure 28-T1). Once cleansed, the wafers were dehydration baked for 20 minutes. Since the TSV wafer was to be DRIE'd using a PR masking layer, a primer (HMDS) was coated to ensure PR adhesion during the aggressive DRIE process. The PR used was AZ P4620, which was a thick positive PR capable of spinning on at a thickness of up to 24µm. During Deep Reactive Ion Etching (DRIE) this PR had approximately a 70:1 etching selectivity with silicon. Once the PR was coated on the wafer, it was soft baked at

110°C for 2.5 minutes. Here it was essential to allow the wafer time to properly outgas in order to avoid deformities during exposure, development and etching. The outgassing allows any trapped gasses to release or solvents to evaporate from the PR. Once outgassed, the wafers were exposed to UV light in a contact mask aligner through a mask. The mask was composed of 10x10 grids of circles ranging in diameter with a maximum of 100µm. The pitch separating the circles was dependent on the via width with the maximum being 30µm. Once exposed, the wafer was developed in the 2:1 H_20:AZ400K developer solution for 1 minute

The wafer was then ready for the Inductively Coupled Plasma Deep Reactive Ion Etcher (ICPDRIE). The machine uses octafluoro-cyclobutane (C_4F_8) as the passivation gas and a mixture of sulfur hexafluoride / oxygen (SF_6/O_2) as the etching gas. The fluorine from the SF_6 provides the etching gas while the oxygen removes the passivaiton. These gasses were used in the BOSCH™ process in order to develop high aspect ratio vias. The etching program used is described in Appendix E . Once etched, the remaining PR on the surface was removed using acetone and a spin-rinse-dry. The wafer was then descumed to ensure via cleanliness. The wafers were then shipped to Aptek Industries for wafer CMP. The wafers were CMP processed down to the desired thickness of 225µm.

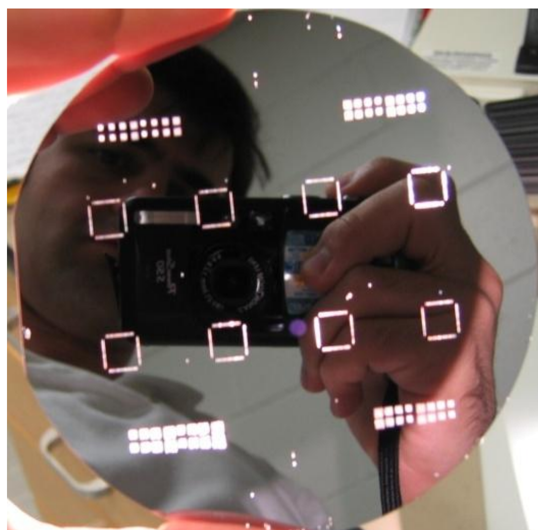


Figure 31: Wafer CMP

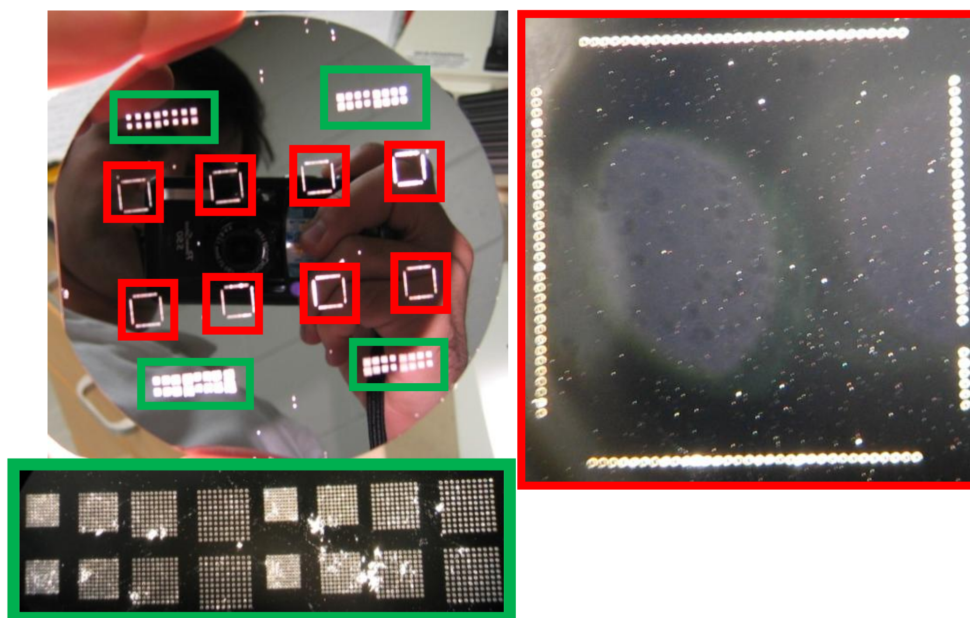


Figure 32: Wafer Feature Details, Post-CMP

This CMP step would be omitted if there were electronic patterns already on the wafer. The wafers were cleaned again using the modified RCA process before oxidation. Silicon dioxide was thermally grown in an oxidation furnace to allow for a conformal SiO_2 growth on all surfaces of the wafer including the via's sidewalls. A two hour H_2/O_2 oxidation at 1000°C

yielded a 6000Å thick layer of silicon dioxide (detailed oxidation settings found in Appendix I). This completed the TSV wafer.

4.3.2 Backing Wafer Fabrication

The backing wafer was processed using a standard (100) orientation, 500µm thick silicon wafer. Both 4 and 5 inch wafers were used during research; however the fabrication for both is identical. The backing wafers were first cleaned using the same modified RCA process used to clean the TSV wafers. The PR was coated with the same dehydration bake, primer and PR spin on procedure used for the TSV wafer's etching mask; however, this wafer was not exposed or developed. It was only softbaked for 2.5 minutes. 250Å of chrome was then E-beam deposited on the wafers for use as an adhesion layer for copper. However, it was later discovered that the chrome adhesion layer caused a high stress surface interaction with the PR which caused the chrome's adhesion to degrade with time and use, although this later proved to be beneficial when attempting to release the TSVs. Since this PR layer is a sacrificial layer intended only to temporarily provide wafer backing support, the easy removal of the copper seed layer from the backing wafer simplified the process.

Figure 33: Backing Wafer

4.3.3 Wafer Assembly Fabrication

The first step was the assembly of three components. The first two components were the TSV and backing wafers. The third component was the introduction of electrically conductive adhesive copper foil tape (Figure 34). The tape was the critical component in making this a successful process. The tape itself is a copper foil tape with a conductive adhesive. The copper is 0.0035” thick and ¼” wide. It is generally used to shield or modify circuit boards and for prototype wiring, but the conductive adhesive gave it a unique application in this process. The surface resistivity is roughly 0.01 ohms/sq. in. The tape connects directly to the copper seed layer to allow for electrode connection once the assembly is sealed.

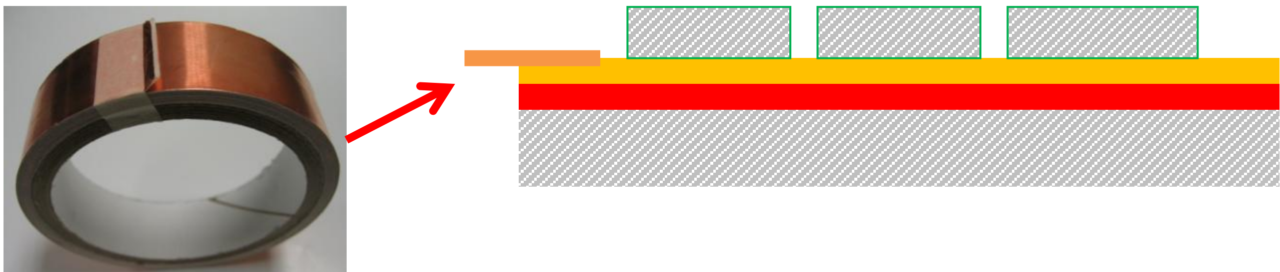


Figure 34: Copper Foil Tape

Once the connection was made, the front of the assembly was taped in a dicing tape fixture (Figure 35), and was then flipped and taped again forming a UV dicing tape seal around the assembly (Figure 36). The UV tape used was an Ultron brand UV dicing tape. Incisions were cut into the tape on the wafer surface to expose the vias (Figure 37). This allowed electroplating fluid to enter the vias.

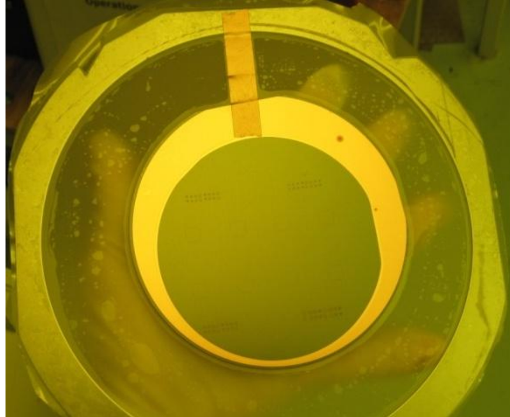


Figure 35: UV Sealed Wafer Assembly (Front)

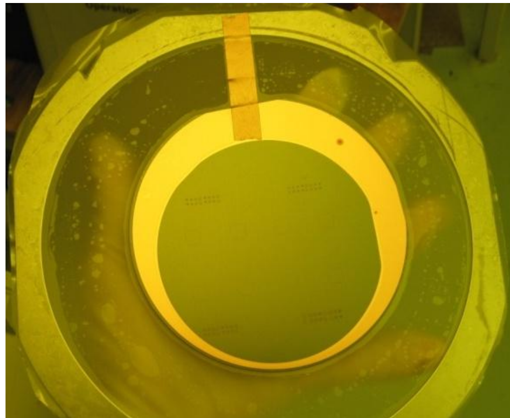


Figure 36: UV Sealed Wafer Assembly (Back)

Figure 37: Sample Dicing Tape Incision

If a 4" TSV is diced into quarters or halves, the backing wafer can also be 4". However, if a full wafer is to be plated, then a full wafer with a larger diameter must be used as the backing wafer. During the initial attempts, we offset the primary flats to allow copper tape to connect to the seed layer of two identically size stacked wafers, the problem we had with doing this was our 225µm thick TSV wafer was too thin. So once the assembly was sealed and pressure was applied to remove air bubbles from the tape, the TSV wafer would crack the thin TSV wafer. This problem didn't occur when we backed the TSV wafers on larger surface area backing wafers.

The assembly was then ready for electroplating. Initial plating was carried out in the beaker copper electroplating bath; however, the first results from a half wafer proved uncontrollable. The plating started at 20mA and was doubled every 15 minutes up to 160mA. The results were non-uniform across the wafer surface (Figure 38) and had significant overburden (Figure 39).

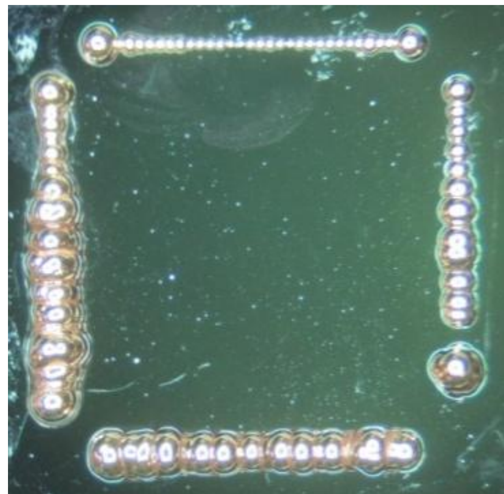


Figure 38: Varying TSV Overburden

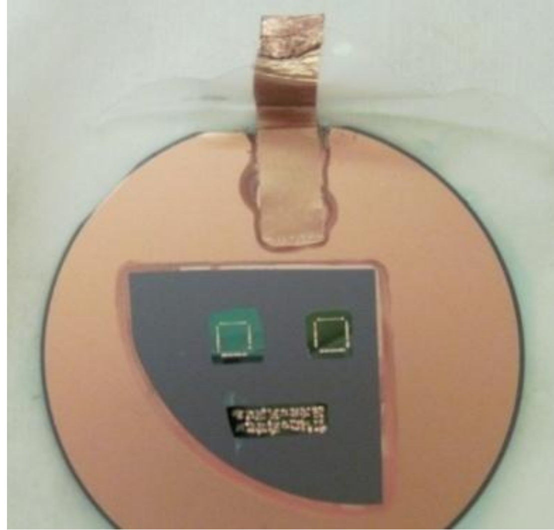


Figure 39: Complete Electroplating In Beaker

Thus, an alternative bath was used to provide more uniform plating in a more ideal bath. The bath was setup with the copper source[1] and the target wafer[3] connected in series through the solution with the sheer plate mixer[2] oscillating vertically at 6Hz in between the source and target (Figure 40, Footnotes 1-3).

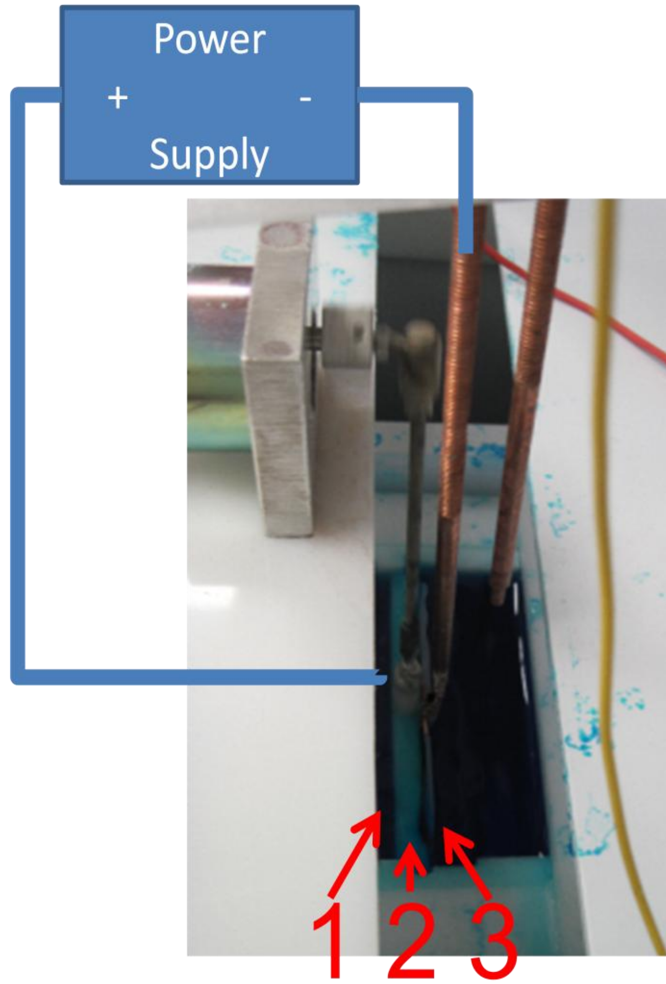


Figure 40: ADE Process Set-up

The plating of quarter wafers were completed at 10μA for 11-13 hours. They were occasionally removed and inspected under the microscope to verify plating. This verification was done using an optical microscope (Figure 41). Focus was set on the wafer surface to see if copper plating had reached the surface or not.

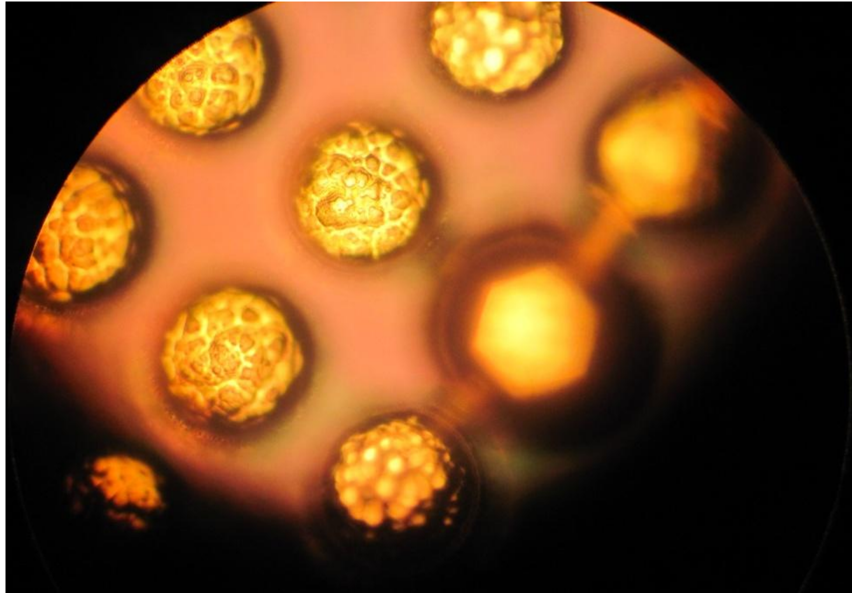


Figure 41: TSV Verification

Once verified, the wafer assembly (Figure 42) was disassembled, first the UV tape was removed by flushing the assembly with UV light (Figure 43), then the remaining TSV wafer attached to the backing wafer was placed in acetone (Figure 44) to remove the sacrificial PR layer. The front and back of the plated quarter wafers are shown in Figure 45 and Figure 46. A thin layer of the Cr/Cu seed layer is seen on the back of the wafer only on the bottom of the TSVs. The bulk of the seed layer came off easily since the seed layer was very thin and easily removable using only a plastic rod with a foam tip in acetone.

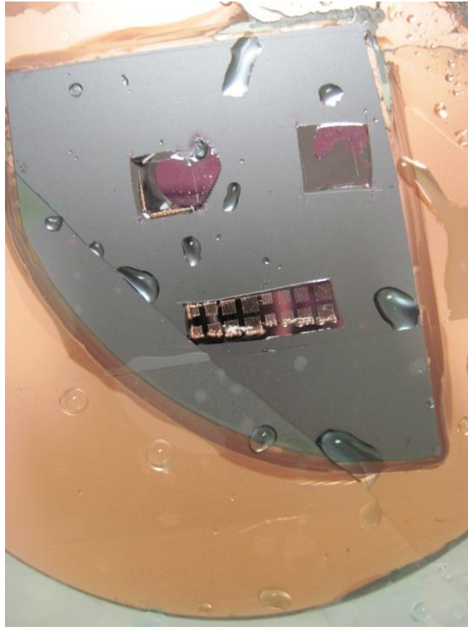


Figure 42: Wafer Assembly

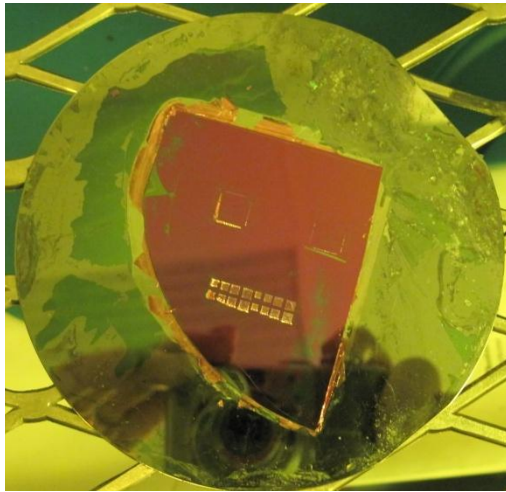


Figure 43: Wafer Assembly After UV Tape Removal

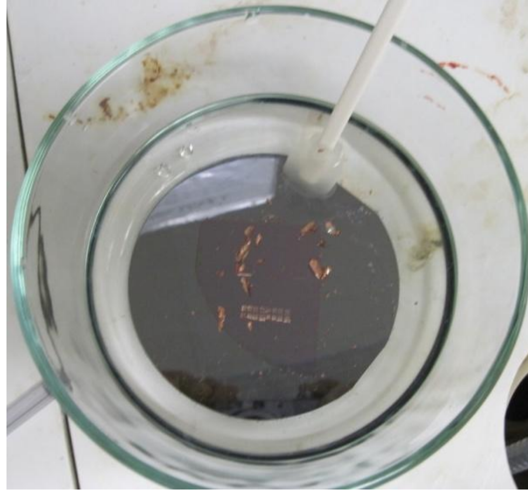


Figure 44: Acetone Removal of Sacrificial PR Removal

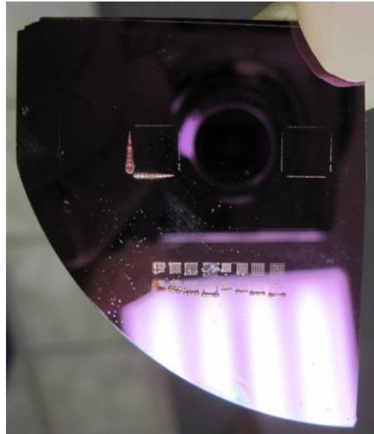


Figure 45: Wafer quarter Post-PR Removal (front)

Figure 46: Wafer Quarter Post-PR Removal (back)

Once the TSV wafer was released, it was placed in epoxy and cured overnight. It was placed such that when grinding was performed, the wafer would be perpendicular to the grinder and thus the TSVs would be ground along the Z-axis. The sample in epoxy was then background on a grinder using gradually finer sandpaper until it was ground to the center of the TSV. The TSVs results were then examined.

4.4 ADE Process Results

The initial beaker plating filled the vias completely, but did not plate uniformly across the wafer surface. We see a gradual height stepping across TSVs even within a grid. The amount of overburden is also too much in some areas whereas others are not completely filled. Although the voids are filled completely and if the plating was allowed to run to fill all the vias, a copper CMP could be applied and processing could continue. Thus, although it may be undesirable it is still workable.

Figure 47: Beaker Plating Result (1 of 2)

Figure 48: Beaker Plating Result (2 of 2)

The sheer plate mixing results (Figure 49 & Figure 50) were ideal. The vias are completely filled up without any voids. There are also no V-shape indentions in the top of the vias (a common side-effect of blind-via TSVs). These results are ideal and completed using a quarter wafer.

Figure 49: Sheer Plate Mixing Results (1 of 2)

Figure 50: Sheer Plate Mixing Results (2 of 2)

The current status of the ADE process allows for the processing of quarter and half wafers. Full wafers have been attempted, but due to limitations of the backing wafer and tape support it is currently not easily achievable. Thus, the ADE process can work well for prototyping applications, small sample TSV implementation, and for research. Modifications to this process are proposed at the end of this work for future work on this process.

Chapter 5: Blind-Via Process Design, Fabrication, and Results

5.1 Blind-Via Process Design

The design of the blind via device began with the TSV specifications of 100µm wide and 200µm deep vias. They were spaced 30µm edge to edge in the same patterns as described in the mask described earlier. Silicon wafers with a (100) orientation were chosen. Although, since the process is orientation independent, any wafer orientation could have been chosen. The wafers were 500µm thick in order to avoid the problem seen in the ADE process with wafers breaking. Thus the wafers were cleaned using the modified RCA process and a final spin-rinse-dry step (3-D representation of wafer cut-out shown in Figure 51). Once clean, the wafers were ready for photolithography.

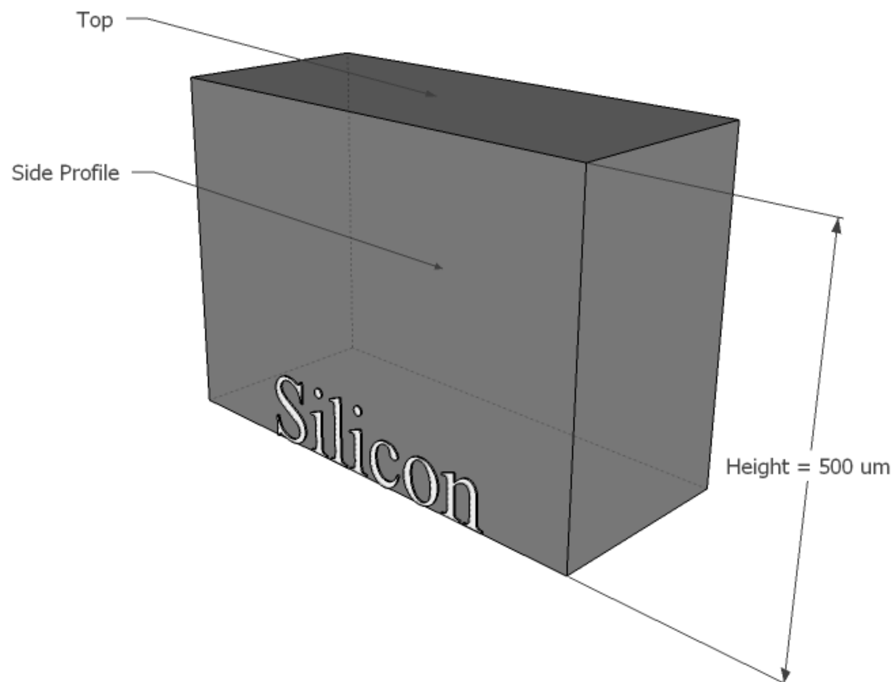


Figure 51: Silicon Wafer

Positive PR AZ P4620 was used as the masking layer for the DRIE. In the AMNSTC DRIE, this PR has approximately a 70:1 selectivity with Si. This, coupled with the PR's

maximum 24μm spin on thickness, led to the etching of any depth TSV. The photolithography process was performed in 5 steps:

1. Dehydration Bake: 120°C for 30 minutes to vaporize moisture, remove organics, and heat the wafer.

2. Primer: the vapor deposition of primer (for this research HMDS) was used to promote adhesion, which is critical during the forceful plasma etching of the silicon wafer.

3. PR: spin-on of PR (Figure 52), soft baked at 110°C for 2.5 minutes.

4. Exposure: Pattern exposure through the mask.

5. PR Development: (Figure 53) in a 2:1 mixture of DI water (200mL) and AZ 400K (100mL) developer. Wafer inspected for under/over developing.

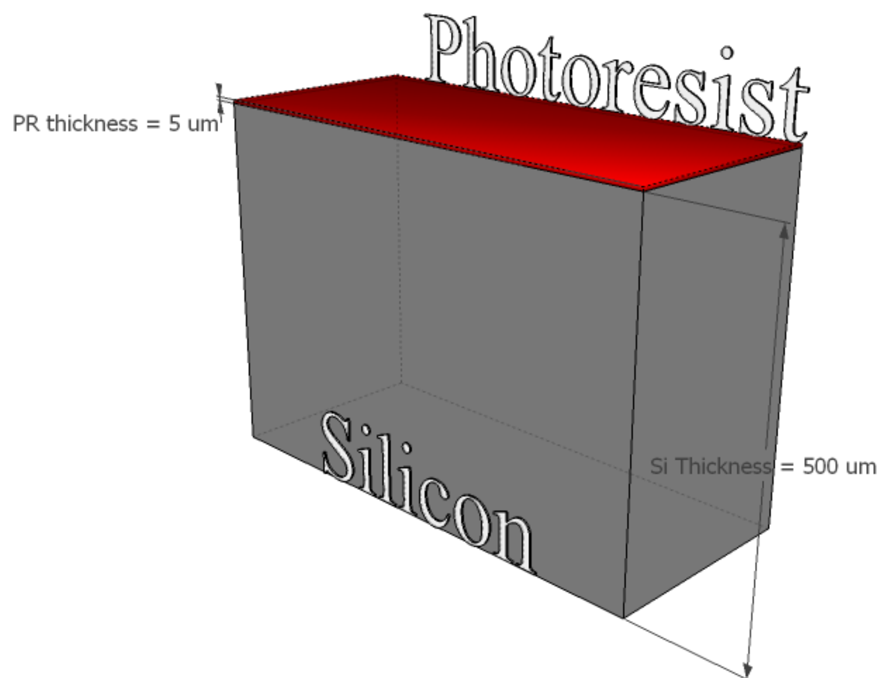


Figure 52: PR

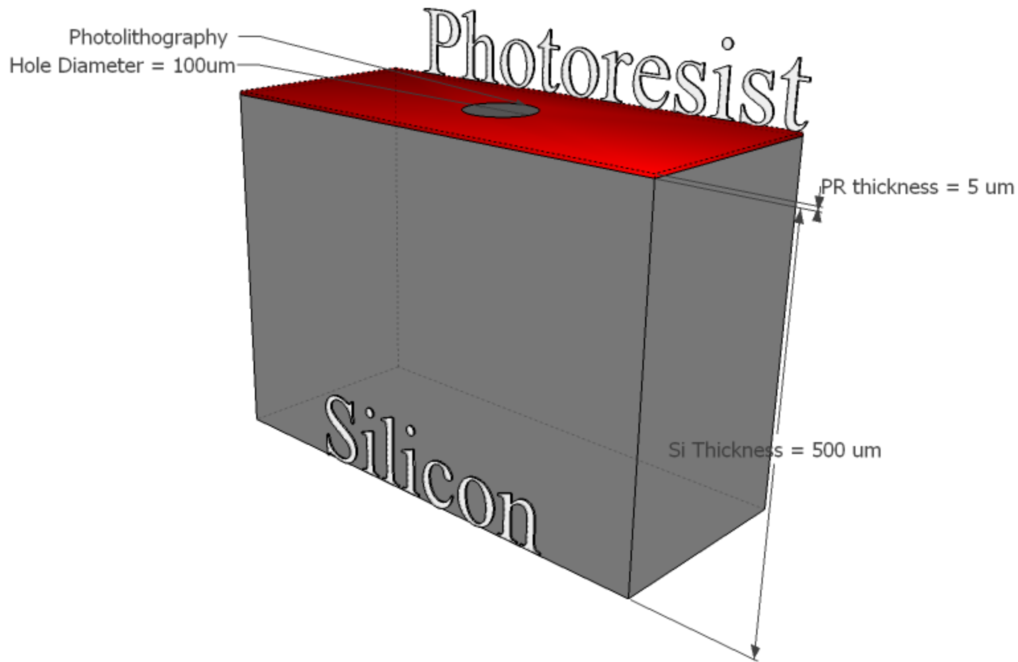


Figure 53: PR Development

With the PR's approximate 70:1 selectivity when DRIE etching Si, the desired PR thickness is calculated for a maximum depth (350µm) TSV using the following equation:

$$350\mu m\ silicon\ etch \times \frac{1\mu m\ PR}{70\mu m\ Silicon} = 5.00\mu m\ PR$$

The PR spin chart for AZ P4620 recommended a spin speed of 5,500 rpm in order to obtain a little more than 5µm of PR [55]. The ramp and time were chosen to be 500rpm/s and 30s respectively.

The wafers were soft baked according to the schedule in Table 7.

Table 7: Softbake Schedule

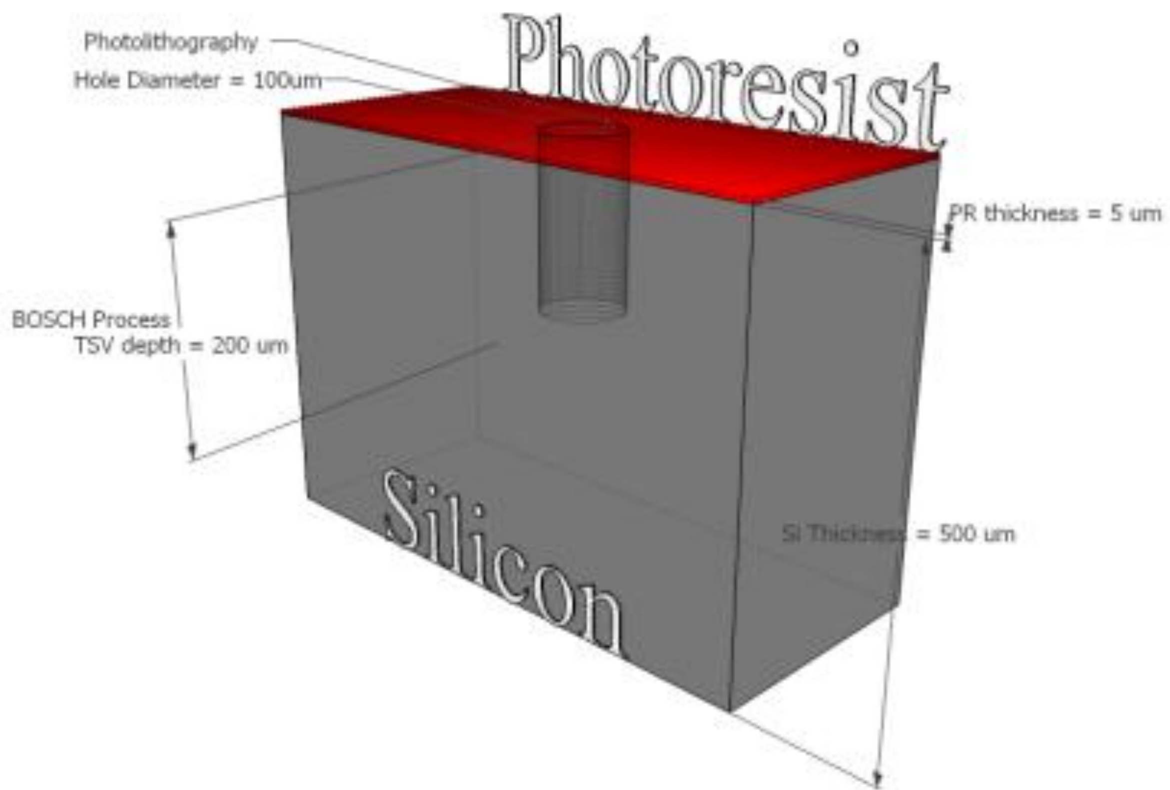
Hotplate Temperature (°C)	Wafer's Distance from hotplate (cm)	Time (s)
110	1.25	30
110	0	150

A multiple exposure process with rests built in was used as described in Table 8. The rests were introduced in order to prevent the flaring out of exposed PR.

Table 8: Exposure Schedule

STEP	Duration (s)	Exposure ON/OFF?
1	10	ON
2	30	OFF
3	10	ON
4	30	OFF
5	10	ON
6	30	OFF
7	10	ON

After the PR development was completed and the wafers were inspected, they were etched in the DRIE. The BOSCH™ process was used with octafluorocyclobutane (C_4F_8) as the passivation gas and sulfur hexafluoride (SF_6) and oxygen as the etching gases. The etch rates of the STS in this research ranged from roughly 0.6 to1.0µm/cycle. The wafer was etched to the desired depth (Figure 54a), and was cleaned using an IPA bath followed by an ultrasonic acetone bath (Figure 54b). The wafers were then put through a spin-rinse-dryer in preparation for oxidation.



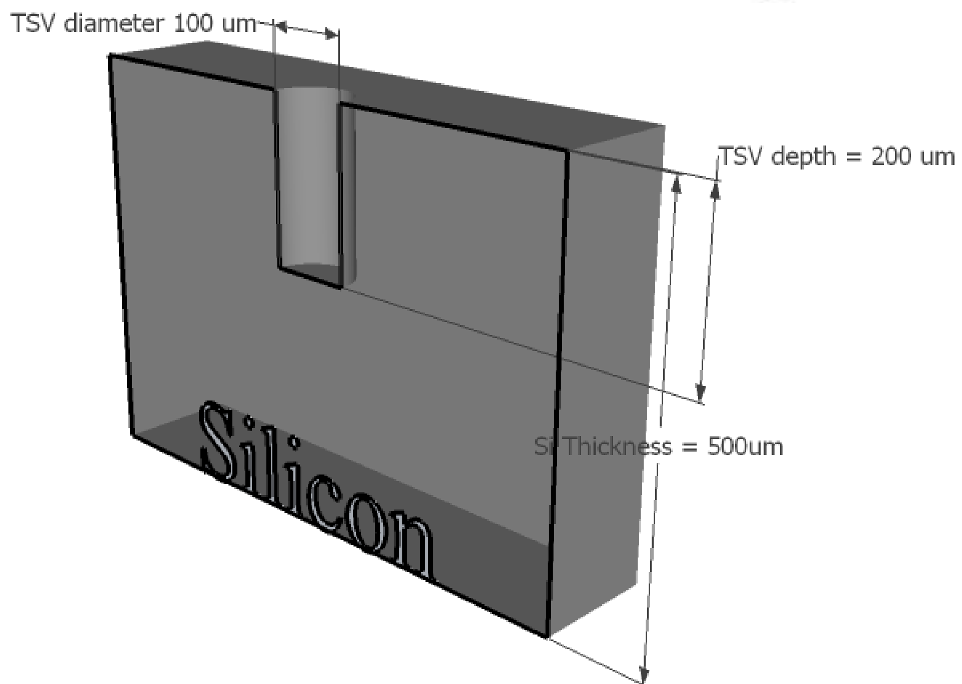


Figure 54: DRIE (BOSCH™ Process)

The electrically insulating oxide (SiO_2) was grown in an oxidation furnace to allow conformal growth on the Si wafer surface as well as the sidewalls and bottom of the via (Figure 55). The oxidation process produced a 6,000Å thick layer of silicon dioxide in H_2/O_2 reacted steam for 2 hours at 1000°C.

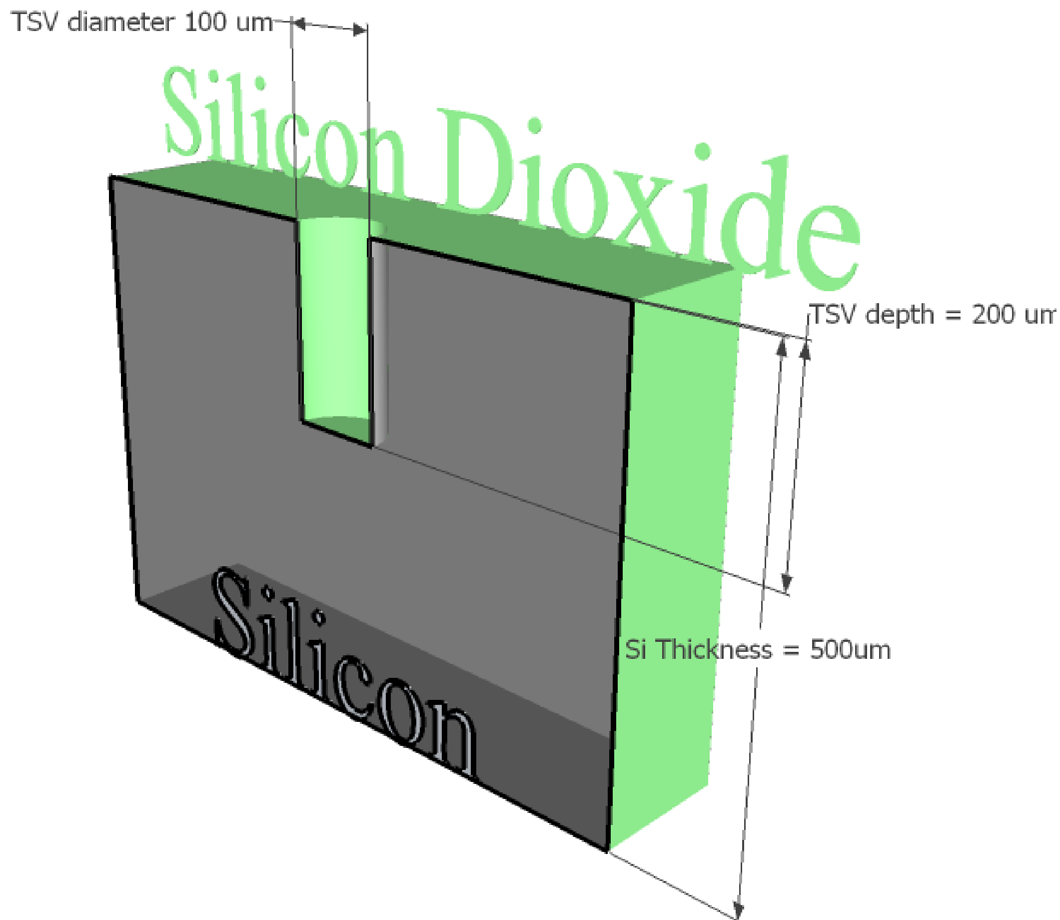
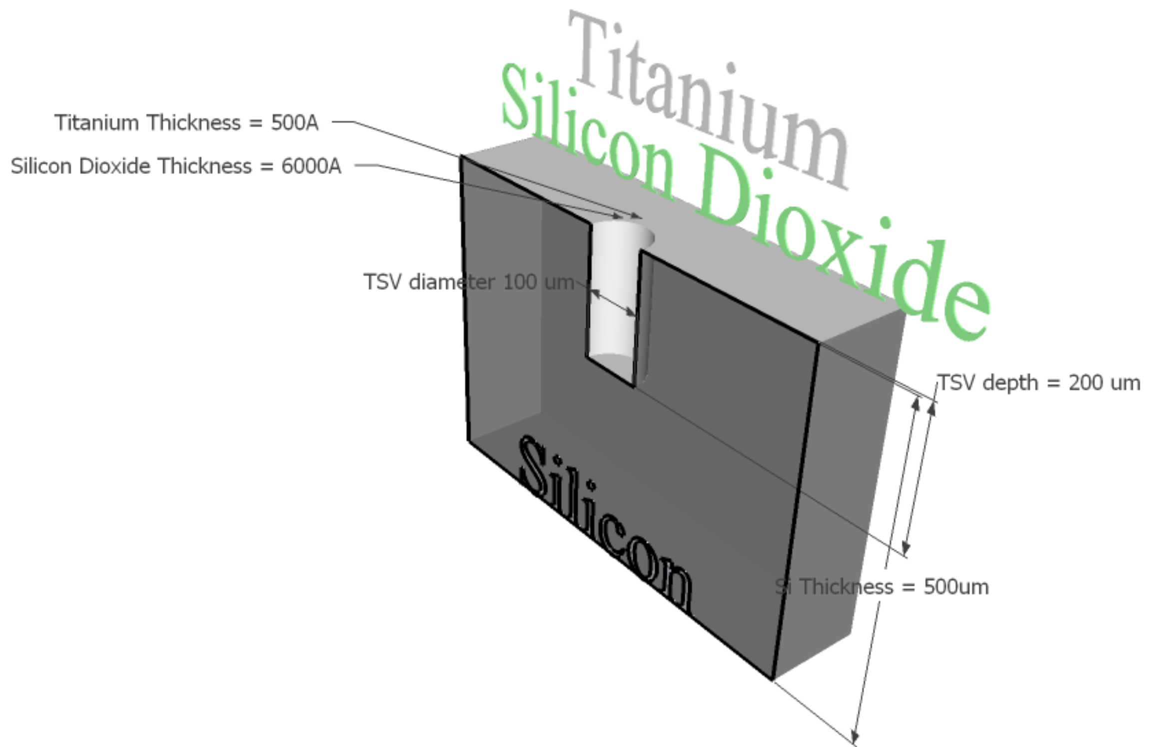


Figure 55: Oxidation

A seed layer was deposited using an electron beam evaporation system. Due to chrome's previous high stress results, an adhesion layer of titanium was deposited in its place. Without breaking vacuum, a thicker layer of copper was then deposited on the titanium as the seed layer for electroplating. In the E-beam system, two coatings were deposited for both the Ti (Figure 56a) and Cu (Figure 56b) layer. This is because the E-beam system deposits in a directional

manner, and thus a 180° rotation between the first and second depositions allowed us to eliminate shadowing within the holes. Thick layers of both metal depositions are required in order to obtain a substantial layer on the via sidewalls. During the e-beam process, the surfaces of the wafers are also coated with the Ti/Cu seed layer, which allowed for a suitable electrical contact point for electroplating. The vias are then filled with copper using an electroplating process (Figure 57). Sample devices were then cross sectioned for analysis using a dicing saw.



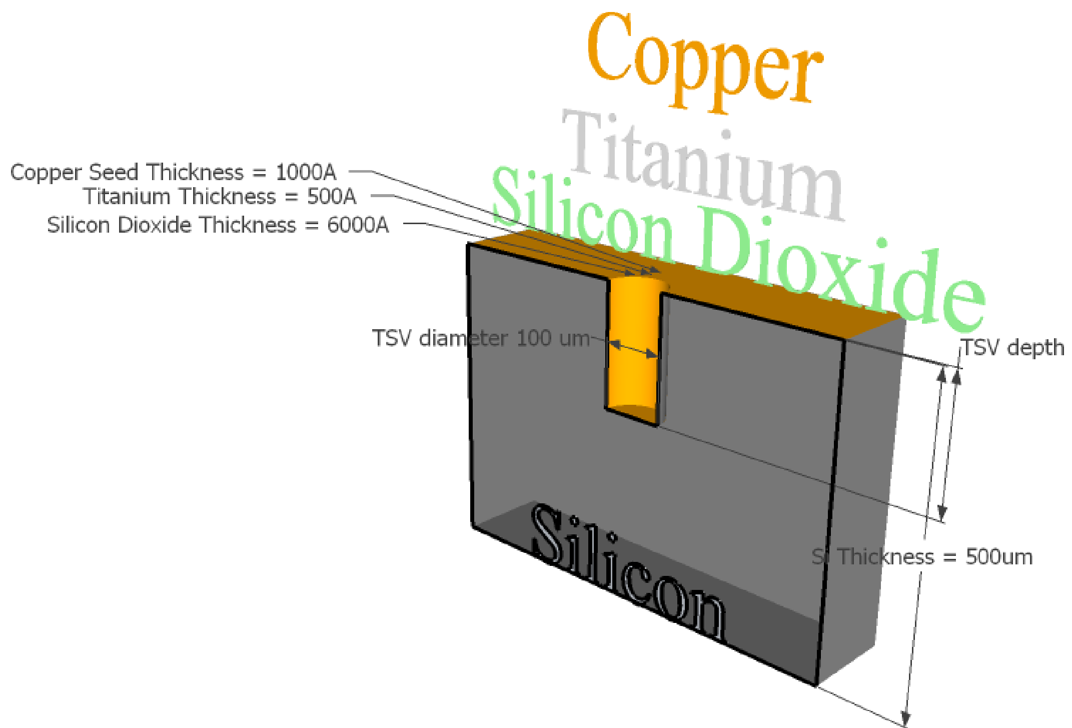


Figure 56: Copper Seed Layer

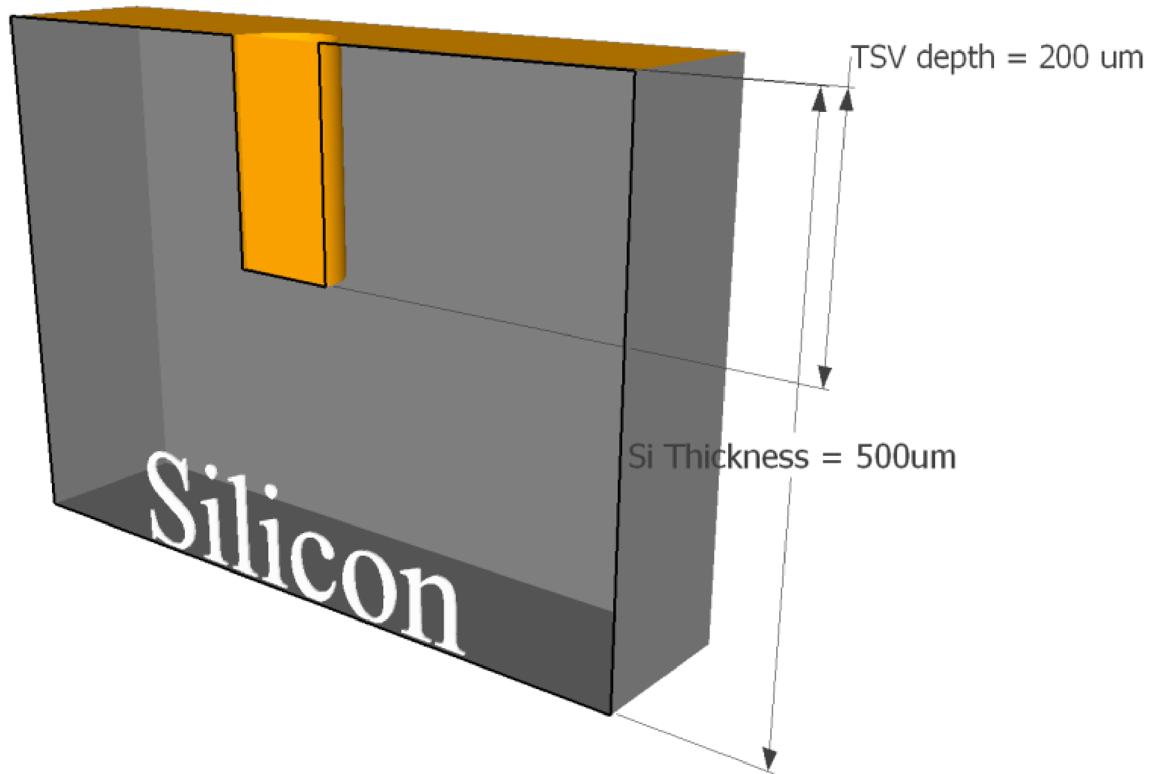


Figure 57: Copper Plating

5.2 Blind-Via Process Fabrication

The fabrication process described in Appendix B was used as a guideline for the blind-via TSV wafer fabrication. After inspection, the wafers were cleaned using the modified RCA process. With the wafers' surfaces free of hydrous oxide and oil, organic and metal impurities they were ready for photolithography. The dehydration bake at 120°C followed by the 10 minute room temperature HMDS vapor application, prepared the wafers for PR application. Although the RPM listed in the design (5,500 RPM) was found to be too fast for achieving the desired thickness (>5µm), it was found that a spin speed of 3000 rpm, ramp rate of 500rpm/s, and a 40s spin time were ideal at producing the desired >5µm thickness. The wafers were softbaked at 100°C first separated by ½ inch for 30 seconds followed by a 2.5 minute contact soft bake. Once

softbaked it was critical that the wafer be allowed to outgas for a period of roughly 1 hour, undisturbed. This prevented the PR from bubbling in later processing steps.

Once outgassed, the wafers were ready for exposure and development. Exposure was accomplished using the settings listed in Appendix C . It consisted of four, 10 second UV exposures through the photolithography mask in the Karl Suss MA/BA6 Contact Aligner. It was then developed in a 2:1 solution of H_2O:AZ400K, for 1 minute. The wafer was then rinsed in DI water and dried with nitrogen. The development was then inspected under the microscope (Figure 59). The development was inspected for cracks, which may lead to bubbling in the DRIE, and also for the quality of the PR development around critical features.

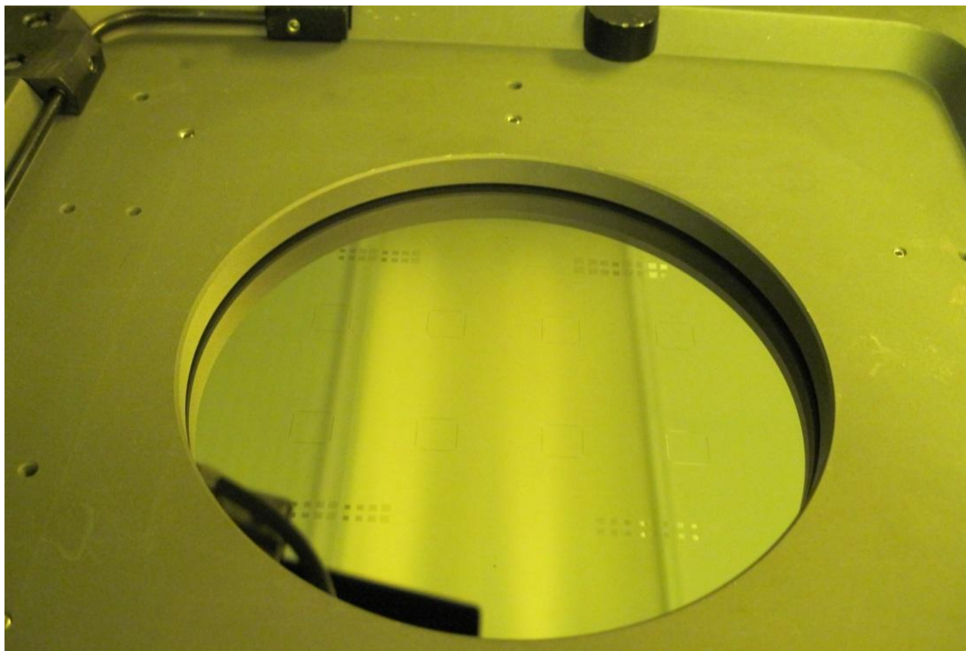


Figure 58: Wafer Mask In Contact Aligner

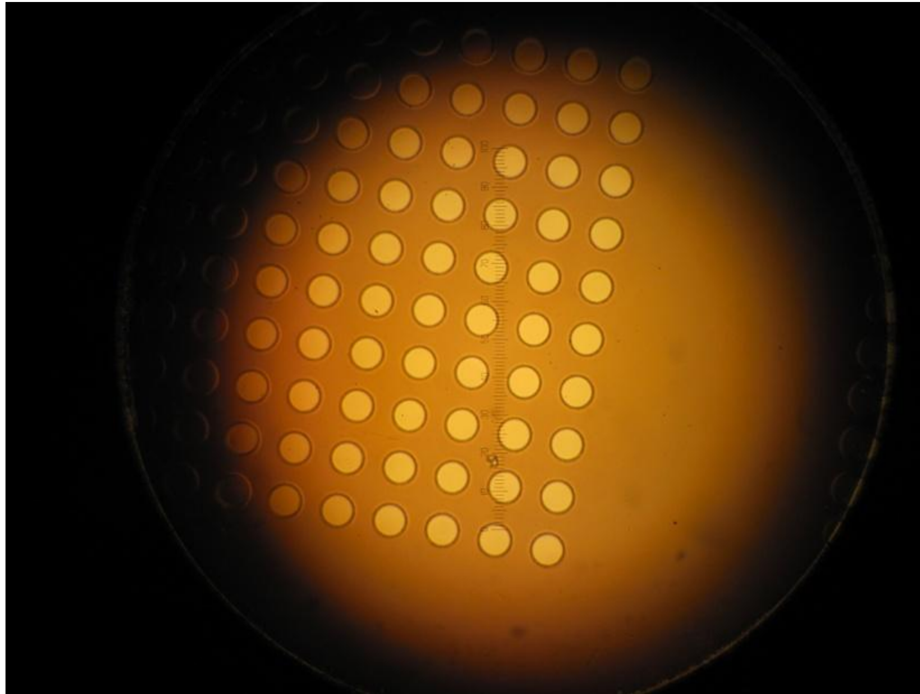


Figure 59: PR Post-Development Inspection

Once inspected the wafers were processed in the descum machine in order to ensure there was no PR residue in the bottoms of the via. If PR residue was present, this would be realized in the DRIE with varying depth vias. Since the PR has such a high selectivity towards silicon, the presence of any PR would offset the via depths across the wafer (or locally if poor development occured in certain areas). Once descummed the wafers were ready for the DRIE (Figure 60).

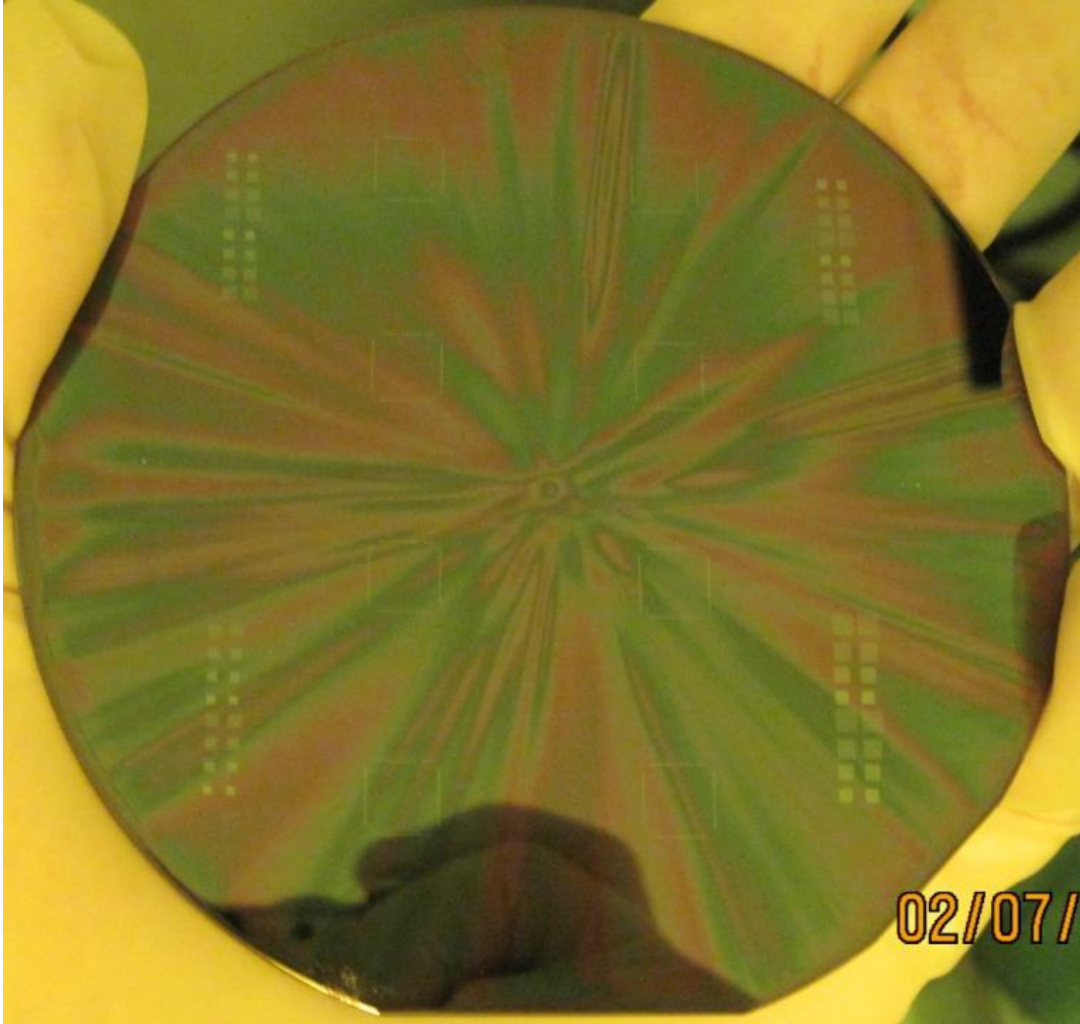


Figure 60: Descummed PR Wafer

The DRIE utilizes the BOSCH process, which alternates cycles of C_4F_8 passivation and SF_6/O_2 etching. This highly anisotropic etch yields the highly desired vertical sidewalls for TSVs. This enables the design to be much denser than with widened via tops. The DRIE etching of high aspect ratio features, requires a little more attention than simply placing the wafers in the machine and running them. The DRIE has a slightly off center focus for etching. Thus, the wafer is rotated every 1/4 or 1/3 of the procedure to rotate the wafer in a attempt to average out the non-uniformity. During this rotation the PR is inspected to see if it is showing signs of weakening from the process (bubbles, cracking, thinning, etc.). Once complete, the wafers are

cleaned in an acetone bath followed by an IPA bath. An ultrasonic shaker was used to disloge any remaining PR in the vias. They were then spin-rinse dried, in preparation for oxidation.

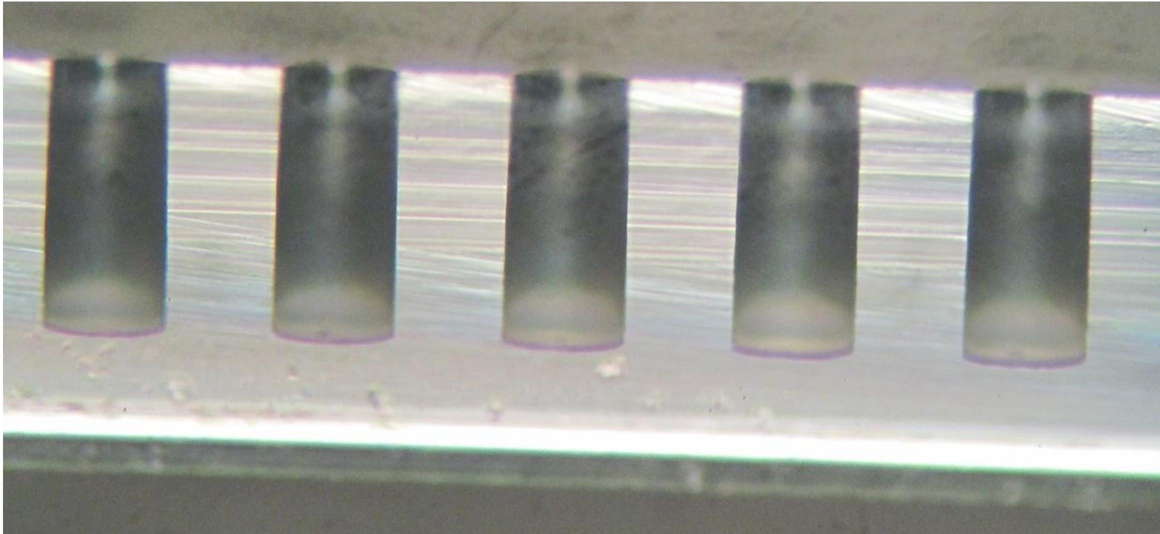


Figure 61: BOSCH Process Anisotropic Etch

The wafers were oxidized in an oxidation furnace to allow the conformal growth on both via sidewalls and along the surface of the wafer. This electrical insulator prevented the shorting of vias through the substrate. A wet oxidation process was used (described in Appendix I) to grow 6,000Ǻ of silicon dioxide in a hydrogen and oxygen reaction from 2 hours at 1000℃. The wafers were then immediately E-beam deposited to coat the seed layer from which the electroplating would start from. If the wafers could not be immediately E-beamed, then a descum step was introduced. The seed layer was a series two metal layer coatings. The first layer was a titanium adhesion layer followed by copper. The reason an adhesion layer is useful here is because copper creates a high stress surface with silicon dioxide and inhibits a proper adhesion to the surface and sidewalls. The titanium adheres well to both the silicon dioxide and to the copper. The deposition was performed by first depositing the titanium and copper once, then rotating the wafers 180° to coat the locations shadowed by the first deposition. 500Ǻ of titanium

was deposited for adhesion while 5000Å of copper was deposited in order to obtain a thick layer on the vias' sidewalls for plating.

Figure 62: Wafer Post-Copper Deposition

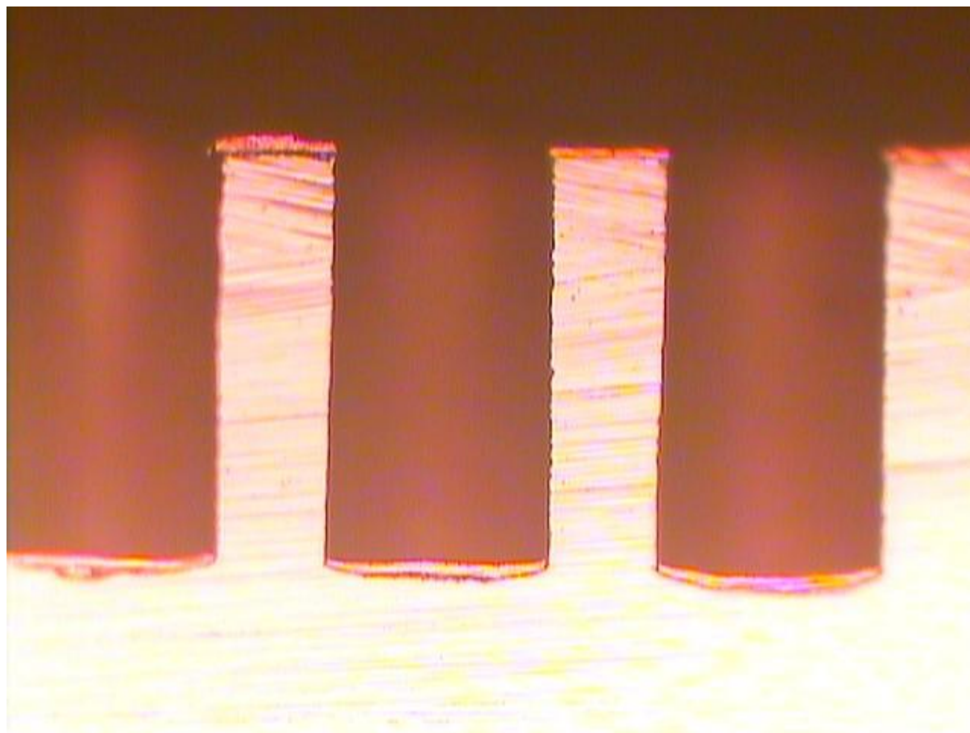


Figure 63: Wafer Cross-Section Post-E-Beam Deposition (Edge Focus)

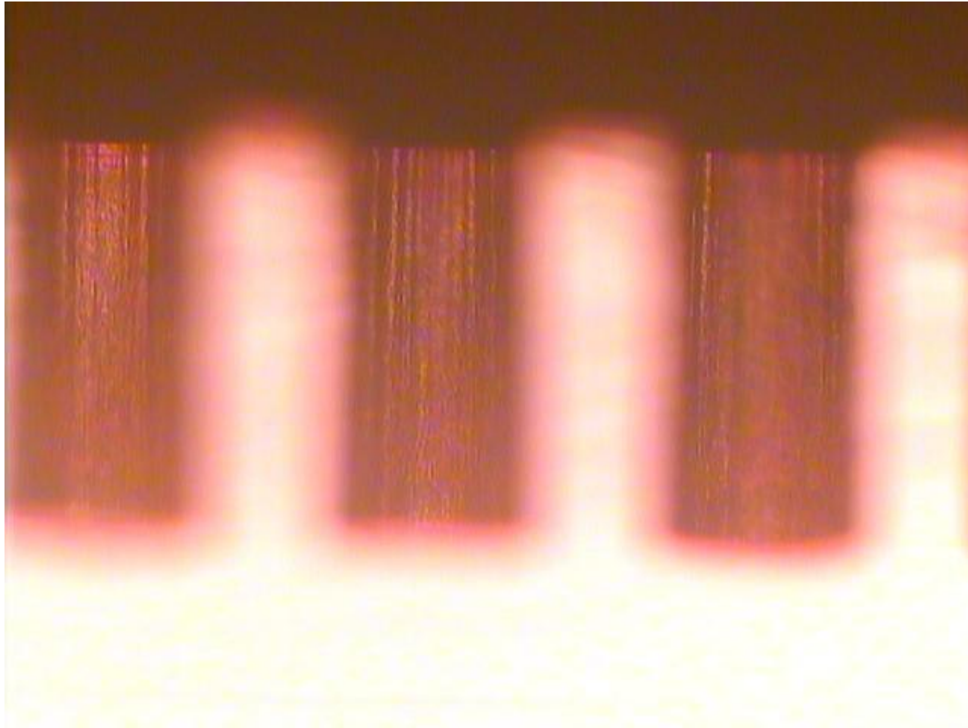


Figure 64: Wafer Cross-Section Post-E-Beam Deposition (Sidewall Focus)

With all surfaces of the wafer covered, copper electroplating was the next step. This electroplating was performed in the custom designed bath using the blind via wafer holder. However, before insertion into the wafer holder, the wafer was pre-wet in a vacuum chamber that filled the vias with IPA (see section 5.10). Once pre-wet the wafers were quickly secured in the wafer holder shown in Figure 65. The dotted line represents a metal ring that is used to connect to the wafer's surface which is sealed away from the plating solution and connected to a wire that exits from the front of the holder and connects to the power supply's negative terminal.

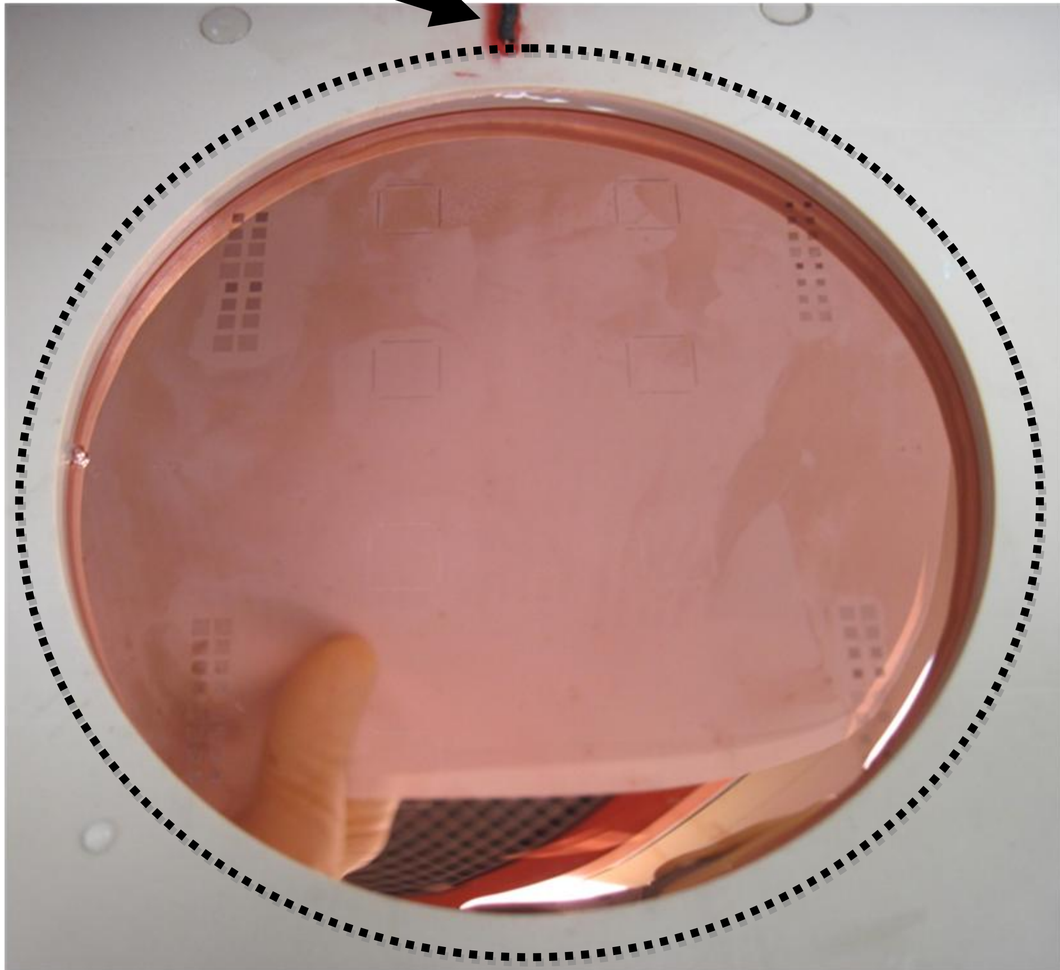


Figure 65: Wafer Secured In Wafer Holder Post-Pre-Wet

Once connected, the wafer holder was placed in series with the copper source in solution. The plating current was doubled from 20mA every 2.5 minutes all the way to 160mA where it remained constant for 7-8 hours. On a four inch (~10cm) wafer this means the applied current (160mA) is roughly .5mA/cm^2. This is a lower current density but ensures a dense copper fill, and with proper chemistry adjustments can be increased for faster TSV development. The pump and the sheer plate mixer (6Hz) are both in operation during this plating period. The assembly

was periodically taken out (Figure 66) and verified for plating. When taken out, if the wafer remained exposed to air and began drying the solution from the wafer surface, oxidation would occur. Thus an immediate rinse (or spin-rinse-dry) assisted in inhibiting significant oxidation during intermittent periods. Wafers were inspected under an optical microscope to see whether or not plating was occurring. One main indicator that plating was not complete is the pinhole feature signifying the via is still plating (Figure 68). Thus plating was continued until complete, which was verified by focusing on the hole to make sure the hole is filled (Figure 69). The U shape indention is natural for blind-vias, and can be nearly eliminated at the cost of excessive plating overburden on the surface.

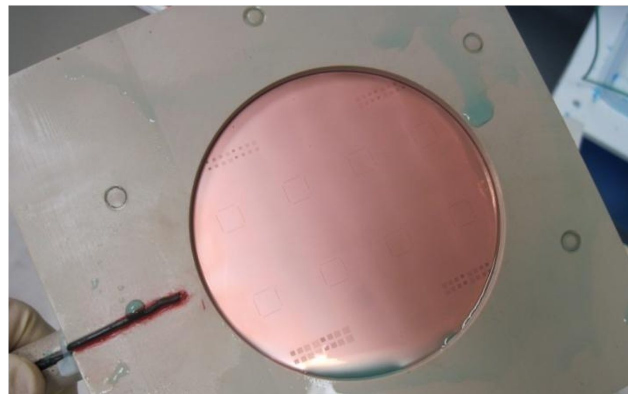


Figure 66: Wafer Removal For Inspection

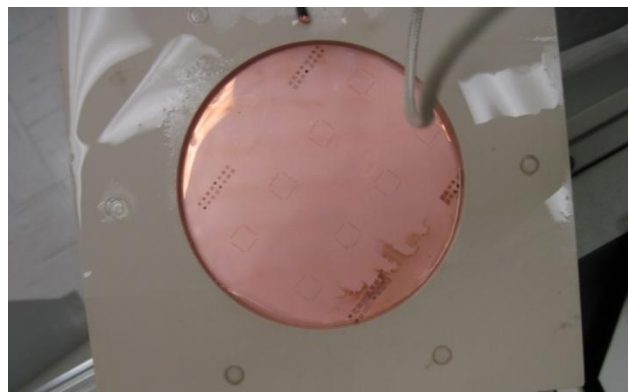


Figure 67: Wafer Removal For Inspection, Surface Oxidation.

Figure 68: Via Inspection.

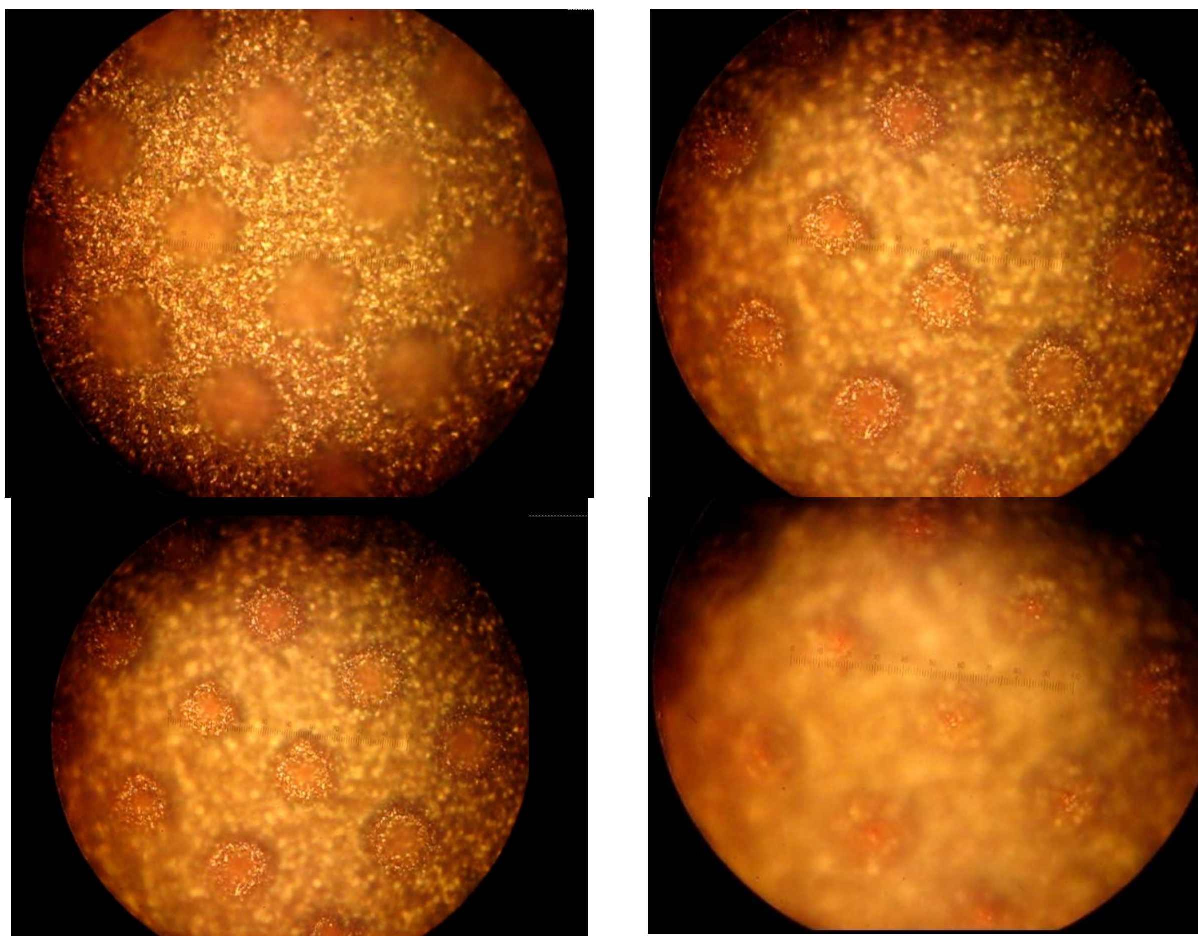


Figure 69: Via Completion Focus Verification (Top Left->Top Right->Bottom Left->Bottom Right)

5.3 Blind-Via Process Results

During the plating of the full wafers, some wafers were taken and diced to examine a cross-section of the actual plating that was occurring. Wafers were cross-sectioned as they neared completion. One wafer was cross-sectioned in the middle of its plating session using the dicing saw and it was apparent that the via was exhibiting a conformal fill from the bottom up (Figure 70). The over-burden on the surface was limited compared to the initial seed layer deposition.

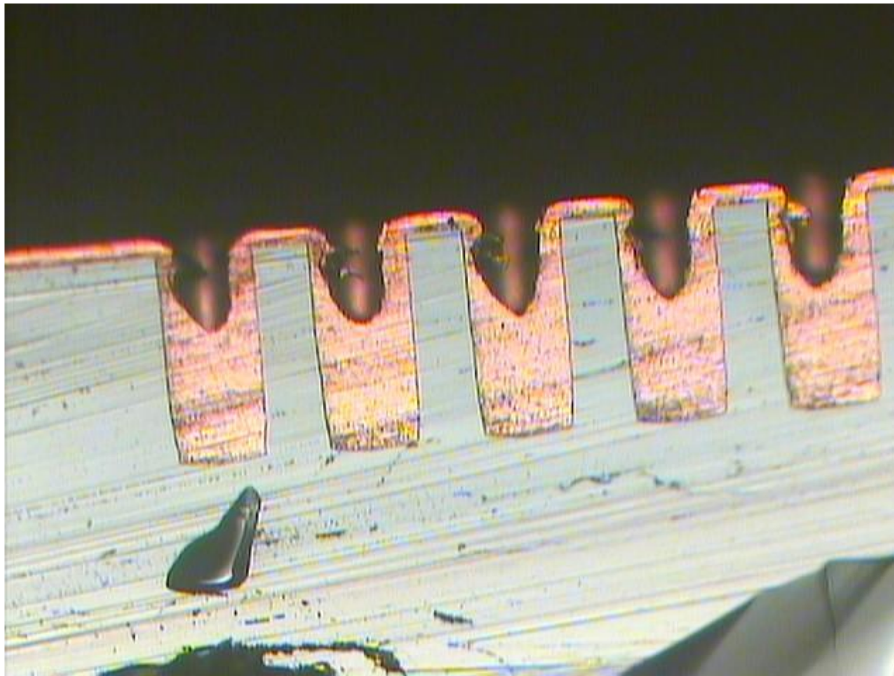


Figure 70: Via Conformal Filling Verified (Left Half of Wafer)

One feature described earlier in literature review of this work was the one sided overburden on the neck of the TSV. This phenomenon was seen during the plating of this wafer. This was due to the fluid flow across the tops of the vias. Figure 70 shows the left half of the wafer, and with the pump flushing the surface of the wafer perpendicularly the solution hits the

center and rolls off the outer edges. This is why the indention in the plating is seen on the opposing side for the TSVs on the right half of the wafer (Figure 71). Although since the bottom up-fill mechanism is working properly, the slight indention is not critical.

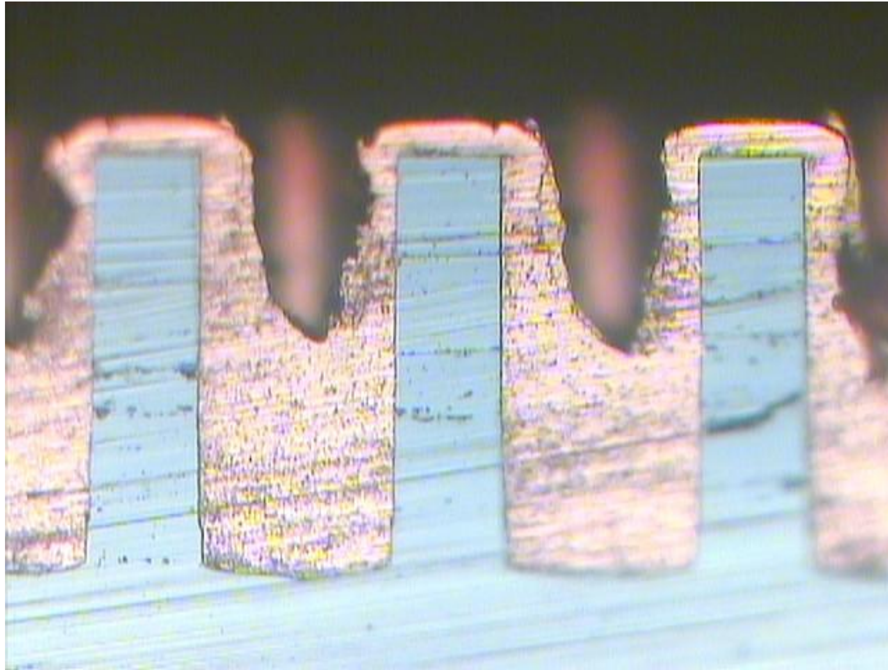


Figure 71: Via Conformal Filling Verified (Right Half of Wafer)

Another wafer was sectioned once plating was complete and the via fill was ideal. First the cross-section was done exactly in the center of the via (Figure 72). The cross-section of the via was also flawless (Figure 73). It was void free. It had a slight U-shaped indention at the mouth of the via, but the bottom of the U was above the top of the silicon wafer. Thus, if this wafer were to be copper CMP'ed, it would have filled vias necessary for developing pads on the surface.

Figure 72: TSV Cross-Section

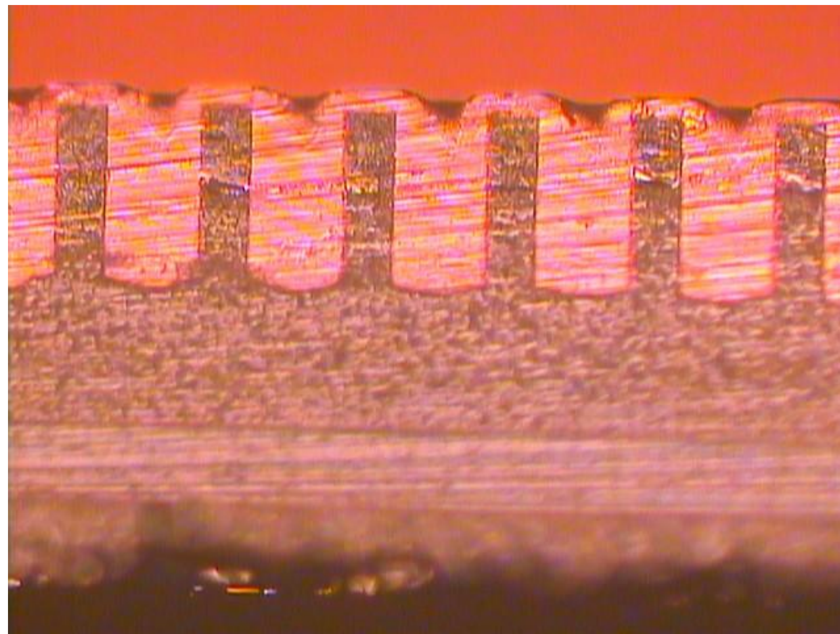


Figure 73: Conformal Via Fill

5.4 PR Bubbling

The PR bubbling mentioned earlier was mainly due to gasses trapped in the PR attempting to surface under varying pressure changes (especially during DRIE). The first few wafers resulted in extreme bubbling around the edges of the wafer. PR AZ 5214 was used in an attempt to brush up the edges, but the bubbles only surfaced again from the new interface of the etched silicon and the new PR (Figure 74 and Figure 75). Thus, it was later discovered that a waiting period of roughly 1 hour post-softbake yielded high quality PR applications that could endure the DRIE process.

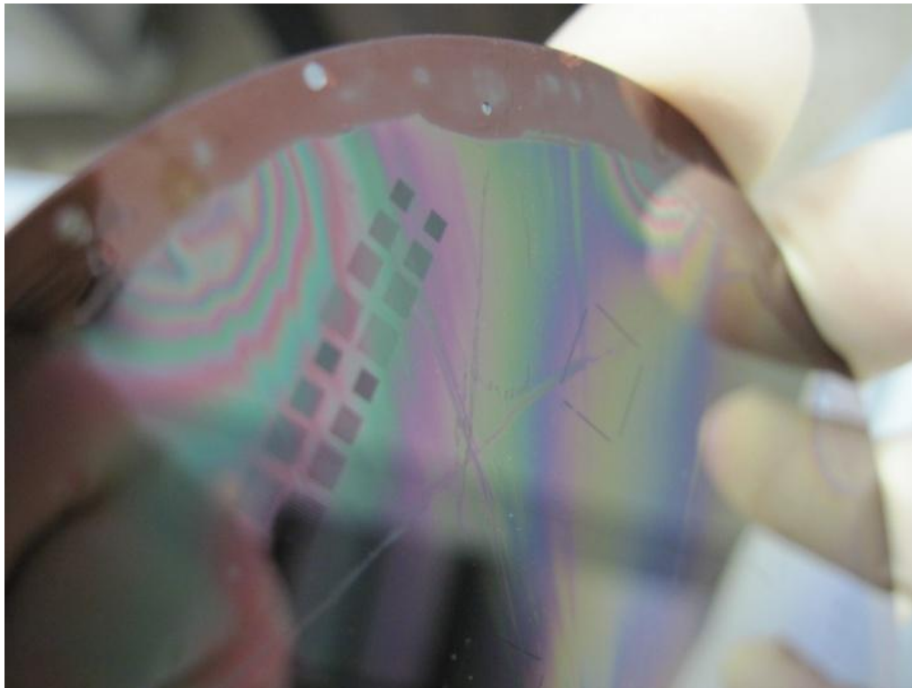


Figure 74: PR Bubbling on Edge of Wafer (1 of 2)

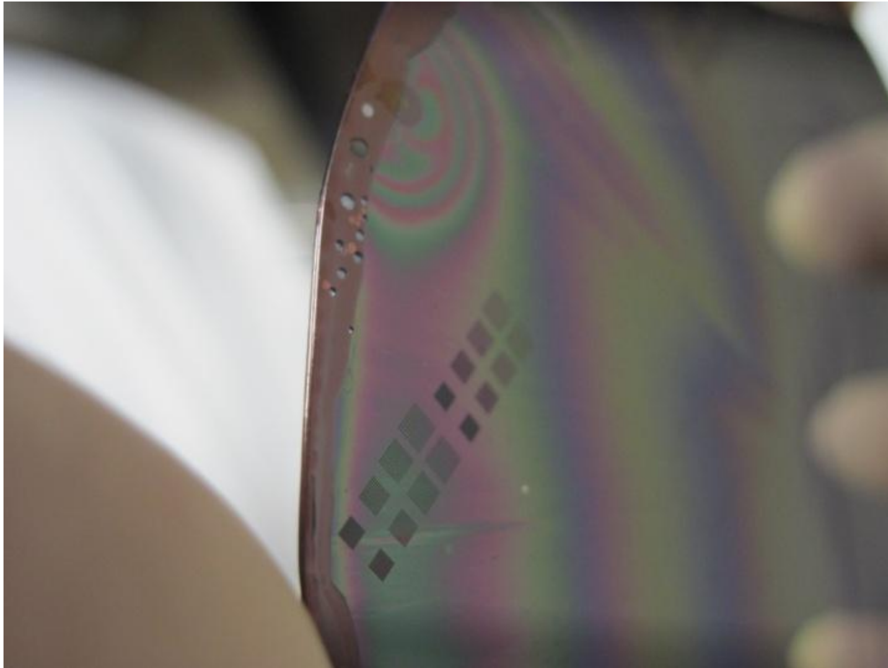


Figure 75: PR Bubbling on Edge of Wafer (2 of 2)

5.5 Mask Cleaning

One issue with the masks was their ability to hold a static charge and thus attract debris from the air. This introduced problems when wafers were being exposed since either the debris blocked light from fine features (via edges), or embedded itself within the PR when the contact aligner did a hard contact. Compressed air was used to blow off the mask prior to exposure to ensure it was clean.

Another problem that occurred was the sticking of PR to the mask during hard contact. Since the PR was only softbaked and undeveloped, it was soft and tended to stick to the mask and leave a residue. The PR residue on the mask was tedious. Removal required the use of a lint-free paper towel and acetone; however, too much acetone would streak the mask causing masking problems again. Once cleaned, the mask was blown with air to ensure cleanliness.

5.6 Via Etching Sidewall Characteristics of Low Power vs. High Power etching

In this research a comparison was made between the two methods of etching listed in Appendix D and Appendix E . The set-up in Appendix D was for low power (12W) and Appendix E was for high power (18W) application to the wafer chuck. It was found that higher power applied to the chuck yielded smoother sidewalls (Figure 77), whereas the lower power caused deep vertical striations (Figure 76).

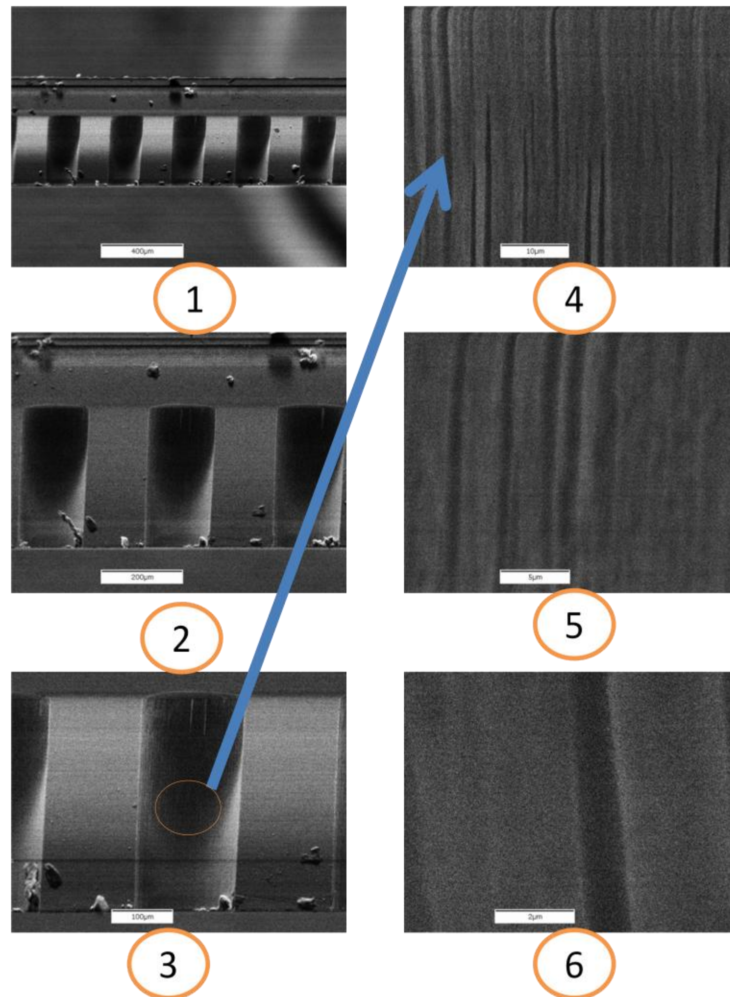


Figure 76: 12W Deep Striations

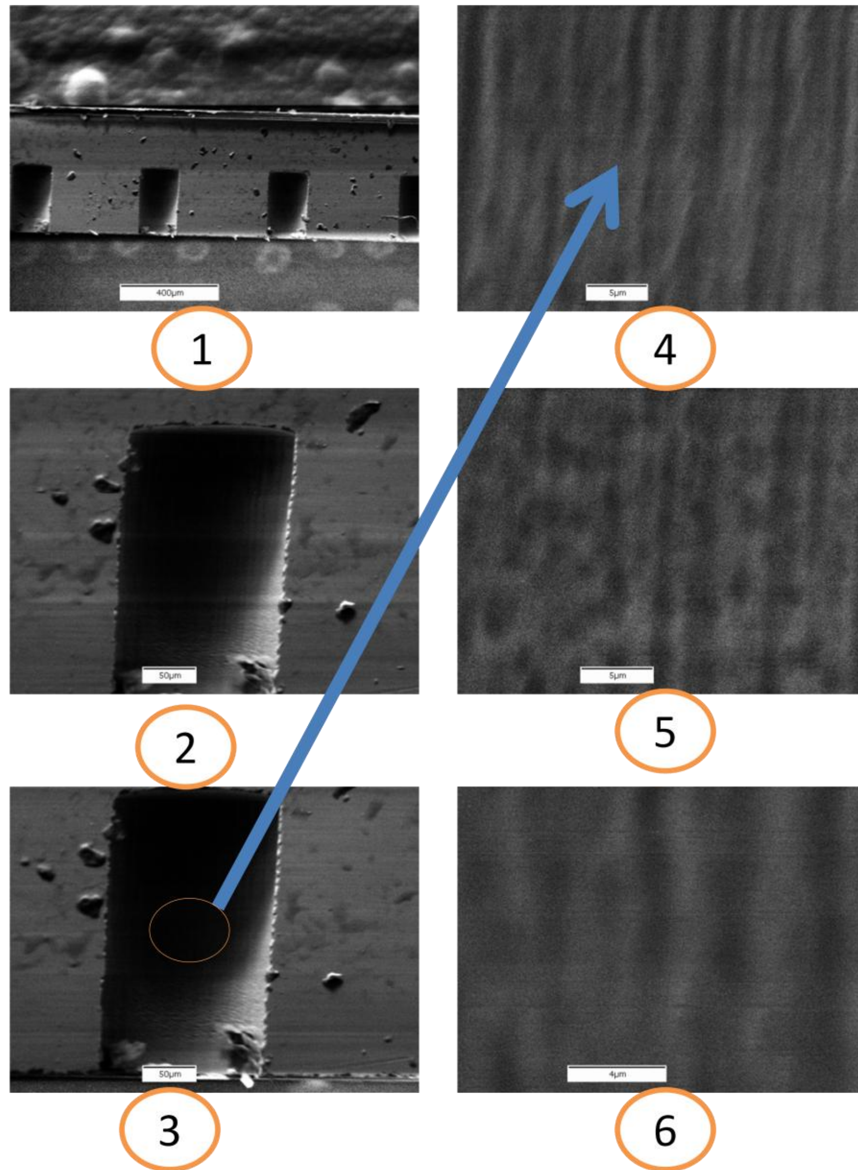


Figure 77: 18W Smoother Shallow Striations

5.7 Chamber Conditioning

Chamber conditioning was critical in maintaining a standard etch rate as well as for controlling uniformity. A variance in the etch rate (~0.05µm) was exhibited when etching the TSVs. This may seem insignificant, but with wafer processing occurring for hundreds of cycles this could potentially lead to ~20µm of variance. In addition to the variance, a phenomenon known as black silicon was observed. After the chamber had been cleaned using the program in

Appendix H , the vias were notably bright (exhibiting a silicon color luster). However, a wafer that has been processed without prior chamber cleaning and etched after several runs of other wafers, exhibited a dark color in the vias. This was caused by the development of black silicon, which is a silicon surface that exhibits low reflectivity due to high absorption of light caused by tiny spike-like structures on the etched surface[56].

5.8 Seed Layer Coverage

Seed layer coverage is critical for obtaining defect free TSVs. Any deformities in the coverage can yield to drastic effects such as seed layer peeling or sidewall/via-bottom void formation. Since the E-beam does exhibit slight directionality, it tends to build up on surfaces perpendicular to the copper source (via bottoms and wafer surface). This limits the sidewall deposition and requires thicker seed layers to be deposited in order to obtain proper sidewall coverage (Figure 78). Via tapering is one method that can be implemented instead of thicker E-beam coatings; however, if an ideal seed layer is truly desired, a MOCVD seed layer would produce ideal results for the TSVs. Due to the lack of an MOCVD machine, this was not an option for this research.

Figure 78: E-beam Deposition of Seed Layer

5.9 Via Tapering

Via Tapering is a common way to increase the sidewall slope of vias in order to deposit more seed layer on the sidewalls. One such method was described in detail by a group working for the Institute of Microelectronics (A*STAR) in Singapore. They detailed two processes (post-etching) that could be utilized to widen the vias opening. The first additional step was a taper procedure which widens the top and center of the via (the widest portion being the via opening). The DRIE settings for this procedure are described in Appendix F . The second additional step is a via rounding step which removes the defects from the first two steps [57]. This via widening approach was attempted but controllability of the process was difficult, especially with such small feature spacing (30μm). Some samples from the trials are shown in Figure 79, Figure 80, and Figure 81. The under etching of the PR was used as a measurement tool for the amount of via widening. The small feature size required for this project, the uncontrollability of the process and irregularity of the etch prevented us from using this method moving forward.

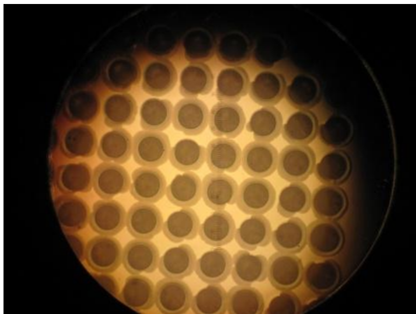


Figure 79: Irregular Via Widening

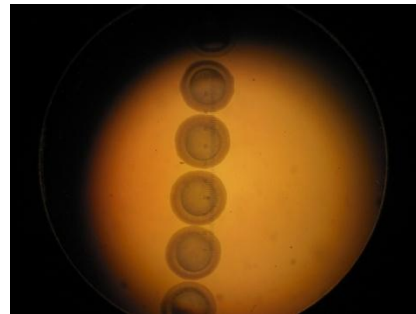


Figure 80: Narrow Spacing After Via Widening

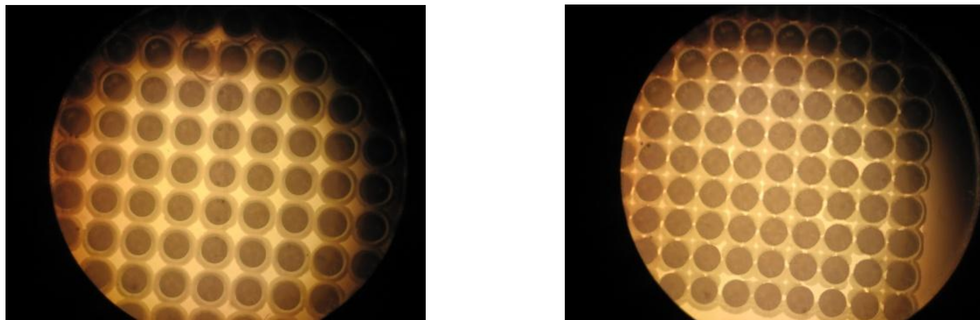


Figure 81: Excessive Via Widening

5.10 Wafer Pre-Wetting

One of the main problems associated with the blind via method was a proper pre-wet. This was especially important for the high aspect ratio TSVs. The act of pre-wetting introduces a solution into the seed-layer deposited vias to allow for fluid exchange once introduced into the plating bath. The first method that was attempted was the IPA first method described earlier. This pre-wet took significantly longer and was not always successful at removing all the air trapped within the vias. The wafer submersed in IPA may have trapped air within the vias while inhibiting the bubbles from evacuating the vias through the IPA. The results of a poor pre-wet are detrimental in future plating and processing as the air trapped within the vias does not escape and prevents plating from occurring in those areas (Figure 82).

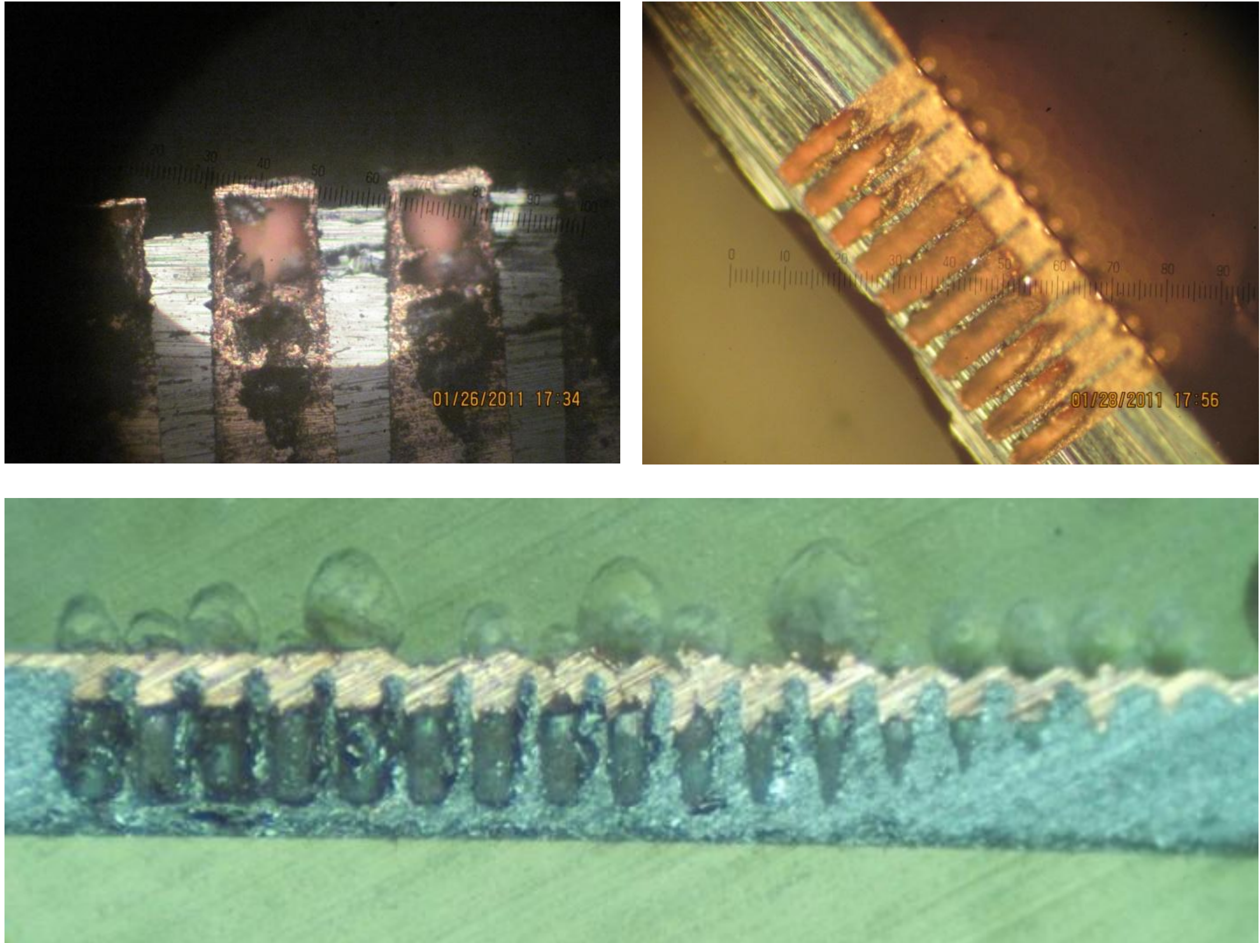


Figure 82: Poor Via Pre-Wet Results

The use of vacuum before introducing IPA yielded improved results as well as shorter processing time; however, even the vacuum before IPA introduction didn't completely eliminate the need for waiting for the air to bubble out. When pre-wetting (using either process) there is a simple color indication of whether or not the vias have been pre-wet. If the wafer is not pre-wet properly, the resulting wafer either has bubbles emerging from the vias or the vias are the same color as the surface copper (difficult to distinguish). A wafer in the process of purging its vias of air is shown in Figure 83 and the resulting properly pre-wet wafer is shown in Figure 84. The resulting plated TSVs described in the blind via process was a direct result of this proper wetting technique.

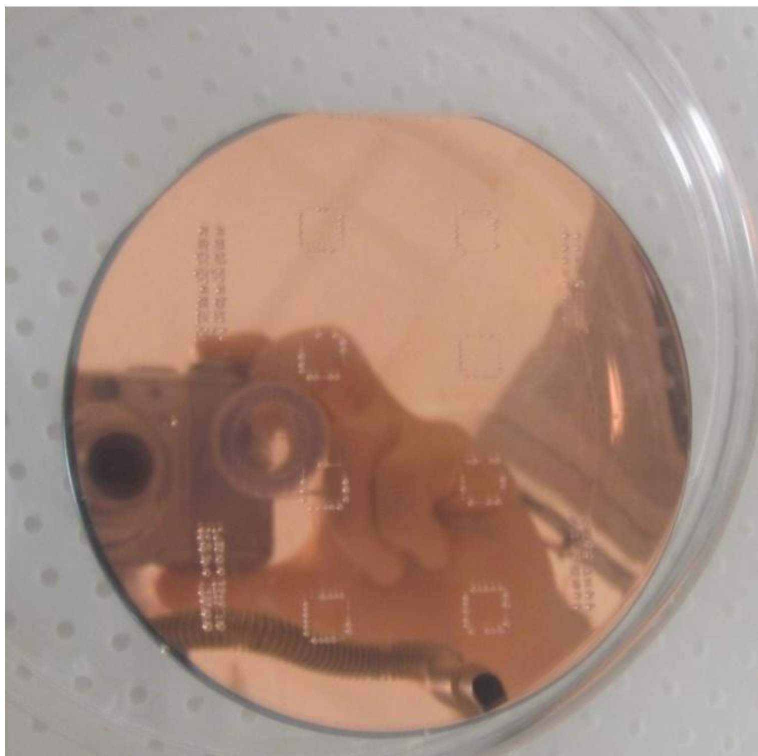


Figure 83: Air Evacuating Vias Under Vacuum in IPA

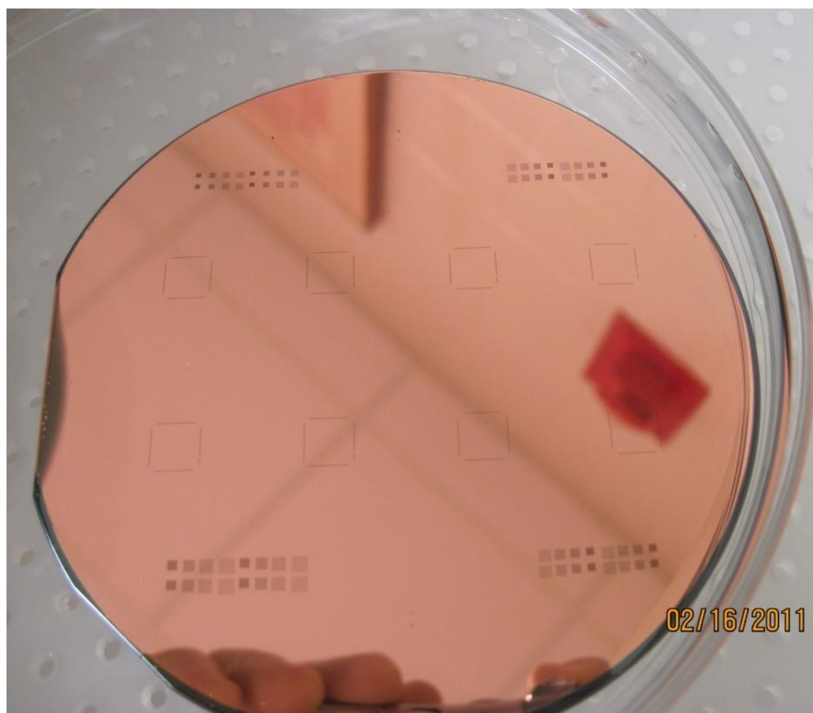


Figure 84: Fully Pre-Wet Wafer (Darkened Via Openings)

Chapter 6: Conclusion and Recommendations for Future work

Two methods were used to develop solid copper filled TSVs. The ADE process was introduced in this research which produced solid filled copper TSVs without defects, voids or indentions. The blind-via method was also used in this research, which also produced solid copper TSVs, but with a slight indention at the top. Although, the blind-via's indentions are common place for this type of fabrication and can easily be polished away. Both methods were successful in developing solid copper filled TSVs. The current status of the ADE process allows for TSVs to be developed in silicon without depositing metal on the surface of the silicon. The process currently works best with quarter and half wafers, and can be used in research, prototyping and small scale manufacturing. The blind-via process requires a full wafer to manufacture (using the set-up detailed in this work).

For future work related to this research, the author suggests a few points for further exploration. The first two suggestions for exploration are in regards to the ADE process development, and will be referred to as the modified-ADE process. The use of the ADE process should be tried using two recommendations. The first recommendation is the replacement of the backing wafer (seed layer) with only copper foil. Initial attempts were made at the end of this research and proved plausible. This way the TSVs would be grown from the foil tape covering the via openings. Minimizing initial copper usage, and eliminating the backing wafer set-up time and material costs. In order to avoid the problem of capillary action with the ADE process, the second recommendation is the use of the wafer holder for the blind via process. The blind via holder would provide backing support and reduce (if not, eliminate) the suction of via fluid into the assembly.

The first recommendation is in regards to the blind via process. The problem with this process is only when fresh chemistry is used does the user know the exact state of the solution. Thus, the researching of a way to test the ratio and quantities of different solutions within the electroplating bath before (and during) electroplating would be ideal for developing a cost effective repeatable process. In addition to this, the use of multiple baths should be attempted for starting the seed layer and plating the seed layer. The use of multiple via materials should also be tested for longer term stress testing.

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Appendix A ADE Process TSV Traveler

TSV WAFER

1. <u>receive and inspect wafers</u>

Type-------------------------- Silicon (or _____________)

Orientation------------------

Diameter---------------------

Thickness--------------------

Dopant-----------------------

Resistivity-------------------

Dopant Concentration-----

Wafer #----------------------

Total # of Wafers-----------

Date-------------------------

Manufacturer/supplier info:

Company Name:

Company Address:

Phone:

SO#:

PO#:

Company website:

2. wafer cleaning

Date:__________________

Table 9: RCA Clean

Process Name	Purpose	Step	Temperature	Mixture	Time
	Removes oils and other impurities	1	Room Temp.	IPA bath	1 min.
		2	Room Temp.	DI Water Bath	1 min.
RCA Standard Clean 1	Removes oxide layer on surface	3	70°C	1 : 30% H_2O_2 1 : 29% NH_4OH 5 : DI H_2O	10 min.
		4	Room Temp.	DI Water Bath	1 min.
RCA Standard Clean 2	Removes thin oxide surface	5	Room Temp.	1 : 49% HF 50 : DI H_2O	30 sec.
		6	Room Temp.	DI Water Bath	1 min.
RCA Standard Clean 3	Removes trace metals	7	70°C	1 : 30% H_2O_2 1 : 37% HCL 6 : DI H_2O	10 min.
		8	Room Temp.	DI Water Bath	1 min.

Following RCA clean, Spin Rinse Dry.

3. photolithography: Mask 1

a. HMDS Vapor Application (for adhesion)

Date:__________________

Temp----------------------------Room Temp.

Time---------------------------- 10 minutes

b. PR Application

Date:__________________

PR AZ P4620 etches at a ratio of roughly 70:1 (70µm Si for every 1µm of PR).

Need ____275___ μm Si etch thus minimum PR needed is:

$$\frac{275 \quad \mu\text{m of Si}}{1} \times \frac{1\mu\text{m of PR}}{70\mu\text{m of Si}} = _____3.93_____\mu\text{m of PR}$$

$$\approx ___4___\mu\text{m of PR}$$

PR Type→ AZ P4620

Spin Speed----------- 3000 rpm (5.5~6μm in our lab)

Spin Time------------- 40 seconds

Ramp Speed----------- 500 rpm/s

Measured PR----------

Wafer #							
PR Thickness (μm)							

c. Softbake

Date:_________________

Temperature-------------------- 110°C

Time---------------------------- 30 sec

Gap from hotplate------------- 1.5 cm

Temperature-------------------- 110°C

Time---------------------------- 150 sec

Gap from hotplate------------- 0 cm (contact)

4. PR Exposure

Date:__________________

Mask Aligner Settings found in Appendix C Karl Suss MA/BA6 Contact Mask Aligner

Mask-----------------------------Mask 1

PR multiple exposure schedule (assuming 5.5~6 μm PR)

Step	Time	Expose?
1	10 sec	Yes
2	30 sec	No
3	10 sec	Yes
4	30 sec	No
5	10 sec	Yes
6	30 sec	No
7	10 sec	Yes
8	30 sec	No

5. PR Develop

Date:__________________

Developer----------------------- 2:1; H_2O:AZ400K

Time----------------------------- 1 minute

DI rinse & N2 dry------------

Wafer #							
PR feature inspection							

6. Plasma Descum

Date:__________________

Ambient/Flow Rate----------- 29%

Pressure------------------------- 5 Torr

Power---------------------------- 300W

Time----------------------------- 14 seconds

7. 275um deep DRIE

Date:_________________

(STS DRIE settings in Appendix E)

Using Bosch process.

Etch : SF_6 / O_2

Passivate : C_4H_8

Assuming roughly.7µm etch per cycle, total number of cycles required

_______275________µm desired etch $\times \frac{1\ cycle}{.7\ \mu m\ etch} = 392\ cycles \approx 400 cycles$

Total time:

$$\frac{20\ \text{seconds}}{1\ cycle} \times 400\ cycles = 8000\ seconds = 2.22\ hours$$

Run cycles 1-100 (etch/passivate)

Rotate wafer 90°

Run cycles 101-200 (etch/passivate)

Rotate wafer 90°

Run cycles 201-300 (etch/passivate)

Rotate wafer 90°

Run cycles 301-400 (etch/passivate)

8. Post DRIE PR strip and sidewall polymerization clean

a. Pre-clean

Date:_________________

Acetone bath---------- complete?

IPA Bath--------------- complete?

Spin-Rinse-Dry------- complete?

b. Pre-clean

Date:_________________

ASHER (Matrix 102)

Ambient/Flow Rate----------- 29%

Pressure------------------------- 5 Torr

Power---------------------------- 300W

Time----------------------------- 5 minutes

9. Send to Aptek for 125µm backside grind and polish optional if wafer vias are etched through wafer depth

10. Wafer cleaning optional if not sent for backgrinding

Date:_________________

Process Name	Purpose	Step	Temperature	Mixture	Time
	Removes oils and other impurities	1	Room Temp.	IPA bath	1 min.
		2	Room Temp.	DI Water Bath	1 min.
RCA Standard Clean 1	Removes oxide layer on surface	3	70°C	1 : 30% H_2O_2 1 : 29% NH_4OH 5 : DI H_2O	10 min.
		4	Room Temp.	DI Water Bath	1 min.
RCA Standard Clean 2	Removes thin oxide surface	5	Room Temp.	1 : 49% HF 50 : DI H_2O	30 sec.
		6	Room Temp.	DI Water Bath	1 min.
RCA Standard Clean 3	Removes trace metals	7	70°C	1 : 30% H_2O_2 1 : 37% HCL 6 : DI H_2O	10 min.
		8	Room Temp.	DI Water Bath	1 min.

11. Thermal Oxidation

Date:_________________

Oxidation schedule found in Oxidation SettingsAppendix I

Oxide Thickness---- 6000Ǻ

12. Frontside seed layer deposition (E-beam 500Ǻ Ti, 5000Ǻ Cu)

Date:_________________

See Appendix J for e-beam settings

3 minute ion clean

Titanium Deposition (500Å)

Copper Deposition (5000Å)

Rotate 180°

3 minute ion clean

Titanium Deposition (500Å)

Copper Deposition (5000Å)

BACKING WAFER

1. receive and inspect wafers

Type-------------------------- Silicon (or _____________)

Orientation------------------

Diameter---------------------

Thickness--------------------

Dopant-----------------------

Resistivity-------------------

Dopant Concentration-----

Wafer #----------------------

Total # of Wafers-----------

Date--------------------------

Manufacturer/supplier info:

Company Name:

Company Address:

Phone:

SO#:

PO#:

Company website:

2. wafer cleaning

Date:__________________

Table 10: RCA Clean

Process Name	Purpose	Step	Temperature	Mixture	Time
	Removes oils and other impurities	1	Room Temp.	IPA bath	1 min.
		2	Room Temp.	DI Water Bath	1 min.
RCA Standard Clean 1	Removes oxide layer on surface	3	70°C	1 : 30% H_2O_2 1 : 29% NH_4OH 5 : DI H_2O	10 min.
		4	Room Temp.	DI Water Bath	1 min.
RCA Standard Clean 2	Removes thin oxide surface	5	Room Temp.	1 : 49% HF 50 : DI H_2O	30 sec.
		6	Room Temp.	DI Water Bath	1 min.
RCA Standard Clean 3	Removes trace metals	7	70°C	1 : 30% H_2O_2 1 : 37% HCL 6 : DI H_2O	10 min.
		8	Room Temp.	DI Water Bath	2 min.

Following RCA clean, Spin Rinse Dry.

3. photolithography: Mask 1

   a. HMDS Vapor Application (for adhesion)

      Date:__________________

      Temp----------------------------- Room Temp.

      Time----------------------------- 10 minutes

b. PR Application

Date:_________________

PR Type→ AZ P4620

Spin Speed------------ 3000 rpm (5.5~6μm in our lab)

Spin Time------------- 40 seconds

Ramp Speed----------- 500 rpm/s

c. Softbake

Date:_________________

Temperature-------------------- 110°C

Time---------------------------- 30 sec

Gap from hotplate------------- 1.5 cm

Temperature-------------------- 110°C

Time---------------------------- 150 sec

Gap from hotplate------------- 0 cm (contact)

ASSEMBLY

Place TSV wafer on backing wafer, connect conductive adhesive copper foil tape on backing wafer's seed layer. Seal in UV dicing tape. Cut incisions to expose via openings

1. Cu plating

Wafer Pre-wet

- Pull Vacuum
- Introduce IPA through nozzle

Electroplating

- Secure wafer in assembly
- Connect negative power supply terminal to target wafer (through wire on assembly)
- Connect positive power supply terminal to copper source.
- Rotate voltage knobs to maximum
- Turn power supply on
- Place target and source in solution
- Ramp current as follows:

Time (seconds)	Current (mA)
1-150	20
151-300	40
301-450	80
450-…	160

Intermittently inspect wafer for plating completion

Appendix B Blind-Via TSV Traveler

1. <u>receive and inspect wafers</u>

Type-------------------------- Silicon (or _____________)

Orientation-----------------

Diameter--------------------

Thickness-------------------

Dopant----------------------

Resistivity------------------

Dopant Concentration-----

Wafer #---------------------

Total # of Wafers-----------

Date-------------------------

Manufacturer/supplier info:

Company Name:

Company Address:

Phone:

SO#:

PO#:

Company website:

2. <u>wafer cleaning</u>

Date:_________________

Table 11: RCA Clean

Process Name	Purpose	Step	Temperature	Mixture	Time
	Removes oils and other impurities	1	Room Temp.	IPA bath	1 min.
		2	Room Temp.	DI Water Bath	1 min.
RCA Standard Clean 1	Removes oxide layer on surface	3	70°C	1 : 30% H_2O_2 1 : 29% NH_4OH 5 : DI H_2O	10 min.
		4	Room Temp.	DI Water Bath	1 min.
RCA Standard Clean 2	Removes thin oxide surface	5	Room Temp.	1 : 49% HF 50 : DI H_2O	30 sec.
		6	Room Temp.	DI Water Bath	1 min.
RCA Standard Clean 3	Removes trace metals	7	70°C	1 : 30% H_2O_2 1 : 37% HCL 6 : DI H_2O	10 min.
		8	Room Temp.	DI Water Bath	3 min.

Following RCA clean, Spin Rinse Dry.

3. photolithography: Mask 1

a. HMDS Vapor Application (for adhesion)

Date:__________________

Temp----------------------------Room Temp.

Time---------------------------- 10 minutes

b. PR Application

Date:__________________

PR AZ P4620 etches at a ratio of roughly 70:1 (70µm Si for every 1µm of PR).

Need ____275___ µm Si etch thus minimum PR needed is:

$$\frac{\textit{275}\quad \mu\text{m of Si}}{1} \times \frac{1\,\mu\text{m of PR}}{\textit{70}\,\mu\text{m of Si}} = \underline{\quad\textit{3.93}\quad}\,\mu\text{m of PR}$$

$$\approx \underline{\quad\textit{4}\quad}\,\mu\text{m of PR}$$

PR Type→ AZ P4620

Spin Speed------------ 3000 rpm (5.5~6μm in our lab)

Spin Time------------- 40 seconds

Ramp Speed----------- 500 rpm/s

Measured PR----------

Wafer #							
PR Thickness (μm)							

c. Softbake

Date:__________________

Temperature-------------------- 110°C

Time----------------------------- 30 sec

Gap from hotplate------------- 1.5 cm

Temperature-------------------- 110°C

Time----------------------------- 150 sec

Gap from hotplate------------- 0 cm (contact)

4. PR Exposure

Date:__________________

Mask Aligner Settings found in Appendix C Karl Suss MA/BA6 Contact Mask Aligner

Mask-----------------------------Mask 1

PR multiple exposure schedule (assuming 5.5~6 µm PR)

Step	Time	Expose?
1	10 sec	Yes
2	30 sec	No
3	10 sec	Yes
4	30 sec	No
5	10 sec	Yes
6	30 sec	No
7	10 sec	Yes
8	30 sec	No

5. PR Develop

Date:__________________

Developer----------------------- 2:1; H_2O:AZ400K

Time----------------------------- 1 minute

DI rinse & N2 dry------------

Wafer #							
PR feature inspection							

6. Plasma Descum

Date:__________________

Ambient/Flow Rate----------- 29%

Pressure------------------------- 5 Torr

Power---------------------------- 300W

Time----------------------------- 14 sec

7. 275um deep DRIE

Date:_________________

(STS DRIE settings in Appendix E)

Using Bosch process.

Etch : SF_6 / O_2

Passivate : C_4H_8

Assuming roughly.7µm etch per cycle, total number of cycles required

_______275________µm desired etch $\times \frac{1\ cycle}{.7\ \mu m\ etch} = 392\ cycles \approx 400 cycles$

Total time:

$$\frac{20\ \text{seconds}}{1\ cycle} \times 400\ cycles = 8000\ seconds = 2.22\ hours$$

Run cycles 1-100 (etch/passivate)

Rotate wafer 90°

Run cycles 101-200 (etch/passivate)

Rotate wafer 90°

Run cycles 201-300 (etch/passivate)

Rotate wafer 90°

Run cycles 301-400 (etch/passivate)

8. Post DRIE PR strip and sidewall polymerization clean

a. Pre-clean

Date:_________________

Acetone bath---------- complete?

IPA Bath--------------- complete?

Spin-Rinse-Dry------- complete?

b. Pre-clean

Date:_________________

ASHER (Matrix 102)

Ambient/Flow Rate----------- 29%

Pressure------------------------- 5 Torr

Power----------------------------300W

Time----------------------------- 5 minutes

9. Send to Aptek for 125µm backside grind and polish optional if wafer vias are etched through wafer depth

10. Wafer cleaning optional if not sent for backgrinding

Date:_________________

Process Name	Purpose	Step	Temperature	Mixture	Time
	Removes oils and other impurities	1	Room Temp.	IPA bath	1 min.
		2	Room Temp.	DI Water Bath	1 min.
RCA Standard Clean 1	Removes oxide layer on surface	3	70°C	1 : 30% H_2O_2 1 : 29% NH_4OH 5 : DI H_2O	10 min.
		4	Room Temp.	DI Water Bath	1 min.
RCA Standard Clean 2	Removes thin oxide surface	5	Room Temp.	1 : 49% HF 50 : DI H_2O	30 sec.
		6	Room Temp.	DI Water Bath	1 min.
RCA Standard Clean 3	Removes trace metals	7	70°C	1 : 30% H_2O_2 1 : 37% HCL 6 : DI H_2O	10 min.
		8	Room Temp.	DI Water Bath	2 min.

11. Thermal Oxidation

Date:_________________

Oxidation schedule found in Appendix I

Oxide Thickness---- 6000Ǻ

12. Frontside seed layer deposition (E-beam 500Ǻ Ti, 5000Ǻ Cu)

Date:_________________

See Appendix J for e-beam settings

3 minute ion clean

Titanium Deposition (500Å)

Copper Deposition (5000Å)

Rotate 180°

3 minute ion clean

Titanium Deposition (500Å)

Copper Deposition (5000Å)

13. <u>Cu plating</u>

Wafer Pre-wet

- Pull Vacuum
- Introduce IPA through nozzle

Electroplating

- Secure wafer in assembly
- Connect negative power supply terminal to target wafer (through wire on assembly)
- Connect positive power supply terminal to copper source.
- Rotate voltage knobs to maximum
- Turn power supply on
- Place target and source in solution
- Ramp current as follows:

Time (seconds)	Current (mA)
1-150	20
151-300	40
301-450	80
450-…	160

- Intermittently inspect wafer for plating completion

Appendix C Mask Aligner Settings

Multiple exposure – ON
Channel 2 – 300W

Setting	Value
Exposure Time [s]	10
Wait Time [s]	30
Cycles	4
Alignment Gap [µm]	25
WEC Type	CONT
Expose Type	Hard
HC wait Time [s]	5

Appendix D Via Low Power Etch, DRIE Settings

Program name LOWPOW.SET

GENERAL

Switching Parameters:

Start: Etch

End: Passivate

Cycles: (varies with use/application)

Parameter Switching Cycle Times

On Time:

Etch: 13 seconds

Passivate: 7 seconds

Overrun:

Etch: .5 seconds

Passivate: .5 seconds

Advanced Options

Parameter Switching: Yes

Parameter Ramping: No

Recipe Process Mode

Discrete or Continuous: Discrete

PRESSURE:

Base Pressure: 0.0 mTorr

Pressure Trip: 94.0 mTorr

Pressure Settings

Manual APC: on

Position: 83%

GASSES

		Etch		Passivation	
Line	Gas Name	Flow (sccm)	Tol (%)	Flow (sccm)	Tol (%)
1	C_4F_8	0	5	85	30
2	SF_6	130	30	0	5
3	O_2	13.0	30	0.0	5
4	Ar	0	5	0	5

R.F.

13.56 MHz Generator connected to Coil

Power: 600W (Passivation and Etch)

Matching: AUTO

Match Load 50.0%

Match Tune: 50.0%

Platen Generator connected to 13.56 MHz

Electrode: 13.56 MHz

Range: 0-300W

Power: 12W etch / 0W passivation

Tolerance: 50%

Matching: AUTO

Match Load: 50.0%

Match Tune: 50.0%

HBC

HBC Active: yes

<u>He Flow</u>

Pressure: 7500mTorr

Tolerance: 25%

Max Flow: 40.0 Sccm

Min Flow: 10.0 Sccm

HeLUR

<u>He Leak-Up Test</u>

Perform Test: yes

Test Time: 00:30 (mm:ss)

Max Leak Rate: 15.0 mTorr/Min

Appendix E Via High Power Etch, DRIE Settings

Program name HIGHPOW.SET

GENERAL

Switching Parameters:

Start: Etch

End: Passivate

Cycles: (varies with use/application)

Parameter Switching Cycle Times

On Time:

Etch: 13 seconds

Passivate: 7 seconds

Overrun:

Etch: .5 seconds

Passivate: .5 seconds

Advanced Options

Parameter Switching: Yes

Parameter Ramping: No

Recipe Process Mode

Discrete or Continuous: Discrete

PRESSURE:

Base Pressure: 0.0 mTorr

Pressure Trip: 94.0 mTorr

Pressure Settings

Manual APC: on

Position: 83%

GASSES

		Etch		Passivation	
Line	Gas Name	Flow (sccm)	Tol (%)	Flow (sccm)	Tol (%)
1	C_4F_8	0	5	85	30
2	SF_6	130	30	0	5
3	O_2	13.0	30	0.0	5
4	Ar	0	5	0	5

R.F.

13.56 MHz Generator connected to Coil

Power: 600W (Passivation and Etch)

Matching: AUTO

Match Load 50.0%

Match Tune: 50.0%

Platen Generator connected to 13.56 MHz

Electrode: 13.56 MHz

Range: 0-300W

Power: 18W etch / 0W passivation

Tolerance: 50%

Matching: AUTO

Match Load: 50.0%

Match Tune: 50.0%

HBC

HBC Active: yes

<u>He Flow</u>

Pressure: 7500mTorr

Tolerance: 25%

Max Flow: 40.0 Sccm

Min Flow: 10.0 Sccm

HeLUR

<u>He Leak-Up Test</u>

Perform Test: yes

Test Time: 00:30 (mm:ss)

Max Leak Rate: 15.0 mTorr/Min

Appendix F Via Widen Etch, DRIE (STEP 2) Settings [57]

Program name WIDENST2.SET

GENERAL

Advanced Options

Parameter Switching: Yes

Parameter Ramping: No

Recipe Process Mode

Discrete or Continuous: Continuous

PRESSURE:

Base Pressure: 0.0 mTorr

Pressure Trip: 30.0 mTorr

Pressure Settings

Manual APC: on

Position: 78%

GASSES

Line	Gas Name	Flow (sccm)	Tol (%)
1	C_4F_8	0	5
2	SF_6	84	99
3	O_2	67	50

4	Ar	59	5

R.F.

<u>RF Mode:</u>

Platen on 13.56 MHz Only – or – 13.56 MHz on Coil Only – or – Simultaneous: Simultaneous

<u>13.56 MHz Generator connected to Coil</u>

Power: 600W (Passivation and Etch)

Tolerance: 99%

Matching: AUTO

Match Load 33.0%

Match Tune: 50.0%

<u>Platen Generator connected to 13.56 MHz</u>

Electrode: 13.56 MHz

Range: 0-30W

Power: 30W

Tolerance: 99%

Matching: AUTO

Match Load: 31.0%

Match Tune: 51.0%

HBC

HBC Active: yes

<u>He Flow</u>

Pressure: 9800mTorr

Tolerance: 99%

Max Flow: 40.0 Sccm

Min Flow: 10.0 Sccm

HeLUR

<u>He Leak-Up Test</u>

Perform Test: yes

Test Time: 00:20 (mm:ss)

Max Leak Rate: 20.0 mTorr/Min

Appendix G Via Widen Etch, DRIE (STEP 3) Settings [57]

Program name WIDENST3.SET

GENERAL

Advanced Options

Parameter Switching: Yes

Parameter Ramping: No

Recipe Process Mode

Discrete or Continuous: Continuous

PRESSURE:

Base Pressure: 0.0 mTorr

Pressure Trip: 13.0 mTorr

Pressure Settings

Manual APC: on

Position: 65%

GASSES

Line	Gas Name	Flow (sccm)	Tol (%)
1	C_4F_8	0	5
2	SF_6	180	99
3	O_2	18.0	50

4	Ar	0	5

R.F.

RF Mode:

Platen on 13.56 MHz Only – or – 13.56 MHz on Coil Only – or – Simultaneous: Simultaneous

13.56 MHz Generator connected to Coil

Power: 600W (Passivation and Etch)

Tolerance: 99%

Matching: AUTO

Match Load 33.0%

Match Tune: 50.0%

Platen Generator connected to 13.56 MHz

Electrode: 13.56 MHz

Range: 0-30W

Power: 30W

Tolerance: 99%

Matching: AUTO

Match Load: 31.0%

Match Tune: 51.0%

HBC

HBC Active: yes

He Flow

Pressure: 9800mTorr

Tolerance: 99%

Max Flow: 40.0 Sccm

Min Flow: 10.0 Sccm

HeLUR

He Leak-Up Test

Perform Test: yes

Test Time: 00:20 (mm:ss)

Max Leak Rate: 20.0 mTorr/Min

Appendix H DRIE Cleaning

Program name CONDITIO.SET

GENERAL

Process:

Pump Down Time: 00:20 mm:ss

Gas Stabilization: 00:10 mm:ss

Process Time: 00:03:00 hh:mm:ss

Advanced Options:

Parameter Switching: No

Parameter Ramping: No

Recipe Process Mode:

Discrete or Continuous: Continuous

PRESSURE:

Base Pressure: 0.0 mTorr

Pressure Trip: 94.0 mTorr

Pressure Settings

Manual APC: on

Position: 67.0%

GASSES

Line	Gas Name	Flow (sccm)	Tol (%)
1	C_4F_8	0	5
2	SF_6	130	5
3	O_2	0.0	5
4	Ar	0	5

R.F.

RF Mode:

Platen on 13.56 MHz Only – or – 13.56 MHz on Coil Only – or – Simultaneous: Simultaneous

13.56 MHz Generator connected to Coil

Power: 600W (Passivation and Etch)

Tolerance: 50%

Matching: AUTO

Match Load 50.0%

Match Tune: 50.0%

Platen Generator connected to 13.56 MHz

Electrode: 13.56 MHz

Range: 0-300W

Power: 12W etch

Tolerance: 50%

Matching: AUTO

Match Load: 50.0%

Match Tune: 50.0%

<u>HBC</u>

HBC Active: yes

<u>He Flow</u>

Pressure: 8000mTorr

Tolerance: 25%

Max Flow: 40.0 Sccm

Min Flow: 10.0 Sccm

HeLUR

<u>He Leak-Up Test</u>

Perform Test: no

Appendix I Oxidation Settings

Table 12: Oxidation Settings

Step	Time (sec)	Temperature (°C)	Gas	Flow Rate (slm)
1	--	400	N2	5
2	Until temp. reached	400→1000	N2	10
3	5	1000	N2	5
4	5	1000	O2	5
5	120	1000	O2/H2	3 / 5.5
6	5	1000	O2	5
7	5	1000	N2	5
8	Until temp reached	1000→400	N2	5
9	---	400	N2	5

Appendix J E-beam settings

Sample settings for 500Å Ti and 5000Å Cu.

Table 13: E-beam Details

Description	Value
Number of Samples:	15
Description:	ion clean 3 mins, 500 A Ti and 5000A Cu
Base:	4.7e-7
Program Number:	31
Ion Time:	0
Cathode I:	3.36
Discharge I:	1.96
Ion Beam current:	178
Ion Acc current:	8
NEU EMM Current:	221
discharge volt:	55.1
Beam Volt:	973
ACC Volt:	99
Fil current:	2.81
Layer Index:	2
Comments:	

Table 14: E-beam Layer Samples

Metal	Crucible	Emm	voltage	Rate (Å/sec)	Power (%)	Thickness (Å)
Chromium	5	.030	9.7	2.0	64.7	500
Titanium	1	.102	9.17	2.0	66.3	500
Copper	6	.098	9.5	4.0	63.4	5000