Vernier Ring Time-to-Digital Converter Based Digital Phase Locked Loop

by

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Abstract

Digital phase-locked loops (DPLLs) recently are widely explored for wireless communication applications. Time-to-digital converter(TDC)-based DPLLs feature a high degree of integration, easy calibration and high programmability, and the DPLL can be easily scaled down to the deep-submicron CMOS process with less area and improved performance. Replacing the function of a phase detector and charge pump used in a conventional PLL, the TDC measures the phase error between the reference signal and the feedback signal in the time domain and directly outputs the phase errors in a digital format that can be processed by an on-chip digital loop filter. Due to the use of a programmable digital loop filter, the loop dynamics of a DPLL can be programmed on the fly and thus can achieve fast settling time and low phase noise simultaneously. The on-chip digital loop filter can provide accurate loop dynamics that are less sensitive to process, voltage and temperature (PVT) variations and more immune to the supply and substrate noise. In addition, the area of the DPLL can be reduced by eliminating large capacitors used in analog loop filters.

TDC is a critical building block of the DPLL. Similar to other sampling circuits, a TDC inevitably generates quantization noise while digitizing the input phase error or time interval. This quantization noise associated with the finite TDC resolution limits the in-band noise of a TDC-based DPLL. On the other hand, it's desired for a TDC to have a large detectable range in order to be able to respond to large phase error during the pull-in of a phase locking process, especially in the low output frequency DPLL.

In this research, a novel 8-ps resolution Vernier ring TDC and a 16-ps resolution 3-D Vernier ring TDC were invented and designed to achieve both the fine resolution and large detectable range. The state-of-art TDC design was also used in the on-chip jitter measurement. The 3.6GHz digital phase locked loop based on the Vernier ring TDC was designed and analyzed. The detailed circuit design and performance analysis are extensively discussed in the dissertation. The simulation and measured results of these circuits are also presented to verify the proposed designs.

Acknowledgments

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Last but not least, this dissertation is dedicated to my family, including my father Daihong Peng, my mother Yimei Yu, my bother Jianping Peng, my sister Qinwei Peng and especially my beloved wife Tao Liu. Without your support and encouragement, I can not finish this work.

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List of Abbreviations

BiCMOS	Bipolar and Complementary Metal-Oxide-Semiconductor
BIST	Build-In-Self-Test
CMOS	Complementary Metal-Oxide-Semiconductor
DCO	Digitally Controlled Oscillator
FOM	Figure of Merit
DPLL	Digital Phase Locked Loop
DNL	Differential Non-Linearity
GRO	Gated Ring Oscillator
IIR	Infinite Impulse Response
INL	Integral Non-Linearity
LIDAR	Light Detection And Ranging
LSB	Least Significant Bit
LPF	Low Pass Filter
MSB	Most Significant Bit
TDC	Time-to-digital Converter
TOF	Time-of-flight
VRTDC	Vernier Ring Time-to-digital Converter

Chapter 1 Introduction

1.1 Background and motivation

Time-to-digital converters (TDCs) are used to measure the time interval between two events by a small quantization step that is called the time resolution. High resolution TDCs have become increasingly popular for time-of-flight (TOF) measurement for applications such as clock data recovery, test instrumentation, light detection and ranging (LIDAR) and all digital phase-locked loop (DPLL). Time resolution, detectable range, measurement time, power consumption and die area are most important concerns in TDC designs. Similar to any other analog to digital converter, the quantization step is the major parameter of TDC that determines the system performance in all the applications stated above. In the standard CMOS technology, the basic logic gates, like inverters and buffers, are often used to generate a small amount of delay (time resolution) for time interval measurement. Time resolution of a single delay line based TDC thus suffers from process, voltage and temperature (PVT) variations. On another hand, the detectable range specifies the maximum time interval a TDC can measure. The requirements of a large detectable range and a fine resolution often conflict with each other in TDC designs. The proposed novel N-dimensional Vernier TDC is intended to provide an efficient solution to address this issue.

TDC is a critical building block for emerging DPLL applications [1][2]. TDC-based DPLLs feature a high degree of integration, easy calibration and high programmability. A DPLL can be

easily scaled down to the deep-submicron CMOS process with less area and improved performance. Replacing the function of a phase detector and charge pump used in a conventional PLL, a TDC measures the phase error between the reference signal and the feedback signal in time domain and directly outputs the phase errors in digital format that can be processed by an on-chip digital loop filter. Due to the use of a programmable digital loop filter, the loop dynamics of a DPLL can be programmed on the fly and thus can achieve fast settling time and low phase noise simultaneously. An on-chip digital loop filter can provide accurate loop dynamics that are less sensitive to PVT variations and are more immune to the supply and substrate noise. In addition, the area of the DPLL can be reduced by eliminating large capacitors used in analog loop filters, making loop filter integratable. Similar to any sample circuits, a TDC inevitably generates quantization noise while digitizing the input phase error or time interval. This quantization noise associated with the finite TDC resolution limits the in-band noise of a TDC-based DPLL. In another words, the finer the TDC resolution is, the better the in-band phase noise the DPLL can achieve. On the other hand, it's desired for a TDC to have a large detectable range in order to be able to respond to large phase error during the pull-in of a phase locking process. DPLLs can be divided into two categories: divider–assisted DPLL and divider-less DPLL. Large range TDC is required in divider-assisted DPLL. The TDC in divider-less DPLL uses the DCO period as the coarse quantization resolution which is not stable and has a large variance compared to the fine resolution of TDC. In addition, more number of TDC bits is required in the divider-less DPLL with a larger DCO period, namely a larger coarse resolution. However, conventional delay-line based TDCs entail the use of an extra hardware to extend its range of operation [2], which requires large area and high power consumption.

1.2 Organization of dissertation

In this dissertation, a new idea of N-dimensional Vernier TDC is proposed to improve both time resolution and detectable range. The organization of the dissertation is as follows:

Chapter 2 gives the overview of the various existing time-to-digital converter (TDC) architectures. Although there are many ways to quantize the input time interval, the digital inverter is still an appealing delay element to build a TDC due to its digital-intensive design approach, easy implementation and compatibility to most technology. The conventional delay line TDC, time-amplifier based TDC and gated ring oscillator based TDC are all introduced in this chapter. The Vernier structure is an attractive way to obtain a fine resolution TDC.

Chapter 3 discusses the novel Vernier ring TDC which achieved a fine resolution of 8 pico-second with a large resolution of 13 bits. The die area and power consumption are improved by placing the delay cells in a ring format. The detailed circuit design along with the simulation and measured data are presented in this chapter.

Chapter 4 presents a novel 3-dimensional Vernier ring TDC which further improved the power consumption and die area by introducing the comparator matrix which is the key element to build a 2-dimensional delay plane. The measured data shows that a time resolution of 16.5ps and 8-bit detectable range were obtained in this design.

Chapter 5 introduces the application of Vernier ring time-to-digital converter to the on-chip jitter measurement. The Vernier TDC was tested by inputting a clock signal with a small amount of jitter modulated by a noise source. The Gaussian distribution of the digitized code was obtained at the TDC outputs and the standard variation of that distribution indicates the rms value of the input jitter.

Chapter 6 explores the design of 12GHz Colpitts VCO using artificial dielectrics to add the shielding of LC tank to the lossy substrate and improve the phase noise performance with the optimized combination of the artificial dielectrics control code.

Chapter 7 shows the dedicated Vernier ring TDC for DPLL and other building blocks such as digital filter and digitally controlled oscillator. The impact of the TDC resolution to the DPLL in-band noise has been analyzed.

Chapter 8 summarizes the research work mentioned above and presents the future work on the TDC and DPLL.

Chapter 2 Overview of Time-to-Digital Converter

2.1 Introduction

In the past, a large amount of TDC topologies have been explored to reduce time resolution and to extend detectable range while keeping the power and area cost at a reasonable level [1-16]. The proposed TDC was evolved from a so-called Vernier ruler concept as explained below.

An inverter-chain based TDC was implemented in the first DPLL chip for a blue-tooth radio application [3]. Ever since, a variety of TDC architectures have been proposed with improved resolution and detectable range [1-16]. Although there are many ways to digitize the input time interval, the digital inverter-delay-line is still an appealing structure due to its digital-intensive design approach [4]. Fig.2.1 shows the conventional inverter-delay-line based TDC. Its time resolution is the propagation delay of each individual inverter stage, while its detectable range is proportional to the number of delay stages used. Its measured time interval can be expressed as $N*T_{delay}$, where T_{delay} is the time resolution of the TDC and N is the number of stages used. Consequently, achieving fine resolution contradicts the goal of achieving large detectable range, since a TDC with finer resolution would require more delay cells in order to achieve the same detectable range. Moreover, both the time resolution and the detectable range of the TDC are very sensitive to PVT variation, which directly affects the accuracy of the measurement and thus degrades the phase noise of a DPLL that employs such kind of TDC.

A Vernier delay line is well known for its fine time resolution [5]. Fig.2.2 illustrates a simplified Vernier inverter delay line TDC that employs two inverter/buffer chains with different delays of T_S and T_F, respectively. Time resolution of the Vernier TDC now becomes the delay difference of two delay lines, namely, $T_S - T_F$. Note that the resolution is greatly improved by using two delay lines. In addition, Vernier delay line architecture can tolerate first order PVT variation if the two delay lines are well matched. Nevertheless the Vernier delay line TDC struggles with reduced efficiency in measuring large time intervals for the same reason mentioned above.

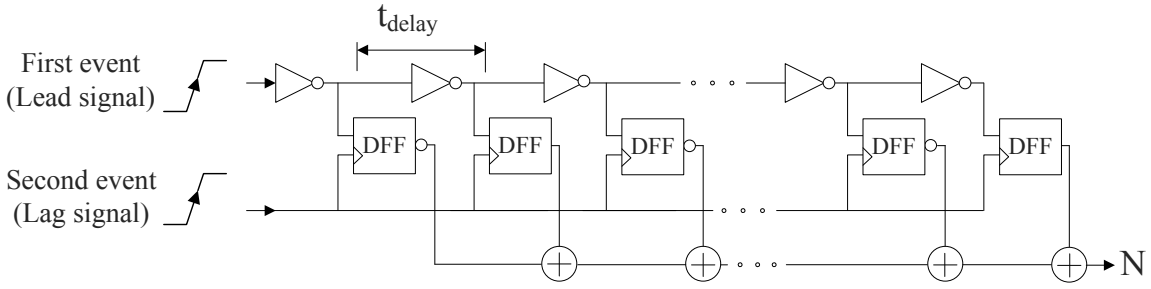


Fig.2.1 Delay line based TDC

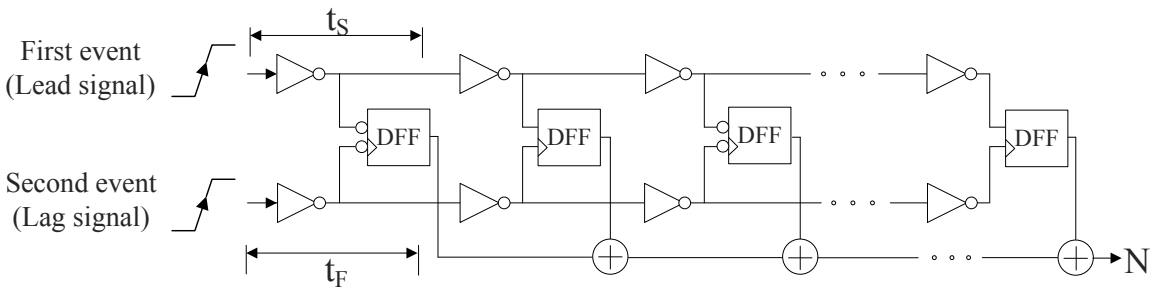


Fig.2.2Vernier delay line TDC.

Recently several topologies have been reported to shrink the TDC time resolution to several picoseconds. The two-step TDC uses a delay-line TDC as a coarse TDC and a Vernier delay-line TDC as a fine TDC to achieve fine resolution and large detectable range [6][7]. As shown in Fig.2.3(a), a time amplifier based TDC improves the resolution and detectable range by

amplifying the time residue left in a coarse TDC before quantizing it using a fine TDC [8]. A multipath gated ring oscillator (GRO) structure (Fig.2.3(b)) was proposed to improve the TDC resolution to 6ps in a 0.13μm technology [9]. This GRO-based TDC also achieves first order quantization noise shaping by holding the phase of the oscillator output between measurements. This GRO based TDC achieves a detectable range of 11 bits with up to 21mW power consumption and an area of 0.04 mm^2. A local passive interpolation TDC employs a differential delay line to obtain a coarse delay. It then interpolates this delay with a resister voltage divider and achieves a sub-gate-delay of 4.7ps [10]. The parallel scaled delay line structure provides an alternative approach for resolution improvement. A two-level interpolation TDC with this parallel structure achieved a time resolution of 12.2ps in a 0.35um CMOS technology [11]. A pulse shrinking delay element based TDC was reported with a sub-gate-delay resolution [12]. A 1 ps-resolution jitter-measurement macro was implemented recently with two-step hierarchical Vernier delay line structure [13].

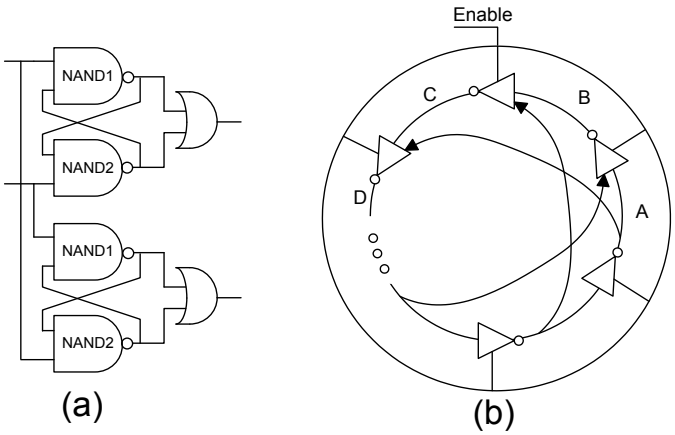


Fig.2.3 (a) time difference amplifier (b) gated ring oscillator with multi-path inputs to the inverter

A 2-dimensional Vernier TDC was reported with a time resolution of 4.8 ps [14]. This TDC places the two Vernier delay lines in two mutually perpendicular directions and a plurality of comparators in a matrix comparing the delays between taps in the two delay lines. The number of the delay stages used in this 2-dimensional structure is almost the square root of what is required in a conventional Vernier delay line TDC for the same detectable range. As a result, the power consumption was reduced due to less toggles of two propagating signals through delay stages. However, the 2-dimensional structure still struggles with the area cost in the applications where the large detectable range is needed, since the number of delay stages and comparators monotonically increase when detectable range increases.

We proposed a Vernier Ring TDC (VRTDC) that leverages the time difference between two rings of delay cells to achieve a time resolution of 8ps [15][16]. Unlike the conventional Vernier TDC, this novel TDC places the Vernier delay cells in a ring format such that the delay chains can be reused for measuring large time intervals. The reuse of Vernier delay cells in a ring configuration achieves fine resolution and large detectable range simultaneously with small area and low power consumption. In the Vernier ring architecture, detectable range can be increased to any large number without causing extra cost in area, as long as the counter has enough space to hold the output data. Compared with other structures mentioned above, less power will be consumed in the measurement of a large time interval due to its build-in coarse-fine two-level interpolation scheme. In this design, a large detectable range of 12 bits has been achieved with a small area of 0.26 mm^2.

The novel structure of Vernier ring TDC proposed here has been further improved in the power consumption and die area by conceiving a new set of Vernier ring TDC structures. This novel

idea of constructing a 3-dimensional up to N-dimensional delay space is presented for the first time after our patent application filed in Jan. 2010 [17]. The idea is intended to build a highly efficient TDC with several pico-second resolution and a large dynamic range, which will fuel the improvement in many TDC applications such as frequency synthesis, time interval measurement and light detection and ranging (LIDAR).

2.2 Time-to-digital converter for digital phase locked loop

DPLL has recently emerged as an attractive alternative to the traditional analog PLL for many applications. Recent results demonstrate that digital frequency synthesizers have good noise performance comparable to that achieved by analog PLLs [4]. Compared to direct digital synthesizers that can offer a high output frequency with fine frequency resolution, fast frequency switching and versatile modulations [8][18][19][20][21], DPLL is characterized with superior spectrum purity at RF frequency and less power consumption. DPLLs have the potential to replace analog PLLs used in wireless transceivers [4][22][23][24].

In transition from analog PLL to digital PLL, phase-frequency detector and charge pump were replaced by a TDC, which quantizes the phase error between the reference clock and feedback clock. Consequently, digital loop filter and digital controlled oscillator are substitutes for their analog counterparts. A fractional DPLL was implemented with DAC and VCO instead of DCO to achieve low phase noise [32]. This hybrid VCO structure leverages a switched capacitor array for frequency band selection and an analog varactor for fine tuning and has become a popular choice in many recent DPLLs due to their ability to achieve a wide tuning range with excellent phase noise. Similar to the analog fractional-N PLL, a multi-modulus divider with sigma-delta modulator in the feedback path was employed to generate fractional divide ratio as shown in

Fig.2.4. Many DPLLs use the divider-less topology [33][34], which are further simplified by replacing the combination of DAC and VCO with a DCO as shown in Fig.2.5. The output frequency is tuned by switching on and off capacitors in the LC tank controlled by a digital control word. Compared to analog PLL, additional quantization noise coming from the DCO and the TDC degrade the output spectral purity. A Sigma-Delta modulator can be used at the input of the DCO to dither and shape DCO quantization noise to high frequency band where it can be rejected by the low pass characteristics of the close loop.

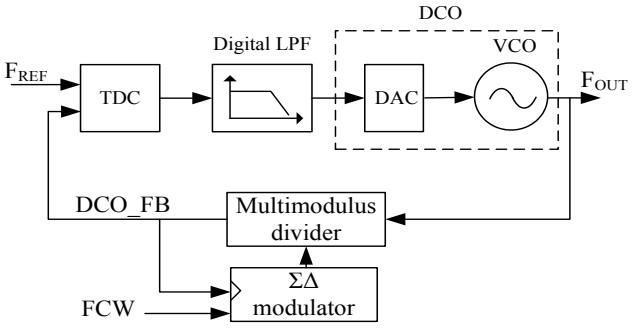


Fig.2.4 Fractional DPLL with multi-modulus divider.

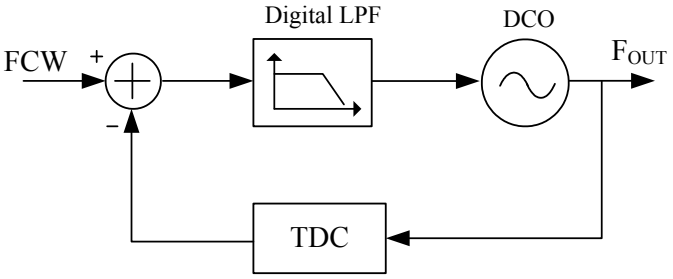


Fig.2.5 Divider-less DPLL with DCO.

Chapter 3 Vernier Ring TDC

3.1 Concept of Vernier ring TDC

The proposed Vernier ring time-to-digital converter evolves from the conventional Vernier delay line TDC (Fig.3.1). Inverters or buffers were used as the delay stages to build the Vernier delay line TDC in a standard digital process. Connecting the outputs of the last delay cells of a Vernier delay line TDC to the inputs of the first pair of delay cells constructs a novel Vernier ring TDC (VRTDC). An odd number of delay cells (15 stages in this design) are used to form the rings. A NAND gate replaces an inverter as the first delay stage is used to input the signals under test. The rising edge of a signal to be measured can be fed into the delay ring through one of the inputs of the NAND gate. The pair of NAND cells in the two rings have the same delay difference as that of the inverter pairs in the two rings. Note that there are some subtle things that must be accounted for in order to construct a fully functional TDC using the proposed Vernier rings.

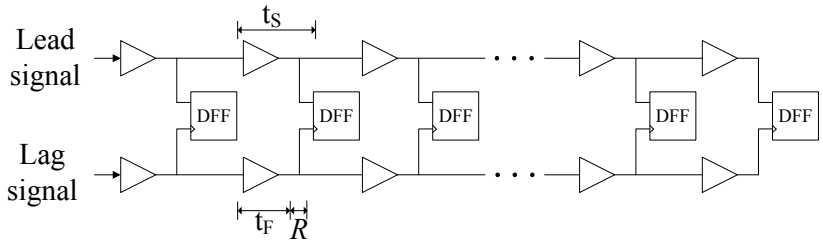


Fig.3.1 Conceptual view of Vernier delay line TDC.

Fig.3.2 illustrates the concept of the proposed VRTDC core. Two rings of inverters with

slightly different delays are used to measure the input time interval. The VRTDC core consists of two chains of arbiters, which operate in odd laps and even laps, respectively. Recall that the VRTDC contains odd number of delay cells. Thus, a rising edge becomes a falling edge after one lap of propagation along the ring. The two types of arbiters are placed alternatively along the rings to compare the rising or falling edges, respectively. The VRTDC core consists of a fast ring with smaller delay, a slow ring with larger delay and 30 arbiters as shown in Fig.2. Each ring has 15 stages of inverters with delays adjustable by external bias voltages. The propagation delay of the inverters in fast and slow rings are set to t_F and t_S, respectively. Thus the time resolution of the proposed TDC is given by

$$R = t_S - t_F \tag{3.1}$$

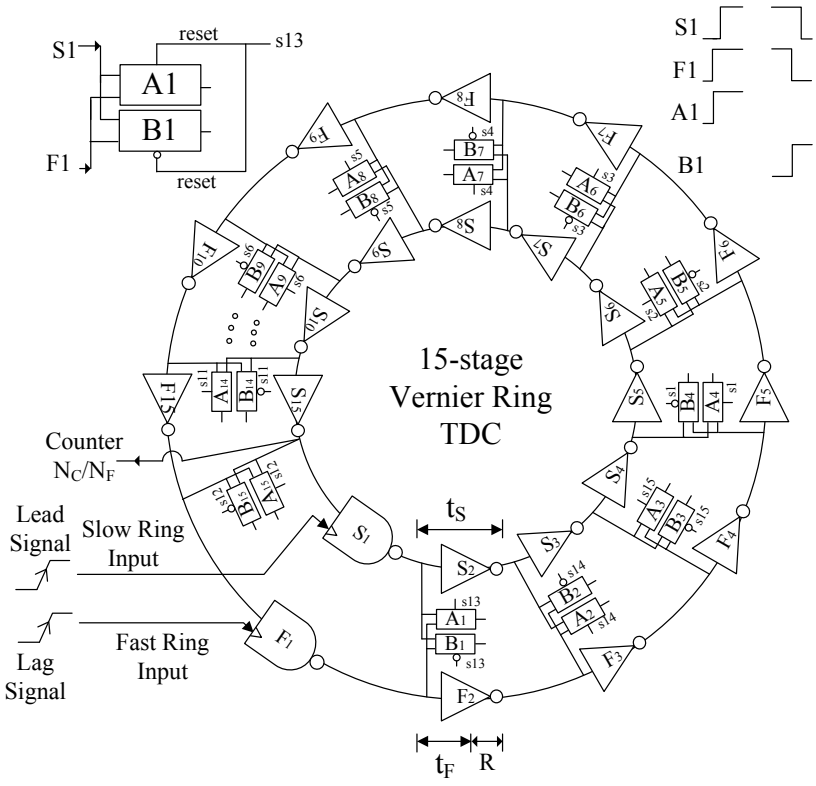


Fig.3.2 Block diagram of the VRTDC core with 15 stages.

Fig.3.3 illustrates the operation of the proposed VRTDC in two successive laps, i.e., the first lap and the second lap. Two arbiter chains (shown in Fig.3.2) work alternatively during the

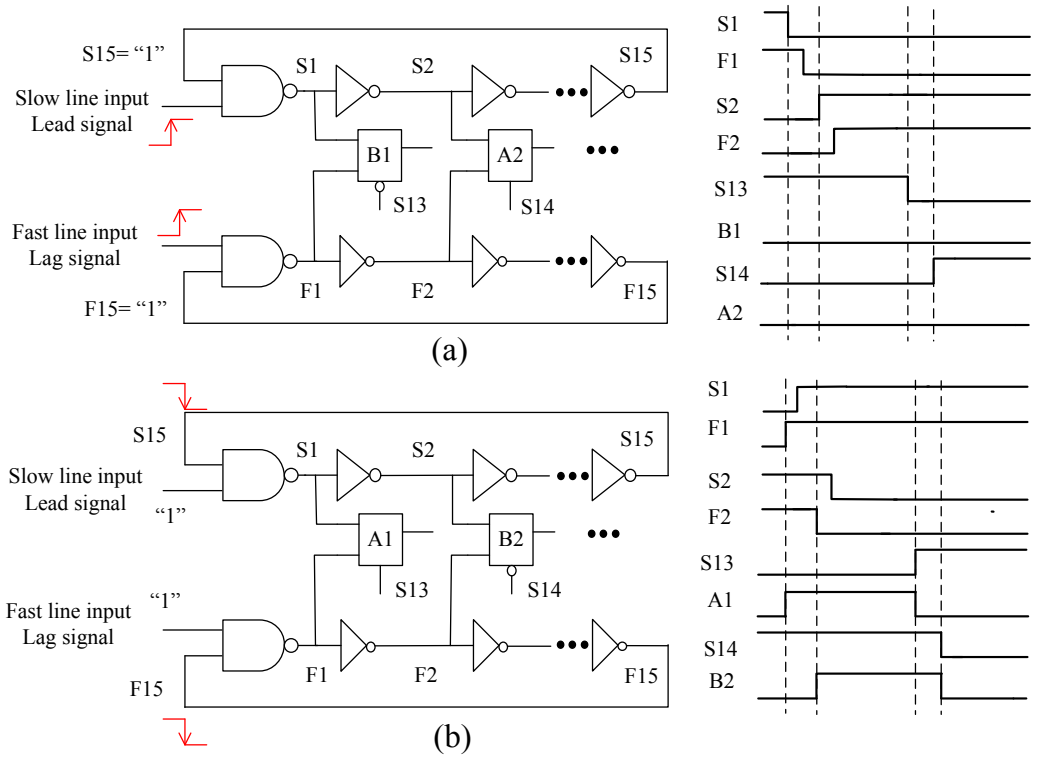


Fig.3.3 Illustration of the VRTDC operation at (a) first lap, and (b) second lap

measurement. To help understand the operation of the proposed VRTDC, we separate the whole VRTDC core into two Vernier delay rings shown in Fig.3.3. Each ring consists of two rings of inverters and one arbiter chain. Fig.3.3 (a) depicts the operation of VRTDC in the first lap. Initially, slow ring and fast ring inputs are pulled down to ground (GND) before measurement starts. Two rings are latched to a stable state, where both inverter S15 and F15 output logic "1". In the first lap, the rising edges of the lead and lag signals are fed into two NAND gates to start their propagations along the fast and slow rings, respectively. Lead signal propagates to S2 after an inverter delay of t_S. Lag signal propagates to F2 after an inverter delay of t_F. Arbiter B1 compares two falling edges at S1 and F1, while the arbiter A2 compares the rising edges at S2

and F2. B1 and A2 will be reset when lead signal propagates to S13 and S14, respectively. Fig.3.3 (b) shows the operation of Vernier ring at the second lap. Both slow and fast ring inputs are set to logic "1" after two signals are fed into the Vernier ring until the lag signal catches up the lead signal. Setting the inputs of the rings to "1" enables two signals to propagate through the delay cells in the rings over and over again, allowing reuse of the hardware. Note that S1 and F1 toggle to logic "1" in the second lap, namely, a falling edge in the first lap becomes a rising edge in next lap. Thus, arbiter needs to compare rising edges at S1 and F1 as well as the falling edges at S2 and F2. Hence another set of arbiters are needed to work in the second lap and the following even number of laps. This novel Vernier ring TDC is constructed by combining two set of delay rings and arbiters as illustrated in Fig.3.2.

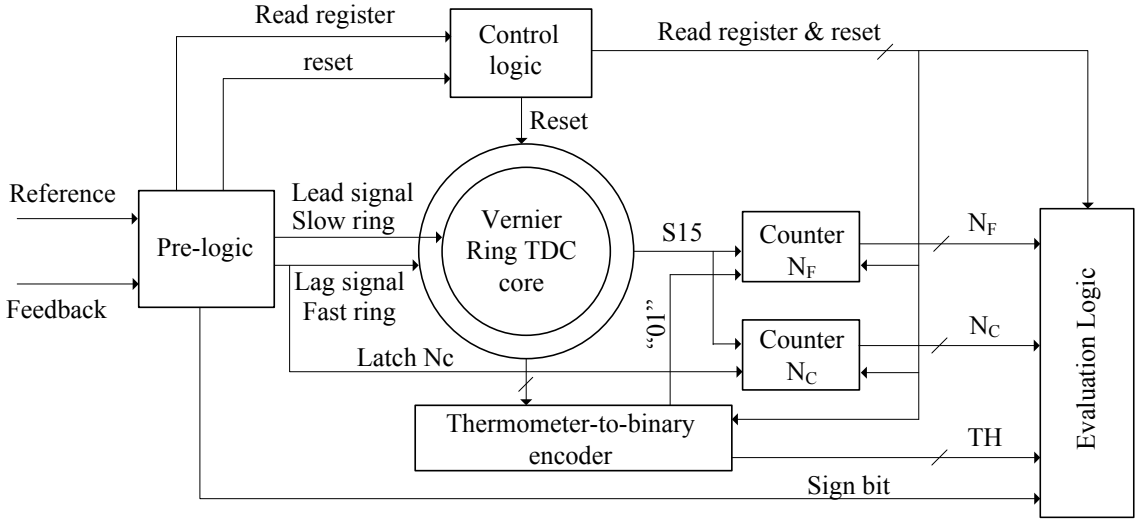


Fig.3.4 Block diagram of the VRTDC system

Fig.3.4 shows the overall architecture of the proposed 12-bit VRTDC system. The IC chip is composed of the VRTDC core, pre-logic, control logic, thermometer decoder, a 6-bit fine counter (N_F) and a 6-bit coarse counter (N_C). The reference signal and oscillator feedback signal in a DPLL are fed into the pre-logic cell, where an arbiter judges whether the reference leads the feedback or vice versa and determines the sign bit of the TDC output. As shown in Fig.3.4, the

lead signal is steered to the slow ring by the output of the arbiter, while the lag signal is fed into the fast ring. The lag signal chases the lead signal along the ring and eventually passes it after a certain amount of propagation.

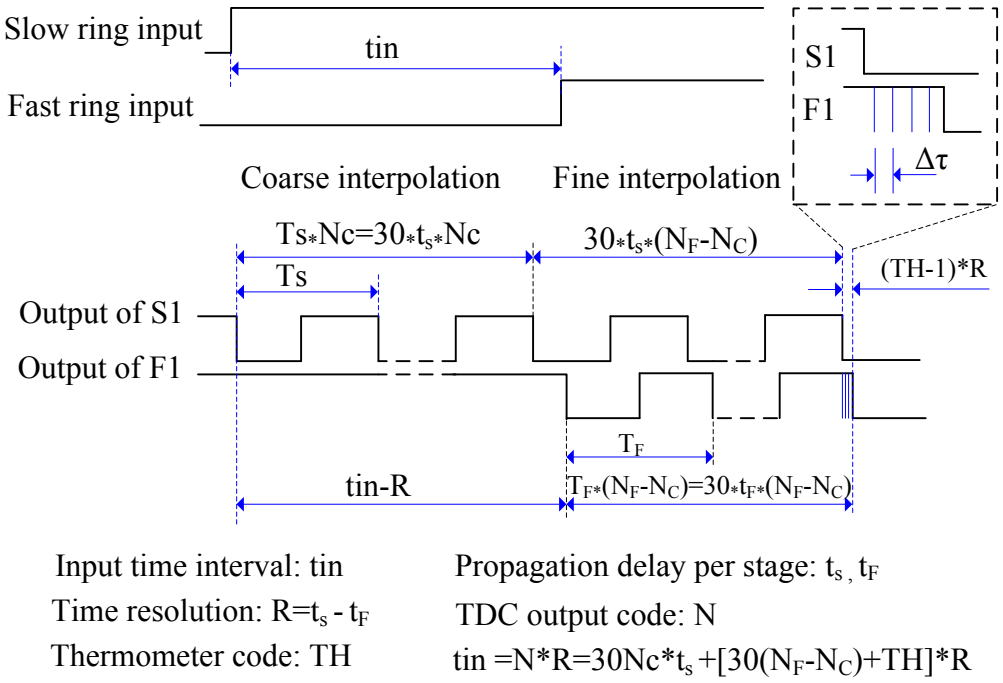


Fig.3.5 Timing diagram of VRTDC

The outputs of 30 arbiters are combined into a 30-bit thermometer code "*TH*" and are translated into a 5-bit binary code by a thermometer-to-binary encoder. *TH* records the location (number of delay cells) where the lag signal passes the lead signal. The fine counter (N_F) records the number of laps (odd and even) that the lead signal has propagated before the lag signal catches up the lead signal. The coarse counter (N_C) records the number of laps that the lead signal has propagated before the lag signal arrives at the input of the TDC. Therefore the total amount of delay *N* consists of four elements: the sign bit, the coarse counter value N_C, the fine counter value N_F and the thermometer code *TH*, as shown in the timing diagram of Fig.3.5. Before the lag signal enters the proposed TDC, only one signal propagates along the slow ring.

Hence, the TDC operates in its coarse measurement mode, where it interpolates the input time interval with a coarse resolution of $30 \cdot t_S$. This coarse interpolation mode improves the power and area efficiency, and the measurement time as well. Once the lag signal enters the ring, the TDC automatically switches to its fine measurement mode using the Vernier principal, where the TDC interpolates the residue of the time interval under test with a fine resolution of $R = t_S - t_F$ till the lag signal catches up the lead signal. Counter N_F is used to assist the counting of the number of fine interpolations due to the limited bit count of thermometer code. The dynamic resolution adjustment of the proposed TDC differs from the *prior art* TDC architectures, where a fixed resolution were employed. Even with the conventional two-step approach, additional hardware is needed to achieve coarse and fine resolutions. The final output code of the proposed TDC, which is the digital representation of the measured time interval, is thus given by

$$N = \pm 30(N_F - N_C) + TH + 30N_C t_S / R \qquad (3.2)$$

where TDC resolution is given by $R = t_S - t_F$ and the polarity of *N*, i.e., the sign bit of the TDC output, is determined by the pre-logic as described above. This sign bit can be used to program the polarity of the phase error in a DPLL implementation. The detectable range is determined by the interpolation ratio t_S / R for a given number of bits of the coarse and fine counters because the fine interpolation code should be equal or less than the coarse resolution, namely $30(N_F - N_C) + TH \le 30t_S / R$. The detectable range is given by the following equations:

$$| N | \ge 30N_C t_S / R = 30[N_F - (N_F - N_C)]t_S / R \qquad (3.3)$$

$$\max(| N |) \ge 30[2^6 - 1 - (N_F - N_C)]t_S / R \ge 30[63 - t_S / R]t_S / R \qquad (3.4)$$

Therefore the detectable range varies with the interpolation ratio. For instance the maximum code is larger than 12 bits for the ratio $t_S / R = 4$ since $\max(|N|) \geq 30 * [63 - 4] * 4 = 7080 > 2^{12}$. It is theoretically possible that the detectable range can achieve 13 bits when the ratio is set to 8.

3.2 Circuit implementation of Vernier ring TDC

In this section, we discuss the detailed circuit implementation of the proposed VRTDC. We present the circuits of the pre-logic unit, two types of arbiters with edge detectors, the thermometer-to-binary encoder, and two delay stages. We also explain the operation of arbiters and the correction circuit for "01"detection.

3.2.1 Pre-logic unit

The pre-logic unit, arbiter and delay stage are the critical building blocks of the Vernier ring TDC. The reference signal may lead or lag the oscillator feedback signal in DPLL applications. Since the two rings of inverters in the Vernier ring TDC core have different propagation delays, the lead signal should be steered to the slow ring, while the lag signal goes to the fast ring. Otherwise, the lag signal will never catch up with the lead signal and the VRTDC will not work. Therefore, the pre-logic unit is essential to the VRTDC implementation. Reference signal and the oscillator feedback signal in a DPLL are first fed into the pre-logic cell. The pre-logic unit consists of an arbiter, two symmetrical delay chains, a multiplexer (MUX) and a reset path, as shown in Fig.3.6. The delay of buffer lines inserted between the input of the arbiter and MUX has sufficient delay to allow the MUX to swich the propagation path before two signals arrive. The arbiter is reset after both lead and lag signals pass by. The output of the sign bit will be "0" when the arbiter judges that the reference signal leads the feedback signal. Otherwise the sign bit is "1". This sign bit and other bits of VRTDC output will be combined into a signed value

representing the positive and negative phase error in the DPLL application. The first arriving signal is used to synchronize the entire VRTDC as a global clock. Two OR gates are employed to generate the “read” and “reset”signal to control the registers where the previous measurement results are stored. The arbiters and other registers associated with the last measurement are reset as well.

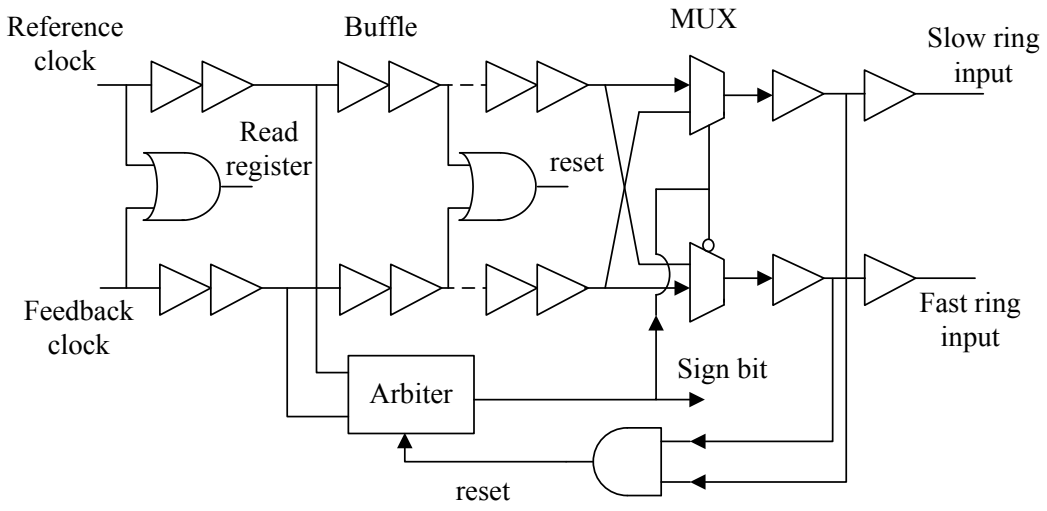


Fig.3.6 Simplified circuits of the pre-logic unit

3.2.2 Arbiter, edge detector and control logic

Similar to the operation of a Vernier delay line TDC, a comparator is needed at every stage to compare the arriving sequence of two signals propagating through the slow ring/line and fast ring/line, respectively. A D-flip-flop is often used to build this type of comparators. However, the clock propagation and data propagation paths in the conventional DFF normally do not match well such that there will be a large time offset in the DFFs characteristics [8]. This time offset is subject to the PVT variations from stage to stage and will cause a shift in the TDC output result. Therefore, an alternate arbiter architecture with symmetric topology was used in this VRTDC,

where the clock path and data path match well so that the comparison is less sensitive to the PVT variation.

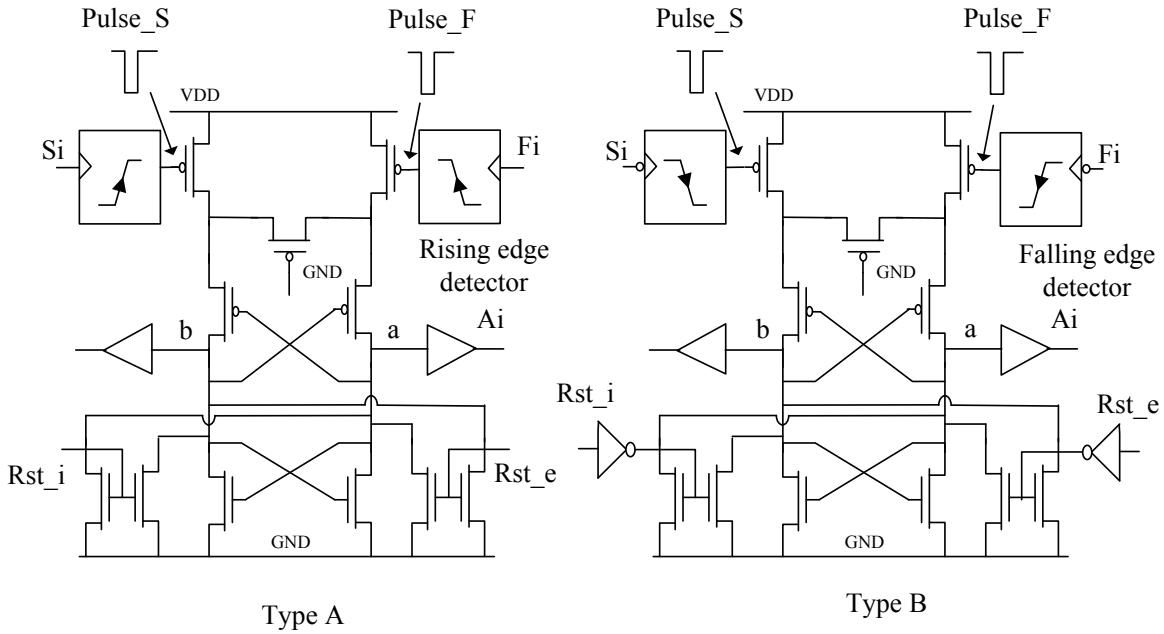


Fig.3.7 Simplified circuits of arbiter A and B

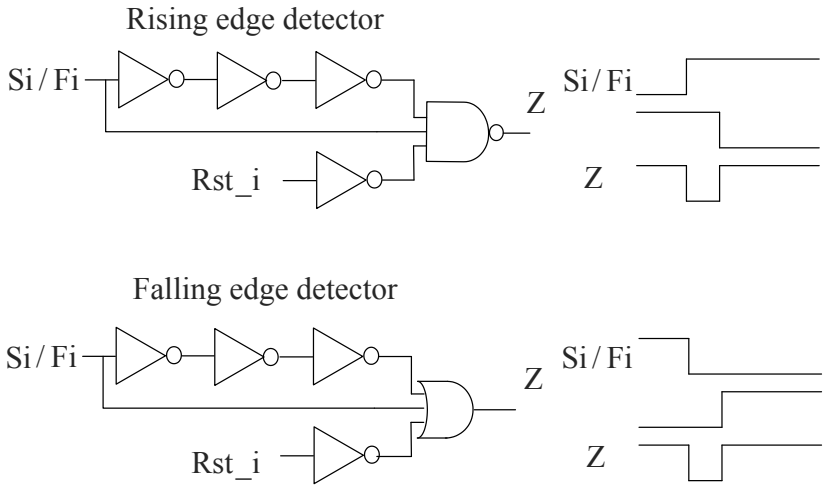


Fig.3.8 Simplified circuits of rising/falling edge detector

Fig.3.7 shows the schematics of arbiters used in the proposed VRTDC. Arbiter *A* and *B* are triggered by rising and falling edges, respectively. Both arbiters consist of a pair of edge detectors, two sets of reset circuits and a core comparator. They are reset by the signal applied to Rst_i every other lap during the propagation of the lead signal in the slow ring. The reset signal coming from the control logic will reset all the arbiters through the port Rst_e before a new measurement starts. As shown in Fig.3.8, the edge detector in both arbiters outputs a narrow negative pulse to set the arbiters and then release the control to the reset signals. The arbiter outputs "*0"* when the signal in the slow ring arrives first at Si, namely, the lag signal has not caught up to the lead signal yet. The arbiter outputs "*1"* when the signal in the fast ring arrives first at *Fi*, namely, the lag signal catches up to the lead signal. The first transition from zero to one at the arbiter output will be detected and used to latch the fine counter.

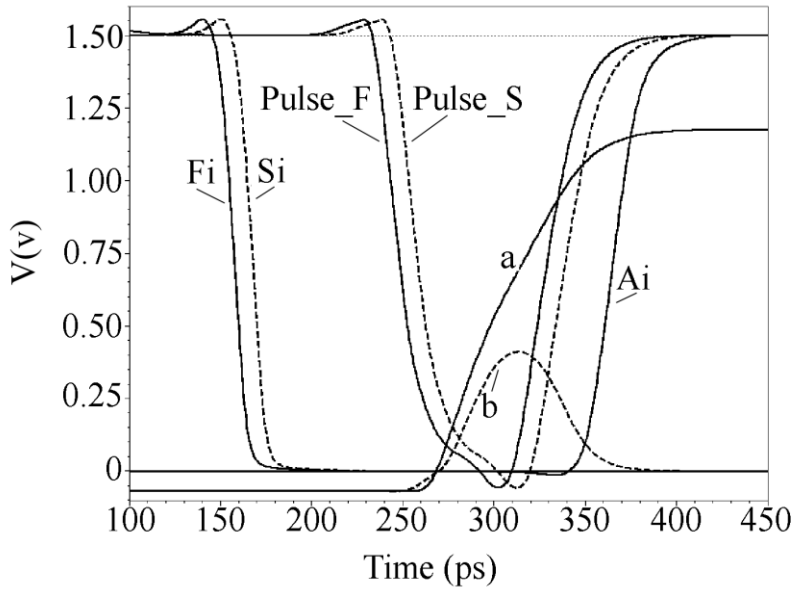


Fig.3.9 Transient simulation of arbiter B with the time interval between Si and Fi setting as 2ps

Fig.3.9 shows the transient simulation of arbiter B when the time interval between *Si* and *Fi* is set to 10ps. Pulse_F and Pulse_S start the core comparator by pulling both node a and node b to

"1" so that the positive feedback loop works then the comparator settles to a stable state. In this simulation, node *a* settles to a higher voltage than node *b* which is around three fourths of VDD, representing that the signal at *Fi* arrives first. A set of buffers are necessary to boost the voltage to VDD. **Ai** is the output of the arbiter. The input-output delay of the arbiter is critical to the TDC. This delay has a dependence on the time interval between two input signals, as shown in Fig.3.10. The arbiter delay increases dramatically when the time interval shrinks to less 1ps. The maximum delay of 369ps shown in Fig.3.10 is obtained at a time interval of 0.2ps. The arbiter delay eventually settles to around 200ps as the time interval increases.

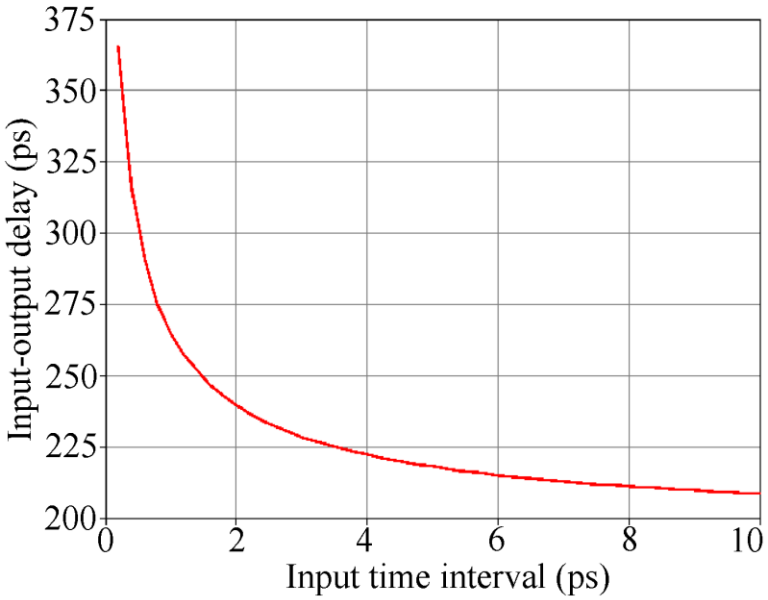


Fig.3.10 Dependence of arbiter delay on the time interval between two input signals

The arbiter needs to be reset before the next comparison starts. The reset signal comes from the output of the delay stage in the slow ring three stages ahead of the current one. Thus the arbiter is ready for comparison in a half period of the slow ring and is reset in another half period. There is always a current leakage path from VDD to ground for conventional arbiters without an edge detector during the reset half period [14], and this current leakage will waste power. In this

design, two types of edge detectors shut off this current leakage path in arbiters A and B. Two types of edge detectors will block the input edge when any reset signal is applied to Rst_i. The edge detectors also make the arbiter into a genuine edge-triggered device and distinguish the arbiter A from arbiter B. The narrow negative pulse can reduce the probability of overlap of negative pulse triggered by the lag signal at *Fi* and reset signal in an arbiter operating cycle so that it also reduces the probability of occurrence of current leakage path. In another word, the narrower the negative pulse can be, the less dynamic power will be consumed. However the narrow negative pulse must be wide enough to set the arbiter. The width of the negative pulse can be easily adjusted through the delay of the inverter chain in the edge detector.

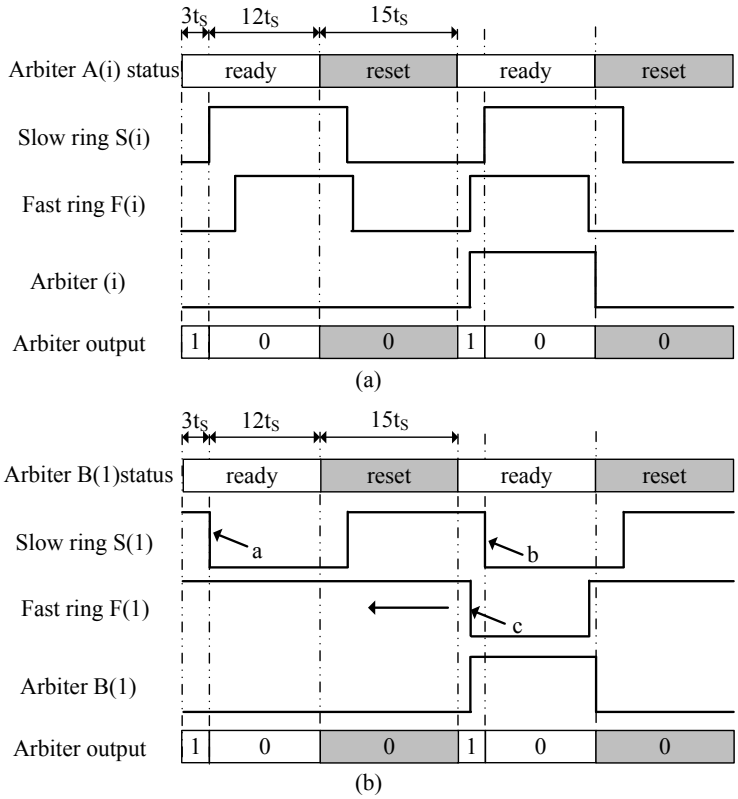


Fig.3.11 Illustration of (a) the operating cycle of arbiter A and (b) unexpected "01" transition at arbiter B(1)

Fig.3.11 (a) shows the operating cycle of arbiter A. The first half cycle is a ready cycle in which the arbiter is ready to receive input signals and judge the arriving timing sequence of them. The following half cycle is the reset cycle, in which the arbiter is reset to zero and the input signals are screened as well. As indicated in the figure, the arbiter will output zero when the rising edge of *F(i)* occurs in "0" zone and output one when it occurs in "1" zone. The process of the lag signal chasing the lead signal in the two rings can be viewed as the rising edge/falling edge of *F(i)* getting closer and closer to the edge of *S(i)* and eventually passing it. Each half period has a length of $15 * t_S$, in which the "1" zone and "0" zone have lengths of $3 * t_S$ and $12 * t_S$, respectively.

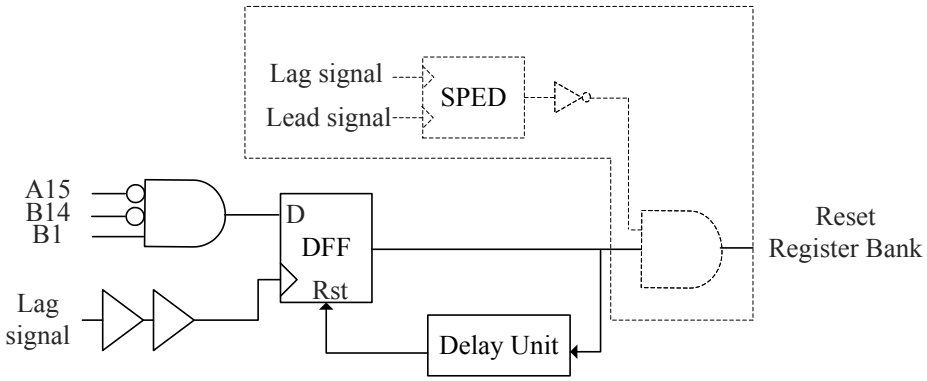


Fig.3.12 Block diagram of correction circuit

As shown in Fig.11 (b), an unexpected "01" transition is likely to occur at B(1) only when the lag signal happens to appear in the "1" zone during its first lap of propagation. Edge **c** is supposed to be compared with edge *a* by the arbiter B(1). Unfortunately this arbiter has been reset after it was set to zero by edge *a* . Therefore the edge is going to be compared with the next falling edge *b* at F_1. Arbiter B(1) and the following few arbiters will be set to "1". Moreover, arbiter A15 and B14 have been set to "0" before lag signal propagates in the fast ring. A "001" transition will be erroneously detected at the least significant bit of thermometer code. The

VRTDC would have mistakenly judged that the lag signal had caught up with the lead signal without proper error detection and correction circuits. This correction circuit will screen the "001" detection signal and keep edge *c* of the lag signal chasing edge *a* till the next catch-up happens. Fig.3.12 illustrates the block diagram of the correction circuit. The properly delayed lag signal will sample $\overline{B}_{14}\overline{A}_{15}B_1$ as soon as it is fed into the slow fast ring. Correction circuit will reset the register bank in the thermometer-to-binary encoder if the erroneous "001" code is detected. This reset signal will remain effective untill edge c in Fig.3.11(b) enters the reset area of arbiter.

As shown in Fig.3.10, the arbiter in pre-logic unit can resolve as tiny as 0.2ps time interval between two input signals, which should be digitized as "zero" time interval in the TDC output code. This arbiter should have very little chance of erronous switching when the two input signals are so close due to phase noise. In that case the lead signal will be fed into the fast ring and set first a few arbiters to zero before its edge enters the reset zone as the edge c shown in Fig.3.11(b). Similarly the correction circuit in Fig.3.12 also works since the $\overline{B}_{14}\overline{A}_{15}B_1 = 1$ is sampled by the lag signal. The lead signal will run away from the lag signal until it overpasses the lag signal the second time. Thus the measured result is $Ts - tin \approx Ts$, which will cause a spur in the TDC output and will be filtered out by the low pass filter in DPLL applications. As shown in Fig.3.12, an amendments can be made to the correction circuit to disable the reset of the register bank with an extra small phase error detector (SPED) when input time interval is very small. SPED will be introduced in Section III D.

Control logic in this design coordinates the entire system to work continually. Apart from the correction circuit decribed above, the control logic also sets up the timing for the read, reset and

output of the measurement results in the pipeline mode. It consists of correction logic, several delay lines and clock trees.

3.2.3 Thermometer-to-binary encoder

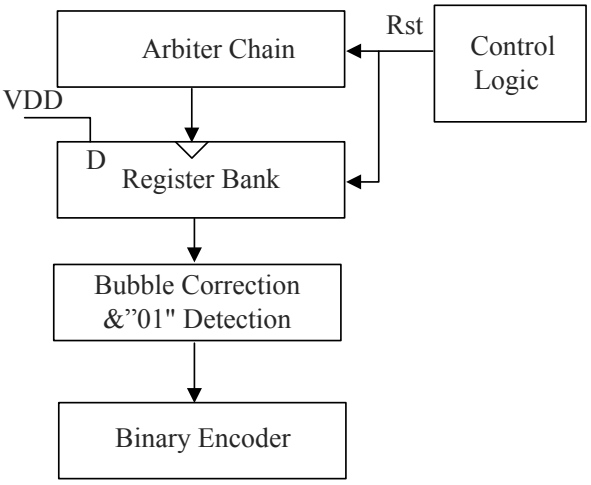


Fig.3.13 Block diagram of thermal-to-binary encoder

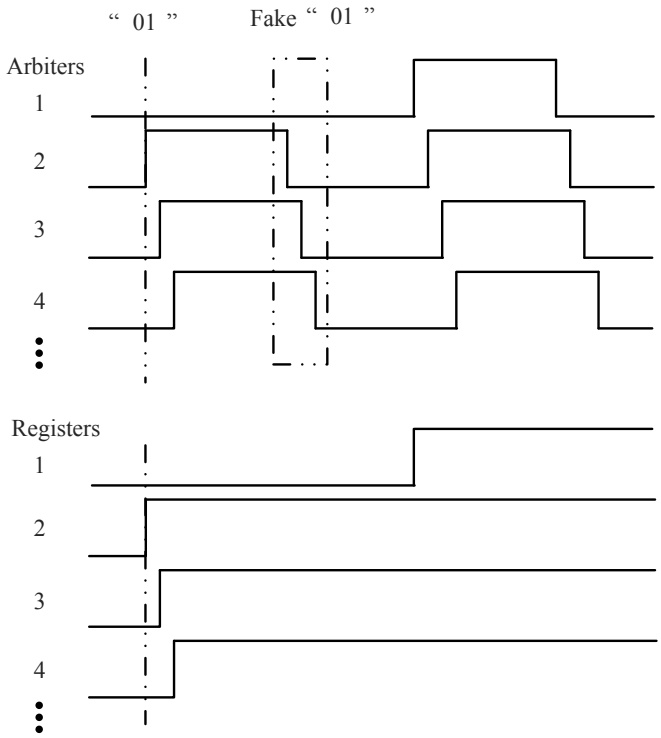


Fig.3.14 Timing diagram showing that register bank filters out the fake "01" at the falling edges.

As shown in Fig.3.13, the thermometer-to-binary encoder consists of a register bank, a bubble correction, a “01”detection circuit and a binary encoder. The outputs of the two arbiter chains are combined to form a 30-bit thermometer code. They are then converted to a 5-bit binary code for further processing by the evaluation unit. The outputs of the arbiters are periodical pulses with the same period as the fast ring after the lag signal catches up with the lead signal. The first “01” transition in the thermometer code will be detected by the “01”detection circuit. However there are many fake “01” transitions shown in Fig.3.14 at the falling edge of the arbiter outputs which have to be removed from the output of the VRTDC. A register bank is designed to filter out those falling edges of the arbiter outputs, thus eliminating the fake “01” transitions in the thermometer code. The register bank also stores the outputs of arbiters and partly eliminates the leakage problem in the arbiters, which often screws up the measurement in many low frequency applications. In addition, the proposed arbiters are reset every other lap at a frequency of several mega-hertz during the chasing process and device leakage should be negligible during the reset interval determined by the total delay of the slow ring. The arbiter outputs will not be monitored after the first “01” is detected, which means the device leakage does not limit the minimum operating frequency of the TDC. The two rings can be stopped when two external inputs of Vernier rings are reset to “0” after the catch-up. As mentioned before, the two rings need to be stopped when the measurement is finished. The ring can be stopped without causing extra propagating edges if the external input of NAND gate is reset during the period that another input to this NAND gate is “0”. The stop sequence of two rings is not of concern in this design since the arbiter outputs are screened by the register bank after the catch-up. However, the stop of two rings will be properly delayed to allow the correction circuit in Fig.3.12 to complete the detection.

Bubble correction is also necessary for the encoding. "*Bubble*" means that it is possible to have an "…00010111…" pattern in the thermometer code due to the delay mismatch in the each arbiter or a disturbance in the circuit causing the arbiter to take more time to settle. The bubble could occur when the single stage delay of the fast and slow rings is occasionally reversed as well as the time interval input to this delay pairs is less than the reversed delay difference of this pair of stages. Therefore the "…00010111…" pattern is most likely to occur in the vicinity where the real "01" transition happens. Similar to the bubble correction circuit in ADCs, the bubble correction is helpful to get rid of the errors in the thermometer code in VRTDC and relax the demand of matching in the arbiter and interconnecting wire layout. In order to simplify the design, a "001" detection circuit is used in this design. The "001"detector can suppress the bubbles in the thermometer code to some extent.

3.2.4 Counters and design redundancy

Fig.3.15 shows the small phase error detector (SPED) which outputs "1" if the time interval between two input signals is smaller than t_W. SPED consists of two arbiters with crossed inputs of lag signal and *S15*. Fig.3. 15 (b) and (c) illustrate the timing diagram of SPED, in which the *Si1*, *Fi2* and *Si2, Fi1* are inversely replicated, with a delay of t_W, of S15 and the lag signal, respectively. B1 will output "1" only if the Fi1 appears in the "1" zone of *B1* and *B2* will output "1"only if *Fi2* appears in the "1" zone of *B2*. As a result, Y is set to "1" only when the lag signal shows up in a small vicinity of *S15* as shown in Fig.3.15 (d). Area *B1* and *B2* are adjacent assuming the four inverters ideally have equal delay. Fig.3.15 (e) shows a slight overlap of *B1* and *B2* achieved by a small decrease of propagation delay Δ in the inverters in *Fi1* and *Fi2* input paths. At least one arbiter outputs "1" when the erroneous switching occurs due to the tiny time

interval between *S15* and lag signal. The overlap in the characteristics adds the redundancy to the design.

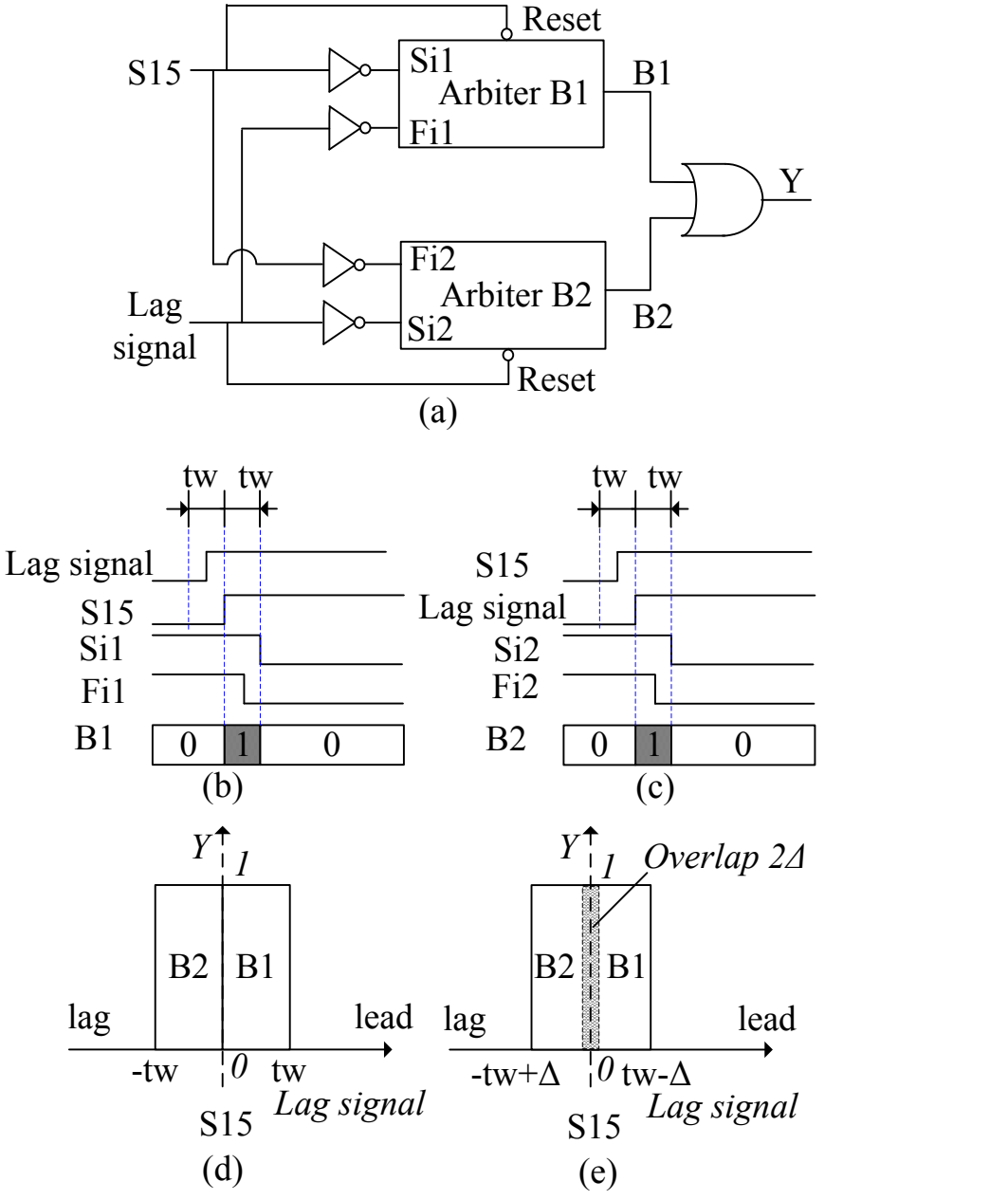


Fig.3.15 (a)The circuit of small phase error detector(SPED), (b,c) timing diagram of B1 and B2, (d,e) characteristics of SPED without and with overlap. (Horizontal axis indicates the time interval by which the lag signal leads or lags S15).

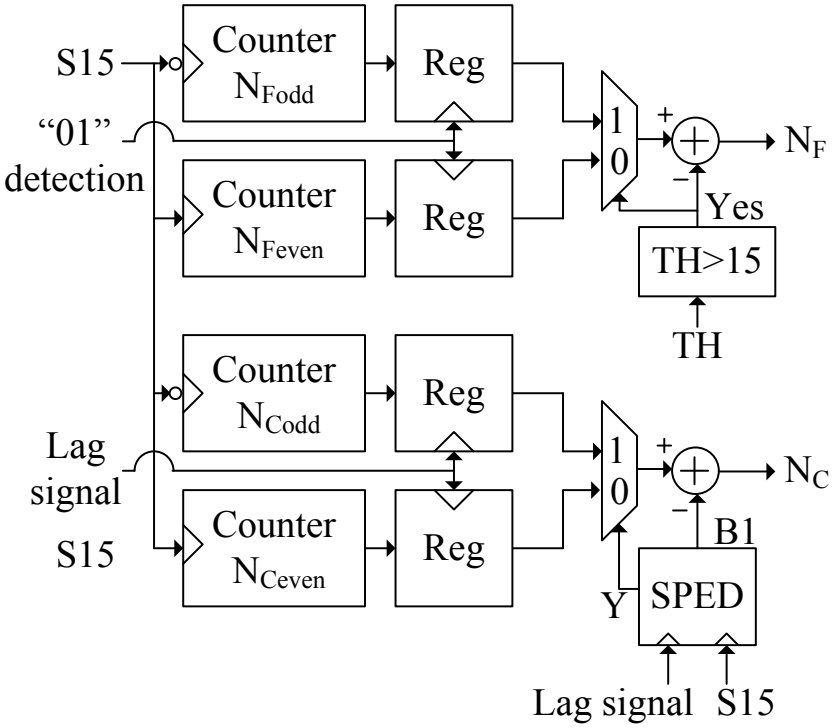


Fig.3.16 Counter design for redundancy

The counters N_C and N_F are triggered by the node *S15* in the Vernier ring as shown in Fig.3.2 and Fig.3.4. The missing-code may occur due to the propagation delay difference between Vernier ring to thermometer-to-binary encoder and Vernier ring to two counters, as well as delay difference between node *S15* to coarse counter N_C and the lag signal to N_C. These delay differences vary with input time intervals and are not easy to match. Two set of counters (N_C and N_F) have been used to tackle the missing code problem

Fig.3.16 shows the circuit diagram of the counters. N_{Ceven} and N_{Codd}, triggered by the rising and falling edges of *S15*, are used to count the number of even and odd laps that the lead signal has propagated before the lag signal's entry into the Vernier ring. N_{Ceven} will be selected by SPED when the lag signal is not close to the *S15*. Otherwise the N_{Codd} minus *B1* will be the result of N_C. *B1* will be set to "1" only when the lag signal leads *S15* by a small time interval and N_{Codd} is

larger than N_C by "1". Similarly, N_{Feven} will be selected when catch-up happens in the odd laps; otherwise N_{Codd} minus "1" will be the output of N_F. Counting all outputs of arbiters will be simple but consumes much more power than the presented double sets of counters with redundancy.

3.2.5 Delay stage

The design of delay stages is crucial to the performance of the VRTDC. Two identical rings are employed in this design to prevent the process variation from affecting the tiny difference in the propagation delay. In order to achieve a programmable delay difference, two different sets of bias voltages and control voltages are applied to the delay stages in the fast and slow rings, respectively. As shown in Fig.3.17, the NAND and inverter also have the same topology in each ring to reduce the variation of the time resolution due to the difference in circuit topology. This delay difference between two identical rings can cancel the first order PVT variation. The simulation results shown in Fig.3.18 and Fig.3.19 verified this cancellation.

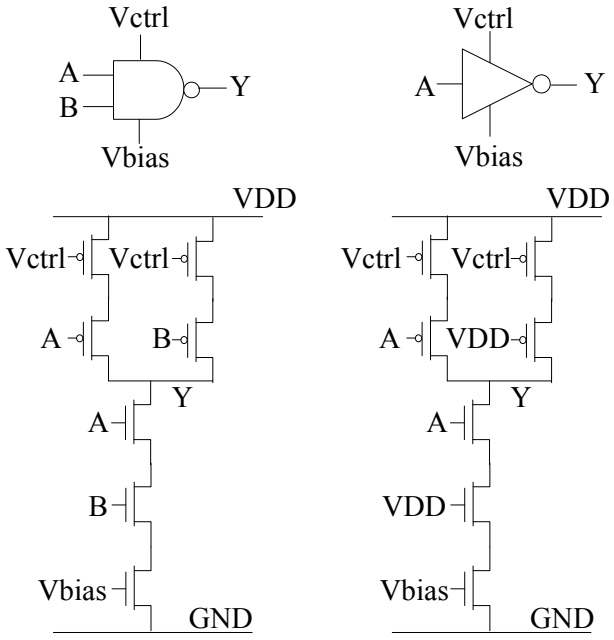


Fig.3.17 Simplified circuits of NAND and inverter.

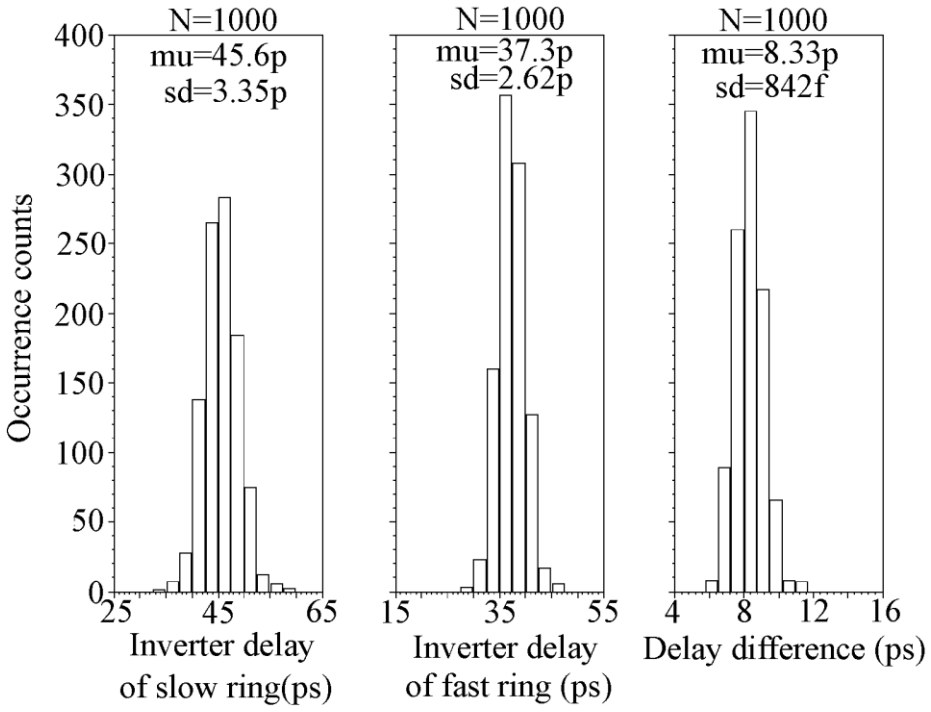


Fig.3.18 Dependence of the inverter delay and delay difference on the process variation.

Fig.3.18 shows the dependence of the inverter delay and delay difference on the temperature. The propagation delays of the inverters in the slow and fast ring exhibit temperature coefficients of 0.094 $ps/°C$ and 0.08 $ps/°C$, respectively. The temperature coefficient of the delay difference between two inverters is reduced to 0.014 $ps/°C$, which is only one sixth of that of the single inverter delay.

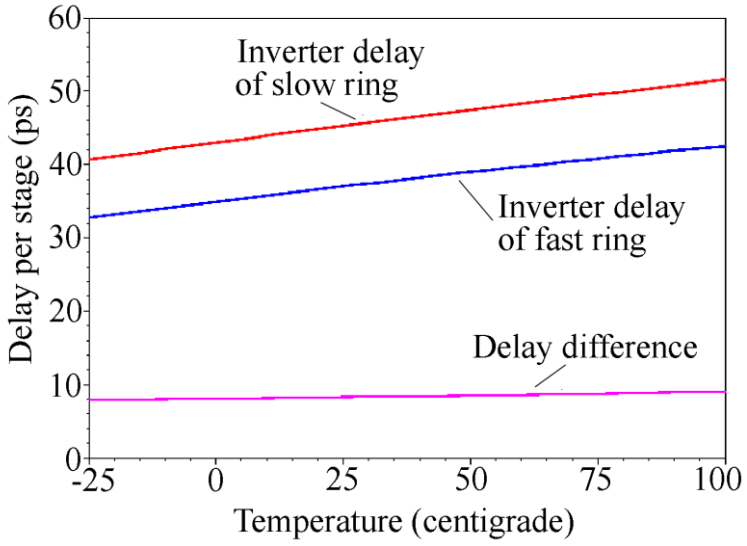


Fig.3.19 Dependence of the inverter delay and delay difference on the temperature.

Fig.3.19 illustrates the monte carlo analysis of the dependence of the inverter delay and delay difference on the process vialation. These two delays and delay difference are subject to Gaussian variations. The propagation delay of inverters in the slow and fast rings has a standard deviation of 3.35ps and 2.62ps, respectively. The standard deviation of the delay difference reduces to 0.84ps, which is only one third of that of both inverter delays. As known, Vernier TDC gains advantages over single-delay-line based TDC for its improved resolution and immunity to device mismatch. To first order accuracy, the mismatches between the Vernier delay chains are cancelled. In our design, the delay difference is obtained through different bias voltages applied to the two delay stages. These delay stages are designed with the same structure and the parameters. Therefore the process variations between two delay stages are correlated assuming the two stages are well matched and close enough in the layout. When two variations are totally independent, the delay difference variance can be calculated with the equation $\sqrt{\alpha^2+\beta^2}$, where α and β are the standard variation of two delays. The Monte Carlo analysis

justified that the standard variation of delay difference is much smaller than that of each stage delay due to symmetry.

The mismatch of delay pair is accumulated as INL from the beginning of the delay line. INL is dependent on the variance of element delay and the length of delay line [11]. Recycling delay line can be considered to shrink the length to reduce the INL, since the INL is viewed as zero at the end of line. Reduced INL can be easily verified in the case that the frequency of two delay rings is calibrated by DLL. The delay error caused by random noise, for instance jitter and power supply noise, will be accumulated as that in the conventional delay line TDC. However, the Vernier structure can cancel out the first order mismatch and common mode noise.

The identical delay stages using different bias voltages in Vernier rings are intended to compensate the PVT variations. For testing purpose, we brought tuning voltages *Vctrl* and *Vbias* off-chip for tunability. However, this approach suffers from noise coupling through the tuning voltages. The measured resolution was also largely degraded by the jitter performance of the test equipment. The bias condition that leads to a 2ps resolution in simulations obtains an 8ps resolution in measurement. In addition to noises from test equipment, PCB and package the resolution degradation is also affected by the loading effect of parasitic capacitances. In the measurement, the fine resolution smaller than 8 ps can be tuned with a higer *Vbias* close to *VDD* and a lower *Vctrl* approaching *GND* according to Fig.3.20. However the performance under those conditions is more sensitive to noise coupling from power supply and ground.

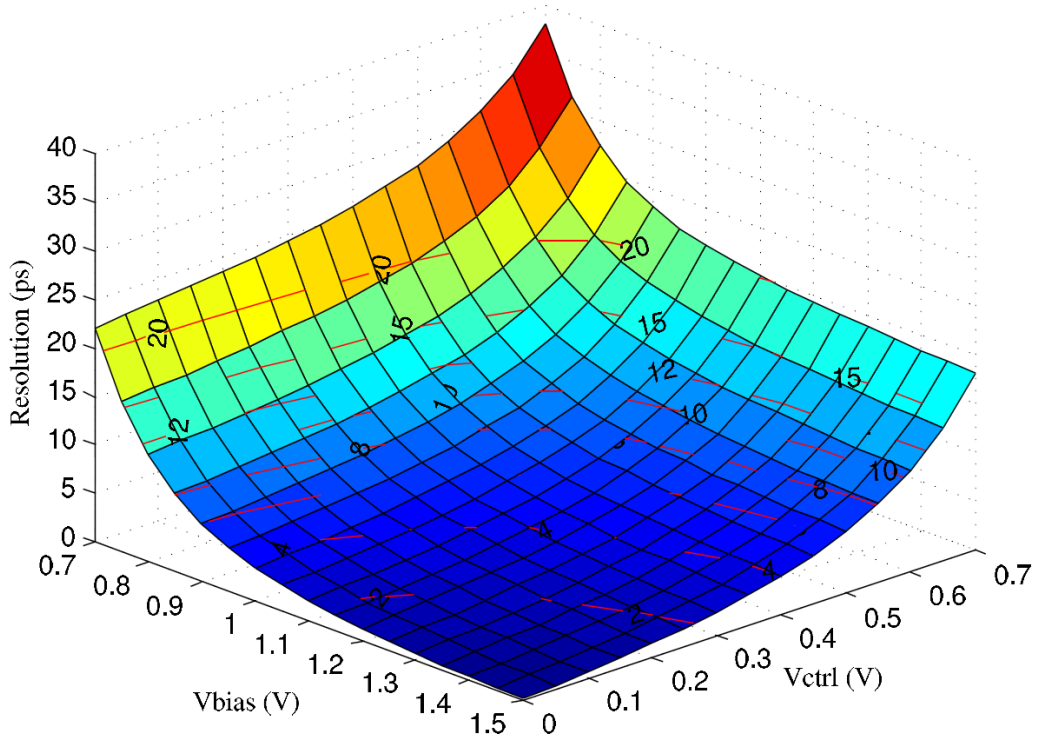


Fig.3.20 Dependence of resolution on Vbias and Vctrl.

3.3 Test setup and measurement results

The prototype of the VRTDC shown in the die photo Fig.3.21 was fabricated in 0.13µm CMOS technology. The chip has an area of 1x2mm^2 including the ESD pads and layer density filling elements. The VRTDC circuit occupies an area of only 0.75 x 0.35 mm^2. The VRTDC core has an area of 0.05mm^2. The other parts of the VRTDC occupy a large portion of the circuit area for testing purpose. The area of the VRTDC can be further shrunk when embedded in a DPLL chip. The entire TDC chip consumes 7.5mW from a 1.5V power supply while operating at 15 MSPS. The TDC prototypes were packaged using 44 pin LCC packages and the PCB test board was developed using FR402 laminate material, which has a loss tangent of 0.015 at 1GHz.

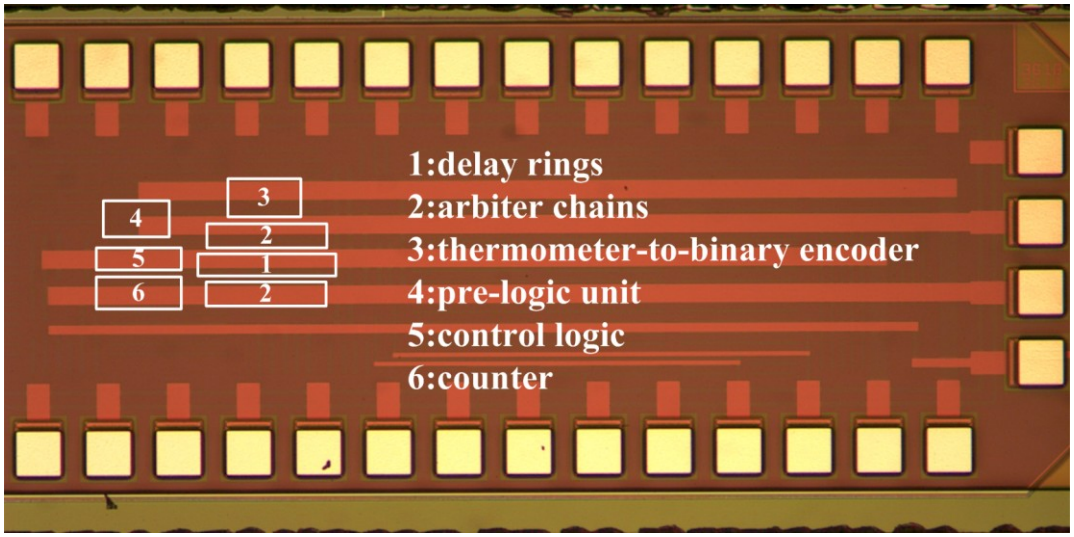


Fig.3.21 Die photo of the 12-bit Vernier ring TDC in 0.13um CMOS technology.

The test setup consists of two pulse generators, an arbitrary waveform generator, an Agilent logic analyzer and a PCB test board. Two types of test setup are employed to obtain the TDC transfer curve and sinusoidal delay sweep response. Fig.3.22(a) shows the test setup for measurement of the TDC transfer curve with a time interval ramp generated by two signals with a slight frequency difference at 15MHz. A logic analyzer was used to collect TDC outputs continually and display the output code for adjustment of control and bias voltage. In the test, an input time interval ramp is subject to the jitter and frequency stability of the signal source, the power supply noise and noise coupled from the PCB board and other environmental noise sources. Fig.3.22(b) illustrates a sinusoidally time-varying phase difference generated by the sinusoidal modulation in one channel. An Agilent 33220A 20MHz arbitrary waveform generator was used to provide the modulating signal of interest. The other channel was set with a fixed output delay.

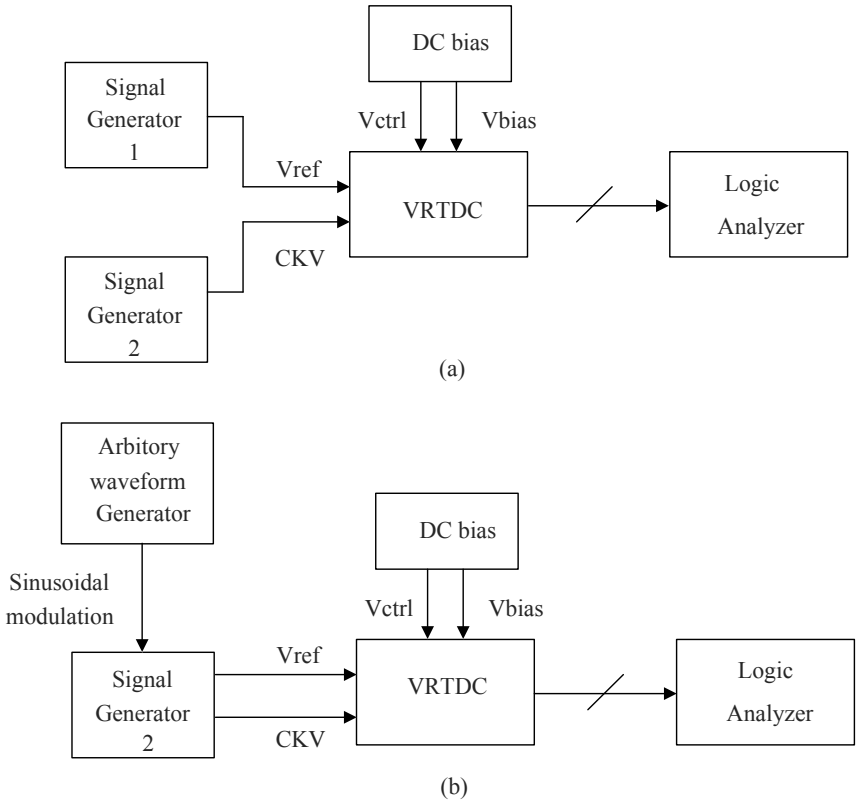


Fig.3.22 (a) Time interval ramp test setup (b) sinusoidal modulation of time interval.

Fig.3.23 (a) shows the TDC output measured with two inputs that have a fixed phase difference of 2.05ns plus a sinusoidally time-varying phase difference of 20ps peak-to-peak. The signal generator shown in Fig.3.22(b) outputs a clock of 15MHz at two channels. The output delay in one channel is modulated by a 100kHz sinusoidal signal. The other channel has a constant delay of 2.05ns. Sixty sequentially measured output codes were averaged to obtain the TDC output in the time domain. The measured TDC output correctly follows the input sinusoidal phase sweep when the time resolution was set to 10.2ps.

Fig.3.23 (b) shows the measured results of a fixed phase difference of 1.95ns plus a 40kHz 20 ps (p-p) sinusoidal delay sweep. The measured TDC output curve swings from 242.6 to 245.2 at a frequency of 40kHz and demonstrates that the TDC works well at a time resolution of 7.6ps, which was achieved by adjusting the delay difference between the two rings. The spurs in

Fig.3.23 are due to the harmonics of the distorted modulation signal generated by the arbitrary waveform generator or the nonlinearity of the delay modulation

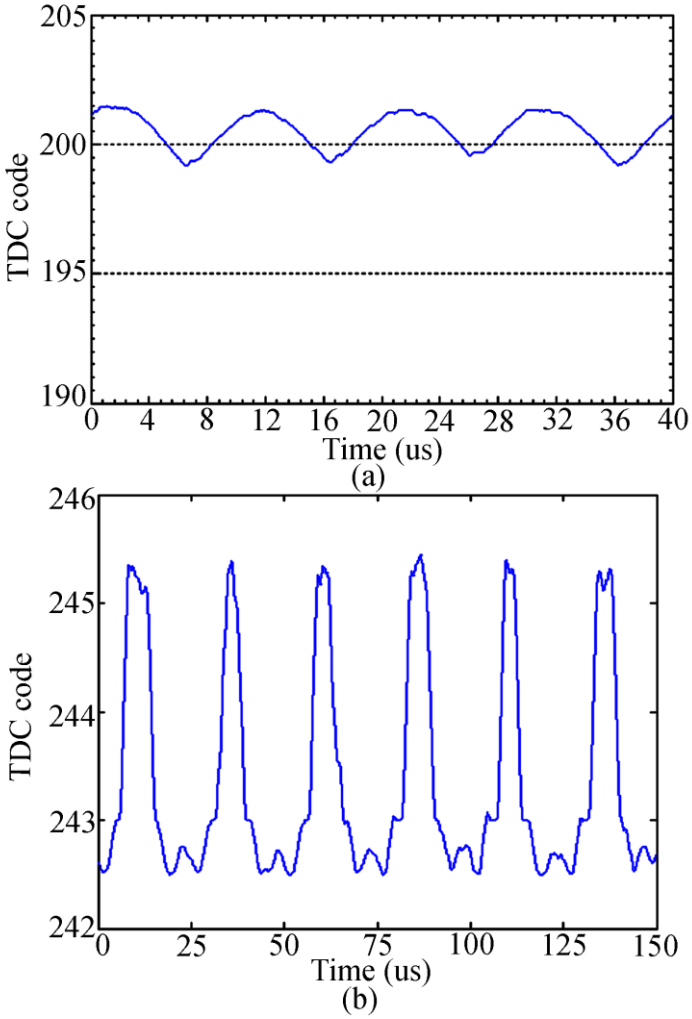


Fig.3.23 Measured TDC output with sinusoidal delay sweep 20 ps(p-p), (a) 100kHz with 2.05ns fixed delay and (b) 40kHz with 1.95ns fixed delay.

Fig.3.24 shows the measured power spectrum of the TDC output corresponding to the conditions used in Fig.3.23 (b). It demonstrates that the TDC output correctly follows the input time interval with its spectral energy concentrated at a single-tone frequency of 40 kHz, which is exactly the input phase-modulation frequency.

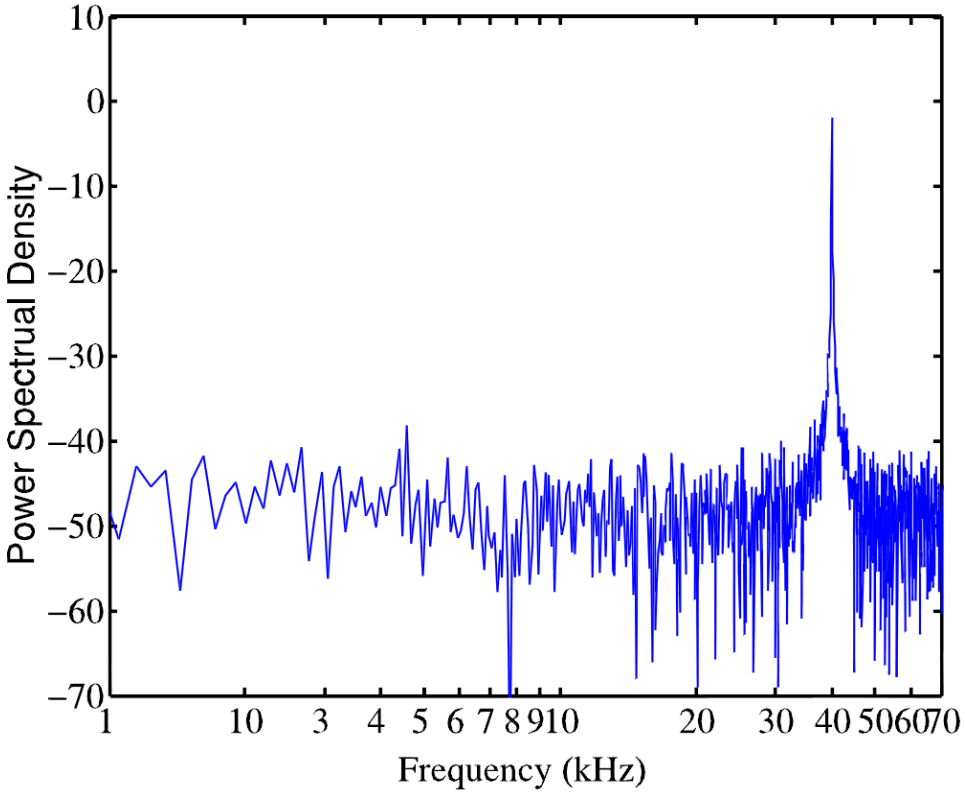


Fig.3.24 The power spectrum of TDC output in Fig.23 (b).

Fig.3.25 shows the measured TDC output after a median filter with 30x averaging. Two input signals with 2Hz frequency difference at 15MHz are applied to generate a ramp of time interval for the measurement of the TDC transfer curve. The input time interval, namely the period difference between two input signals, will increase or decrease 8.9fs every single pulse. The slope of the transfer curve indicates an average measured time resolution of 8ps. The measured time resolution of 8ps was limited by the available test equipment and test setup. Noise coupling from PCB/power supply and the frequency variation of the signal generators can affect the TDC test. The simulated TDC performance achieves better than 2ps resolution. Fig.3.26 gives the measured code distribution with a constant input time interval. It indicates that the standard deviation of the TDC output is less than 1-LSB for 256,000 tests.

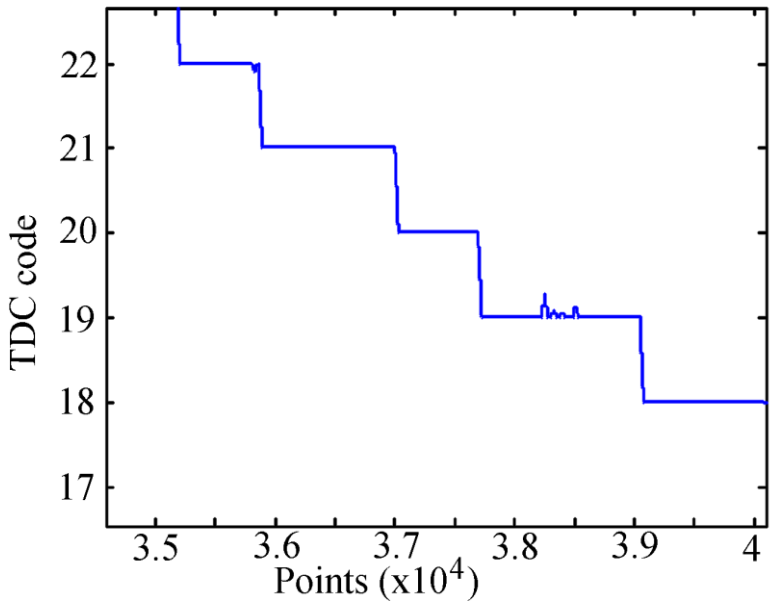


Fig.3.25 Measured TDC output after median filter with 30X averaging.

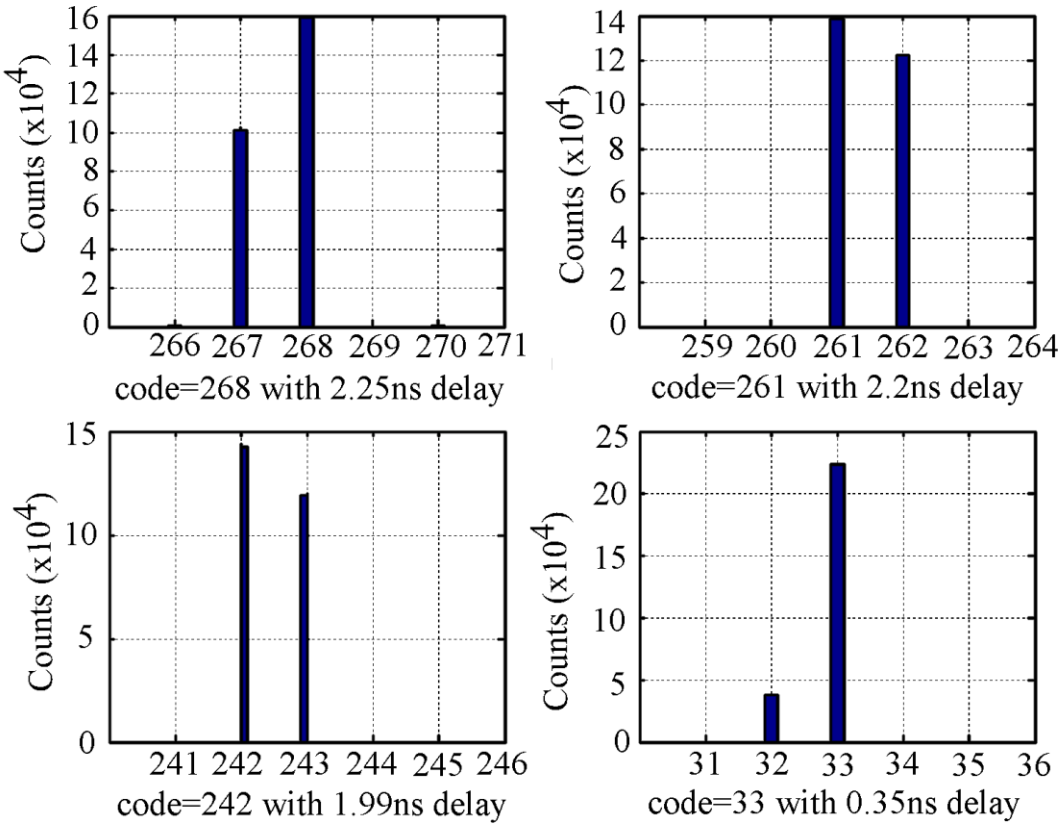


Fig.3.26 Measured TDC code distributions at 4 constant delays.

3.4 Summary of Vernier ring TDC

This dissertation presented a novel TDC architecture that places the Vernier delay cells in a ring format such that the delay chains can be reused for measuring large time intervals. The reuse of Vernier delay cells in a ring configuration achieves fine resolution and large detectable range simultaneously with small area and low power consumption. The proposed Vernier ring TDC, featuring 12-bit measuring range and 8-ps resolution, was implemented in a 0.13 μm CMOS technology. The core of the TDC circuit occupies an area of only 0.75 x 0.35 mm^2. The entire TDC chip consumes 7.5mW from a 1.5V power supply with operation frequency of 15 MSPS. Finally, Table I summarizes the performance comparison between the proposed work and recently reported TDCs.

Table 1 Performance Summary and Comparison of Vernier Ring TDCs.

Reference	[7]	[8]	[9]	[10]	[11]	[4]	This work
Sample Rate (MS/s)	130	10	50	180	5	26	15
Time resolution (ps)	24	1.25	6	4.7	12.2	20	8
Measuring range (bit)	8	9	11	7	14	5	12
Power Supply (V)	3-3.6	1	1.5	1.2	3.3	1.3	1.5
Power (mW)	<50	3	2.2-21	3.6	40	6.9	7.5
Technology(nm)	350	90	130	90	350	90	130
Area (mm2)	0.6	0.6	0.04	0.02	7.5	0.01	0.26

Chapter 4 3-dimensional Vernier Ring TDC

4.1 Concept of 3-dimensional Vernier ring TDC

Time resolution, detectable range, measurement time, power consumption and die area are most important concerns in TDC designs for all-digital phase-locked loop applications. Shrinking the time resolution has fueled the exploration of various TDC architectures recently [8][15][18]. Time-amplifier based two-step TDC amplifies the time residue and then quantizes it with a delay-line based coarse TDC [8]. Various Vernier TDCs have been implemented with fine resolutions. However, they all struggled with low efficiency, long testing time and high power consumption for measuring large time intervals. Recently a 2D Vernier structure was developed to reduce the number of delay stages required by linear TDCs [18]. Vernier ring TDC re-uses the hardware by placing the delay stages in a ring format and thus extends the detectable range without compromising the resolution [15]. To further improve the Vernier ring TDC (VR-TDC), This dissertation presents a 3-dimensional Vernier ring TDC that re-uses two delay rings and a comparator matrix. The proposed TDC greatly improves the measurement time, efficiency and power consumption. Moreover, it can achieve large detectable range without compromising the resolution.

To explain the concept of the proposed 3-D Vernier ring TDC, Fig.4.1 illustrates a delay-space that is composed of a slow-ring with 7 slow delay stages, a fast-ring with 5 fast delay stages and Z planes formed by comparator matrix. As shown, two delay axes with a comparator matrix form

a 2-D delay plane. While the delay plane can be extended to a 3-D delay space by adding more 2-D delay planes, we implemented the 3-D space by connecting the Venier delay chains to form Vernier delay rings and reusing comparator matrix. The propagation delay per stage in the slow and fast rings are t_S and t_F respectively. The exemplary 3-dimensional Vernier ring TDC evolves from a 5-stage VR-TDC [3] by extending the slow-ring to 7-stages and adding two comparator columns to the right-side of the existing comparator line (labeled with red) to form a 2-dimensional comparator matrix. The 2D placement of the comparator array extends the detectable range from 5R to 15R comparing to conventional Vernier TDC, where $R = t_S - t_F$ is TDC time resolution.

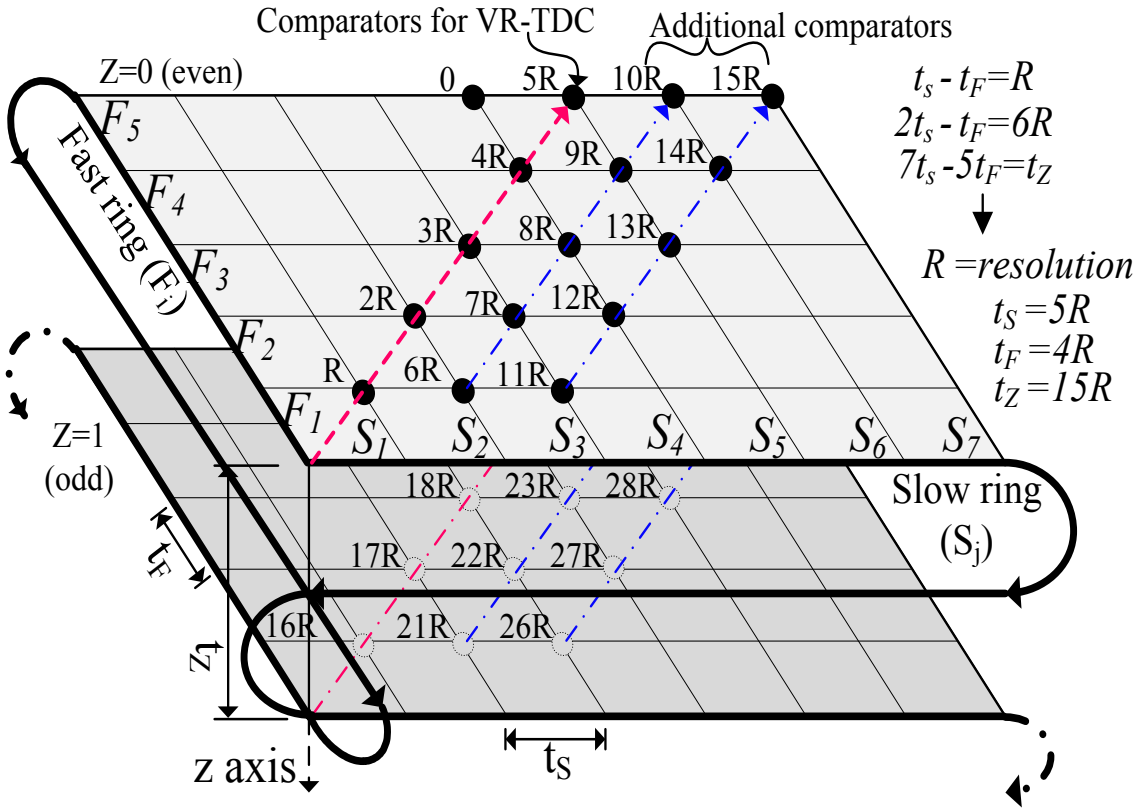


Fig.4.1 Conceptual view of 3-D Vernier delay-space

Assuming two input signals start their propagations from the origin on the plane Z=0 along two rings. The 2D comparator array compares the edges of two signals in fast- and slow-rings every lap. If the lag signal propagating along the fast-ring doesn't catch up with the lead signal propagating along the slow-ring after one lap of propagation, i.e., the input time interval is larger than 15R, the race goes into the 2nd lap with re-use of the delay rings and the comparators. In this scenario, the race in the 2nd lap is represented in the delay-space using another plane denoted Z=1, where the detectable range goes from 16R to 30R. The re-use of hardware will continue until the catch occurs and the delay-space can theoretically contain any number of planes. Similar to Vernier ring TDC, a large time interval is first interpolated with coarse resolution, i.e., the period of slow-ring prior to the arrival of the lag signal at TDC input. After lag signal arrives, the residue of the coarse interpolation will be automatically quantized with a fine resolution, which is the delay difference between fast- and slow-stages. Thus, the maximum detectable range of the proposed TDC can be infinitely large without sacrificing the fine resolution. The delay difference detected by a comparator located at (i, j, z) in delay-space is given by

$$D(i,j,z) = j \cdot t_S - i \cdot t_F + z \cdot (7t_S - 5t_F) = i \cdot R + (j-i)t_S + z \cdot t_Z \qquad (4.1)$$

where i, j, z are the coordinates in exemplary delay-space. R is the minimum time interval and $t_Z = 7t_S - 5t_F = 15R$ is the maximum time interval detected by the comparator array on the same Z-plane. The delay difference in all Z-planes becomes a monotonic function without overlap when $2t_S - t_F = 6R$ and $7t_S - 5t_F = 15R$.

4.2 Circuit implementation of 3-dimensional Vernier ring TDC

4.2.1 3-D Vernier ring TDC core

Based on the concept proposed above, we implemented a novel Vernier ring TDC chip that contains 10 fast stages, 12 slow stages, two MUXs and 62 DFF comparators, as shown in Fig.4.2. DFF1 to DFF30 works in the odd laps while DFF31 to DFF61 operates in the even laps since output of each delay stage toggles between rising and falling edges when two signals are propagating in two rings lap by lap. The implemented Vernier TDC chip can detect a minimum time interval of R that is set by the delay difference of two Vernier rings and can be programmed to a very small delay. Without increasing the delay stages and comparators, this TDC can measure very large time intervals as long as the counters have sufficient number of bits to hold the data. Unlike the conventional Vernier TDC that requires large testing time to measure large time interval, the measurement time for the proposed 3-dimensional Vernier ring TDC has been reduced. For instance, the time taken to measure the time interval of 30R requires only propagating 12 delay stages instead of 30 stages needed by a conventional Vernier TDC.

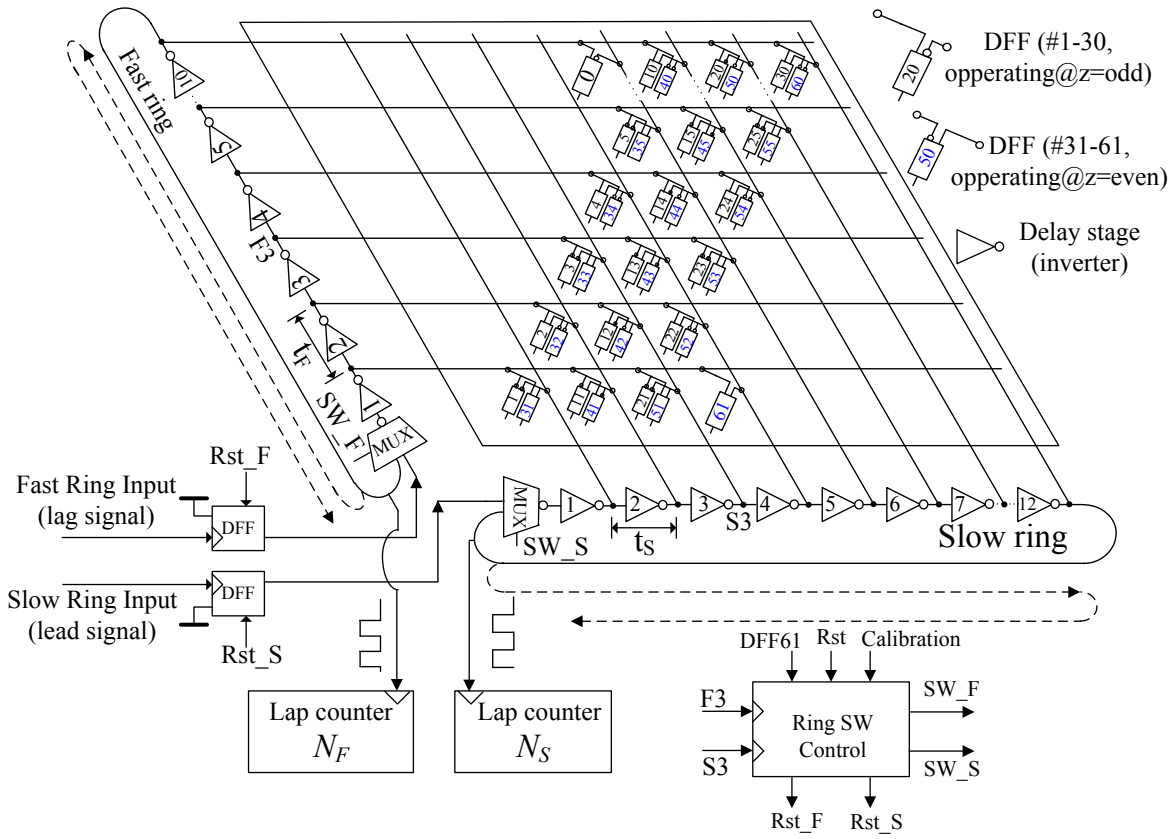


Fig.4.2 Block diagram of the proposed Vernier ring TDC core

Also included in the TDC core are two input-DFFs, a ring switch control unit, a fast-ring lap counter (NF) and a slow-ring lap counter (NS). Initially control signal SW_S and SW_F switch two MUXs to feed input lead signal and lag signal into the slow ring and fast ring, respectively. After around 3 inverter-delays, rising edges at F3 and S3 trigger two MUXs to switch to the outputs of the last stages of two rings to close two rings. This enables two input signals to propagate in the rings lap by lap until the lag signal catches up with the lead signal. When the catch occurs, two MUXs are switched back to the ring inputs to break two rings. Meanwhile, two input-DFFs are also reset by the first rising edges at F3 and S3. The propagating signals then stop at the end stages of two rings and the TDC core are ready for the next measuring cycle. To avoid causing unexpected toggle of delay stages when two MUXs switch back to the initial positions,

the output of two DFFs need to be reset to "zero" before breaking two rings. Two input DFFs are used to isolate two delay rings from the input signals when two rings are cut off.

The mechanism of breaking two rings will greatly simplify the design and save power. For the ring delay structure, counting the lap number is a challenge to the design. The delay variation between the triggering signal and stop signal of a counter may cause the miscoding of lap number. For instance, the triggering signal of the slow-ring lap counter (NS) is from S12 while the stop signal is activated by detection of the catch-up. The catch-up could occur at any stage in the slow ring. Breaking two rings can simplify the redundant circuitry to avoid miscoding [3].

As we know in the conventional Vernier delay line TDC, two signals will propagate same number of delay stages before the lag signal catches up with the lead signal. In the proposed Vernier TDC, two lap counters (*NF* and *NS*) record the number of laps that the signals have propagated in each ring before the catch-up happens. The number of laps that two signals have propagated during the fine interpolation should be equal since the two rings are disconnected immediately after the catch-up is detected. Therefore, the difference between two counters, namely NS-NF, is the number of propagation laps in the coarse interpolation while the NF is the number of propagation laps in the fine interpolation. Detecting the catch-up before two signals passing the MUXs is critical for the design. We find the delay difference between delay stages F1 and S4 is equal to the one between F1 and S1 in the next lap. DFF61 is connected to the outputs of F1 and S4. A "01" transition at DFF61 output indicates the catch-up happens at the very lap and the detection is 9 fast-stages ahead of the switches, which relaxes the timing requirement of the ring-switch-control unit. Thus DFF61 can be used to monitor the catch-up of the two signals.

As discussed above, a quantitative relationship between the delay-per-stage of two rings, t_S and t_F, need to be guaranteed to ensure that there is neither overlap nor gap in detectable range (DR) between two adjacent comparator columns. For example, the dateable range of the first and second columns of the comparator array are $(t_S - t_F) \le DR_1 \le 10(t_S - t_F)$ and $2t_S - t_F \le DR_2 \le t_S + 10(t_S - t_F)$, respectively. Thus $t_S = 10(t_S - t_F) = 10R$ and $t_F = 9R$ where $R = (t_S - t_F)$. The validity of these equations might be dependent on the process, voltage and temperature variation. Hence calibration is necessary for the proposed Vernier TDC. DFF0 is employed to calibrate the delay-per-stage in the fast-ring [2] to ensure that $9t_S = 10t_F$. Consequently, as shown in Fig.4.3, $t_S = 10R$, $t_F = 9R$ and $t_Z = 12t_S - 10t_F = 30R$. The period of the slow-ring is $24t_S + 2t_{SW}$, which is the coarse resolution of the TDC.

Fig.4.3 (a) depicts the block diagram of the proposed Vernier TDC chip. The pre-logic unit determines the lead and lag signals from the reference clock and feedback signal, then switches the lead signal to the slow ring and the lag signal to the fast ring, and outputs a sign bit [3]. The splitter generates differential signals for the use of the following differential TDC core. The outputs of 61 DFFs (1-61) are combined into a 61-bit thermometer code to find the location where the “01” transition happens.

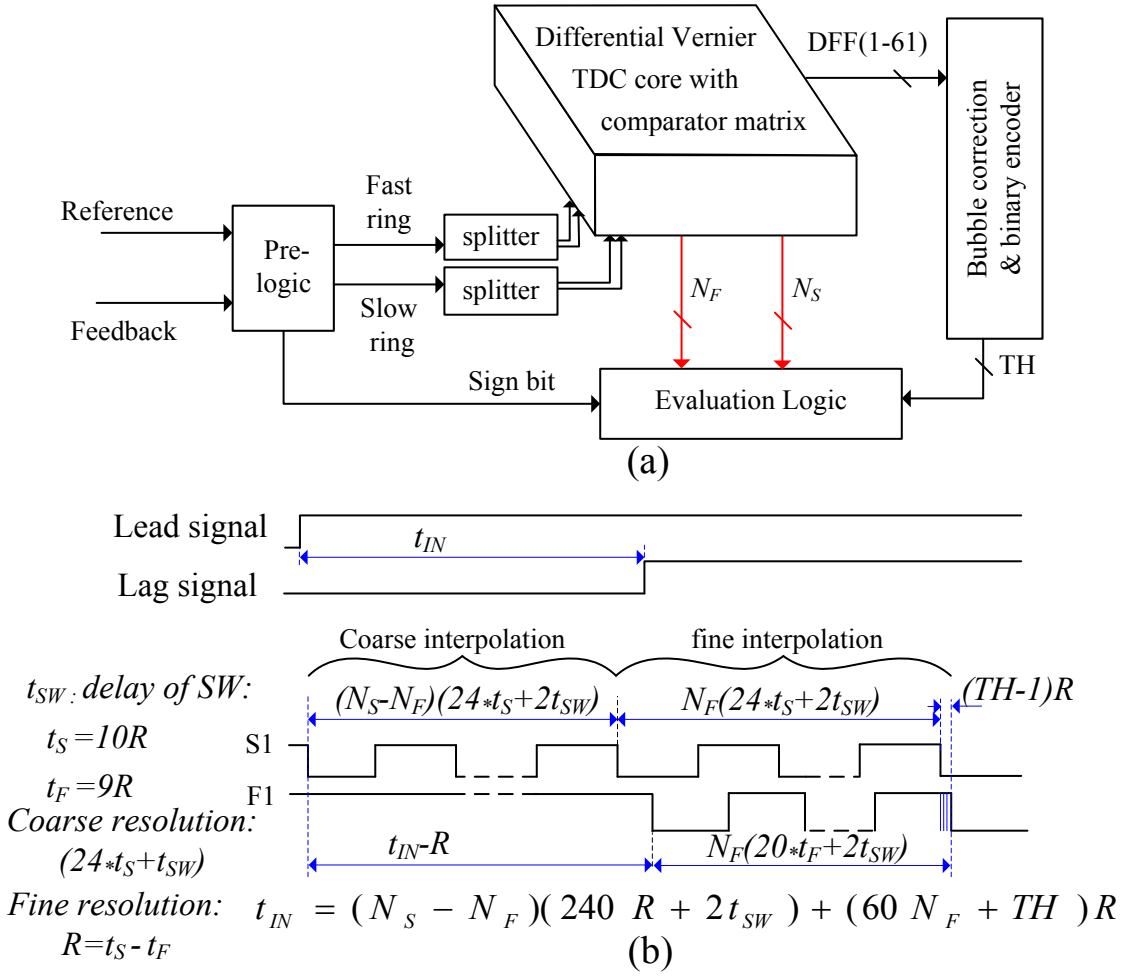


Fig.4.3 (a) Block and (b) timing diagrams of the proposed TDC chip.

Similar to any other thermometer-code-encoding circuits, the disturbance in the circuit and the variation of delay-per-stage in either fast or slow ring may cause the bubble pattern, for instance "…00010111…", in the thermometer code. The bubble correction circuit built with the following logic equation will not only get rid of the erroneous encoding, but also detect the real "01" transition and output "one" at the corresponding bit.

$$BC_{(i)} = (DFF_{(i-1)} \oplus DFF_{(i+2)}) \bullet (DFF_{(i)} \oplus DFF_{(i+1)}) \qquad (4.2)$$

Then the outputs of bubble correction circuit are converted to a 6-bit binary code TH.

Fig.4.3(b) shows the timing diagram of the 3-dimensional Vernier ring TDC. This diagram indicates the measured input time interval consists of two parts. The first part is coarse interpolation result $(N_S - N_F)(240R + 2t_{SW})$ while the second part is the fine interpolation result $(60N_F + TH)R$. Thus, the input time interval can be represented by

$$t_{IN} = \pm[(N_S - N_F)(240R + 2t_{SW}) + (60N_F + TH)R] \qquad (4.3)$$

where the polarity is determined by the sign bit of pre-logic unit and the t_{SW} is the propagation delay of the MUX.

4.2.2 Circuits of the main building blocks

Fig.4.4-4.6 gives the circuits of the main building blocks of the TDC. The circuit of pre-logic unit is shown in Fig.4.4(a). The comparator in the pre-logic unit determines whether the reference signal leads or lags behind the feedback signal and outputs the sign bit. The comparator then is reset after both reference and feedback signals arrive at end stages. Fig.4.4(b) shows the circuit of splitter which converts a single-ended signal to a differential signal. The transmission gate can compensate the delay of the first inverter in lower delay line. Two Schmitt trigger circuits are embedded in the splitter to increase noise immunity.

Fig.4.5 shows circuits of delay stage and differential DFF. The pseudo-differential inverter is employed as delay stage to suppress the common mode power supply noise. Also the DNL due to unmatched strength between pull-up and pull-down in the delay stage will be improved since each stage outputs both rising and falling edges. The inverter delay can be fine tuned by Vctrl and Vbias, or coarsely adjusted through E1-E2 turning on or off binary- weighted current sources and sinks. For testing purpose, we brought tuning voltages Vctrl and Vbias off-chip for

tenability. As shown in Fig.4.5(b), the differential DFF operates as the phase error comparator in the proposed TDC. Compared to the arbiter structure in the Vernier ring TDC, this differential DFF does not need be reset every lap when determining the sequence of arrival, which greatly simplified the design of TDC. The presented differential DFF also features a matched delay between two complementary signals.

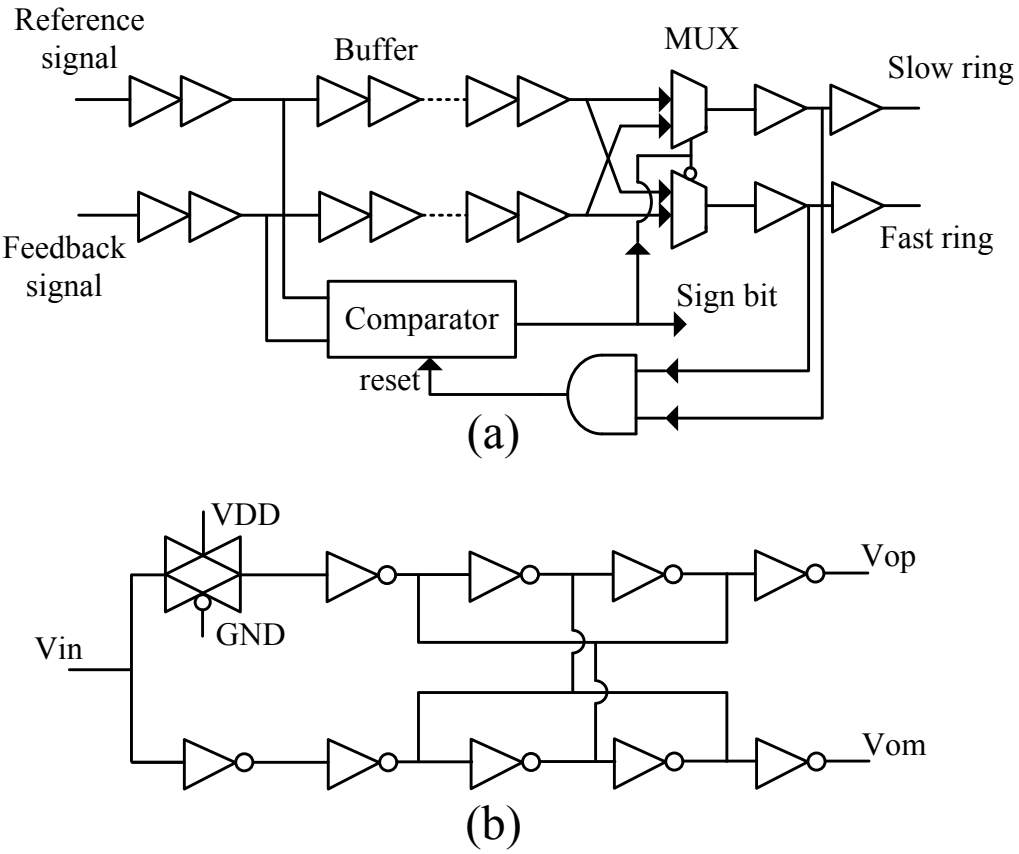


Fig.4.4 Block diagram of the proposed Vernier ring TDC core

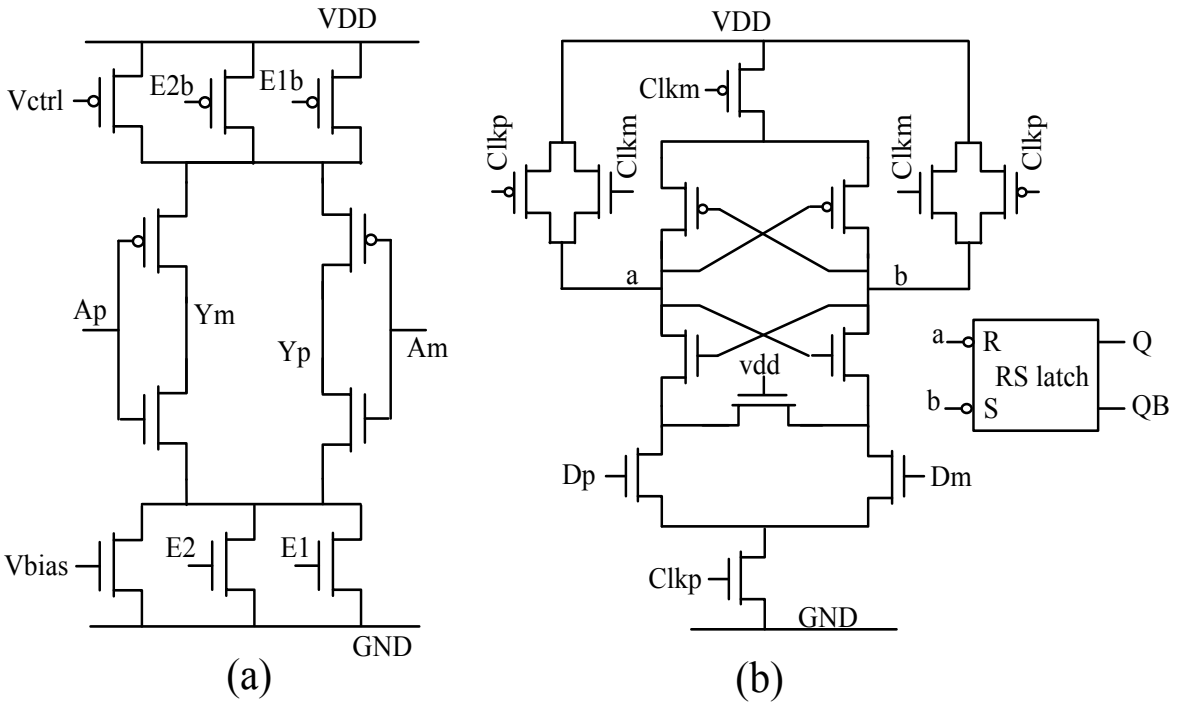


Fig.4.5 Circuits of (a) delay stage and (b) differential DFF

Fig.4.6 depicts the simplified circuit and symbol of the ring switch control unit. Two DFFs are used to keep the status of MUX-control-signal SW_F and SW_S. In every operation cycle, these two DFFs will be reset by a global reset signal "Rst" before lead and lag signals come to the inputs of TDC core. After the lead and lag signals first time arrives at the 3rd delay stage of each ring, the rising edge of the 3rd delay stage output (S3 or F3) will trigger the corresponding DFF. These DFFs will output "one" to close the rings when the "calibration" is disabled (set to logic "zero"). In addition, the "01" transition at the DFF61 will reset the two DFFs in the switch control unit therefore break two rings to terminate the propagation of both lead and lag signals. When TDC works in the calibration mode, the two rings are always cut off since two DFFs will output "zero" all the time.

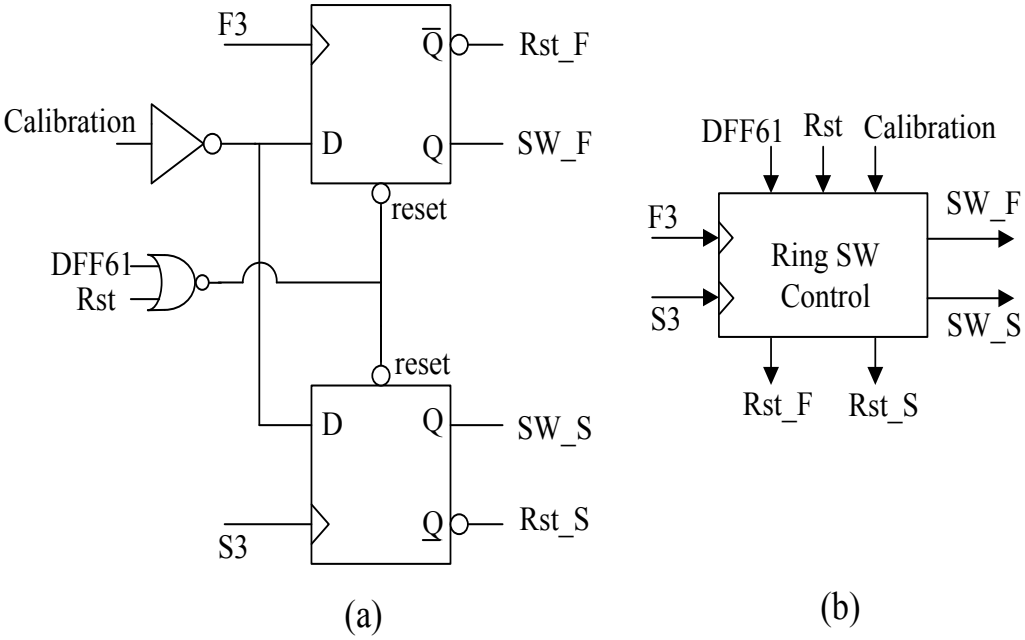


Fig.4.6 (a)Simplified circuit and (b)symbol of ring switch control unit

4.2.3 Chip information and measurement results

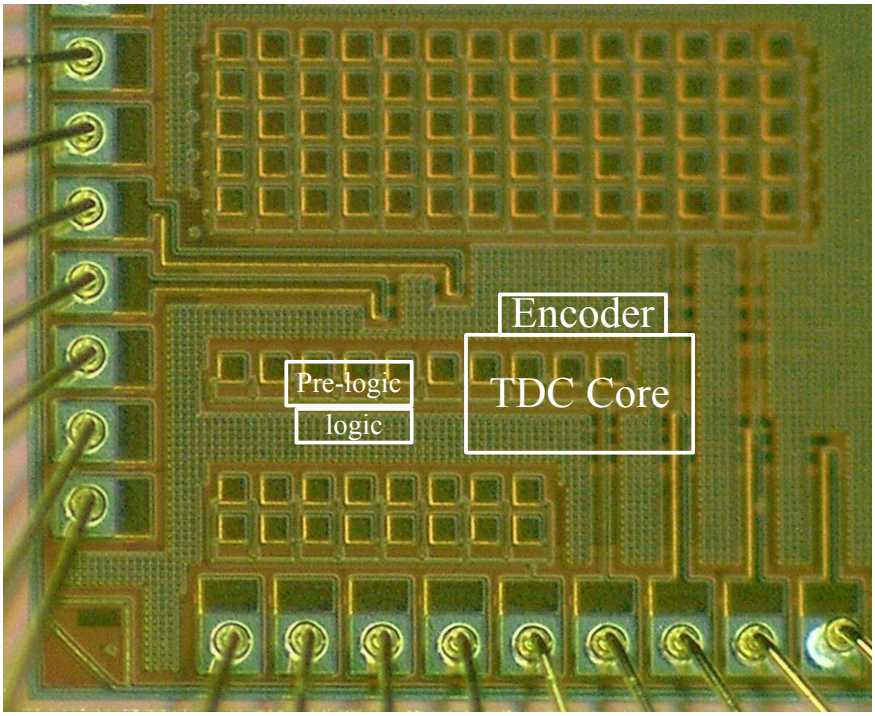
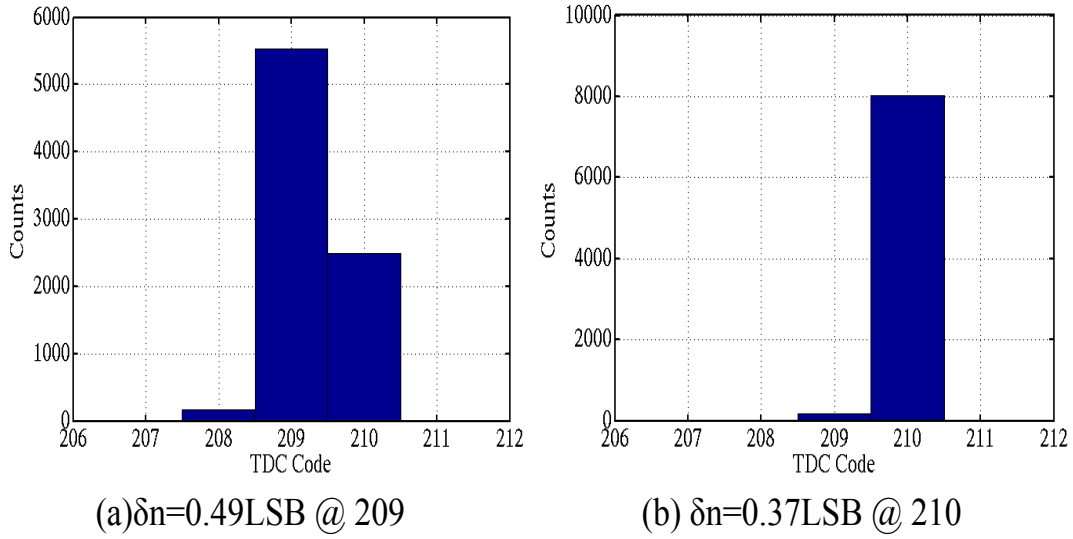


Fig.4.7 Chip photo of the proposed TDC

The prototype of the TDC was implemented in 0.13μm CMOS technology. Fig.4.7 shows the chip photo of the proposed TDC. The TDC core occupies 0.11 mm2 while TDC total area is 0.16 mm^2. The TDC chip consumes only 4.5mW under a 1.5V power supply while operating at 15 MSPS. Compared to the Vernier ring TDC [3], the proposed 3-dimensional Vernier TDC improves measurement efficiency, area and power consumption. Compared to 2D Vernier TDC [2], the proposed TDC also extends the detectable range by employing Vernier rings for hardware re-use.



(a)δn=0.49LSB @ 209 (b) δn=0.37LSB @ 210

Fig.4.8 Measured TDC output code distribution.

Fig.4.8(a, b) shows the measured TDC output code distributions for two inputs with constant delays. The standard deviation of two distributions (code 209 and 210), each with total 8096 hits, are 0.49LSB and 0.37LSB, respectively. The distributions indicate a good stability of the proposed structure. Fig.4.9 shows the measured TDC transfer characteristics with a time resolution of 16.5ps. A ramp of phase differences between two input signals, with a step size of 2ps, was fed into the proposed TDC to generate a ramp of TDC output codes. Note that the

measured TDC characteristic curve is affected by the noise coupled from PCB board and the jitter of the available test equipments. The proposed Vernier TDC is capable of measuring a very large time interval almost without extra hardware cost. According to (3), the detectable range is mainly determined by the bit number of the slow-ring lap counter (NS). The proved detectable range shown in Fig.4.9 is greater than 8 bits.

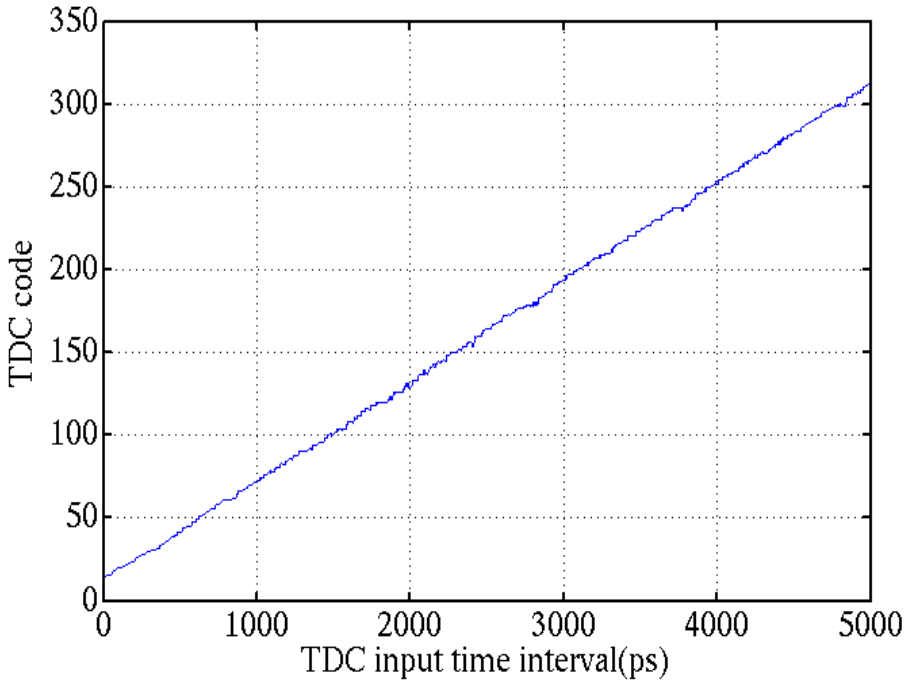


Fig.4.9 Measured TDC characteristics of 3-D Vernier ring TDC

Chapter 5 On-Chip Jitter Measurement Using Vernier Ring TDC

5.1 Introduction of on-chip jitter measurement

With the development of the process scaling down, the clock frequency of the communication systems keeps growing and the deviation of signal and clock from ideal position, namely jitter, becomes a severe issue since the jitter tolerant budget shrinks with the increase of clock speed. Consequently, jitter measurement is necessary but difficult to implement. The measurement using external automatic test equipments and on-chip driver can hardly achieve the results as accurate and efficient as the on-chip jitter measurement provides. It is also hard to take the deep-embedded signal out of the chip without being polluted by the environmental noise. On-chip jitter measurement can circumvent these problems and offer an easy and inexpensive BIST solution. In addition, monitoring the jitter performance locally can provide feedback mechanisms for self-healing, which is one of the most appealing techniques at ultra-deep-submicron process nodes. With the built-in jitter measurement circuit, the frequency synthesizer, including all digital phase-locked loop (DPLL), can self-adjust loop parameters and generate a clock with the optimized jitter performance.

Recently, the time-to-digital converters (TDCs) have been used in many on-chip jitter measurement macros and BIST applications[19][20][21]. Time-to-digital converter quantizes the time interval between the clock and reference signal with a time resolution as tiny as several

pico-seconds (ps). The histogram of the digitized time intervals obtained in the successive measurements reflects the distribution of the clock jitter assuming the reference signal is jitter free. The interval histogram can be easily processed by the digital signal processing algorism to characterize the jitter performance of the clock signal. The time resolution and detectable range of the TDC are critical to the on-chip jitter measurement. Many TDC architectures have been reported to improve time resolution, detectable range or both. The digital inverter is widely used in the time-to-digital converter to digitize the time interval due to its digital-intensive design approach. The inverter delay thus becomes a basic scale in the quantization of time interval[4].

The Vernier delay line is still an attractive structure for the implementation of a high performance TDC, although there are many new techniques invented to improve the time resolution of TDC. Vernier ring TDC places the delay cells in the ring format to achieve the small resolution and large detectable range simultaneously by reusing the hardware.

The jitter of signal under test is usually compared with an approximately jitter-free reference clock. The phase error between two signals can vary in the range of one period of the test signal. Therefore, a large detectable range with a fine resolution TDC is desired in measuring the jitter of a low frequency signal. This dissertation presents the on-chip measurement scheme utilizing VR TDC, the fine resolution and large detectable range solution compared with other TDC designs.

This chapter is organized as follows: section II describes the Vernier ring TDC architecture and explains the on-chip jitter measurement using this novel TDC. Section III describes the application of this jitter measurement technique in the DPLL to achieve loop dynamics

adjustment. Section IV gives experimental results for a proposed jitter-measurement scheme using VR TDC fabricated in 0.13μm CMOS process. Conclusions will be drawn in section V.

5.2 Jitter measurement using Vernier ring TDC

The Vernier Ring TDC (VRTDC) leverages the time difference between two rings of delay cells to achieve a sub-gate-delay time resolution. Unlike the conventional Vernier delay line TDC, VR TDC places the Vernier delay stages in a ring format such that the delay chains can be reused for measuring large time intervals. Arbiters compare the arrival sequence of lead and lag signals and detect the location where the lag signal catches up with the lead signal. Lap counters are used to monitor the number of laps the signals propagate along the rings. The reuse of Vernier delay stages and arbiters achieves a fine resolution and large detectable range simultaneously while both area and power consumption remain at a reasonable level. With the Vernier ring structure, detectable range can be increased to a very large number, as long as the counter has enough bits to count laps that two signals have propagate along the rings.

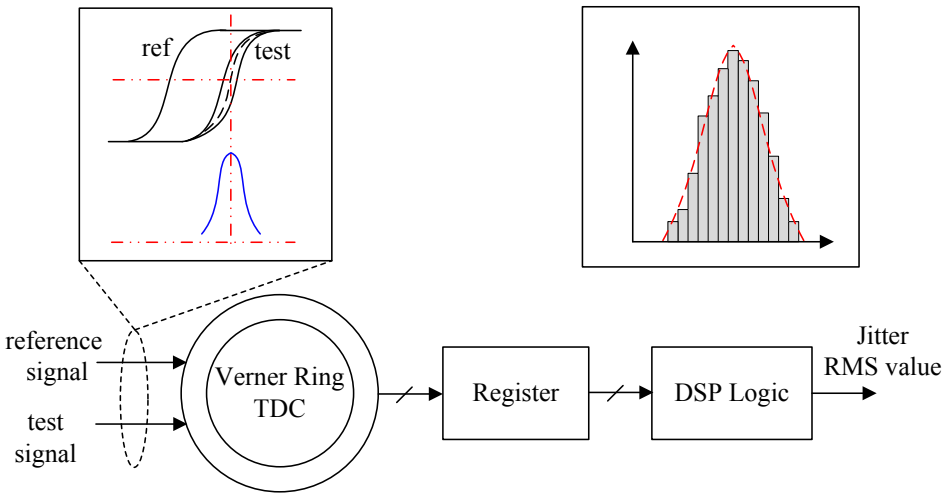


Fig.5.1 Block diagram of jitter measurement using Vernier ring TDC.

Fig.5.1 shows the block diagram of the jitter measurement using Vernier ring TDC. A stable reference signal with much less jitter is required in the jitter measurement using TDC. The test signal is assumed to have a Gaussian distribution with a standard deviation of δt while reference signal's standard deviation is δ_{ref}. Thus δ_{ref} must be much smaller than δt. The jitter measurement circuit consists of Vernier ring TDC, register and DSP logic. The reference signal and test signal are input to the Vernier ring TDC and the time interval between these two signals are quantized with a tiny time resolution. The outputs of Vernier TDC are collected in the register where a certain number of the test results are stored and ready for processing by the followed DSP logic. The DSP logic will output the estimated standard derivation and mean value of the measured jitter distribution by calculating the statistics data of the histogram of the collected TDC outputs.

There are many factors that have effects on the accuracy of the jitter measurement. The on-chip jitter measurement using TDC put a stringent requirement on the reference signal. The frequency variation and fluctuation will cause the error in measured jitter. The fixed frequency error, even very small, between reference signal and test signal will generate a ramp of phase error, namely time interval, which will expand the histogram of the collected TDC outputs. The TDC outputs may spread out over a large range of time interval when the accumulated frequency error is larger than the jitter variation range. Moreover, the jitter of reference signal should be negligible compared to the signal under test. The jitter of reference signal is uncorrelated to the test signal therefore this jitter will be added to the measured RMS value of the jitter. The time resolution of the TDC will determine the accuracy of the jitter measurement. The smaller the time resolution is, the more accurate of the measurement can be achieved. The INL and DNL of TDC also affect the measurement accuracy.

5.3 DPLL with built-in jitter measurement

As mentioned above, Vernier ring TDC has an important application in digital phase-locked loop (DPLL). The VRTDC can be used not only as a phase-frequency comparator, but also as a timing jitter and phase noise detector that can provide tuning controls for a self-healing DPLL.

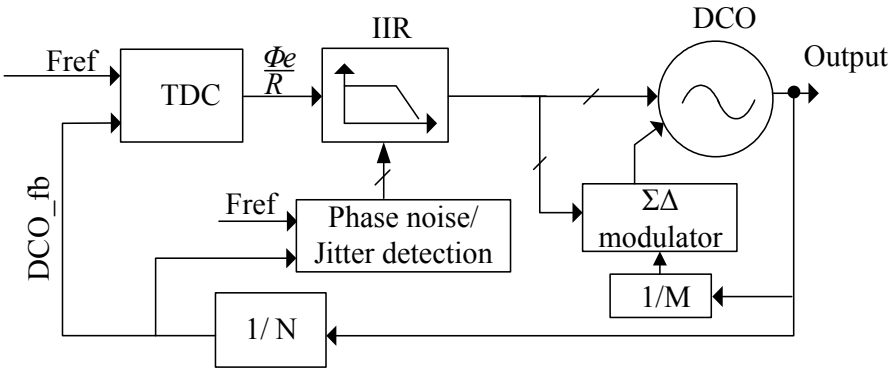


Fig.5.2 Block diagram of the DPLL.

Fig.5.2 shows the block diagram of the DPLL with dynamic loop bandwidth adjustment. This DPLL consists of a Vernier ring TDC, an IIR low pass filter, a phase noise and jitter detector, an integer-N or a fractional-N frequency divider, a sigma-delta modulator and a DCO.

PLL loop bandwidth influences the loop settling time, stability, and loop noise performance. A narrow loop bandwidth benefits the in-band noise filtering while a wide loop bandwidth is helpful to remove out-band noise and reduce the loop settling time. In order to minimize the total PLL phase noise, the optimal loop bandwidth should be chosen around the cross point of the in-band and out-band (VCO) phase noise spectral density curves. It's highly desirable that the loop filter bandwidth can be adaptively adjusted during the PLL operation, namely, a wider bandwidth is programmed at the initial stage to allow fast settling of the loop followed by a

narrower loop bandwidth that can be chosen by detecting the phase noise or timing jitter of the PLL output and programming the loop filter bandwidth for optimal phase noise and spur rejection, as shown in the proposed DPLL architecture (Fig.5.2). Even if a loop filter can be integrated, a problem associated with integrated analog filters is the cutoff frequency variation due to PVT variations. In a conventional analog PLL, the loop filter is normally placed off-chip due to large component values that are not suitable for integration. For the DPLL, the digital loop filter can be integrated and programmed on the fly.

The digitized phase error between reference signal and DCO feedback signal can be utilized to characterize the DPLL output jitter performance when the DPLL is in locked and the reference jitter is negligible. The DPLL output jitter is dependent on the loop bandwidth and thus can be optimized through detecting the minimum jitter value when sweeping the loop bandwidth in a reasonable range. As mentioned above, the output jitter can be measured by comparing the DCO feedback signal with the reference signal and the histogram of the phase error can be converted into the RMS value of the jitter. Sweeping the loop bandwidth will generate a curve of the jitter vs. loop bandwidth. A DSP optimization algorism is employed to find the appropriate loop bandwidth where the minimum of RMS jitter of the DPLL output signal is achieved.

5.4 Jitter test results

In order to verify the proposed jitter measurement scheme using VR-TDC, a jitter testing set up is illustrated in Fig.5.3. Two off-chip signal generators are used to generate reference signal and test signal for the jitter measurement. The phase modulation is achieved by adjusting the delay of the test signal with a modulating signal to introduce the jitter. The modulating signal is a random signal (noise) with the tunable amplitude and DC offset. An exemplary test for the proposed VR-

TDC jitter measurement was configured as depicted in Fig.5.3. A prototype Vernier ring TDC fabricated in 0.13μm CMOS technology was tested using a test signal and reference signal from two channels of the Agilent pulse generator 81134A. A Gaussian noise with the adjustable amplitude and dc offset was generated by an arbitrary waveform generator and then applied to the delay control input of the pulse generator. This voltage input can linearly modulate the delay of the test signal pulses, namely the phase of the pulses. Thus the jitter of the test signal is known since the delay-to-voltage gain is pre-defined in the aforementioned pulse generator.

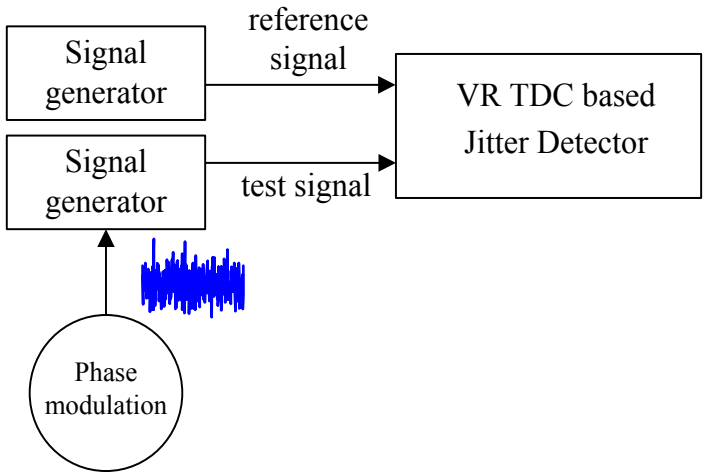


Fig.5.3 Block diagram of jitter testing setup.

In this exemplary test, a peak-to-peak 20ps phase variation was modulated to the test signal and the average time interval between two signals is 2.05ns. Vernier ring TDC measured the time-varying jitter in a successive way and the transient measurement results are shown in Fig.5.4 (a). The TDC output code varies from 199 to 202 when the time resolution is set to 10.2ps. Fig.5.4 (b) displays the histogram of quantized time intervals and a normal distribution curve drawn in red. The estimated standard derivation and mean value of the histogram are 11.2ps and 2.047ns, respectively. The measurement results are consistent with the jitter of the test signal. The linearity of phase modulation, phase noise of reference signal, TDC quantization

noise and noise coupled from PCB and power supply may affect the distribution of TDC output codes.

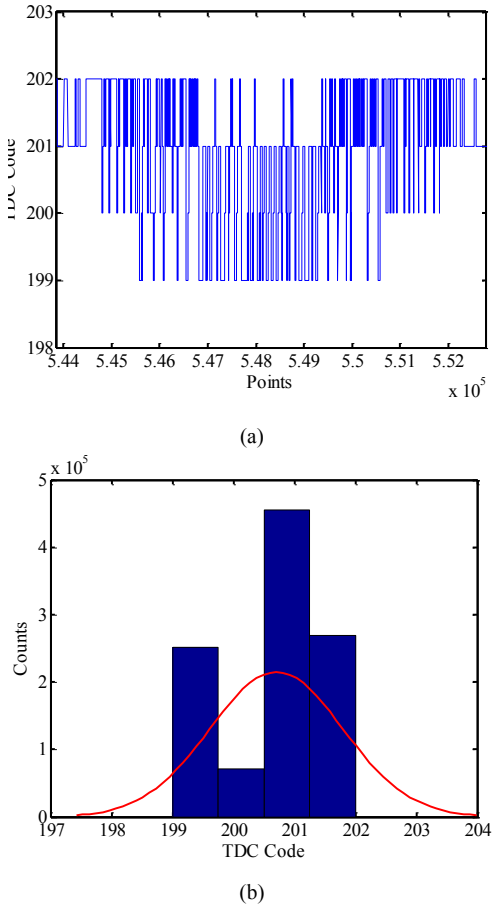


Fig.5.4 (a)Transient waveform and (b) histogram of TDC output when measuring a pre-defined 20ps peak-to-peak jitter with a DC offset phase error of 2.05ns**.**

5.5 Summary

This dissertation presents an on-chip jitter measurement scheme using Vernier ring TDC. The VR-TDC can achieve a fine resolution and large detectable range simultaneously while the power consumption and area cost are kept at a low level. An exemplary test is given to demonstrate the capability of this on-chip jitter measurement scheme. The proposed on-chip

jitter measurement scheme can be used to provide feedback controls for jitter cancellation in RF clock generation circuits with self-healing capability.

Chapter 6 VCO with Digitally Controlled Artificial Dielectric

6.1 Introduction of artificial dielectric

Voltage controlled oscillators (VCOs) suffer from degraded phase noise due to substrate and metal losses. In addition, the quality factor of integrated inductors degrades with increase of operating frequency. In order to reduce the substrate loss thus improving the Q factor, patterned ground shields are widely used underneath the inductors. Unlike the solid ground shield, the patterned ground shield reduces mutual coupling and the impedance to ground, providing a good short for the electric field [22]. Similar to the patterned ground shield, artificial dielectric can not only improve the quality factor, but also add frequency tunability to the VCO with digital control techniques.

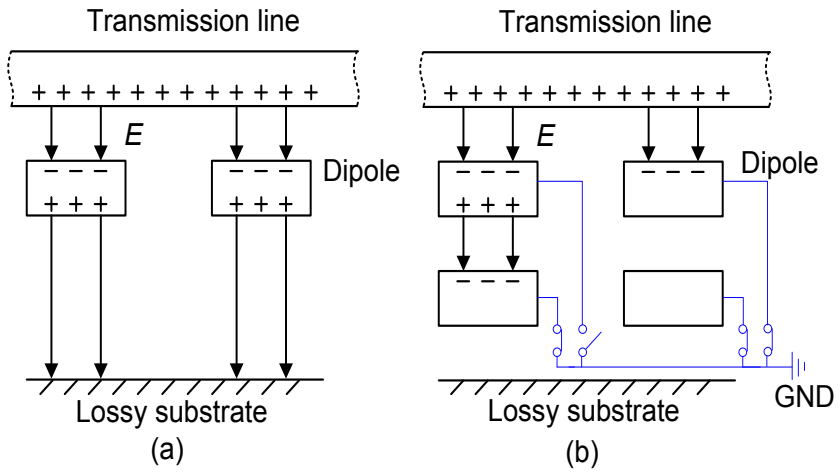


Fig.6.1 (a) Conventional artificial dielectrics, and (b) proposed multi-layer digitally controlled artificial dielectrics.

The artificial dielectric, a technique first used in 1948, was reinvented recently to reduce the substrate loss and increase the effective dielectric constant. The low-layer metal strips are inserted underneath the inductor and connected to a varactor array [23]. 2-D floating metal arrays placed under transmission lines has shown a two- to three-fold loss reduction compared to unshielded lines at frequencies below 30GHz [24].

Fig.6.1(a) shows the conventional dielectric which has been widely used in microwave applications. Small conducting materials, for instance metal strips, are placed under a transmission line. When applied with an external field, the charges on each conducting metal strip are displaced, simulating the behavior of the molecules in an ordinary dielectric. The electrical field starts from bottom plate of the transmission line and ends at the lossy substrate in a implementation using standard CMOS technologies. The induced charge in the metal strips will alter the artificial dielectric constant. The transmission line is loaded with distributed parasitic capacitors. The effective dielectric constant is given by

$$D = \varepsilon_0 E + P = \varepsilon' E \qquad (6.1)$$

where E is the electrical field and P is the polarization [25].

As known, the electrical field would end at the embedded conducting material if it is grounded. With the digital controlled switches, the artificial dielectric becomes reconfigurable by grounding the selected conducting materials as shown in Fig.6.1(b). The multi-layer metal strips are used to make the dielectric configurable. Meanwhile less electrical field would leak to the lossy substrate thus less power would be dissipated. The quality factor of the LC tank could be improved by the placement of multi-layer artificial dielectrics.

This dissertation presents the design of a Colpitts VCO with digitally controlled artificial dielectric. Section II discusses the design dilemma in VCO phase noise optimization and the appealing solution of using artificial dielectric. The detailed design of the VCO core is introduced in section III. The measurement results and chip fabrication are presented in section IV.

6.2 Colpitts VCO with digitally controlled artificial dielectric

In an LC VCO design, there is always a trade-off between the tuning range and the phase noise performance. A wide tuning range usually requires large varactor size that has higher loss than an MIM capacitor with equal capacitance. As a result, the varactor will cause more phase noise than MIM capacitor. In order to solve this dilemma, an alternate scheme to control the oscillating frequency is explored in this design.

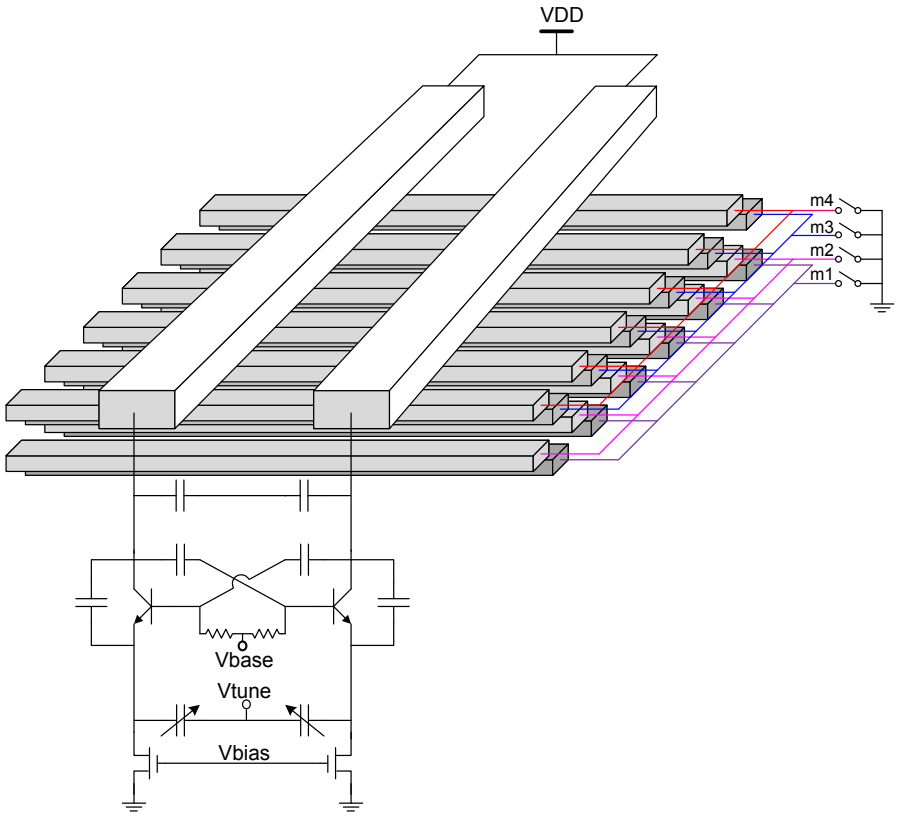


Fig.6.2 Differential Colpitts VCO with digital controlled artificial dielectric

The digitally controlled artificial dielectric is used to expand the tuning range of the proposed VCO. Fig.6.2 depicts the simplified diagram of the proposed differential Colpitts VCO with digitally controlled artificial dielectric. The core of the proposed VCO employs the differential Colpitts topology since it has a better phase noise performance than the conventional cross-coupled LC structure. The transmission line inductor has a higher quality factor in the target frequency range. In addition, the underlying artificial dielectric pattern can be easily implemented symmetrically with the transmission line inductor, compared to the spiral inductors in LC VCOs [26][27][28][29].

The artificial dielectric is composed of 4-layer metal strips underneath the transmission line. The metal strips are connected to an array of MOS switches that controls the metal strips to be either grounded or floating. The two states affect the parasitic capacitance to the resonant tank

differently. In this design, 3-bit control signal selects the number and layer of the metal strips to be grounded in order to alter the parasitic capacitance of resonant tank. As a result, the control signal of the switches can digitally adjust the resonant frequency, expanding the tuning range of the proposed VCO.

6.3 Circuit design of the VCO

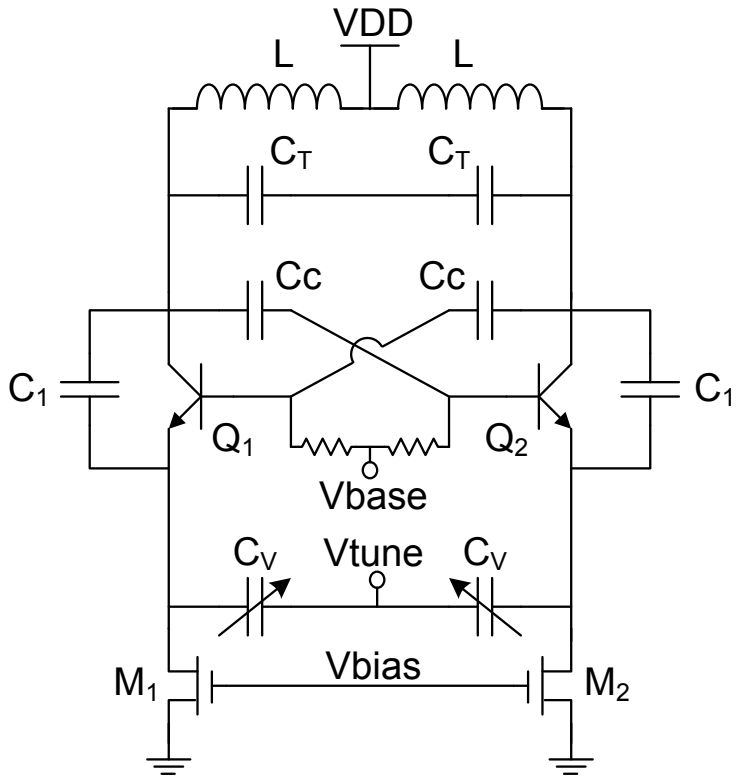


Fig.6.3 Simplified schematics of the proposed Colpitts VCO.

Fig.6.3 shows the schematic diagram of the proposed VCO core. The VCO configuration includes a bipolar cross-coupled pair that provides a negative resistance of -2/gm to overcome the loss due to the parasitic and loaded resistance. C1 and CV constitute a feedback path in the Colpitts VCO. CT accounts for both capacitance of tank MIM capacitor and parasitic capacitance to the underlying metal strips. CV is the MOS varactor which has a much lower quality factor

than MIM capacitor CT. CC is the coupling capacitor. All the above capacitors contribute to the tank capacitance. The noise on the control voltage *Vtune* coupled from environmental noise or power rail will degrade the VCO performance. In order to reduce the noise injected to the LC tank from the *Vtune* line, varactor pair is placed between current tails and the bipolar cross coupled pair. Thus, varactors will load the tank with a capacitance less than its nominal value.

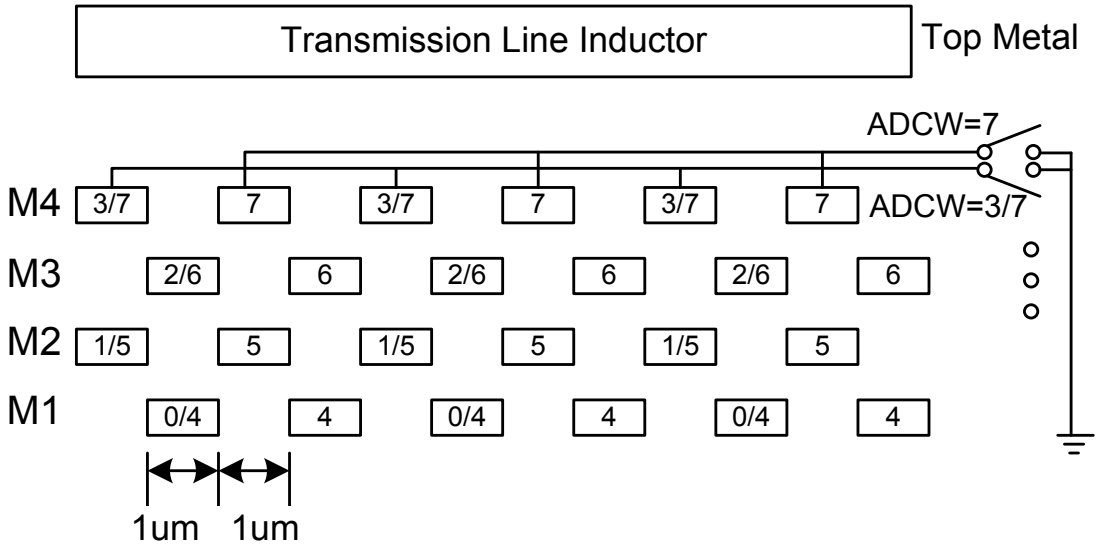


Fig.6.4 Cross-sectional view of the proposed RF transmission line with underlying artificial dielectric.

The artificial dielectric is built with a large number of metal strips using four layers from M1 through M4 in a 1P7M 0.13μm BiCMOS technology. The width and length of each metal strip are 1μm and 320μm, respectively. The spacing between two adjacent metal strips is set as 1μm. In order to reduce the electrical flux which directly goes to the lossy substrate, the metal strips in odd number of layers are shifted horizontally by 1um. In each layer there are 100 metal strips which are equally divided into two groups forming an inter-digitized layout as shown in Fig.6.4. Each of the total 8 strip groups is connected to a MOS switch and 3-bit artificial dielectric control word (ADCW) applied to these MOS switches configures the connectivity of the metal

strips, either grounded or floating. The least 2 bits of the ADCW select which layer of the strips is connected to the ground. The MSB of the 3-bit ADCW determines that either the half or entire of the strips in the selected layer are grounded. For instance, in metal 4 layer, one group of metal strips are connected to a MOS switch that is closed only when ADCW=7. The other group is grounded when ADCW is set to either 3 or 7. Therefore, the parasitic capacitance of the resonant tank to the metal strips is digitally tuned by the control signal.

6.4 Chip fabrication and measured results

The proposed differential Colpitts VCO chip was fabricated in a 0.13um BiMOS technology.

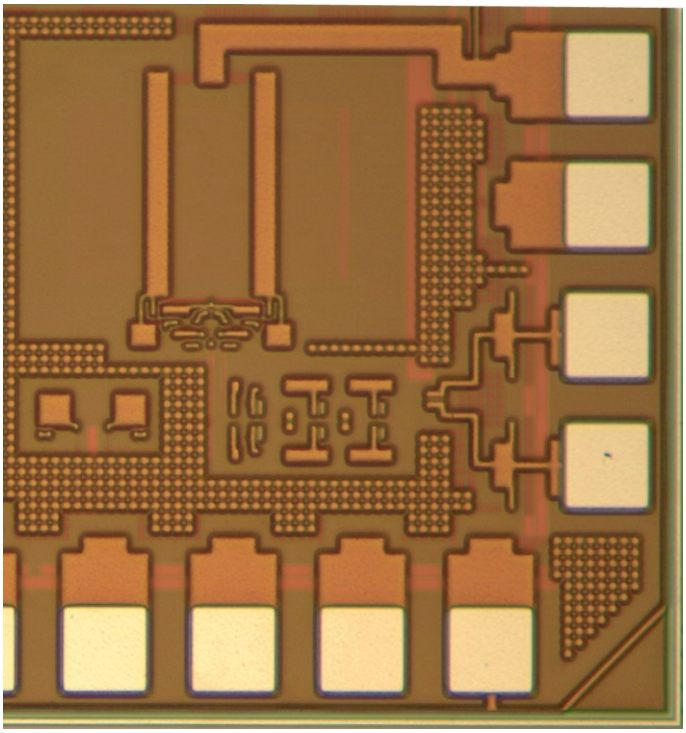


Fig.6.5 Die photo of the Colpitts VCO MMIC.

Fig.6.5 shows the die photo of the VCO with digitally controlled artificial dielectric. The chip occupies an active area of 0.32 mm2, while the VCO core takes an area of 0.1 mm2. The output buffers were designed to boost output power for testing purpose. The VCO core consumes only

6.8mW power from a 1.8V voltage supply. The entire VCO chip consumes a current of 18mA and most of the power is dissipated in the output buffer stages. The VCO chip was packaged using 28pin QFN packages and a test board was developed using Rogers 4003 laminate material.

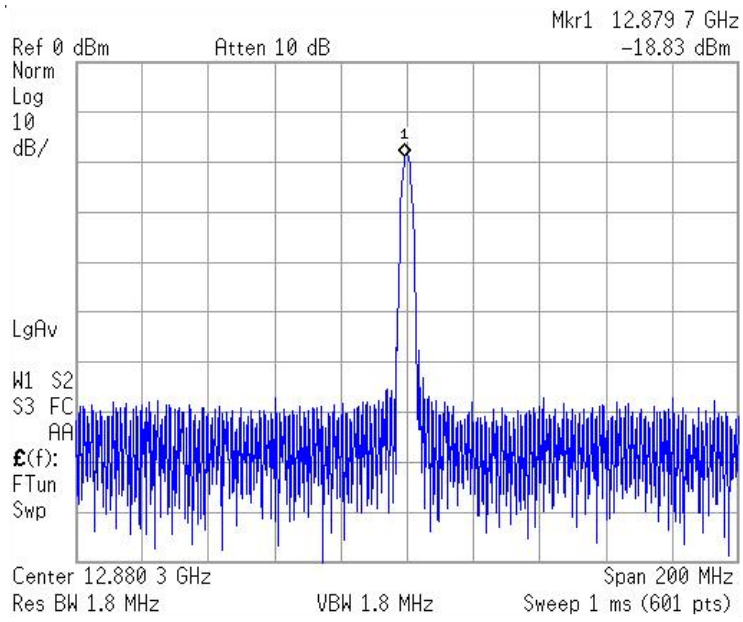


Fig.6.6 The measured power spectrum of the proposed VCO.

Fig.6.6 depicts the measured output power spectrum of the proposed VCO with reconfigurable artificial dielectric. The output power is about -18.83 dBm at the output frequency of 12.88 GHz. This reading includes all the losses through cable, connectors and the PCB. Fig.6.7 shows the measured phase noise curve of the VCO. This VCO achieves a phase noise of -106.7dBc/Hz at 1MHz offset frequency and -123.6dBc/Hz at 10MHz offset.

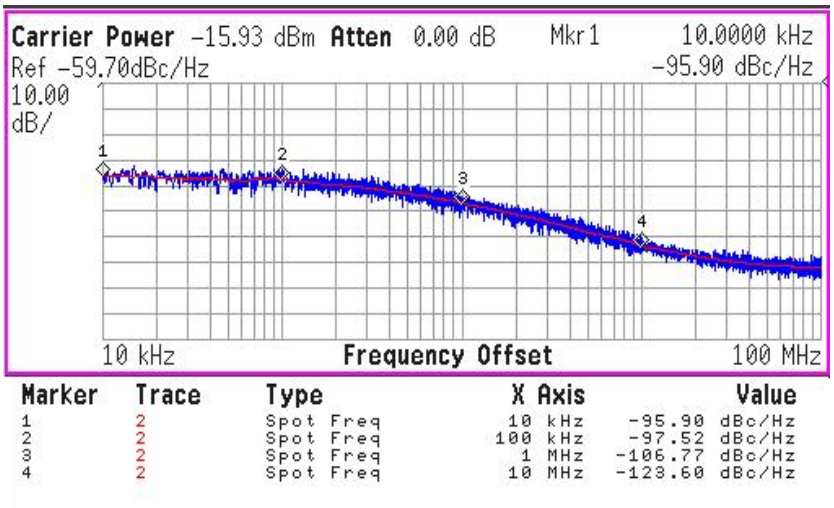


Fig.6.7 The measured phase noise of the proposed VCO.

The proposed VCO oscillates at the central frequency of 12.9GHz. Fig.6.8 shows the measured curve of VCO resonant frequency versus tuning voltage. The limited tuning range was due to the small varactors used in this design to trade for a better phase noise performance. Also the underlying artificial dielectric contributes a large amount of parasitic capacitance to the LC tank. The tuning curve in Fig.6.8 can be shifted up and down by setting different artificial dielectric control word (ADCW). The larger ADCW denotes that the higher layer of metal strips is grounded and consequently more capacitance is introduced to the LC tank. These turning curves are almost evenly distributed over the control word range.

The dependence of the phase noise on the artificial dielectric has been investigated. As shown in Fig.6.9, phase noise @ 1MHz offset were measured versus the combination of 3-bit artificial dielectric control word (ADCW) under 5 different settings of the tuning voltages. Each mark in the curve represents the phase noise averaged from 10 measurement results. The phase noise @ 1MHz offset varies in a range from -103.4 dBc/Hz to -106.7 dBc/Hz with different settings of ADCW and Vtune. The best phase noise of -106.7dBc/Hz was obtained when the tuning voltage was set to 0.5 volt. According to Fig.6.9, no significant relationship has been found between the

ADCW and the phase noise. However, the phase noise performance has dependence on the tuning voltage as indicated by the curves in Fig.6.9. This dependence is due to the noise coupled from tuning voltage line and the amount of noise introduced to the tank varies with the voltage drop on the varactor, namely the instantaneous capacitance of the varactor.

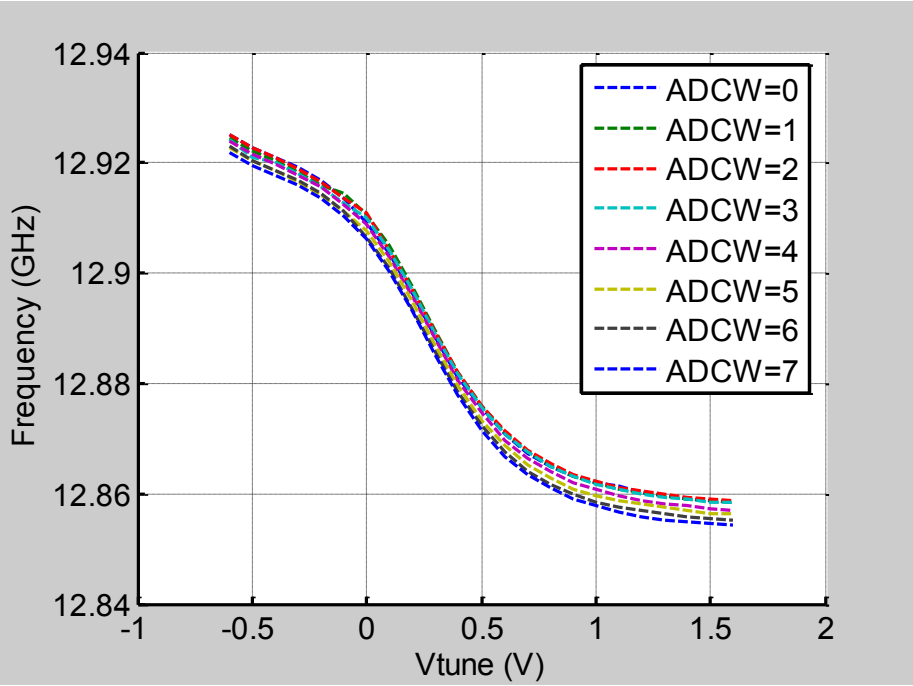


Fig.6.8 The measured VCO output frequency vs. tuning voltage with digital controlled artificial dielectric.

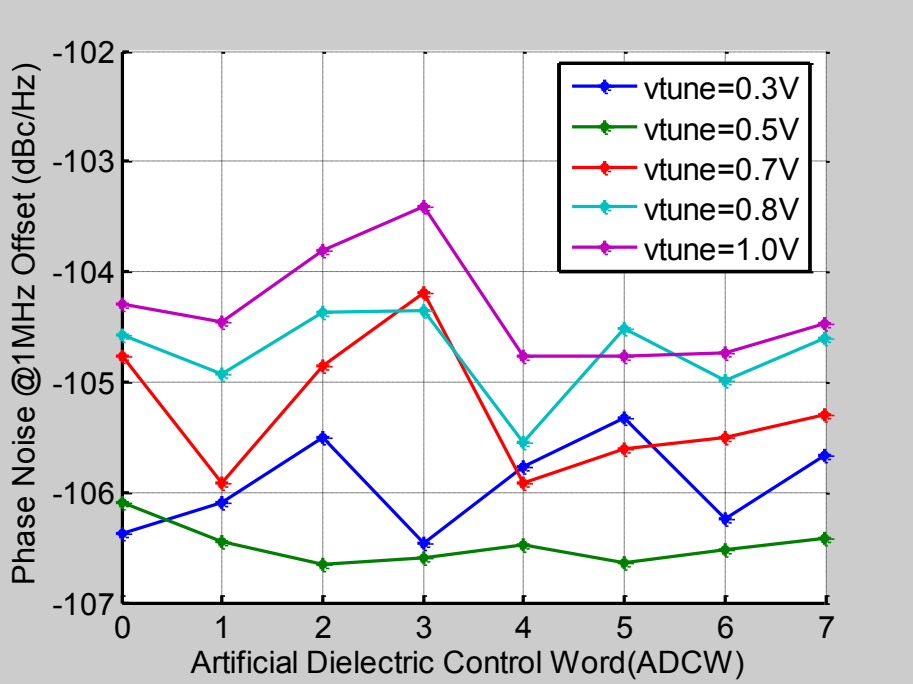


Fig.6.9 The measured phase noise @ 1MHz offset vs. artificial dielectric control word under various tuning voltages of varactor

6.5 Summary

We have presented a 12.9 GHz differential Colpitts VCO with digitally controlled artificial dielectric fabricated in a 0.13um BiCMOS technology. The oscillation frequency can be adjusted by either tuning voltage applied to the varactor or by grounding the selected layer of the artificial dielectric. The artificial dielectric can also reduce the substrate losses thus improving the Q factor of the VCO. The proposed VCO exhibits a phase noise Table I summaries the comparison between the features of the proposed VCO and previously published VCOs. This design achieves a figure of merit (FOM) of -180.7dBc/Hz, which is calculated based on the following expression:

$$FOM = L(f_{offset}) - 20\log(\frac{f_o}{f_{offset}}) + 10\log(\frac{P}{1mW}) \qquad (6.2)$$

Table 2 Performance Comparison of VCOs

Ref	Tech. (um)	Frequency (GHz)	VDD (V)	Power (mW)	Phase noise @1MHz	FOM (dBc/Hz)
[26]	0.18	11.22	1.8	6.84	-109.4	-181.8
[27]	0.09	11.75	1.2	7.67	-106	178.5
[28]	0.18	11.55	1.8	8.1	-110.8	-183
[29]	0.13	12.4	3.3	69	-103.9	-
this work	0.13	12.9	1.8	6.8	-106.7	-180.7

Chapter 7 Vernier Ring TDC and Other Building Blocks for Digital Phase Locked Loop

7.1 Overview of digital phase locked loop

Digital phase-locked loops (DPLLs) recently are widely explored for wireless communication applications. Time-to-digital converter replaces the phase frequency detector and charge pump in conventional analog PLL to measure the phase/frequency error between reference clock and feedback clock from digital controlled oscillator (DCO). The TDC digitizes this error with a finite time resolution which introduces the quantization noise to the DPLL, similar to the in-band phase noise generated by PFD in an analog PLL. The first TDC-based all-digital PLL was designed with a classical divider-less structure as shown in Fig.7.1(a), which relaxes the number of bits required in the TDC design with assistance of a counter[1]. The time resolution interpolated by counter is the period of the DCO output signal, which is time varying and dependent on the frequency control word (FCW). Additional logic is required to synchronize and combine fractional and integer parts of the measurement results. Fig.7.1(b) depicts another divider-assisted structure using a divider in the feedback path, which was proposed in a gated ring oscillator TDC based DPLL[2]. In that design, an absolute phase error was digitized by a fine resolution less than gate delay. The divider-assisted structure is simple and easy for implementation, but requires a state-of-art TDC with both small resolution and large detectable range.

This chapter is organized as follow: the DPL system is discussed in Section 7.2. The

modification of Vernier ring TDC for DPLL use is presented in Section 7.2. Digital filter and digitally controlled oscillator are introduced in section IV.

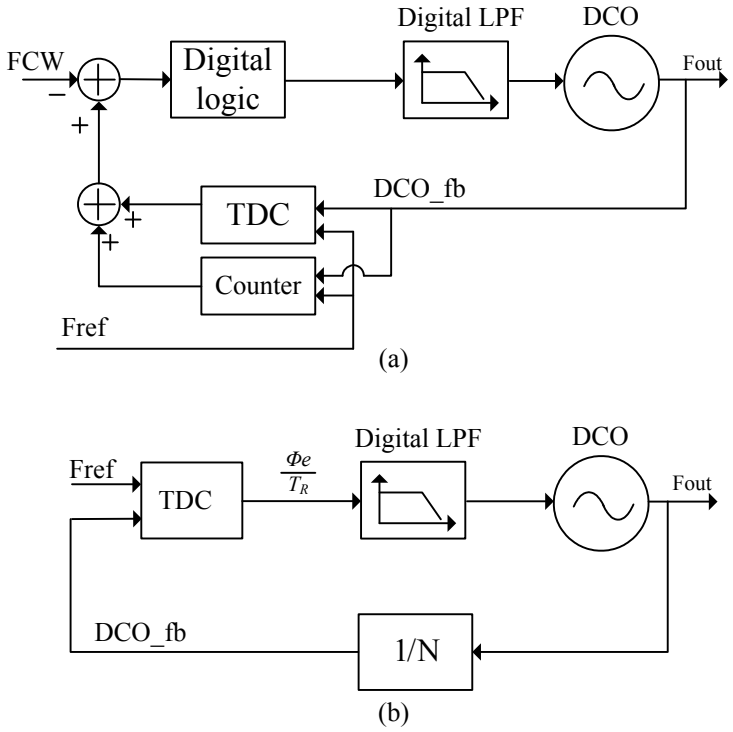


Fig.7.1 Simplified block diagram of (a) divider-less DPLL and (b) divider-assisted DPLL

7.2 System analysis of the digital phase locked loop

The proposed DPLL is the 3rd 0rder Type II DPLL consisting of Vernier TDC, IIR, integer divider and DCO. As we know the major phase noise sources of DPLL are the TDC quantization noise and DCO phase noise. The in-band phase noise is mainly determined by TDC time resolution. The in-band phase noise level is estimated with the following equation [4],

$$L = 10\log\left[\frac{(2\pi)^2}{12}\left(\frac{R}{T_{DCO}}\right)^2\frac{1}{f_R}\right] \qquad (7.1)$$

where R is the time resolution of TDC, f_R is the reference frequency and T_{DCO} is the period of DCO output signal. Fig.7.2 shows this estimation in which the time resolution is swept from 2ps to 20ps with a parametric reference frequency set from 10MHz to 25MHz. According to the plot,

the smaller time resolution, the lower estimated in-band noise due to TDC quantization noise. But the too small time resolution will bring challenge to TDC design. Given the above equation, the time resolution has to be less than 10ps to achieve <-95dBc/Hz in-band noise if the reference frequency is equal to 15MHz.

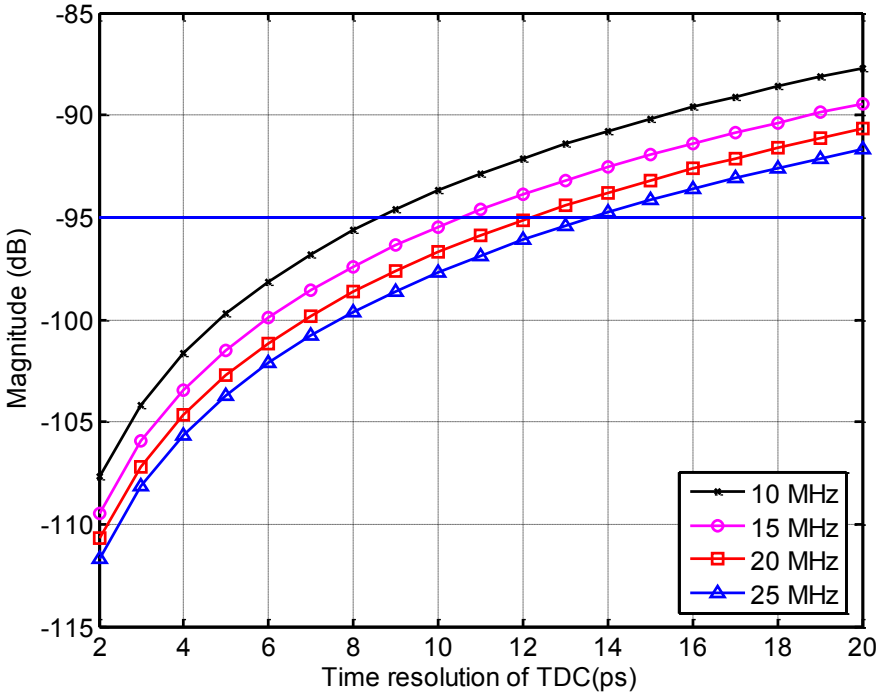


Fig.7.2 Estimated in-band PN due to TDC quantization vs. time resolution

The bandwidth of DPLL is tentatively set to be 400 kHz when the phase noise due to TDC quantization is set to -95dBc/Hz and DCO phase noise is -120dBc/Hz at an offset frequency of 1MHz. The output phase noise of synthesizer is plotted in Fig.7.3 using cppsim.exe [37].

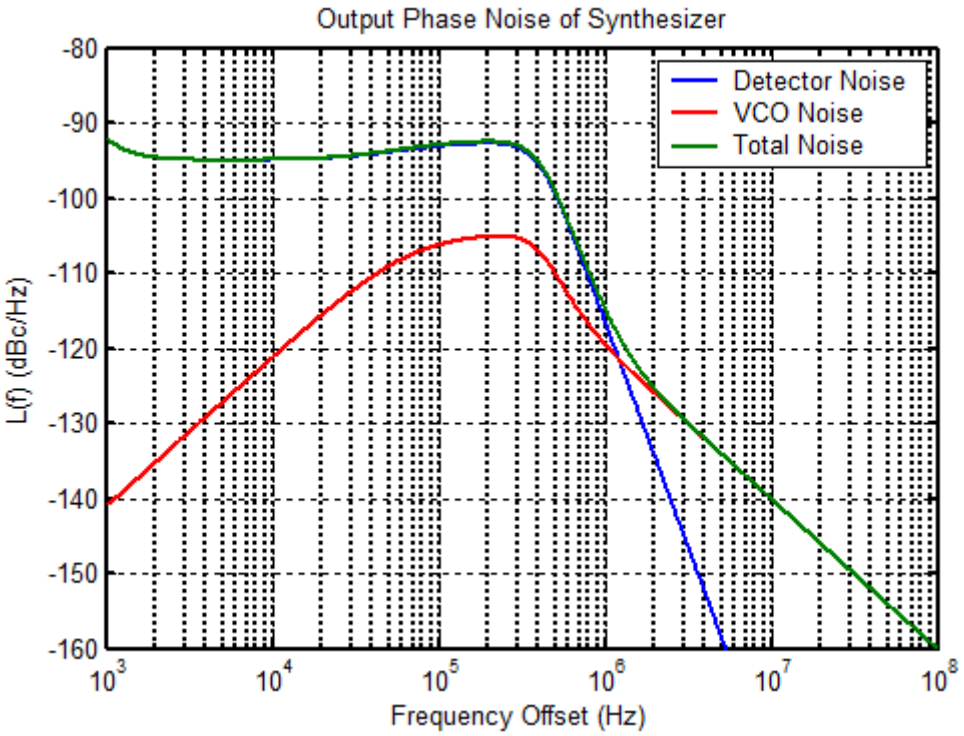


Fig.7.3 Simulated phase noise spectrum of DPLL

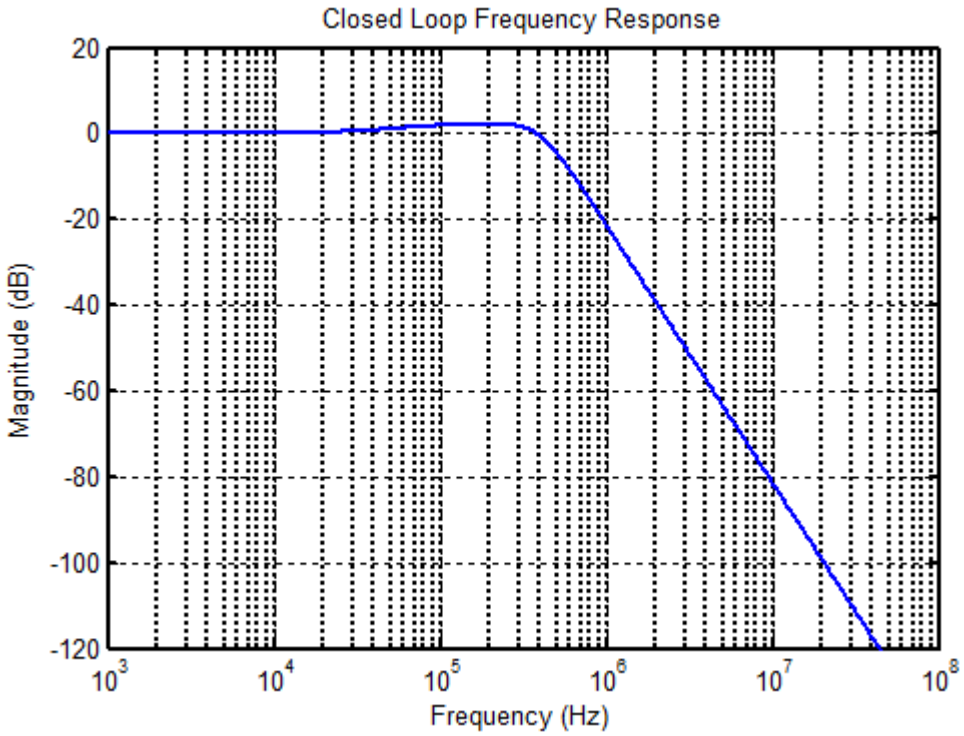


Fig.7.4 Simulated transfer curve of DPLL

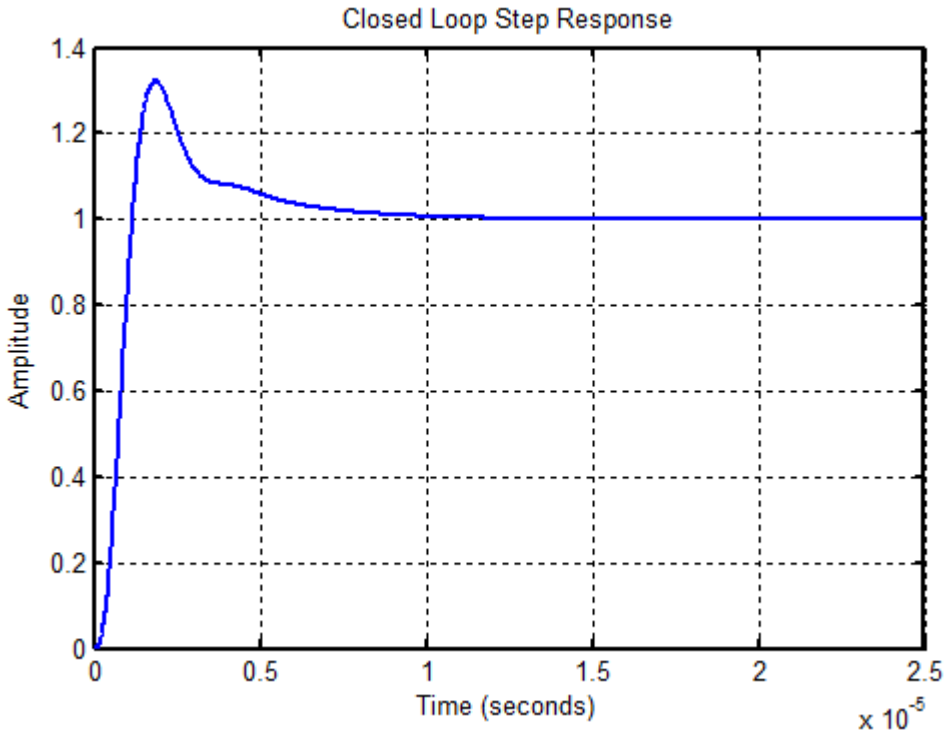


Fig.7.5 Simulated step response of DPLL

Fig.7.4 shows the transfer curve of the proposed DPLL. The step response is also simulated showing a stable settling process in Fig.7.5.

7.3 TDC for digital phase locked loop

The TDC is the key building block of the DPLL since its time resolution, detectable range and linearity are critical to the overall performance of DPLL.

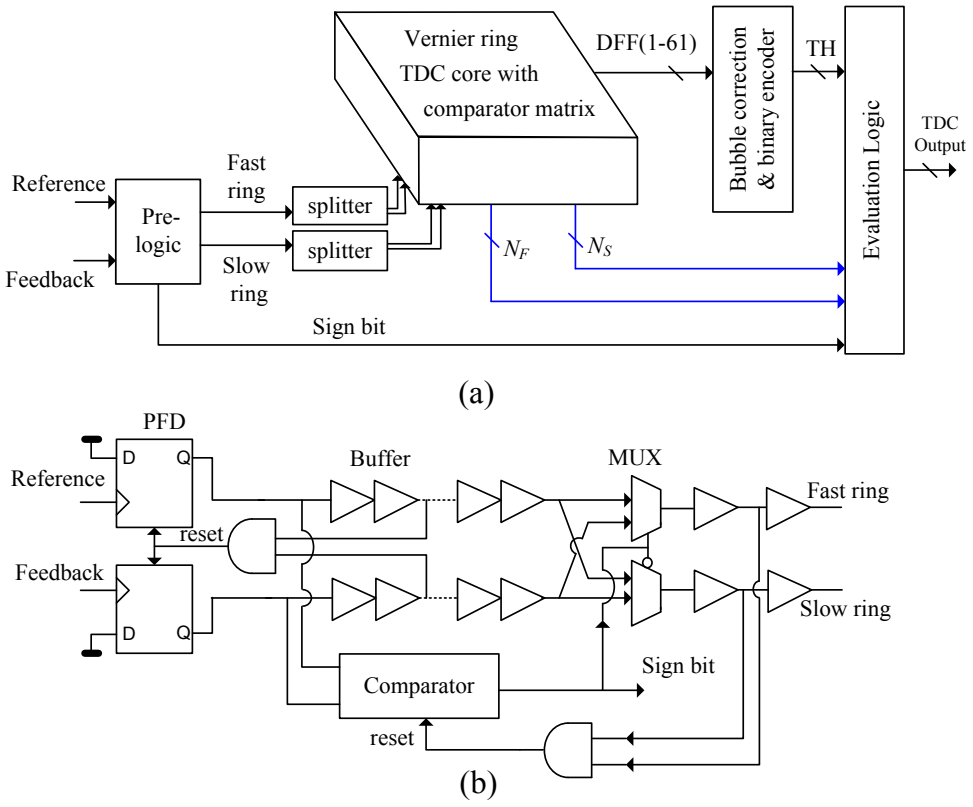


Fig.7.6 (a) Block diagram of the Vernier ring TDC and (b) schematic of the PFD embedded pre-log unit for DPLL applications

The 3-D Vernier ring TDC can not be used in DPLL directly. The instantaneous frequency of reference signal may be much larger or smaller than that of the feedback signal during the frequency acquisition. In that scenario, more than one pulse of reference signal or feedback signal will be input to the TDC at a single measurement. The erroneous data will occur inevitably. To prevent such a scenario from happening, a phase frequency detector (PFD) is embedded in the pre-logic unit which can filter out the possible multiple pulses at either reference input or feedback input during phase comparison. Fig.7.6(b) depicts the schematic of pre-logic unit which compares the arriving sequence of the input reference signal and feedback signal. Consequently, pre-logic unit determines the lead and lag signals and feeds the first-arriving lead signal to the slow ring and the second-arriving lag signal to the fast ring.. Splitter

converts a single-ended signal to the pseudo-differential signals and feed them to the TDC core. Bubble correction circuitry removes the bubble pattern in the thermometer code caused by the metastability of DFFs in TDC core.

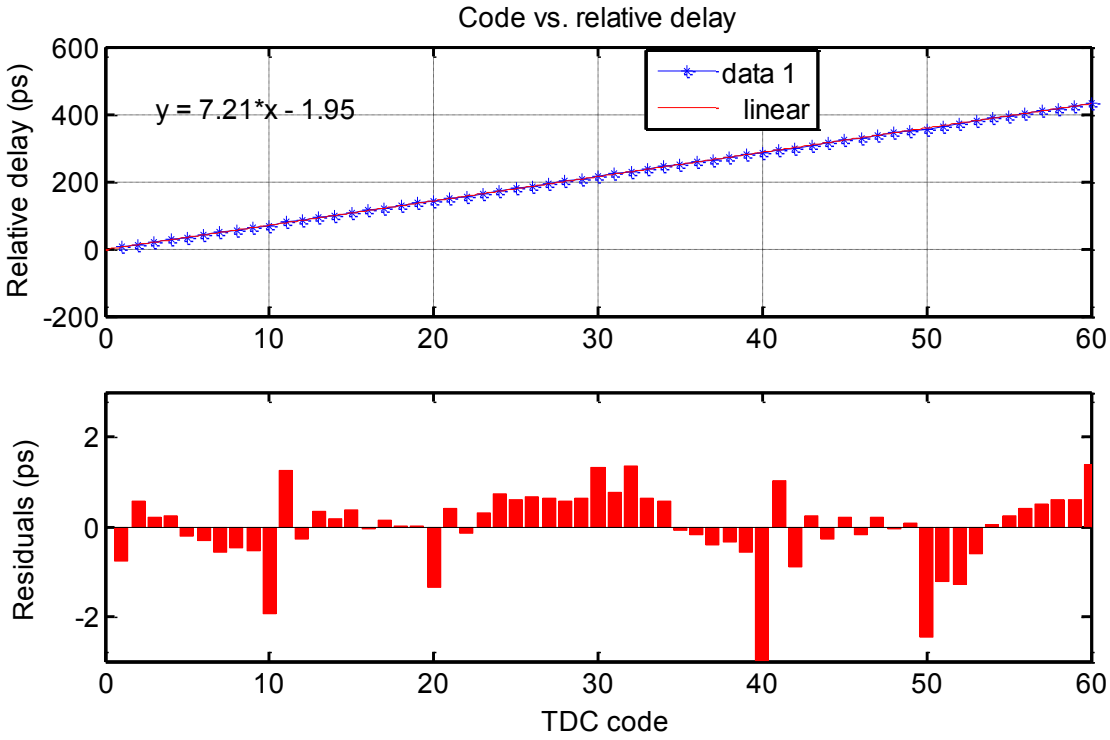


Fig.7.7 Simulated quantization code vs. relative delay of the Vernier ring TDC with comparator matrix

The TDC quantization noise dominates the in-band noise while its linearity affects the power of fractional spur [1]. According to the analysis in previous section, the TDC resolution should be less than 8 ps to keep the DPLL in-band phase noise less than -90dBc/Hz.

Fig.7.7 shows the simulated transfer curve and interpolation residue (aka. error) of the Vernier ring TDC with comparator matrix. The slope of the curve indicates the average resolution of the TDC, which is 7.21ps. A good linearity of the TDC characteristics has been achieved. The maximum error between the ideal fitting line and real delay data is 3ps which is around 0.42 LSB. The large errors occurred at the end of diagonals (Fig.4,5) of the comparator matrix where the integral non-linearity has the peak value.

The detectable range should be large enough to measure the maximum phase error which usually equals to the reference period if there is no reference divider in divider-assisted DPLL. Otherwise, additional circuitry is necessary to extend the operation range of TDC[2]. The TDC has a 14-bit detectable range which is capable of measuring an input time interval as large as 67ns.

7.4 Other building blocks design

In this section, the programmable digital IIR filter and digitally controlled oscillator (DCO) will be discussed. The design consideration and simulation results will be presented also.

7.4.1 Digital IIR filter

Similar to the low pass filter in the analog PLL, the digital filter in DPLL will act as a high pass filter for the DCO and a low-pass filter for the TDC. The bandwidth of the filter should be programmable so that the loop bandwidth can be adjusted during the frequency acquisition for both fast locking and better phase noise performance. The 2nd-order infinite impulse response (IIR) filter is employed in this design since IIR filter is easy to implement in the low order filter design and the phase linearity is not a concern. The 2^{nd}-ordr IIR filter can be converted from the 2^{nd}-order analog filter. The transfer function is shown in the following equation:

$$H(z) = g \bullet \frac{1 + 2Z^{-1} + Z^{-2}}{1 - a_1 Z^{-1} - a_2 Z^{-2}} \quad \text{.....(7.2)}$$

where the g, a_1 and a_2 are three variables used to get the tunable gain and bandwidth.

Fig.7.8 shows the simplified diagram of the IIR filter structure. It will operate at the reference frequency of 15 MHz. The bandwidth can be tuned from 50 kHz to 1 MHz.

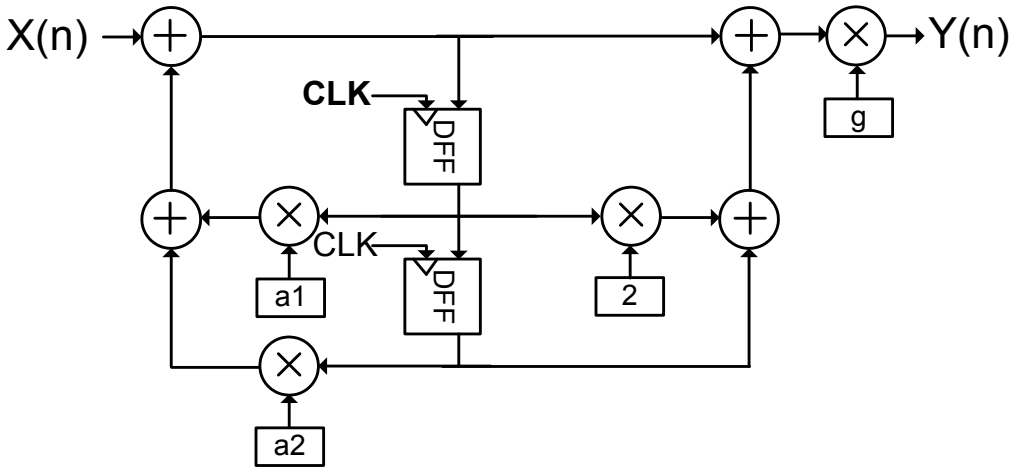


Fig.7.8 Simplified diagram of the 2nd-order IIR filter

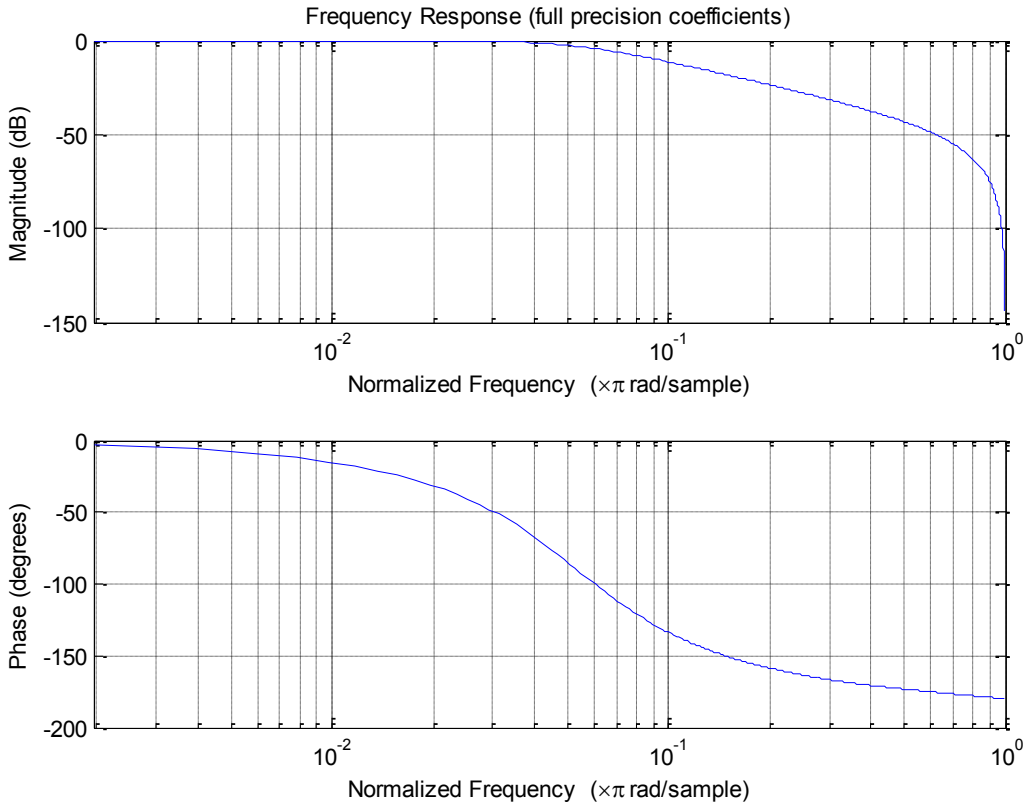


Fig.7.9 Frequency response of IIR with 400 kHz cutoff frequency

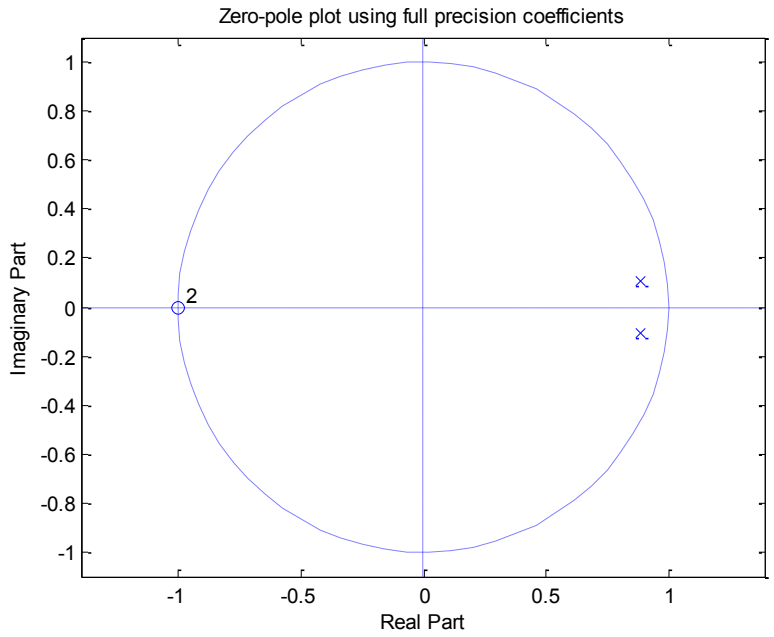


Fig.7.10 Zeros and poles of IIR with 400 kHz cutoff frequency

Fig.7.9 illustrates the frequency response of the IIR with 400 kHz cutoff frequency. The location of poles and zero are shown in Fig.7.10.

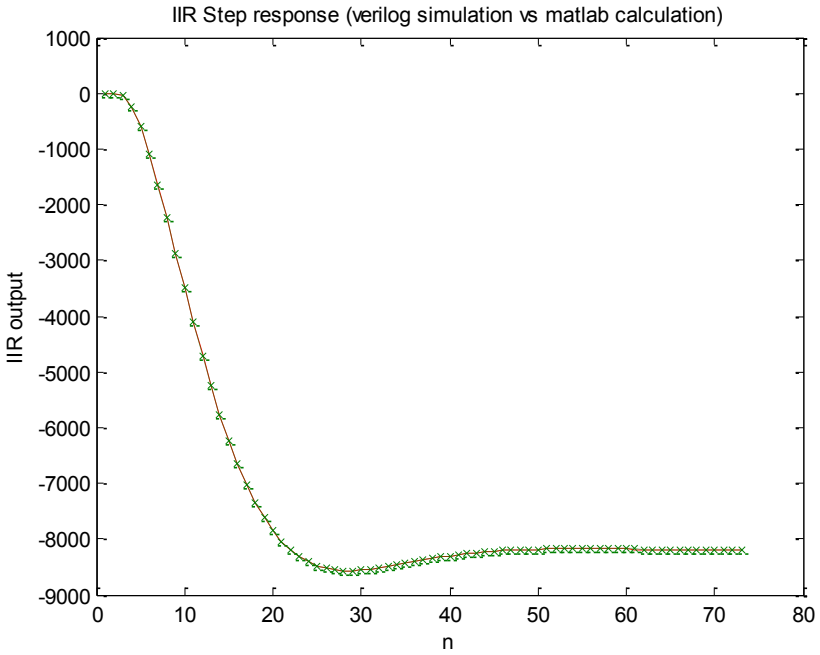


Fig.7.11 Step response of the 2nd-order IIR filter and its mathematic model

For the fixed-point digital filter, the quantization error should be checked in the design. Fig.7.11 shows the step response of the IIR filter (green dots) and the ideal transfer function Eq.7.2 (red line). IIR filter demonstrates a great consistence with its ideal mathematical model, only with a small quantization error.

7.4.2 Digitally controlled oscillator

Digitally controlled oscillator (DCO) is a key component in a DPLL replacing its counterpart, the VCO, in an analog PLL [30]. Finite frequency step site will add quantization noise to PLL output. Therefore fine frequency step is another important concern in DCO design apart from phase noise, power and area. Binary weighted varactors are popular in many recently published DCOs due to easy implementation [38-40]. However, MOS varactor has the capacitance sensitive to the PVT variation, and a quality factor lower than MIM capacitor. It's very difficult to get an accurate fine capacitance with a small-size varactor in the presence of parasitic capacitance which is comparable to the varactor value. In this DCO, MIM capacitor banks in series with several small constant MIM capacitors were used to achieve a fine capacitance step.

Fig.17.2 shows a simplified diagram of the capacitor array, which consists of three 4-bit capacitor banks: coarse-step-size capacitor bank A, medium-step-size capacitor bank B and fine-step-size capacitor bank C. Bank A is in series with a constant cap C_A, while bank B is connected to bank C with a constant capacitor C_B. The whole capacitor array is connected to VCO via terminal Vop and Von. The fine capacitance step in bank A has been achieved by these small constant capacitors between 2 banks. With properly selected capacitance value of capacitor C_A and C_B and three banks, a small variation of frequency step can be obtained also. Fig.7.13 shows the simplified schematic of the DCO circuit. The DCO consists of switched capacitor banks, inductor, NMOS and PMOS cross-coupled pairs. The combination of NMOS and PMOS cross-

coupled pairs will increase the signal swing with same amount of current as in NMOS or PMOS only topologies.

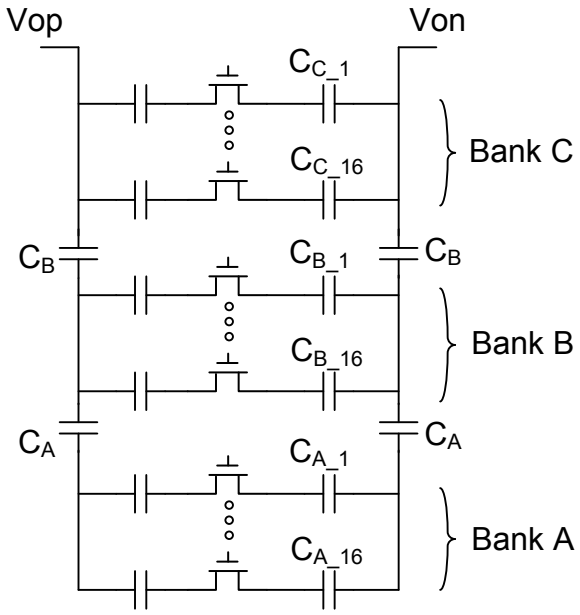


Fig.7.12 Simplified diagram of the capacitor array

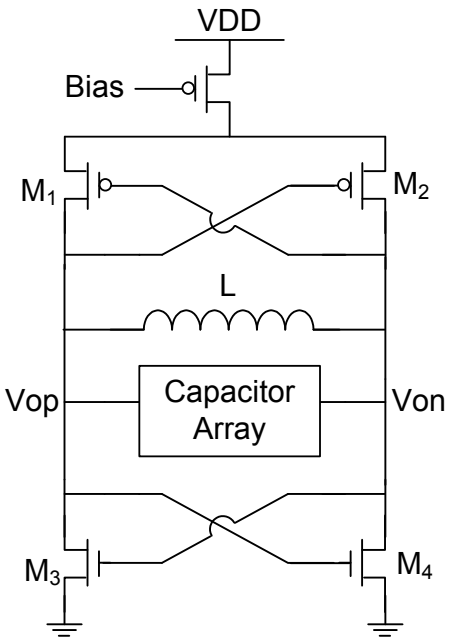


Fig.7.13 Simplified schematic of the DCO.

Chapter 8 Conclusion

8.1 Summary of dissertation

Time-to-digital converters (TDCs) are used to measure the time interval between two events by a small quantization step that creates a time resolution. High resolution TDCs have become increasingly popular for time-of-flight measurement, jitter measurement, process control, LIDAR applications, measurement and instrumentation, and digital phase-locked loops. The standard digital inverter is often employed as the delay element in the TDC design due to its compatibility to the digitally intensive design approach and easy transfer to other CMOS technologies. Thus the inverter propagation delay becomes the bottle neck for the improvement of the TDC time resolution. Although there are various methods to reduce the time solution, the Vernier ring TDC structure is an attractive way to obtain the sub-gate-delay resolution and large detectable range simultaneously.

Vernier ring TDC structure is also featured with the reduction in power consumption and die area. It has naturally incorporated two-step interpolation, coarse interpolation and fine interpolation, in time interval measurement due to two-delay-ring structure. When the input time interval smaller than the period of slow ring, it will be interpolated directly with a fine resolution which is the difference between fast inverter delay and slow inverter delay. When the input time interval is large, Vernier ring TDC will work at the coarse interpolation step first. At the beginning of measurement, only lead signal propagates along the slow ring lap by lap and the lap number is monitored by a coarse lap counter. Vernier ring TDC interpolates the input interval

with the coarse resolution which is the slow inverter delay in slow ring. After the lag signal comes to the TDC, and starts to propagate along the fast ring chasing the lead signal in the slow ring, The TDC automatically works at the fine interpolation step using fine resolution. The residue of the coarse interpolation step will be input to the fine interpolation without any extra hardware cost. The coarse interpolation step has the higher power efficiency than the fine interpolation step in the measurement. Therefore Vernier ring TDC structure saves power when measuring large time interval. In addition, the reuse of the delay cells and comparators in Vernier ring TDC structure leads to the reduction in the die area. The measured results of the prototype chips has proved that the power consumption and die area cost of the Vernier ring TDC can stay at a low level due to the reuse of the delay elements. 3-dimensional Vernier ring TDC further reduces both the power and die area by constructing 2-dimentional delay plane with the comparator matrix. Multiple comparisons are carried out at a single stage of delay rings. To sum up the discussion above, Vernier ring TDC and 3-dimensional Vernier ring TDC are much more competitive in the time interval measurement that demands the high resolution and vary large detectable range than other existing TDCs.

Vernier ring TDC can offer an easy and inexpensive BIST solution to the jitter measurement. The jitter measurement using external automatic test equipments and on-chip driver can hardly achieve the results as accurate and efficient as the on-chip jitter measurement provides. High performance TDC quantizes the time interval between the reference signal and signal under test with a time resolution as tiny as several pico-seconds. The histogram of the digitized time intervals obtained in the successive measurements reflects the distribution of the clock jitter assuming the reference signal is jitter free. It is easy to characterize the peak-to-peak jitter value and rms value from the measured time interval distribution using digital signal processing

algorism. Vernier ring TDC is a good candidate for the on-chip jitter measurement, which has been proved by the its measurement results.

Both voltage controlled oscillators (VCOs) and digitally controlled oscillators (DCOs) suffer from degraded phase noise due to substrate and metal losses. The artificial dielectric technique was reinvented recently in many microwave designs to reduce the substrate loss and increase the effective dielectric constant. In this dissertation, the digitally controlled artificial dielectric was used in the 12GHz VCO circuit, and the affect of artificial dielectric on the VCO phase noise has been tested and shown in chapter 6. The comparison of measured data with the referred VCOs shows that a good overall performance was achieved in this design.

TDC based digital PLL is a hot topic both in academic research and industry design. Since TDC quantization noise dominates the TDC-based DPLL in-band phase noise, low in-band phase noise can be achieved with a well-designed high resolution TDC. 3-dimensional Vernier ring TDC with small modification is quite a fit for the proposed DPLL design. Digital controlled oscillator is another critical building block in DPLL. The finite frequency step will add the quantization noise to the DPLL output. Thus fine frequency step is desired in the DCO design. It is very difficult to achieve an accurate capacitance step at the order of several femto-farads using the conventional MOS varactor since the parasitic capacitance is comparable to the varactor capacitance value. The MIM capacitor banks in series with several small constant capacitors were used in this DCO to achieve a fine capacitance step.

8.2 Conclusion and future work

The conventional delay line TDC, Vernier delay line TDC and any other existing Vernier TDCs all struggled with the limited detectable range when pursuing the fine resolution. The proposed Vernier ring structure provides a smart solution to this dilemma with other valuable

features. Both Verneir ring TDC and 3-dimentional Vernier ring TDC can achieve fine resolution and large detectable range simultaneously. The die area and power consumption are both saved due to the two-delay-ring structure and naturally incorporated two-step interpolation mechanism.

Although the proposed Vernier ring TDC and 3-dimentional Vernier ring TDC have demonstrated the capability of achieving the good performance in time resolution, detectable range, die area and power consumption. There are still a few things that can be improved in the future.

As discussed before, Vernier structure can cancel out the first order variation in inverter delay. Nevertheless the time resolution still changes with the process, voltage and temperature (PVT) variations. The automatic PVT compensation and digital calibration of the TDC resolution will be the topic of the future TDC design. The noise shaping feature can further improve the TDC time resolution and is also a great technique for the reduction of in-band noise in TDC-based DPLL. The Vernier TDC added with noise shaping feature will make it more appealing to both time interval measurement and DPLL design.

Many TDC based digital PLLs have been reported recently. The overall performance of digital PLL is getting to close to its counterpart analog PLL. However there are still many challenges in dealing with the fractional spur and reliability issues when the DPLL is exposed to the PVT variations. Thus the digital calibration is necessary to compensate these variations. The DSP techniques will get more involved in the digital PLL design to further improve the performance.

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