Enhanced Polymer Passivation Layer for Wafer Level Chip Scale Package

by

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Abstract

Wafer level chip scale package (WLCSP) have been used in many consumer products, and thus they are competitive in cost, size, yield, and technology. For advanced WLCSP, solder joint reliability is a major concern. Underfilling is a common solution to addressing WLCSP reliability concerns. Typical stress-relieving methods such as molding compounds and capillary underfills have proven successful in CSP protection, but their added cost to the assembly process is generally prohibited. Instead, successful low cost reliability solutions have generally been the adaptation of wafer level backend packaging processes such as modification of the redistribution layer materials, solder selection, or metal pad thickness. However, the increased performance is limited.

In this research, a new approach is presented to reexamine the final passivation layer as more than a dielectric, but also a partial underfill. The new material, branded as "SolderBrace" as an alternative to underfill, is a photo-imageable molding compound with a low CTE. This layer of SolderBrace coating adds a mechanical buffer to the front side of the WLCSP and delivers improved reliability with conventional tools, short process times and lower costs. SolderBrace coated WLCSPs and standard non-coated WLCSPs, were designed and fabricated with known standard fabrication procedures. The processing of the SolderBrace coatings was achieved by two methods. The first is similar to that of standard polyimide processing: spin coat, bake, photo-image, solvent develop, and ball drop. The second application process involves printing the material on the already-balled wafers followed by solder cleaning and cure. These

SolderBrace coatings were low temperature cured and generated minimal wafer bow. The test WLCSPs were assembled to the circuit boards after the wafer singulation. The standard thermal cycling test was used for reliability testing. A finite element based approach was also used to gain a deeper understanding of the solder joint failure mechanism caused by the repeated thermal stress. According to the test results, the SolderBrace coated dies had much higher lifetime than the non-coated dies. SolderBrace technology may offer a unique method to package low cost high performance WLCSPs. The simulation results also give insight on the stress generation and can provide guidance to appropriate design adjustment.

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Table of Contents

List of Tables

List of Figures

CHAPTER 1

INTRODUCTION

In the era of communications and entertainment, packaging technology is becoming an important issue with the driving force of consumer demand for thin, small and high functionality electronic products including personal computers, cell phones, televisions, and so forth. To meet these requirements, a large diversity of IC packages are being developed.

1.1 Trends in Integrated Circuit (IC) Package

Electronic packaging is traditionally defined as the back-end process that transforms bare integrated circuits (IC) into functional products [1]. The earliest integrated circuits used for high reliability military application were packaged in ceramic flat packs. In the 1960s, flat packs were replaced with dual in-line packages (DIPs), first in ceramic and later in plastic. In the 1980s, pin counts of VLSI circuits exceeded the practical limit for DIP packaging, leading to leadless chip carrier (LCC) and pin grid array (PGA) packages. Surface mount packaging such as small-outline integrated circuit (SOIC) and plastic leaded chip carrier (PLCC) packages appeared in the early 1980s and became very popular in the late 1980s. These packages use finer lead pitch with leads formed as either J-lead or gull-wing. With the entry of thin, small packages and the increase of their packaging densities, quad flat packages (QFPs), thin SOPs (TSOPs), and other packages have been developed consecutively in the late 1990s.

Ball grid arrays (BGAs), which allow for much higher pin count than other package types, have been playing an important role in small, large-capacity packages since the latter half of the 1990s [2]. BGAs have been reduced to sizes comparable to chips, that is, to chip scale packages (CSPs). Driven by the application of CSPs in handheld electronics and wireless handsets, the pace of CSP technology development is accelerating in the semiconductor industry [3]. As the IC feature size decreases and the silicon wafer size increases, high-density packaging technologies have been developing at an accelerating rate and the cost per IC is reduced while the performance is enhanced. To achieve this greater functionality per unit volume for miniature and portable electronic assemblies, wafer level chip scale packaging (WLCSP) has become an important packaging technology for the electronics industry since the package is done at the wafer level rather than individual diepackaging [4]. After packages reach the limit of horizontal dimensions, three dimensional packaging (3D) technologies provide more efficient packages by expanding packages in the vertical dimension. Face-to-face silicon (Si) dies stacking is one of the 3D packaging technologies to form a high density module. With the future trends of increased device complexity, and the requirement for a large diversity of new IC package types to meet specific applications or markets, it will generate an explosion of new creative and disruptive technology packaging solutions. Figure 1.1 indicates the trends in the development of package technology.

1.2 Chip Scale Package

Based on IPC/JEDEC J-STD-012 definition, chip scale package (CSP) is a single-die, direct surface mountable package. It is originally defined as the package that is no greater than 1.2 times the size of the chip. However, some types of CSPs maintain their package size as the internal silicon die reduces in size as a result of the fabrication lithography process gets smaller.

This effect changes the package to die size ratio. More recently the acronym CSP has been redefined as chip size package inferring a 1 : 1 relationship between package and chip size [6]. Chip scale packaging technology combines the best of flip chip assembly and related surface mount technology. It not only provides almost the same size and performance benefits as the bare die chip assembly, but also the advantage of an encapsulated package. The size and weight reduction has driven its faster application in cell phones, laptops and other portable electronics [7].

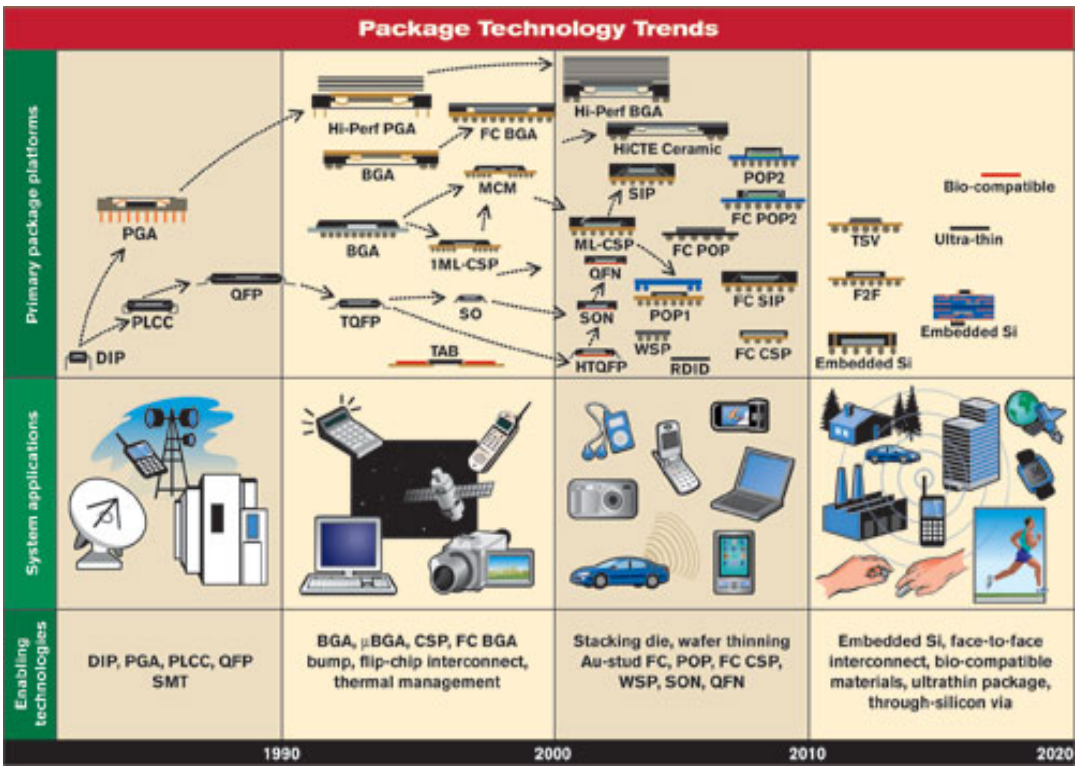


Figure 1.1 Trends in the Packaging Technology [5]

1.3 Wafer Level Chip Scale Package

While chip scale packages have been implemented worldwide in both peripherally leaded and area array format, they are also being pressured to meet demanding cost targets. To ameliorate this matter, most of the world's leading IC companies have packaged ICs directly on the wafer. This concept brings forth a lot of new opportunities and benefits compared to traditional IC packaging methods [8]. The potential economies of processing in this concept result from batch processing, simplified logistics, elimination of bare chip testing and a reduction in materials. Wafer level package (WLP) is one type of chip scale packages, which enables the IC to be attached face down to the printed circuit board (PCB) by conventional SMT assembly methods and the chip's pads connect directly to the PCB pads through individual solder balls. No requirement of bond wires or interposer connections makes wafer level chip scale package (WLCSP) a different technology from other leaded and laminate-based CSPs. The principle advantage is that the IC inductance is minimized while as secondary benefits, both package size and manufacturing cycle time are reduced. [9]. In its simplest form, the WLCSP process technology needs a deposited layer of under bump metallization (UBM) which is patterned over the passivation openings on a wafer. A solder ball is subsequently dropped through a stencil mask on the UBM stack. The wafer is then subjected to a thermal reflow process in an oven. The thermal reflow melts the solder ball and cools it in a well defined shape as shown in Figure 1.2.

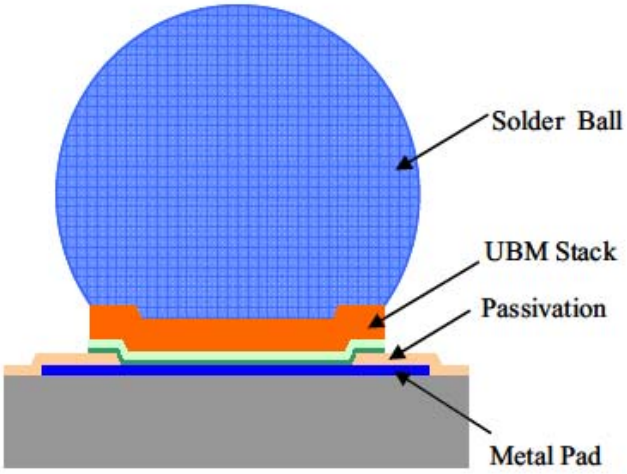


Figure 1.2 Cross section view of WLCSP ball formation [10]

1.4 Solder Joint Fatigue

Thermal mechanical fatigue life of the solder joints has become a bottleneck to apply WLCSP technology in a more complicated package. This thermal mechanical issue is primarily attributed to the thermo mechanical stress in the soldered joints, caused by differences in the coefficient of thermal expansion (CTE) between packaging components. The CTE mismatch can strain solder joint connections, and over the component lifetime can contribute to mechanical solder joint fatigue failure [11].

A Coffin-Manson type equation is the most popular equation in literature for predicting solder joint fatigue [12]. The first-order approximation of the solder joint fatigue life is described by the equation shown in Figure 1.3. The important mechanical variables in this equation are: 1) the bump standoff (h); 2) ball distance from neutral point, DNP (L), which is determined by the bump pitch and chip size (see Fig 1.4); 3) the coefficient of thermal expansion difference ($\Delta\alpha$); and 4) the temperature change (ΔT). The Coffin–Manson equation predicts that the thermal

fatigue lifetime of a solder joint is proportional to the square of the bump standoff and inversely proportional to the square of DNP, Δα, and ΔT. Therefore, the solder joint reliability can be enhanced by using smaller die, lower CTE mismatch, smaller temperature range of operation and the higher standoff height [13].

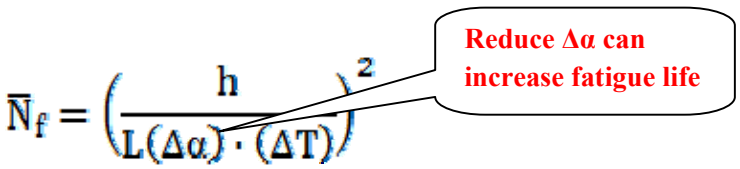


Figure 1.3 Coffin-Manson low cycle fatigue equation

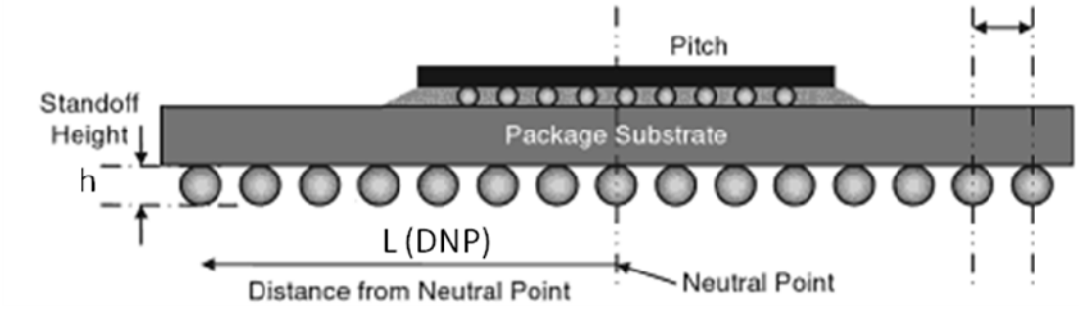


Figure 1.4 Distance from netural point for a BGA type package [14]

1.5 Photo-definable Epoxy Resin

Epoxy resins have long been widely used in industries due to their ease of processing, less curing shrinkage, excellent heat and chemical resistance, low cost, and extreme versatility in chemical structures. However, the large CTE mismatch between the neat epoxy resin (50-80 ppm/K) and the silicon chip (2.8 ppm/K) results in a huge amount of stress at the interface

leading to the solder joint failure. This stress effect is pronounced in the large area application on the whole wafer [15]. Since the early 1960's, ceramic substrate materials have been assembled into the electronic packaging industries. The introduction of well dispersed low CTE ceramic fillers into a polymer matrix has been demonstrated to be extremely effective to reduce the CTE, increase the elastic modulus, and therefore improve the performance of the polymer. The higher the amount of fillers content that can be added into the polymer, the lower is the CTE of the polymer composites [16]. Due to the high Si-O bond energy, the low CTE SiO2 (silica) filled composite materials have been widely used to reduce the CTE of epoxy and improve the mechanical properties [17]. Figure 1.5 shows the schematic illustration of polymer coated ceramic filler. Here the filler particle is assumed in the round shape.

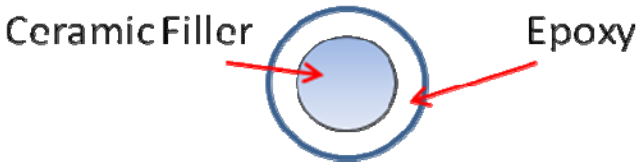


Figure 1.5 Polymer coated ceramic filler particle

In recent years, a number of investigations have demonstrated the feasibility of photo-polymerization for curing thick polymers and their composites. These polymers can be categorized into two types, depending on whether the polymerization proceeds by a radical-type or cationic-type reaction. The first type is based on the acrylate or vinyl compounds initiated by the free radical, while the second one is based on the photo-initiated cationic polymerization. Due to the high reactivity, radical-type systems are by far the most widely studied and used in today's photo curing application [18-20]. Before the study conducted by Dr. C.P. Wong's group at Georgia Tech [21], there are only a few reports in the photo-polymerization of silica/epoxy

composites via the cationic crosslinking reaction because silica fillers with micrometer size can scatter the UV light, impede the photo reaction, and hence are incompatible with the photo-polymerization process. Based upon their results, nanosilica composites have displayed desirable optical properties and were chosen as the filler to reduce the thermal expansion of photo-definable epoxy material. A photo-sensitive initiator was added into the formulation, releasing the cations after UV exposure and initiating the epoxy crosslinking reaction. This photo-crosslink reaction makes the epoxy a negative photoresist that can be utilized in the fabrication process, and also make it a good wafer level protective material [22].

1.6 Research Objective and Outlines

The objective of this research was to develop a new WLCSP fabrication process with the use of a wafer level SolderBrace coating to achieve low cost reliability improvement. This SolderBrace material is a kind of photo-definable epoxy resin which not only replaces the capillary underfills (the process that employs capillary action to underfill the die to substrate undergap), but also replaces the final passivation layer of the silicon device fabrication process, making it an attractive low cost solution for future WLCSP designs. The package proposed here has a single bump solder joint geometry with a thick coating of SolderBrace material deposited on the die. Processing of this coating layer can be achieved by two methods. The first is done at the wafer level using the standard semiconductor lithography processing method. The second application process involves printing the material on the pre-balled wafers followed by the solder cleaning and cure.

Figure 1.6 outlines the steps for the first method. The coating is spin applied, UV defined, and bumped. Figure 1.7 outlines the processing steps for the second method with printing over

bumped wafers. The coating is stencil printed over the pre-balled wafer, pre-baked, the uncured film on top of the solder balls is cleaned, and cured at high temperature. While both UV defined and print over ball methods of SolderBrace application are used to address the solder/die junction stress, the materials differ significantly in their formulation.

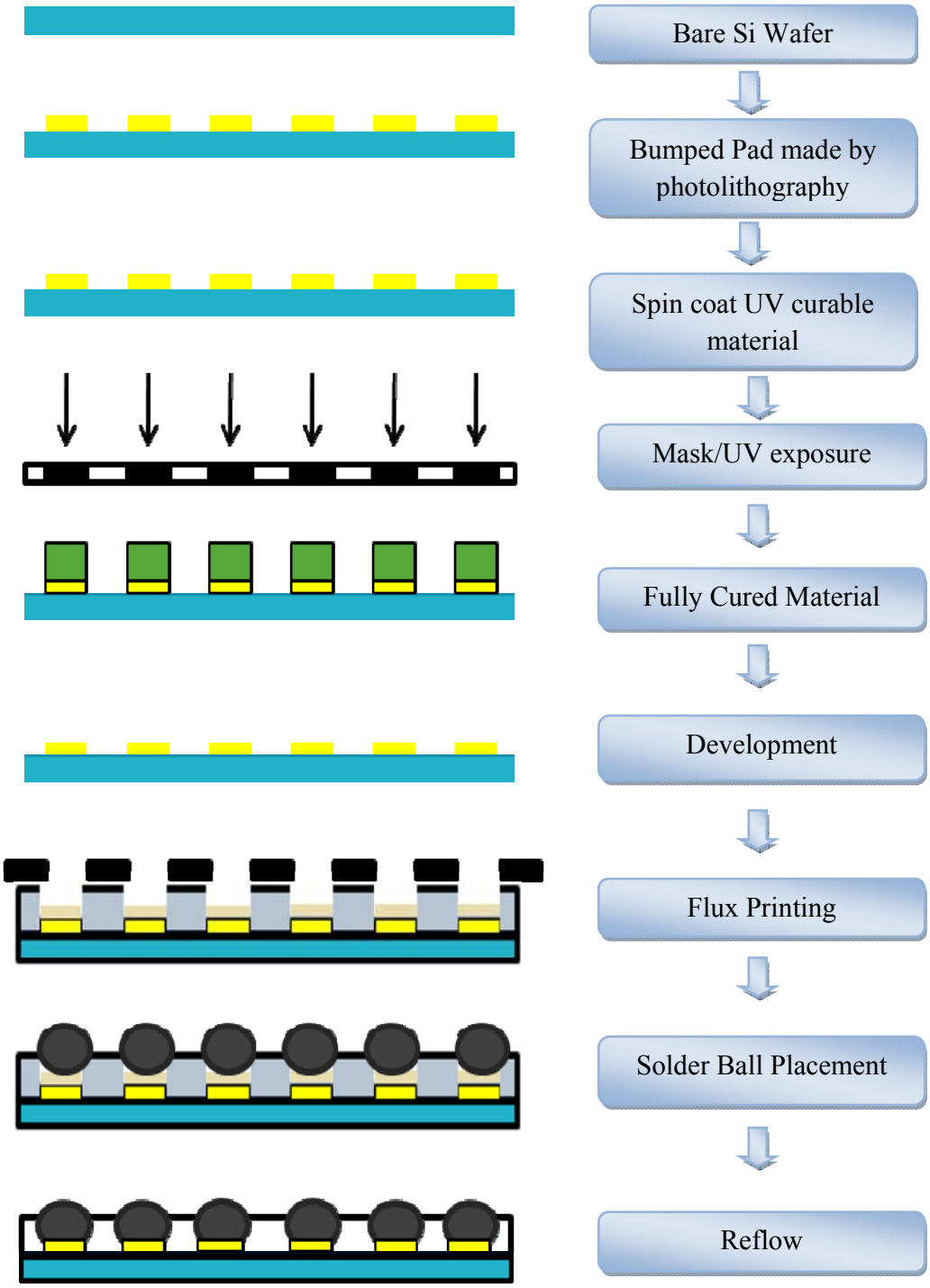


Figure 1.6 Application method of SolderBrace material by UV definition

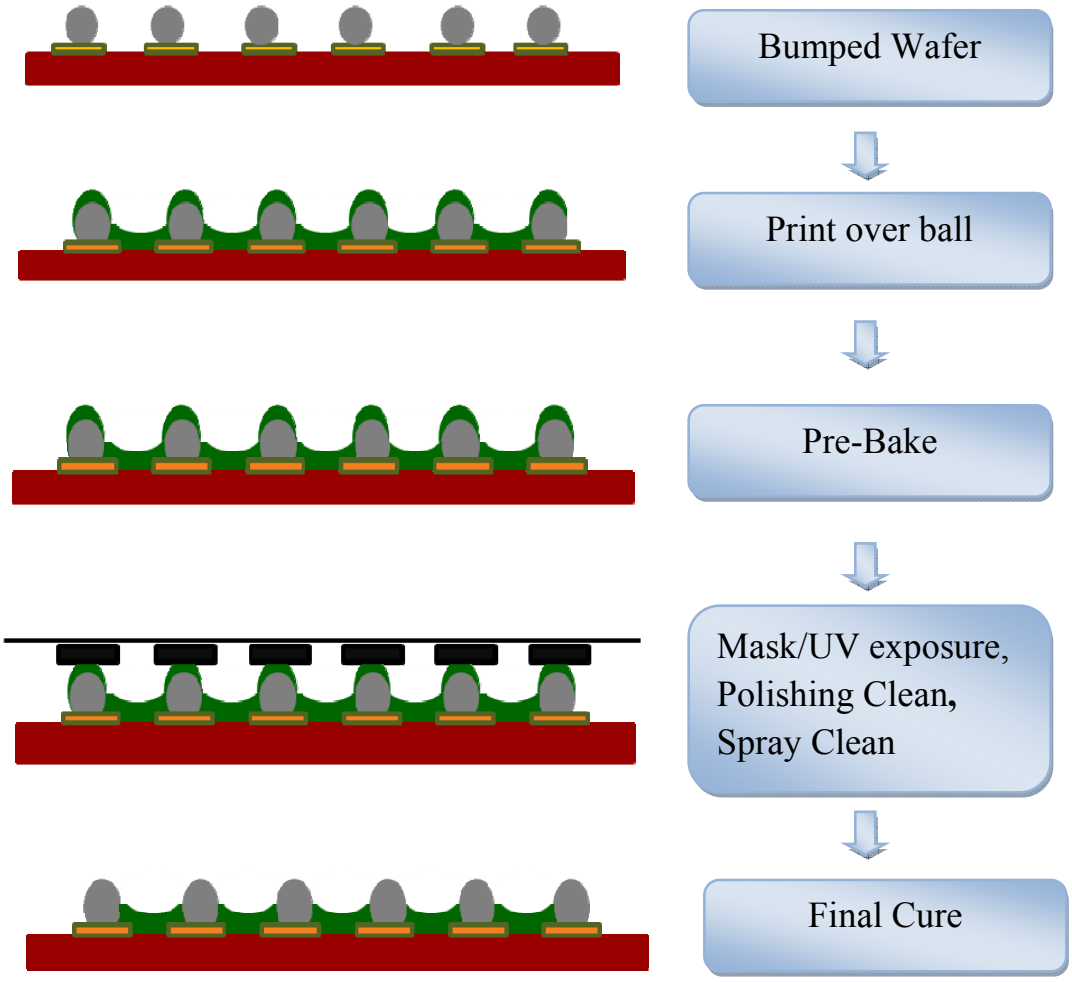


Figure 1.7 Application of SolderBrace Material by printing over balled wafer

Chapter 2 reviews the wafer level chip scale package (WLCSP) technology including its process flow, technical challenges, reliability issues and current approaches for solder joint reliability improvement. In addition, a new SolderBracing technology is introduced as a cost effective solution to WLCSP protection. Chapter 3 presents the fabrication process development for WLCSP dies such as photolithography, wet/dry etching, and electroless plating. A number of different types of SolderBrace materials are also described and selected to optimize the processing parameters. In Chapter 4, the assembling processes as well as the results of failure analysis for WLCSPs with and without SolderBrace material are discussed in detail, which include alternate processing approaches to apply the SolderBrace materials. Furthermore, Chapter 5 describes a 3D finite element model established for both packages. FEM results were compared in terms of stress, and failure locations. Conclusions and suggestions for future work are summarized in Chapter 6.

CHAPTER 2

LITERATURE REVIEW

2.1 Chip Scale Package Technology

Over the past decade, chip scale packages (CSPs) have evolved from an imaginative, leading-edge innovation to a mainstream technology. CSPs are mainly used for electronic devices requiring a smaller implementation area on the board since they are extremely small physical size and they have the ability to enable improved electrical performance.

2.1.1 Background

The term chip scale package (CSP) began to be used in the mid 1990s. The pace of CSP technology development is accelerating in the microelectronics industry, driven by broad adoption of CSPs in the portable electronics market. The utility of the CSPs lies in their ability to route out fine pitch peripheral die into course pitch area array footprints on the PCB. CSPs have grown from 158 million units in 1997 to more than 1 billion units in 1999 [23].

Due to the variety of CSPs developed in the industry, one can not make any generalized assumptions on the reliability or manufacturability of the CSPs as a homogeneous package group. CSPs are often classified based upon their structure. It is very important to determine what the structure of the CSP is before making any conclusion on its robustness or manufacturability [24]. At least five major categories have been proposed. These are: flex circuit interposer, rigid substrate interposer, custom lead frame, transfer molded, and wafer-level assembly. Examples of

these categorized packages as well as their manufactures are given in Figure 2.1. Lead frame, flex and rigid substrate CSPs occupy the bulk of the current CSP market due to their better fit into the current packaging infrastructure. These CSP packages are processed as conventional packages. However, the most intriguing CSPs are the wafer level assembly type in which the area array "package" is manufactured and usually tested on the wafer before dicing [6]. The CSP (shown in Figure 2.2 as a flex interposer type) is a cost effective first level package. It is often used for single or dynamic random access memories, lower I/O count microprocessors, and flash memories. Typical packages are those with a pin count in the range of 4 to 256 with sizes between 2 and 21 mm per side [23].

2.1.2 Advantages and Disadvantages

Chip Scale Packages combine the best of flip chip assembly and surface mount technology. In comparison to the standard surface mount technology, CSPs have the following advantages [26]:

- Reduced footprint and thickness
- Reduced weight
- Relatively easier assembly process lower over-all production costs
- Better electrical performance
- Area array distribution of connections (for most CSPs)

In comparison to the bare die assembly, CSPs have the advantages such as [27]:

- Reworkability
- Encapsulated package
- Testability

- Mountable with conventional assembly line
- Accommodates die shrinkage without changing package footprint
- Some CSPs do not require underfill when mounted on organic substrates

However, CSPs also have some disadvantages such as limited package/assembly data availability, moisture sensitivity, potential high cost, and packages with high I/O counts require expensive high-density boards, etc.

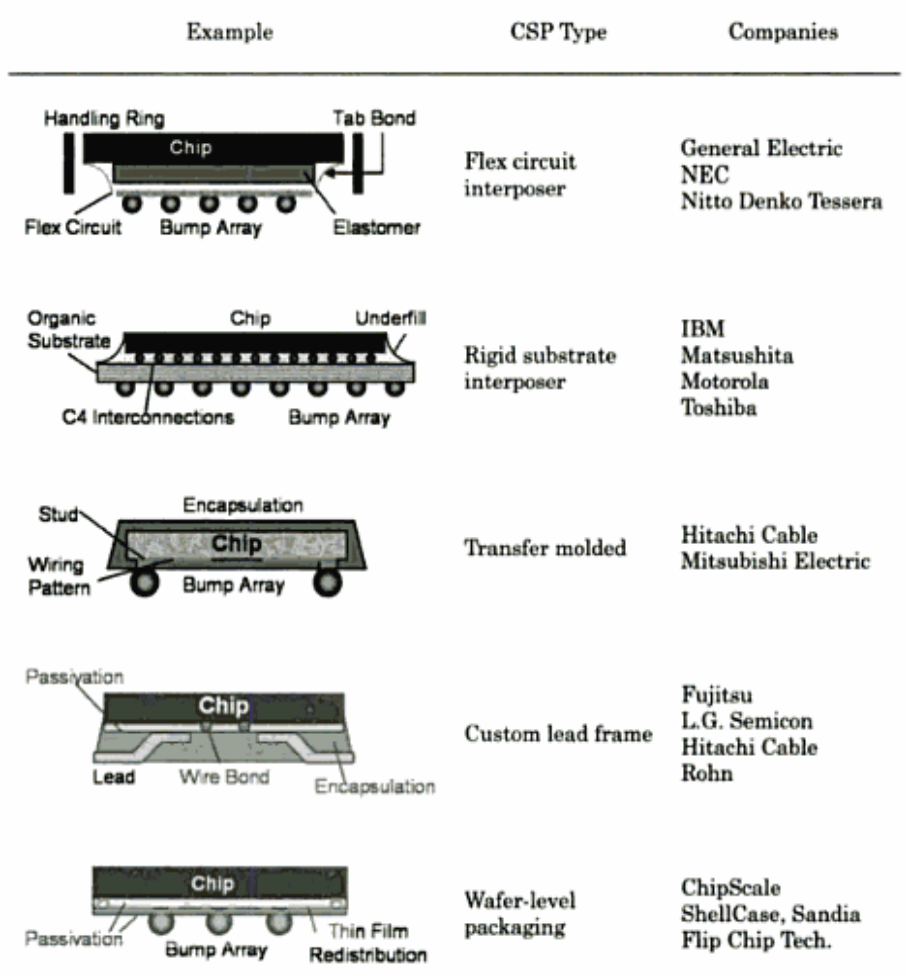


Figure 2.1 Main CSP Categories [23]

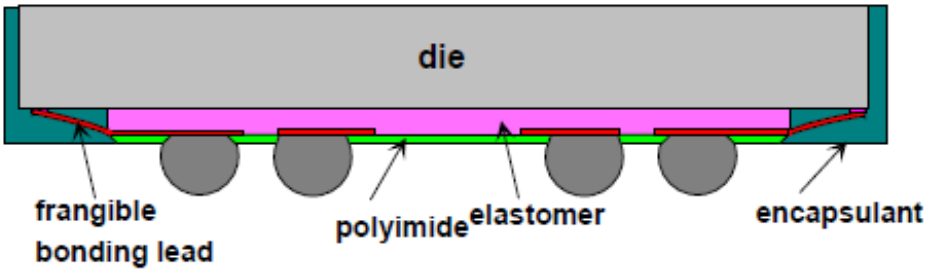


Figure 2.2 Example of a flex tape style CSP [25]

2.2 Wafer Level Chip Scale Packaging Technology

2.2.1 Background

Instead of the traditional process of assembling individual units in packages after dicing them from a wafer, wafer level chip scale packaging technology packages an integrated circuit at the wafer level. This process is basically an extension of the wafer fab processes, where the device protections and interconnects are accomplished using the traditional fab processes and tools. In the final form, the device is essentially a die with an array pattern of solder balls or bumps attached at an I/O pitch that is compatible with traditional circuit board assembly processes [28]. One of the features of most WLCSP structures is the application of a metal layer to redistribute the fine pitch pads on the chip to larger pitch area arrayed pads with much taller solder joints on the substrate. This technology not only provides the means of external connection, but also improves the reliability by allowing the use of larger and more robust balls for interconnection (Figure 2.3) [29].

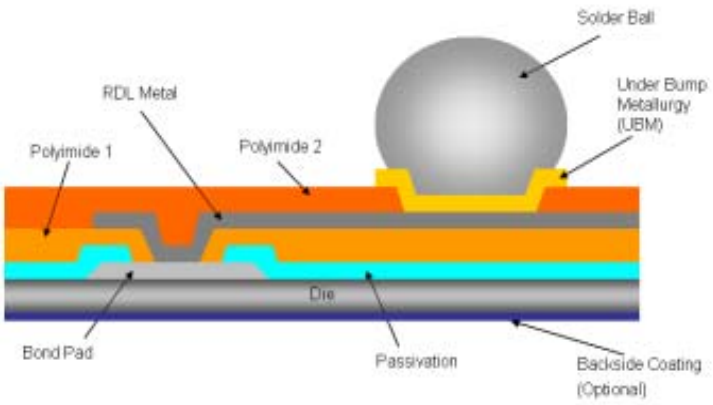


Figure 2.3 Cross section of a typical Polyimide-RDL WLCSP [28]

WLCSP combines the conventional chip scale package advantages of thinning, miniaturizing, low mass packaged chips, and ease of handling with an efficient volume production approach based upon batch packaging at the wafer level [30]. Table 2.1 compares the differences between traditional packaging and wafer level packaging [8].

Many companies around the world are developing or have begun providing devices packaged in chip size fashion. Amkor, Fujitsu, Shell Case, Chip Scale, Oki, Unitive, Flip Chip Technologies (FCT), Fraunhoffer Technical University, Tessera, and some other companies have all shown diligence in the area [8]. Although all of these technologies result in packaged area array chips, the technologies still differ, sometimes significantly, in processing steps such as redistribution technologies, encapsulated technologies, and flex tape technologies. Table 2.2 lists and compares the key process features for most of manufactures [6] while Figure 2.4 shows some of their products such as (1). The Casio Wrist Camera with super CSP 48 developed by Fuji, (2). The Ultra CSP by Flip chip International, (3). The National Semiconductor Micro-SMD, (4). The Ericsson Bluetooth, and (5). The Tessera Wafer-Level Camera (WLC) technologies.

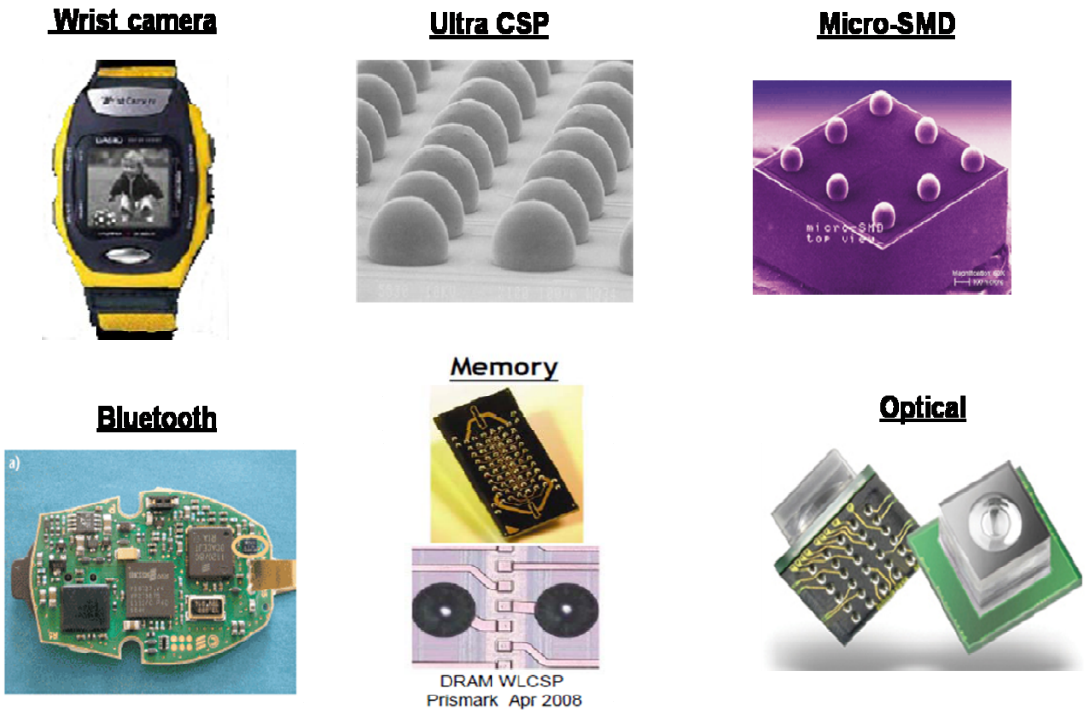


Figure 2.4 Examples of WLCSP [31-35]

Table 2.1 Comparison between traditional packaging and wafer level packaging [8]

Traditional IC Packaging	**Wafer level Packaging**
Current Situation	**Current Opportunity**
Wafer is probed, diced and sorted	Wafer moved directly to packaging
ICs packaged away from fab	ICs packaged in fab
ICs are packaged one at a time	ICs are packaged en masse
Burn in performed in sockets	Burn in performed on wafer
Device tested two to three times	Device tested once
Current Situation	**Next generation opportunity**
Power and ground taken from PCB	Power and ground distributed in assembled structure
High pin counts required	Lower external I/O possible
Less than optimal power to performance efficiency	Power to performance efficiency increase possible
All function in the chip	Function shared between package and chip
More complex substrate required	Simpler substrates possible
Lead inductance concerns	Lead inductance nearly eliminated

Table 2.2 Comparison of Wafer Level Chip Scale Packaging Technologies[6]

Company	Technology	Feature	UBM	Dielectric	Solder Bump Ball dia / pitch (mm)
Amkor	wsCSP™	WB connection Cu/PI film	NA	PI film	0.3-0.5 / 0.5-0.8
FCT	Ultra CSP™	redistribution	Al/NiV/Cu	BCB	0.35-0.5 / 0.5-0.8
FormFactor	MOST™	WB "springs"	NA	NA	NA
Fujitsu	Super CSP™	Encapsulated 0.1 mm Cu posts	Ti/Ni/Cu	PI	0.35-0.5 / 0.5-0.8
IZM Berlin	-	Cu redistribution	TiW/Cu/Ni/Au	BCB	0.3 /
Intarsia	MicroSMT™	Epoxy Si/glass encapsulation	Ti/Cu/Ni/Au	proprietary	0.3
Oki	-	CMP encapsulated Cu posts	-	PI	-
Shellcase	Shell BGA™	Glass encapsulation	Ni/Au	BCB Epoxy	0.3
Tessera	WAVE™	Cu/PI film Low modulus encapsulant		PI film	-
Unitive	-	redistribution	Al/Ti/Cr-Cu	BCB	Plated bumps 0.125 – 0.25

2.2.2 WLCSP Process Flow

In the semiconductor industry, front-end corresponds to the wafer fabrication process while back-end corresponds to product assembly, packaging and testing operations [36]. There are two types of back-end process flows, one is for wafers with in-situ bump formation and the other is for wafers requiring the placement of preformed solder balls for larger bumps. Figure 2.5 shows two separate paths for the backend processing of bumped wafers. One processes wafers with bumps already formed in the bumping front end and the other includes the process steps required for reflowing preformed solder balls [37].

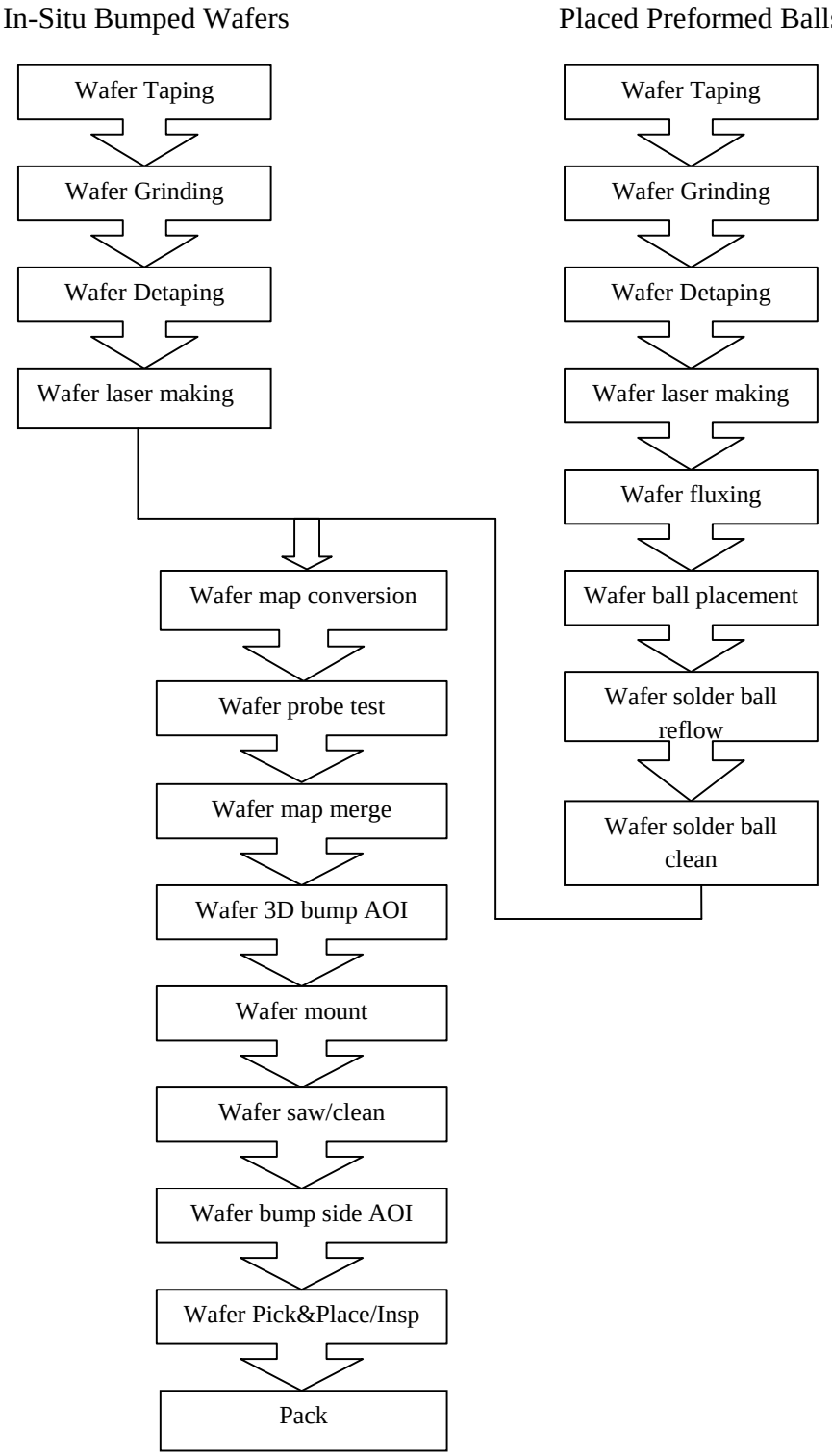


Figure 2.5 Bumping Backend Process Flow [37]

2.2.3 Technical Challenges

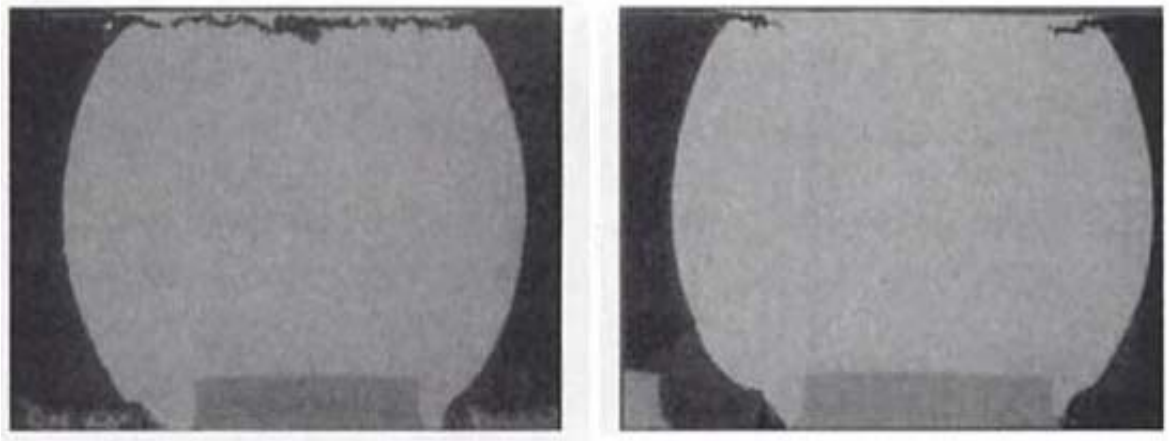
Just like many other new technologies, WLCSPs, especially for solder-bumped WLCSPs, face many critical issues listed below and still have room for improvement [38]:

- High cost for poor-yield IC wafers
- High cost for low wafer-bumping yield, especially for high-cost dies
- Wafer-level redistribution and wafer bumping is still too costly
- PCB assembly of WLCSP is more difficult
- Impact of lead-free solder regulations on WLCSP
- Limitation for large die and high I/O devices in high performance applications
- Solder joint reliability is more critical

2.2.4 Reliability

Reliability is the ability of a device to conform to its mechanical and electrical specifications over a given period of time under specified conditions at a specified confidence level. Solder joint reliability has become very important in recent years as a result of several factors such as the emergence of fine pitch surface mount packages, and the shift of the semiconductor industry to lead free solder. It is a measure of the possibility that a solder joint will not fail throughout its intended operating life, subject to the various thermo-mechanical stresses during its operation. Component-level and board-level are two main aspects of solder joint reliability, which are respectively dealing with the reliability of solder joints within the package structure itself prior to the board mounting and the reliability after the board mounting. Board-level solder joint reliability is usually more representative of the reliability of a package operating in the field. Creep failure, fatigue, and tensile rupture are the three major mechanisms

of solder joint failure, and they often interplay with each other simultaneously. As to the WLCSP assemblies, solder joint fatigue is a serious concern that is caused by cyclical stress or loads [39-40]. In traditional WLCSP structures without underfill, due to the global expansion mismatch between the component and the test board, as well as the local expansion mismatch between the solder and the test board or the solder and the Si die, the solder joints suffer very large shear stresses [41]. Thermal cycling test is a useful qualification test for applications that have significant changes in ambient temperature throughout the life of the product. During the cycling process, the solder joints are subject to more shear strains for larger die sizes or distance to the neutral point [42]. Figure 2.6 shows the thermal fatigue failure of UltraCSP solder balls from the Flip Chip Technologies. One set of UltraCSP specimens was mounted on ceramic substrates without underfill. The testing conditions were -40^{o}C to 125^{o}C with a cycle period of 80 min. The thermal fatigue failure of the solder is near the chip side [43].



(a) (b)

Figure 2.6 (a).Thermal fatigue failure of UltraCSP solder ball and (b). Partial thermal fatigue failure of UltraCSP solder ball from Flip Chip technologies

2.2.5 Current approaches to improve reliability

An extensive amount of work, focused on improving the reliability of WLCSP, has been developed to reduce shear stresses in the solder joints, especially for the large die application with WLCSP technology.

One of the improvements is the application of the soft stress buffer layer (SBL) structure which is formed under the solder bumps to reduce the shear stress in the solder joints [44-47]. This thick SBL coated on the die side can enhance packaging reliability, but the manufacturing process is difficult and the production cost is high. The silicone material introduced by IMEC research center is one example that is able to absorb deformations and reduce stresses created in the device by the CTE mismatches of different materials. These patternable silicones were integrated into a silicone under bump (SUB) design which improved the solder joint reliability through reduction of the strain experienced by the solder. Figure 2.7 shows a schematic view of SUB configuration. The process protocols for building a silicone under the bump wafer level package using both photo-patternable silicones and printable silicones (see Figure 2.8) [48].

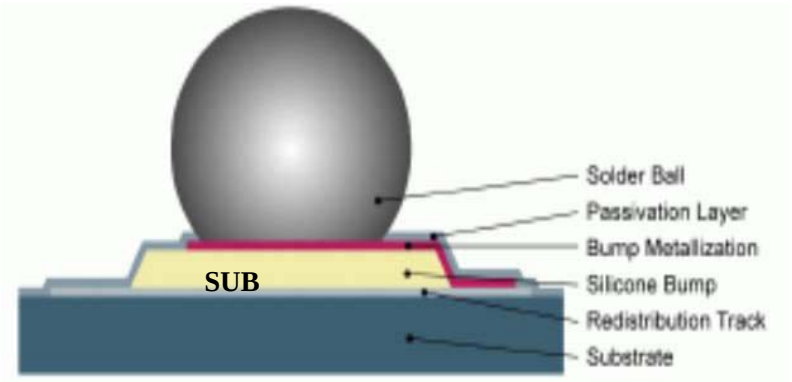
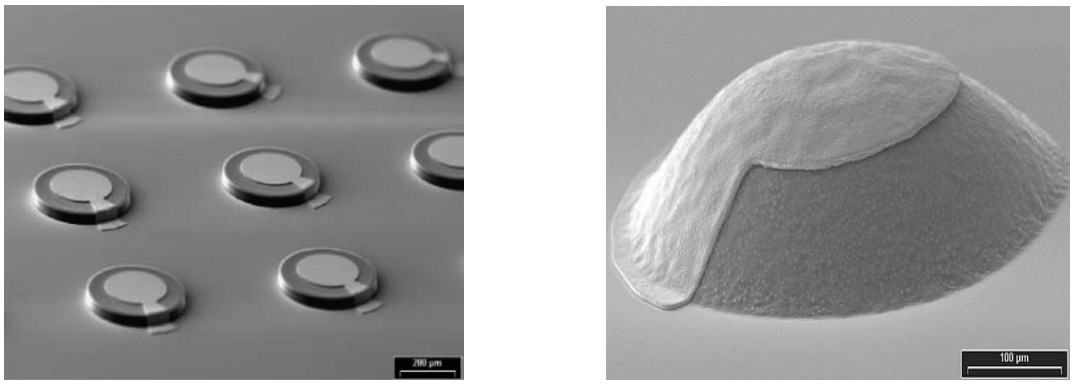


Figure 2.7 Illustration of SUB build-up



(a) (b)

Figure 2.8(a). Metalized photo-paternable silicone bumps and (b). Stencil printed silicon bumps [48]

Another stress release method was developed by the Fujitsu Co. by forming high copper posts to increase the gap between the chip and PCB. This chip-sized package is marketed by the trademark name SuperCSP [46]. Figure 2.9 shows a cross-sectional view and layer structure of this package. The processes of making the SuperCSP involve several main steps such as the redistribution traces and metal post forming, encapsulating the wafer, and peeling the film. First the peripheral pads on the wafer are rearranged in a real array pattern after photolithographic plating. About 100 μm high metal posts are then fabricated on the wafer. After encapsulating the entire surface of the wafer, a package having the same size as the chip is fabricated using a wafer-level packaging method. The connecting portion of copper post and solder ball has a strong structure that can tolerate the stress because solder balls catch hold of the entire surface of copper posts, which stick out from the encapsulant and have a mound-like structure [49].

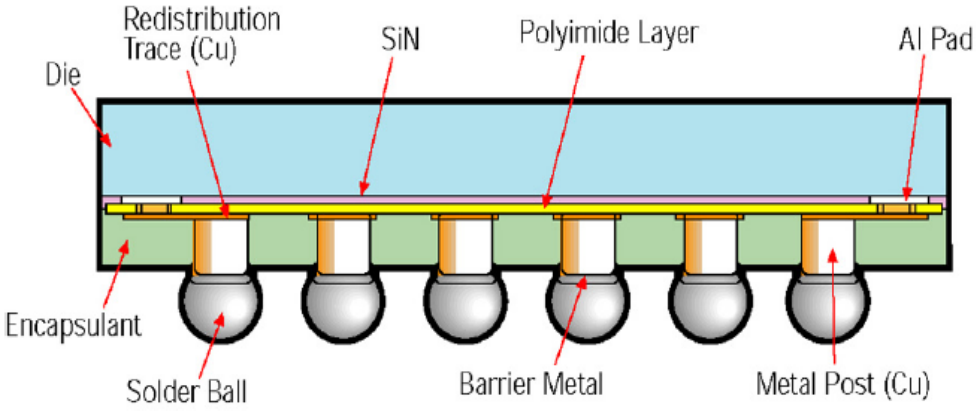
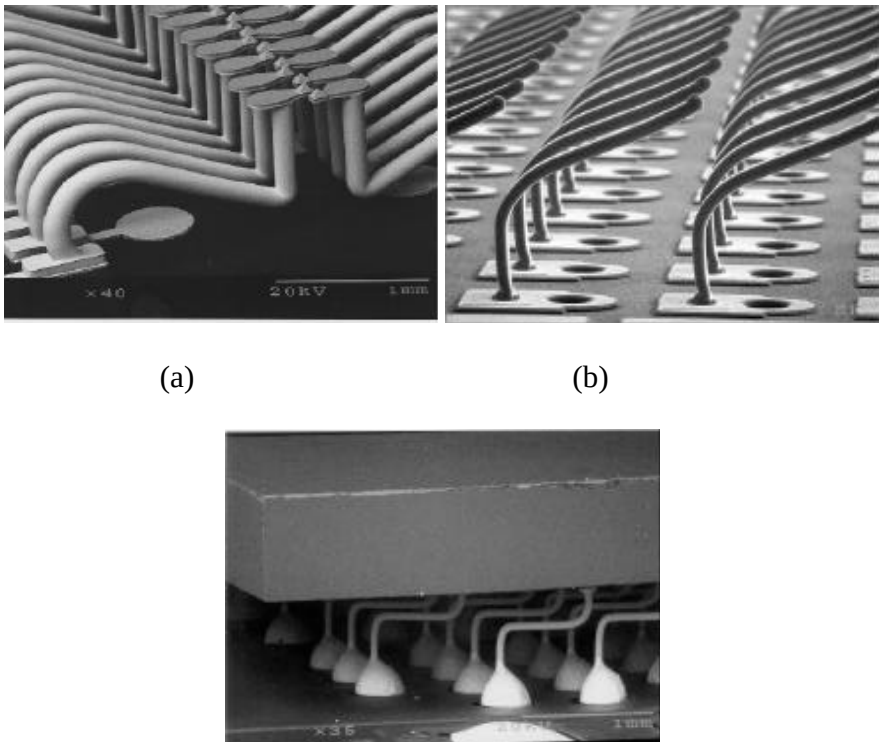


Figure 2.9 Cross section of package structure of Fujitsu's Super CSP [49]

FormFactor developed the so-called MOST WLCSP with a compliant bump structure based on their microspring technology. Microsrpings created by extending wire bonding technology are formed as a joint for the electrical circuit between the silicon chip and the FR-4 substrate. This spring can easily deform under any mechanical stresses [47]. Several examples of Microspring technology are shown in Figure 2.10.

Fraunhofer IZM/Technical University of Berlin developed a wafer level package using a double ball. The technological structure of this double-ball CSP is a pad redistributed die with a solder ball array. A stress compensation layer embeds the first solder balls before the second solder balls are stencil printed or placed on top of embedded balls. Figure 2.11 shows a schematic process flow of the redistribution and bumping technology for this WL-CSP. The first screen-printed solder balls can be covered in a CTE matched "underfill" and mechanically polished to expose the solder balls, and then solder balls can be placed at these sites. This produces a solder ball stack that is ~2x the height of a normal solder ball, while the half

"underfilled" structure distributes the stress on the solder columns and protects the redistribution layer from stress concentrations. Such structures have shown ~2x the cycles to first fail in thermal cycling [50].



(a) (b)

(c)

Figure 2.10 Examples of Microspring technology (a). Probe Cards (b). Sockets Interposers (c). Die Size Spring Grid Array (DSSGA) Modules

National Semiconductor enlarged the passivation layer opening at the solder die interface to improve the solder joint reliability [51], and a WLCSP technology evaluated by Keser in Motorola SPS demonstrated that board level solder joint reliability of the WLCSP can be improved through wafer thinning [52].

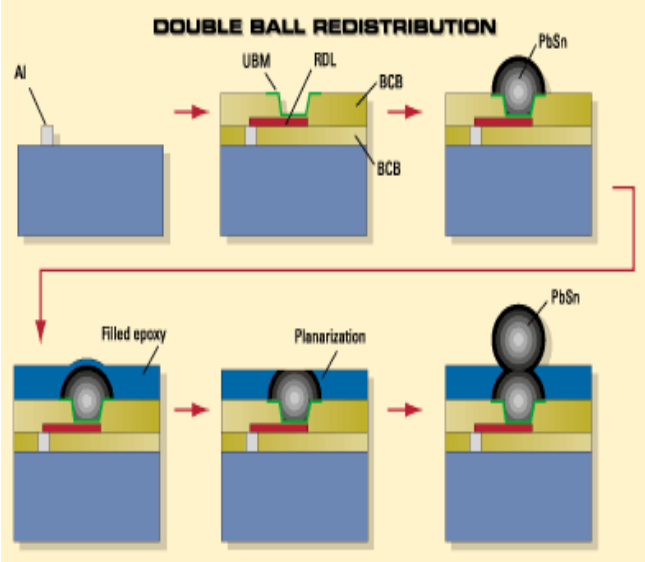


Figure 2.11 Schematic process flow of the double ball redistribution and bumping technology

However, some issues still remain to be improved before these technologies can be considered for widespread use such as the complex processes and higher production costs.

2.3 Solder Bracing Technology

2.3.1 Protection Options

No-flow underfill materials (this material eliminates the need for flow time and cure time after reflow), molding compounds (composite materials consisting of epoxy resins, silicas, catalysts, mold release agents, etc) , capillary underfills (a post-reflow process that is dispensed after the formation of the solder joints between the chip and substrate), and corner/edge bonding adhesives have been proven successfully in increasing CSP reliability. They are adhesives that rely on strong surface to surface bonding between the die, solder interconnect, and the board to achieve high reliability packages. However, these solutions are sometimes cost-prohibitive and they also lack convenient reworkability. Successful low cost reliability solutions for WLCSPs

have generally been the modification of existing materials such as the adaptation of redistribution layer materials and solder types, but these solutions still have the limitation of increased performance.

In addition to the assembly adhesives that fill the gap between the die and board, solder bracing is another WLCSP protection scheme to delocalize the stress of solder under the die. Unlike adhesives, there is no adhesive bond between the die and board which makes solder bracing a reworkable process. Since the packaging is done at the wafer level, relative low cost becomes the biggest advantage of solder bracing.

The future trend of die protection may combine the functions of both technologies, and it follows the needs for new chemical technologies that are capable of minimizing any impact on assembly cost and improvement of reliability [53-54].

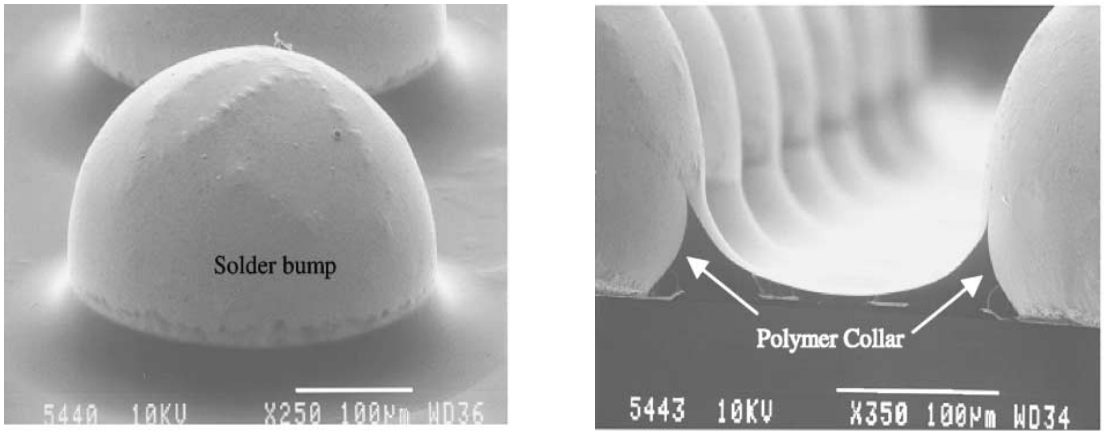
2.3.2 PolymerCollar WLP

Conceptually, solder bracing is defined for any material that mechanically supports the solder and the front side of the die. Few commercial wafer level solder bracing materials are available to date. PolymerCollar WLP is the most notable example of solder bracing. Figure 2.12 shows some photos of PolymerCollar WLP built on an Ultra CSP 50 daisy chain test wafer. It is a WLP having a wafer-applied polymer reinforcement structure that surrounds the solder joints to transfer the stress away from the interconnection joint. This PolymerCollar material performs two functions: One is a fluxing action during solder ball attachment and the other is to form the polymer reinforcement structure itself. The main process flow consists of:

- Application of Polymer Collar material instead of solder flux on chip side UBM pad
- Placement of preformed solder balls onto the Polymer Collar material

- Reflow
- Final cure of the polymer material

Since the base of the bump receives the most stress during the device lifetime, the addition of the Polymer Collar improves solder joint reliability by up to 50% over the standard *Ultra*CSP process[43,55]. However, it was also found that the Polymer Collar material did not produce significant solder life improvements in SAC lead-free solder joints when compared with the improvement in eutetic Sn-Pb solder joints during the same test [55].



(a) (b)

Figure 2.12 PolymerCollar WLP (a), and a cleaved section of Polymer Collar WLP (b)

2.3.3 Processing of SolderBrace Material

The concept of a solid, preformed, wafer applied brace can also be realized through coating application [56-57]. The coating method is either spin coating or stencil printing. All of the steps

are “low temperature” wafer level steps except the solder reflow. Figure 2.13 describes a process flow of a laser ablated coating-type wafer level solder brace, including spin coating, curing, laser ablation of solder vias, and bumping. This film method demonstrates a good method of forming a solder brace [53].

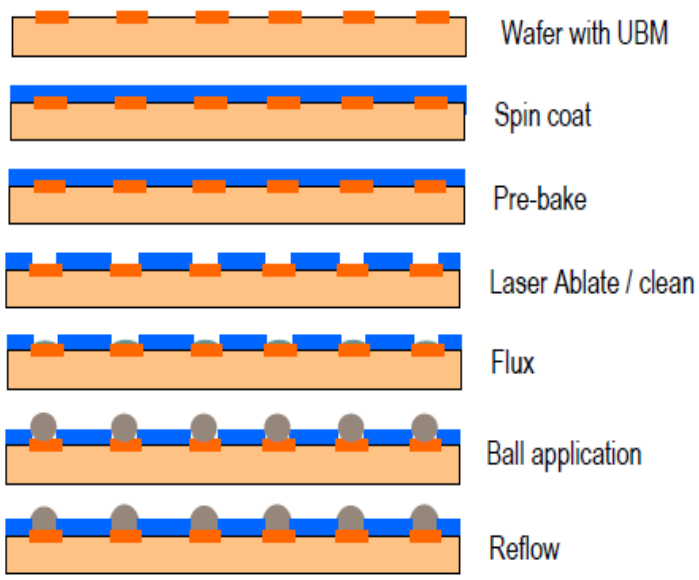


Figure 2.13 Process flow of a laser ablated coating-type wafer level solder brace

Figure 2.14 outlines another method to introduce a solder brace type material to the WLCSP without laser ablated via opening processing. Based upon a bumped wafer, the coating is printed over the balls, back groud and cleaned to expose the solder, and re-bumped. This process can improve the reliability of the package by increasing the standoff height [53,57].

The application of photo-defined material has simplified the coating-type bracing process flow without the need for laser ablation or re-bumping [24]. This process requires a UV sensitive material that can cure in the thick films. Figure 2.15 describes a process flow by the photo-definition method.

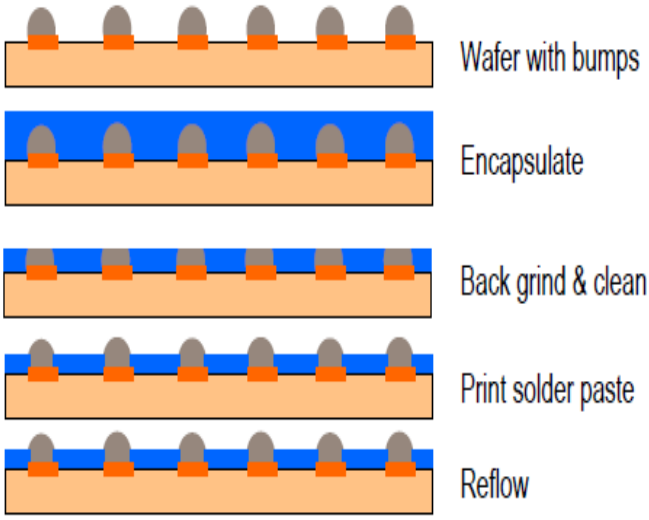


Figure 2.14 Process flow of a back grind and double bump coating-type wafer level solder brace

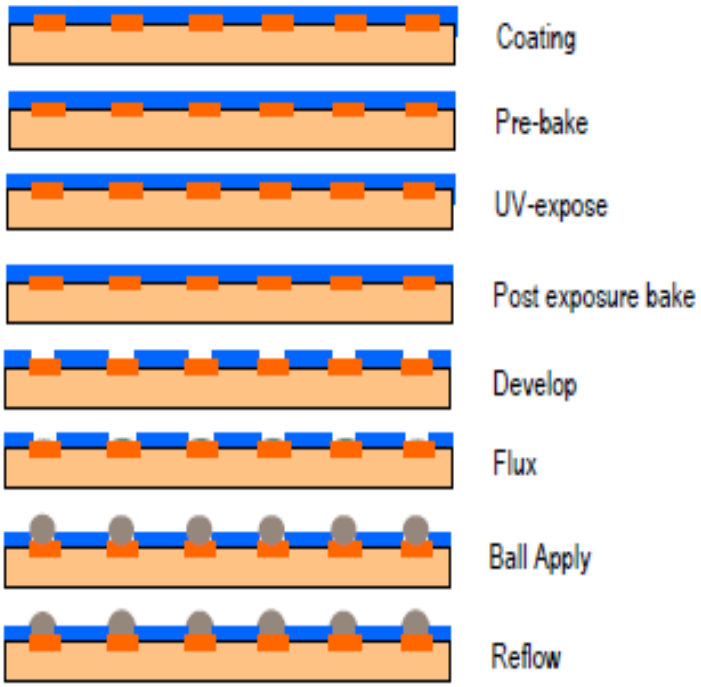


Figure 2.15 Application method of SolderBrace by photo definition

2.3.4 Optimized SolderBrace Material developed by Lord Corporation

In the development of a wafer-level underfill targeted at fulfilling the needs of future designs such as fine pitch and 3D wafer level packaging, Lord Corporation has developed a new SolderBrace Material which is being presented as an alternative to underfill. It is a photo-imigable frontside molding compound with a low CTE that can increases the reliability of the package without added cost. More specifically, this SolderBrace technology is a partial underfill in which a thick coating is deposited on the underside of the die at the wafer level by utilizing the same back-end tools normally used in polyimide processing. The wafer-coated material is either spin coated or printed first, and then goes through a low-temperature pre-bake and UV exposure process. The cross section of a SolderBrace supported solder bump is shown in the Figure 2.16.

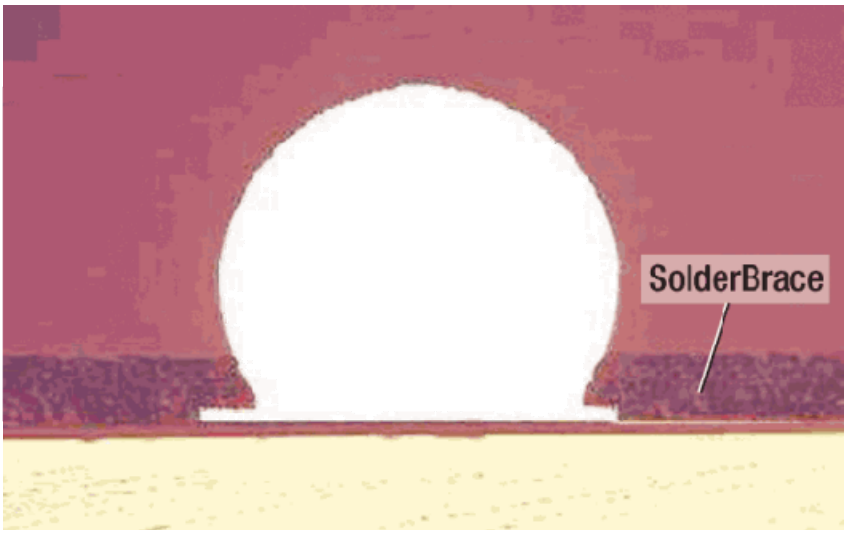


Figure 2.16 Cross section of a WLCSP 250μm solder bump supported by the thick front-side passivation SolderBrace [58].

Since the material developed by Lord is photo-sensitive, certain mask dimensions can not be photo-imaged. The current generation of SolderBrace commercialized is mainly targeted at CSP pitches ranging from 0.3mm to 1mm. In order to expand the application to fine pitch and maskless applications, a second-generation wafer-level Solderbrace material is now under development by Lord Scientists. It will improve the resolution by changing the curative formulation and material chemistry to minimize the amount of scattering that usually occurs in a thick coating [58].

2.4 Summary

Use of large die WLCSPs is a rapid growth area which needs cost effective packaging. To address the improved board level solder joint reliability, typical costly stress-relieving methods such as molding compounds and capillary underfills have been utilized by many designers.

Wafer level solder bracing is a new technology and cost effective solution to WLCSP protection. It delivers the improved reliability by conventional tools and short process times. The photo-defined SolderBrace materials are similar to polyimide in their UV processing steps, but have extra flexibility of being processed in other ways such as printing over balled wafer.

CHAPTER 3

WLCSP DIE FABRCIATION

In this study, the WLSCP was designed as a daisy chain to allow in-situ measurement of the resistance during the accelerated temperature cycling testing. Area array solder bumps were used to form electrical connections to the PCB. WLCSPs with and without SolderBrace materials were fabricated using known standard methods at the Alabama Microelectronics Science and Technology Center (AMSTC). The die fabrication process will be discussed in this chapter.

3.1 Test Die Dimension

As shown in Figure 3.1, the die size was 6mm x 6mm, with a bump diameter of 300μm in a 6 x 6 (36 I/O) full area array pattern on a 800μm pitch. The wafer, e.g. die, thickness was approximately 560 μm. “LASI 7” software was utilized to design the geometry of the die as well as the photomasks.

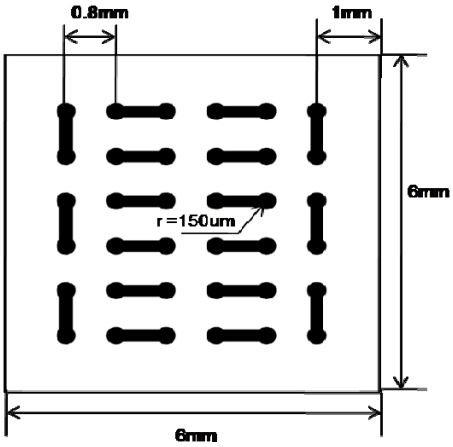


Figure 3.1 6mm x 6mm daisy chained test die

3.2 Standard Die Fabrication

Two types of test dies were designed and fabricated as summarized in Table 3.1. Die A was built for initial process development while die B was optimized to improving the device reliability. Figure 3.2 shows a piece of patterned wafer with the dielectric layer and metal pads. Each singulated die could be either used as a standard die (control sample die) or the starting point for a SolderBrace die.

Table 3.1 Test Die used for Reliability Testing

	Die A	**Die B**
Format	Daisy Chain	Daisy Chain
Die size	6mm x 6mm	6mm x 6mm
Bump Pitch	800µm	800µm
Bump Diameter	300µm	300µm
UBM	Ti/Ni/Cu/Au by E-beam	Al IC pad, Ni/Pd/Au by Electroless Plating
Passivation Layer	Polymide	Low Temperature PECVD Si Oxide

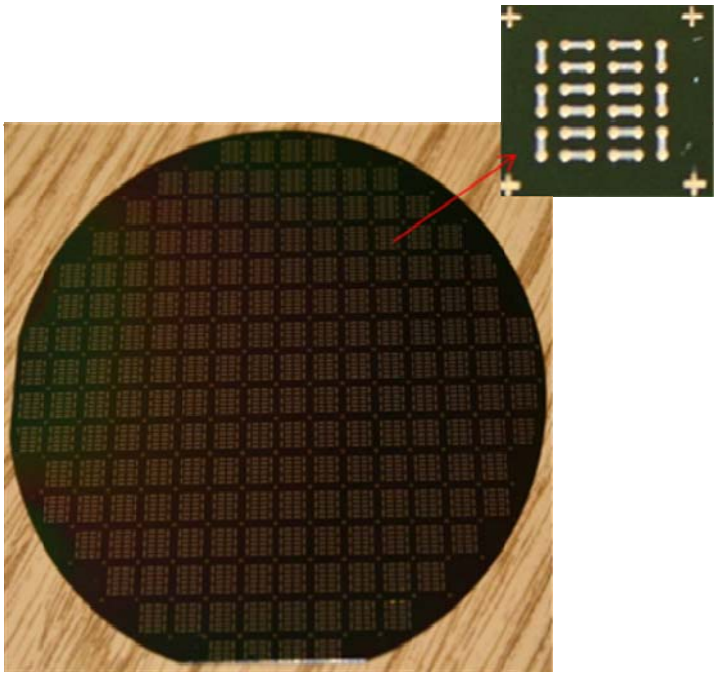


Figure 3.2 Wafer of WLCSPs without SolderBrace coating and WLCSP close-up view

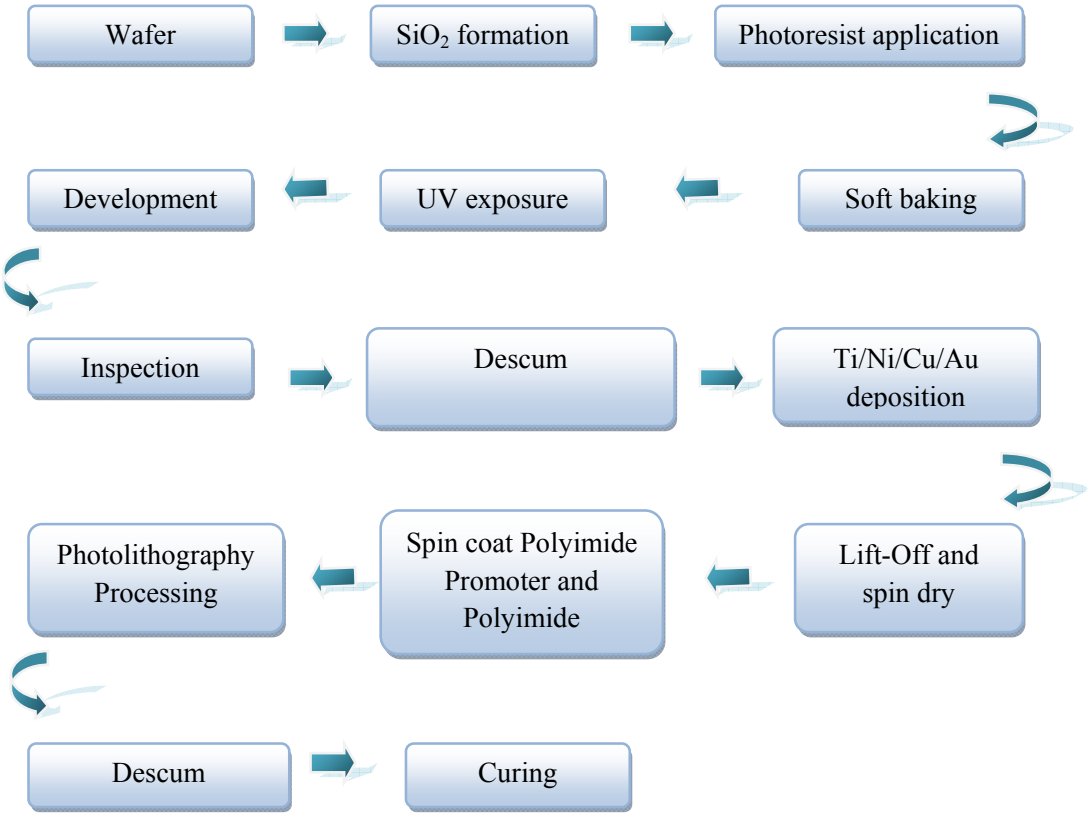


Figure 3.3 Fabrication Process Flow of Die A

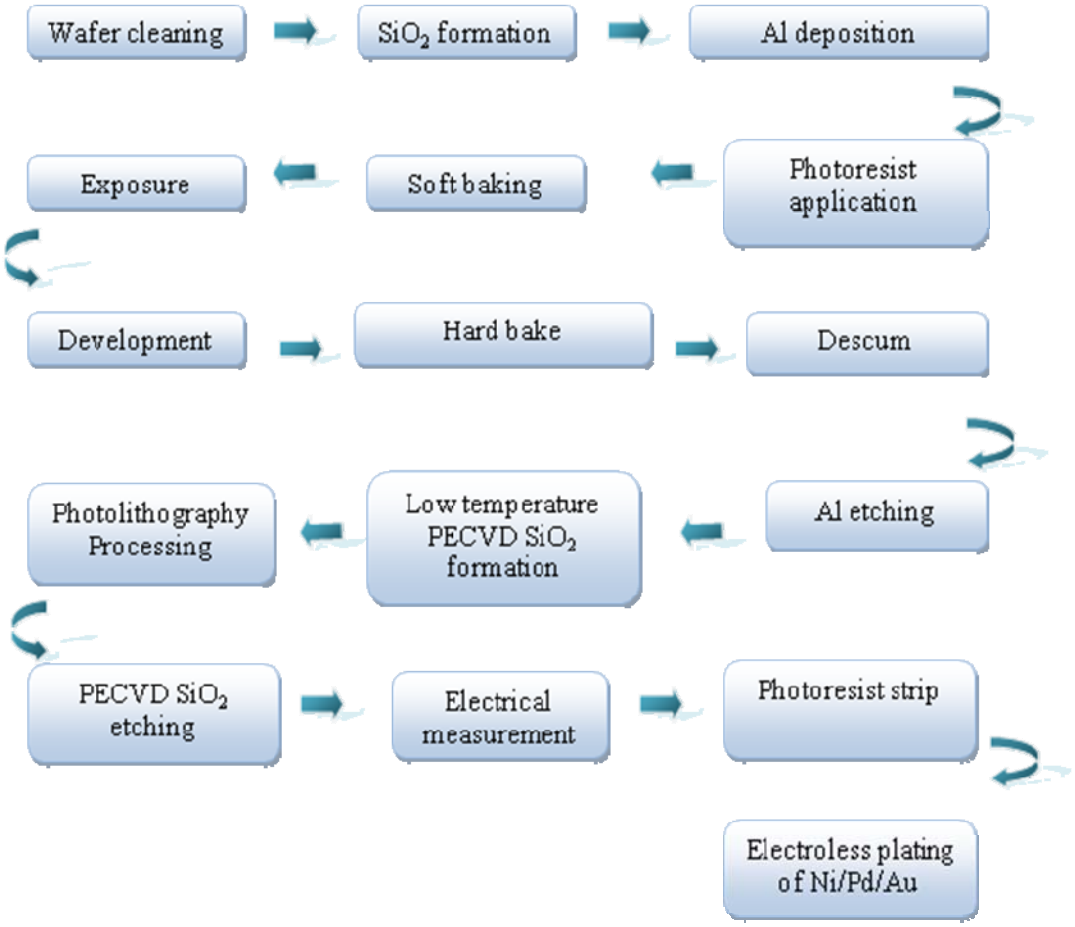


Figure 3.4 Fabrication Process Flow of Die B

The fabrication process flow of die A and die B are illustrated in Figure 3.3 and Figure 3.4. Detail steps are as follows:

1. Wafer cleaning: Prior to use, the 4 inch wafer was first chemically cleaned to remove ionic, organic, or metallic impurities from the silicon surface. Table 3.2 details the cleaning process used in this research. Throughout the wafer cleaning and the microelectronic fabrication process, deionized (DI) water was used as a final rinse.

Table 3.2 Silicon Wafer Cleaning Procedure [59-61]

A. Solvent Removal
   1. Immerse in boiling trichloroethylene(TCE) for 3 min
   2. Immerse in boiling acetone for 3 min
   3. Immerse in boiling methyl alcohol for 3 min
   4. Wash in DI water for 3 min

B. Removal of Residual Organic/Ionic Contamination
   1. Immerse in a (5:1:1) solution of H_2O-NH_4OH-H_2O_2; heat solution to 75-80°C and hold for 10min
   2. Quench the solution under running DI wafer for 1 min
   3. Wash in DI water for 5 min

C. Hydrous Oxide Removal
   1. Immerse in a (1:50) solution of HF-H2O for 15 sec
   2. Wash in running DI water with agitation for 30sec

D. Heavy Metal Clean
   1. Immerse in a (6:1:1) solution of H_2O-NH_4OH-H_2O_2 for 10min at a temperature of 75-80°C
   2. Quench the solution under running DI water for 1 min
   3. Wash in running DI water for 20 min

2. Insulation formation: After wafer cleaning, a layer of silicon dioxide (SiO_2) was formed on the silicon wafer surface acting as an insulation layer. This SiO_2 barrier layer was produced using thermal oxidation. The wafers were thermally oxidized in a furnace at 1000°C under one atmosphere of pure oxygen for 2 hours. The thickness of the oxidation layer was measured to be 6084 Å and the color of the wafer surface was blue green.

3. Photoresist application and soft baking: In order to ensure good photoresist adhesion, the wafer surface was exposed to hexamethyldisilazane (HMDS) for 20 minutes prior to the

spin coating. A layer of light sensitive AZ 5214 positive photoresist from AZ Electronic Materials was coated onto the oxidized surface of the wafer using the spin coating method. The wafer was held on a vacuum chunk, the photoresist was dispensed and the wafer was spun at 3000 rpm for 30 seconds to obtain a 1 μm thick uniform layer. After the photoresist application, the wafer was soft baked at 105^{o}C for 1 minute to remove the solvents from the photoresist coating. For die B, before step 3, a layer of 1μm aluminum metal was deposited by E-beam on the oxidized wafer to form the bump pads.

4. Mask alignment and UV exposure: The mask was aligned with the wafer to transfer the designed pattern onto the wafer surface. Once the mask was accurately aligned, the photoresist was exposed through the pattern on the mask with a high intensity ultraviolet light. 12 seconds continuous exposure time was used for all the wafers.

5. Development: The resist in the patterned area that had been exposed to the ultraviolet light was washed away using a 1:3 AZ 400K developer-to-water solution for 30-35 seconds, leaving other areas still covered with photoresist. The exposed part without the resist was the exact pattern layout on the wafer surface.

6. Post-development inspection: The inspection is to ensure the resist processing steps conducted earlier had produced the desired results. This was done using an optical microscope.

7. Descum process: Descumming is the process to ensure full removal of resist from uncovered areas after development through gentle oxygen plasma cleaning. Oxygen plasma etching is a more controlled process than wet chemical etching, able to remove

any residual photoresist in the exposed area while limiting removal of the unexposed photoresist. 15 seconds descum was used in this study.

8. Under bump metallization (UBM) deposition: WLCSP is a well established IC package technology. In its simplest form, this technology requires a UBM layer deposited and patterned over the passivation openings on a wafer. The UBM protects the initial bond pad from the solder bump metallurgy and provides a wettable bond pad for the subsequent solder ball bumping.

   - For die A, after the descum step the wafer was deposited with 4 layers of metals: titanium, nickel, copper and then gold (Ti/Ni/Cu/Au), using a CHA Industries Mark-50 Electron Beam. These metal seed layers form a general under bump metallization structure for the WLCSPs which include an adhesion layer (Ti), a diffusion barrier layer (Ni), a solderable layer (Cu), and an oxidation barrier layer (Au). After that, the metal coated wafer was cleaned using acetone in an ultrasonic bath, leaving the patterned metal film, which is called "metal lift-off" process.

9. For die B, aluminum etchant (PAE etchant) was utilized to etch the exposed Al not covered by photoresist. The etch time was 26-28 minutes. The whole wafer was then sprayed with acetone to remove the photoresist on the Al pattern. Electroless Ni/Pd/Au Plating was selected as a new UBM structure for die B due to its advantages such as photolithography not required, suitable for Al pad metallization, improvement of the intermetallic layer stability, low UBM process cost compared to electroplating, and improvement of the device life time at temperature cycling tests. Electroless Palladium, deposited as an additive metal layer of a few hundred nanometers on top of the Nickel

layer, is investigated as a potential improvement of intermetallics formation with lead-free solders especially under high temperature conditions. Formation of passivation layer: This layer can serve to greatly reduce the transport of corrosive species to the underlying metal's surface. It also serves as a solder mask to prevent flow of solder along the interconnect traces. For die A, a thin layer of polyimide was used as the dielectric layer. The detail process steps are described as follows:

- Polyimide adhesion promoter application: After the spin dry and dehydration bake, a layer of VN651 Polyimide Promoter was spin coated at 3000 rpm for 30 seconds on the wafer. The bonding of the polyimide promoter to the substrate was achieved during the 1 min soft bake at 120^{o}C as the priming chemistry is activated by temperature.
- HD PI2556 polyimide coating: A layer of 0.7μm polyimide was spin coated at 3500 rpm for 30 seconds, and soft baked at 120^{o}C oven for 5-10 min.
- Photolithographic process: step 3 to step 7 were repeated to form a layer of photoresist which exposed each bump pad. The photoresist as well as the polyimide coated on the bump pads was removed with AZ 400K during developing.
- Acetone was sprayed onto the wafer to strip off the remaining photoresist layer.
- Finally, the whole wafer was placed into a programmable oven to cure the polyimide film. The cure heating cycle converts the polyamic acid to the insoluble imide form and drives out remaining solvents. The curing profile consisted of :
    - Heating from room temperature to 200 ^{o}C, ramp 4 ^{o}C /minute in air
    - Hold time at 200^{o}C for 30 minutes in air

- Heating from 200^{o}C to 300^{o}C, ramp rate 2.5^{o}C /minute in Nitrogen
- Hold time at 300^{o}C for 60 minutes in Nitrogen
- Gradual cooling to room temperature

For die B, about 1μm low temperature PECVD SiO_2 was deposited to form the passivation layer. This layer is much more stable with better adhesion to the wafer surface than polyimide. Due to the facility limitation at AMSTC, the growth of the low temperature PECVD SiO_2 was performed by Straglass. Inc.

- Photolithographic process: step 3 to step 7 were used to form a layer of photoresist pattern exposing each bump pad.
- The PECVD SiO_2 coated on the bump pad was etched away with buffered HF solution.
- The resistance of the Al pad was measured using a 4-point probe station.
- The remaining photoresist was removed with an acetone spray.
- Electroless Ni/Immersion Pd/Immersion Au Plating was selected as the UBM structure due to advantages such as photolithography not required, suitable for Al pad metallization, improvement of the intermetallic layer stability, low UBM process cost compared to electroplating, and improvement of the device life time in temperature cycling tests. Electroless Palladium, deposited as an additive metal layer of a few hundred nanometers on top of the nickel layer, was used to avoid “Black Pad” that can occur with immersion Au in electroless Ni [62].

10. Final cleaning: After the passivation layer deposition, wafers were cleaned with alcohol, DI water, and blown dry for the next assembly steps.
11. Solderball placement, reflow and singulation will be discussed in the following section.

3.3 Preparation of SolderBrace Material

With several years' diligent work on the development of SolderBrace Material as the final WLCSP passivation layer, researchers from LORD have announced that this product is expected to be commercialized in the near future. However, at the initial stage of this research, a large number of test samples (see Table 3.3) having various chemical formulas were investigated, tested, and compared to optimize the SolderBracing process.

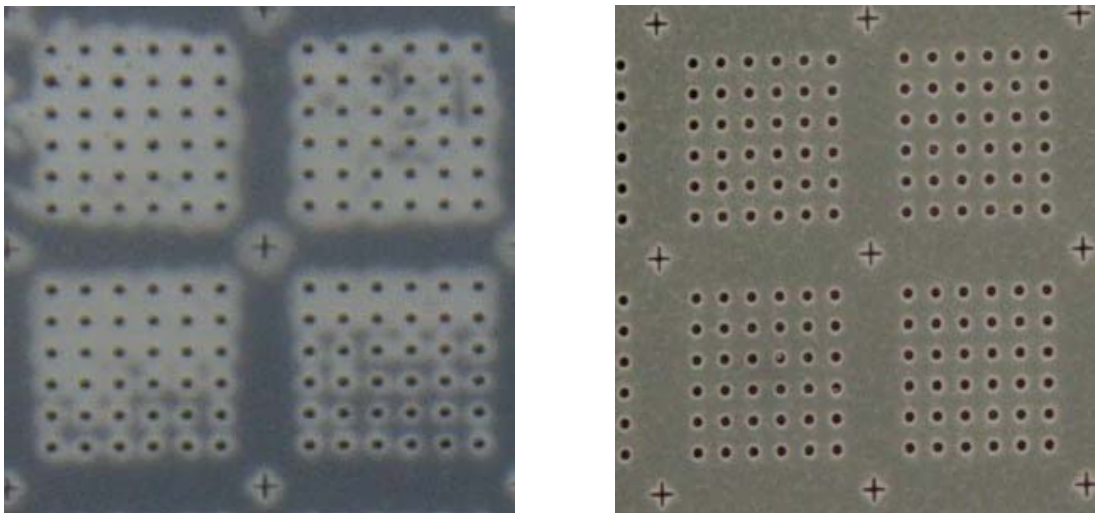
The introduction of silica into the polymer compound plays an important role in reducing the CTE and cure shrinkage. According to published literature, smaller size filler such as nano-silica should be more suitable for the photopolymerization process because it would not scatter the UV light and hinder the photo reaction [63]. However, this type of filler also has some negative effects on the underfill materials due to interfacial interactions and large surface areas, including inhibiting the epoxy cure, reducing the composite glass transition temperature (Tg), low density, high moisture absorption, and high viscosity at high loading level [20, 63]. In this research, particular difficulties were encountered with nano-silica filled samples were in washing the unexposed areas. The nano-silica tended to form a "gel" which was hard to remove after developing. In addition, the CTE of nano-silica was not as low as regular silica. Larger size silica and high silica loading were found to be the preferred choice. Low CTE and low cure shrinkage were achieved with high loadings of silica.

Table 3.3 Test samples with various material formulations

Filler Size	Nano silica	1 μm silica	5 μm silica
Filler Loading (% by weight)	15	30	60
Solvent	Cyclopentanone	Butylacetate	Acetone
Viscosity	low	medium	high
Adhesion	low	medium	high

Cyclopentanone, a colorless liquid organic compound, is usually used in the production of synthetic resins. As one of the most popular and stable solvents for SolderBrace material, it dries slowly giving a nice uniform film after spin coating and soft baking. But drying slowly also means longer drying times prior to UV exposure. Furthermore, cyclopenanone is considered an organic solvent by regulatory agencies around the world, and while it can be used, it is better to use a more environmentally friendly solvent. Acetone, another ordinary chemical, was also selected as a possible solvent. However, it dried too quickly in air to have a stable coating surface. Butylacetate, also known as butyl ethanoate, is capable of forming a uniform and mirror-like surface. But, it requires much a longer curing time to get the surface dry for UV exposure since the coating is much thicker than those formed by cyclopentanone and acetone.

SolderBrace materials with various viscosities and die adhesion characteristics were tested and optimized to achieve dry coating and no delamination after developing. The lower the viscosity, the faster the silica filler settled; the higher the viscosity, the thicker the film without complete drying. Proper viscosity was the starting point to obtain a smooth and dry coating for the rest of the lithography process. Adhesion, on the other hand, plays a crucial role in the final developing step. Figure 3.5 shows delamination caused by poor adhesion between the wafer surface and SolderBrace material.



(a) (b)

Figure 3.5 Delaminated surface coatings (a) and good surface coatings (b)

3.4 SolderBracing Die Fabrication Process

Two wafer level processing methods were introduced and developed to form SolderBrace in this research: Coating-type solder bracing and Maskless printing over solder balled wafer.

3.4.1 Coating Method

The coating method included the process steps of spin coating, pre-bake, UV exposure, and development followed by solder ball placement and reflow as outlined in Figure 3.6. With the exception of solder reflow, all of the steps are "low temperature" wafer level steps, where the maximum processing temperature is 100^{o}C. According to the various SolderBrace material developed at Lord Corporation, a large number of photolithography experiments were investigated and optimized to identify the most stable fabrication parameters. Detail steps to build SolderBrace dies (based on Die A or Die B) are described below. Si and Si dioxide wafers were

used to check the basic spin and photo performance prior to the application on the real metalized wafers.

1. **Cleaning and dehydration bake:** Acetone, methanol, and DI water were in turn used to clean the wafer surface making sure no dust, dirt, or residual photoresist remained. A 20 minutes dehydration baking at 120^{o}C ensured that any H_2O on the surface evaporated.

2. **SolderBrace material application:** A layer of Lord 9809-19 was spun coated onto the wafer with a 1000 rpm/s acceleration rate to a final spin speed of 2000 rpms, held for 30 seconds. The film thickness vs. spin-speed curves plotted in Figure 3.7 provide the information required to select the appropriate spin speed needed to achieve the desired coating thickness (45-50μm).

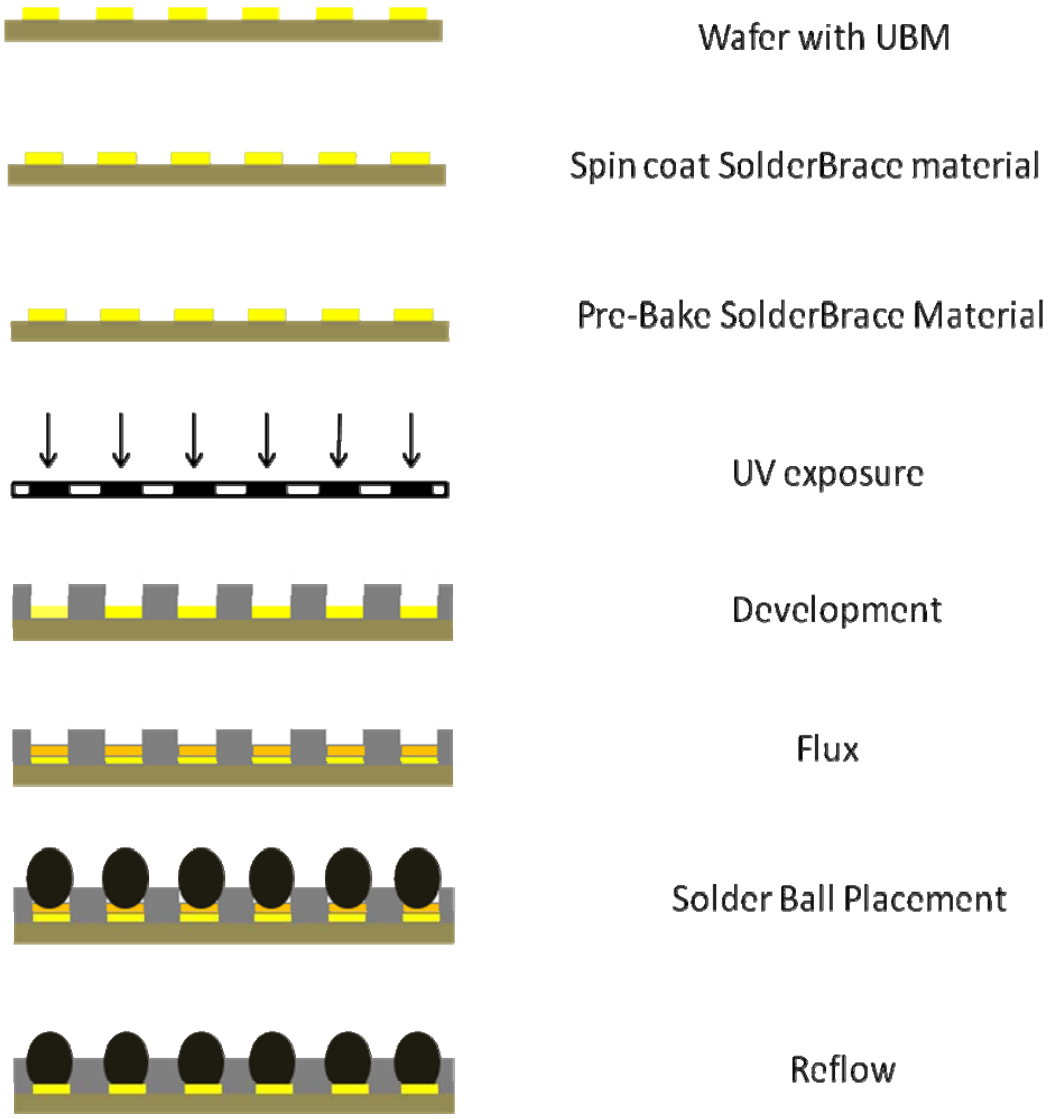


Figure 3.6 Process flow of UV defined SolderBrace bumping sites and ball placement

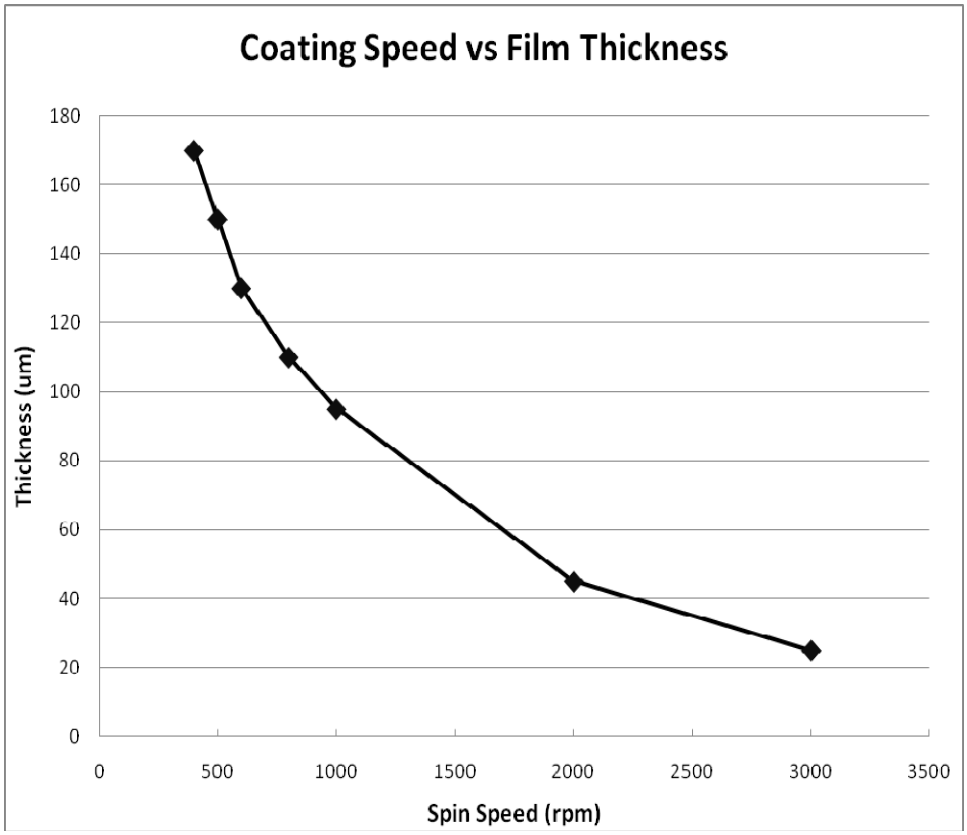


Figure 3.7 SolderBrace film thicknesses as a function of spin speed

3. **Soft baking:** Right after the coating, the wafer was pre-baked at 100°C on a hot plate for 5 minutes to remove all of the solvents from the material. After soft bake completion, the hotplate was turned off and the wafer cooled slowly to room temperature. The softbake time and temperatures were optimized based upon the film thickness and sample stability. Prolonged dry times and higher temperatures decreased the via size and cured the film prior to exposure.

4. **Edge bead removal:** It is a standard requirement for a lithographic process. Without any intervention, the material may accumulate at the edge of the wafer, up to several times

the nominal thickness of the resist near the center due to the dynamics of the spin coating process. In order to achieve better contact between the photomask and the coating layer, it was strongly recommended to remove the edge bead. Edge bead removal is performed immediately after spin coat by directing a stream of acetone near the edge of the wafer while it is spinning. Also, due to the opaqueness of this SolderBrace material, it was necessary to scrape off some of the film along the outer edge of the wafer to expose some features for accurate alignment.

5. **Mask alignment and exposure:** The mask (see Figure 3.8) was aligned to the first layer pattern on the wafer. Once the mask was accurately aligned, the SolderBrace material was exposed through the pattern on the mask with a high intensity ultraviolet light. 25 seconds continuous exposure time was used. If the sample were over exposed, the film would have a very light pink/brown color after the post exposure bake step and the apertures could not be completely developed out or the opening sizes would be very small. If the sample was under exposure, it would cause a delamination problem due to poor adhesion between the wafer and SolderBrace material, or the material residue could flow back into the opening after development. These films were filled with silica, and the light needed to "penetrate" through. Without a sufficiently strong light source, the light would be reflected from the silic and the material underneath would not crosslink. The fact that the resin flowed back suggested that the resin closest to the wafer was not cured. If properly crosslinked, the film was a gel, unable to revert back to a liquid, regardless of solvent or heat. In order to get the small features in the pattern, care had to be taken not to over expose or under expose the material. Figure 3.9 is a depiction of different aperture sizes obtained vs. exposure time.

6. **Post-UV exposure bake:** This step was accomplished at 100^{o}C for 5min on a hotplate to cure and crosslink the material right after the exposure. Without this step, the resin will not cure all the way, which will lead to the bad development result. Since the photo initiator of the SolderBrace material is thermally unstable, the processing conditions are critical. Therefore, a thermocouple was attached to the sample to make sure the hotplate was at the proper temperature. +/- 5 ^{o}C would not change the cure, but a 10-15^{o}C change might, and the drying procedure in particular is sensitive to large changes in temperature. Too hot and the film will have more internal stress and cracks while too cool and the film remains tacky.

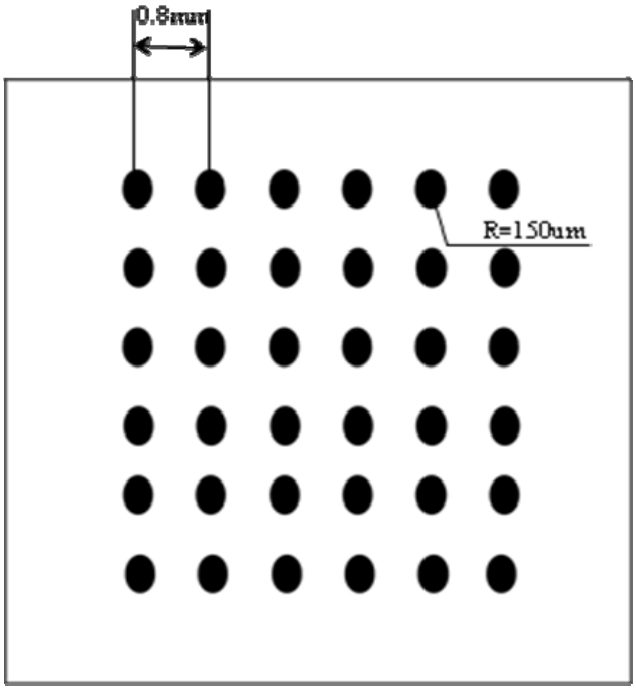


Figure 3.8 Pattern for SolderBrace coating

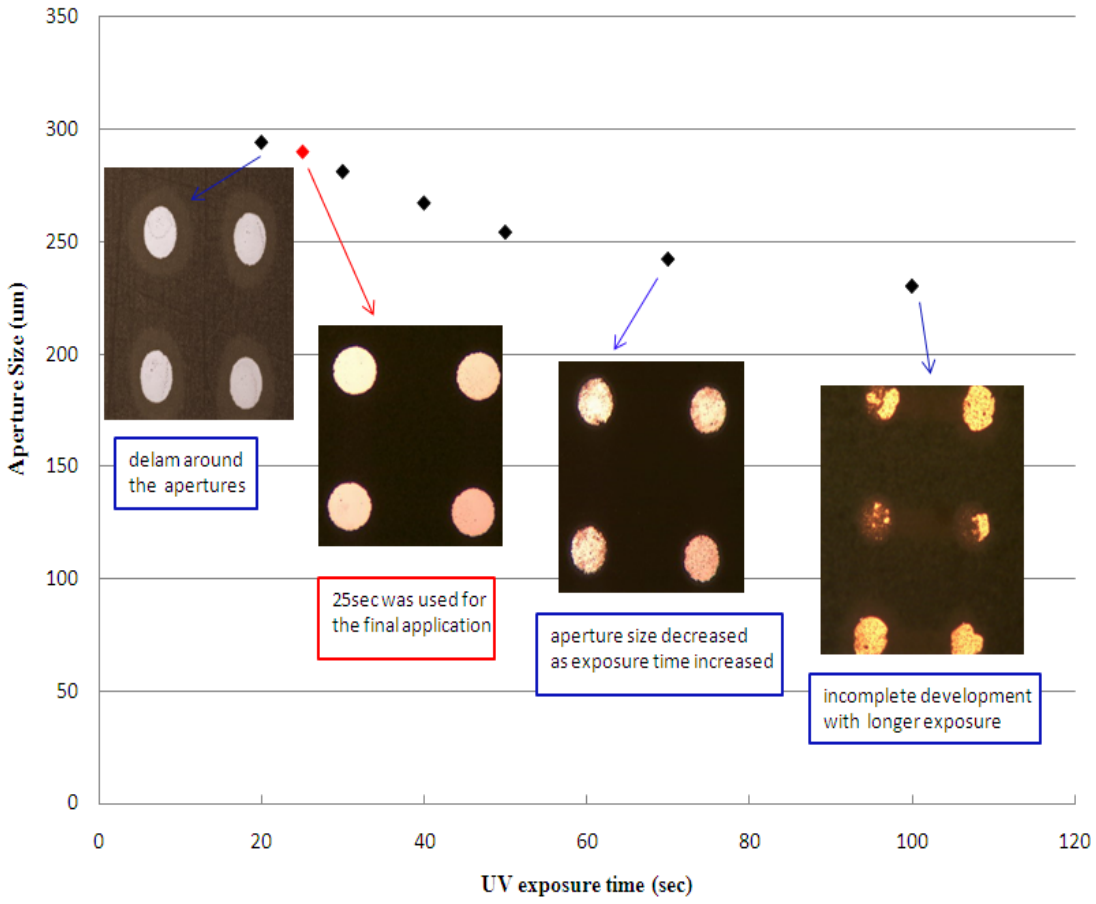


Figure 3.9 Exposure time vs. Aperture Size

7. **Development:** The SolderBrace material in the patterned area that had not been exposed to the UV light was washed away by a three step cleaning process: a). 30sec acetone spray and dry; b). 2-3 min ultrasonic develop in DI(PROPYLENE GLYCOL) METHYL ETHER ACETATE (PGMEA); c). 30sec isopropanol (IPA) rinse and dry. Acetone was very effective in cleaning the residue from the pads and IPA has a higher vapor pressure making drying the film easy.

8. **Pattern characterization:** The substrate was inspected using a microscope to determine the quality of the developed features. A stylus-type profilometer was used to measure the height of the features.
9. **Final baking:** 15 minutes final bake at 100^{o}C oven was very important to adhere and completely cure the material on the wafer. Figure 3.10 is an SEM cross-section picture of the fabricated bumping sites.

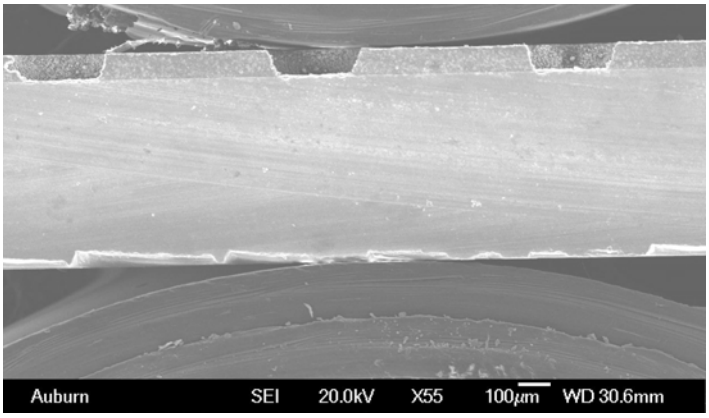


Figure 3.10 Cross-section of the open vias

10. **Fluxing:** The application of flux onto the bond pads.
    - **Flux:** Flux is a chemical cleaning agent that prepares a clean surface for joining and facilitates soldering by removing oxides and other nonmetallic impurities from the soldering surfaces. **Flux selection**: Commercial Kester TSF-6592 and Lord no-flow flux were used in this research for the pre-formed solderball placement. TSF-6592 is a no-clean paste flux designed as a lead fr**ee solution fo**r an array of Lead Free alloys such as SnAgCu, SnCu, SnAg, and SnAgBi. Stencil printing was chosen as the method to transfer the flux onto the wafer. Lord no-flow flux is a new product that

fluxes the solder bumps, forms a nice fillet, and was fully cured during a single reflow exposure (see Figure 3.11, picture from Lord Research group). The assembled packages using this material were expected to achieve high reliability and yield. However, this material had some non-wetting issues when applied on the metalized wafers. In addition, Lord no-flow flux is not a no clean flux. It needs more cleaning steps after the assembly. If the flux is not completely cleaned, it may be trapped in the tight spaces between surface mount components and substrates, leading to reliability problems. Or the flux would become more tenacious as a result of relatively longer times and higher temperatures during reflow, hence is more difficult to clean. Therefore, TSF-6592 was selected as the flux for solderball placement and die placement in this research.

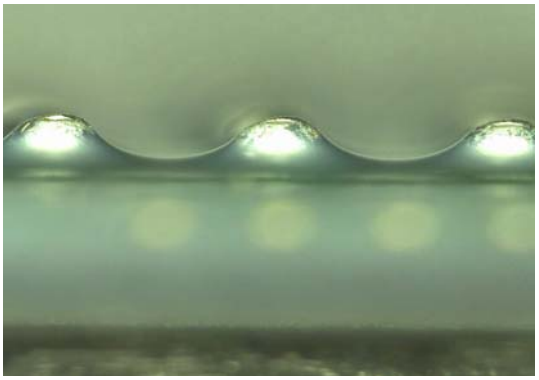
- 

Figure 3.11 Supported structure around solder balls formed by no-flow flux

- **Stencil design:** The volume and bump geometry of the printed material is mainly determined by the stencil thickness and aperture opening size[64]. In this research, an electroformed stencil was chosen for the printing since its aperture wall smoothness

offers the optimum flux release characteristics. The aperture pattern of the stencil was designed to match the pattern on the bumped wafer, the same as Figure 3.8.

- **Printer setup:** The printer parameters must be appropriately defined to achieve consistent prints during stencil printing. The flux must be able to roll evenly across the stencil surface. The driving force plus speed of the squeegee are the main factors that determine the kinematics of this rolling motion. An MPM TF100 Printer with vision system was used for the flux printing process in this research. Parameters optimized for the printer are listed in Table 3.4. Once all the printing parameters were set, the vision alignment system of the printer checked the precise alignment of the stencil aperture openings to the bumping openings on the wafer. This step was required to be carefully handled; otherwise the resulting misalignment could cause the partial wetting or non-wetting issue of the solder ball. After the flux was printed onto the wafer, further inspection under a microscope was needed to eliminate the printing defects.

Table 3.4 Printer Set up and Parameters

Squeegee type	Polymer
Squeegee Hardness	90 dorameter
Angle of squeegee with respect to stencil surface	45 degrees
Down stop force applied on the squeegee	8 lb
Height of stencil above wafer	0 (contact printing)
Printing speed	0.5”/sec

11. **Solder ball placement**

- **Solder alloy selection:** Although tin-lead solder was the most commonly used solder for decades in electronic assembly, the European Union and others have banned the use of lead in electronics for applications due to the adverse effects of lead on human health. Lead poisoning is linked to health hazards such as disorders of the nervous system, impaired pituitary – thyroid endocrine system, and delayed cognitive development [65]. After review by multiple organizations including NCMS, NEMI and SOLDERTEC, Sn–Ag–Cu (SAC) alloys have become the mainstream alloy system used to replace the conventional tin-lead solder in electronic assembly applications [66]. The main benefits of the various SAC alloy systems are their relatively low melting temperatures, solderability and superior mechanical properties [67-68]. Table 3.5 lists some leading lead free candidates that are near eutectic, with acceptable strength, thermal fatigue and wettability properties. Among all of these alloys, SAC305 is gaining wider acceptance for surface mount assemblies, especially for the thermal cycling environments. Good features of this alloy include excellent

fatigue resistance, lower cost SAC alloy, low melting point, best wetting SAC alloy, and excellent solder joint reliability.

In this research, 300μm diameter SAC305 solder spheres from Cookson were used.

Table 3.5 Popular Pb-Free solder Alloys [69]

Indalloy No.	Composition	Solidus (°C)	Liquidus (°C)	U.S. Patent	Comments
241[1]	95.5Sn/3.8Ag/0.7Cu	217	220		Popular SAC alloy for SMT assembly.
246	95.5Sn/4.0Ag/0.5Cu	217	225		Petzow (German) prior art reference makes this alloy patent-free.
252[1]	95.5Sn/3.9Ag/0.6Cu	217	225		NEMI promoted alloy
256[1]	96.5Sn/3.0Ag/0.5Cu	217	220		Reduced silver SAC alloy.
232	93.6Sn/4.7Ag/1.7Cu	217	244	5,527,6283	Original Iowa State Ames Lab SAC alloy.
249	91.8Sn/3.4Ag/4.8Bi	211	213	5,439,6393	Board & component metallizations must be completely Pb-Free.
121	96.5Sn/3.5Ag	221	(eutectic)		Simple binary alloy solder has history of use; marginal wetting.
2442	99.3Sn/0.7Cu	227	(eutectic)		Inexpensive, popular use in wave soldering.

[1] Alloys of choice for general SMT assembly
[2] Alloy of choice for general wave solder assembly
[3] ICA Licensed Patent

- **Solder sphere transfer methods:** Chip-scale packaging is one of the technologies that required rapid increases in the capacity for placing solder spheres onto strips, wafers and substrates [70]. Traditionally, WLCSP bumps have been produced by dropping preformed solder spheres through a metal template onto silicon wafers using modified stencil printers. However, this technology has some limitations for its

widespread use in high yield and high volume applications such as the practical lower limit to the size of sphere that can be dropped, and the yields are statistically low [71]. Over the last 10 years, several methods for the mass transfer of solder balls to wafers have been investigated and developed. Figure 3.12 shows the ball placement method developed by DEK [72]. It utilized screen printing. The process begins with loading the wafer in a conveyorized aluminum pallet. This pallet is then transported into the flux printing machine, which can visually align the wafer with an emulsion mesh fluxing screen. After flux printing onto all bumping pads, the wafer and pallet are transported to the ball placement machine. Following accurate visual alignment with the metal ball placement stencil, the wafer is brought into contact with the underside of the stencil before the ball transfer head traverses the topside of the stencil. This deposits a single solder ball into each of the stencil's apertures. The alignment process accurately ensures that the apertures coincide with the fluxed solder bump pads.

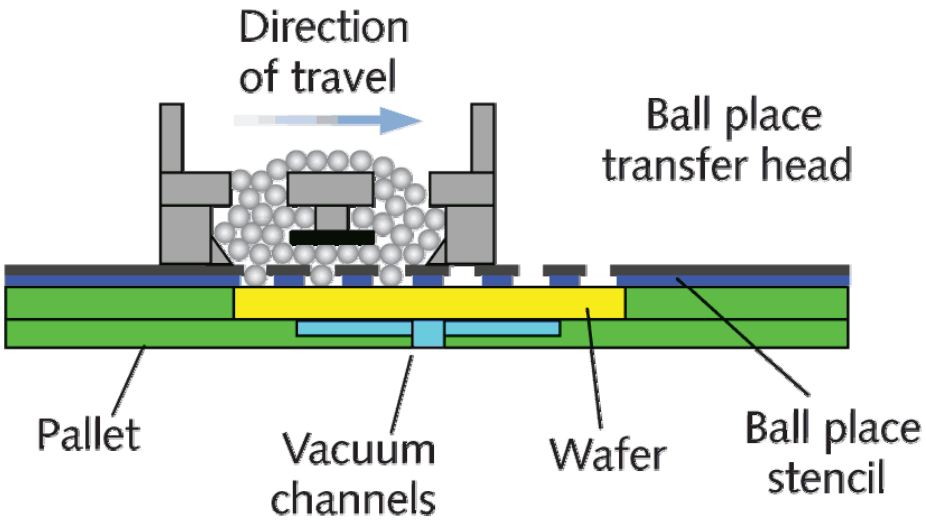


Figure 3.12 Solder Ball Placement Method by DEK [72]

Pac Tech USA also invented a new solder sphere transfer technology that uses patterned vacuum tooling to simultaneously pick up preformed spheres and transfer them over to the wafer [71]. Figure 3.13 outlines the main steps in this solder ball transfer process. First, the vacuum stencil (tooling plate) is lowered into the sphere reservoir. Vacuum is applied to the tooling plate to selectively pick up the spheres. Then the tooling is lowered and aligned to the wafer to bring the solder spheres into contact with the wafer pads. Finally, the vacuum is turned off; the tooling plate is raised; and the solder spheres are reflowed. Since this Solder Ball Transfer equipment has a placement accuracy of $<\pm 10\mu m$, the process can be used for both WLCSP and flip chip applications.

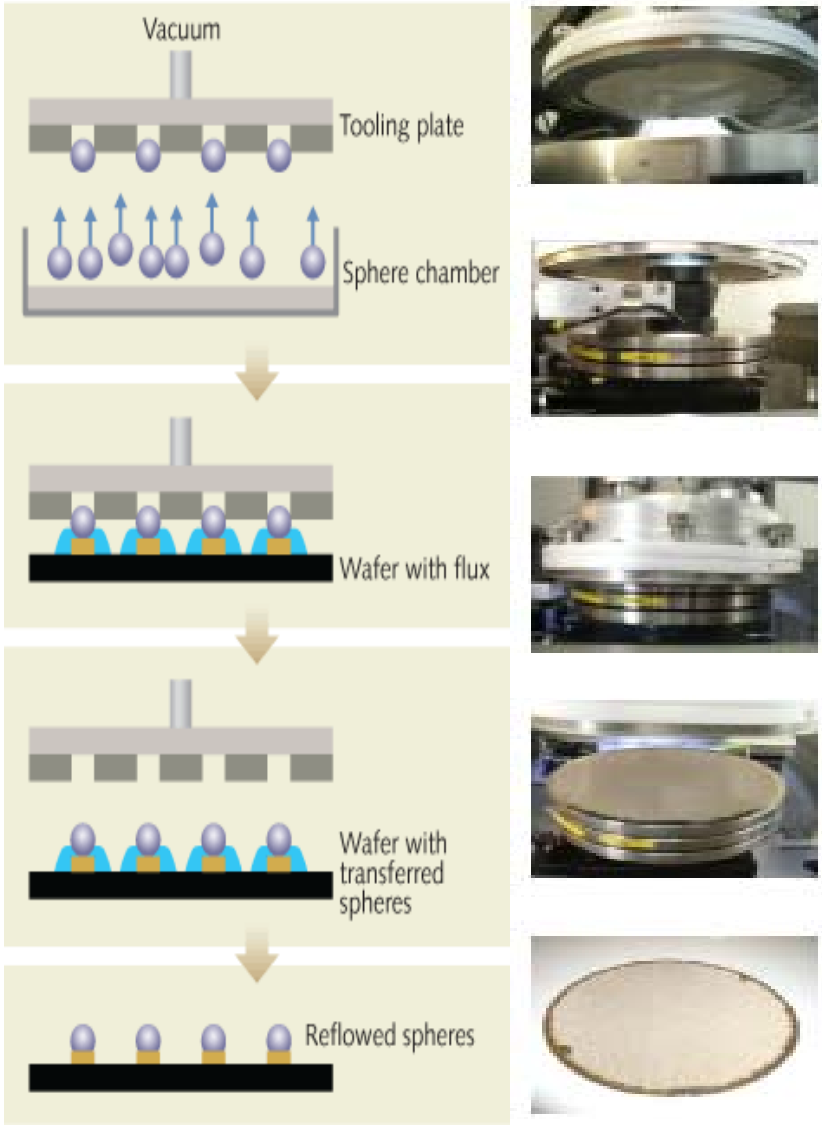


Figure 3.13 Wafer Level Solder Sphere Transfer Process Flow [71].

In this research, a very simple and accurate method was developed to achieve the ball placement process for small volume application. It included the steps of: 1) providing a carrier plate having a series of holes, each hole capable of holding a single solder ball; 2) aligning this plate with the substrate with a microscope; 3) pushing a pattern

of solder balls to the holes on the plate; 4) removing the plate after the solder balls rolled into all the fluxed bumping pads on the substrate; and 5) cleaning the extra balls if needed. The carrier plate was made from a Si wafer. The pattern of the holes was fabricated by standard photolithography process and deep reactive-ion etching (DRIE) (see Figure 3.14). The open size of the holes, 320μm in diameter, was designed a little larger than the solder sphere size to guarantee a smooth placement without stuck solder spheres. Figure 3.15 illustrates the placement steps.

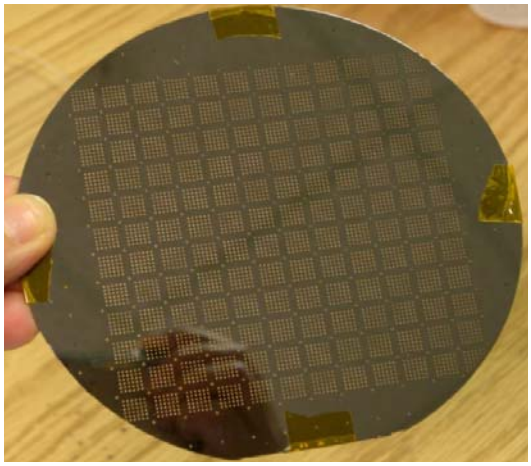


Figure 3.14 Carrier plate made by etched Si wafer.

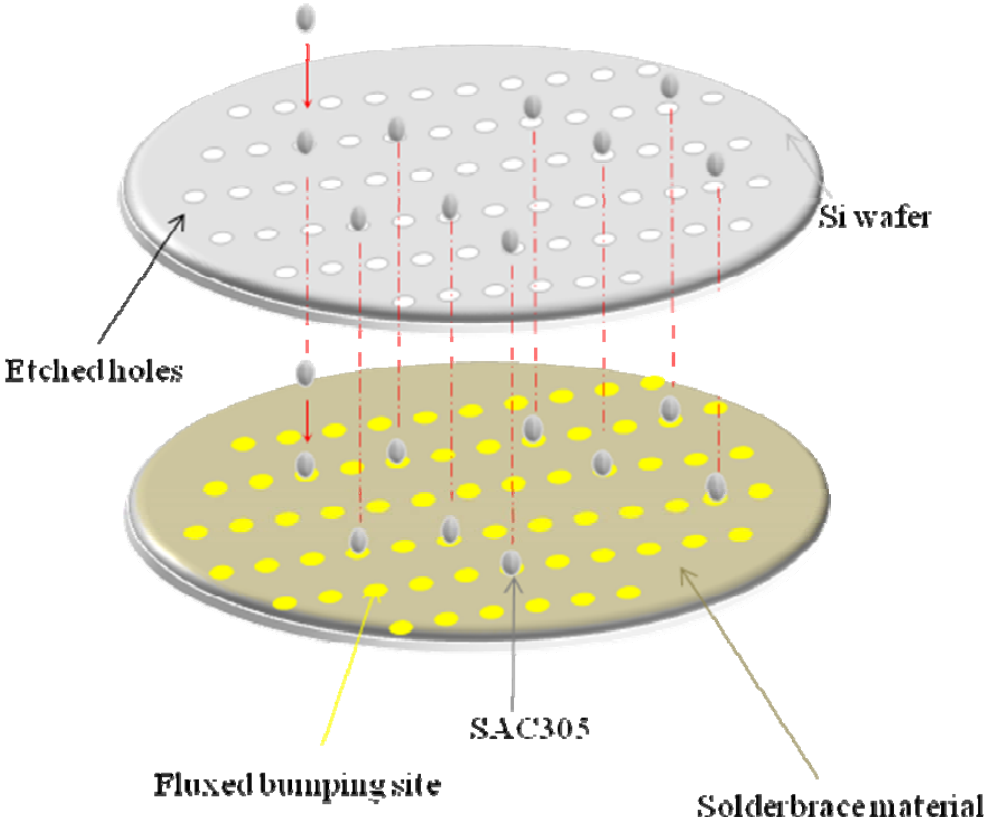


Figure 3.15 Solder ball placement method developed in this research

12. **Reflow soldering**

- **Reflow oven:** Right after the solder ball placement, the wafer was transferred into a reflow oven to melt the solder, heat the adjoining surface, and form a metallurgical bond between the solder and pads. The reflow soldering process can be divided into four phases, called "zones" as shown in Figure 3.16 for lead free alloy. They are: preheat, soak, reflow, and cooling. The preheat zone is introduced to reduce the risk

of thermal shock. If the temperature rate is too fast, the component may be damaged due to the thermal influence such as thermal stress inside the components.

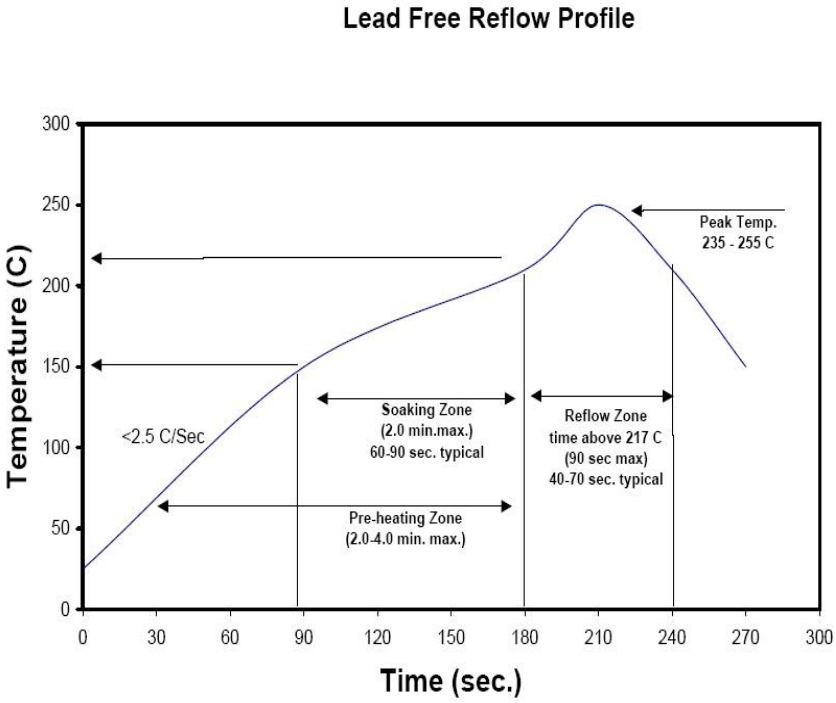


Figure 3.16 Schematic of the four zones of reflow soldering [73]

The soak zone is intended to achieve a uniform thermal distribution before reaching the reflow zone. It is the flux activation zone where the volatiles in flux are further evaporated and the acid is thermally triggered. The flux reacts with the oxides on the surface of the solder spheres and bumping pads. If an oven has many heating zones, a significant number of zones should be dedicated to the soak zone. Once the temperature is above the melting point of the solder, the system enters the reflow zone. With the aid of flux, the solder bumps melt and the molten solders spread onto

the bumping pads. The peak temperature should be high enough for good wetting, but it should not be so high as to cause assembly damage or excessive intermetallic growth, which reduces the solder joint fatigue resistance and makes the solder joint brittle. In the cooling phase the parts should be cooled down as fast as possible in order to acheive small metal grains and hence a higher fatigue resistance of the solder joint. Too slow a cooling ramp will decrease the strength and give the joint a rough surface. In addition, reflow in nitrogen can help to prevent oxidation of the solder ball surface [73-74]. A nitrogen purged Heller 1800 reflow oven with nine heating zones was used for this work.

- **Reflow profile:** The reflow profile is one of the important variables that significantly impacts product yield in the manufacturing process. In soldering, it is a complex set of time-temperature data related with an objected heat up and cool down. It is often measured as temperature values for a variety of process dimensions including slope, soak, time above liquidus, and peak [75]. Figure 3.17 is the reflow profile used in this research to form the solder joint on the wafer that met the requirement provided by the solder sphere vendor.

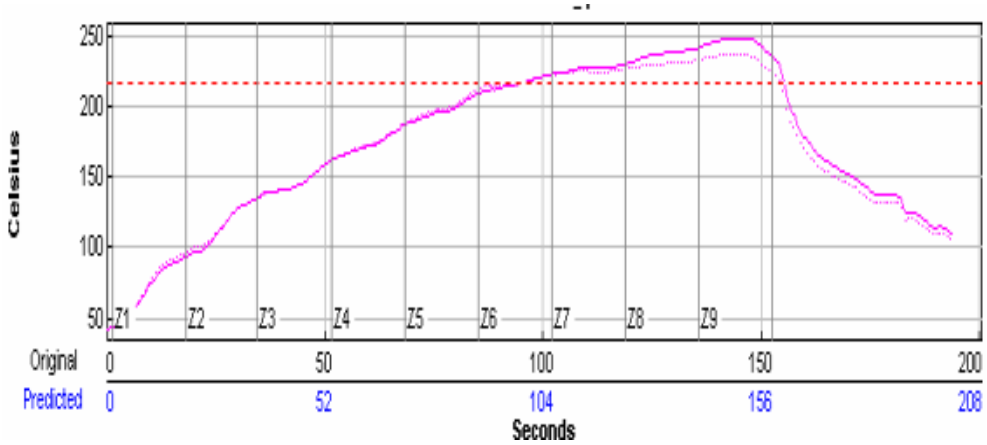
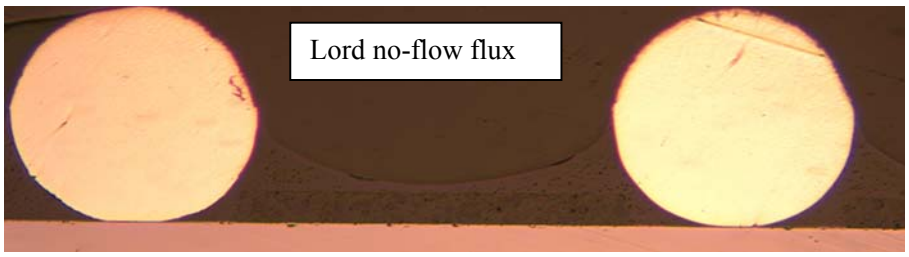


Figure 3.17 SAC305 Reflow profile

- **Solder wetting with different fluxes:** Figure 3.18 shows the solder wettability with TSF-6592 no-clean flux and Lord no-flow flux after thermal reflow. Obviously, the no-clean flux had a very good solder wetting performance while the no-flow flux did not wet the solder onto the bumping sites. To investigate the root cause, different heating methods and bond pad cleaning processes were tried such as hotplate, higher reflow temperature, acid cleaning with various levels, etc. However none of these resolved the problem.

(a)



(b)

Figure 3.18 Solder wettability with different flux after reflow

‘

- **Post reflow cleaning**

The term “no-clean” is really a misnomer because many critical applications do require the flux to be cleaned. Nowadays, one of the most common reasons to remove no-clean fluxes is to increase the adhesion of conformal coatings and underfill materials. Residue of the flux can absorb moisture causing the underfill material to separate from the board by forming a little pocket of stream or gas during the underfill curing. Also, the cleaning is needed to prevent corrosion in PCBs exposed to extreme environments, or simply to improve the cosmetic appearance of the boards [76]. Therefore, a post reflow cleaning process was added to this process by using a 10% concentration of HYDREX DX aqueous cleaner. HYDREX DX is a low-

foaming and high performance cleaner selected to remove a broad range of lead free water soluble and no-clean flux residues from circuit assemblies. Prior to the cleaning process, HYDREX DX solution wash bath was diluted and heated to 60°C~ 74°C on the hotplate. Then the bumped wafer was submerged into the cleanser for 5 minutes and then rinsed with DI wafer. Further inspection with a microscope was required to check the surface cleanness. Figure 3.19 shows the top view of a single SolderBrace coated WLCSP die.

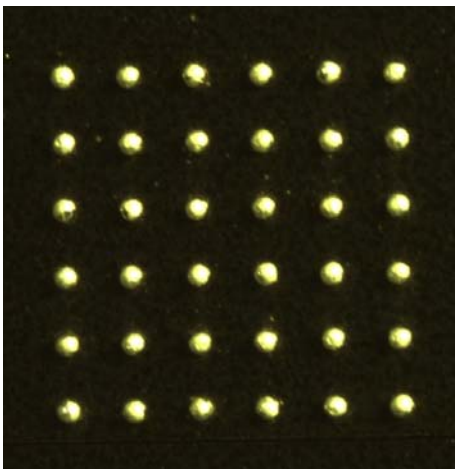


Figure 3.19 A single WLCSP die with coated SolderBrace material

3.4.2 Printing Method

Optionally there is another way to introduce the SolderBrace type material to the WLCSP wafer, called “printing on bumped wafer” as outlined in Figure 3.20.

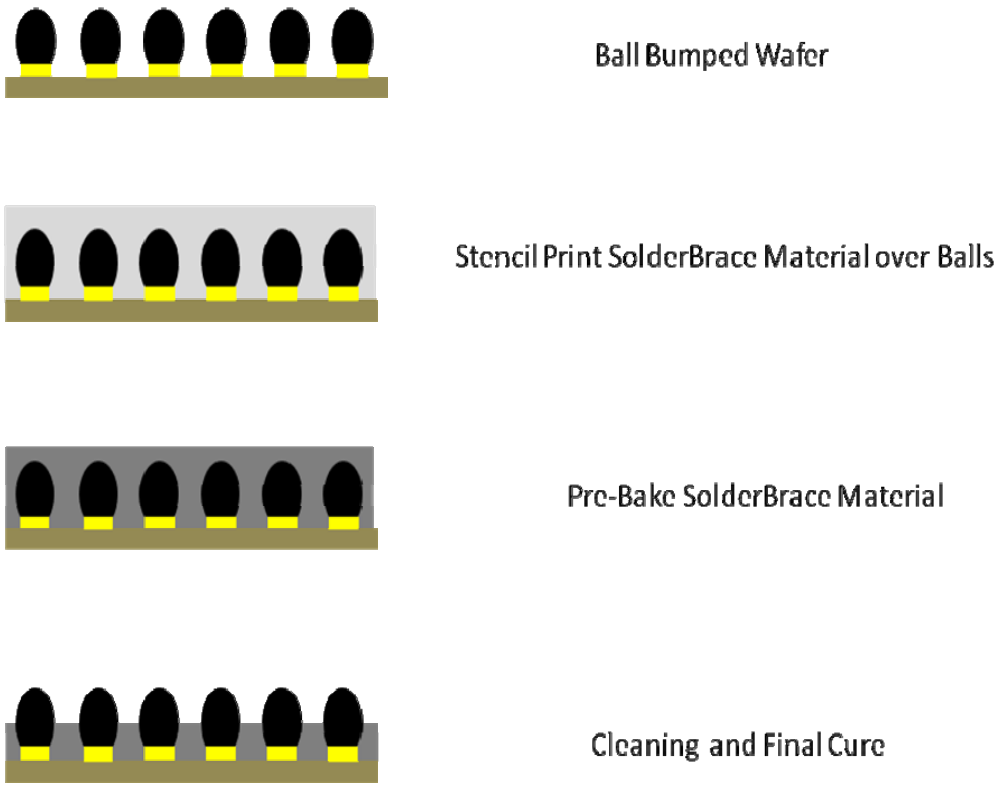


Figure 3.20 Application of SolderBrace Material by maskless printing over balled wafer

This method is theoretically designed to reduce the processing time by eliminating the lithography steps, but practically it is less appealing than the coating method because of the ball height variation, printing consistency, and low yield for high volume WLCSPs. However, significant effort was expended to evaluate this approach. Starting with solder bumped wafers, a layer of SolderBrace material was stencil printed with an MPM TF100 Printer. A 5 minute soft bake at 100^{o}C was still necessary to remove the solvent in the material. Several different cleaning methods were developed to remove the material coated on the top and side of the solder balls such as polish clean, photo-defined clean, and solvent spray clean.

- Polish clean: used the optimized polishing media and grinding condition to gently polish off the material. The polishing approaches and parameters are listed in Table 3.6. The combination of microcloth, alumina suspension, and manual polishing was found to be the best polishing method. However, the polishing uniformity for the whole wafer as well as the limited material removal was a serious challenge and obstacle to prevent its practical implementation (see Figure 3.21).

Table 3.6 Polishing Parameters

Polishing Abrasive	Polishing Suspension	Polishing Method
Tissue Paper	Isopropanol	Vibratory Polishing
Rubber sheet with different hardness	PGMEA	Auto Polishing
Microcloth	Buehler Alumina Polishing Suspension	Manual Polishing

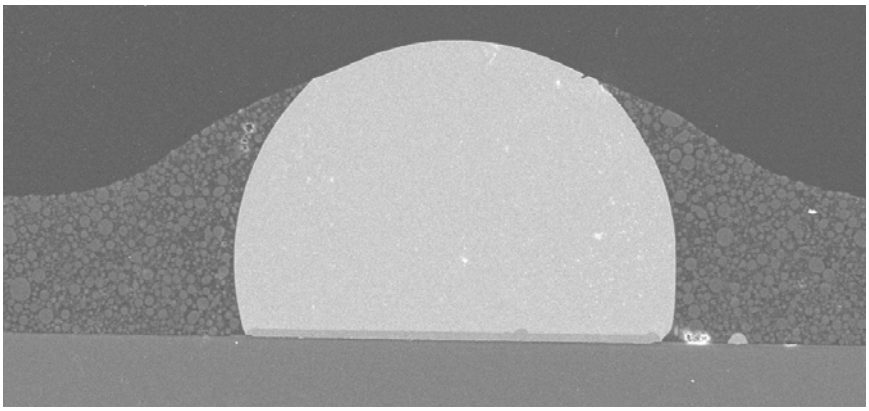


Figure 3.21 SolderBrace Material Cleaning by Polishing Method

- UV-Defined cleaning: This method was similar to the one described in Section 3.4.1, but the SolderBrace material was printed on the bumped wafer instead of spin coating the wafer followed by the solder bumping. Figure 3.22 shows the partially printed 8" wafer that was used to test this method as the start point. Due to the large size of the wafer, it was first diced into small pieces or panels. With the pattern mask, UV exposure and development, the material coated on the top of the solder balls could be removed (see Figure 3.23). However, for an array of dies or the whole wafer of dies, the size of the exposed areas was still not consistant which might be caused by the non-uniform printing over the solder spheres. What is more, silica filler residue was sometimes left on the solder ball after development (see Figure 3.24).

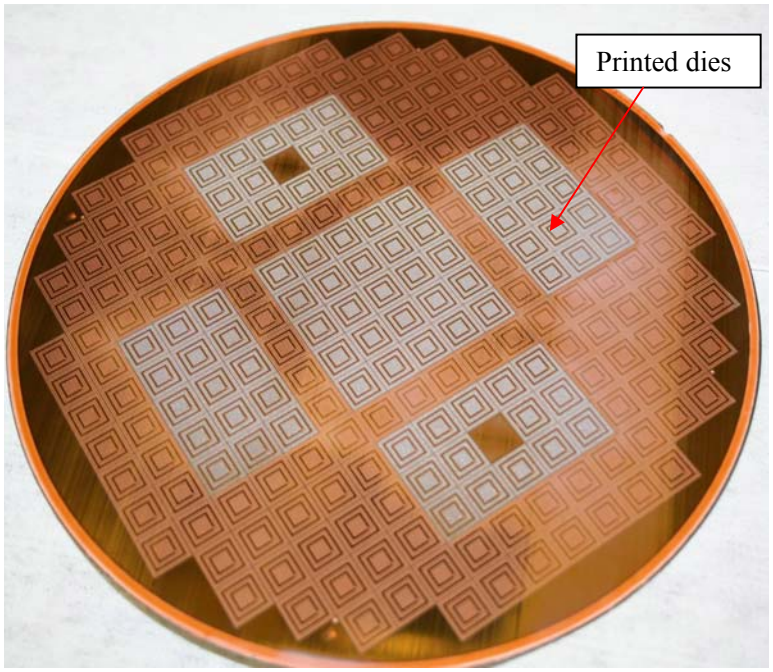


Figure 3.22 SolderBrace printed wafer for the UV-defined cleanning application

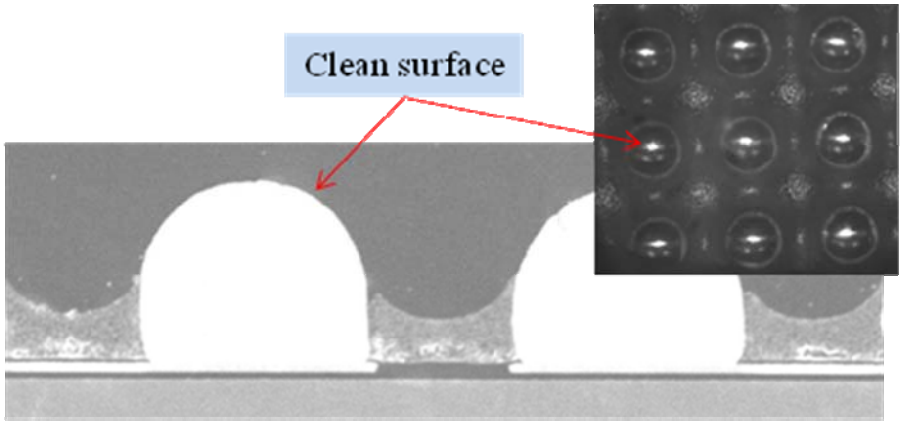


Figure 3.23 SolderBrace Material cleaned by UV-Defined Method

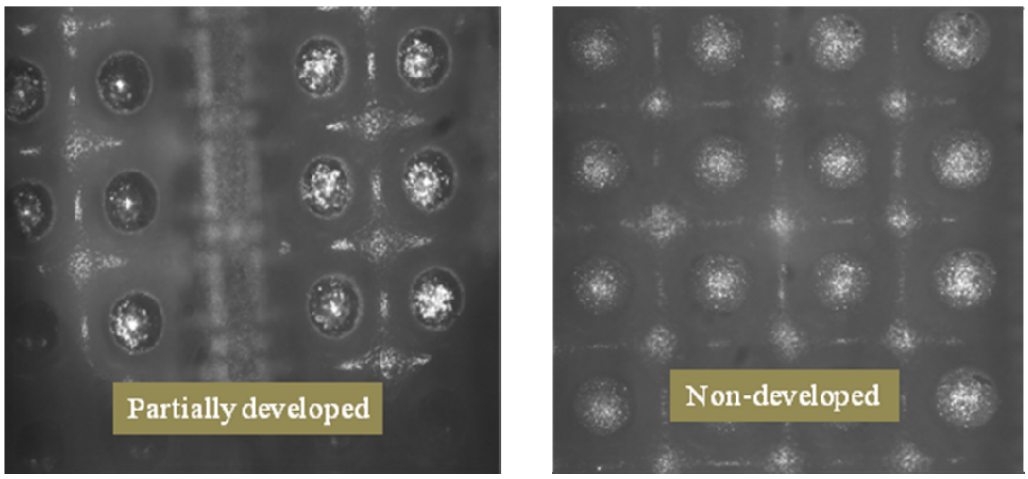


Figure 3.24 Inconsistant development due to non-uniform material priting

- Solvent spray method: The processing sequece is different from the previous two methods. The cure is excuted after the SolderBrace material removal. Figure 3.25 is the cross sections of the die that were printed, sprayed with PGMEA solvent, cured, and reflowed onto boards by Lord's Customer. The coating was over 100μm to begin, but after solvent etching the material (spray for 25s with PGMEA) thickness was ~75μm. The majorty of the ball was clean while the only non-uniformities were from poor printing. It was found that when reflowing the die after the material (see Figure 3.26) was cured, voids formed at the solder junction, which was not good for reliability.

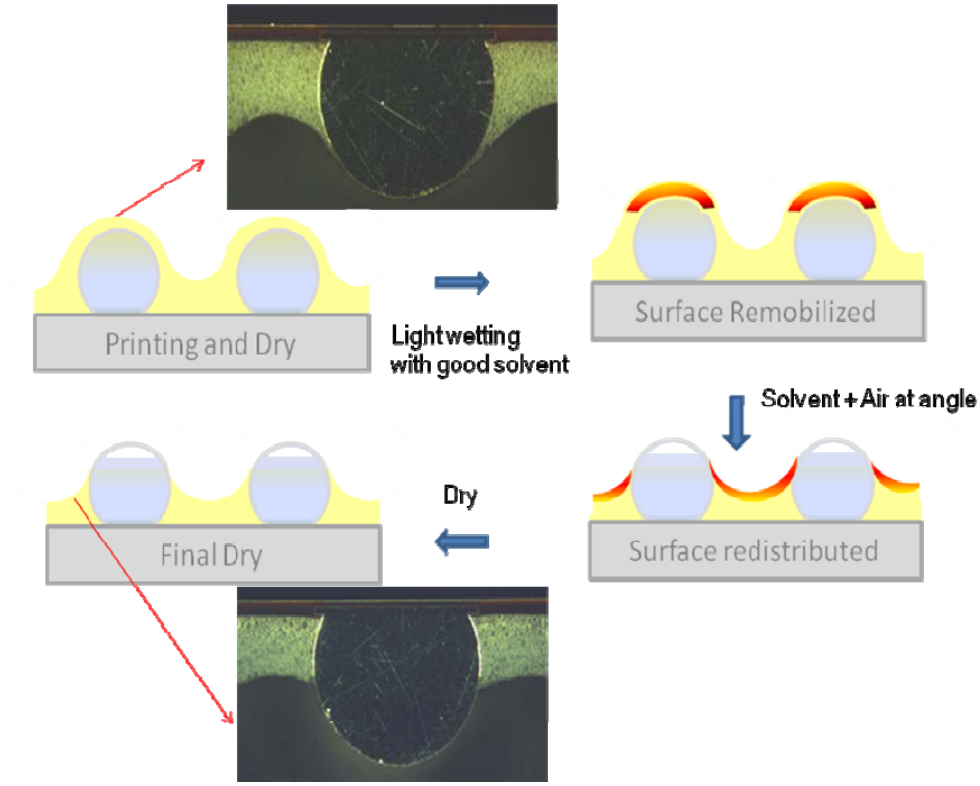


Figure 3.25 SolderBrace Material removal by Srpay

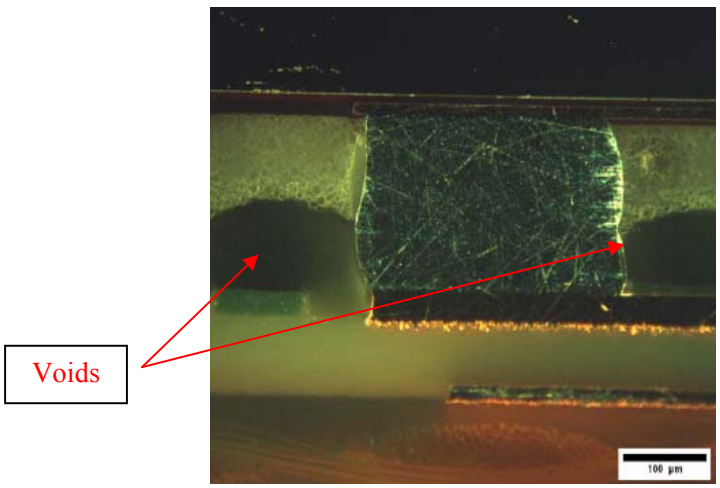


Figure 3.26 Void from flux after assembly

CHAPTER 4

WLCSP PCB ASSEMBLY AND TEST RESULTS

After the fabrication process, the standard dies (controlled dies) and the SolderBracing dies were singulated and assembled to the printed circuit boards. Standard thermal cycling test at -55^{o}C to 125^{o}C was used for the reliability test. Assembly processes including component placement, solder reflow, and inspection are presented in this chapter. The results of failure analysis will also be discussed in detail to provide valuable information for future process and material development.

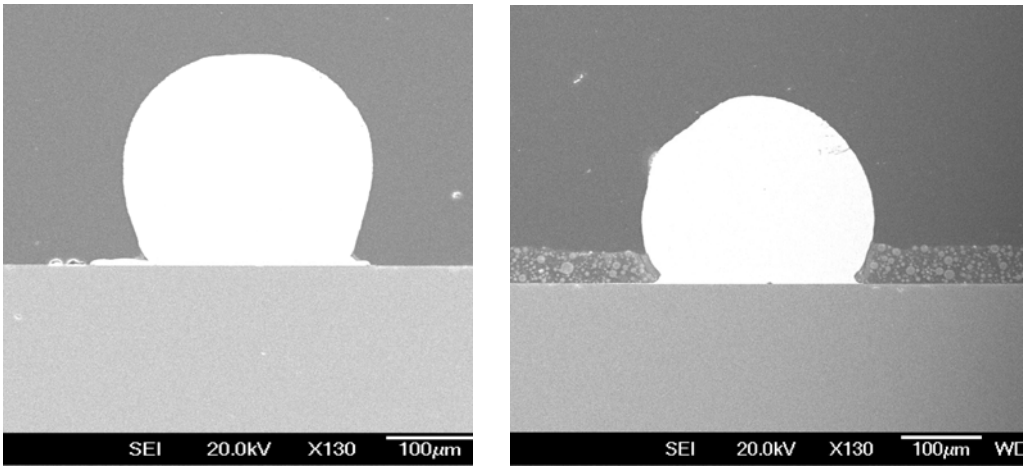
4.1 Wafer Singulation

This is the process to separate the die from the wafer. It can be accomplished by mechanical sawing or by laser cutting. In this application, a Micro Automation 1500 wafer dicing saw was used to singulate the coated wafer into individual dies. The dicing machine used a closed circuit TV system with a split image to align the wafer before cutting. The wafer was mounted on dicing tape that had a sticky backing which held the wafer on a thin metal frame. Due to the effect of the SolderBrace material, which did not reflect the light as well as the silicon did, there were some challenges during this process with accurate alignment. An enhanced light source for each row or column was used to intensify the reflected images of the cutting alignment mark. Manual single cutting rather than auto index cutting was also used to enhance the cutting accuracy. Table 4.1 lists the dicing parameters for the SolderBrace coated wafer. The

cutting speed was set at a low value (80mil/sec) to avoid peeling the SolderBrace material off of the silicon, and to reduce the loading on the blade. All of the singulated dies were cleaned, dried, and then stored in a dry box after dicing, ready for surface mount assembly. The cross section of a standard WLCSP solder ball and a solder ball on a SolderBrace coated WLCSP are shown in Figure 4.1.

Table 4.1 Specifications for wafer dicing

Spindle Speed	2200 rpm
Cutting Speed	80 mil/sec
Film Height	2 mil
Wafer thickness	20 mil



(a) (b)

Figure 4.1 Cross-section of Standard (a) and SolderBrace coated (b) Solder Ball

4.2 WLCSP-PCB Assembly

The goal of this research was to evaluate the reliability performance of WLCSPs with SolderBrace material. The bumped dies (both standard and coated dies) were oriented facedown, accurately aligned to the PCB, flux dipped, placed, and reflowed sequentially as shown in Figure 4.2.

4.2.1 Test Vehicle

The test vehicle as shown in Figure 4.3 was a four layer test board with ten CSP attachment sites on one side and four BGA sites on the other. In this application, only the CSP side of the board was assembled. FR4 laminate was used for board fabrication with no high density interconnect (HDI) or build-up layers. The board dimensions were 2.95" x 7.24" x 0.040", and the pads were 0.012” in diameter, non-solder mask defined. Immersion Sn and immersion Ag finishes were used as the board surface finishes. Two types of test dies were used in the assembly for comparison: standard WLCSP dies passivated with a low temperature PECVD dielectric layer (B-die); and the SolderBrace coated WLCSP B-dies. The PCB’s were pre-baked (125^{o}C for 15 mins) to drive any absorbed moisture out of the PCB to prevent outgassing, warpage and other defects.

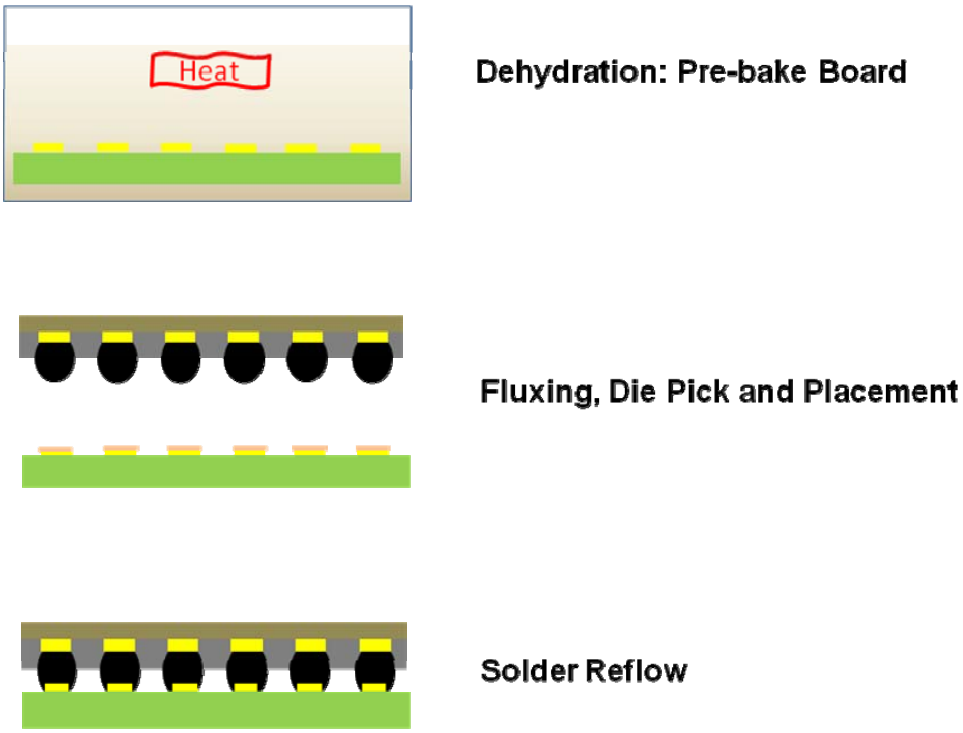


Figure 4.2 Process Flow of Board Assembly

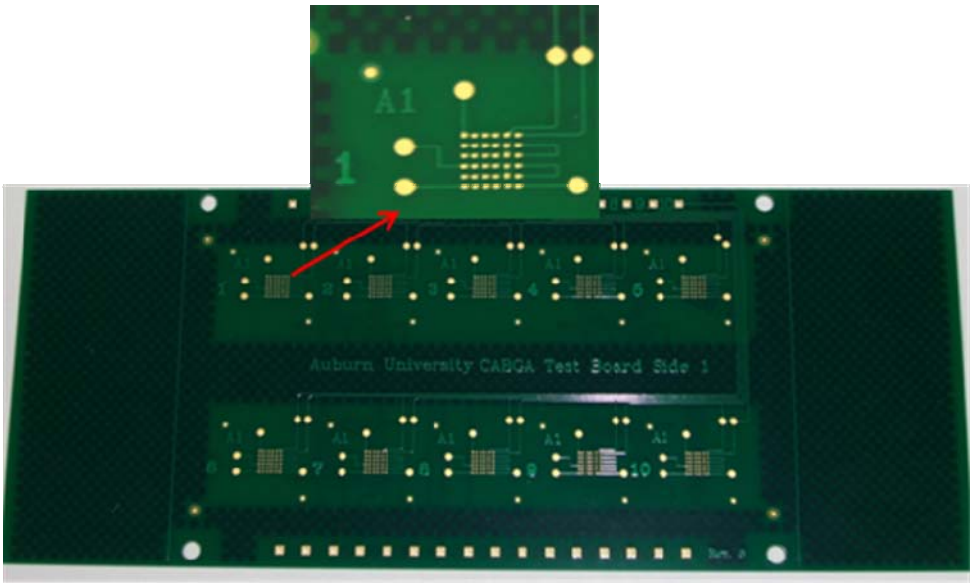


Figure 4.3 The test board with the individual bonding site and its close-up view

4.2.2 Die Placement

Pick-and-place machines are used to place surface mount devices onto printed circuit boards. They are used for high speed, high precision placing of a broad range of electronic components. In general, the die placement cycle is composed of four steps: 1) pattern recognition of the substrate using local or global fiducials; 2) picking of the die; 3) die imaging and theta correction; and 4) die placement. In direct chip attach applications, the dies are sorted prior to the attachment, and presented for placement via either waffle packs or tape & reel. In most cases, flux dispensing and die placement operations are performed on one machine. Approaches to accomplish the fluxing process include: 1) flooding the chip site by dispensing the flux, and then place the chip; and 2) dipping the die into a thin film of flux to coat the solder balls and then placing the chip onto the substrate. There are several key considerations for the die placement such as the placement speed, force of placement, material properties of the flux, die metrics (size,

pitch, and bump diameter), and substrate imaging capabilities. The placement accuracy is dependent on the bump pitch and diameter.

In this study, a Universal GSM Genesis 141 Pick and Place System and flux dipping using Kester TSF-6592 no clean flux (as described in section 3.4.1) was used for the WLCSP die placement.

4.2.3 Reflow

After die placement, the board was immediately transferred into the reflow oven where the solder reflowed and formed the joint between die and substrate (see Figure 4.4). As previously mentioned, the reflow temperature profile is the most important aspect of proper control for the solder reflow process. A profile board with representative component density, thermal mass, and size needs to be used for profile development. Thermocouples are used to measure temperature and are bonded with thermally conductive adhesive or Kapton® tape at desired locations on the board. The thermocouples were connected to a SlimKIC 2000 profiler, which includes software to record the thermal profile when the profile baord travelled through the oven. Due to the higher melting temperature (217^{o}C) of SAC alloy than the SnPb solder (183^{o}C), the peak temperature of lead free assemblies should be controlled between 240°C and 260°C. The soak and reflow temperatures of the SAC alloy need to be higher than the corresponding temperatures in the SnPb profile. Typical reflow parameters recommended by Cookson electronics(the SAC305 solder ball supplier)are listed in Table 4.2. The experimental reflow profile used in this application is plotted in Figure 4.5. The average peak temperature, soak time and reflow time were respectively 252°C, 93sec, and 53sec.

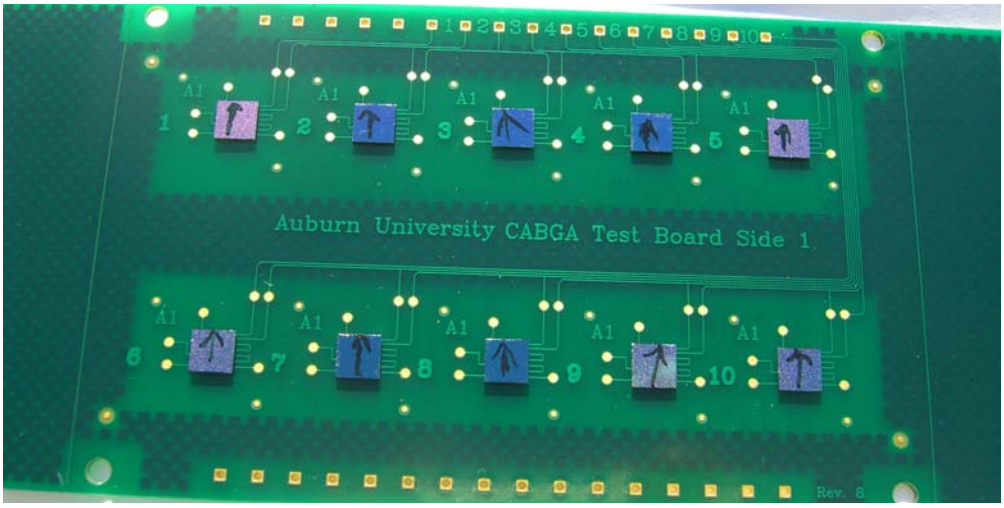


Figure 4.4 Circuit board with attached dies after reflow

Table 4.2 Reflow Profile Parameters

Ramp up rate	1.0~2.0 ^{o}C/ sec to 130^{o}C
Peak temperature	235 ~ 260^{o}C
Preheat time / zone	90~120 sec @ 130~180^{o}C
Time above liquidus temperature	30~60 sec
Ramp down to Room Temperature	3.0~8.0^{o}C

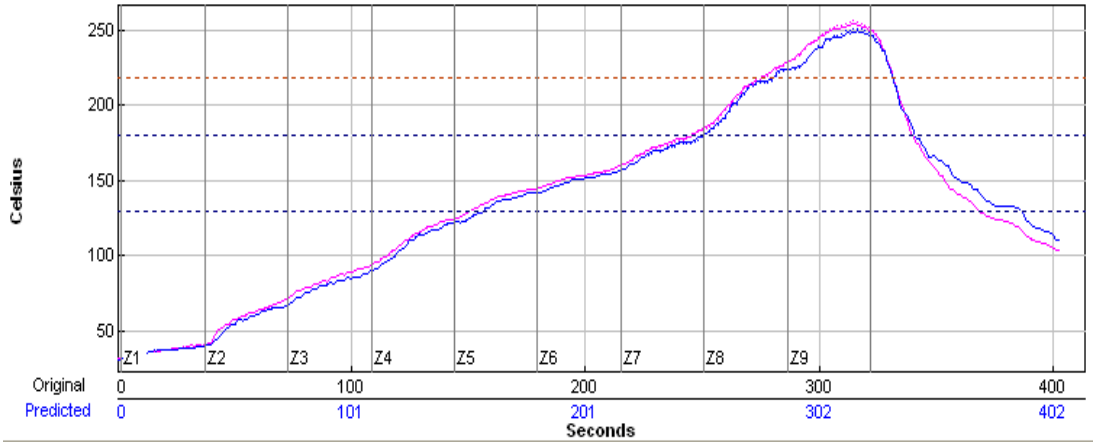


Figure 4.5 Reflow profile for SAC305 WLCSP assembly

4.2.4 X-Ray Inspection

High resolution X-ray technology has been widely used in failure analysis and production quality testing of electronic devices. X-rays are generated from an x-ray source. Some of the X-rays are absorbed by the sample, while most are transmitted through the sample striking the surface of the image intensifier. The image is then digitized and sent to an image processor. The final X-ray image is displayed on the monitor. The X-ray image provides immediate feedback for necessary adjustments to the reflowsprofile, provides alignment information for pre- and post-component placement, and is the final quality inspection. As to the specific solder joint inspection, any quality characteristic and material flaw affecting the shape of solder joints can be detected such as voids, solder bridges, non-wetting defects, and missing solder fillets. A Phoenix X-Ray PCBA Analyzer system was used to monitor the assembly quality at the end of the assembly process in this research [77].

4.3 Reliability Test

Common board level solder joint reliability tests include temperature cycling, thermal shock, temp-humidity-bias, as well as board drop and board bend. Thermal cycling accelerates fatigue failures in solder joints. It determines the ability of assemblies to withstand cyclical exposures in real applications. Since the bulk of real-life solder joint failures are caused by the mismatch between the coefficients of thermal expansion between the component and the substrate, which results in viscoplastic deformation and low cycle fatigue of solder joints, board level thermal cycling has become an industry standard for assessing solder joint reliability.

In this research, the industry standard JEDEC JESD22-A 104 specifications were selected as the thermal cycling condition. The cycle temperature was from -55°C to 125°C, with 15 minutes dwell time at each temperature extreme and a total cycle time of 90 minutes. Figure 4.6 shows the time-temperature profile measured by 4 thermocouples attached onto the board and dies at different locations during cycling. Two test vehicles were subject to the thermal cycling test. One group was assembled with reference WLCSPs (or control WLCSPs) without coating material, while the other group was the SolderBrace coated WLCSPs. Each group contained 34 measurement sites (4 boards).

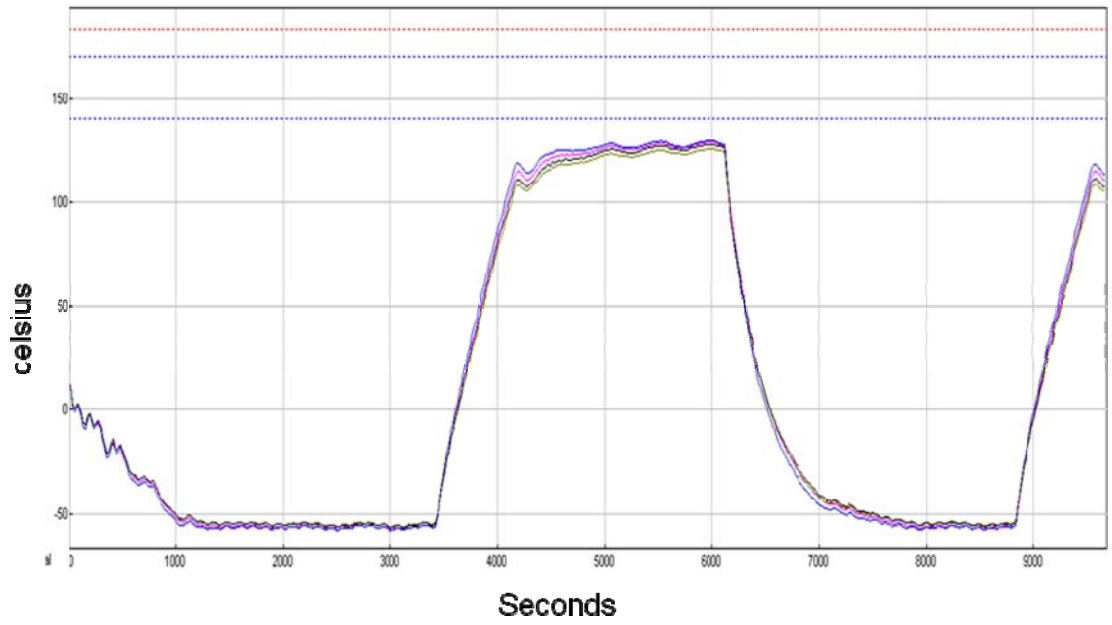


Figure 4.6 Air to air thermal cycling chamber temperature profile

In order to monitor the resistance of each daisy chain of the test WLCSP in-situ during the thermal cycling, each board was wired outside of the Blue-M air thermal cycle chamber to a PC based data acquisition system, which incorporated Keithley Instruments 7002 switch boxes, Kethley Instruments 2001 multimeters, GPIB scanning system and Labview software (see Figure 4.7). The initial resistance of each daisy-chained WLCSP assembly was measured at room temperature before the cycling as the starting point, and the change in resistance was measured and monitored real-time during the thermal cycling until the part failed. A failure was defined as a resistance reading of 100 ohms. The computer monitoring system counted the number of thermal cycles and recorded the cycle count with the failure data. Five failures were measured prior to the recording of the failure in the data file to avoid false failures.

The tests were terminated at 681 cycles when the last assembled SolderBrace WLCSPs failed. Most of the assembled reference dies failed early, within 50 cycles while the last one

failed at cycle 328. Weibull distributions have been widely used to characterize failure distribution and provide modeling for predictions in reliability engineering. After the air-to-air thermal cycling test, Weibull analysis was conducted to characterize the failure data. Figure 4.8 presents the Weibull distribution plot of the thermal cycling test results for the two types of assembly. The horizontal scale is a measure of aging or life while the vertical scale is the cumulative percentage failed. The slope, beta, and the characteristic life, eta, are the two defining parameters of the Weibull line. β is particularly significant and may provide a clue to the physics of the failure, and η is the typical time to failure in Weibull analysis. Table 4.3 summarizes the last failure, characteristic life and the shape parameter for both assemblies. The results show that the SolderBrace coated dies have much higher lifetime than the non-coated dies. The curves of the coated dies are shifted significantly to the right, which indicates their improved reliability.

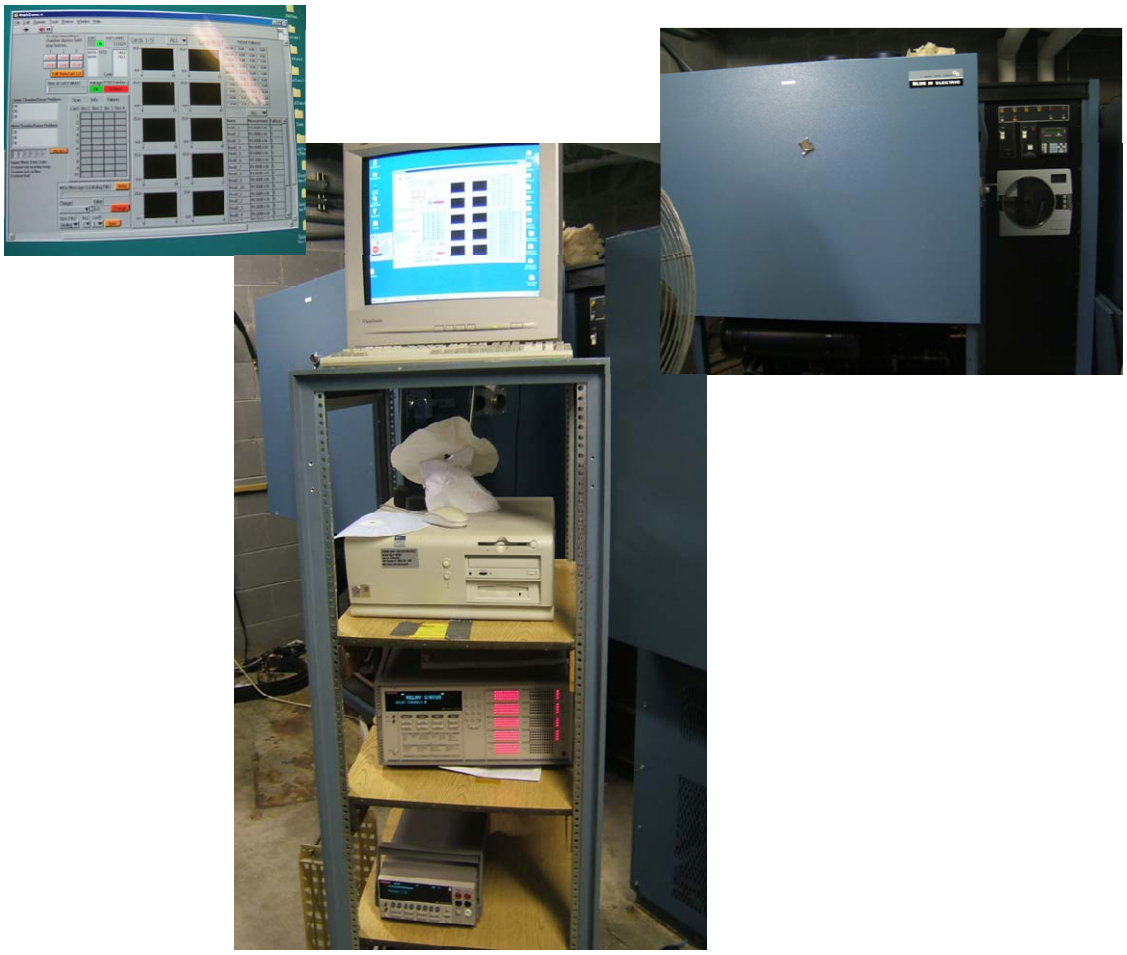


Figure 4.7 Thermal Cycling Setup

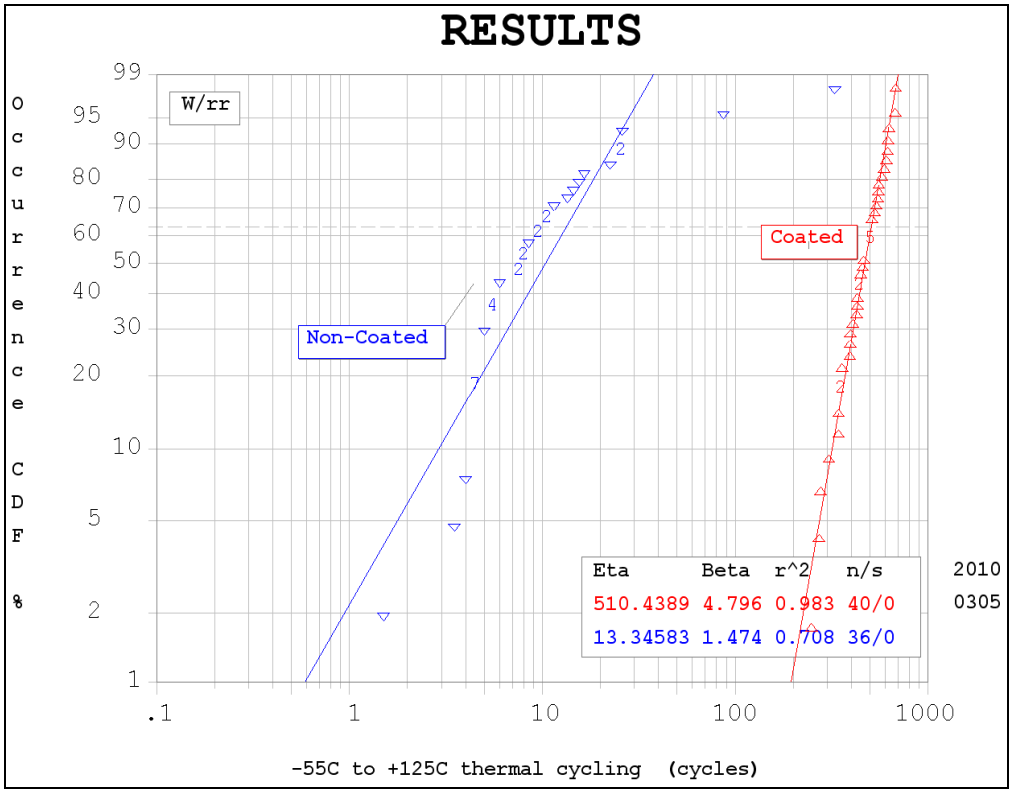


Figure 4.8 Weibull plot of SolderBrace coated WLCSP vs. standard WLCSP at Thermal Cycling Test

Table 4.3 Summary of Thermal Cycling Test Results

Die	Last Failure	Characteristic Life	Shape parameter
Non-Coated	328 cycles	13	1.4
Coated	681 cycles	510	4.7

4.4 Failure Analysis

The main purpose for reliability test was to define the failure mode, determine the location of the failure, and understand the weakness of the package. General failure mechanisms include solder fatigue, inter-metallic (IMC) formation, and Si cratering,. Figure 4.9 shows the failure modes that are known to occur in assemblies subjected to mechanical loading conditions. The distribution of these failure modes depend on several factors such as the package type, the solder metallurgy used, PCB materials, and component-to-PCB-pad size ratio. Usually, multiple failure modes occur concurrently, at different strain and strain rate levels.

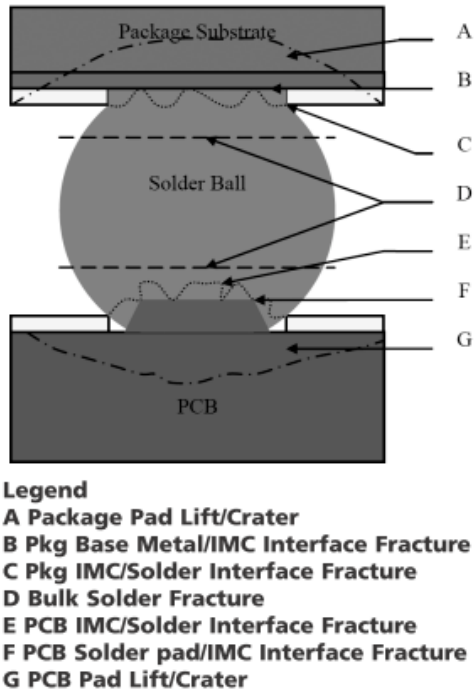


Figure 4.9 Different failure modes in PCB assembly [78]

Failure analysis techniques can be classified with non-destructive analysis and destructive analysis. The non-destructive evaluation will not damage the test sample and uses techniques such as X-ray inspection and C-mode scanning acoustic microscopy (C-SAM). In this research, destructive analysis was performed to determine the solder bump failure mechanism. The test sample was cut from the test board, molded in room temperature cure epoxy resin, and carefully ground and polished to the desired cross sectional interface. The sample was inspected with a microscope periodically during polishing to ensure the proper polishing depth was achieved to reveal the desired cross section. After polishing the surface of the test sample smooth, a scanning electron microscope (SEM) was used to observe and evaluate the micro-structure. Figure 4.10 shows the silicon cratering failure mode of the non-coated dies after thermal cycling test. Silicon cratering is a fracture within the silicon, typically manifesting under the bump. The fracture can be caused by the bumping/WLP process, the assembly process, or the excessive mechanical stresses on the bond pads during thermal cycling. There was no evidence of cratering is as-assembled WLCSPs.

The failure mode for the SolderBrace coated WLCSPs was observed to be the thermal fatigue crack formation and propagation in the solder near the pad surface on the package side of the joint as shown in Figure 4.11. This micrograph clearly shows failure occurred by thermal fatigue crack propagation. The solder bump surface did not deform during thermal cycling.

Finite element analysis was used to investigate the thermal stress induced inside both of the packages. Details are discussed in Chapter 5. The simulation results provide insight into the stress generation and provide guidance on appropriate design changes.

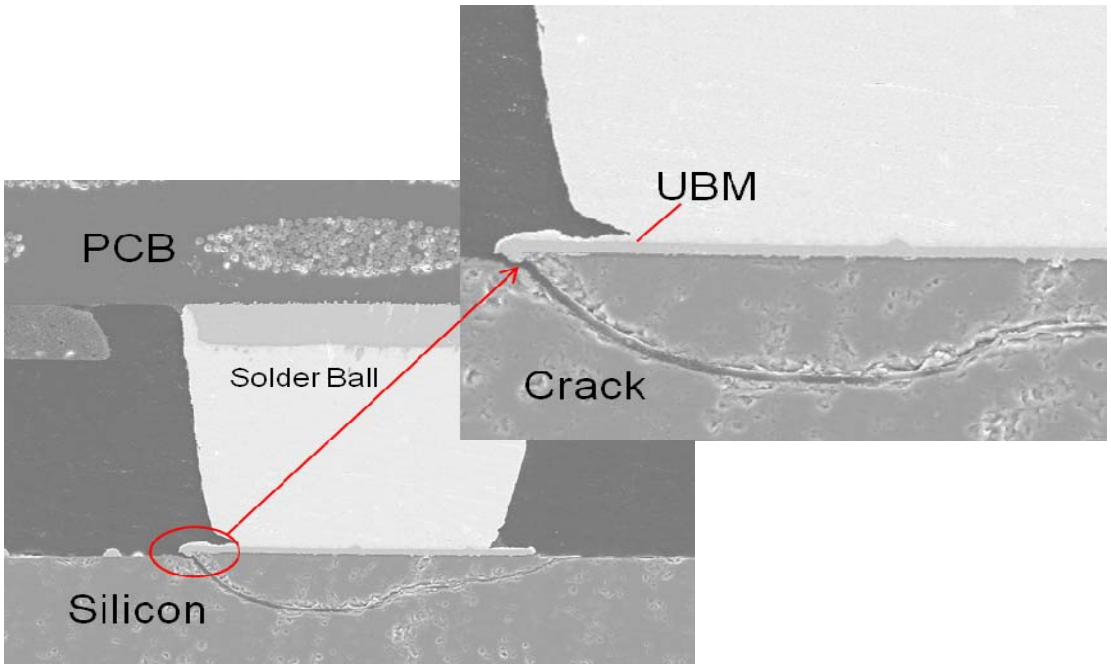


Figure 4.10 Pad cratering failure of non-coated assembled die

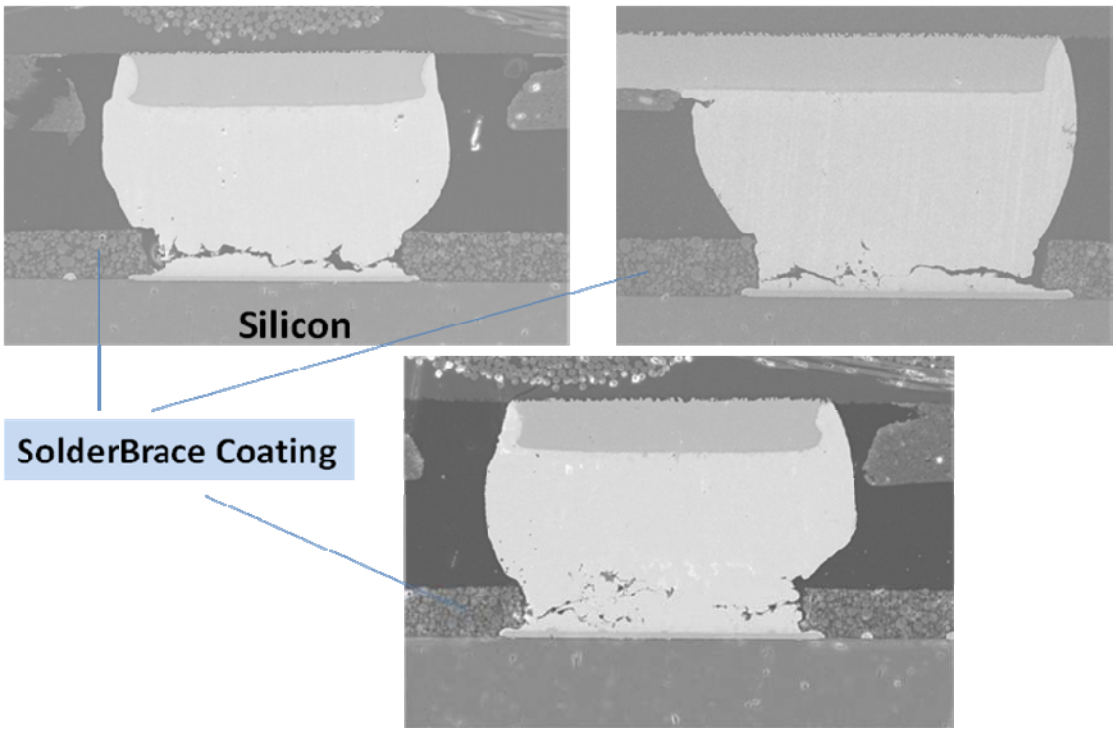


Figure 4.11 Cross Section of SolderBrace coated dies with cracks in the solder near the pad surface

CHAPTER 5

FINITE ELEMENT ANALYSIS

In order to develop a deeper understanding of the solder joint failure mechanism caused by the repeated thermal stress, a finite element based approach for estimating the thermal cycling reliability of chip scale packages is presented in this chapter. ANSYS modeling software was used to model the WLCSP structure to evaluate stress and deformation at various points across the device structure.

5.1 Finite Element Analysis (FEA) models

Finite element analysis (FEA) is a computer based numerical technique for calculating the strength and behavior of engineering structures. It is based on the premise that an approximate solution to any complex engineering problem can be reached by subdividing the problem into smaller and manageable elements. The behavior of each individual element can be described with a set of equations. These equations will finally join into an extremely large set of equations that has the behavior of the whole structure. [79]. This technique has being widely used as a convenient and powerful tool for approximation of the solution to many engineering problems in disciplines such as electronics, biomedical, aerospace, chemicals, geotechnical, and manufacturing. In addition to the analysis in classical static structural problems, FEA is also used for such diverse areas as heat transfer, dynamics, mass transport, and stability problems.

In the field of microelectronic packaging, solder joint reliability is increasingly becoming the main concern with the extremely small electronic package sizes and large numbers of connections. Accelerated temperature cycling is one of the commonly used methods as part of the package qualification process. Due to the temperature fluctuations caused by environmental changes or power dissipation, the thermal expansion mismatch between different package materials can result in the temperature and time dependent creep deformation of solder, which will accumulate damage in the solder joint failure along fatigue from the repeated cycling. Performing the experimental reliability tests is one of the methods to aid in design and to develop a deeper understanding of the failure mechanism, however it is usually costly and time consuming. In order to maximize the reliability performance, minimize the development costs, and also predict the fatigue life time of a solder joint, advanced analysis is a necessity during the design and development phase of a microelectronic package [80-81]. A validated finite element model is therefore becoming a powerful tool to help better analyze the various effects, and a more practical route for obtaining strain-stress relationships and their local distributions within the package. There are various steps involved in the finite element method [82]:

1. Specify the geometry of the structure that is to be analyzed.
2. Define the element type and material properties such as Young's modulus, the Poisson's ratio, CTE, and viscoplasticity.
3. Mesh/divide the structure into small elements.
4. Specify and apply boundary conditions and external loads
5. Generate a solution based on the previously input parameters.
6. Refine the mesh to achieve more accurate results.
7. Interpret the simulation results.

5.1.1 Modeling Approaches

Due to the variations in material properties, modeling assumptions and inconsistencies in the FE modeling process itself, analyzing the complete assembly generally takes significant time and sometimes may be beyond the computing capability. Therefore, insuring 100% simulation accuracy in a solder joint fatigue model is a difficult task. However, the accuracy still needs to be guaranteed such that it can provide a positive impact on the designed package performance [83]. In addition to the application of 2-dimensional finite element model, 3-dimensional modeling has been widely used in the industry for solder joint life prediction as it physically describes the structure and therefore improves the accuracy over 2D modeling. These common 3D modeling approaches can be grouped as Global modeling, Sub-structure modeling, Sub-modeling, and Slice modeling [84].

1. Global modeling

The global modeling approach is widely used to capture the local solder joint behavior. All of the materials and their respective non-linearities are included in the simulation analysis. The objective is to use a very detailed model of the critical joint while transmitting the correct load vector and assembly stiffness from the rest of the structure to this model. As shown in Figure 5.1, the global model uses a relatively coarse mesh for all of the components except for the critical solder joints. However, it is still time consuming to obtain accurate analysis results because the fine mesh of the critical solder joints must match to the coarse mesh of the remaining solder joints.

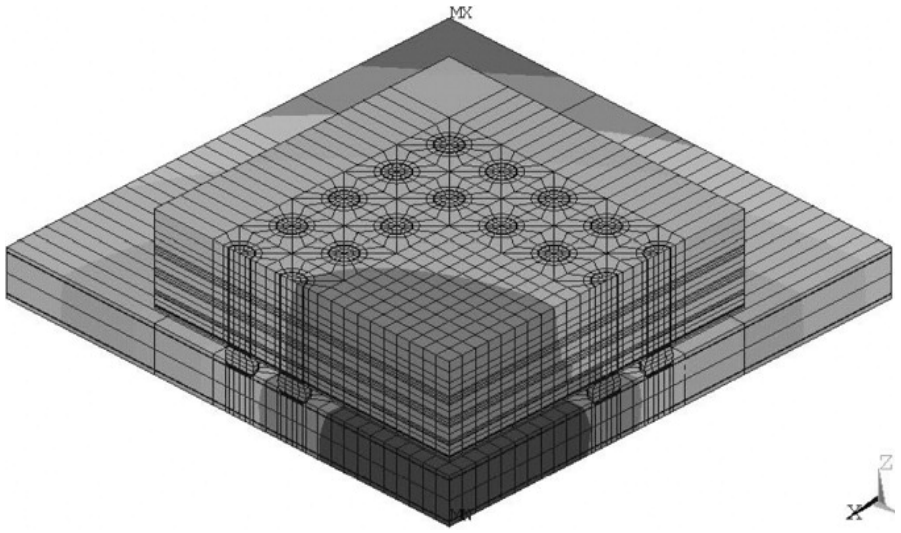


Figure 5.1 Global modeling with highly refined mesh for the solder joint [85]

2. Sub-structuring and Submodeling

The sub-structuring approach is a procedure that condenses a selection of global model material elements into a sub-structure, which is called a super-element. The unit load of this sub-structure is obtained by analyzing the global model over 1 degree rise or fall of temperature for temperature cycling or unit displacement for bend cycle. Using appropriate scaling factors, the super-element can be repeatedly used for multiple bend or temperature cycle conditions [84]. Application of sub-structuring in solder joint reliability models has been discussed in previous publications by Sycd [87]. The limitation of using this method is that materials having non-linear, temperature dependent behavior cannot be used as the super-element.

The sub-modeling approach is the reduction of the entire global model to a single critical solder joint along with its rest of the package. The boundary displacements extracted from the global model for the critical solder joint are applied to a highly refined local solder joint model [88]. Refinements of the mesh in the submodel and the coarse mesh in the octant global model

are shown in Figure 5.2. However, this technique has slower computation speeds than the sub-structuring approach. For example, with the same computation time, sub-structure model can produce the results for four solder joints , while sub-modeling approach can only produce results for a single joint.

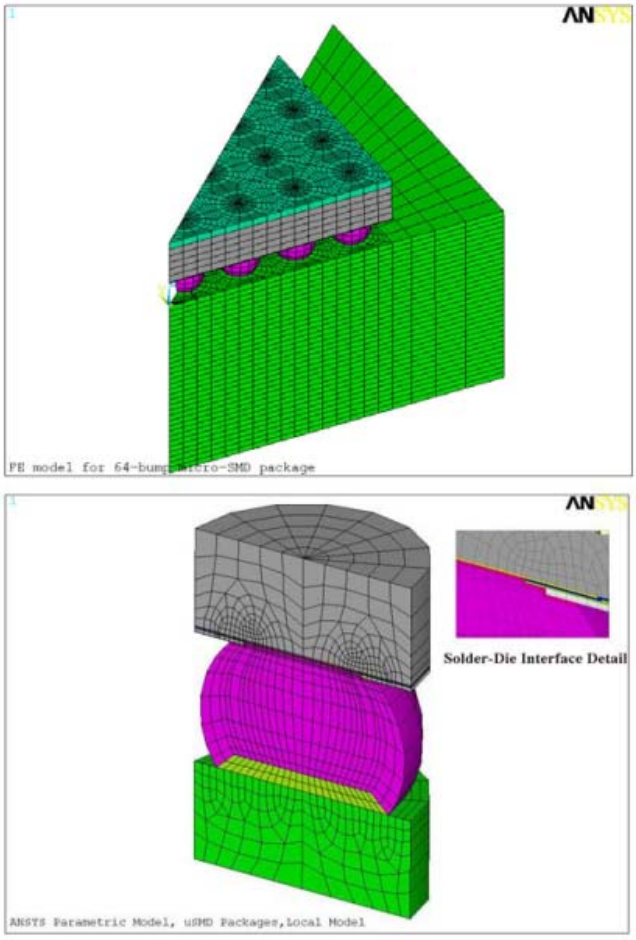


Figure 5.2 Global model with a submodel [89]

3. Slice Modeling

This approach utilizes only a diagonal slice of the assembly in order to reduce computation time and model complexity. It is usually applicable to packages having octant symmetry structures. The slice passes through the thickness of the assembly, and captures a full set of solder joints as well as all major components. The model imposes symmetry boundary conditions on one surface of the slice. On the other cut surface, a state of general plane strain is imposed. Therefore, the slice model actually simulates a package that is infinitely long in the direction perpendicular to the plane of the slice. However, this may cause an underestimation of the warpage of the package during the temperature cycling, and thus results in under prediction of the thermal cycle life [90]. Figure 5.3 shows a slice model that includes the package, solder balls and PCB materials.

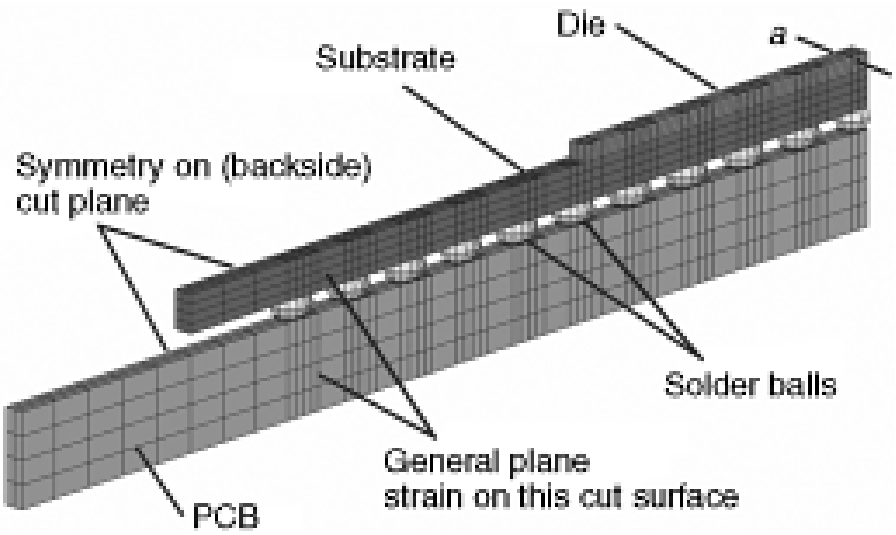


Figure 5.3 Slice model [88]

5.1.2 Material Properties

Many packaging materials have temperature and time dependent behavior, which is one of the most important considerations in the simulation. Although it sounds reasonable to input as much information about a material as possible in a model, the calculating time required for actual analysis puts a limitation on what should be included. Therefore, prior to implementing a constitutive model for a specific material, several important aspects need to be carefully considered. First is the analysis objective. The main focus should be put on the most critical response the analyst is interested in rather than other materials that may seriously slow down the analysis time without significant accuracy improvement. Second, the simulation requires modeling the material behavior, not the actual material. For example, the creep behavior of eutectic Sn/Pb solder can occur at room temperature, but not under the circumstance with high loading and high rate of strain. As a result, in order to avoid inefficiencies in the analysis, there is no need to predict solder deformation caused by the rapid mechanical cycling at room temperature if the rate of loading is high enough to cause no deformation, while it is essential to include the creep behavior when simulating fatigue due to thermal cycling [83, 86].

5.1.3 Constitutive Models for SnAgCu Solder

A constitutive model is an approach to mathematically describe the relationship between strain, stress and other state variables. The material constitutive model plays a very important role in the development of thermomechanical models for microelectronic packaging assembly. Two types of deformation (elastic and inelastic) are formed inside the solder alloy when it is under thermomechanical loading. Since the inelastic deformation consists of time-dependent

creep deformation and time independent plastic deformation, it is not recoverable while the elastic deformation is recoverable. A combination of plastic, elastic, viscoplastic, or viscoelastic/creep models can be used to represent the constitutive behavior of materials.

In order to simulate correct solder stress-strain behavior under different loadings, the selection of constitutive model for solder joints is very critical since it is one of the important factors that can affect the accurate evaluation of the fatigue strength. Several creep and viscoplastic models have been discussed in the past to describe the thermomechanical behavior of SnAgCu solders.

Anand Viscoplastic Model: Anand [91] proposed a simple set of constitutive equations for large, isotropic, viscoplastic deformations. There are two basic features of this model. First, no explicit yield condition and no loading/unloading criterion are used. Second, this model consists of single scalar internal state variable "s", called the deformation resistance, to measure the isotropic resistance offered by the solder to the plastic flow. The Anand model can represent the physical phenomena of strain-rate and temperature sensitivity, strain rate history effects, strain-hardening and the restoration process of dynamic recovery. This model is broken down into a flow equation and three evolution equations. The flow equation accommodates the strain rate dependence on the stress at constant structure:

$$\dot{\varepsilon}_p = A\exp\left(-\frac{Q}{RT}\right)\left[\sinh\left(\xi\frac{\sigma}{s}\right)\right]^{1/m} \qquad (5\text{-}1)$$

where $\dot{\varepsilon}_p$ is the inelastic strain rate, A is a pre-exponential factor, Q is the activation energy, T is the current absolute temperature, R is the universal gas constant, ξ is a multiplier of stress, σ is the current tensile stress, s is the internal state variable (deformation resistance), and m is the

strain rate sensitivity. The evolution equation describes the strain hardening or softening of the material:

$$\frac{ds_o}{dt} = \left\{ h_o \left(|B| \right)^a \frac{B}{|B|} \right\} \frac{d\varepsilon_p}{dt} \tag{5-2}$$

$$B = 1 - \frac{S_o}{S^*} \tag{5-3}$$

$$S^* = S^{\wedge} \left[\frac{\frac{d\varepsilon_p}{dt}}{A} \exp\left(\frac{Q}{kT} \right) \right]^n \tag{5-4}$$

where h_o is the hardening/softening constant, a is the strain rate sensitivity of hardening/softening, the quantity s* represents a saturation value of deformation resistance, sˆ is a coefficient for deformation resistance saturation value, and n is the strain rate sensitivity for s saturation. Anand's model has been shown to provide reasonable results when compared to a combination of plasticity and creep model [Tunga et al, 2002]. It has been used in the ANSYS program as the standard option to describe viscoplastic elements. Nine material parameters (A, Q, m, n, ξ, *s*ˆ, *a*, h_o, and $s_{o,}$) need to be determined to model the material behavior of solder.

Creep Model: The elastic-creep model (Creep) incorporates the creep effect on solder material and all inelastic deformation is induced by creep phenomena.

Wiese et al. [92] studied the creep behavior of flip chip solder joint samples with Sn4.0Ag0.5Cu solder and the bulk solder specimen sample (a dog-hone type specimen), PCB specimen sample (copper wire soldered into a printed circuit board). They identified two mechanisms for steady state creep deformation for the bulk and PCB samples, and attributed these to low stress (climb controlled) and high stress (combined glide/climb) mechanisms. They represented steady state creep behavior by a double power law model as equation (5) shown

below, where $\dot{\varepsilon}$ is the total strain rate (1/sec), σ is the stress (MPa), E is the elastic modulus, T is the temperature, σ_n is 1Mpa, A_1 is 4.0 x10^{-7} 1/sec and A_2 is 1.0 x 10^{-12} 1/sec, D_1 is $\exp\left(\frac{-3223}{T}\right)$ and D_2 is $\exp\left(\frac{-7348}{T}\right)$. The second term in the equation (5-5) represents the climb controlled creep strain and the third term represents the combined glide/climb strain. Syed [93] has applied this creep model to develop a fatigue life model for SnAgCu solders.

$$\dot{\varepsilon} = \frac{\dot{\sigma}}{E} + A_1 D_1 \left(\frac{\sigma}{\sigma_n}\right)^3 + A_2 D_2 \left(\frac{\sigma}{\sigma_n}\right)^{12} \tag{5-5}$$

Zhang et a1. [94] and Schubert et a1. [95] generated data from different sources and from their own testing on different compositions of SnAgCu solder. They both modeled the steady state creep behavior using the hyperbolic sine function, and postulated the high stress region as a power law break-down region. The constitutive model proposed by both of them predicted very similar behavior at low stresses but start diverging at higher stresses. On the other hand, the model proposed by Wiese et a1. [92] predicts lower creep rate at low stresses. Figure 5.4 compares the creep curves for SAC solder from different constitutive models as mentioned here. Equation (5-6) represent the constitutive model of Schubert and Zhang, where A_1 = 277984 s^{-1}, α =0.02447MPa^{-1}, n=6.41, H_1/k =6500, E(MPa)=61251-58.5T(^{o}K), CTE=20ppm/K, Poisson's ration = 0.36 .

$$\dot{\varepsilon}_{cr} = A_1 \left[\sinh(\alpha\sigma)\right]^n \exp\left(\frac{-H_1}{kT}\right) \tag{5-6}$$

Morris et a1 [96] used a double power law constitutive model to represent creep data on single lap shear specimens of SAC305 solder joints. The stress exponents of 6.6 and 10.7 were suggested for the low and high stress regions.

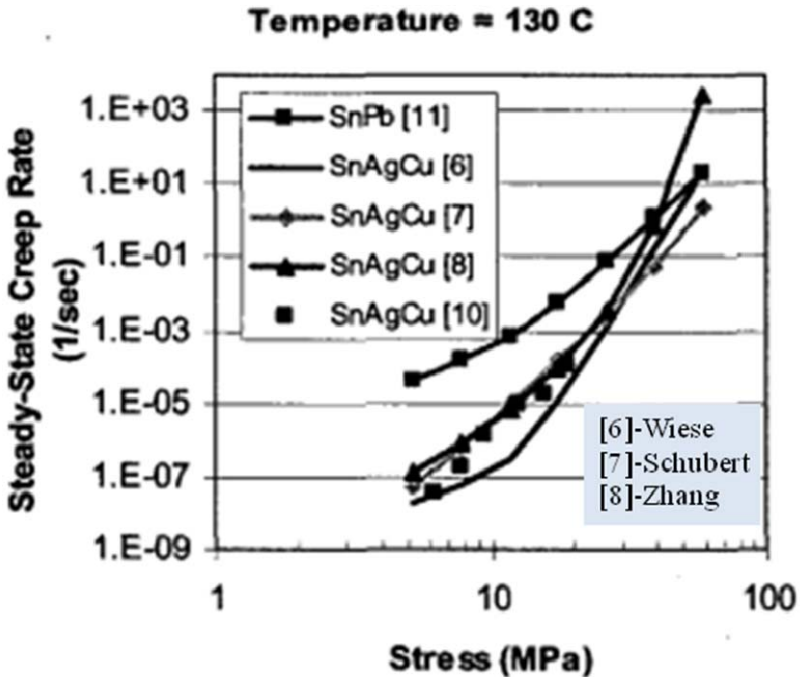


Figure 5.4 Comparison of Creep Models for SnAgCu and SnPb solder [92]

Elastic-Plastic-Creep Model: Pang et al. [97], Yang et al. [98], Vandevelde et al. [99], and Qian et al. [100] used the bilinear elastic-plastic and hyperbolic sine creep equation to describe the solder deformation response. This approach uses separate constitutive models for time independent plastic deformation and time-dependent creep deformation**.** The solder is modeled as an elastic-plastic-creep material with temperature and strain rate dependent Young modulus and yield stress material properties expressed by following equations [101]:

$$E(T,\dot{\varepsilon}) = (\alpha_1 T + \alpha_2)\log(\dot{\varepsilon}) + (\alpha_3 T + \alpha_4) \tag{5-7}$$

$$\sigma_y(T,\dot{\varepsilon}) = (b_1 T + b_2)(\dot{\varepsilon})^{(b_3 T + b_4)} \tag{5-8}$$

where T has unit of degree °C; strain rate for thermal cycling was usually correspond to 10^{-4}1/s. Constants in equation (5-7) and (5-8) are given in Table 5.1.

Table 5.1 Apparent modulus and yield stress constants for SAC solders [101]

SAC solder	α_1	α_2	α_3	α_4
	-0.0005	4.72	-0.117	37
	b_1	b_2	b_3	b_4
	-0.1362	67.54	5.59E-4	0.0675

5.1.4 Solder-fatigue life Models

Approaches for modeling of solder joint reliability can be divided into five major categories: (a) stress-based, (b) plastic strain-based, (c) creep strain-based, (d) damage accumulation-based, and (e) energy-based.

The stress-based model is based on the application of a stress to a component that can result in a strain. Typically, stress-based fatigue applies to vibrational or physically shocked or stressed components [102].

The strain-based model can be categorized into two groups: plastic strain and creep strain. Plastic strain deformation accounts for the time-independent plastic effects while creep strain

focus on the time-dependent effects [103]. Coffin-Manson, Solomon, Engelmaier, and Miner have proposed solder joint fatigue models based on plastic strain, and the Coffin-Manson fatigue model has become one of the most widely used approaches today. Creep strain fatigue models account strictly for the creep phenomenon involved in solder joints. Fox and Knecht have developed a simple matrix creep fatigue model relating the matrix creep shear strain range and solder microstructure [104], and later Syed [105] reported on the factors that affect matrix creep, grain boundary sliding. He also concluded a complex number of parameters that could affect the life prediction results.

The damage-based fatigue models are based on calculating the overall damage done to the solder joint that are produced by crack propagation through the solder connection. This model is developed based on a fracture mechanics approach. Stolkarts[106] has reported successful application of this model over a damage-free model.

The energy-based fatigue model is based on calculating the overall stress–strain hysteresis energy of the system or solder joint. This type of model has been increasingly used to predict the fatigue life of solder alloys. Over the years, Dasgupta[107], Akay[108], Liang et al [109], Wu et al. [110], Jung et al. [111], Gustafsson[112], and Darveaux[113] have proposed several finite element based analysis methodologies. Of all these methodologies, Darveaux's model seems to be the most popular due to the ease in its implementation. It utilizes finite element analysis to calculate the viscoplastic strain energy density accumulated per cycle during thermal or power cycling. It links laboratory measurements of low-cycle fatigue crack growth rates and crack initiation to the inelastic work of the solder. The strain energy density is then utilized with crack growth data to calculate the number of cycles to initiate a crack, and the number of

cycles for the crack to propagate across a solder joints diameter. The number of cycles before crack initiation N_0 is calculated as:

$$N_0 = C_1 \Delta W_{ave}^{C_2} \tag{5-9}$$

where ΔW_{ave} is the incremental inelastic energy per cycle at the stable cycle, and at the solder joint in concern, C_1 and C_2 are constants. The crack growth rate (da/dN) per cycle was also calculated in the similar equation as:

$$d_a / dN = C_3 \, \Delta W_{ave}^{C_4} \tag{5-10}$$

and the total number of cycles before failure (Na) can thus be written as:

$$N_a = N_0 + \frac{a}{d_a / dN} \tag{5-11}$$

where a is the total distance the crack has to travel before failure. For a solder joint, it can be conveniently interpreted as the solder diameter at the solder die interface. The viscoplastic strain energy density ΔW_{ave} (in psi) is defined by averaged quantity across the element along the solder joint interface where the crack propagates. Because Darveauxs model was developed in English Unit, the unit of a and ΔW_{ave} have been converted from a Metric Unit (mm and MPa) to an English Unit (in and psi) during the calculation of the fatigue life prediction. ΔW_{ave} was introduced and defined by:

$$\Delta W_{ave} = \frac{\sum_{i=1}^{n} dW_i V_i}{\sum_{i=1}^{n} V_i} \tag{5-12}$$

where dW_i is the incremental inelastic energy of element i at the first stable cycle, n is the total number of elements considered and V_i is the calculated volume of element i.

5.2 Modeling Procedure

In this project, all packages were subjected to thermal cycle testing and modeled in the ANSYS V.11.0 finite element program. The thermal cycle environment was simulated and the finite element model was validated with the actual thermal cycling results. The goal of the modeling effort was to achieve good correlation between the actual testing failure mode and simulation failure mode for the two different packages fabricated in this research: standard WLCSP and SolderBrace material coated WLCSP.

As mentioned in the previous sections, the construction of a finite element model is mainly composed of the consideration of the package geometry, the material properties, the mesh, and the loading profile. Several assumptions were specified in the simulation such as uniform temperature distribution in the package, no initial residual stress, no transient heat transfer, and gradually applied temperature loading.

5.2.1 Geometry

A 6x6 mm, 36-ball (6x6 Full Matrix) package was analyzed in this study. The schematic representation of the assembly (standard and SolderBrace-coated WLCSP) is shown in Figure 5.5, where different structural elements and their relative positions have been identified. All the UBM, soldermask and cupper pads were omitted in the simulation for simplicity.

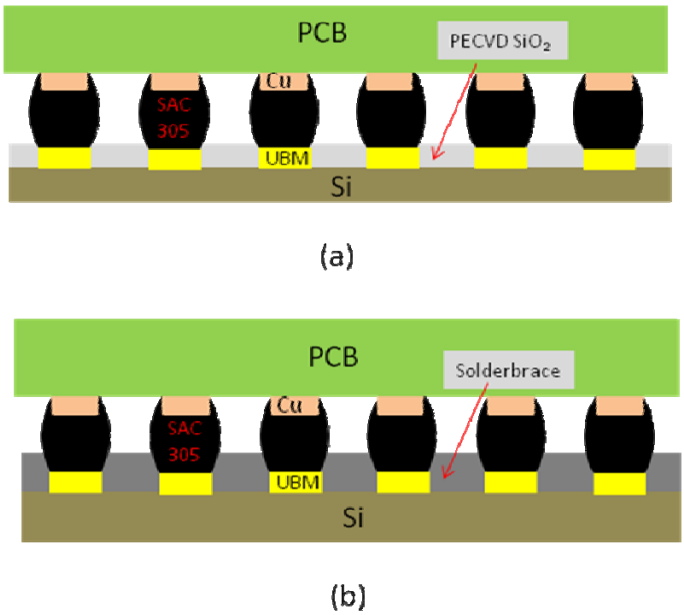
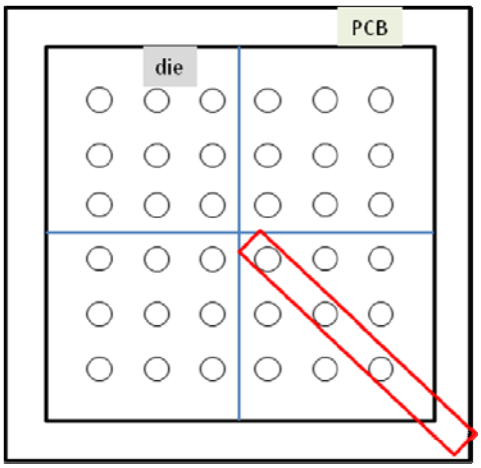


Figure 5.5 Schemiatic representation of the standard (a) and solderbrace-coated (b)WLCSP assembly (not to scale)

A diagonal slice symmetry model was used for finite element modeling in this study to reduce the computation time and capture the critical solder ball. This technique is usually used for packages having octant symmetry. The slice passed through the package, capturing the full set of solder joints and all major components as shown in Figure 5.6.



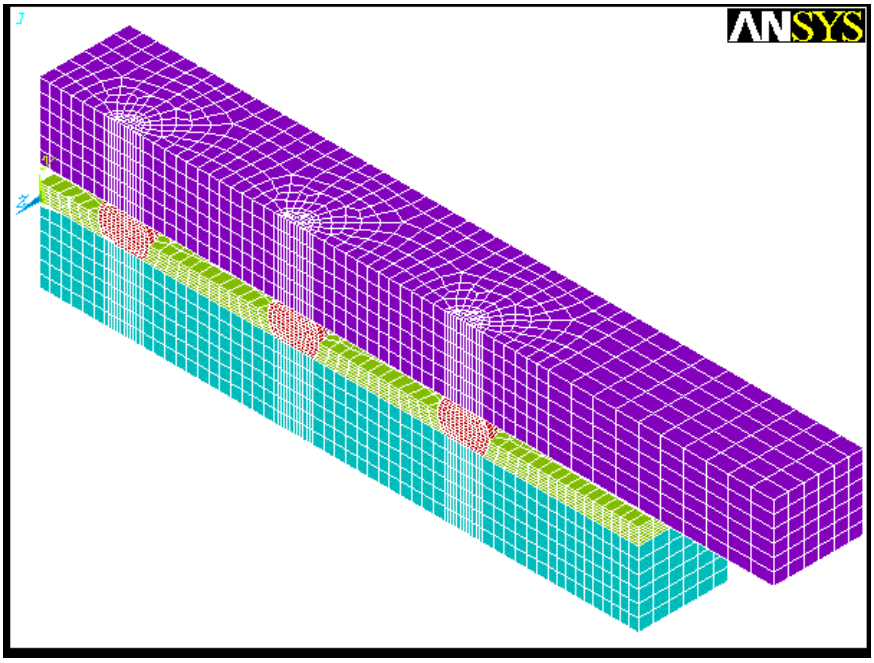


Figure 5.6 The diagonal symmetry model

5.2.2 Material Properties

Elements used for simulation were the eight node SOLID45 brick and the VISCO107 elements. Other than the solder balls modeled by VISCO107, all the rest of the materials in the package were modeled by eight nodes SOLID45.

As taken from the ANSYS element library, SOLID45 is used for 3-D modeling of solid structures. It is defined by eight noded elements and has three degrees of freedom at each node. It has the capability to model creep, plasticity, swelling, and other deformation features. The VISCO107 element also has eight nodes and three degrees of freedom at each node. It is used to model rate dependent plasticity. This element is chosen for solder defined with the Anand model, while the SOLID 45 element is used for solder defined with elastic-plastic-creep model.

All of the materials in the package were modeled as isotropic except for the PCB which was modeled as orthotropic. For the Sn3.0Ag0.5Cu solder, material properties used in the Anand model are shown in Table 5.2. The material properties for the finite element models of both WLCSP packages are shown below in table 5.3.

Table 5.2 Anand constants SAC 305 [112]

SAC 305 Anand constants	
S_o	45.9 (MPa)
Q/k	7460 $(1/K)$
A	5.87e6 $(1/\text{sec})$
ζ	2
m	.0942
h_o	9350(MPa)
n	.015
a	1.5
$\hat{s}$	58.3(MPa)

Table 5.3 Material Properties of models

Material	Elastic Modulus (GPa)	CTE ppm/^{o}C	Possion's Ratio
PCB	17(x,z) , 7(y)	15(x,z) 67(y)	0.39
Solder Ball	30	25	0.35
Silicon Die	162	2.54	0.28
SolderBrace	4	14	0.3
PECVD SiO_2	80	0.5	0.25

5.2.3 Meshing

Accuracy of the FE model depends on not only the accuracy of the materials properties, but also the proper meshing. In this study, the model was built from the top down. The mesh

was created at the same time when the volumes were created using the "VSWEEP" command in ANSYS. This command guarantees a coincident node and mesh at the interfaces of different volumes. Figure 5.7 is a close-up view of the meshed model, specially the fine mesh at the solder joint due to the interest of the solder joint fatigue study.

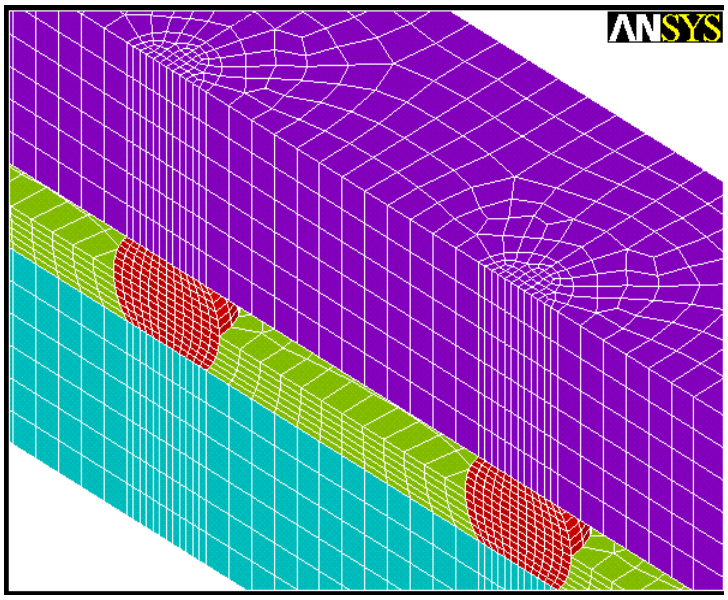


Figure 5.7 Finished mesh for the solderbrace-coated WLCSP package

5.2.4 Boundary Conditions

The use of a slice model involves a choice on the part of the analyst on the boundary constraints to be applied at the slice plane. The plane is neither a free surface nor a true symmetry plane. The reasonable compromise of coupling the y-displacements of the nodes on the slice plane was chosen. This has the effect that the slice plane is free to move in the y-

direction, but that the surface is required to remain planar. Boundary constraints applied in this study are shown in Figure 5.8.

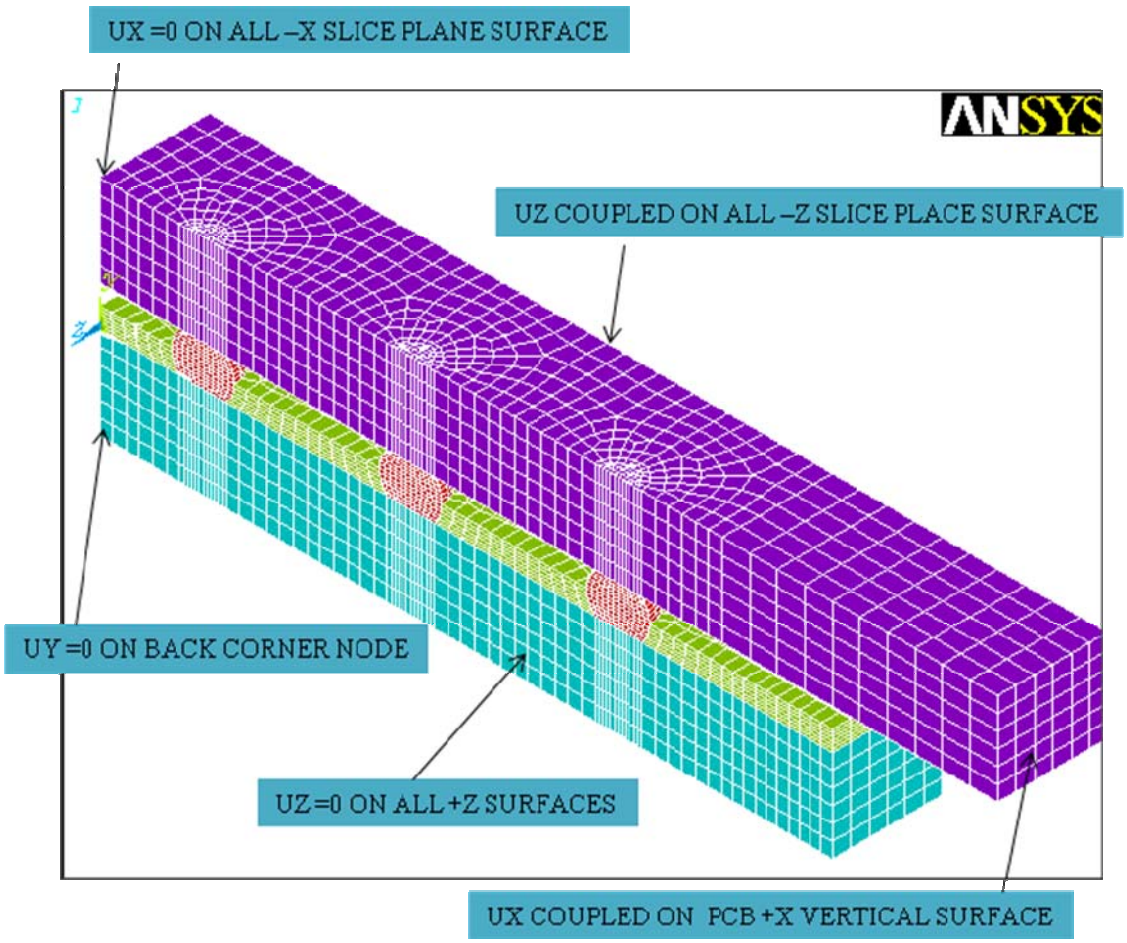


Figure 5.8 Boundary Conditions applied to a typical slice model

5.2.5 Thermal Loading

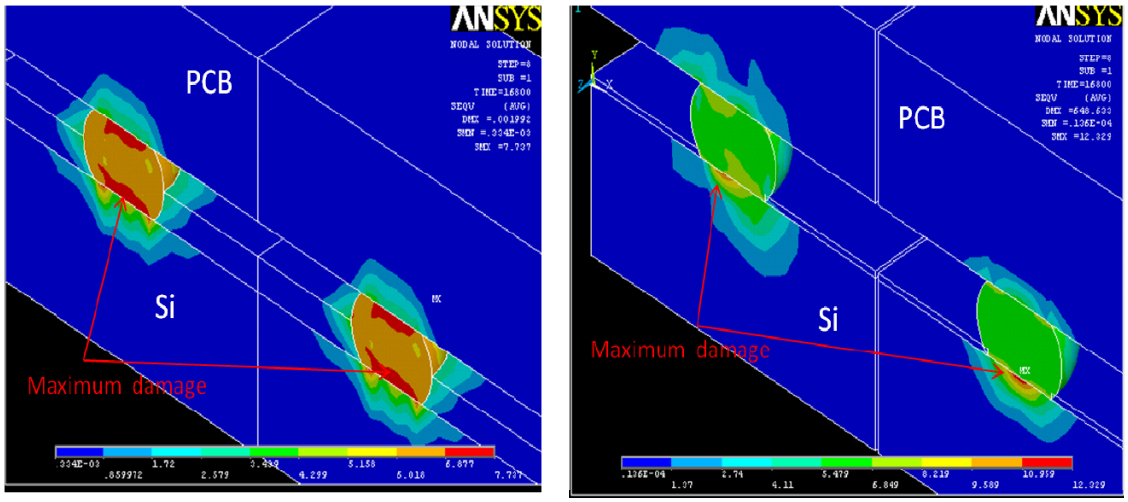
The temperature profile in the thermal cycle used for the modeling consists of four stages: temperature ramping to low extreme in 30 minutes; temperature dwelling at low extreme for 15 minutes; temperature ramping to high extreme in 30 minutes; temperature dwelling at high extreme for 15 minutes. The temperature cycling range was from -55°C to 125°C. The zero strain (zero deformation) reference temperature was set at the high temperature since the package deformation trend occurs from the maximum temperature. The sequence of ANSYS commands below indicates the setting of the zero strain reference temperature along with those required for the first thermal cycle. To finish the simulation of the second thermal cycle, the above ANSYS command groups for load steps 1 through 4 were repeated.

/PREP7	
tref,398	! set zero strain temp at 125^{o}C
toffset,0	! temp offset
tref,398	! set zero strain temp at 125^{o}C
autots,on	! turn on auto time step
/SOLU	
bf,all,temp,218	! apply temp to all nodes at -55^{o}C
kbc,0	! linearly ramp loads
time,900	! set time for 15 minutes
solve	! solve load step
save	
bf,all,temp,218	! apply temp to all nodes at -55^{o}C
kbc,1	! maintain loads
time,2700	! set time for 45 minutes
solve	! solve load step
save	
bf,all,temp,398	! apply temp to all nodes at 125^{o}C
kbc,0	! linearly ramp loads
time,3600	! set time for 60minutes
solve	! solve load step
save	
bf,all,temp,398	! apply temp to all nodes at 125^{o}C
kbc,1	! maintain loads
time,5400	! set time for 90minutes
solve	! solve load step
save	
finish	

5.2.6 Fatigue Model Results

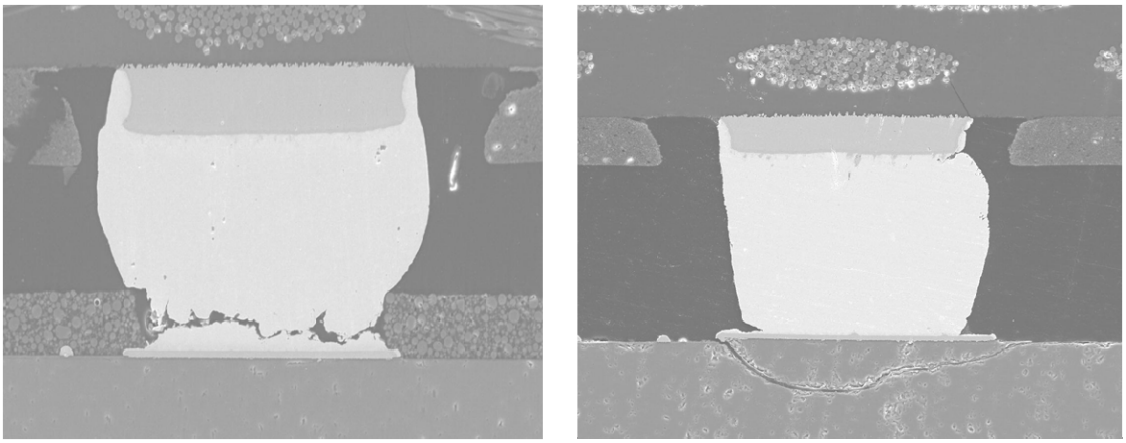
The results of the simulation are shown in Figure 5.9. It can be seen that the maximum Von Mises stress in the Solderbrace-coated models appears inside the solder ball while the maximum damage was seen inside the Si pad for the control (non-coating) models. These

simulation results correlate to the air-to-air thermal cycling reliability test results as described in Chapter 4 (see Figure 5.10).



(a) (b)

Figure 5.9 Von Mises stress (MPa) distribution in the solder joint for (a) Solderbrace-coated model and (b) Reference (non-coating) model



(a) (b)

Figure 5.10 Air-to-air thermal cycling reliability test results

5.2.7 Thermal Fatigue Life Prediction of Solderbrace-coated Solder Joints

According to the literature review of prediction models given in the previous section, Darveaux prediction model was used in this research for Solderbrace-coated Solder Joints due to the ease in its implementation. The governing equations and parameters are listed in Table 5.4.

Table 5.4 Prediction model and parameters used in this study

Category	Failure Parameter	Equations	Reference
Energy-based life prediction model	ΔW_{ave} (psi)	$N_0 = C_1 \Delta W_{ave}^{C_2}$ $d_a/dN = C_3 \Delta W_{ave}^{C_4}$ $N_a = N_0 + \frac{a}{d_a/dN}$ C_1= 22400, C_2= -1.52 C_3= 2.76E-7, C_4= 0.98 a= 0.0118(inch), ΔW_{ave}= 79.75 (psi)	Darveaux [114]

Simulation results were compared to the air-to-air thermal cycling reliability test results as described in Chapter 4. Table 5.5 summarizes the characteristic life from the exterimental test results and the model prediction results. The Darveaux model produced a close correlation but

still over-estimated by approximately 20%. As the Solderbrace material is still new, further investigation is required to determine its exact material properties. In addition to material properties deviations may result from various model parameters such as element type, or shape and size.

Table 5.5 Summary of the characteristic life

	Experimental Result	Prediction Result
Characteristic life N_a	510 cycles	613 cycles

CHAPTER 6

CONCLUSIONS

Wafer level chip scale package (WLCSP) designs have been used in many consumer products, and thus they are competitive in cost, size, yield, and technology. Solder joint reliability is a major concern for advanced WLCSPs. Typical stress-relieving methods such as capillary underfills and molding compounds have not been the preferred solutions due to the extra packaging cost they bring into the assembly process. Instead, successful low cost reliability solutions have generally been the adaptation of wafer level backend packaging processes such as modification of the redistribution layer materials, solder selection, or metal pad thickness. However, the increased performance is limited.

In this research, a cost effective solution to WLCSP reliability improvement can be enabled through wafer level coatings (SolderBrace coating). This new approach is presented to reexamine the final passivation layer as more than a dielectric, but also a partial underfill. SolderBrace coating adds a mechanical buffer to the front side of the WLCSP and delivers improved reliability with conventional tools, short process times and lower costs.

Test WLCSPs, including the SolderBrace coated WLCSPs and standard non-coated WLCSPs, were designed and fabricated with known standard fabrication procedures. The processing of the SolderBrace coatings was achieved by two different methods: Coating-type solder bracing and Maskless printing over solder balled wafer. These coatings were low

temperature cured, had low CTE values and generated minimal wafer bow. After the singulation, test WLCSPs were assembled to the circuit boards. The standard thermal cycling test from -55^{o}C to 125^{o}C was used for reliability testing. A finite element based approach was also used to gain a deeper understanding of the solder joint failure mechanism caused by the repeated thermal stress. According to the test results, the SolderBrace coated dies had much higher lifetime than the non-coated dies. SolderBrace technology may offer a unique method to package low cost high performance WLCSPs. The simulation results also give insight on the stress generation and can provide guidance to appropriate design adjustment.

Since the current generation of SolderBrace is targeted to CSP pitches i.e., 0.3mm to 1mm pitch device, future research can be focused on the application of new SolderBrace for much finer pitch device. In addition, this SolderBrace material is photosensitive, but limited to the minimum dimensions that can be resolved. Future research needs to address the development of a second generation material that will improve the resolution by changing the curative formulation and material chemistry to reduce the amount of scattering that normally would take place in a thick coating.

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