HIGH TEMPERATURE HIGH POWER SiC DEVICES PACKAGING PROCESSES

AND MATERIALS DEVELOPMENT

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HIGH TEMPERATURE HIGH POWER SiC DEVICES PACKAGING PROCESSES AND MATERIALS DEVELOPMENT

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HIGH TEMPERATURE HIGH POWER SiC DEVICES PACKAGING PROCESSES

AND MATERIALS DEVELOPMENT

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Cai Wang, son of Hanping Wang and Saier Chang, was born August 6, 1970, in Jiangsu, China. He attended Tsinghua University in Beijing, China, and graduated with a bachelor of Material Science and Engineering in July of 1993. He entered Graduate School at Auburn University in March 2000. He received Master degree of Electrical and Computer Engineering in 2003. He then continued his education in the Ph.D. program in the Department of Electrical and Computer Engineering of Auburn University.

DISSERTATION ABSTRACT

HIGH TEMPERATURE HIGH POWER SiC DEVICES PACKAGING PROCESSES AND MATERIALS DEVELOPMENT

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Silicon power devices have reached their theoretical limits in terms of higher temperature and higher power operation by virtue of the physical properties of the material. SiC has been identified as a material with the potential to replace Si devices because of its superior material advantages. However, there is a lack of reliable packaging techniques and materials for SiC, in particular die attach, wire bonding and die passivation that can survive temperature as high as 500ºC.

Based on the high melting point of Au-In alloy (81/19 wt%), it was evaluated as a potential high temperature die attach material using a transient liquid phase bonding process in this study. Thermal cycle test results over the temperature range from 35ºC to

400ºC and high temperature storage at 450ºC results are presented. Vertical cracks developed in the die attach on Mo tabs during the thermal cycling tests and indium segregated to the defects (voids and cracks) during the high temperature storage and thermal cycling tests. This segregation appeared to negatively impact the reliability of the die attach.

The 6μm of nickel or nickel phosphorous commonly used as a barrier layer in conventional ceramic substrate metallization did not prevent Cu diffusion to the surface at a temperature of 450°C. A multi-layer nickel phosphorous structure was found to serve as a good barrier to prevent Cu diffusion for high temperature applications.

The bondability and reliability of large diameter (250μm) gold and platinum wire using thermosonic wedge bonding was investigated. High temperature storage results at 350ºC for wire bonds on the substrate metallization and 300ºC for die metallizations are presented. A simplified FEMA 2D model was used to understand the effects of bond force and die metallization structure on the failure modes, SiO_2 cracking and SiC cratering. The results matched the experimental results very well. This work demonstrated the effects of wire and pad stack metallurgy on bond reliability.

Polyimide PI2611has been evaluated as a passivation coating material. The results were promising at 300°C; however, higher temperature tests have shown rapid decomposition of the polyimide.

In this work, electrical characteristics of VJFET and SIT diode modules were measured over the temperature range from 25°C to 400°C to demonstrate the feasibility of paralleling SiC power VJFETs to develop Si IGBT replacements. Paralleled VJFETs formed an equivalent switch of much greater current than the single VJFET, and showed

a positive temperature coefficient of on-resistance. The paralleled SIT diodes resulted in a lower cut-on voltage than the single SIT diode, and the leakage current of the paralleled SIT diodes was less than 70 μA when V_{ds} = 100 V at 400°C, validating the impressive blocking performance of the SIT diode at extreme temperatures.

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CHAPTER 1 INTRODUCTION

There is a growing demand for cost effective high power, high temperature semiconductor devices to support the latest advancements in aerospace, automotive, and high power electronics systems. The goal of power electronics is to transfer power from an electrical source to an electrical load in a highly efficient, highly reliable and cost-effective way. Power electronics packages provide mechanical support, device protection, cooling and electrical connection and isolation. Controlling and reducing power loss from packaging materials in the package is becoming increasingly important [1].

High power devices usually operate at high current densities, high internal electric fields and, consequently, high temperatures. High operating temperatures can result from either the ambient environment, dissipated power or a combination of both. For applications at temperatures above 300°C, it is very challenging to use conventional semiconductor electronics because they are generally limited to operating temperatures below 250°C due to the limitations imposed by their material properties and traditional packaging technology [2].

The use of silicon carbide device technology opens the door for electronic circuits operating at 350°C and higher. SiC has long been viewed as a potentially useful semiconductor for high temperature applications. SiC-based electronics and sensors have been demonstrated to operate at temperatures up to 600°C, thereby offering the promise

of direct insertion into high temperature environments without the need for cooling. However, the lack of reliable device packaging methodologies for this operating environment has so far largely prevented the application of these devices[3][4][5][6].

Figure 1.1 shows the structure of a potential SiC power transistor package. The thick metallization on the ceramic substrate is typically a thick layer of copper, covered by a thick coating of nickel that serves as a barrier layer, capped by an electroplated gold layer, which functions as the die attaching or wire bonding metallization. The power SiC transistor is attached to the gold metallization, typically using a soldering or brazing process. Then, wires are thermosonically wedge bonded from the pads on the power die to the lead frame or substrate metallization. Finally, a passivation layer is applied and cured to provide high voltage insulation.

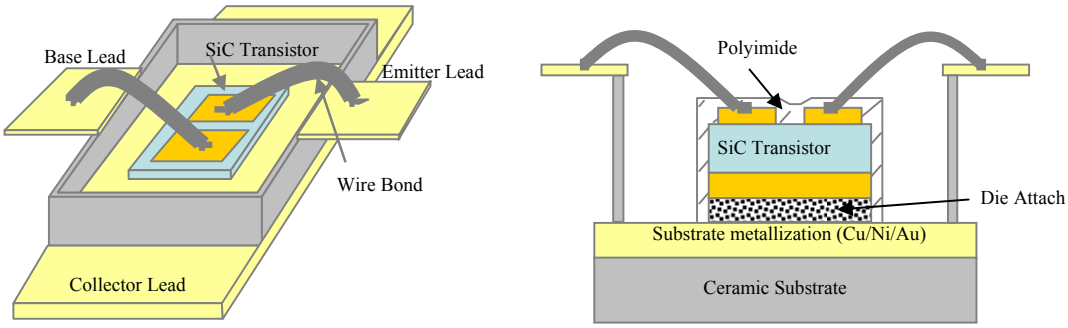


Figure 1.1 SiC power transistor device structure

The SiC power transistor is expected to be capable of functioning in harsh environments and needs an appropriate package in order to sustain operation throughout the entire planned life cycle. In the absence of robust and reliable packaging, this device

is useless if it cannot perform its designed functions and survive the harsh environments. In order to realize the potential of the SiC transistor for high temperature applications, appropriate high temperature packaging technologies must therefore be developed [7].

The key processes and materials that need to be developed for the SiC transistor device package include:

- Die attach. For power SiC transistor devices used in high temperature applications, the die attach must produce a joint between the die and substrate, which must have a higher melting point than the operating temperature, and have good electrical and thermal conductivity. The material selection of SiC die backside metallization, substrate metallization, and die attach material is very important to the bonding process success.

  Typically, SiC die backside metallization requires three metallization layers for high temperature applications: the ohmic or Schottky contact, the diffusion/oxidation barrier layer and the cap layer. For die attach process success, the die backside metallization must have good adhesion; the cap layer, in general, Au, must have good wettability with the die attach material in order to obtain a void-free bond joint; and the barrier layer must have high resistance to oxidation and inter-diffusion in order to keep the contact resistance consistent for device performance.

  The ceramic substrate metallization provides a base for the die attachment of the power device. The conventional substrate metallization, Cu/Ni/Au on alumina ceramic, was used in this research. Cu provides high electrical current and thermal conducting paths from the power device to the outside circuit, Ni

functions as a barrier layer to prevent Cu diffusion, and Au provides good wettability with the die attach material in order to obtain a void-free bond joint.

Au based alloys are the ideal die attach materials due to their good adhesion to the die and substrate metallization, high electrical and thermal conductivity, and good corrosion resistance. In this dissertation, a transient liquid phase bonding method using gold-indium (81/19 wt%) preforms was developed for the die attach process. Either excess Au plated on the die backside metallization SiC/Ni_2Si/Ti/TiW/Au or Ag plated on the substrate metallization was used to change the Au-In preform composition, thus leading to an increased solidus temperature. Die attach reliability testing and failure analysis were also performed.

- Wire bonding. Large diameter wire bonding is the most widely used method to make electrical connections from the power device to its package because large diameter wire provides high current carrying capability. Large diameter aluminum wire bonding is used with Si power devices, but at high temperatures the mechanical strength of the Al decreases significantly. Also, Al is incompatible with the Au wire bond pads due to intermetallic formation and Kirkendall voiding at high temperatures [5]. Large diameter gold and platinum wire appear to offer good alternatives to Al wire for high temperature applications because they have no incompatible issues with the Au wire bond pads and provide high current capability, and both Au and Pt are highly corrosion resistant to air and harsh environments. The main disadvantages of large diameter wire bonding, especially for Pt wire, are the high bonding force or high ultrasonic energy required for the

bonding process, which have significant impact on the layers underneath the die bonding pads. In the worst case, the SiC may be damaged. For the substrate bonding pads, the high bonding force or ultrasonic energy has less impact because of the thickness of the substrate metallization compared to the thin die metallization. A thermosonic wedge bonding method was developed to bond the large diameter (250μm) Au and Pt wires used in this dissertation. The wire bondability and reliability of conventional substrate metallization Cu/Ni/Au and three die metallizations ($SiC/Ni_2Si/SiO_2/Ti/Pt/Au$, $SiC/Ni_2Si/SiO_2/Ti/TiW/Au$ and $SiC/Ni_2Si/TaSi$-(2%)/Pt-N/Au) were evaluated in this study.

- High temperature passivation. Devices operating at high power conditions may also be exposed to high voltages, and as a result high voltage breakdown may occur between adjacent electrical connections and/or between high voltage electrical connections and the surrounding air. This issue is particularly important as the breakdown voltage of air decreases with increasing temperature. With the die contact pads exposed to air, leakage current through the air or at the die surface will increase with increasing temperature. An effective dielectric passivation coating must therefore be applied to ensure reliable package operation.

  Polyimides have both higher insulation resistances and higher breakdown voltages than air at high temperatures, so they can be used as a passivation layer to decrease the leakage current and increase the breakdown voltage between adjacent ohmnic contact pads. This research evaluated the reliability of one

polyimide material (PI2611) as a passivation layer for high temperature applications.

The primary goal of the project was to develop assembly materials and processes for SiC power electronic components that can be used in extreme environments. In Chapter 2, the properties, processing and device technology related to SiC are briefly reviewed and some key issues in packaging of power electronics are discussed, including SiC properties, SiC die thin film metallization, substrate and substrate metallization, die attach materials and processes, wire bonding, and high voltage passivation coatings.

Chapter 3 describes an investigation of the Au-In die attach using a transient liquid phase bonding process, including die metallization, substrate metallization, the die attach bonding process, reliability based on shear strength tests and the cross-section microstructure of the die joint. Failure analysis after reliability testing was performed. In addition, a variety of barrier materials for copper diffusion in the substrate metallization stack was evaluated for high temperature applications.

Chapter 4 reports the results of an investigation of large diameter gold and platinum wire bonding on substrate metallization and die metallizations, including the wire bonding process itself, bondability and reliability based on pull and shear strength tests. A simplified FEMA 2D model was used to understand the failure mode observed.

In Chapter 5, the results of electrical breakdown tests of PI2611 polyimide are presented. This chapter includes a study of the polyimide application and curing process, breakdown tests and reliability tests.

In chapter 6, electrical characteristics of VJFET and SIT diode modules were measured over the temperature range from 25°C to 400°C to demonstrate the feasibility of paralleling SiC power VJFETs to develop Si IGBT replacements for use in electric vehicles.

Chapter 7 summarizes the results and findings of this dissertation. Topics for future work are also discussed.

CHAPTER 2 BACKGROUND

This chapter provides background information related to the topics that will be discussed in this dissertation. SiC properties, thin film die metallization, thick substrate metallization, wire bonding, die attach, and the properties and applications of polyimide passivation coatings are discussed.

Power devices capable of functioning in harsh environments need an appropriate package in order to sustain operation throughout their entire planned life cycle. In order to realize the potential of high temperature electronics, appropriate high temperature packaging technologies must therefore be developed [8]. The basic elements of the SiC transistor device package include: 1) the substrate; 2) the SiC die attach materials; 3) wire bonding; and 4) insulation materials.

For high power devices that will be used in high temperature and harsh environment applications, the most critical issues to be considered are[7][8][9]: 1) current carrying capability, which requires thick substrate metallization and large diameter wire bonds; 2) high voltages, which requires a suitable insulation material with high stability at high temperatures; 3) the mitigation of thermal stresses caused by the thermal expansion mismatches (CTE) between the devices and the various packaging elements, including substrates; 4) resistance to the fatigue brought about by thermal cycling during service; 5) the provision for appropriate heat removal to maintain the temperatures at safe

operating levels; and 6) resistance to high temperature effects such as those induced by diffusion, intermetallic formation, creep and decomposition. Material properties can significantly impact how well the package can meet these stringent requirements. Therefore, the package design is, to a great extent, influenced by the available materials.

The following material properties must be considered during the process of selecting proper materials for high temperature, high power devices for use in harsh environment applications [7][8][9][10][10]:

- Electrical conductivity: For power electronics, thick copper metallization is required to provide the high current carrying capability. Thick copper metallization on ceramic substrates can be achieved by direct bond copper (DBC), copper electroplating onto an adhesion layer or by reactive brazing a copper foil to the ceramic.
- Thermomechanical compatibility: Thermal expansion differences between the die and the substrate, as well as between the different packaging components, can produce stress during assembly as well as during operation that can result in the failure of the package or the device. The coefficient of thermal expansion (CTE) mismatch between the die, substrate, and other packaging components should be as small as possible at all temperatures to minimize thermal stresses.
- Fatigue resistance: the SiC package should have good fatigue resistance in order to withstand cyclic stresses due to exposures to high and low temperature extremes.
- Thermal conductivity: If the die temperature exceeds the safe operating temperature, the device will fail prematurely. Therefore, the system's thermal

resistance must be minimized. The substrate metallization and die attach joint thermal conductivity must also be maximized. The fact that the thermal conductivity of packaging materials decreases with increasing temperature must be considered.

- Chemical stability: Wire bonding materials should have good corrosion resistance in harsh environments, and be compatible with Au wire bond pads. Die and substrate metallizations should limit inter-diffusion and oxidation for long term stability at assembly and service temperatures. The insulating materials should have high temperature stability without suffering problems due to decomposition.

2.1 SiC Properties

Historically, germanium was one of the first semiconductors to be used. However, it was rapidly supplanted by silicon, which today is the most important semiconductor material. Silicon has a wider bandgap energy than germanium, allowing it to be used in higher temperature applications. Thermal oxidation of silicon forms a stable insulating oxide, giving silicon significant processing advantages over germanium during the fabrication of ICs. In addition to silicon, GaAs is commonly encountered today in optoelectronic applications, including light-emitting diodes (LEDs), lasers, and photo detectors. However, the superior physical and electronic properties of SiC make it the foremost semiconductor material for short wavelength optoelectronic, high temperature, radiation resistant, and high-power/high-frequency electronic devices [2][12]. The key properties of SiC compared to other semiconductor materials are shown in Table 2.1 [13].

Table 2.1 Key properties of semiconductor materials [13]

	Si	GaAs	4H-SiC	6H-SiC
Band Gap (eV)	1.12	1.43	3.26	3.03
Breakdown Electric Field (V/cm for 1000V Operation)	2.50E+05	3.00E+05	1.00E+06	1.00E+06
Thermal Conductivity (W/cm-K@ R.T)	1.5	0.5	3.38	3.38
Saturation Electron Drift Velocity (cm/s@E>2x105V/cm)	1.00E+07	1.00E+07	2.00E+07	2.00E+07

SiC has many polytypes, but 6H and 4H (H=hexagonal) are the two most commonly used. SiC offers unique electrical and thermophysical properties compared to Si and GaAs, which include [13]:

- Wide energy bandgap. With bandgaps of only 1.12eV for Si and 1.43eV for GaAs, both become intrinsic and lose their pn junction characteristics at 200~350°C, depending on their doping concentrations. Leakage currents also become a challenge, requiring silicon-on-insulator technology as temperatures approach 200°C. With a bandgap over 3eV, electronic devices formed in SiC can operate at extremely high temperatures without suffering from intrinsic conduction effects. Also, this property allows SiC to emit and detect short wavelength light, which makes the fabrication of blue light emitting diodes and nearly solar blind UV photodetectors possible.
- High breakdown electrical field. SiC can withstand a voltage gradient (or electric field) over eight times greater than either Si or GaAs without undergoing avalanche breakdown. This high breakdown electric field enables the fabrication of very high-voltage, high-power devices such as diodes,

power transistors, power thyristors and surge suppressors, as well as high power microwave devices. Additionally, it allows the devices to be placed very close together, providing high device packing density for integrated circuits.

- High thermal conductivity. SiC is an excellent thermal conductor. Heat will flow more readily through SiC than other semiconductor materials, and at room temperature, SiC even has a higher thermal conductivity than many metals. This property enables SiC devices to operate at extremely high power levels and still dissipate the large amounts of excess heat generated.
- High saturated electron velocity. SiC devices can operate at high frequencies (RF and microwave) because of its high saturation electron drift velocity.

Collectively, these properties allow SiC devices to offer tremendous benefits over other available semiconductor devices for a large number of industrial and military applications, such as geothermal well logging and instrumentation, distributed controls for aircraft, and power electronics for more electric aircraft, ships and combat vehicles.

2.2 Thin Film SiC Die Metallization

Composite (multi-layer) contacts that are compatible with the techniques and procedures used for packaging (wire bonding and die attach) are used for high temperature, high power devices [1]. A typical composite contact is shown in Figure 2.1

[14]. The simplest composite contact requires three metallization layers: 1) the ohmic or Schottky contact; 2) the diffusion/oxidation barrier layer and 3) the cap layer [1][14].

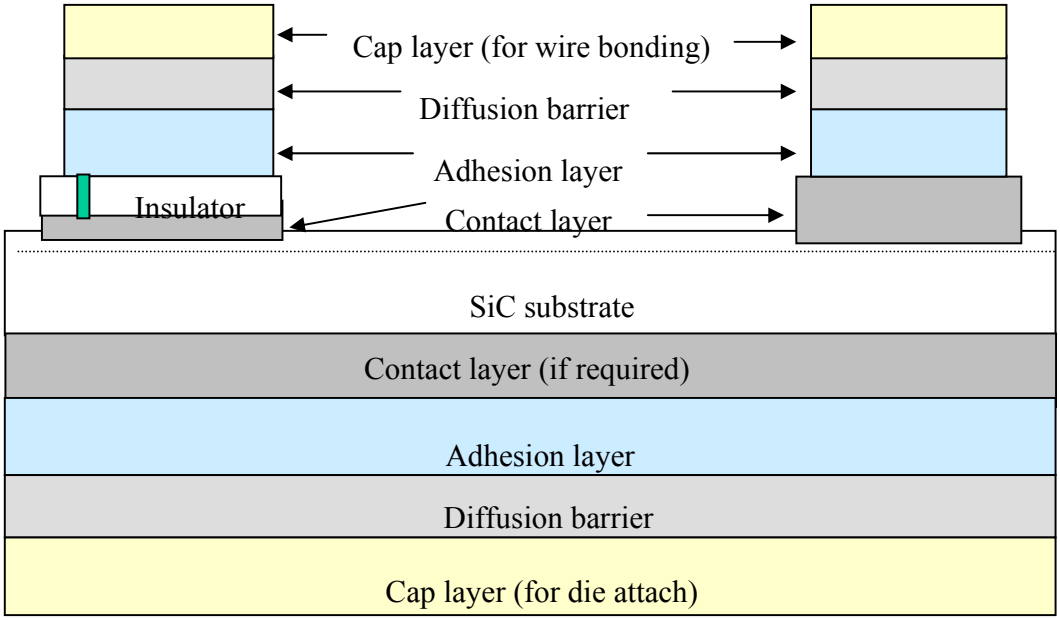


Figure 2.1Typical composite contact on SiC bipolar transistor [14]

An ohmic contact must have symmetric current-voltage (I-V) characteristics, with the lowest possible specific contact resistance. A Schottky contact is a metal-semiconductor contact with asymmetric I-V characteristics. It should be able to turn on at low forward voltages, and the reverse leakage current should be as low as possible. The diffusion/oxidation barrier layer must have metal-like conduction while preventing, or at least slowing, the intermixing of stack layers as well as preventing oxidation of the contact, which can lead to increased contact resistance. Because of the non-ideality of the barrier layer, it may be necessary to introduce other layers (e.g., a suitable adhesion layer) in the metallization stack. Finally, the cap layer must be suitable for packaging through wire bonding or die attach [14].

When a metallized SiC die in a package is exposed to a harsh environment (generally a high ambient temperature) during the packaging process and during its service life at high temperature, several things can happen [7][8][9][10]:

- The reactivity of the metal with its substrate may increase. This reactivity could be limited to inter-diffusion or it could lead to a chemical reaction, resulting in new compound formation.
- The electrical resistance of the metal stack may increase due to: 1) oxygen diffusion in the composite metallization and consequent oxidation of the contacts; 2) the intermixing/diffusion between different layers; or 3) grain growth even if there is no significant inter-diffusion or reaction with the surroundings. This reduction in conductivity can cause additional heat generation, and can also contribute to increased time delays and a loss of performance in high-speed applications.
- Electromigration induced by flowing current may be enhanced due to increased self-diffusion. Electromigration can lead to failures by forming open or short circuits.
- The difference between the coefficient of thermal expansion (CTE) of the metallization and that of the die may increase with increasing temperature. CTE mismatches cause thermal stresses that often lead to delamination.

The reactivity of the metal, electromigration, grain growth, and hillock growth are influenced by the self-diffusion in the metal and between the metal and its surroundings. Diffusion in metals is related to the melting point and the crystallinity of the metal; the

higher the melting point, the lower the diffusivity. As a rule of thumb [7], the melting temperature of the metal should be at least 1.5 times higher than the operating temperature in order to prevent diffusion-related problems such as creep and electromigration. Also, an effective diffusion barrier layer in the stack can prevent or hinder oxidation and inter-diffusion problems.

Therefore, an effective die metallization for high temperature applications should possess the following features:

- High oxidation and inter-diffusion resistance;
- Good adhesion to the wafer passivation layer and contact (ohmic or Schottky);
- Low contact resistance;
- Low thermal stress;
- High compatibility with the packaging process (wire bonding and die attachment); and
- High temperature stability.

Evaporation and sputtering are the two most used technologies for thin film metallization deposition. In the evaporation process, the substrate is placed inside a vacuum chamber, in which a block (source) of the material to be deposited is also located. The source material is then heated to the point where it starts to boil and evaporate. Vacuum is required to allow the molecules to evaporate freely in the chamber, and they subsequently condense on all surfaces [15]. This principle is the same for all evaporation technologies, only the method used to heat (evaporate) the source material differs. There are two popular evaporation technologies, e-beam evaporation and resistive

evaporation. In e-beam evaporation, an electron beam is aimed at the source material causing local heating and evaporation. In resistive evaporation, a tungsten boat, containing the source material, is heated electrically with a high current to make the material evaporate. Many materials are restrictive in terms of what evaporation method can be used (i.e. aluminum is quite difficult to evaporate using resistive heating), which typically relates to the phase transition properties of that material [15]. A schematic diagram of a typical system for e-beam evaporation [16] is shown in the Figure 2.2.

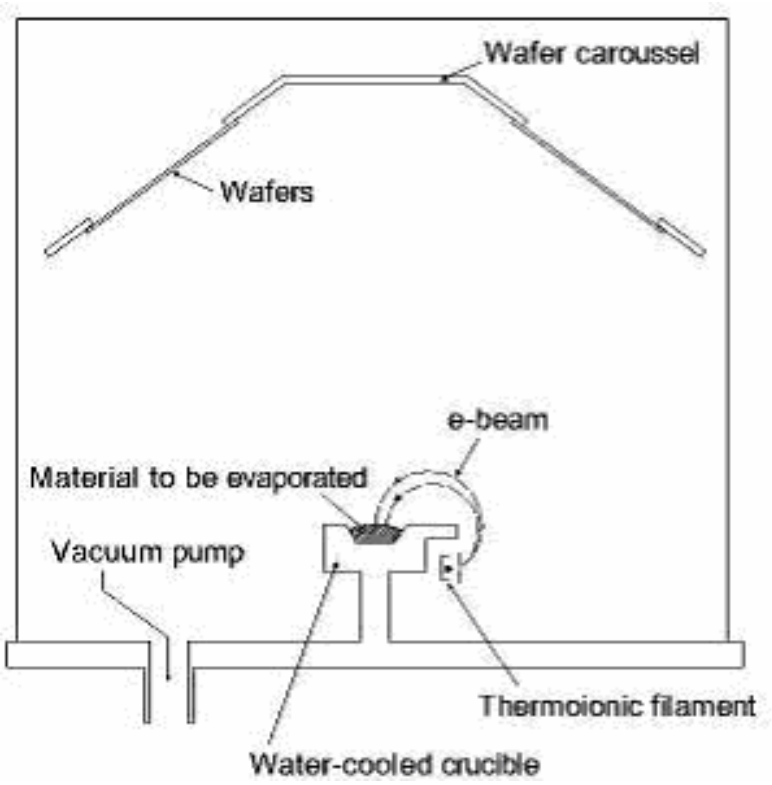


Figure 2.2 Typical system of e-beam evaporation of materials [16]

Sputtering is a technology in which the material is released from the source at much lower temperature than evaporation. The substrate is placed in a vacuum chamber with the source material, called a target, and an inert gas (such as argon) is introduced at low pressure. A gas plasma is struck using a DC or RF power source, causing the gas to become ionized. The ions are accelerated towards the surface of the target, causing atoms of the source material to break off from the target in vapor form and condense on all surfaces including the substrate. The basic principle of sputtering is the same for all sputtering technologies. The differences typically relate to the manner in which the ion bombardment of the target is realized. A schematic diagram of a typical DC sputtering system is shown in the Figure 2.3 [16].

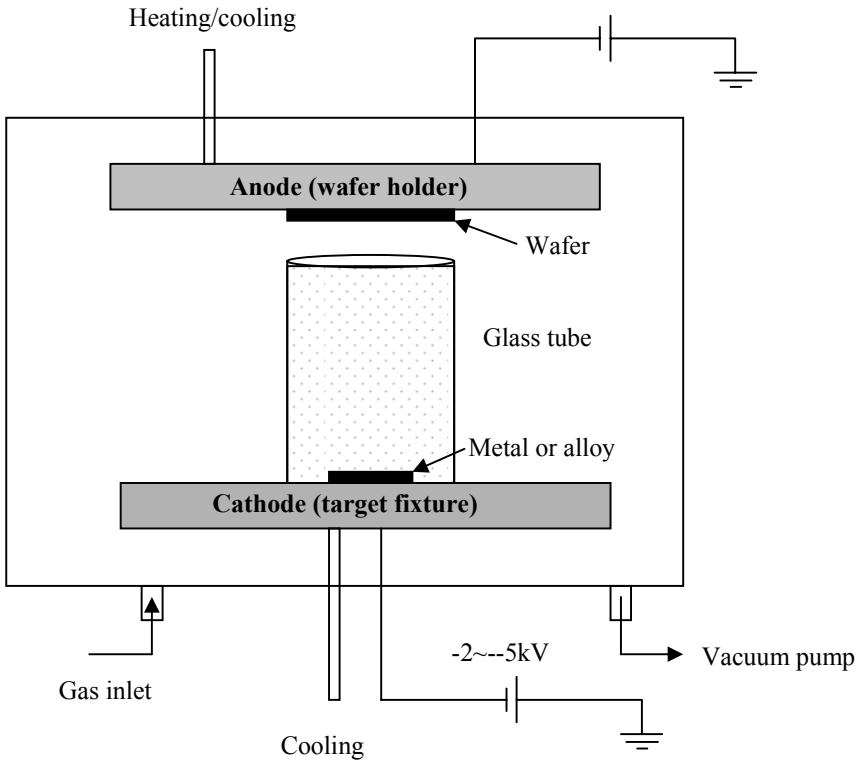


Figure 2.3 Typical DC sputtering system [16]

2.3 SUBSTRATE AND SUBSTRATE METALLIZATION

Ceramic substrates have been successfully used for SiC packaging and typical properties are presented in Table 2.2 [17]. Alumina (Al_2O_3) has been used to package high temperature SiC based amplifiers [5]. These circuits used screen-printed thick film metallization. However, this technology will not provide the current carrying capability required for power applications. Ceramic substrates with thick copper metallization are used for power devices because the thick copper provides both high current capability and high thermal conductivity. Thick copper can be achieved by direct bond copper (DBC), copper electroplating onto an adhesion layer or by reactive brazing a copper foil directly to the ceramic [5]. However, how to overcome the CTE mismatch between the copper (16 ppm/ºC) and the ceramic is a significant challenge.

Table 2.2 High temperature substrate properties [17]

	96% Al_2O_3	AlN	Si_3N_4
Flexural Strength (MPa)	400	345	700
Fracture Toughness (MPa•m1/2)	3.85-3.95	2.79	6.50
Thermal Conductivity (W/m-K@ R.T)	26	140-220	60
Coefficient of thermal expansion (ppm/ºC)	7.4	4.40	2.70

Aluminum nitride (AlN) appears to be an ideal candidate for packaging SiC devices for high temperature applications due to its high thermal conductivity (140-220 $W \bullet m^{-1} \bullet k^{-1}$), a CTE (4.4 ppm/°C) that closely matches that of 4H-SiC (4.2~4.68 ppm/°C)

[18], environmental stability and chemical inertness at high temperature. However, when used in conjunction with thick copper, aluminum nitride is prone to fracture during thermal cycling due to its low flexural strength and poor fracture toughness.

Silicon nitride has an intermediate thermal conductivity, but the highest mechanical strength and fracture toughness. The poorer thermal performance of the silicon nitride substrate can be improved through the use of thick copper metallization. The CTE of Si_3N_4 is lower than that of SiC and AlN.

Although alumina has the lowest thermal conductivity, and intermediate fracture toughness, Al_2O_3 based ceramics are popular as substrates because of their availability, low cost, and good electrical properties. The poorer thermal performance can be improved through the use of thick copper metallization.

Copper metallized ceramic substrates (Si_3N_4, AlN and Al_2O_3) can be supplied with a standard Ni/Au surface finish. Typically 5-6μm Ni is electrolessly plated or electrolytically plated over the copper foil, and then a thin layer of gold (0.1~0.5μm) is plated on top of the Ni to prevent Ni oxidation.

Nickel provides good corrosion protection by creating a physical barrier between the corrosive environment and the underlying copper [19]. For traditional temperature ranges, Ni/Au functions as a good barrier for preventing copper oxidation and diffusion. However, the solubility of Ni into Au and Au into Ni increases with increasing temperature. Furthermore, copper and nickel are soluble in each other, and the copper will continue to diffuse to the surface and oxidize in air.

A schematic diagram of a typical nickel electroplating setup is shown in the Figure 2.4 [19]. The substrate is placed into a solution of nickel salts and connected to an

electrical circuit, forming the cathode of the circuit, while the nickel plate forms the anode. When an electrical current is passed through the circuit, nickel ions in the solution are attracted to the cathode. The cathode releases electrons to neutralize the nickel ions, resulting in a layer of nickel deposited on the cathode [20].

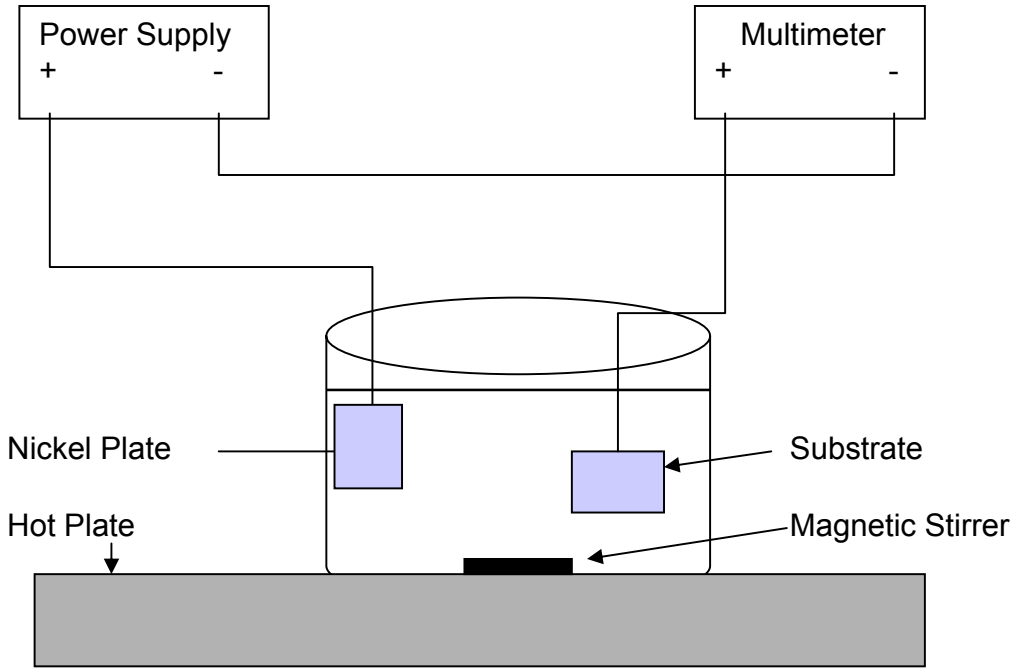


Figure 2.4 Typical nickel electroplating setup [20]

There are three main types of electroplated nickel coatings: bright nickel electroplating (Watts nickel), sulfamate nickel electroplating, and chloride nickel [20]. Watts nickel is deposited from a nickel sulfate bath. Watts nickel normally yields a brighter finish than other methods since the Watts bath contains a grain refiner to improve the quality of the deposit. The brightener in the Watts bath levels the deposit, yielding a smoother surface than that of the underlying part. However, these brighteners

may also lead to problems with soldering and brazing, and this should be considered when selecting a finish for various applications. Sulfamate nickel is deposited from a nickel sulfamate bath, and is the most widely used electrolytic nickel. It is often used as a final plating layer and also as an underlayer for precious metals. Sulfamate nickel is a pure deposit that allows soldering and brazing during later assembly steps. Sulfamate nickel deposits can be much more formable than bright nickel deposits because sulfamate nickel has little to no tensile stress in the deposit and very good ductility. The chloride nickel can be plated thick with low pitting, however, it is sometimes less pure and the mechanical properties of the deposit are not as good as those from the Watts bath [20].

Electroless nickel plating is an autocatalytic process and does not use externally applied electric current to produce the deposit. The electroless process deposits a uniform coating of metal, regardless of the shape of the part or its surface irregularities. It therefore overcomes one of the major drawbacks of electroplating, namely the variation in plating thickness that results from variations in current density caused by the geometry of the plated part and its relationship to the plating anode. An electroless plating solution produces a deposit wherever it contacts a properly prepared surface, without the need for conforming anodes and complicated setup. Since the chemical bath maintains a uniform deposition rate, the deposit thickness can be precisely controlled simply by controlling the immersion time [21].

There are three main types of electroless nickel coatings: nickel-phosphorus, nickel-boron and poly alloys. Nickel-phosphorus is generally used for engineering applications. In the most widely used electroless technique, nickel is deposited by the catalytic reduction of nickel ions with sodium hypophosphite in acid baths at a pH of 4.9

and at a temperature of 88°C. The deposit typically contains 3 to 13 wt% phosphorus, depending on the chemical composition of the solution and the operating conditions. The phosphorus content significantly influences the nickel's chemical and physical properties in both the as-plated and after-heat-treatment conditions. High phosphorus nickel is recommended where superior corrosion resistance is desired. Uses include various components in the electronics industry, oil and gas, printing, aerospace, and the chemical processing industries. The narrow melting range of the deposit makes it suitable for certain welding and brazing applications [21].

One of the drawbacks to electroless phosphorus nickel is the slow speed at which the plated layer is developed. The speed restriction of this technique typically precludes it from being used in continuous plating processes [22].

Recent developments in electroplating chemistry have lead to the introduction of an electroplated phosphorous nickel technique, which not only enhances the deposition rate of the phosphorous nickel alloy, but also allows for the selective placement of this deposit in a continuous plating process [23][24].

2.4 Die Attach

Die attach is the process of attaching the silicon carbide transistor onto the substrate. For high temperature SiC transistor devices, the die attach material must have a melting or decomposition point that is well above the operating temperature in order to provide mechanical attachment, good thermal conductivity, and good electrical conductivity for the device operation. There are four bonding options for the SiC

transistor die attach: conductive adhesive bonding, soldering, brazing, and transient liquid phase bonding.

Conductive adhesive bonding is a material jointing process in which an electrically conductive adhesive is dispensed between two facing surfaces, and cured to produce an adhesive bond. An electrically conductive adhesive is made by incorporating conductive particles such as silver, nickel, or gold into the adhesive formulation. These particles carry electrical current through the adhesive. The most popular filler material is silver due to its moderate cost and superior conductivity [25]. Table 2.3 presents typical conductive compositions and properties [26]. Electrically conductive adhesives are not suitable for use above 250ºC. Electrically conductive adhesives also have higher resistance than solders and brazes, which limits their use in high current applications.

Table 2.3 Conductive adhesive properties [26]

Basic Resin	Filling materials	Configuration of Particles	Glass transition temperature	Operating temperature	Curing conditions
Epoxy	Ag	Flakes	90ºC	-65~150ºC 0	1hr/130ºC
Epoxy	Ag-plated Cu	Flakes	N/A	20~160ºC	30min/125ºC
Epoxy	Ni	other	N/A	-50~150ºC	2hr/65ºC
Silicone	Ag-plated Cu	Flakes/ball	-55ºC	-55~125ºC	168hr/25ºC
Silicone	Ag	Flakes	N/A	-50~200ºC	1hr/150ºC
Polyimide	Ag	Flakes	249ºC	20~250ºC	1hr/140ºC

Soldering is a method to bond the die to the substrate using an alloy of low melting point (solder) below 427°C. These solders are typically lead- and tin-based alloys. The solder can be introduced as a solder paste, or solder preform between the die and the substrate. The assembly is heated until the solder melts and bonds the two

surfaces under a protective atmosphere (forming gas or N_2) [27]. After the solder cools down, a solid connection is established. A controlled temperature profile is required to define the liquidus/solidus transition. A range of commonly used solders is given in Table 2.4 [28]. Soldering is not suitable for the SiC power transistor die attach because all the solder liquidus temperatures are much less than the potential application temperature.

Table 2.4 Some common solder materials for die attach [28]

Alloy	Solidus (°C)	Liquidus (°C)
95% Pb, 5% Sn	310	314
80% Au, 20% Sn	280 (eutectic)	
63% Sn 37% Pb	183 (eutectic)	
65% Sn, 25% Ag, 10% Sn	233	233
95% Sn, 5% Sb	235	240
1% Sn, 97.5% Pb, 1.5% Ag	309	309
75% Pb, 25% In	240	260
50% Pb, 50% In	180	209
62% Sn, 36% Pb, 2% Ag	179 (eutectic)	

Brazing is a bonding process in which the filler metal has a melting point higher than 427ºC but lower than that of the materials being joined. To prevent oxidation, brazing is normally conducted in an inert gas or in a vacuum. At its liquid temperature, the molten filler metal interacts with a thin layer of the base metal, cooling to form an exceptionally strong, sealed joint due to grain structure interaction [29].

In actual practice, most brazing alloys melt at temperatures well above 427ºC, and most solders at temperatures well below 427ºC [30]. For brazing process under 600ºC, the Au-In alloy (81/19 wt%), which has a melting point of 487ºC, is the most commonly

used brazing alloy. Most of brazing alloys based on silver have melting points above 600ºC.

Transient liquid phase (TLP) bonding is a jointing process that has been applied to many metallic systems throughout the ages, and yet it still holds promise as a technique for joining in aerospace and semiconductor applications. The TLP process produces a strong, interface-free joint with no remnant of the bonding agent. A schematic illustration of the process, shown in Figure 2.5 [31], indicates that by placing a thin interlayer of an alloying metal containing a melting point depressant (MPD) between the two pieces of parent metal to be joined and heating the entire assembly, a liquid interlayer is formed. The liquid may form because the melting point of the interlayer has been exceeded, or because reaction with the parent metal results in a low melting liquid alloy. The liquid then fills voids formed by unevenness of the mating surfaces and can sometimes dissolve residual surface contamination. With time the MPD diffuses into the parent metal resulting in isothermal solidification. Upon cooling there remains no trace of the liquid phase, and ideally the joint becomes indistinguishable from other grain boundaries. The formation of a thin liquid interlayer eliminates the need for a high bonding or clamping force. The interlayer can be provided by foils, electroplated, sputter coats, or any other process that deposits a thin film on the surfaces that need to be bonded [32].

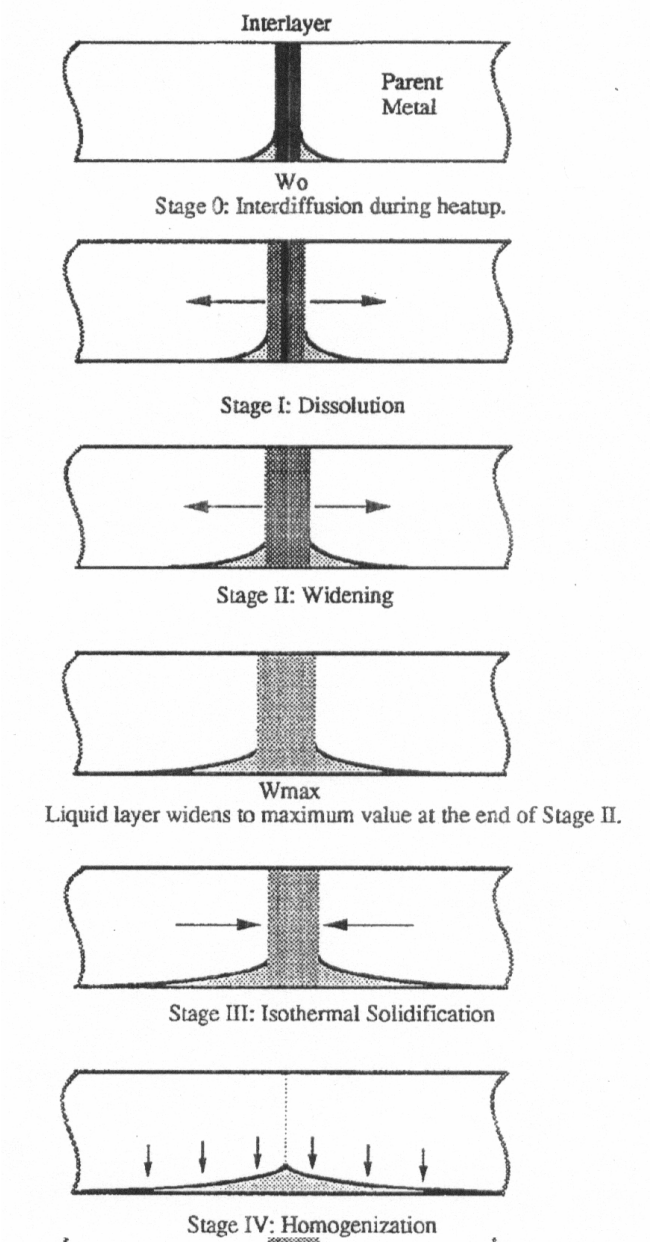


Figure 2.5 Four stages of TLP bonding process [31]

The TLP process is not limited to binary eutectics, but can be applied to any system where the parent metal or alloy will form a relatively low melting temperature

phase and has solubility for the MPD. The concept can also be applied to other systems whereby a chemical or other driving force inherently leads to solid state equilibrium.

In summary, the advantages of transient liquid phase bonding are as follows [33]:

- Transient liquid phase bonding is an isothermal process, so there are minimal thermal stresses formed between the die and substrate, thus avoiding the risk of cracking or fracture.
- During transient liquid phase bonding, oxides on the surface of the substrate are either dissolved by the liquid interlayer or reduced by subjecting the substrate to high-temperature vacuum exposure. Thus, transient liquid phase bonding is normally tolerant to the presence of oxide layers on the surface of the substrate and die, and can be applied to a wider range of materials.
- There are fewer geometrical restrictions on the materials to be bonded because no pressure or scrubbing is required.
- The use of high vacuum environment reduces the amount of air trapped in the joint, therefore fewer or no voids are formed after transient liquid phase bonding.

2.5 Wire Bonding

Wire bonding is the most widely used method for making electrical connections from a semiconductor chip to its package [33]. There are basically two forms of wire bonds, wedge bonds and ball bonds. There are three wire bonding methods that are commonly used: thermocompression, thermosonic, and ultrasonic bonding. Thermocompression bonding requires a high-force on a surface with a high temperature

around 300°C to form a bond [35]. Thermosonic ball bonding combines the thermocompression bonding with the use of ultrasonic vibration to produce strong bonds at low stage temperatures of around 100°C to 240°C. Due to the lower stage temperature of thermosonic ball bonding it has largely replaced thermocompression bonding in the industry. Figure 2.6 shows the thermosonic ball bonding steps [36].

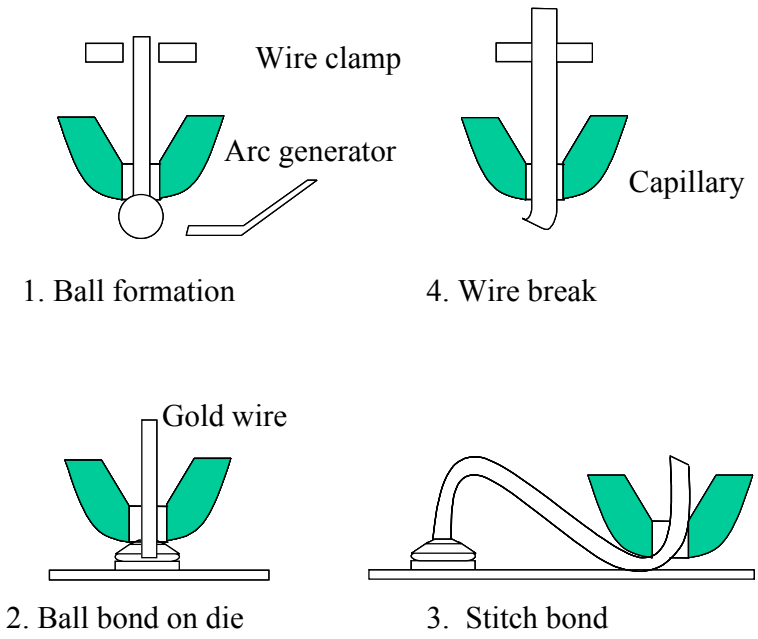


Figure 2.6 Thermosonic bonding of gold wire [36]

Usually, gold wire is used in thermosonic ball bonding because of the ease with which it forms a uniform ball when melted. The gold wire protruding from the capillary is melted by an electric arc to form a ball. This process is called “flame off”. The capillary with the ball lowers to the first bonding site, where pressure, ultrasonic energy and temperature are applied to form the bond. The capillary then rises off the surface with

the wire flowing out to form a loop. Once the loop has been formed, the capillary lowers to the second bond site. Pressure, ultrasonic energy and temperature are again applied to form the second bond, which is generally called the stitch bond. Once the stitch bond is made, the capillary rises to a pre-determined height with the wire clamps open to pull wire through the capillary. The wire clamps are then shut as the capillary continues to move up, breaking the wire behind the stitch bond and thus producing a wire tail used to form the next ball [37].

Thermosonic ball bonding cannot be easily used with aluminum wire because aluminum wire does not form a uniform ball during flame off unless an inert cover gas is used. This led to the development of a second type of wire bonding for aluminum wire, namely ultrasonic wedge bonding. Ultrasonic wedge bonding applies a combination of pressure and ultrasonic vibration of the bonding tool to form a bond. The ultrasonic wedge bonding process starts by feeding aluminum wire through a bond tool. This bond tool then moves to the first bond site, where ultrasonic vibration (20-60 KHz) and pressure is used to form the bond. The bond tool then rises and moves to the second bond site. Once the second bond is made, the bond tool rises and a cutter is applied to the aluminum wire which causes the wire to break behind the second bond. Figure 2.7 shows the steps used in ultrasonic wedge bonding [37]. Ultrasonic wedge bonding is slower than thermosonic ball bonding because the second bond must be directly behind the first bond in order to maintain proper wire alignment through the bonding tool. To accommodate wire bonds that are at different angles to each other, either the bond tool or the substrate must be rotated. The time needed to perform this rotation limits the rate of bond formations.

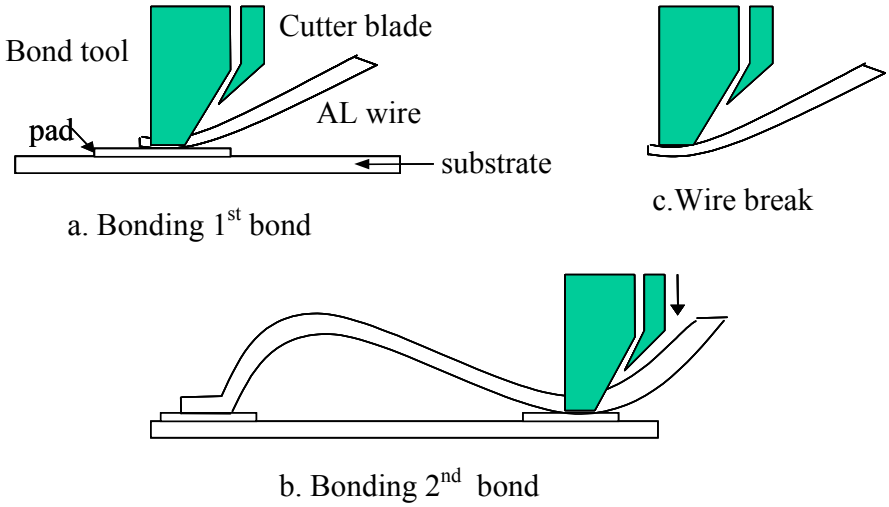
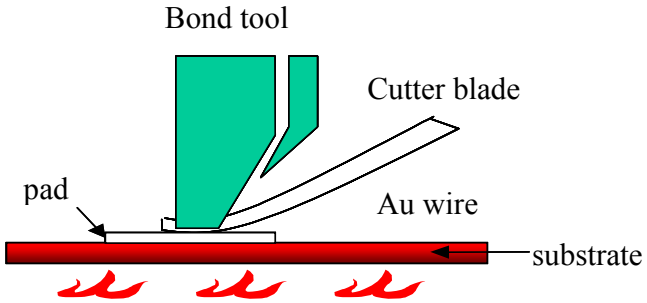


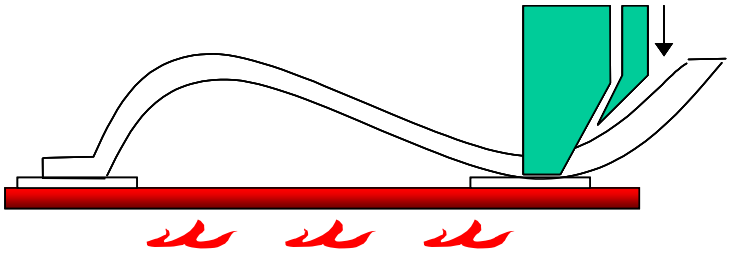
Figure 2.7 Aluminum ultrasonic wedge bonding [37]

Large diameter aluminum wire bonding is used with Si power devices to provide high current carrying capability. However, high temperature annealing increases the grain size in the wire, reducing the wire's strength and fatigue resistance. Also, Al is incompatible with the Au wire bond pads due to intermetallic formation and Kirkendall voiding at high temperatures [5].

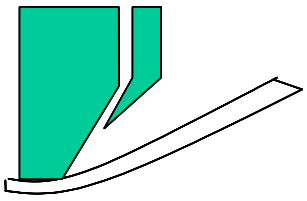
Large diameter gold and platinum wire are alternatives to Al wire for high temperature applications because both have high current capability, excellent corrosion resistance to air and harsh environments at high temperature and no incompatible issues with the Au wire bond pads. Pt also has high mechanical strength at high temperatures. Large diameter Au and Pt ultrasonic wedge bonding requires a heated stage and can appropriately be called thermosonic wedge bonding. Figure 2.8 shows the steps used in thermosonic wedge bonding.



a. Bonding 1st bond



b. Bonding 2nd bond



c. Wire break

Figure 2.8 Gold wire thermosonic wedge bonding

One of the most common ways to determine wire bond strength is destructive pull testing. Destructive pull testing places a hook under the wire between the two bonds and pulls upward along a line centered and perpendicular to the base line running between the bonds until the wire breaks, either at one of the bond sites or in the span itself. Figure 2.9 shows the placement of the hook for pull testing [37].

$$\text{Force (true)} = \frac{F_M}{2 \sin a}$$

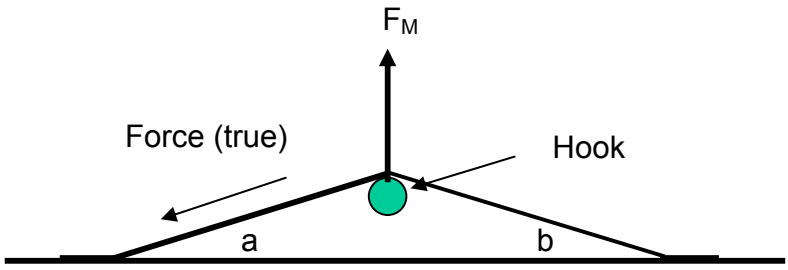


Figure 2.9 Pull test [37]

The force applied to each bond is equal if a = b and has the value:

$$\text{Force (true)} = F_M/2\sin a \qquad (2.1)$$

where Force (true) is the actual force applied to the bond through the wire; F_M is the gage reading; and a is the angle between the baseline and the wire when both angles a and b are equal [37].

Note that raising the height of the loop yields higher breaking load values, as measured by the pull test machine. Thus, angle becomes an important factor that must be recorded if this data is to be used in comparisons. Any changes in loop height or angle will affect the gage reading.

The amount of force required to break the wire in grams-force (g-f) and the failure mode are recorded for each wire tested. The typical failure mode for a wire that has a good bond is in the middle of the loop. The worst type of failure for wire bonding is a bond lift, which occurs when the bond peels off the pad to which it has been bonded

during destructive pull testing. This type of failure indicates that the bond formed was not sufficiently strong. The most common failure for a wire bond occurs at the heel of the bond. Figure 2.10 shows the bond heel definition [38].

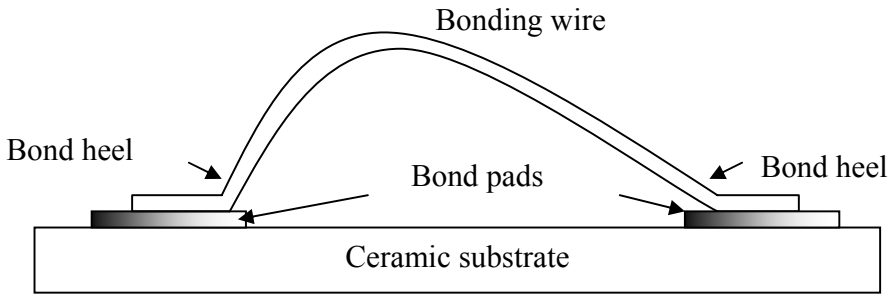


Figure 2.10 Bond heel definition [38]

Wire bond shear testing is routinely used for large diameter aluminum wedge bonds. The shear tester pushes a chisel against the side of a bond until it gives way. The shear height is an important variable, and it must be set high enough to avoid dragging on the substrate surface but low enough to produce a shear load rather than a rolling force. For most large wire bonds, 25μm is a reasonable working height. Figure 2.11 illustrates the shear test process [37].

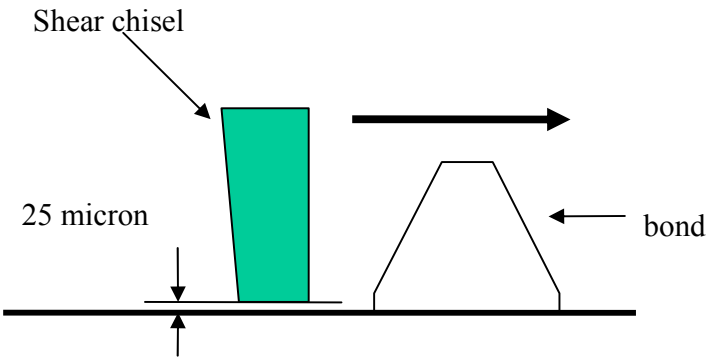


Figure 2.11 Shear test [37]

2.6 POLYIMIDE

Devices operating under high power conditions may also be exposed to high voltages, and as a result high voltage breakdown may occur between adjacent electrical connections and/or between high voltage electrical connections and the surrounding air. To prevent this, an effective dielectric passivation coating must be applied to ensure reliable package operation [39].

Polyimide films are amber in color and highly transparent, being formed by the condensation reactions of aromatic dianhydrides with aliphatic or aromatic diamines. The synthesis includes two steps [40]: the synthesis of the polyamic acid, followed by thermal imidization. The synthesis of Dupont PI2611 polyimide is shown as Figure 2.12. Here, S-Biphenyldianhyride (BPDA) is mixed with a solution of P-phenylenediamine (PPD), generating an intermediate, polyamic acid. The intermediate acid is then heated to produce cyclodehydration in the imidization stage. Interaction between adjacent imide

and benzene rings results in a rigid backbone structure and causes spontaneous molecular orientation during thermal imidization.

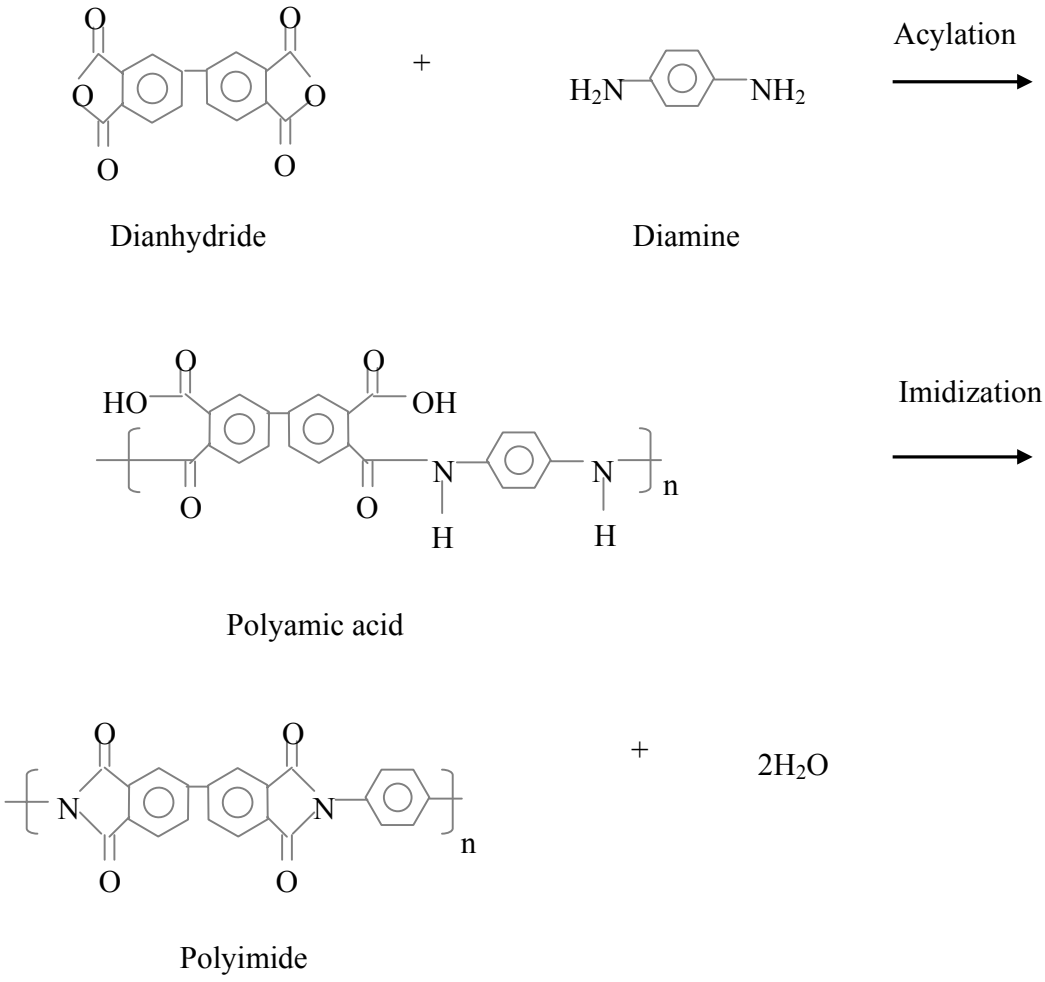


Figure 2.12 Synthesis of polyimide [40]

This kind of polyimide has a rodlike structure with a backbone composed of rigid cyclic elements. This stiff structure exhibits an exceptional combination of high thermal stability (>500°C), a very low lateral CTE (coefficient of thermal expansion) of 3ppm/°C, good mechanical toughness (6.6GPa), good chemical corrosion resistance, excellent

dielectric properties (dielectric constant 2.9 (out of plane)) and relatively low moisture uptake (0.8%) [41] compared to most other organic or polymeric materials. Because of its high degree of ductility and inherently low CTE, PI2611 polyimide can be readily implemented into a variety of microelectronics applications.

In the fabrication of microelectronic devices, polyimide coatings can be applied to the substrate by spin, draw, spray, extrusion, roller, dip and drop coating automatically or manually, depending on the dimensions, the shape of the part or its surface irregularities, and then thermally cured into a smooth, rigid, intractable polymeric film or structural layer. For optimal adhesion to silicon, oxides, and most metals, adhesion promoters are required [42].

CHAPTER 3 SIC DIE ATTACH CHARACTERATION

3.1 TRANSIENT LIQUID PHASE BONDING PROCESS

In this research, AuIn alloy (81/19 wt%) preform (size: 130mil x 130mil) manufactured by Williams Advanced Materials was selected as the interlayer of metal for the transient liquid phase bonding for die attach. In this case, the indium acted as the MPD. Figure 3.1 is the phase diagram for gold-indium [43].

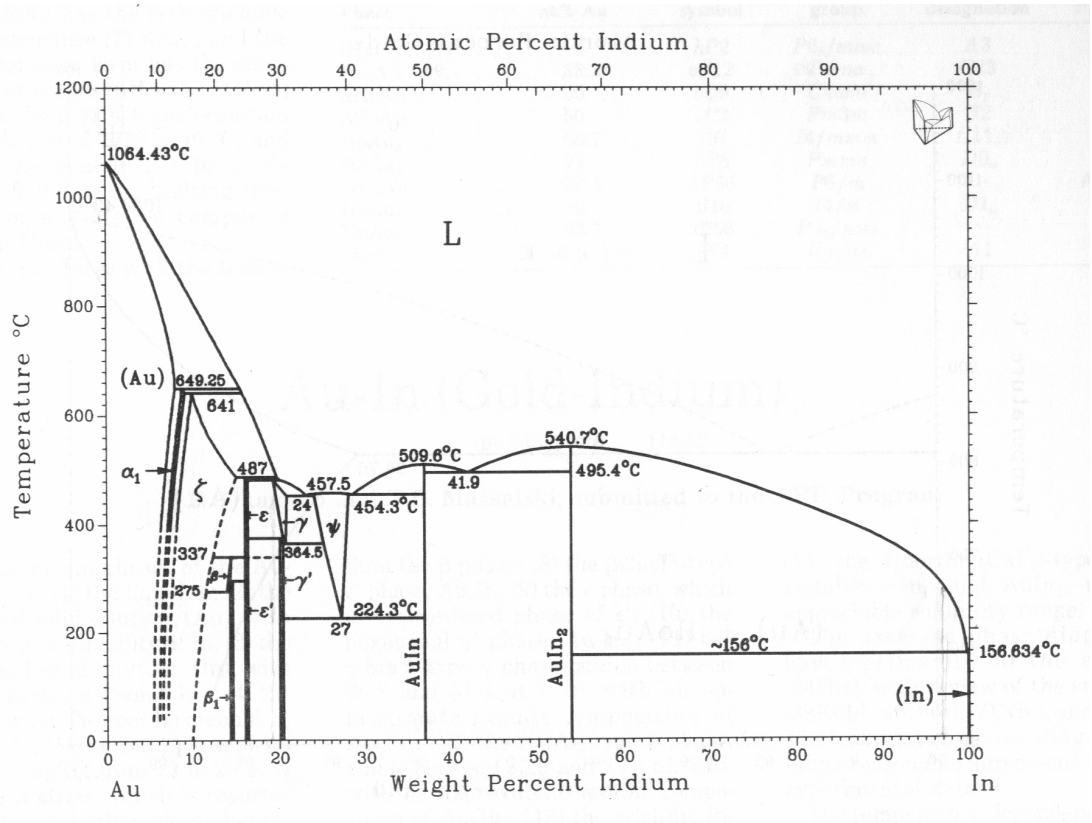


Figure 3.1Gold-Indium phase diagram [43]

From the Au-In phase diagram, if the concentration of indium changes from 19% to less than 12 wt%, the alloy solidus temperature will increase to 550°C. Thick gold on the SiC die backside provided a source of gold to lower the concentration of indium to less than 12 wt% in this work. Figure 3.2 shows the schematic for calculation of the thickness of the Au required on the SiC die.

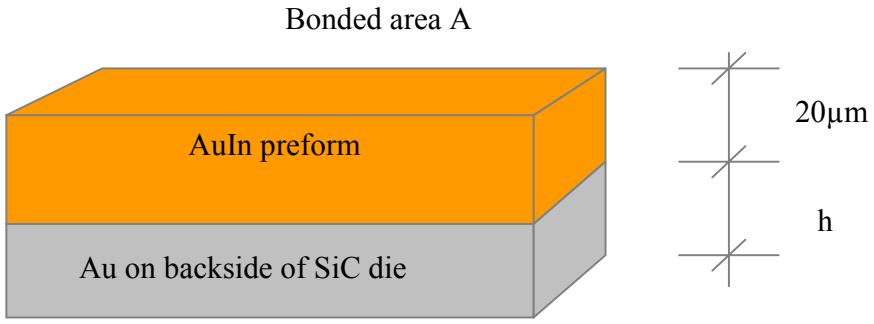


Figure 3.2 Calculation schematic for thickness of added Au

To lower the concentration of indium to 12 wt%, the thickness of the Au layer on the SiC die was calculated from Equation (3.1) to be 9μm. Hence, a thickness of 10μm Au was selected for the SiC die metallization cap layer.

$$W_{In}\% = \frac{\rho_{AuIn} * A * 19\% * 20}{\rho_{AuIn} * A * 28 + \rho_{Au} * A * h} \qquad (3.1)$$

In Equations (3.1):

A : Bonded area

h : Thickness of Au or Ag

ρ_{AuIn} : Density of eutectic AuIn, 14.72 mg/cm^3

ρ_{Au} : Density of Au, 19.3 mg/cm^3

Thick silver was studied as an alternative metal to gold due to its moderate cost, superior conductivity, and high solubility of indium at high temperature. The diffusion coefficient of indium in silver D=0.41 exp (-40630/RT) cm^2/sec [44], and gold in silver D=0.26 exp (–45500/RT) cm^2/sec [45] at 500~720ºC. When the temperature increases above 487°C, the preform melts to form a liquid phase. Indium and gold both diffuse into the silver, but indium diffuses in silver much quicker than gold at high temperature. For example, at the temperature of 510ºC, the diffusion coefficient of indium in silver is about 1.97×10^{-12} cm^2/sec which is much more than that of gold in silver, 5.49×10^{-14} cm^2/sec, resulting in reduction of the concentration of the indium in the liquid phase. Therefore, thick silver on the ceramic substrate side acted as a sink for indium in the second approach to lower the concentration of indium. The second approach differs from the first in that the gold-silver-indium ternary alloys form in the joint due to the indium and gold diffusion into the silver and silver dissolved by the melt. The melting point of the bond joint will depend on the gold-silver-indium ternary alloy composition and structure. However, the thickness of the added silver, the alloy composition and the melting point of the bond joint could not be predicted because there is no Au-Ag-In ternary phase diagram available in this field. In this research, a thickness of 20μm silver was selected as the substrate metallization cap layer.

3.2 THICK GOLD DIE SPECIMEN PREPARATION

In the first approach, the AuIn preform was sandwiched between the SiC die and substrate. The preforms were supplied with dimensions of 3.3mm x 3.3mm x 0.020mm. The properties of AuIn preform include a melting point of of 487°C, density of 14.72 mg/cm^3, thermal coefficient of expansion (CTE) of 14.7 ppm/K at 25ºC, and tensile strength of 33700 psi at 25ºC [47]. Figure 3.3 shows the sandwich structure. This assembly is referred to as the thick Au die-to-thin Au substrate construction.

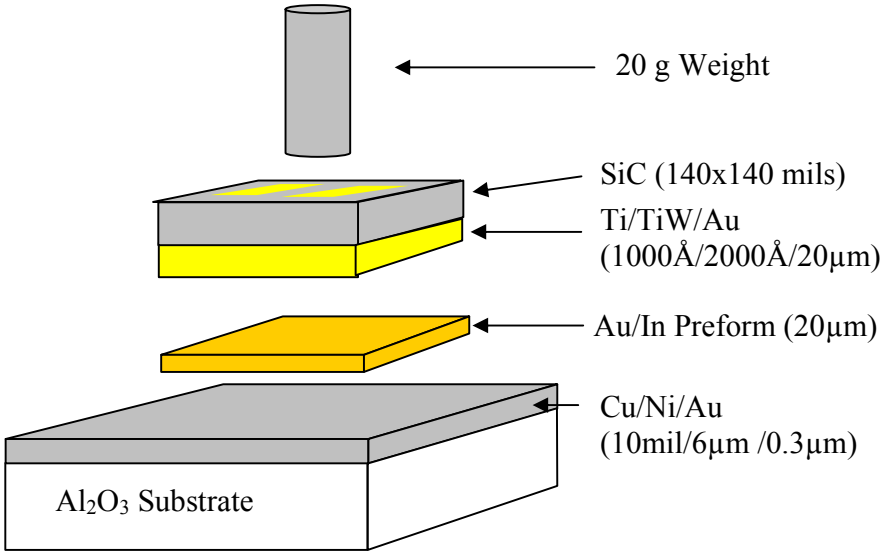


Figure 3.3 Thick Au die TLP bonding sketch

3.2.1 SiC Die Metallization Fabrication

A metallization stack, Ti/TiW/Au (thickness: 1000Å/2000Å/20µm), deposited on an n-type 4H-SiC wafer provided by Cree Inc., was used as the die metallization for the

liquid transient phase bonding process. The SiC wafer metallization fabrication process was as follows:

- Pre-Clean SiC wafer in organic and inorganic solution.
- High vacuum sputter the Ni (thickness < 800 Å) on the SiC wafer.
- Anneal at 900°C for 1 minute in a high vacuum chamber to form Ni_2Si as ohmic contact.
- High vacuum sputter each of the Ti, TiW and Au (2000Å) layers in turn without breaking the vacuum.
- Electroplate Au to a thickness of 20μm.
- Dice the wafer to the experimental size (140x140 mils).

The inclusion of a pure Ti film improves adhesion to the device contacts (Ni_2Si, an ohmic contact), reducing the interfacial oxide layer and improving the step coverage. The TiW (10/90 wt%) film usually consists of columnar grains of tungsten without any free Ti phase [46]. The titanium is in solid solution, with some tungsten atoms distributed at the grain boundaries. The distribution of titanium is important for improving the barrier properties of TiW. The Au film protects the underlying layer TiW from oxidation and serves as a die bonding wettable surface.

3.2.2 Substrate Metallization Fabrication

A thick metallization, Cu/ Ni/ Au (thickness: 250μm/6μm /0.3μm), deposited on 96% Al_2O_3 provided by Stellar Industries Corp was used as the substrate metallization. The substrate metallization fabrication process was as follows:

- Put 10mil Cu foil on Al_2O_3 ceramic, heat to 1065ºC to 1085ºC to form a CuO and Al_2O_3 joint.
- Electroplate 6µm Ni on DBC Cu.
- Immersion plate 0.3µm Au on Ni.
- Dice the substrate to the experimental size (200x200 mils).

The direct bond copper provides high electrical and thermal conductivity, and high mechanical strength due to the strong joint between Cu and Al_2O_3. Nickel acts as the barrier layer to prevent Cu diffusion and oxidation. The Au film protects the underlying layer Ni from oxidation and serves as a die bonding wettable surface.

3.2.3 TLP Process of Thick Gold Die Attach

From the Au-In phase diagram shown in Figure 3.1, when the temperature increases above 487°C, the preform melts to form a liquid phase. Indium in the liquid zone diffuses into the gold on the SiC die and substrate, and the gold on the die and substrate diffuses into the liquid zone, resulting in reduction of the concentration of the indium in the liquid phase. Upon cooling a strong joint is produced. And because of the reduction of the concentration of the indium in the joint, the solidus temperature of the bond joint will be higher than 487°C.

The TLP bonding process was performed in a SST 3150 high vacuum furnace. The components were assembled within a graphite block, which was heated under vacuum by passing a high current through it. Inside the fixture were placed successively the substrate, a graphite slip with cavities for the preform and die, an AuIn preform, and the die. The samples were compressed with a 20g weight.

The bonding profile for the thick Au die is shown in Figure 3.4. It included a 2 minute soak at 420ºC to bake out residual moisture and then 25 minutes ramping from 420ºC to 525ºC, followed by a soak at 525ºC for 15 minutes.

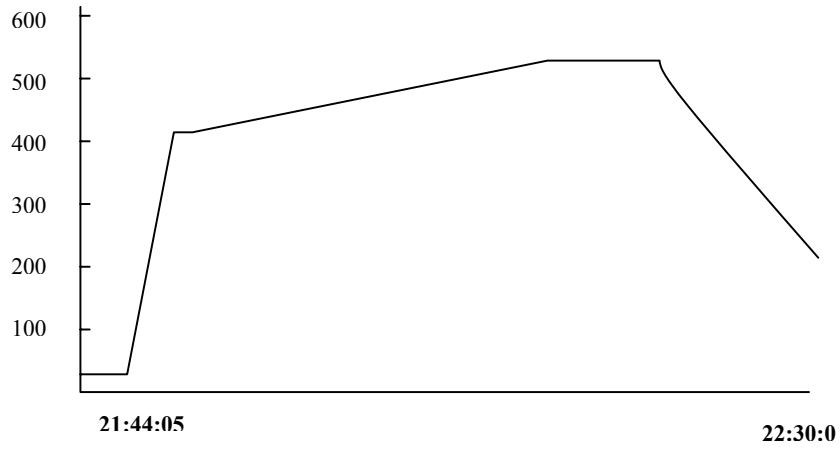


Figure 3.4 Thick Au die TLP bonding profile

Figure 3.5 shows the SEM image with EDX spot analysis for the AuIn as-built sample. Indium diffused into the thick Au layer on the SiC backside, and Ni and Cu from the substrate diffused into AuIn layer. The Ni layer plated over the direct bond copper was not an effective diffusion barrier during the die attach process. Voids were observed in the bond joint due to the hydrogen entrapped in the Au layer on the SiC die during the Au electroplating process. A semi-continuous crack was observed in the bond joint. Cu was detected in the area under the crack, while no Cu was detected in the area above the crack (Figure 3.5); no Cu and no such crack was observed in the bond joint for samples fabricated with thin Au die-to-thick Ag substrates or for thin die-to-Mo tab combinations (Figure 3.12 and Figure 3.19) discussed in section 3.3.3 and section 3.4. Cu, which diffused from the substrate, changed the liquid phase and caused pre-solidification, which is thought to be the reason that caused the crack formation.

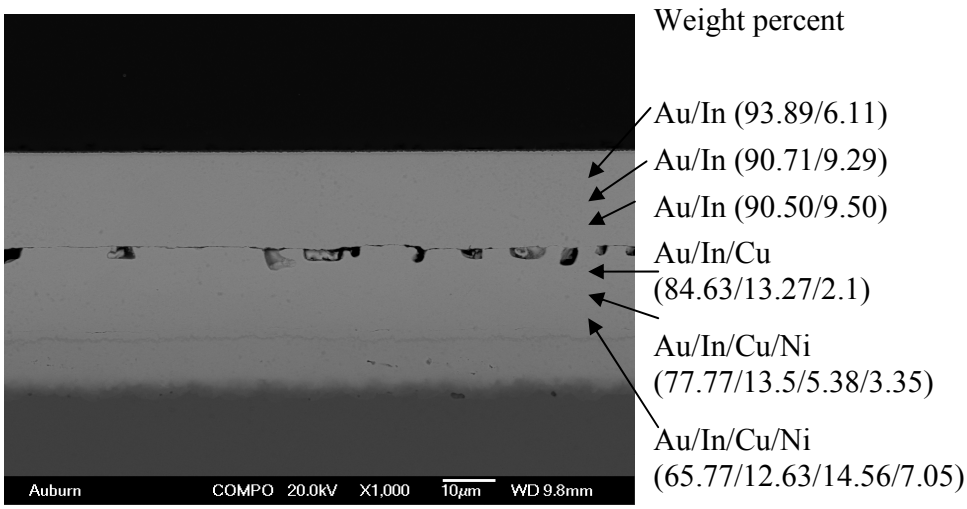


Figure 3.5 EDX spot analysis of the as-built sample (TLP temperature @ 525°C)

A TLP bonding process was conducted at the temperature of 550°C in order to eliminate the pre-solidification. Figure 3.6 shows the SEM image of the die attach sample after 550°C TLP bonding process, no crack was observed in the bond joint.

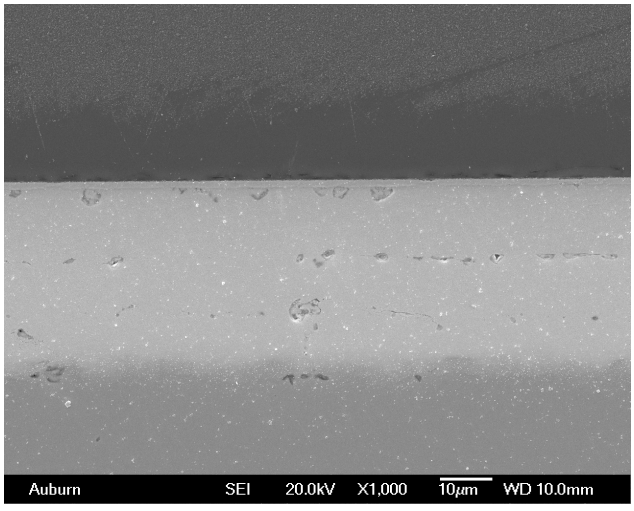


Figure 3.6 SEM image of the as-built sample(TLP temperature @ 550°C)

3.2.4 High Temperature Storage Test

The as-built samples were stored in a Blue-MOV-10C high temperature chamber at 450ºC with ±1ºC accuracy for long-term reliability tests. The storage times were 100, 250, 500, 1000, and 2000 hours. The bond shear strength was used to evaluate the bond reliability. The reliability test results are shown in Table 3.1. The bond shear strength of the thick Au die samples decreased to below 100kg-f after 1000 hours of storage. The shear test limit of the Dage PC2400 is 100kg-f. The sample size was 8.

Table 3.1 Thick Au Die shear strength as a function of aging time (unit: kg-f)

Thick Au Die	0	100hr	250hr	500hr	1000hr	2000hr
Shear strength (kg-f)	> 100	> 100	> 100	> 100	81.5, 87.6, 91.3, 79.2, 85.6, 89.6, 100, 100	11.2, 26.1, 16.8, 12.9, 11, 13.1,12.7, 11.5

Figure 3.7 shows the SEM image with EDX element dot maps for the AuIn sample after 1000 hour aging. Ni and Cu were uniformly distributed in the bond joint. Voids coalesced together along the cracks observed in the as-built sample. It was also observed that the In had segregated to the voids and cracks. Thomas [48] has previously reported the surface enrichment of In in evaporated Au (98%) – In (2%) thin films at room temperature. The voids and cracks create internal free surfaces for In segregation. The cracks and the segregation of the indium are thought to be the cause of the degradation in shear strength with aging at 450^{o}C.

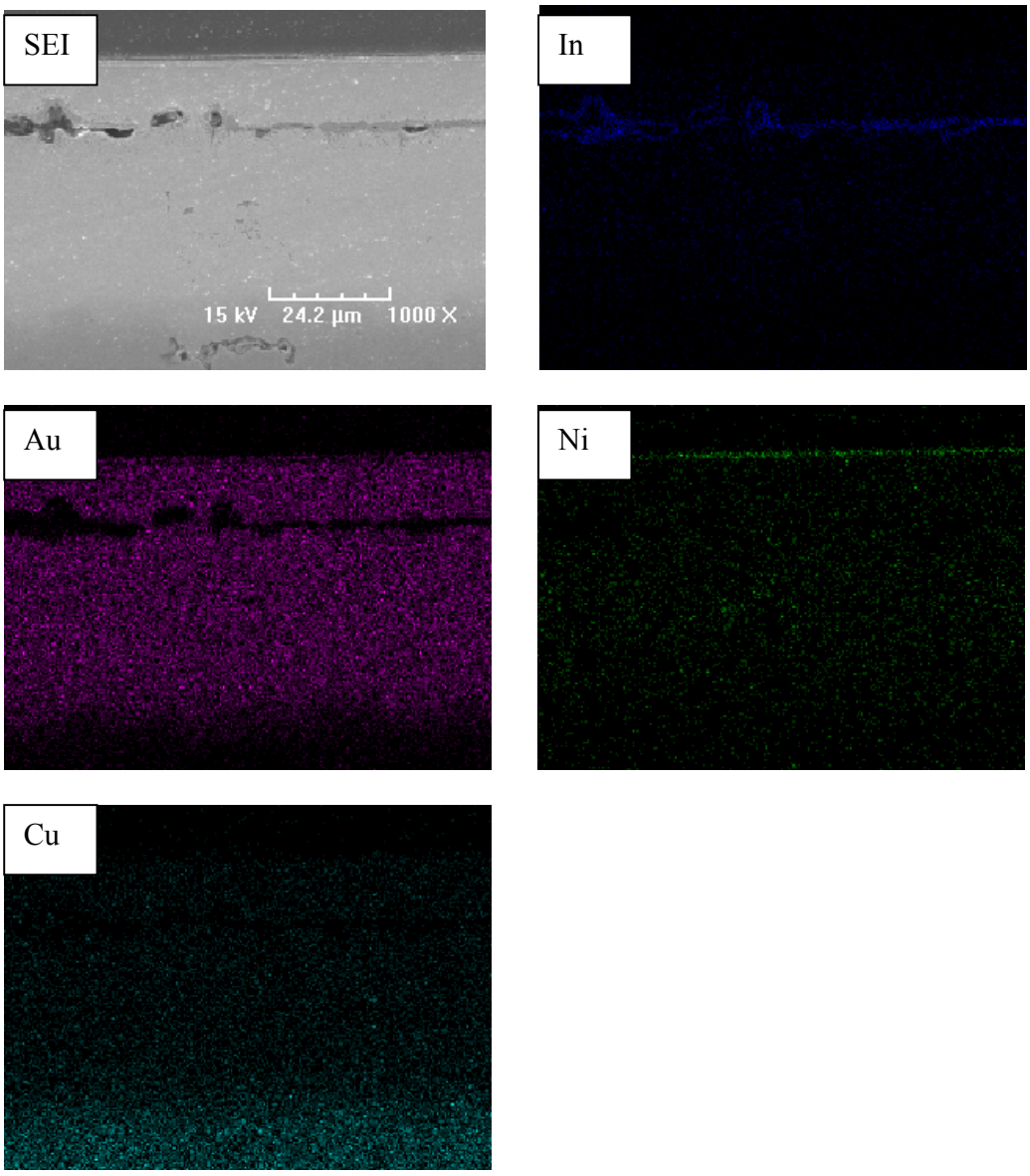


Figure 3.7 EDX element dot maps of the AuIn sample after 1000 hour aging

3.3 THICK SILVER SUBSTRATE SPECIMEN PREPARATION

3.3.1 SiC Die Metallization Fabrication

In the second approach, a metallization stack, Ti/TiW/Au (thickness: 1000Å/2000Å/3μm), deposited on a n-type 4H-SiC wafer provided by Cree Inc., was used as the die metallization for the liquid transient phase bonding process. The SiC wafer metallization processing was almost same as for the thick Au die. The only difference from the thick Au die is that the thickness of Au was electroplated to 3μm, not 20μm.

3.2.2 Substrate Metallization Fabrication

A thick metallization, Cu/ Ni/ Au (thickness: 250μm/6μm /0.3μm), deposited on 96% Al_2O_3 provided by Stellar Industries Corp, followed by 20μm silver electroplated at Auburn University was used as the substrate metallization. The substrate metallization processing was as follows:

- Put 10mil Cu foil (1x1 inch) on Al_2O_3 ceramic (1x1 inch), heat to 1065°C to 1085°C to form a CuO and Al_2O_3 joint.
- Electroplate 6μm Ni on DBC Cu.
- Immersion plate 0.3μm Au on Ni.
- Electroplate Ag to a thickness of 20μm.
- Dice the substrate to the experimental size (200x200 mils).

The silver electroplating setup used is shown in Figure 3.8 [49]. Silver 1025, supplied by Technic Inc., was used as the silver electroplating solution. A silver bar was connected to the anode and the substrate to be plated was connected to the cathode. A multimeter was connected in series with the circuit to monitor the current flowing through the solution. After cleaning the substrate with TSC 1501, TAS-1, a blend of dry acid salts, was used to pickle the metals prior to electroplating in order to produce a cleaner, smut free and active surface with better adhesion and a more uniform metal coating. Technic silver strike, an acid silver strike, was deposited prior to the Silver 1025 deposition to ensure excellent adhesion on the base metal. The TAS-1 and Technic Silver strike solutions were both supplied by Technic Inc.

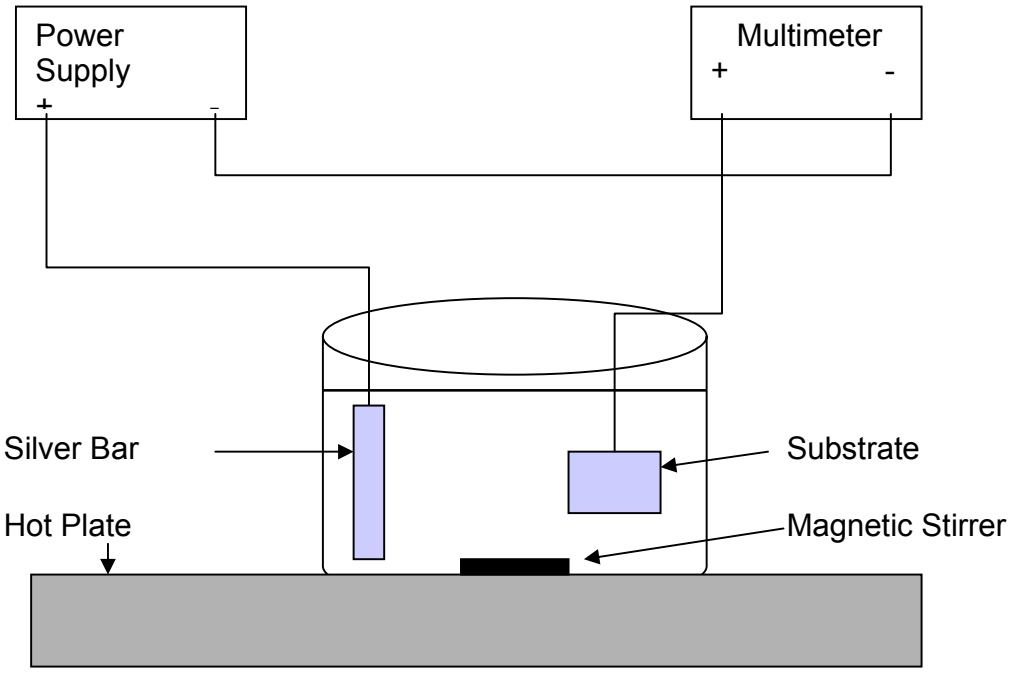


Figure 3.8 Silver electroplating setup [49]

The details of the silver electroplating process were as follows:

- Pre-clean in TSC 1501 formulated soak cleaner for two minutes at 65°C to remove grease and oil.
- Rinse substrate by DI water.
- Soak in TAS-1 for two minutes at room temperature.
- Rinse substrate by DI water.
- Electroplate the substrate in Technic Silver strike solution for 1 minute at room temperature and 1 volt potential.
- Rinse substrate by DI water.
- Electroplate the wafer in Silver 1025 solution at room temperature, current = area of substrate (ft^2) x 10 A/ft^2. The plating time depends on the Ag thickness required. Normally, the plating rate was about 1μm per minute. Frequent measurement was needed for accurate thickness control.
- Rinse substrate by DI water and dry by N_2.
- Dice the substrate to the experimental size (200mil x 200mil).

3.3.3 TLP Process of Thin Gold Die Attach on Thick Silver Substrate

The TLP bonding process was performed in a SST 3150 high vacuum furnace. The components were assembled within a graphite block, which was heated under vacuum by passing a high current through it. Inside the fixture were placed successively the substrate, a graphite slip with cavities for the preform and die, an AuIn preform, and the die. The samples were compressed with a 20g weight. The AuIn preform was

sandwiched between the SiC die and substrate. Figure 3.9 shows the sandwich structure. This assembly is referred to as the thin Au die-to-thick Ag substrate construction.

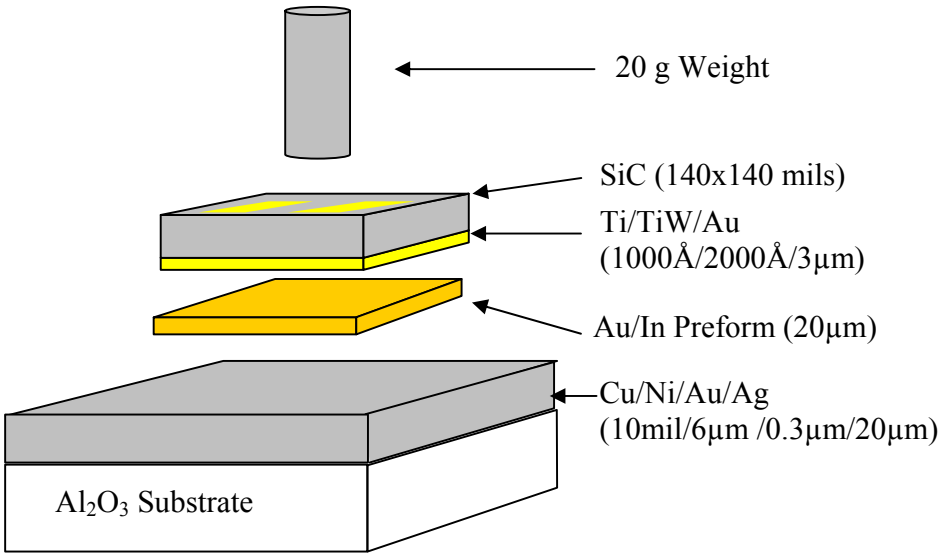


Figure 3.9 Thin Au die TLP bonding sketch

The bonding profile for the thin Au die is shown in Figure 3.10. It included a 2 minute soak at 420ºC to bake out residual moisture and then 25 minutes ramping from 420ºC to 510ºC, followed by a soak at 510ºC for 15 minutes.

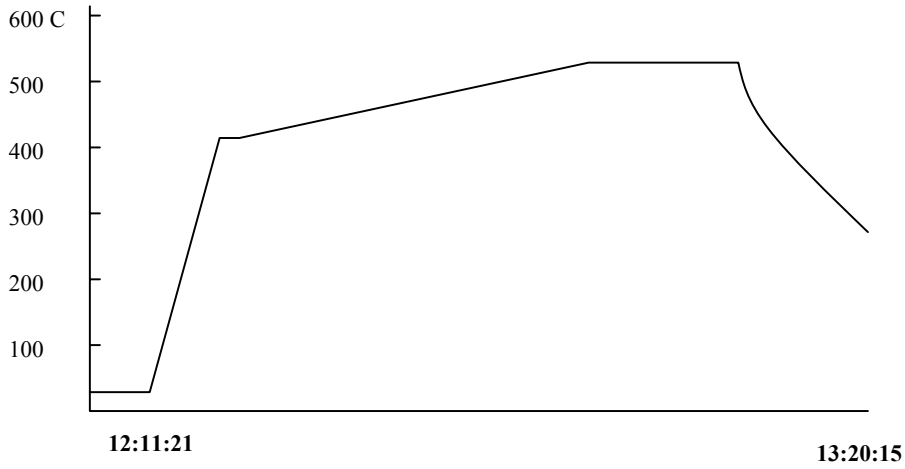


Figure 3.10 Thin Au die TLP bonding profile

An optical image of an as-built thin gold die sample is shown in Figure 3.11. The bond shear strength was used to monitor the bond joint quality using a Dage PC 2400 tester (equipment capability up to 100kg). The average as-built sample die shear strength was over 100kg-f. The sample size was 8.

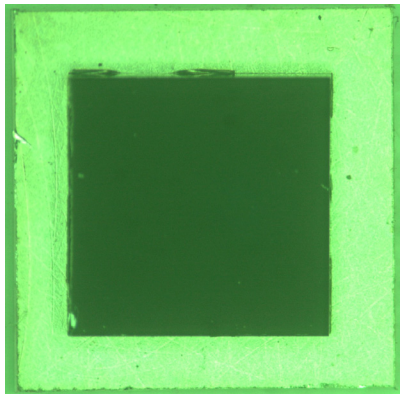


Figure 3.11 X-ray picture of as-brazed thin gold die sample

Figure 3.12 shows the EDX element dot maps for the AuIn as-built sample. Low level voids occurred in the bond joint. Ni and Cu did not diffuse into the AuIn layer. Because the silver and indium signals lie close together in EDX element analysis, the silver most likely dwarfed the indium signal, so there is no In dot map in Figure 3.12. One as-built sample was fixed on a heated stage and heated to over 540°C, then tweezers were used in an attempt to push the die off the substrate horizontally for 30 seconds. The die did not move, providing evidence that the In diffused into the silver, reducing the concentration of In in the AuIn layer.

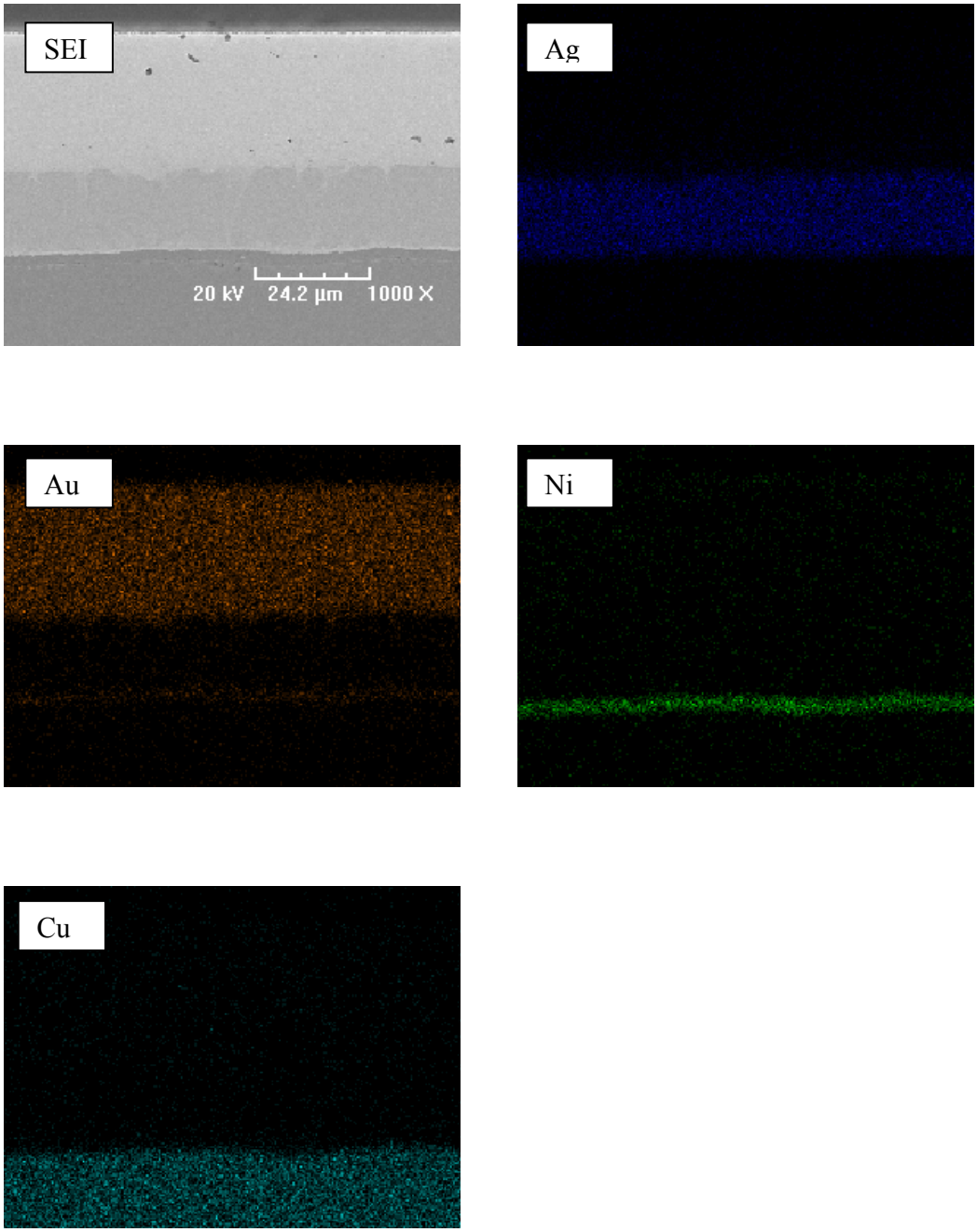


Figure 3.12 EDX element dot maps for as-built thin Au die sample

3.3.4 High Temperature Storage Test

The as-built samples were stored in a Blue-MOV-10C high temperature chamber at 450ºC with ±1ºC accuracy for long-term reliability tests. The storage times were 100, 250, 500, 1000, and 2000 hours. The bond shear strength was used to evaluate the bond reliability. The thick Ag substrate samples were all over 100kg-f after 2000 hours of storage. Figure 3.13 shows the EDX element dot maps for the AuIn after 2000 hours of aging. There were few voids and no crack in the bond joint. Ni and Cu diffused into the bond joint. It is noticed that there is some overlap between the In and Ag, which the instrument may not be able to totally deconvolute. So there was no In dot map in Figure 3.13.

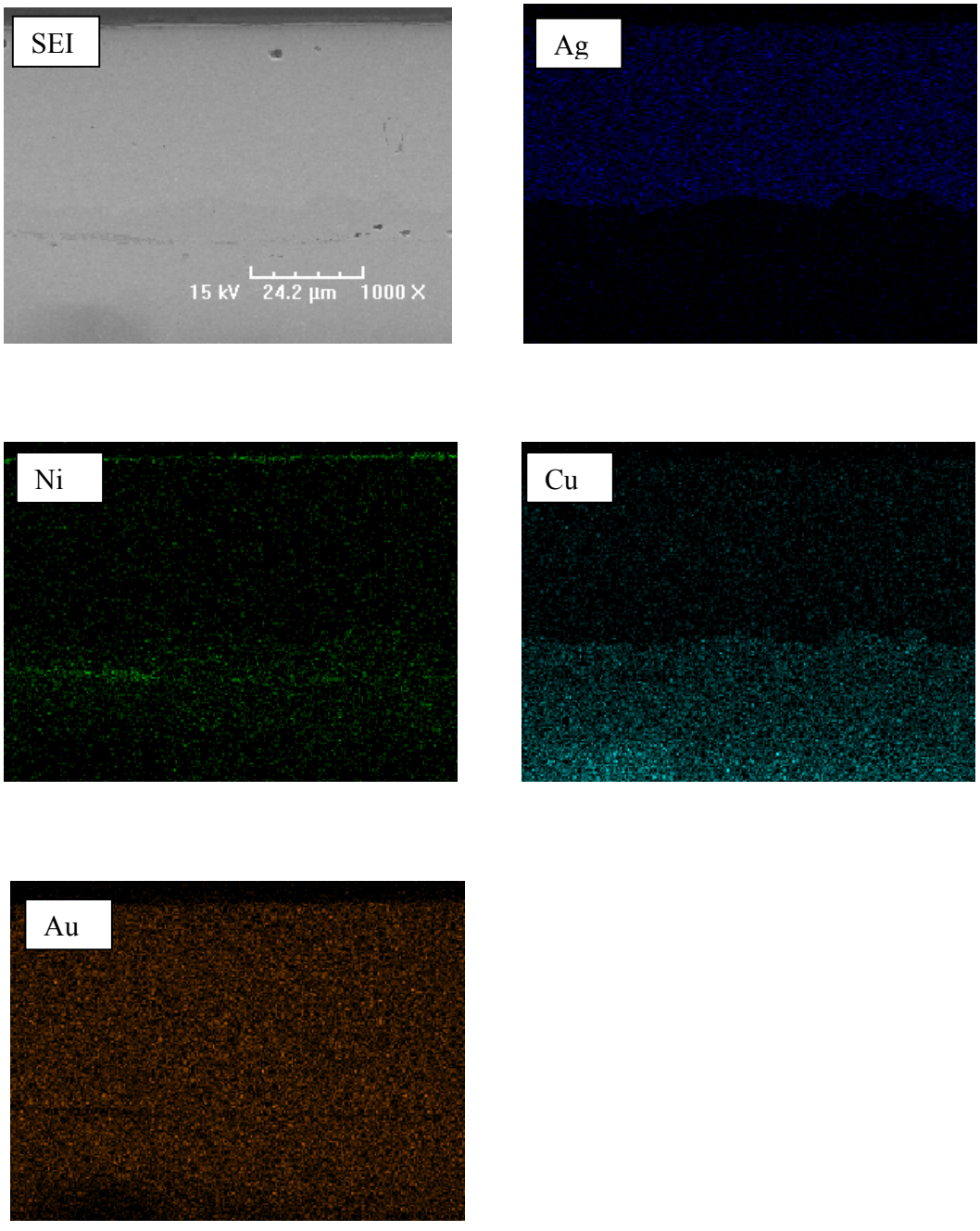


Figure 3.13 EDX element dot maps for thin Au die sample after 2000 hour aging

3.3.5 Thermal Cycling Test

Thermal cycling tests were performed to determine the ability of the thin Au SiC die on thick Ag substrate package to withstand cyclic exposures to high and low temperature extremes. The thermal cycle profile consisted of 20 minutes ramp from 35°C to 400°C, then soak for 10 minutes, followed by 20 minutes cool down from 400°C to 35°C, as shown in Figure 3.14. A die shear test was used to evaluate the die shear strength and a cross-section sample was subjected to SEM/EDX analysis to determine if any cracks developed during the test.

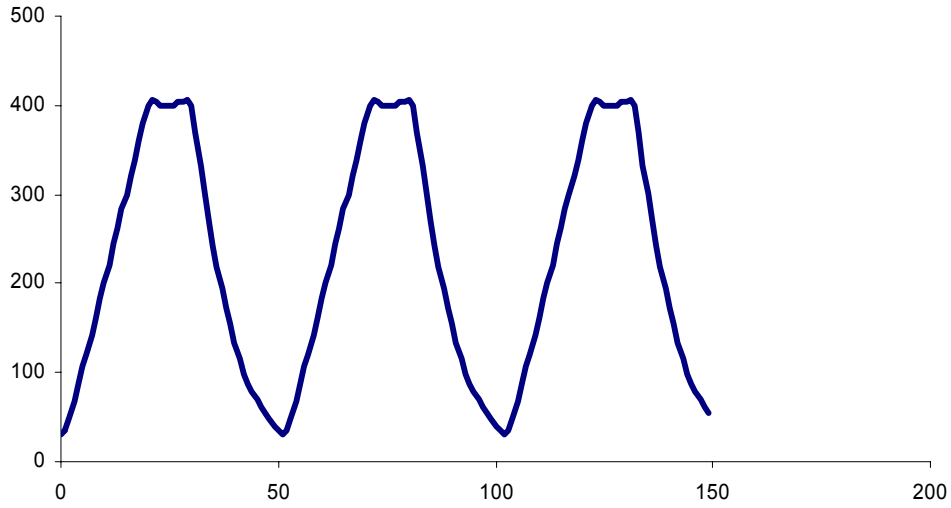
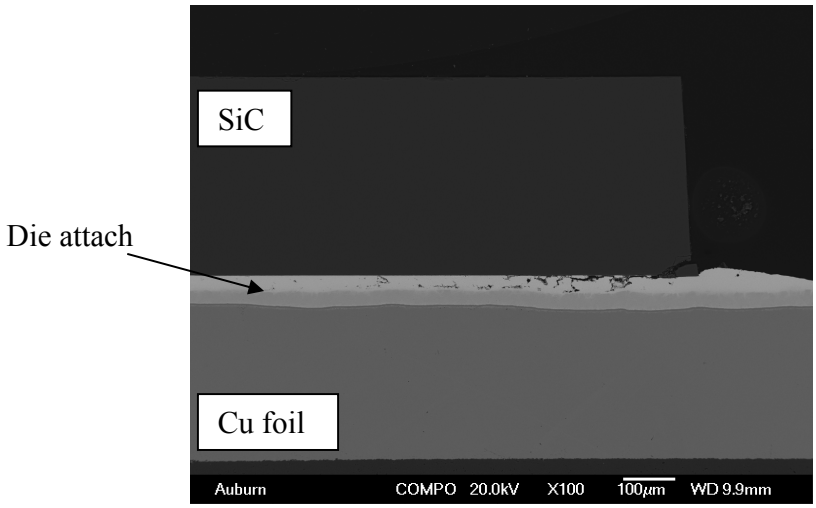


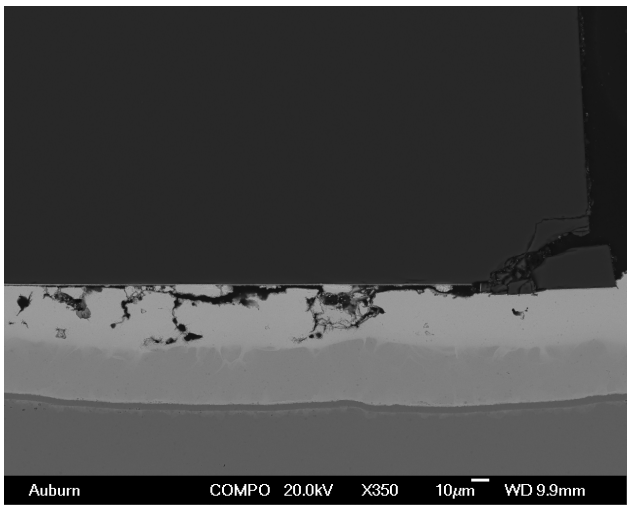
Figure 3.14 Thermal cycle test profile

The average die shear strength was over 100 kg-f after 120 cycles and dropped to around 20 kg-f after 300 cycles. Figure 3.15 and Figure 3.16 show the cross section picture and the EDX element dot maps for the sample after 120 cycles. Cracks occurred at the SiC edge and propagated into the bond joint. It was caused by the stress induced by CTE mismatch between SiC and Al_2O_3 substrate. Figure 3.17 shows the cross-section

picture for the sample after 300 cycles. The crack propagated through the bond joint. The Al_2O_3 substrate fractured during the thermal cycle test as a result of the CTE mismatch induced stress between the Cu foil and Al_2O_3 substrate. Indium segregation was observed in the crack for the samples after 120 and 300 cycles.



(a) Cross-section picture 100X



(b) Cross-section picture 350X

Figure 3.15 Cross-section picture for thin Au die on thick Ag sample after 120 cycles

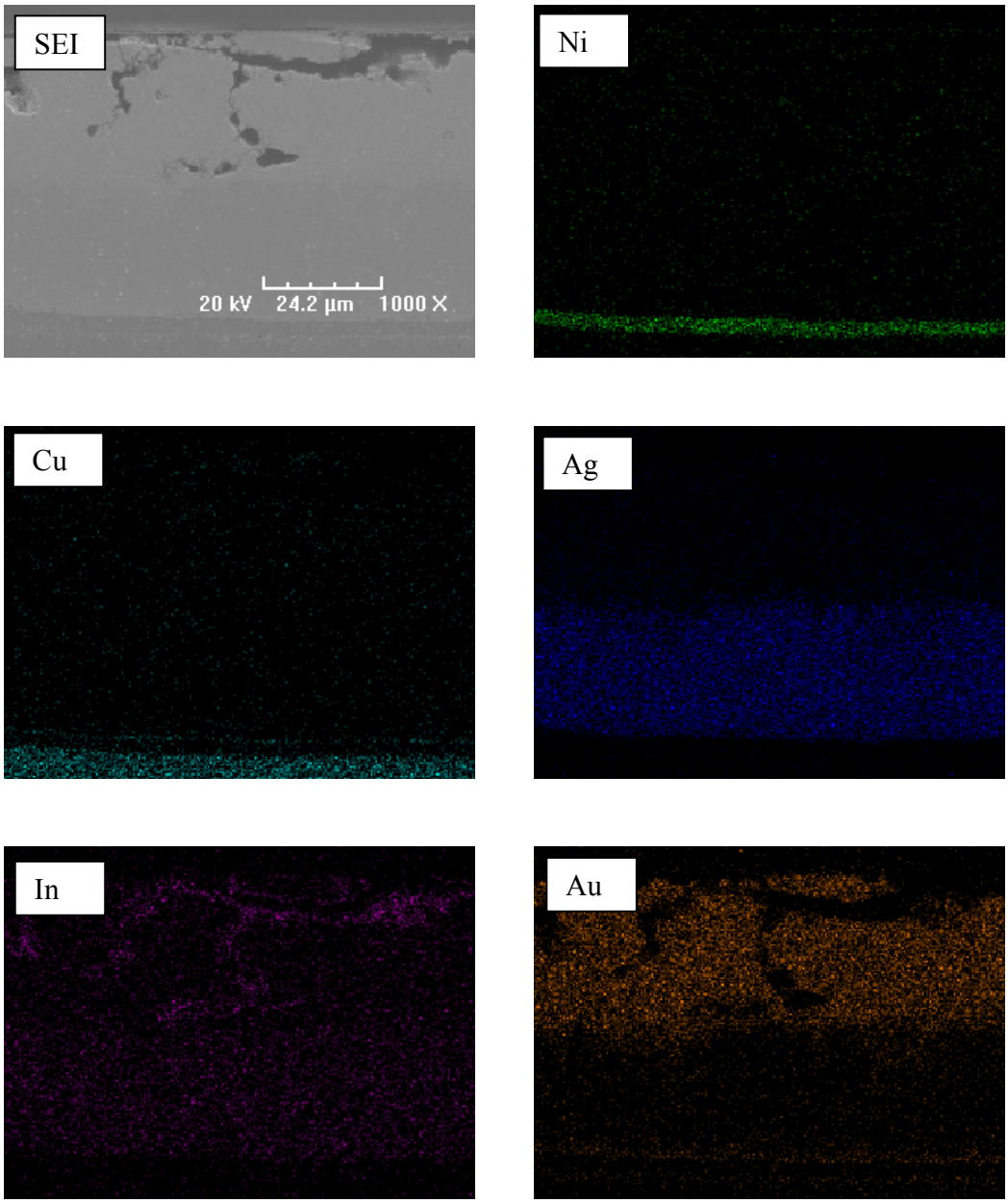
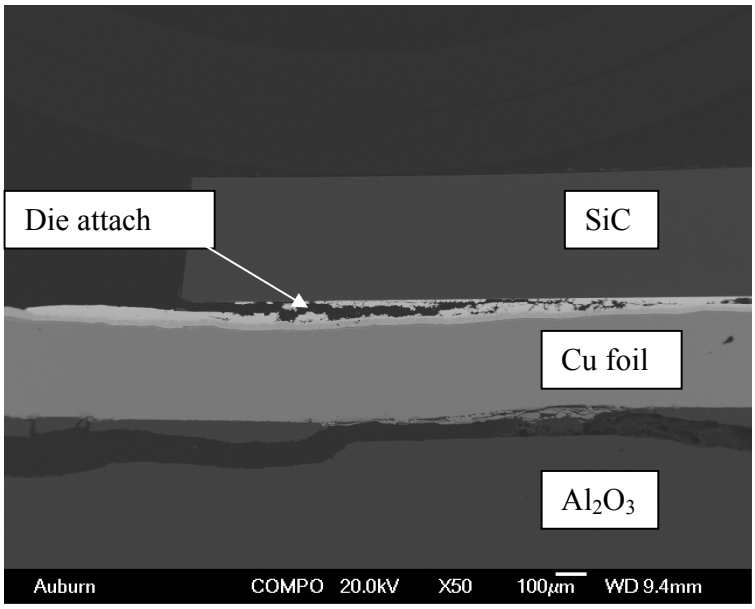
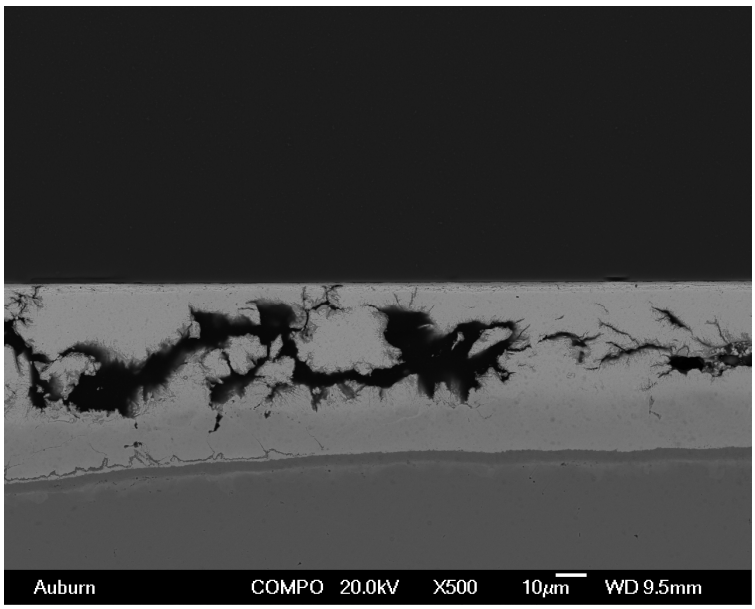


Figure 3.16 EDX element dot maps for thin Au die on thick Ag sample after 120 cycles



(a) Cross-section picture 50X



(b) Cross-section picture 500X

Figure 3.17 Cross-section picture of thin Au die on thick Ag sample after 300 cycles

3.4 THERMAL CYCLING TESTS OF THIN AU DIE BONDING ON MO TAB

In the experiments described in section 3.3.5, the Al_2O_3 substrate fractured during the thermal cycle test as a result of the CTE mismatch induced stress between the Cu foil and Al_2O_3 substrate after 300 cycles. To eliminate this failure mode, a molybdenum tab electroplated with 12μm of Au, provided by Williams Advanced Materials, was used as the substrate. A metallization stack, Ti/TiW/Au (thickness: 1000Å/2000Å/3μm), deposited on a n-type 4H-SiC wafer provided by Cree Inc., was used as the die metallization. The AuIn preform was sandwiched between the SiC die and Mo tab to perform the liquid transient phase bonding process. Figure 3.17 shows the sandwich structure. This assembly is referred to as the thin Au die-to-Mo tab construction.

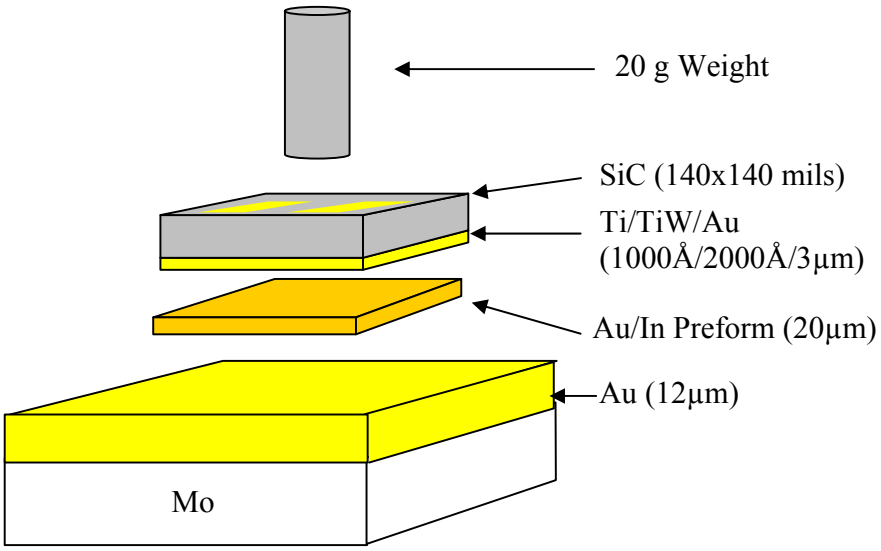


Figure 3.18 Thin Au die bonding on Mo tab sketch

The SEM image for the as-built sample of the thin Au die bonded on the Mo tab is shown in Figure 3.19. There was no crack in the bond joint, but voids still occurred,

mostly, in the original Au layer. The voids could be caused by hydrogen entrapped in the Au layer during the Au electroplating process. Figure 3.20 shows that the Mo tab blistered when exposed to the TLP process without a AuIn preform and SiC die, indicating a problem with the as-plated Mo tabs.

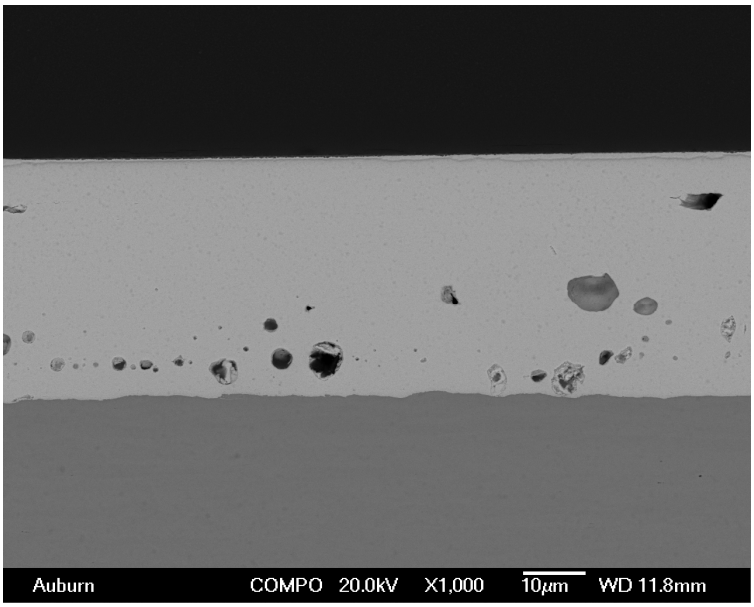
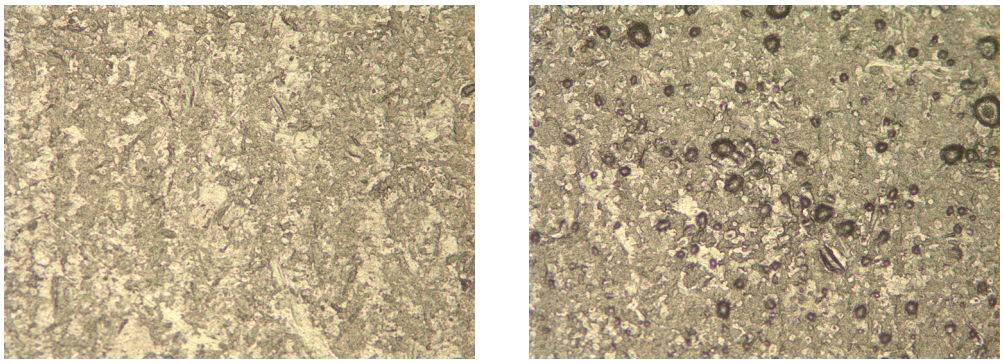


Figure 3.19 SEM image for as-built sample of thin Au die bonding on Mo tab



(a) Before TLP (b) After TLP

Figure 3.20 Bare Mo tab before and after TLP process

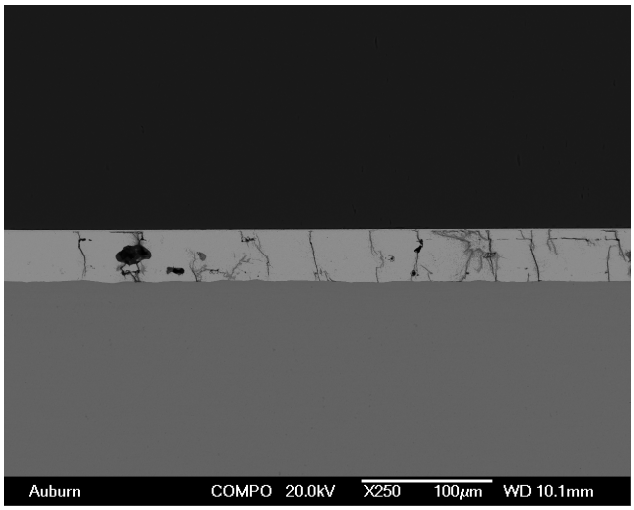
Thermal cycling tests were performed to determine the reliability of the structure. The thermal cycle profile was same as shown in Figure 3.14.

The samples subjected to thermal cycling were tested after 120, 300, 600, 1200, 2400, and 2880 cycles with a group sample size of 7. A die shear test was used to evaluate the die shear strength and a cross-section sample was subjected to SEM/EDX analysis to determine if any cracks developed during the test. Table 3.2 presents the die shear strength after each thermal cycle test. After 2400 cycles, the average die shear strength dropped from over 100 kg-f to 67 kg-f, and the die shear strength was around 1-2 kg-f after 2880 cycles. The shear test limit of the Dage PC2400 is 100kg-f.

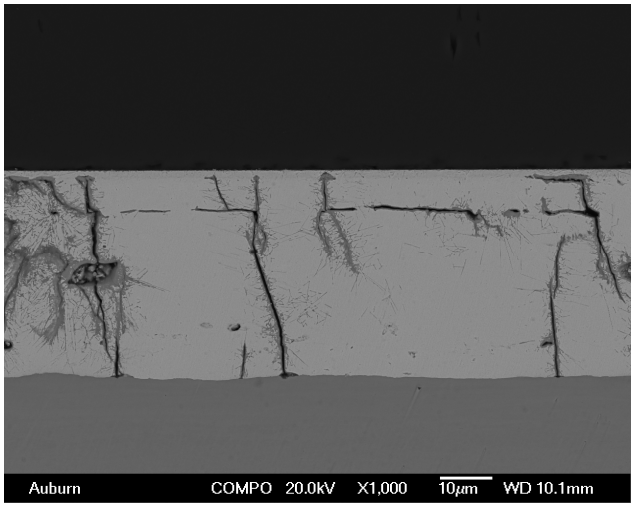
Table 3.2 Die shear strength (unit: kg-f) as a function of thermal cycling numbers3

	0	120 cycles	300 cycles	600 cycles	1200 cycles	2400 cycles	2880 cycles
Au die on Mo	> 100	> 100	> 100	> 100	> 100	88, 72, 79, 86, 70, 34, 41	1-2 kg

Figure 3.21 and Figure 3.22 show the cross section picture and the EDX element dot maps for the sample after 120 cycles. Vertical cracks were observed in the bond joint. Indium segregation was observed in the crack.



(a) Cross-section picture of 250X



(b) Cross-section picture of 1000X

Figure 3.21 Cross-section of sample after 120 cycles

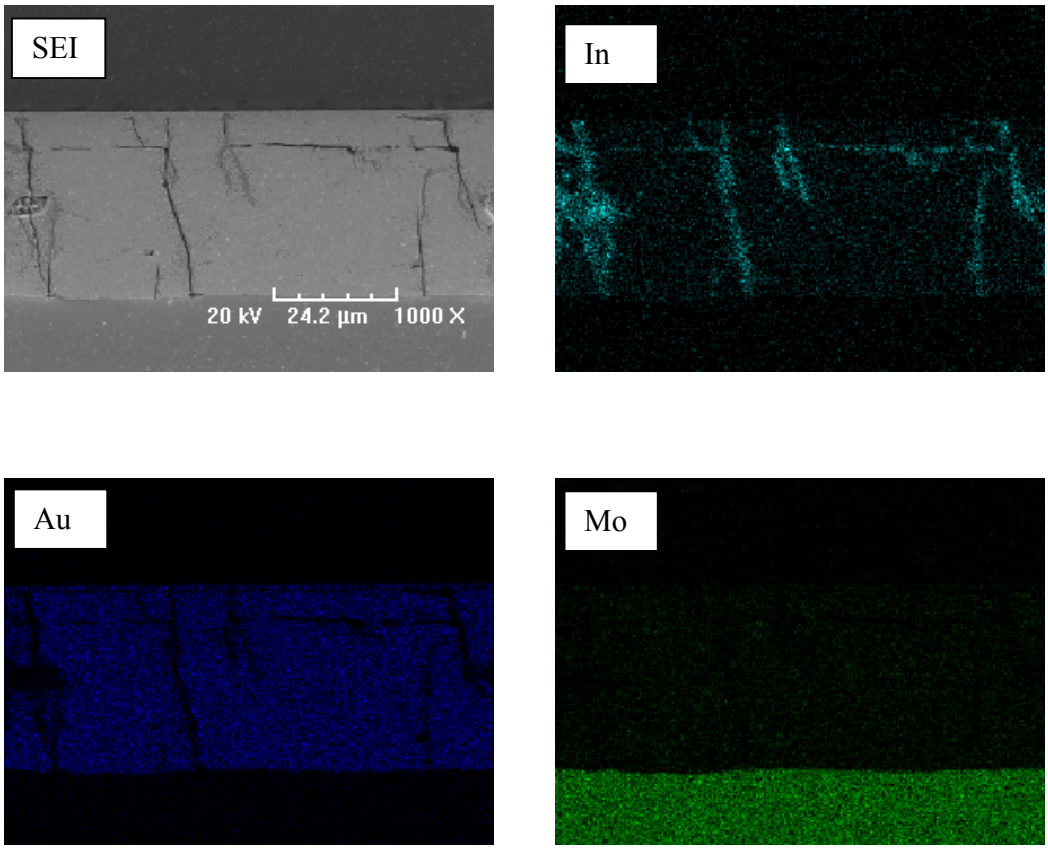


Figure 3.22 EDX element dot maps for sample after 120 cycles

The CTE of the Mo is 4.5ppm/°C, and that of 4H-SiC is about 4.2-4.68ppm/°C, but the CTE of the Au-In is significantly higher. There is almost no CTE mismatch between the Mo and SiC die. Figure 3.23 shows the die attach thermal expansion in the TLP bonding process. At the soak temperature of 525°C, the preform melted and the die was bonded to the Mo tab by the TLP bonding process. Once the bond joint solidification was complete, the length of the AuIn was equal to that of the SiC and Mo. At this stage, there was minimum stress between the SiC and AuIn, and between the Mo and AuIn.

When the package cooled down to room temperature, the AuIn should shrink faster than the SiC and Mo. If there were no bonding restriction, the length of the AuIn would be shorter than the SiC and Mo upon cooling. Because the bond joint was very strong, the AuIn was constrained to the same length as the SiC and Mo, leading to a high tensile stress in the die attach layer. The stress reached the maximum strength at room temperature. When this package was subjected to thermal cycling, the stress decreased during the heating up period, and increased during the cooling down period. The cyclic tensile stress caused the vertical cracks.

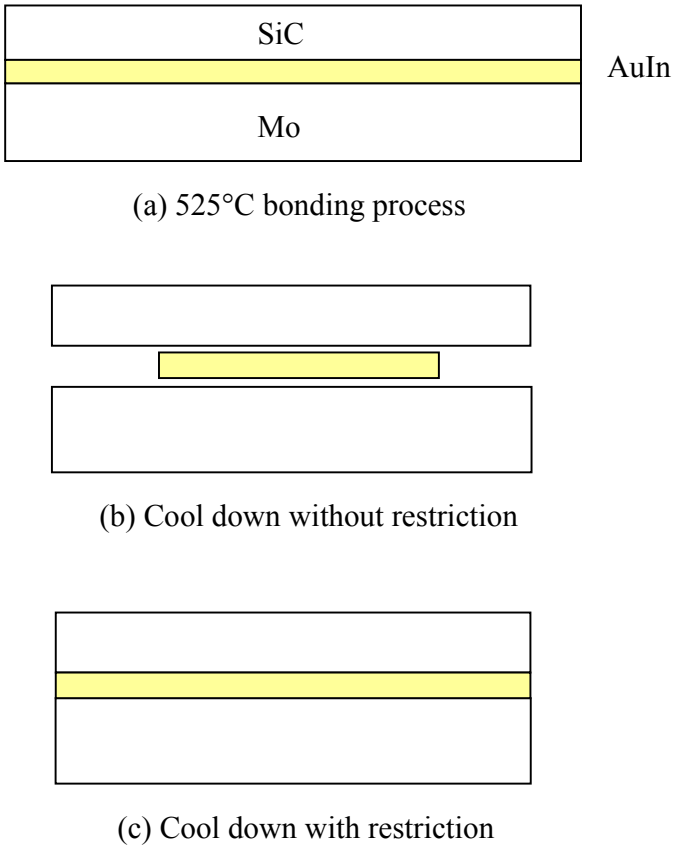


Figure 3.23 Die attach thermal expansion in the TLP bonding process

Figure 3.24 shows the SEM and EDS analysis after 1200 thermal cycles. The images are similar to those after 120 cycles, but some horizontal cracks are forming.

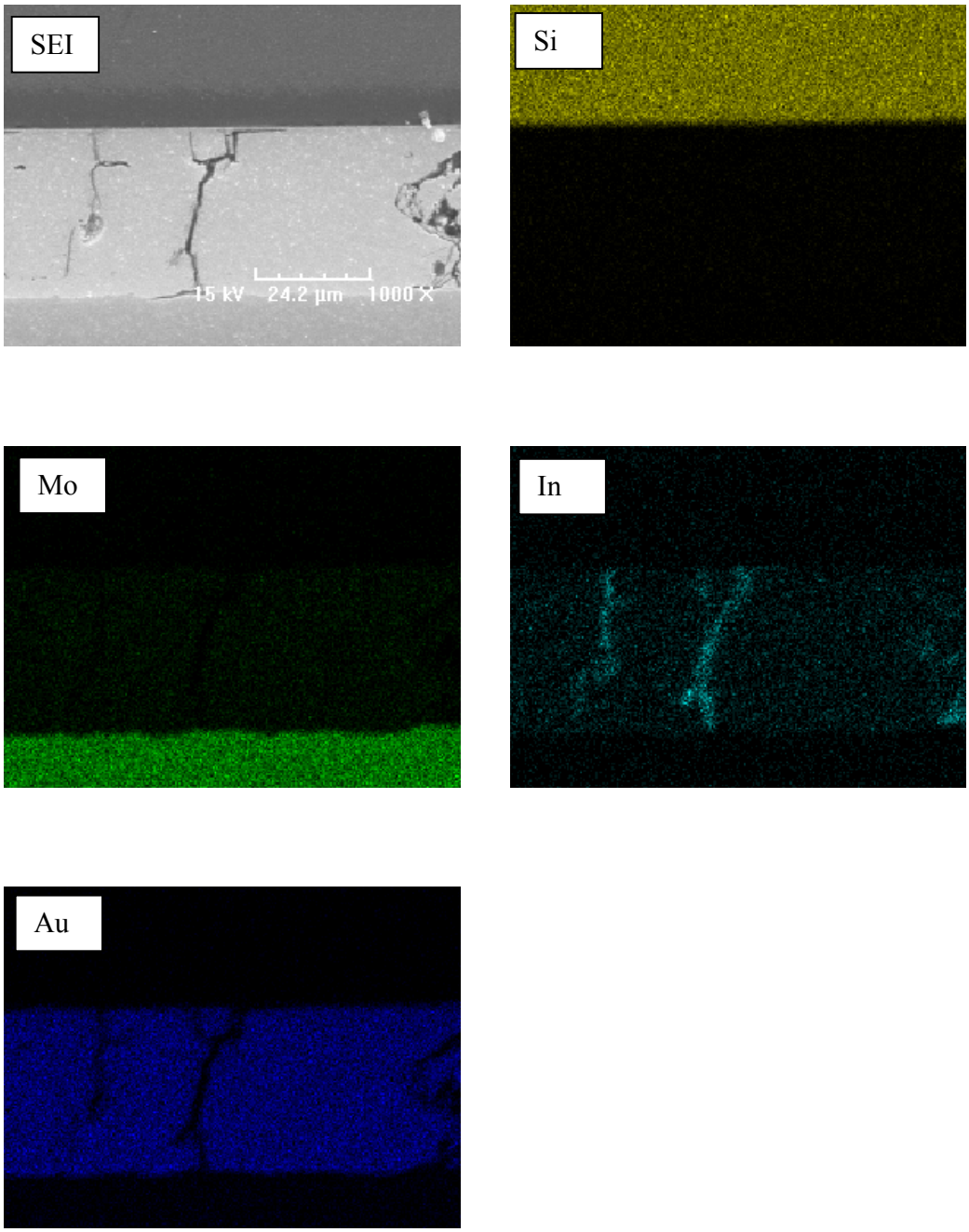


Figure 3.24 Cross-section picture with EDX In dot map for sample after 1200 cycles

After 2880 cycles, the die fell off from the Mo tab or the shear strength was around 1-2 kg-f. Figure 3.25 shows the cross section picture for the sample after 2880 cycles. Delamination occurred between bond joint and Mo. Indium segregation was observed in the cracks and in the exposed bottom surface of the braze layer.

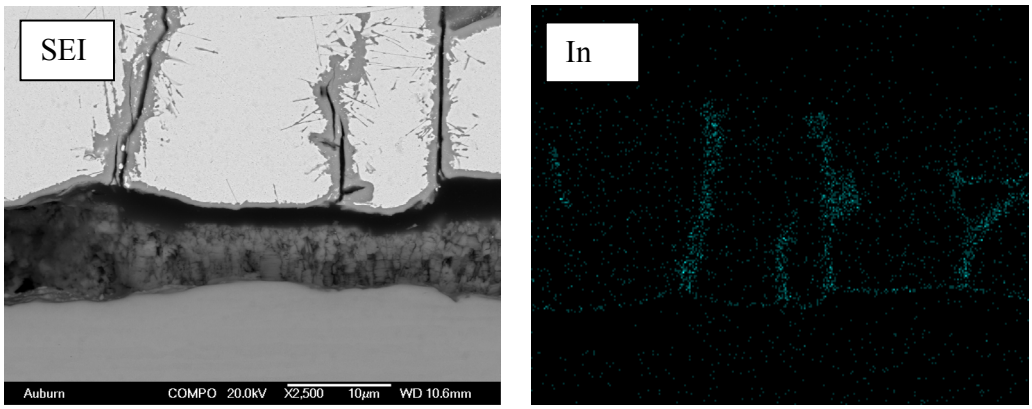


Figure 3.25 Cross-section of sample after 2880 cycles

Figure 3.26 shows the substrate surface after the SiC die sheared off after 2880 cycles. There were only Mo and In on the substrate, which indicates that the entire bond joint delaminated from the Mo.

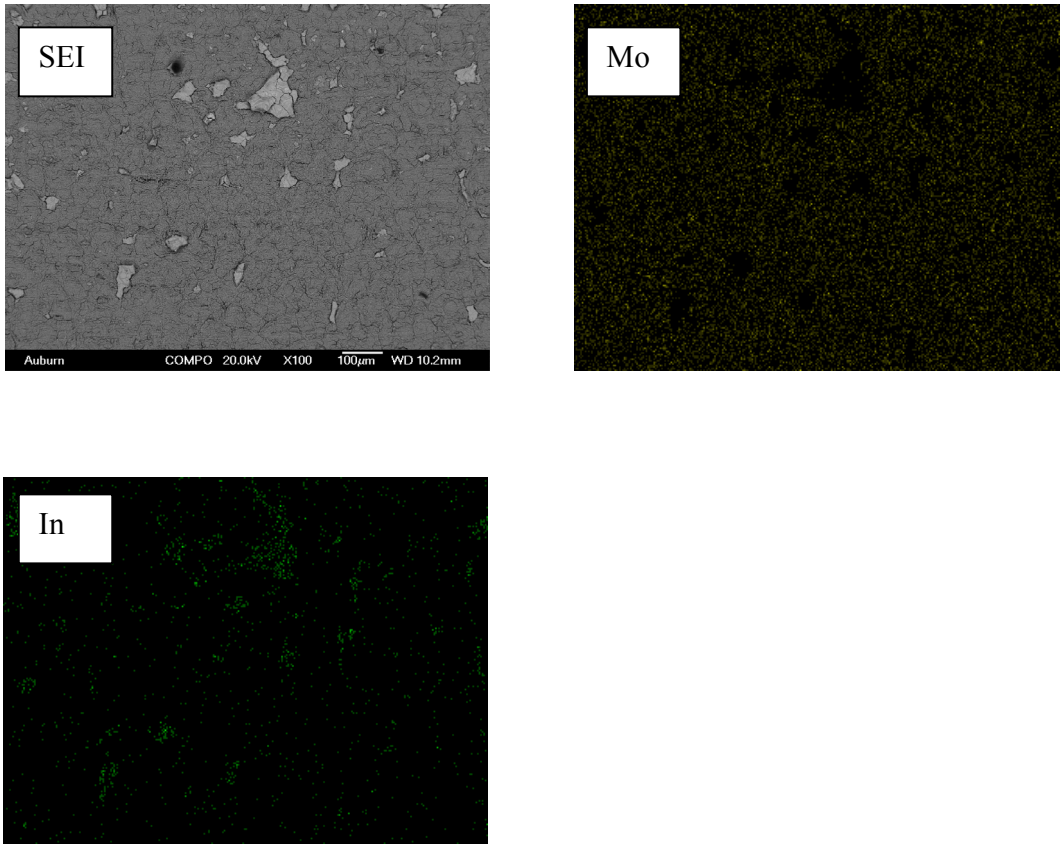


Figure 3.26 SEM image of fell off substrate after 2880 cycles

3.5 SUBSTRATE METALLIZATION BARRIER MATERIAL EVALUATION

During the reliability testing of the thick Au die samples, the unbonded area on the substrate metallization (Cu/Ni/Au) became black after only 100 hours of aging and began to flake off after 250 hours of aging. This indicates that copper had diffused through the Ni barrier and the gold layer onto the substrate surface and then oxidized in the air. This presents a serious problem for the device packaging. An effective barrier

material must therefore be developed in order to prevent this copper diffusion in the substrate metallizations.

In this part of the research, several metallization barrier materials provided by HH Sumco company were evaluated for high temperature applications. Table 3.3 shows the composition and the thickness of the protective layer over the copper for each sample evaluated.

Table 3.3 Substrate metallization structure

Sample	Nickel	Cobalt	Gold
1	5 µm		1.25 µm
2	5 µm		2.5 µm
3		1.25µm	2.5 µm
4		2.5µm	2.5 µm
5	5 µm	1.25 µm	2.5 µm

All the samples were stored in a Blue-MOV-18C high temperature chamber at 450ºC with ±1ºC accuracy. The storage times were 100, 250, 500, 1000, and 2000 hours. Auger Electron Spectroscopy (AES) was used to detect the appearance of copper in the metallization surface. Figures 3.27-30 show the results of the AES analyses for these samples. Copper appeared on the sample surface before or after 1000 hours at 450ºC. Thus, none of these protective materials offered good barrier properties to prevent copper diffusion at 450ºC.

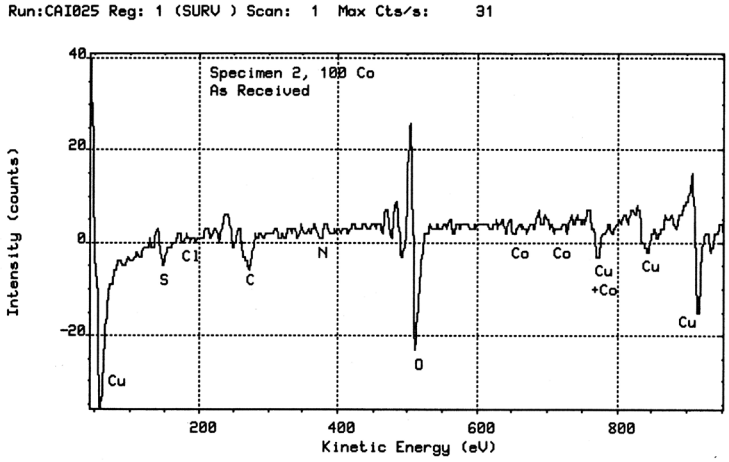


Figure 3.27 2.5µm Co/ Au after 500 hours at 450ºC

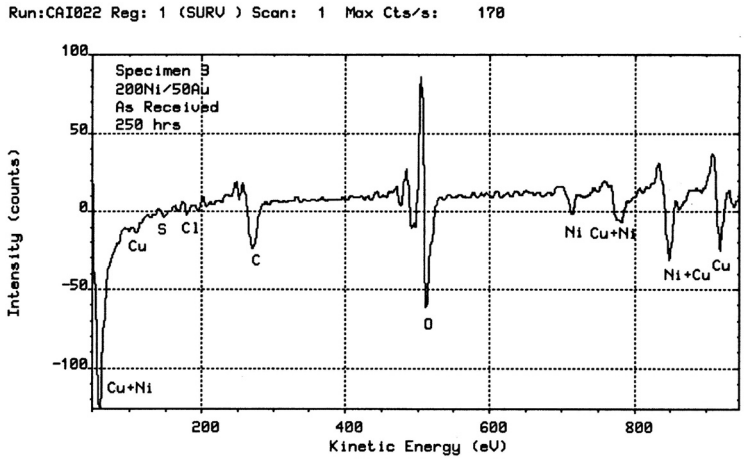


Figure 3.28 5µm Ni/1.25µm Au after 250 hours at 450ºC

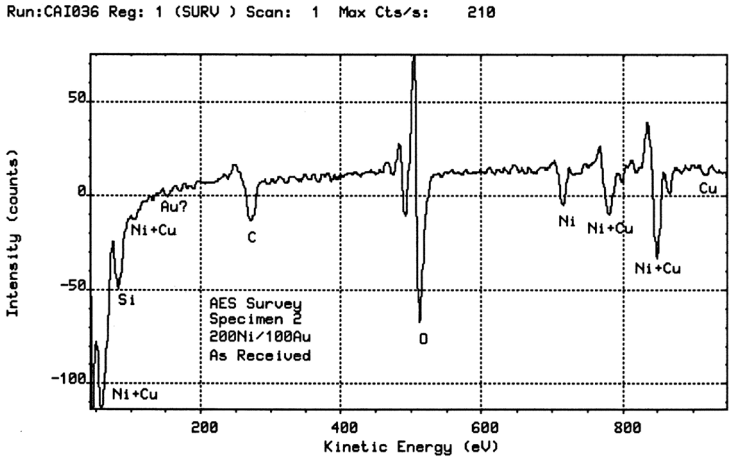


Figure 3.29 5µm Ni/2.5µm Au after 1000 hours at 450ºC

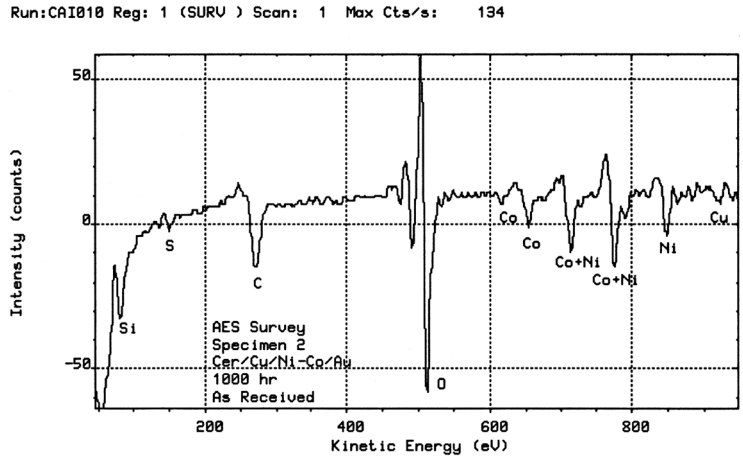


Figure 3.30 Co-Ni/ Au after 500 hours at 450ºC

One multi-layer nickel phosphorous coupon without an Au cap layer manufactured by HH Sumco company was also evaluated. The test coupons were electroplated with an AIRTech coating consisting of a dual layer of nickel sulfamate capped by a thin layer of electroplatable phosphorous-nickel. The thickness of the nickel coating totaled approximately 2.75µm, with the nickel phosphorous layer measuring approximately 0.625µm. The phosphorous content of the top layer was between 6 and 7% [23]. Figure 3.30 shows the AES analysis result after 2000 hours of aging at 450ºC. No copper had appeared on the coupon surface even after 2000 hours at 450ºC. Thus, this multi-layer nickel phosphorous structure acts as a good barrier to prevent copper diffusion for high temperature applications.

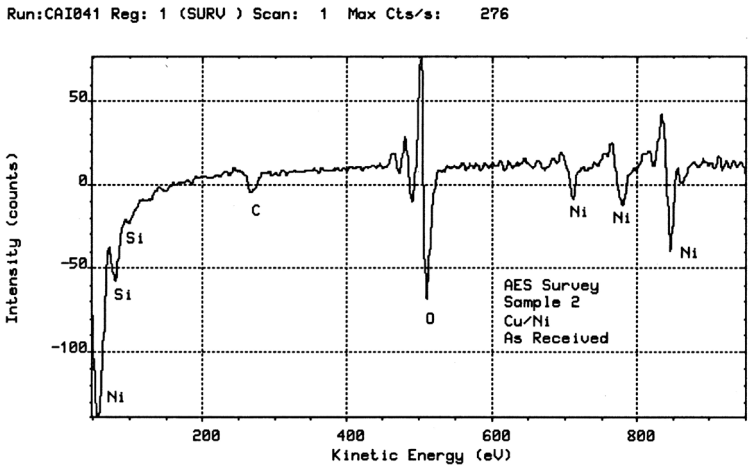


Figure 3.31 Multilayer Ni-P after 2000 hour at 450ºC

3.6 SUMMARY

Based on the high melting point of Au-In alloy (81/19 wt%), it was evaluated as a potential high temperature die attach material using a transient liquid phase bonding

process in this study. The die shear strength of samples fabricated with thin Au die-to-thick Ag substrate combination remained above 100kg-f after 2000 hours storage at 450ºC in air. The Al_2O_3 substrate fractured after 300 thermal cycles (35-400°C) as a result of the CTE mismatch induced stress between the Cu foil and Al_2O_3 substrate. The die attach layer also cracked due to CTE mismatches.

The die shear strength of samples fabricated with thick Au die-to-Au substrate combination degraded after 1000 hours storage at 450ºC in air. Voids formed in the as-built sample due to hydrogen entrapped in the Au layer during the Au electroplating process. In and Cu diffused from the substrate formed weak intermetallics in the bond joint. Voids coalesced to form cracks during the high temperature storage.

The die shear strength of samples fabricated with thin Au die-to-Mo tab degraded after 2400 cycles (35-400°C). Voids also formed in the as-built sample due to hydrogen entrapped in the Au layer during the Au electroplating process. Vertical cracks developed in the bond joint during thermal cycling tests due to the tensile stress induced by the CTE mismatch between the AuIn and the SiC and Mo tab.

The indium in the samples fabricated with thick Au die-to-Au substrate and thin Au die-to-Mo tab combinations segregated to defect surfaces (cracks and voids) during high temperature storage and thermal cycling. Indium surface enrichment of evaporated Au-In thin films has been reported at room temperature [48]. This segregation appeared to negatively impact the reliability of the die attach. Alternate high temperature die attach materials must be evaluated for SiC devices operating at 400-450^{o}C.

6μm of nickel or nickel phosphorous as a barrier material in conventional ceramic substrate metallization did not prevent Cu diffusion at the temperature of 450°C. A multi-

layer nickel phosphorous structure was found to serve as a good barrier to prevent Cu diffusion for high temperature applications. Based on an AES analysis, no copper appeared on the coupon surface even after 2000 hours of aging at 450ºC.

CHAPTER 4 LARGE DIAMETER WIRE BONDING ON SIC SUBSTRATE AND DIE METALLIZATIONS

4.1 LARGE DIAMETER WIRE BONDABILITY OF SUBSTRATE METALLIZATION

4.1.1 Wire Bond Test Substrate and Bonding Wires

In this research, 96% Al_2O_3/ (DBC) Cu/ electroless Ni/ electroplated Au (thickness: 625/200/6/3 μm) were used as the wire bonding test vehicle. Two types of large diameter wires (250μm), gold and platinum, were evaluated. The wires were manufactured by Custom Chip Connections. The gold wire had 10-20% elongation and a tensile strength range of 900-1300 grams [50]. The platinum wire had 8-15% elongation and a tensile strength range of 2100-2400 grams [51].

An Orthodyne model 360B automatic wedge wire bonder with a heated stage was used to perform thermosonic wedge bonding for all the wire bond experiments. The wire bonding process is shown in Figure 2.8. Wire bond pull and shear strength were used to monitor the wire bondability and reliability. Pull and shear tests were performed with a Dage PC2400 tester.

4.1.2 Bonding Parameters and Bond Criteria

The bonding force, substrate bonding temperature, bonding time and ultrasonic power are the machine parameters that can be controlled to optimize the bonding process. The function of the bond force is to maintain contact and aid the process by causing wire flow. The bonding force applied during bonding must be sufficient to maintain tool/wire contact without slippage. It must be sufficient to affect maximum ultrasonic coupling at the wire-pad interface, but not so excessive that it causes severe deformation or damage to either the wire or the bond pad [46]. Figure 4.1 illustrates the wire and bond tool before and after bonding [37].

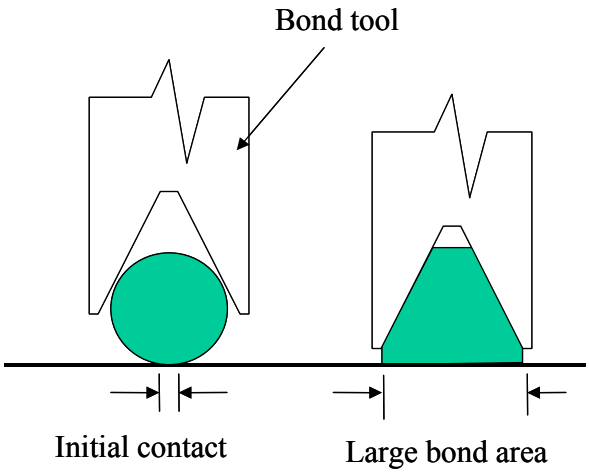


Figure 4.1 Before and after bonding [37]

The bonding temperature at the bond site also plays an important role in the strength of the bond formed, having a more significant impact than even the ultrasonic energy used. The higher the temperature, the lower the ultrasonic energy required to form the bond. Providing extra energy to the bond site in the form of heat generally causes the

process to be more robust and allows for a larger working window of the wire bonding parameters [46]. For reliable thermosonic gold or platinum bonding, the wire bonding process requires a certain minimum temperature, after which increasing the bonding temperature will produce stronger thermosonic bonds. In general, the higher the temperature the greater the reaction rate and the shorter the time required for thermosonic bonding. However, very high bonding temperatures may cause damage to the components, oxidation of the metallization or raise other reliability issues, so the bonding temperature should be kept below 250°C [46].

Bond time is the time duration for the application of ultrasonic energy. If the bond time is too short, insufficient wire deformation and bond formation occurs and bond lifts will be observed during pull tests. In contrast, excess bond time can result in damage to both the wire and the bond. As discussed above, if the bonding temperature is higher, the bonding time required for thermosonic bonding will be shorter. Therefore, on production lines, higher bonding temperatures and shorter times are used to increase productivity [46]. Compared to the bond force, bonding temperature and ultrasonic power, the bonding time is usually of lesser significance during the wire bond process.

Ultrasonic energy, coupled to the tool from a transducer, moves the bonding tool back and forth along a line parallel to the axis of the wire. The wire begins to soften as the ultrasonic energy is absorbed at existing dislocations in the wire. The ultrasonic energy causes still more dislocations to form and eventually slip occurs at crystal planes on both sides of the bond site and wire, exposing metals along the new slip faces. As the interface is shielded from the surrounding air, the freshly exposed wire surface readily

mixes with the substrate metallization and seizes, creating a metallurgical bond at the interface [37].

The amplitude of the vibration impacts the bond deformation: the amount of deformation is directly proportional to the amplitude of the vibration. For the ultrasonic vibration frequency, if the amplitude is excessively high, there is a possibility of fracturing already bonded contact areas before the welding period is complete [46].

As the result of a comprehensive design of experiments methodology with different bonding parameters, the optimal bonding parameters were identified and used to wire bond test parts for high temperature storage testing. The following criteria were used to determine the optimal bonding parameters [38]:

- Smallest number of bond misses
- 100% residue left after shear test
- Wire bonds with good destructive pull strengths
- Wire bonds with good shear test strengths
- Smallest number of bond lift failures during destructive pull testing
- Deformation (< 1.2x wire diameter)
- Smallest unbonded area in the center of the bond

Figure 4.2 shows the 3-D structure of the “perfect wire bond”[37]. It should not be deformed or distorted any more than necessary to produce an adequate cross-sectional area at the interface between the bond site and the wire. The “perfect wire bond” should have no deformation (normally referred to as an “ear”) on either side of the bond because the presence of an ear indicates a degree of over bonding. The top should be shiny. There

should be a smooth transition into the bond, without heel cracks. The interface with the metallization should have a small (or no) central, unbonded region surrounded by an oval band of uniformly disturbed metal. The shear strength is proportional to the bonded area; a larger bonded area yields higher shear strength. The bond interface should be free of microcracks. The wire tail should be short and without any shards of metal, normally between one quarter and one wire diameter in length. The bonding tool's impression on the wire should be free of black dust, which indicates an overlong bond time setting.

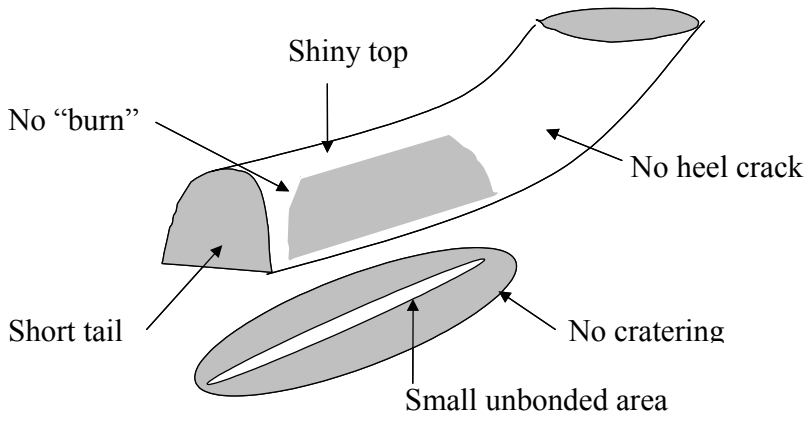


Figure 4.2 Perfect bond [37]

Figure 4.3 shows an image of a real wire bond. It has a smooth transition into the round wire, with no sharp transitions or cracks that could concentrate stresses. The tail is short and without any shards of metal that could break free within the package or short across to an adjacent metal area. The top of the wire is shiny. This bond has very small ears alongside the bonded area.

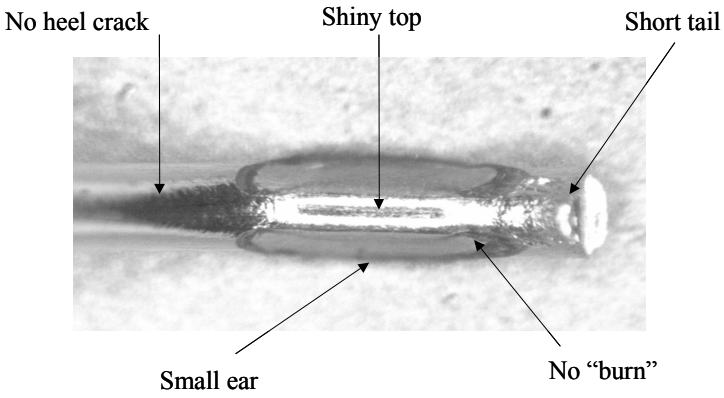


Figure 4.3 Real bond

4.1.3 Optimization of Wire Bond Parameters

Using the Orthodyne 360B bonder, the ultrasonic power and bond time can be set independently for the first and second bond. However, the bond force used must be the same for both the first and second bond. Bond force, ultrasonic energy, and bond time were varied and the qualities of the resulting bonds were assessed to establish minimum and maximum parameter values. Because high bonding temperatures may cause damage to the components, oxidation of the metallization or raise other reliability issues, the substrate temperature for Au wire was selected at 225ºC and for Pt wire at 250ºC. At the minimum limits, bond "no sticks" (wire did not bond) and wire lifts during pull testing were observed. At the maximum, excess deformation occurred. Once the parameter boundaries had been estimated, a series of experiments were performed varying the bond force and ultrasonic power between these extremes to find the optimal combinations. In this part of the work, three main factors were investigated: bond force, ultrasonic energy

(bond power), and bond time. For example, the factors and levels of the first bond gold wire bonding are shown in Table 4.1, with the corresponding Taguchi 3k factorial design shown in Table 4.2. For each design of experiment (DOE) run, 12 bonds were bonded and the shear strengths were collected for analysis.

Table 4.1 Control factors and levels for DOE of wire bonding parameters

Controllable Factor	Level 1	Level 2	Level 3
A: Force (g-f)	330	350	370
B: Power (μinch)	110	120	130
C: Time (μsec)	110	120	130

Table 4.2 Taguchi 3k factorial design for wire bonding DOE

Test Run	Force	Power	Time	Shear
1	330	110	110	2109
2	330	120	120	2237
3	330	130	130	2204
4	350	110	120	2134
5	350	120	130	2261
6	350	130	110	2245
7	370	110	130	2009
8	370	120	110	2122
9	370	130	120	2099

Table 4.3 shows the ANOVA DOE analysis results. Figure 4.4 is the main effect plot for means based on shear strength. From Table 4.3 and Figure 4.4, time has no significant effect on shear strength, so a single time was selected and used for all experiments based on the initial results; bond force and power both have a significant effect on the shear strength. The 350 g-f bond force and 120 μinch bond power had the

best shear strength. The optimal parameters selected as a result of this processes are shown in Table 4.4.

Table 4.3 ANOVA for wire bond shear strength

Source	DF	Adj SS	Adj MS	F	P
Force	2	30955.6	15477.8	182.57	0.0005
Power	2	25358.2	12679.1	149.56	0.007
Time	2	6.2	3.1	0.04	0.965
Error	2	169.6	84.8		
Total	8				

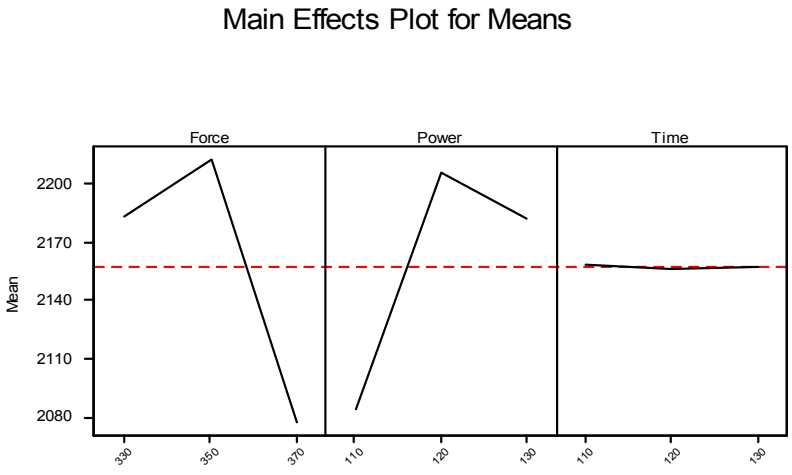


Figure 4.4 Main effects plot for means based on shear strength

Table 4.4 Optimal wire bonding parameters for thick gold substrate

	Gold	Platinum
Force (g-f)	350	450
Power 1 (µinch)	120	130
Power 2 (µinch)	125	135
Time 1 (µsec)	120	110
Time 2 (µsec)	120	110
Predelay Time (µsec)	100	100
Temperature (ºC)	225	250

4.1.4 Accelerated Aging Testing

Accelerated aging was performed on the wire bonds to examine the effect of aging on the strength of the wire bonds. The accelerated aging was performed in a Blue MOV-18C oven at 350°C with ±1°C accuracy for 0, 100, 250, 500, 1000 and 2000 hours. Figures 4.5 and 4.6 show the results of the gold and platinum wire bond pull and shear strength testing as a function of aging time performed on the ceramic substrate metallization. Shear1 is the shear strength of the first bond and shear2 is the shear strength of the second bond. The wire loop geometry produced a 45º angle during the pull test. As shown in Figure 2.7, the force applied to the wire (Force (true)) was 0.707 times the measured force (F_M). The pull test data reported and plotted is F_M. 24 measurements (shears or pulls) were made and averaged per data point.

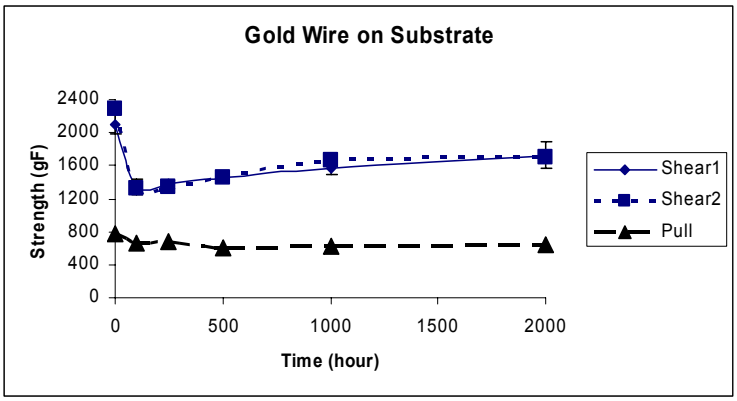


Figure 4.5 Average pull/shear strength of gold wire on substrate metallization

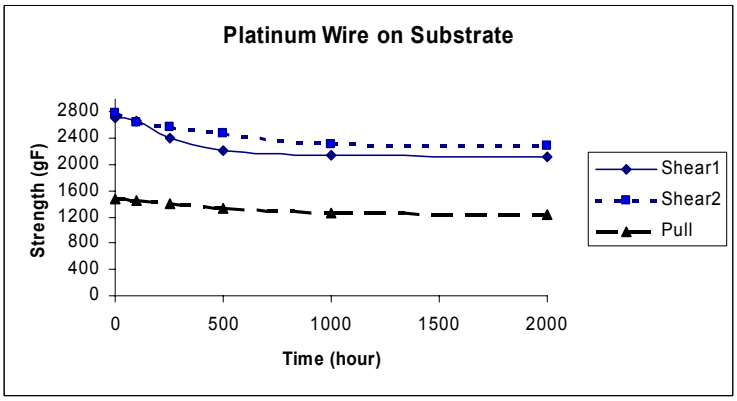


Figure 4.6 Average pull/shear strength of platinum wire on substrate metallization

From Figure 4.5, it can be seen that the average pull and shear strength of the gold wire bonds decreased during the first 100 hours, which was caused by the stress released by annealing, after which the pull strength remained constant throughout the remainder of the tests. The shear strength increased slightly with increasing aging time and remained approximately constant for long time aging. The gold remnant was 100% and there were no bond lifts during the whole accelerated aging test process.

From Figure 4.6, it can be seen that the average pull and shear strength of the platinum wire bonds decreased during the first 500 hours, which was again caused by the stress released by annealing, then the pull and shear strength both remained constant throughout the remainder of the tests. The platinum remnant was 100% and again there was no bond lift at any aging time during the accelerated aging test process. This indicates that no voids were formed in the interface between platinum wire and wire bond pads during the aging test.

4.2 Large Diameter Wire Bondability of SiC Die Metallizations over SiO_2

4.2.1 Wire Bond Test Die Metallization and Bonding Wires

A layer of nickel was deposited on an n-type 4H-SiC wafer, then annealed at high temperature to form nickel silicide, which acted as the ohmic contact of the SiC power device. A layer of SiO_2 was PECVD deposited on the nickel silicide, which acted as the passivation layer of the SiC power device. Two metallization stacks on this passivated SiC die were evaluated for this research: Ti/TiW/Au (thickness: 1000 Å /2000 Å /2000 Å) or Ti/Pt/Au (thickness: 1000Å /1000Å /2000Å) were sputter deposited on the SiC wafer. A Au cap layer was electroplated to 3μm on top of the thin film layers. These metallized wafers were supplied by Cree, Inc.

Two types of large diameter wires (250μm), gold and platinum, were evaluated. The wires were manufactured by Custom Chip Connections. The gold wire had 10-20% elongation and a tensile strength range of 900-1300 grams. The platinum wire had 8-15% elongation and a tensile strength range of 2100-2400 grams.

An Orthodyne model 360B automatic wedge wire bonder with a heat stage was used to perform thermosonic wedge bonding for all wire bond experiments, the wire bonding process was shown as Figure 2.8. Wire bond pull and shear strength were used to monitor the wire bondability and reliability. Pull and shear tests were performed with a Dage PC2400 tester.

4.2.2 Wire Bond Parameters

The optimal wire bonding parameters were selected according to the criteria discussed in the previous section, and are shown in Table 4.5.

Table 4.5 Optimal wire bonding parameters for die metallizations

	Gold	Platinum
Force (g-f)	280	350
Power 1 (μinch)	85	110
Power 2 (μinch)	90	115
Time 1 (μsec)	100	100
Time 2 (μsec)	100	100
Predelay Time (μsec)	100	100
Temperature (ºC)	225	250

4.2.3 Accelerated Aging Testing

Accelerated aging was performed on the wire bonds to examine the effect of aging on the strength of the wire bonds. The accelerated aging was performed in a Blue MOV-18C oven at 300°C with ±1°C accuracy for 0, 100, 250, 500, 1000 and 2000 hours. Shear1 is the shear strength of the first bond and shear2 is the shear strength of the second bond. The wire loop geometry produced a 45º angle during the pull test. As shown in Figure 2.7, the force applied to the wire (Force (true)) was 0.707 times the

measured force (F_M). The pull test data reported and plotted is F_M. 15-18 measurements (shears or pulls) were made and averaged per data point.

For the gold wire bonds on Ti/TiW/Au metallization, during the second bond shear test performed on the samples after 100 hours of aging aging, there were 2 bond pad metallization failures of the 18 bonds tested. These two failures were located at the wafer edge. There were no further failures of this type for the duration of the test, including the first bond shear tests, second bond shear tests and pull tests. The reason for the failed bond pad metallization is therefore likely to be the non-uniform deposition of the metallization or contamination at the wafer edge during the wafer fabrication process.

Figures 4.7 shows the gold wire bond pull and shear results of the aging tests performed on the Ti/TiW/Au metallization, excluding the 2 failed bonds at 100 hours.

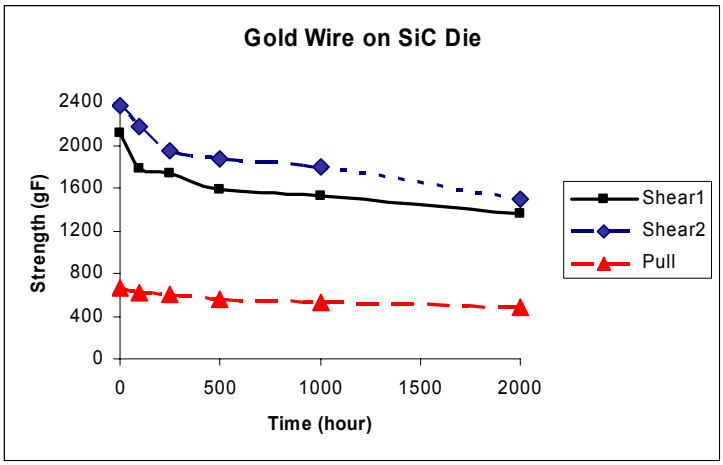


Figure 4.7 Average pull/shear strength of Au wire on Ti/TiW/Au metallization

From Figure 4.8, it can be seen that the average pull and shear strength of the gold wire bonds decreased during the first 500 hours of aging, which was caused by the stress released by annealing. After this, the pull and shear strength both remained relatively

constant throughout the remainder of the test. The gold remnant was 100% during the whole accelerated aging test process.

For the Au wire bonds on Ti/Pt/Au metallization, 10 of 16 wire pulls resulted in lifts after 1000 hours of aging; and all failed by lifts after 2000 hours of aging. The failure mode was the fracture of the SiO_2 layer.

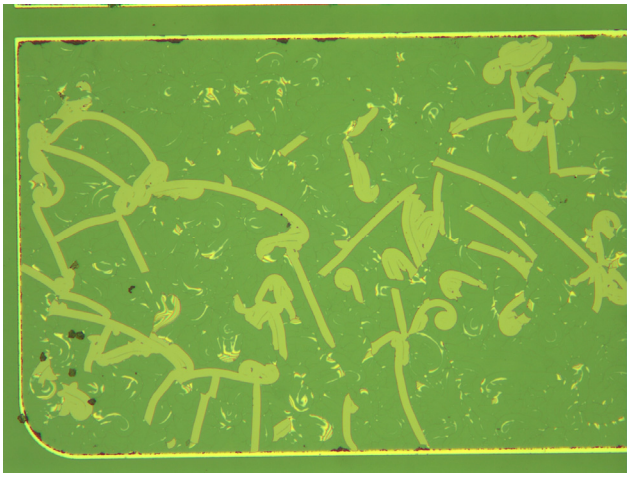
For the Pt wire bonds on Ti/TiW/Au, there were 4 of 19 second bond pad metallization failures during the shear test performed on the samples after 100 hours of aging. The failure happened at the thin film metallization-to-SiO_2 interface. No bond pad failure occurred during second bond shear testing at the other test times. These 4 bond pad metallization failure are believed to be due to poor initial film adhesion. 2 of 15 wire pulls resulted in lifts after 2000 hours of aging, the failure mode was the fracture of the SiO_2 layer.

For the Pt wire bonds on Ti/Pt/Au, 5 of 14 wire pulls resulted in lifts after only 250 hours of aging; and all failed by lifts after 500 hours of aging. The failure mode was the fracture of the SiO_2 layer which lifted from the SiC surface and SiC damage (cratering).

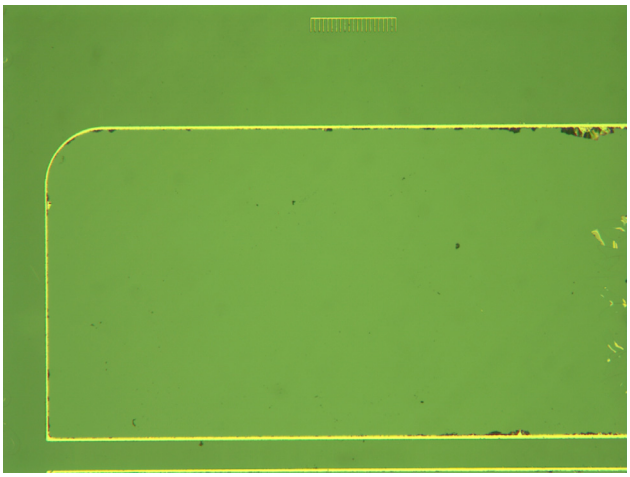
The failure mode (SiO_2 layer fracture and SiC damage) under the bond pad can only be seen by removing the bond pad metallization and lifting the bond. This was accomplished by etching the metallization using a chemical solution and gently lifting the bond, thus revealing the failure modes underneath. Figure 4.9 shows optical microscope images of the SiO_2 after removal of the Ti/Pt/Au and Ti/TiW/Au metallization. From Figure 4.8 (c) and Figure 4.8 (a), respectively, it can be seen that SiO_2 under both Ti/TiW/Au with a gold bond and Ti/Pt/Au without a wire bond were intact after 2000

hours of aging at 300°C, while SiO_2 under Ti/Pt/Au with a gold bond showed fractures after 2000 hours of aging at 300°C (Figure 4.8 (b)).

(a) SiO_2 under Ti/Pt/Au without wire bonds after 2000 hour of aging



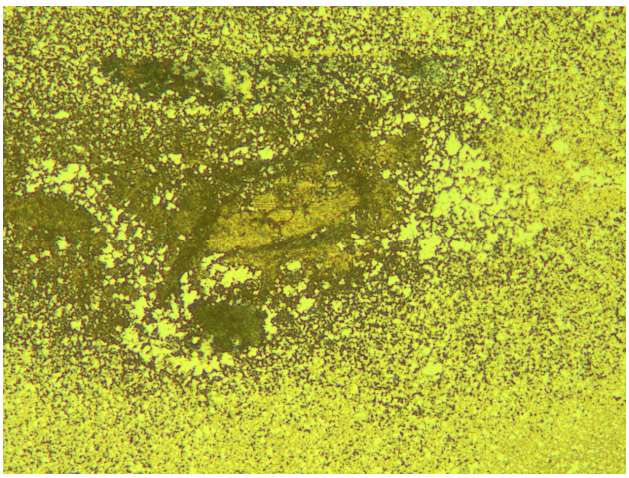
(b) SiO_2 under Ti/Pt/Au with Au wire bond after 2000 hour of aging



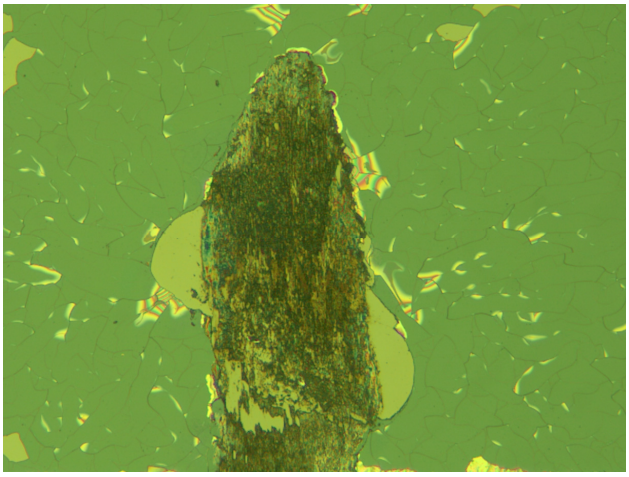
(c) SiO_2 under Ti/TiW/Au with Au wire bond after 2000 hour of aging

Figure 4.8 SiO_2 under Ti/Pt/Au without and with wire bond after 200 hour aging

Another failure mode was SiC damage as shown in Figure 4.9. This SiC damage failure mode only occurred for platinum wire bonding on Ti/Pt/Au metallization.



(a) Ti/Pt deformation after the Au layer has been etched off



(b) SiC damage after the Ti/Pt layers have been etched off

Figure 4.9 Picture of SiC damage under Ti/Pt/Au metallization with Pt wire bond

4.2.4 Failure Analysis

Compared to fine wire bonding, much higher bond force is required in the large diameter wedge bonding process. Cratering has been observed in both Al ultrasonic and Au thermosonic bonding at high bonding force in silicon devices [46]. High bonding force coupled with ultrasonic energy may cause craters in the silicon, particularly if there is any localized stress concentration. In some cases, particularly in Al wedge bonding, even low bond forces seem to cause cratering [46].

Ultrasonic energy is also a major cause for cratering. For example during thermocompression bonding it has been observed that even application of very high stress and high temperature does not cause excessive cratering. During ultrasonic and thermosonic bonding, initially the bonding tool presses the wire on the bond pad and only

a few localized points are in actual physical contact. If there is a small defect in the SiC under the bond pad, the application of ultrasonic energy coupled with localized high stress could propagate through the micro crack [46].

There are no clear experimental studies that have been done to show a correlation between wire hardness and cratering. But generally it has been observed that during copper ball bonding there is greater cratering. Since copper is harder than Au it is expected that the cause of cratering is higher hardness. The higher the wire hardness the greater is the bonding force and ultrasonic energy required for bonding; and this leads to cratering [46].

Bond pad metallization materials and structures affect bondability as well as bond reliability. It has been observed from experiments that as the metallization thickness increases there is a significant reduction in the cratering failure mode during shear test. It has also been experimentally shown that thinner metallization has a higher tendency for cratering than thicker metal. This has been attributed to the "cushioning effect" of the thicker metal [46].

In this dissertation work, gold wire had better reliability results on SiO_2 over SiC than platinum wire, based on a comparison of the failure start times and failure modes for the same metallization. Higher bonding force and ultrasonic energy levels were required for platinum wire bonding because the platinum wire has higher hardness than gold wire. Ti/TiW/Au metallization produced better aging test results than the Ti/Pt/Au metallization based on a comparison of the failure start times and failure modes. The differences between the two types of metallization were TiW versus Pt as well as their

thickness. Therefore the metallization structure is likely to contribute to the different reliabilities.

A complete understanding of the effect of bonding force and bonding pad metallization structure is necessary in order to explain wire bonding failures such as cratering, peeling and cracking. In reality, wire bonding is a complicated, multi-physics, transient dynamic process, which is completed within a very short time. The bond pad thickness normally is only a few microns. It is almost impossible to directly measure the strains or stresses experimentally. Hence, a simplified FEMA model was performed to understand the effect of bonding force and bond pad metallization on the failure mode, and may further help to improve the bonding process and bond pad metallization design by avoiding die failure modes, such as SiO_2 fracture and SiC damage.

For FEMA success, the bonding process, especially the bond head movement must be clearly understood. Figure 4.10 shows the bond head movement of the Orthodyne bonder used in this research [37].

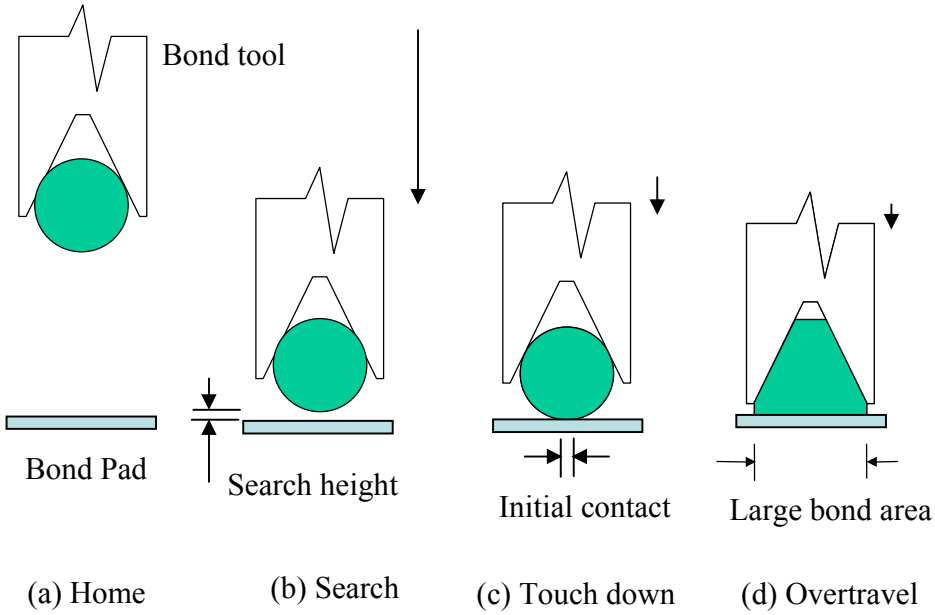


Figure 4.10 Bond head movement [37]

At the beginning of the wire bonding process, the bond head moves from home over and down to a position above the bond point. The position above the bond point is "search". The bond head reaches the design velocity limit while traversing half the distance, then decreases to zero velocity at the search position.

At search, the velocity of the bonding tool is reduced to allow the head to move down to the wire surface gently and slowly so as not to flatten the wire when the tool makes contact with the surface. The bond head positions the tool at a height above the work surface (search height) before continuing down at a slow constant velocity (search to bond pad).

Before the head moves down from the search height toward the bond pad, the programmed bonding force is fully applied to the transducer at search height. The head continues down until the touch down switch opens indicating the tool and wire touched

the work surface. A programmed prebond delay period 100msec is applied to assure that the head has come to a complete stop before beginning the bonding process. Then, ultrasonic bonding power is applied to the transducer to begin the bonding process. During this period, the head moves down beyond the point where the touch down switch opened to provide a small vertical distance for the tool to lower as it flattens the wire during bonding.

Bonding force (gram force) is the static load applied downward against the wire. And the initial touch down contact area is very small in order to obtain 100% bonded area. A high bonding force is required for the large diameter wire bonding. Thus, a high pressure focuses on the touch down area.

Ansys 9.0 software was used to carry out the simulation in this study. The construction of a finite element model includes a consideration of the material properties, the geometry and mesh, and the loading. In addition, the careful selection of the element type is also essential due to its effect on the simulation accuracy. A summary of the material properties used in the simulation is shown in Table 4.6 [52][53][54][55].

Table 4.6 Materials properties at 225/250ºC [52][53][54][55].

	Thermal Expansion Coefficient (10^{-6}/K)	Young's Modulus (/GPa)	Poisson Ratio
Au	14.2	73	0.44
Pt	8.8	157	0.38
TiW	4.5~5.8	407	0.28
Ti	8.6	102	0.32
SiO_2	0.4	165	0.23
SiC	4.5	430	0.21

Several assumptions were specified in this simulation: 1) all the materials are linear elastic; 2) temperature in the metallization is uniformly distributed; 3) Young's modulus of all the materials do not change with the application of ultrasonic energy; and 3) there are no contact intermetallic effect and diffusion in the bond formation.

A simplified 2D model was established according to the previous description of the bond head movement. The 2D model is shown in Fig 4.l1, which is cut from a die with 3 layer metallization Ti/TiW/Au (thickness: 1000Å/2000Å /3μm) and SiO2 layer (thickness: 1000Å) above the SiC (thickness: 10μm). It is noted that the real thickness of SiC was about 400μm. 10μm thickness was used in the model to save calculation time. The bottom of the SiC is fixed and the two sides are constrained in the horizontal direction. Figure 4.12 gives the meshes and load on the bond pad metallization. The bonding force was replaced by pressure on a line, the length of the line equaled to the initial wire touch down width, and the pressure equaled to the bonding force over the initial wire touch down area. The initial touch down width was

selected as 2μm, the area is about 2 μm x 420μm; the bonding force for gold wire was 280 g-f, platinum wire 350 g-f. In this 2D model, the geometry unit used was nm, the corresponded pressure for Au wire was 3.3E-7 g/nm^2, and for Pt wire was 4.2E-7 g/nm^2. The simulation temperature used for Au wire bonding was 225ºC, and for Pt wire bonding was 250ºC.

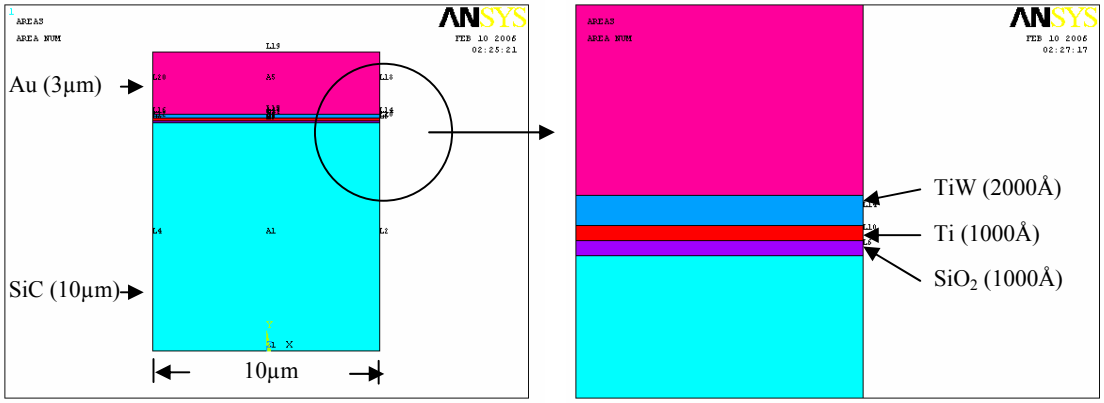


Figure 4.11 Bond pad metallization 2D model

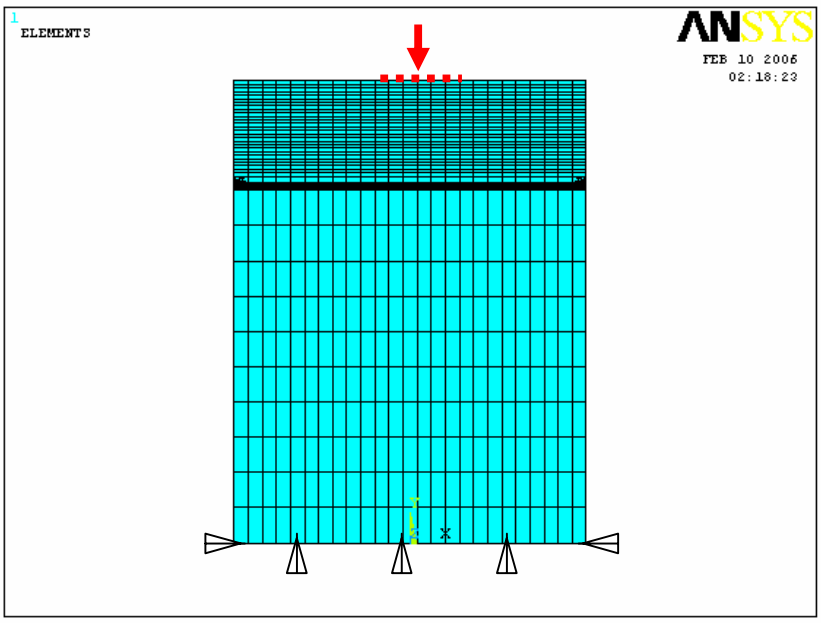


Figure 4.12 Pad metallization mesh and load

Figures 4.13-20 show the simulation results of Von Mises stress and strain in the bond pad metallizations for Au and Pt wire bonding. Table 4.7 shows the comparison between the FEMA simulation results and experimentally testing results.

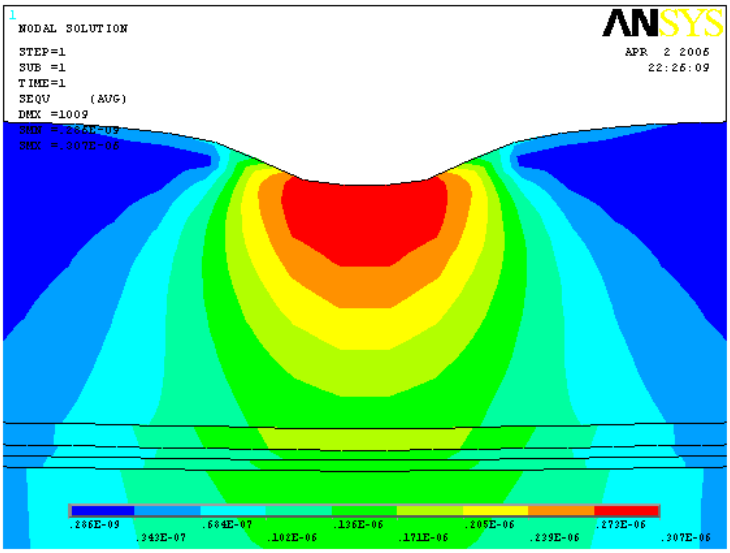


Figure 4.13 Von Mises stress in Ti/TiW/Au metallization for Au wire bonding

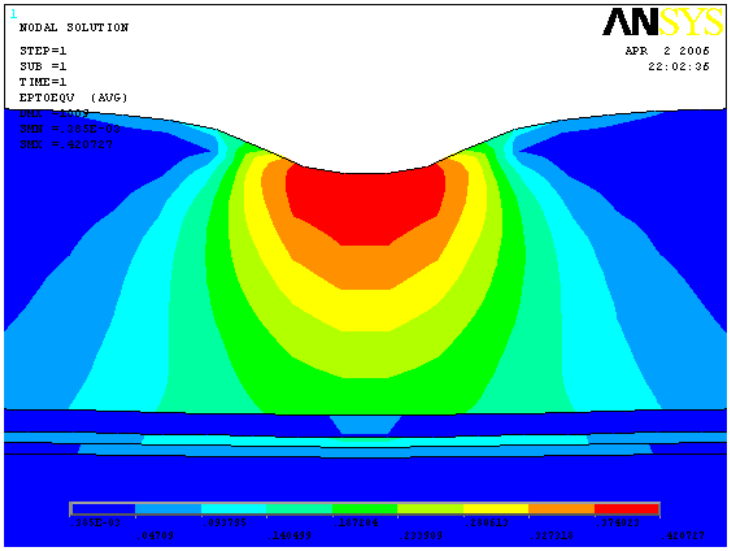


Figure 4.14 Von Mises strain in Ti/TiW/Au metallization for Au wire bonding

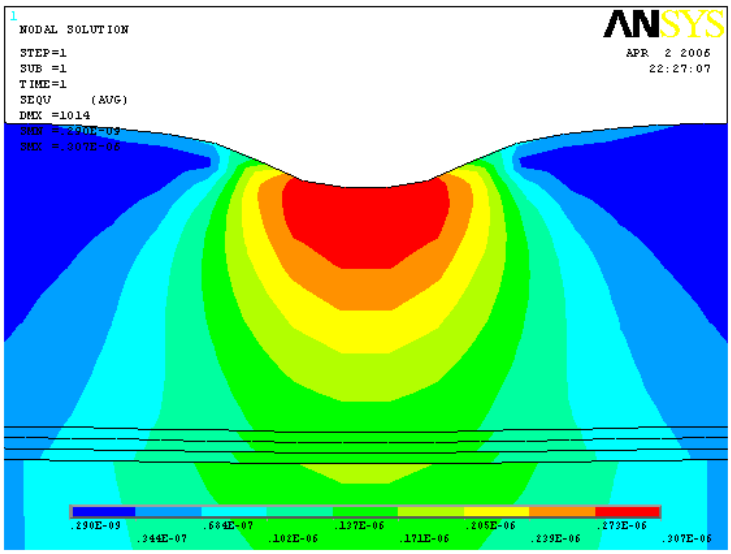


Figure 4.15 Von Mises stress in Ti/Pt/Au metallization for Au wire bonding

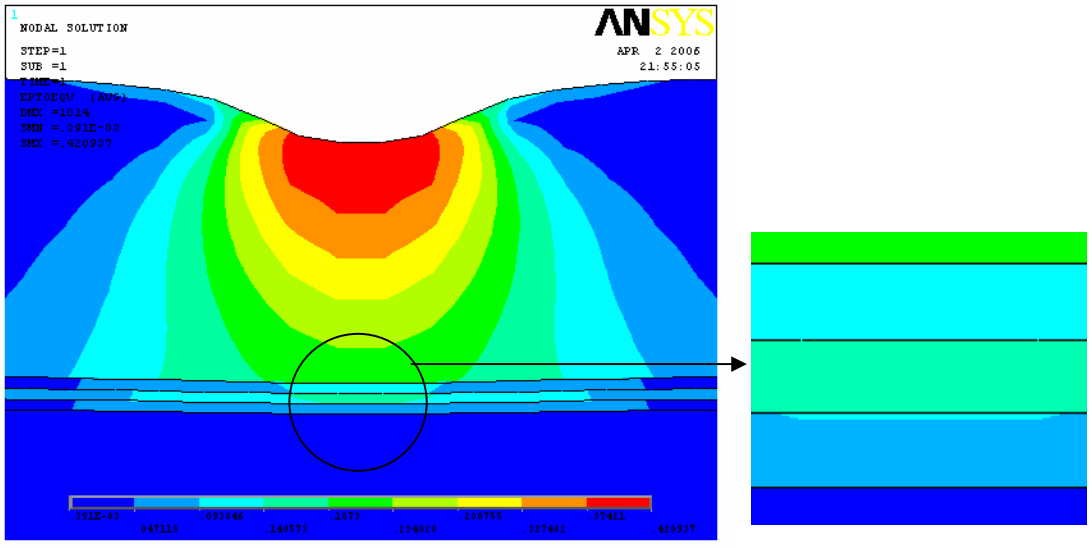


Figure 4.16 Von Mises strain in Ti/Pt/Au metallization for Au wire bonding

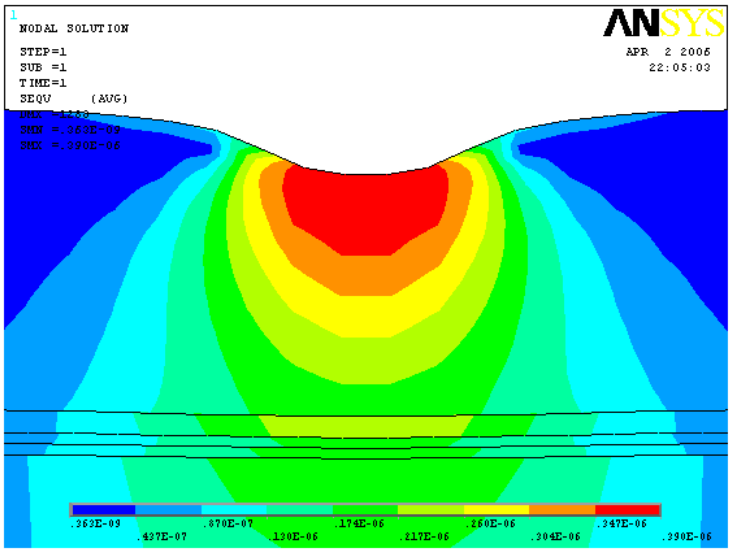


Figure 4.17 Von Mises stress in Ti/TiW/Au metallization for Pt wire bonding

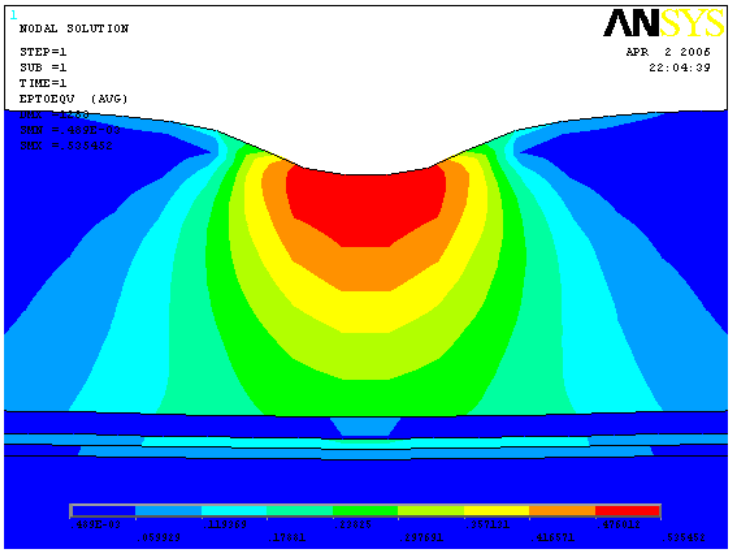


Figure 4.18 Von Mises strain in Ti/TiW/Au metallization for Pt wire bonding

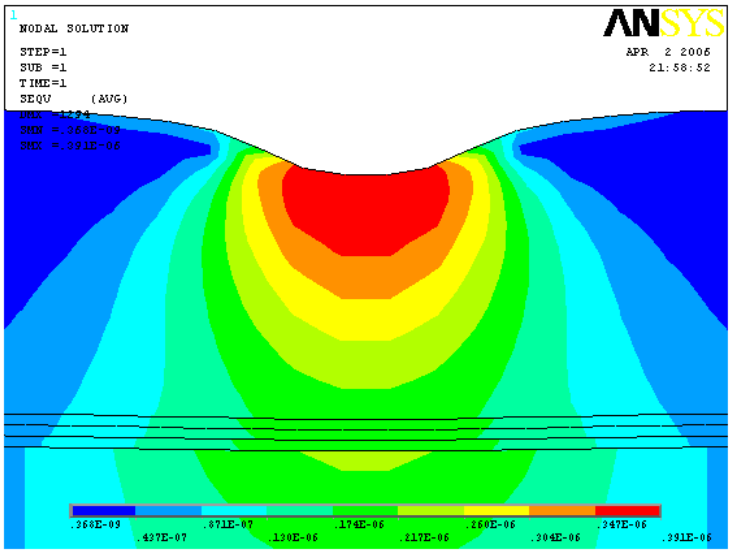


Figure 4.19 Von Mises stress in Ti/Pt/Au metallization for Pt wire bonding

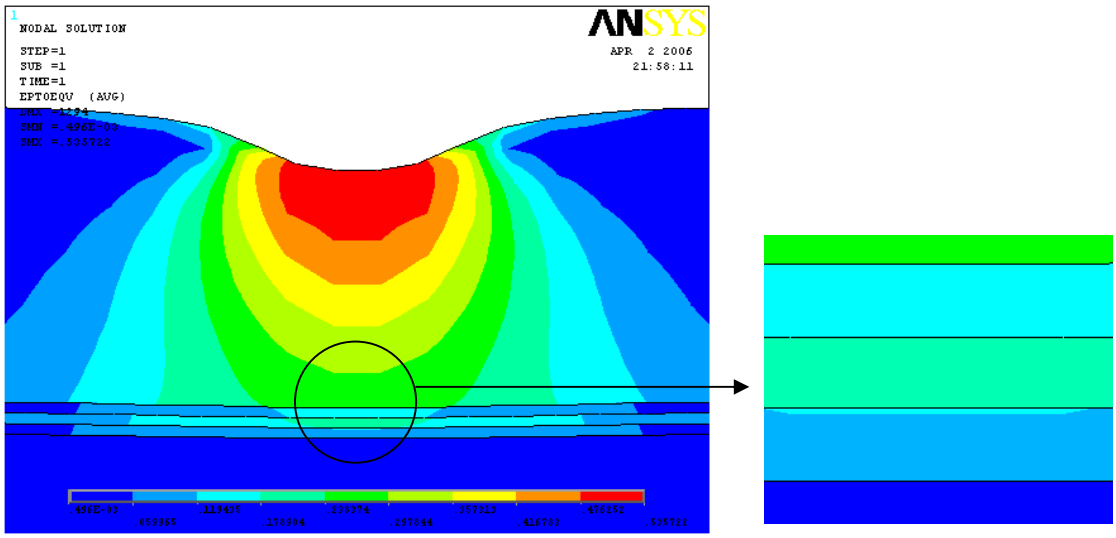


Figure 4.20 Von Mises strain in Ti/Pt/Au metallization for Pt wire bonding

Table 4.7 Comparison between FEMA simulation and testing results

Comparison		Ti/TiW/Au		Ti/Pt/Au	
		Au wire	Pt wire	Au wire	Pt wire
Testing result	Bond lifts	N/A	2 of 15 after 2000 hour	10 of 16 after 1000 hour	5 of 14 after 250 hour
	Failure mode	N/A	SiO_2 crack	SiO_2 crack	SiO_2 crack & SiC damage
FEMA simulation	Strain in SiO_2	0.047	0.06	0.094	0.12
	Stress in SiC (g/nm^2)	1.36E-07	1.74E-07	2.05E-07	2.60E-07

The Au wire bonding force induced the minimum Von Mises strain in the SiO_2 layer under the Ti/TiW/Au metallization. No micro-crack formed in the bonding process and no bond lift occurred during the pull tests; while the Pt wire bonding force induced the maximum Von Mises strain in the SiO_2 layer under the Ti/Pt/Au metallization. The maximum strain coupled with high ultrasonic energy during bonding process caused the most or largest micro-cracks in the SiO_2, which lead to bond lifts earliest during the pull tests. The Pt wire bonding force induced the maximum Von Mises stress in the SiC surface region under the Ti/Pt/Au metallization. The maximum Von Mises stress coupled with high ultrasonic energy during bonding process caused SiC damage. The FEMA simulation results correlated with the testing results very well.

4.3 LARGE DIAMETER WIRE BONDABILITY OF SIC DIE METALLIZATION WITHOUT SiO_2

4.3.1 Wire Bond Test Die Metallization and Bonding Wire

An innovative composite contact metallization on SiC for high temperature applications has been developed by Auburn University researchers [13]. The metallization stack Ta-Si-N (2%)/Pt-N/Au (thickness: 1500Å /1000Å /3μm) deposited on nickel silicides on a SiC wafer using a hot sputtering technique was proven to have high stability at a high temperature of 350ºC. This work was to investigate the wire bonding reliability of this metallization stack.

The metallization stack Ta-Si-N (2%)/Pt-N/Au on nickel silicide ohmic contact on SiC wafer was fabricated as follows:

- Pre-Clean SiC wafer in organic and inorganic solution.
- High vacuum sputter the Ni (thickness < 800 Å) on the SiC wafer.
- Anneal at 900°C for 1 minute in a high vacuum chamber (10^{-6} torr) to form Ni_2Si as ohmic contact.
- Load SiC wafer on the back-heated wafer holder in a three target high vacuum sputtering chamber.
- Pump vacuum to 10^{-7} torr.
- Vent Ar/N_2 (2%) gas mixture into the chamber.
- Sputter $TaSi_2$ on to the SiC wafter.
- Heat to 250ºC, and sputter Pt on to the SiC wafer.
- Sputter Au on to the SiC wafer at temperature of less than 150ºC.

- Electroplate Au to a thickness of 3μm.
- Dice the wafer to the experimental size (1inch x1inch).

Large diameter gold wire (250μm) manufactured by Custom Chip Connections was used again in this work. The wire loop geometry produced a 45º angle during the pull test. As shown in Figure 2.7, the force applied to the wire (Force (true)) was 0.707 times the measured force (F_M). The pull test data reported and plotted is F_M. 16 measurements (shears or pulls) were made and averaged per data point.

4.3.2 Accelerated Aging Testing

Accelerated aging was performed on the wire bonds to evaluate the wire bond reliability with this metallization stack. The accelerated aging was performed in a Blue MOV-18C oven at 350°C with ±1°C accuracy for 0, 100, 250, 500, 1000 and 2000 hours.

Figure 4.21 shows the gold wire bond pull and shear results for the accelerated aging tests performed on the metallization. Shear1 is the shear strength of the first bond and shear2 is the shear strength of the second bond. From the figure, it can be seen that this metallization stack Ta-Si-N (2%)/Pt-N/Au had good reliability with gold wire bond for applications at 350ºC.

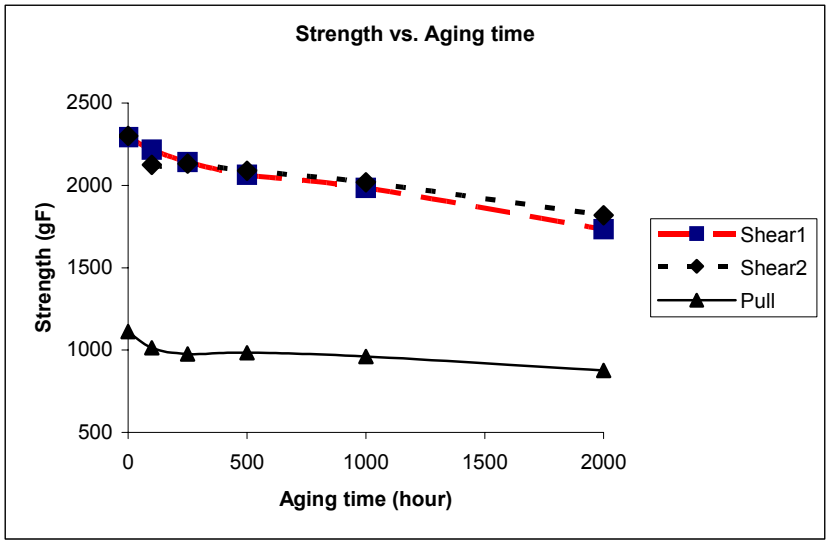


Figure 4.21 Average shear/pull strength of gold wire bonds on Ta-Si-N 92%)/Pt-N/Au

4.4 SUMMARY

Large diameter (250μm) gold and platinum wires have good bondability on ceramic substrate thick metallization and high reliability with 350ºC aging. Platinum wire bonds have higher strength than gold wire.

For SiC/Ni_2Si/SiO_2/Ti/TiW/Au metallization, Au wire bonds had good reliability with 300ºC aging, while 2 of 15 Pt wire bonds had bond lifts during pull testing after 2000 hours of aging. For SiC/Ni_2Si/SiO_2/Ti/Pt/Au metallization, 10 of 16 Au wire bonds had bond lifts during pull testing after 1000 hours of aging, 5 of 14 Pt wire bonds had bond lifts during pull testing after 250 hours of aging.

A simplified FEMA 2D model was used to understand the effects of bond force and die metallization structure on the failure mode. The results matched the experimental

results very well. The best combination was Au wire on a Ti/TiW/Au pad stack over PECVD SiO_2. This work demonstrated the effects of wire and pad metallurgy on bond reliability.

The metallization stack Ta-Si-N (2%)/Pt-N/Au had good reliability with gold wire bonds for applications at 350ºC. More work need to be done to investigate the reliability of this metal system for applications at higher temperatures.

CHAPTER 5 POLYIMIDE BREAKDOWN TEST

5.1 POLYIMIDE TEST SAMPLE FABRICATION AND EXPERIMENT SET-UP

Devices operating under high power conditions may also be exposed to high voltages, and as a result high voltage breakdown may occur between adjacent electrical connections and/or between high voltage electrical connections and the surrounding air. To prevent this, an effective dielectric passivation coating must be applied to ensure reliable package operation.

Dupont PI2611 polyimide has an exceptional combination of high thermal stability, good mechanical toughness, good chemical corrosion resistance, excellent dielectric properties and relatively low moisture uptake due to its rodlike structure with a backbone composed of rigid cyclic elements. It can be used as a passivation material to decrease the leakage current and increase the breakdown voltage between adjacent ohmic contact pads.

In this research, Dupont PI2611 polyimide coated on quartz substrates (2 x 1 x 0.040 inch) was evaluated for its breakdown strength at high temperature. The test pattern was designed as shown in Figure 5.1. Two 25μm wide, 3mm long metal traces were paralleled with 100μm spacing, and two 1mm x 1mm probe pads were spaced 2cm apart.

The metal traces were sputtered Cr/Au (thickness: 1000Å /2000Å) thin film; the polyimide material covered only the two parallel traces, the thickness was about 6-9μm. The polyimide test sample fabrication was as follows:

- Pre-Clean quartz substrate in organic and inorganic solution.
- Spin apply negative photoresist on the substrate, and soft-bake at 105ºC on a hot plate for 60 seconds.
- Pattern test circuit on the substrate by UV Exposure using Kurl Sauss MA6.
- Remove exposed photoresist by developer.
- Hard-bake the substrate at 120C on a hot plate for 60 seconds.
- High vacuum E-beam deposite Cr/Au (thickness: 1000 Å /2000 Å) on the substrates.
- Strip photoresist by Acetone solution.
- Spin apply adhesion promoter on the substrate, and soft-bake at 150°C on a hot plate for 90 seconds.
- Manually dispense the polyimide PI2611 to cover the test circuit with a syringe.
- Soft-bake polyimide film at 90°C and then 150°C on separate hot plates for 90 seconds each.
- Load the substrates into the programmable oven SST 3150.
- Ramp to 150°C in Nitrogen at a rate of 10°C/Min.
- Ramp to 350°C in Nitrogen at a rate of 4°C/Min, and cure for 30 minutes at 350°C (the curing profile is shown in Figure 5.2).

- Cool down to ambient.

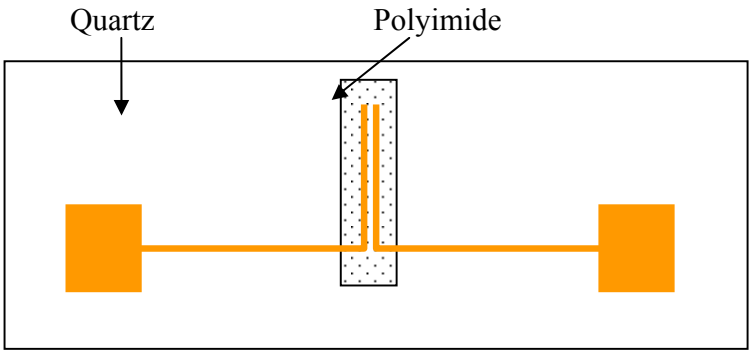


Figure 5.1 Polyimide breakdown testing sample pattern

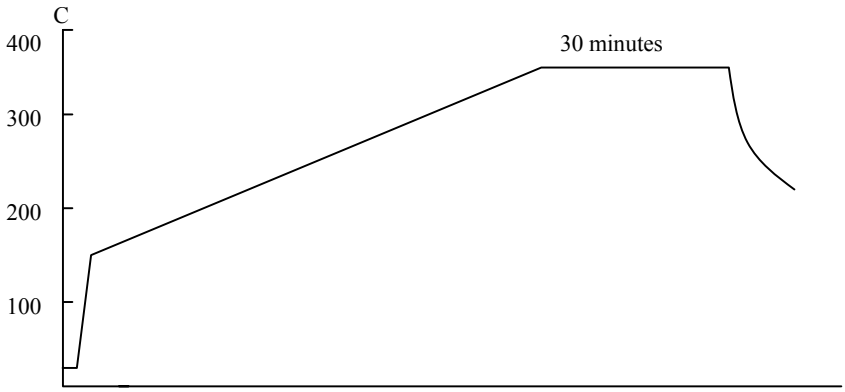


Figure 5.2 Polyimide PI2611 curing profile

After the samples were fabricated, as-built and aged samples (100, 250, 500, 1000 and 2000 hours at 300ºC in an air chamber) were tested using a high temperature probe station. The two contact pads were connected to a computer controlled power supply and a current meter using special probes and cables.

The temperature of the probe station was controlled at 300°C with an accuracy of ±1°C by the Signatone model S-1045 control device. Using a high voltage power supply

capable of supplying up to 5000V, the DC voltage was increased in increments of 50 V until breakdown occurred, and the leakage currents were measured using the current meter. The circuit is illustrated in Figure 5.3.

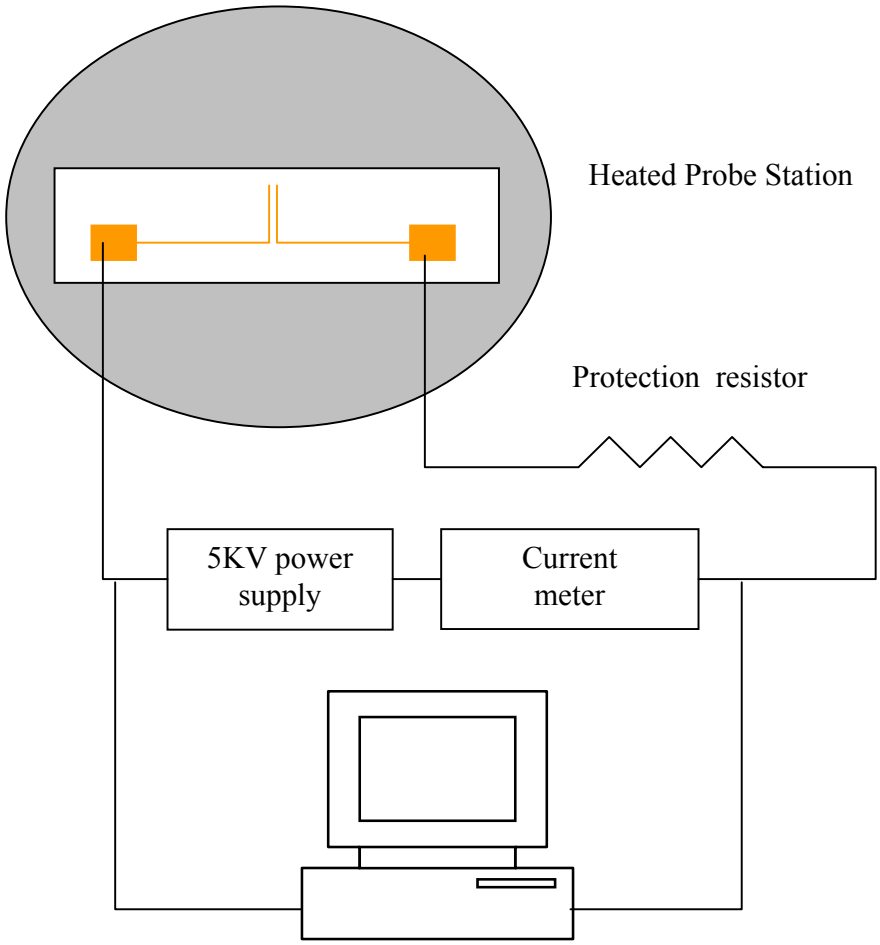


Figure 5.3 Polyimide breakdown measurement circuit schematic

5.2 Experiment Results

Table 5.1 shows the results of the polyimide breakdown test. In the table, "no sign" means that no visible evidence of breakdown was observed either during or after

breakdown test; “bridge” means that black lines were detected in the gap between the traces after the breakdown test; “light” means that blue light was observed in the gap between the traces during the breakdown test; and “burn” means that the polyimide film or circuit traces were burned during the breakdown test.

From Table 5.1 it can be seen that the breakdown voltage had a tendency to increase with increasing aging time. There are several possible reasons for this:

- The polymer was not volatilized completely in the inert gas during the curing process, and there was still some of the residual organic solvent and water (moisture) produced during imidization stage remaining in the as-built polyimide films. When the as-built polyimide films were aged at a high temperature in air, the residual organic solvent and moisture slowly evaporated, thus causing the breakdown voltage to increase.
- Spatial cross-linking of the macromolecules increased with increasing aging time at high temperature, which caused the polyimide structure to be more rigid than the as-built polyimide. This more rigid structure could then lead to a higher breakdown voltage [56].

The decomposition temperature of the PI2611 polyimide is reported to be 620°C [41]. When the as-built samples were aged at 350°C in an air chamber after 100 hours, PI2611 decomposed and evaporated entirely, showing that it was not suitable for applications at 350°C and higher.

Table 5.1 Polyimide breakdown test results

Sample	0		100hr	
	Breakdown voltage (V)	Leakage Current (A)	Breakdown voltage (V)	Leakage Current (A)
1	3450	no sign	3950	no sign
2	3500	bridge	3825	light
3	3700	light	3575	bridge
4	3475	bridge	3450	bridge
5			3425	bridge
Sample	250hr		500hr	
	Breakdown voltage (V)	Leakage Current (A)	Breakdown voltage (V)	Leakage Current (A)
1	4425	burn	4620	burn
2	4800	light	4550	burn
3	over 5000	4.20E-06	4730	burn
4	over 5000	2~20E-08	4900	light
5	over 5000	2~20E-08	over 5000	3.00E-08
6	over 5000	2~20E-08	over 5000	1.20E-07
Sample	1000hr		2000hr	
	Breakdown voltage (V)	Leakage Current (A)	Breakdown voltage (V)	Leakage Current (A)
1	over 5000	5.00E-05	over 5000	3.00E-03
2	over 5000	5.00E-05	over 5000	2.00E-03
3	over 5000	1.00E-08	over 5000	4-16E-08
4	over 5000	1.00E-08	over 5000	4-16E-08
5	over 5000	1.00E-08	over 5000	4-16E-08
6	over 5000	1.00E-08	over 5000	4-16E-08

CHAPTER 6 SIC VJFET DEVICES OPERATING AT EXTREME TEMPERATURES

6.1 INTRODUCTION

There is a growing demand for more efficient, higher power, and higher temperature operation of semiconductor devices to support the latest advancements in extreme environmental conditions in aerospace, automotive, and high power electronics systems. Si power devices have reached their theoretical limits in terms of higher temperature and higher power operation by virtue of the physical properties of the material. SiC has been identified as a material with the potential to replace Si devices because of their superior material advantages such as large bandgap, high thermal conductivity, and high critical breakdown field strength [13]. SiC devices are capable of operating at higher voltages, higher frequencies, and at higher junction temperatures. SiC unipolar devices such as Schottky diodes, VJFETs, and MOSFETs have much higher breakdown voltages compared to their Si counterparts, which make them suitable for use in high voltage applications.

SiC Schottky diodes are already commercially available, and with the advancements in substrate quality and process technology that have been made in the last few years, other SiC devices for power applications will soon follow. It is likely that the

next power device offering will be a unipolar transistor such a MOSFET or JFET. Unipolar devices have the particular advantage for power applications of having a positive temperature coefficient. That is, as temperature increases, the on resistance of the device increases. Because the current decreases as the device heats up, devices can be paralleled without concern of thermal runaway [57]. The SiC JFET is of particular interest because the JFET is not so sensitive to the oxide interface and reliability issues, while SiC MOSFET currently suffers from low channel mobility [58] and may have reliability problems when operated under both high electric fields and high temperatures [59].

Vertical junction power field effect transistors (VJFET) in SiC are especially attractive for high power applications because of the inherent stability of the p-n junction gate and the basic maturity of all aspects of the JFET technology in SiC. The VJFETs described herein, provided by SemiSouth Laboratories, Inc., were fabricated on 4H-SiC n+ substrates with epitaxially grown n type drift and channel layers. Source fingers were defined by dry etching. Al+ was implanted into the etched trenches to form the p+ gate regions. After implant activation, the trenches were filled with oxide followed by the formation of ohmic contacts and contact pads [56]. Figure 6.1 shows a typical cross-section trench-implanted VJFET [60]. As seen, the gates are recessed, and the conduction path is vertical (the high current carrying terminals, namely the source and the drain are placed on the top and bottom of the wafer respectively). This gives a higher packing density (as the chip area is greatly reduced) and many devices can be placed in parallel. VJFET is simpler to fabricate because it (i) does not need the expensive epitaxial re-growth, (ii) eliminates the lateral JFET, making it possible to achieve near theoretical

performance over a wide voltage range, and (iii) only one mask requires critical alignment [61]. VJFETs with different blocking capabilities in a single fabrication run can be realized by simply using the appropriate thickness and doping concentration for the drift layer [61].

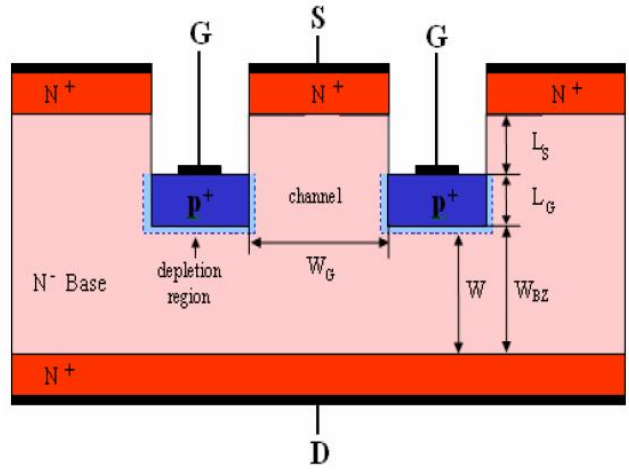


Figure 6.1 Cross-sectional view of a SiC VJEFT [60]

Structures like those in Figure 6.1 exhibit two distinct modes of conduction, unipolar and bipolar. In the unipolar mode (Figure 6.2) [60], the JFET acts as a majority carrier device, where electrons flow from the source to the drain. For the cross-section shown in Figure 6.1, there is a depletion region at the gate-N- base layer interface from either a p-n or Schottky metal junction depending on the gate configuration.

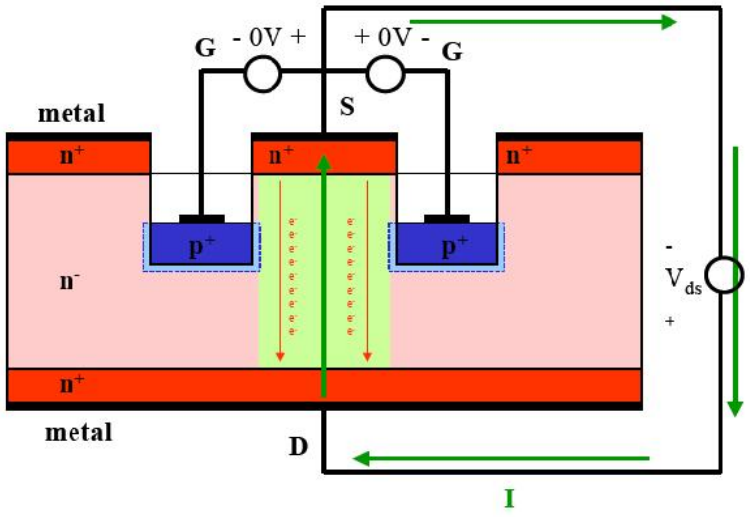


Figure 6.2 VJFET in unipolar mode [60]

The width of this depletion region can be controlled by the magnitude of V_{gs}. As V_{gs} becomes increasingly negative, the channel that forms has a width equal to the distance between the two depletion regions. The variation of the width of the depletion region can be seen in Figure 6.3 [60]. For sufficiently negative gate voltages, the channel is "pinched off" (Figure 6.4) due to the intersecting depletion regions.

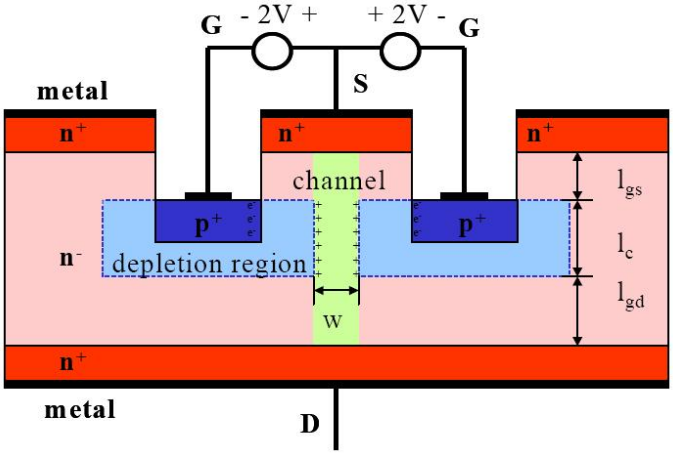


Figure 6.3 Variation of width of depletion region [60]

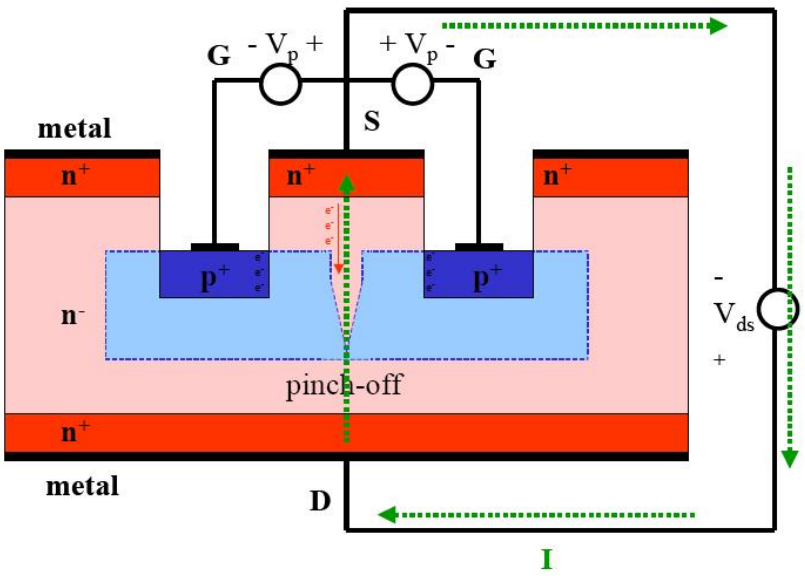


Figure 6.4 Pinch-off condition in the JFET [60]

In the bipolar mode, the gate voltage is positive relative to the source such that the gate-source junction becomes forward biased. The forward-biased junction injects minority carrier holes into the channel, thus reducing the on-state resistance of the device. This gives the device greater power handling capability. Figure 6.5 illustrates the bipolar mode of operation in the JFET [60].

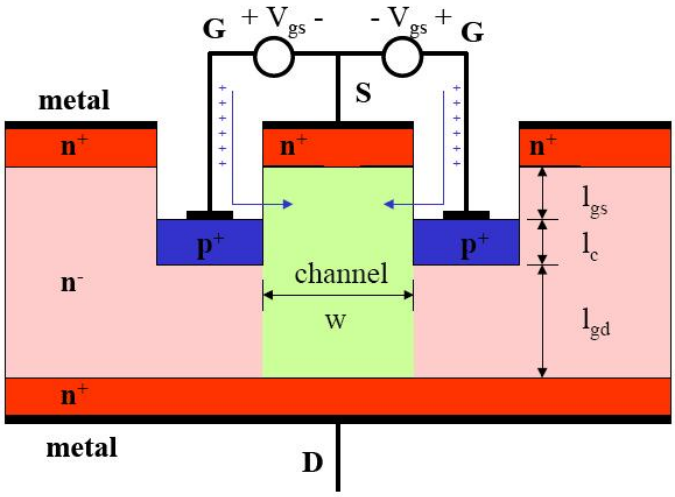


Figure 6.5 JFET operating in the bipolar mode [60]

Individual devices are applicable to kilowatt-class power supplies requiring 5- to 10-A, 600-V or 1200-V ratings. Because the 4H-SiC VJFETs reported here are 100% unipolar, they can be easily paralleled to form equivalent switches of much greater current; meaning hundreds of amperes [62]. This makes the possibility of developing IGBT replacements a realistic goal. The resulting scaled switch can then have average and surge current ratings comparable to silicon IGBTs while exhibiting switching properties like silicon MOSFETs, but lower thermal resistance and higher rated junction temperature than available in silicon because of the thermal properties of silicon carbide. This part of work demonstrated the feasibility of paralleling SiC power VJFETs to develop Si IGBT replacements.

6.2 Performance of SiC VJFETs at Extreme Temperatures

6.2.1 VJFET Packaging Process

The VJFET package approach used a Mo tab (200mil x 200mil, front side: 12μm Au, backside: 30μm Ni/0.3μm Au) bonded on ceramic substrate as the die attach substrate for the AuIn alloy (81/19 wt%) TLP bonding process and fine Au wire thermosonic ball bonding to connect the SiC die with the leads in order to reduce the impact of the bonding force and ultrasonic energy. The VJFET substrate fabrication was as follows:

- Saw the metallization (Cu/Ni/Au, thickness: 250μm/6μm/0.3μm) on the Al_2O_3 ceramic substrate into three separate parallel parts, the middle one was used as the Mo tab attaching metallization, the other two parts were used as the JFET external gate and source leads;
- Electroplate thick Au (3-5μm) on the ceramic substrate metallization;
- Braze the Mo tabs backside metallization with the middle ceramic substrate metallization using Ag-Cu alloy perform (133mil x 133mil x 2mil, 72/28 wt%) in high temperature chamber in nitrogen ambient (the profile is shown in Figure 6.6);
- Polish the gate and source lead metallization to eliminate the Cu diffused on the surface during the high temperature brazing process;
- Electroplate thick nickel (10μm) onto the gate and source leads;
- Electroplate thick Au (10μm) onto the gate and source leads;
- Electroplate thick Au (10μm) onto the Mo tab.

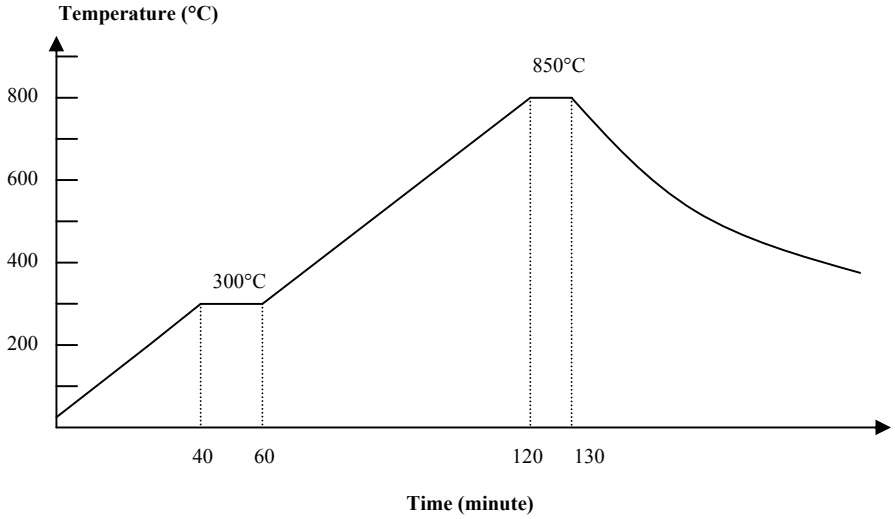
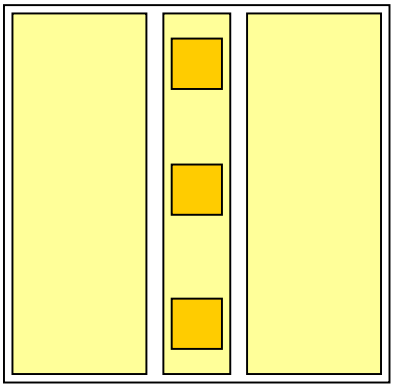
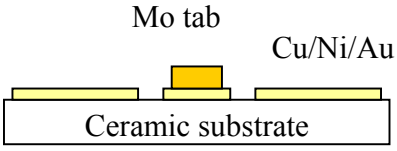


Figure 6.6 Ag-Cu brazing profile

The VJFET substrate structure is shown in Figure 6.7. According to the work described in the Chapter 3, Cu diffused into the AuIn layer and formed weak intermetallics with In. The Mo tab served as a high temperature diffusion barrier between the Au-In die attach and the Cu foil on the substrate. The Mo tab also served as a CTE buffer between the SiC die and the copper foil. Thick nickel and Au were electroplated on the gate and source lead metallization after AgCu brazing in order to prevent Cu diffusion during the following TLP bonding process and provide good wire bondability in the Au wire bonding step. Thick Au was electroplated on the Mo tab in order to provide the excess Au to shift the solidus temperature of the AuIn alloy.



(a) Top view



(b) Cross-section

Figure 6.7 Substrate structure for VJFET package

After the substrate was fabricated, four VJFET dies were attached onto the Mo tab using the AuIn TLP bonding process described in section 3.2. One of the VJFET die was wire bonded first. One 1.0mil Au wire was bonded from the gate contact to the external gate lead, ten 1.5mil Au wires were bonded from the source contact to the external source lead to provide high electrical current capability. The forward characteristics at room temperature were tested using a Sony Tektronix 371 high voltage curve tracer; the pinch-off voltage V_p as a function of temperature was measured using an HP 4145 semiconductor parameter analyzer. Then, the other three VJFET dies were added in parallel by bonding the gate and source wire bonds as was done for the first die. The four dies were paralleled as shown in Figure 6.8. The forward characteristics as a function of temperature were measured using a Sony Tecktronix 371 curve tracer; the pinch-off

voltage V_p and the drain-source leakage current as a function of temperature were measured using an HP 4145A analyzer.

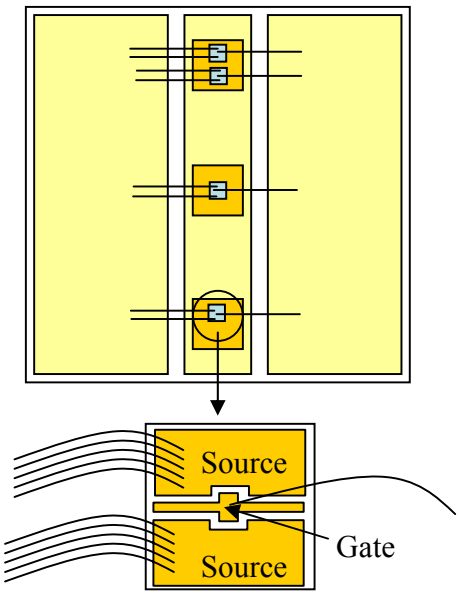


Figure 6.8 Paralleled VJFET package structure

6.2.2 DC Characterization of Paralleled VJFETs

Figure 6.9 shows the comparison of the forward characteristics between the paralleled VJFETs and a single VJFET at room temperature. The forward current was about 11.38A for the paralleled VJFETs at V_{ds} equal to 5V and V_{gs} equal to 2V, and that was about 2.28A for the single VJFET at the same V_{ds} and V_{gs} conditions. The paralleled VJFETs formed an equivalent switch of much greater current at low on-state voltage.

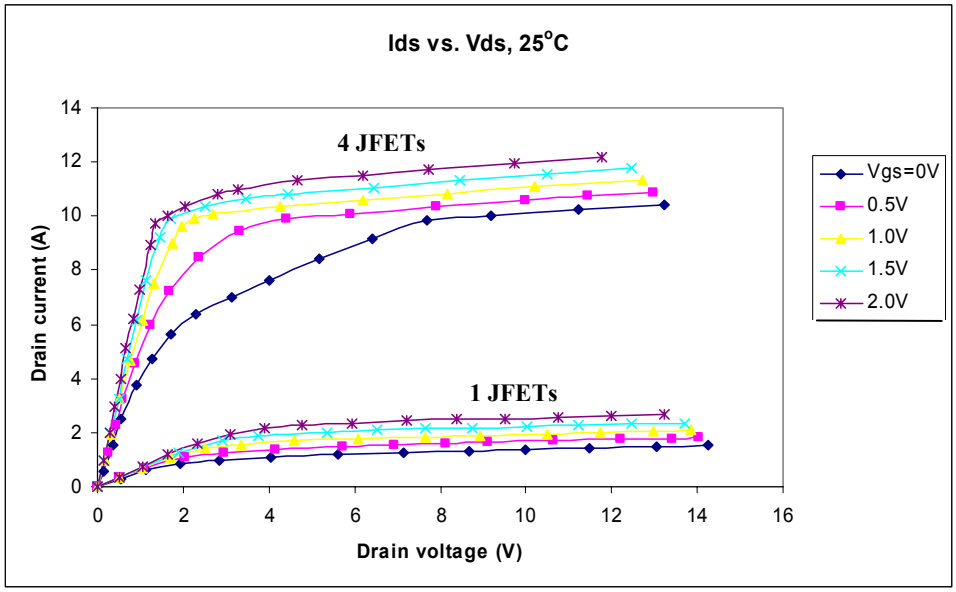


Figure 6.9 Forward characteristics of the paralleled VJFETs and single VJFET

Figure 6.10 provides a plot of drain current as a function of temperature for the paralleled VJFETs operated between 25°C and 400°C. The paralleled VJFETs device showed a positive temperature coefficient. In this figure, with V_{gs} = 2 V and V_{ds} = 5 V, I_{ds} decreases to around 27% of the room temperature value at a temperature of 400ºC, which meant that as temperature increased, the on resistance of the device increased. Because the current decreased as the device heated up, there is no concern of thermal runaway for the paralleled VJFETs. It should be noted that these VJFET dies are normally on in the sense that a small positive gate-source bias produces a lower on resistance.

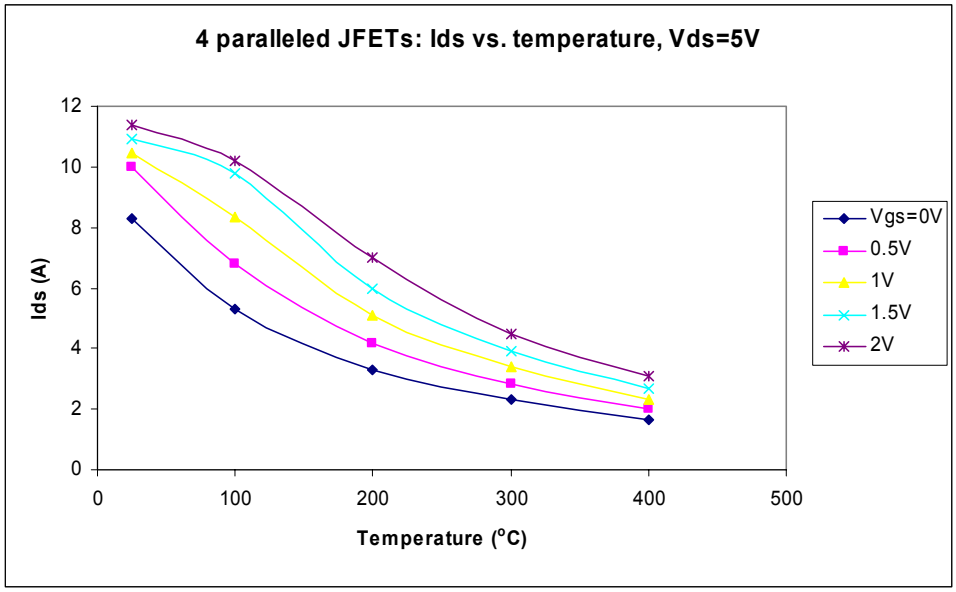


Figure 6.10 Drain current as a function of temperature for paralleled VJFETs

Figure 6.11 illustrates a comparison of the pinch-off voltage as a function of temperature for the paralleled VJFETs and a single JFET operated between 25°C and 400°C at V_{ds} equal to 5V. The paralleled VJFETs had a pinch-off voltage V_p of -3.7V, while the single VJFET had -3.36V at 25°C. Both the paralleled VJFETs and single VJFET showed a slight decrease in V_p with increasing temperature.

Figure 6.12 shows the source-drain leakage current as a function of temperature for the paralleled VJFETs and single VJFET operated between 25°C and 400°C when V_{gs} was -6V, and V_{ds} was 5V. The paralleled VJFETs had a higher I_{ds} than the single VJFET. And both the paralleled VJFETs and single VJFET showed an increase in I_{ds} with increasing temperature. The I_{ds} of the paralleled VJFETs is less than 0.8μA at 400°C.

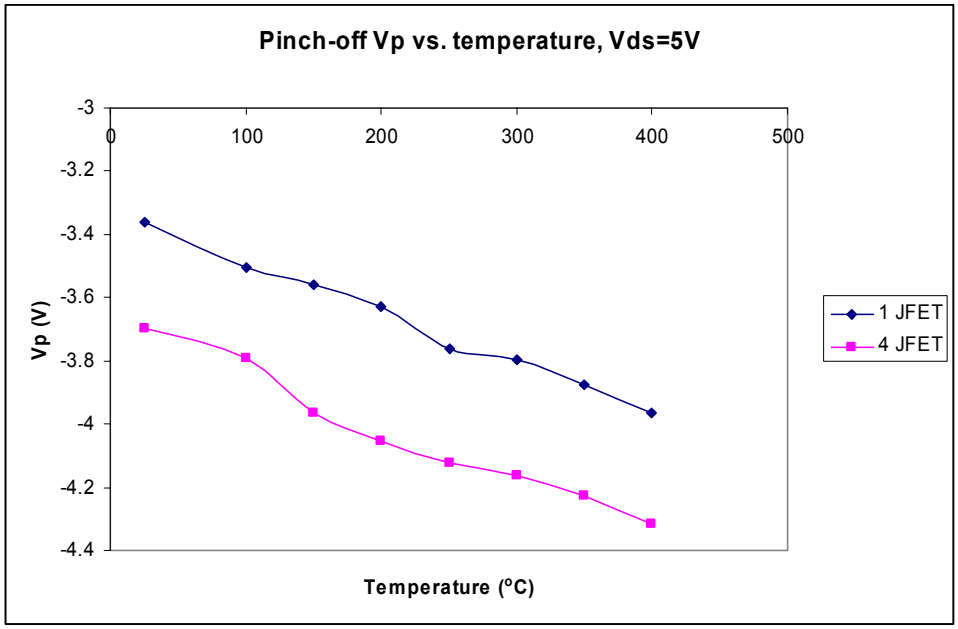


Figure 6.11 V_p vs. temperature for the paralleled VJFETs and single JFET

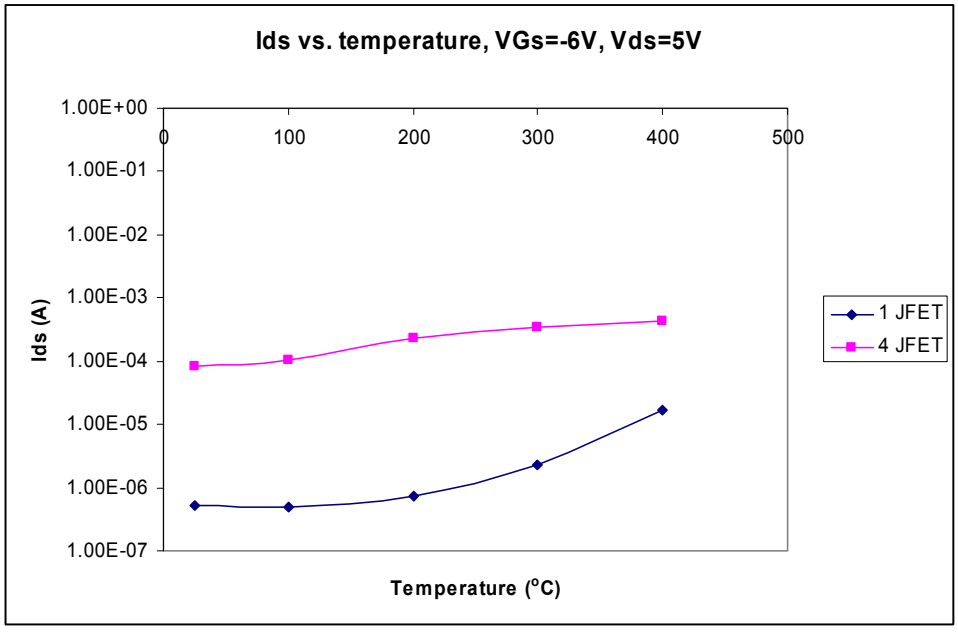


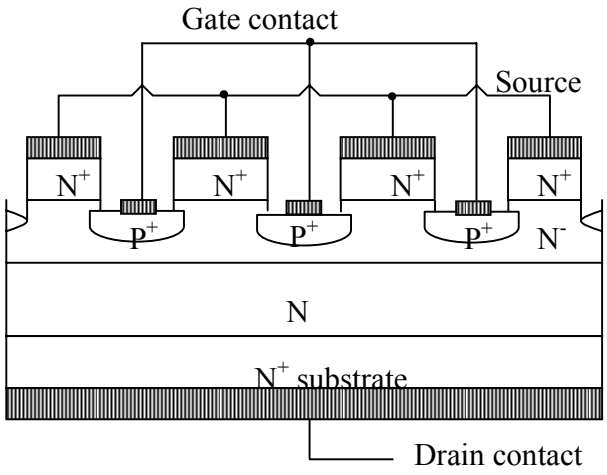
Figure 6.12 I_{ds} vs. temperature for the paralleled VJFETs and single VJFET

6.3 Performance of SIT Diode Operating at Extreme Temperatures

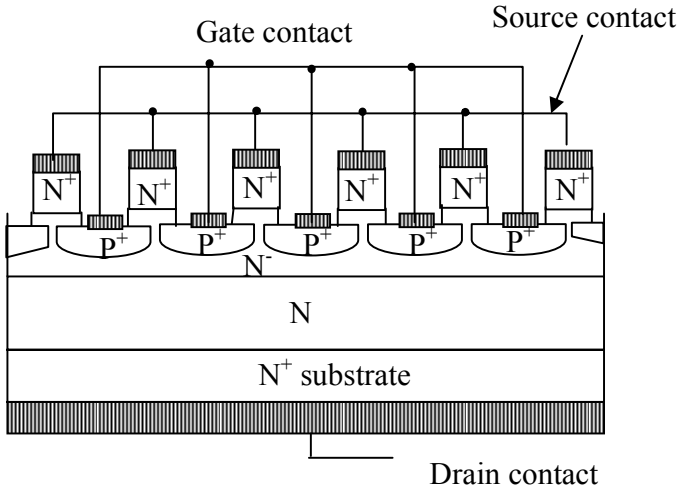
6.3.1 SIT Diode

An advantage of the VJFET presented here is that one can shift the threshold voltage negative or positive by widening or narrowing the nominal source finger width, respectively [56]. Figure 6.13 shows the structure of a "normally-on" and "normally-off" VJFET. If the devices have a negative V_T, they are "normally-on" at zero source-gate bias, while others have a small negative or slightly positive V_T and are therefore "normally-off" at zero source-gate bias. In general, the more "on" a JFET is, the lower the specific on resistance. However, the more negative V_T, the more gate bias is required to pinch the drain current off, especially at high drain voltages. Normally-off JFETs typically require very small negative gate biases to block the rated maximum voltage, but usually suffer from much lower saturation current than normally-on devices.

By shorting the gate-source terminals of a normally-off VJFET, the device will act as a so-called static induction transistor (SIT) diode [63]. The SIT diodes have low cut-on voltage, and low reverse leakage current. Paralleled SIT diodes result in a lower on-state voltage, primarily due to the gain resulting from majority carrier injection over the channel potential barrier induced by minority carrier injection from the forward-biased gate-drain junction [63]. This becomes an especially attractive feature when high forward currents are concerned.



(a) Normally-on



(b) Normally-off

Figure 6.13 "Normally-on" and "normally-off" VJFET

6.3.2 SIT Diodes Packaging Process

Three VJFET dies were attached to a Mo tab on a substrate using the same process described in section 6.2. One of the VJFET die was wire bonded first. One 1mil Au wire was bonded from the gate contact to the external source lead, and ten 1.5mil Au wires were bonded from the source contact to the external source lead to provide large

electrical current capability. The forward characteristics of the single SIT diode at room temperature were tested with a Sony Tektronix 371 high voltage curve tracer and an HP 4145A analyzer. Then, the other two VJFET dies were added in parallel by bonding the gate and source wire bonds. The three dies were paralleled as shown in Figure 6.14. The forward, reverse, and breakdown characteristics of the paralleled SIT diodes as a function of temperature were tested with a Sony Techtronics 371 high voltage curve tracer and an HP 4145A analyzer.

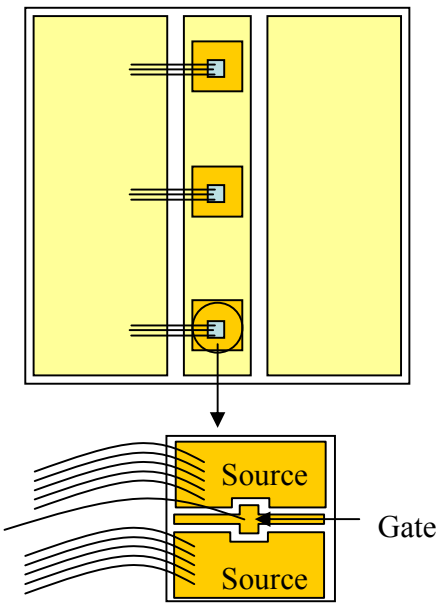


Figure 6.14 Paralleled SIT diodes package structure

6.3.2 DC Characterization of Paralleled SIT Diodes

Figure 6.15 shows the forward characteristics for the single SIT diode at room temperature. Figure 6.16 shows the forward characteristics as a function of temperature for the paralleled SIT diodes. The single SIT diode had a cut-on voltage of 1.35V, while

the paralleled SIT diodes had a lower cut-on voltage of 1.25V at room temperature. The paralleled SIT diodes also showed a decrease in cut-on voltage with increasing temperature.

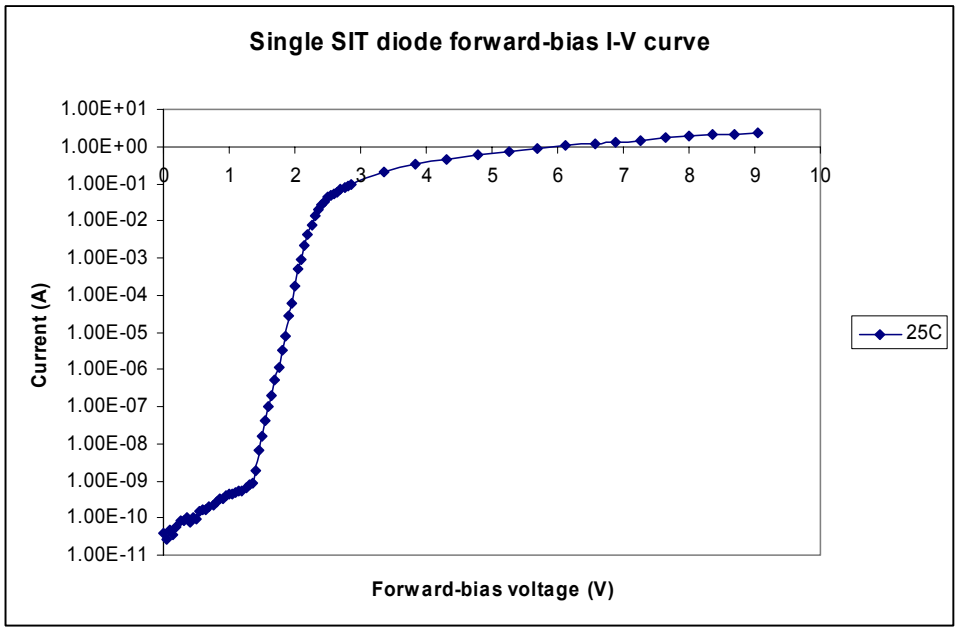


Figure 6.15 Forward characteristics for the single SIT diode

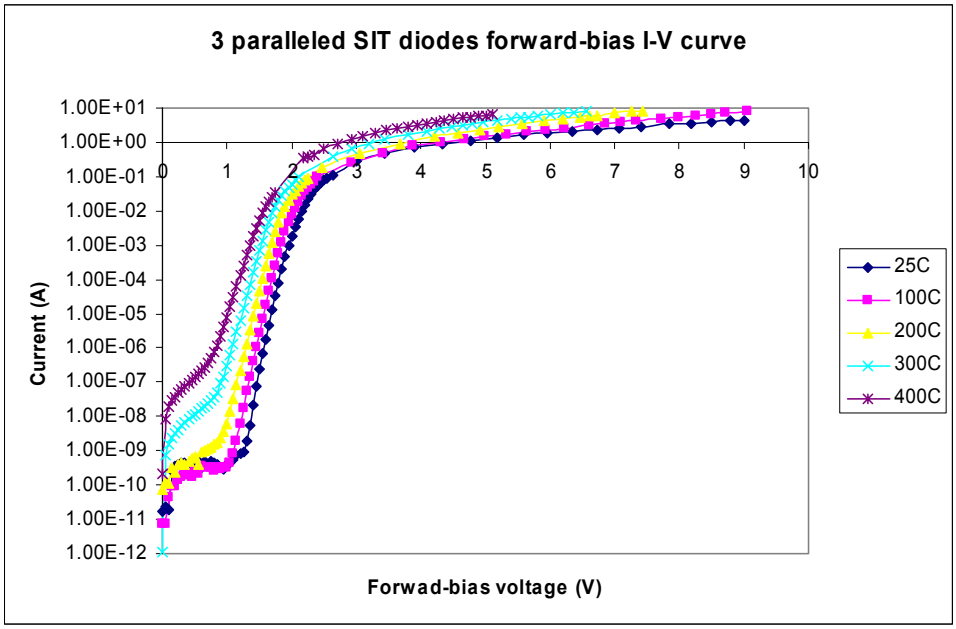


Figure 6.16 Forward characteristics for the paralleled SIT diode

Figure 6.17 shows the reverse characteristics as a function of temperature for the paralleled SIT diodes. Reverse bias measurements up to 100V showed that leakage current increases by only an order of magnitude from room temperature to 400°C. The leakage current of the paralleled SIT diodes was less than 70 µA at V_{ds} = 100 V at 400°C, validating the impressive blocking performance of the SIT diode at extreme temperatures. The paralleled SIT diodes showed a decrease in breakdown voltage with increasing temperature as shown in Figure 6.18; the breakdown voltage was 128V at 400°C.

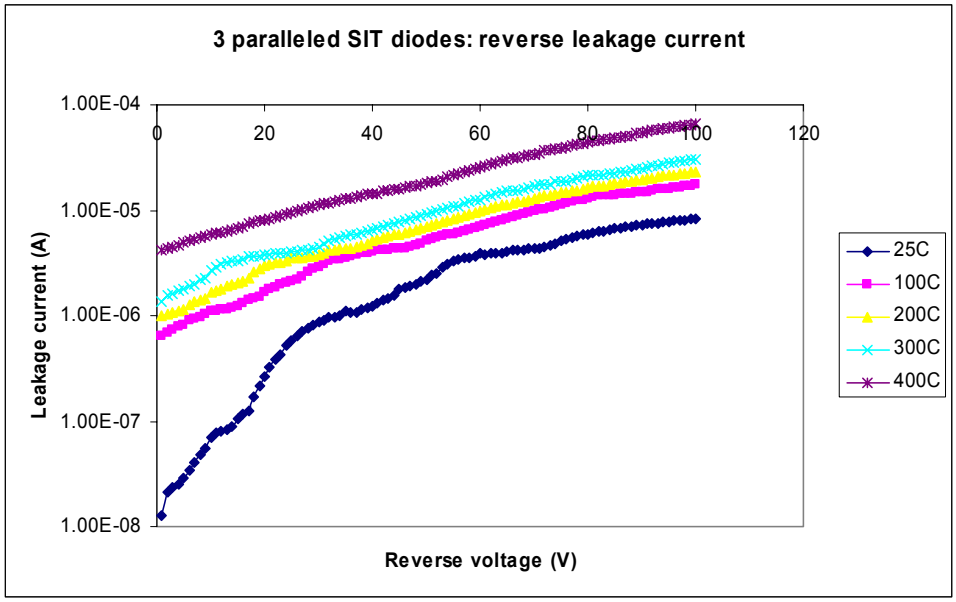


Figure 6.17 Reverse characteristics for the paralleled SIT diodes

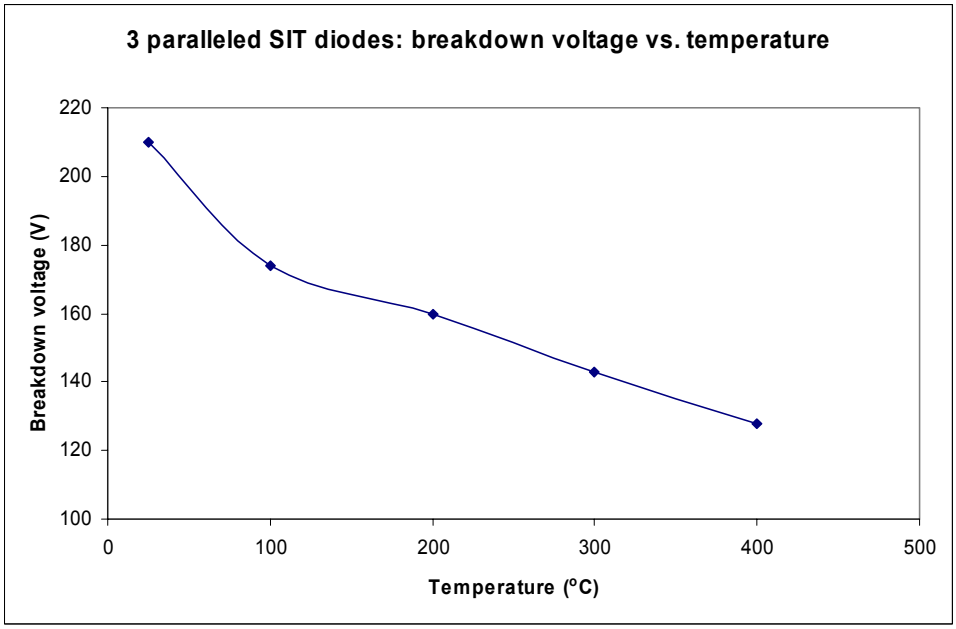


Figure 6.18 Breakdown voltage for the paralleled SIT diodes

6.4 SUMMARY

The paralleled VJFETs formed an equivalent switch of much greater current than the single VJFET, and showed a positive temperature coefficient of on-resistance. Because the current decreased as the device heated up, there is no concern of thermal runaway for the paralleled VJFETs which allows many devices to be paralleled to scale the power handling of the composite switch to whatever value is required. The paralleled VJFETs had a lower negative pinch-off voltage V_p than the single VJFET. The V_p decreased slightly with increasing temperature for both the paralleled VJFETs and single VJFET. The paralleled VJFETs showed an increase in source-drain leakage current I_{ds} with increasing temperature. The I_{ds} was less than 0.8μA when V_{gs} was -6V, and V_{ds} was 5V at 400°C. The VJFET will be a highly versatile device for extreme temperature application.

Paralleled SIT diodes resulted in a lower cut-on voltage than the single SIT diode. The cut-on voltage and on-state voltage decreased with increasing temperature. Reverse bias measurements up to 100V showed that leakage current increases by only an order of magnitude from room temperature to 400°C. The leakage current of the paralleled SIT diodes was less than 4 μA at V_{DS} = 100 V at 400°C, and the breakdown voltage was 128V at 400°C, validating the impressive blocking performance of the SIT diode at extreme temperatures.

CHAPTER 7 CONCLUSON

7.1 TRANSIENT LIQUID PHASE BONDING PROCESS

Based on the high melting point of Au-In alloy (81/19 wt%), it was evaluated as a potential high temperature die attach material using a transient liquid phase bonding process in this study. The die shear strength of samples fabricated with the thin Au die-to-thick Ag substrate combination remained above 100kg-f after 2000 hours storage at 450ºC in air, samples fabricated with the thick Au die-to-Au substrate combination degraded after 2000 hours storage at 450ºC in air, and samples fabricated with the thin Au die-to-Mo tab degraded after 2400 wide temperature range (35-400°C) cycles.

This is the first time in the packaging industry to report that vertical cracks developed in the die attach on Mo tabs during the thermal cycling tests and indium segregated to the defects (voids and cracks) during the high temperature storage and thermal cycling tests. Indium surface enrichment of evaporated Au-In thin films has been reported at room temperature [57]. This segregation does appear to negatively impact the reliability of the die attach.

7.2 BARRIER MATERIAL EVALUATION

The 6μm of nickel or nickel phosphorous commonly used as barrier layer in conventional ceramic substrate metallization did not prevent Cu diffusion to the surface

at a temperature of 450°C. This dissertation reports the first investigation of a multi-layer nickel phosphorous structure which was found to serve as a good barrier to prevent Cu diffusion for high temperature applications. Based on an AES analysis, no copper appeared on the coupon surface even after 2000 hours of aging at 450ºC.

7.3 Large Diameter Wire Bonding

The bondability and reliability of large diameter gold and platinum wire using thermosonic wedge bonding was investigated. Reliability tests based on bond shear and pull strength showed that large diameter (250μm) gold and platinum wire had good bondability on ceramic substrate thick metallization (Cu/Ni/Au) and good reliability with 350ºC aging. Platinum wire bonds had higher strength than gold wire.

For SiC/Ni_2Si/SiO_2/Ti/TiW/Au metallization, Au wire bonds had good reliability with 300ºC aging, while 2 of 15 Pt wire bonds had bond lifts during pull testing after 2000 hours of aging. For SiC/Ni_2Si/SiO_2/Ti/Pt/Au metallization, 10 of 16 Au wire bonds had bond lifts during pull testing after 1000 hours of aging, and 5 of 14 Pt wire bonds had bond lifts during pull testing after 250 hours of aging.

A simplified FEMA 2D model was used to understand the effects of bond force and die metallization structure on the failure mode. The results matched the experimental results very well. The best combination was Au wire on a Ti/TiW/Au pad stack over PECVD SiO_2. This work demonstrated the effects of wire and pad stack metallurgy on bond reliability.

The metallization stack Ta-Si-N (2%)/Pt-N/Au had good reliability with gold wire bond for applications at 350ºC. More work needs to be done to investigate the reliability for applications at higher temperatures.

7.4 High Temperature, High Power Passivation

The decomposition temperature of the PI2611 polyimide is reported to be 620°C [41]. PI2611 as a thin coating was found to decompose after 100 hours of aging at 350°C. PI2611 can only provide good passivation for power devices at 300°C or lower.

7.5 4H-SiC VJFETs Devices Operated at Extreme Temperatures

The paralleled VJFETs formed an equivalent switch of much greater current than the single VJFET, and showed a positive temperature coefficient of on-resistance. Because the current decreased as the device heated up, there is no concern of thermal runaway for the paralleled VJFETs, which allows many devices to be paralleled to scale the power handling of the composite switch to whatever value is required. The source-drain leakage current I_{ds} of the paralleled VJFETs was less than 0.8μA when V_{gs} was -6V, and V_{ds} was 5V at 400°C.

Paralleled SIT diodes resulted in a lower cut-on voltage than the single SIT diode, and the cut-on voltage decreased with increasing temperature. Reverse bias measurements up to 100V showed that leakage current increases by only an order of magnitude from room temperature to 400°C. The leakage current of the paralleled SIT diodes was less than 70 μA when V_{ds} = 100 V at 400°C, and the breakdown voltage was

128V at 400°C, validating the impressive blocking performance of the SIT diode at extreme temperatures. This was the first reported measurement of SIT diode characteristics at high temperatures.

7.6 Recommendations for Packaging SiC High Power, High Temperature Devices

Based on the studies reported in this dissertation, the packaging options for SiC high temperature, high power devices are recommended as following:

- Die attach: die-to-thick Ag substrate combination using AuIn transient liquid phase bonding for application temperatures up to 450ºC with limited thermal cycle requirements; die-to-Mo tab combination for application with high thermal cycle requirements.
- Wire bonding: 10mil or less diameter Au wire bonding on a Ti/TiW/Au pad stack over PECVD SiO_2 for application temperatures up to 300ºC; on a pad stack Ta-Si-N (2%)/Pt-N/Au for application temperatures up to 350ºC.
- Passivation: Polyimide PI2611 for application temperatures up to 300ºC.

7.7 Recommendations for Future Work

Based on the results presented in this dissertation, some recommendations for future work are as follows:

- Develop a new process to eliminate the hydrogen entrapped in plated films to decrease void formation and improve the die attach reliability;

- Investigate compatibility and reliability of the multi-layer nickel phosphorous structure to prevent Cu diffusion in the AuIn die attach process, which will eliminate the crack in the die attach;
- Investigate die attach with thick Ag plated on Mo tabs;
- FEMA simulation with the combination of bond force, ultrasonic energy, metallization structure and thickness to fully understand the wire bonding failures such as cratering, peeling and cracking;
- New passivation materials need to be developed and evaluated for use at higher temperature.

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