COMPACT MODELING OF SIGE HBTS USING VERILOG-A

Except where reference is made to the work of others, the work described in this thesis is my own or was done in collaboration with my advisory committee. This thesis does not include proprietary or classified information.

_____

Zhiming Feng

Certificate of Approval:

_____	_____
Bogdan M. Wilamowski Professor Electrical and Computer Engineering	Guofu Niu, Chair Professor Electrical and Computer Engineering
_____	_____
Lloyd Stephen Riggs Professor Electrical and Computer Engineering	Stephen L. McFarland Dean Graduate School

COMPACT MODELING OF SIGE HBTS USING VERILOG-A

Zhiming Feng

A Thesis

Submitted to

the Graduate Faculty of

Auburn University

in Partial Fulfillment of the

Requirements for the

Degree of

Master of Science

Auburn, Alabama
August 7, 2006

COMPACT MODELING OF SiGe HBTs USING VERILOG-A

Zhiming Feng

_____
Signature of Author

_____
Date of Graduation

VITA

Zhiming Feng, son of Baogui Feng and Wenzhen Bian, was born on 29 April, 1973, in Daan, Jilin Province, P. R. China. He received his BS degree from Jilin University in 1995, majoring in Electronics and Information Systems. In Spring 2003, he was accepted into the Electrical and Computer Engineering Department of Auburn University, Auburn, Alabama, where he has been pursuing his Masters degree.

THESIS ABSTRACT

COMPACT MODELING OF SIGE HBTS USING VERILOG-A

Zhiming Feng

Master of Science, August 7, 2006
(B.S., Jilin University, July, 1995)

123 Typed Pages

Directed by Guofu Niu

SiGe HBTs, integrated with CMOS, have demonstrated their usefulness in digital and analog circuit designs for wired and wireless telecommunication applications over the past decade. Of critical importance to successful circuit design is the availability of accurate device compact models and a good understanding of internal device characteristics, especially for analog RFIC designs.

A technique that is beginning to be applied in research on device physics and compact modeling based on the Verilog-A hardware language is presented in this thesis. This new Verilog-A based model can be easily modified and implemented into circuit simulators such as Cadence and Agilent ADS without the need to interface with simulators. Moreover, the internal currents, charges, and noise sources are accessible, which is not the case when built-in models are used in circuit simulators. Using the Verilog-A based VBIC model, three applications for SiGe HBT noise modeling and VBIC temperature mapping models are presented.

First, a new inverse circuit simulation based low frequency noise extraction method is proposed based on the Verilog-A based VBIC model. The low frequency noise of device biasing at high currents can be measured more accurately through this method. Secondly, in order to better understand the different phase noise upconversion mechanisms involved in the base current $1/f$ noise and base current short noise in oscillator designs, the internal I_{BE} and the internal I_{CE} were separated from the external I_{BE} and the external I_{CE} using the Verilog-A based VBIC model. Clearly, the noise generating current, I_{BE}, is only a small portion of the terminal I_B. In the third application, a group of improved temperature mapping models that can be used to model of DC currents down to 43 K are presented. The new VBIC based model was implemented using Verilog-A, compiled into binary code, and dynamically linked to a circuit simulator through its compact modeling interface. Excellent Gummel and output fitting across a wide temperature range from 300 K down to 43 K were achieved on a 50 GHz SiGe HBT device.

Finally, the intermodulation linearity simulation capability of the VBIC, HICUM and Mextram models were evaluated using harmonic balance in a 200 GHz SiGe HBT technology. The impact of avalanche and selfheating on IIP3 were examined and a weak avalanche shown to have a significant impact on IIP3. These results provide valuable new insights into the device physics underlying linearity behavior and the use of quantified simulations for data comparison of linearity that will be useful for both designers and modelers.

ACKNOWLEDGMENTS

I would like to express my gratitude to my supervisor, Dr. Guofu Niu. Without him, this thesis would not have been possible. His patience and encouragement have carried me through difficult times, and his insights and suggestions have helped to shape my research skills. I would also like to thank the other members of my committee, Dr. Bogdan Wilamowski, and Dr. Lloyd Stephen Riggs for the assistance they have provided.

I would like to thank Ying Li, Chendong Zhu, and Laleh Najafizadeh for helping with device measurement, and Jun Pan for useful discussions on Cadence simulation tools. I thank all the students in our research group, Yan Cui, Jin Tang, Xiaoyun Wei, Kejun Xia, Yun Shi, Hua Yang, and Muthubalan Varadharajaperumal for the vivid discussions we have had on various topics and the fun of being a member of this fantastic group. I am forever indebted to my family for the support they have provided me through my entire life, and in particular I must acknowledge my wife and best friend, Yan Cui, without whose love, encouragement and editing assistance, I would not have finished this thesis.

This research would not have been possible without the financial assistance of the National Science Foundation under grants ECS-0119623 and ECS-0112923, NASA grant NNL05AA37C, and the Georgia Electronic Design Center at Georgia Tech. I am also grateful for the assistance of C. Moore, M. Watson, M. Beatty, L. Nadeau of NASA, E. Kolawa of JPL, and the IBM SiGe development group, as well the many contributions

of the SiGe ETDP team, including: M. Mojarradi, B. Blalock, W. Johnson, R. Garbos, R. Berger, F. Dai, L. Peltz, A. Mantooth, P. McCluskey, M. Alles, R. Reed, A. Joseph, C. Eckert and J.D. Cressler.

Style manual or journal used IEEE Transactions on Nuclear Science (together with the style known as "aums"). Bibliography follows van Leunen's *A Handbook for Scholars*.

Computer software used The document preparation package TEX (specifically LATEX) together with the departmental style-file `aums.sty`. The plots were generated using VossPlot® and MATLAB®.

TABLE OF CONTENTS

List of Figures

LIST OF TABLES

CHAPTER 1

INTRODUCTION AND OVERVIEW

SiGe HBTs (heterojunction bipolar transistors), integrated with CMOS, have demonstrated their superior abilities in digital and analog circuit designs for wired and wireless telecommunication applications in recent years. Tremendous advances in fabrication technology have led to the extreme scaling down of devices with corresponding performance improvements. A 350 GHz peak f_T SiGe technology was announced in 2003 [1], that has led to the highest speed yet among current technologies. The rapid development of this technology has made the study of device characteristics and modeling a high priority due to the unpredictable new features that have appeared with this device scaling. Of critical importance to successful circuit design is the ability to implement accurate device compact models, along with a good understanding of internal device characteristics, especially for analog RFIC design. This indicates the need for a detailed study of device characteristics and compact modeling techniques. Another important aspect is the ease of modifying existing device compact models to keep pace with the rapid development of modern technology and deal with the new features that continuously arise with device scaling. This requires an improvement in the language tools used to write portable device compact models that can be used with circuit simulators such as Cadence and Agilent ADS. Moreover, mankind's exploration of the universe calls for robust circuit designs that will function in the extreme temperature environments found

outside the Earth's atmosphere. Accurate device modeling over a wide temperature range has desperately needed.

This thesis investigates both device physics and compact modeling using a new technique – the Verilog-A based VBIC (Vertical Bipolar Inter-Company) model, which makes a portable device compact model for device simulator that can be easily modified and implemented into circuit simulators without the need to interface with the simulators. Moreover, the internal currents, charges, and noise sources are accessible, which is currently not the case for the built-in models used in circuit simulators. Based on the Verilog-A based VBIC model, three applications for SiGe HBT noise modeling and VBIC temperature mapping models are presented. This introductory chapter briefly reviews the basic principles of SiGe HBT, and provides an overview of the thesis.

1.1 Basic Principles of SiGe HBT

This section gives a brief overview of the DC and *ac* performance abilities of SiGe HBTs. Only the final results are included. Detailed derivations can be found in [2].

The fundamental differences between the SiGe HBT and Si BJT (bipolar transistor) are emitter-base (EB) and collector-base (CB) Si-SiGe heterojunctions. The essential operational differences between SiGe HBT and Si BJT can be illustrated by considering the schematic energy band diagram shown in Fig. 1.1. For simplicity, assume a constant doping in the emitter, base and collector regions. The Ge mole fraction is linearly graded from 0% near the EB junction to some maximum value near the CB junction. This graded Ge profile creates an accelerating electric field in the neutral base.

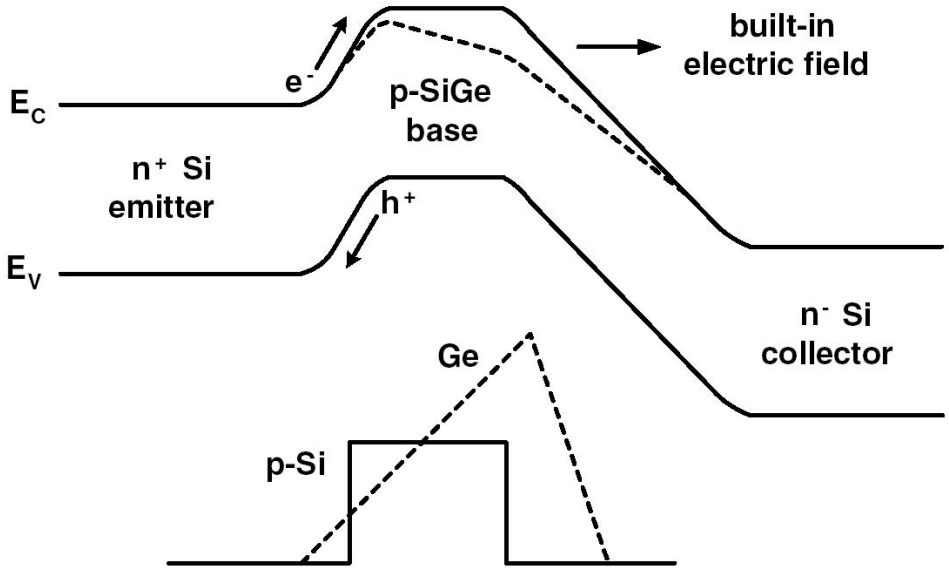


Figure 1.1: Energy band diagram of a graded-base SiGe HBT as compared to an identically constructed Si BJT.

Germanium has a bandgap of 0.66 eV, which is considerably smaller than Silicon's bandgap of 1.12 eV. Hence, SiGe's bandgap is less than the bandgap of Si and there is a roughly 7.5 meV band offset per 1% Ge. Adding Ge in the base primarily affects the DC performance of SiGe HBT through the collector current density J_C, which is proportional to the minority carrier (electron) density in the base region. The Ge-induced bandgap offset exponentially increases the intrinsic carrier density and hence increases the minority carrier density in the base region, leading to an increase in J_C. Meanwhile, because the emitter region is the same for both SiGe HBT and Si BJT, the base current density J_B is roughly the same. The Gummel curves for a SiGe HBT and a Si BJT are compared in Fig. 1.2. The SiGe HBT and Si BJT have been identically processed to

allow unambiguous comparison. The SiGe HBT clearly has a much higher J_C than the Si BJT, although it has a similar J_B. Accordingly, the DC current gain β, defined as J_C/J_B, is much higher in the SiGe HBT than in the Si BJT.

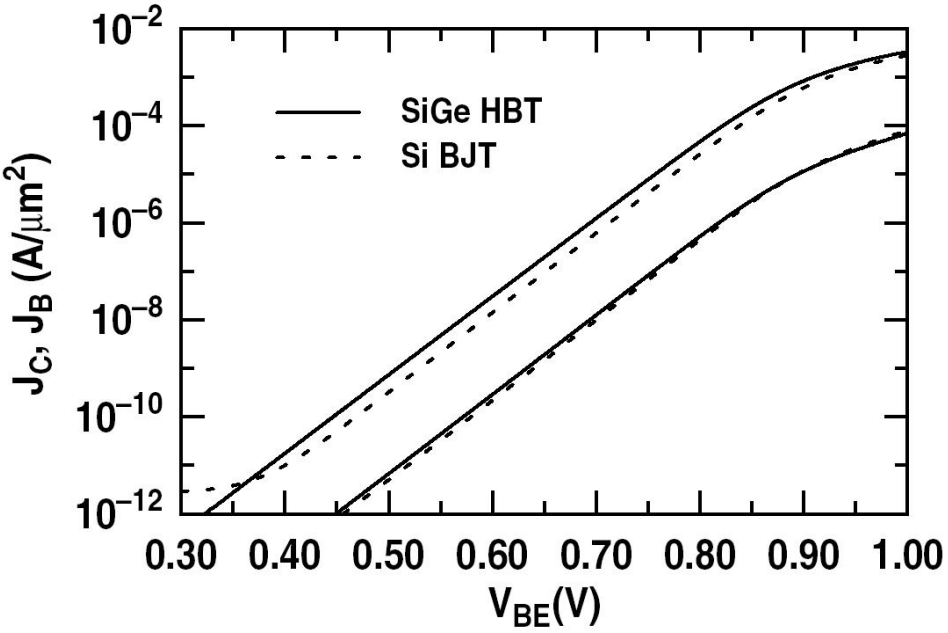


Figure 1.2: Comparison of Gummel characteristics of a comparably constructed SiGe HBT and Si BJT.

In most RF and microwave circuit applications, it is the transistor frequency response that limit system performance. An important figure-of-merit in bipolar transistor is the unity gain cutoff frequency f_T, which is given by

$$f_T = \left[\frac{1}{g_m}(C_{eb} + C_{cb}) + \tau_b + \tau_c + \tau_e\right]^{-1} \tag{1.1}$$

where g_m is the transconductance, C_{eb} and C_{cb} are the EB and CB capacitances and τ_b, τ_c, τ_e are the base, collector and emitter transit times, respectively. Of these three transit times, τ_b is the primary portion that limits the maximum f_T of a conventional bipolar transistor. The built-in electric field created by the graded Ge content across the neutral base region accelerates the minority carriers across the base region, resulting in a decrease in τ_b, and hence higher f_T for a SiGe HBT. Fig. 1.3 shows a comparison of the f_T performance for a SiGe HBT and a comparably constructed Si BJT. Note that f_T is increased from 35 GHz to 50 GHz by introducing a graded Ge mole fraction in the base.

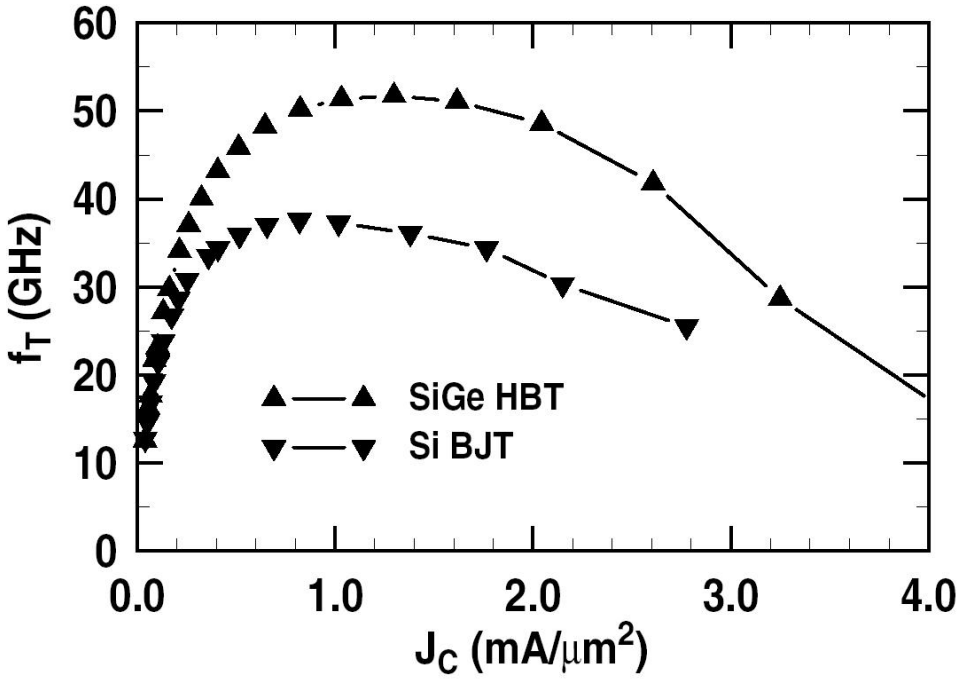


Figure 1.3: Measured comparison of unity gain cutoff frequency f_T as a function of collector current for a comparably constructed SiGe HBT and Si BJT.

A more relevant figure-of-merit for practical RF and microwave applications is the maximum oscillation frequency f_{max}, since it depends on both the f_T and the device parasitics. f_{max} is given by

$$f_{max} = \sqrt{\frac{1}{8\pi C_{cb}} \cdot \frac{f_T}{r_b}} \tag{1.2}$$

where C_{cb} is the total CB capacitance and r_b is the total base resistance. f_T/r_b ratio needs to be increased to improve f_{max}. For a double contact base, r_b is related to the product of base doping N_B and base width W_B by,

$$r_b = \frac{1}{12q\mu_p} \frac{X_E}{L_E} \frac{1}{N_B W_B} \tag{1.3}$$

where X_E is the lateral emitter width, L_E is the lateral emitter length, and μ_p is the majority hole mobility in the base. For a conventional Si BJT, there is a tradeoff between β and r_b due to the base doping. Increasing the level of doping in the base will decrease the minority carrier density in the base, resulting in a decrease in J_C and, hence, β. Meanwhile, to reduce r_b, the base doping needs to be increased. With careful bandgap engineering, however, r_b can be reduced by decreasing N_B without compromising β, since β can be increased exponentially by adjusting the Ge-induced bandgap offset. Moreover, as discussed above, f_T is increased by the graded Ge content in the base. As a result, it is possible to increase f_T, and reduce r_b without sacrificing β performance, leading to an increase in the f_T/r_b ratio, and hence improve f_{max} for a SiGe HBT.

1.2 Thesis Contributions

This thesis presents a new technique for use in investigating device physics and compact modeling using Verilog-A hardware language. This new Verilog-A based model can be easily modified and implemented into circuit simulators without the need to interface with simulators. The internal currents, charges, and noise sources, which are currently not available when existing built-in models are used in circuit simulators, all become accessible using this technique.

The Verilog-A Language is introduced in Chapter 2. The essence of using Verilog-A based compact modeling in place of low-level simulator code is explained in detail. An example of Verilog-A based modeling is given to illustrate the use of the Verilog-A language. Chapter 3 introduces the physics behind the VBIC model and the temperature models in VBIC.

In Chapter 4, the VBIC model is realized in the new Verilog-A language, and implemented into the circuit simulators Cadence and ADS. Several problems such as syntax errors, convergence problems and numerical problems were encountered and their solutionis are reported in this chapter. Noise models were added in the Verilog-A based model to be consistent with the Cadence built-in model. The DC, *ac*, noise and large signal simulation comparisons between Verilog-A based VBIC modeling and the Cadence built-in VBIC model revealed identical results.

Based on the new Verilog-A based VBIC model, two applications for SiGe HBTs noise modeling are presented in Chapter 5. First, a new inverse circuit simulation based

low frequency noise extraction method is proposed based on the Verilog-A based VBIC model. The low frequency noise of a device biasing at high current can be measured more accurately through this method. Secondly, to better understand the different phase noise upconversion mechanisms of the base current $1/f$ noise and base current short noise in oscillator design, the internal I_{BE} and the internal I_{CE} were separated from the external I_{BE} and the external I_{CE} using the Verilog-A based VBIC model. Clearly, the noise generating current, I_{BE}, makes up only a small portion of the terminal I_B.

A group of improved temperature mapping models for modeling of DC currents down to 43 K are presented in Chapter 6. The new VBIC based model was implemented using Verilog-A, compiled into binary code, and dynamically linked to a circuit simulator (ADS) through its compact modeling interface. Excellent Gummel and output fitting across a wide temperature range from 300 K down to 43 K were achieved for a 50 GHz SiGe HBT device.

Intermodulation linearity that relates to the selectivity of an RF receiver is another important figure-of-merit for SiGe HBTs. In Chapter 7, the intermodulation linearity simulation capability of the VBIC, HICUM and Mextram models is evaluated using harmonic balance in a 200 GHz SiGe HBT device and the impact of avalanche and self-heating on IIP3 are discussed. A weak avalanche was shown to have a significant impact on IIP3 and the results provide new insights into the device physics underlying the linearity behavior and quantified simulation data for comparisons of linearity that will be useful for both designers and modelers.

Chapter 8 presents the major conclusions of this work.

Appendix A presents the code for the new Verilog-A based VBIC model, along with a group of improved temperature mapping models for modeling DC currents down to 43 K.

CHAPTER 2

VERILOG-A LANGUAGE

In most circuit simulators, compact models such as the built-in model are embedded in the simulators and serve as the basic simulation function components. Meanwhile, the interfaces in the compact model define its connections with the simulators and the analysis engine. As a consequence, an in-depth understanding of simulator architecture and analysis engine is a basic requirement for model developers due to the complexity involved, which extends far beyond the model descriptions. Moreover, any changes in the models will require lengthy, recompilation and re-linking to the SPICE program, which in turn increases the model implementation process period and reduces the number of choices for end users. In addition, these kind of models are not portable for use in different simulators as a result of their own differently compiled model interfaces.

C (Spice3) programming has been the standard language for most compact models used in circuit simulators since 1985 because of its flexibility and ease of compilation for the simulators. However, writing the model source code is still a lengthy task. For example, the BSIM4 model requires over 20k lines and could take an experienced engineer months to write and debug.

2.1 Introduction of Verilog-A

Verilog-A (one of the subsets of Verilog-AMS), is derivated from IEEE 1364-1995 Verilog HDL and is an IEEE standard analog hardware description language that uses modules to describe the structure and behavior of analog systems and their components for multi-domain simulations (electrical, thermal, and mechanical). With the release of the Verilog-AMS Language Reference Manual (LRM) version 2.2 by Accellera on February 14, 2005 [3], many new features were added, making it possible to easily develop new compact models for semiconductor devices such as transistors and diodes in a standard language. Today, Verilog-A is widely accepted as a more powerful, portable, suitable, and flexible language for compact model description.

Specialized features are provided by Verilog-A to create and use modules that encapsulate high-level behavioral descriptions of systems and components [3]:

- Verilog-A modules are compatible with Verilog-AMS HDL.
- Analog behavioral modeling descriptions are contained in a separate analog block.
- Branches can be named for easy selection and access.
- Parameters can be specified with valid range limits.
- Systems can be modeled by using expressions consisting of operators, variables, and signals, including:
  - a full set of operators including trigonometric functions, integrals, and derivatives;

- a set of waveform filters to modify the waveform results for faster and more accurate simulations, such as transition, slew, Laplace, and Z-domain;
- a set of events to control when a certain code is simulated;
- selection of the simulation time step for simulation control; and
- support for accessing SPICE primitives from within the language.

The major reason for choosing Verilog-A as a standard language for the compact model is to avoid the need for complex interfaces in the circuit simulators [4]. With the development of the modern semiconductor manufacturing processes, the period required for new device releases is becoming shorter and shorter, and the geometries of the devices themselves are becoming smaller and smaller. The new equations written in C for the new physical effects need to be installed into the circuit simulators in a very short time. However, the simulator interface, which includes various functions such as topology checking, parameter reading, Jacobian matrix and current vectors loading, and value initializing, presents a significant barrier for model developers [4] [5]. Normally, an in-depth understanding of interfaces is more difficult than the description of the compact model, resulting in a slowdown when adopting a new model process. Since Verilog-A is a simulator-independent standard language, the model developers no longer need to deal with these specific details.

Moreover, Verilog-A is a higher-level language than the C programming language. For example, the symbolic partial derivations of the charges and currents in compact models can be automatically computed by Verilog-A simulators. Traditionally, partial

derivatives of the equations in a compact model for the Newton-Raphson algorithm need to be written in the C programming language in circuit simulators.

From a device research standpoint, an important benefit of Verilog-A based compact modeling is that users can access the internal currents, charges, and noise parameters which cannot be modified in the built-in models traditionally used in circuit simulators such as Spectre and ADS. This makes it possible for individuals or small research groups to develop and modify a compact model according to their specific research objectives. Three important applications based on a Verilog-A VBIC model will be introduced in chapters 5 and 6.

2.2 Verilog-A basics

As an efficient language for writing compact models, Verilog-A is both simple and easy to learn. As mentioned previously, Verilog-A uses modules to describe the structure and behavior of analog systems and their components. Here, the module can be described mathematically by its terminals and external parameters. Both electrical and non-electrical system descriptions can be used with Verilog-A. The concepts of nodes, branches, and terminals are provided to support the conservative and signal-flow descriptions. In addition, Kirchhoff's Potential and Flow Laws (KPL and KFL) are obeyed in the analog behavior solutions, and defined by the quantities associated with the analog behaviors.

2.2.1 Example: Simple Diode

Diode Model Equations

The example of a simple junction diode will provide a better understanding of the utility of Verilog-A. Fig. 2.1 shows the equivalent circuit of a junction diode used in this example. Here, only a brief discussion regarding the usage of Verilog-A is given. For more detailed description, please refer to [3] [5] and [6].

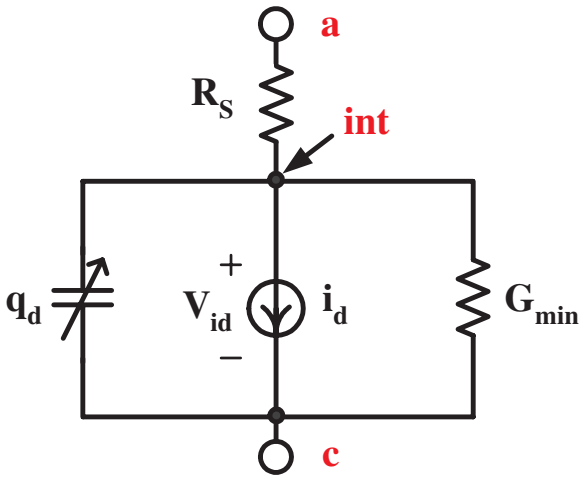


Figure 2.1: Equivalent circuit of junction diode.

A single linear resistor R_S represents both the external contact resistance and any voltage drop in the neutral n and p regions. The voltage drop in the neutral regions is significant under a high level injection condition. G_{min} is the minimum conductance, which is a constant selected for numerical reasons. The dc characteristic of the device

is modeled by a nonlinear current source i_d with the ideal diode equation

$$i_d = i_s \exp\left(\frac{V_{id}}{nV_T} - 1\right) \tag{2.1}$$

where i_s is the saturation current, $V_T = kT$ is the thermal voltage, n is the emission coefficient, and V_{id} is the intrinsic voltage between nodes `int` and `c`.

The charge storage element q_d in Fig. 2.1 models both the diffusion charge storage by injected minority carriers and the charge stored in the depletion region. The total charge q_d is given by

$$q_d = q_{diff} + q_j \tag{2.2}$$

q_{diff} is the diffusion charge, which depends on the transit time parameter tt,

$$q_{diff} = i_d tt \tag{2.3}$$

with a diffusion capacitance $c_{diff}(V)$,

$$c_{diff}(V) = \frac{dq_{diff}}{dV} = \frac{1}{nV_T} i_d tt. \tag{2.4}$$

q_j is the stored charge in the depletion region,

$$q_j = \int_0^{V_{id}} c_j(V) dV \tag{2.5}$$

where $c_j(V)$ is the junction capacitance. Substituting (2.3) and (2.5) into (2.2), we have

$$q_d = i_d tt + \int_0^{V_{id}} c_j(V) dV \tag{2.6}$$

Assuming an abrupt junction, $c_j(V)$ is:

$$c_j(V) = \frac{c_{j0}}{\sqrt{1 - \frac{V_{id}}{\phi}}} \tag{2.7}$$

where c_{j0} is zero voltage junction capacitance, and ϕ is the built-in potential. However, (2.7) has numerical problems at $V_{id} \geq \phi$, and $c_j(V)$ is not continuous at $V_{id} = \phi$. To solve this discontinuity problem, a factor f_c is introduced: $0 < f_c < 1$. If $V_{id} < f_c\phi$, (2.7) is used. If $V_{id} \geq f_c\phi$, $c_j(V)$ begins at the capacitance determined by the theoretical curve $c_j(f_c\phi)$, and with a slope determined by the slope of the tangent to the theoretical curve at the break point $V_{id} = f_c\phi$,

$$c_j(V)\Big|_{V_{id} \geq f_c\phi} = \frac{c_{j0}}{(1 - f_c)^{\frac{3}{2}}} \left[1 - \frac{3}{2} f_c + \frac{V}{2\phi}\right] \tag{2.8}$$

Therefore, taking integration of (2.7) and (2.8), the total charge q_d is as follows. If $V_{id} < f_c\phi$,

$$q_d = i_d tt + 2c_{j0}\phi \left[1 - \sqrt{1 - \frac{V_{id}}{\phi}}\right] \tag{2.9}$$

If $V_{id} \geq f_c\phi$,

$$q_d = i_d tt + 2c_{j0}\phi\left[1 - \sqrt{1 - f_c}\right] + \frac{c_{j0}}{(1 - f_c)^{\frac{3}{2}}}(V_{id} - f_c\phi)\left(1 - \frac{5}{4}f_c + \frac{V_{id}}{4\phi}\right) \quad (2.10)$$

Verilog-A code

The Verilog-A code for the above simple diode model is as follows.

```
‘include "disciplines.vams"

‘include "constants.vams"

‘define GMIN 1.0e-12


module diodefinal (a, c);

inout a, c;

electrical a,c,int;

branch (a,int) v_rs;

branch (int,c) v_id;


parameter real is=10f from (0.0:inf);

parameter real n=1.0 from (0.0:inf);

parameter real rs=1 from [0.0:inf);

parameter real fc=0.9 from (0.0:1.0);

parameter real tt=1e-12 from [0.0:inf);

parameter real cjo=1e-15 from [0.0:inf);
```

```
parameter real phi=0.7 exclude 0.0;
parameter real kf=0.0 from [0.0:inf);
parameter real af=1.0 from (0.0:inf);
parameter real imax=1.0 from[0.0:inf);
parameter real imelt=imax from[0.0:inf);
real Grs, expi, vmax, id, qd;

analog begin
Grs =  rs >1.0e-6 ? 1/rs   : 1.0e6;
expi = limexp(V(v_id)/(n*$vt));
vmax = n*$vt*ln(imax/is+1);
if (V(v_id) < vmax) begin
    id = is*(expi-1);
end else begin
    id = imax+(V(v_id)-vmax)*(imax+is)/(n*$vt);
end
if (V(v_id)<fc*phi) begin
    qd = tt*id+2*cjo*phi*(1-sqrt(1-V(v_id)/phi));
end else begin
    qd = tt*id+2*cjo*phi*(1-sqrt(1-fc))+
        cjo*(V(v_id)-fc*phi)*(1-1.25*fc+V(v_id)/(4*phi))/pow((1-fc), 1.5);
end
```

```
I(v_rs) <+ V(v_rs)*Grs;
I(v_id) <+ id+‘GMIN*V(v_id);
I(v_id) <+ ddt(qd);
I(v_rs) <+ white_noise(4*‘P_K*$temperature*Grs);
I(v_rs) <+ white_noise(2*‘P_K*id)+flicker_noise(kf*pow(abs(id),af),1);
if (I(<a>) > imelt)
    $strobe( "Warning: diode is melting!" );
end
endmodule
```

`disciplines` is used for definitions of related physical signal types, variables, and absolute tolerance, which can be defined by users. This file can be loaded into model descriptions by the command ‘`include`. Basic physical quantities such as units, expected quantity size, and access name are described in `disciplines`. `constants.vams` is used to define the mathematical and physical constants necessary for the descriptions involved in device modeling.

‘`define` is used for text macro substitution, which allows meaningful names to be used to present commonly used pieces of text. It can be used both inside and outside module definitions.

As a basic building block, a Verilog-A `module` describes the individual components, and can be instantiated into a netlist of circuit simulators. The module name `diode` is followed by the ports `(a, c)`, which are used for component connection. The port direction is declared by `inout`, which indicates the signal flow. For the compact

model, the port type `electrical` is defined by the `disciplines` file, where the signal associated with the ports is declared in terms of its variable voltage and variable current.

`branch` is a new statement and represents an explicit term in model descriptions. A `branch` is a path between two nets. Two branches, `v_rs` and `v_id`, are declared in this example. The `branch` declaration statement can be directly used for current and voltage descriptions and to simplify model descriptions.

`parameter` is used for parameter declaration and should follow the port statement. The default value should be given and can be re-specified when the module is instantiated. `real` defines the type of parameters, although this is optional. Sometimes range limits are used to specify that the parameters fall within a particular range and may be used to avoid non-theoretical values or mathematical calculation errors. Here, the parentheses `()` exclude the endpoints while the brackets `[]` include the endpoints, and `exclude` indicates that it must not include the endpoints. If the specified value is out of range when the module is instantiated, the simulator will automatically generate an error message.

The `real` statement, which represents a real physical connection between structural entities, declares `id` to be a real variable. It should not store its value. For an analog process, the real net is associated with a continuous time kernel and is always initialized to zero. It can only be connected to a compatible interconnect and other real expressions.

The expression `rs>1.0e-6 ? 1.0/rs : 1.0e6` is used for conditional operation. If `rs>1.0e-6` evaluates as false, then `1.0e6` is used as the result of the conditional expression; if `rs>1.0e-6` evaluates as true, `1.0/rs` is used as the result.

The `analog` block is used to describe the behavior of the module. Delimited by the keywords `begin` and `end`, statements which are used to describe the relationship of signals in an analog block can be grouped together and executed sequentially in a given order. Only one analog block can be used in each module.

Analog conditional statements such as `if-else` are used to determine whether a statement should be executed or not. The terms `GMIN` and `imax` are used to aid convergence and prevent numerical overflow during iterations in simulation. The term `imelt` is used as a limit warning for the junction current.

The branch contribution operator `<+` is used in statement to describe analog behavior. It can only be used in an analog block. A branch contribution statement is separated by a branch contribution operator into two parts, a left side and a right side. In general, the right side can be any expression which evaluates to or can be promoted to a real value. The left side specifies the source branch signal where the right side is to be assigned.

The symbol `$` serves as a system function or system task indicator. It is often used in environment parameter functions. For example, the simulation temperature is defined as `$temperature`, which does not take any input arguments and returns the circuit's ambient temperature in Kelvin units, and the thermal voltage is represented by `$vt`.

The operators + - * / and functions **sqrt**, **pow**, **ln**, **exp**, and **abs** are available in Verilog-A. In general, the operator **limexp** is used instead of **exp** to obtain better convergence in a semiconductor compact model. The charge time-derivation operator function `ddt` is used for capacitive current. The noise sources are described by `white_noise`

and `flicker_noise`, which generate white noise and pink noise, respectively. The term `‘P_Q` is included in the `constants.vams` file. The <> is used to delimit the port name. The `I(<a>)` used here presents the accessing current that passes through module port `a`. The `$strobe` term is used to display simulation data or print a newline character when the simulator has converged on a solution for all nodes. The `endmodule` keyword is used when the module definition is complete.

Simulation Results

A voltage V_d is applied between nodes `a` and `c`. The simulated Diode $I_d - V_{id}$ and $I_d - V_d$ curves are shown in 2.2.

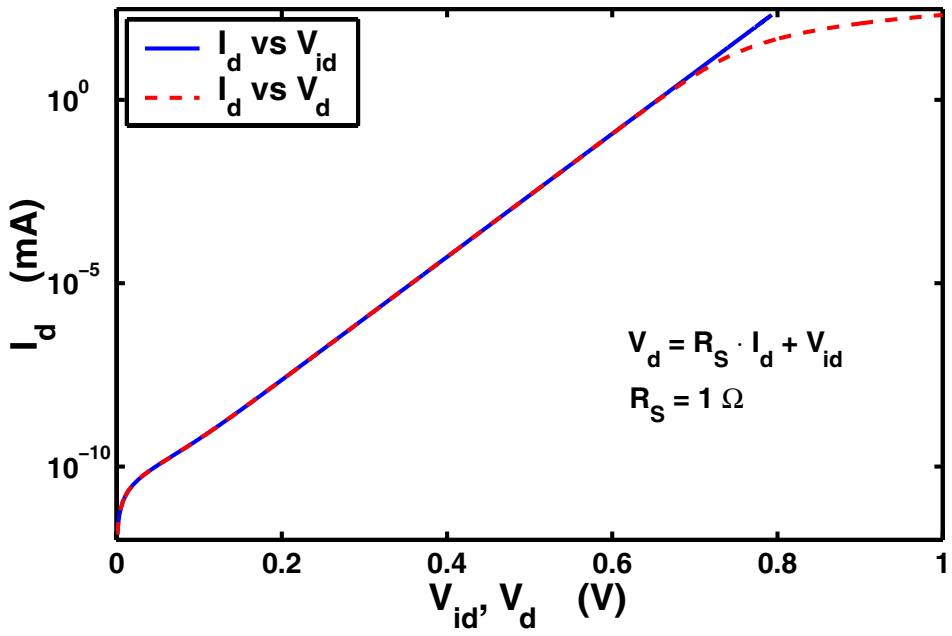
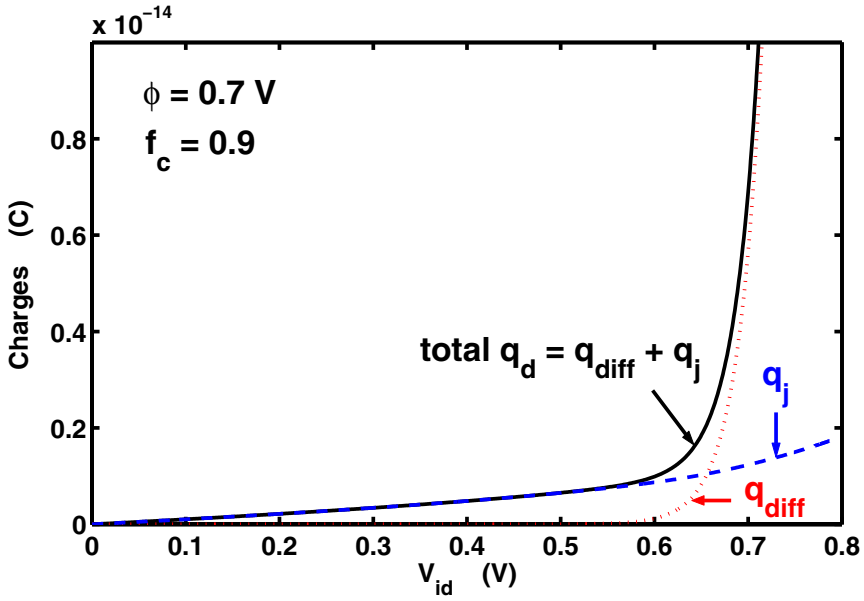
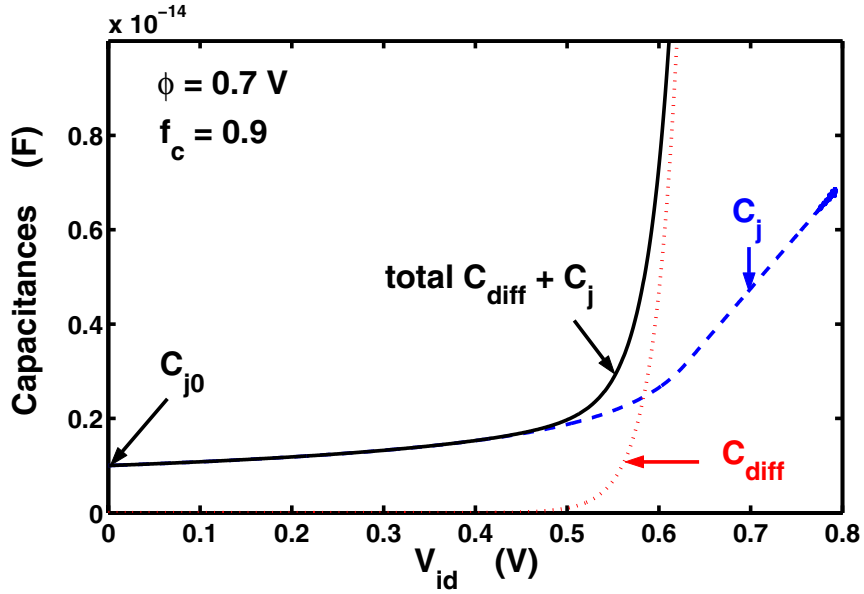


Figure 2.2: Simulated Diode $I_d - V_{id}$ and $I_d - V_d$ curves.



(a)



(b)

Figure 2.3: (a) Simulated Diode q_d, q_{diff}, and q_j vs V_{id}. (b) Extracted Diode $C-V$ curves.

q_d, q_{diff}, and q_j vs intrinsic voltage V_{id} are shown in Fig. 2.3 (a). The extracted C_V curves are shown in Fig. 2.3 (b). Note that both c_j and q_j are continuous at $V_{id} = \phi$.

2.3 Summary

This chapter introduced the Verilog-A Language. The use of a Verilog-A based compact modeling in place of low-level simulator code was explained in detail. Finally, an example of Verilog-A based modeling was given to demonstrate the use of the Verilog-A programming language.

CHAPTER 3

VBIC MODELING

The SPICE Gummel-Poon (SGP) model has been the IC industry standard for modeling bipolar junction transistors (BJT) for almost thirty years. However, the Gummel-Poon model is unable to model collector resistance modulation (quasi-saturation) and parasitic substrate transistor action, and is not adequate to model modern HBT (heterojunction bipolar transistor) devices due to the high speed and accurate simulation requirements for the modern telecommunication industries, especially for RF design. An improved VBIC (Vertical Bipolar Inter-Company model) was introduced by IC and CAD industry representatives in 1995 and is widely used. VBIC is based on the SPICE Gummel-Poon model, with a modified version of the Kull-Nagel quasi-saturation model. The main improvements in VBIC compared to SGP [7] include:

- a modified form is used in Early effect (g_o) modeling to better describe the output conductance of the bipolar transistor,
- an improved quasi-saturation modeling process is implemented to avoid a negative value for the output conductance,
- parasitic substrate PNP transistor modeling,
- parasitic fixed (oxide) capacitance modeling,
- avalanche multiplication modeling,

- improved temperature dependence modeling,
- decoupling of base and collector currents,
- electrothermal (self heating) modeling,
- C_∞ continuous (smooth) modeling,
- improved HBT modeling.

VBIC is used particularly for 4-terminal vertical NPN transistors. For 5-terminal vertical PNP transistors in smartpower technologies, VBIC can be treated as a subcircuit. However, the geometry scaling cannot be taken into account in VBIC because of the plethora of BJT structure and layout considerations.

Fig. 3.1 shows an equivalent network for VBIC, which includes an intrinsic NPN transistor (the same equivalent circuit used in the standard Gummel-Poon model), a parasitic PNP transistor, and parasitic resistances and capacitances. The external local thermal network is used only with the electrothermal version of the model. It is composed of a thermal resistance R_{th}, a thermal capacitance C_{th}, and a thermal source (heat generation) I_{th} which can model the thermal properties of a BJT transistor by connecting to the local heating and power dissipation in the device. The excess phase for forward transport current I_{tzf} is also considered in another separate external subcircuit.

In this thesis, only a brief discussion on VBIC modeling is provided. For a more detailed model description, please refer to [7] and [8].

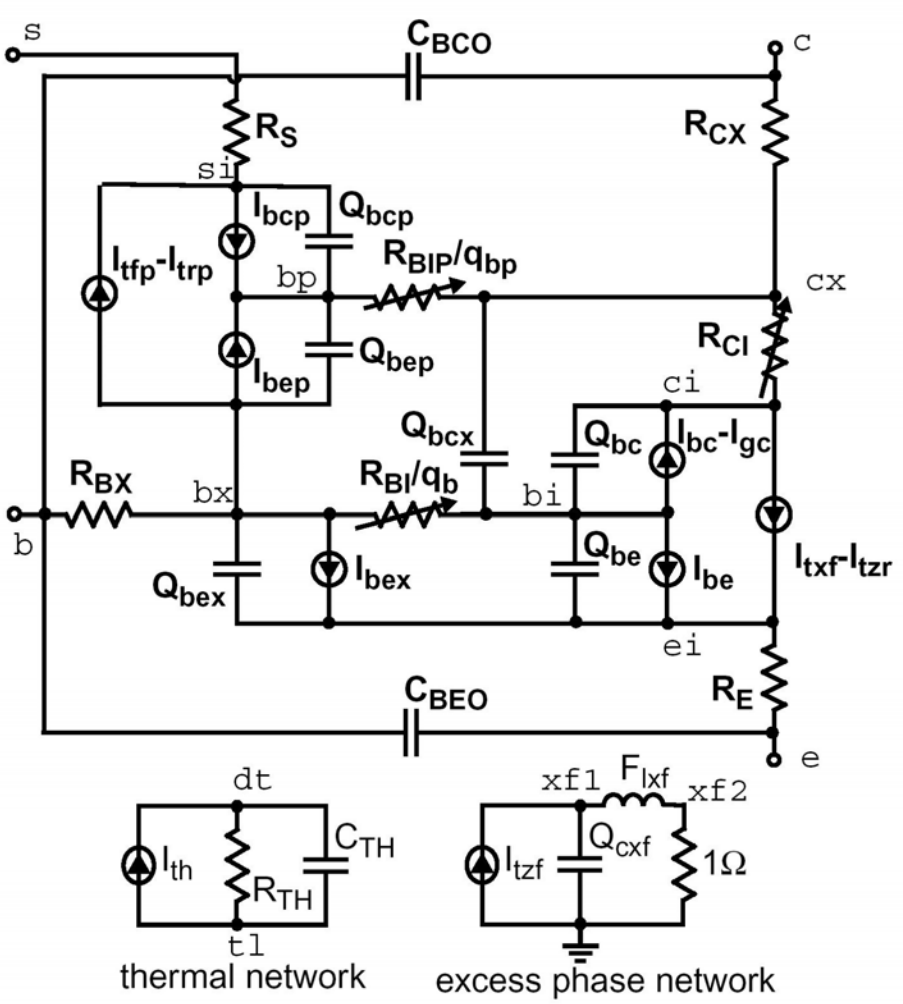


Figure 3.1: VBIC equivalent network

3.1 Modeling of Transfer Current

The band diagram of an intrinsic bipolar transistor is shown in Fig. 3.2. Nodes `bi`, `ei`, and `ci` are the internal nodes shown in Fig. 3.1. V_{BEI} is the intrinsic BE forward bias voltage between nodes `bi` and `ei`. V_{BCI} is the intrinsic BC forward bias voltage between nodes `bi` and `ci`. At zero bias, i.e., $V_{BEI} = 0$ and $V_{BCI} = 0$, the neutral base region starts at 0, and ends at W_p. The quasi-Fermi level of the electrons E_{fn} is flat, and equal to the quasi-Fermi level of the holes E_{fp}, as shown in Fig. 3.2 (a). When a forward bias V_{BEI} is applied to the internal device, the EB junction depletion width is shortened. The left edge of the quasineutral base region moves from 0 to $x1$, as shown in Fig. 3.2 (b). Similarly, the right edge of the quasineutral base region moves from W_p to $x2$ when a forward bias V_{BCI} is applied to the CB junction. $x2 - x1$ gives the width of the quasineutral base region.

As the recombination is negligible in a narrow base, the electron current density in the base region can be written as,

$$J_n = n\mu_n \frac{dE_{fn}}{dx} \tag{3.1}$$

where n is the electron concentration, and μ_n is the electron minority carrier mobility. The hole quasi-Fermi level E_{fp} can be assumed to be constant, since

$$\frac{dE_{fp}}{dx} = \frac{J_p}{p\mu_p} \approx 0 \tag{3.2}$$

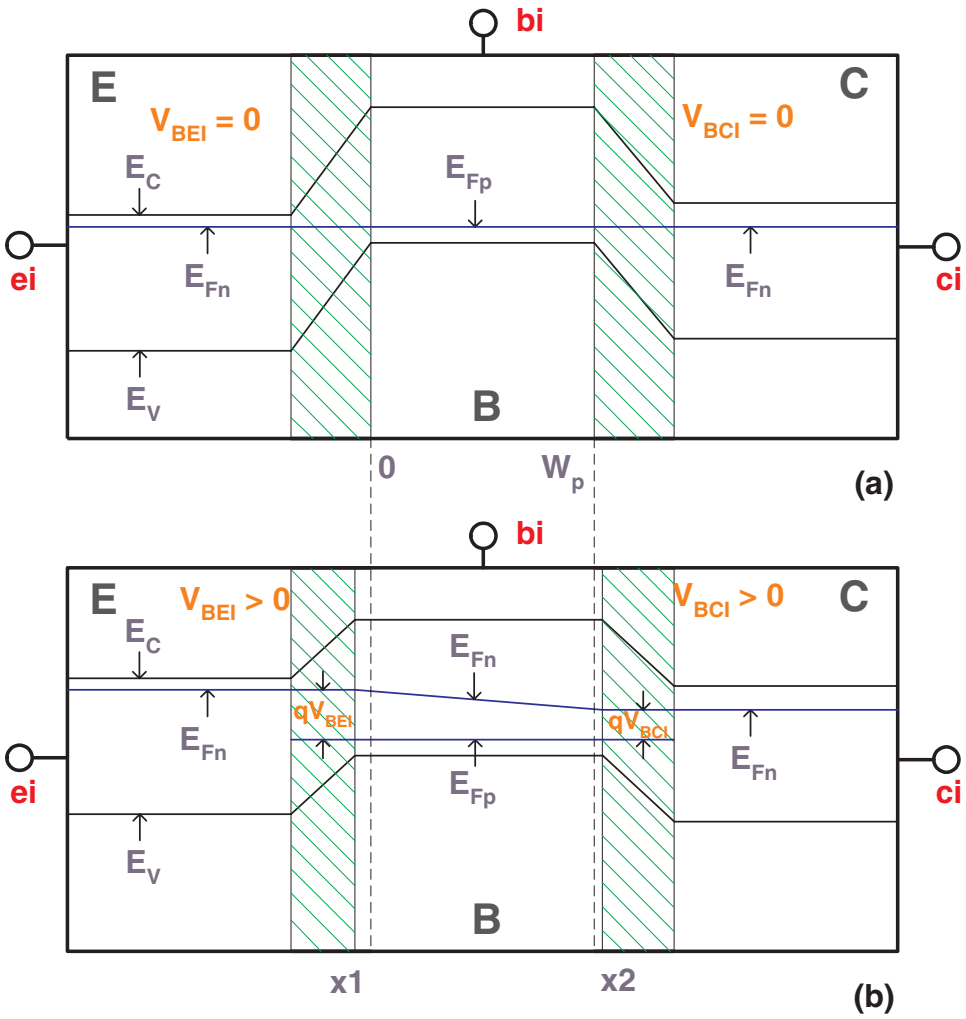


Figure 3.2: Band diagram of an intrinsic bipolar transistor. (a) $V_{BEI} = 0$, $V_{BCI} = 0$; (b) $V_{BEI} > 0$, $V_{BCI} > 0$.

where p is the majority hole concentration in the base, which is very large. μ_p is the hole majority carrier mobility, and J_p is the hole current density in the base region. The np product is

$$E_{fn} - E_{fp} = kT \ln\left(\frac{np}{n_i^2}\right) \tag{3.3}$$

where k is Boltzmann's constant, T is temperature in degrees Kelvin, and n_i is the effective intrinsic concentration. From (3.1), (3.2) and (3.3), J_n can be rewritten as

$$J_n = n\mu_n \frac{d(E_{fn} - E_{fn})}{dx} \tag{3.4}$$

$$= qD_n \frac{n_i^2}{p} \frac{d}{dx}\left(\frac{np}{n_i^2}\right) \tag{3.5}$$

where q is the magnitude of the electronic charge and the electron diffusivity D_n is related to the electron mobility μ_n through the Einstein relations, $D_n = \mu_n kT/q$.

Electrons, injected from the emitter into the base, reach the collector and become the collector current. Moving $qD_n\frac{n_i^2}{p}$ in (3.5) to the left-hand side gives

$$\frac{J_n p(x)}{qD_n n_i^2} dx = d\left(\frac{np}{n_i^2}\right) \tag{3.6}$$

Integrating on both sides gives

$$J_n \int_{x1}^{x2} \frac{p(x)}{qD_n n_i^2} dx = \left.\frac{np}{n_i^2}\right|_{x2} - \left.\frac{np}{n_i^2}\right|_{x1} \tag{3.7}$$

The boundary conditions for EB and CB junctions are

$$\left.\frac{np}{n_i^2}\right|_{x1} = \exp\left(\frac{V_{BEI}}{V_T}\right) \tag{3.8}$$

$$\left.\frac{np}{n_i^2}\right|_{x2} = \exp\left(\frac{V_{BCI}}{V_T}\right) \tag{3.9}$$

where $V_T = kT/q$ is the thermal voltage. Applying these boundary conditions gives

$$J_n \int_{x1}^{x2} \frac{p(x)}{qD_n n_i^2} dx = -\left[\exp\left(\frac{V_{BEI}}{V_T}\right) - \exp\left(\frac{V_{BCI}}{V_T}\right)\right] \tag{3.10}$$

Note that the negative value for J_n indicates that the electrons are flowing towards the collector. Let

$$Q_B = q \int_{x1}^{x2} p(x) dx \tag{3.11}$$

which represents the total majority charge per unit area in the base. Assuming D_n and n_i^2 are position independent, (3.10) can then be rewritten as

$$J_n = -\frac{q^2 D_n n_i^2}{Q_B}\left[\exp\left(\frac{V_{BEI}}{V_T}\right) - \exp\left(\frac{V_{BCI}}{V_T}\right)\right] \tag{3.12}$$

Defining Q_{B0} as the Q_B at zero applied voltage, i.e., $V_{BEI} = 0$, $V_{BCI} = 0$,

$$Q_{B0} = q \int_0^{W_p} N_B(x) dx \tag{3.13}$$

The Q_B/Q_{B0} ratio is denoted as q_b, which represents the normalized base charge. Then (3.12) can be rewritten as

$$J_n = \frac{J_S}{q_b}\left[\exp\left(\frac{V_{BEI}}{V_T}\right) - \exp\left(\frac{V_{BCI}}{V_T}\right)\right] \tag{3.14}$$

$$J_S = \frac{q^2 D_n n_i^2}{Q_{B0}} \tag{3.15}$$

where J_S is the saturation current density.

The simple theory discussed above shows that the forward collector current is exponentially related to the inverse thermal voltage. Empirically, however, a non-ideality factor N_F must be introduced to numerically describe the nonideal effect induced by the spatial coordinate dependence of mobility, doping concentration, diffusion constant, and carrier lifetimes. Similarly, a non-ideality factor N_R is used for the reverse collector current. Therefore the final collector current is

$$I_C = A_E|J_n| = \frac{I_{tf} - I_{tr}}{q_b} \tag{3.16}$$

$$I_{tf} = I_S\left[\exp\left(\frac{V_{BEI}}{N_F V_T}\right) - 1\right] \tag{3.17}$$

$$I_{tr} = I_S\left[\exp\left(\frac{V_{BCI}}{N_R V_T}\right) - 1\right] \tag{3.18}$$

$$I_S = A_E J_S \tag{3.19}$$

where I_{tf} and I_{tr} are the forward and reverse transport currents. A_E is the emitter area, and I_S represents the saturation current.

Moving on to examine the normalized base charge q_b, $p(x)$ in the base has three components: the base doping $N_B(x)$, $n_{be}(x)$ due to EB applied voltage V_{BEI}, and $n_{bc}(x)$ due to CB applied voltage V_{BCI},

$$p(x) = N_B(x) + n_{be}(x) + n_{bc}(x) \tag{3.20}$$

Therefore, Q_B changes with applied voltages V_{BEI} and V_{BCI} in several ways:

1. $x1$ changes with V_{BEI}, causing extra depletion charge of Q_{JE} as shown in Fig. 3.3, corresponding to the reverse Early Effect.

$$Q_{JE} = \int_{x1}^{0} qN_B(x)dx \tag{3.21}$$

2. $x2$ changes with V_{BCI}, causing extra depletion charge of Q_{JC} as shown in Fig. 3.3, corresponding to the forward Early Effect.

$$Q_{JC} = \int_{W_p}^{x2} qN_B(x)dx \tag{3.22}$$

3. $n_{be}(x)$ changes with V_{BEI}, corresponding to the diffusion charge Q_{ne}.

$$Q_{ne} = \int_{x1}^{x2} qn_{be}(x)dx \Big|_{V_{BEI}>0, V_{BCI}=0} \tag{3.23}$$

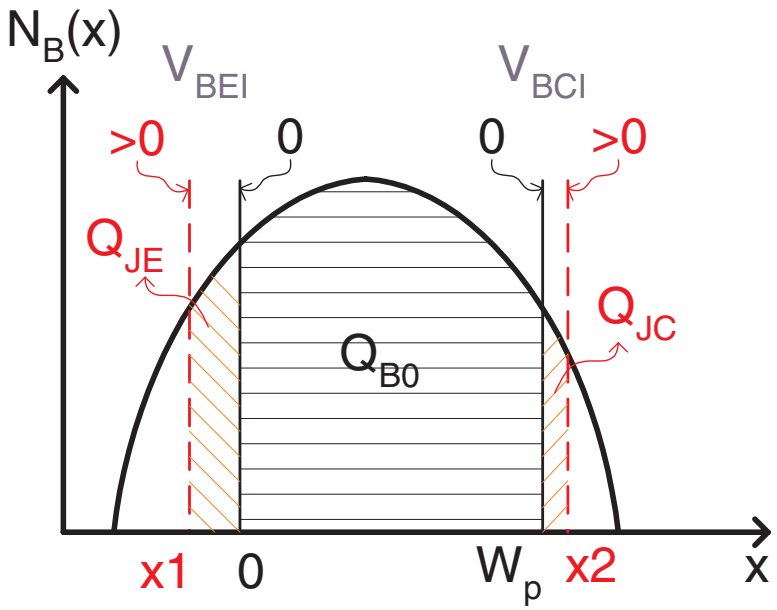


Figure 3.3: Zero bias charge Q_{B0}, EB depletion charge Q_{JE}, and CB depletion charge Q_{JC} in the neutral base region.

4. $n_{bc}(x)$ changes with V_{BCI}, corresponding to the diffusion charge Q_{nc}.

$$Q_{nc} = \int_{x1}^{x2} q n_{bc}(x) dx \Big|_{V_{BEI}=0, V_{BCI}>0} \tag{3.24}$$

The total base charge Q_B is the sum of Q_{B0}, Q_{JE}, Q_{JC}, Q_{ne}, and Q_{nc}:

$$Q_B = \int_{x1}^{x2} (N_B(x) + n_{be}(x) + n_{bc}(x)) dx \tag{3.25}$$

$$= Q_{N_B} + Q_{ne} + Q_{nc} \tag{3.26}$$

$$Q_{N_B} = \int_{x1}^{x2} N_B(x) dx \tag{3.27}$$

$$Q_{N_B} = \int_{x1}^{0} N_B(x)dx + \int_{0}^{W_p} N_B(x)dx + \int_{W_p}^{x2} N_B(x)dx, \tag{3.28}$$

$$= Q_{JE} + Q_{B0} + Q_{JC}. \tag{3.29}$$

Therefore q_b can be written as

$$q_b \triangleq \frac{Q_{NB}}{Q_{B0}} + \frac{Q_{ne}}{Q_{B0}} + \frac{Q_{nc}}{Q_{B0}} \tag{3.30}$$

$$= q_1 + \frac{Q_{ne}}{Q_{B0}} + \frac{Q_{nc}}{Q_{B0}} \tag{3.31}$$

and

$$q_1 \triangleq \frac{Q_{NB}}{Q_{B0}} \tag{3.32}$$

$$\triangleq 1 + \frac{Q_{JE}}{Q_{B0}} + \frac{Q_{JC}}{Q_{B0}} \tag{3.33}$$

q_1 is a function of bias, and represents the normalized base charge under the low level injection conditions, where $\frac{Q_{ne}}{Q_{B0}} \ll 1$ and $\frac{Q_{nc}}{Q_{B0}} \ll 1$, and hence $q_b \approx q_1$.

In practice, it is not possible to directly determine Q_{JE} and Q_{JC}. Instead the EB and CB depletion capacitances are given as

$$C_{je}(V) = \frac{dQ_{JE}}{dV_{BEI}} \tag{3.34}$$

$$C_{jc}(V) = \frac{dQ_{JC}}{dV_{BCI}} \tag{3.35}$$

Therefore, (3.33) can be rewritten as

$$q_1 = 1 + \frac{1}{Q_{B0}} \int_0^{V_{BEI}} C_{je}(V)dV + \frac{1}{Q_{B0}} \int_0^{V_{BCI}} C_{jc}(V)dV \tag{3.36}$$

Let $C_{JE} = C_{je}(0)$, and $C_{JC} = C_{jc}(0)$. Define the reverse Early voltage V_{ER} and the forward Early voltage V_{EF} as

$$V_{ER} \triangleq \frac{Q_{B0}}{C_{JE}} \tag{3.37}$$

$$V_{EF} \triangleq \frac{Q_{B0}}{C_{JC}} \tag{3.38}$$

Therefore, (3.36) can be rewritten as,

$$q_1 = 1 + q_{je} + q_{jc} \tag{3.39}$$

$$q_{je} = \frac{1}{V_{ER}} \frac{1}{C_{JE}} \int_0^{V_{BEI}} C_{je}(V)dV \tag{3.40}$$

$$q_{jc} = \frac{1}{V_{EF}} \frac{1}{C_{JC}} \int_0^{V_{BCI}} C_{jc}(V)dV \tag{3.41}$$

However, in VBIC modeling, V_{ER} and V_{EF} are treated as completely independent parameters for flexibility in fitting data. Moreover, $V_{ER}C_{JE}$ does not necessarily equal $V_{EF}C_{JC}$ in real device model parameters.

At high injection, the diffusion charges Q_{ne} and Q_{nc} are important. Assuming the transit time τ associated with each diffusion charge remains the same as for low injection

$$Q_{ne} = \frac{I_{tf}\tau_f}{q_b} \tag{3.42}$$

$$Q_{nc} = \frac{I_{tr}\tau_r}{q_b} \tag{3.43}$$

where τ_f and τ_r are the forward and reverse transit time, respectively. Now (3.31) can be rewritten as

$$q_b = q_1 + \frac{I_{tf}\tau_f}{q_b Q_{B0}} + \frac{I_{tr}\tau_r}{q_b Q_{B0}} \tag{3.44}$$

$$= q_1 + \frac{q_2}{q_b} \tag{3.45}$$

and

$$q_2 \triangleq \frac{I_{tf}\tau_f}{Q_{B0}} + \frac{I_{tr}\tau_r}{Q_{B0}} \tag{3.46}$$

Further assuming τ_f and τ_r are independent of bias, the forward Knee current I_{KF} and reverse Knee current I_{KR} can be defined as,

$$I_{KF} = \frac{Q_{B0}}{\tau_f} \tag{3.47}$$

$$I_{KR} = \frac{Q_{B0}}{\tau_r} \tag{3.48}$$

Then (3.46) is rewritten as

$$q_2 \triangleq \frac{I_{tf}}{I_{KF}} + \frac{I_{tr}}{I_{KR}} \tag{3.49}$$

Solving (3.45) gives q_b in terms of q_1 and q_2, so

$$q_b = \frac{1}{2}\left[q_1 + \sqrt{q_1^2 + 4q_2}\right] \tag{3.50}$$

In summary, the equations for transfer current are:

$$I_C = A_E|J_n| = \frac{I_{tf} - I_{tr}}{q_b} \tag{3.51}$$

$$I_{tf} = I_S\left[\exp\left(\frac{V_{BEI}}{N_F V_T}\right) - 1\right] \tag{3.52}$$

$$I_{tr} = I_S\left[\exp\left(\frac{V_{BCI}}{N_R V_T}\right) - 1\right] \tag{3.53}$$

$$q_b \triangleq \frac{1}{2}\left[q_1 + \sqrt{q_1^2 + 4q_2}\right] \tag{3.54}$$

$$q_1 = 1 + q_{je} + q_{jc} \tag{3.55}$$

$$q_{je} = \frac{1}{V_{ER}}\frac{1}{C_{JE}}\int_0^{V_{BEI}} C_{je}(V)dV \tag{3.56}$$

$$q_{jc} = \frac{1}{V_{EF}}\frac{1}{C_{JC}}\int_0^{V_{BCI}} C_{jc}(V)dV \tag{3.57}$$

$$q_2 \triangleq \frac{I_{tf}}{I_{KF}} + \frac{I_{tr}}{I_{KR}} \tag{3.58}$$

3.2 Modeling of Internal EB and BC Diodes

The internal EB diode is more complicated in the VBIC model than that in Gummel-Poon model because of the need to introduce additional emission coefficients. The ideal base current and nonideal current are included in the internal EB diode by

$$I_{bt} = I_{BE} + I_{BEX} \tag{3.59}$$

$$= I_{BEI}\left[\exp\left(\frac{V_{BEI}}{N_{EI}V_T}\right) - 1\right] + I_{BEN}\left[\exp\left(\frac{V_{BEX}}{N_{EN}V_T}\right) - 1\right] \tag{3.60}$$

The ratio between I_{BE} and I_{BEX} is defined by parameter W_{BE}.

The current in the internal BC diode can be written as

$$I_{bc} = I_{BCI}\left[\exp\left(\frac{V_{BCI}}{N_{CI}V_T}\right) - 1\right] + I_{BCN}\left[\exp\left(\frac{V_{BCX}}{N_{CN}V_T}\right) - 1\right] \tag{3.61}$$

A weak avalanche current source I_{gc}, modeled by the formula of Klosterman and de Graaff, is also included in the BC diode,

$$I_{gc} = (I_{cc} - I_{bc})A_{VC1}(P_C - V_{BCI})\exp\left[-A_{VC2}(P_C - V_{BCI})^{M_C - 1}\right] \tag{3.62}$$

The excess phase is modeled in the external subcircuit of Fig. 3.1 for both ac and transient analyses. If the capacitance of Q_{cxf} and the inductance of F_{lxf} are assumed to be C and L, respectively, the voltage V_{xf2} across the 1 Ω resistance caused by the

controlled current source I_{tf} can be written as

$$V_{xf2} = \frac{1}{1 + j\omega RC - \omega^2 LC} \tag{3.63}$$

where $L = T_D/3$, $C = T_D$, and $T_D = 1/\omega_0$. The current I_{xf2} flows through R and produces a voltage, which can be used to describe the delay in the voltage response of the transfer current.

3.3 Modeling of Quasi-Saturation

The voltage drop across the collector resistance, which includes the resistance formed by the undepleted portion of the epilayer, the subcollector and the collector contact, decreases the potential differences across the CB space charge layer, resulting in an increase in the base width and, hence, the base transit time and may even cause the BC diode to be internally forward biased. This phenomena is called the quasi-saturation effect. Using a modified version of the Kull model, the quasi-saturation effects are included in the modeling of the intrinsic collector (epi) region to avoid producing a negative value for g_o at high V_{BE}. If the velocity saturation is ignored, the current in the epi layer is written as

$$I_{epi0} = \frac{V_{rci} + V_T \left[K_{bci} - K_{bcx} - \ln\left(\frac{K_{bci}+1}{K_{bcx}+1} \right) \right]}{R_{CI}} \tag{3.64}$$

where

$$K_{bci} = \left[1 + \gamma \exp\left(\frac{V_{BCI}}{V_T}\right)\right]^{1/2} \tag{3.65}$$

$$K_{bcx} = \left[1 + \gamma \exp\left(\frac{V_{BCX}}{V_T}\right)\right]^{1/2} \tag{3.66}$$

Moreover, an alternative velocity saturation model is introduced,

$$\mu = \mu_0/[1 + (\mu_0 \delta \phi_e / v_{sat})^2]^{1/2} \tag{3.67}$$

Meanwhile, converting V_{rci} into $I_{epi0}R_{CI}$, the current across R_{CI} becomes

$$I_{rci} = \left(\frac{I_{epi0}}{\left[1 + \frac{I_{epi0}R_{CI}}{V_O\left(1+\frac{0.5(V_{rci}^2+0.01)^{1/2}}{V_O H_{RCF}}\right)}\right]^2} \right)^{1/2} \tag{3.68}$$

where H_{RCF} is a dimensionless fitting parameter that allows one to partially replace V_O by V_{RCI}.

3.4 The Parasitic PNP Transistor

For the npn bipolar device with a p-type substrate, the parasitic vertical pnp transistor formed by the BC and CS junctions can be modeled by a simplified Gummel-Poon

equivalent circuit. The forward current can be written as

$$I_{tfp} = I_{SP}\left[W_{SP}\exp\left(\frac{V_{BEP}}{N_{FP}V_T}\right) + (1 - W_{SP})\exp\left(\frac{V_{BCI}}{N_{FP}V_T}\right) - 1\right] \tag{3.69}$$

The normalized base charge of the parasitic transistor only comprises high-level injection effects, as the Early effect can be neglected, so

$$q_{bp} = 1 + \frac{q_{2p}}{q_{bp}} \tag{3.70}$$

$$q_{2p} = \frac{I_{tfp}}{I_{KP}} \tag{3.71}$$

The parasitic base currents are then modeled similar to the internal EB base current.

3.5 Temperature Mapping

The temperature effects of saturation currents, current gains, serious resistances, and depletion capacitances in BJT are all modeled in the VBIC model.

3.5.1 Resistance

The temperature dependence of the series resistances is modeled as:

$$R_X(T) = R_X(T_{nom})\left(\frac{T}{T_{nom}}\right)^{X_{RX}} \tag{3.72}$$

Here, X_{RX} is different for the emitter, base, collector and substrate resistances.

3.5.2 Capacitance

The temperature dependence of zero-bias depletion capacitances is modeled as:

$$C_X(T) = \left(\frac{P_X(T)}{P_X(T_{nom})} \right)^{M_X} \tag{3.73}$$

where M_X denotes the grading exponent of the corresponding junction. The built-in voltage P_X is modeled by a temperature-dependent function derived from

$$P_X = V_T \left(\frac{n_{n0} p_{p0}}{n_{ie}^2} \right) \tag{3.74}$$

3.5.3 Knee current I_{KF}

The Knee current I_{KF} was originally used as the onset of the high injection effect in the base, but in the VBIC model it is used as an empirical parameter. The temperature dependence of the Knee current I_{KF} is modeled as:

$$I_{KF}(T) = I_{KF}(T_{nom}) \left(\frac{T}{T_{nom}} \right)^{X_{IKF}} \tag{3.75}$$

where X_{IKF} is the temperature coefficient for I_{KF}.

3.5.4 Ideality Factor N_F

N_F is the ideality factor for the collector current I_C. The temperature dependence of N_F is modeled as:

$$N_F(T) = N_F(T_{nom})\left(1 + T_{nf} d_T\right) \tag{3.76}$$

where T_{nf} is the temperature coefficient for N_F. $d_T = T - T_{nom}$.

3.5.5 Saturation Current I_S

From (3.15) and (3.19), assuming that freezeout does not occur, Q_{B0} is independent of temperature and the saturation current I_S is

$$I_S(T) = A_E \frac{q^2 D_n(T) n_i^2(T)}{Q_{B0}} \tag{3.77}$$

At the reference temperature T_{nom},

$$I_S(T_{nom}) = A_E \frac{q^2 D_n(T_{nom}) n_i^2(T_{nom})}{Q_{B0}} \tag{3.78}$$

which becomes

$$I_S(T) = I_S(T_{nom}) \frac{D_n(T)}{D_n(T_{nom})} \frac{n_i^2(T)}{n_i^2(T_{nom})} \tag{3.79}$$

$$= I_S(T_{nom}) \frac{T}{T_{nom}} \frac{\mu_n(T)}{\mu_n(T_{nom})} \frac{n_i^2(T)}{n_i^2(T_{nom})} \tag{3.80}$$

Since n_i^2 is proportional to $T^\gamma \exp\left(-\frac{E_g(T)}{kT}\right)$, and μ_n is proportional to T^{-m}, (3.80) can be rewritten as

$$I_S(T) = I_S(T_{nom}) \left(\frac{T}{T_{nom}}\right)^{\gamma+1-m} \exp\left(-\frac{E_g(T)}{kT} + \frac{E_g(T_{nom})}{kT_{nom}}\right) \tag{3.81}$$

$$= I_S(T_{nom}) \left(\frac{T}{T_{nom}}\right)^{X_{TI}} \exp\left(-\frac{E_g(T)}{kT} + \frac{E_g(T_{nom})}{kT_{nom}}\right) \tag{3.82}$$

where E_g is the bandgap energy, and$X_{TI} = \gamma + 1 - m$. Assuming linear T dependence of $E_g(T)$,

$$E_g(T) = E_g(0) - \alpha T \tag{3.83}$$

Thus,

$$-\frac{E_g(T)}{kT} + \frac{E_g(T_{nom})}{kT_{nom}} = -\frac{1}{kT}\left(E_g(0) - \alpha T - (E_g(0) - \alpha T_{nom})\frac{T}{T_{nom}}\right) \tag{3.84}$$

$$= -\frac{1}{kT} E_g(0) \left(1 - \frac{T}{T_{nom}}\right) \tag{3.85}$$

Substituting (3.85) in (3.82) gives

$$I_S(T) = I_S(T_{nom}) \left(\frac{T}{T_{nom}}\right)^{X_{TI}} \exp\left[-\frac{1}{kT} E_a \left(1 - \frac{T}{T_{nom}}\right)\right] \tag{3.86}$$

$$E_a = E_g(0) \tag{3.87}$$

The general temperature dependence of saturation currents is therefore modeled in VBIC as:

$$I_X(T) = I_X(T_{nom}) \left(\frac{T}{T_{nom}} \right)^{X_X/N_X} \exp \left[-\frac{E_X}{N_X V_T} \left(1 - \frac{T}{T_{nom}} \right) \right] \tag{3.88}$$

The temperature variation of the current gain is directly determined by the temperature dependences of the saturation currents. The thermal network in Fig. 3.1 can be used to calculate the excess temperature due to the power dissipated in the device.

CHAPTER 4

VERILOG-A IMPLEMENTATION

The Verilog-A language and VBIC model have been introduced in Chapter 2 and Chapter 3. In this chapter, the VBIC model is reframed in Verilog-A language, and implemented into two circuit simulators, Cadence and ADS. The major problems such as syntax errors, convergence problems and numerical problems, are solved. The DC, *ac*, noise and large signal simulation comparisons between Verilog-A based VBIC modeling and the Cadence built-in VBIC model show identical results.

4.1 Basic code description

The Verilog-A code, based on VBIC version 1.2, used in this thesis can be downloaded from several open source websites [9] [10] [11] and was automatically generated from special code. The four terminal mode was chosen to ensure consistency with the IBM design kit used in this work.

The Verilog-A based VBIC code includes the basic node definitions, branch definitions, parameter definitions, temperature mappings, electrical branch constituent relations, and branch contributions for the VBIC model. The thermal network and excess phase network are also included.

The major improvements introduced in the version 1.2 Verilog-A based VBIC code compared to previous versions include:

- base-emitter breakdown model added
- bug in built-in potential fixed
- smooth depletion capacitance model re-parameterized
- separate temperature dependencies added for all resistances and I_{SP}
- temperature dependence added for I_{KF}
- reach-through voltage for C_{bc} limiting added
- ability to separately control saturation current I_S in reverse operation (GaAs/AlGaAs HBTs)
- only one thermal node is used, and *tl* was dropped (this was deemed unnecessary as it was never used in implementations)
- reference directions of current sources in thermal end excess-phase networks were changed, to be from node to ground (for Verilog-A compatibility)
- transport current explicitly separated into forward and reverse components, for convenience and compatibility of code between constant and excess-phase versions
- N_{KF} parameterization of forward beta rolloff added
- ability to switch to SGP base charge formulation added (Q_{BM})

4.2 Implementation into Simulators

4.2.1 Implementation into Agilent ADS

In Agilent ADS, a directory called **veriloga** was created for the current project, and the Verilog-A module was placed in that directory [12]. The Verilog-A module can be instantiated as a symbol using the "User Compiled Models", which is a function provided in ADS. The Verilog-A compiler in ADS, developed by Tiburon Design Automation, then automatically compiles all Verilog-A files in the ADS Project **veriloga** directory into simulator. This compiler-based solution results in a simulation time for the Verilog-A based models that is comparable to that of the built-in models.

4.2.2 Implementation into Cadence

The same Verilog-A VBIC model code used in ADS can also be implemented into Cadence. In Cadence, a Verilog-A module can be created using the Verilog-A editor without modifying the interface between the internal compact model and the simulator [13]. The newly created Verilog-A module can then be instantiated into the simulator, and added into the new schematic window as a symbolic view instance. Here, the Verilog-A based VBIC model code was implemented into Cadence in the same way.

The discussions in the following sections in this chapter are all based on the Verilog-A based VBIC code implemented in Cadence.

4.3 Main debugging issues

Since the Verilog-A based VBIC code downloaded from open websites is automatically generated from special code, it could not be directly used in Cadence and ADS due to syntax errors. Moreover, the convergence problems induced by numerical issues had to be considered in common Verilog-A based model coding. The main debugging procedures involved were as follows.

4.3.1 Syntax Errors

Cadence does not support the symbol `$limexp`, which is defined in the Verilog-A VBIC code in order to achieve better convergence. Consequently, all the syntax errors due to `$limexp` had to be corrected to `limexp`. For instance, the Verilog-A equation for the forward transit time `tff` is defined as:

```
tff=TF*(1.0+QTF*q1)*(1.0+XTF*$limexp(V(bci)*IVTF/1.44)
       *(slTF+mIf*mIf)*sgIf);
```

For this project, it had to be modified to:

```
tff=TF*(1.0+QTF*q1)*(1.0+XTF*limexp(V(bci)*IVTF/1.44)
       *(slTF+mIf*mIf)*sgIf);
```

The module name `vbic` in Verilog-A VBIC code also conflicts with the primitive definition in Cadence, causing a name duplication in the primitive VBIC. It was therefore corrected to `vbicfinal`.

4.3.2 Convergence Problems

Once the syntax errors had been dealt with, the Verilog-A based model was implemented into Cadence. However, the DC and *ac* simulations suffered from convergence problems, especially for the large signal simulations. Since the high level Verilog-A description had to be automatically converted to low level simulator code, junction limiting and linearization of exponentials must be explicitly handled to aid convergence and prevent numerical overflow [14].

The simulator global parameters `gmin`, `imax`, and `imelt` set the limitation of the diode-like branch current level. The main purpose of explicitly adding these global parameters was to help with convergence. They also solved the ambiguity problem induced by the linearization scheme in the `limexp` function [14]. The `gmin` related current in the Verilog-A code was therefore added in each diode-like branch as follows:

```
Ibe = Ibe + gmin * V(bei);
Ibex = Ibex + gmin * V(bex);
Ibep = Ibep + gmin * V(bep);
Ibc = Ibc + gmin * V(bci);
Ibcp = Ibcp + gmin * V(bcp);
```

where `gmin` = 1.0e-12. `imax` is the branch current threshold. If `imax` is exceeded during iterations, the linear model is used instead of the exponential model until the current drops below `imax`, or until convergence is achieved. The `imelt` serves as a limit warning for the junction current [15]. Using the forward transport current I_{tf} as an example, the

programming flow is as follows [16]. Defining $V_{max} = N_F V_T \ln\left(\frac{imax}{I_S} + 1\right)$, if $V_{BEI} < V_{max}$,

$$I_{tf} = I_S \left[\exp\left(\frac{V_{BEI}}{N_F V_T}\right) - 1\right] \tag{4.1}$$

which is the normal exponential model. If $V_{BEI} \geq V_{max}$,

$$I_{tf} = imax + \frac{V_{BEI} - V_{max}}{N_F V_T}(imax + I_S) \tag{4.2}$$

which becomes the linear model of V_{BEI}. All other currents are limited in the same way. An example of I_{tf} in Verilog-A is as follows. First, an analog function `expf` that includes a switch to the exponential model and the linear model controlled by the threshold current `imax` is defined for a junction current. This analog function is suitable for all the junction currents.

```
analog function real expf;
  input v,fac1,fac2;
  real v,fac1,fac2;
  real vmax, expL;
  begin
  if (fac2>0) begin
      vmax= fac1*ln(1.0+imax/fac2);
    end else begin
```

```
      vmax = 0.0;
    end
  expL = limexp(v/fac1);
  if (v<vmax) begin
      expf = expL;
    end else begin
      expf = imax+(v-vmax)*(imax+fac2)/fac1;
    end
  end
endfunction
```

Finally, the `Ifi` is written as,

```
fac = NFatT*Vtv;
expfi = expf(V(bei),fac, ISatT);
Ifi = ISatT*(limexp(expfi)-1);
```

The `imelt`, used for a current limit warning in a single branch like `be`, is described as,

```
if (I(be) > imelt)
     $strobe( "Warning: branch be is melting!" );
```

The Warning message "`Warning: branch be is melting!`" will be displayed in the output log file. If it is used for port current, like `b`, it is described as,

```
if (I(<b>) > imelt)
     $strobe( "Warning: device port b is melting!" );
```

4.3.3 Logarithm Error

Once the convergence problems had been solved, the Verilog-A based model ran relatively smoothly and fast. However, the Verilog-A based model DC and *ac* simulation results failed to produce the same results as the Cadence built-in VBIC model. Carefully debugging the code revealed that it was the definition of `log` that was causing the deviations. In Verilog-A, `log` stands for $\log_{10}$, not $\log_e$ as needed here. Therefore, `ln` must be used instead of `log`.

In the original Verilog-A VBIC code, the function definitions of `psiio`, `psiin`, and `psibi` are related to the temperature mapping model of all the capacitances. They are defined using `log`, as shown in the following,

```
psiio = 2.0*(Vtv/rT)*log(exp(0.5*P*rT/Vtv)-exp(-0.5*P*rT/Vtv));
psiin = psiio*rT-3.0*Vtv*log(rT)-Ea*(rT-1.0);
psibi = psiin+2.0*Vtv*log(0.5*(1.0+sqrt(1.0+4.0*exp(-psiin/Vtv))));
```

If `log` is not corrected to be `ln`, this will cause the inaccurate temperature mapping models observed for the capacitances. Even at room temperature, problems will occur in the high bias due to the self-heating effect. The corrected code becomes,

```
psiio = 2.0*(Vtv/rT)*ln(exp(0.5*P*rT/Vtv)-exp(-0.5*P*rT/Vtv));
psiin = psiio*rT-3.0*Vtv*ln(rT)-Ea*(rT-1.0);
```

```
psibi = psiin+2.0*Vtv*ln(0.5*(1.0+sqrt(1.0+4.0*exp(-psiin/Vtv))));
```

Another error introduced by the `log` definition is related to the epi layer current I_{rci}. The original code is,

```
Iohm=(V(rci)+Vtv*(Kbci-Kbcx-log(rKp1)))/RCIatT;
derf=IVO*RCIatT*Iohm/(1.0+0.5*IVO*IHRCF*sqrt(V(rci)*V(rci)+0.01));
Irci=Iohm/sqrt(1+derf*derf);
```

If not corrected, this causes an the error in I_{rci}. The corrected code becomes,

```
Iohm=(V(rci)+Vtv*(Kbci-Kbcx-ln(rKp1)))/RCIatT;
derf=IVO*RCIatT*Iohm/(1.0+0.5*IVO*IHRCF*sqrt(V(rci)*V(rci)+0.01));
Irci=Iohm/sqrt(1+derf*derf);
```

4.3.4 Noise Modeling

At present, the Verilog-A model does not include noise modeling. For RF simulation purposes, it is necessary to add in a noise modeling component in the Verilog-A based VBIC model in order to be consistent with the Cadence built-in model. The noise models were added as follows.

```
I(cei)  <+ white_noise(2*‘QQ*abs(Itzf));
I(bei)  <+ white_noise(2*‘QQ*abs(Ibe))
           +flicker_noise(KFN*pow(abs(Ibe,AFN),BFN);
I(bex) <+ white_noise(2*‘QQ*abs(Ibex))
```

```
            +flicker_noise(KFN*pow(abs(Ibex),AFN),BFN);
I(rcx) <+ white_noise(4*`KB*Tdev*(1/RCX));
I(rci)  <+ white_noise(4*`KB*Tdev*(1/RCI));
I(rbx) <+ white_noise(4*`KB*Tdev*(1/RBX));
I(rbi) <+ white_noise(4*`KB*Tdev*(1/RBI));
I(re)  <+ white_noise(4*`KB*Tdev*(1/RE));
I(rs)  <+ white_noise(4*`KB*Tdev*(1/RS));
I(cep) <+ white_noise(2*`QQ*abs(Iccp));
I(bep) <+ white_noise(2*`QQ*abs(Ibep))
            +flicker_noise(KFN*pow(abs(Ibep),AFN),BFN);
I(rbp) <+ white_noise(4*`KB*Tdev*(1/RBP));
```

4.4 Comparison with built-in model

Finally, the complete Verilog-A based VBIC model was successfully implemented into Cadence. The DC, *ac*, noise, and large signal simulation results for a 50 GHz technology device were compared between the Verilog-A based VBIC model and Cadence built-in VBIC model. The emitter area used was 0.5×2.5 μm^2. The results of the comparison show that the new Verilog-A based VBIC model is identical to the Cadence built-in VBIC model.

4.4.1 DC Simulation

Fig. 4.1 (a) shows a Gummel curve comparison of the Verilog-A based VBIC model and Cadence built-in VBIC model. Perfect agreement is achieved. A comparison of the output curves of the Verilog-A based VBIC model and the Cadence built-in VBIC model is shown in Fig. 4.1 (b). The Verilog-A based VBIC model clearly agrees with the Cadence built-in VBIC model very well.

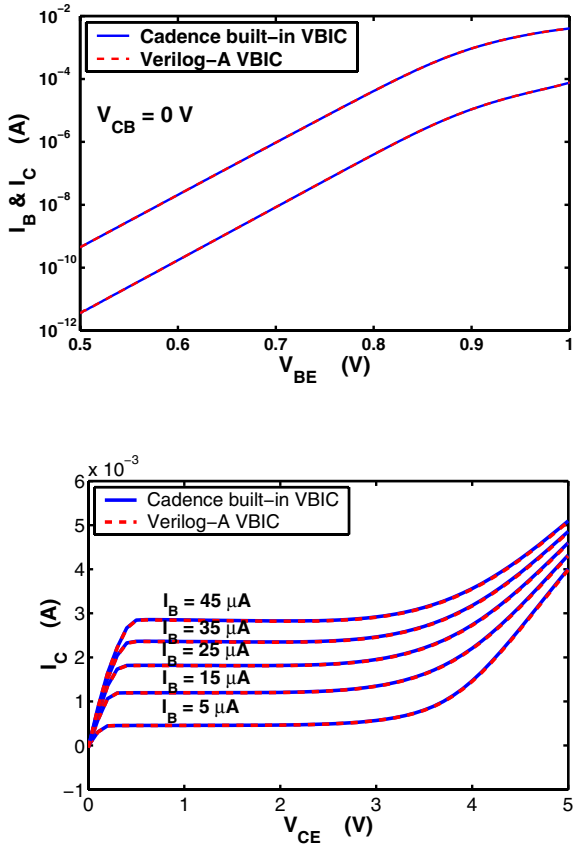


Figure 4.1: (a) Gummel curve comparison of Verilog-A based VBIC model and Cadence built-in VBIC model. (b) Output curve comparison of Verilog-A based VBIC model and Cadence built-in VBIC model.

4.4.2 *ac* Simulation

Fig. 4.2 and 4.3 show the comparisons of the bias and frequency dependence of S-parameters for the Verilog-A based VBIC model and the Cadence built-in VBIC model. All of the S-parameters of the Verilog-A based VBIC model are identical to the Cadence built-in VBIC model. Since the S-parameters of the Verilog-A based VBIC model are identical to the Cadence built-in VBIC model, the cutoff frequency f_T is the same for the two models, as shown in Fig. 4.4.

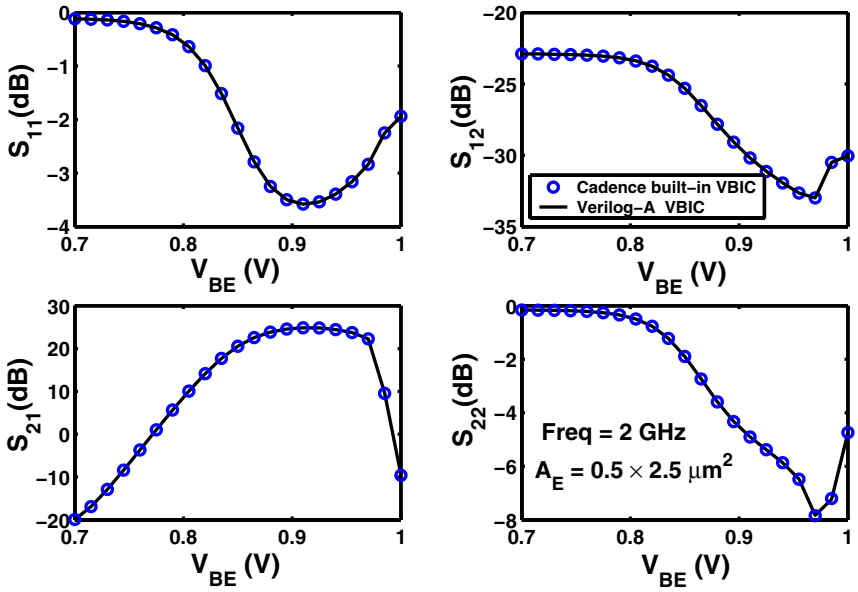


Figure 4.2: S-parameters vs V_{BE} curves of Verilog-A based VBIC model and Cadence built-in VBIC model.

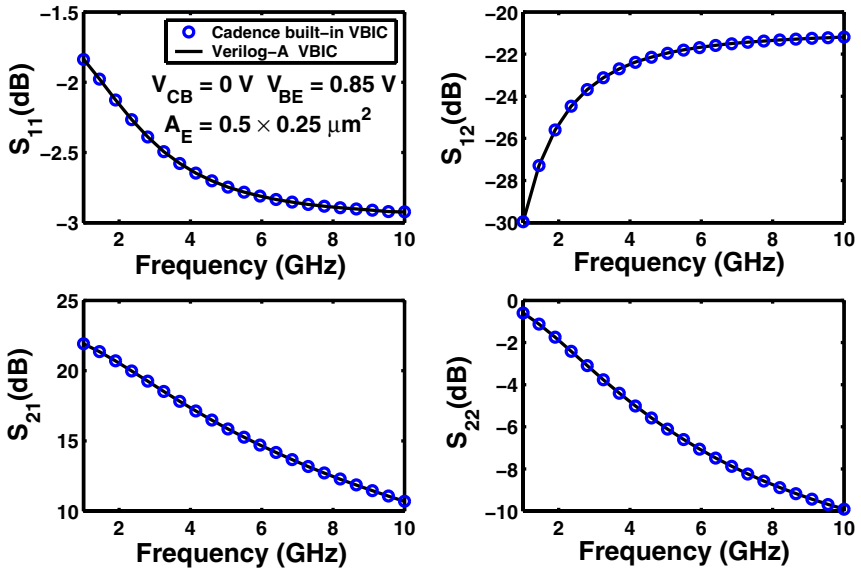


Figure 4.3: S-parameters vs f curves of Verilog-A based VBIC model and Cadence built-in VBIC model.

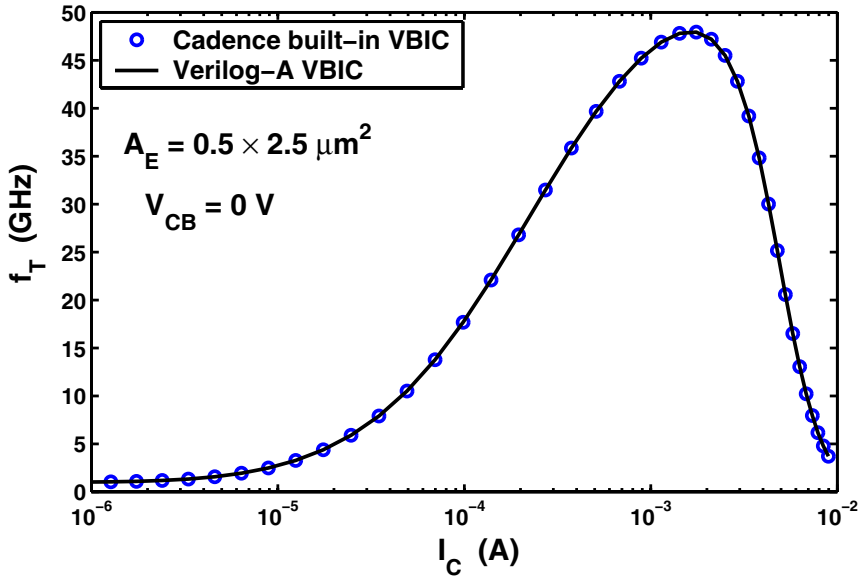


Figure 4.4: f_T vs I_C of Verilog-A based VBIC model and Cadence built-in VBIC model.

4.4.3 Noise Simulation

The Verilog-A based VBIC model generates identical minimum noise figure NF_{min} and noise resistance R_n results to the Cadence built-in VBIC mode, as shown in Fig. 4.5.

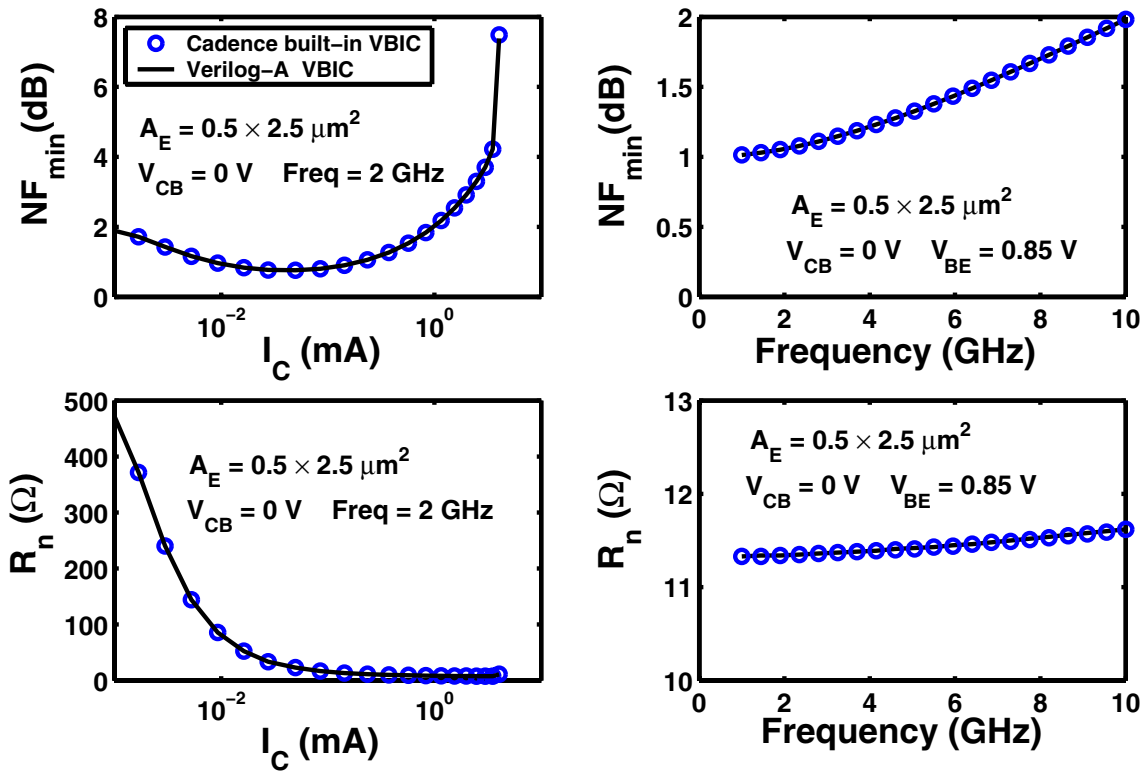


Figure 4.5: Bias and frequency dependence of NF_{min} and R_n of Verilog-A based VBIC model and Cadence built-in VBIC model.

4.4.4 Large Signal Simulation

P_{out} vs P_{in} of Verilog-A based VBIC model and Cadence built-in VBIC model are compared in Fig. 4.6. The results show that the Verilog-A based VBIC model produces identical large signal simulation results to the Cadence built-in VBIC mode.

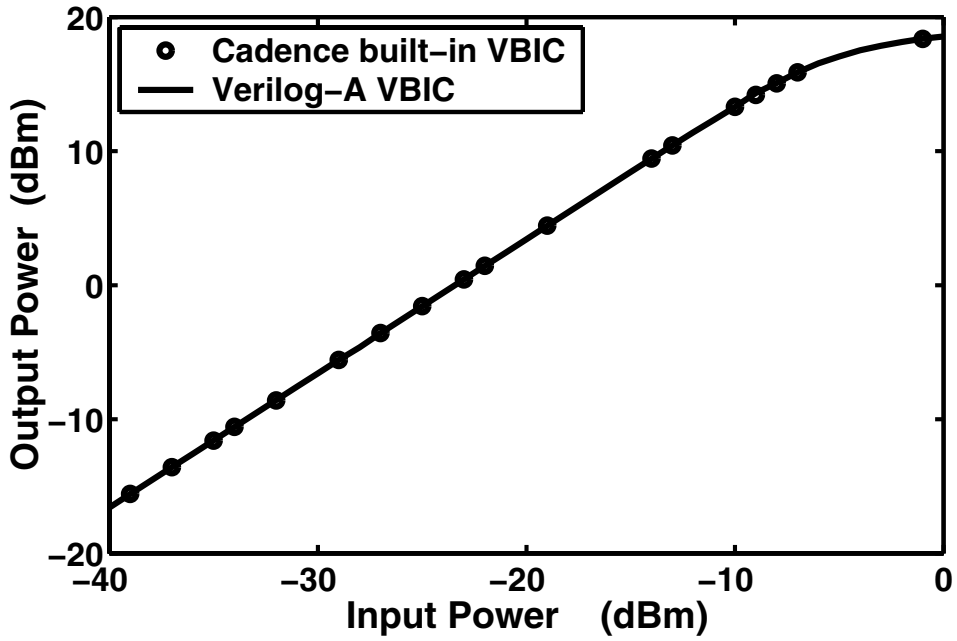


Figure 4.6: P_{out} vs P_{in} of Verilog-A based VBIC model and Cadence built-in VBIC model.

4.5 Summary

The VBIC model was converted into the Verilog-A language, and implemented into circuit simulators Cadence and ADS. The main problems that arose, including syntax errors, convergence problems and numerical problems, were solved. Noise models

were then added to the Verilog-A based model to be consistent with the Cadence built-in model. Comparisons of the DC, *ac*, noise and large signal simulation comparisons between the Verilog-A based VBIC model and the Cadence built-in VBIC model revealed identical results.

CHAPTER 5

USING VERILOG-A FOR SIGE HBT NOISE MODELING

As discussed in Chap 2, the main reason for using Verilog-A based modeling is its convenience, as it can be easily modified without the need to interface with the circuit simulator. In addition, the internal currents, capacitors, and noise sources are accessible, which is not the case for built-in models. This makes it possible for device and modeling researchers to investigate the device physics and modeling in detail and more efficiently. In this chapter, two Verilog-A based VBIC model applications for SiGe HBT noise modeling are presented.

5.1 Inverse circuit simulation for $1/f$ Noise

Transistor low-frequency noise is an important issue in both the baseband and RF circuits of a wireless transceiver due to its conversion to phase noise. In a bipolar transistor, the major low-frequency noise source lies in the base current. Experimentally, it has been established that this base current noise source is located between the internal base and emitter nodes in an equivalent circuit. This base current low-frequency noise, denoted as i_{bn}, is often measured indirectly from the collector voltage noise by applying to the transistor base a source impedance that is much greater than the input impedance, as shown in Fig 5.1. The measured collector voltage noise is converted to collector current noise using $S_{I_C} = S_{V_C}/R^2_{C,eff}$ which is then converted to the base current noise using $S_{I_B} = S_{I_C}/\beta^2_{ac}$, with β_{ac} being the low-frequency small signal ac current gain. β_{ac}

is often determined from the device's Gummel characteristics, measured under a biasing condition close to that used in the noise measurement. The base current noise can also be measured "directly" from the base using a high precision current amplifier with an input impedance much lower than the transistor input impedance. Each method has its advantages and disadvantages in practice, as discussed in [17]. In general, the indirect method is easier to implement, and is widely used. The indirect method was applied for this research project [18]. Similar limitations and assumptions exist in the "direct" measurement method.

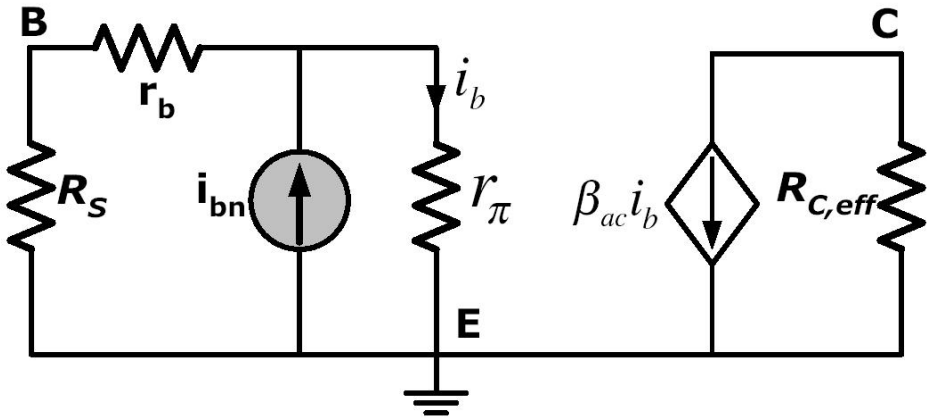


Figure 5.1: Small signal equivalent circuit assumed in the conventional method.

The widely used conventional measurement method is based on a simplified equivalent circuit derived under isothermal conditions. However, in modern SiGe HBTs, self-heating can be significant, in part due to their high operating current density. To enable high current density operation, the collector doping is increased with device vertical

scaling, which then increases the collector-base junction field and thus creates problems with avalanche multiplication. Errors are therefore expected in the low-frequency noise measured using conventional method in high speed SiGe HBTs.

Here, a new method was developed to extract the base current low-frequency noise that takes into account the higher order physical effects that are significant in modern SiGe HBTs, such as avalanche multiplication and self-heating. Instead of basing the extraction on a simplified small signal equivalent circuit, the same circuit as that used in noise measurement was simulated. The circuit simulator used in this work was Cadence SpectreRF. For a given internal base current noise excitation, the collector voltage noise was simulated, and the noise transfer function, or the noise gain G_{noise}, obtained from the ratio of the simulated collector voltage noise and internal base current noise excitation. The internal base current noise was then extracted from the measured collector voltage noise using $S_{I_B} = S_{V_C}/G_{noise}$. This extraction method is referred to as inverse circuit simulation based low-frequency noise extraction, as the input base current noise is essentially simulated from the measured output voltage noise.

The Verilog-A based VBIC model is the best way to implement this new inverse circuit simulation method due to its easy access to the internal base and collector currents, the key point of this method. The VBIC model also takes into account self-heating and avalanche multiplication effects. As a result, the impact of self-heating and avalanche multiplication on low-frequency noise extraction are automatically included. Furthermore, other non-ideal effects such as the Early effect, terminal parasitic resistances, and high injection effects are also accounted for.

When a unity magnitude small signal noise current is placed between the internal base and emitter nodes, the resulting collector voltage noise gives the noise gain. The measured collector voltage noise is then divided by the simulated noise gain for all frequencies to obtain the internal base current noise spectrum, i.e. $S_{I_{BE}} = S_{V_C}/G_{noise}$. Fig 5.2 compares the $S_{I_{BE}}$ spectra extracted using the conventional method and the proposed inverse circuit simulation method. $V_{CB} = 2$ V, $I_{BE} = 10\ \mu A$, terminal base current I_B is 8.1 μA,. The $S_{I_{BE}}$ extracted from inverse circuit simulation is almost 10 times higher than that from the conventional method.

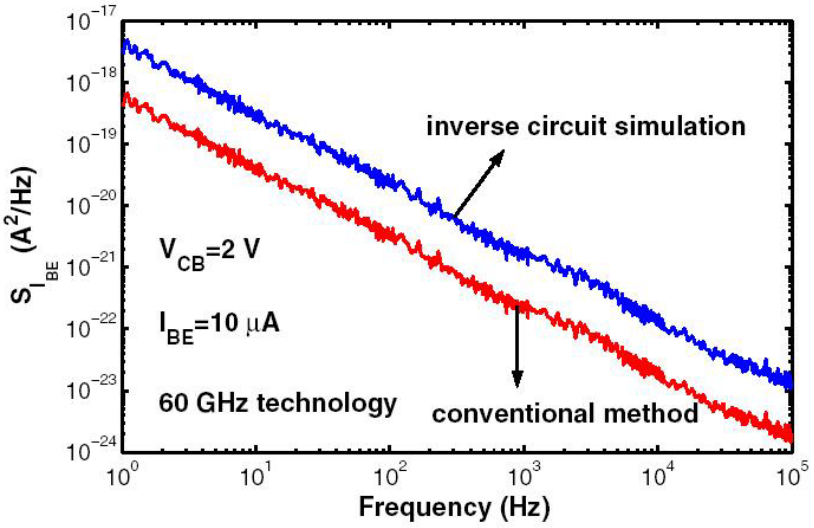


Figure 5.2: Comparison of $S_{I_{BE}}$ spectra extracted to the proposed inverse circuit simulation and the conventional measurement method. V_{CB}=2 V, I_{BE}=2 μA.

In the research reported here, an inverse circuit simulation based method was developed for the extraction of base current noise spectra in advanced SiGe HBTs. A

key difference from the conventional method is that the noise gain is obtained much more accurately by taking into account higher order effects such as avalanche multiplication and self-heating. The utility of the method was demonstrated by examining the collector-base voltage and base transport current dependence of $1/f$ noise. The proposed method can be applied to the extraction of the correlation between base current noise and collector current noise using a double channel dynamic signal analyzer.

5.2 Noise generating current in oscillators

Oscillator phase noise is an important concern for RF semiconductor technology. Physically speaking, oscillator phase noise results from transistor $1/f$ noise, base resistance thermal noise, the base and collector current shot noise, as well as any other thermal noise sources in the passive components (e.g. inductors).

Besides $1/f$ noise, there is always thermal noise due to base resistance and the base and collector current shot noise associated with the DC currents. To identify the phase noise limitations of today's technologies, it is helpful to separate the phase noise contributions from various physical noise sources. The bottle neck of phase noise can then be identified and improved [19] [20].

In a small signal noise measurement, the transistor is biased at a fixed I_B or I_C. The small signal base current $1/f$ noise and base current shot noise are simple functions of the base terminal current I_B, and the collector current shot noise is simple function of terminal current I_C. In an oscillator, the situation is complicated as:

1. The terminal base current I_B has a large capacitive component, which does not contribute to either $1/f$ noise or shot noise. Instead, the internal base to emitter junction current, I_{BE}, is responsible for noise generation. This is illustrated in Fig. 5.3 using a simplified large signal transistor model. Similarly, the terminal I_C is different from the noise generating collector to emitter transport current I_{CE}.

2. The internal I_{BE} and I_{CE} responsible for base and collector current noise generation is periodically oscillating.

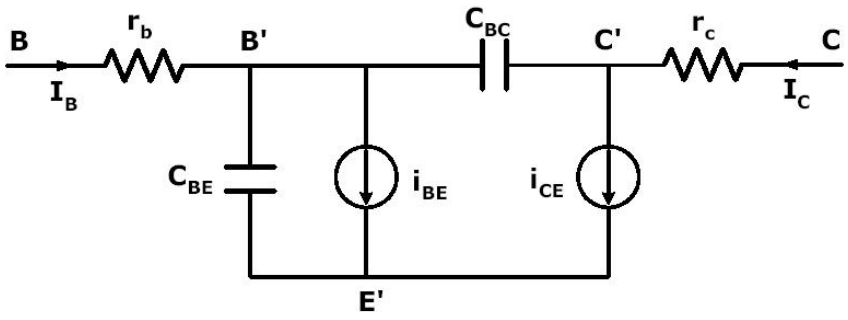


Figure 5.3: A simplified large transistor model.

Therefore, to understand the phase noise upconversion process, it is first necessary to separate the internal I_{BE} from the external I_B, and the internal I_{CE} from the external I_C. The internal I_{BE} and the internal I_{CE} can be accessed by the Verilog-A based VBIC model to better understand the different upconversion mechanisms of the base current $1/f$ noise and base current short noise.

Fig. 5.4 shows the waveforms of the terminal I_B, the noise generating internal I_{BE}, and internal base-emitter voltage V_{BE} for an oscillator designed with the 50 GHz peak f_T SiGe HBT. The difference between I_B and I_{BE} is obvious even where the device peak f_T is much higher than the oscillation frequency (5.5 GHz). Due to the nature of oscillations, the base emitter junction is turned on and off periodically, as shown on the right y-axis of Fig. 5.4 . A significant portion of the terminal base current is due to capacitive charging and discharging of the strongly nonlinear junction capacitances. The noise generating current, I_{BE}, is only a small portion of the terminal I_B.

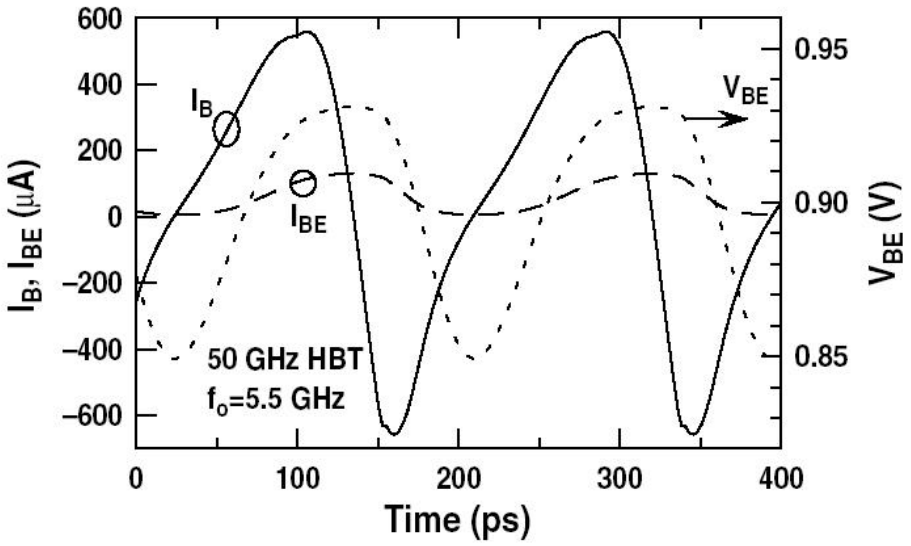


Figure 5.4: Comparison of terminal I_B and internal I_{BE} for the 50 GHz HBT. The internal V_{BE} is shown on the right y-axis.

5.3 Summary

Using the Verilog-A base VBIC model, a new inverse circuit simulation based method for extraction of base current noise spectra in advanced SiGe HBTs was proposed. The utility of the method was demonstrated by examining the collector-base voltage and base transport current dependence of $1/f$ noise. To better understand the different upconversion mechanisms of the base current $1/f$ noise and base current short noise, the internal I_{BE} from the external I_B, and the internal I_{CE} from the external I_C were successfully separated by the Verilog-A based VBIC model.

CHAPTER 6

TEMPERATURE SCALABLE MODELING OF DC CURRENTS

SiGe HBTs have demonstrated their ability to operate over a wide temperature range that is of particular interest for designers of extreme environment electronics, from -230°C to 300°C, along with excellent tolerance to high doses of radiation [2]. This, together with its integration with CMOS, makes SiGe BiCMOS technology very attractive for implementing electronics for aviation and space exploration [21].

Of critical importance to successful circuit design is the availability of accurate device models. At present, designers of electronics for extreme environment electronics have to use the same device models used by general purpose electronics designers, which are only suitable between -55°C to 120°C. Fig. 6.1 compares the measured and simulated Gummel curves at 43 K and 85 K for an IBM SiGe HBT with 50 GHz peak f_T. The general purpose model parameters from IBM's design kit were used to generate the curves in the figure, which are intended for applications from -55°C to 120°C. Clearly, the VBIC model, as is, does not work well at these low temperatures.

A temporary solution is to use VBIC as an isothermal model. The temperature dependences of device parameters are turned off, and device parameters are extracted to fit measured data at a single temperature. This can be repeated for several temperature points across the temperature range of interest. Clearly, this approach does not allow for self-heating. More importantly, this approach cannot be used to design circuits that require continuous description of device performance over temperature [2], such as the

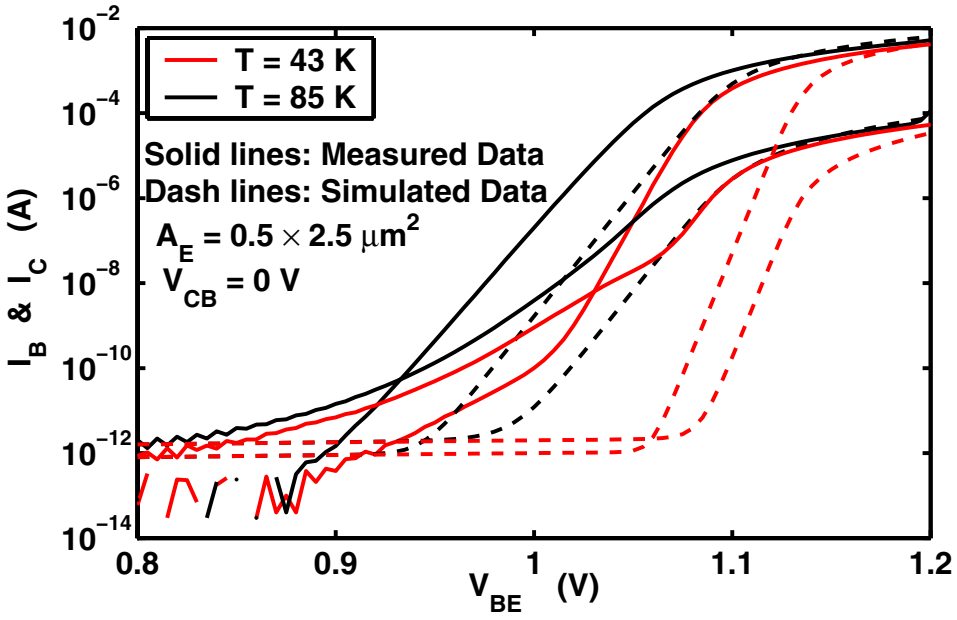


Figure 6.1: Comparison of Gummel curves from Cadence simulation results and measurement data at low temperatures.

bandgap reference circuit, a fundamental circuit block critical to the reliable operation of numerous analog, digital, and mixed-signal circuits over a wide range of temperatures. The VBIC model is chosen for these simulations as it is used in the design kit for this technology.

Here, the temperature dependence of key VBIC model parameters for DC current modeling from 300 K to 43 K was examined. The temperature mapping models were then evaluated. A group of improved temperature mapping models for DC currents were presented and implemented using Verilog-A, with an emphasis on lower temperature operation down to 43 K. Excellent fitting was obtained using a single set of model

parameters. These results are useful for the design of circuits that need to operate from 300 K down to 43 K [22].

6.1 Evaluation of Temperature Mapping Models in VBIC

The isothermal model parameters were first extracted using gradient search and quasi-Newton search optimization based on least-squares error functions. Device physics was considered during extraction to obtain physically meaningful parameters.

In VBIC, as outlined in Chapter 3, the collector current is described by

$$I_C = \frac{I_{tf} - I_{tr}}{q_b} \tag{6.1}$$

$$I_{tf} = I_S \left[\exp\left(\frac{V_{BEI}}{N_F V_T} \right) - 1 \right] \tag{6.2}$$

$$I_{tr} = I_S \left[\exp\left(\frac{V_{BCI}}{N_R V_T} \right) - 1 \right] \tag{6.3}$$

I_S and N_F are temperature dependent. The T dependence of I_S is described by

$$I_S(T) = I_{s,nom} r_T^{\frac{X_{is}}{N_{F,nom}}} e^{-\frac{E_a(1-r_T)}{N_{F,nom} V_T}} \tag{6.4}$$

where the subscript *nom* indicates nominal temperature, $r_T = T/T_{nom}$, X_{is} is the temperature exponent of I_S, and $E_a = E_g(0)$ is activation energy for I_S. The T dependence of N_F in VBIC is given by

$$N_F(T) = N_{F,nom}(1 + T_{nf} d_T) \tag{6.5}$$

where T_{nf} is temperature coefficient of N_F, and $d_T = T - T_{nom}$.

As shown in Eq. (6.5), N_F in VBIC is linearly dependent on temperature. The extracted isothermal N_F parameter, however, indicates a stronger dependence on temperature, as shown in Fig. 6.2. A similar temperature dependence is also observed for the extracted N_{EI} parameter, the counterpart of N_F for base current that is described in VBIC.

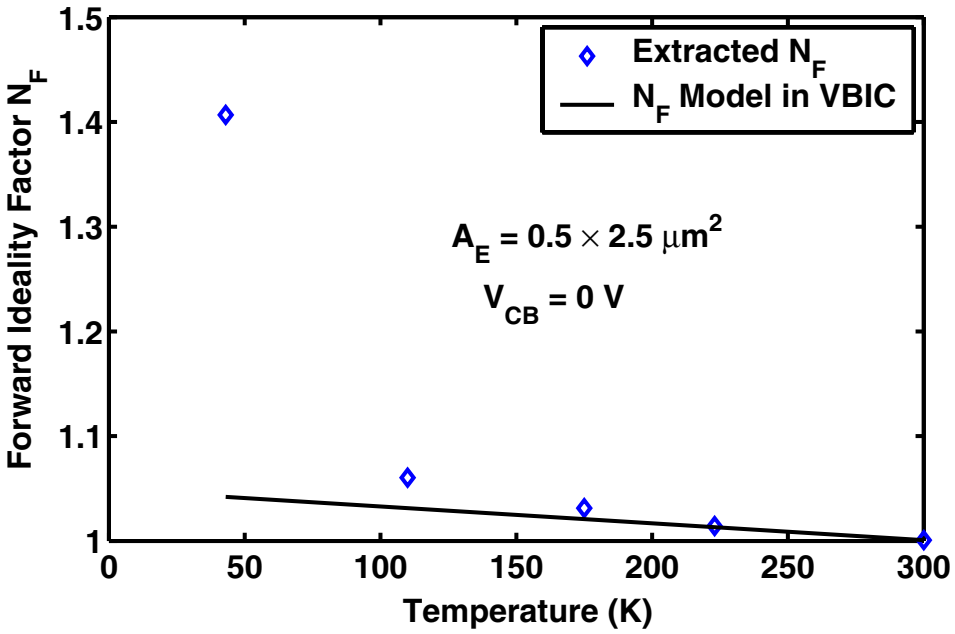


Figure 6.2: Comparison of extracted isothermal N_F and N_F temperature mapping model in VBIC.

Fig. 6.3 shows the extracted isothermal I_S vs temperature, together with fitting results using Eq. (6.4). The fitting is good at high temperature, but becomes worse at low temperatures. Attempts were made to calibrate temperature related parameter E_a

and X_{is} to obtain a better fitting, but it was not possible to fit the data for 43 K and 110 K simultaneously.

Other parameters related to DC current modeling were also extracted for all the temperatures, and their temperature mapping models were evaluated, including terminal resistances, quasi-saturation parameters, forward knee current I_{KF}, ideal B-E saturation current I_{BEI}, and so forth. In general, the temperature mapping models of many of the parameters in VBIC were not sufficient to cover the wide temperature range from 300 K to 43 K. Improved equations are therefore clearly necessary. For the following parameters, the temperature mapping models in VBIC were found to be sufficient:

1. terminal resistances: intrinsic base resistance R_{bi}, extrinsic base resistance R_{bx}, extrinsic collector resistance R_{cx}, and emitter resistance R_e.

2. quasi-saturation parameters: intrinsic collector resistance R_{ci}, epi drift saturation voltage V_o, epi doping parameter G_{amm}, and high current RC factor H_{rcf}.

The temperature mapping models of the key parameters that need to be improved for modeling over a wide temperature range are discussed below.

6.2 Improved Temperature Mapping Models

The primary reason for the limited applicable temperature range of current models is thought to be that the model equations were derived using simplified physics or assumptions that do not cover the wide temperature range of interest for this work. Improved temperature mapping models for key parameters of importance to DC currents

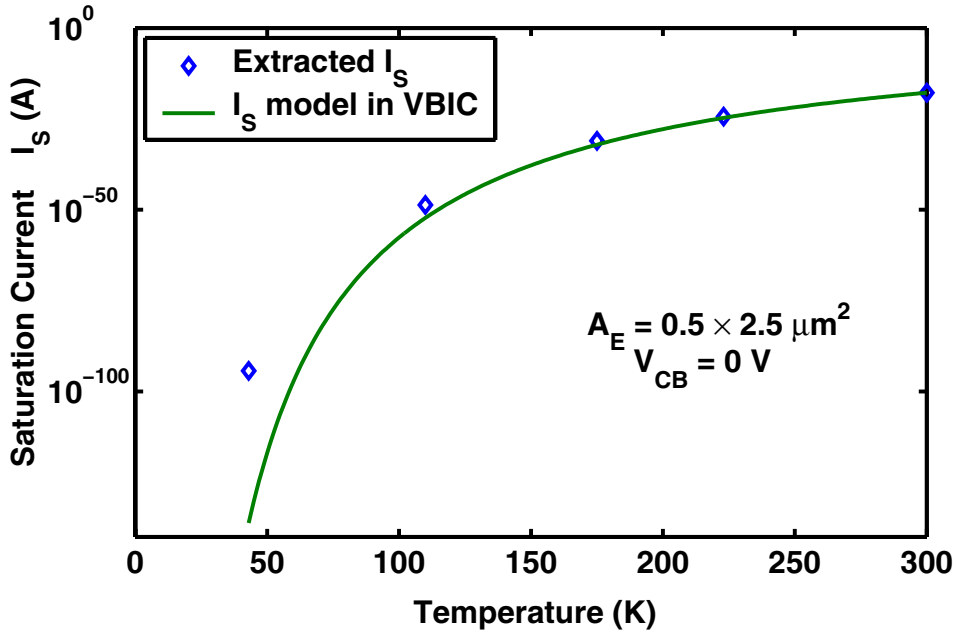


Figure 6.3: Comparison of I_S temperature mapping model in VBIC and extracted isothermal I_S parameters.

were therefore constructed. The corresponding Verilog-A code for each section can be found in Appendix A.

6.2.1 Improved N_F Temperature Mapping Model

As shown in Fig. 6.2, the ideality factor N_F increases exponentially with decreasing temperature as a result of carrier transport mechanism across the E-B heterojunction [23]. To better describe the temperature dependence of N_F, two extra terms, A_{nf} and X_{nf}, can be introduced based on the N_F temperature mapping model in VBIC. The

modified equation is

$$N_F(T) = N_{F,nom}(1 + T_{nf}d_T + A_{nf}(r_T^{X_{nf}} - 1)). \tag{6.6}$$

Similarly, N_{EI} also increases exponentially with decreasing temperature due to additional base current induced by extra recombination [23]. This can be modeled using the same temperature mapping equation, but with different $N_{F,nom}$, T_{nf}, A_{nf}, and X_{nf} values. Fig. 6.4 shows the improved N_{EI} and N_F modeling results using Eq. (6.6).

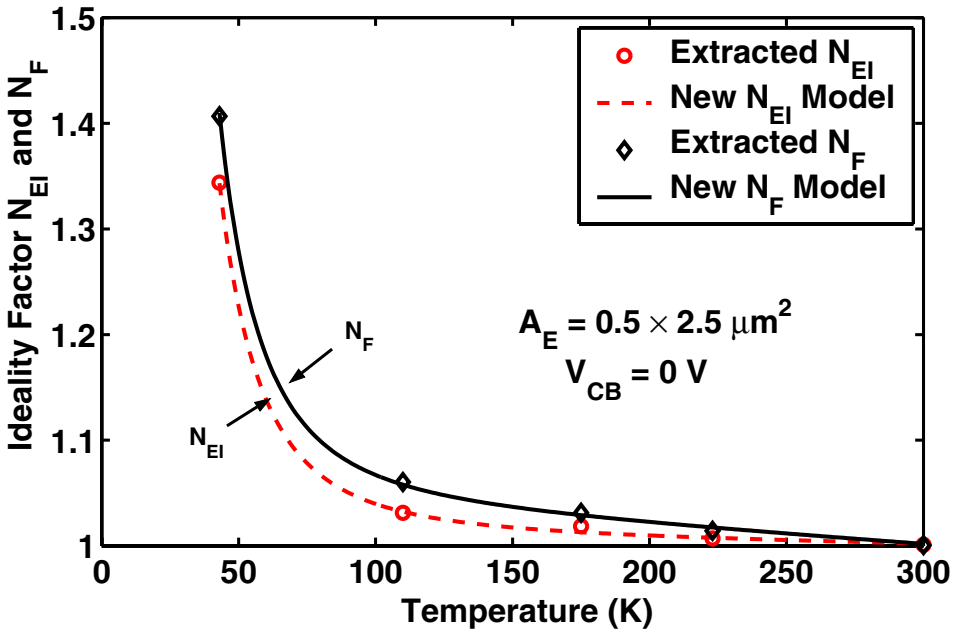


Figure 6.4: Improved N_{EI} and N_F model with new equations.

6.2.2 Improved I_S Temperature Mapping Model

The most significant parameter responsible for T dependence of I_S is E_a, which is essentially the bandgap energy at 0 K, and thus a constant. However, a close examination of the derivation of I_S shows that this is only true when the bandgap is assumed to be a linear function of temperature. This assumption becomes less valid, however, over a wide temperature range. A new derivation of I_S taking into account the nonlinear T dependence of the bandgap leads to a new I_S equation of similar form to (6.4), but with a temperature dependent activation energy, which we denote as $E_{a,true}$ [24]. The detailed derivation of $E_{a,true}$ is shown as follows. Physically, as derived in (3.82) in Chapter 3, I_S can be rewritten as

$$I_S(T) = I_S(T_{nom}) \left(\frac{T}{T_{nom}} \right)^{X_{IS}} \exp \left[-\frac{E_g(T)}{KT} + \frac{E_g(T_{nom})}{KT_{nom}} \right] \tag{6.7}$$

Empirically,

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta} \tag{6.8}$$

where α and β are temperature related parameters. E_g can be introduced into the exponential term of I_S. Let

$$A = -\frac{E_g(T)}{KT} + \frac{E_g(T_{nom})}{KT_{nom}} \tag{6.9}$$

$$= -\frac{1}{KT} \left[E_g(T) - E_g(T_{nom}) \frac{T}{T_{nom}} \right] \tag{6.10}$$

$E_g(T_{nom})$ is obtained by substituting T by T_{nom} in (6.8),

$$E_g(T_{nom}) = E_g(0) - \frac{\alpha T_{nom}^2}{T_{nom} + \beta} \tag{6.11}$$

Substituting (6.8) and (6.11) in (6.13) gives

$$A = -\frac{1}{KT}\left[E_g(0) - \frac{\alpha T^2}{T+\beta} - E_g(0)\frac{T}{T_{nom}} + \frac{\alpha T_{nom}^2}{T_{nom}+\beta}\frac{T}{T_{nom}}\right] \tag{6.12}$$

$$= -\frac{1}{KT}\left[E_g(0)\left(1 - \frac{T}{T_{nom}}\right) + \frac{\alpha T_{nom}^2}{T_{nom}+\beta}\frac{T}{T_{nom}} - \frac{\alpha T^2}{T+\beta}\right] \tag{6.13}$$

Let

$$B = \frac{\alpha T_{nom}^2}{T_{nom}+\beta}\frac{T}{T_{nom}} - \frac{\alpha T^2}{T+\beta} \tag{6.14}$$

$$= \frac{\alpha T^2 T_{nom} + \alpha\beta T T_{nom} - \alpha T^2 T_{nom} - \alpha\beta T^2}{(T+\beta)(T_{nom}+\beta)} \tag{6.15}$$

$$= \frac{\alpha\beta T T_{nom} - \alpha\beta T^2}{(T+\beta)(T_{nom}+\beta)} \tag{6.16}$$

$$= \frac{\alpha\beta T T_{nom}\left(1 - \frac{T}{T_{nom}}\right)}{(T+\beta)(T_{nom}+\beta)} \tag{6.17}$$

$$= \frac{\alpha\beta\frac{T}{T_{nom}} T_{nom}^2}{(T+\beta)(T_{nom}+\beta)}\left(1 - \frac{T}{T_{nom}}\right) \tag{6.18}$$

Substituting (6.18) into (6.13) produces

$$A = -\frac{1}{KT}\left[E_g(0)\left(1 - \frac{T}{T_{nom}}\right) + \frac{\alpha\beta\frac{T}{T_{nom}} T_{nom}^2}{(T+\beta)(T_{nom}+\beta)}\left(1 - \frac{T}{T_{nom}}\right)\right] \tag{6.19}$$

$$A = -\frac{1}{KT}\left(1 - \frac{T}{T_{nom}}\right)\left[E_g(0) + \frac{\alpha\beta\frac{T}{T_{nom}}(T_{nom})^2}{(T+\beta)(T_{nom}+\beta)}\right] \tag{6.20}$$

$$= -\frac{1}{KT}(1 - r_T)\left[E_g(0) + \frac{\alpha\beta r_T(T_{nom})^2}{(T+\beta)(T_{nom}+\beta)}\right] \tag{6.21}$$

Substituting (6.21) into (6.7), I_S becomes

$$I_S(T) = I_S(T_{nom})\left(\frac{T}{T_{nom}}\right)^{X_{IS}} \exp\left\{-\frac{1}{KT}(1 - r_T)\left[E_g(0) + \frac{\alpha\beta r_T(T_{nom})^2}{(T+\beta)(T_{nom}+\beta)}\right]\right\} \tag{6.22}$$

Comparing (6.22) to (3.86) in Chapter 3, the new E_a is

$$E_a(T) = E_g(0) + \frac{\alpha\beta r_T(T_{nom})^2}{(T+\beta)(T_{nom}+\beta)} \tag{6.23}$$

Mapping E_a from T_{nom} to T gives

$$E_a(T_{nom}) = E_g(0) + \frac{\alpha\beta(T_{nom})^2}{(T_{nom}+\beta)^2} \tag{6.24}$$

hence,

$$E_g(0) = E_a(T_{nom}) - \frac{\alpha\beta(T_{nom})^2}{(T_{nom}+\beta)^2} \tag{6.25}$$

Finally, $E_{a,true}$ is

$$E_{a,true}(T) = E_a(T_{nom}) + \frac{\alpha\beta r_T (T_{nom})^2}{(T+\beta)(T_{nom}+\beta)} - \frac{\alpha\beta (T_{nom})^2}{(T_{nom}+\beta)^2} \tag{6.26}$$

$$= E_{a,nom} + \frac{\alpha\beta^2 T_{nom}^2 (r_T - 1)}{(\beta + T_{nom})^2 (\beta + T)} \tag{6.27}$$

where $E_{a,nom} = E_a(T_{nom})$. Then I_S is changed to

$$I_S(T) = I_{s,nom} r_T^{\frac{X_{is}}{N_{F,nom}}} e^{-\frac{E_{a,true}(1-r_T)}{N_{F,nom} V_T}} \tag{6.28}$$

In addition, to alleviate the convergence problem at low temperatures, the temperature dependent parameter N_F is used to replace N_{Fnom} in the I_S equation. The new I_S equation is

$$I_S(T) = I_{s,nom} r_T^{\frac{X_{is}}{N_F}} e^{-\frac{E_{a,true}(1-r_T)}{N_F V_T}} \tag{6.29}$$

$E_{a,true}$ can be extracted as the E_a required to fit the I_S at each temperature in the original I_S model. Fig. 6.5 compares the extracted and modeled $E_{a,true}$. A good fitting has been obtained.

With the new I_S model, good I_S modeling is achieved, as shown in Fig. 6.6, from 300 K down to 43 K. The new I_S model is also expected to work at temperatures from 300 K to at least 400 K, the same range for which the conventional I_S model works. The same equation is also applied to describe the saturation current for I_B, I_{BEI}.

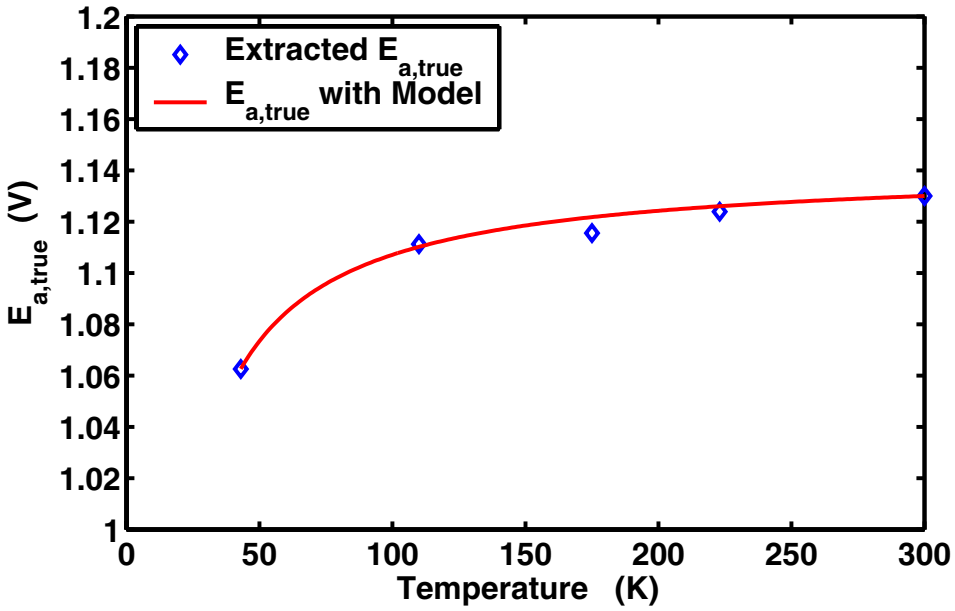


Figure 6.5: $E_{a,true}$ as a function of temperature fitted using Eq. (6.27).

6.2.3 Improved I_{KF} Temperature Mapping Model

The knee current I_{KF}, which was originally used to physically describe high injection in the base of a BJT, has now become an empirical parameter for SiGe HBT due to highly doped base. However, the I_{KF} extraction results show that the I_{KF} temperature mapping model in VBIC is no longer adequate for SiGe HBTs. A new temperature mapping model for I_{KF} is proposed

$$I_{KF}(T) = I_{KF,nom}(1 - T_{ikf}d_T + A_{ikf}(r_T^{X_{ikf}} - 1)) \tag{6.30}$$

Using Eq. 6.30, excellent fitting of I_{KF} is achieved, as shown in Fig. 6.7.

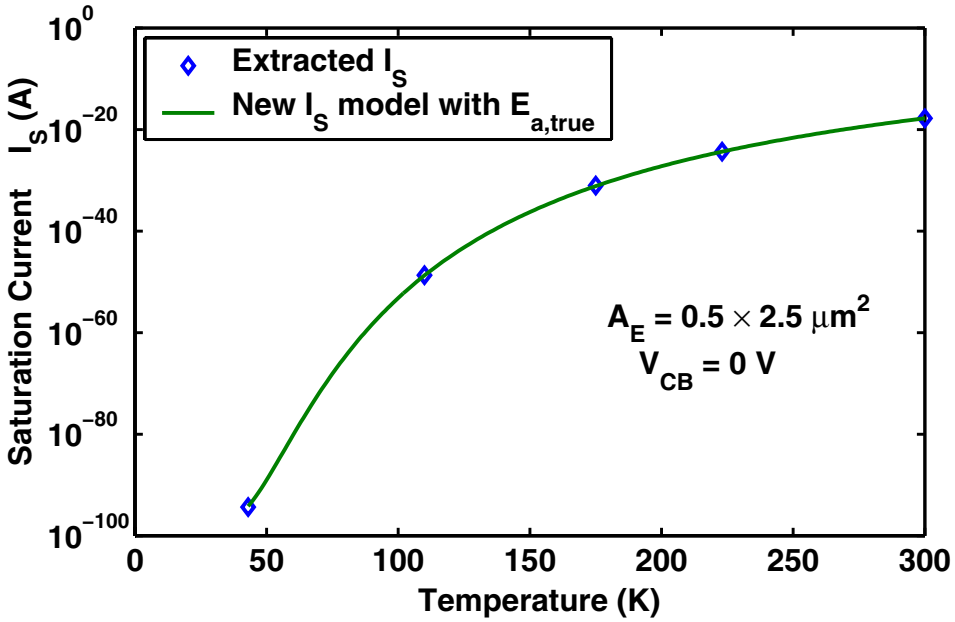


Figure 6.6: Improved I_S fitting with new $E_{a,true}$ model.

6.2.4 Temperature Mapping Models for R_{th} and $avc2$

The temperature dependence of thermal resistance R_{th}, which describes the excess temperature due to dissipated power, is not included in VBIC. The extracted R_{th} decreases with decreasing temperature. The temperature dependence of R_{th} can be modeled similarly to the way other regular resistances are modeled [25] [26].

The avalanche model parameter $avc2$ is a linear function of T in VBIC. A more complicated temperature model for better output curve fitting is therefore necessary. It has also been observed that the weak avalanche model itself in VBIC has limitations at 43 K, even when used as an isothermal model. Avalanche current data cannot be fitted by simply changing the temperature related avalanche parameters at 43 K.

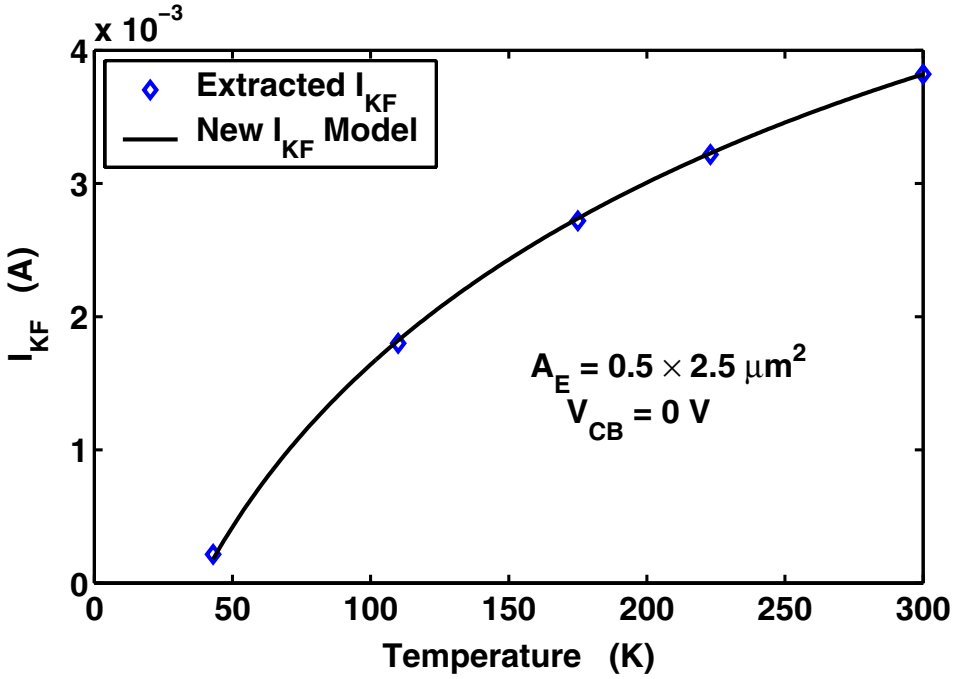
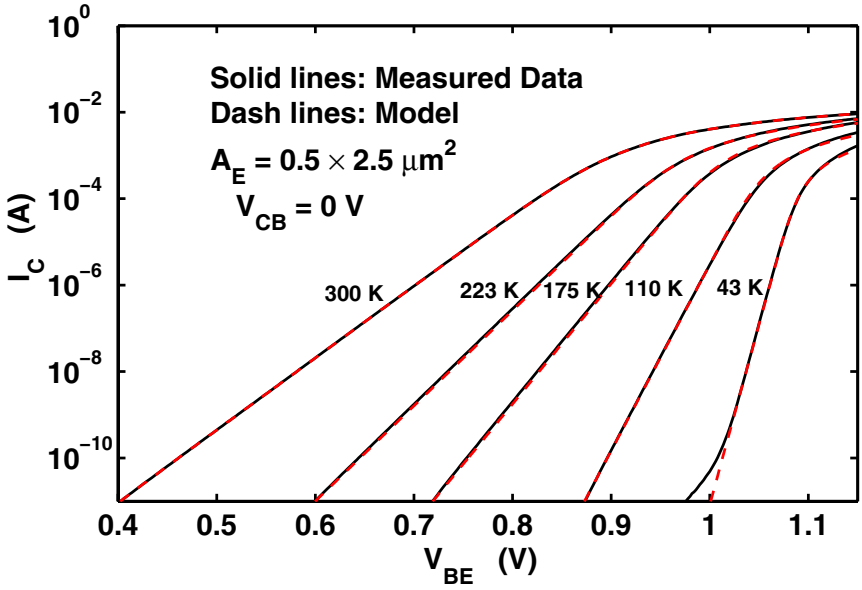


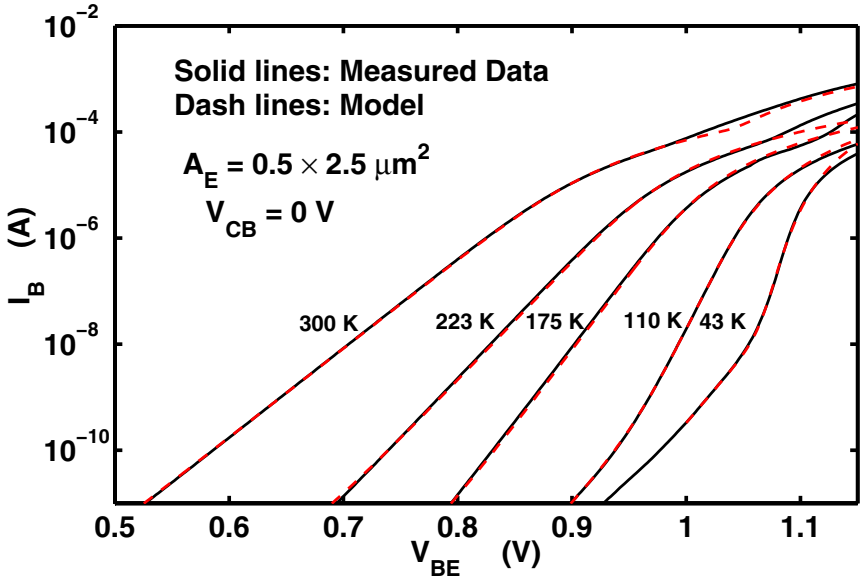
Figure 6.7: Improved I_{KF} fitting with new temperature mapping model.

6.3 Simulation Results

The VBIC based new model was implemented using Verilog-A, a hardware description language, compiled into binary code, and dynamically linked to a circuit simulator (ADS) through its compact modeling interface. Fig. 6.8 shows the collector current and base current modeling results. Good fitting down to 43 K was obtained. Fig. 6.9 (a) and (b) show the output curve modeling results at 175 K and 43 K, respectively. Good data-model fitting was obtained at both temperatures. Note that a single set of model parameters was used to achieve fitting at all temperatures.

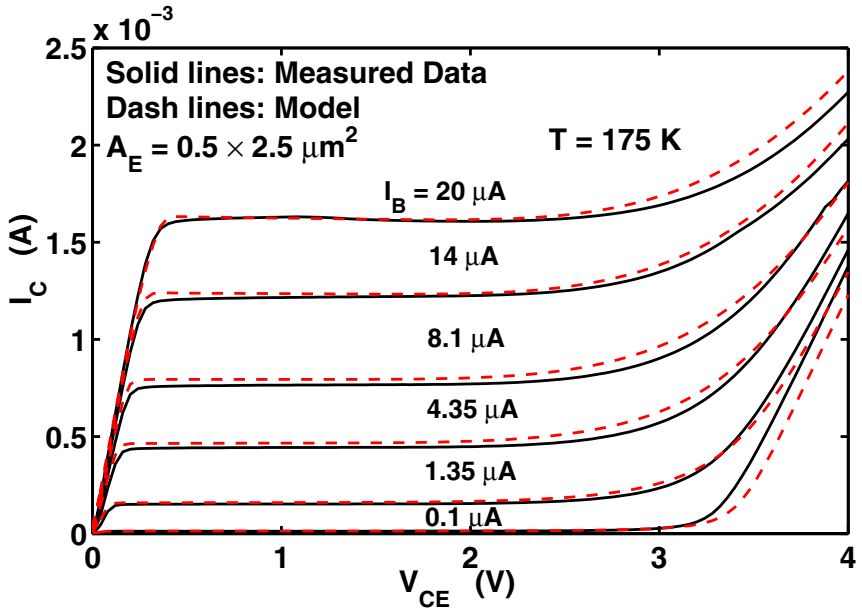


(a)

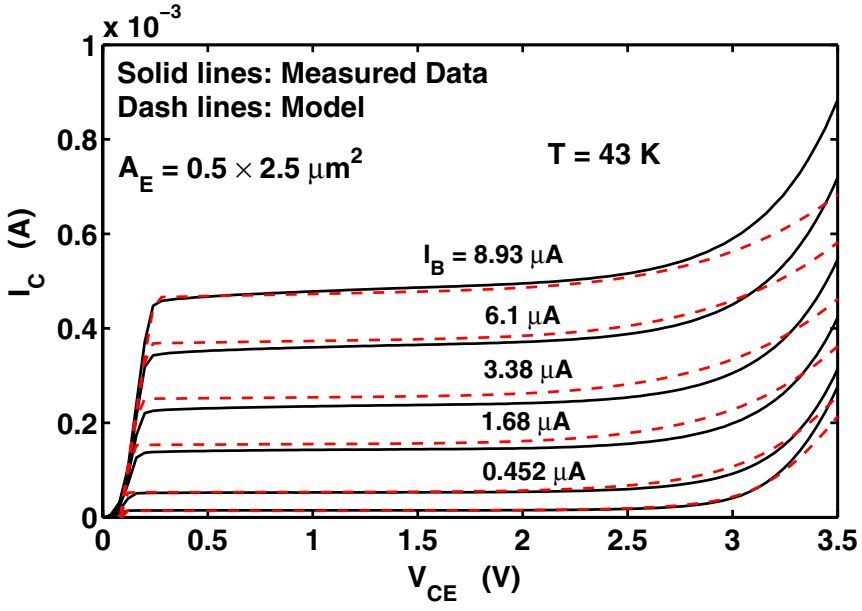


(b)

Figure 6.8: (a) Improved I_C-V_{BE} fitting with new models, and (b) Improved I_B-V_{BE} fitting with new models.



(a)



(b)

Figure 6.9: Improved DC output fitting at (a) 175 K, and (b) 43 K, with new models.

6.4 Summary

This chapter reported the experimental examination of the temperature dependence of key VBIC model parameters for DC current modeling from 300 K to 43 K, and evaluated their temperature mapping models. New model equations were presented and implemented using Verilog-A. An excellent fitting was obtained using a single set of model parameters.

CHAPTER 7

MODELING OF INTERMODULATION LINEARITY IN A 200 GHZ SIGE HBT TECHNOLOGY

Intermodulation linearity is an important figure-of-merit for RF devices, as it relates to the selectivity of a RF receiver and the spectral purity of a RF transmitter. Various theories, simulations, and experimental investigation of linearity have been reported for Si, SiGe and III-V bipolar transistors [27] [28] [29] [30] [31] [32]. Accurate simulation and modeling of linearity is challenging, as it requires accurate descriptions of the higher order derivatives of all the nonlinear current and charge relationships in the device. From a circuit design standpoint, it is desirable to understand how linearity changes as a function of biasing current and voltage, as well as device breakdown voltage, as both biasing point and breakdown voltage are design variables. Another important issue practically is how accurate the compact models are in simulating linearity. Model validation is typically done using DC I-V data and small signal s-parameters, rather than linearity data because of the complexity involved and the time consuming nature of linearity measurements.

The purpose of this work was to evaluate the linearity simulation capability of the VBIC, HICUM and Mextram models in a 200 GHz SiGe HBT technology using harmonic balance. The results provide valuable new insights into the device physics underlying linearity behavior, guidelines to optimal biasing, device selection (e.g. high breakdown versus low breakdown versions), as well as quantified simulations for data

comparison of linearity that will be useful for designers and modelers. The input 3rd order intercept point, IIP3, is used here as a figure-of-merit for intermodulation linearity. IIP3 was measured on the I_C-V_{CE} plane for devices of various size and breakdown voltage [34].

Initially, the models used in this work were examined by comparing the simulated and measured I-V and small signal s-parameters. For the standard breakdown HBT, VBIC, Mextram and HICUM models were used from the design kit developed for the same HBT used in this work. All three of the models produced reasonable fittings for the I-V curves at low current levels. Fig. 7.1 and Fig. 7.2 show comparisons of the measured and VBIC simulated S-parameters vs frequency at V_{CE} = 1.0 V, I_C = 12.8 mA. Clearly, VBIC can model standard breakdown HBT well at low current. The Mextram and HICUM models also produced reasonable fitting of S-parameters at low current. The main difference is the high current behavior for the models. A detailed comparison of the high current I-V and S-parameters as a function of bias shows that for all the models, accuracy degrades at higher I_C (even below peak f_T). Only the VBIC model is available for the high breakdown HBT. ADS, as opposed to Cadence SpectreRF, was used for this part of the research, because of its accuracy and efficiency for IP3 simulation. The Cadence design kit was accessed through the ADS dynamic link in the Cadence tools.

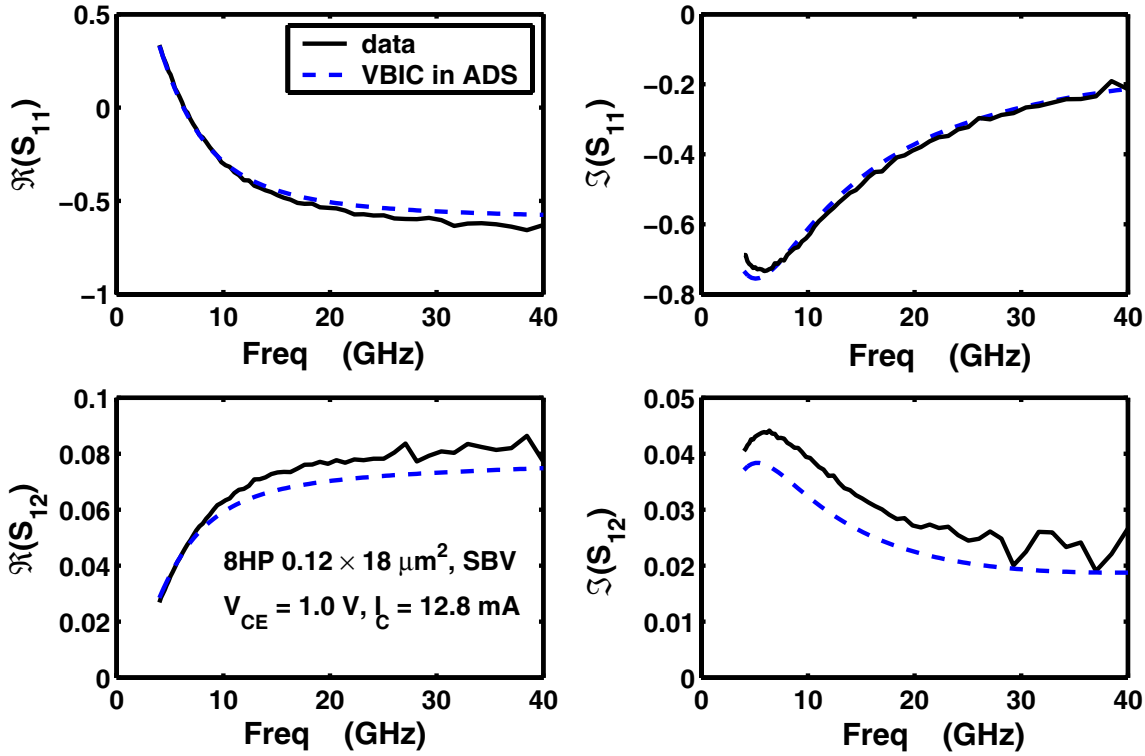


Figure 7.1: Comparison of measured and VBIC simulated S_{11} & S_{12} vs frequency at V_{CE} = 1.0 V, I_C = 12.8 mA. Standard Breakdown HBT.

7.1 Standard Breakdown HBT

Fig. 7.3 (a)-(d) compare the simulated and measured IIP3 as a function of I_C for the standard breakdown HBT. Initially, the V_{CE} = 1.0 V case was examined. All three of the models performed well at I_C < 5 mA. For I_C > 5 mA and I_C < 20 mA, all of the models were off by approximately 2 dB. At V_{CE} = 1.0 and 1.3V, only HICUM was able to model the high current IP3 rolloff and rise behavior (near 30 mA), because of its improved high current region modeling. However, in terms of the IIP3 value

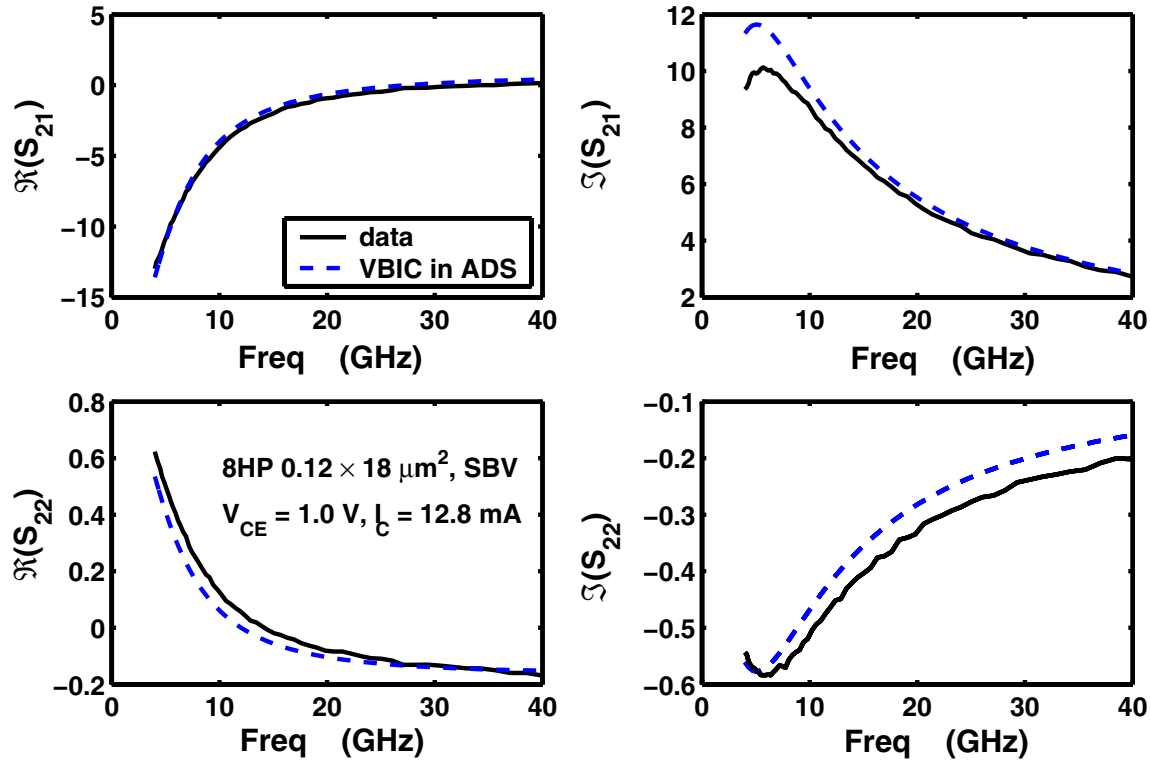


Figure 7.2: Comparison of measured and VBIC simulated S_{21} & S_{22} vs frequency at V_{CE} = 1.0 V, I_C = 12.8 mA. Standard Breakdown HBT.

discrepancy, the VBIC model was the most accurate below 25 mA. Model comparisons at V_{CE} = 1.3 V were similar to those at V_{CE} = 1.0 V. At V_{CE} = 1.6 and 1.9 V, HICUM and Mextram show no clear advantages over VBIC.

7.2 High Breakdown HBT

Moving on to a comparison of the simulated and measured IIP3 for the high breakdown HBT, Fig. 7.4 (a)-(d) compares simulated and measured IIP3 as a function of I_C for V_{CE} = 1.3, 1.9, 2.5 and

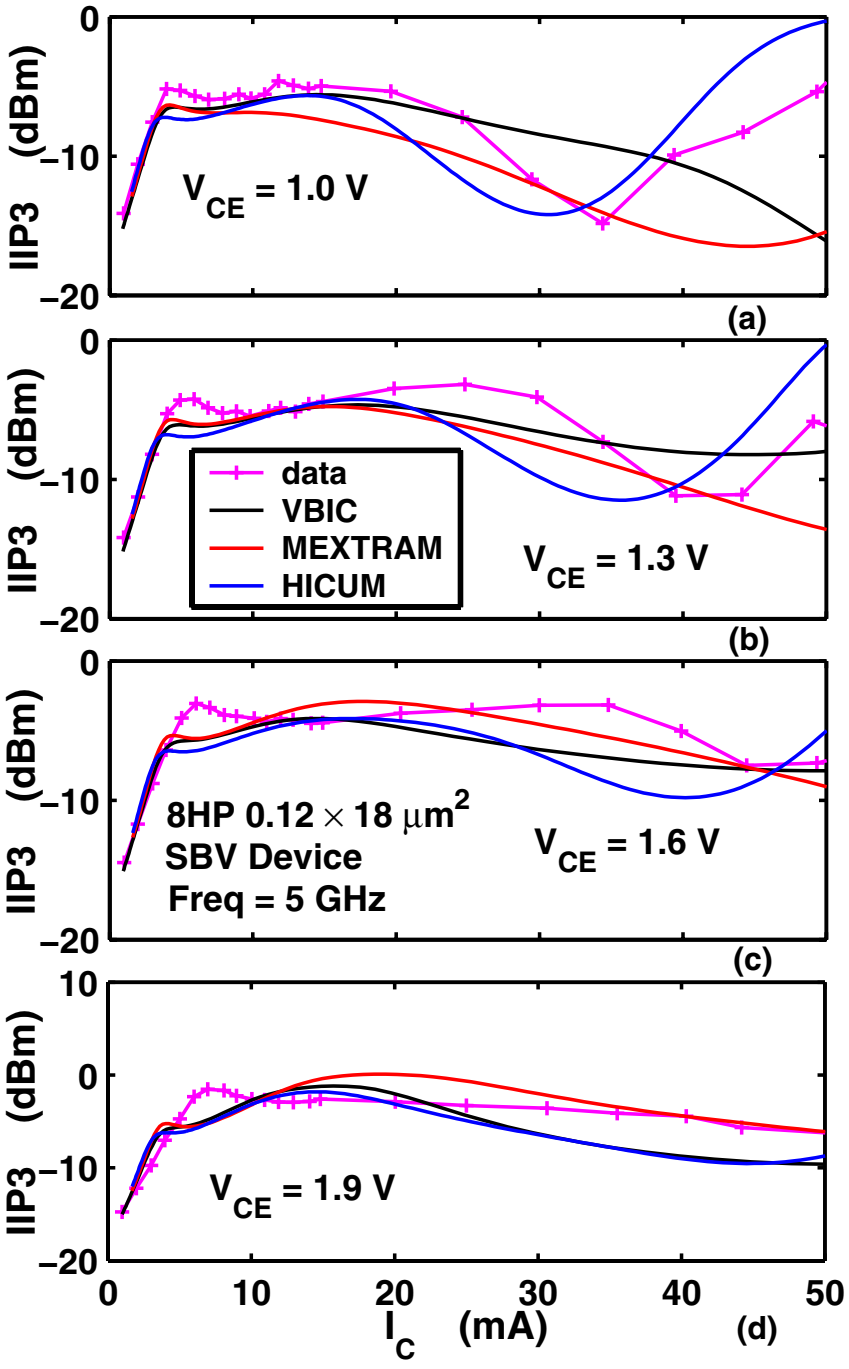


Figure 7.3: Comparison of simulated and measured IIP3 at V_{CE} = 1.0, 1.3, 1.6 and 1.9 V. Standard Breakdown HBT.

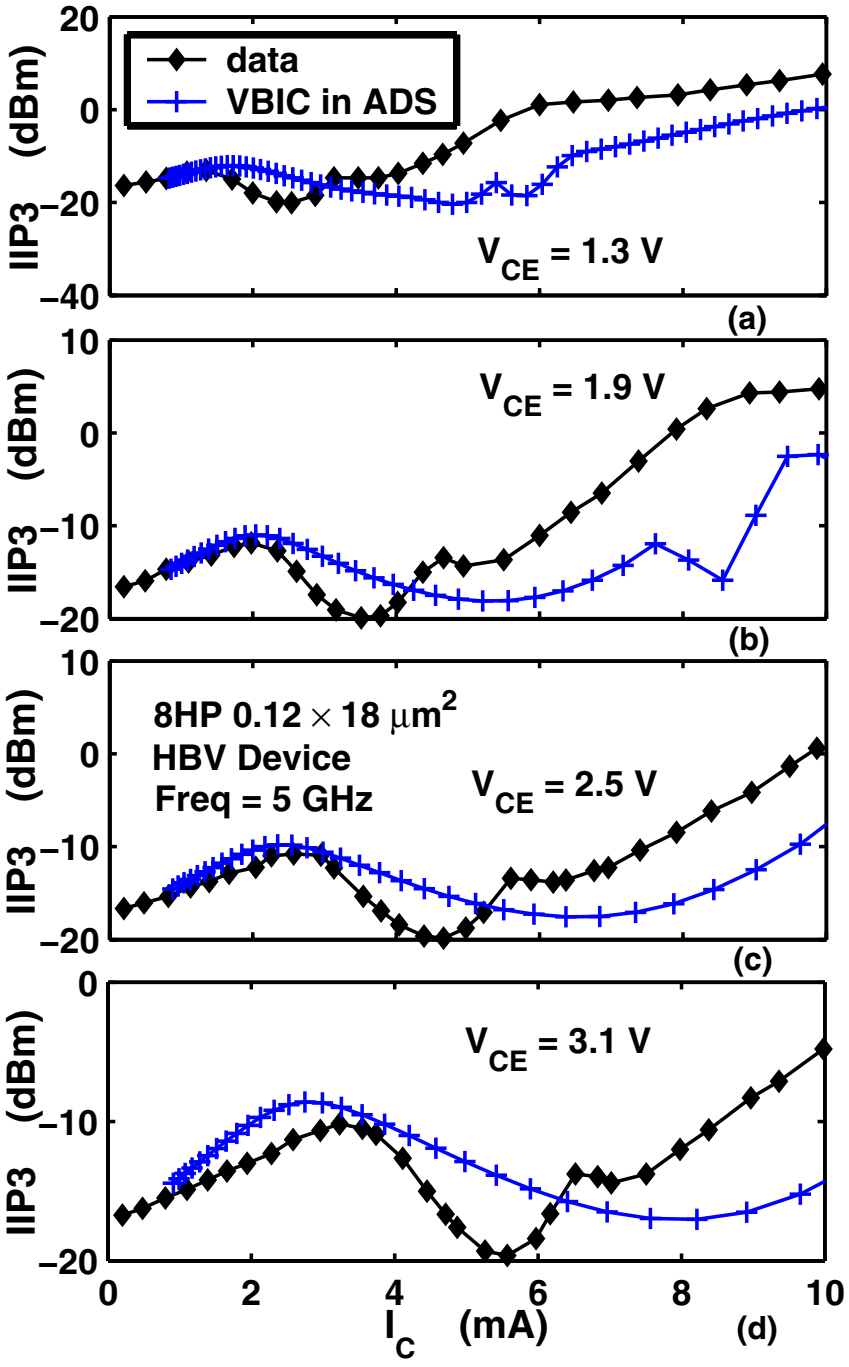


Figure 7.4: Comparison of simulated and measured IIP3 at V_{CE} = 1.3, 1.9, 2.5 and 3.1 V. High Breakdown HBT.

3.1 V, using VBIC, the only model available. The simulation agrees well with the measurement at lower I_C and lower V_{CE} and captures the overall variation of IIP3 with I_C and V_{CE}. Quantitative agreement, however, is not satisfactory at higher I_C or higher V_{CE}.

7.3 Impact of Avalanche and Self-heating

The Volterra series based analysis reported in [29] showed that cancellation of CB capacitance nonlinearity and avalanche nonlinearity can result either in improvement of IIP3, or they can enhance each other to further degrade IIP3. In this simulation, it is possible to turn on and off the avalanche function, as well as self-heating, to examine their impact on IIP3. Initially, the avalanche model was examined by comparing the simulated and measured multiplication factor M-1, as shown in Fig. 7.5. Good multiplication factor M-1 fitting was obtained. Fig. 7.6 compares the IIP3 simulated with various options for the standard breakdown HBT, at V_{CE}=1.9V. The M-1 value in simulation (and measurement) is 0.002 at 5 mA and V_{CE} = 1.9V, which is weak. Below 25 mA, the IIP3 simulated with avalanche is considerably higher, both with and without self-heating. Above 25 mA, the IIP3 simulated without avalanche is higher. In the existing compact models, M-1 is only a function of the internal VCB. Therefore, only the I_C dependence of M-1 due to the ICRC voltage drop is included, while the I_C dependence of avalanche due to charge modulation in the CB junction is not accounted for. This results in an overestimation of M-1 at higher I_C in simulation. Including the decrease of M-1 with increasing I_C brings the high I_C region IIP3 closer to the experimental results in the

high I_C region. Given that a weak avalanche can have a large impact on IIP3, accurate measurement and modeling of the I_C dependence of avalanche are clearly necessary. Self-heating exhibited only a weak effect on IIP3.

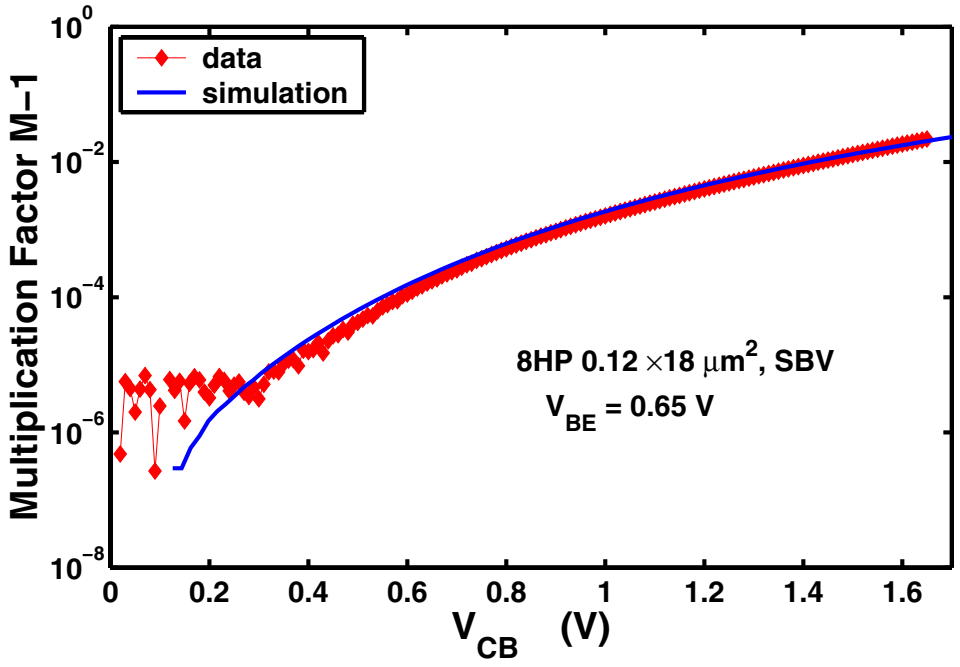


Figure 7.5: Comparison of simulated and measured M-1 at V_{BE} = 0.65 V. Standard Breakdown HBT.

7.4 Summary

This chapter presented the results of VBIC, HICUM, and Mextram simulation of intermodulation linearity in a 200 GHz standard breakdown SiGe HBT device and compared the I_C and V_{CE} dependences of IIP3. At relatively low values of I_C and V_{CE},

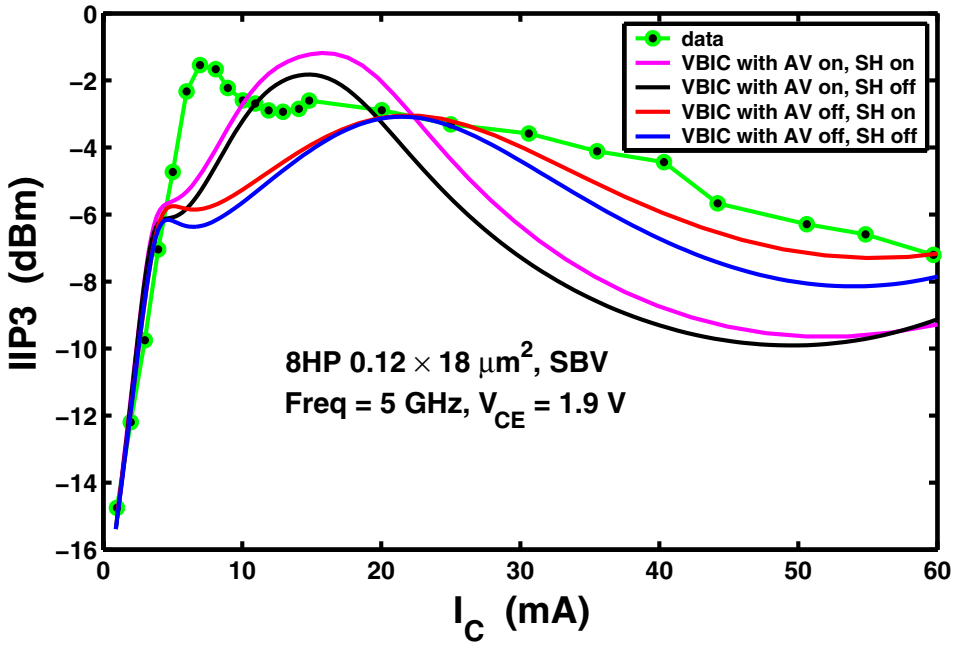


Figure 7.6: Comparison of IIP3 simulated using different combinations of avalanche and self-heating settings and measured IIP3 at $V_{CE} = 1.9$ V. Standard Breakdown HBT.

VBIC, HICUM, and Mextram all yielded reasonably accurate IIP3. However, at relatively higher I_C (still well below peak f_T for standard breakdown HBT) and V_{CE}, significant deviations between simulation and measurement occurred. In some cases, HICUM better captured the trend of IIP3 variation with I_C in the high current region. The effect of avalanche on IIP3 was shown to be significant, while the effect of self-heating on IIP3 was weak.

CHAPTER 8

CONCLUSIONS AND FUTURE WORK

8.1 Conclusions

This research study investigated device physics and compact modeling using a new technique – the Verilog-A based VBIC model, which makes a portable device compact model for the simulator and can be easily modified and implemented into SPICE simulators without the need to construct new interfaces. The internal currents, charges, and noise sources used in SPICE simulators, which are not available in built-in models, became readily accessible using this technique.

Chapter 2 introduced the Verilog-A Language. The principles involved in using Verilog-A based compact modeling instead of low-level simulator code were discussed. An example of Verilog-A based diode modeling was given to provide a better understanding of the Verilog-A language. The device physics behind the VBIC model and the temperature models in VBIC were introduced in Chapter 3. The VBIC model was converted to the Verilog-A language, and implemented into the SPICE simulators Cadence and ADS in Chapter 4. The major problems that arose, such as syntax errors, convergence problems and numerical problems, were addressed and solved. Noise models were added to the Verilog-A based model to be consistent with the Cadence built-in model. The DC, *ac*, noise and large signal simulation comparisons showed identical results for the Verilog-A based VBIC modeling and the Cadence built-in VBIC model.

Based on the new Verilog-A based VBIC model, two applications for SiGe HBTs noise modeling were presented in Chapter 5. First, a new inverse circuit simulation based low frequency noise extraction method was prosed based on the Verilog-A based VBIC model. The low frequency noise of device biasing at high current can be measured more accurately through this method. Second, to better understand the different phase noise upconversion mechanisms of the base current $1/f$ noise and base current short noise in oscillator design, the internal I_{BE} and the internal I_{CE} were separated from the external I_{BE} and the external I_{CE} using Verilog-A based VBIC model. The results showed that the noise generating current I_{BE} made up only a small portion of the terminal I_B.

A group of improved temperature mapping models for modeling DC currents down to 43 K were presented in Chapter 6. The new VBIC based new model was implemented using Verilog-A, compiled into binary code, and dynamically linked to a circuit simulator (ADS) through its compact modeling interface. The detailed coding of the Verilog-A based VBIC model with a group of improved temperature mapping models was documented in Appendix A. Excellent Gummel and output fitting across a wide temperature range from 300 K down to 43 K were achieved for a 50 GHz SiGe HBT device.

The intermodulation linearity simulation capability of the VBIC, HICUM and Mextram models were evaluated using harmonic balance in a 200 GHz SiGe HBT device in Chapter 7. The impact of avalanche and selfheating on IIP3 were examined. The results showed that a weak avalanche has a significant impact on IIP3. The results provided

valuable new insights into the device physics underlying linearity behavior and quantified simulations for data comparisons of linearity that will be useful for designers and modelers.

8.2 Future Work

The Verilog-A based modeling is a very powerful new method that provides useful insights into device characteristics to improve compact modeling. Topics for future investigation include:

1. SiGe HBT noise modeling can be investigated using the Verilog-A based VBIC model. The internal noise sources can be analyzed and the correlation between the internal noise sources can be addressed by the Verilog-A based model. This is potentially very useful, especially for accurate high bias and high frequency noise modeling of the SiGe HBTs desired for RFIC circuit designs.

2. Verilog-A based modeling methods can also be similarly applied to the BSIM model for MOSFET devices.

BIBLIOGRAPHY

[1] J. Rieh, B. Jagannathan, H. Chen, K. Schonenberg, S. Jeng, M. Khater, D. Ahlgren, G. Freeman, and S. Subbanna, "Performance and design considerations for high speed SiGe HBTs of f_T /f_{max}=375 GHz/210 GHz," *Proceeding of IEEE Indium Phosphide and Related Materials Conference*, pp. 374 – 377, 2003.

[2] J.D. Cressler and G. Niu, *Silicon-Germanium Heterojunction Bipolar Transistors*, Artech House, Jan. 2003.

[3] Accellera, *Verilog-AMS Language Reference Manual, version 2.2*.

[4] M. Mierzwinski, P.O. Halloran, B. Troyanovsky, and R. Dutton, "Changing the paradigm for compact model integration in circuit simulators using Verilog-A," *Technical Proceedings of the 2003 Nanotechnology Conference and Trade Show*, pp. 376–379, 2003.

[5] G.J. Coram, "How to (and how not to) write a compact model in Verilog-A," *Proceeding of 2004 IEEE International Behavioral Modeling and Simulation Conference*, pp. 97–106, 2004.

[6] K.S. Kundert and O. Zinke, *The Designer's Guide to Verilog-AMS*, Kluwer Academic Publication, Sept. 2004.

[7] C.C. McAndrew, J.A. Seitchik, D.F. Bowers, M. Dunn, M. Foisy, I. Getreu, M. McSwain, S. Moinian, J. Parker, D.J. Roulston, M. Schroter, P. van Wijnen, and L.F. Wagner, "VBIC95, the vertical bipolar inter-company model," *Workshop on Compact Modeling at the 6th International Conference on Modeling and Simulation of Microsystems*, Oct. 1996.

[8] M. Reisch, *High-Frequency Bipolar Transistors*, Springer, 2003.

[9] *http://www.designer-guide.org*.

[10] *http://www2.fht-esslingen.de/institute/iafgp/neu/VBIC/downloads.html*.

[11] *http://www.silvaco.com*.

[12] Agilent Technologies, *Using Verilog-A in Advanced Design System*.

[13] Cadence, *Cadence Verilog-A Manual*.

[14] C.C. McAndrew, T. Bettinger, L. Lemaitre, and M. Tutt, "BJT modeling with VBIC, basics and v1.3 updates," *Workshop on Compact Modeling at the 6th International Conference on Modeling and Simulation of Microsystems*, pp. 278–281, Feb. 2003.

[15] *Virtuoso Spectre Circuit Simulator Components and Device Models Manual.*

[16] *Nonlinear Devices, ADS Manual*.

[17] *OVI Website, http://www.ovi.org*.

[18] G. Niu, J. Tang, Z. Feng, D.C. Sheridan, and D.L. Harame, "Inverse circuit simulation based low-frequency noise extraction in SiGe HBTs," *IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 221–224, 2004.

[19] G. Niu, J. Tang, Z. Feng, A. Joseph, and D.L. Harame, "SiGe HBT scaling implications on $1/f$ noise and oscillator phase noise," *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 299–302, Dec. 2004.

[20] G. Niu, J. Tang, Z. Feng, A.J. Joseph, and D.L. Harame, "Scaling and technological limitations of $1/f$ noise and oscillator phase noise in SiGe HBTs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, pp. 506–514, Feb. 2005.

[21] J. Cressler, "On the potential of SiGe HBTs for extreme environment electronics," *Proceedings of the IEEE*, vol. 93, pp. 1559–1582, Sept. 2005.

[22] Z. Feng, G. Niu, C. Zhu, L. Najafizadeh, and J.D. Cressler, "Temperature scalable modeling of SiGe HBT DC currents down to 43K," *2006 SiGe and Ge Processing, and Devices Symposium, 210th Electrochemical Society*, Oct. 2006.

[23] H.J. Pan, W.C. Wang, K.B. Thei, C.C. Cheng, K.H. Yu, K.W. Lin, C.Z. Wu, and W.C. Liu, "Investigation of temperature-dependent performances of InP/$In_{0.53}Ga_{0.34}Al_{0.13}As$ heterojunction bipolar transistors," *Semiconductor Science and Technology*, vol. 15, pp. 1101–1106, Dec. 2002.

[24] Z. Feng, G. Niu, C. Zhu, L. Najafizadeh, and J. Cressler, "Impact of nonlinear temperature dependence of bandgap on saturation current modeling," *to be published*.

[25] P. Baureis and D. Seitzer, "Parameter extraction for HBT's temperature dependent large signal equivalent circuit model [MMIC oscillator]," *Technical Digest of 15th Annual Gallium Arsenide Integrated Circuit (GaAs IC) Symposium*, pp. 263–266, Oct. 1993.

[26] C. Anghel, N. Hefyene, R. Gillon, M. Tack, M.J. Declercq, and A.M. Ionescu, "New method for temperature-dependent thermal resistance and capacitance accurate extraction in high-voltage DMOS transistors," *Technical Digest of IEEE International Electron Devices Meeting*, pp. 133–136, Dec. 2003.

[27] J. Reynolds, "Nonlinear distortions and their cancellation in transistors," *IEEE Transactions on Electron Devices*, vol. 12, pp. 595–599, Nov. 1965.

[28] S.A. Maas, B.L. Nelson, and D.L. Tait, "Intermodulation in heterojunction bipolar transistors," *IEEE Transactions on Microwave Theory and Techniques*, vol. 40, pp. 442–448, Mar. 1992.

[29] G. Niu, Q. Liang, J.D. Cressler, C.S. Webster, and D.L. Harame, "Rf linearity characteristics of SiGe HBTs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, pp. 1558–1565, Sept. 2001.

[30] M.P. van der Heijden, H.C. de Graaff, and L.C.N. de Vreede, "A novel frequency-independent third-order intermodulation distortion cancellation technique for BJT amplifiers," *IEEE Journal of Solid State Circuits*, vol. 37, pp. 1176–1183, Sept. 2002.

[31] M. Iwamoto, P.M. Asbeck, T.S. Low, C.P. Hutchinson, J.B. Scott, A. Cognata, Xiaohui Qin, L.H. Camnitz, and D.C. D'Avanzo, "Linearity characteristics of GaAs HBTs and the influence of collector design," *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, pp. 2377–2388, Dec. 2000.

[32] M. Iwamoto, C.P. Hutchinson, J.B. Scott, T.S. Low, M. Vaidyanathan, P.M. Asbeck, and D.C. D'Avanzo, "Optimum bias conditions for linear broad-band InGaP/GaAs HBT power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, pp. 2954–2962, Dec. 2002.

[33] S.J. Jeng, B. Jagannathan, J.S. Rieh, J. Johnson, K.T. Schonenberg, D. Greenberg, A. Stricker, H. Chen, M. Khater, D. Ahlgren, G. Freeman, K. Stein, and S. Subbanna, "A 210-GHz f_T SiGe HBT with a non-self-aligned structure," *IEEE Electron Device Letters*, vol. 22, no. 11, pp. 542–544, Nov. 2001.

[34] G. Niu, Y. Li, Z. Feng, J. Pan, and D.C. Sheridan, "Characterization and modeling of intermodulation linearity in a 200 GHz SiGe HBT technology," *IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, Oct. 2006.

APPENDIX A

VERILOG-A CODE WITH KEY IMPROVED TEMPERATURE MAPPING MODELS

A.1 Improved N_F and N_{EI} Temperature Mapping Models

According to (6.6) in Chapter 6, the improved temperature model for N_F and N_{EI} in Verilog-A based model is as follows.

```
NFatT = NF*(1.0+dT*Tnf+Anf*(pow(rT, Xnf)-1));

NEIatT = NEI*(1.0+dT*Tnei+Anei*(pow(rT, Xnei)-1));
```

Table A.1 lists the value of the parameters in the improved models.

Parameter	Value	Parameter	Value
NF	1.00072	NEI	1.0001
Tnf	-0.00018	Tnei	-0.00005
Anf	0.0012	Anei	0.0012
Xnf	-2.94	Xnei	-2.89

Table A.1: Parameters used for improved N_F and N_{EI} temperature mapping models.

A.2 Improved $E_{a,true}$, I_S and I_{BEI} Temperature Mapping Models

According to (6.27) and (6.29) in Chapter 6, the improved temperature model for $E_{a,true}$ and I_S in Verilog-A based model is as follows.

```
EAatT = EA+EAalpha*pow(EAbeta,2)*pow(Tini,2)*(rT-1)
        /(pow((EAbeta+Tini),2)*(EAbeta+Tdev));
EAIEatT = EAIE+EAIEalpha*pow(EAIEbeta,2)*pow(Tini,2)*(rT-1)
          /(pow((EAIEbeta+Tini),2)*(EAIEbeta+Tdev));
ISatT = IS*pow((pow(rT,XIS)*
        limexp(-EAatT*(1.0-rT)/Vtv)),(1.0/NFatT));
IBEIatT = IBEI*pow((pow(rT,XII)*
          limexp(-EAIEatT*(1.0-rT)/Vtv)),(1.0/NEIatT));
```

Table A.2 lists the value of the parameters in the improved models.

Parameter	Value	Parameter	Value
IS	1.62694e-18	IBEI	1.09629e-20
XIS	1.78	XII	1.78
EA	1.13	EAIE	1.145
EAalpha	2	EAIEalpha	2.7
EAbeta	1.326	EAIEbeta	1.21

Table A.2: Parameters used for improved $E_{a,true}$, I_S and I_{BEI} temperature mapping models.

A.3 Improved I_{KF} Temperature Mapping Model

According to (6.30) in Chapter 6, the improved temperature model for I_{KF} in Verilog-A based model is as follows.

```
IKFatT = IKF*(1.0-dT*Tikf+Aikf*(pow(rT, Xikf)-1));
```

Table A.3 lists the value of the parameters in the improved models.

Parameter	Value
IKF	0.00382
Tikf	0.00141
Aikf	2.64
Xikf	0.355

Table A.3: Parameters used for improved I_{KF} temperature mapping model.