VIBRATION ANALYSIS OF TEST CHIPS WITH INTEGRATED PIEZORESISTIVE

STRESS SENSORS

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VIBRATION ANALYSIS OF TEST CHIPS WITH INTEGRATED PIEZORESISTIVE STRESS SENSORS

Kapil Gore

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THESIS ABSTRACT

VIBRATION ANALYSIS OF TEST CHIPS WITH INTEGRATED PIEZORESISTIVE STRESS SENSORS

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Vibration analysis of the WB200 test chip containing an array of optimized piezoresistive stress sensor rosettes has been performed. The test chip was attached to the printed circuit board with an underfill encapsulant used as an adhesive. Different underfill dispense patterns were studied and the best suited pattern was selected for die attachment. Cross-sections of the chip-on-board assembly were made and observed to record the thickness values.

Values of junction capacitances in the test chip were measured, calculated and used in SPICE simulations to obtain the electrical cut-off frequency of the stress sensors. A shaker system was then used to vibrate the chip-on-board assembly over a range of frequencies to study the response curves of the stress sensors. Static bending experiments of the assembly were performed, and the results were compared with the finite element analysis predictions obtained from ANSYS^{TM}.

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Style manual of journal used Graduate School: Guide to preparation and submission of theses and dissertations

Computer software used Microsoft Office XP

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Chapter 1

INTRODUCTION

Vibration is an oscillating motion where some structure or body moves back and forth. If the motion repeats itself, with all of the individual characteristics after a certain period of time, it is called periodic motion. Simple harmonic motion is the simplest form of periodic motion, and is usually represented by a continuous sine wave on a plot of displacement versus time.

A vibrating system requires some coordinates to describe the positions of the elements in the system. If there is only one element in the system that is restricted to move along only one axis, and only one dimension is required to locate the position of the element at any instant of time with respect to some initial starting point, then it is a single degree of freedom system. A two degree of freedom system requires two coordinates to describe the positions of the elements.

A standard manner in which a particular system can vibrate is known as a vibration mode. Each vibration mode is associated with a particular natural frequency and represents a degree of freedom. A single degree of freedom system will have only one vibration mode and only one resonant frequency. A simply supported beam can have an infinite number of degrees of freedom and thus can have an infinite number of vibration

modes. The fundamental resonant mode of a vibrating system is usually called the natural frequency or the resonant frequency of the system. Sometimes it is called the first harmonic mode of the system which often has the greatest displacement amplitudes and usually the greatest stresses. The second harmonic mode usually has a smaller displacement than the first harmonic mode, so the stresses are smaller. The displacements continue to decrease for the higher resonant modes.

Electronic equipment can be subjected to many different forms of vibration over a wide range of frequencies and acceleration levels. It can be said that all electronic equipment will be subjected to some type of vibration at some time in its life. If the vibration is not due to an active association with some sort of a machine or a moving vehicle, then it may be due to transporting the equipment from the manufacturer to the customer. Vibration is usually considered to be an undesirable condition and can produce many different types of failures in electronic equipment.

Mechanical vibrations can have many different sources. In vehicles such as automobiles, trucks and trains most of the vibration is due to the rough surfaces over which these vehicles travel. In ships and submarines the vibration is due to the engines and to buffeting by the water. In airplanes, missiles and rockets the vibration is due to jet and rocket engines and to aerodynamic buffeting.

Portable electronic devices such as pagers, palm-top organizers and compactly designed cell phones are vulnerable to damage from mechanical shock and vibration. With a drop from the desk or an inadvertent bump against a wall, closely assembled components can collide rendering the device inoperable. Over a period of time, the post-shock ringing vibration can fatigue boards and connectors, creating hard to spot electrical

problems. Integrated circuit chips in these devices can also be affected by the resulting stresses due to such vibrations, especially at high frequencies. Therefore, the testing of these devices should include vibration analysis of its circuit board and the integrated circuit chips on the board.

1.1 Piezoresistive Stress Sensor Chips

Thermal and mechanical loadings often produce stresses in integrated circuit chips incorporated in electronic packages. Stresses occur due to non-uniform thermal expansions of the packaging material and the semiconductor die. These stresses can cause mechanical failures of the integrated circuit chip such as fracture of the die, solder fatigue, die bond failure, encapsulant cracking or parametric shifts of devices. Parametric shifts can affect the failure of both analog and digital devices, and it has been shown that characterization of die stresses can be done with piezoresistive stress sensors.

Piezoresistive effect is caused by the change of resistivity of semiconductors as a function of applied stresses. Smith [1] first proposed to use the piezoresistive behavior of semiconductors for stress and strain measurements. Since then, Tufte and Stezer [2] and Suhling, et al. [3-4] have investigated the temperature dependence of piezoresistive coefficients of silicon or germanium. Kanda [5] represented the piezoresistive coefficients graphically and Yamada, et al. [6] addressed the nonlinearity of the piezoresistive effect. Bittle, et al. [7] derived the detailed theory for silicon piezoresistive sensors.

Piezoresistive sensors are a powerful tool for experimental structural analysis of electronic packages. Figure 1.1 illustrates the basic application concept. The sensors are resistors that are conveniently fabricated into the surface of the die using current microelectronic technology, and are capable of providing non-intrusive measurements of surface stress state on a chip even with encapsulated packages. If the piezoresistive sensors are calibrated over a wide temperature range, thermally induced stresses can be measured. A full field mapping of the stress distribution over the surface of a die can be obtained using specially designed test chips, which incorporate an array of sensor rosettes.

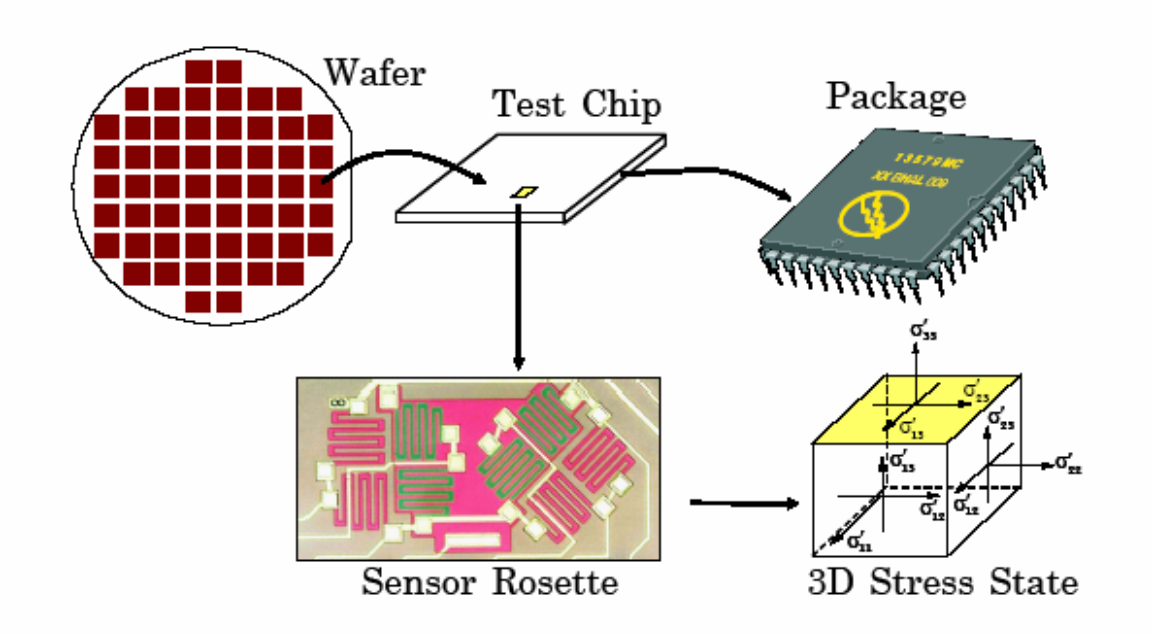


Figure 1.1 Piezoresistive Sensor Concept

Several investigators, namely Edwards, et al. [8-11] and Groothuis, et al. [12], have used stress test chips based on piezoresistive sensors to examine die stress in plastic

encapsulated packages. Miura, et al. [13-18] have used test chips incorporating four element dual polarity rosettes to characterize thermally induced die stresses in dual-in-line packages. Stresses developed on the silicon surface due to die attachment, and encapsulation and molding processes have also been discussed in several publications [19-26]. Measurement of die stresses in flip chip on laminate assemblies was performed by Rahim, et al. [27-29], in which the authors have investigated the mechanical stresses present on the back side and the device side of the die at each stage of the flip chip assembly process. Several other researchers have studied the effect of thermo mechanical properties of underfill and underfill technology on flip chip packages reliability [30-35].

Theoretical analyses by Suhling and co-workers [7, 36-40] have established that properly designed sensor rosettes on the (111) silicon wafer plane have several advantages relative to sensors fabricated using standard (100) silicon. Optimized rosettes on (111) silicon can be used to measure the complete state of stress (six stress components) at a point on the top surface of the die, and offer the unique capability of measuring four temperature compensated combined stress components.

Stress test chips need to be calibrated to obtain the piezoresistive coefficients required for the stress calculation. A four-point bending calibration procedure is typically used. Details of this method are discussed by Beaty, et al. [41-42], Suhling, et al. [43-45], and Jaeger, et al. [46-48]. An analysis of the errors associated with the design and calibration of stress sensors in (100) silicon has been made by Jaeger, et al. [46-48].

Although, extensive research has been done in various aspects of the piezoresistive stress sensor chips, as can be seen in the above mentioned references, their vibration analysis has not been fully performed yet. The work done in this thesis focuses

mainly on the frequency response of the stress sensor chips subjected to beam bending and vibrations.

1.2 Thesis Contribution and Content Organization

The WB200 piezoresistive stress sensor test chip has been used to perform vibration analysis. The test chip was attached to a specially designed printed circuit board with the help of perimeter wire bonds and underfill encapsulant used as an adhesive. Different patterns of underfill dispense were studied and the best suited pattern was selected for die attachment. A scanning acoustic microscope was used to measure the underfill thickness, whose value would be used in finite element analysis of the chip-on-board assembly.

Values of junction capacitances in the test chip were measured on a LCR meter and were verified using theoretical formulae. These capacitance values and the p-type and n-type resistor values were used to perform SPICE simulations of the RC network to obtain its electrical cut-off frequency.

The chip-on-board assembly was mounted on a shaker system where static bending experiments were performed and the results were compared with the finite element analysis results obtained from ANSYS^{TM}. Static bending of the assembly was also performed on a simple cantilever beam holder to verify the results from the shaker system. Lastly, the shaker system was used to vibrate the chip-on-beam assembly over a range of frequencies and at different chip offsets to obtain the frequency response curves of the stress sensors.

The contents of this thesis are divided into six chapters. Chapter One is designed to introduce the basics of vibration and piezoresistive stress sensor chips along with a brief overview of the work that has been done to investigate the different aspects of these sensor chips. Chapter Two will explain the piezoresistive theory and the WB200 test chip. The chip-on-board assembly will be discussed in Chapter Three along with the underfill dispense and thickness measurement. Chapter Four will deal with the capacitance measurements and calculations, and finding the electrical cut-off frequency using SPICE simulations. The shaker system will be described in Chapter Five along with the various static and dynamic experiments performed. It also includes comparison of the results with those obtained from finite element analysis of the chip-on-board assembly in ANSYS^{TM}. Finally, a conclusion of the thesis will be presented in Chapter Six.

Chapter 2

REVIEW OF PIEZORESISTIVE THEORY AND WB200 TEST CHIP

2.1 General Resistance Change Equations

An arbitrarily oriented silicon filamentary conductor is shown in Fig. 2.1. The unprimed axes x_1 = [100], x_2 = [010], and x_3 = [001] are the principal crystallographic directions of the cubic silicon crystal.

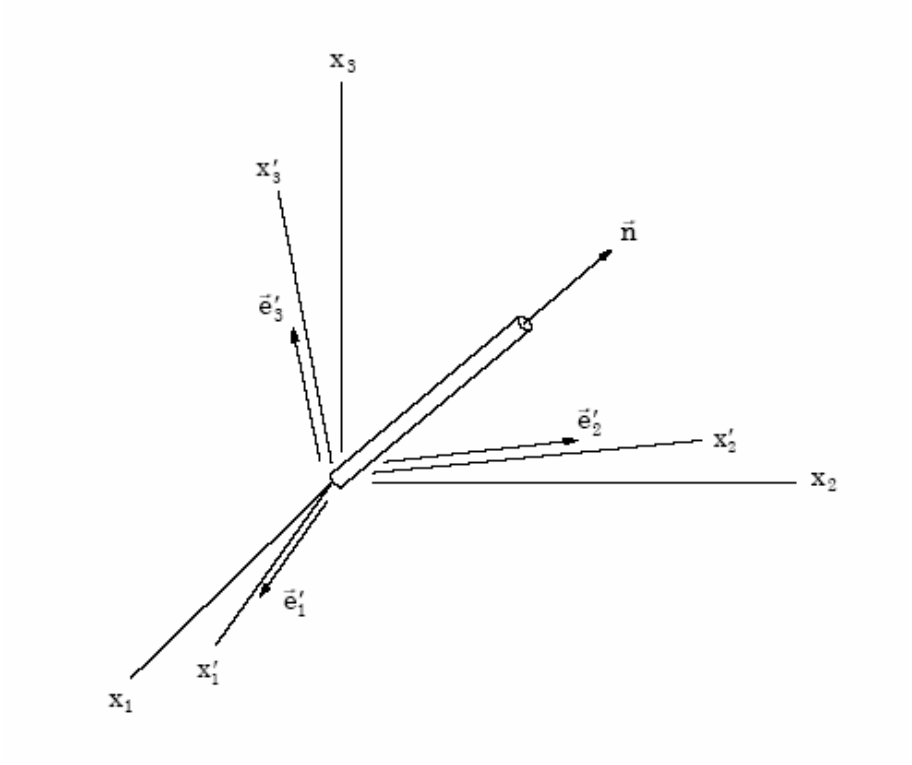


Figure 2.1 Filamentary Silicon Conductor

The primed coordinate system is arbitrarily rotated with respect to the unprimed crystallographic system. For this conductor, the normalized change in resistance can be expressed in terms of the off-axis stress components using [7]

$$\frac{\Delta R}{R} = \left(\pi'_{1\alpha}\sigma'_{\alpha}\right)l'^{2} + \left(\pi'_{2\alpha}\sigma'_{\alpha}\right)m'^{2} + \left(\pi'_{3\alpha}\sigma'_{\alpha}\right)n'^{2} + 2\left(\pi'_{4\alpha}\sigma'_{\alpha}\right)l'n' + 2\left(\pi'_{5\alpha}\sigma'_{\alpha}\right)m'n' + 2\left(\pi'_{6\alpha}\sigma'_{\alpha}\right)l'm' + \left[\alpha_1 T + \alpha_2 T^2 + \ldots\right] \tag{2.1}$$

where $\pi'_{\alpha\beta}\left(\alpha,\beta = 1,2,...,6\right)$ are the off-axis temperature dependent piezoresistive coefficients, $\alpha_1, \alpha_2, ...$ are the temperature coefficients of resistance, $T = T_m - T_{ref}$ is the difference between the measurement temperature and reference temperature, and l', m', n' are the direction cosines of the conductor orientation with respect to the x'_1, x'_2, x'_3 axes respectively. In Eq. (2.1) and future indicial notation expressions, the summation convention is implied for repeated indices, and reduced index notation has been used for the stress components:

$$\sigma'_1 = \sigma'_{11}\ , \quad \sigma'_2 = \sigma'_{22}\ , \quad \sigma'_3 = \sigma'_{33} \tag{2.2}$$

$$\sigma'_4 = \sigma'_{13}\ , \quad \sigma'_5 = \sigma'_{23}\ , \quad \sigma'_6 = \sigma'_{12}$$

The 36 off-axis piezoresistive coefficients in Eq. (2.1) are related to the three unique on-axis piezoresistive coefficients $\pi_{11}, \pi_{12}, \pi_{44}$ (evaluated in the unprimed coordinate system aligned with the crystallographic axes) using the transformation [7]

$$\pi'_{\alpha\beta} = T_{\alpha\gamma}\pi_{\gamma\delta}T_{\delta\beta}^{-1} \tag{2.3}$$

where

$$\left[\pi_{\alpha\beta}\right] = \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{bmatrix} \tag{2.4}$$

is the on-axis piezoresistive coefficient matrix, and $\left[T_{\alpha\beta}\right]$ is the 6 x 6 transformation matrix whose elements are related to the direction cosines of the primed coordinate directions with respect to the unprimed coordinate directions. When the primed axes are aligned with the unprimed axes, this transformation matrix reduces to a 6 x 6 identity matrix. Thus, Eq. (2.3) reduces to

$$\pi'_{\alpha\beta} = \pi_{\alpha\beta} \tag{2.5}$$

and Eq. (2.1) simplifies to

$$\begin{aligned} \frac{\Delta R}{R} = {} & \left[\pi_{11}\sigma_{11} + \pi_{12}\left(\sigma_{22} + \sigma_{33}\right)\right] l^2 + \left[\pi_{11}\sigma_{22} + \pi_{12}\left(\sigma_{11} + \sigma_{33}\right)\right] m^2 \\ & + \left[\pi_{11}\sigma_{33} + \pi_{12}\left(\sigma_{11} + \sigma_{22}\right)\right] n^2 + 2\pi_{44}\left[\sigma_{12} lm + \sigma_{13} nl + \sigma_{23} mn\right] \\ & + \left[\alpha_1 T + \alpha_2 T^2 + \ldots\right] \end{aligned} \tag{2.6}$$

where *l, m, n* are the direction cosines on the conductor orientation with respect to the unprimed crystallographic axes. Equation (2.6) demonstrates that the resistance change of an arbitrarily oriented silicon resistor depends on all six stress components.

2.2 Resistance Change Equations for Silicon Wafer Planes

For a given wafer orientation, Eq. (2.1) can be used to obtain the resistance change equation for an arbitrarily oriented in-plane resistor. In the current microelectronics industry, it is most common for silicon devices to be fabricated using (100) silicon wafers. A general (100) silicon wafer is shown in Fig. 2.2. The surface of the wafer is a (100) plane, and the [001] direction is normal to the wafer plane.

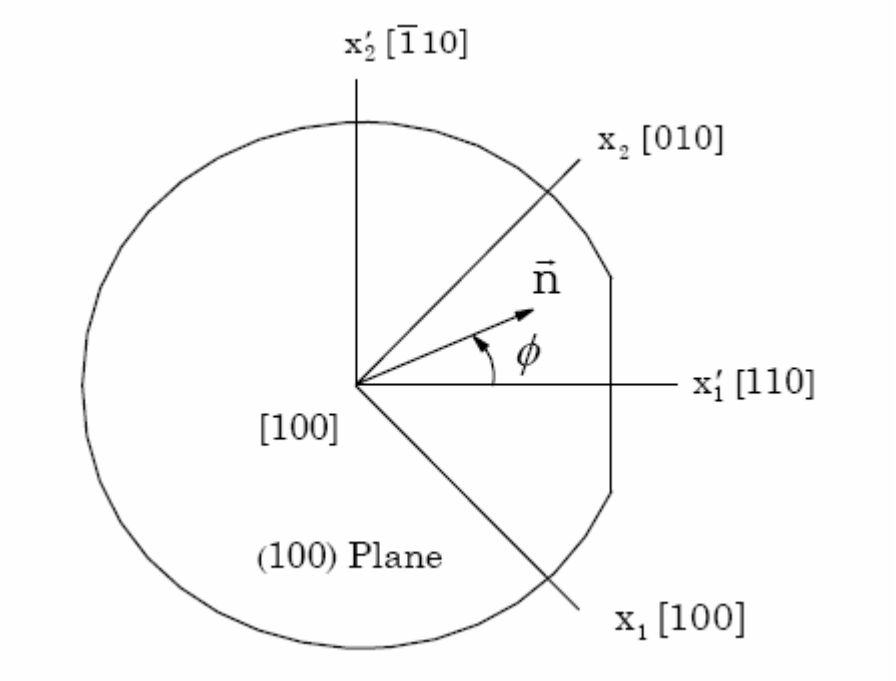


Figure 2.2 (100) Silicon Wafer

Calculation of the off-axis piezoresistive coefficients and substitution into Eq. (2.1) yields

$$\frac{\Delta R}{R} = \left[\left(\frac{\pi_{11}+\pi_{12}+\pi_{44}}{2}\right)\sigma'_{11} + \left(\frac{\pi_{11}+\pi_{12}-\pi_{44}}{2}\right)\sigma'_{22}\right]\cos^2\phi$$
$$+\left[\left(\frac{\pi_{11}+\pi_{12}-\pi_{44}}{2}\right)\sigma'_{11} + \left(\frac{\pi_{11}+\pi_{12}+\pi_{44}}{2}\right)\sigma'_{22}\right]\sin^2\phi \qquad (2.7)$$
$$+\pi_{12}\sigma'_{33} + (\pi_{11}-\pi_{12})\sigma'_{12}\sin 2\phi + \left[\alpha_1 T + \alpha_2 T^2 + \ldots\right]$$

where

$$l' = \cos\phi \qquad m' = \sin\phi \qquad n' = 0 \qquad (2.8)$$

has been introduced, and ϕ is the angle between the x'_1-axis and the resistor orientation. Eq. (2.7) indicates that the out-of-plane shear stresses σ'_{13} and σ'_{23} do not influence the resistances of stress sensors fabricated on (100) wafers. This means that a sensor rosette on (100) silicon can at best measure four of the six unique stress components.

The other common silicon crystal orientation used in semiconductor fabrication is the (111) surface. A general (111) silicon wafer is shown in Fig. 2.3. The surface of the wafer is a (111) plane, and the [111] direction is normal to the wafer plane. The principal crystallographic axes x_1 = [100], x_2 = [010], and x_3 = [001] do not lie in the wafer plane and have not been indicated. It is convenient to work in an off-axis primed wafer coordinate system where the axes x'_1 and x'_2 are parallel and perpendicular to the primary wafer flat.

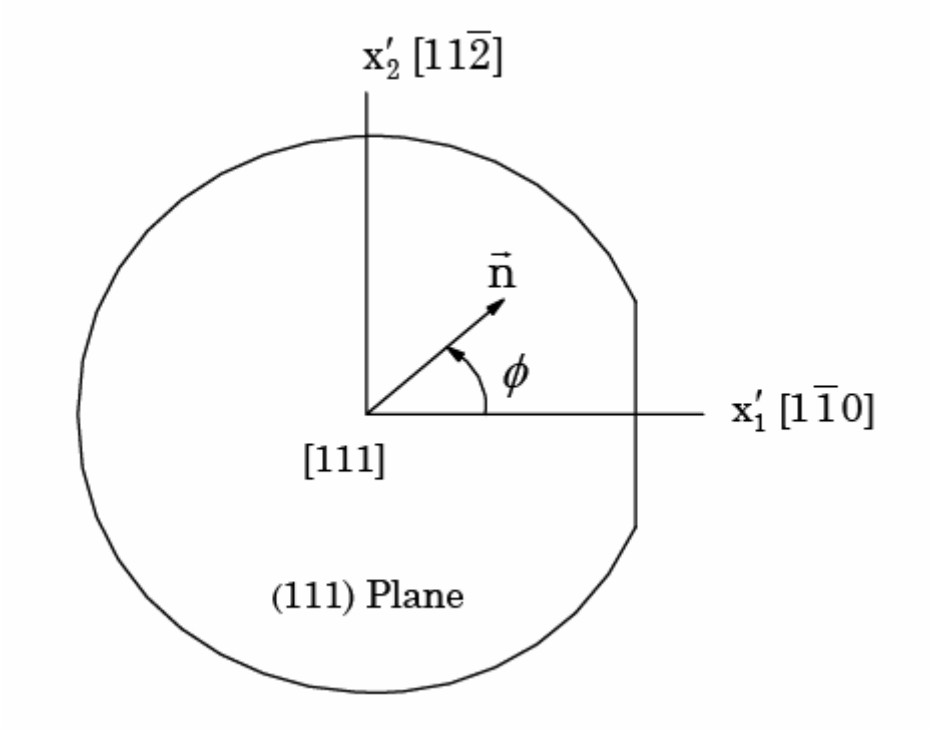


Figure 2.3 (111) Silicon Wafer

Using Eq. (2.1), the resistance change of an arbitrarily oriented in-plane sensor can be expressed in terms of the stress components resolved in this natural wafer coordinate system. For the primed coordinate system indicated in Fig. 2.3, the appropriate direction cosines for the primed axes are

$$[a_{ij}] = \begin{bmatrix} \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} & 0 \\ \frac{1}{\sqrt{6}} & \frac{1}{\sqrt{6}} & -\frac{2}{\sqrt{6}} \\ \frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} \end{bmatrix} \tag{2.9}$$

Substitution of the off-axis piezoresistive coefficients into Eq. (2.1) yields

$$\frac{\Delta R}{R} = \left[B_1\sigma'_{11} + B_2\sigma'_{22} + B_3\sigma'_{33} + 2\sqrt{2}\left(B_3 - B_2\right)\sigma'_{23}\right]\cos^2\phi$$
$$+ \left[B_2\sigma'_{11} + B_1\sigma'_{22} + B_3\sigma'_{33} - 2\sqrt{2}\left(B_3 - B_2\right)\sigma'_{23}\right]\sin^2\phi \qquad (2.10)$$
$$+ \left[2\sqrt{2}\left(B_3 - B_2\right)\sigma'_{13} + \left(B_1 - B_2\right)\sigma'_{12}\right]\sin 2\phi + \left[\alpha_1 T + \alpha_2 T^2 + \ldots\right]$$

where ϕ is the angle between the x'_1-axis and the resistor orientation. The coefficients

$$B_1 = \frac{\pi_{11} + \pi_{12} + \pi_{44}}{2}$$
$$B_2 = \frac{\pi_{11} + 5\pi_{12} - \pi_{44}}{6} \qquad (2.11)$$
$$B_3 = \frac{\pi_{11} + 2\pi_{12} - \pi_{44}}{3}$$

are a set of linearly independent temperature dependent piezoresistive parameters. These parameters must be calibrated before stress component values can be extracted from resistance change measurements. Equation (2.10) indicates that the resistance change for a resistor in the (111) plane is dependent on all six of the unique stress components. Therefore, the potential exists for developing a sensor rosette that can measure the complete three-dimensional state of stress at points on the surface of a die.

Besides the ability to measure two additional stress components, theoretical analysis has established that properly designed sensor rosettes on the (111) silicon wafer plane have other advantages relative to sensors fabricated using standard (100) silicon. In particular, optimized sensors on (111) silicon are capable of measuring four temperature compensated combined stress components, while those on (100) silicon can only be used to measure two temperature compensated quantities.

2.3 Eight Element Rosette

It has been theoretically proved that when considering all possible resistor orientations at a point, there are only three unique responses on any given silicon plane. Therefore, it is not possible to design a p-type or n-type rosette that can measure more than three stress components. However, dual polarity sensing elements fabricated on both n-type and p-type silicon can measure all six stress components. Thus, a six-element rosette having three n-type and three p-type resistors can measure the complete stress state at a point on the silicon surface. However, including two extra resistors allows for more convenient bridge measurements of the resistance changes and better stress measurement localization.

Layout of the half-bridge circuits with four n-type and four p-type resistors is shown in Fig. 2.4. The rosette is interconnected as half-bridge circuits to reduce the number of pads needed to completely access all sensors.

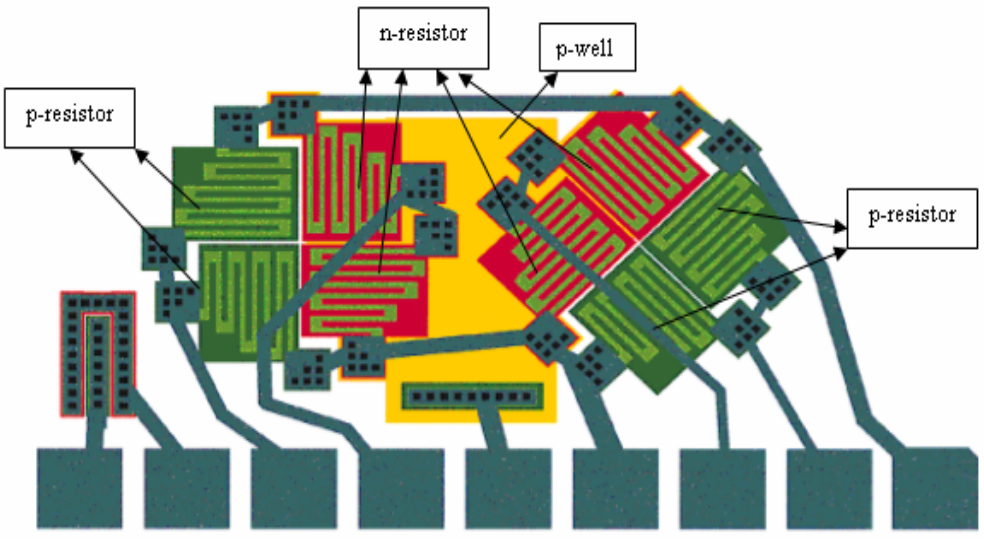


Figure 2.4 Rosette Layout

Careful layout of the eight-element rosette design maximizes the matching and minimizes sensitivity to mask misalignment during fabrication. The (111) silicon eight-element dual polarity rosette in Fig. 2.5 has been developed at Auburn University.

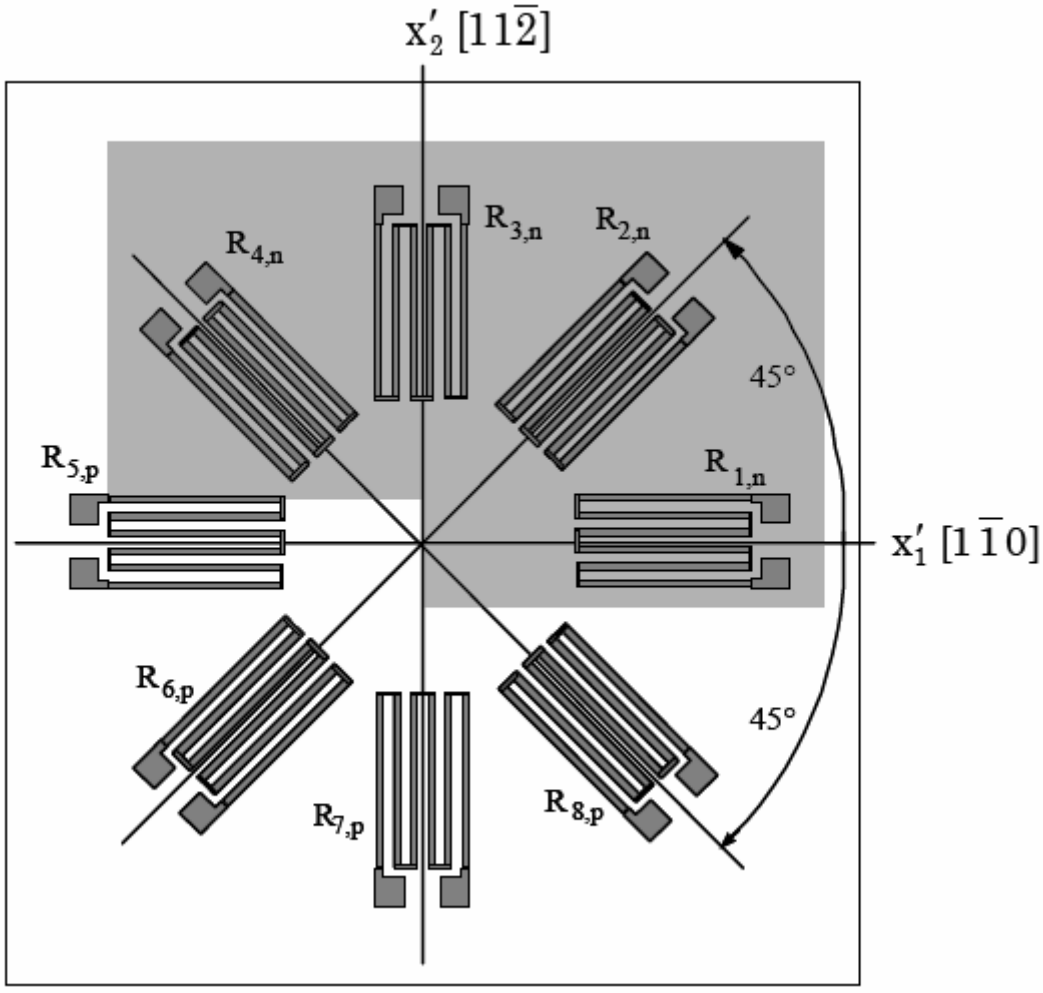


Figure 2.5 Optimized Eight Element Rosette

The rosette in Fig. 2.5 contains p-type and n-type sensor sets, each with resistor elements making angles of $\phi = 0°, \pm 45°, 90°$ with respect to the x_1'-axis. Repeated

application of Eq. (2.10) to each of the piezoresistive sensing elements leads to the following expressions for the stress-induced resistance changes

$$\frac{\Delta R_1}{R_1} = B_1^n \sigma'_{11} + B_2^n \sigma'_{22} + B_3^n \sigma'_{33} + 2\sqrt{2}\left(B_3^n - B_2^n\right)\sigma'_{23} + \left[\alpha_1^n T + \alpha_2^n T^2 + \ldots\right]$$

$$\frac{\Delta R_2}{R_2} = \left(\frac{B_1^n + B_2^n}{2}\right)\left(\sigma'_{11} + \sigma'_{22}\right) + B_3^n \sigma'_{33} + 2\sqrt{2}\left(B_3^n - B_2^n\right)\sigma'_{13} + \left(B_1^n - B_2^n\right)\sigma'_{12} + \left[\alpha_1^n T + \alpha_2^n T^2 + \ldots\right]$$

$$\frac{\Delta R_3}{R_3} = B_2^n \sigma'_{11} + B_1^n \sigma'_{22} + B_3^n \sigma'_{33} - 2\sqrt{2}\left(B_3^n - B_2^n\right)\sigma'_{23} + \left[\alpha_1^n T + \alpha_2^n T^2 + \ldots\right]$$

$$\frac{\Delta R_4}{R_4} = \left(\frac{B_1^n + B_2^n}{2}\right)\left(\sigma'_{11} + \sigma'_{22}\right) + B_3^n \sigma'_{33} - 2\sqrt{2}\left(B_3^n - B_2^n\right)\sigma'_{13} - \left(B_1^n - B_2^n\right)\sigma'_{12} + \left[\alpha_1^n T + \alpha_2^n T^2 + \ldots\right]$$

(2.12)

$$\frac{\Delta R_5}{R_5} = B_1^p \sigma'_{11} + B_2^p \sigma'_{22} + B_3^p \sigma'_{33} + 2\sqrt{2}\left(B_3^p - B_2^p\right)\sigma'_{23} + \left[\alpha_1^p T + \alpha_2^p T^2 + \ldots\right]$$

$$\frac{\Delta R_6}{R_6} = \left(\frac{B_1^p + B_2^p}{2}\right)\left(\sigma'_{11} + \sigma'_{22}\right) + B_3^p \sigma'_{33} + 2\sqrt{2}\left(B_3^p - B_2^p\right)\sigma'_{13} + \left(B_1^p - B_2^p\right)\sigma'_{12} + \left[\alpha_1^p T + \alpha_2^p T^2 + \ldots\right]$$

$$\frac{\Delta R_7}{R_7} = B_2^p \sigma'_{11} + B_1^p \sigma'_{22} + B_3^p \sigma'_{33} - 2\sqrt{2}\left(B_3^p - B_2^p\right)\sigma'_{23} + \left[\alpha_1^p T + \alpha_2^p T^2 + \ldots\right]$$

$$\frac{\Delta R_8}{R_8} = \left(\frac{B_1^p + B_2^p}{2}\right)\left(\sigma'_{11} + \sigma'_{22}\right) + B_3^p \sigma'_{33} - 2\sqrt{2}\left(B_3^p - B_2^p\right)\sigma'_{13} - \left(B_1^p - B_2^p\right)\sigma'_{12} + \left[\alpha_1^p T + \alpha_2^p T^2 + \ldots\right]$$

Superscripts n and p are used on the combined piezoresistive coefficients to denote n-type and p-type resistors respectively.

For an arbitrary state of stress, these expressions can be inverted to solve for the six stress components in terms of the measured resistance changes

$$\sigma'_{11} = \frac{\left(B_3^p - B_2^p\right)\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right] - \left(B_3^n - B_2^n\right)\left[\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right]}{2\left[\left(B_2^p - B_1^p\right)B_3^n + \left(B_1^p - B_3^p\right)B_2^n + \left(B_3^p - B_2^p\right)B_1^n\right]}$$
$$+ \frac{B_3^p\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^n T\right] - B_3^n\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^p T\right]}{2\left[\left(B_1^n + B_2^n\right)B_3^p - \left(B_1^p + B_2^p\right)B_3^n\right]}$$

$$\sigma'_{22} = -\frac{\left(B_3^p - B_2^p\right)\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right] - \left(B_3^n - B_2^n\right)\left[\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right]}{2\left[\left(B_2^p - B_1^p\right)B_3^n + \left(B_1^p - B_3^p\right)B_2^n + \left(B_3^p - B_2^p\right)B_1^n\right]}$$
$$+ \frac{B_3^p\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^n T\right] - B_3^n\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^p T\right]}{2\left[\left(B_1^n + B_2^n\right)B_3^p - \left(B_1^p + B_2^p\right)B_3^n\right]}$$

$$\sigma'_{33} = \frac{-\left(B_1^p + B_2^p\right)\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^n T\right] + \left(B_1^n + B_2^n\right)\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^p T\right]}{2\left[\left(B_1^n + B_2^n\right)B_3^p - \left(B_1^p + B_2^p\right)B_3^n\right]}$$

$$\sigma'_{13} = \frac{\sqrt{2}}{8}\left[\frac{\left(B_1^p - B_2^p\right)\left[\frac{\Delta R_4}{R_4} - \frac{\Delta R_2}{R_2}\right] - \left(B_1^n - B_2^n\right)\left[\frac{\Delta R_8}{R_8} - \frac{\Delta R_6}{R_6}\right]}{\left(B_2^p - B_1^p\right)B_3^n + \left(B_1^p - B_3^p\right)B_2^n + \left(B_3^p - B_2^p\right)B_1^n}\right]$$

$$\sigma'_{23} = \frac{\sqrt{2}}{8}\left[\frac{-\left(B_1^p - B_2^p\right)\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right] + \left(B_1^n - B_2^n\right)\left[\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right]}{\left(B_2^p - B_1^p\right)B_3^n + \left(B_1^p - B_3^p\right)B_2^n + \left(B_3^p - B_2^p\right)B_1^n}\right]$$

$$\sigma'_{12} = \frac{-\left(B_3^p - B_2^p\right)\left[\frac{\Delta R_4}{R_4} - \frac{\Delta R_2}{R_2}\right] + \left(B_3^n - B_2^n\right)\left[\frac{\Delta R_8}{R_8} - \frac{\Delta R_6}{R_6}\right]}{2\left[\left(B_2^p - B_1^p\right)B_3^n + \left(B_1^p - B_3^p\right)B_2^n + \left(B_3^p - B_2^p\right)B_1^n\right]} \tag{2.13}$$

From the expressions in Eq. (2.13), it is clear that the extraction of the three shear stresses $\sigma'_{12}, \sigma'_{13}, \sigma'_{23}$ from the measured resistance changes is temperature compensated. Evaluation of the normal stress components requires measurement of the normalized resistance changes of the sensors and the temperature change T experienced by the sensing elements. The expressions also indicate that a calibration procedure must be performed to determine all six of the combined piezoresistive parameters $B_1^n, B_2^n, B_3^n, B_1^p, B_2^p, B_3^p$ prior to using the sensor rosette. A combination of uniaxial and hydrostatic pressure testing can be utilized to complete this task.

2.4 WB 200 Test Chip

The WB 200 wire bondable chip used in this study is shown in Fig. 2.6. The 5 mm x 5 mm chip is fabricated on a (111) silicon wafer and contains sixteen eight-element rosettes for stress mapping and diodes for temperature measurement. Each rosette contains four p-type and four n-type resistors as described in the previous section. Every rosette is independently accessible through outer or inner pads.

Cross section of the test chip is shown in Fig. 2.7. The starting wafer is a lightly doped p-type substrate of 25 mil thickness. A heavily doped n-type buried layer is formed and used as a buried heater. Above the buried layer, a moderately doped n-type epitaxial layer is grown into which moderately doped p-type layers are diffused to form the p-type resistors. Similarly diffused p-layer forms p-well inside the epitaxial layer. N-resistors are

formed by n^+ diffused layers inside the p-well. These resistors are diffused in a serpentine pattern to occupy smaller area. Heavy doping of the n^+ diffused layers results in n-type

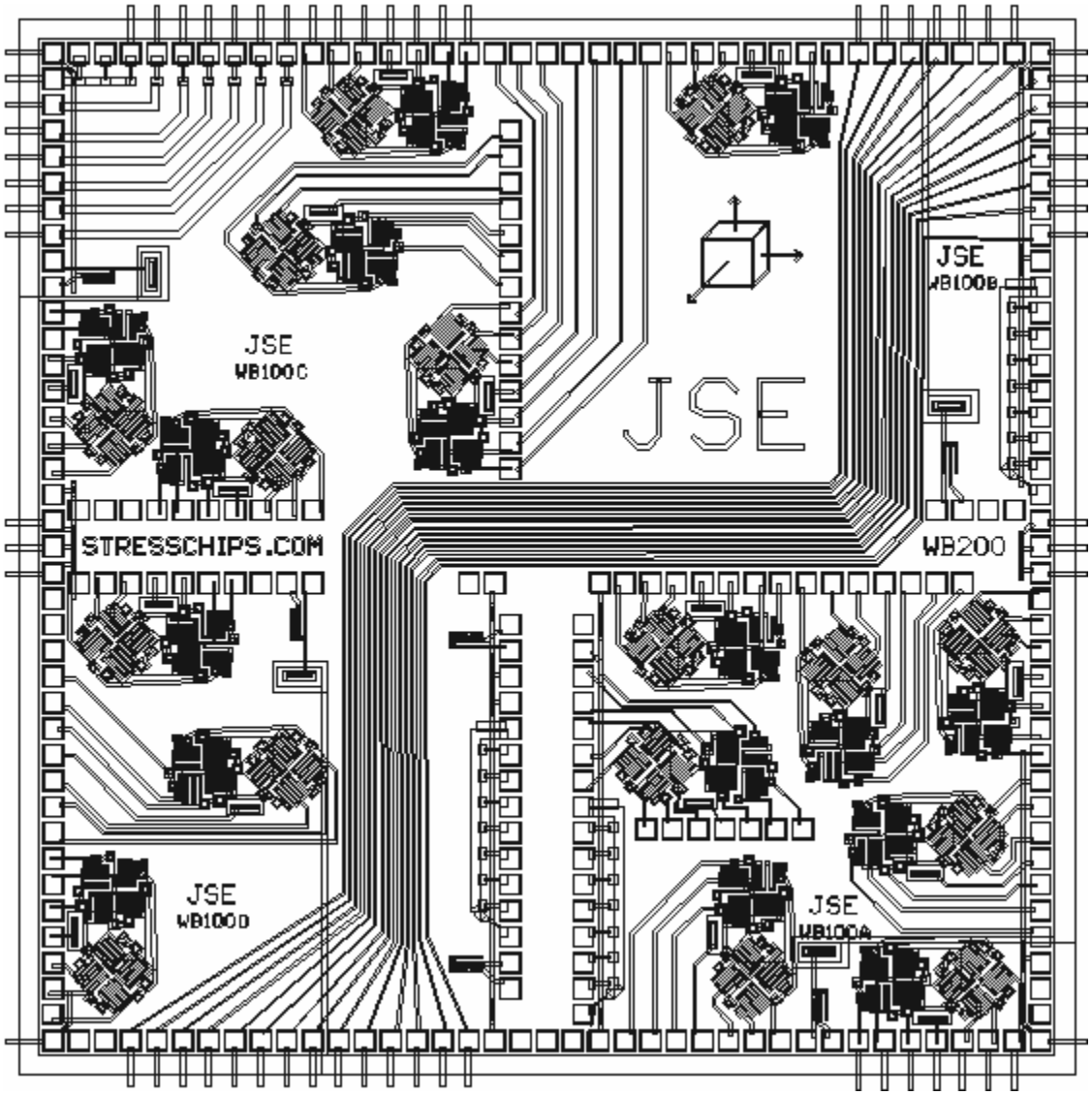


Figure 2.6 WB 200 Test Chip

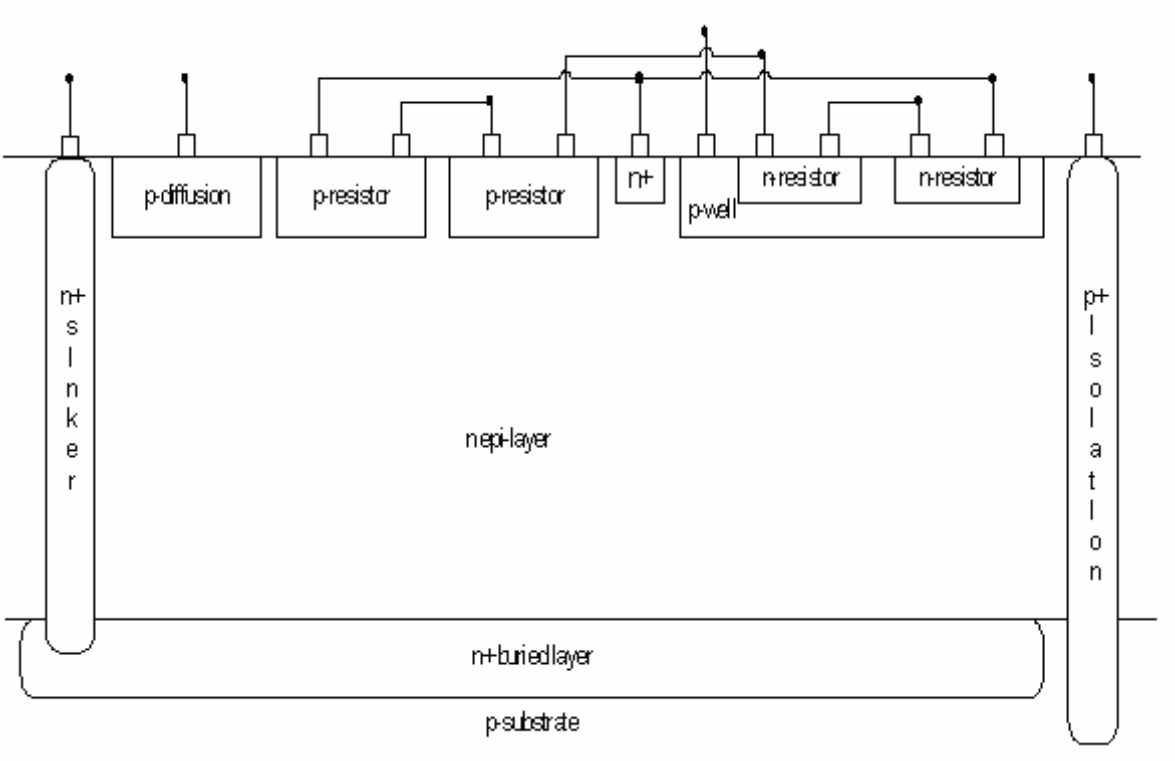


Figure 2.7 Cross Section of WB 200 Test Chip

resistors having a value of approximately 2.2 $k\Omega$, while the more lightly doped p-diffusion layer yields p-type resistors of about 10.5 $k\Omega$. The fabrication process uses ion implantation to achieve the best possible resistor matching and uniformity. Highly doped p-type diffusion connected to the substrate can act as an isolation ring. Lastly, highly doped n-type diffusion can act as contact to both n-type resistors and the n-epi layer.

Chapter 3

TEST CHIP ON BOARD ASSEMBLY

3.1 FR-4 Board Properties

A printed circuit board has been designed to facilitate wire bonding of the test chip. FR-4 material is the predominant material used for printed circuit boards due to its low cost and sufficiently large glass transition temperature (T_g) for most applications and hence has been chosen for our boards. FR-404, which is a standard multilayer material, is a multifunctional epoxy system with a T_g of 150° C and dielectric constant of 4.6. However, FR-406 which is a tetrafunctional epoxy system with a higher T_g of 170° C and lower dielectric constant of 4.3 is used for making our boards. Its higher glass transition temperature minimizes out-of-plane expansion and potential for pad lifting in high temperature applications.

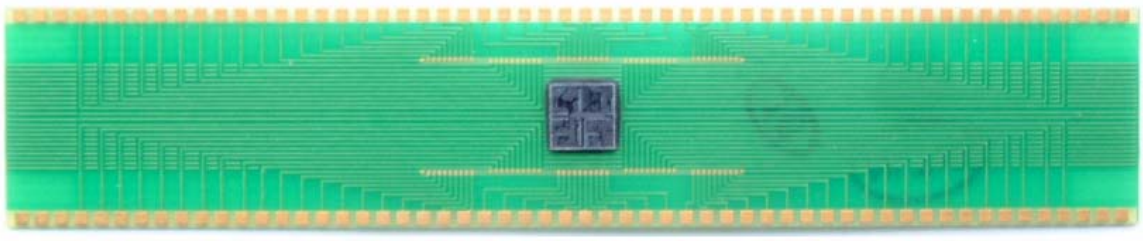


Figure 3.1 Chip on Board

Figure 3.1 shows the test chip attached to the board with the help of underfill encapsulant used as an adhesive. The dimensions of the test chip are 200×200 mils while that of the board are 3400×650 mils. The solder line thickness on the board is 7 mils. Gold wires were used to wire bond the chip to the wire bonding pads on the board. These wire bonding pads are 8×8 mils and the spacing between any two of them is 8 mils. External wires were soldered to the board using the soldering pads which are 40×40 mils and the spacing between any two of them is 20 mils.

3.2 Underfill Dispense Pattern

The underfill material used as the die attachment adhesive for the chip-on-board assembly in this work was Thermoset ME-525. It is a one component, fast cure, semiconductor grade epoxy and has excellent thermo-mechanical properties including a low coefficient of thermal expansion. It also has good moisture resistance which reduces moisture-induced failures. It is a low viscosity system that flows rapidly under devices with stand-offs down to $25\,\mu m$. In contrast to older underfill systems, this encapsulant does not require a two step curing to minimize stress and can be quickly cured in 30 minutes at 150° C.

The CAM/ALOT System 3700 shown in Fig. 3.2 was used for dispensing underfill on the boards. In order to obtain the optimal quantity and pattern of underfill on the board, various combinations of the machine parameters were tried. Different values for amount of underfill dispense from the needle per unit time, speed of dispense needle, and height of dispense needle from the board surface were used. Also, three patterns of

underfill dispense were studied – one big dot in the center, one dot in the center and four dots near the four corners, and a criss-cross diagonal pattern. All these combinations were tried using glass die for underfill visibility and practice boards.

Figure 3.2 CAM/ALOT System 3700

One dot in the center and four dots near the four corners was the pattern that gave the best results and hence was selected along with the following parameters:

Height of Dispense = 0.6 inches

Shotsize = 750 msec for center dot and 225 msec for corner dots

Pump speed = 250 revolutions per minute

Shift height up = 0.3 inches

On delay = 150 msec

The Pick-and-Place System shown in Fig. 3.3 was used to place the die over the underfill on the board with a constant force. Different values of the force were tried, and it was concluded that the smallest possible force gave the best results. Finally, the samples were placed in an oven for 30 minutes at 150° C to cure the underfill.

The C-Mode Scanning Acoustic Microscope (C-SAM) shown in Fig. 3.4 is an ultra high frequency pulse-echo ultrasonic imaging system that is used to look inside optically opaque samples and view internal features such as voids and delamination. C-SAM images of the samples were taken to observe the underfill uniformity after curing.

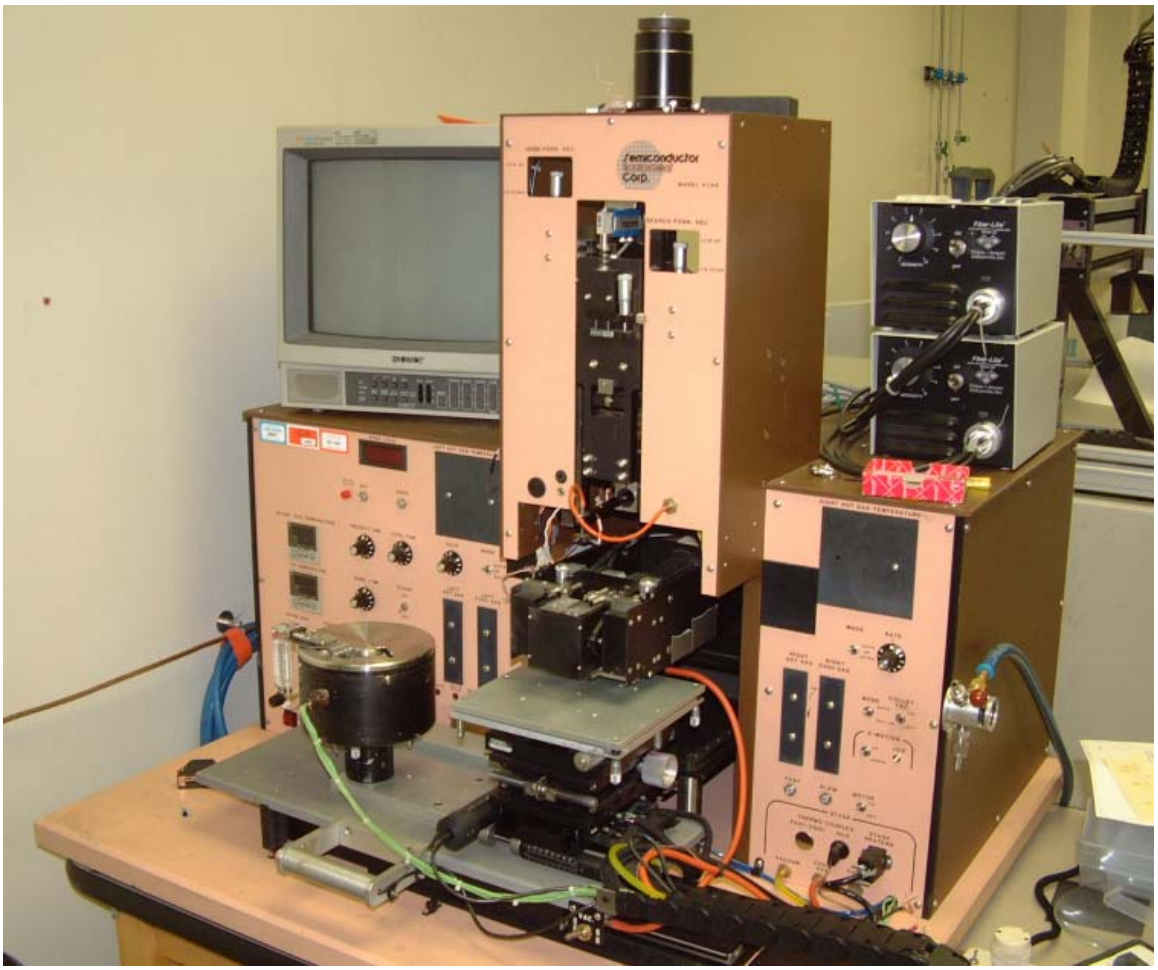


Figure 3.3 Pick-and –Place System

Figure 3.4 C-SAM System

The C-SAM images revealed the presence of numerous voids (white regions) in the cured samples as can be seen in Fig. 3.5. In order to avoid voids in the underfill layer, the boards were kept for dehydration in an oven at 125°C for 45 minutes prior to dispensing the underfill layer on them. As can be seen in Fig. 3.6, dehydrated boards gave improved uniformity of the underfill layer eliminating the voids. The grayscale variation in Fig. 3.6 is due to the copper trace patterns in the circuit board beneath the die.

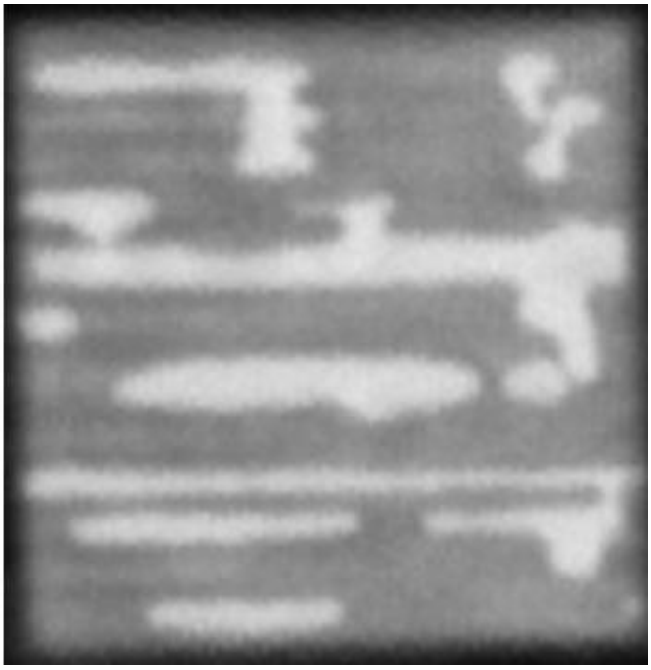


Figure 3.5 C-SAM Image showing voids in underfill layer

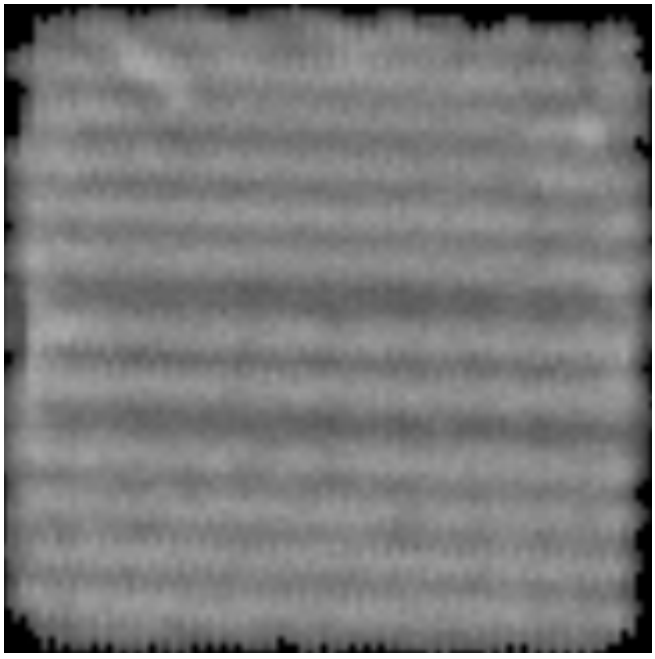


Figure 3.6 C-SAM Image showing no voids in underfill layer

3.3 Underfill Thickness Measurement

In order to measure the thickness of underfill layer, cross-sections of the chip-on-board samples had to be made and observed under a high power microscopy system shown in Fig. 3.7 consisting of Nikon Measurement Microscope MM-11 and Quadra-Check 2000 position controller. An Isomet 1000 wet saw was used to cut the samples. A solution containing 1 part of coolant with 9 parts of water was used to cover the bottom of the saw. The samples were cut with a cutting speed of 200 rpm. The cut samples were placed in an epoxy resin and left for hardening in plastic holders.

Silicone release agent was liberally applied to the inside of the plastic holders and was left to dry before reapplying. Sampl-Klip I clips were put on the cut samples and were placed in the holders, with the area of interest on bottom side of the holder. Next, 100 parts of epoxy resin was mixed with 50 parts of hardener and was scooped with a tongue depressor until the mixture turned colorless, which is an indication of complete mixing of the resin and hardener. This mixture was poured on the samples in plastic holders until the mixture completely covered the samples, and was kept for 24 hours at room temperature to allow hardening of the mixture after which the hardened samples can be pushed out of the plastic holders.

Polishing of these samples was done in three parts. In the first part, the samples were polished using two types of grits of paper sequentially. Group 1 corresponds to 120, 240, 320 and 400 grits and group 2 corresponds to 600, 800 and 1200 grits. Group 1 type papers were used to remove the bulk of the material until the cross-section of the chip-on-board sample was first seen. Then, Group 2 papers were used to fine tune the cross-section and reduce the appearance of scratches. The surface polisher used was a Buehler

Figure 3.7 Microscope System for Thickness Measurement

Ecomet 6. The appropriate grit of paper was placed on the wheel and its main water valve was turned on. Once the paper was secured on it, the wheel was turned on at a speed of 150 rpm. With moderate pressure, the sample was placed on the spinning wheel and moved back and forth for 3 to 5 seconds. The sample was then lifted up, rotated by $90°$, and placed back on the spinning wheel. Progress was checked by washing the sample with water and observing under the microscope. These steps were carried out for second type of paper grit and finally the samples were dried using compressed air.

The second part of polishing was done using 3 micron alumina diamond paste. The grinding wheel on polisher was replaced by the polishing wheel and dots of diamond paste were placed on top of the polishing wheel. Extender was sprayed on the wheel and the sample was swabbed in the mixture. The wheel was turned on to a speed of 150 rpm and the sample was placed with moderate pressure on the spinning wheel. The sample was moved back and forth for 3 to 5 seconds and then lifted up, rotated by $90°$, and placed back on the spinning wheel. Progress was checked after every 2^{nd} rotation of the sample by cleaning the sample and observing under the microscope. The scratches began to fade and the image had become sharper. After satisfactory progress was made, the samples were washed with water and then dried with compressed air.

The third and last part of polishing was done using Buehler Masterprep, which is a water based 0.05 micron alumina polishing solution. The wheel was rotated at a speed of 100 rpm and steps similar to the previous polishing parts were followed while adding a couple of drops of the Masterprep solution on the spinning wheel after every couple of seconds. Progress was observed under the microscope and polishing was continued until the scratches in the sample disappeared.

Figure 3.8 shows the final polished samples that were used to record the thickness values of the three components. The thickness of the FR-4 board was measured to be 0.583 mm, while that of the test chip was 0.650 mm. Finally, the thickness of the underfill material was found to be consistent in all samples and was recorded to be 0.029 mm.

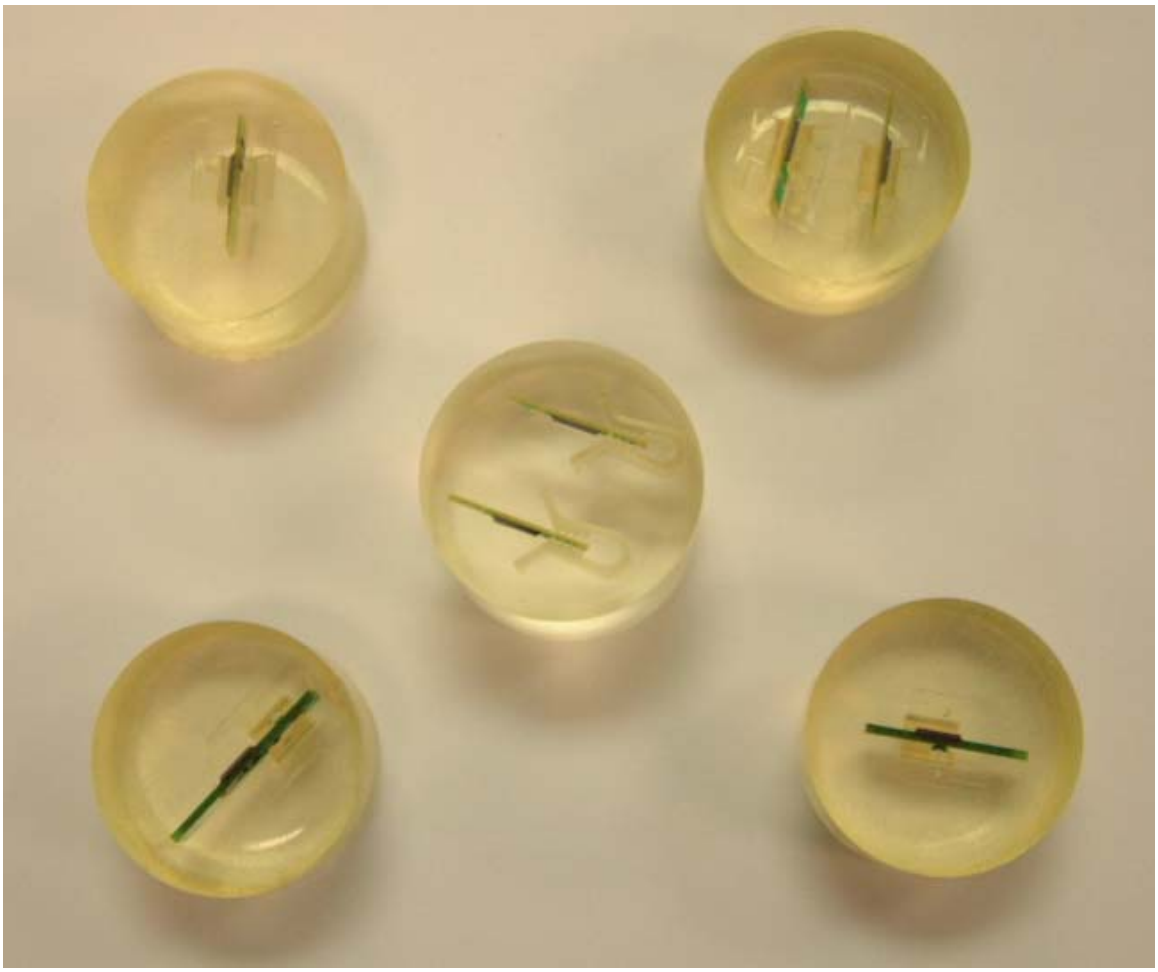


Figure 3.8 Polished Samples for Thickness Measurement

Chapter 4

CAPACITIVE EFFECT

Any variation of charge within a p-n diode with an applied voltage variation yields a capacitance. The capacitance associated with the charge variation in the depletion region is called the junction capacitance, while the capacitance associated with the excess carriers in the quasi-neutral region is called the diffusion capacitance. The total capacitance is the sum of both junction and diffusion capacitance. The junction capacitance dominates for reverse-biased diodes, while the diffusion capacitance dominates in strongly forward-biased diodes. The diodes in our test chip are reverse-biased under normal operating conditions, and hence only junction capacitances will be discussed in this topic.

The junction capacitances in the test chip form a RC network with the piezoresistances, which defines the electrical cut-off frequency of the stress sensors. In this chapter, values of these junction capacitances will be calculated using mathematical expressions and will be verified with its values measured on a LCR meter. These values will then be used to simulate the RC network and obtain its electrical cut-off frequency.

4.1 Capacitance Values from Theory

The cross section of WB200 test chip is shown in Fig. 2.7. Spreading resistance profiles through various sections of the chip indicate that the background doping of the n^+ epi-layer and the p-substrate were 1.3 x 10^{15} /cm^3. The p-well and p-diffusion for the diode ring were doped at 2 x 10^{18} /cm^3. The peak value of doping of the n^+ buried layer was found to be 5 x 10^{18} /cm^3, while that of the p^+ isolation ring was 3 x 10^{19} /cm^3. Peak values of n-resistor doping and n^+ contacts were found to be 2.5 x 10^{19} /cm^3. These values will be used to calculate two types of junction capacitances in the test chip, namely, p-resistor to n epi-layer capacitance and n-resistor to p-well capacitance.

4.1.1 p-resistor to n-epi Capacitance

The built-in potential is given by

$$\phi_{bi} = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{4.1}$$

where, $n_i = 1\times10^{10}/cm^3$

$$N_A = 2\times10^{18}/cm^3$$

$$N_D = 1.3\times10^{15}/cm^3$$

$$\therefore \phi_{bi} = 0.0259\times\ln\left(\frac{2.6\times10^{33}}{10^{20}}\right) = 0.8\,Volts$$

The junction capacitance per unit area is given by

$$\frac{C_j}{Area} = \frac{\varepsilon_s}{w} = \sqrt{\frac{q\varepsilon_s}{2(\phi_{bi}-V_a)}\times\frac{N_A N_D}{N_A+N_D}} \tag{4.2}$$

where, $q = 1.6 \times 10^{-19} Coulombs$

$V_a = -1 Volt$

$\varepsilon_s = K_s \times \varepsilon_0 = 11.8 \times 8.85 \times 10^{-14} = 104.4 \times 10^{-14} Farads/cm$

$$\therefore \frac{C_j}{Area} = \sqrt{\left(\frac{1.6 \times 10^{-19} \times 104.43 \times 10^{-14}}{2(0.8 - [-1])}\right) \cdot \left(\frac{2.6 \times 10^{33}}{(2 \times 10^{18}) + (1.3 \times 10^{15})}\right)}$$

$$= \sqrt{\left(\frac{167.088 \times 10^{-33}}{2(1.8)}\right) \cdot \left(\frac{2.6 \times 10^{33}}{2 \times 10^{18}}\right)}$$

$$= 7.767 \times 10^{-8} \ nanoFarads/\mu m^2$$

Area of the capacitance was measured from the chip layout and found out to be11960 μm^2. Hence, value for the p-resistor to n-epi junction capacitance is

$$C_j = 7.767 \times 10^{-8} \times 11960 = 0.928 \ picoFarads$$

4.1.2 n-resistor to p-well Capacitance

Here again the built-in potential is given by

$$\phi_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{4.3}$$

where, $n_i = 1 \times 10^{10} / cm^3$

$N_A = 2 \times 10^{18} / cm^3$

$N_D = 2.5 \times 10^{19} / cm^3$

$$\therefore \phi_{bi} = 0.0259 \times \ln\left(\frac{5 \times 10^{37}}{10^{20}}\right) = 1.056 \ Volts$$

The junction capacitance per unit area is given by

$$\frac{C_j}{Area} = \frac{\varepsilon_s}{w} = \sqrt{\frac{q\varepsilon_s}{2(\phi_{bi} - V_a)} \times \frac{N_A N_D}{N_A + N_D}} \tag{4.4}$$

where, $q = 1.6 \times 10^{-19} Coulombs$

$V_a = -1 Volt$

$\varepsilon_s = K_s \times \varepsilon_0 = 11.8 \times 8.85 \times 10^{-14} = 104.4 \times 10^{-14}\ Farads/cm$

$$\therefore \frac{C_j}{Area} = \sqrt{\left(\frac{1.6 \times 10^{-19} \times 104.43 \times 10^{-14}}{2(1.056 - [-1])}\right) \cdot \left(\frac{5 \times 10^{37}}{(2 \times 10^{18}) + (2.5 \times 10^{19})}\right)}$$

$$= \sqrt{\left(\frac{167.088 \times 10^{-33}}{2(2.056)}\right) \cdot \left(\frac{5 \times 10^{37}}{2.7 \times 10^{19}}\right)}$$

$$= 274.2 \times 10^{-8}\ nanoFarads/\mu m^2$$

Area of the capacitance from the chip layout was found out to be11960 μm^2. Hence, value for the n-resistor to p-well junction capacitance is

$$C_j = 274.2 \times 10^{-8} \times 11960 = 32.79\ picoFarads$$

4.2 Capacitance Values Measured on LCR Meter

Capacitance measurements were made from one of the eight-element rosettes on the test chip shown in Fig. 4.1. To measure the capacitance between p-type resistor and n-epi layer, pads from the $0°$ p-type resistor and $90°$ p-type resistor were connected to one terminal of the LCR meter and n-epi layer was connected to the other terminal. Thus, the value measured on the LCR meter would be that of a parallel combination of two p-type resistor to n-epi layer capacitances and three capacitances due to the three bonding pads used in the measurement. Internal biasing of the LCR meter was used to bias its terminals

in order to maintain the diodes connected to them in reverse-biased mode. Similar connections were made to measure the n-type resistor to p-well capacitance, and hence the value measured would again be a parallel combination of two n-type resistor to p-well capacitances and three bonding pad capacitances.

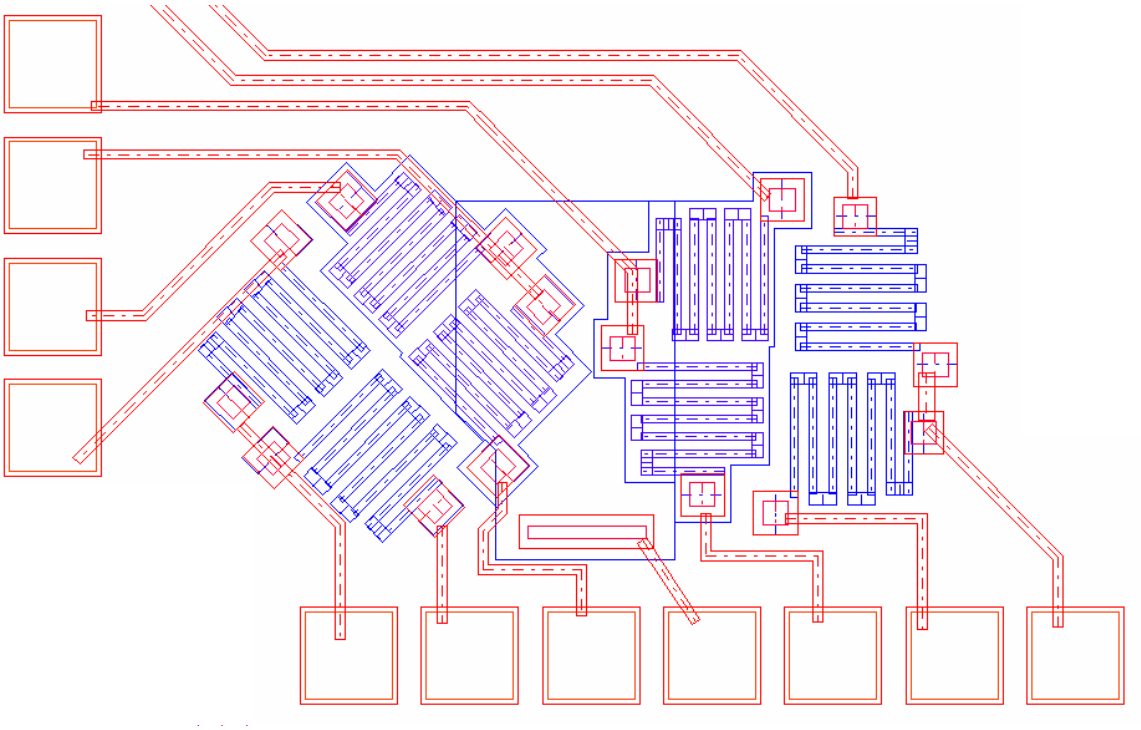


Figure 4.1 Eight-Element Rosette used for Measurements

Capacitance values were noted at different frequencies as shown in the following tables along with its transconductance value (G), dissipation factor (D) and quality factor (Q). Measurements were taken from three chip-on-board samples and all the sets of values are shown in Table 4.1 to Table 4.6 and capacitance plots are shown in Fig. 4.2 to Fig. 4.7.

Freq (KHz)	C (pF)	G (μS)	D	Q	mag(Z) (kΩ)	angle(Z)
30	7.43	0.06	0.04	25	714	-92.4
50	7.52	0.06	0.02	50	423.5	-91.6
100	7.56	0.06	0.01	100	210.7	-90.9
300	7.57	0.09	0.006	166.67	70.2	-90.89
500	7.57	0.15	0.006	166.67	42.11	-91.2
1000	7.55	0.48	0.01	100	21.05	-92.3
3000	7.5	3.5	0.02	50	7.08	-91.3
5000	7.43	11.5	0.04	25	4.28	-92.5
10000	7.31	54.5	0.12	8.3333	2.164	-96.6

Table 4.1 p-res to n-epi values for Sample #1

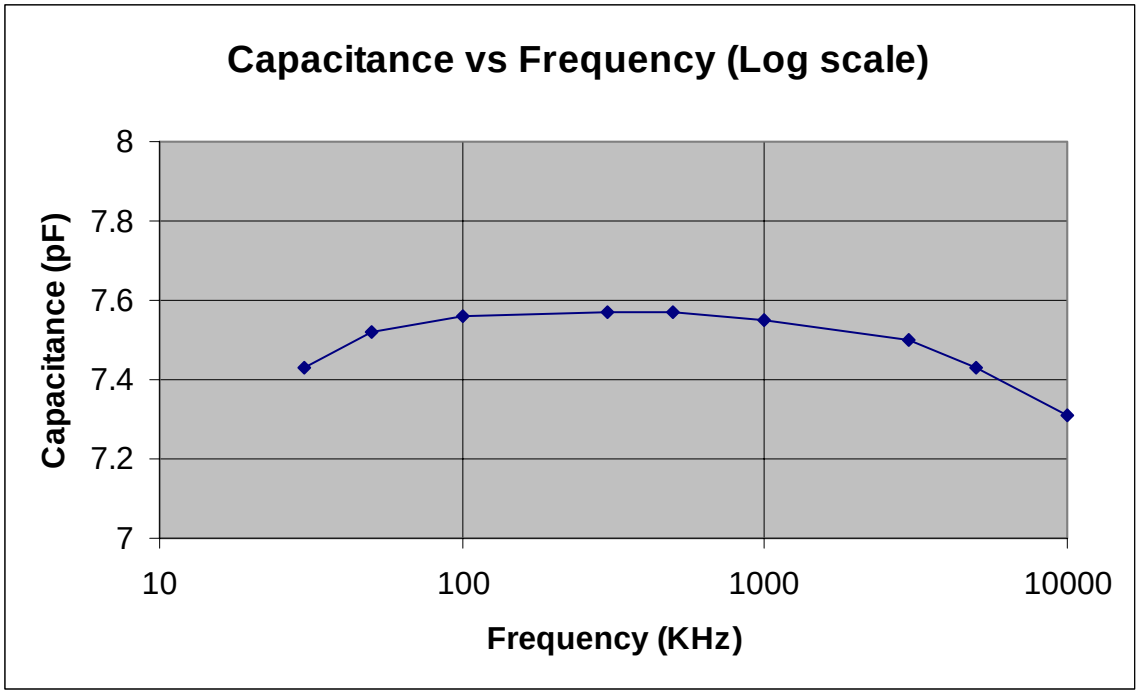


Figure 4.2 p-res to n-epi Capacitance Plot for Sample #1

Freq (KHz)	C (pF)	G (μS)	D	Q	mag(Z) (kΩ)	angle(Z)
30	7.36	0.06	0.05	20	721	-92.89
50	7.46	0.07	0.03	33.333	426	-91.89
100	7.52	0.07	0.01	100	211.5	-90.9
300	7.53	0.02	0.002	500	70.4	-90.18
500	7.53	0.04	0.001	1000	42.27	-90.02
1000	7.51	0.3	0.005	200	21.18	-89.78
3000	7.46	3.5	0.02	50	7.11	-88.86
5000	7.38	8.3	0.03	33.333	4.31	-88.16
10000	7.23	23.7	0.05	20	2.198	-87.08

Table 4.2 p-res to n-epi values for Sample #2

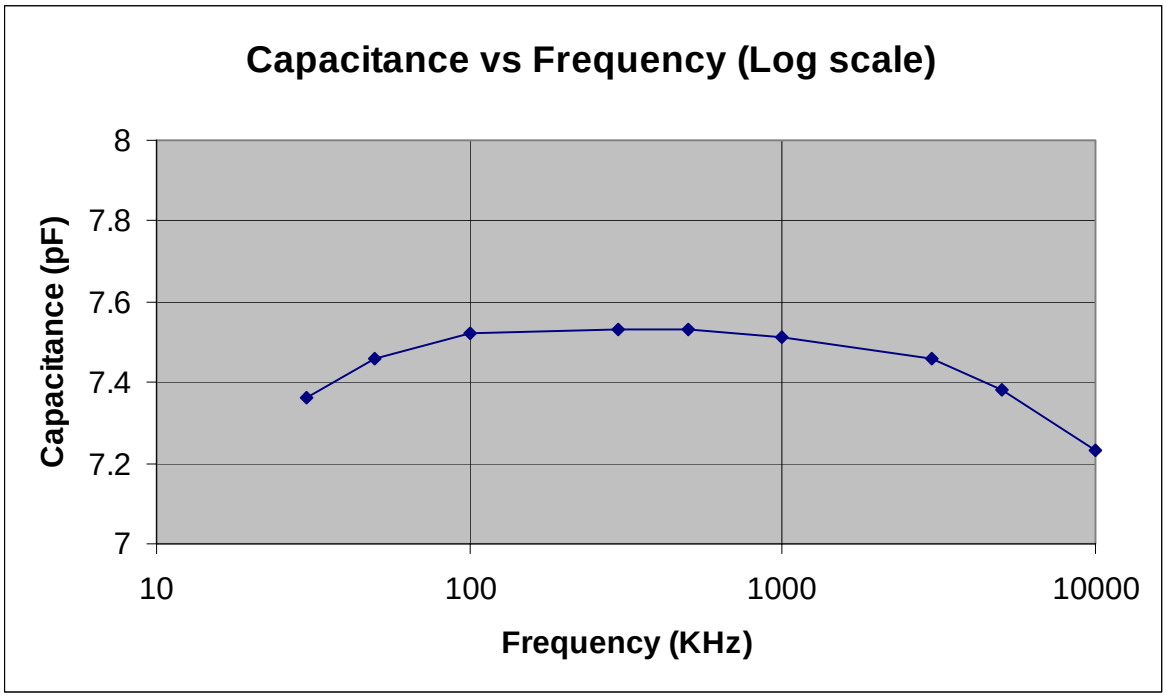


Figure 4.3 p-res to n-epi Capacitance Plot for Sample #2

Freq (KHz)	C (pF)	G (μS)	D	Q	mag(Z) (kΩ)	angle(Z)
30	7.4	0.08	0.06	16.667	715	-93.6
50	7.52	0.09	0.04	25	423	-92.25
100	7.58	0.09	0.02	50	210	-91.05
300	7.59	0.06	0.004	250	69.9	-90.27
500	7.59	0.02	0.001	1000	41.93	-90.05
1000	7.57	0.15	0.003	333.33	21	-89.81
3000	7.52	2.7	0.018	55.556	7.05	-88.97
5000	7.44	5.7	0.024	41.667	4.27	-88.6
10000	7.3	10.2	0.022	45.455	2.17	-88.69

Table 4.3 p-res to n-epi values for Sample #3

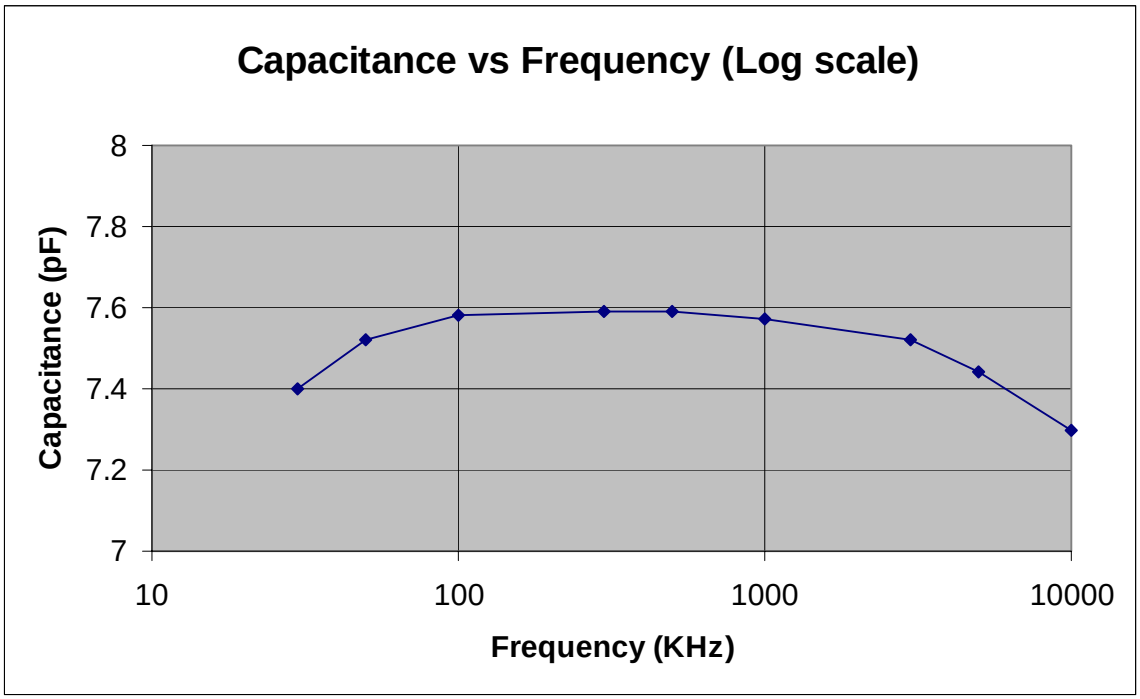


Figure 4.4 p-res to n-epi Capacitance Plot for Sample #3

Freq (KHz)	C (pF)	G (μS)	D	Q	mag(Z) (kΩ)	angle(Z)
30	72.41	0.13	0.007	142.86	73.3	-89.59
50	72.25	0.24	0.007	142.86	44.05	-89.59
100	72.05	0.65	0.008	125	22.08	-89.51
300	71.74	5.1	0.019	52.632	7.37	-88.89
500	71.34	13.6	0.032	31.25	4.42	-88.23
1000	69.7	50.9	0.059	16.949	2.22	-86.59
3000	68.63	224	0.183	5.4645	0.763	-79.9
5000	63.97	564	0.294	3.4014	0.48	-73.82
10000	50.83	1611	0.529	1.8904	0.282	-62.55

Table 4.4 n-res to p-well values for Sample #1

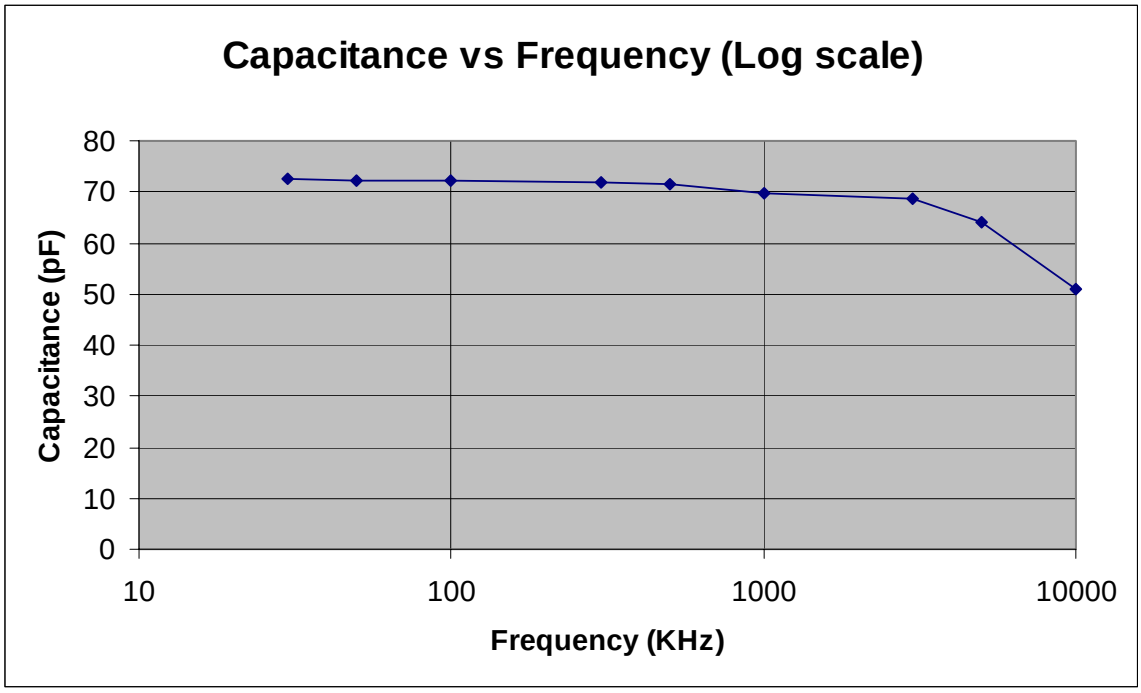


Figure 4.5 n-res to p-well Capacitance Plot for Sample #1

Freq (KHz)	C (pF)	G (μS)	D	Q	mag(Z) (kΩ)	angle(Z)
30	72.63	0.08	0.006	166.67	73	-89.68
50	72.54	0.14	0.006	166.67	43.88	-89.67
100	72.39	0.31	0.006	166.67	21.99	-89.61
300	72.26	2.3	0.016	62.5	7.34	-89.06
500	72.19	5.9	0.026	38.462	4.409	-88.5
1000	71.83	22.7	0.05	20	2.213	-87.09
3000	69.31	197	0.151	6.6225	0.757	-81.44
5000	65.24	496	0.242	4.1322	0.474	-76.3
10000	53.62	1419	0.422	2.3697	0.273	-66.97

Table 4.5 n-res to p-well values for Sample #2

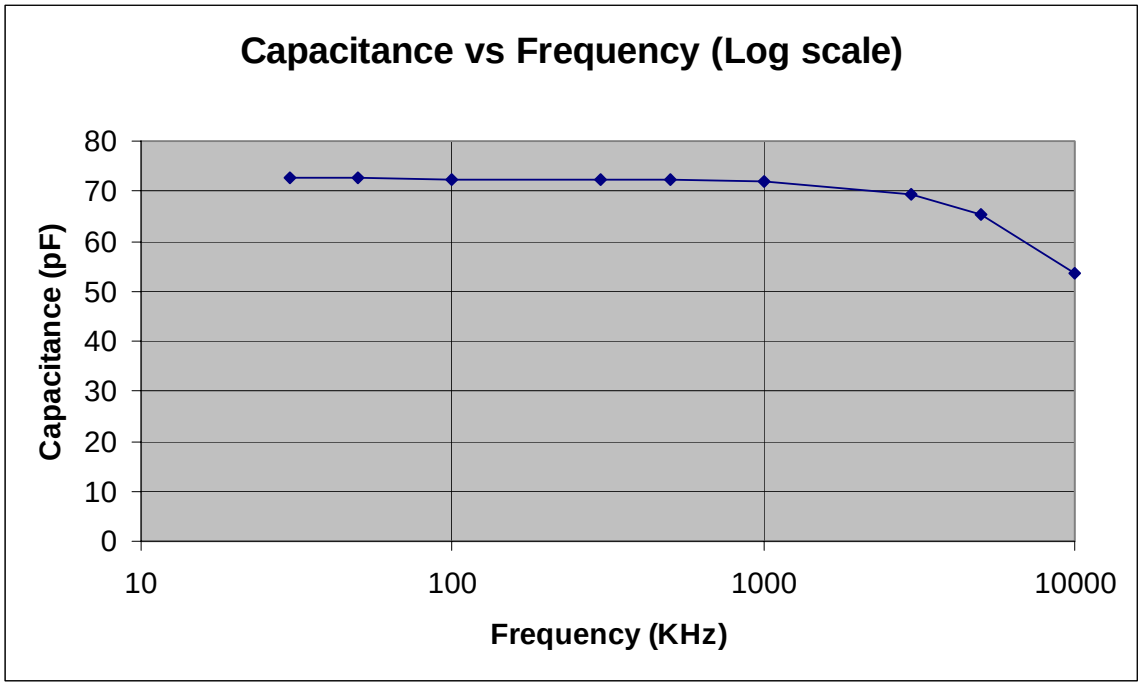


Figure 4.6 n-res to p-well Capacitance Plot for Sample #2

Freq (KHz)	C (pF)	G (μS)	D	Q	mag(Z) (kΩ)	angle(Z)
30	72.6	0.1	0.007	142.86	73	-89.6
50	72.45	0.17	0.007	142.86	43.9	-89.59
100	72.3	0.4	0.008	125	22.01	-89.5
300	72.15	2.9	0.021	47.619	7.35	-88.81
500	72.05	7.5	0.033	30.303	4.415	-88.1
1000	71.62	28.8	0.064	15.625	2.217	-86.33
3000	68.6	248	0.192	5.2083	0.76	-79.16
5000	63.57	627	0.315	3.1746	0.477	-72.52
10000	49.19	1818	0.589	1.6978	0.279	-59.46

Table 4.6 n-res to p-well values for Sample #3

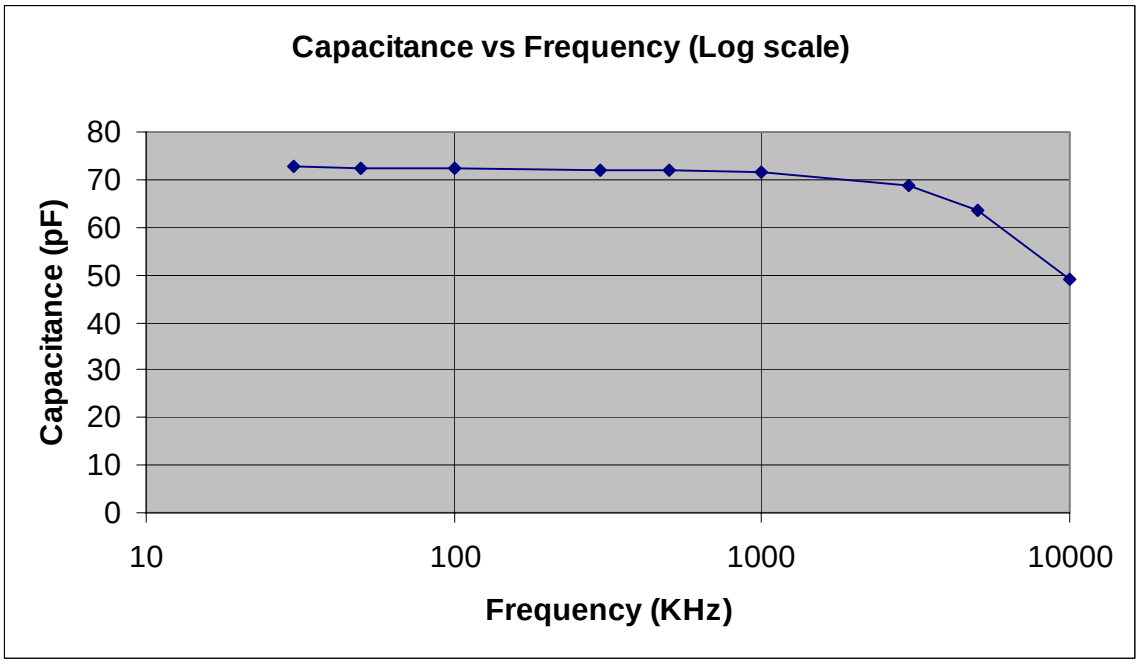


Figure 4.7 n-res to p-well Capacitance Plot for Sample #3

As can be seen from these tables, the typical value of the parallel combination of two p-type resistor to n-epi layer capacitances and three bonding pad capacitances is 7.4 pF. The parallel plate capacitance between an empty pad and substrate was measured on the LCR meter and was found to be 1.5 pF. As three bonding pads were used for each measurement on the LCR meter, the parallel combination of these three bonding pad capacitances would contribute 4.5 pF. Thus, the value of a single p-type resistor to n-epi layer capacitance would be 1.45 pF which is close to the calculated value of 0.928 pF.

Similarly, the typical value of the parallel combination of two n-type resistor to p-well capacitances and three bonding pad capacitances from the LCR measurements is 72.6 pF. Thus, the value of a single n-type resistor to p-well capacitance would be 34 pF which is close to the calculated value of 32.8 pF.

4.3 SPICE Simulations of the RC Network

The RC network formed by the p-type and n-type resistors and above mentioned capacitances determines the electrical cut-off frequency of the stress sensors. Here, we represent the piezoresistances in the test chip by resistors in SPICE whose values are made to oscillate around a center value at different frequencies. The aim of these simulations is to determine the oscillating frequency at which response of the RC network drops down by a considerable amount, which would be the electrical cut-off frequency of the stress sensors.

4.3.1 Voltage Controlled Resistor

Upon vibration of the chip-on-board system, values of piezoresistances on the chip oscillate at the vibrating frequency. This action is simulated with the help of Voltage Controlled Resistor (VCR) in SPICE. In a VCR circuit, an external voltage source controls the value of a resistor. The voltage source is usually of sinusoidal type whose frequency determines the oscillating frequency of the resistor.

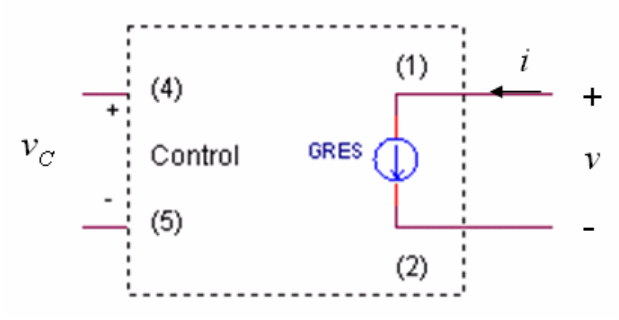


Figure 4.8 VCR Subcircuit

An important step in modeling a VCR is creating a model of a resistor without using a resistor. Applying voltage across the terminals of a resistor generates a current through it according to Ohm's Law. In a VCR circuit, this current is generated by a current source which senses the voltage across its terminals. As shown in Fig. 4.8, the control voltage (v_C) is applied across terminals 4 and 5, and GRES is the current source which senses the voltage and outputs a current according to Ohm's Law given by

$$i = \frac{v}{R \times v_C} \tag{4.5}$$

The SPICE model for a 2625Ω resistor whose value is forced to fluctuate by 10Ω at a frequency of 10 Hz is as follows

```
K_vcr.CIR - VOLTAGE-CONTROLLED RESISTOR

* CONTROL VOLTAGE
Vcont  10 0 DC 0 AC 1
+SIN 1 0.0039 10 0 0 0
RD10    10  0   1MEG


* CURRENT SOURCE
IS      0       1       DC      1

* VC RESISTOR
XVCR2           1 0     10 0    VC_RES2_10K
RD2     1       0       100MEG


*** VC RESISTOR USING A CURRENT SOURCE *********
*       RESISTOR - 1,2    CONTROL - 4,5
.SUBCKT VC_RES2_10K    1 2      4 5
GRES  1         2       VALUE = { V(1,2) / (2625*V(4,5)) }
.ENDS


* ANALYSIS
.TRAN           0.1MS  100MS

* VIEW RESULTS
.PRINT          TRAN V(1)
.PROBE
.END
```

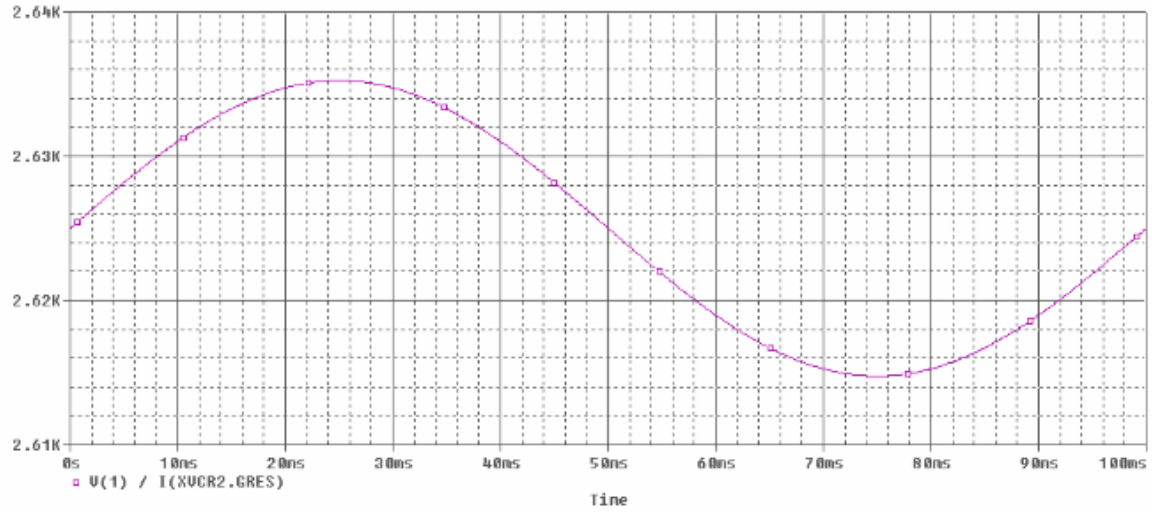


Figure 4.9 VCR Waveform

The frequency of oscillation is set by frequency of the sinusoidal control voltage, V_{cont}, whose amplitude sets the magnitude of oscillation. As I_S and G_{RES} are current sources, there is no DC conductance to ground. Hence, a large dummy resistor RD2 is placed across node 1 and ground. The resulting waveform in Fig. 4.9 shows the resistance value oscillating by $10\,\Omega$ at 10 Hz.

4.3.2 RC Network

The p-type resistor having value $10.50\ \mathrm{k}\Omega$ and the p-resistor to n-epi capacitance having value 0.924 pF is split into several sections as can be seen in Fig. 4.10 to increase the accuracy of simulation of the entire RC network. Each resistor in the network is a Voltage Controlled Resistor having a center value of $2625\,\Omega$. The $p0^o$ resistor is split into four VCRs, namely R1 to R4, which are controlled by control voltage V_{cont1}, while the $p90^o$ resistor is split between VCRs R5 to R8 controlled by V_{cont2}.

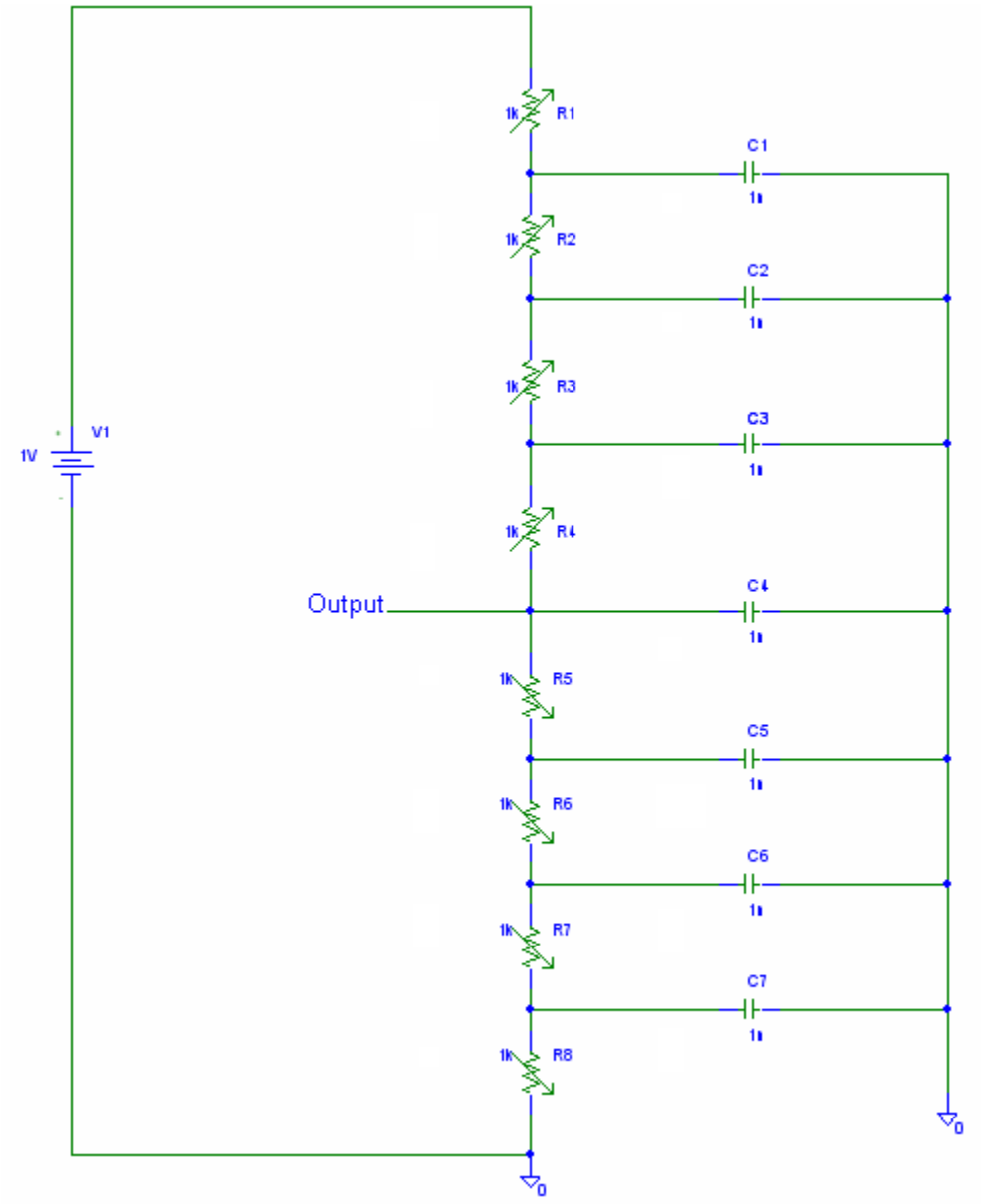


Figure 4.10 Entire RC Network

The two control voltages, V_{cont1} and V_{cont2}, are 180^o out of phase with each other such that when the value of the set of VCRs representing the $p0^o$ resistor increases, there is an equivalent decrease in the value of the set of VCRs representing the $p90^o$ resistor. A voltage source, V_1, is used to provide the biasing voltage of 1V to the resistors. The parallel combination of two p-type resistor to n-epi capacitances amounts to 1.855 pF which is split into 7 capacitors of 265 fF each. The SPICE model for the entire RC network is as follows

```
K_8vcrs+7cap+vin.CIR - VOLTAGE-CONTROLLED RESISTOR

* CONTROL VOLTAGE
Vcont1  10 0 DC 0 AC 1
+SIN 1 0.0039 50MEG 0 0 0
RD10a    10  0   1MEG

Vcont2  20 0 DC 0 AC 1
+SIN 1 0.0039 50MEG 0 0 180
RD10b    20  0   1MEG

* CURRENT SOURCE
IS1a 2   1   DC  1
IS1b 3   2   DC  1
IS1c 4   3   DC  1
IS1d 5   4   DC  1

IS2a 6   5   DC  1
IS2b 7   6   DC  1
IS2c 8   7   DC  1
IS2d 0   8   DC  1


* VC RESISTORS
XVCR1a   1 2 10 0    VC_RES_1K
RD1a 1 0 100MEG
XVCR1b   2 3 10 0    VC_RES_1K
RD1b 2 0 100MEG
```

```
XVCR1c   3 4 10 0    VC_RES_1K
RD1c 3 0 100MEG
XVCR1d   4 5 10 0    VC_RES_1K
RD1d 4 0 100MEG


XVCR2a   5 6 20 0    VC_RES_1K
RD2a 5 0 100MEG
XVCR2b   6 7 20 0    VC_RES_1K
RD2b 6 0 100MEG
XVCR2c   7 8 20 0    VC_RES_1K
RD2c 7 0 100MEG
XVCR2d   8 0 20 0    VC_RES_1K
RD2d 8 0 100MEG



C1  2  0 265e-15
C2  3  0 265e-15
C3  4  0 265e-15
C4  5  0 265e-15
C5  6  0 265e-15
C6  7  0 265e-15
C7  8  0 265e-15


Vin 1 0 1

*** VC RESISTOR USING A CURRENT SOURCE *********
*   RESISTOR - 1,2     CONTROL - 4,5
.SUBCKT VC_RES_1K 1 2 4 5
GRES    1   2   VALUE = { V(1,2) / (2625*V(4,5)) }
.ENDS


* ANALYSIS
.TRAN   0.001uS  0.1uS

* VIEW RESULTS
.PRINT  TRAN    V(1)
.PROBE
.END
```

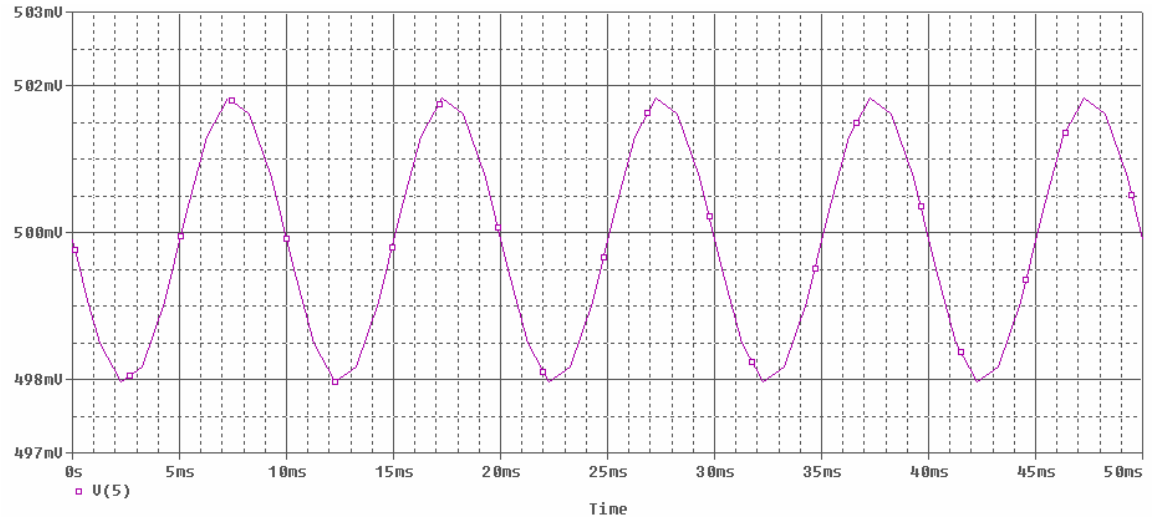


Figure 4.11 Output Voltage at 100Hz Oscillating Frequency

Figure 4.11 shows the plot of output voltage of the RC network at an oscillating frequency of 100Hz. The swing in output voltage at this frequency is 1905 μ V for a 10 Ω swing in each VCR in the circuit. The model was simulated at various values of the control voltage frequency which is the oscillating frequency of the VCRs and the change in output voltage was observed. Table 4.7 shows the change in output voltage of the RC network at various frequencies and the results are plotted in Fig. 4.12.

As can be seen from the simulation results, there is a considerable swing in the output voltage for oscillating frequencies up to 10 MHz after which the circuit response drops sharply.

Frequency (Hz)	Voltage Change (μV)
1.0E+00	1931
1.0E+01	1931
1.0E+02	1931
1.0E+03	1931
1.0E+04	1930
1.0E+05	1930
1.0E+06	1923
5.0E+06	1861
1.0E+07	1815
5.0E+07	1093
1.0E+08	726
1.0E+09	170
1.0E+10	20

Table 4.7 RC Network Simulation Results

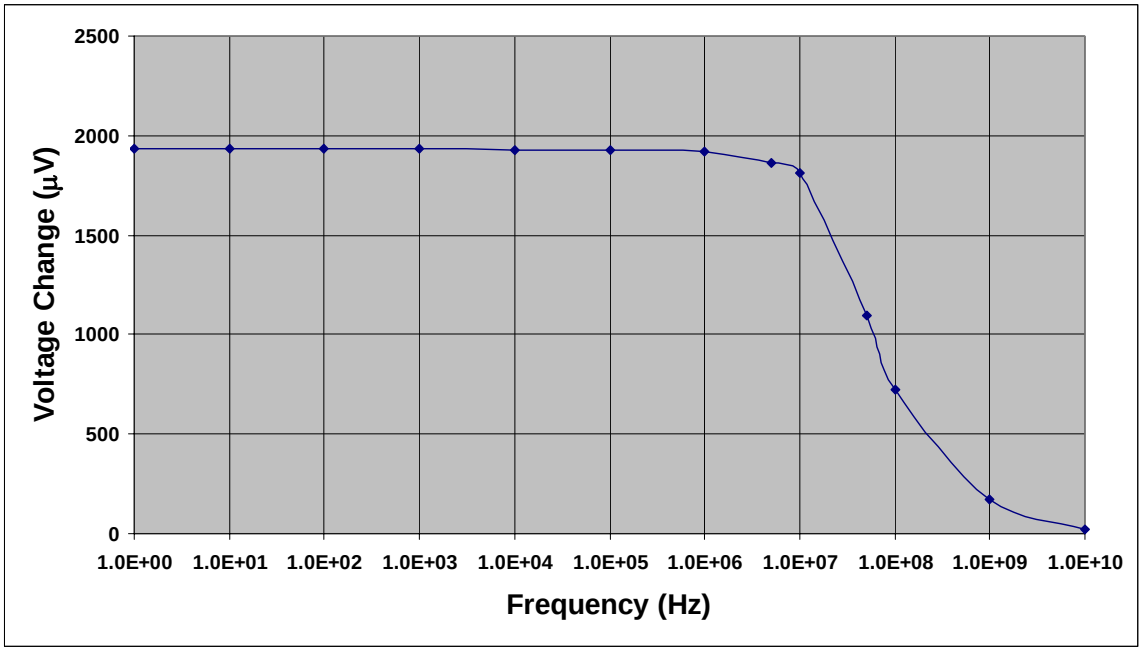


Figure 4.12 Change in Voltage Output of RC Network at Various Frequencies

4.3.3 Cut-off Frequency Estimation

An estimate of the cut-off frequency can be obtained using the classical open circuit time constant approach. The cut-off frequency of a RC network is given by

$$f_H = \frac{1}{2\pi \sum_i \tau_i} \tag{4.6}$$

where τ is the time constant given by

$$\tau = RC \tag{4.7}$$

The circuit in Fig. 4.10 has seven capacitors and hence will have seven time constants. To find the time constant for the circuit with capacitor C_1, all other capacitors will be represented by an open circuit. Thus, the equivalent circuit will be as shown in Fig 4.13 in which the equivalent resistance would be $2297\,\Omega$. The equivalent circuit with capacitor C_7 will be exactly the same and hence its equivalent resistance would also be $2297\,\Omega$.

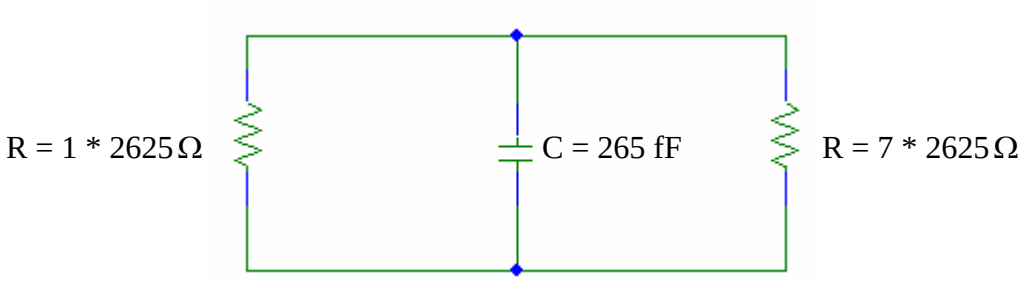


Figure 4.13 Equivalent circuit to calculate time constant due to capacitor C_1 or C_7

Similarly, the equivalent circuit for capacitor C_2 will be the same as capacitor C_6 and that for C_3 will be the same as C_5. Equivalent circuits for these capacitors are shown in Figs. 4.14 to 4.16.

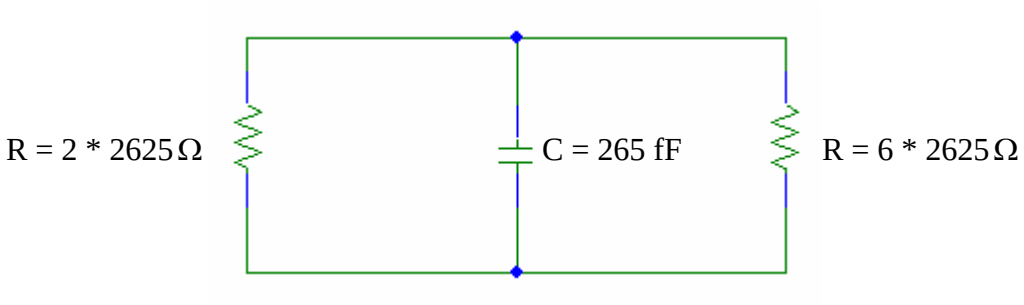


Figure 4.14 Equivalent circuit to calculate time constant due to capacitor C_2 or C_6

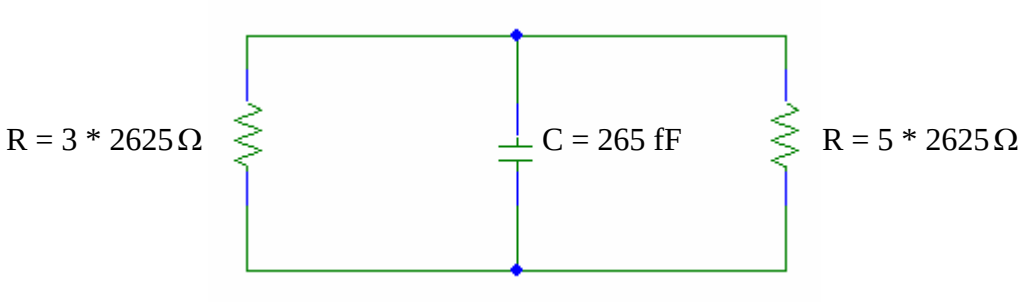


Figure 4.15 Equivalent circuit to calculate time constant due to capacitor C_3 or C_5

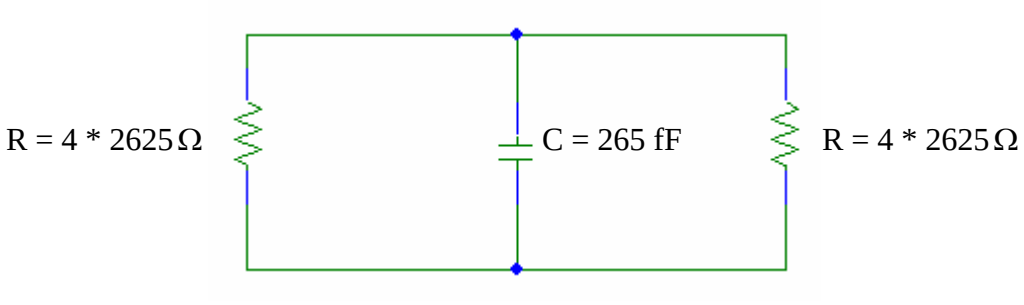


Figure 4.16 Equivalent circuit to calculate time constant due to capacitor C_4

Thus, substituting the values of equivalent resistances from the above circuits for individual capacitances in Eq. (4.7) and eventually in Eq. (4.6), we get

$$f_H = \frac{1}{2\pi\left(265\times10^{-15}\right)\left[2(2297)+2(3938)+2(4922)+5250\right]} \tag{4.8}$$

$$\therefore f_H = 21.8\ MHz$$

Thus, the estimated cut-off frequency of the RC network by open circuit time constant approach is 21.8 MHz.

4.3.4 Cut-off Frequency from SPICE Simulations

The cut-off frequency, f_H, is defined as the frequency at which output power of the circuit is reduced to half the value of its maximum power and is given by

$$P_{out}\left(f_H\right) = \frac{P_{\max}}{2} \tag{4.9}$$

Plugging in the definition of power across a resistor, we obtain the equation

$$\frac{V^2\left(f_H\right)}{R} = \frac{V_{\max}^2}{2R} \tag{4.10}$$

which leads to

$$V\left(f_H\right) = \frac{V_{\max}}{\sqrt{2}} \tag{4.11}$$

The decibel is a convenient unit when measuring values over a wide range. If the measurement is voltage, the value in decibels is defined as

$$V_{dB} = 20\log\left(\left|V\right|\right) \tag{4.12}$$

Plugging in Eq. (4.11) we get

$$V_{dB}(f_H) = 20\log\left(\frac{|V_{\max}|}{\sqrt{2}}\right) = 20\log(|V_{\max}|) - 20\log(\sqrt{2}) \tag{4.13}$$

$$\therefore V_{dB}(f_H) = V_{dB\max} - 3dB$$

Thus the voltage is 3dB down at the cut-off frequency. Substituting the maximum voltage value of 1931 μ V from Table 4.7 in Eq. (4.11), we get

$$V(f_H) = \frac{1931}{\sqrt{2}} = 1365\mu V$$

From SPICE simulations, the frequency at which output voltage change drops to 1365 μ V is obtained which equals 28 MHz. Thus, the electrical cut-off frequency, f_H, of the stress sensors represented by the RC network is 28 MHz. Fig. 4.14 shows the plot of output voltage of the RC network at 28 MHz where the voltage change is 1365 μ V.

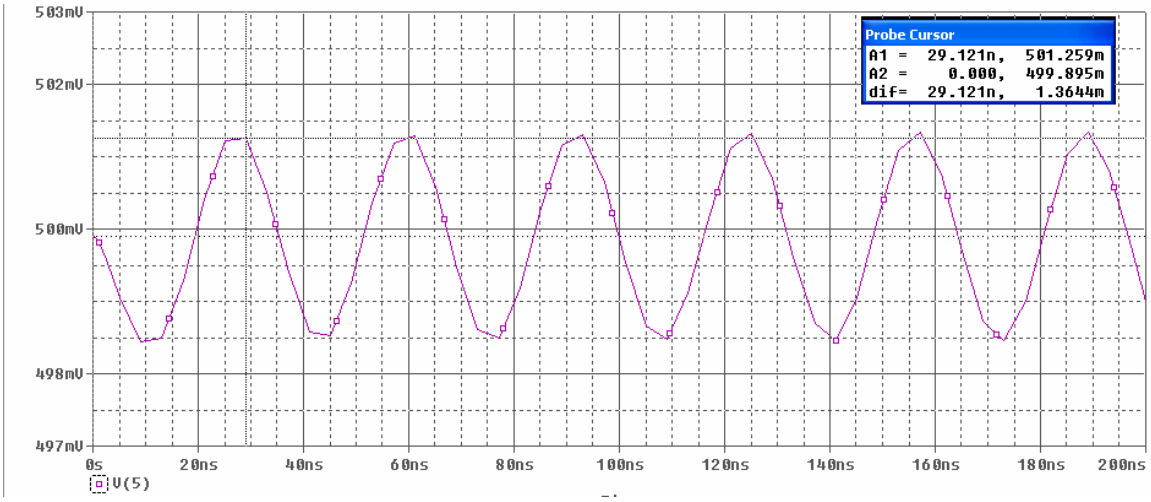


Figure 4.17 Output Voltage at the cut-off frequency of 28 MHz

Chapter 5

BEAM BENDING & SINUSOIDAL VIBRATIONS

Static beam bending experiments and sinusoidal vibrations of the test chip-on-board assembly were carried out on a shaker system. The shaker system along with the necessary electronics will be discussed in this chapter, followed by the static and dynamic test results. Tests carried out on a cantilever beam holder to support the variation in sensor output at low frequencies will be explained. Finally, the static test results will be compared with the finite element analysis results of the chip-on-board assembly in ANSYS™.

5.1 Shaker System

A block diagram of the shaker system is shown in Fig. 5.1. The heart of the shaker system is the HP35665A Dynamic Signal Analyzer shown in Fig. 5.2, which is used to control the vibrations of the shaker head and also acquire data output from the test chip. It is a two channel FFT spectrum analyzer with a frequency range that extends from DC to 102.4 KHz. It has a 3.5” built in floppy disk drive and a maximum of 800 lines of resolution. It can also be used to provide excitation signal through its source terminal.

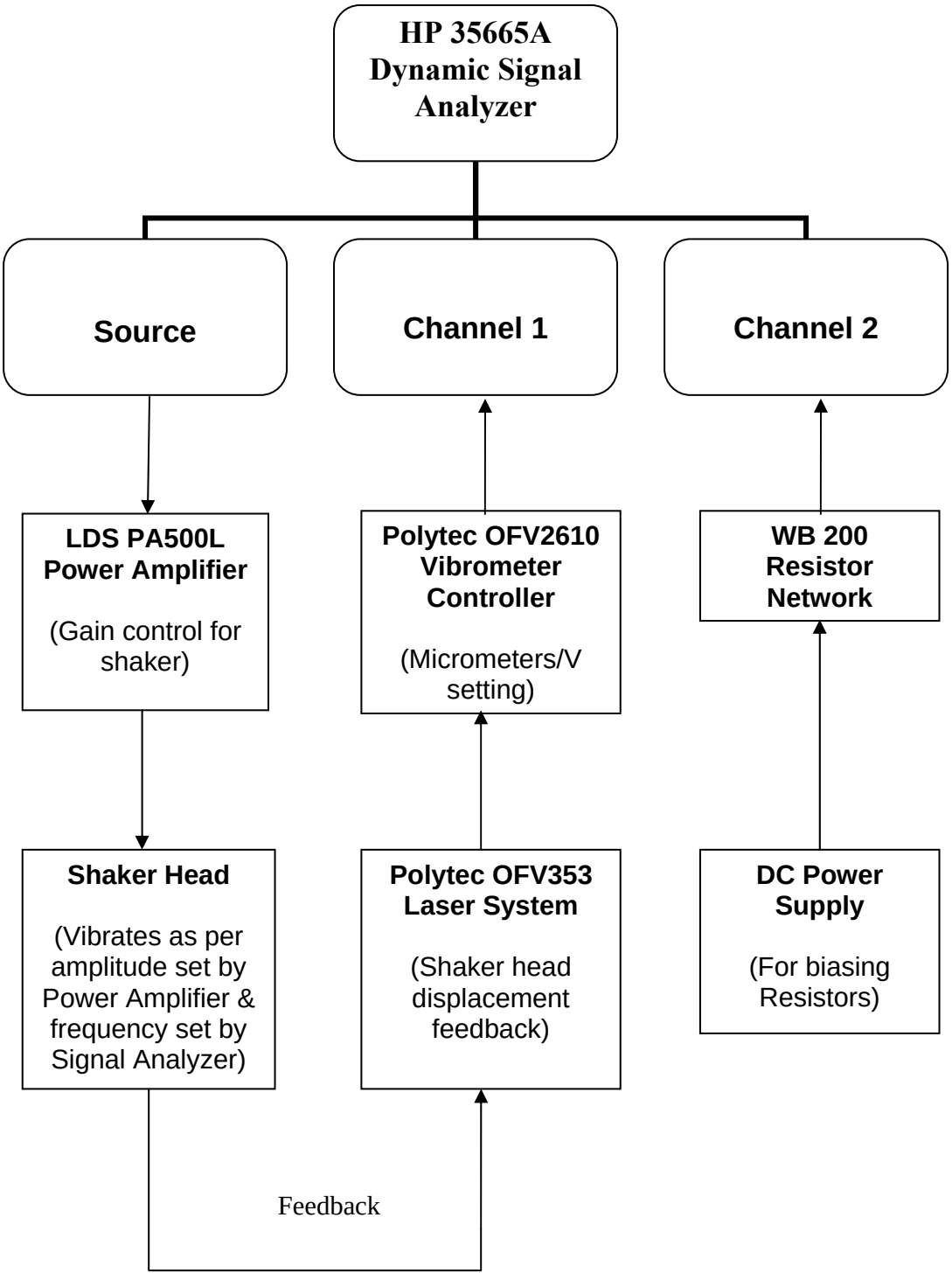


Figure 5.1 Block Diagram of Shaker System

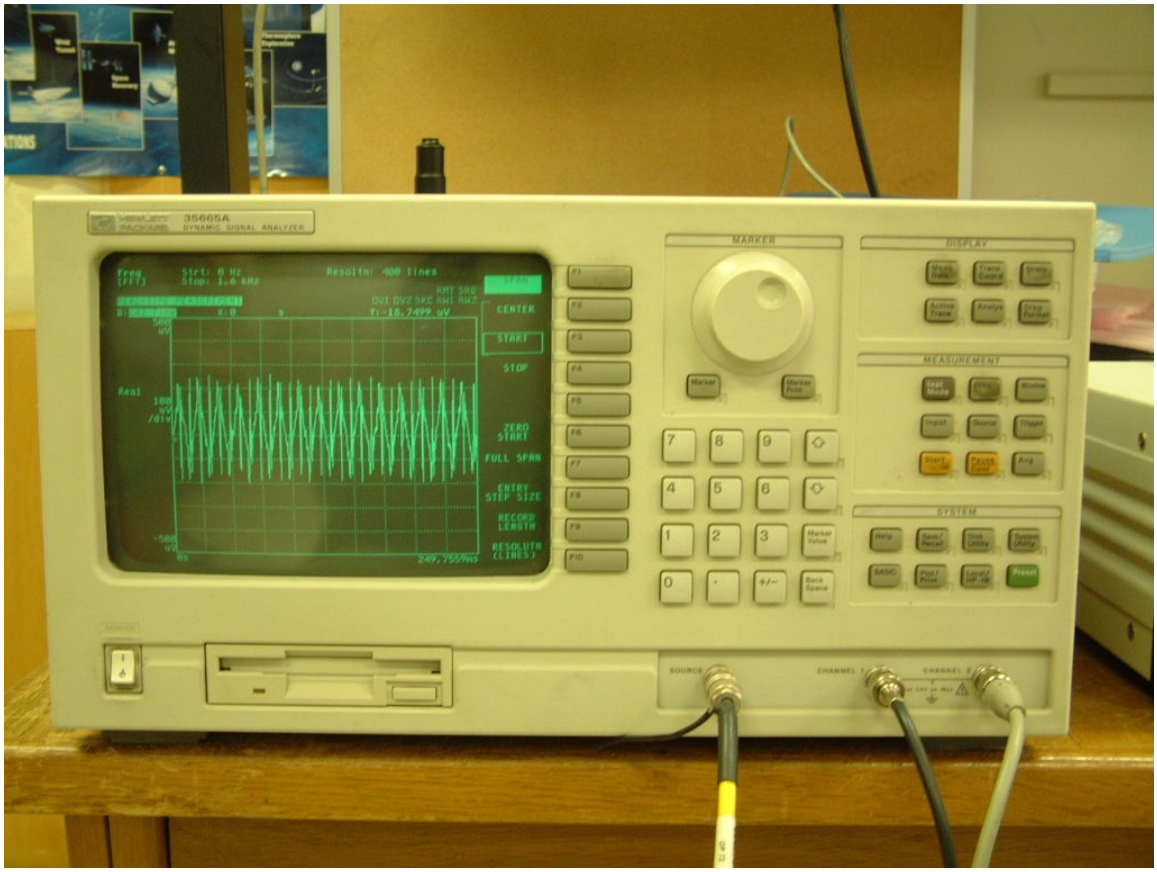


Figure 5.2 HP35665A Dynamic Signal Analyzer

A sinusoidal excitation signal can be provided through the source terminal of the signal analyzer to the LDS PA 500L power amplifier. The PA 500L shown in Fig. 5.3 is a linear amplifier designed for use with vibration test systems. With very low noise and low distortion performance, it has protection designed for vibration test equipment. The gain of the power amplifier can be adjusted to modify the amplitude of vibration of the shaker head.

Figure 5.3 LDS PA 500L Power Amplifier

The amplified sinusoidal signal from the power amplifier is applied to the shaker which makes the shaker head vibrate at the frequency specified in the signal analyzer settings and having an amplitude set by the gain control of the power amplifier. One end of the test chip-on-beam assembly is clamped to the shaker head such that it vibrates in vertical direction with the shaker head. A specially designed metal piece is used to rigidly clamp the other end of the chip-on-beam assembly. Thus, the PCB is approximately a clamped-clamped beam. The metal piece is firmly attached to the shaker bed as shown in Fig. 5.4.

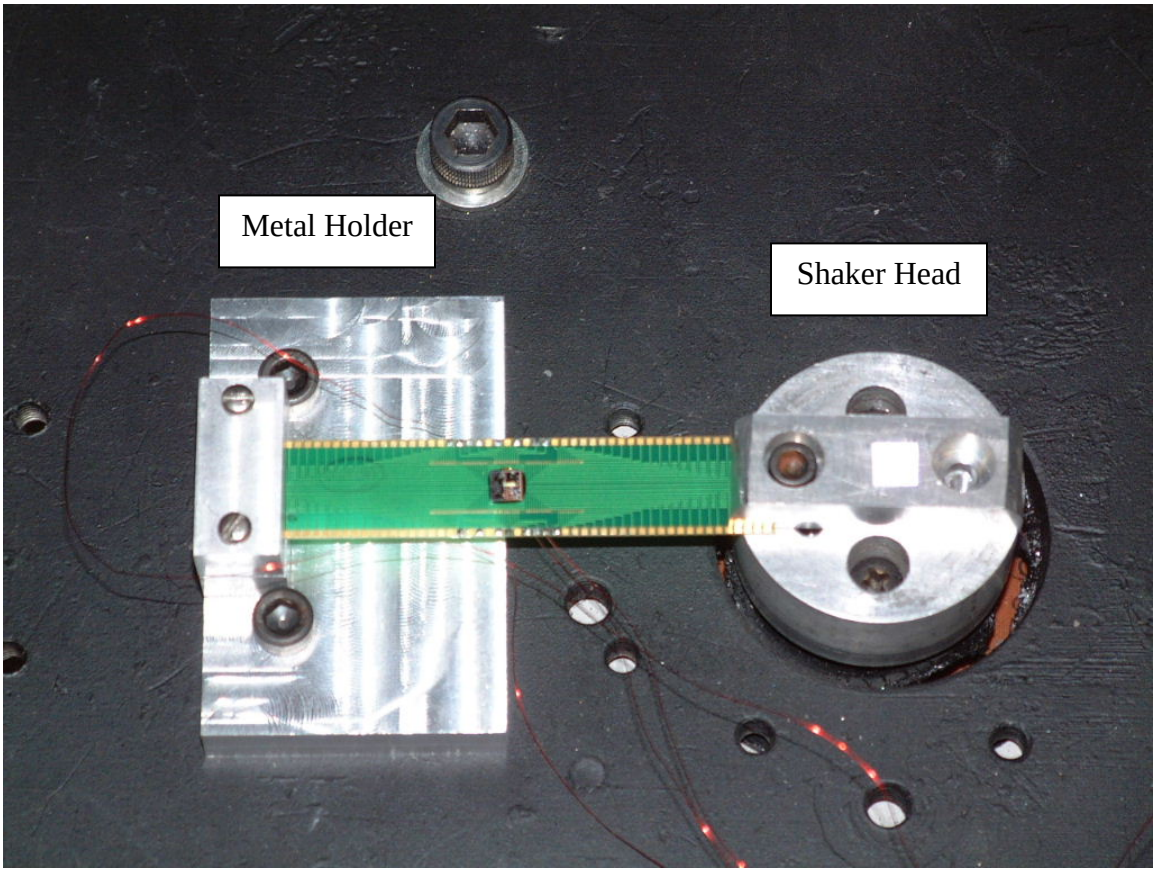


Figure 5.4 Chip-on-beam Attached to the Shaker Head and Metal Holder

A feedback system is implemented using a Polytec OFV 353 Laser System shown in Fig. 5.5 to measure the displacement of the laser head in the vertical direction. The laser beam is directed towards the shaker head with the help of reflectors in the laser system. The beam gets reflected by another reflector on the vibrating shaker head and is received back by the laser system. The corresponding signal which has information on position of the shaker head is fed to the Polytec OFV 2610 Vibrometer Controller, shown in Fig. 5.6, that can be set to pass the signal at different levels of micrometer/volt or millimeter/volt to a data acquisition system.

Figure 5.5 Polytec OFV 353 Laser System

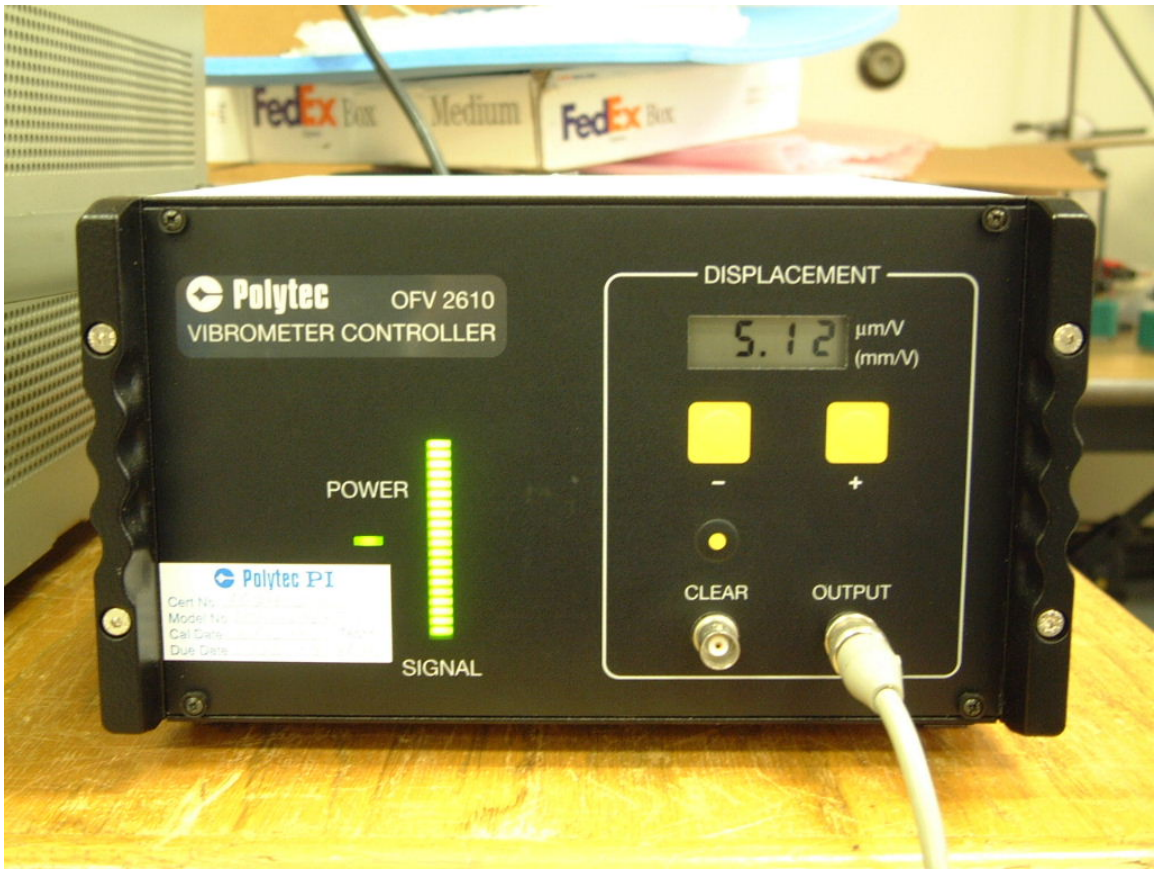


Figure 5.6 Polytec OFV 2610 Vibrometer Controller

The output signal from the vibrometer controller is fed to Channel 1 of the signal analyzer and can be displayed or recorded by the analyzer. The displacement amplitude of vibration of the shaker head can be calculated by multiplying the voltage amplitude of this sinusoidal signal from the vibrometer controller with the millimeter/volt or micrometer/volt setting.

Channel 2 of the signal analyzer receives the output signal from the test chip resistor network which is biased with the help of a DC source.

5.2 Sinusoidal Vibrations

Vibration analysis of the chip-on-board assembly was carried out on the shaker system shown in Fig. 5.4. As can be seen in the figure, one end of the board was securely held by the metal holder while the other end was clamped by another metal piece on top of the shaker head. It is important to note here that the board assembly does not represent a cantilever beam due its boundary conditions.

The p-type resistor pair from the sensor rosette shown in Fig. 5.7 is used for measurements. The top terminal of the p90 resistor was held at 1V, while bottom terminal of the p0 resistor was connected to ground. The terminal between the two resistors was connected to the signal analyzer to obtain the sensor output. To ensure proper biasing of the diodes, the n-epi layer was also connected to 1V.

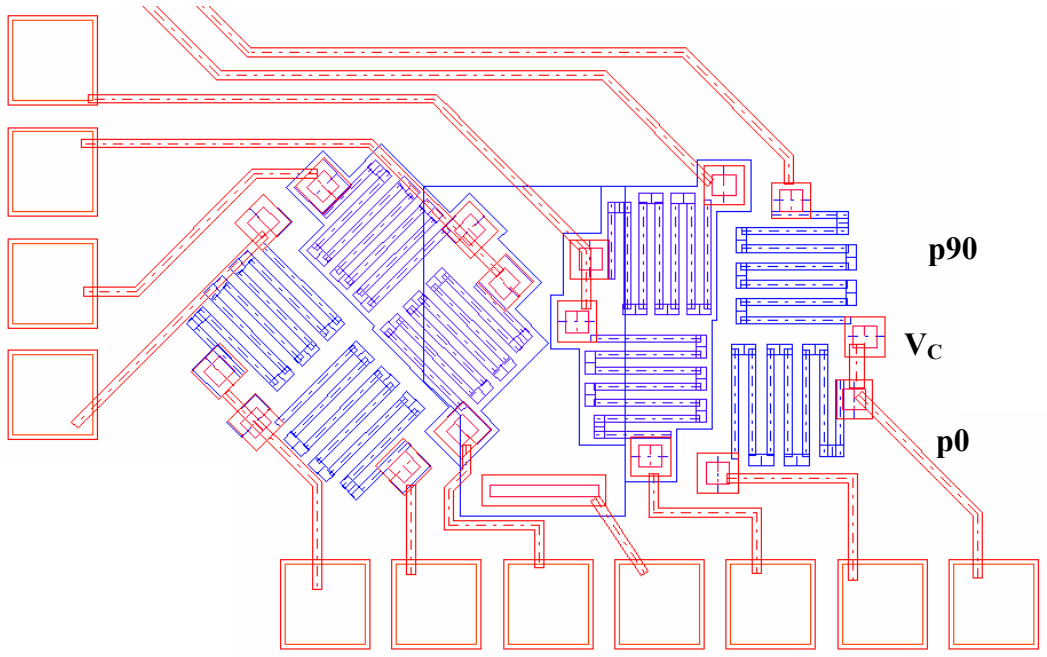


Figure 5.7 Sensor Rosette used for Measurements

At steady state, when the test assembly is not vibrated, the output from the center terminal V_C would remain fixed at approximately 500mV. On application of sinusoidal vibrations, the voltage output from the center terminal V_C starts oscillating about the fixed value at exactly the vibrating frequency of the shaker. However, the amplitude of voltage oscillation is dependent on the amplitude of vibration of the shaker head which is set by adjusting gain of the power amplifier and measured by the laser system. Thus, observing the amplitude of voltage oscillation on the signal analyzer gives a measure of the stresses developed on the test chip surface due to vibrations.

Initially, the test assembly was vibrated with the chip positioned at an equal distance of 3.5 cm from the two metal holders on either side. In this case, part of the board on one side of the chip would be under tension while the other half would be under compression. Thus, the chip was almost in a neutral zone with minimum stress and hence the change in voltage output from the p-type resistor circuit was low. In order to avoid this condition, clamping of the board was shifted such that the test chip was now at an offset measuring 2.9 cm from the metal holder and 4.1 cm from the shaker head. The change in voltage output from the sensor showed improvement at all frequencies and provided encouragement to increase the chip offset to obtain larger voltage change.

The chip was now placed at a maximum offset of 1.7 cm from the metal holder and 4.1 cm from the shaker head, obtained by rotating the metal holder by 180^o. The shaker head was forced to vibrate at a particular frequency with various amplitudes and the voltage signal from the center terminal of the p-type resistor pair was observed on the signal analyzer along with the laser signal. The amplitude of the laser signal was used to calculate the amplitude of vibration of the shaker head.

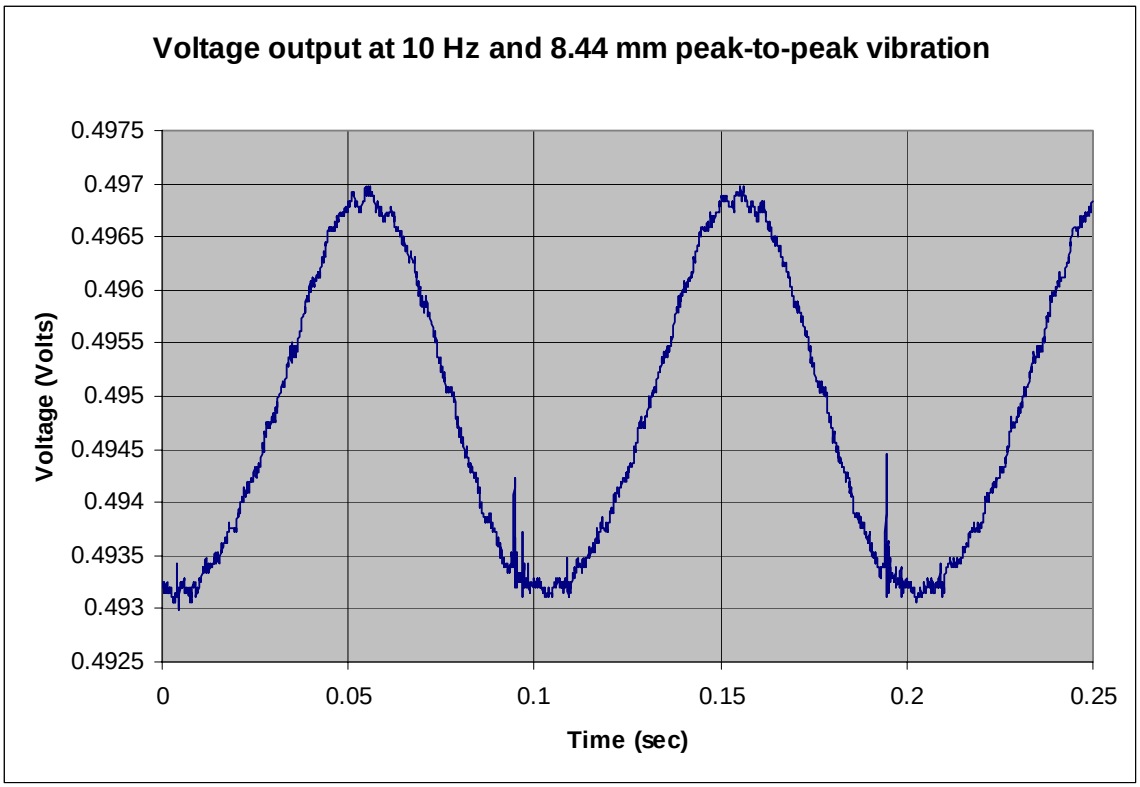


Figure 5.8 Voltage Output from center terminal V_C at 10 Hz

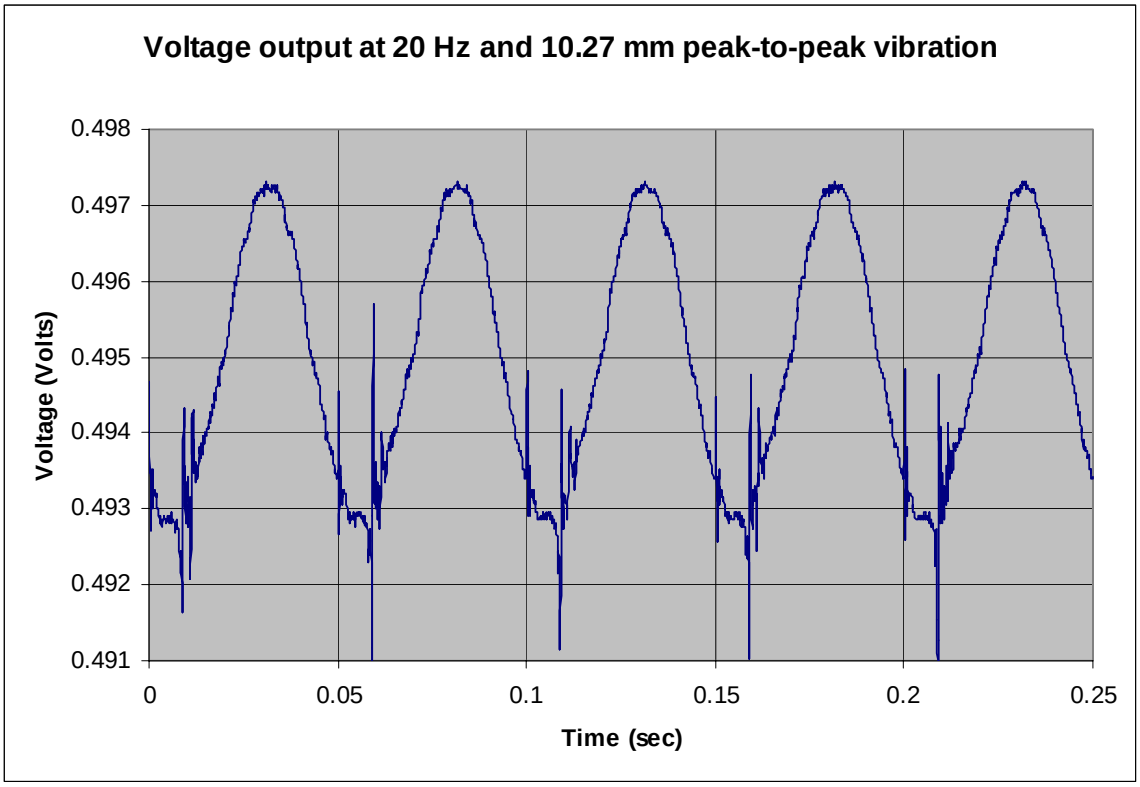


Figure 5.9 Voltage Output from center terminal V_C at 20 Hz

Voltage output from the center terminal observed on the signal analyzer for a vibrating frequency of 10 Hz and a peak-to-peak vibration of 8.44 mm of the shaker head is shown in Fig. 5.8, while the output at a vibrating frequency of 20 Hz and peak-to-peak vibration of 10.27 mm is shown in Fig. 5.9.

The stresses developed on the chip surface are represented by the change in output voltage at the center terminal. In order to note the value of change in output voltage as accurately as possible in the presence of noise signals, the frequency spectrum of the voltage signal was observed on the signal analyzer. The spectrum is a plot of voltage versus frequency and shows a sharp peak at the operating frequency and almost zero value at other frequencies. Voltage value at the sharp peak is the root mean square of the change in voltage of our output signal from the center terminal, and is multiplied by 1.41 to obtain the voltage change. Ten consecutive values of voltage change were recorded from the spectrum for every measurement and their average was used to plot graphs of change in voltage output versus peak-to-peak amplitude of the shaker head vibration at each frequency. The board was vibrated at various frequencies from 0.5 Hz to 200 Hz and the corresponding plots are shown in Fig. 5.10 to Fig. 5.28 with the voltage change values in Table 5.1 to Table 5.19.

Peak to Peak Vibration Amplitude(mm)	Change in Voltage Output (μVrms)	Change in Voltage Output (μV)
0.42	95	133.95
0.645	137	193.17
1.008	195	274.95
1.349	256	360.96
1.6	300	423
1.894	351	494.91

Table 5.1 Voltage Change Values at 0.5 Hz

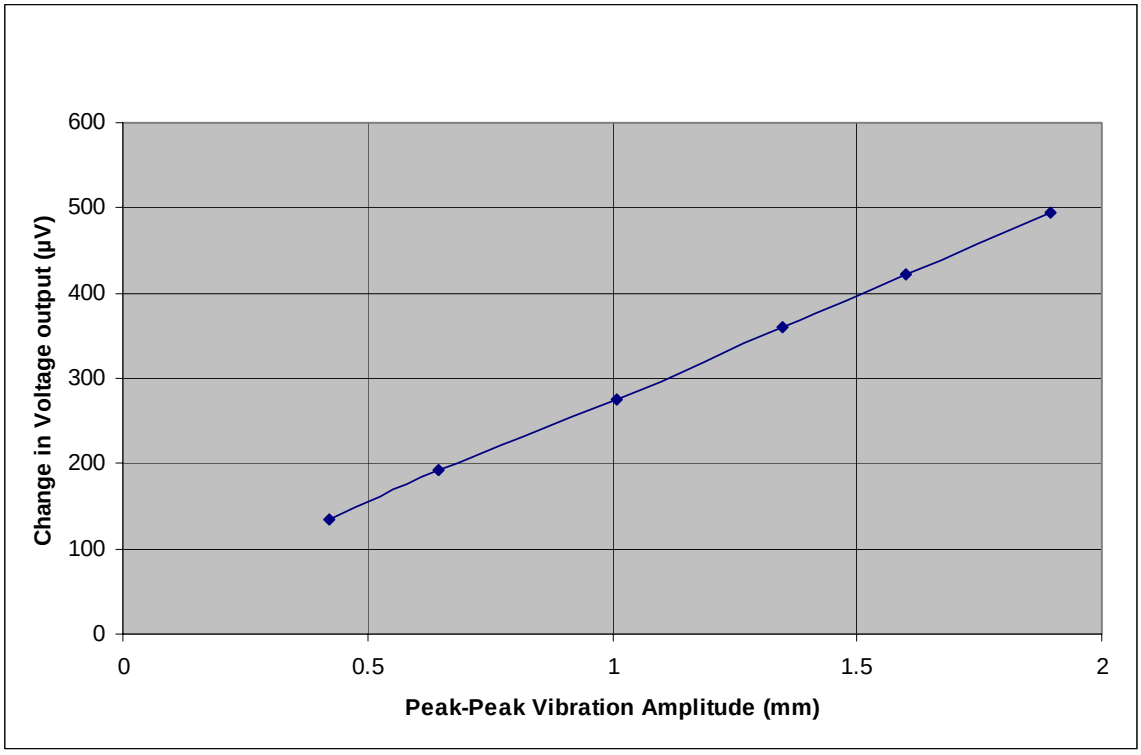


Figure 5.10 Voltage Change Plot at 0.5 Hz

Peak to Peak Vibration Amplitude(mm)	Change in Voltage Output (μVrms)	Change in Voltage Output (μV)
0.392	81	114.21
0.84	163	229.83
1.313	249	351.09
1.818	343	483.63
2.529	468	659.88
3.226	585	824.85
3.942	704	992.64

Table 5.2 Voltage Change Values at 0.75 Hz

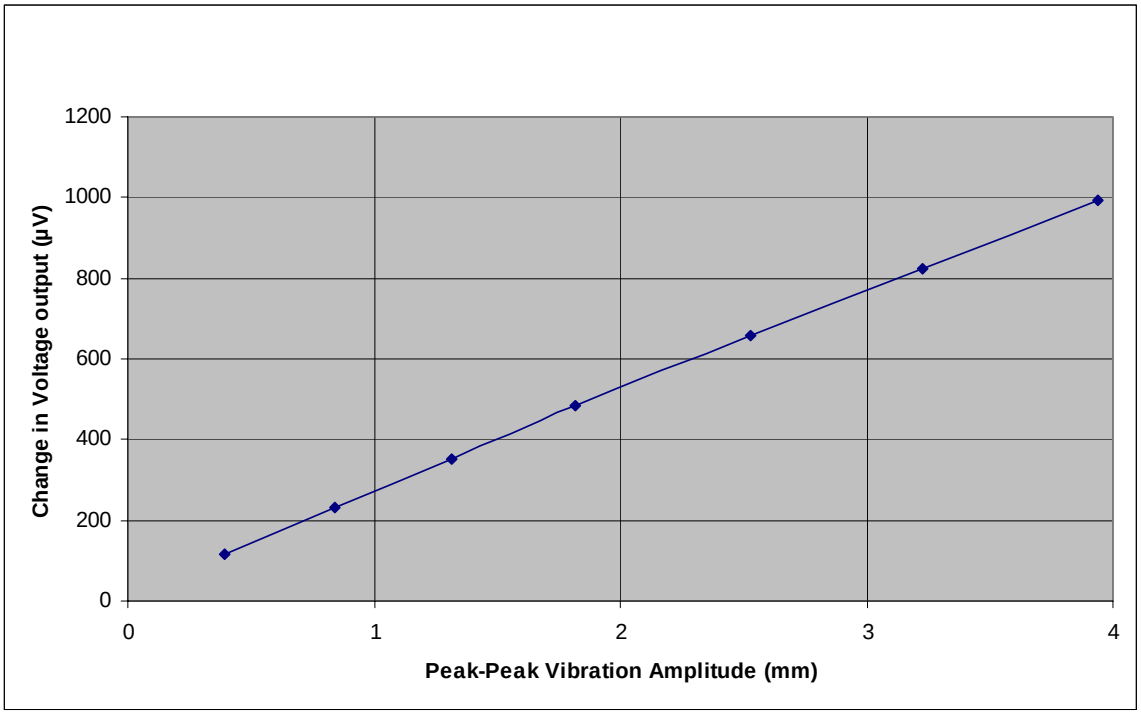


Figure 5.11 Voltage Change Plot at 0.75 Hz

Peak to Peak Vibration Amplitude(mm)	Change in Voltage Output (μVrms)	Change in Voltage Output (μV)
0.35	61	86.01
0.753	135	190.35
1.444	257	362.37
2.196	404	569.64
3.123	569	802.29
3.61	667	940.47
4.378	825	1163.3

Table 5.3 Voltage Change Values at 1 Hz

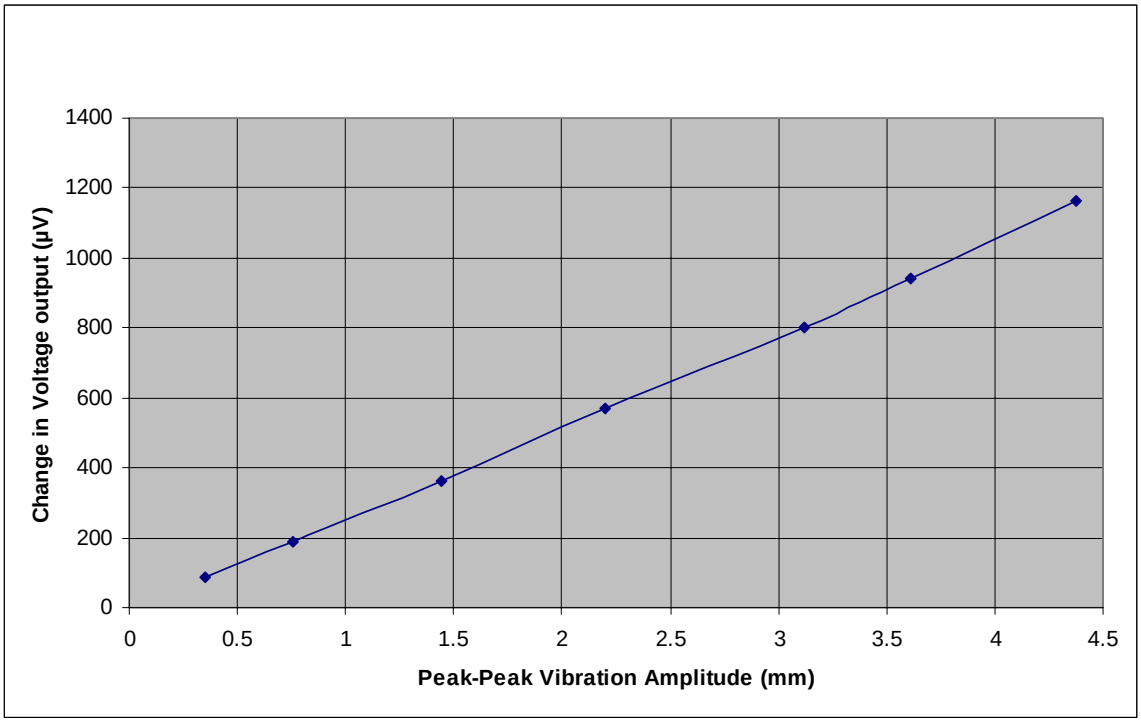


Figure 5.12 Voltage Change Plot at 1 Hz

Peak to Peak Vibration Amplitude(mm)	Change in Voltage Output (μVrms)	Change in Voltage Output (μV)
0.563	104	146.64
1.421	252	355.32
2.168	386	544.26
3.328	598	843.18
3.866	697	982.77
4.915	890	1254.9

Table 5.4 Voltage Change Values at 2 Hz

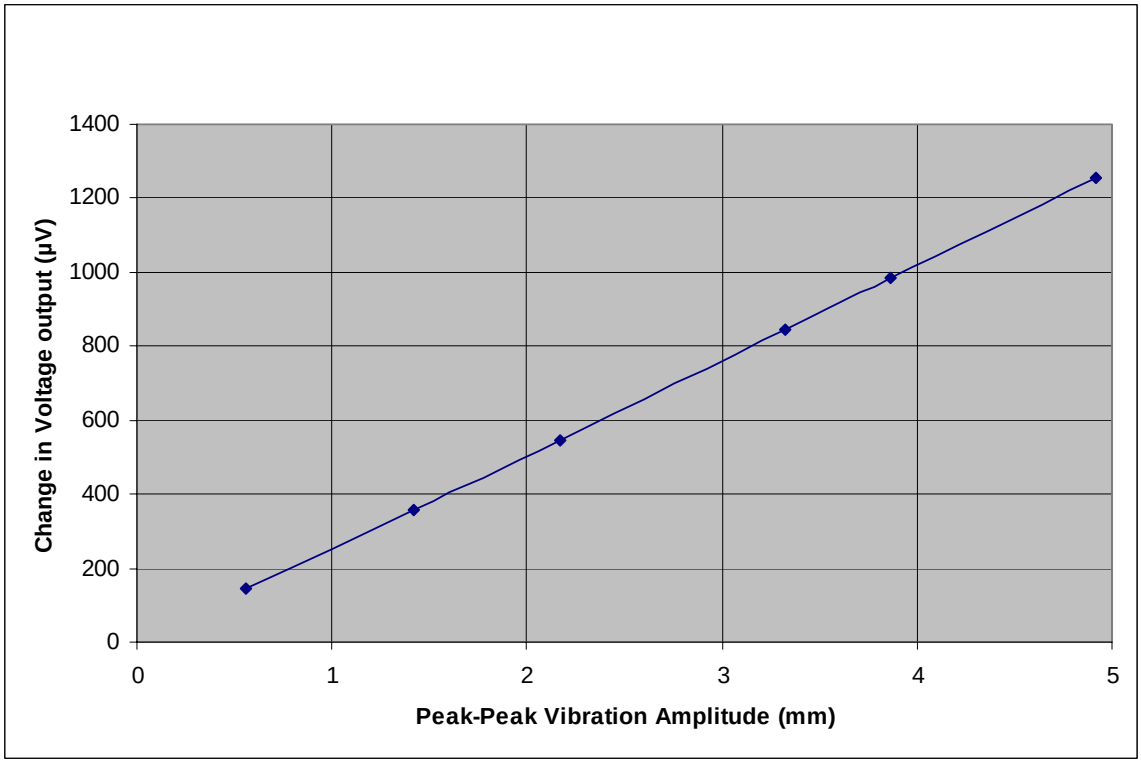


Figure 5.13 Voltage Change Plot at 2 Hz

Peak to Peak Vibration Amplitude(mm)	Change in Voltage Output (μVrms)	Change in Voltage Output (μV)
0.402	67	94.47
1.421	249	351.09
2.173	380	535.8
3.174	556	783.96
3.942	702	989.82
4.71	840	1184.4

Table 5.5 Voltage Change Values at 3 Hz

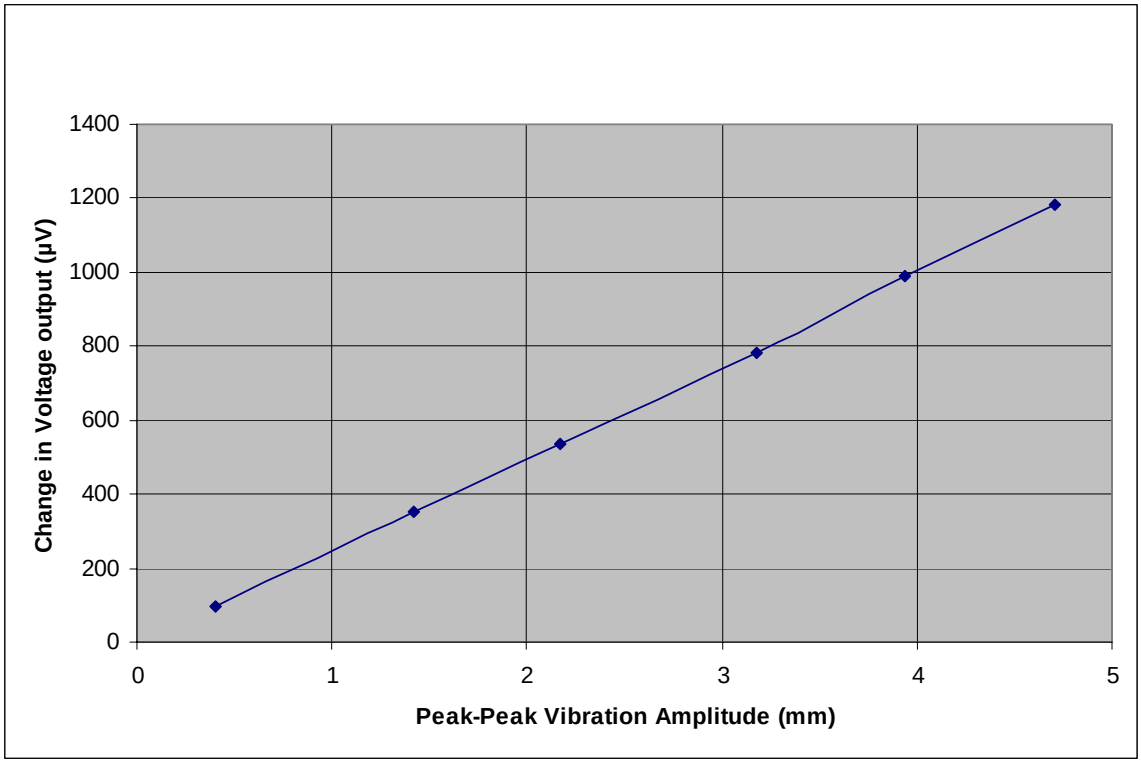


Figure 5.14 Voltage Change Plot at 3 Hz

Peak to Peak Vibration Amplitude(mm)	Change in Voltage Output (μVrms)	Change in Voltage Output (μV)
0.481	83	117.03
1.252	218	307.38
1.958	342	482.22
2.714	477	672.57
3.405	596	840.36
4.211	743	1047.6
4.634	819	1154.8

Table 5.6 Voltage Change Values at 4 Hz

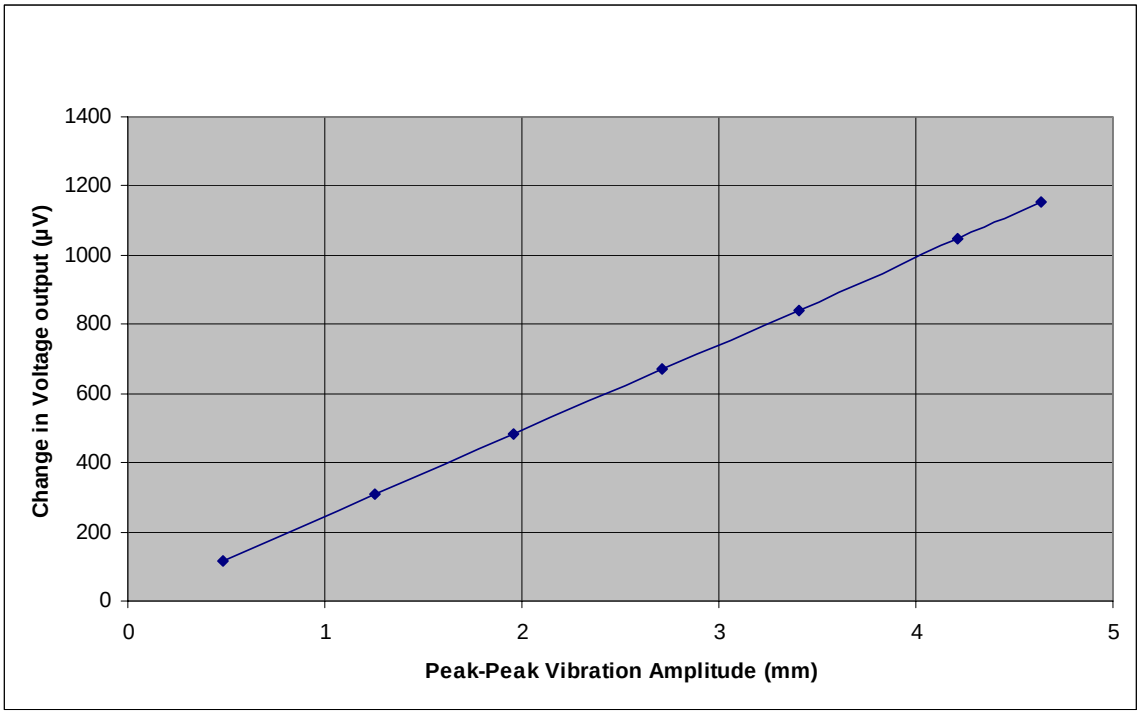


Figure 5.15 Voltage Change Plot at 4 Hz

Peak to Peak Vibration Amplitude(mm)	Change in Voltage Output (μVrms)	Change in Voltage Output (μV)
0.494	85	119.85
1.078	187	263.67
1.572	274	386.34
2.127	370	521.7
2.79	488	688.08
3.418	599	844.59
4.16	730	1029.3

Table 5.7 Voltage Change Values at 5 Hz

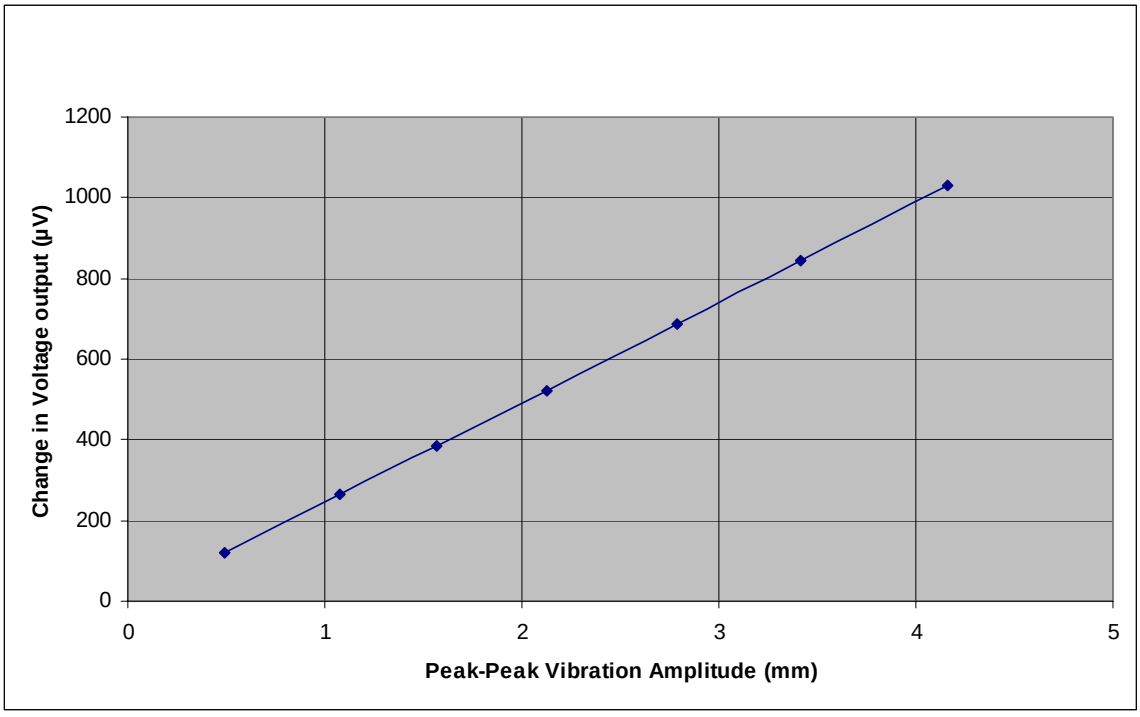


Figure 5.16 Voltage Change Plot at 5 Hz

Peak to Peak Vibration Amplitude(mm)	Change in Voltage Output (μVrms)	Change in Voltage Output (μV)
0.397	67	94.47
1.014	174	245.34
1.656	287	404.67
2.442	422	595.02
2.944	512	721.92
3.584	626	882.66
4.173	733	1033.5

Table 5.8 Voltage Change Values at 10 Hz

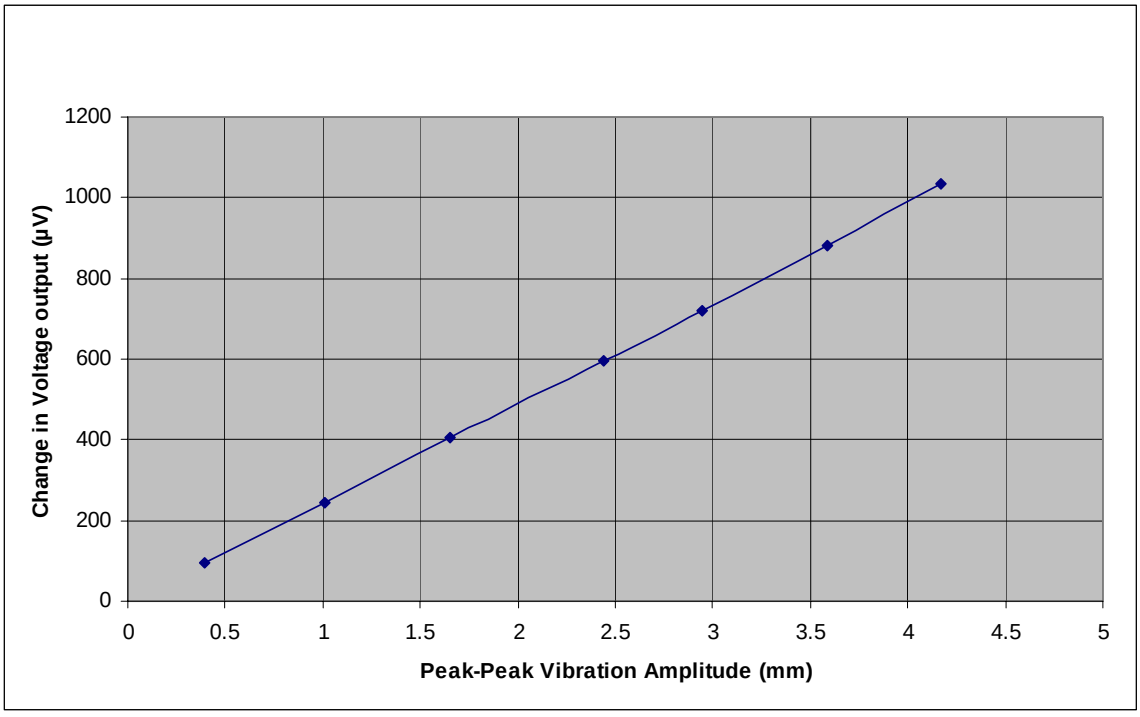


Figure 5.17 Voltage Change Plot at 10 Hz

Peak to Peak Vibration Amplitude(mm)	Change in Voltage Output (μVrms)	Change in Voltage Output (μV)
0.371	69	97.29
0.822	150	211.5
1.293	234	329.94
1.987	355	500.55
2.455	439	618.99
2.995	539	759.99
3.405	611	861.51
4.045	728	1026.5

Table 5.9 Voltage Change Values at 20 Hz

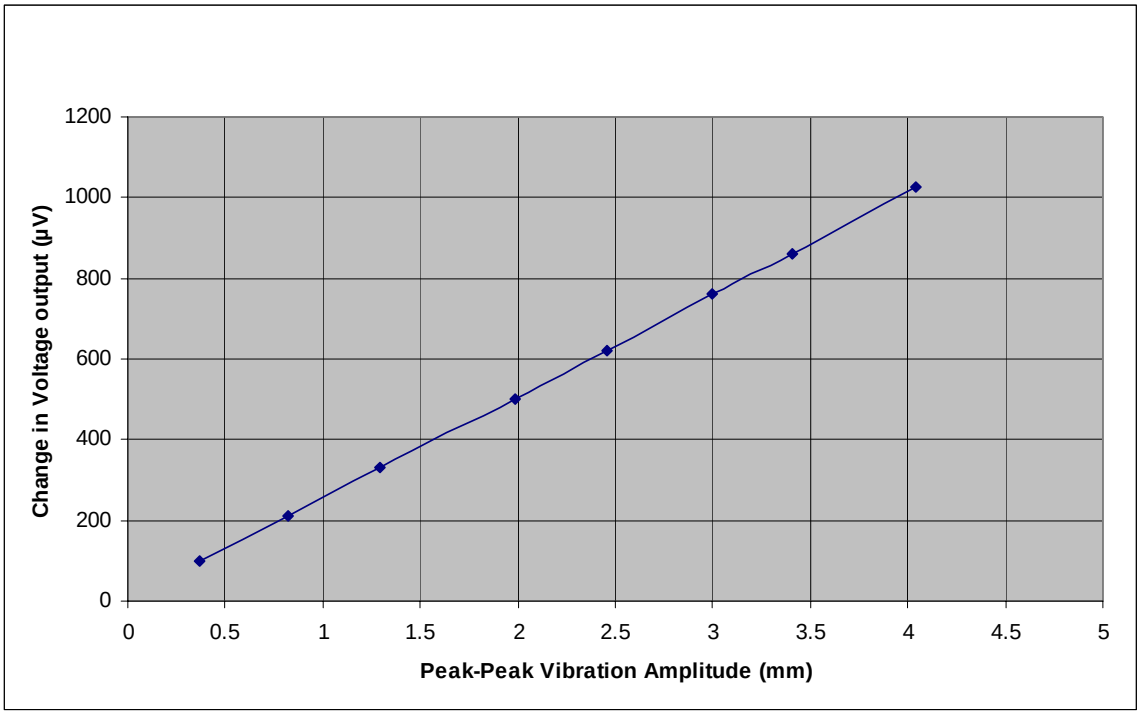


Figure 5.18 Voltage Change Plot at 20 Hz

Peak to Peak Vibration Amplitude(mm)	Change in Voltage Output (μVrms)	Change in Voltage Output (μV)
0.358	58	81.78
0.712	123	173.43
1.05	188	265.08
1.536	274	386.34
2.191	389	548.49
2.842	511	720.51
3.622	648	913.68
4.301	774	1091.3

Table 5.10 Voltage Change Values at 30 Hz

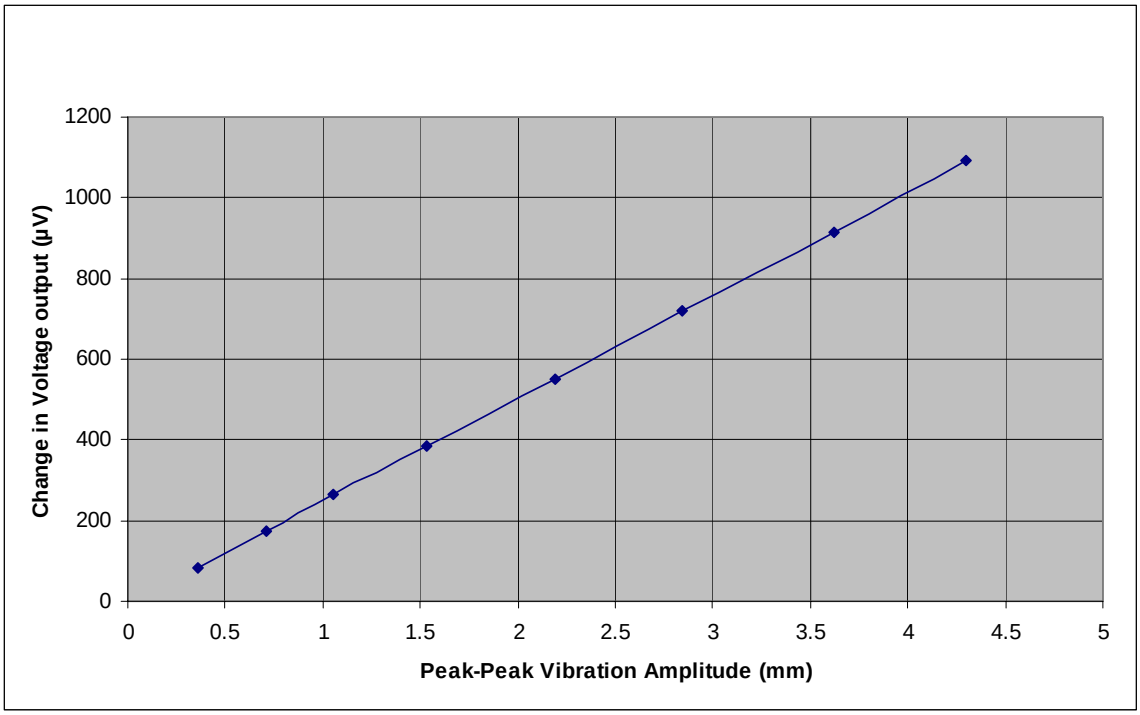


Figure 5.19 Voltage Change Plot at 30 Hz

Peak to Peak Vibration Amplitude(mm)	Change in Voltage Output (μVrms)	Change in Voltage Output (μV)
0.489	79	111.39
0.947	168	236.88
1.365	245	345.45
2.056	368	518.88
2.586	466	657.06
3.418	618	871.38
4.147	749	1056.1

Table 5.11 Voltage Change Values at 40 Hz

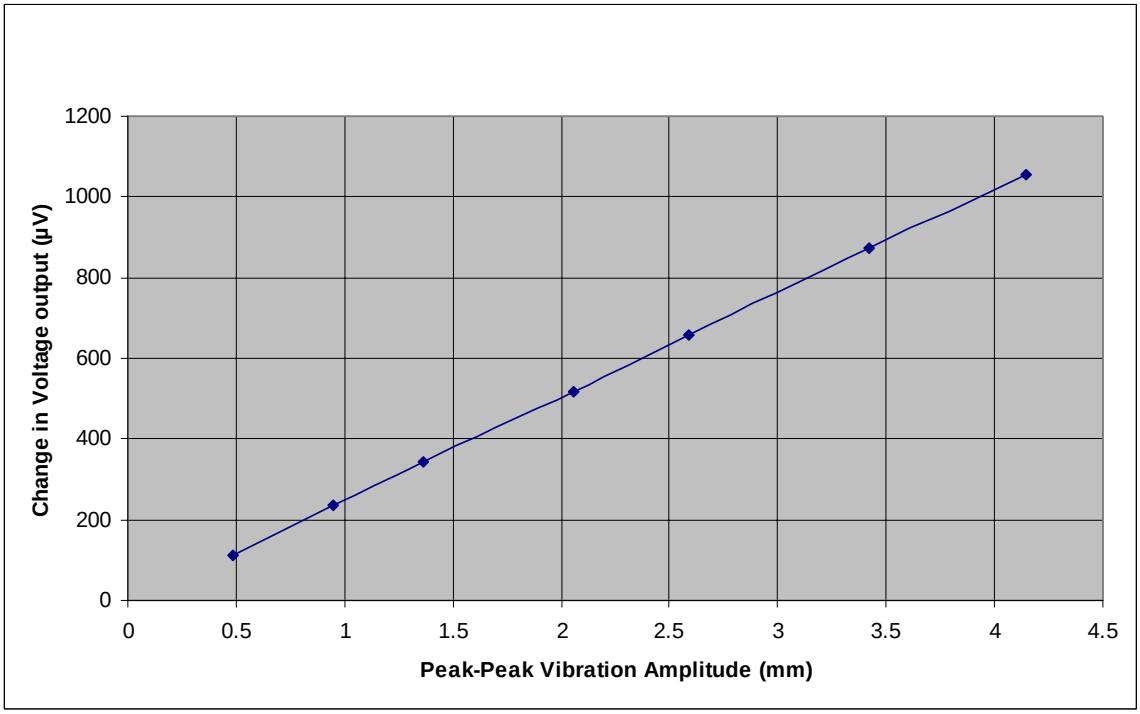


Figure 5.20 Voltage Change Plot at 40 Hz

Peak to Peak Vibration Amplitude(mm)	Change in Voltage Output (μVrms)	Change in Voltage Output (μV)
0.412	72	101.52
0.801	144	203.04
1.28	231	325.71
1.861	335	472.35
2.427	437	616.17
2.982	543	765.63
3.635	658	927.78
4.001	733	1033.5

Table 5.12 Voltage Change Values at 50 Hz

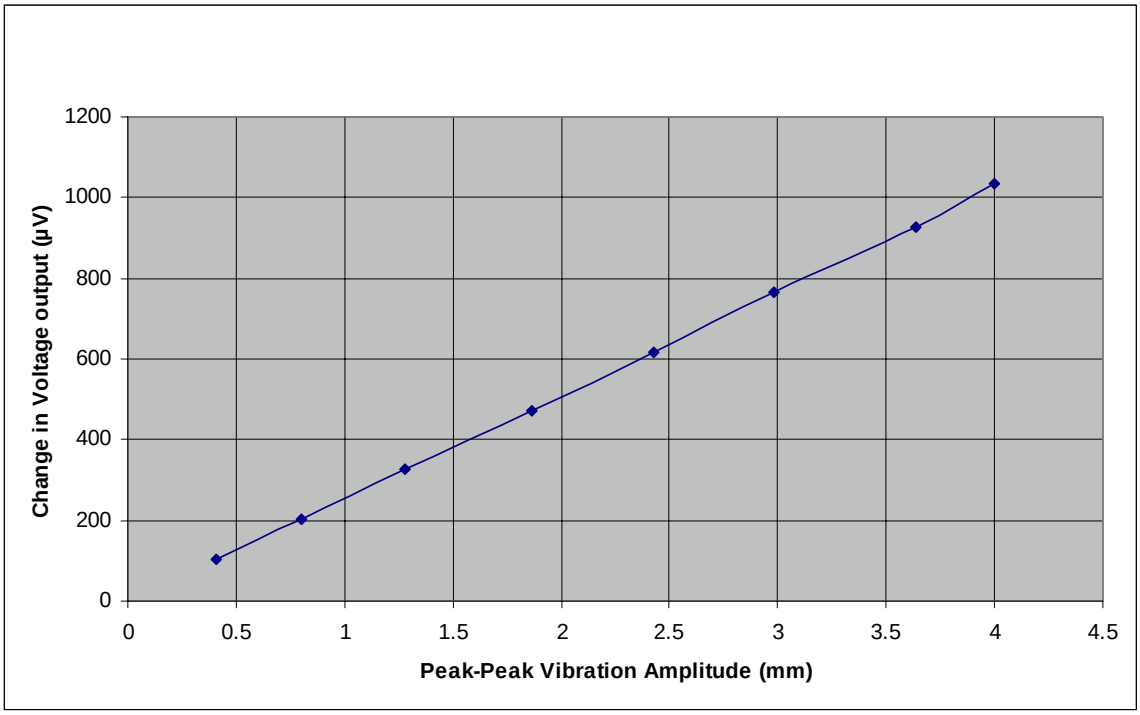


Figure 5.21 Voltage Change Plot at 50 Hz

Peak to Peak Vibration Amplitude(mm)	Change in Voltage Output (μVrms)	Change in Voltage Output (μV)
0.325	62	87.42
0.604	112	157.92
0.973	169	238.29
1.485	261	368.01
1.869	337	475.17
2.255	413	582.33
2.662	482	679.62
3.328	620	874.2

Table 5.13 Voltage Change Values at 70 Hz

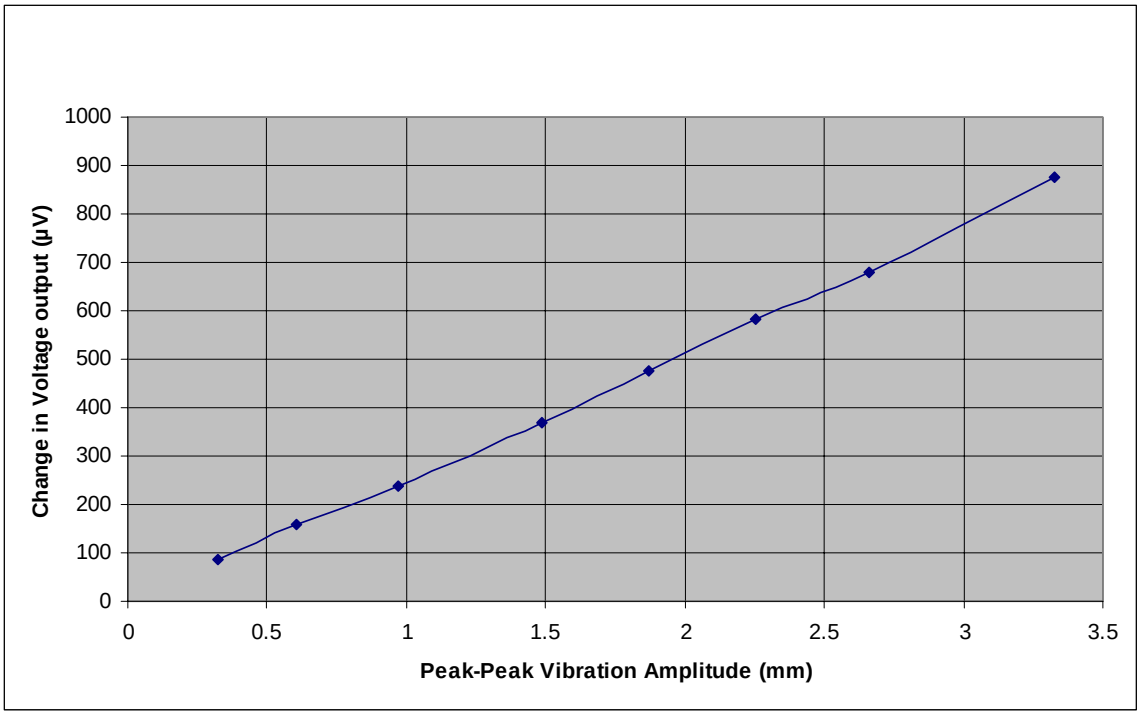


Figure 5.22 Voltage Change Plot at 70 Hz

Peak to Peak Vibration Amplitude(mm)	Change in Voltage Output (μVrms)	Change in Voltage Output (μV)
0.479	85	119.85
0.696	125	176.25
1.037	186	262.26
1.344	246	346.86
1.641	299	421.59
1.874	344	485.04
2.158	392	552.72
2.463	457	644.37

Table 5.14 Voltage Change Values at 80 Hz

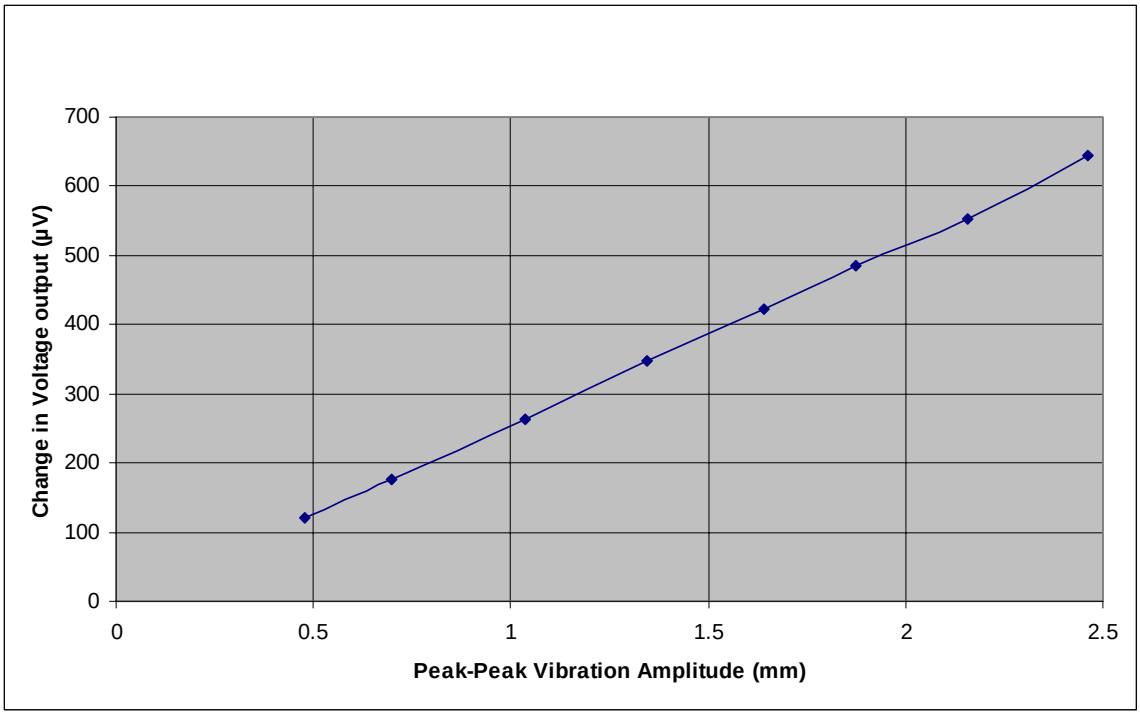


Figure 5.23 Voltage Change Plot at 80 Hz

Peak to Peak Vibration Amplitude(mm)	Change in Voltage Output (μVrms)	Change in Voltage Output (μV)
0.381	63	88.83
0.576	97	136.77
0.911	159	224.19
1.165	212	298.92
1.418	256	360.96
1.677	310	437.1
1.917	347	489.27

Table 5.15 Voltage Change Values at 90 Hz

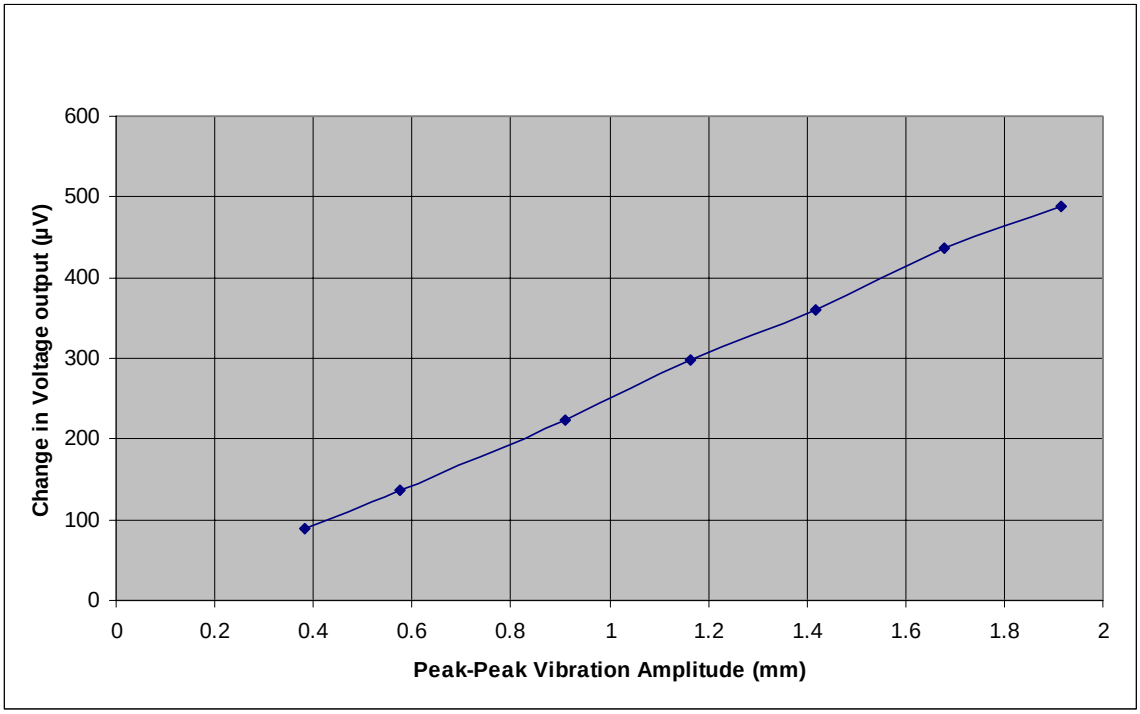


Figure 5.24 Voltage Change Plot at 90 Hz

Peak to Peak Vibration Amplitude(mm)	Change in Voltage Output (μVrms)	Change in Voltage Output (μV)
0.307	51	71.91
0.515	86	121.26
0.768	135	190.35
0.988	173	243.93
1.144	208	293.28
1.341	242	341.22
1.485	272	383.52

Table 5.16 Voltage Change Values at 100 Hz

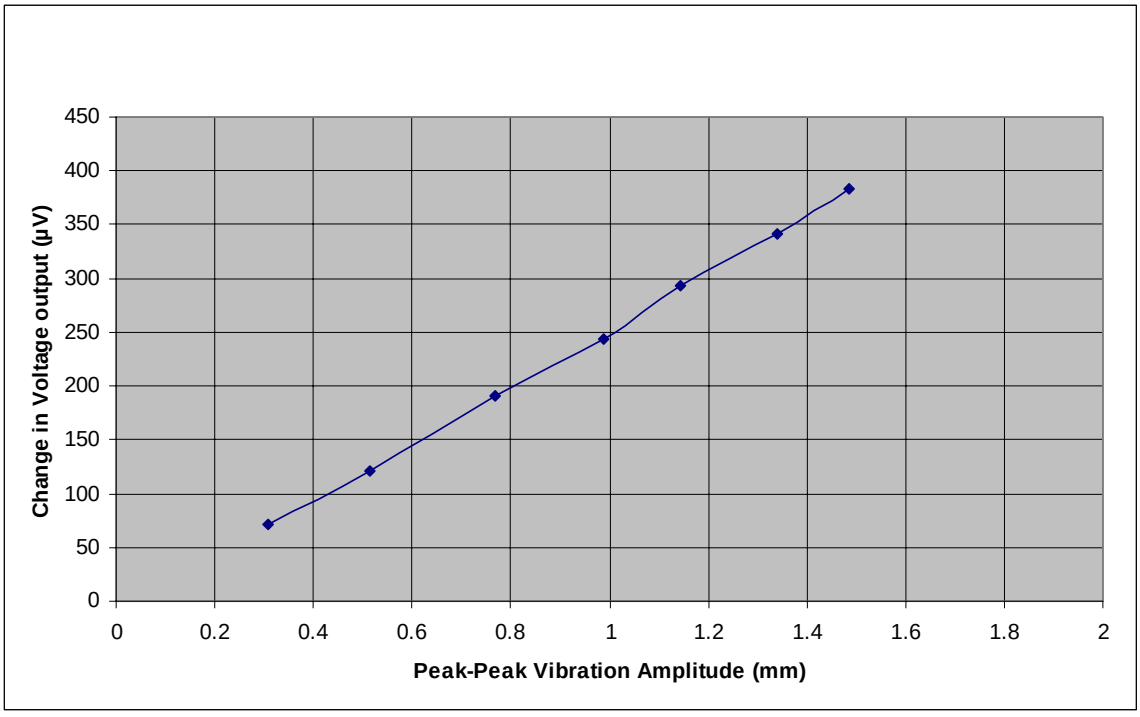


Figure 5.25 Voltage Change Plot at 100 Hz

Peak to Peak Vibration Amplitude(mm)	Change in Voltage Output (μVrms)	Change in Voltage Output (μV)
0.238	37	52.17
0.384	65	91.65
0.548	96	135.36
0.684	118	166.38
0.806	143	201.63
0.906	156	219.96

Table 5.17 Voltage Change Values at 125 Hz

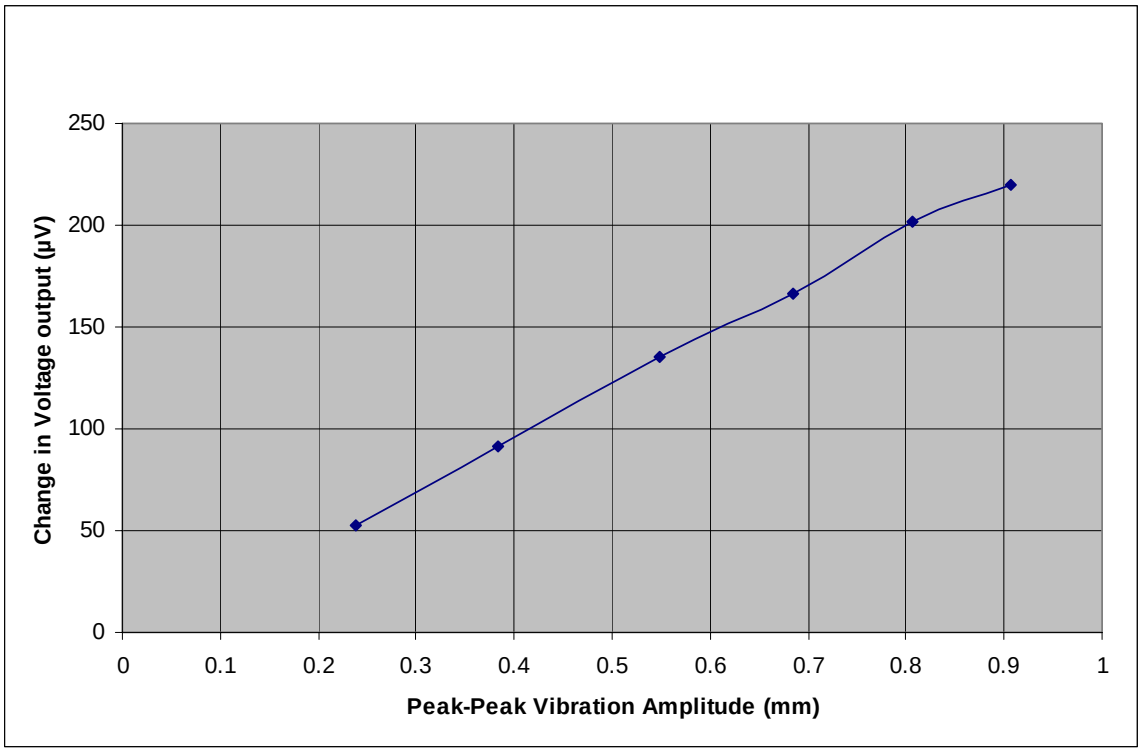


Figure 5.26 Voltage Change Plot at 125 Hz

Peak to Peak Vibration Amplitude(mm)	Change in Voltage Output (μVrms)	Change in Voltage Output (μV)
0.172	26	36.66
0.277	45	63.45
0.384	62	87.42
0.479	80	112.8
0.563	93	131.13
0.589	100	141

Table 5.18 Voltage Change Values at 150 Hz

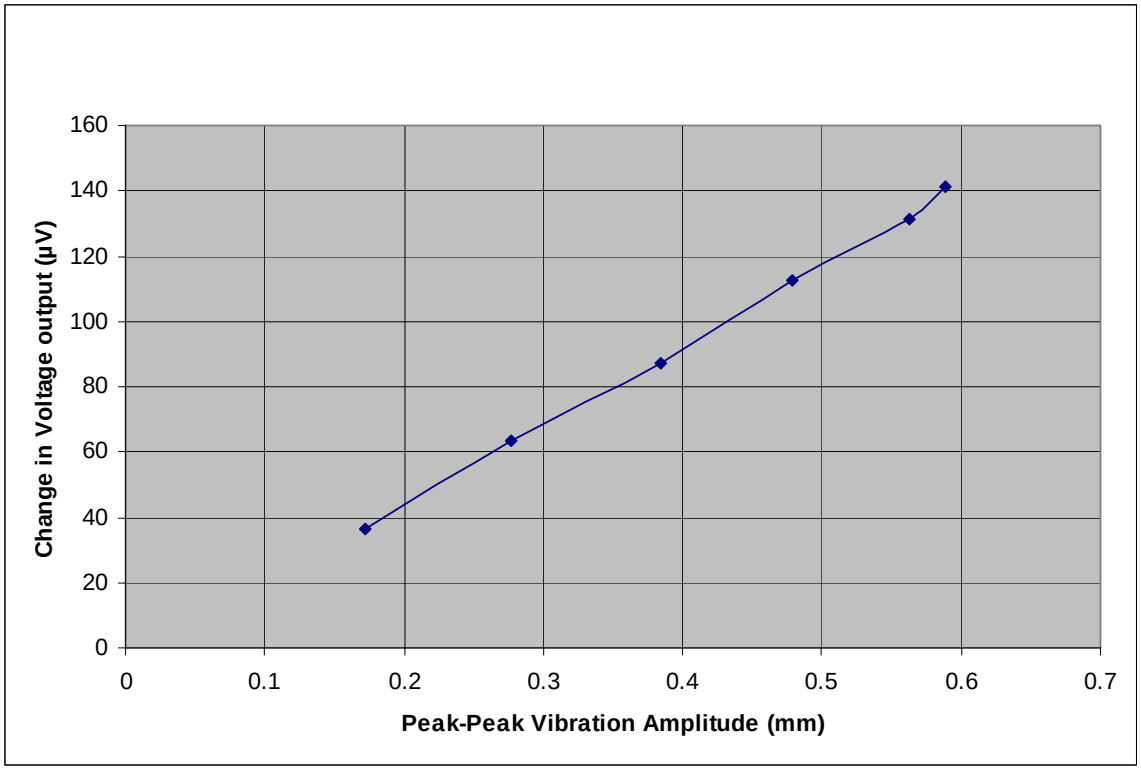


Figure 5.27 Voltage Change Plot at 150 Hz

Peak to Peak Vibration Amplitude(mm)	Change in Voltage Output (μVrms)	Change in Voltage Output (μV)
0.172	21	29.61
0.207	27	38.07
0.251	36	50.76
0307	44	62.04

Table 5.19 Voltage Change Values at 200 Hz

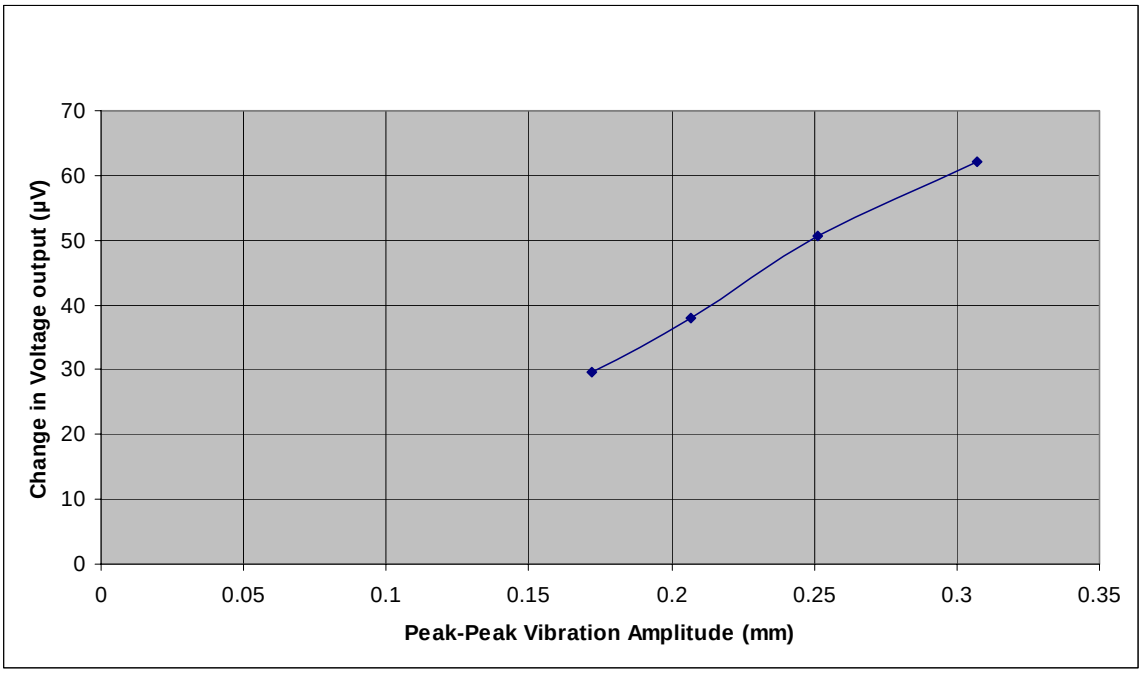


Figure 5.28 Voltage Change Plot at 200 Hz

Data points extracted from these response curves were combined with the results from static bending of the chip-on-board assembly on the shaker head to plot the frequency response of the test chip sensors. Comparison was made at 2 mm peak-to-peak vibration of the shaker head. A trend line was fitted to the individual response curves and its equation was used to extract the voltage change values at the given amplitude of vibration of the shaker head.

5.3 Beam Bending

Static tests were carried out by placing various weights on the shaker head thereby bending the test board. Voltage change values are shown in Table 5.20 and the corresponding plot is shown in Fig. 5.29.

As the set-up for beam bending is exactly the same for dynamic vibrations, its voltage change values correspond to the voltage change values of dynamic tests at 0Hz. However, a 2 mm peak-to-peak vibration in the dynamic tests represents 1 mm deflection of the shaker head in either direction and hence corresponds to 1 mm deflection in the static tests.

Shaker Head Deflection (mm)	Change in Voltage Output (μV)	Weight on Shaker Head (kgs)
0.218	150	0.213
0.67	360	0.702
0.96	525	1.000
1.382	712	1.414
1.715	822	1.797
2.086	940	2.116
2.624	1156	2.57
3.302	1368	3.211
3.482	1460	3.417
4.122	1687	3.984
4.403	1846	4.264

Table 5.20 Voltage Change Values for Beam Bending

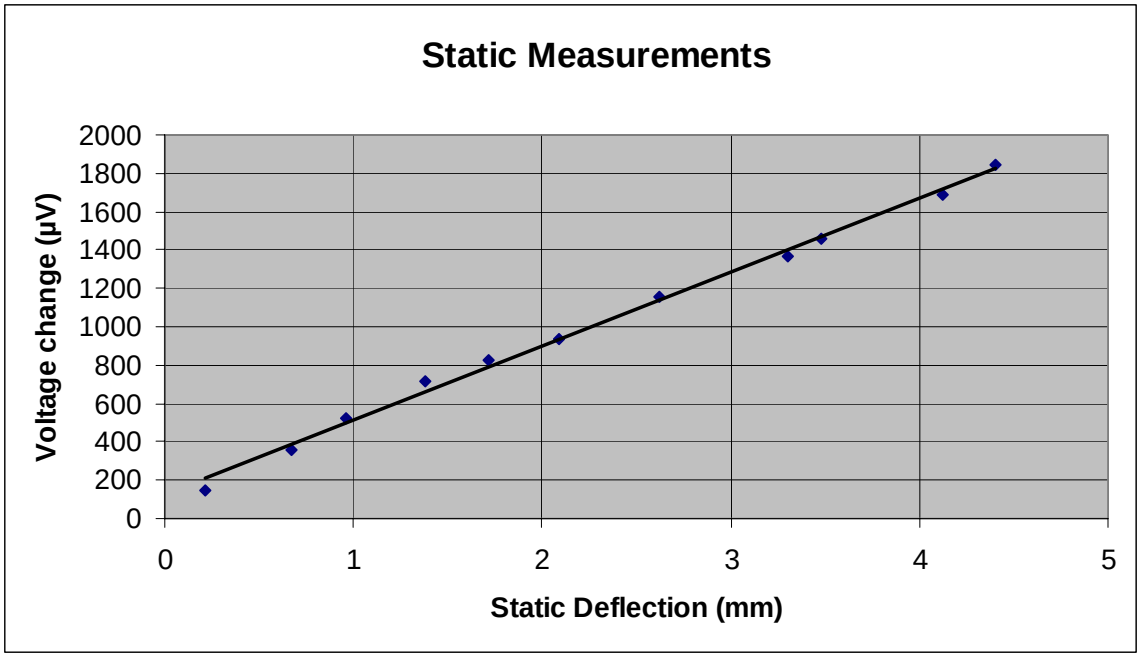


Figure 5.29 Voltage Change Plot for Beam Bending

5.4 Frequency Response Combining Static and Dynamic Test Results

The frequency response of the test chip stress sensors over a frequency range from 0 Hz to 200 Hz at 2 mm peak-to-peak deflection of the shaker head is shown in Fig. 5.30, and the corresponding voltage change values are shown in Table 5.21.

Vibration Frequency (Hz)	Change in Voltage Output (μV)
0	511.94
0.5	520.163
0.75	520.181
1	517.443
2	506.554
3	495.54
4	494.206
5	492.396
10	489.851
20	507.44
30	503.064
40	505.368
50	510.577
70	514.402
80	517.386
90	516.37
100	517.466
125	501.057
150	486.417
200	475.344

Table 5.21 Voltage Change values at 2 mm peak-to-peak vibration

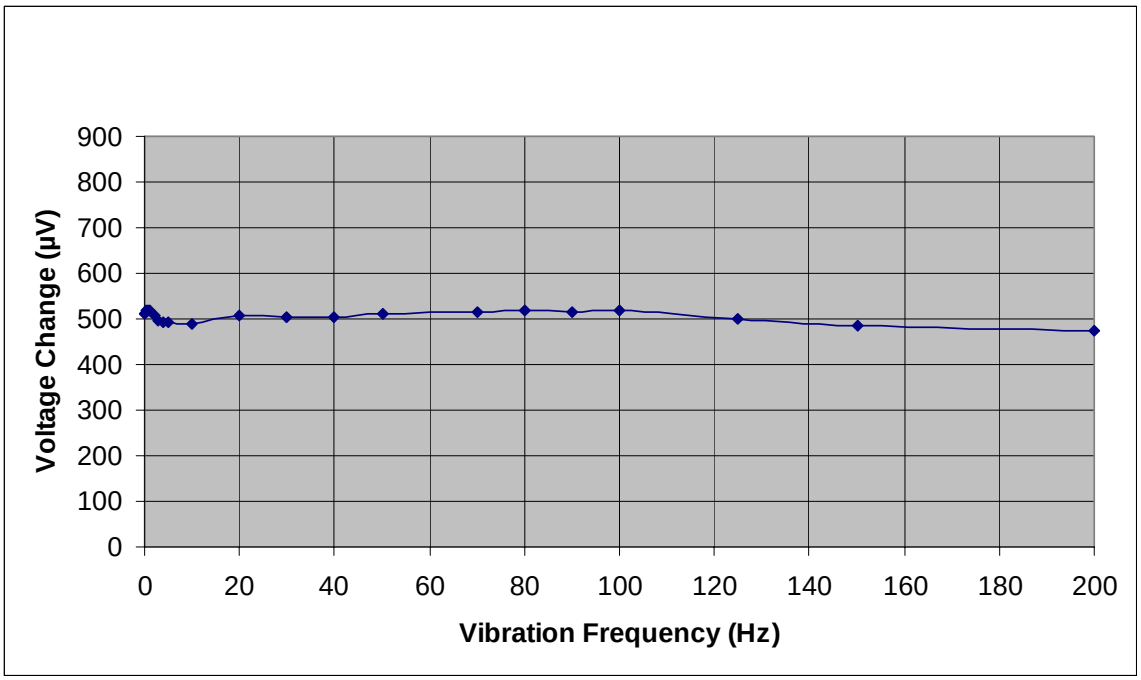


Figure 5.30 Frequency Response at 2 mm peak to peak Vibration

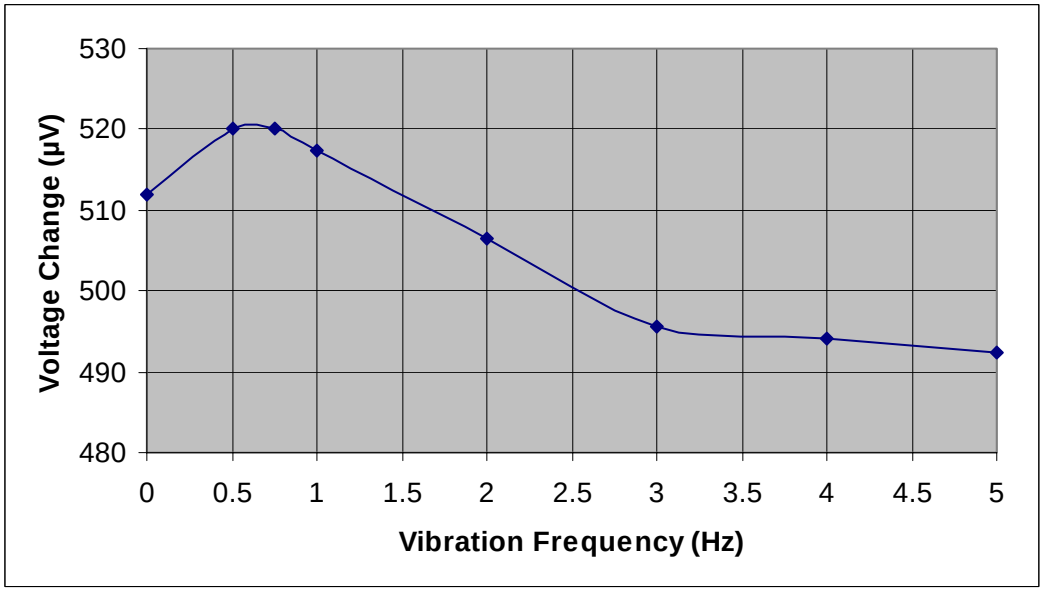


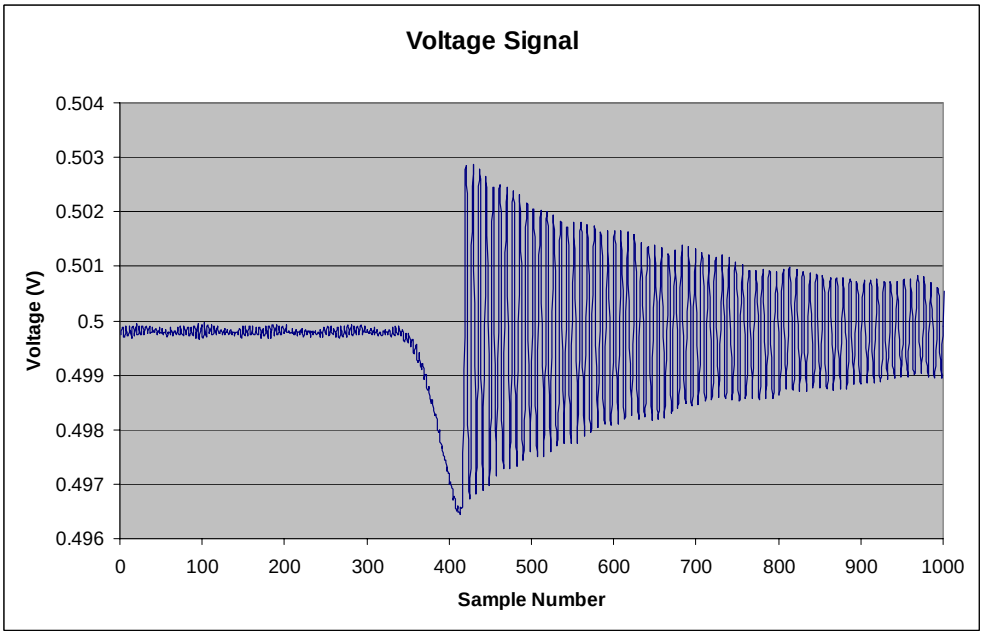
Figure 5.31 Frequency Response at Low Frequencies

As can be seen from the frequency response plot, the change in voltage output from the sensor, which is a measure of the stress developed on the test chip surface, is consistent over 0 Hz to 200 Hz and thus the sensor cut-off frequency is not reached. However, at low frequencies of up to 5 Hz, the change in voltage is not uniform which indicates the presence of additional stresses. This state of stress at low frequencies could be a result of underfill creeping, as the underfill material gets time to creep at low frequencies. At high frequencies, the beam gets bent in the other direction in a very short time and hence there is not enough time for the underfill to creep.

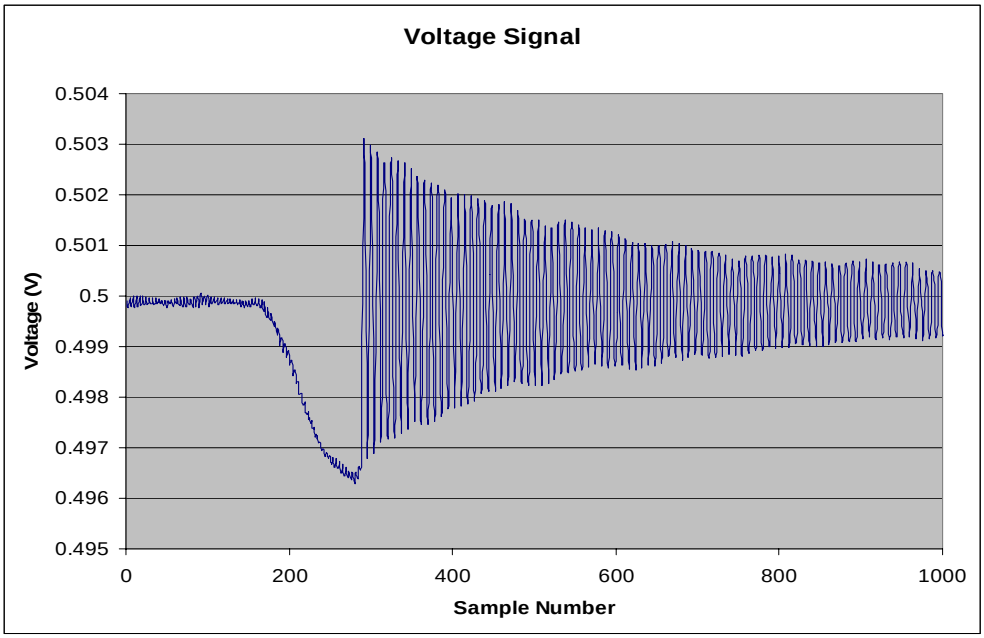
In order to verify this hypothesis of underfill creeping at low frequencies, the chip-on-board assembly was attached to a metal beam and held tightly on a pure cantilever beam fixture. Voltage output from the p-type resistor network was observed on a parameter analyzer while the beam was plucked and forced to vibrate at its natural frequency of 27 Hz.

As can be seen in Figs. 5.32 (a) and (b), the voltage output shows ideal decaying characteristics when free end of the beam is pushed down by a point load and released immediately. However, when the free end is held down by a point load for a small amount of time before being released, the voltage output starts decaying at a different level as can be seen in Figs. 5.33 (a) and (b). This happens because the underfill gets time to creep when the beam is held down by the load for some time, and thereby alters the stresses on the test chip.

Thus, when the beam is released immediately on the cantilever structure and when it is vibrated on the shaker system at high frequencies, the underfill does not get time to creep and the voltage output shows ideal characteristics.

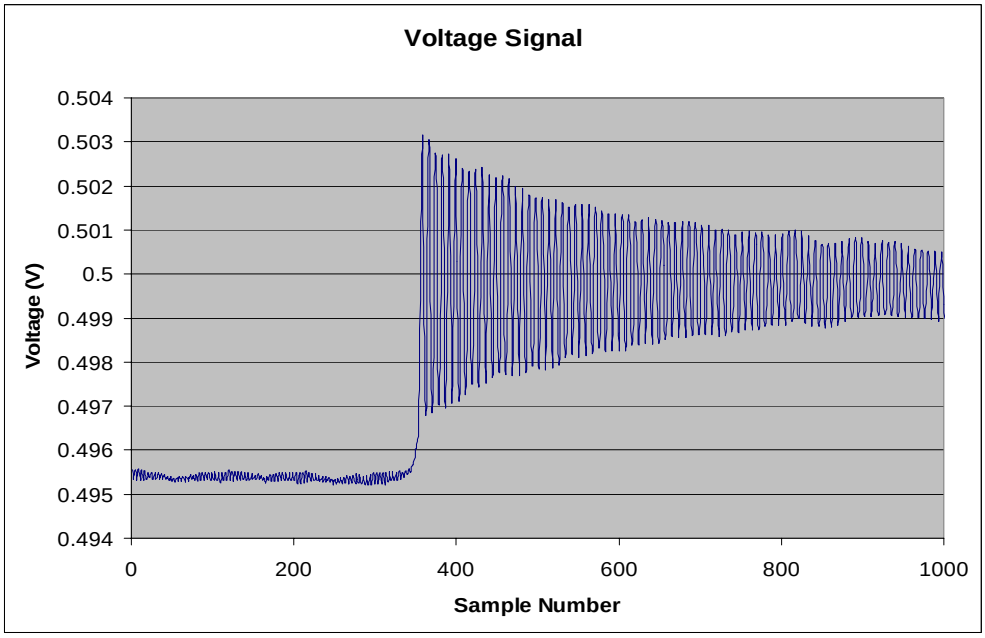


(a)

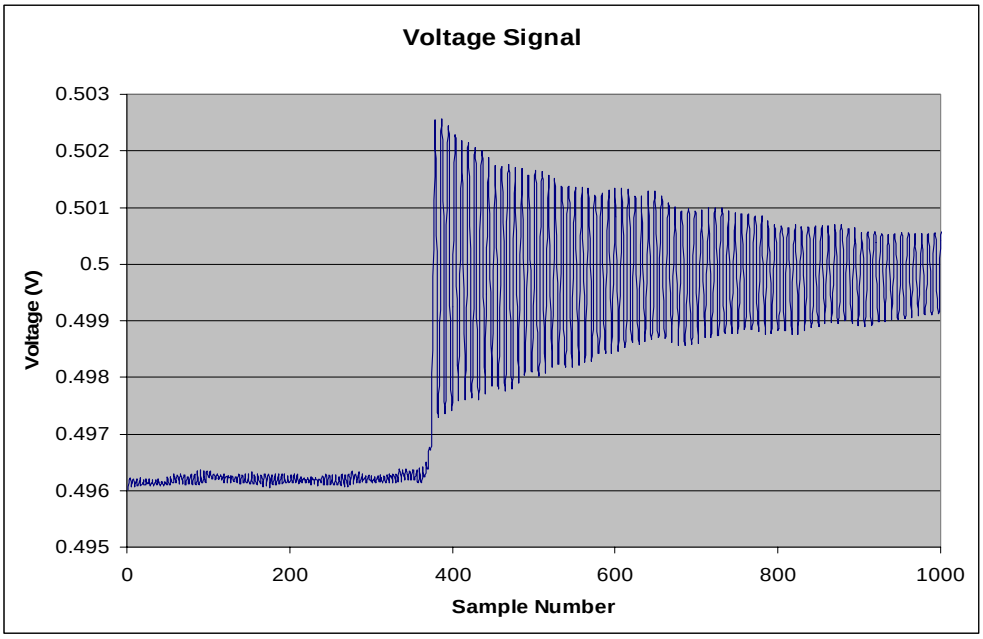


(b)

Figure 5.32 (a) and (b) Voltage Outputs when beam was plucked



(a)



(b)

Figure 5.33 (a) and (b) Voltage Outputs when beam was held down before release

5.5 Finite Element Analysis

ANSYS™ was used to perform the finite element analysis of the chip-on-board assembly. A fine mesh of the assembly was created as shown in Fig. 5.34 and boundary conditions were applied such that the finite element model represents chip-on-board assembly fixed on the shaker system.

Thickness values for the three elements used in model were as follows:

Silicon chip thickness = 0.650 mm

FR-4 board thickness = 0.583 mm

ME-525 underfill thickness = 0.029 mm

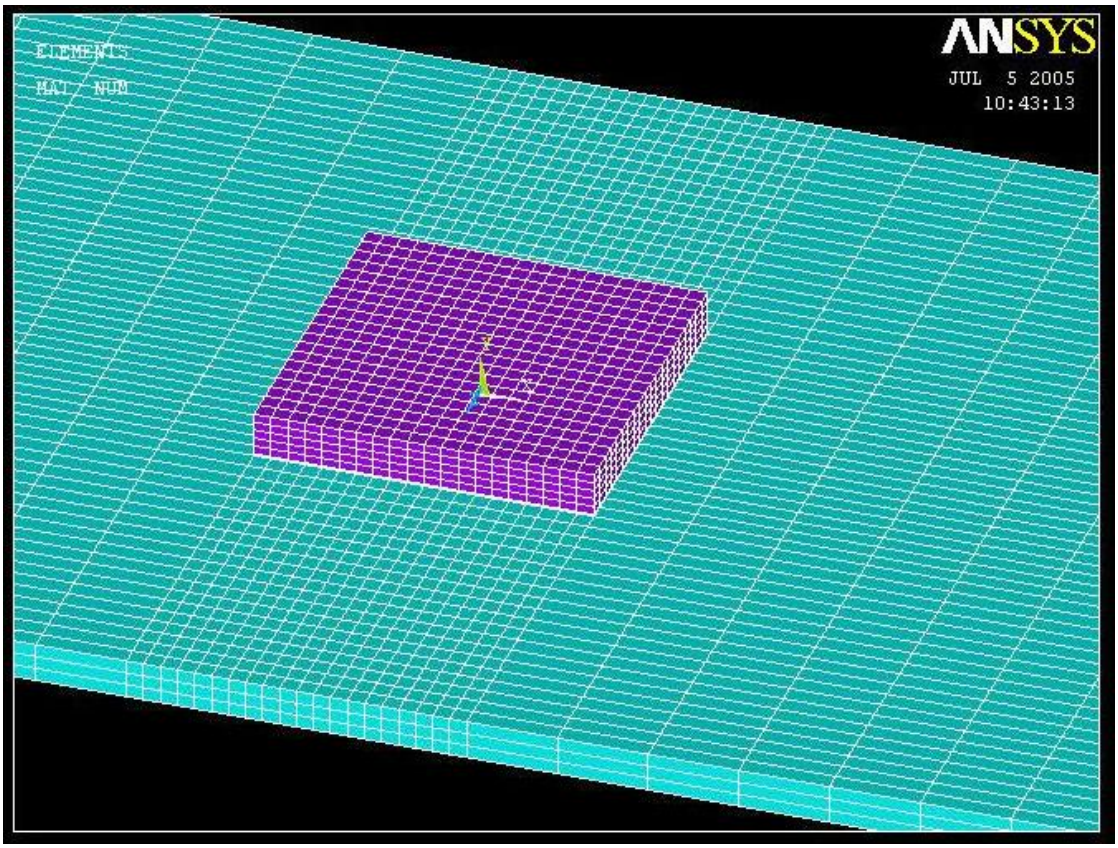


Figure 5.34 Mesh for the chip-on-board

Material properties for silicon chip, FR-4 board and ME-525 underfill used in the simulations are shown in Table 5.22.

	Young's Modulus	**Poisson's ratio**
Silicon	169 GPa	0.28
FR-4	20 GPa	0.35
ME-525	10.43 GPa	0.3

Table 5.22 Material Properties used in ANSYS^{TM} simulations

Simulations were carried out to determine various stresses developed on the chip surface when one end of the board was forced down by 1mm. Displacement of the assembly in vertical direction is shown in Figs. 5.35 and 5.36, while displacement of the chip is shown in Fig. 5.37. Stress distributions obtained from the ANSYS^{TM} simulations are shown in Fig. 5.38 to Fig. 5.43. The coordinate system in ANSYS^{TM} simulations is such that its X-axis lies along the length of the board, Y-axis is in the vertical direction, and Z-axis is along the width of the board.

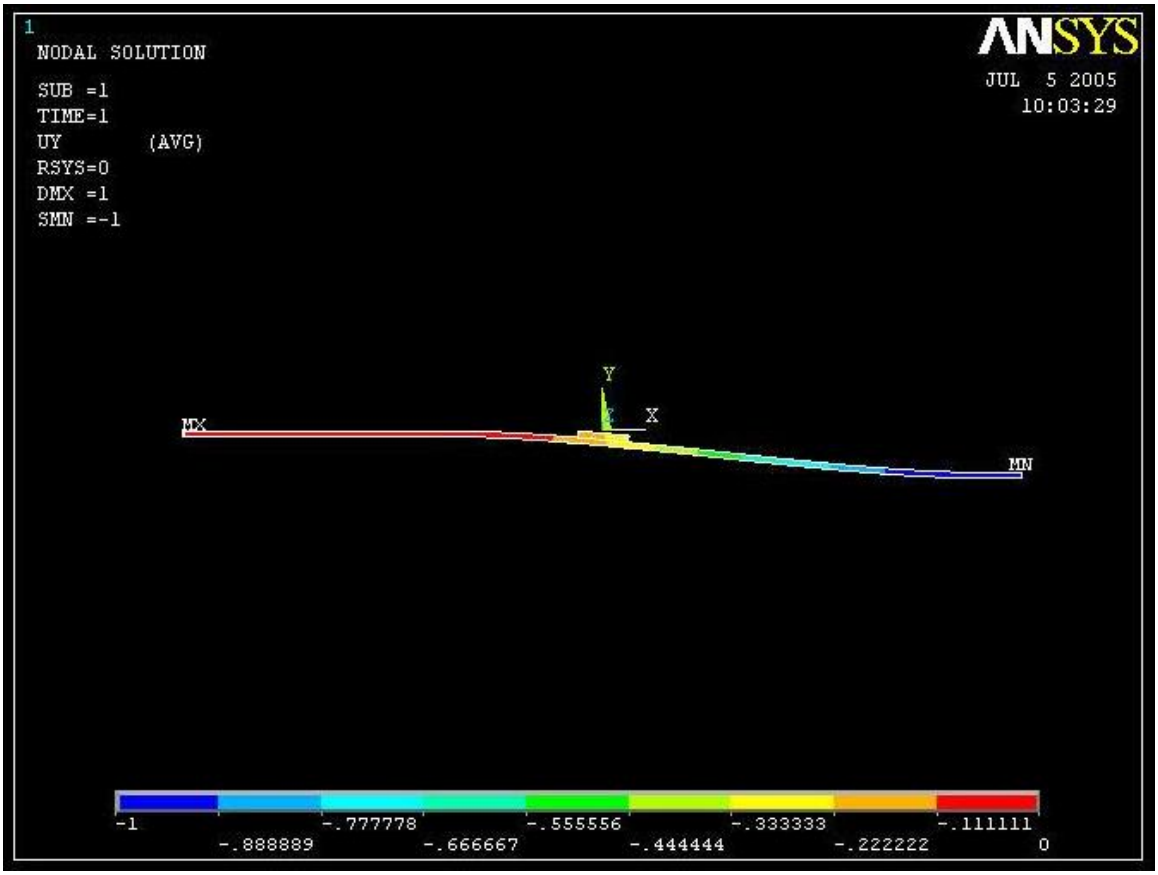


Figure 5.35 Displacement of the assembly in Y-direction

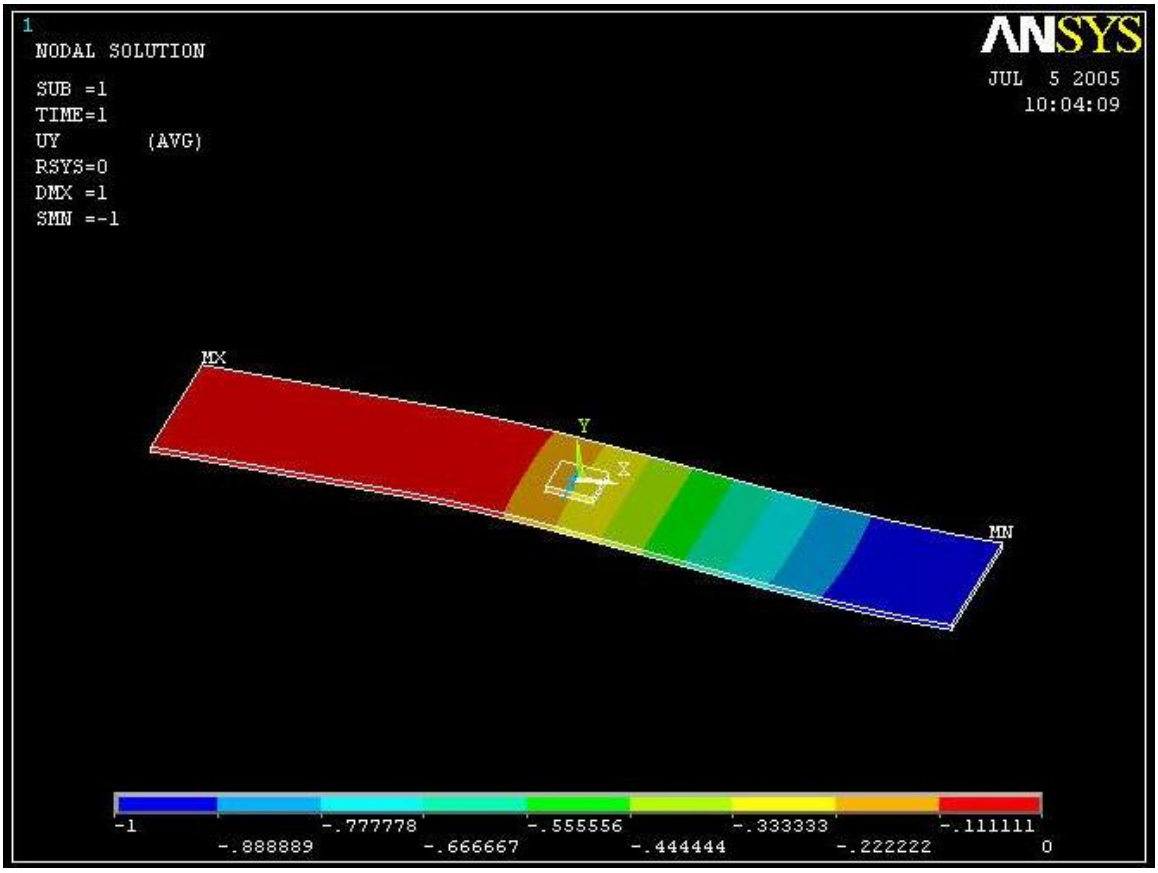


Figure 5.36 Oblique view of displacement of the assembly in Y-direction

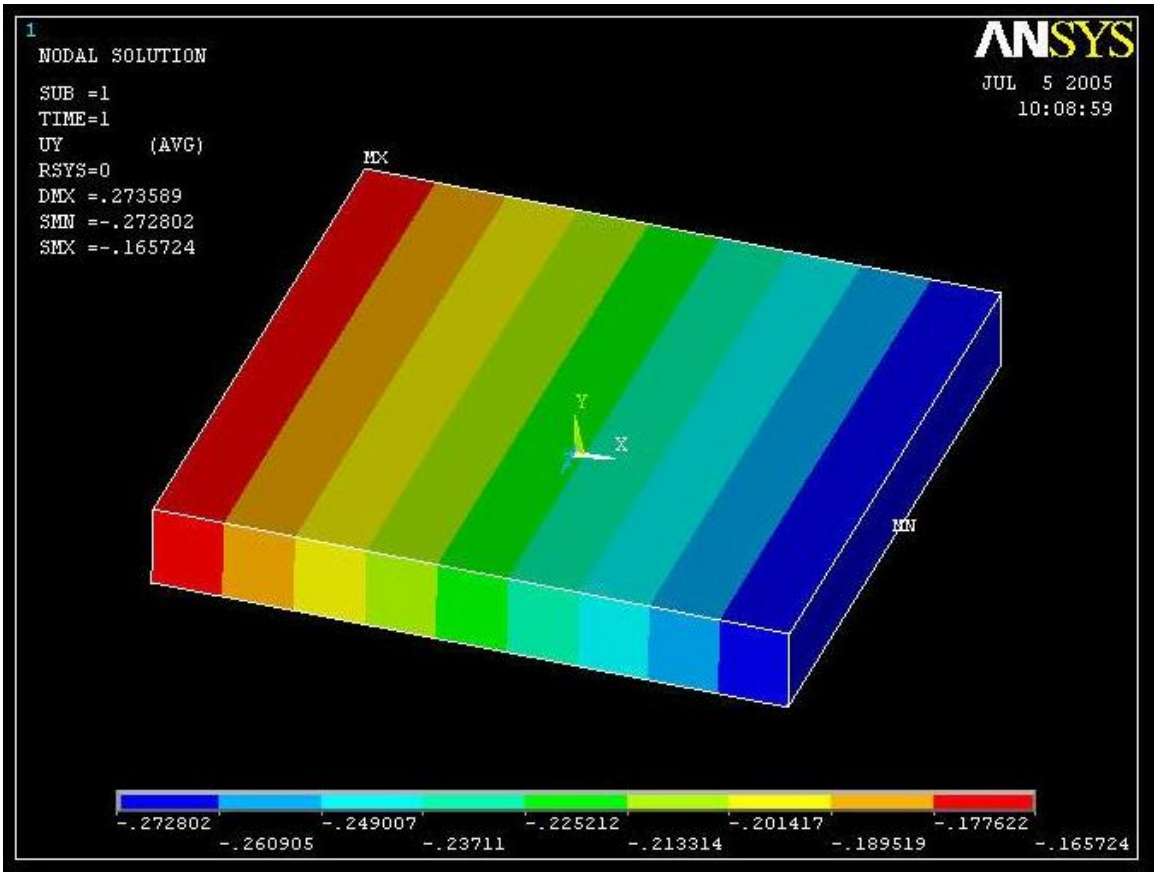


Figure 5.37 Displacement of the chip in Y-direction

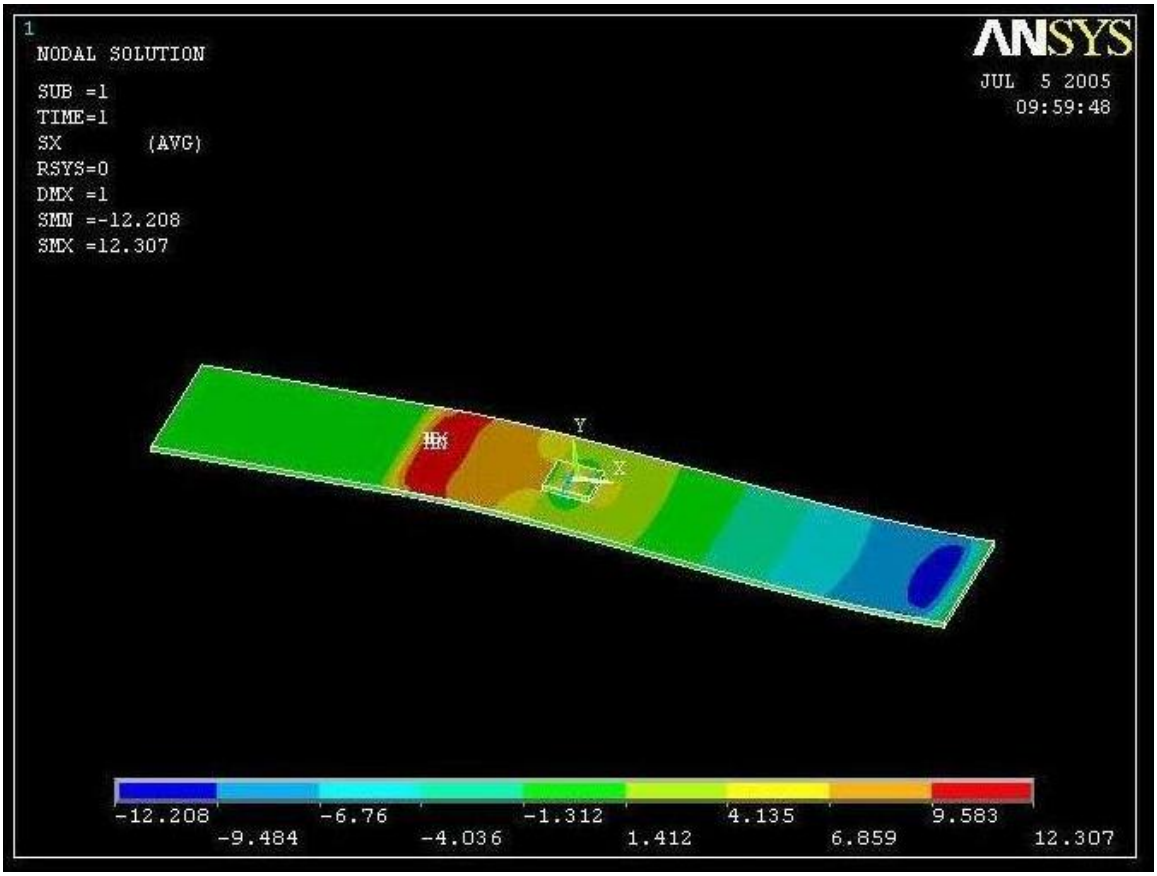


Figure 5.38 Stress distribution on the board in X-direction

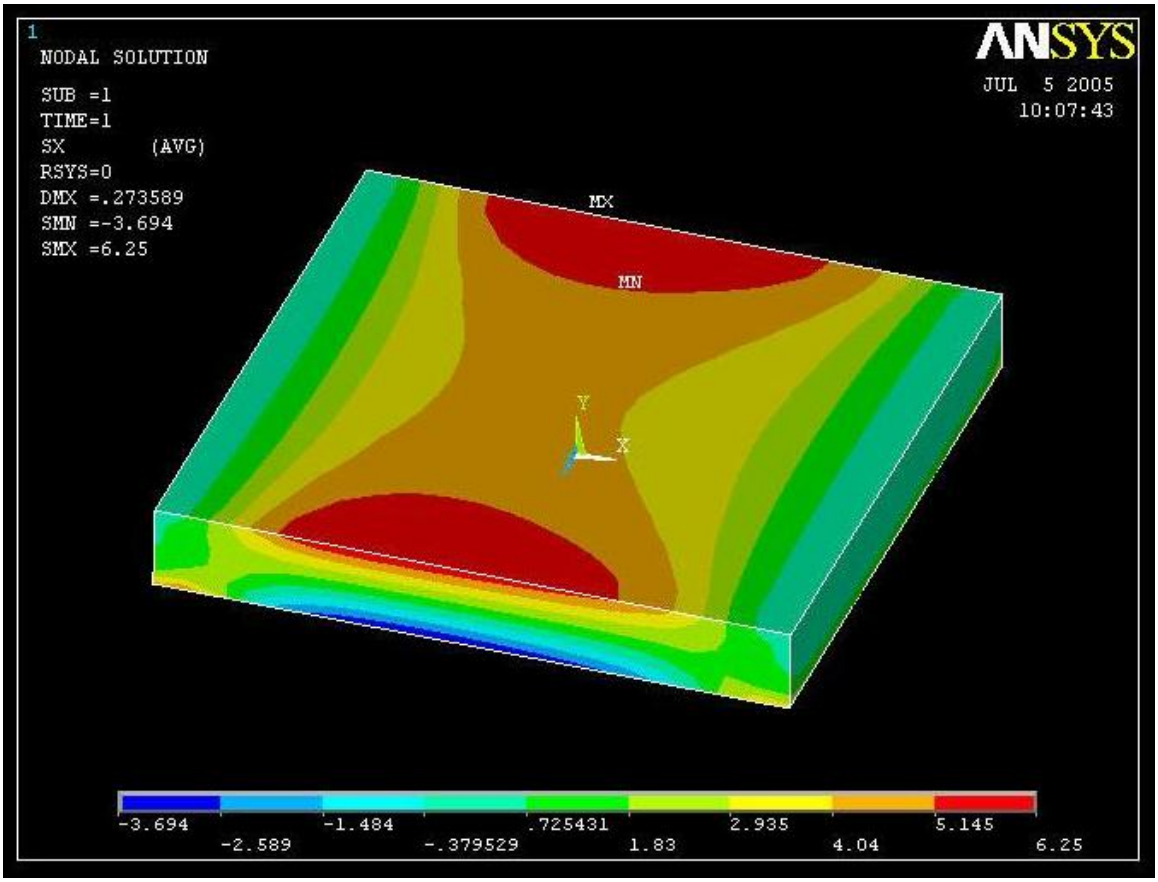


Figure 5.39 Stress distribution on the chip in X-direction

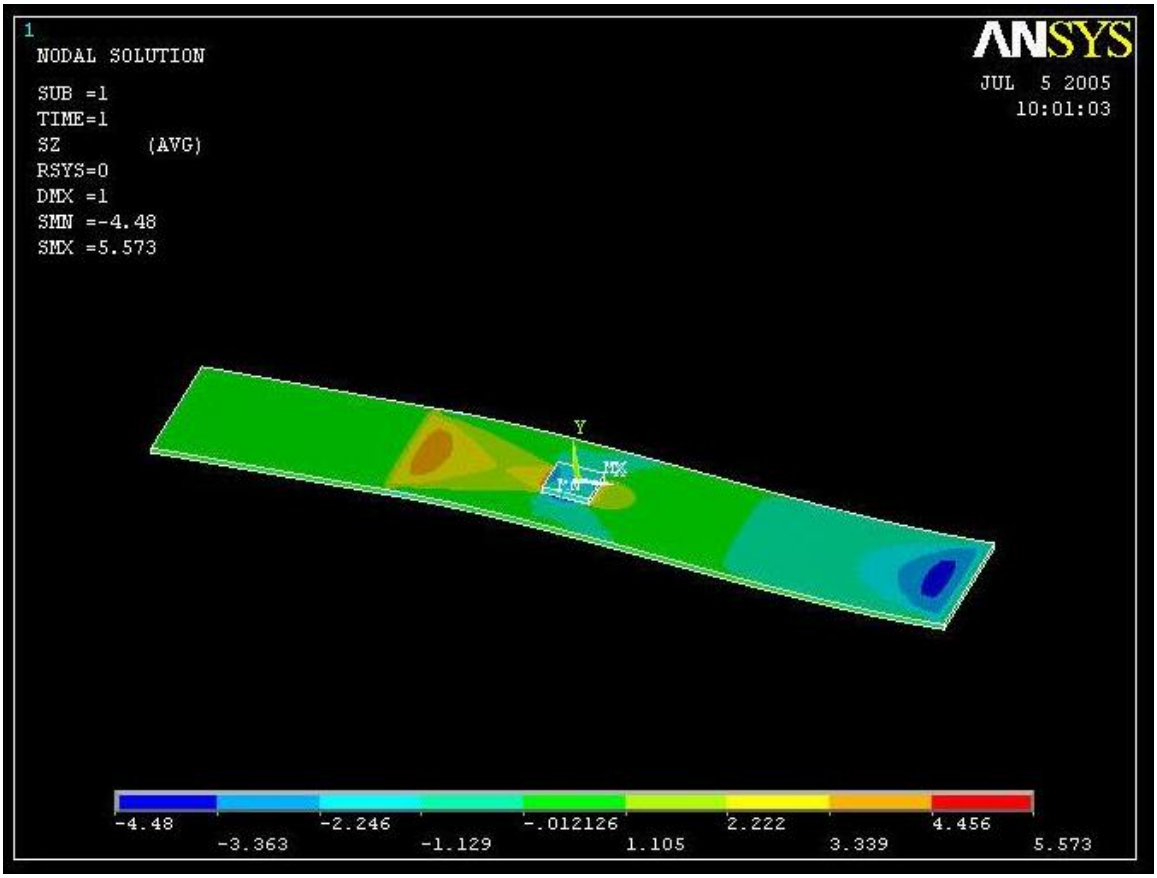


Figure 5.40 Stress distribution on the board in Z-direction

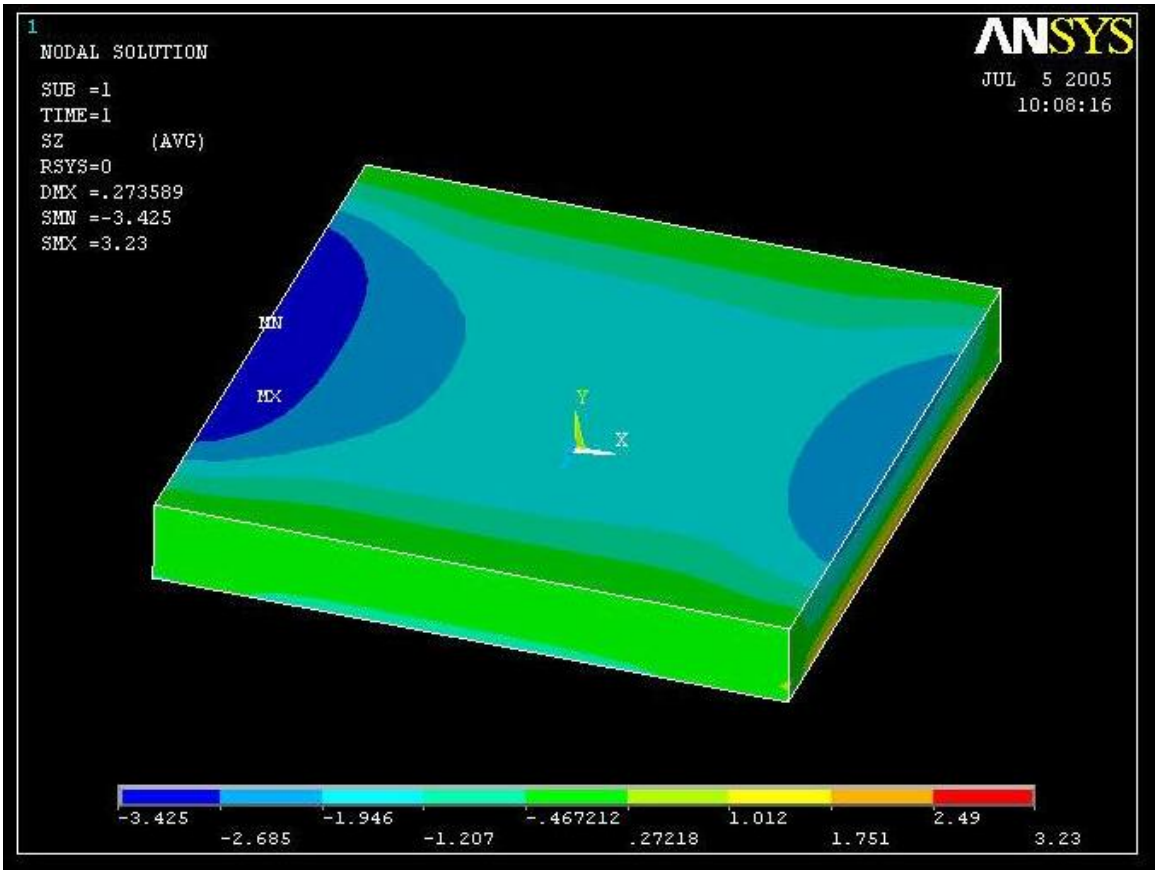


Figure 5.41 Stress distribution on the chip in Z-direction

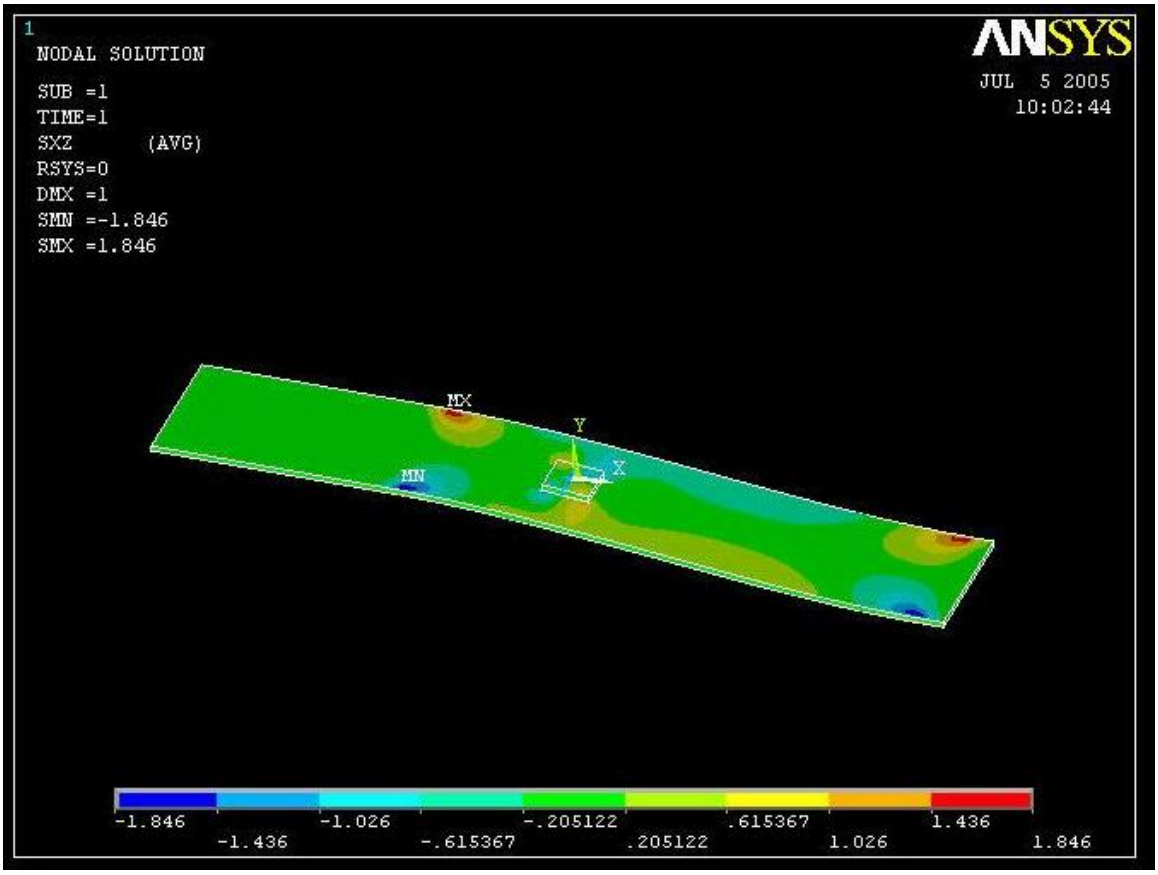


Figure 5.42 Shear Stress distribution on the board in XZ-direction

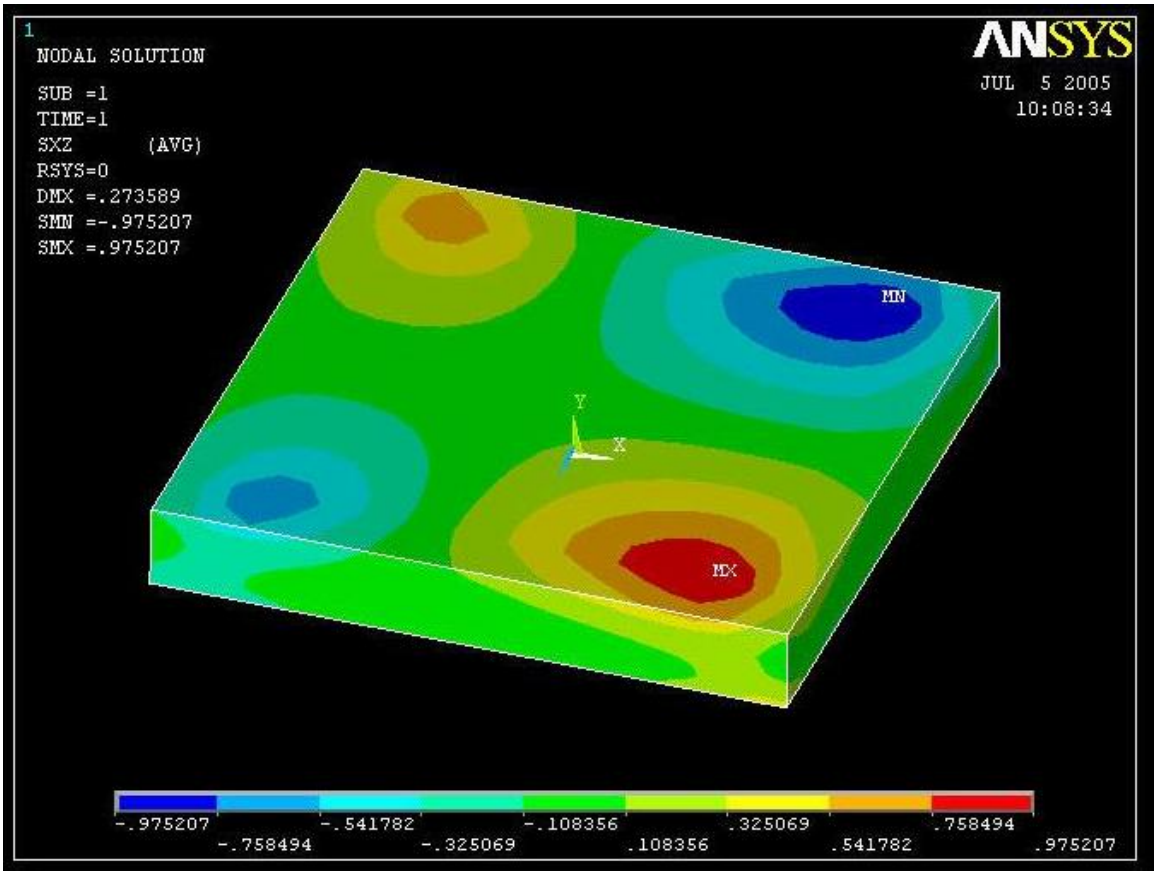
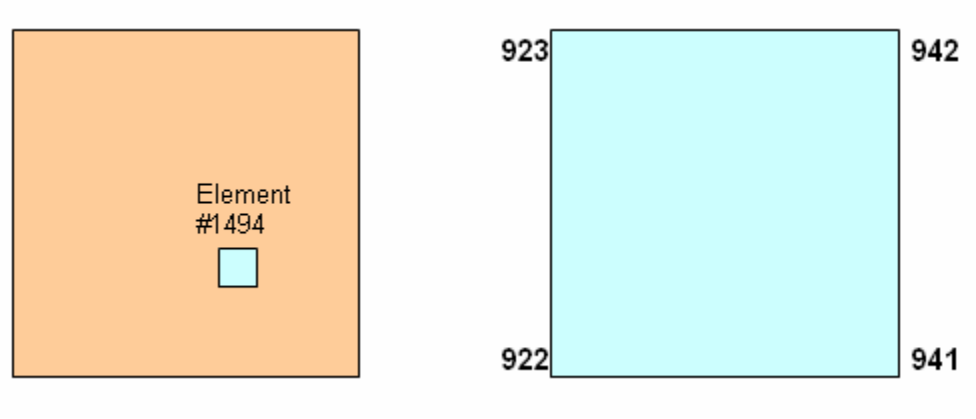


Figure 5.43 Shear Stress distribution on the chip in XZ-direction

Size of each element in the finite element model in ANSYS^{TM} is 0.25 mm × 0.25 mm, whereas the size of the p-resistor network on the test chip used to measure voltage values during tests carried out on the shaker system is 0.14 mm × 0.28 mm. Therefore, values from only one element in the finite element model are extracted. Location of this element in the model which corresponds to the location of the p-resistor on the test chip was determined. Stress values at the four nodes of this element (number 1494) shown in Fig. 5.44 were extracted from ANSYS^{TM}.



(a) JSE Chip **(b) Element #1494**

Figure 5.44 (a) and (b) Mapping of p-resistor with its corresponding element

Stress values extracted from ANSYS^{TM} are shown in Table 5.23. The average value of each stress component is calculated and used to determine the change in resistance due to these stresses developed by beam bending.

	S_X ($\sigma 22$)	S_Y ($\sigma 33$)	S_Z ($\sigma 11$)	S_{XY} ($\sigma 23$)	S_{YZ} ($\sigma 13$)	S_{XZ} ($\sigma 12$)
922	4.277	3.159e-3	-1.501	-3.033e-2	4.401e-2	0.477
923	4.095	-1.737e-3	-1.582	-2.802e-2	2.578e-2	0.377
941	4.002	-0.478e-3	-1.46	-4.393e-2	4.193e-2	0.551
942	3.834	-4.6e-3	-1.549	-4.087e-2	2.461e-2	0.431
Average	4.052	-0.914e-3	-1.523	-3.579e-2	3.408e-2	0.459

Table 5.23 Stress values at the four nodes of element #1494

The average stress values are substituted in the resistance change equations for the p-type resistors mentioned in chapter two. Change in resistance of p0 resistor is given by

$$\frac{\Delta R_5}{R_5} = B_1^p \sigma'_{11} + B_2^p \sigma'_{22} + B_3^p \sigma'_{33} + 2\sqrt{2}\left(B_3^p - B_2^p\right)\sigma'_{23} + \left[\alpha_1^p T + \alpha_2^p T^2 + \ldots\right]$$

while that of p90 resistor is given by

$$\frac{\Delta R_7}{R_7} = B_2^p \sigma'_{11} + B_1^p \sigma'_{22} + B_3^p \sigma'_{33} - 2\sqrt{2}\left(B_3^p - B_2^p\right)\sigma'_{23} + \left[\alpha_1^p T + \alpha_2^p T^2 + \ldots\right]$$

Here, the change in temperature is neglected and the values for the combined piezoresistive coefficients are

$B_1 = 387$

$B_2 = -92$

$B_3 = -453$

Taking resistance values for R_5 and R_7 as 10.3 kΩ and solving for ΔR_5 and ΔR_7, we get

$$\Delta R_5 = -0.000925315 \times 10.3K\Omega = -9.53\Omega$$

$$\Delta R_7 = 0.001672135 \times 10.3K\Omega = 17.22\Omega$$

Thus, after bending one end of the board by 1 mm, the new resistance values are

$p0 = R_5 = 10290.47\,\Omega$

$p90 = R_7 = 10317.22\,\Omega$

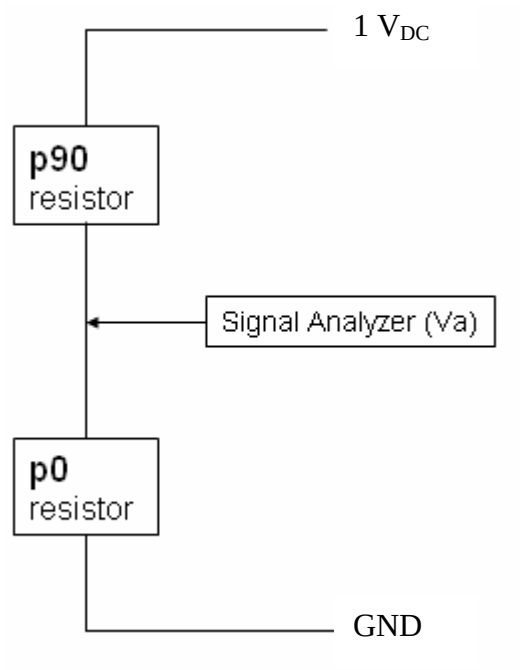


Figure 5.45 Resistor Network

As seen in the resistor network shown in Fig. 5.45, current flowing through the two resistors is given by

$$I = \frac{V_{DC}}{p_{90} + p_0} = \frac{1}{10290.47 + 10317.22} = 48.526\mu A$$

Voltage measured at the center terminal by the signal analyzer would be

$$V_a = I \times p_0 = 48.526 \times 10^{-6} \times 10290.47 = 499.355mV$$

Therefore, at 1mm deflection of one end of the board, change in voltage output at the center terminal according to the ANSYS^{TM} simulations would be

$$V = 500mV - 499.355mV = 645\mu V$$

Change in voltage output at the center terminal when the shaker head was displaced by 1 mm in the static tests was 512 μV . Thus, the experimental value is close to the simulation value having an error of 20 per cent.

Chapter 6

SUMMARY & CONCLUSION

In this work, vibration analysis of the WB200 test chip containing an array of optimized piezoresistive stress sensor rosettes has been performed. ME525 underfill material is used for die attachment. Various underfill layout patterns were tried with varying machine parameters and best results were obtained using one underfill dot in the center and four dots near the four corners. Also, in order to avoid formation of voids in the underfill layer, dehydration of boards before dispensing underfill on them is suggested. Cross-sections of the chip-on-board assembly were observed under microscope to determine thickness values of the three elements.

Junction capacitances in the test chip form a RC network with the piezoresistances, which defines the electrical cut-off frequency of the stress sensors. Capacitance values were measured on a LCR meter, which matched well with the values calculated analytically. These values were used to simulate the RC network in SPICE, the results of which were analyzed to obtain the cut-off frequency value of 28 MHz. Thus, as expected, the electrical cut-off frequency of the sensors is found out to be relatively high and should not be a cause of concern for the vibration tests.

Test chip-on-board was mounted on a shaker system to perform bending and vibration tests. A finite element model of the chip-on-board system was built in ANSYS^{TM} and simulation results were compared with the static bending tests on the shaker head. For 1mm deflection of one end of the board and the other end being fixed, the finite element simulations predicted a normal stress value of 4.059 MPa at the sensor location on the test chip. The finite element predictions were found to be adequate when they were compared with the actual values obtained from the static bending tests. Sinusoidal vibrations of the chip-on-board system were performed at various frequencies over a range of 0 Hz to 200 Hz. The sensor output was compared at a peak-to-peak deflection of 2 mm of the shaker head. The frequency response plot thus obtained showed a steady line indicating that the cut-off frequency is beyond 200 Hz. However, at low frequencies the sensor output showed the presence of additional stresses. In order to analyze this behavior at low frequency, the chip-on-board assembly was attached to a metal beam and held tightly on a pure cantilever beam fixture. After analyzing results from bending and vibration tests on this fixture, it was inferred that the underfill was creeping at low frequencies and was the cause for additional stresses.

Sinusoidal vibrations on the shaker system were limited to a frequency of 200 Hz as the shaker head displacement at higher frequencies was too small to produce any significant output from the stress sensors. There are several opportunities for future work on the WB200 test chip. Inclusion of a Lock-In amplifier in the shaker system electronics may help in extracting sensor output at frequencies higher than 200 Hz as the amplifier will lock-in to the vibration frequency and amplify only the sensor output at that frequency.

The test chip-on-board assembly can be vibrated on a different shaker system which can produce high shaker head displacements at high frequencies. Finally, the test chip can be mounted on a specially designed board for performing drop tests.

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