Advanced SiO_2/SiC Interface Passivation

by

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Abstract

Silicon carbide is a wide band semiconductor with high critical field E_C (~ x7 Si) and excellent thermal conductivity (~ x3 Si). These properties make SiC a good candidate for power switching applications. The Baliga figure of merit for high power operation is almost 400 times greater for 4H-SiC than for Si. Silicon carbide is the only wide band gap semiconductor that has a native oxide, and, as such, is a leading candidate for the development of next-generation, energy efficient power MOSFETs (metal-oxide-semiconductor field effect transistors). This implies that the current silicon MOS device technology can be adopted for SiC MOS device fabrication without much effort in the development of new processing methods.

The 4H polytype of SiC has a wider band gap and higher, more isotropic bulk mobility and is preferred for MOSFET fabrication. However, the wider band gap is accompanied by a high defect density at the SiO_2/4H-SiC interface. The best passivation process for these traps is currently a post-oxidation anneal in NO or NO followed by a H_2. These anneals introduce nitrogen and hydrogen and reduce the trap density near the 4H-SiC conduction band edge by an order of magnitude to around $10^{12}eV^{-1}cm^{-2}$ (compared to 10^{10}-$10^{11}cm^{-2}eV^{-1}$ for the SiO_2/Si interface passivated with H_2). Nitric oxide and NO + H_2 passivations produce mobilities of 40-50$cm^2/V\text{-}s^2$ by removing electrically active dangling bonds, oxygen vacancies and carbon clusters at the interface. But this mobility value is 5% of the bulk mobility of SiC.

In this research, two advanced passivation techniques are applied, in order to obtain better understanding of the interface properties and achieve improved electrical

characteristics – Phosphorus (P) passivation and Nitrogen plasma (N2P) passivation. In addition to these passivation processes the concept of "low carbon" MOSFET fabrication has been proposed. Less carbon liberation during oxidation may reduce the number of mobility-degrading carbon-related defects at the oxide-semiconductor interface and/or in the near-surface channel region of the SiC.

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CHAPTER 1

Introduction

1.1 Progress in semiconductor devices

The first solid state amplifier was fabricated using germanium (Ge) which was seen as the semiconductor material of the future. But later on, silicon (Si) turned out to be more suitable for several reasons [1,2,3,4]. Silica, the source of Si is widely available, and it is easier to get high purity Si from it. Si can easily be doped to produce n-type, p-type and semi-insulating material [5]. Another very important reason is that a native oxide SiO_2 can be formed on Si using thermal oxidation at the relatively low temperature of around 900°C [6,7,8]. These characteristics make Si semiconductor industry favorite.

At present, our national semiconductor industry total is more than $290 billion [9]. Around 10% of this worth is in smart integrated circuits and electronic power devices [10,11]. More than 50% of our electricity is conditioned by electronic power devices [12,13]. These devices are important because they determine the cost and efficiency of electronic systems. Hence they have a greater impact on the economy of a country. The arrival in the 1950s of solid state devices like the bipolar transistor led to the replacement of vacuum tubes [13,14], and these improvements made possible the Second Electronic Revolution with silicon as the material of choice. Power devices had an important place in this revolution. During the 1970s, there were bipolar devices with blocking voltage capacity of 500V and high current capabilities. Also in 1970, International Rectifier Inc. launched the first metal-oxide-field effect transistor (MOSFET) [15]. The idea was to replace bipolar devices with MOSFETs for high power use. The MOSFET is a unipolar device and thus has a high switching speed. The MOSFET is also a voltage controlled device where the junction transistor is a current controlled device. Higher switching speed means operation at higher frequency where other

system components such as inductors can be made smaller, and voltage control instead of current control means less internal energy loss in the device.

1.1.2 Need of wide band gap semiconductor devices

In order to save energy on the national electric power grid, the idea of redesigned 'micro-grids' has been proposed [16,17]. For this we need power devices which can operate at higher switching speeds and block voltages of up to 20kV [18]. A potential solution for this problem is to employ power devices fabricated using a wide band gap semiconductor material such as silicon carbide [19]. For a power device, the Baliga figure of merit (BFOM) [20] is given by

$$BFOM = \mu_N \varepsilon_S E_C^3$$

μ_N = bulk mobility of SiC

ε_S = permittivity of SiC

E_C = critical electric field of breakdown for SiC

The higher the BFOM, the more suitable the semiconductor for high power operation.

1.2 Diode and transistor

In power electronics, we need both a rectifier and a transistor [13,21]. The characteristics of an ideal rectifier and a transistor are shown in figures 1.1(a) and (b). For an ideal rectifier, there is no voltage drop in on state and no current flows while the diode is not conducting (off state). So there is no power loss during operation. Similarly, in the case of an ideal transistor, there is no power dissipation in the on/off states. Figure 1 shows that the transition from the on to off state is instantaneous, meaning there is no power loss during switching. The

waveforms of an ideal power switching system are shown in figures 1.2(a) and (b). For an ideal switch, there is a zero voltage drop in on state. In the off state there is no leakage current, and again there is no power loss. But in reality, this is not the case, and the characteristics of a non-ideal rectifier / transistor are shown in figures 1.3(a), (b) and the

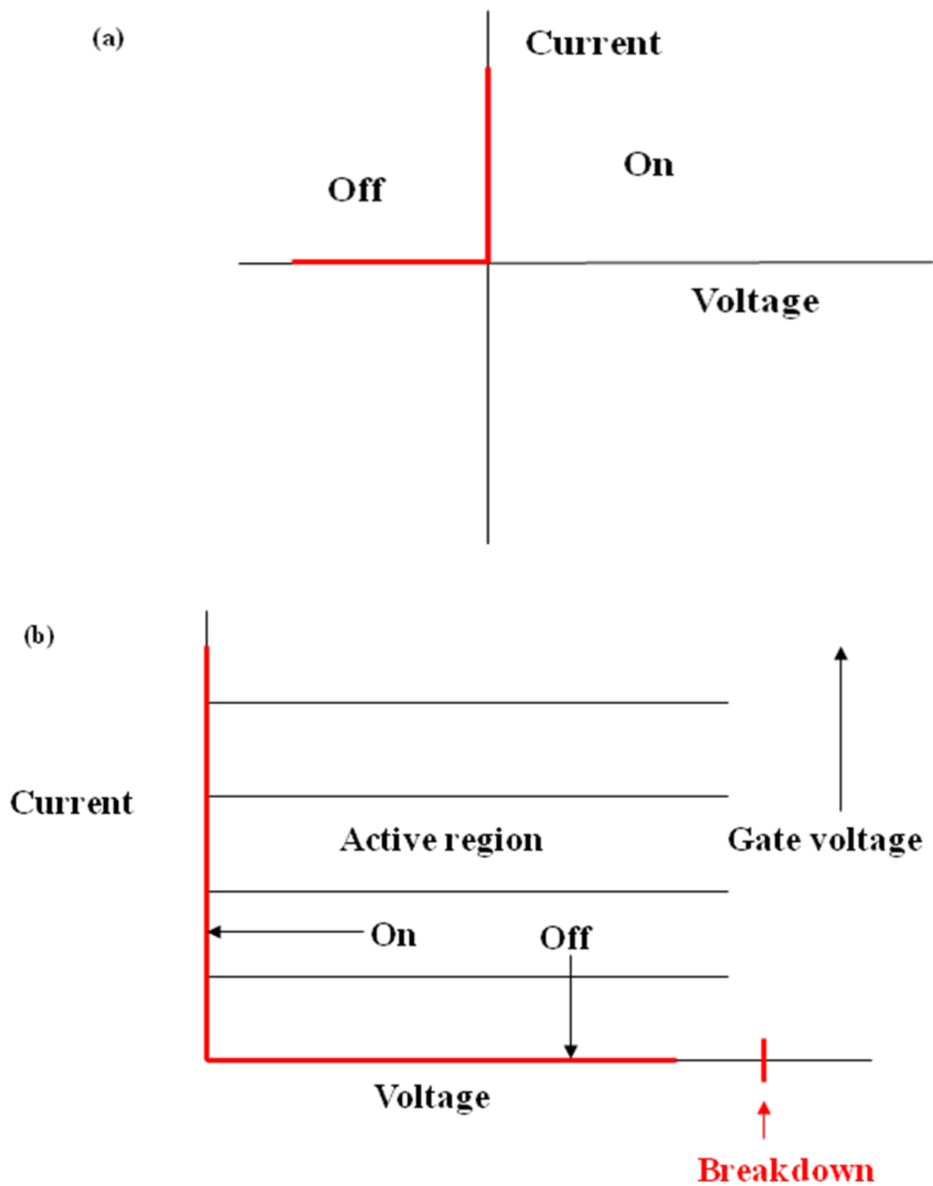


Figure 1.1: Ideal current-voltage characteristics of a diode (a) and transistor (b) [13].

corresponding waveforms of the power system are shown in figure 1.4.

Total power loss in a switch is P_{total} and is given by

$$P_{total} = P_{turn\text{-}on} + P_{turn\text{-}off} + P_{on} + P_{off}$$

At high frequencies, the switching power loss is very large, so fast switching power devices are desirable. At low frequencies, on-state power loss dominates, so we need power devices with low on-state resistance**.**

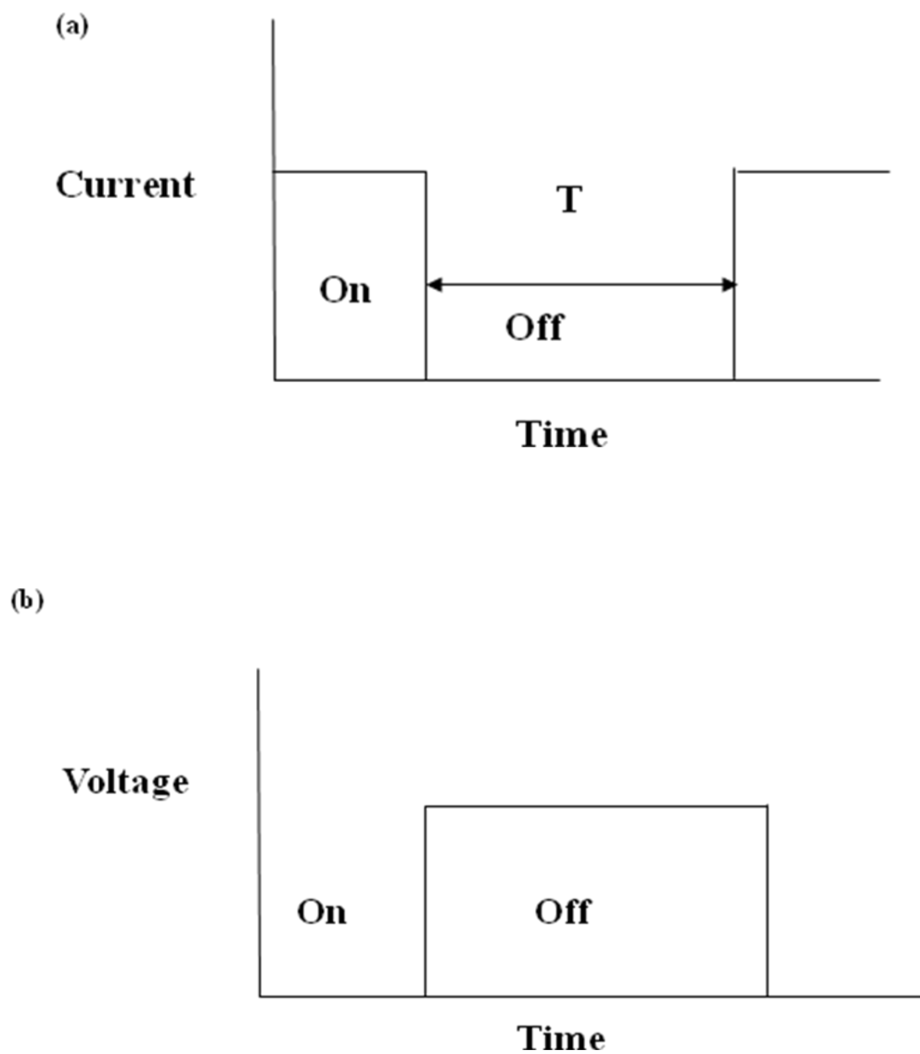
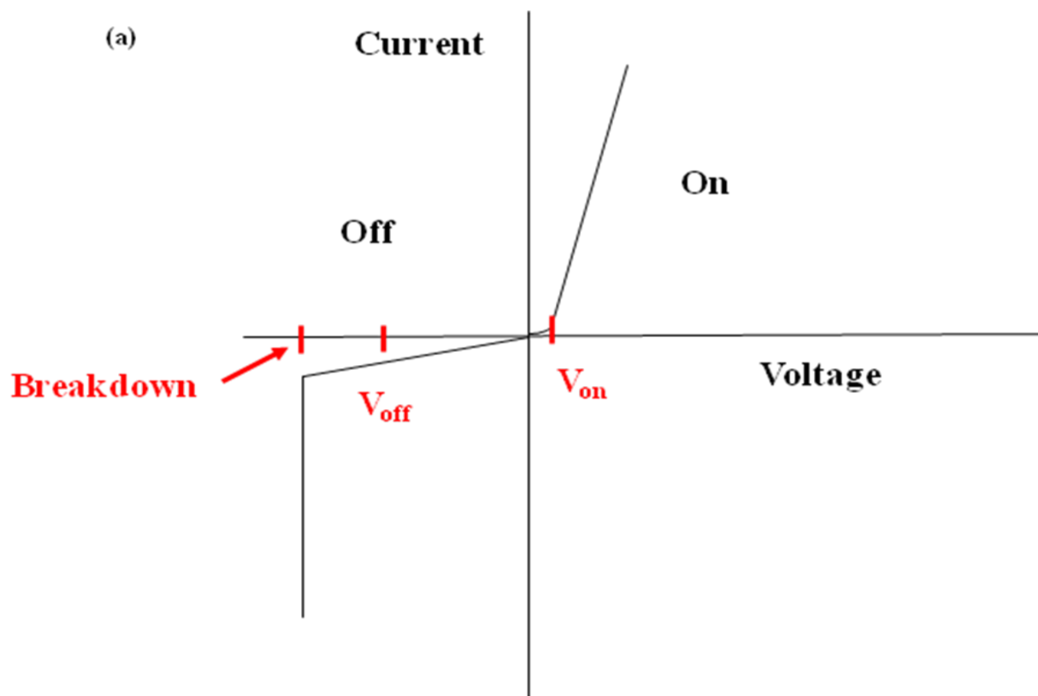


Figure 1.2: Switching waveforms of an ideal power system.



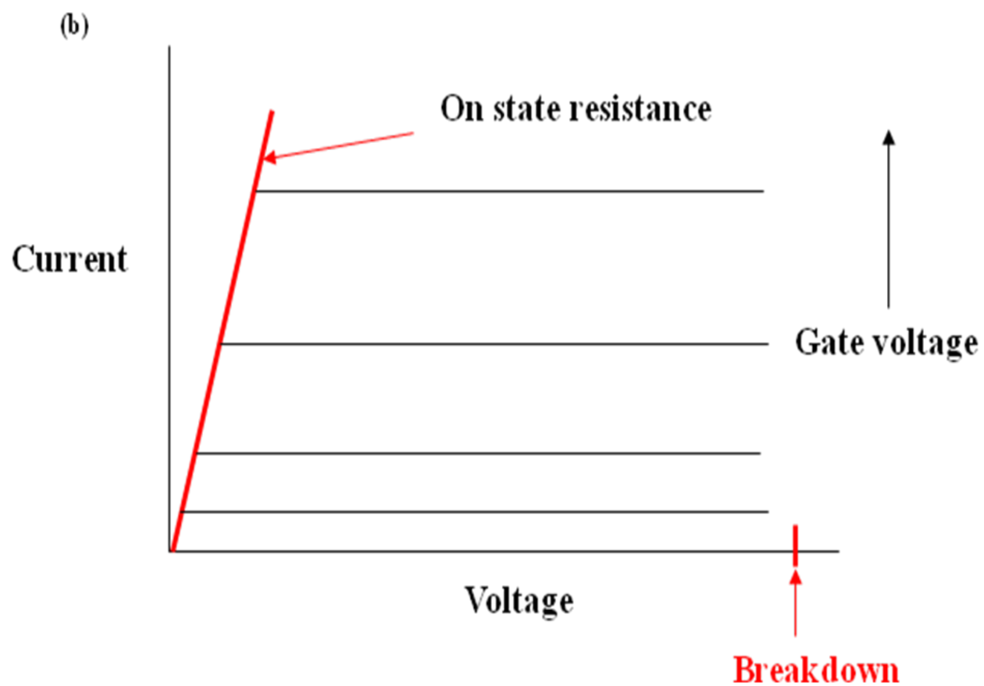


Figure 1.3: Real (non - ideal) current-voltage characteristics of a diode (a) and transistor (b). On sate resistance is $\Delta V/\Delta I$ [21].

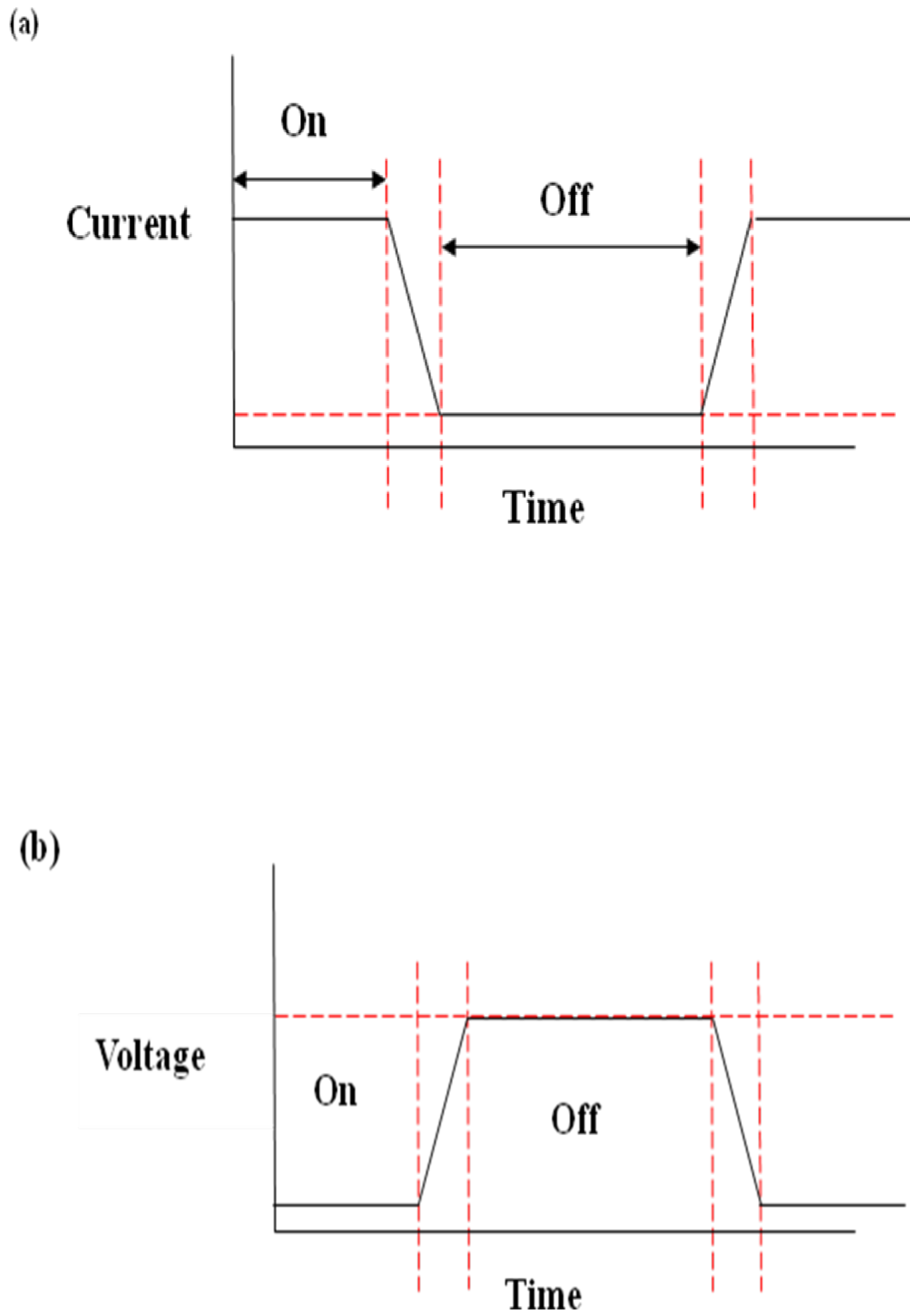


Figure 1.4: Switching waveforms in a real (non - ideal) power system [13].

1.3 Unipolar device

Power devices mainly fall in two categories - unipolar and bipolar. Schottky diodes and MOSFETs are examples of unipolar devices. In a unipolar device, only one type of carrier (either a majority electron or a majority hole) is responsible for current flow. The device can operate at higher frequencies which results in lower switching losses [22]. There is a flow of both majority and minority carriers in bipolar devices. The slower minority carriers have to be injected and removed to get the device to turn on and off, so in bipolar devices there is power loss due to switching and leakage current.

The n-channel Si-MOSFET is a good choice for low voltages (around 100V), and it can operate at high switching speed, 100 kHz. But as the blocking voltage increases, the on-state resistance increases drastically. The SiC-MOSFET enables us to go to higher operating voltages (order of kilo volts) with higher switching speed. This is possible because SiC has a high critical breakdown field, almost 7 times that of Si. The specific on résistance of the MOSFET is given by [23]

$$r_{ON} = 4V_B^2 / \mu_N \varepsilon_S E_C^3$$

V_B is the desired blocking voltage, μ_N is the bulk electron mobility and ε_S is the semiconductor permittivity. Bulk electron mobilities are similar for lightly doped Si and SiC (900-1200cm^2/V-s) [24]. However, $E_C^{SiC} \sim 7E_C^{Si}$, so that for a given blocking voltage, the specific on-resistance can be a factor of 7^3 or 343 times lower for SiC. Another way to think of this advantage is that at higher critical field of SiC means a much thinner drift region can support the source-drain voltage in blocking state. A thinner drift region means lower drift

resistance and thus lower on-resistance. Moreover, due to unipolar nature of the device we do not have to deal with stored charge and hence MOSFET will have higher switching speed.

SiC exists in different polytypes. 4H-SiC polytype has the highest bandgap energy. It has higher and more isotropic mobility compared to other polytypes and hence is used to fabricate MOSFET devices [25,26]. To use SiC to its full potential, we must continue to work to improve the electrical characteristics of the SiO_2/SiC interface by developing more efficient processes to passivate defects at the interface that form during the oxidation process. These defects trap carriers (electrons) from the channel to become charged, thereafter acting as Coulomb scattering centers that scatter other channel electrons. The result of trapping and scattering is lower effective channel mobility. At present there is a standard passivation process based on post-oxidation annealing in nitric oxide (NO) or nitric oxide followed by hydrogen annealing ($NO+H_2$) [27,28]. These passivations increase the inversion electron channel mobility of a SiC-MOSFET from single digits (~ 8$cm^2/V\cdot s$) to around 30$cm^2/V\cdot s$. Although these processes have made the commercialization of SiC MOSFETs a reality, there is still room for significant improvement. This inversion channel mobility value is only around 4% of bulk mobility value of SiC. In case of Si, the inversion channel mobility can be as much as 50% of bulk mobility [29]. Remember that both Si and SiC have similar bulk mobilities of around 900-1100$cm^2/V\cdot s$.

In addition to interface passivation, some groups have tried oxide growth in presence of sodium and have reported mobility values as high as 250 $cm^2/V\cdot s$ [30]. But as sodium moves under stress (high electric field of high temperature), devices fabricated with it are highly unstable and are of no practical use.

Phosphorus passivation (P-passivation) is more effective for reducing the interface tarp density at the 4H-SiC/SiO_2 interface compared to NO passivation. The peak value of the

effective mobility for a 4H-MOSFET after phosphorus passivation is ~ 90cm^2/V.s [31]. But phosphorus process causes voltage instability in the device by converting SiO_2 to phosphosilicate glass (PSG) which is a polar material [32]. The application of positive gate bias produces a sheet of positive polarization at the interface that acts in much the same way as do Na^+ atoms at the interface. Our research work involved the stabilization of P-passivated devices. We showed that if a thin PSG layer capped with deposited oxide is used as the gate oxide we can stabilize the device and also keep the passivating effect of phosphorus process. We obtained a peak field effect mobility of 72cm^2/V.s using this approach.

In addition to P-passivation, we also studied the effect of nitrogen plasma (N2P) passivation on the interface. The idea is to introduce nitrogen at the interface without the additional oxidation that occurs during an NO passivation anneal. During an NO anneal, thermal oxidation with defect creation continues in competition with defect passivation by nitrogen. Plasma nitridation improves SiO_2/SiC interface quality in the sense that it introduces nitrogen with little or no simultaneous oxidation (as compared to NO). In our studies, we demonstrated that nitrogen plasma passivation is very effective in reducing interface traps (D_{it}) in the top half of the 4H-SiC bandgap to around $2x10^{11}$ cm^{-2}eV^{-1}. This number is similar to the trap density that can be obtained using phosphorous and approximately a factor of two lower than the trap density following an NO anneal.

We also worked on a new process to fabricate 4H-SiC MOSFET. This new process limits the liberation of carbon during MOSFET fabrication and paves a way to study the role of carbon in limiting the channel mobility. In our research we worked on three projects:

1. Stable devices using P- passivation
2. Improved N2P passivation
3. Role of carbon in limiting the mobility of SiC-MOSFET

1.4 Properties of silicon carbide

1.4.1 Polytypsim in silicon carbide

Silicon carbide exhibits the material characteristic of polytypism [33,34]. The tetrahedron is the building block of the SiC crystal with silicon (Si) at the center of tetrahedron and carbon (C) at the four corners as shown in figure 1.5.

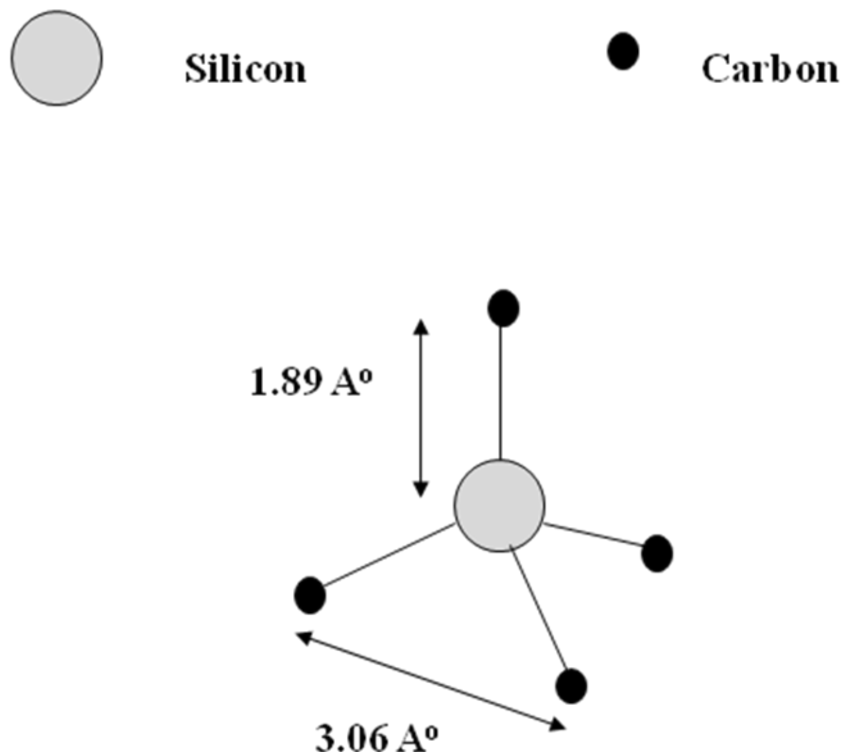


Figure 1.5: Building block of SiC [34].

The distance between Si and C is 1.89A^{o}, and the distance between C and C is 3.06A^{o}.There exists a second type of tetrahedron which is rotated by 180°. Silicon carbide has more than 200 polytypes. Among all polytypes, the technologically important are 3C-SiC, 4H-SiC and 6H-SiC. Depending upon the polytype SiC shows different electrical and physical properties.

All polytypes of SiC have a hexagonal arrangement of SiC bilayers. Close packing of three bilayers (A, B and C) is shown in figure 1.6. In the 3C-SiC, the cubic polytype, the stacking sequence is ABCABC…….. The simplest hexagonal polytype is 2H-SiC having a stacking sequence ABAB…....... For 4H-SiC and 6H-SiC stacking sequences are ABCBABCB……………..and ABCACBABCACB…………… respectively. In notation for SiC, the letter designates the crystal structure of that particular sacking sequence and the number in the notation gives the periodicity of the sequence. The 4H-polutype was used in this work.

For an electronic device a high purity material is required. Initially in SiC it was very difficult to get large size polytype crystal. But then modified Lely process (1978) which is bulk crystal growth using seeded growth change the picture. And now SiC crystal with four inch diameter is available commercially [35]. Even though the modified Lely process makes the growth of bulk SiC wafer possible still it is not flawless. There are two types of defects seen in the crystal after growth-micropipes and low-angle grain boundaries [36].

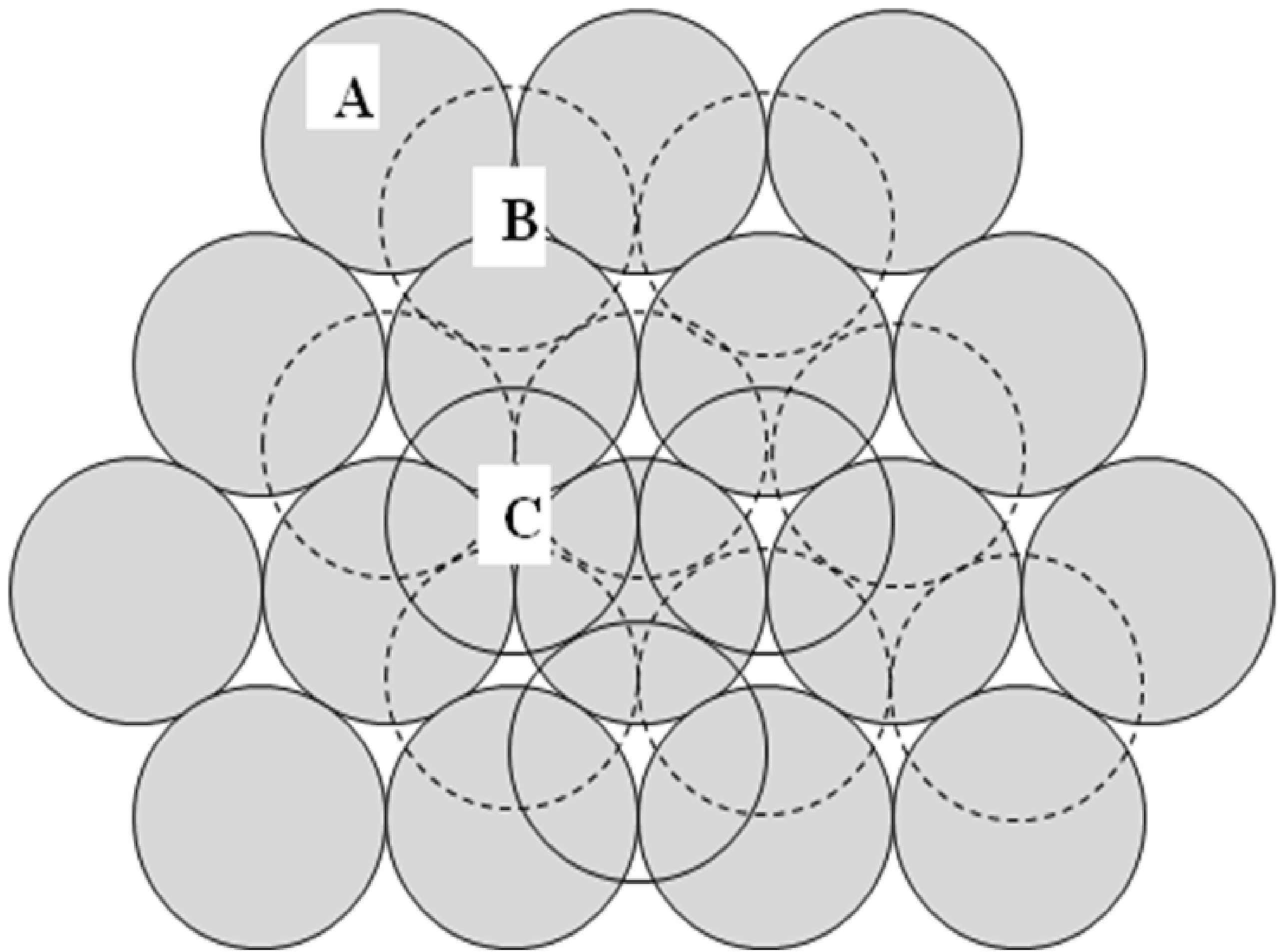


Figure 1.6: Close packing of three planes of spheres, one plane above the other. Each plane represents Si-C bilayers.

1.4.2 Electrical and physical properties of silicon carbide

SiC is a robust material with a Young's modulus of 424GPa, and is inert at room temperature [37]. As a semiconductor, silicon carbide has a number of advantages as compare to silicon. Important electrical properties are compared in Table 1.7 for both semiconductors.

Table: Electrical properties of Si and several SiC polytypes [37].

Semiconductor	Si	3C-SiC	6H-SiC	4H-SiC
Bandgap (eV)	1.12	2.4	3.03	3.26
Breakdown Field (MV/cm)	0.25	>1.5	2.4 parallel to c-axis > 1, perpendicular to c-axis	2.2 parallel to c-axis
Intrinsic Carrier Conc.(cm^{-3})	1.45e10	1.5e-1	1.6e-6	5e-9
Electron Mobility @ $n_d = 10^{16}$ cm^{-3}	1430	800	60 parallel to c-axis 400 perpendicular to c-axis	900 parallel to c-axis 800 perpendicular to c-axis
Hole Mobility @ $n_a = 10^{16}$ cm^{-3}	480	40	90	115
Saturated Electron Vel (10^7cm/s)	1	2.5	2	2
Thermal Conductivity (W/cm-K)	1.5	3.2	3.0-3.8	3.0-3.8

SiC devices can withstand higher temperature as compare to Si [38,39]. The intrinsic carrier concentration of a semiconductor is given by

$$n_i = \sqrt{N_C N_V}\ e^{(-Eg/2kT)}$$

where

N_C = effective density of states in conduction band;

N_v = effective density of states in valance band;

E_g = band gap energy;

k = Boltzmann's constant;

T = absolute temperature.

Due to low band gap of Si, the intrinsic carrier concentration n_i of Si increases rapidly with increasing temperature. If n_i becomes equal to the doping concentration, a material loses its semiconductor characteristics and behaves as a simple resistor. If we want to use a Si device at temperatures >100°C, then we have to increase the doping. But there is a problem with this approach. Increased doping results in a higher internal electric field in the device and which leads to electrical breakdown. The much larger band gap of SiC (x3 Si) leads to lower intrinsic carrier concentration and a theoretical operating temperature of up to 500°C.

SiC is best suited for high power devices due largely to its large band gap, high breakdown field and high thermal conductivity. However, it would not be fair to say that power devices are not fabricated using Si. Silicon thyristors are used for high voltage DC transmission. Bipolar junction transistors (BJTs) are used for medium power conditioning and moderate speeds. But in order to use BJTs at higher voltages, one must use complicated control circuits and which leads to additional power dissipation. The invention of the MOSFET circumvented some of these problems. This unipolar device in Si is very good for low voltage (less than a few hundred volts) and high frequencies (>100 kHz). Because of low critical field of Si, these devices are not used at higher voltages. Then there is the invention of the Si IGBT (insulated gate bipolar transistor) that can be used at higher voltages compare to the MOSFET. As minority carriers play an important role during its operation of bipolar devices, the switching

speed of the IGBT devices is lower. For higher voltage, high current and low switching frequencies, the IGBT is good choice, while for lower voltage, high current and high switching speed, the MOSFETs is better.

SiC has three times the thermal conductivity of Si, and this is very important for the power devices. It makes heat dissipation much easier during device operation. Material properties can change with rising temperature that is the result of poor heat dissipation. High saturated electron velocity also makes SiC a good choice for microwave and radio frequency applications. SiC Schottky diodes have been on the market for a few years, and they are proving to be reliable replacements for better than silicon junction diodes. Recently, CREE Inc. has also marketed 1200V SiC power MOSFETs [40], so that the components of the ‘all SiC” power switch are not available.

1.5 References

[1] W. G. Pfann and J.H. Scaff, *Proceedings of the I.R.E.* **38**, 1151 (1950).

[2] L. B. Valdes, *Proceedings of the I.R.E.* **40**, 445 (1952).

[3] J. A., *Proceedings of the I.R.E.* **40**, 1314 (1952).

[4] Chrisrophe Lecuyer, *Making Silicon Valley: Innovation and the Growth of High Tech, 1930-1970* (The MIT Press, 2007).

[5] William C. ÓMara, Robert B. Herring, and Lee P. Hunt, *Handnook of Semiconductor and Silicon Technology* (Willam Andrew, 1990).

[6] B.E. Deal and A.S. Grove, J. Appl. Phys. **36**, 3770 (1965).

[7] N. F. Mott, S. Rigo, F. Rochet, A. M. Stoneham,*PHIL. Mag. B.* **60**, 189 (1989).

[8] K. Dah-Bin, M. P. James, N. D. William, C.S. Krishna, *IEEE Trans. Elec. Dev.* 35, 25 (1998).

[9] http://www.sia-online.org/news/2012/02/06/global-sales-report-2012

[10] http://www.icinsights.com

[11] http://www.electroiq.com/articles/sst/print/volume-54/issue-7.html

[12] http://www.power-mag.com/news.detail.php?NID=38

[13] B. J. Baliga, *Fundamentals of Power Semiconductor Devices,* (Springer, 2008).

[14] R. M. Warner, IEEE Trans. Elec. Dev. **48**, 2457 (2001).

[15] http://www.irf.com/60anniversary/index.html#1970s.

[16] R. H. Lasseter, P. Paigi, *IEEE 35th Annual Conference on Power Electronics Specialists* **6**, 4285 (2004).

[17] N. Hatziargyriou, *IEEE Power and Energy Magazine* **5**, 78 (2007).

[18] Q. Zhang, R. Callanan, M. K. Das, S. H. Ryu, A. K. Agarwal, and J. W. Palmour, *IEEE Trans. Power Elec.* **25**, 2889 (2010).

[19] S. E. Saddow, A. Agarwal, *Advances in Silicon Carbide and Applications*, (Artech House 2004).

[20] M. Bhatnagar and B. J. Baliga, *IEEE Trans. Elec. Dev.* **3**, 645 (1993).

[21] B. J. Baliga, *Advanced Power MOSFET Concepts*, (Springer, 2010).

[22] B. J. Baliga, *Silicon Carbide Power Devices,* (World Scientific, 2005).

[23] B.J. Baliga, *IEEE Trans. Electron Dev.* **43**, 1717 (1996).

[24] N. D. Arora, J. R. Hauser, and D. J. Roulston, *IEEE Trasns. Elec. Dev.* **29**, 292 (1982).

[25] J. A. Cooper Jr. and A. Agarwal, *Proceedings of the IEEE* **90**, 956 (2002).

[26] S. Dhar, S. Wang, J. R. Williams, S. T. Pantelides, and L. C. Feldman, *MRS Bulletin* **30**, 288 (2005).

[27] G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, R. K. Chanana, Robert A. Weller, S. T. Pantelides, Leonard C. Feldman, Member,O. W. Holland, M. K. Das, and John W. Palmour, *IEEE Elec. Dev. Lett.* **22**, 176 (2001).

[28] J. Senzaki, K. Kojima, S. Harada, R. Kosugi, S. Senzaki, and K. Fukuda, *IEEE Elec. Dev. Lett.* **23**,13 (2002).

[29] J. Welser, J. L. Hoyt, J. F. Gibbons, Elec. Dev. Lett. **15**, 100 (1994).

[30] E,O. Sveinbjornsson,F. Allerstam, G. Gudjónsson, H.Ö. Ólafsson, D. Dochev, T. Roddle,and R. Jos, *Mater. Sci. Forum* **556-557**, 487,(2007).

[31] D. Okamato, H. Yano, T. Hatayama, and T. Fuyuki, *IEEE Electron Dev. Lett.* **31** 710 (2010).

[32] Y. K. Sharma, A. C. Ahyi, T. Issacs-Smith, X. Shen, S. T. Pantelides, X. Zhu, J. Rozen, L.C. Feldman, Y. Xu, E. Garfunkel, and J.R. Williams, *Mat. Sci. For.* **717 – 720**, 743 (2011).

[33] F. Bechstedt, P. Kackell, A. Zywietz, K. Karch, B. Adolph, K. Tenelsen, and J. Furthmuller,*Phy. Sta. Sol. (b)* **202**, 35 (1997).

[34] S. E. Saddow and A. Agarwal, *Advances in Siliocn Carbide Processing and Applications*, (Artech House 2004).

[35] http://www.cabotcmp.com/sicceed-1210-a/b-series-silicon-carbide-slurry.

[36] S. H. Vanger, *Silicon Carbide: New Materials, Production Method, and Applications,* (Nova Science, Inc. 2011).

[37] G. L. Harris, Properties of Silicon Carbide, (IET, 1995).

[38] M. R. Werner and W. R. Fahrner, *IEEE Trans. Indust. Elec.* **48**, 249 (2001).

[39] R. W. Johnson, J.L. Evans, P. Jacobsen, J. R. Thompson, and M. Chrirstopher, *IEEE Elec. Pack. Manf.* **27**, 164 (2004).

[40] http://www.cree.com/power/products.

CHAPTER 2

Metal oxide semiconductor capacitor/transistor

2.1 Ideal metal oxide semiconductor capacitor (MOS-C)

What is a MOS-C? It is a structure in which SiO_2 is sandwiched between a metal layer and a semiconductor as shown in figure 2.1 [1,2]. With the help of this structure, we can study the characteristics of an oxide-semiconductor (O-S) interface as well as the breakdown characteristics of the oxide [1,3]. The O-S interface is crucial for a metal-oxide-semiconductor field-effect transistor (MOSFET) [4,5]. The concept of MOS-C was proposed in Lilienfeld's patent (1926) [6], but the real working MOS device was demonstrated by Atalla and Kahng in 1959 [7,8].

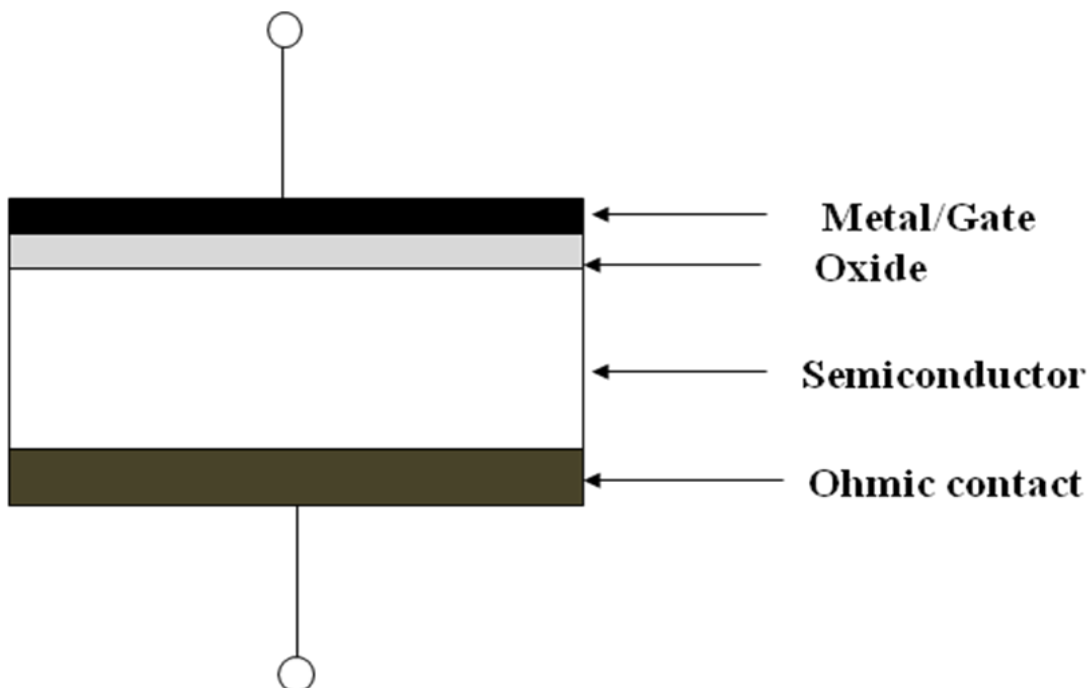


Figure 2.1: Metal oxide capacitor [2].

MOSFET fabrication involves additional and more complicated processing steps, and it is much easier to study the MOS-C to determine the characteristics of the O-S interface. Interfacial characteristics are similar for both devices. The following is a discussion of the properties of an ideal MOS-C.

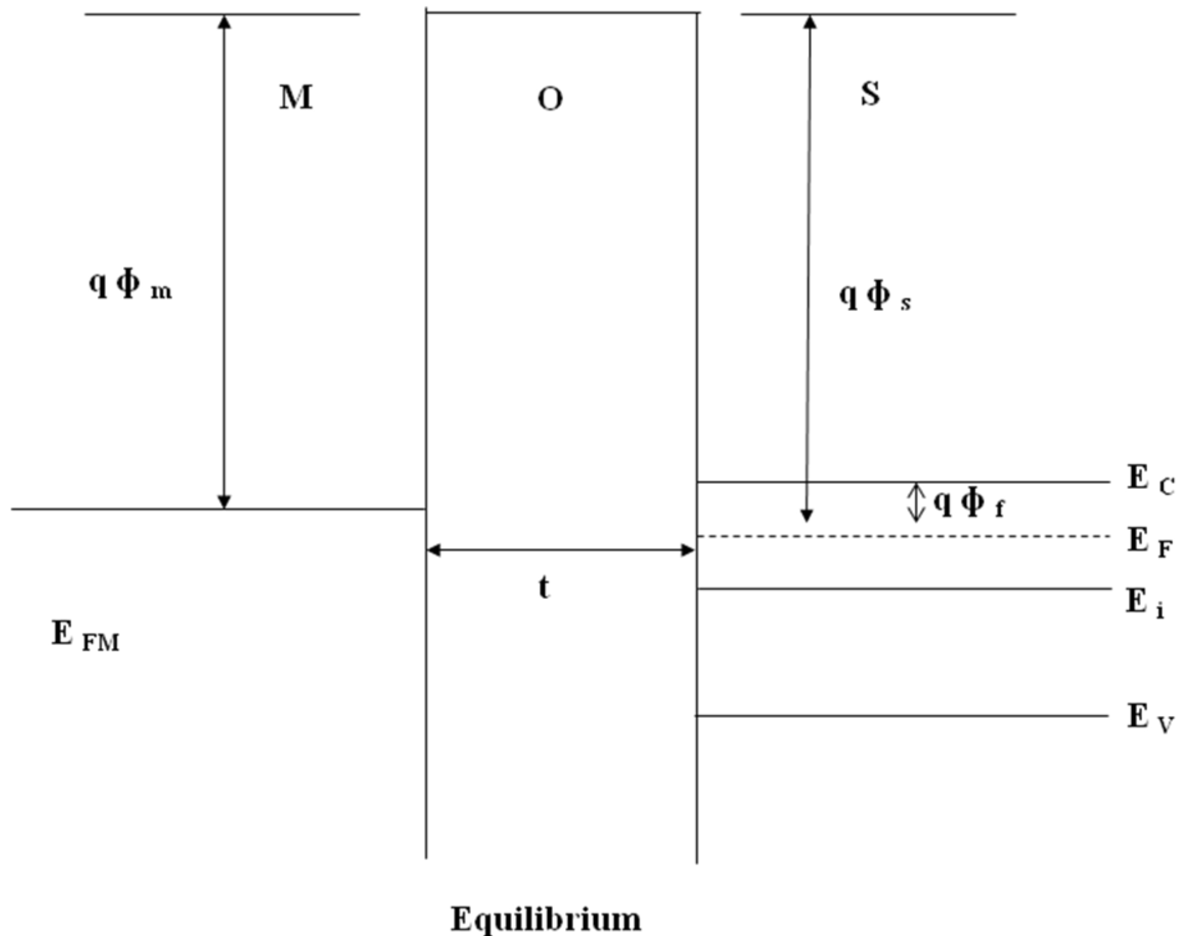


Figure 2.2(a): Energy band diagram of a metal oxide semiconductor capacitor with $\phi_m = \phi_s$ [4].

The following assumptions are made for the ideal MOS-C:

(1) The gate metal is very thick.

(2) The oxide is perfect insulator so that no current is flowing under static bias.

(3) The oxide is free of mobile charges and trap centers, and there are traps and defects at the O-S interface.

(4) The semiconductor is uniformly doped.

(5) The semiconductor is very thick.

(6) Work functions of metal and semiconductor are equal, $\phi_m = \phi_s$.

The band diagram of an ideal MOS-C at equilibrium is shown in figure 2.2 (a). Here semiconductor is n-type. In order to simplify the discussion of the ideal MOS-C, the work functions of metal, ϕ_m, and semiconductor, ϕs, are defined with respect to the conduction band of the oxide. The oxide thickness is $t_{ox,}$ and the quantity $q\phi_f$ is the energy difference between the intrinsic Fermi level, $E_{F,}$ and the quasi Fermi level, E_F.

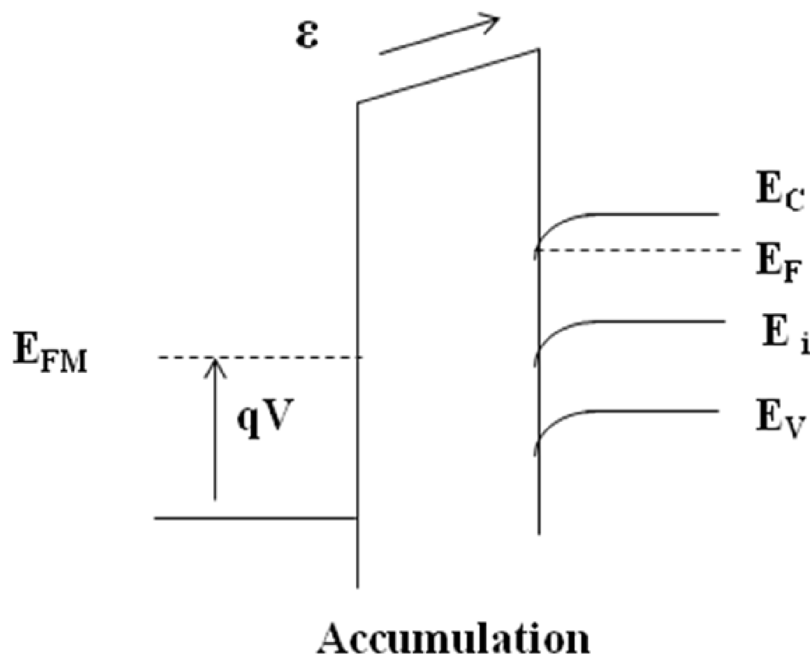


Figure 2.2(b): n-MOS-C in accumulation.

When a positive bias, V > 0, is applied to the metal gate, the metal becomes positively charged, and, in response, there is equal charge of opposite polarity induced in the semiconductor.

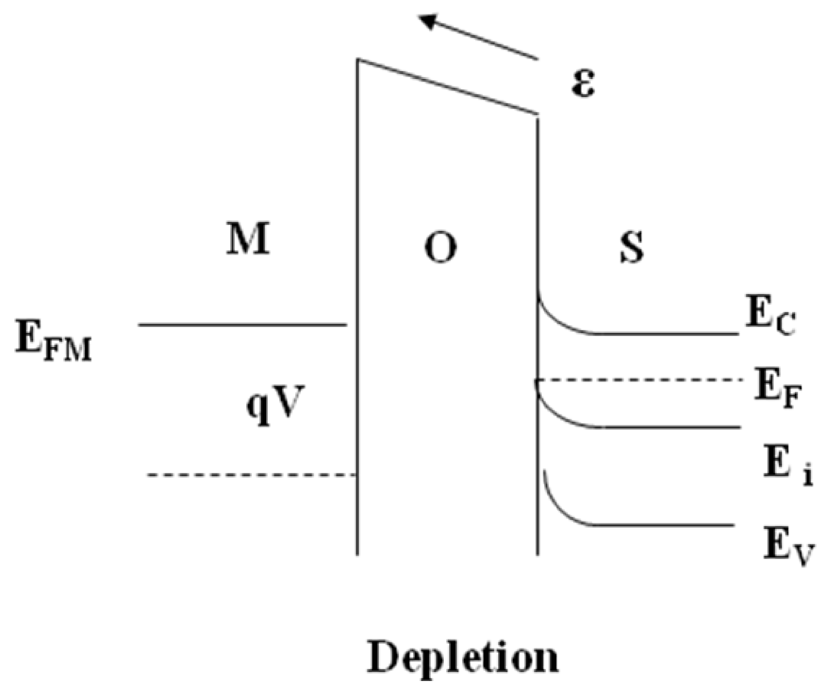


Figure 2.2(c): n-MOS-C in depletion [5].

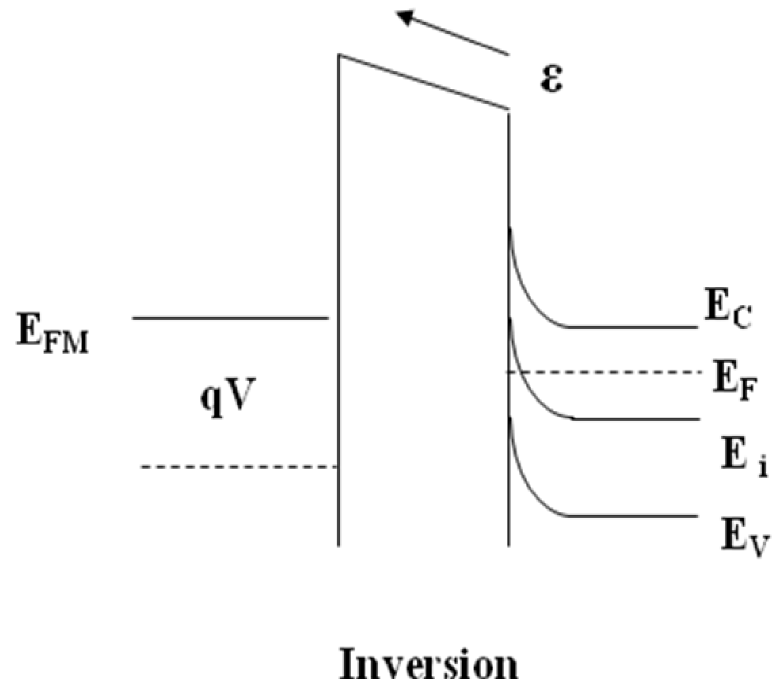


Figure 2.2(d): n-MOS-C in inversion.

Negatively charged electrons accumulate in the semiconductor near the O-S interface. Under this condition, the MOS-C is said to be in accumulation as the majority charges, in this case electrons, collect near the surface of the semiconductor. Also, as the applied voltage is positive, the Fermi energy of the metal is lowered below its equilibrium value. But as ϕ_m and ϕ_s are fixed, positive bias decreases the Fermi energy of metal with respect to semiconductor and leads to an electric field across the oxide. The direction of the electric field is from the metal to the semiconductor. The magnitude of the electric field depends upon the slope of the energy levels in the band diagram and is given by

$$\varepsilon(x) = 1/q \ (dE / dx)$$

where E is the energy of conduction or valance band, and

x is the distance from the interface in to the semiconductor.

In accumulation mode, there is an increase in the concentration of electrons at the O-S interface. The electron concentration is given by

$$n = n_i e^{(E_F - E_i)/kT}$$

where n_i is the intrinsic carrier concentration of the semiconductor, k is the Boltzmann canasta and T is temperature. As n_i increases the difference of $E_F - E_i$ increases, and as E_F should be constant under static bias condition E_i must moves near the O-S interface as shown in fig. 2.2 (b). Under static bias there is no current flow in semiconductor [assumption (2)].

When a negative bias, $V < 0$, is applied to the MOS-C, a net positive charge is induced at the interface on the semiconductor side. This positive charge arises due to the depletion of majority carriers (electrons) at the interface. This positive charge is due to uncompensated donor ions. The concentration of electrons at the interface is less than the concentration of electrons in the bulk of the n-type semiconductor as shown in figure 2.2(c).

If we keep increasing the negative bias, the intrinsic energy, $E_{i,}$ at the interface will become higher than the quasi Fermi energy, $E_{F.}$ Under this condition, the conductivity of semiconductor surface is like that of a p-type semiconductor. This situation is called the inversion mode of a MOS-C. Figure 2.3 shows the band bending under inversion for an n-type semiconductor. In this figure, ϕ is the potential energy at position x relative to position of E_i at equilibrium and is given by

$$\phi(x) = E_i(x) - E_i(\text{bulk})$$

This quantity describes the band bending under biasing. ϕ_s is the surface potential at the O-S

interface where x=0. The requirement for strong inversion is given by

$$\phi_s = 2\phi_F = 2\, kT/q \ln (N_a/n_i)$$

where N_a is the acceptor doping concentration in the p-type semiconductor.

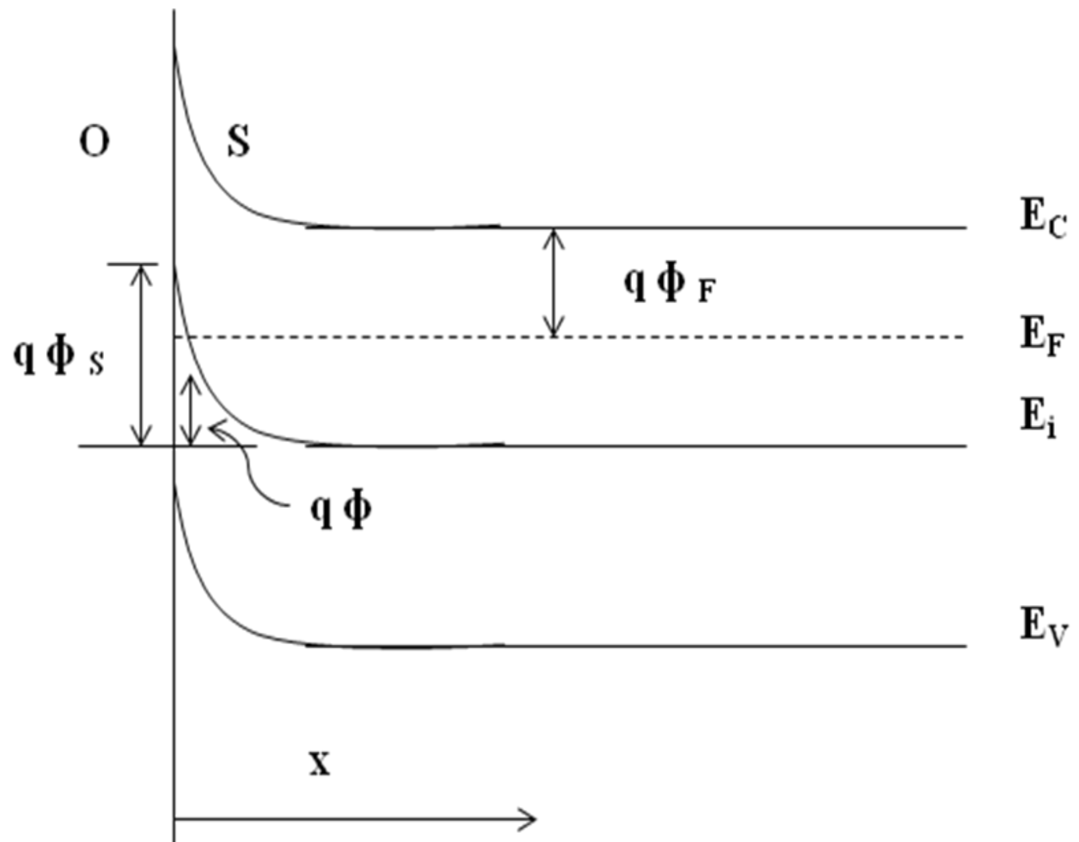


Figure 2.3: Band bending in n-type semiconductor for an inversion mode [4].

2.2 Charge distribution in different modes of operation of a MOS-C

2.2.1 Accumulation

When a positive bias, V > 0, is applied to the n-MOS-C, there is an accumulation of a net negative charge (due to electrons) at the interface on the semiconductor side as shown in figure 2.4 (a).

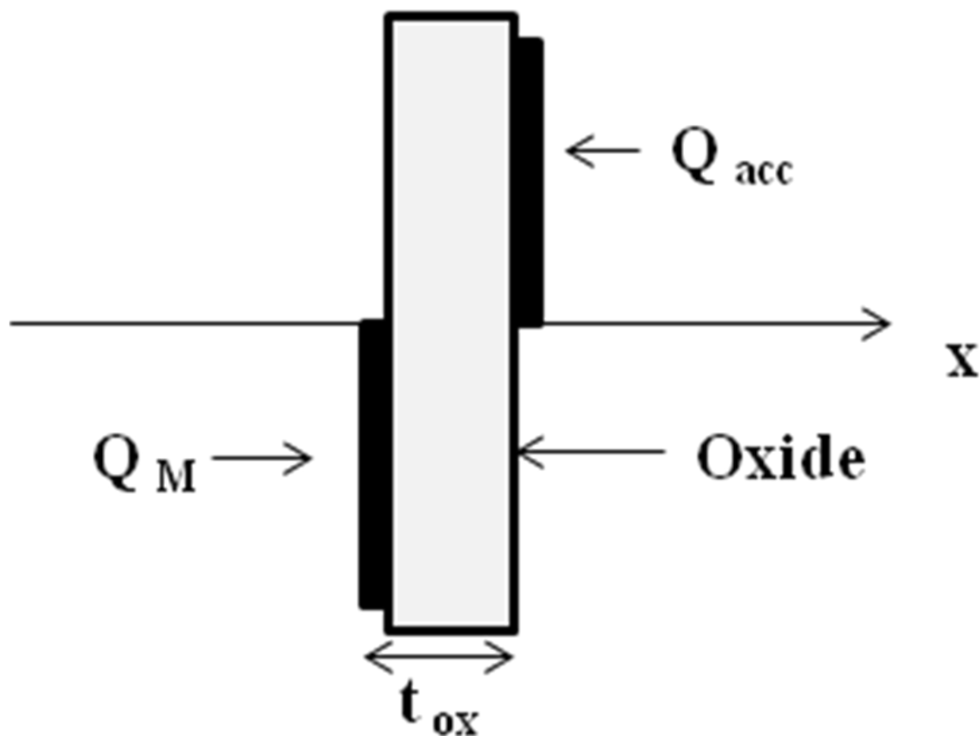


Figure 2.4(a): Charge distributions in the accumulation mode of a MOS-C [9].

This negative charge is equal in magnitude but opposite in polarity to the charge on the metal. When the dc voltage is superimposed with a small ac signal, these majority carriers (electrons) respond immediately to the ac signal. Hence in accumulation mode, the MOS-C is equivalent to a parallel plate capacitor with a sheet charge of electrons acting as a second

plate of the capacitor. The accumulation mode capacitance per unit area, C_{acc}, of the MOS capacitor is equal to the capacitance of the oxide, C_{ox} and is given as

$$C_{acc} = C_{ox} = \frac{K_{ox}}{t_{ox}}$$

where K_{ox} is the dielectric constant of oxide, and t_{ox} is the thickness of oxide layer.

2.2.2 Depletion

When a negative bias, $V < 0$, is applied to the n-MOS-C, there is a depletion of majority

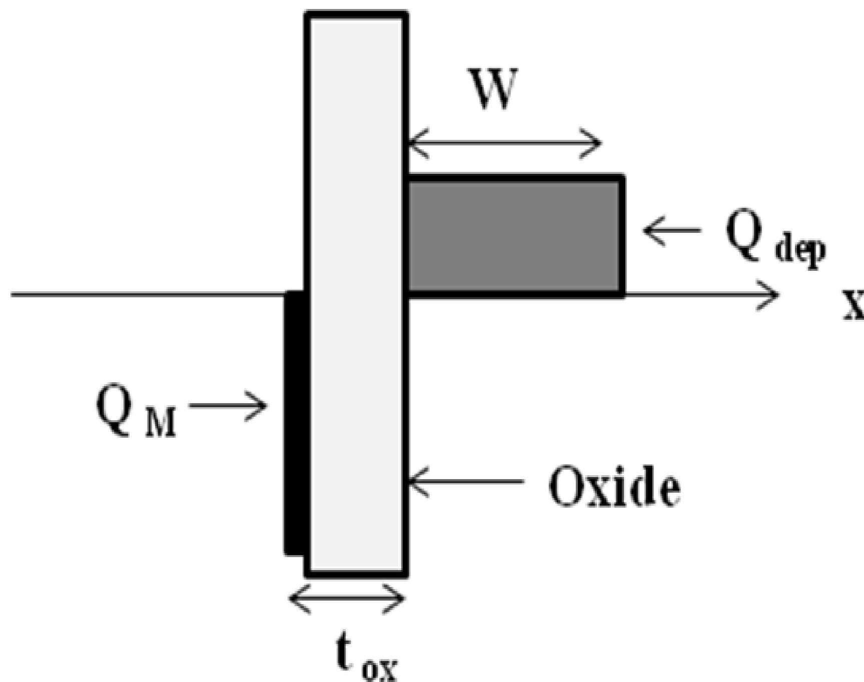


Figure 2.4 (b): Charge distributions in the depletion mode of a MOS-C.

carriers at the interface. The concentration of electrons at the interface is less than the concentration in the bulk of the semiconductor. The negative charge at metal surface is balanced by a net positive charge from the ionized donors in semiconductor.

The capacitance of MOS-C is equivalent to a parallel plate capacitor, but now instead of a single oxide layer there are two different layers - an oxide layer and a depletion layer in the semiconductor. Total capacitance of the MOS-C in this case is a series combination of an oxide capacitance and semiconductor capacitance. The depletion mode capacitance (C_{dep}) is given by

$$C_{dep} = [1/C_{ox} + 1/C_s]^{-1} = [t_{ox}/K_{ox} + K_s/W_{dep}]^{-1}$$

where K_s is the dielectric constant of semiconductor and W_{dep} is the width of depletion layer in semiconductor. All these capacitance are in per unit area.

2.2.3 Inversion

If we keep increasing the negative bias, the n-MOS-C will eventually reach its inversion mode. The block charge diagram is shown in figure 2.4(c). The total capacitance (C_{inv}) of the MOS-C depends upon the frequency of the small ac voltage signal (see section 2.4). If frequency is low, $\omega \to 0$, then the minority carries (holes) in inversion layer will respond to the small ac signal. In that case the capacitance is equal to the C_{ox}.

$$C_{inv} = C_{ox} = \frac{K_{ox}}{t_{ox}} \quad \text{if} \quad \omega \to 0$$

where C_{inv} is inversion capacitance.

If the frequency of the ac signal is high, $\to\infty$, then the minority carriers (holes) cannot respond, while the electorns at the edge of the depletion layer can, and capacitance is given by

$$C_{inv} = C_{ox} + C_{smin} = \frac{K_{ox}}{C_{ox}} + \frac{K_S}{W_{max}} \quad \text{if } \omega \to \infty$$

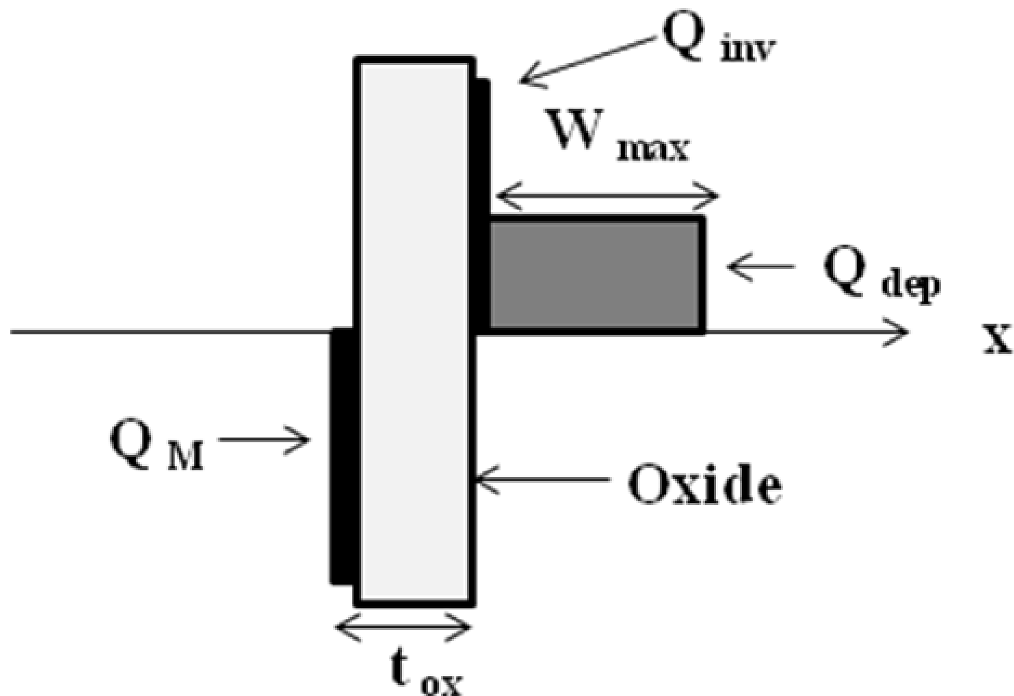


Figure 2.4 (c): Charge distributions in the inversion mode of a MOS-C.

2.3 Non - ideal metal oxide semiconductor capacitor (MOS-C)

For realistic MOS-Cs, there are several important non-idealities [4,10]**.** The threshold voltage, V_T, which decides the formation of an inversion layer in a MOS-C, depends upon all these non-idealities. These non-idealities include the gate metal-semiconductor work function difference, interface taps, charges in the oxide, etc [11,12].

2.3.1 Work function difference

The work function difference, $\phi_{ms} = \phi_m - \phi_s$, between metal and semiconductor gives rise to

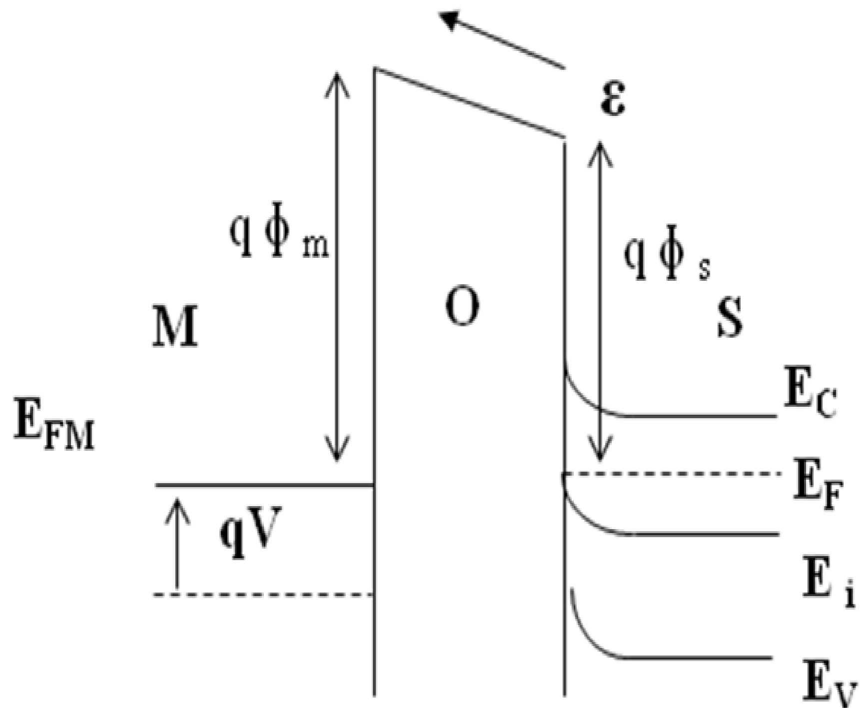


Figure 2.5(a): Band bending due to work function difference of metal and semiconductor, $\phi_m > \phi_s$.

band bending, figure 2.5(a) and results in an induced electric field. Here, the work function of metal is higher than that of semiconductor. To have flat band conditions in the semiconductor, (i.e., semiconductor surface potential = 0), we need to apply a voltage which is equal to ϕ_{ms} as shown in figure 2.5(b). This is the first correction term (ΔV_1) to the ideal $V_{gate} = 0$ flat band condition of a MOS-C.

$$\Delta V_1 = \phi_{ms} = \phi_m - \phi_s$$

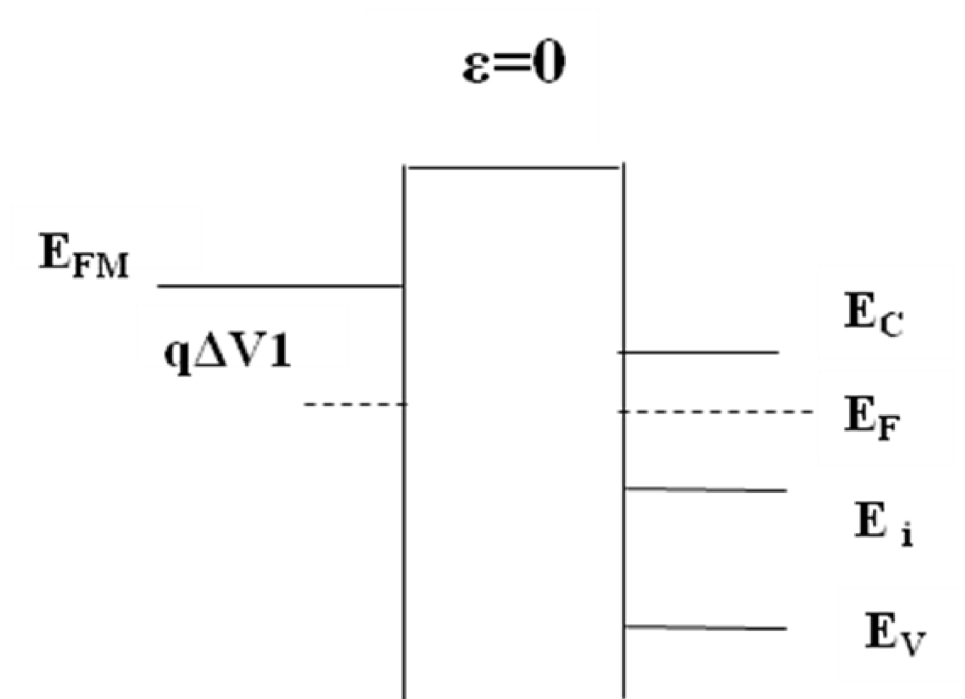


Figure 2.5(b): First correction term for a non-ideal ideal MOS-C due to the gate metal-semiconductor work function difference.

In addition to work function difference, as many as four types of charge can be found that exist in the SiO_2-semiconductor system. These charges are not present in an ideal MOS-C. The four types - mobile oxide charge, fixed oxide charge, oxide trapped charge and interface trapped charge - are shown in figure 2.6.

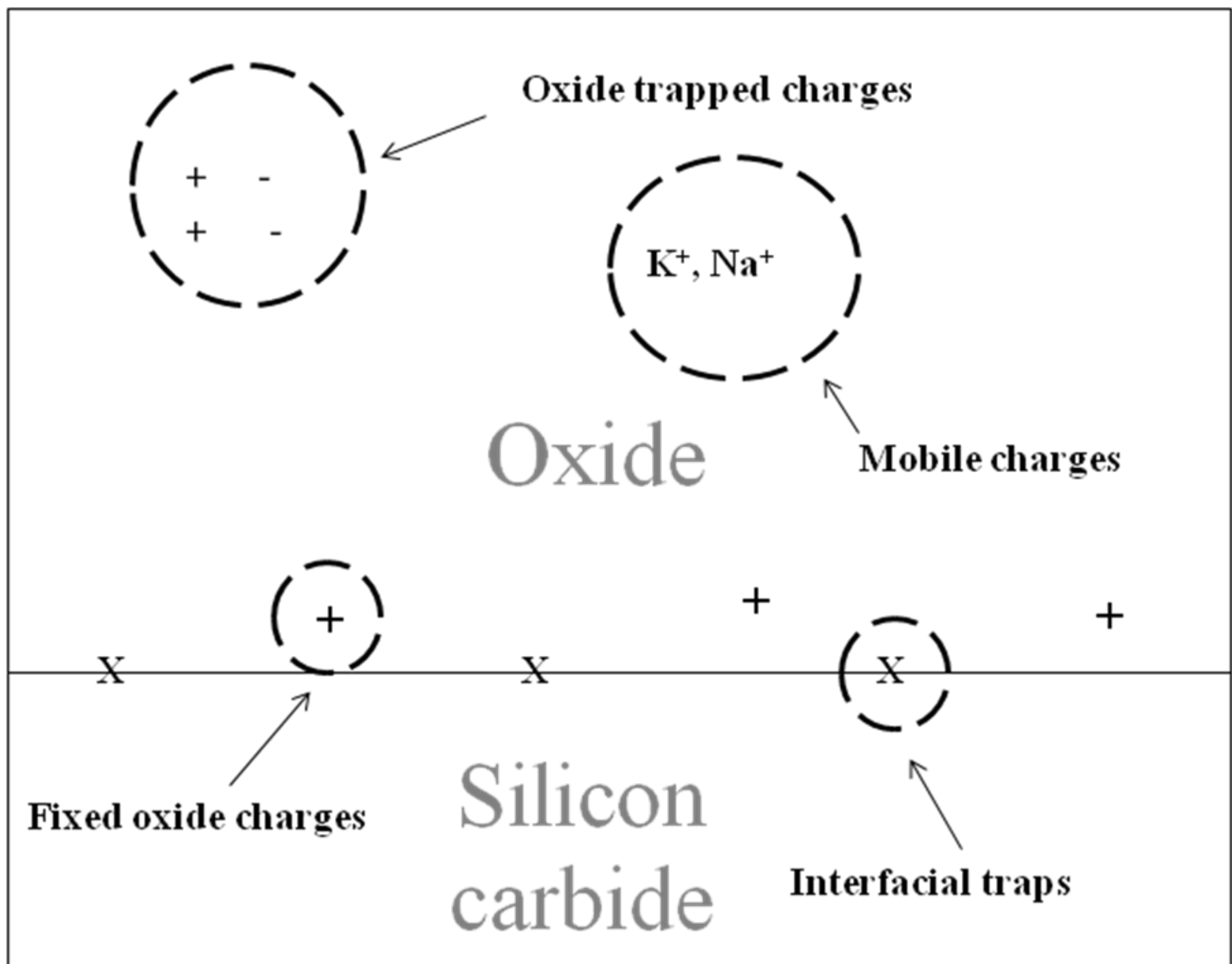


Figure 2.6: Various charges in SiC-SiO_2 system [10].

2.3.2 Fixed oxide charge (Q_f)

Fixed oxide charges are positive and appear in the oxide very near the interface. These charges are fixed and do not move under high temperature or bias. The appearance of fixed charge is related to the conditions under which the oxidation of SiC is performed. These conditions are oxidation temperature, gas ambient, cool down following oxidation and crystal orientation of the SiC. These charges give rise to a second correction term (ΔV_2)

$$\Delta V_2 = -\frac{Q_f}{C_{ox}}$$

2.3.3 Mobile oxide charge (Q_m)

This charge exists due to the presence in the oxide of mobile ions such as Na^+ and K^+. These charges are mobile under temperature and bias, and depending upon the polarity of dc bias, they can be moved to and from the interface. The presence and position of these positive charges gives rise to a third correction term (ΔV_3)

$$\Delta V_3 = -\frac{\gamma Q_m}{C_{ox}}$$

where $\gamma = 1$ if the mobile charge is at the oxide-semiconductor interface, and $\gamma=0$ if the mobile charge is at the gate metal-semiconductor interface.

2.3.4 Oxide trapped charge (Q_{ot}):

This charge is immobile, and it can be negative or positive depending upon the nature of trapping. Radiation damage in the bulk of the oxide is often a source for Q_{ot} (sign is +/-) The correction term (ΔV_4) in this case is

$$\Delta V_4 = \frac{Q_{ot}}{C_{ox}}$$

2.3.5 Interface trapped charge

Interface trapped charge is currently a major obstacle for the silicon carbide MOS R&D community. The origin of these charges is not well understood but may be related to mainly silicon & carbon dangling bonds, carbon clusters, carbon dimmers in the SiC, and oxygen vacancies in the oxide very near the interface [13]. Interfacial traps create localized energy levels the energy band gap of SiC. These interfaces traps form potential wells that capture

electrons and holes. In addition, charge traps also act as Columbic scattering centers. These two effects decrease the effective channel mobility in a MOSFET. Depending upon the surface potential, these traps can be charged positively or negatively. Figure 2.7 shows how these interface traps behave under different modes of operation of a MOS-C. Interface traps are present throughout the energy band gap of SiC. The interface traps from the intrinsic energy level, E_i, to conduction band edge, E_c, behave as acceptor-like traps. An acceptor-like trap is neutral when it is empty and negatively charged when it is filled with an electron. On the other hand, all the traps from intrinsic E_i down to the top of valence band behave as donor-like traps – i.e., neutral when filled with an electron and positively charged when empty. Either trap (acceptor or donor) is considered to have an electron when its energy is below the Fermi level or to be empty when its energy is above the Fermi energy. As we see from figure 2.7(b), for accumulation, these traps cause a net negative charge and for depletion, figure 2.7(c), causes no net charge as all the acceptor like traps are empty and donor like taps are filled. For inversion, figure 2.7(d), these traps lead to a net positive charge at the interface. Since the band bending depends upon the semiconductor surface potential, the occupancy of the interface traps is a function of surface potential ϕ_s. The correction term to flatband voltage for the interface traps is

$$\Delta V_5 = -\frac{Q_{it}\ (\phi_S)}{C_{ox}}$$

Finally then, the flatband voltage, V_{FB}, for a real MOS-C is

$$V_{FB} = V_{FB}\,(\text{ideal}) + (\,\Delta V_1 + \Delta V_2 + \Delta V_3 + \Delta V_4 + \Delta V_5)$$

$$V_{FB} = 0 + \phi_{ms} - \frac{Q_f}{C_{ox}} - \frac{\gamma Q_m}{C_{ox}} + \frac{Q_{ot}}{C_{ox}} - \frac{Q_{it}\,(\phi_S)}{C_{ox}}$$

$$V_{FB} = \phi_{ms} + Q_{eff}$$

where Q_{eff} "effective charge" = $\left[-\frac{Q_f}{C_{ox}} - \frac{\gamma Q_m}{C_{ox}} \pm \frac{Q_{ot}}{C_{ox}} - \frac{Q_{it}\,(\phi_S)}{C_{ox}} \right]$

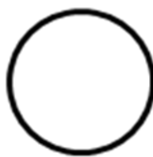
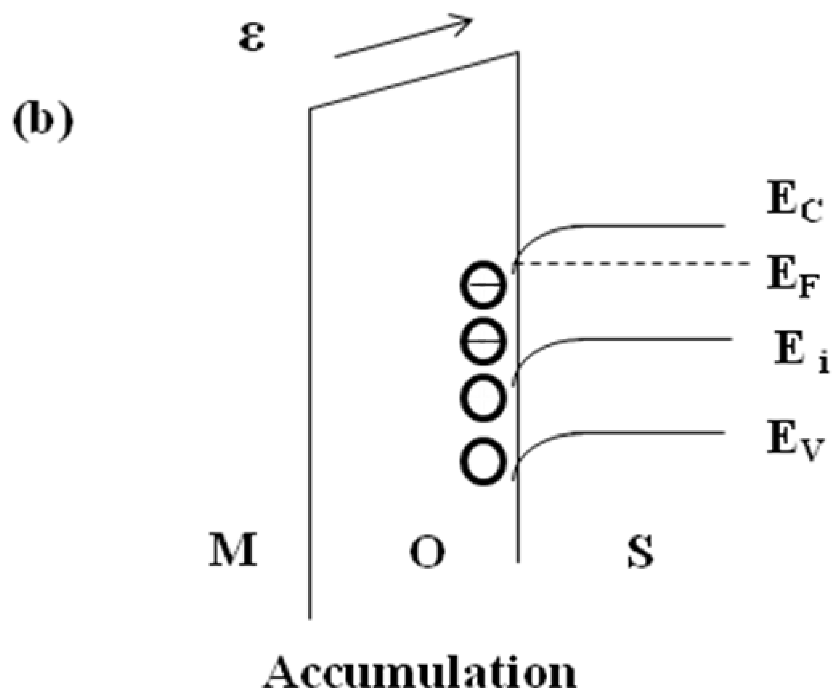
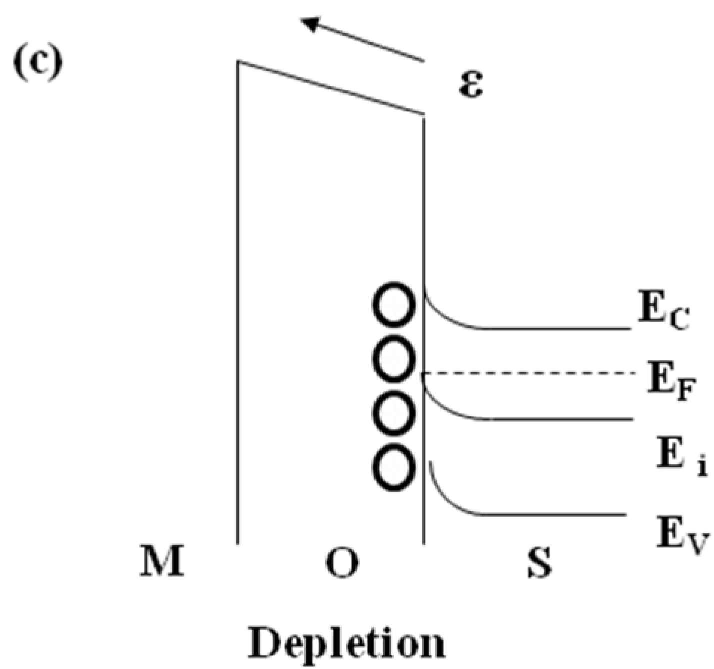


Figure 2.7(a): Pictorial representation of interface traps under different conditions.


ε
(b)
E_C
E_F
E_i
E_V
M
O
S
Accumulation


(c)
ε
E_C
E_F
E_i
E_V
M
O
S
Depletion

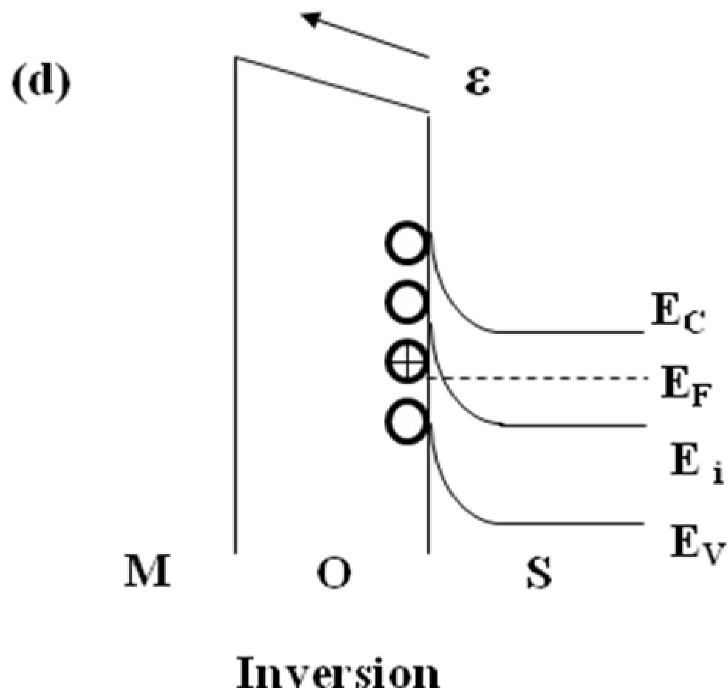


Figure 2.7: The interface trap charges under different mode of a MOS-C.

2.4 High- low capacitance - voltage (C-V) measurement technique

Capacitance is defined as

$$C = \frac{\Delta Q}{\Delta V}$$

where ΔQ is a change in the charge corresponding to a voltage change ΔV [14,15].

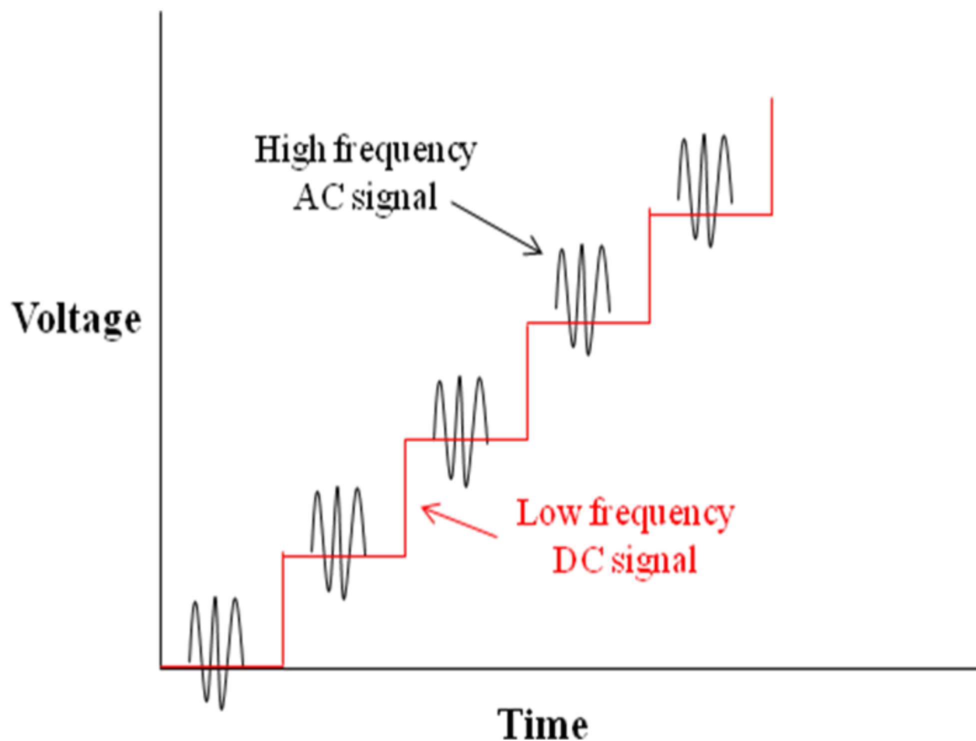


Figure 2.8: DC voltage ramp and AC measurement voltage for capacitance – voltage (C-V) measurement [14].

In a MOS-C, capacitance-voltage measurements are carried out using two simultaneous voltage sources. A DC voltage that is ramped linearly or stepped linearly in time has a small amplitude AC signal superimposed as shown figure 2.8. This makes sure that the measured capacitances reflect interface state reponse at the same surface potebtial.

In the high-low C-V technique, cpaciatnce is measured at two different frequencies – one frequency low enough so that all the interface staes can respond to the signal and one high enough so that all the states at the given surface potential can not respond to the signal. The equivalent model shows that depletion capacitance (C_{dep}) is in parallel with interface trap capacitance (C_{it}) which is in series with oxide capacitnace (C_{ox}). So at low frequency, the capacitance (C_{lf}) is given by

$$C_{lf} = 1 \Big/ \left[C_{ox}^{-1} + (C_{it} + C_{dep})^{-1}\right]$$

solving for Cit and dividing by q gives us the intrrface trap density (D_{it}),

$$D_{it} = \left[\frac{C_{ox}\, C_{lf}}{C_{ox} - C_{lf}} - C_{dep} \right] .1/q$$

The high frequecy capacitance (C_{hf}) is given by

$$C_{hf} = \frac{C_{ox}\, C_{dep}}{C_{ox} + C_{dep}}$$

After solving for C_{dep} we can re-write the expression for D_{it} as

$$D_{it} = \left[\frac{C_{ox}\, C_{lf}}{C_{ox} - C_{lf}} - \frac{C_{ox}\, C_{hf}}{C_{ox} - C_{hf}} \right] .1/q$$

To obtain the profile of D_{it},we need to find the energetic location of the traps. For this, first, the width of depletion region (W_{dep}) is calculated

$$W_{dep} = AK_s K_o \Big/ C_{dep}$$

Then using depletion approximation trap energy os given by

$$E - E_v = E_g/2 - kT \ln(N_{bulk}/n_i) + \phi s$$

Where the surface potential is given by

$$\phi s = qN_{bulk} W_{dep}^2 \Big/ 2K_s K_o$$

Also, $E_c - E_v = E_g$, which allows us to detremine D_{it} profile across the bandgap.

2.5 Data extraction using the C-V technique

A C-V measurement contains a wealth of information. From the measurement, we can extract oxide thickness (t_{ox}), flatband voltage (V_{FB}), metal-semiconductor work function difference (ϕ_{ms}), effective charge (Q_{eff}), threshold voltage (V_T) and the doping profile of the substrate [14,15].

2.5.1 Oxide thickness (t_{ox})

When a MOS-C is in accumulation, the high frequency capacitance is equal to the oxide capacitance (C_{ox}), and the calculation of t_{ox} is straightforward.

$$t_{ox}\,(\text{nm}) = A\,\frac{K_{ox}}{t_{ox}}(\,10^7\,)$$

where

t_{ox} is the oxide thickness in nanometers

A is the area of one plate of MOS-C in cm^2

K_{ox} is the dielectric constant of the oxide in F/cm

C_{ox} is the capacitance in F

2.5.2 Metal-semiconductor work function difference (ϕ_{ms})

The metal-semiconductor work function difference (ϕ_{ms}) causes a shift in V_{FB} from the ideal value of zero. The work function difference, ϕ_{ms}, is given by

$$\phi_{ms} = \phi_m - \phi_s$$

$$= \phi_m - \chi_s + \phi_b - E_g/2$$

where E_g is the band gap energy, ϕ_b is the bulk potential of semiconductor and χ_s is the electron affinity of the semiconductor - i.e., the energy required to move an electron from the bottom of the conduction band to a position at rest infinitely far from the semiconductor.

$$\phi_b = \pm \frac{kT}{q} \ln \frac{N_{bulk}}{N_i}$$

2.5.3 Doping concentration of substrate ($N_{substrate}$)

The substrate doping concentration can be calculated using the following expression

$$N_{substrate} = \frac{2}{qKA^2 \frac{\Delta(\frac{1}{C2})}{\Delta V_G}}$$

where V_G is the gate bias, K is the dielectric constant of the semiconductor, A is the area of one plate of MOS-C in cm^2.

The substrate concentration (N) is related to the reciprocal of the slope of the $1/C^2$ plotted as a function of V_G when this plot is a straight line.

2.5.4 Doping profile

The doping concentration is calculated using the expression

$$N= \left| \frac{-2}{qKA^2 \frac{d(\frac{1}{C2})}{dV}} \right|$$

Here, we make use of a differential capacitance. Differential change in $1/C^2$ is monitored with respect to a differential variation in the gate bias in the depletion region of the MOS-C.

The depth for the doping profile is calculated using

$$W = (\frac{1}{C} - \frac{1}{Cox}) (10^2)$$

K is the dielectric constant of the semiconductor, and A is the capacitor area

2.5.5 Fltatband voltage

For a non-ideal MOS-C, even if there is no bias, there is band bending. To remove band bending, we need to apply a particular bias to the gate, and this bias is called the flatband voltage (V_{FB}). In order to find V_{FB} we need to know flatband capacitance (C_{FB}). C_{FB} is known when we know the Debye length (λ) and the oxide capacitance. To calculate Debye length, we need the bulk doping concentration (N_{bulk}) of semiconductor and the concentration at 90% of W_{max} (W is the width of the depletion layer).

$$C_{FB} = \frac{C_{ox}\left(\frac{K\,A}{\lambda}\right)(10^2)}{C_{ox} + \left(\frac{K\,A}{\lambda}\right)(10^2)}$$

C_{FB} is the flatband capacitance in F

C_{ox} is the oxide capacitance in F

K is the dialectic constant of semiconductor

A is the area of the MOS-C in cm^2

λ is extrinsic Debye length given by

$$\lambda = \sqrt{\frac{K\,kT}{q^2 N}}\,(10^{-2})$$

λ is in meters

kT is thermal energy at room temperature, $4.2 x 10^{-23}$J at 300K

q is the electronic charge, $1.6 x 10^{-23}$C

N is the doping concentration at 90% of W_{max} .

2.5.6 Threshold voltage

A MOSFET starts conducting when an inversion channel region forms between the source and drain regions as the result of the application of gate bias, and the gate voltage corresponding to the onset of conduction is called the threshold voltage (V_T). The formation of a channel in a MOSFET corresponds to the formation of an inversion layer in a MOS-C. When n-type source and drain regions are added to a p-type MOS-C, the structure becomes a lateral, n-channel MOSFET. For a n-type MOS-C we get p-channel MOSFET if we add p-type source and drain regions. At threshold voltage, the semiconductor surface potential is twice the bulk potential. In enhancement type MOSFET, at threshold voltage device starts conducting. Threshold voltage means onset of conduction for a MOSFET and onset of inversion for a MOS-C. For a MOS-C, threshold voltage is given by

$$V_T = V_{FB} + [\frac{Q_{dep} A}{C_{ox}} + 2\phi_b]$$

$$V_T = V_{FB} + [\frac{A}{C_{ox}}\sqrt{4KN_{bulk}|\phi_b|} + 2\phi_b]$$

where ϕ_b is bulk potential and is given by

$$\phi_b = \pm \frac{kT}{q}\ln(\frac{N_{bulk}}{N_i})$$

The positive sign is used for p-type and the negative sigh n-type material,

N_{bulk} is the bulk carrier concentration and N_i is the intrinsic carrier concentration.

2.5.7 Charges in the oxide and at the O-S interface

In the SiO_2/SiC system, we can divide charges mainly into two categories: charges in the oxide and charges at the oxide-semiconductor interface. Charges in the oxide include mobile chare (Q_m), fixed charge (Q_f) and oxide trapped charge (Q_{ot}). These charges are collectively called effective charge (Q_{eff}).

$$Q_{eff} = Q_m + Q_f + Q_{ot}$$

Effective charge is different compared to interface trapped charge (Q_{it}). Interface trapped charge depends upon the surface potential at the O-S interface, while Q_{eff} does not depend upon the gate bias. In order to distinguish between the three components of the effective charge, we have to do temperature cycling during a C-V measurement. Q_{eff} per unit area is given by the following expression

$$V_{FB} - \phi_{ms} = -\frac{Q_{eff}}{C_{ox}}$$

or

$$Q_{eff} = - C_{ox} (V_{FB} - \phi_{ms})$$

Hence, the effective trap concentration is given as

$$N_{it} = \frac{Q_{eff}}{q} A$$

2.6 Metal oxide semiconductor field effect transistor (MOSFET)

One of the most widely used electronic devices is the metal- –insulator-semiconductor (MIS) field-effect transistor. When the insulator is SiO_2, the term metal-oxide-semiconductor (MOS) field-effect transistor (MOSFET) is used. The other name for an MIS transistor is insulated-gate field-effect transistor (IGFET) [4,5,9].

The basic structure of a MOSFET is shown in figure 2.9(a).There is no current through the device until there is a formation of an n-type inversion channel between the source and drain regions. Figure 2.9(b) shows that there is a potential barrier for electrons to move from the source to the drain. The cause of this barrier is a built-in potential due to the p-n junctions between source and drain. When a positive bias is applied to the gate relative to substrate, induced negative charges appear at the O-S interface. This induced charge is formed by the electrons generated in p-substrate and negative uncovered acceptors. This leads to a flow of electrons in the device from source to drain. The direction of current is from drain to source. The gate voltage at which the formation of n-channel takes place is called as threshold voltage (V_T) of the MOSFET. Depending upon the sign of V_T, we can divide MOSFETs in to two categories. There are some n-channel MOSFETs for which there is already a channel even with zero gate bias. These MOSFETs are as called normally on MOSFETs, and one needs to apply a negative gate voltage to deplete the channel which exists at equilibrium.

These are called depletion-mode n-MOSFETs. On the other hand, if we need to apply a positive gate bias to create a channel in an n-MOSFET, then the FET is called as an enhancement-mode MOSFET. Similar definitions apply for a p-channel MOSFET, as well.

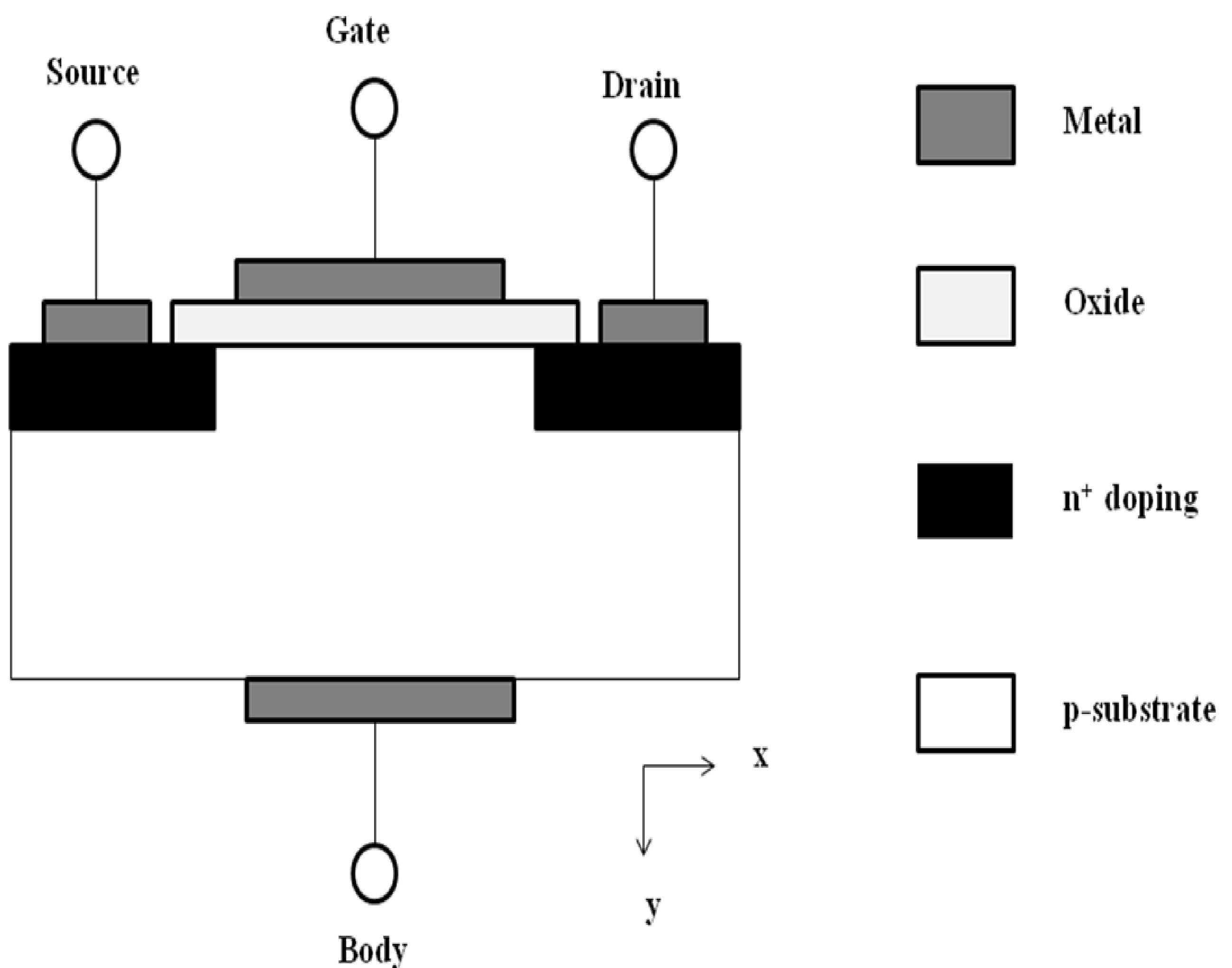


Figure 2.9(a): n-channel lateral MOSFET.

• **Electron** ∘ **Hole** (+) **Ionized donor** (-) **Ionized acceptor**

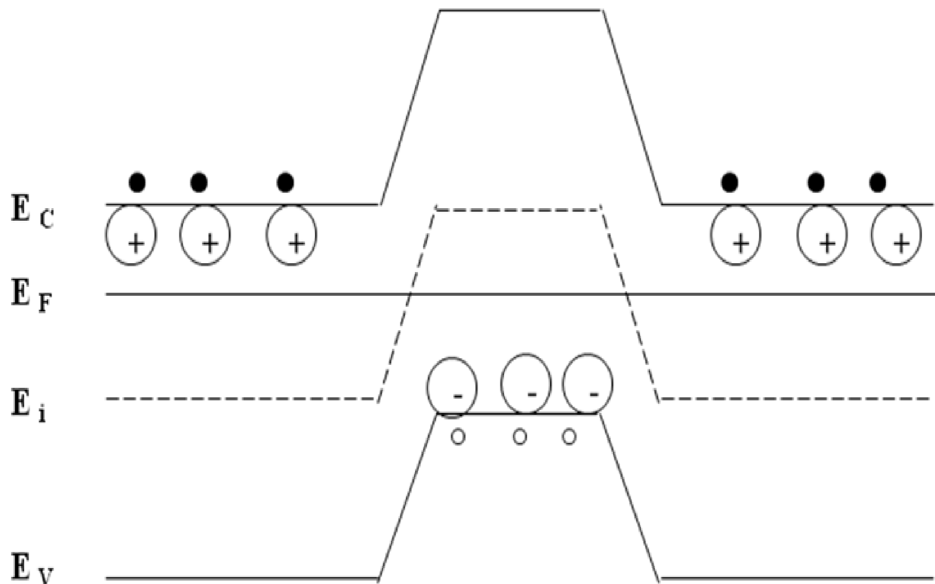


Figure 2.9(b): Energy band diagram of a n-MOSFET along the channel.

A MOSFET can also be considered a voltage controlled resistor. Voltage is applied at the gate terminal of a MOSFET. Let us consider an n-channel MOSFET. If a positive gate voltage, V_G, exceeds the threshold voltage, V_T, an inversion layer forms in the p-substrate at the O-S interface, and a conducting channel is established between the source and drain. The output characteristics of an n-MOSFET are shown in figure 2.10. If we increase the positive bias at gate terminal there will be an increased charge in the inversion layer and hence the drain current increases. This increased current leads to more potential drop along the channel. If the source and body of a MOSFET are grounded, then the potential along the channel

varies from 0V (channel end close to source region) to V_G-V_D at the other end (closer to drain region). If we keep increasing the drain bias, then finally V_G-V_D=V_T, and there is saturation in the drain current. Under these conditions a MOSFET is said to be in a saturation mode.

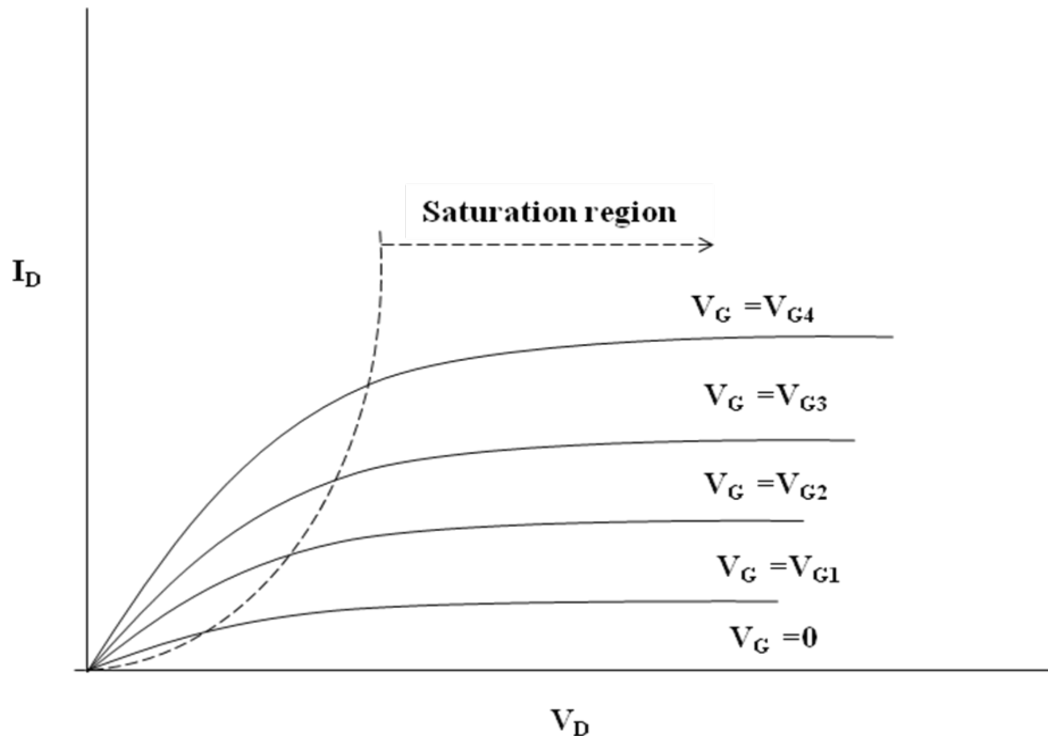


Figure 2.10: Output characteristic of an n-channel MOSFET.

2.7 Electrical characteristics of a MOSFET

2.7.1 Output characteristics

An output characteristic can be the variation of drain current with drain voltage at a constant value of gate bias. The channel current is the result of drift of electrons from source to drain region. Let us define a local electric potential V(x) along the length of the channel. Its value varies from V(x=0) = 0 at the source end to V(x = L) = V_D at the drain end. L is the channel length. We can consider a channel as a simple resistor with an electron current flowing from

source to drain. Let V(x) bes the potential at a point x along the channel. The electric field in the channel is given by

$$E(x) = \frac{dV(x)}{dx}$$

and channel current is

$$J(x) = q\ \mu\ n\ E(x) = q\ \mu\ n \frac{dV(x)}{dx}$$

where μ is inversion channel electron mobility, and n is the concentration of electrons in the channel region. Drain current is

$$I_D = -\ W \int_{y=0}^{\infty} J\ dy$$

where W is the width of the channel region – i.e., the maximum value of y. The inversion charge in the channel region at position x is

$$Q_{inv} = -q \int_{y=0}^{\infty} n(x,y)\ dy$$

Using inversion charge value, current density, J, can be rewritten as

$$J(x) = -W\ Q_{inv}\ \mu \frac{dV(x)}{dx}$$

As there is a channel, we can write the surface potential as

$$\phi_{surface}(x) = 2\phi_F + V(x) \text{ and}$$

$$-Q_G(x) = Q_d(x) + Q_{inv}(x)$$

where

Q_G is the charge on the gate

Q_d is the depletion charge

Q_{inv} is the inversion charge

The potential drop in gate oxide is

$$V_{ox} = V_G - \{V_{FB} + 2\phi_F + V(x)\} = \frac{Q_G(x)}{C_{ox}},$$

And the inversion charge is given by

$$Q_{inv}(x) = C_{ox}\{V_G - (V_{FB} + 2\phi_F + V(x))\}$$

There is a variation of electric potential V(x) along the channel from 0 to V_D. This means there is a variation in the energy band curvature along the y-direction from the substrate towards the channel region. At the source end the energy band curvature is equal to 2 q ϕ_F $_+$qV_S. At the drain end it is equal to 2 q ϕ_F +q V_D .The channel region can be viewed as an n-type slab which forms a p-n junction with a p-type substrate. The electric potential along the length of the slab (in x-direction) varies from V_S to V_D, and as a result, the width of depletion layer also varies. The depletion layer charge in a strong inversion at any point x is

$$Q_{dep}(x) = -\sqrt{2qK_S N_a(2\phi_F + V(x))}$$

Integrating the equation

$$I_D = -W\, Q_{inv}\, \mu \frac{dV(x)}{dx}$$

from source to drain gives

$$I_D \int_{x=0}^{x=L} dx = -W\,\mu \int_{V_D}^{V_S} Q_{inv}(x)\, dV(x)$$

Using expression for $Q_{inv}(x)$ we have

$$I_D = \mu\, C_{ox}\, \frac{W}{L} \int_{V_D}^{V_S} \{V_G - [V_{FB} + 2\phi_F + V(x)] - \sqrt{2qK_S N_a[2\phi_F + V(x)]}/C_{ox}\}.$$

Let us define

$$\eta = \frac{\sqrt{2qK_S N_a}}{C_{ox}} .$$

then if $V_{DS} = V_D - V_S$,

$$I_D = \mu\, C_{ox}\, \frac{W}{L} \{ (V_G - V_{FB} - 2\phi_F - \frac{V_{DS}}{2})\, V_{DS} - \frac{2}{3}\, \eta\, [(2\phi_F + V_D)^{\frac{3}{2}} - (2\phi_F + V_S)^{\frac{3}{2}}]\}$$

This expression gives the drain current as a function of gate, source and drain voltages. Note that substrate is grounded. The drain current is maximum at V_{DSAT} , which is the saturation drain voltage calculated by setting

$$\frac{dI_D}{dV_D} = 0$$

$$V_{DSAT} = V_G - V_{FB} - 2\phi_F + \frac{\eta^2}{2} - \eta\sqrt{V_G - V_{FB} + \frac{\eta^2}{4}}$$

At the drain saturation voltage, the drain current is called as a saturation drain current, and an expression for it can be obtained by putting the value of V_{DSAT} into the equation for I_D. At saturation, Q_{inv} (L) = 0, and the channel gets pinched-off near the drain region. At pinch-off, the local potential on the drain side of the channel is V_D - V_{DSAT}, and the presence of a high electric field between this pinch-off point and the drain causes the drift of electrons from channel into the drain. The magnitude of the current depends upon the difference, V_D - V_{DSAT}, and hence it is constant, independent of drain voltage as shown in figure 2.9.

The expression derived here for drain current can be simplified if we consider that there is no variation of depletion charge with drain voltage i.e., that its value is simply equal to the depletion charge, Q_{dep}, at the threshold voltage with no drain current. This approximation is fairly accurate for low values of V_D. Under this assumption, I_D is given by

$$I_D = \mu\, C_{ox}\, \frac{W}{L} \{ (V_G - V_T)\, V_D - \frac{V^2{}_D}{2}\}$$

If $V_G > V_T$ and the drain voltage is small, I_D is

$$I_D = \mu C_{ox} \frac{W}{L} (V_G - V_T) V_D$$

So the drain current varies linearly with drain voltage at a constant gate bias, and the transistor is said to be in a linear region. The conductance of the transistor is given by

$$g = \frac{dI_D}{dV_D} = \mu C_{ox} \frac{W}{L} (V_G - V_T)$$ assuming no variation of μ with V_G.

In this linear regime at saturation where $V_{DSAT} = V_G - V_T$, the saturated drain current is

$$I_{DSAT} = \mu C_{ox} \frac{W}{2L} (V_G - V_T) V_{DSAT}$$

$$I_{DSAT} = \mu C_{ox} \frac{W}{L} V^2{}_{DSAT}$$

The transconductance in the saturation is

$$g_m = \frac{dI_D(sat)}{dV_G} = \mu C_{ox} \frac{W}{L} (V_G - V_T)$$

2.7.2 Transfer characteristics

Transfer characteristics are shown in figure 2.11 as the variation of drain current with gate

bias at a constant drain voltage. In a linear regime, drain current varies linearly with gate bias.

$$I_D = \mu C_{ox} \frac{W}{L} (V_G - V_T) V_D$$

The zero drain current intercept of the linear portion of the curve gives the threshold voltage of the MOSFET, and the slope gives mobility μ. At higher gate voltages there is a deviation from linearity. The cause of this non-linear behavior is source-drain resistance (R_{SD}), and a mobility dependence on the electric field as the gate bias is increased.

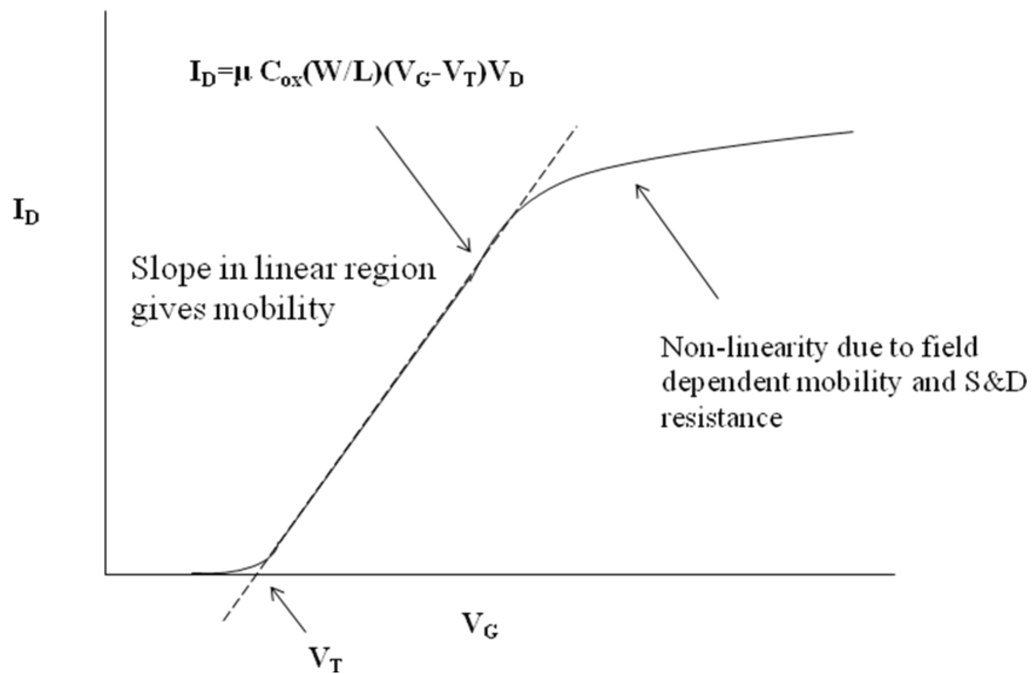


Figure 2.11: Transfer characteristic of n-channel MOSFET in a linear regime.

For the work described herein, we fabricated lateral SiC-MOSFETs and used the linear model to characterize them. Our research focus was to improve the interface quality of the SiO_2 / 4H-SiC interface by using phosphorous passivation and nitrogen plasma passivation. Results are compared to those using standard NO passivation. Interface quality is currently the limiting factor in 4H-SiC MOSFET performance.

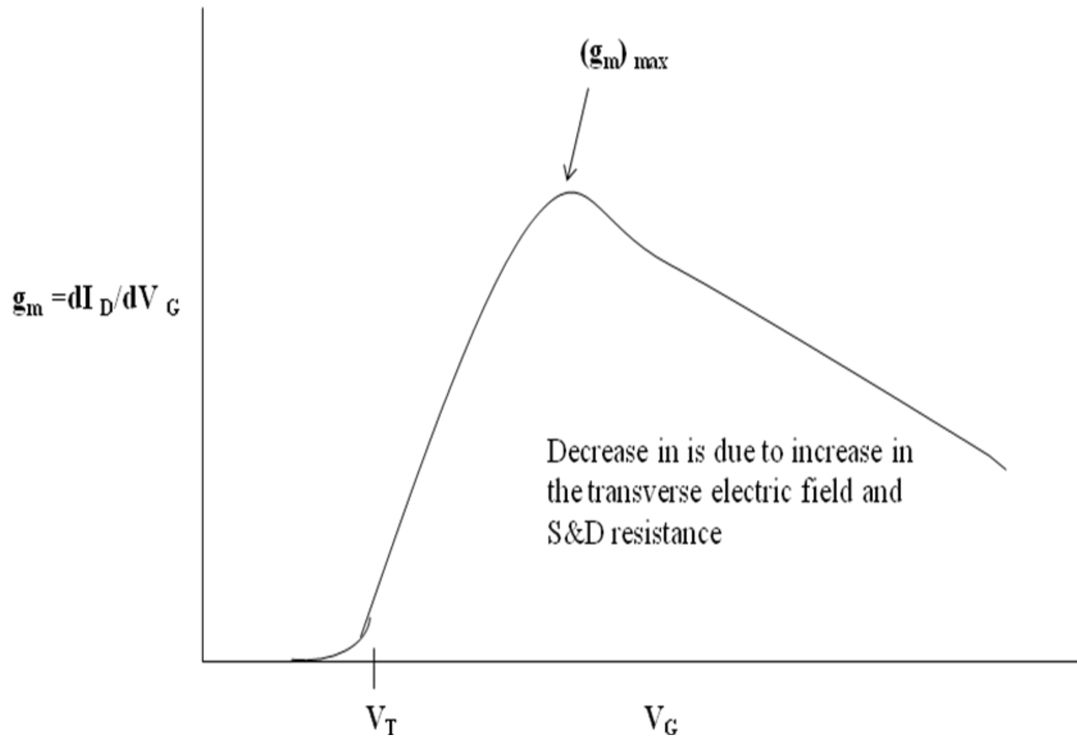


Figure 2.12: Transconductance of an n-channel MOSFET in linear regime.

The variation of transconductance in the linear region is shown in figure 2.12. For a gate bias less than the threshold voltage, there is a very small drain current, and as a result, the transconductance is almost zero. The initial increase in g_m is followed by a decrease caused R_{SD} and the increased transverse electric field at higher gate bias.

The square root of the saturation current, I_{DSAT}, is plotted as a function of gate voltage for in figure 2.13 for the linear regime. The zero current intercept gives the threshold voltage.

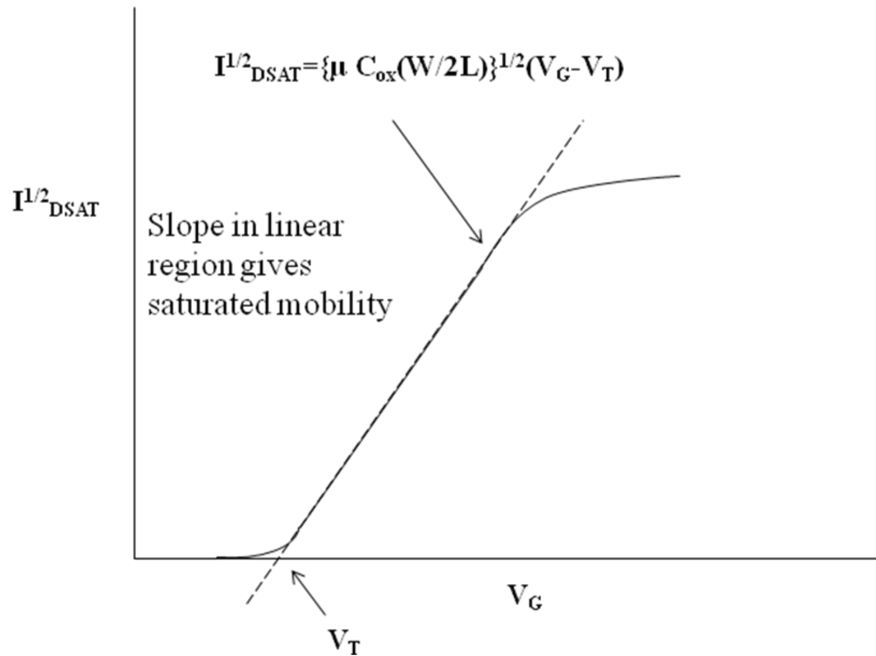


Figure 2.13: Saturated transfer characteristics of a n-channel MOSFET in linear regime.

2.8 Effect of substrate bias on threshold voltage

The threshold voltage of a MOSFET when the substrate is grounded is given by

$$V_T = V_{FB} \pm [\frac{A}{Cox}\sqrt{4\,Ksq\ |Nbulk\phi b|} + 2\phi_b]$$

and can be rewritten as

$$V_T = V_{FB} + 2\phi_b + \eta\sqrt{2\phi_b}$$

where $\eta = \frac{\sqrt{2qK_SN_a}}{C_{ox}}$

If a negative bias is applied to the substrate, V_T becomes

$$V_T = V_{FB} + 2\phi_b + \eta\sqrt{2\phi_b - V_{sub} + V_s}$$

This equation is a general definition of the threshold voltage and is valid for any source and substrate bias.

2.9 References

[1] L. M. Terman, *Solid-State Electron* **5**, 28 (1962).

[2] Robert F. Pierret, *Field Effect Devices*, (Prentice Hall, 1990).

[3] N. Klein, *IEEE Trans Electron Dev.* **13**, 788 (1966).

[4] B. Streetman and S. Banerjee, *Solid State Electronic Devices,* (Prentice Hall, 2005).

[5] S. Sze and K. Ng, *Physics of Semiconductor Devices*, (John Wiley and Sons, 2007).

[6] J. E. Lilienfeld, *Method and Apparatus for Controlling Electric Currents* (1930).

[7] M. M. Atalla, AT&T Tech. J. **38**, 749 (1959).

[8] D. Kahng, *Electric filed controlled semiconductor device*, (1963).

[9]J. P. Colinge and C. A. Colinge, *Physics of Semiconductor Devices*, (Kluwer Academics, 2002).

[10] D. K. Schroder, *Semiconductor Material and Device Characterization*, (Wiley – IEEE Press, 2006).

[11] B. E. Deal, *J. Electro. Soc*. **121**, 198C (1974).

[12] B. E. Deal, *IEEE Trans. Elec. Dev.* **27**, 606 (1980).

[13] V.V. Afanasev, M. Bassler, G. Pensl, and M. Schulz, *Phys. Sta.sol.(a)* **162**, 321 (1997)

[14] http://www.keithley.com/knowledgecenter.

[15] *User Guide, Model 82 –WIN Simultaneous C-V. Keithley Instruments, Inc.*

CHAPTER 3

Device processing

SiC wafers used for the research were provided by Dow Corning and Cree, Inc. MOS capacitors were fabricated on n^-/n^+, 4° and 8° off-axis material with an epilayer doping concentration of $8.3x10^{15}cm^{-3}$. The thickness of the epilayer was 5µm. These wafers were diced into 5mm x 5mm pieces (samples). Samples were cleaned using both organic and Radio Corporation of America (RCA) cleaning processes. Thermal oxidation of the samples was performed at 1150°C in oxygen for different time intervals. The flow rate was set at 500sccm. The oxide growth rate under these conditions was ~7nm/min. 275nm high purity molybdenum gate contacts were deposited by sputtering, and backside ohmic contacts were formed using the silver colloidal paste.

Lateral MOSFETs were fabricated on a 4° off axis 5µm p-epilayer grown on an n^+ substrate. The epilayer was doped with aluminum at $8x10^{15}cm^{-3}$. Source and drain regions were formed by nitrogen implantation at 700°C with different doses and energies to form a $5x10^{19}$ cm^{-3} box profile with an n^+/p junction depth around 400nm. Nitrogen implants were activated at 1550°C for 30min in an Argon ambient. A sacrificial oxide layer of 30nm thickness was grown and removed using Buffered Oxide Etch (BOE) prior to gate oxide growth. NiV7% was sputtered (~120nm) above the source and drain regions for ohmic contacts. High-purity molybdenum (~150nm) was then deposited for the gate contacts. After gate contact deposition, ohmic annealing of source and drain contacts was carried out at 950°C for 30sec in an Argon ambient. The length and width of source and drain were 200µm and 400µm, respectively. The gate length was 120µm.

Figure 3.1 shows the clean room used for device processing.

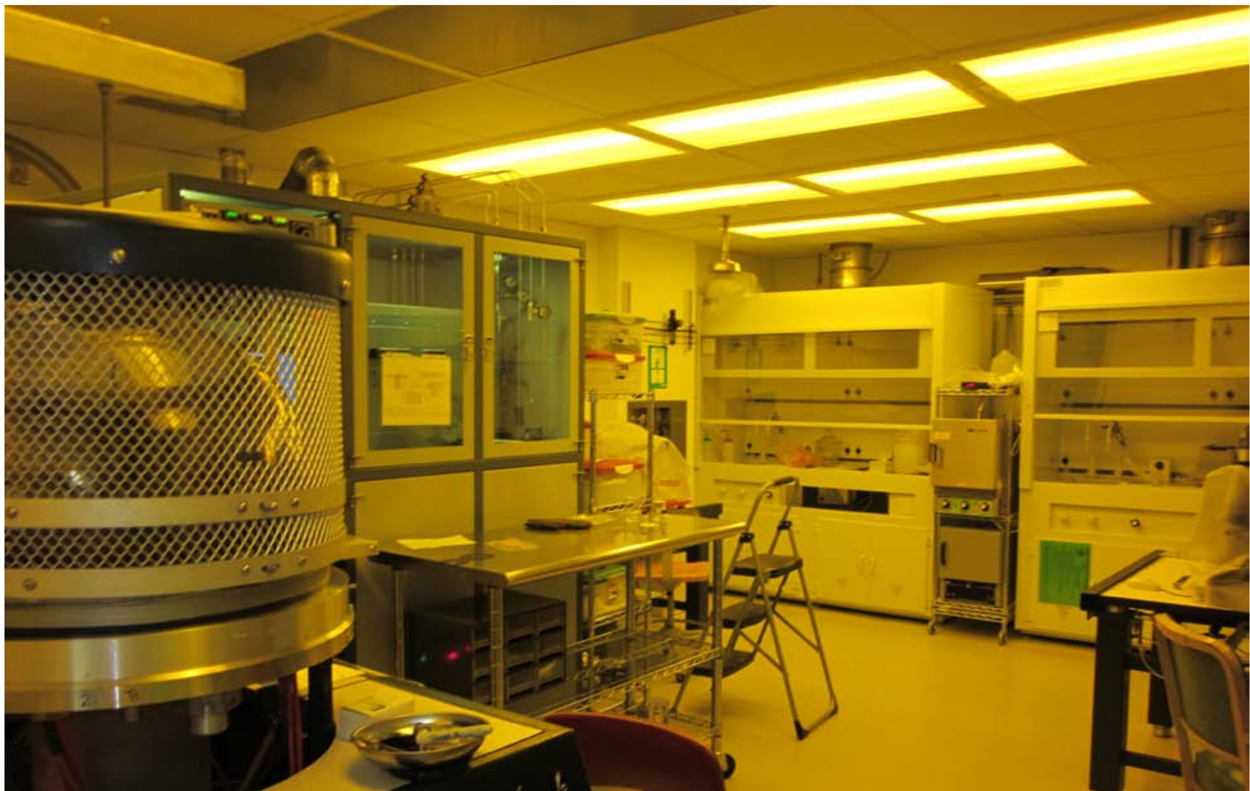


Figure 3.1: Clean room.

3.1 Sample Cleaning

Sample cleaning can be divided in to two parts - organic cleaning and Radio Corporation of America (RCA) cleaning.

3.1.1 Organic cleaning

Organic cleaning is done to remove oils and organic residues that appear on glass surfaces [1,2]. For SiC, the organic cleaning procedure uses acetone, trichloroethylene, acetone, methanol, and methanol. The cleaning process is carried out in a fume hood (figure 3.2).

Each of the organic cleaning steps takes five minutes in an ultrasonic cleaner. Particles ranging in sizes from several micromeres to a tenth of a micron can be removed using ultrasonic waves [3]. First acetone and trichloroethylene is used for complete organic degreasing. Second, acetone serves as the solvent to dissolve trichloroethylene, and methanol is the solvent for acetone. Finally, methanol is used to further clean organic solvents. The sample is then rinsed in deionized (DI) water and blown dry using nitrogen gas.

Figure 3.2: Fume hood for sample cleaning.

3.1.2 RCA cleaning

This cleaning is done to remove organic, ionic and metallic impurities from the sample [1,2]. First, the sample is immersed in buffered oxide etch (BOE) for five minutes to remove a thin layer of native oxide, and then it is rinsed in DI water. Next the sample is immersed in a piranha etch solution (H_2SO_4+H_2O_2) with a volume ratio of 1:1. The piranha etch is used to remove heavy organic materials such as photoresist and other visible contaminations of organic nature. The sample is rinsed well in DI water and immersed in BOE for one minute. The sample is rinsed again in DI water and immersed for 15min in a heated (~100°C) solution of DI water, ammonium hydroxide and hydrogen peroxide (3:1:1). This solution dissolves many metallic contaminations: copper, for example, forms $Cu(NH_3)_4^{+2}$ amino-complex. The next step is again the cleaning sequence of DI water and BOE. To dissolve alkali ions and metal hydroxides, a strong acidic solution of DI water, hydrochloric acid, and hydrogen peroxide (3:1:1) is used for 15min at 100°C. Next the sample is rinsed in DI water and immersed in BOE for one minute. Finally, it is well rinsed in DI water and blow-dried using nitrogen gas.

3.2 Oxidation

The oxidation of SiC is a very important processing step. The performance of an MOS device critically depends upon the quality of the oxide layer. Of many oxidation processes, thermal oxidation is the process most commonly used to form the interface (SiC/SiO_2). Thermal oxidation is carried out in an oxygen (O_2) ambient (500sccm) at 1150°C. The thermal oxidation process has been analyzed both experimentally and theoretically. First-principles calculations by Di Ventra et al. [4] showed that during thermal oxidation, atomic oxygen diffused onto the surface of SiC and formed an advancing interface (SiC/SiO_2). Tan et al. [5] confirmed experimentally that the excess carbon atoms diffused out as CO. In case of a thick

oxide layer, their simulations show that CO may break up either in SiO_2 bulk or at the interface (SiC/SiO_2). The released oxygen participates in another round of oxidation, and the carbon atoms may lead to the formation of carbon clusters. Di Ventra et al. also suggested the formation of carbon dioxide (CO_2) while CO was emitted out through a thick oxide layer. Kanup et al. [6] developed theoretical predictions of the formation of stable carbon pairs and carbon interstitials. These defects combined with silicon interstitials form near-interface traps (N_{IT}). Near-interface traps are more critical compared to bulk traps for the mobility of SiC MOSFETs. The oxidation process can also cause the injection of carbon into SiC substrate. This injected carbon can exist in different forms such as carbon interstitials (C_i) and carbon di-interstitials $(C_i)_2$ to further degrade the FET channel mobility [7,8].

In addition to formation by thermal oxidation, SiO_2 can also be deposited on SiC using chemical vapor deposition (CVD), pulsed layer deposition or sputtering. In this work, thermal and deposited oxides have been used to form the interface. The low pressure CVD system shown in figure 3.3(a) was used to deposit both thick and thin oxide layers. High purity quartz (GE 224) furnace tube was used for thermal oxidation, figure 3.3(b). The tube has gas inlets for O_2, N_2 and Ar. The furnace tube is 48in long, 4in in diameter with a maximum operating temperature of 1200°C.

Figure 3.3(a): LPCVD system (NanoH CVD™) used to deposit SiO_2 on SiC.

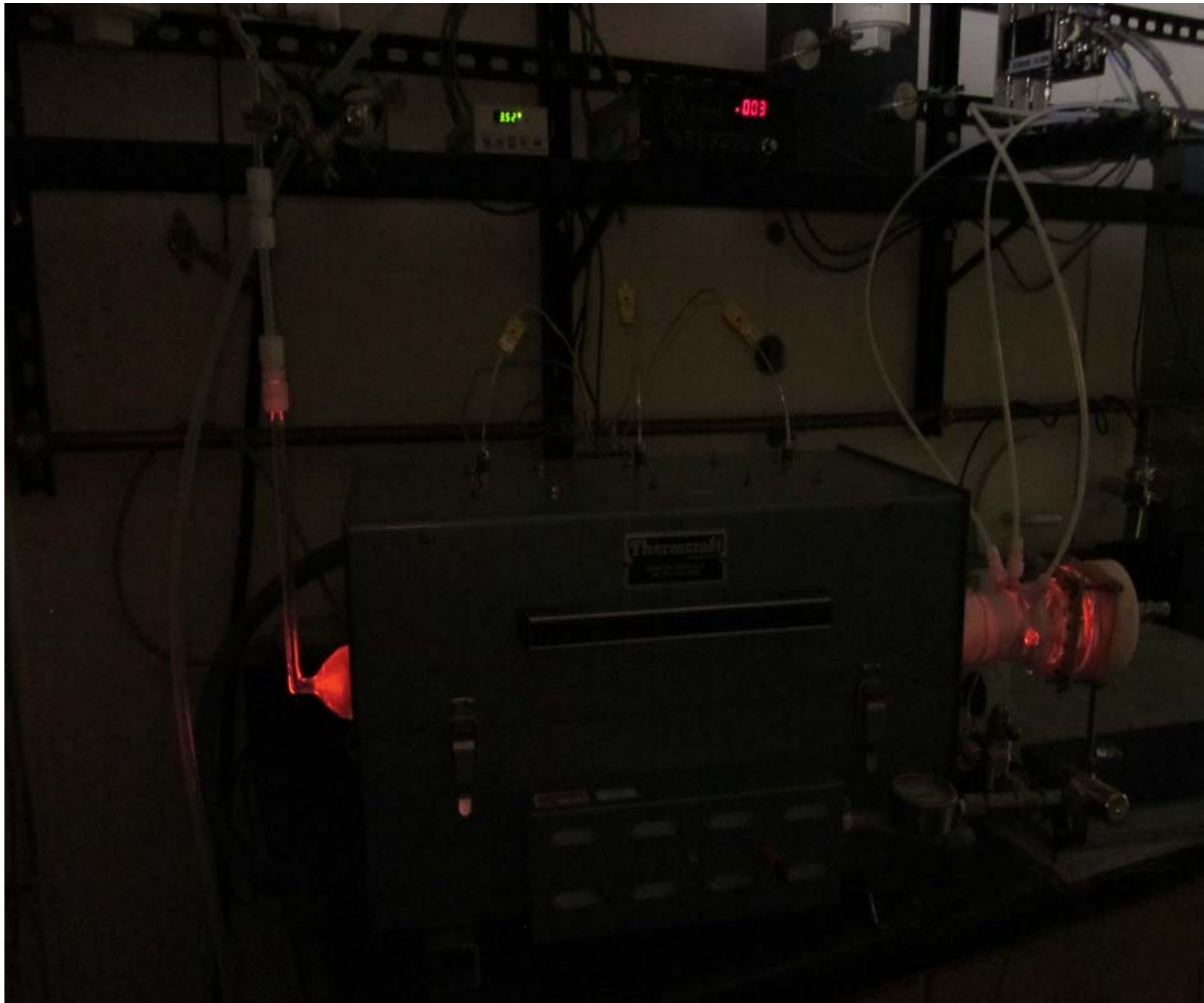


Figure 3.3(b): Thermal oxidation furnace.

The oxidation rate of SiC depends upon the orientation of SiC wafer. This has been determined experimentally by Shenoy et al. [9]. The oxidation rate for C-face is 3-5 times faster than for the Si-face. Alumina enhanced oxidation (AEO) is very fast due to the Na that is released from the alumina at the oxidation temperature. AEO on Si-face at 1050°C gives growth rate which is ten times faster than normal thermal oxidation at 1150°C [10].

3.3 Photolithography

The complex patterns of electronic circuitry can be formed using photolithography. Photolithography is the most critical step during the device processing since this step defines the device dimensions and the resolution that can be achieved. Patterns are transferred from a photo-mask to a light sensitive chemical, photoresist, on the SiC sample. There are two typical categories of photo-masks: clear field masks, which have a clear background and opaque images; and dark field masks, which have an opaque background and clear images. There are transparent and opaque regions on a mask. Opaque regions block ultra violet (UV) light. A Karl Suss MJB3 photo-mask aligner is shown in figure 3.4(a). The 5mm x 5mm (or 10mm x 10mm) sample is first attached to a three inch silicon wafer, using photoresist for a mechanical support. Shipley AZ5214E photoresist is spun on the sample for 30 seconds at 4,000 revolutions per minute to get a uniform layer of photoresist (1.5μm). The photoresist is prebaked at 110°C for one minute, to make it UV light-sensitive. The sample is aligned under mask, and then it is exposed to a 160W ultra violet (UV) source for 30 seconds. The sample is developed in a 1:4 diluted AZ 400K developer for about 30 seconds.

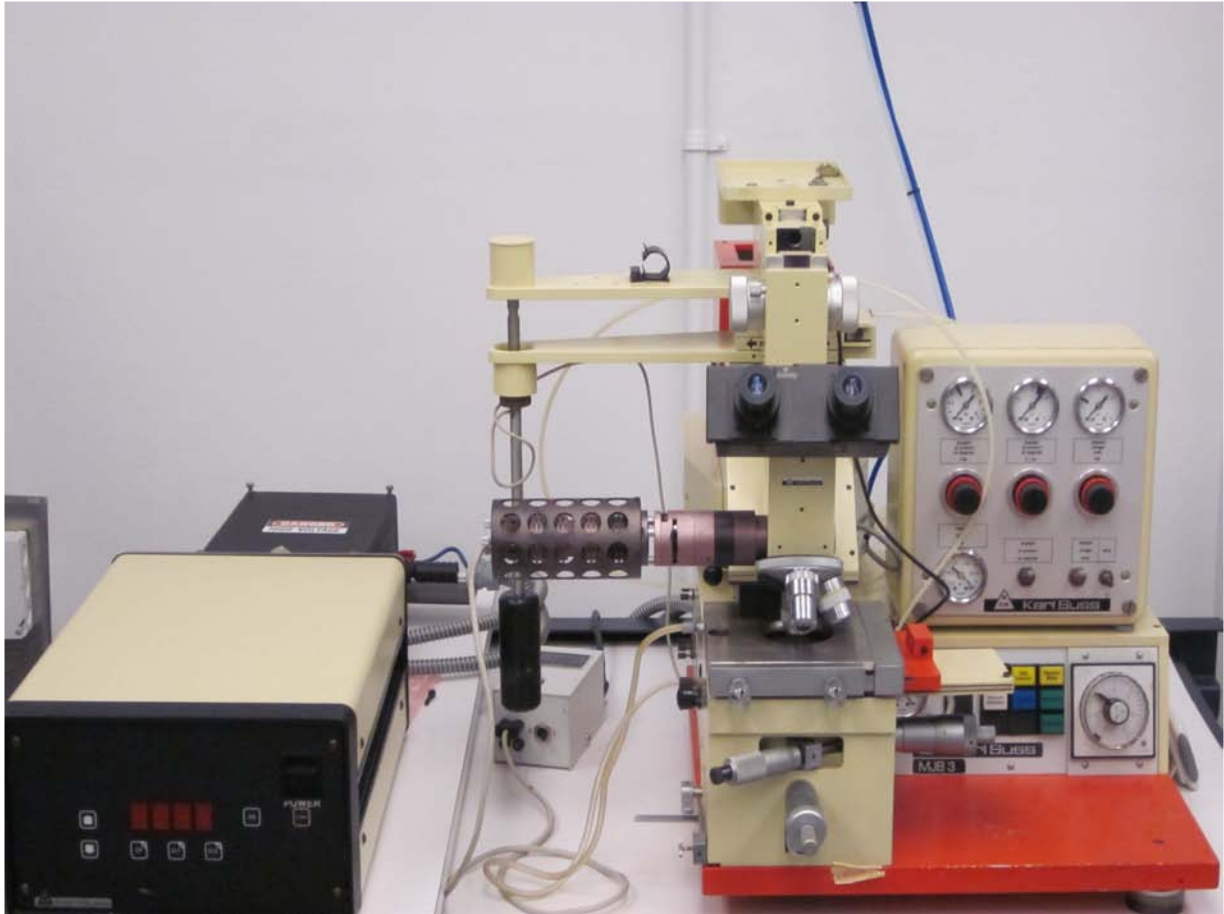


Figure 3.4(a): Karl Suss MJB3 photo-mask aligner.

There are two types of photoresist - positive photoresist and negative photoresist. For a positive photoresist, UV exposed regions on the sample are dissolved when it is immersed in a developing solution, figure 3.2(b). Figure 3.2(c) shows the pattern on the sample after using a negative photoresist.

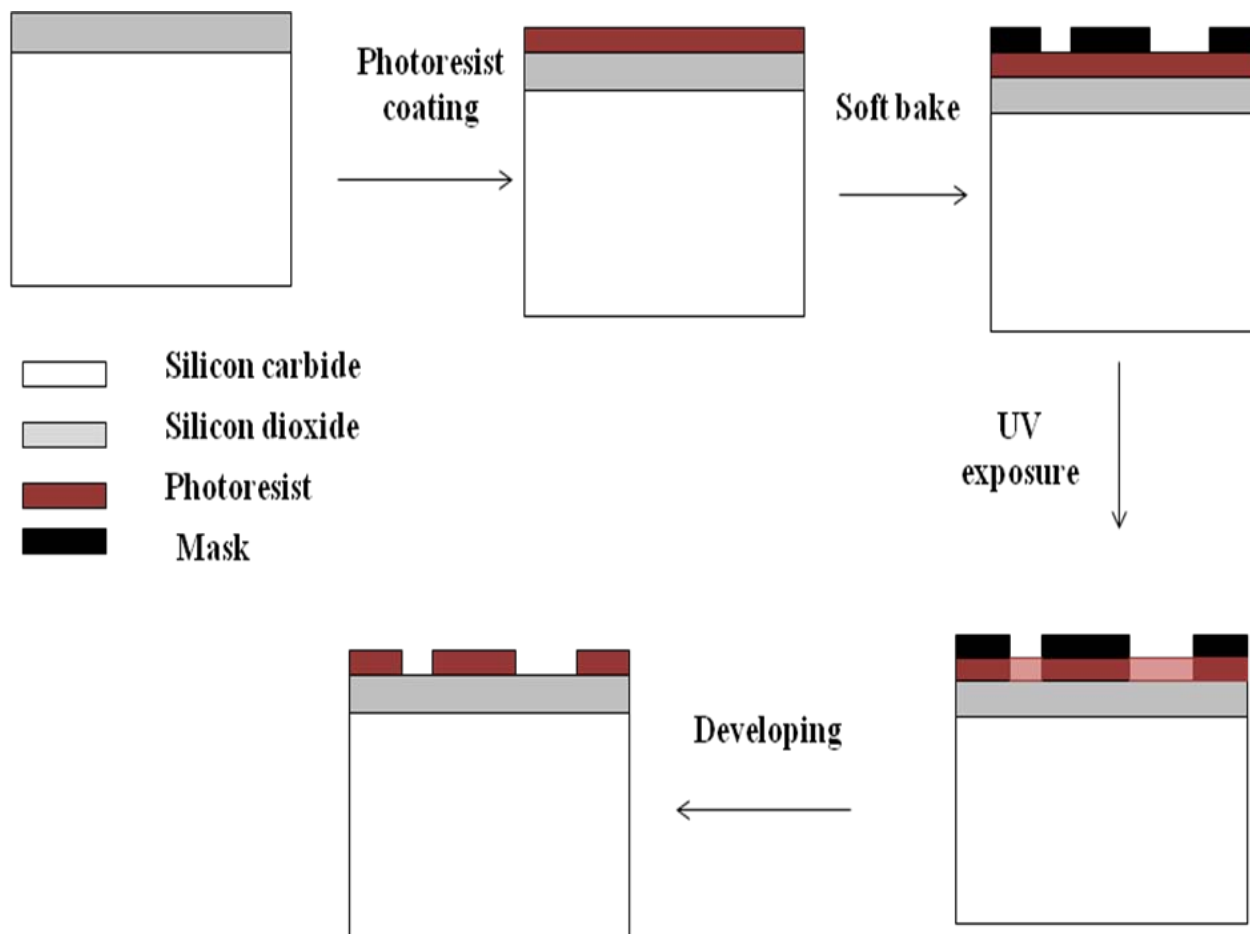


Figure 3.4(b): Photolithography and positive photoresist.

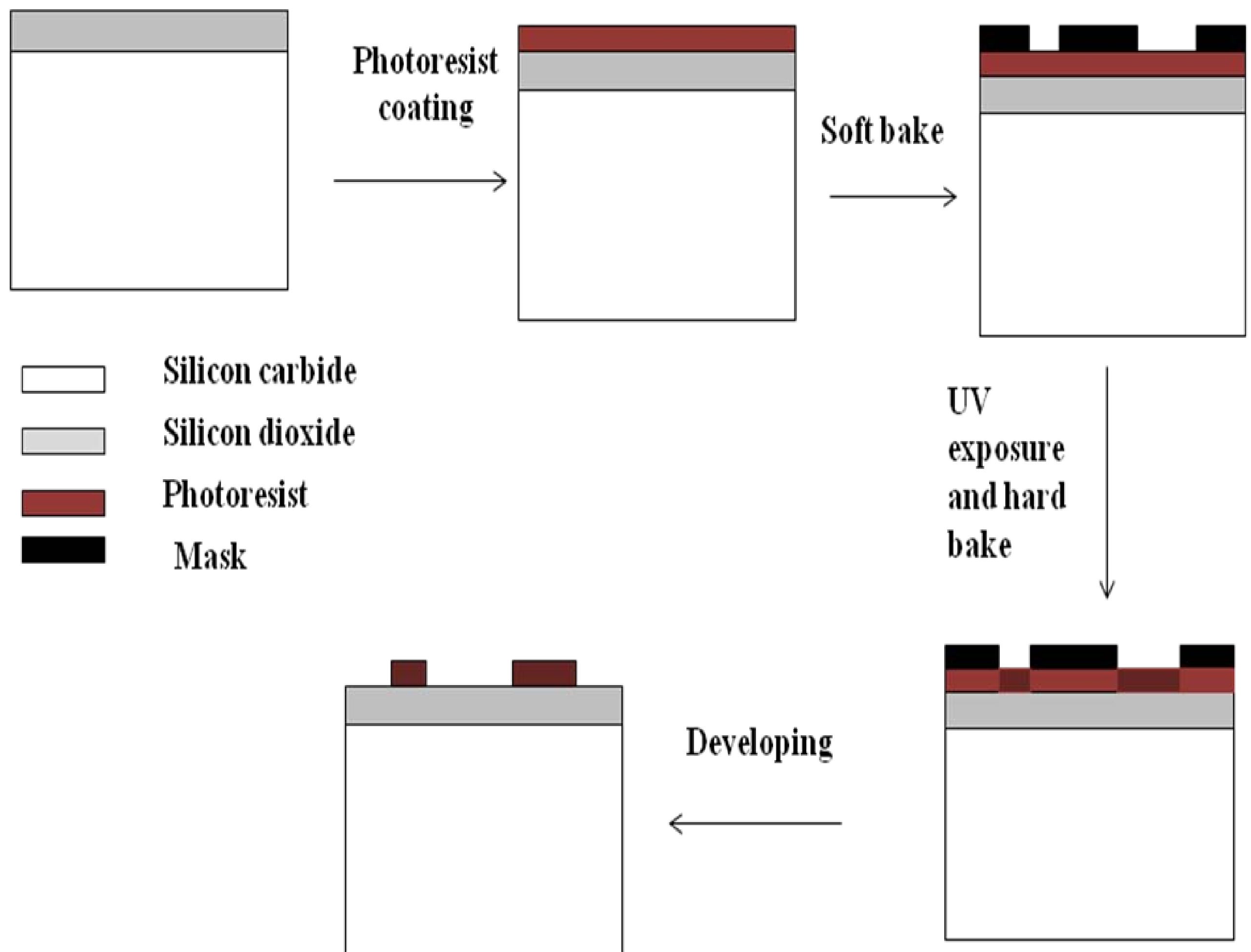


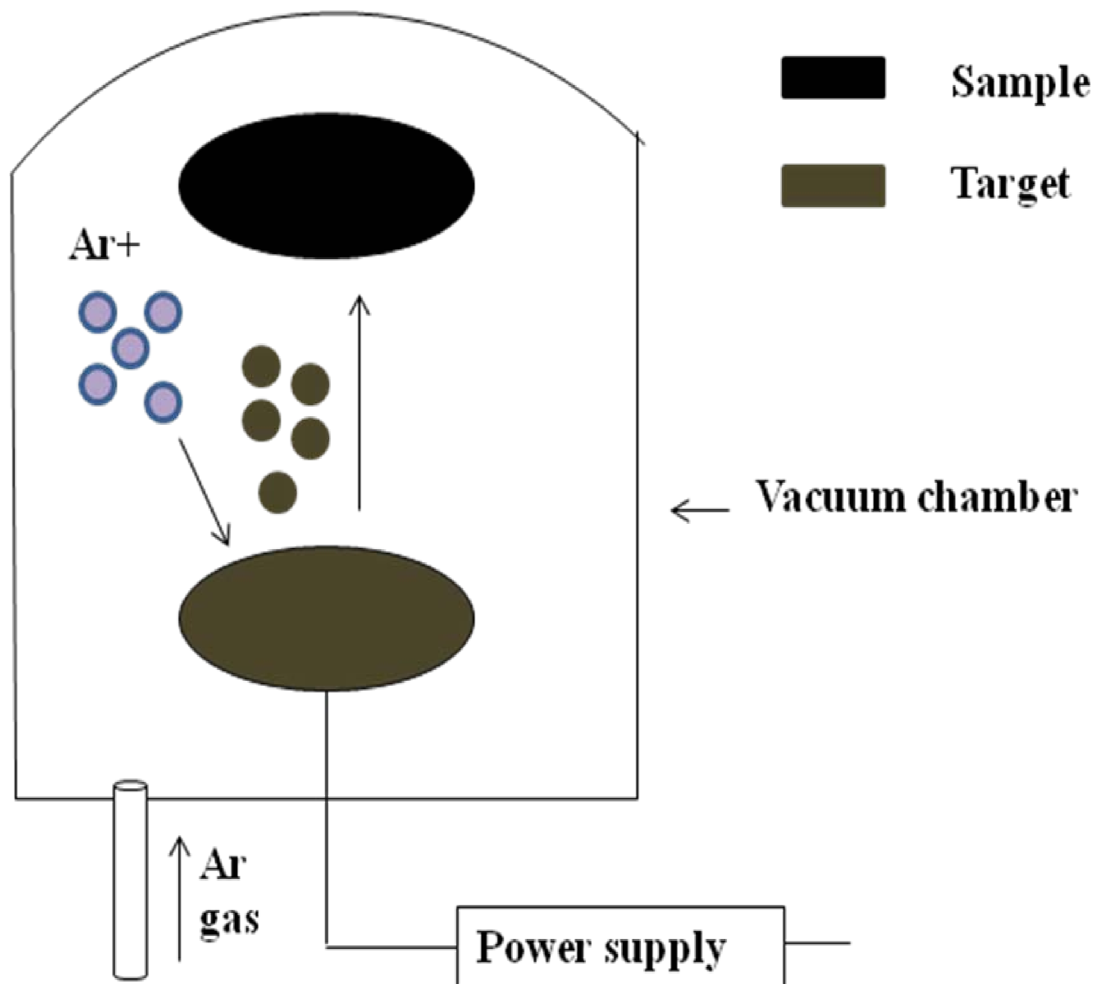
Figure 3.4(c): Photolithography and negative photoresist.

A double exposure is required when inverse photolithography is needed. Between the two exposures there is another bake at 100°C for sixty seconds. The second exposure is done without any mask.

3.4 Sputtering

Magnetron sputtering systems are widely used for thin-film deposition. Sputter deposition is performed at a low pressure (~100mT of Argon gas) in a vacuum chamber. A typical system is shown in figure 3.5(a), and figure 3.5(b) explains the system's working mechanism. This is a direct current (DC) magnetron sputtering system. Substrate (sample) and the material that is to be deposited (target) form a parallel plate capacitor. A high voltage is applied between these two plates such that a strong electric field exists between the target and the substrate. During sputtering, ions of inert gas (Argon) are accelerated into the target by the electric field where they collide with and eject atoms of the target material. The sputtered atoms are ejected from the target and deposited onto the sample. Before deposition, the vacuum chamber is evacuated to a base pressure of $4x10^{-7}$Torr. Argon is introduced into the chamber at a flow rate of 100sccm, and the pressure in the chamber is stabilized to 20mTorr for five minutes. A pre-sputtering process is used to remove trapped impurities at the surface of the targets. Depending on the target metal, this process requires thirty seconds to five minutes. After pre-sputtering, the sample is positioned at about 4in above sputter target. Approximately 150nm of molybdnum is sputtered to from the gate contacts on our SiC-MOSFETs. 120nm nickel-vanadium (Ni/V, 93/7 wt %) is sputtered to form ohmic contacts on the source/drain regions of the devices [11].

Figure 3.5(a): DC magnetron sputtering system.



3.5(b): Working mechanism of sputtering.

3.5 Lift - off

Lift-off is the procedure that is used to pattern metal films on the sample. First, the pattern is defined on the sample by applying and exposing photo-resist. Metal is then sputter deposited all over the patterned sample. The sample is then exposed to acetone which is a solvent for

the photoresist. Areas where no metal is required are protected by the photoresist. Acetone, in the process of dissolving the photoresist, also removes the metal deposited on top of it. Afterwards, the sample is washed with methanol to make sure that there is no remnant of acetone. Finally, it is rinsed in DI water and blow-dried using nitrogen gas.

3.6 Etching

Etching is used to remove a layer or define a pattern on the sample. There are two types of

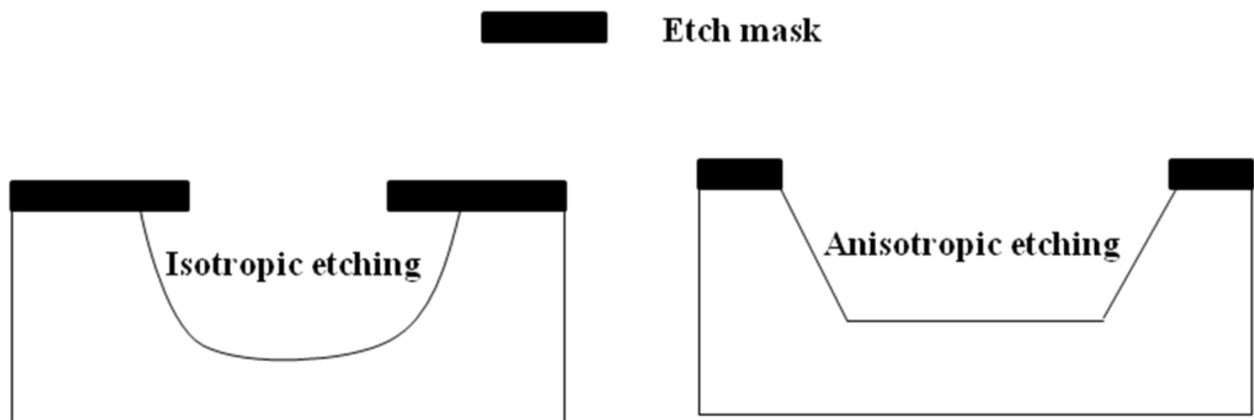


Figure 3.6(a): Wet etching.

Figure 3.6(b): Dry etching.

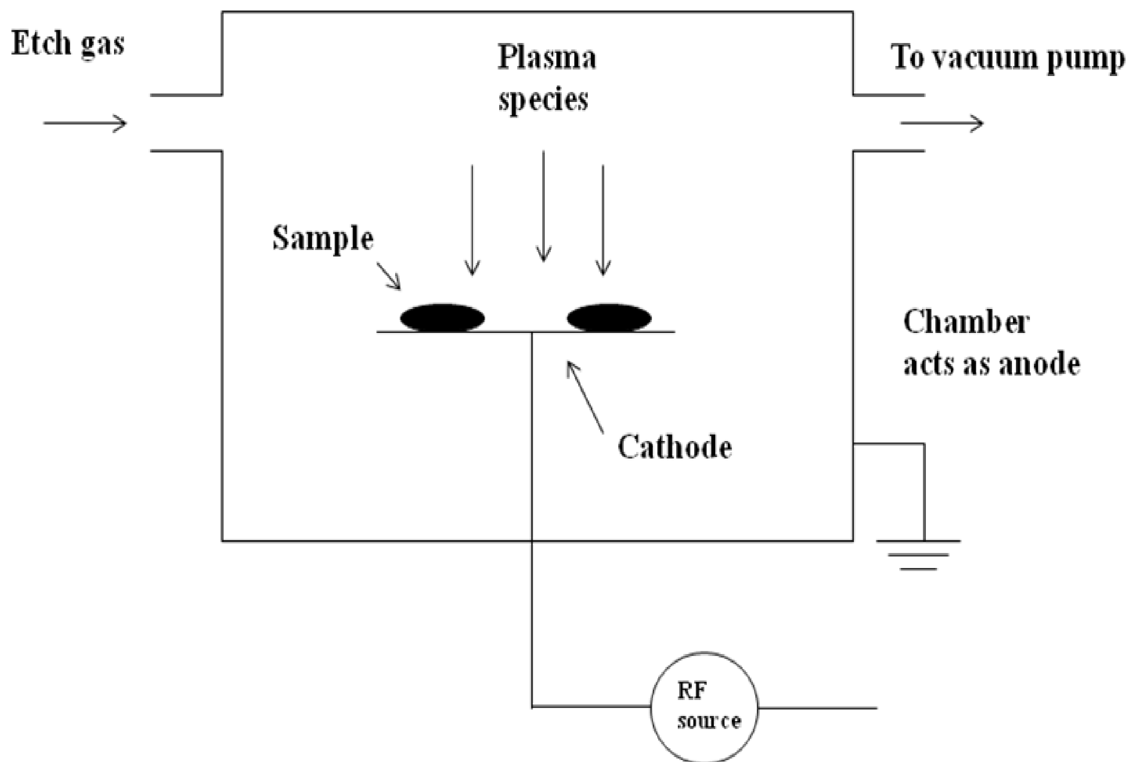


Figure 3.6(c): Working mechanism of an RIE (Reactive Ion Etching) system.

etching: dry etching [or reactive ion etching (RIE)] and wet etching. Wet etching is fast and more selective. For example, hydrofluoric acid (HF) etches SiO_2 but not etch Si or SiC [12]. Wet etching is also isotropic in nature. It etches in the vertical and horizontal directions with same rate, figure 3.6(a). Dry etching involves a plasma formation in which there are chemically reactive species. In case of dry etching, we can achieve both selectively and anisotropy, figure 3.6(b). Apart from these advantages of using plasma etching system, we

can also achieve reactions which are only possible at high temperatures. This is possible because the equivalent temperature of the electrons is very high because of the inefficient energy transfer mechanism between the plasma electrons and the ions. To etch SiC, a plasma formed with NF_3 gas is used [13]. The working mechanism of a typical RIE system is shown in figure 3.6(c). Our RIE system is shown in figure 3.6(d). The system is comprised of a cylindrical vacuum chamber, an isolated sample holder, an impedance matching unit (Advanced Energy's ATX-600) and an 13.65MHz RF power supply (Advanced Energy's RFX-600).

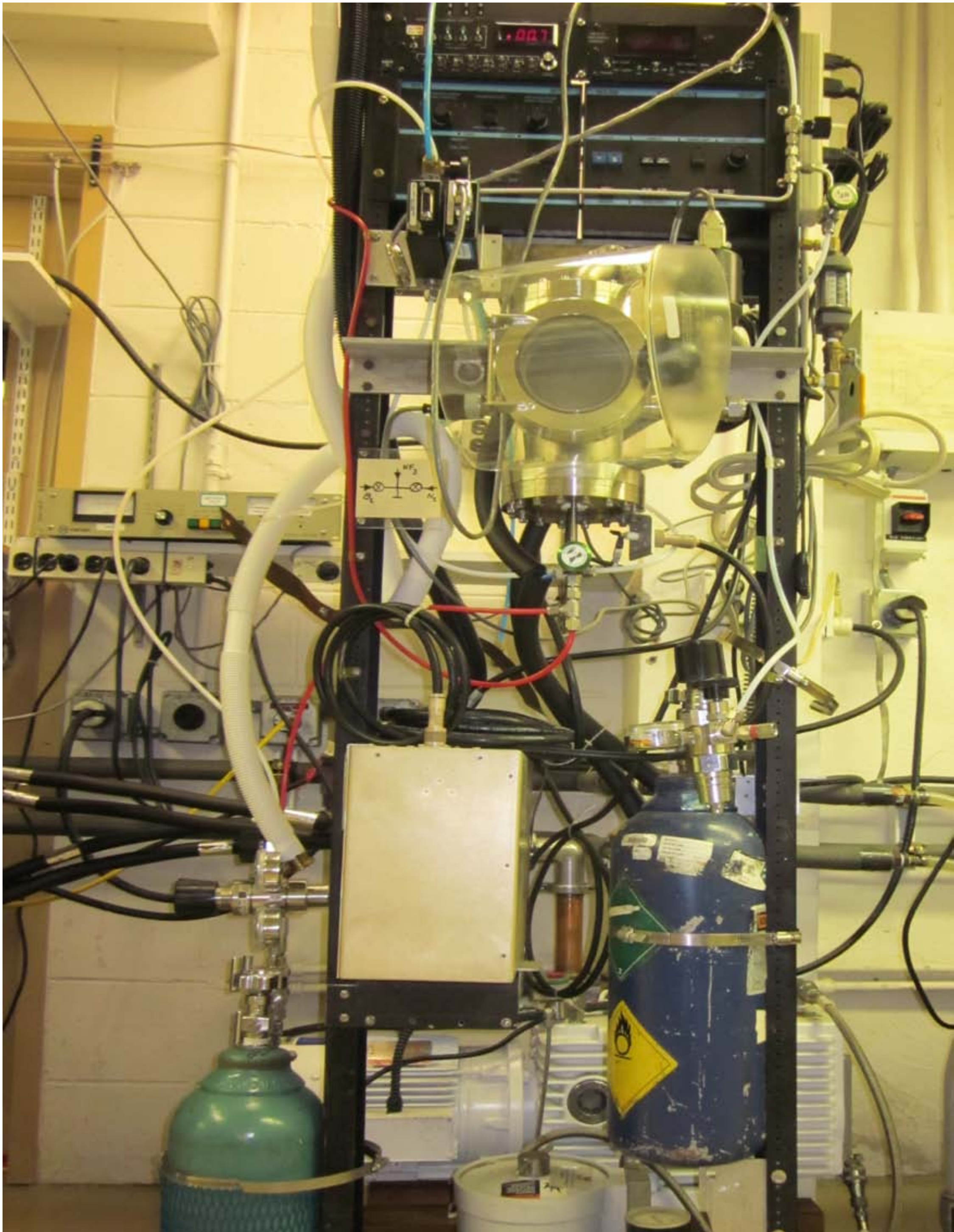


Figure 3.6(d): Reactive Ion Etching system.

3.7 Implantation and activation

Doping of the MOSFET source/drain regions is required for ohmic contact formation. However, it is difficult to dope SiC using a thermal diffusion process. The diffusion coefficients of most dopants are too low except at temperatures approaching the growth temperature of SiC. Doping by ion implantation, therefore, has been widely adopted. Implantation put dopants at the desired depth in the sample, but they are not electrically active. The process of activation moves implanted dopants from interstitial sites to lattice sites where they become electrically active. Figure 3.7 shows the system used to carry out the activation anneal. A temperature of 1650°C is used to activate aluminum (p-type dopant), and 1550°C is used to activate nitrogen (n-type dopant) [15,16,17].

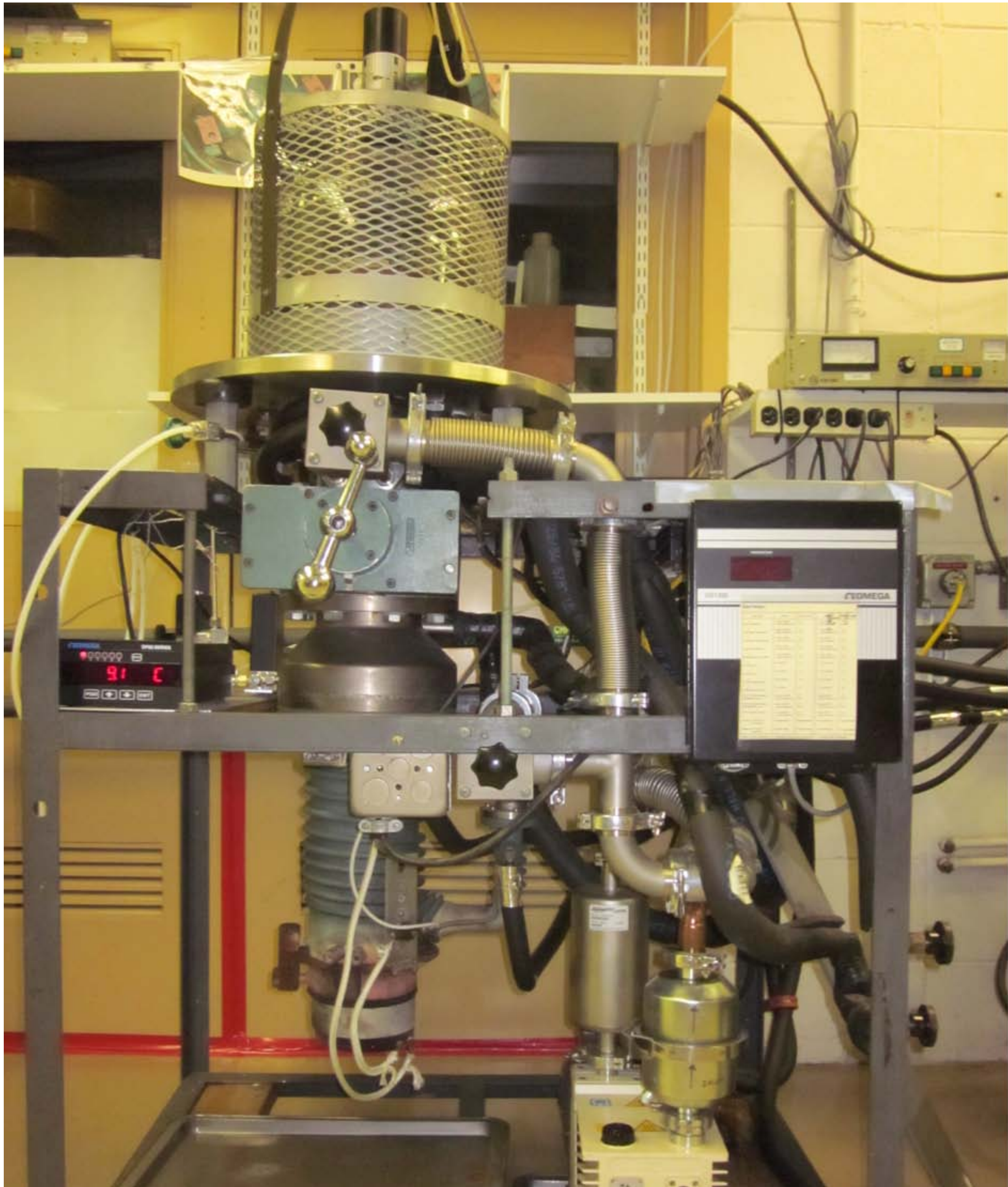


Figure 3.7: High temperature annealing system used to activate implanted n and p-type dopants.

3.8 Ohmic annealing

Nickel-vanadium (Ni/V, 93/7 wt %) is used to form ohmic contacts to the source/drain regions of n-channel SiC-MOSFETs. However, the as-deposited metal-semiconductor structure acts as a Schottkty contact. To transform this Schottky contact into an ohmic contact a short (30 seconds), high temperature (950°C) anneal is performed in Ar (760Torr, 4000sccm).

3.9 Simultaneous high-low C-V measurements

Simultaneous high-low frequency capacitance-voltage (C-V) measurements are employed to characterize MOS devices, especially the interface characteristics. Figure 3.9(a) shows the schematic of an n-/n+ metal oxide semiconductor (MOS) capacitor. A detailed discussion of MOS devices has been provided earlier (see chapter two). Figure 3.9(b) shows a photograph of the C-V system used for these measurements. A grounded black box is used for better insulation from stray magnetic/electric fields and from light. Electrical measurements are made with a Keithley 595 analyzer and a Keithley 590 CV meter. The Keithley 590 CV meter measures the quasi-static capacitance and Keithley 595 analyzer measures the high-frequency capacitance. Both measurements are made simultaneously. The bias voltage for the measurements is provided by a Keithley 230 programmable voltage source. These components are controlled using the Interface Characterization Software (ICS) package. This package is provided by Metric Technology Inc. and is designed to run the measurements, record the raw data, extract parameters and plot the results. During the measurement, the device is swept from accumulation to depletion using a slowly changing DC bias to obtain a quasi-static capacitance curve. A high frequency signal, 100KHz for room temperature (1MHz for high temperatures C-V measurement), is applied simultaneously between the gate and back contact. The high frequency curve does not reflect the effects of interface traps and

other possible defects, as they fill and empty at frequencies that are much lower compared to the 100kHz or 1MHz high frequency signal [18]. This high frequency C-V curve can therefore be assumed to be the theoretical ideal curve in calculations. For a given bias voltage (i.e., given position in the band gap and given interface trap energy), the separation between the quasi-static and high-frequency C-V curves determines the number of interface traps.

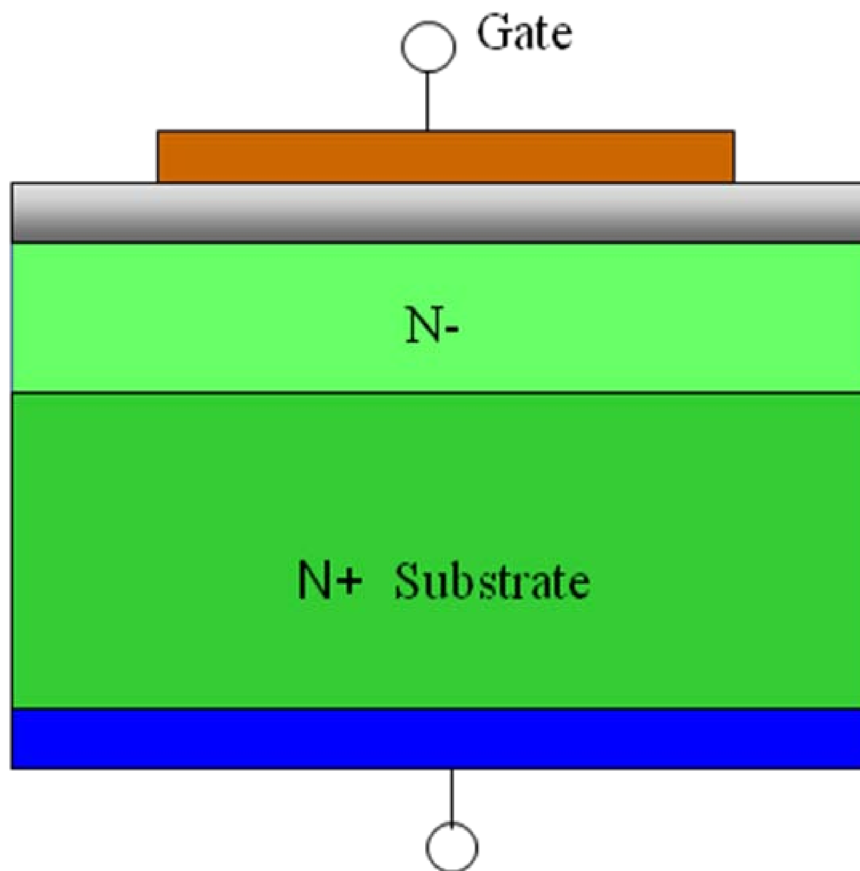


Figure 3.9(a): N-/N+ Metal Oxide Semiconductor (MOS) capacitor.

A typical high-low C-V curve for an n-type MOS capacitor is illustrated in figure 3.9(c). This curve is for an unpassivated MOS device. The corresponding interface trap density is shown in figure 3.9(d) where the solid line represents the high-frequency capacitance (CH), and the

dotted line represents the quasi-static capacitance (CQ). The energy level of a trap in the band gap is determined by the position of the Fermi level at the silicon carbide surface for a given gate bias voltage. Due to wide band gap of silicon carbide (3.2eV), only the interface traps with energies between E_c - 0.6eV can respond to quasi-static signal at room temperature. To determine defect state densities between the conduction band edge and mid-gap, C-V measurement are made at 23°C, 150°C, and 300°C. These measurements are made using a Signatone S-1060 probe station with temperature control and active cooling.

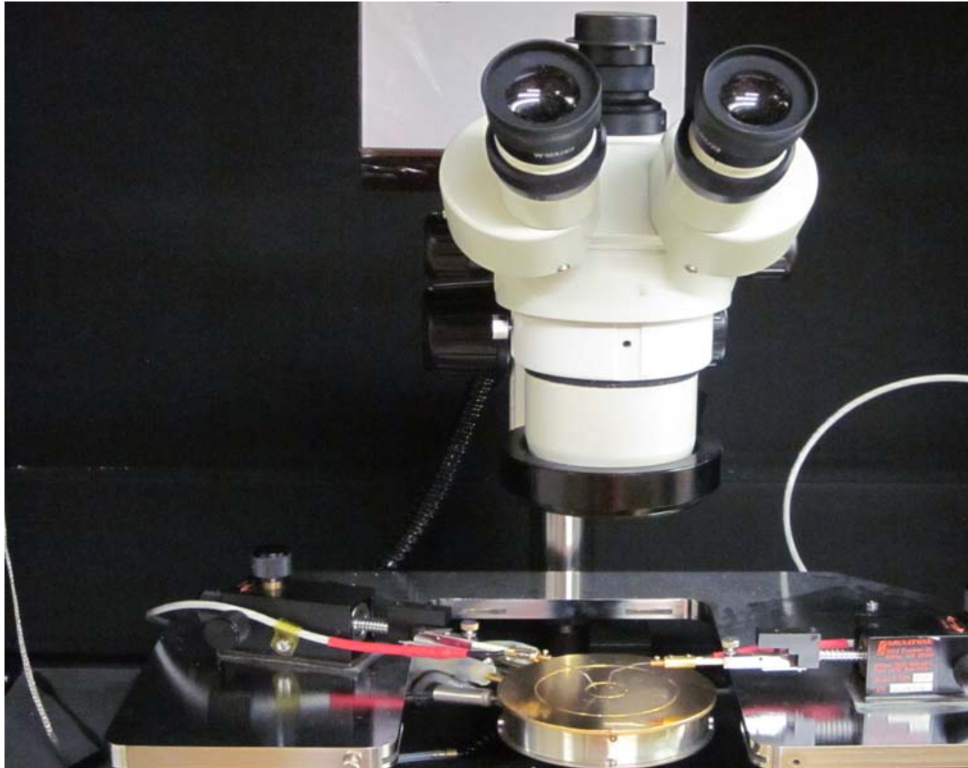
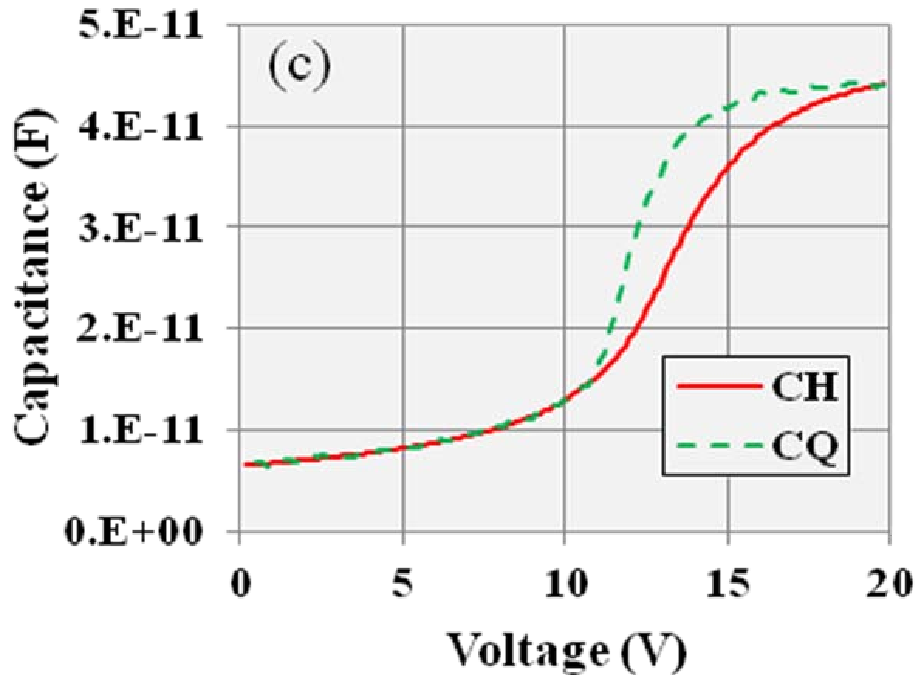


Figure 3.9(b): High-low C-V station with high temperature capability.



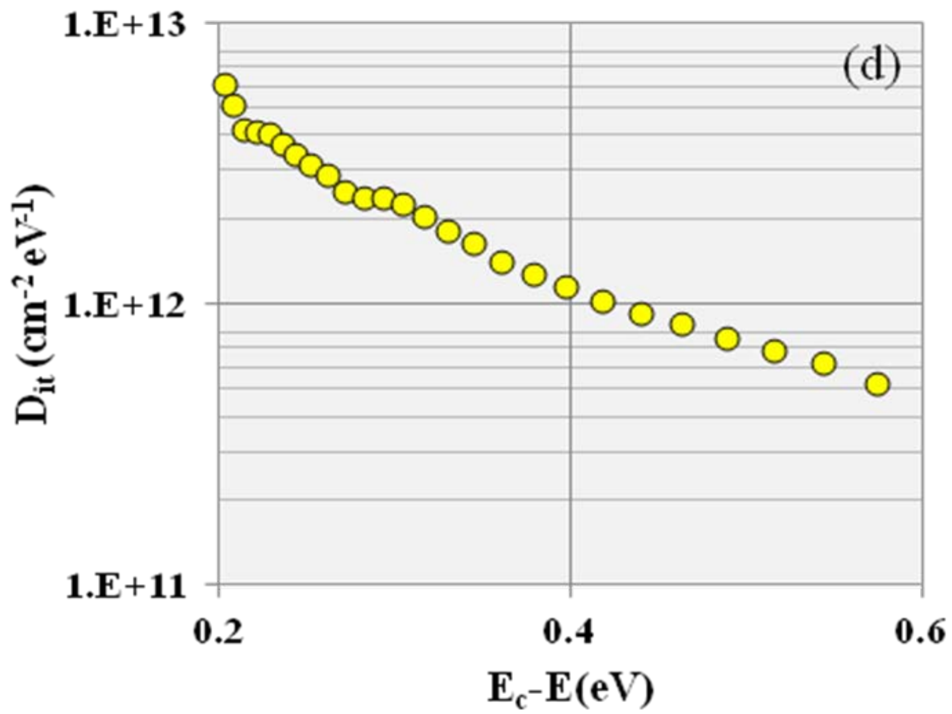


Figure 3.9(c) and (d): room temperature C-V characteristics (c) and interface trap density of an unpassivated n-4H-SiC MOS capacitor (d). Area of circular MOS device is $28.26 x 10^{-4} cm^2$.

3.10 I-V measurement system

Current-voltage (I-V) measurement is a necessary tool to characterize the performance of MOS device and to extract parameters such as oxide breakdown field and leakage current. Figure 3.10(a) shows the I-V measurement system which is comprised of a Keithley 6517 electrometer, a 6487 picoammeter, a metallic shield box, optical microscope and a probe station with a heated sample mounting stage. The Keithley 6487 picoammeter can measure current ranging from 20fA to 20mA. The Keithley 6517 electrometer has a maximum current measurement capability of 10mA with an accuracy of 10fA.

I-V measurements are performed on MOS capacitors. Two needles are used as probes, one of which is grounded for the backside contact, while the bias on the other one can be varied for the gate contact. This system is also capable of high temperature measurements (up to 300°C). The data obtained is usually plotted as current density (A/cm^2) versus oxide field (MV/cm). The breakdown field for a MOS device is usually considered as the point on the plot where a drastic increase in the current density is observed. Otherwise, it is taken to be the point at which current density crosses the value of 1x10^{4}A/cm^2.

Figure 3.10(b) illustrates the current density versus oxide field plot of three MOS devices. These devices have been passivated using different processes – NO (nitric oxide), phosphorus, and nitrogen plasma passivation. The breakdown field for all these devices, according to the plot is around 8MV/cm. The leakage currents are higher (by four or more orders of magnitude) for phosphorous and plasma passivated devices compare to NO.

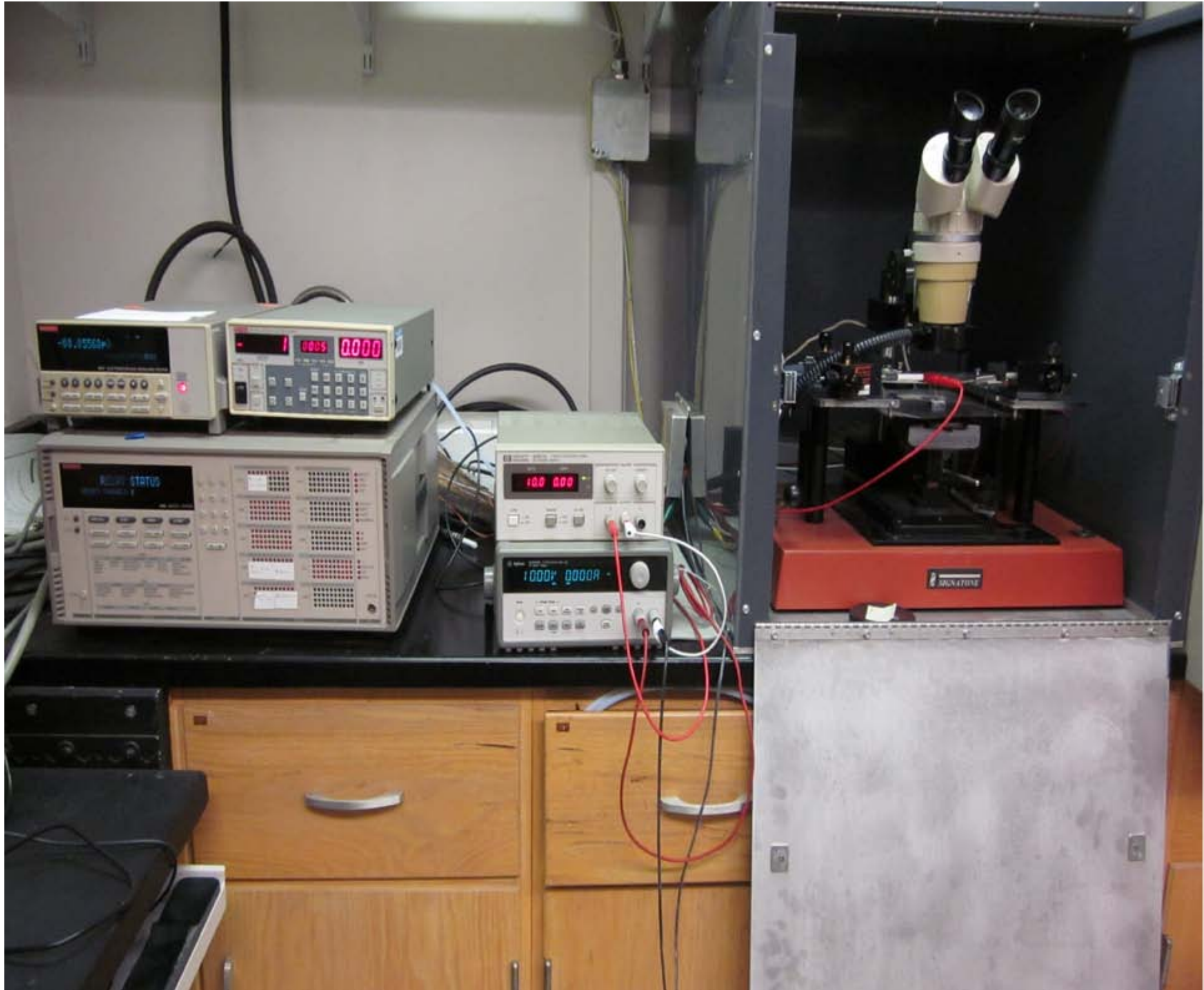


Figure 3.10(a): Current-voltage measurement system.

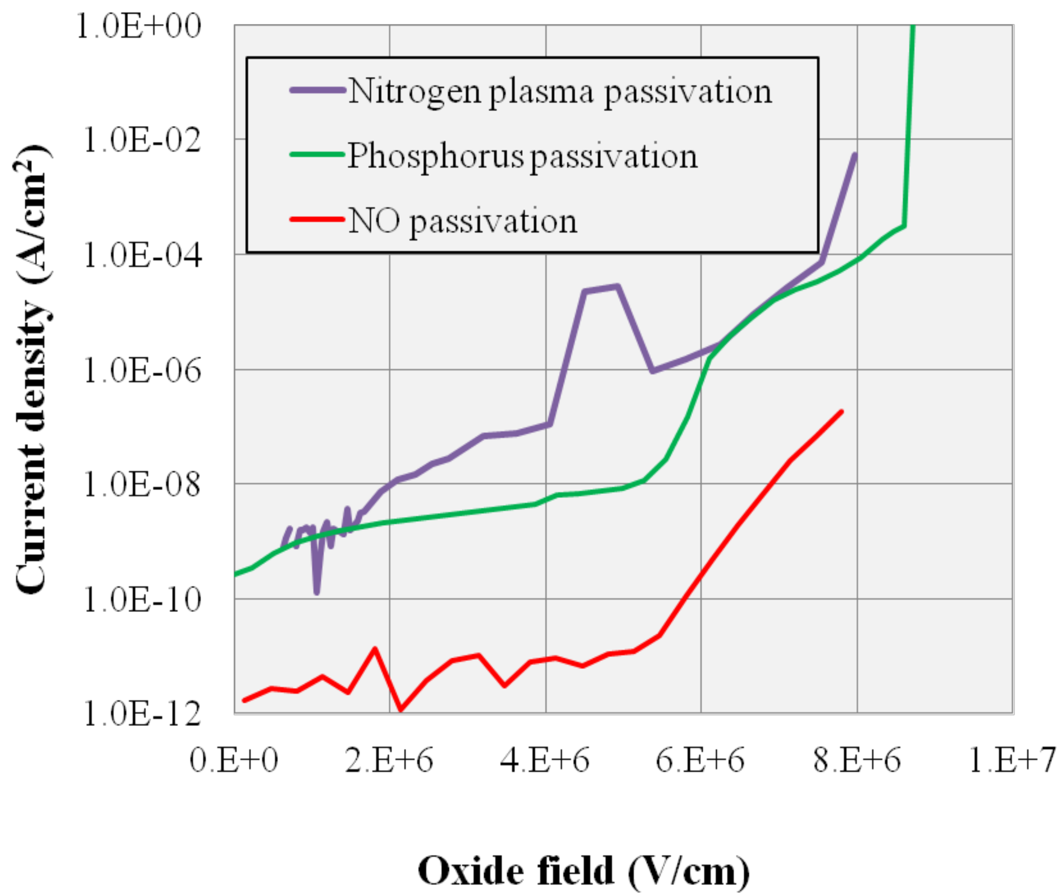


Figure 3.10(b): I-V characteristics of MOS devices after nitric oxide, phosphors, and nitrogen plasma passivation.

3.11 MOSFET characterization

In addition to MOS capacitors, n-channel lateral MOSFETs shown in figure 3.11(a) have been fabricated and characterized. The FET has source, drain and gate terminals. Therefore, three probes are required for characterization measurements. Although many parameters are important for MOSFET devices, we focused on the channel mobility and threshold voltage that can be extracted from the characterization measurements. Figure 3.11(b) shows the setup used for these measurements. The system is comprised of two source measurement units.

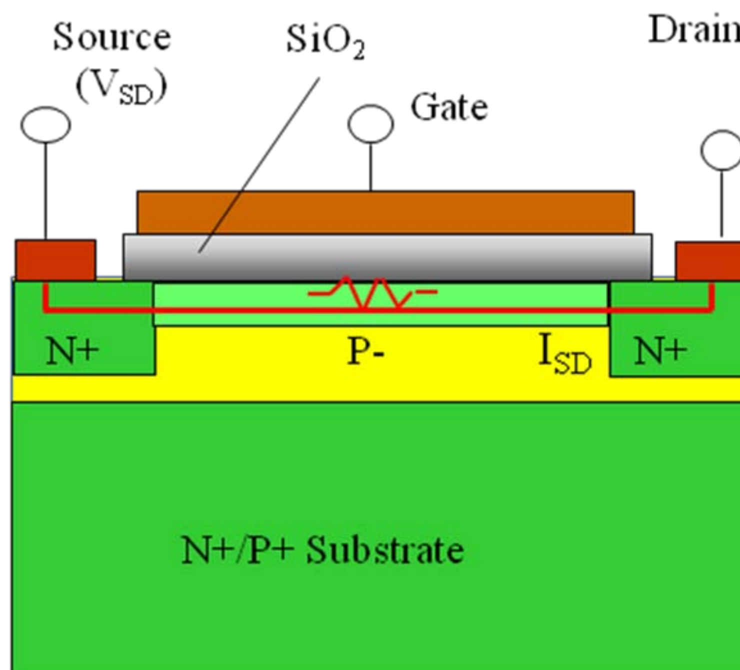


Figure 3.11(a): Lateral n-channel Metal Oxide Field Effect Transistor (MOSFET).

The Keithley 4100 measures gate voltage and gate current, while the Keithley 4210 measures source-drain voltage and source-drain current. A Labview program is used to control these units and automatically extract the data. All measurements are performed using

a constant low value of the source-drain voltage, 25mV, so that the linear model can be used to extract different parameters (see chapter 2). Figure 3.11(c) shows the mobility curve for a phosphorus passivated device (thick PSG). The maximum field effect mobility is around $80cm^2/V.s$. Another important parameter is the threshold voltage (V_T). It can be defined as the intercept on the V_g (gate voltage) axis of the tangent line to the I_d curve (drain current) drawn at its maximum slope. It should be noted that the gate current should be kept small (around $10^{-10}A$) by choosing a suitable range of gate bias, otherwise leakage current through the oxide layer will give erroneous results.

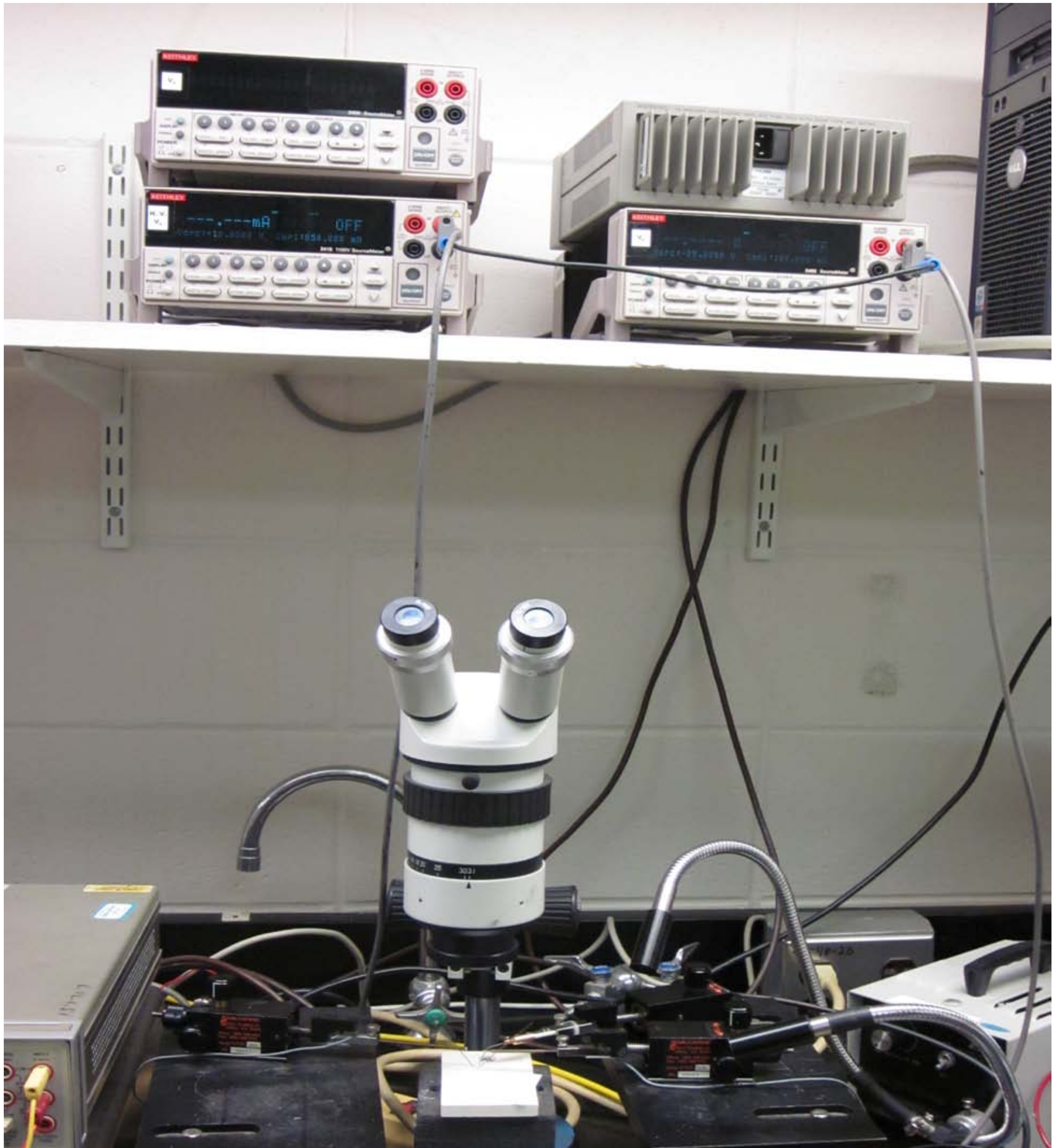


Figure 3.11(b): The three probe current-voltage measurement station consisting of a Keithley 2400 source meter, a Keithley 2410 source meter, a microscope and the sample holder.

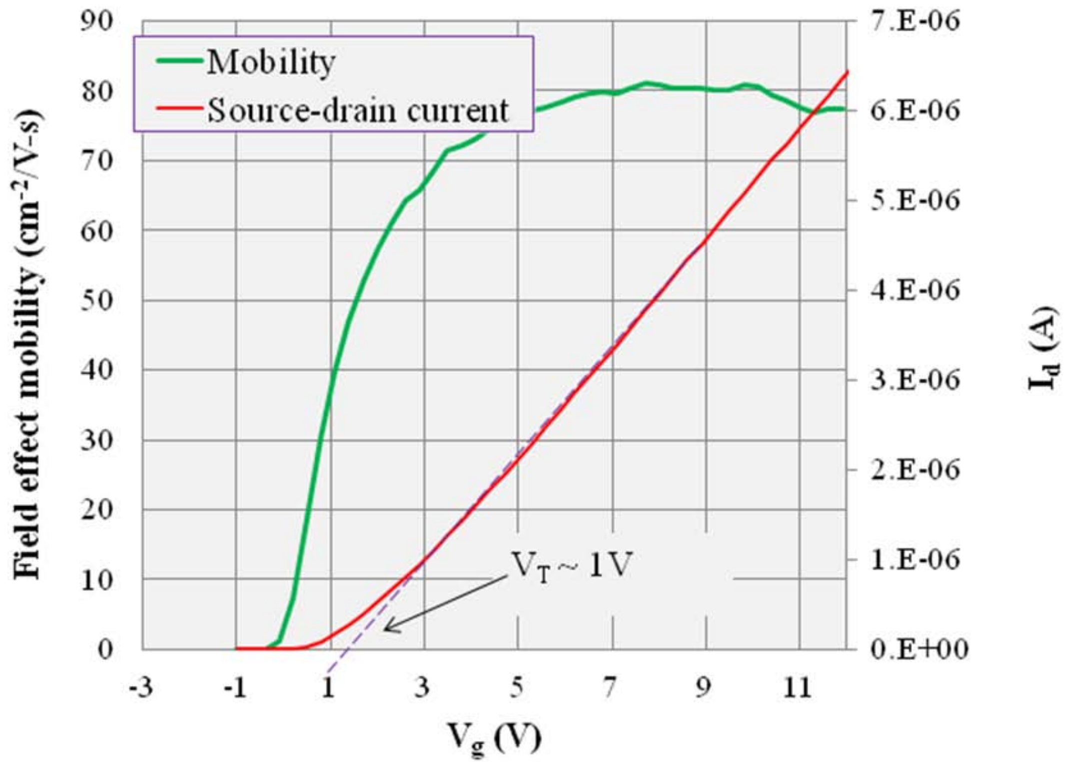


Figure 3.11(c): Channel mobility and threshold voltage (V_T) of an n-channel MOSFET with gate oxide grown by standard dry oxidation followed by phosphorus passivation. Drain source voltage (V_{ds}) = 25mV. Gate length = 120µm and gate width = 400µm.

3.12 References

[1] W. Kern and J. L. Vossen, *Thin Film Processes*, (Academic Press, 1991).

[2] W. Kern, Handbook of Semiconductor cleaning technology, (Noyes Publishing, 1993).

[3] W. Kern, J. Electrochem. Soc. **37**, 1887 (1990).

[4] M. D. Ventra and S. Pantelides, *Phys. Rev. Lett.* **83**, 1624 (1999).

[5] J. Tan, M. Das, J. Cooper, and M. Melloch, *Appl. Phys. Lett.* **70**, 2280 (1997).

[6] J. Knaup, P. Deak, T. Frauenheim, A. Gali, Z. Hajnal, and W. Choyke, *Phys. Rev. B* **71**, 235321 (2005).

[7] S. Wang, M. D. Ventra, S. Kim, and S. Pantelides, *Phys. Rev. Lett.* **86**, 5946 (2001).

[8] X. Shen and S. T. Pantelides, *Appl. Phys. Lett.* **98**, 053507 (2011).

[9] J. Shenoy, M. Das, J. Cooper, M. Melloch, and J. Palmour, *J. Appl. Phys.* **79**, 3042 (1996).

[10] E. Opila, *J. American Cer. Soc.* **78**, 1107 (1995).

[11] F. La Via, F. Roccaforte, V. Raineri, M. Mauceri, A. Ruggiero, P. Musumeci, L. Cacagno, A. Castaldini, and A. Cavallini, *Microelectronic Engineering* **70**, 519 (2003).

[12] D. Martin Knotter, J. Am. Chem. Soc. **122**, 4345 (2000).

[13] P. H Yih, V. Saxena, and A. J. Steckl, *Phys. Stat. Sol. (b)* **202**, 605 (1997).

[14] G. L. Harris, *Propertries of Silicon Carbide*, (IET, 1995).

[15] S. Seshadri, G. W. Eldridhe, and A. K. Agarwal, *Appl. Phys. Lett.* **72**, 2026 (1998).

[16] T. Komoto, N. Inoue, and H. Matsunami, *Phys. Stat. Sol.* (a) **162**, 263 (1997).

[17] M. A. capano, S. Ryu, M. R. Melloch, J. A. Cooper, and M. R. Buss, *J. Elect. Mat.* **27**, 370 (1998).

[18] J. A. Cooper, *Phys. Stat. Sol.* (a) **162**, 305 (1997).

CHAPTER 4

Phosphorous passivation of the interface

Oxidation of SiC is different compared to oxidation of Si [1,2]. In SiC, there is an additional element, carbon (C), whose liberation during oxidation complicates the process. Interface traps form due to silicon dangling bonds, carbon dangling bonds, oxygen vacancies and carbon clusters [3,4,5]. Liberated carbon forms complex structures and exists as an interstitial in the SiC bulk [6,7]. Unlike Si/SiO_2, the interface in SiC/SiO_2 is not abrupt [8]. The 4H-SiC band gap (3.2eV) is three times larger than Si which allows the energies of many more interface traps lie within the semiconductor band gap [9,10,11]. All these differences lead to a higher tarp density near the SiC conduction band edge. [12,13]. For an unpassivated MOS-C, the trap density at $E_c - E = 0.2eV$ is of the order of $10^{13}eV^{-1}cm^{-2}$ [14]. Where E_c is the energy of conduction band of SiC and E is the energy of trap in bandgap. Different passivation techniques have been tried to reduce interface trap density – e.g., post-oxidation anneals in NH_3, H_2, N_2O and NO. Post-oxidation anneals to introduce nitrogen are called "nitridation" of the interface. The best interface trap density after nitridation is ~ $10^{12}eV^{-1}cm^{-2}$ at $E_c - E = 0.2eV$ which is much higher compared to SiO_2/Si interface ($10^{10}eV^{-1}cm^{-2}$) [15,16.17]. Using NO and N_2O passivations, mobilities of around 30-35$cm^2/V.s$ can be obtained [15,18]. Nitridation leads to incorporation of nitrogen at the interface which bonds as C-N, Si-N, Si-N-O and hence removes dangling bonds [19]. Nitridation followed by passivation with hydrogen increases the mobility to approximately 40$cm^2/V.s$ [20,21]. Implantation of the channel region with nitrogen also produces a mobility of around 40 $cm^2/V.s$ [22,23,24].

F. Allerstan, et al. have shown that sodium ions at the interface lead to significantly higher inversion channel mobility (150$cm^2/V.s$) on the Si face of 4H-SiC MOSFET [25]. However, sodium ions move under bias and hence destabilize the threshold voltage of the device.

Devices fabricated on the a-face (1120) of 4H-SiC and devices with Al_2O_3/SiO_2 composite gate dielectrics also have channel mobilities of 100 $cm^2/V.s$ or more, but these MOSFETs showed higher leakage currents and lower breakdown voltages [26,27].

4.1 Passivation

Passivation with phosphorous is more effective in reducing the interface traps. As discussed further in section 4.2, the interface trap density (D_{it}) near conduction band edge ($E_c - E$ = 0.2eV) is around $2x10^{-11}eV^{-1}cm^{-2}$. This results in an increased mobility of approximately $80cm^2/V.s$.

Silicon carbide wafers were provided by Dow Corning and Cree, Inc. MOS capacitors were fabricated on n/n+, 8° off-axis, 4H wafers with a 5µm n-epilayers doped with nitrogen at $8.3x10^{15}cm^{-3}$. Planar MOSFETs were fabricated on a 4° off-axis 5µm p-epilayer grown on an n^+ substrate. The epilayer was doped with Al at $8x10^{15}cm^{-3}$. The furnace used for P-passivation is shown in figure 4.1(a). Samples were annealed using the arrangement in figure 4.1(b) for a small planar diffusion source (PDS) that produces a P_2O_5 passivating ambient.

Figure 4.1(a): A planar diffusion source (PDS) furnace.

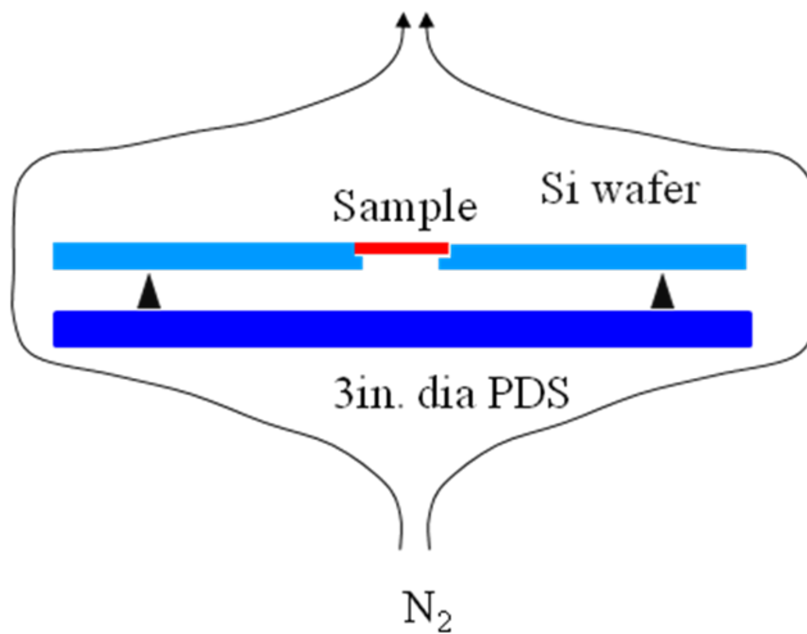


Figure 4.1(b): Schematic of process inside the PDS furnace.

Samples were annealed in PDS furnace with pure nitrogen, 2L/min, at 1000°C for 3 hours.

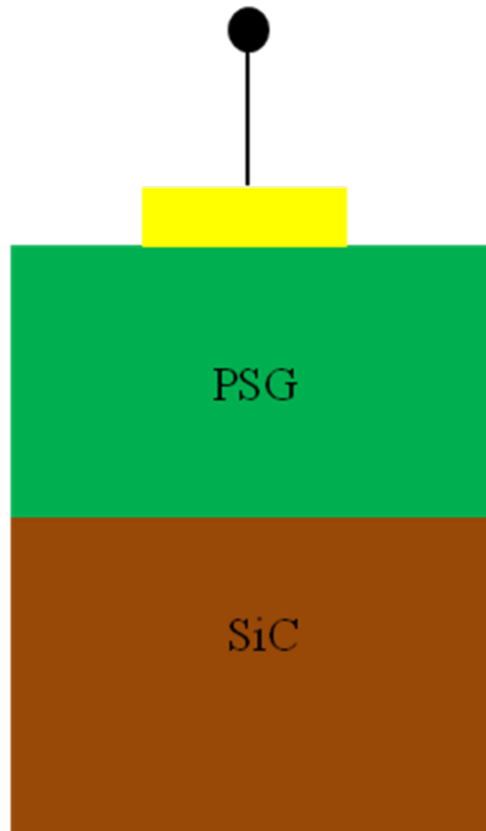


Figure 4.1(c): MOS-C with P-passivation. Oxide transforms to phosphosilicate glass (PSG) after P-passivation.

The following reaction takes place and which leads to the formation of phosphorous pent-oxide.

$$SiP_2O_7 + 1000C \rightarrow SiO_2 + P_2O_5$$

P-passivation converts SiO_2 to phosphosilicate glass (PSG) and is shown in figure 4.1(c). There is additional oxide growth during P-passivation. If we start with 70 nm of oxide, we have 90-95nm then after 3 hours of passivation.

4.2 Capacitance-Voltage (C-V) measurements interface trap density (D_{it})

Simultaneous high-low C-V curves measured at room temperature for a P-passivated MOS-C are shown in figure 4.2(a).

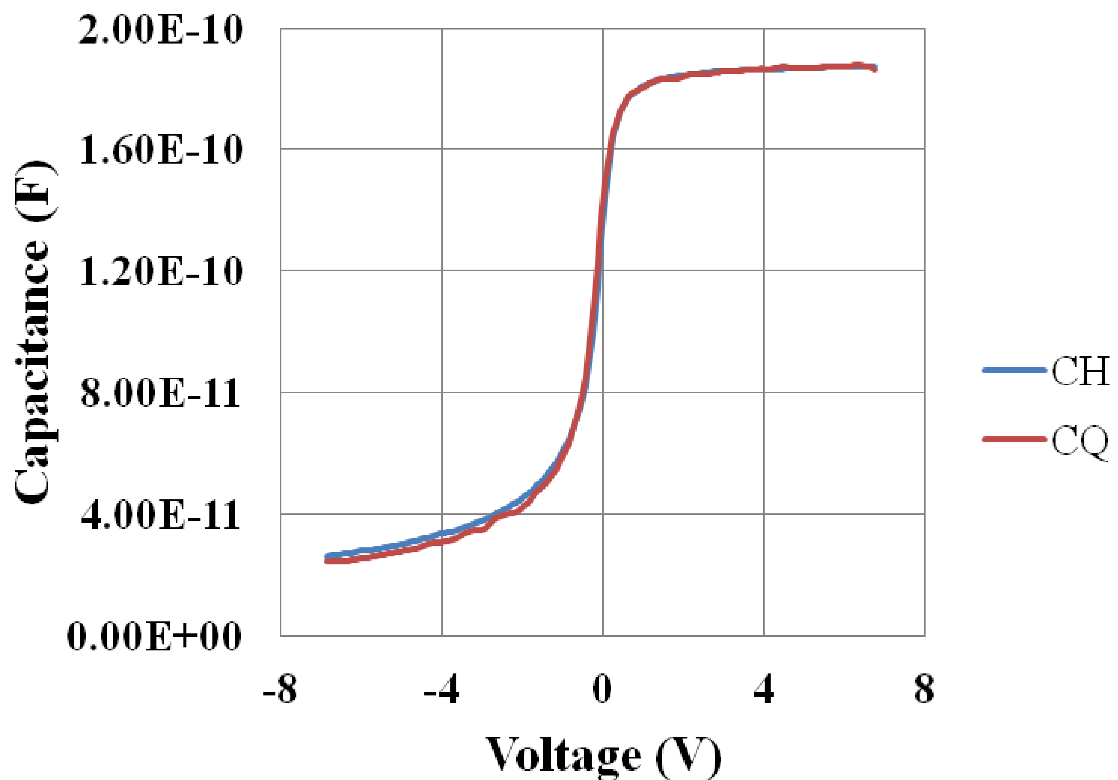


Figure 4.2(a): C-V measurement of P-passivated MOS-C. Area of circular MOS device is $28.26x10^{-4}cm^2$.

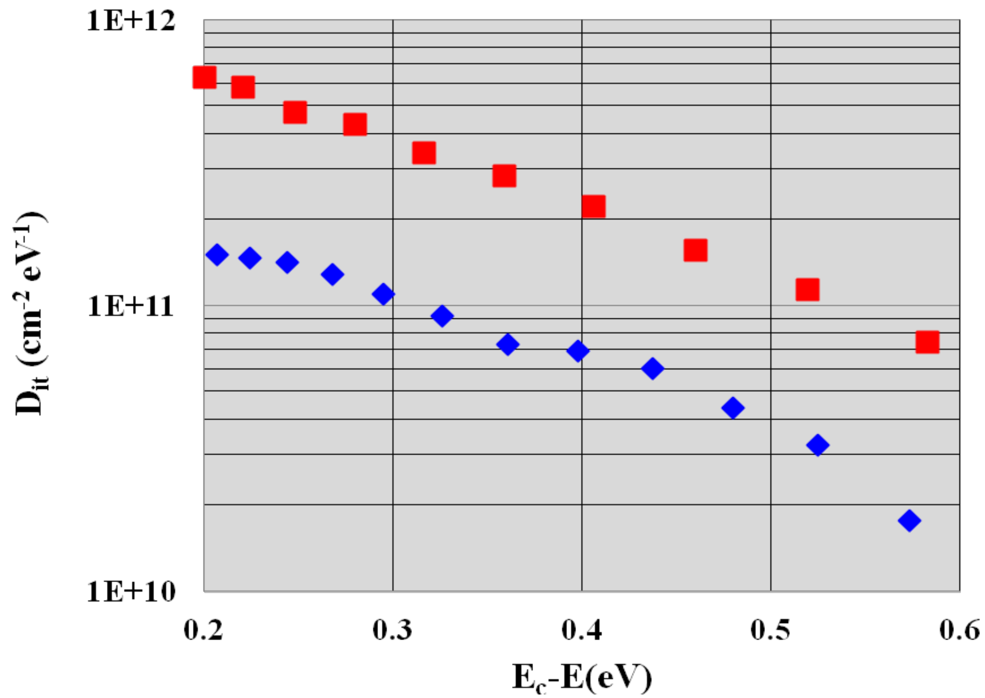


Figure 4.2(b): D_{it} after 4 hr P-passivation and comparison with NO passivation.

The interface trap density is shown in figure 4.2(b) and compared with the trap density following NO passivation. These results are for 3 hours P-passivation. The thickness of PSG layer is 90nm. D_{it} is significantly lower compared to NO passivation and is $2x10^{-11}eV^{-1}cm^{-2}$ at $E_c - E = 0.2eV$. MOS capacitor results show that P-passivation is more effective than NO-passivation.

4.3 Phosphorus profile after passivation

A SIMS (Secondary Ion Mass Spectroscopy) profile of the P concentration in the SiO_2 layer is shown in figure 4.3(a). After P-passivation there is a significant P concentration at the interface (~ $2x10^{21}cm^{-3}$). Figure 4.3(b) shows the N profile in an oxide after NO passivation. The interfacial nitrogen concentration is $1.2x10^{21}cm^{-3}$. There is another major difference in N

and P profiles. After NO passivation, N accumulates only at the interface. In P-passivation, P distributes throughout the oxide and converts the oxide to PSG. PSG is a polar material with different properties compared to SiO_2.

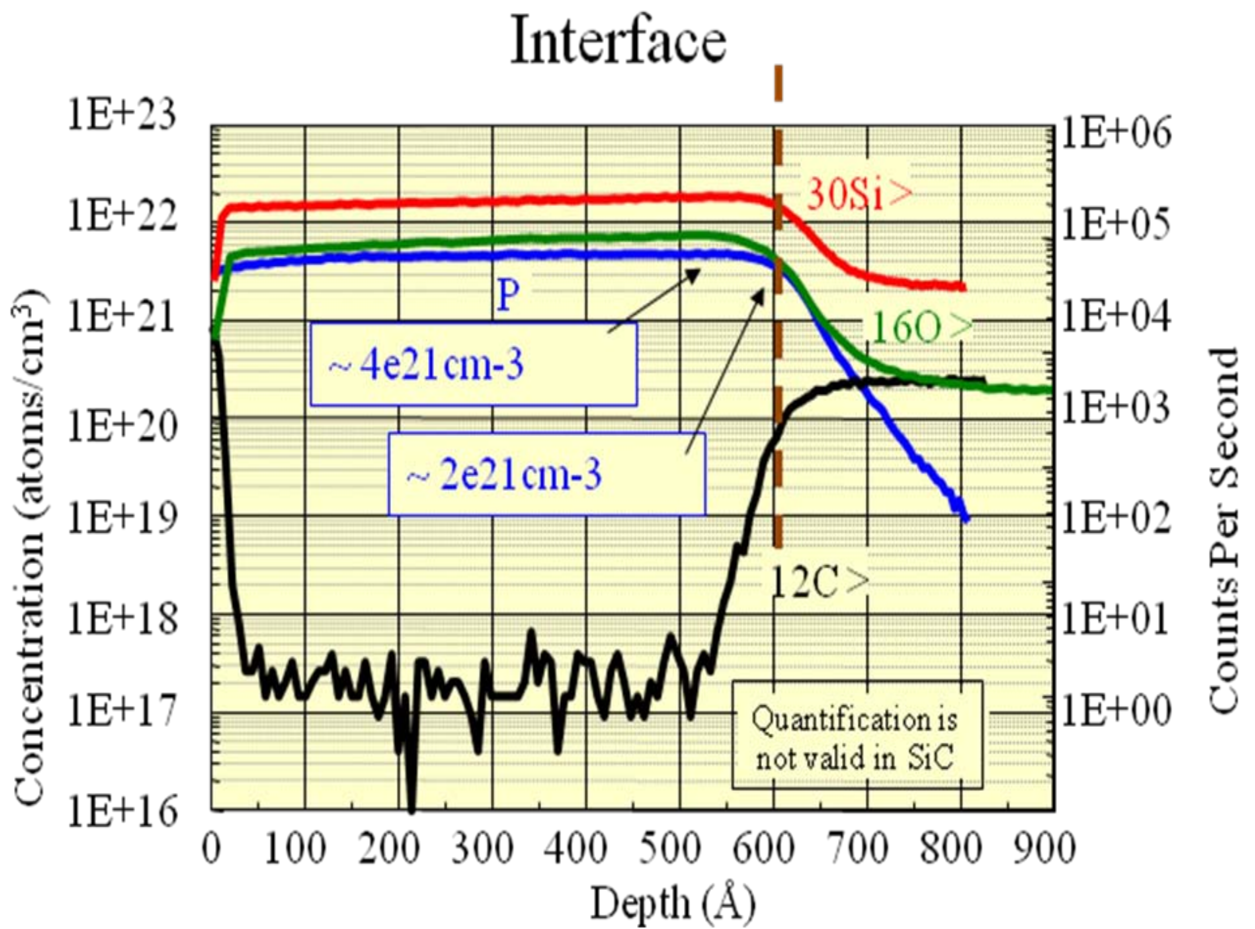


Figure 4.3(a): SIMS profile of P in SiO_2 after P - passivation of a MOS-C.

4.4 Breakdown characteristics of PSG

As mentioned earlier, P-passivation converts the oxide to PSG. I-V characteristics of PSG MOS-Cs are compared to NO in figure 4.4. The breakdown field for the PSG devices is around 8 MV/cm which is similar to that of the NO device. However, the leakage current, though still acceptable, is four orders higher for the PSG devices.

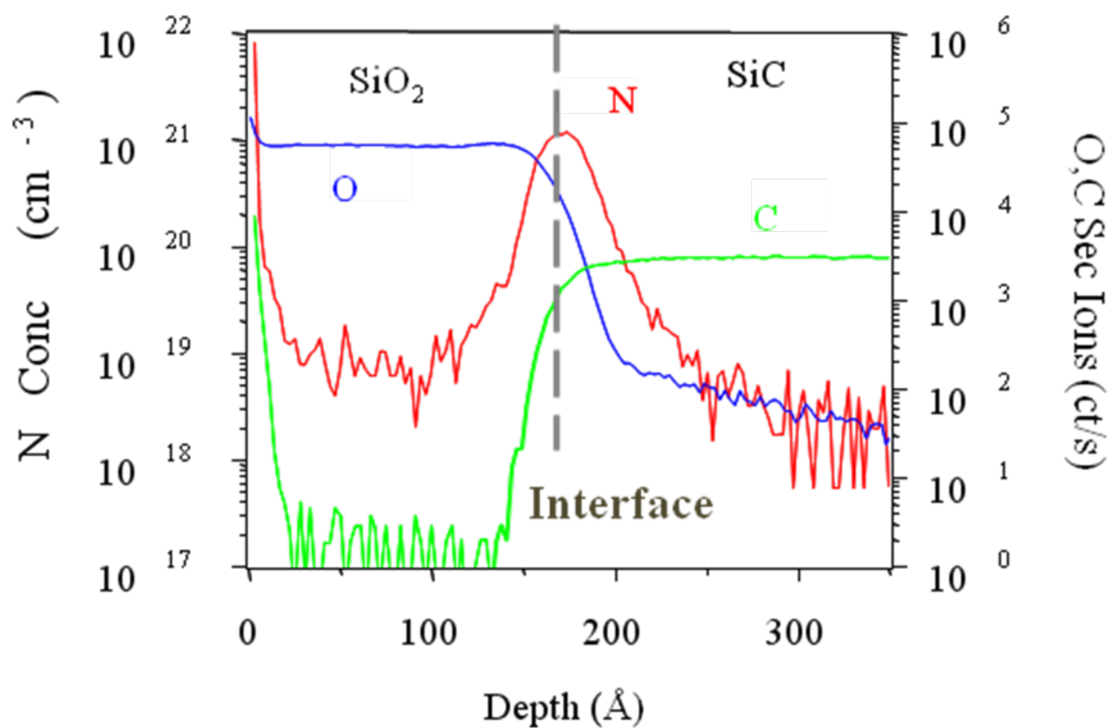


Figure 4.3(b): SIMS profile of N in SiO_2 after NO passivation. [28].

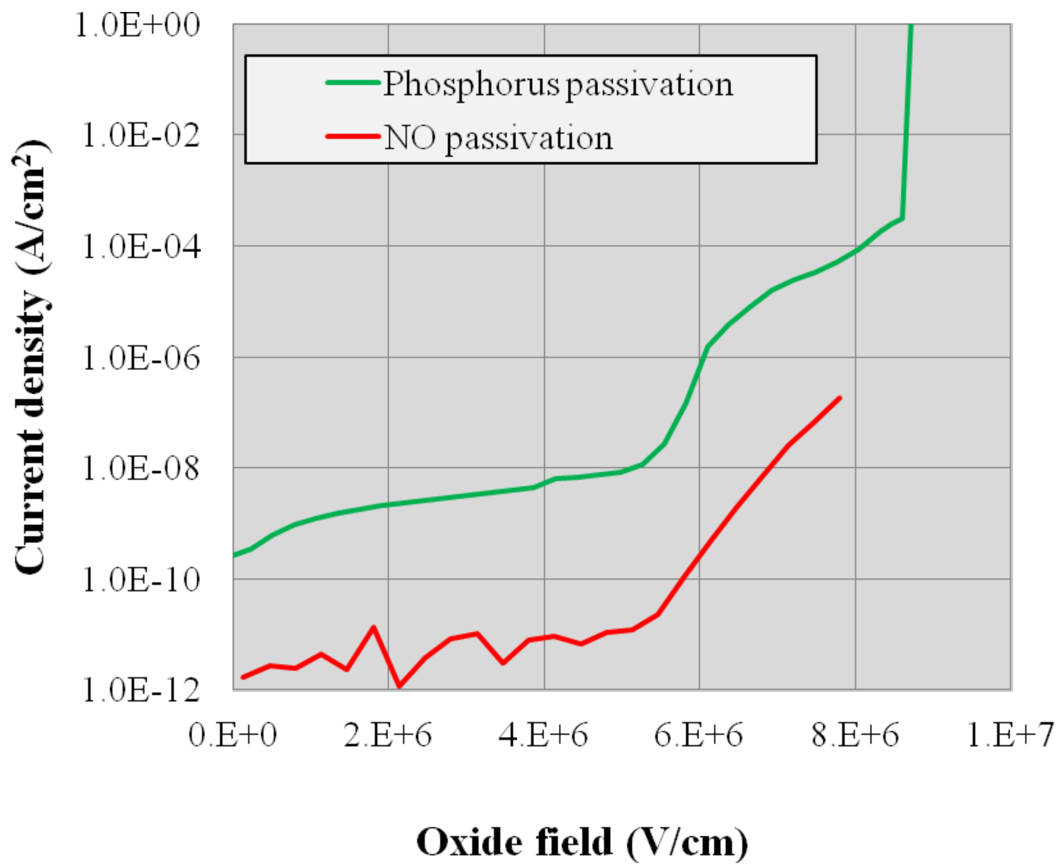


Figure 4.4: I-V characteristic of MOC devices after P-passivation compared with NO-passivation.

4.5 Field effect mobility

The field effect inversion channel mobility of an n-channel MOSFET after P-passivation is shown in figure 4.5. Mobility after P-passivation is two times higher compared to standard

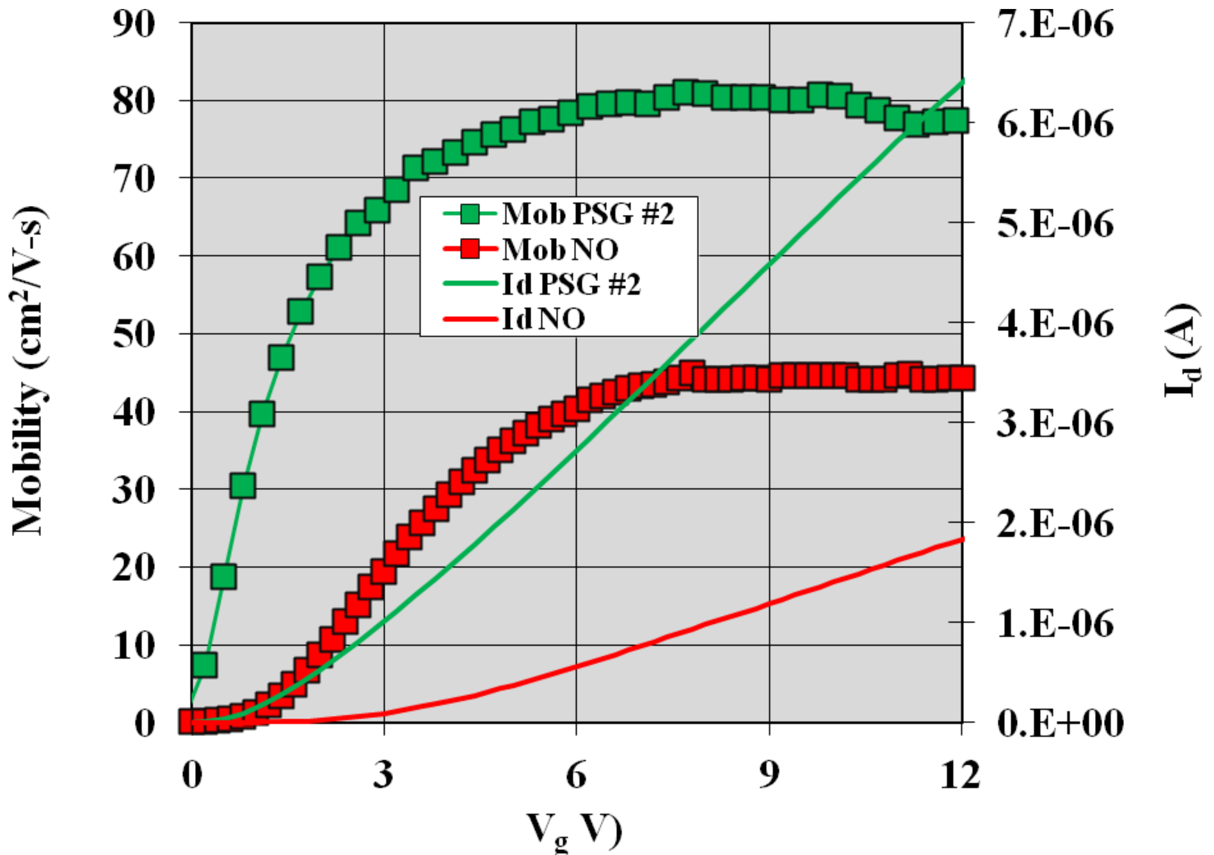


Figure 4.5: Inversion channel mobility of MOSFET after P-passivation and comparison with NO-passivation.Drain source voltage (V_{ds}) = 25mV. Gate length = 120µm and gate width = 400µm.

NO–passivation. Also, the drain current for the phosphorous MOSFET is higher. Increased mobility and lower threshold voltage, $V_{T,}$ means that there is more interface trap passivation with the phosphorous process.

4.6 Theoretical considerations

Theoretical work is done by our collaborators at Vanderbilt University. It suggests that the effect of P-passivation on interface state density and electron mobility can be explained by considering the interactions of phosphorous with carbon-related defects in the SiO_2/4H-SiC

system. As discussed by Wang, et al. [19], the main defects at the SiC/SiO_2 interface are three-fold coordinated carbon atoms in an interfacial transition layer, correlated carbon dangling bonds and Si-Si bonds. First-principles calculations were performed to investigate the effect of phosphorus in passivating the three-fold carbon atoms. Results show that a phosphorus atom can replace a three-fold coordinated carbon atom at the interface and remove the interface state associated with the C atom. Replacement produces a configuration that has an electronic level at about 0.6eV above the valence band of 4H-SiC, which is due to the lone-pair state of the three-fold P atom. Recall that defect states in the bottom half of the 4H-SiC do not adversely affect the channel mobility. A similar result has been reported previously for nitrogen replacement [29,30, 31]. Calculations also show that a three-fold carbon atom can be replaced by a P=O group, where the P atom forms a double bond with an O atom in addition to the three single bonds and having the oxidation state 5+. In this configuration, there are no interface states within the band gap of 4H-SiC. Phosphorus annealing thus eliminates interface states caused by three-fold carbon atoms. Recent XPS measurements for SiC/SiO_2 samples passivated with phosphorous show a phosphorous 2*p* peak at 133.9eV [32], which agrees with the spectrum of the P^{5+} state (2*p* peak around 133eV) [33, 34], and is consistent with the proposed mechanism of P=O groups replacing 3-fold carbon atoms at the interface.

Phosphorus can diffuse into the substrate during the reaction between bare SiC and P_2O_5 as the result of Si moving from the substrate to react with oxygen in a P_2O_5 over-layer [35]. However, Si out-diffusion and thus phosphorous diffusion into the SiC may be less likely for SiO_2/SiC samples. In figure 4.3, the inverse slope of the P profile to the right of the interface in the SiC is 115A/decade, which is higher than an inverse slope of 60-70A/decade that results from P atom drive-in by the 3keV O_2^+ beam used for SIMS profiling [36].

Phosphorous diffusion into the SiC cannot therefore be ruled out. However, more accurate measurements are needed to resolve the issue with certainty.

The presence of P in the substrate could have two effects. (1) Phosphorous in the SiC can passivate carbon di-interstitial clusters that may form in the channel region during thermal oxidation. These "substrate traps" are not effectively passivated by NO, H_2 and atomic hydrogen due to the difficulties of incorporating nitrogen and neutral hydrogen [37]. (2) Phosphorous can also passivate the correlated dangling bonds of excess carbon atoms. Such a correlated bond defect consists of two carbon atoms sitting at a Si site, as designated by the notation $(C_2)_{Si}$. This defect is resistant to an H_2 gas anneal because of the large barrier for H_2 dissociation [19,38], but the defect can be passivated by atomic hydrogen and possibly atomic and molecular fluorine. We noted that one P atom can replace the two C atoms in the $(C_2)_{Si}$ defect and become a simple substitutional donor P_{Si}. This, together with other processes of incorporating substitutional phosphorus, will increase the concentration of n-type dopants in the SiC interface region to produce an effect similar to the counter-doping effect observed following the oxidation of nitrogen-implanted 4H-SiC [24]. Counter-doping and interface trap reduction both contribute to a lower threshold voltage and higher field effect mobility as observed in figure 4.5.

The reconstruction of the oxide network when SiO_2 transforms into PSG may also reduce the amount of Si-Si bonding so that the number of shallow, interfacial band-tail states is reduced. Furthermore, positively charged, four-fold P atoms (phosphorous ions with four P-O bonds) may exist in the PSG. As mentioned previously, these ions are not mobile, but, as with positively charged Na ions [39], the Coulomb potentials of a positive P^+ ion in the oxide can extend into the SiC substrate and create a shallow electron level under the SiC conduction band. If the concentration of near-interface positive ions is high, the Coulomb potentials from individual positive ions overlap and form a relatively smooth potential surface throughout the

interface. Thus, a conducting impurity band is created in the interfacial SiC layer. Such a band adds a new conducting channel to the system, and can enhance the field-effect mobility. This band also prevents the detection of shallow interface states.

4.7 BTS measurements

P-passivation converts SiO_2 to a phosphosilicate glass (PSG) which is known to be a polar material [40, 41]. This polar characteristic makes the flatband and threshold voltages of MOS capacitors and FETs unstable [42]. We studied the stability of P-passivated MOS caps and MOSFETs by performing bias-temperature-stress (BTS) measurements as follows.

1) Heat the device to 150°C.

2) Apply an electric field, ~ ±1 to 1.5 MV/cm.

3) Keep the device at high temperature and high field for a desired time (~ 5min).

4) Decrease the device temperature to room temperature under bias.

5) Perform a C-V measurement in case of a MOS cap, and extract V_{FB}. For a MOSFET, extract V_T from a mobility measurement.

6) Compare V_{FB} and V_T before and after BTS measurement.

7) Repeat the BTS measurements for different time intervals - 10min, 30min, 60 min, etc.

4.7.1 BTS results for MOS-C

BTS results for a positive bias are shown in figure 4.6(a). Since the bias voltage is positive, the measurement is called as positive BTS. Here the applied electric field is ~ + 1.5 MV/cm. V_{FB} before BTS measurement is around 0V for different time intervals. This confirms more interface trap passivation for the phosphorous process. With NO-passivation V_{FB} is higher at around 2V. V_{FB} after positive BTS

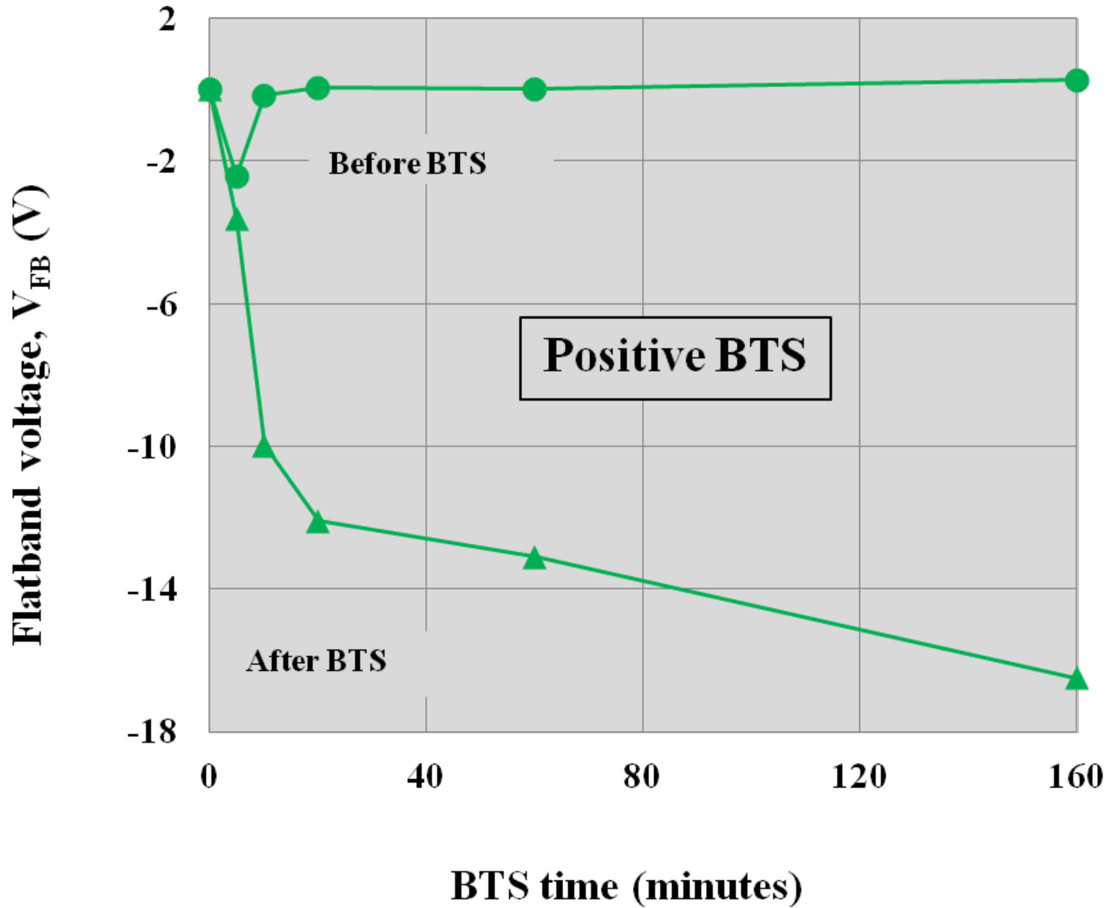


Figure 4.6(a): V_{FB} before and after positive BTS of a MOS-C.

increases from 0 V to - 18 V. This negative shift in V_{FB} is due to induced positive PSG polarization charge at the interface. Negative BTS results are shown in figure 4.6(b). The positive shift in V_{FB} is due to induced negative polarize charge. Thus, polar nature of PSG makes P passivated devices unstable by shifting V_{FB} in different directions.

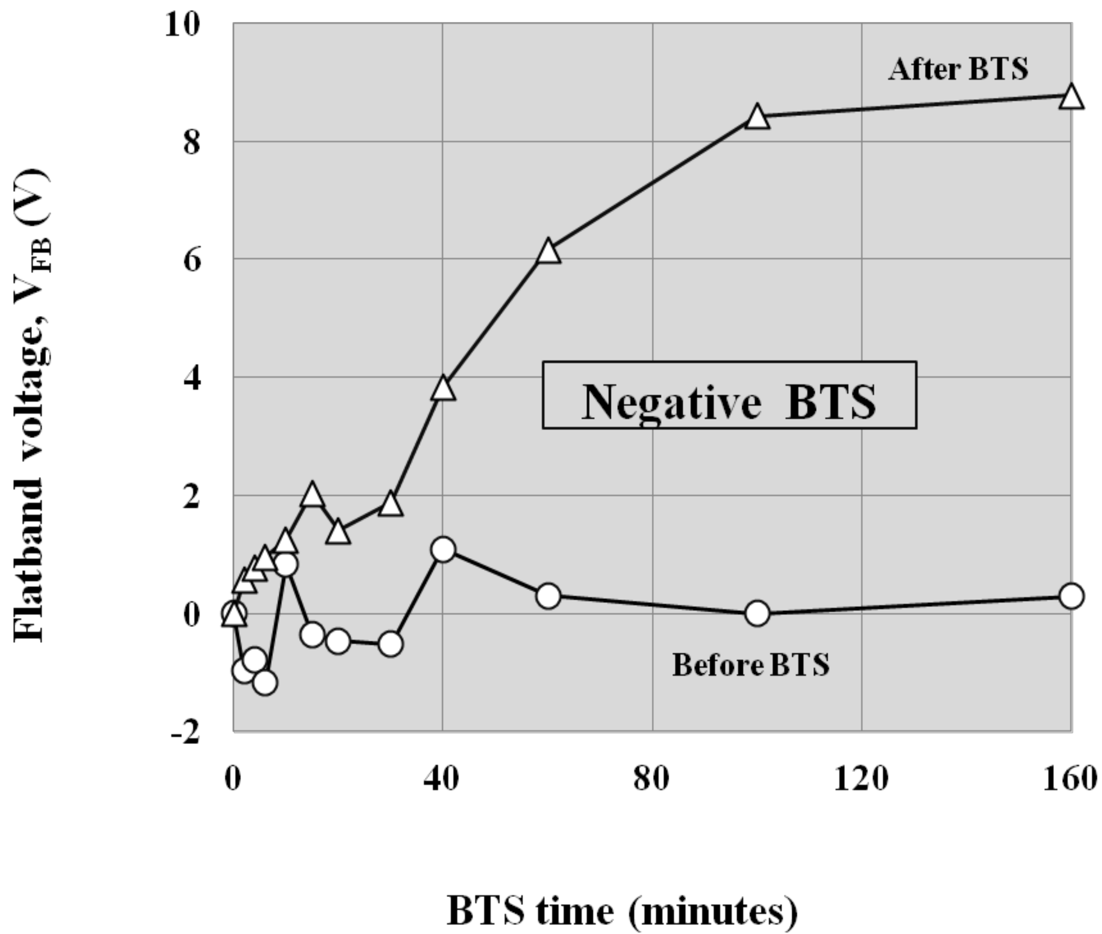


Figure 4.6(b): V_{FB} before and after negative BTS of a MOS-C.

4.7.2 BTS results for MOSFET

Positive BTS results of a phosphorous MOSFET are shown in figure 4.7. The near zero values for V_T again confirms that P-passivation is more effective than NO-passivation in reducing the interface traps. In case of an NO-passivated MOSFET V_T is around 2V. To see how threshold voltages are determined for these curves see section 3.12. The mobility curve before positive BTS is designated as "Before". The induced polar charge at the interface after BTS shifts V_T to left.

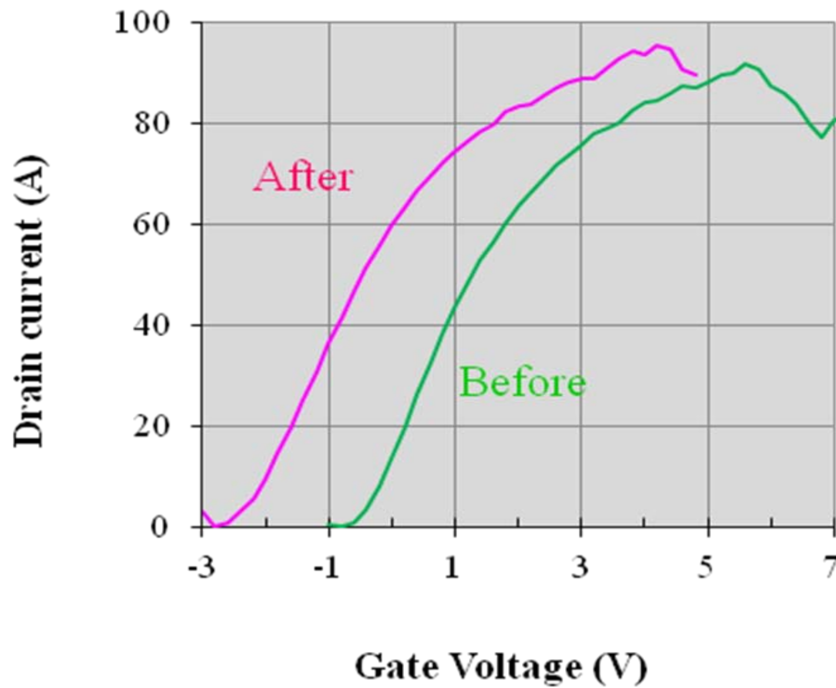


Figure 4.7: Mobility data before and after positive BTS on a phosphorous MOSFET.

4.8 Etching experiment with P-passivation

As discussed above, annealing SiO_2 in a P_2O_5 ambient converts the oxide to a phosphosilicate glass (PSG) layer [40]. PSG is a polar material [41], and if a positive bias is applied at the gate terminal of MOSFET a positive polarization sheet charge appears at the O-S interface. The effect of this charge is similar to the effect of Na^+ ions at the interface – i.e., the presence of either charge or distribution results in an unstable FET threshold voltage that shifts towards negative values and thus "normally-on" instead of "normally-off" operation. XPS results (courtesy of Professor Leonard Feldman at Rutgers) show that PSG layers can be completely removed by etching in buffered HF when the original SiO_2 layer is grown on Si substrate. On the other hand, as shown in figure 4.8(a), buffered HF does not completely

remove PSG layers from SiC. After hard etching (2-3 min is buffered HF), a 2-3nm Si-C-O-P interfacial layer can still be observed. Phosphorous areal density in this layer is around $2x10^{14}$atoms/cm^2 (about one tenth of a monolayer). The areal density of phosphorus before etching is 10^{15}cm^{-2}. We lose P after etching which is consistent with higher trap density for the etched PSG sample shown in figure 4.9(a). Also, there is a right shift of 1eV in the binding energy of the P after etching. This suggests that P is in different chemical environment at the interface compared to the bulk of the PSG layer. Figure 4.8(b) shows the XPS signals from 1s oxygen (O).

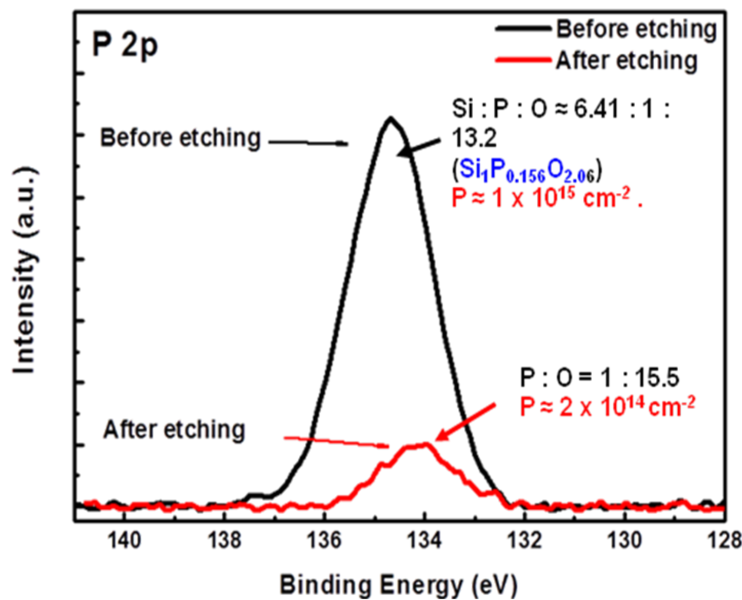


Figure 4.8(a): XPS phosphorous signal from a 100nm PSG layer on 4H-SiC before and etching in buffered HF. The red signal corresponds to ~ $2x10^{14}$ P atoms/cm^2 (about 0.1monolayer) in a Si-O-C-P interfacial layer that does not etch. No interfacial layer containing P is observed after etching PSG layers on Si.

Two questions naturally arise. 1) Is the unetched phosphorous responsible for the low interface trap density and high mobility that we observe? 2) Does the same phosphorous in the interfacial layer exhibit the polar characteristics of PSG, or could the positive polarization

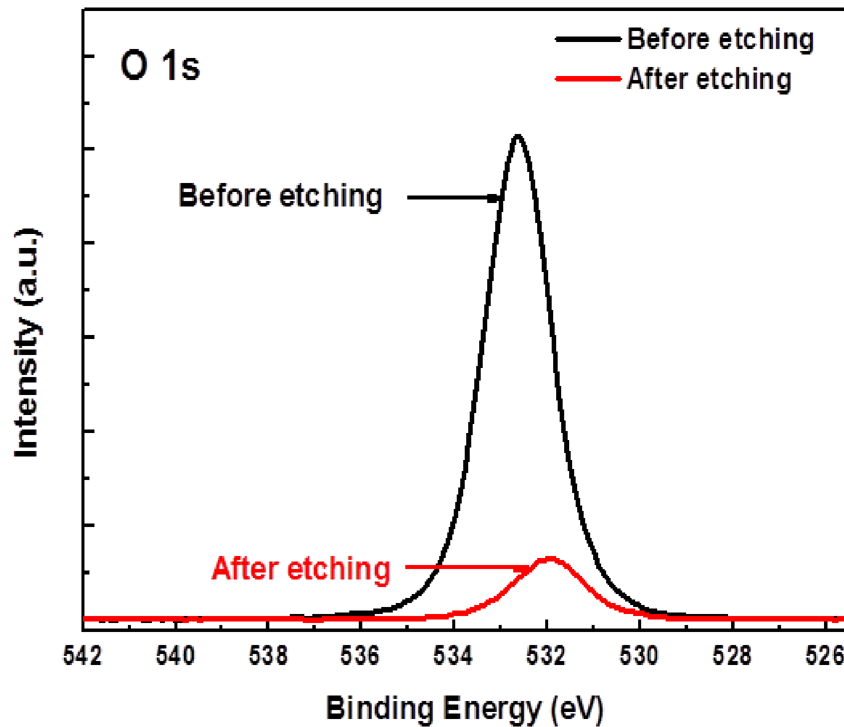


Figure 4.8(b): XPS signal of 1s O from PSG before and after etching.

charge in the original PSG layer has been positioned near the interface but just outside the un-etched layer? These questions have important implications for mobility and threshold voltage stability, and to answer them, we did etching experiments on P passivated MOS caps. We used an LPCVD system operating with TEOS (tetraethylorthosilicate) for SiO_2 deposition at 650°C (well below the temperature for thermal oxide growth on SiC). The experiment involved following steps.

1) Thermal oxidation.

2) Phosphorus passivation at 1000°C.

3) Etching of PSG layer in buffered HF for 2-3 minutes to leave a thin PSG layer.

4) Deposition of a TEOS oxide layer using LPCVD system.

5) Densification of the TEOS layer (950°C, 2hr, 0.5L/min pure N_2).

Electrical results are shown in figures 4.9(a) and 4.9(b).

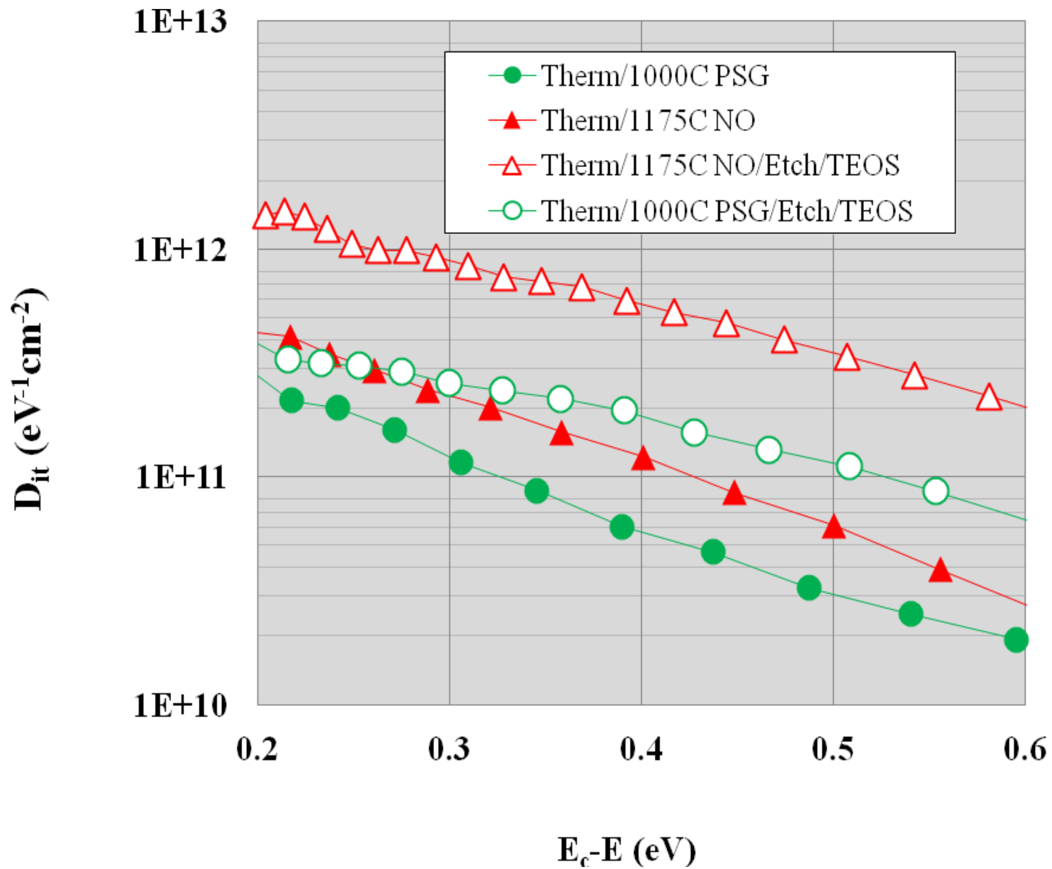
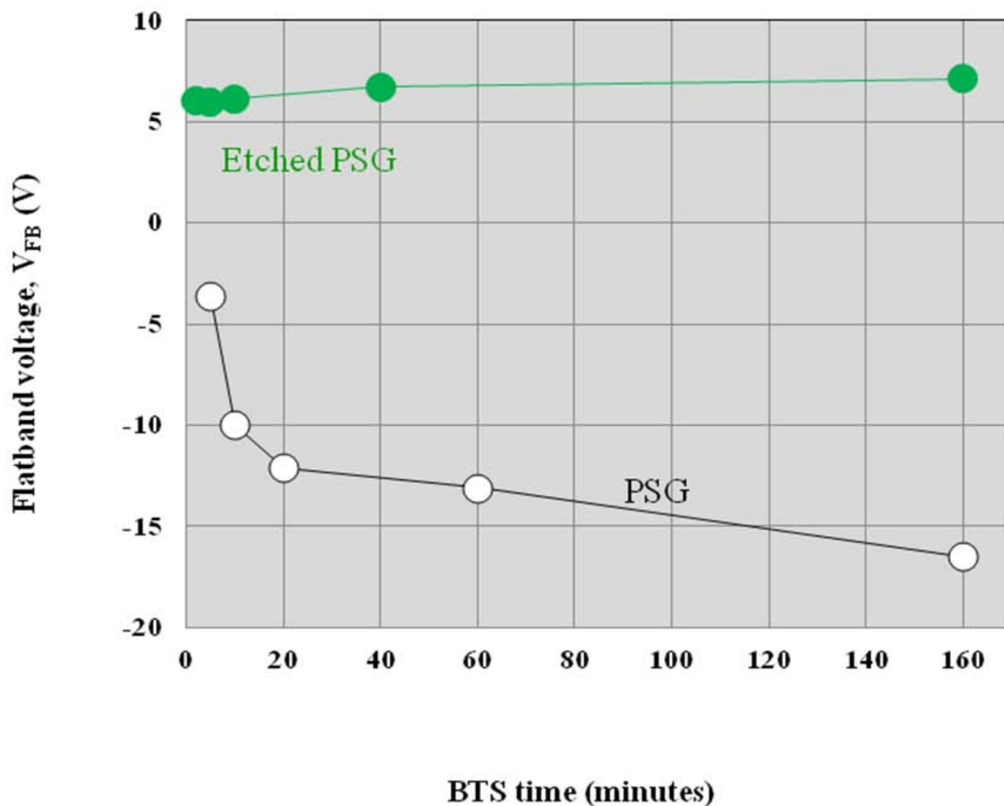


Figure 4.9 (a): Interface trap density before and after etching for NO and PSG MOS caps. Trap density increases after etching.

Etching experiments was also carried out for NO passivated MOS caps. From figure 4.9(a), it is clear that etching increases the interface trap density. Although, there is an increase in the phosphorous trap density, the profile is similar to the profile for an unetched NO MOS-C. The trap density for an etched NO MOS-C is significantly higher and similar to the profile for

an unpassivated interface. These results show that, after etching, there is a loss of both phosphorous and nitrogen from the interface. As a result, we observe increased interface trap densities.

The results of BTS measurements for etched PSG MOS caps are shown in figure 4.10. The etched samples have flatband voltages which remain constant around 6V and are the result of



. Figure 4.9 (b): V_{FB} of a PSG MOS-C before and after BTS.
Device stability improves after etching.

electron injection from the SiC into the PSG layer. The absence of any shift towards negative threshold voltage indicates that the polarization charge at the interface for the etched PSG MOS-C is significantly reduced.

For the unetched PSG devices, polarization charge induces a negative shift in V_{FB} that keeps increasing with increasing BTS time.

BTS results for the etched PSG MOS caps show that, after etching, stability improves at the cost of higher interface trap density.

4.9 Thin phosphorus passivation

Phosphorous passivation of 4H-SiC/SiO_2 interfaces reduces the trap density significantly. After phosphorus passivation, the SiO_2 layer is transformed to phosphosilicate glass (PSG). The thickness of the PSG layer in the devices (MOS/MOSFET) discussed in the previous sections was around 90nm. These devices are hereafter called thick PSG devices. PSG is a polar material and is a source of instability in these devices. In order to stabilize devices after P-passivation, we designed an experiment based on using a thin PSG layer (~6nm). We first grew a thin thermal oxide and then performed a 2hr phosphorus passivation anneal. The thin PSG layer was then capped with a TEOS deposited oxide (~ 45nm). The TEOS deposition was performed using an in-house LPCVD system by cracking tetraethylorthosilicate (TEOS) at 650°C and 0.6Torr. To improve the breakdown characteristics, the deposited oxide was densified at 850°C for 2hr in nitrogen ambient. Figure 4.10 shows the different layers in a thin PSG MOS-C. The total thickness of the composite layer (thin PSG layer + deposited oxide layer) was around 50nm. Thin PSG experiment involves the following steps

1) Thermal oxidation to get ~ 6nm of SiO_2 layer.
2) P-passivation of the interface for 2 hours.
3) Deposit ~ 45nm of SiO_2.
4) Densify the deposited oxide at 850°C for two hours.

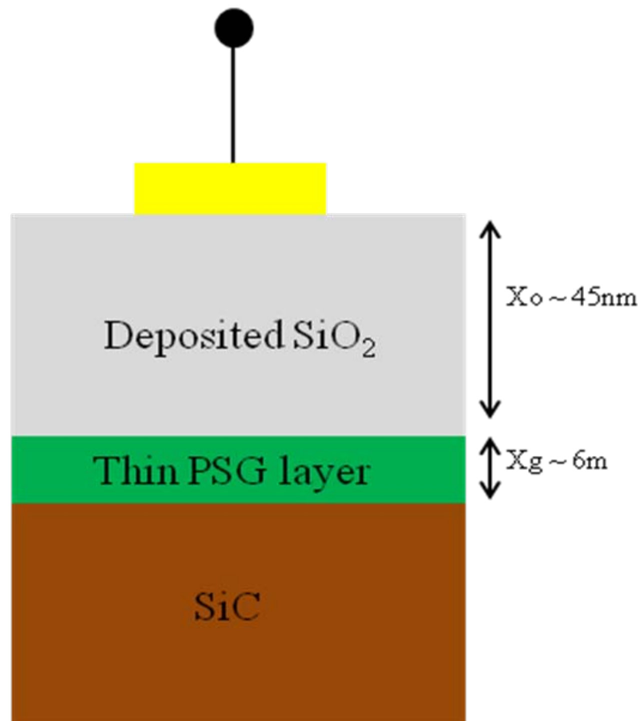


Figure 4.10: Thin PSG MOS-C.

4.9.1 Device fabrication

MOS capacitors were fabricated on n/n+, 8° off-axis, 4H wafers with a 5µm n-epilayers doped with nitrogen at $8.3 \times 10^{15} cm^{-3}$. All the samples were cleaned prior to processing using a standard RCA process. Dry thermal oxides were grown at 1150°C (~ 6nm) and passivated with phosphorous, after 275nm, high purity Mo gate contacts were sputter deposited. Broad area backside contacts were formed using Ag colloidal paste after backside oxide removal. Standard high-low (1MHz/quasi-static) capacitance-voltage (C-V) measurements were performed to determine the interface trap density in the top half of 4H-SiC band gap.

Planar MOSFETs were fabricated on a 4° off-axis 5µm p-epilayer grown on an n^+ substrate. The epilayer was doped with Al at $8 \times 10^{15} cm^{-3}$. The gate length was 120µm. Length and width of source and drain were 200µm and 400µm, respectively.

4.9.2 Results and discussion

The results of a high-low (1MHz/quasi-static) C-V measurement for a thin MOS-C are shown in figure 4.11(a). The corresponding interface trap density is shown in figure 4.11(b) and compared to results for thick PSG and NO. D_{it} value for thin PSG MOS device is $3x10^{11}eV^{-1}cm^{-2}$ at E_c - E = 0.2eV which is two times lower than NO passivated device. Mobility measurement results for lateral 4H-SiC MOSFET are shown in figure 4.12.The device has a peak channel mobility of $72cm^2/V.s$. This number is approximately 2x higher compared to NO device. Figure 4.12 also shows mobility for a thick PSG MOSFET (~ 90nm composite oxide thickness). Although the mobility of thick PSG device is higher, the device is plagued with threshold voltage instability. The breakdown field for thin PSG device is NO-like, but its leakage current is significantly higher (though still acceptable) as shown in figure 4.13.

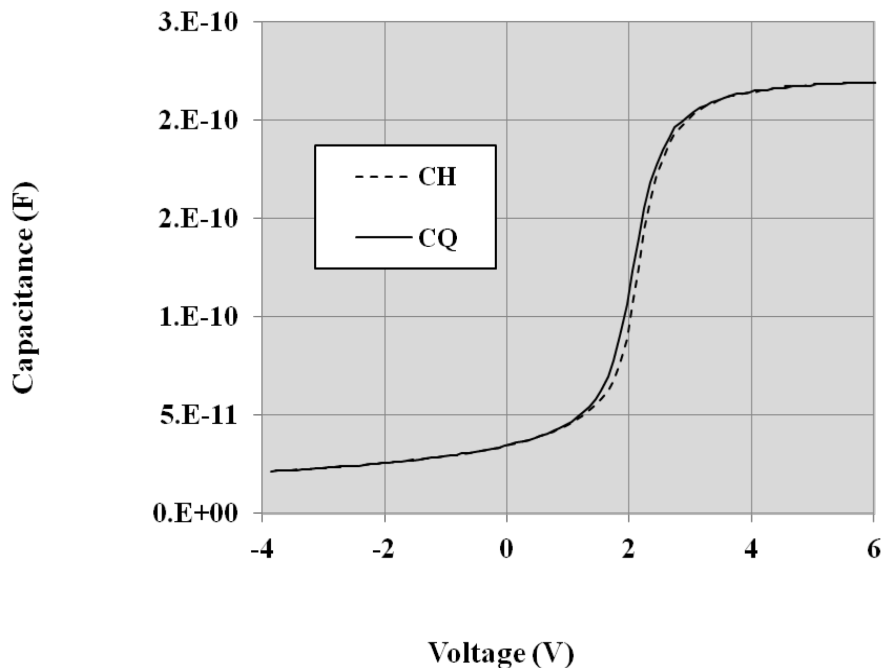


Figure 4.11(a): C-V characteristics of thin PSG MOS-C.

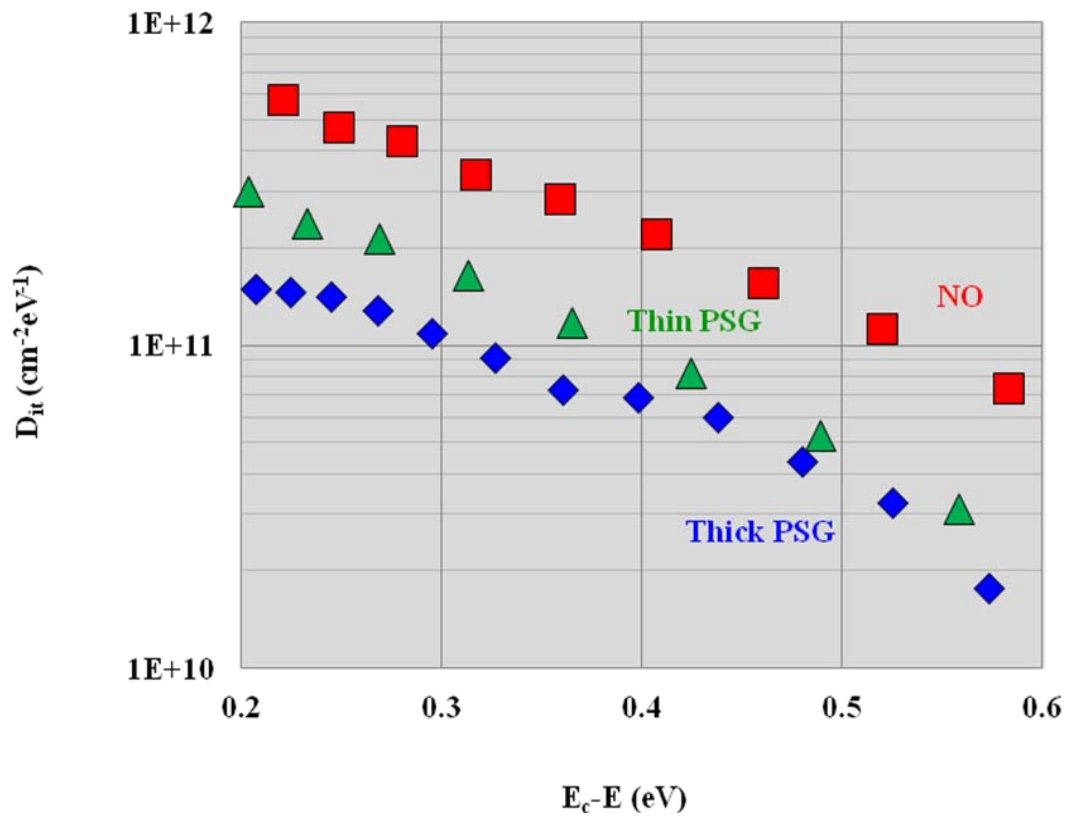


Figure 4.11(b): Interface trap density, Di_t, for thin PSG-MOS-C. Dit is lower compared to NO device, but higher compared to thick (~90nm) PSG device.

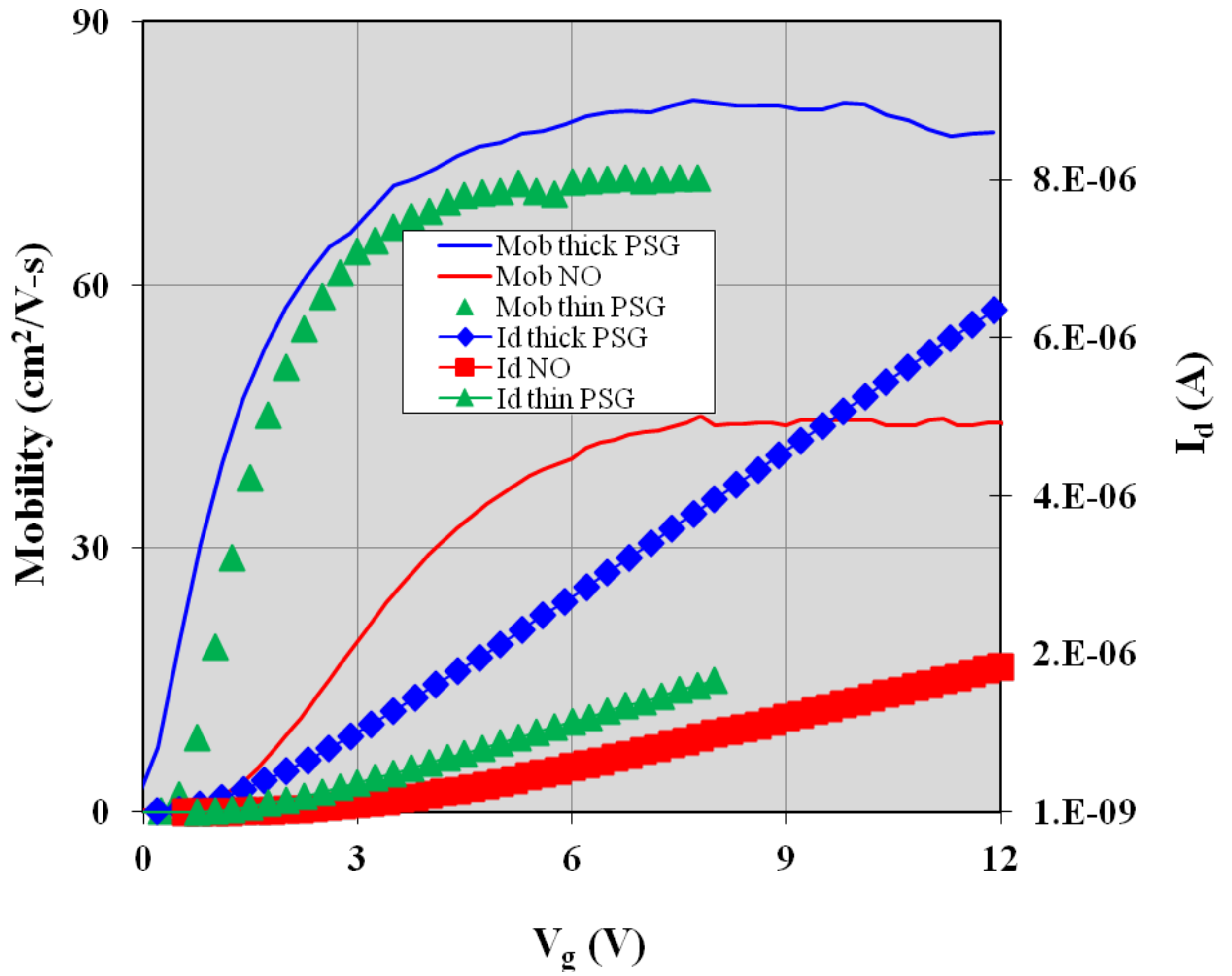


Figure 4.12: Mobility data for a thin PSG-MOSFET compared to thick PSG and NO.

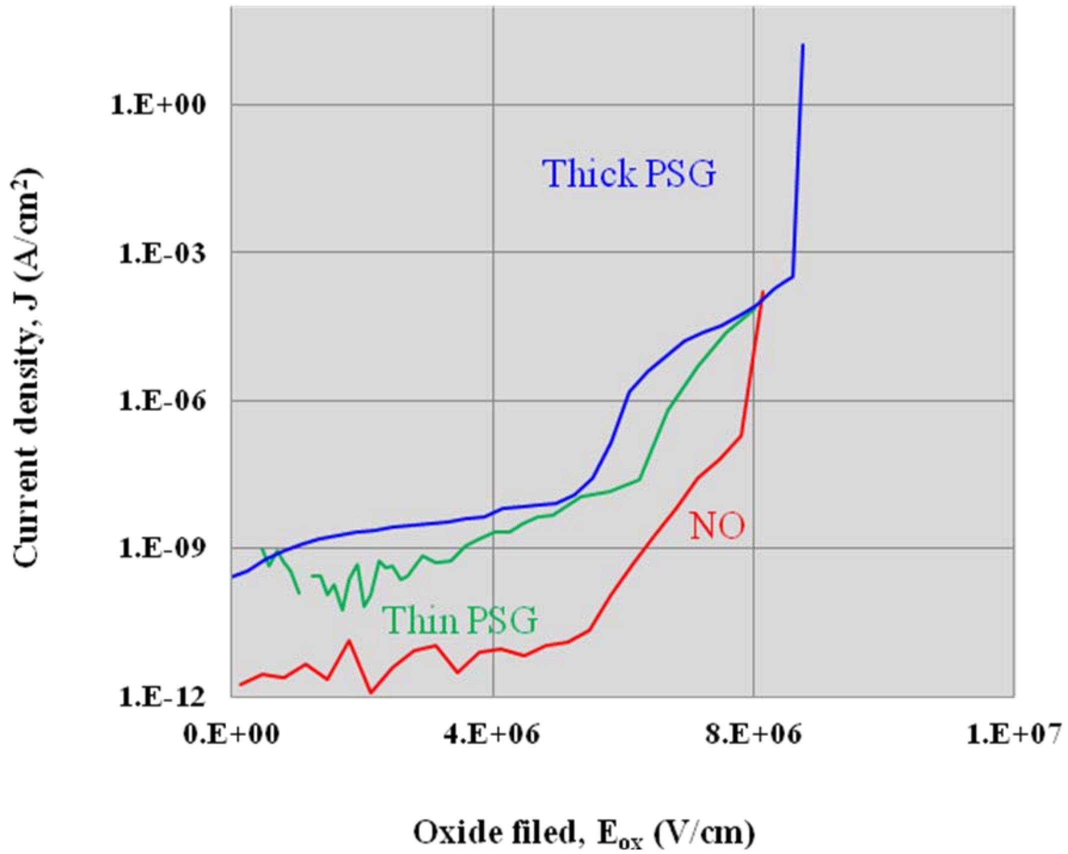


Figure 4.13: The electric of breakdown for thin PSG device is same as for NO device ~ 8MV/cm

Positive BTS results for thin PSG MOS caps and MOSFETs are shown in figures 4.14 and 4.15, respectively. Positive biases for an oxide field of 1.5MV/cm were applied at 150°C for all samples. A different capacitor was subjected to bias-temperature stressing for each of the BTS times indicated in figure 4.14. The positive shift for V_{FB} in the BTS measurements of MOS caps is due to the electron injection and is a well-known phenomenon in NO passivated devices [43]. The thin PSG devices show much improved stability in flatband voltage. Figure 4.15 shows mobility results before and after positive BTS for 8 hours. And as we can see, there is only slight right shift (possibly due to electron injection) in the mobility curve

following BTS. This is again a confirmation of improved stability using the thin PSG process.

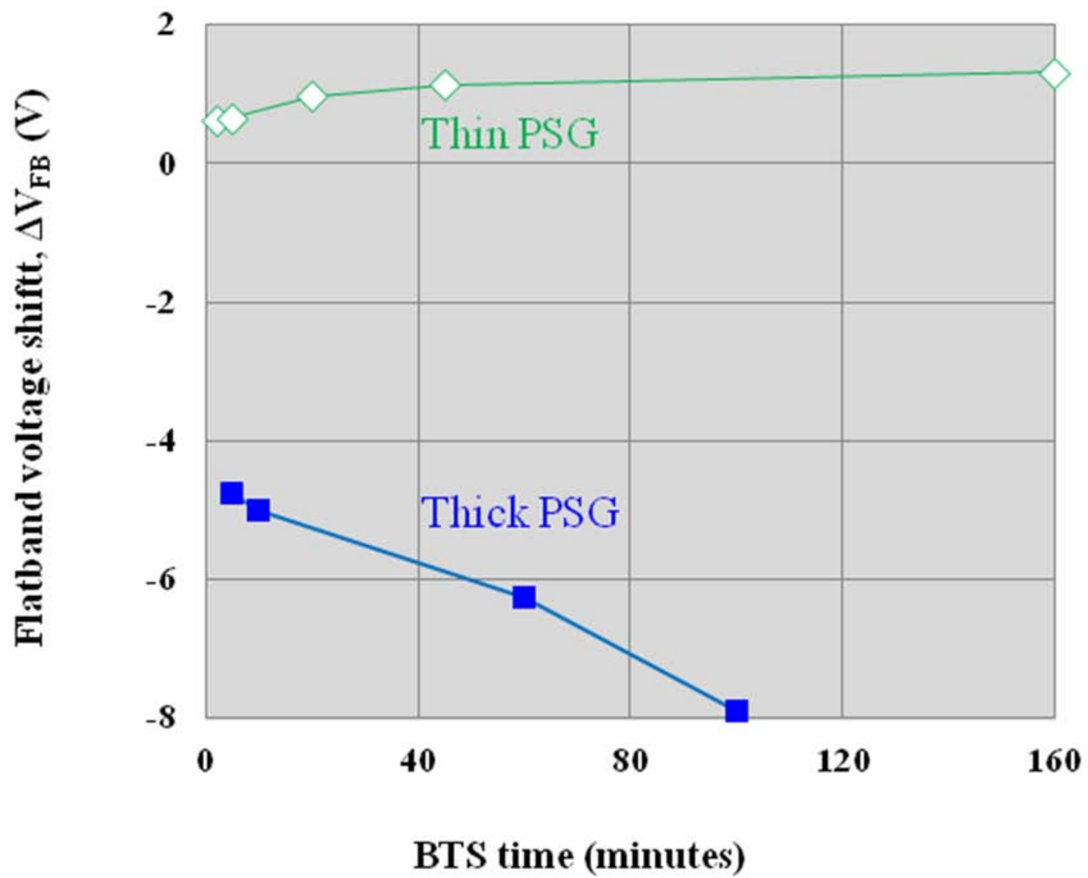


Figure 4.14: Positive BTS data of a thin PSG MOS-C. Data shows improved device stability. $\Delta V_{FB} = V_{FB}^{final} - V_{FB}^{initial}$.

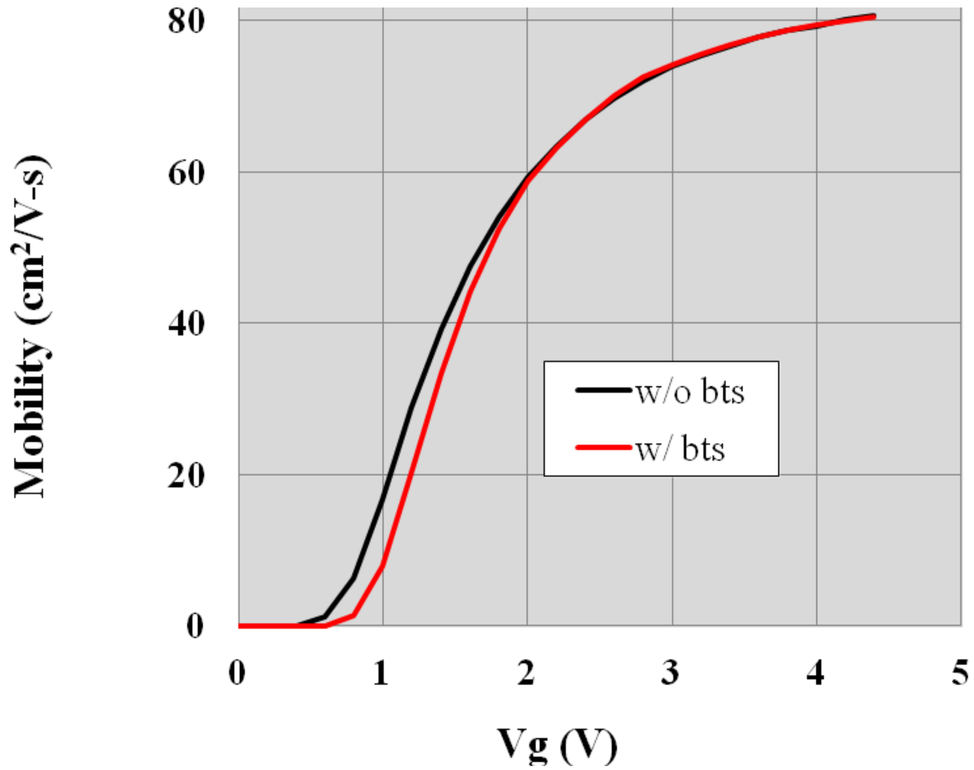


Figure 4.15: Mobility data with and without 8hr positive BTS.

The stability of thin PSG devices is due to less polarization. For a given BTS voltage, there is a direct dependence of the shift in flatband voltage (ΔV_{FB}) on the thickness of the PSG layer [44].

$$\Delta V_{FB} = Q_p / C_g = Q_p X_g / \varepsilon_o K_g$$

$$= - \frac{K_o X_g \chi_p V_p}{K_g [(K_g + \chi_p) X_o + K_o}$$

Q_p = polarization charge,

C_g = capacitance of PSG layer,

X_g = thickness of thin PSG layer,

X_o = thickness of deposited oxide layer,

K_g = dielectric constant of PSG layer,

K_o = dielectric of deposited oxide,

ε_o = permittivity of deposited oxide,

χ_p = polarizability of PSG layer and,

V_p = voltage during BTS.

We see from above expression that for finite bias (V_p), ΔV_{FB} decreases with decreasing X_p. By reducing the thickness of PSG layer to 10-12nm, device stability in improved and the advantage of higher mobility compared to NO is maintained. There must be a minimum thickness of the PSG layer to keep the passivation effect of P on the interface traps.

To summarize briefly, by reducing the thickness of the PSG layer we can stabilize the device and at the same time do not lose the beneficial effect of phosphorus passivation. We need BTS measurements at higher temperatures (higher than 150°C), higher electric fields (higher than 1.5MV/cm) and for longer time intervals to compare the stability of thin PSG devices with the stability of NO devices.

4.10 References

[1] M. Di Ventra and S.T. Pantelides, *Phys. Rev. Lett.* **83**, 624 (1999).

[2] J. M. Kanup, Peter DeáK, and T. Frauenheim, *Phys. Rev. B* **71**, 235321 (2005).

[3] J.L. Cantin, H.J. Bardeleben, and W.J. Choyke , *Phys. Rev. Lett.* ***92***, 015502 (2004).

[4] F. Devynck and A. Pasquarello, Physica B: Condensed Matter **401**, 556 (2007).

[5] V.V. Afanasev, M. Bassler, G. Pensl, and M. Schulz, *Phys. Sta.sol.(a)* **162**, 321 (1997).

[6] X. Shen, M.P. Oxley, Y. Puzyrev, B.R. Tuttle, and G. Duscher, J. Appl. Phys. **108**, 123705, (2010).

[7] X. Shen and S.T. Pantelides, *Mater. Sci. Forum* **717-720**, 445 (2012).

[8] G.L. Harris, *Properties of Siliocn Carbide*, IEEE INSPEC (1995).

[9] F. Ren and J. C. Zolper, *Wide Energy Bandgap Electronics Devices,* World Scientific Publishing (2003).

[10] J.A. Cooper Jr., *Phys. Sta. Sol.(a)* **162**, 305 (1997).

[11] T. Zheleva, A. Lelis, G. Duscher, F. Liu, I. Levin, and M. Das, *Appl. Phys. Lett.* **93**,022108(2008)

[12] P. Friedrichs and E.P. Burte, *J. Appl. Phys.***79**, 7814 (1996).

[13] R. Schorner, P. Friedrichs, D.Peters, and D. Stephani, *IEEE Elec. Dev. Lett.* **22**, 176 (2001).

[14] P. Friedrichs, T. Kimoto, L. Ley, and G. Pensl, *Silicon Carbide,* Wiley-VCH (2009).

[15] G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, R. K. Chanana, Robert A. Weller, S. T. Pantelides, Leonard C. Feldman, Member,O. W. Holland, M. K. Das, and John W. Palmour, *IEEE Elec. Dev. Lett.* **22**, 176 (2001).

[16] G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, M. Di Ventra, R.K. Chanana, S. T. Pantelides, Leonard C. Feldman, and R. A. Weller, *Appl. Phys. Lett.***77**,3601(2000).

[17] G. Gudjónsson, H.Ö. Ólafsson and E. O. Sveinbjornsson, *Mater. Sci. Forum* **457-460**,1425 (2004).

[18] L. A. Lipkin, M.K. Das, and J.W. Palmour, *Mater. Sci. Forum* **389–393**, 985 (2002).

[19] S. Wang, S.Dhar, A. C. Ahyi, A. Franceschetti, S. T. Pantelides, Leonard C. Feldman, and J. R. Williams, *Phys. Rev. Lett.* **98**, 026101-1 (2007).

[20] K. Fukuda, S. Suzuki, T. Tanaka, and T. K. Arai, *Appl. Phys. Lett* **12**, 1585 (2000).

[21] J. Senzaki, K. Kojima, S. Harada, R. Kosugi, S. Senzaki, and K. Fukuda, *IEEE Elec. Dev. Lett.* **23**,13 (2002).

[22] K. Ueno and T. Oikawa, *IEEE Elec. Dev. Lett.* **20**, 624 (1999).

[23] F. Moscatelli, A. Poggi, S. Solmi, and R. Nipoti, *IEEE Tran. Elec. Dev.* **55**, 961 (2008).

[24] S. Dhar, S. H. Ryu, and A. K. Agarwal, *IEEE Trans. Elec. Dev.* **57**, 1195 (2010).

[25] E,O. Sveinbjornsson,F. Allerstam, G. Gudjónsson, H.Ö. Ólafsson, D. Dochev, T. Roddle,and R. Jos, *Mater. Sci. Forum* **556-557**, 487,(2007).

[26] H. Yano, T. Hirao, T. Kimoto, H. Matsunami, K. Asano and Y. Sugawara, *IEEE Electron Dev. Lett.* **20**, 613 (1999).

[27] T. Hatayama, S. Hino, N. Miura, T. Oomori and E. Tokumitsu , *IEEE Tran. Electron Dev.* **55**, 2041 (2008).

[28] X. Zhu, *Alternative Growth and Interface Passivation Techniques for SiO2 on 4H-SiC*, Dissertation, Auburn University, AL, U.S.A. (2008).

[29] D. Okamato, H. Yano, T. Hatayama and T. Fuyuki, *IEEE Electron Dev. Lett.* **31**, 710 (2010).

[30] S.K. Dixit, S. Dhar, J. Rozen, S. Wang, R.D. Schrimpf, D.M. Fleetwood, S.T. Pantelides, J.R. Williams and L.C. Feldman, *IEEE Tran. Electron Dev.* **53**, 3687 (2006).

[31] J. Rozen, S. Dhar, S. K. Dixit, V. V. Afanas'ev, F. O. Roberts, H. L. Dang, S. Wang, S. T. Pantelides, J. R. Williams and L. C. Feldman, *J. Appl. Phys.* **103**, 124513 (2008).

[32] D. Okamoto, H. Yano, S. Kotake, T. Hatayama, and T. Fuyuki, *Mater. Sci. Forum* **679-680**, 338 (2011).

[33] A. Nakahira, K. Konishi, K. Yokota, T. Honma, H. Aritani, and K. Tanaka, *J. Ceram. Soc. Jpn.* **114**, 46 (2006).

[34] A.-M. Goncalves, O. Seitz, C. Mathieu, M. Herlem, and A. Etcheberry, *Electrochem. Comm.* **10**, 225(2008).

[35] C. C. Tin, S. Mendis, K. Chew, I. Atabaev, T. Saliev, E. Bakhranov, B. Atabaev, V. Adedeji, and Rusli, *Thin Solid Films* **518(24) Supplement 1**, 118 (2010).

[36] Charles Evans Associates, private communication.

[37] X. Shen and S. T. Pantelides, *Appl. Phys. Lett.* **98**, 053507 (2011).

[38] Y. Liu, M.R. Halfmoon, C.A. Rittenhouse and S. Wang, *Appl. Phys. Lett.* **97**, 242111(2010).

[39] B. R. Tuttle, S. Dhar, S.-H. Ryu, X. Zhu, J. R. Williams, L. C. Feldman, and S. T. Pantelides, *J. Appl. Phys.* **109**, 023702 (2011).

[40] E.H. Snow and B.E. Deal , *J. Electro. Soc.,* **113**,263 (1966).

[41] E.H. Snow and M.E. Dumesil, *J. Appl. Phys.*, **117** (1966).

[42] Y. K. Sharma, A. C. Ahyi, T. Issacs-Smith, X. Shen, X. Zhu, L.C. Feldman, and J.R. Williams, *Solid-State Electron.* **68**, 103 (2012).

[43] Aivars J. Lelis, Daniel B. Habersat, Ronald Green, and Neil Goldsman, *Mater. Sci. Forum* **600-603**, 807 (2009).

[44] J. M. Eldridge, R. B. Laibowitz, and P. Balk, *J. Appl. Phys*. **40**, 1922 (1968).

CHAPTER 5

Nitrogen plasma passivation

Standard (i.e., NO) nitridation of the 4H-SiC/SiO_2 interface increases the inversion channel mobility from single digits (~ 8cm^{2}/V.s) to 30cm^2/V.s [1,2,3] with a trap density D_{it} of around $1x10^{12}eV^{-1}cm^{-2}$ at $E_c - E = 0.2eV$. The mobility of 30cm^2/V.s is still far less compared to the bulk mobility of silicon carbide which is 950cm^2/V.s for lightly doped material [4]. Phosphorus passivation is more effective than NO for trap passivation as discussed in detail in chapter 4. Mobility is 2.5 times higher, at around 80cm^2/V.s, after P-passivation. Phosphorus transforms SiO_2 to phosphosilicate glass (PSG) [5]. PSG is a polar material, and polarization charge is source of instability in these devices [6,7]. The problem of instability can be minimized by using composite gate stacks fabricated with a thin PSG layer (< 10nm) capped with an unpassivated deposited oxide (~ 60nm). A typical thin PSG MOSFET mobility is around 70cm^2/V.s.

In addition to the NO and PSG processes, trap passivation can be accomplished using nitrogen plasma passivation (N2P-passivation). Zhu et al. reported NO-like trap density with N2P-passivation [8]. In a continuation of Zhu's work, we have used an upgraded plasma system to obtain trap densities similar to the best that we have measured for P-passivated oxides. During NO nitridation, there is the formation atomic N and O [9]. The N leads to passivation of interface traps while the atomic oxygen causes additional oxidation. These two processes compete with each other - trap passivation and trap formation by continued oxidation. Nitrogen plasma passivation introduces atomic nitrogen using pure nitrogen and thus minimizes oxide growth during the passivation process. As a result, more nitrogen may remain at the interface for better trap passivation.

Before passivation, the system is flushed with nitrogen such that passivation takes place in minimal oxygen ambient. The N2P process results in almost no oxidation of SiC and thus to

very little carbon liberation compared to thermal oxidation and NO passivation. [10,11]. Carbon contributes to a higher interface tarp density, and carbon may also contribute to defect formation in the SiC channel region. Both factors contribute to low channel mobility [12,13]. N2P-passiavtion of thin deposited oxides followed by deposited oxide capping limits carbon liberation and enables studies of the role of carbon in degrading the channel mobility. To check this hypothesis, we have proposed fabrication processes for a "low carbon" MOSFET.

5.1 Set-up

The N2P system is shown in figure 5.1(a). Figure 5.2(b) is the schematic of process that occurs in the furnace. The furnace tube is GE 224 low sodium quartz, 6.5cm in diameter with a heated length of 46cm. The furnace operates at a maximum temperature of 1200°C. A 10kW, 2.54GHz microwave generator is attached to the furnace via a waveguide and used to produce nitrogen plasma. The furnace is equipped with two mechanical pumps such that a pressure of 2-3 Torr can be maintained during the high flow (3L/min) of high purity nitrogen gas (99.999%). The system is also equipped with a dampener to dissipate the unused microwave energy. A radiation detector is used after nitrogen plasma generation to determine that minimal microwave radiation escaped the system.

Ground state atomic nitrogen is created in the microwave plasma, and a portion of these atoms recombine to emit at visible wavelengths. Figure 5.1(c) shows a typical optical spectrum recorded with an Ocean Optics USB2000 spectrometer. In the spectrum, the peak corresponding to wavelength 589nm results from the recombination of active ground state (^{4}S) nitrogen atoms followed by the decay of an excited state in the nitrogen molecule and gives rise to yellow afterglow [14]. This afterglow is attributed to the recombination reaction of ground state of nitrogen atoms. The production of afterglow takes place by following mechanism.

Also, the intensity of yellow-afterglow of emission is proportional to the square of concentration of active ground state atoms. The amount of radiation detected at 589nm is therefore a measure of the atomic nitrogen concentration in the plasma. [15,16] The plasma system currently operates at 1160°C, 2.8Torr, and 3L/min. The passivation process can be divided in to two parts - N2 plasma exposure and recovery without microwave power.

5.1.1 Nitrogen plasma (N2P) exposure

Samples are loaded in the plasma treatment furnace prior to generating a plasma. The various steps leading to plasma generation are listed below. After generation of a plasma, samples are typically exposed for 4-8hr.

1) Pump furnace pressure to 1mTorr.

2) Introduce nitrogen at 0.25L/min.

3) Set furnace temperature to 1160°C.

4) Increase nitrogen flow to 3L/min after set temperature is achieved.

5) Maintain pressure inside the furnace by adjusting the vacuum pump inlet valve.

6) Initiate plasma by powering on the microwave generator. Proper tuning will reduce the reflected power to almost 0W.

7) Maintain the output power of generator at 2kW.

Figure 5.1(a): High temperature microwave plasma furnace used for nitrogen plasma passivation (N2P-passivation).

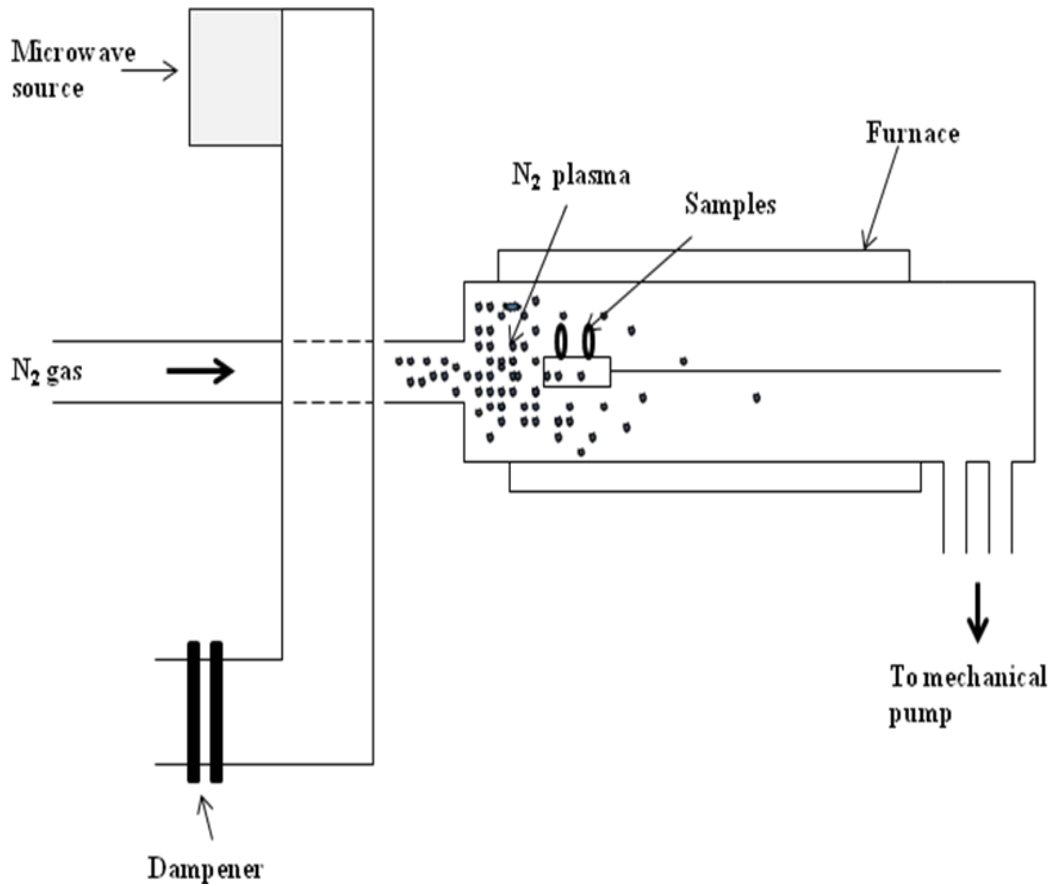


Figure 5.1(b): Schematic of the process during N2P-passivation.

5.1.2 Recovery

A recovery step is required in order to repair the damage caused during the exposure of the samples to N2 plasma. Damage is caused by the bombardment of the oxide with electrons, nitrogen ions and fluctuations associated with nitrogen plasma during exposure. Recovery is performed with the following steps.

1) Stop plasma generation by powering off the microwave generator.

2) Bring the furnace back to atmospheric pressure.

3) Decrease the N_2 flow rate to 0.5L/min.

4) Maintain temperature at 1160°C.

Depending upon the exposure time, N2P-passivation recovery times are 2hr (4hr N2P-passivation) or 6hr (8 hours N2P passivation).

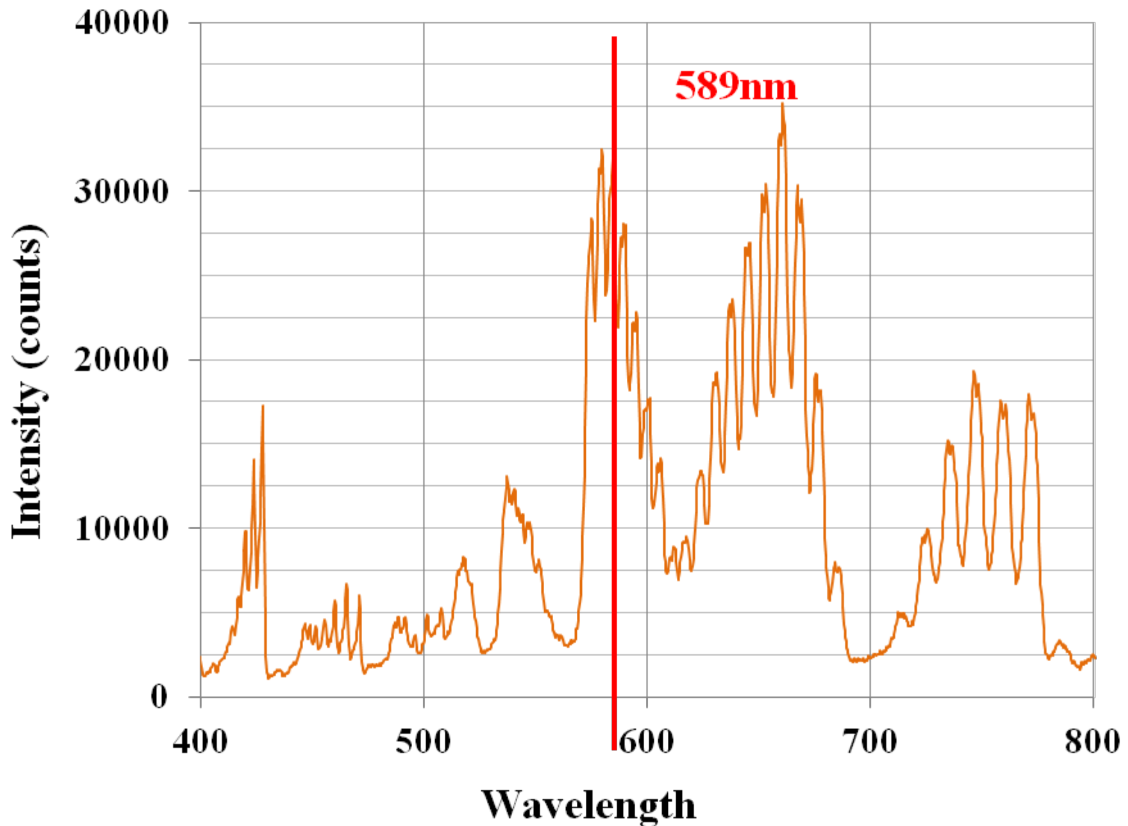


Figure 5.1(c): Typical emission spectrum of nitrogen during N2P-passivation.

5.2 Four hour N2P-passivation

5.2.2 Thermal oxide

Results for 4hr N2P-passivation with 2hr recovery are shown in figures 5.2(a) and (b). The interface trap density of the N2P MOS-C and the mobility of N2P FET are both "NO-like". The oxides were grown using our standard dry oxidation process for a thickness of 70nm. The threshold voltage determined by extrapolating the linear portion of the drain current – gate voltage curve in figure 5.2(c) V_T is around 3V [figure 2.2(c)].

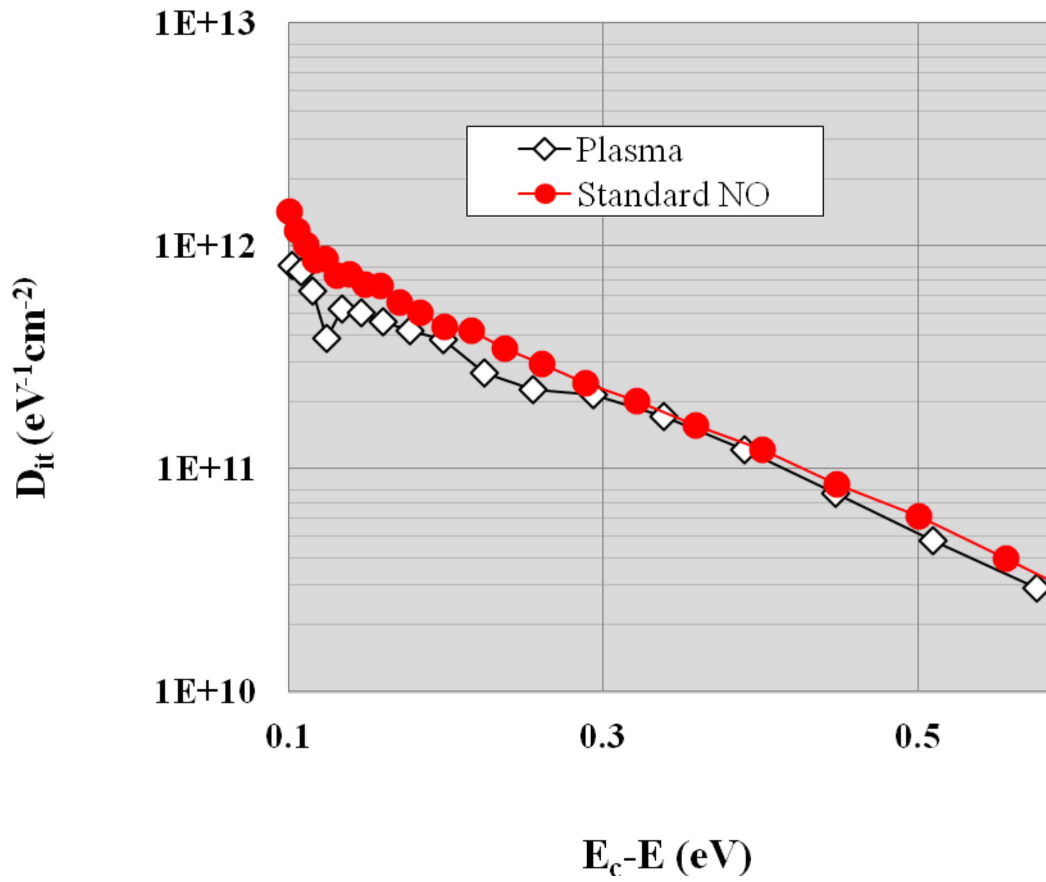


Figure 5.2(a): Interface trap density for 4hr N2P-passivation compared to NO-passivation.

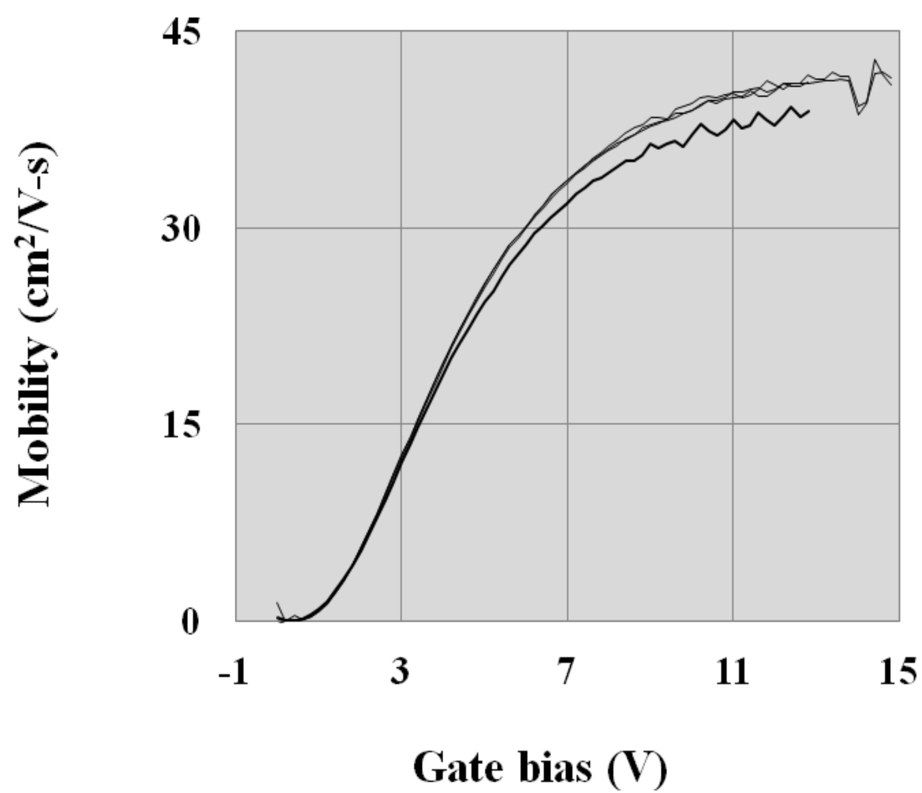


Figure 5.2(b): Mobility for 4hr N2P-passivation.

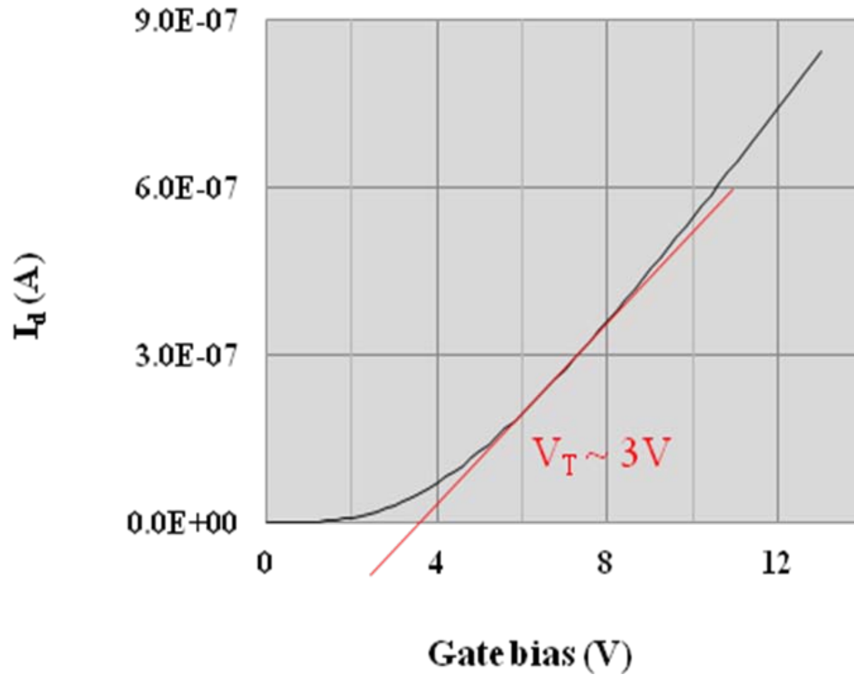


Figure 5.2(c): Threshold voltage (V_T) for a 4hr N2P-passivation.

Figure 5.2(e) depicts breakdown characteristics of the oxide after N2P-passivation. The breakdown field is ~ 4MV/cm, and the gate leakage current is significantly higher compared to NO. Higher leakage current is an indication of oxide degradation that is not repaired during the recovery anneal.

5.2.3 Deposited oxide

To limit carbon liberation, thermal oxide layers can be replaced by deposited oxides. We used an LPCVD system with TEOS as a precursor to deposit SiO_2 layers. The interface trap density for a 60nm deposited was found to be NO-like [similar to figure 5.2(a)]. The mobility for a companion MOSFET is shown in figure 5.3. The peak value of 50cm^2/V.s is higher than

typical values of 30-40cm^2/V.s obtained using NO. The threshold voltage of the N2P FET (I_d-V_g plot not shown) is similar to V_T for an NO MOSFET at around 3V.

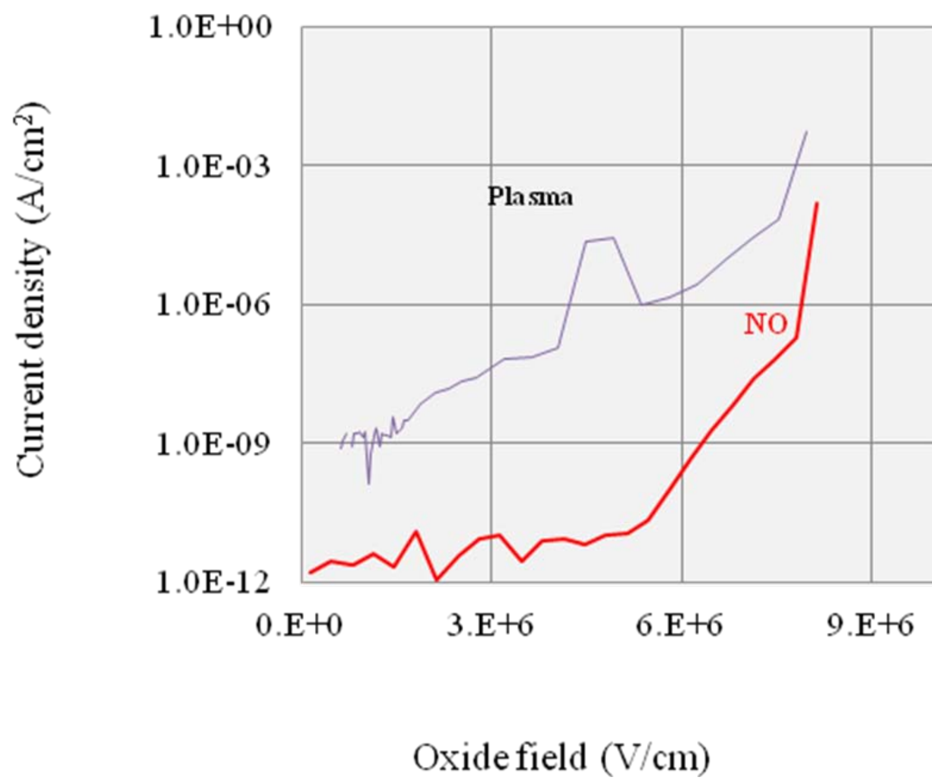


Figure 5.2(d): Breakdown characteristics of a MOS-C after 4hr N2P-passivation.

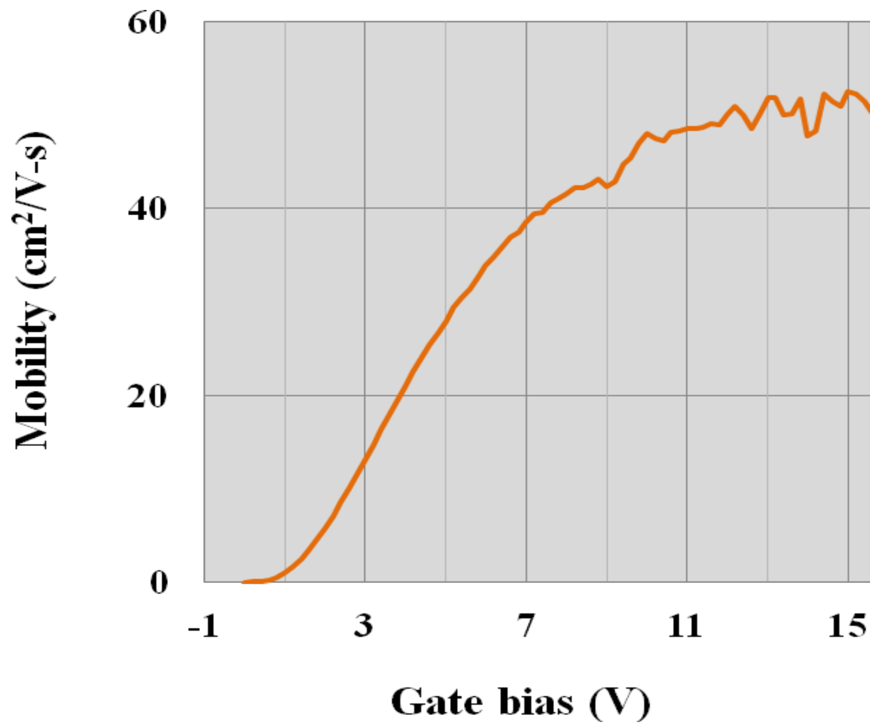


Figure 5.3: Mobility for 4hr N2P-passivation. A 60nm deposited oxide was used for gate.

5.3 Eight hour N2 plasma passivation

The interface trap density after eight hours of nitrogen plasma passivation with 6hr recovery is shown in figure 5.4 for 60nm thermal oxides. The interface trap density at E_c - E = 0.2eV is $2x10^{11}cm^{-2}eV^{-1}$. Also shown are trap densities for NO and P passivated MOS caps. D_{it} for the 8hr N2P process compares favorably with the trap density measured for the PSG process (the lowest that we have ever measured). However, recall that thick PSG devices are unstable due to polarization effects. There is no instability after N2P-passivation because the process generates nothing similar to PSG polarization charge. Figure 5.5(a) shows SIMS (Secondary Ion Mass Spectroscopy) profile for a MOS-C after 8hr N2P-passivation. The nitrogen

concentration is highest at around 60nm which corresponds to the O-S interface in the MOS-C. Figure 5.5(b) shows XPS data for 8hr N2P passivated MOS-C. The oxide was etched in buffered HF before the measurements. The N concentration at the interface increases with increasing passivation time (from 4hr to 8hr) and results in more interface trap passivation. The areal density of nitrogen at the interface for different passivation times is listed in table 5.6. Four hour N2P passivation and standard NO passivation introduces the same amount of

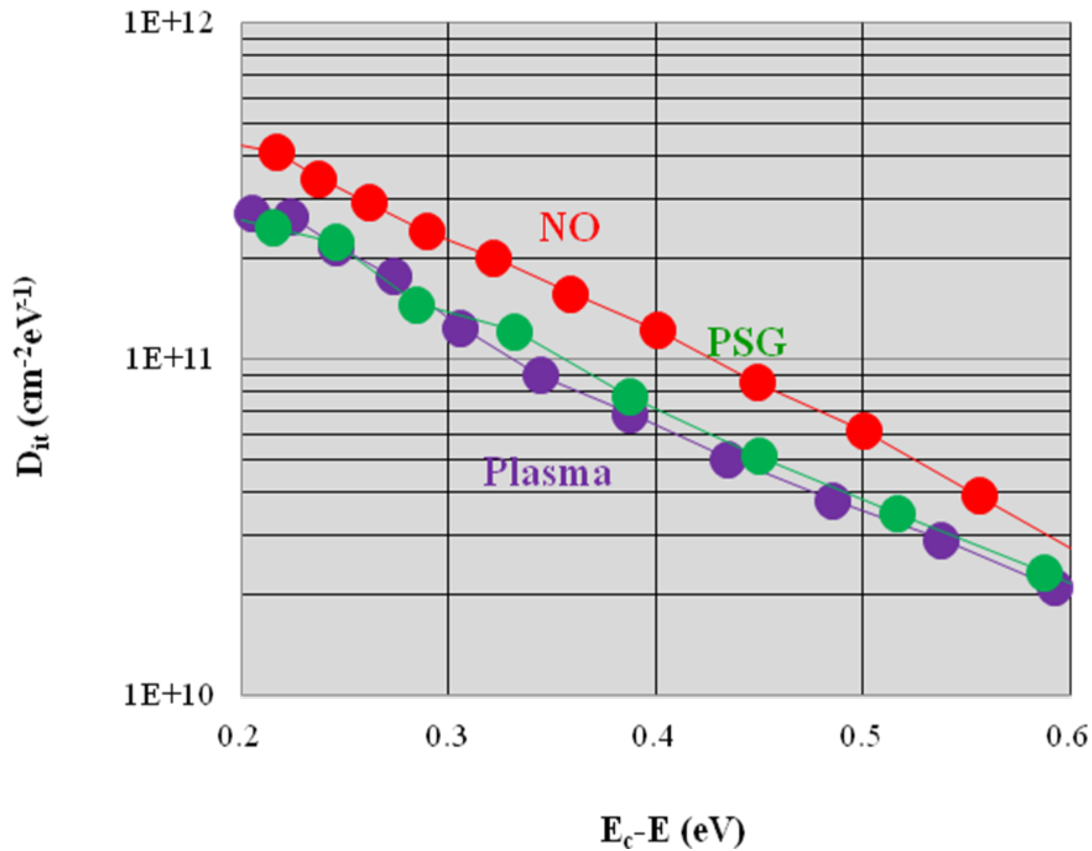


Figure 5.4: Interface trap density for 8hr N2P-passivation compared to NO and phosphorous.

nitrogen at the interface, resulting in similar trap densities. Figure 5.7 shows breakdown characteristics after an 8hr N2P passivation. The oxide is leaky compared to NO, and the breakdown field is lower (around 2MV/cm for some devices).

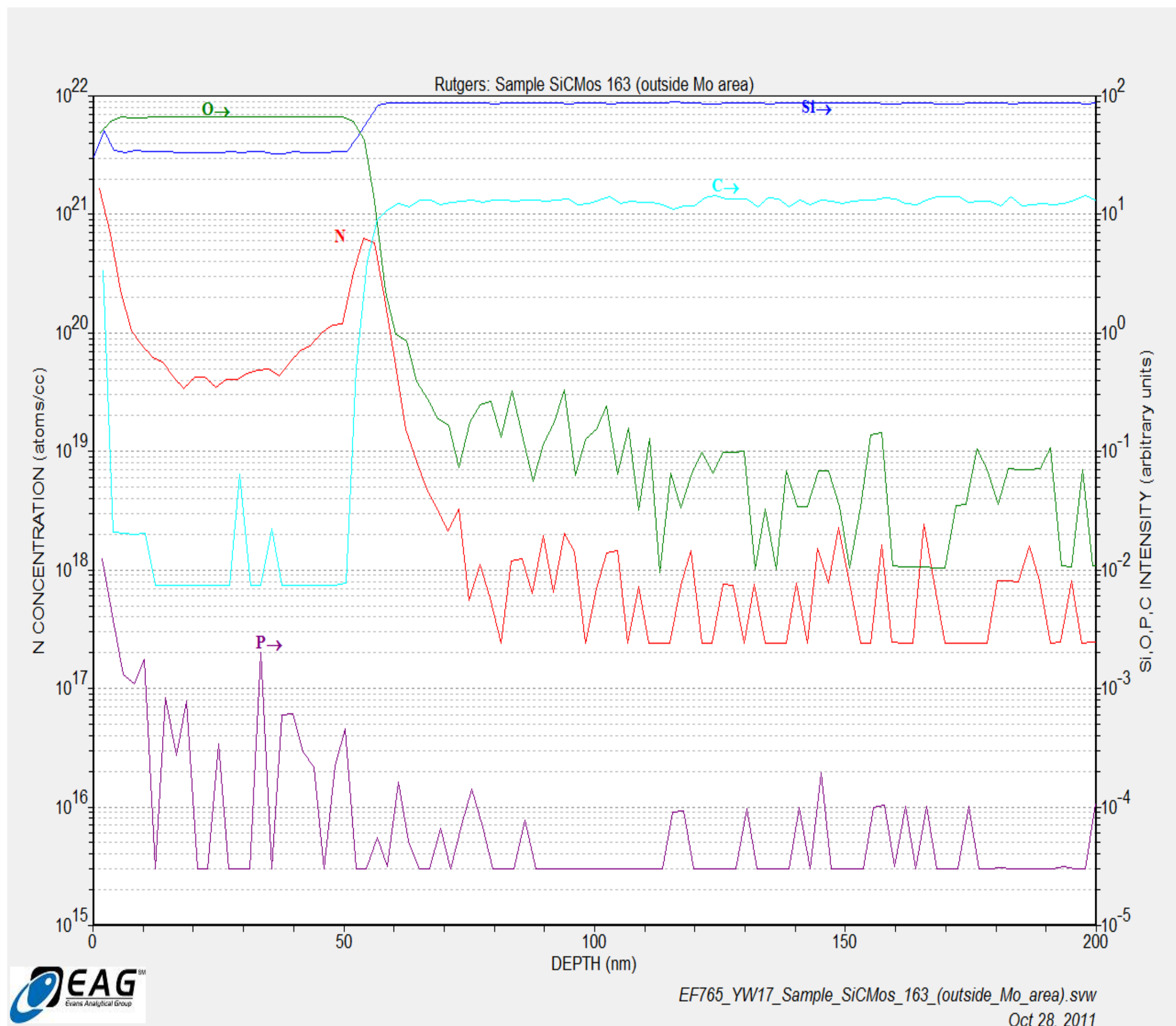


Figure 5.5(a): SIMS profile for 8 hr N2P passivation. Quantitative results (left ordinate) are valid only for N. As with NO, nitrogen is found only at the O-S interface. Recall that after annealing, phosphorous is distributed throughout the PSG gate layers.

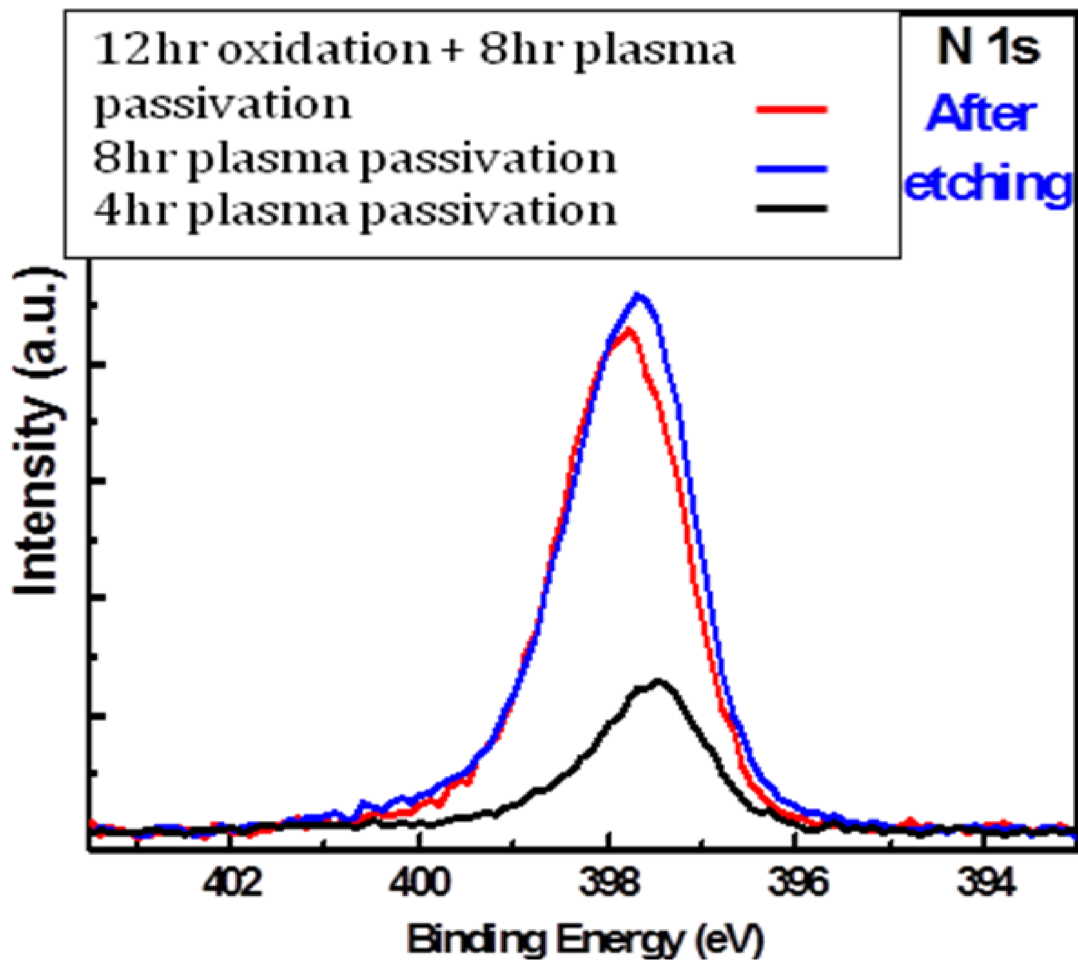


Figure 5.5(b): XPS data for 4hr and 8hr N2P-pasivations after oxide removal by buffered HF etching.

Table 5.6: Areal density of N at the interface for NO passivation and N2P passivation.

Passivation	Interfacial N concentration (cm^{-2})
Standard NO passivation	6e14
4hr N2 plasma passivation	6e14
8hr N2 plasma passivation	1.5e15

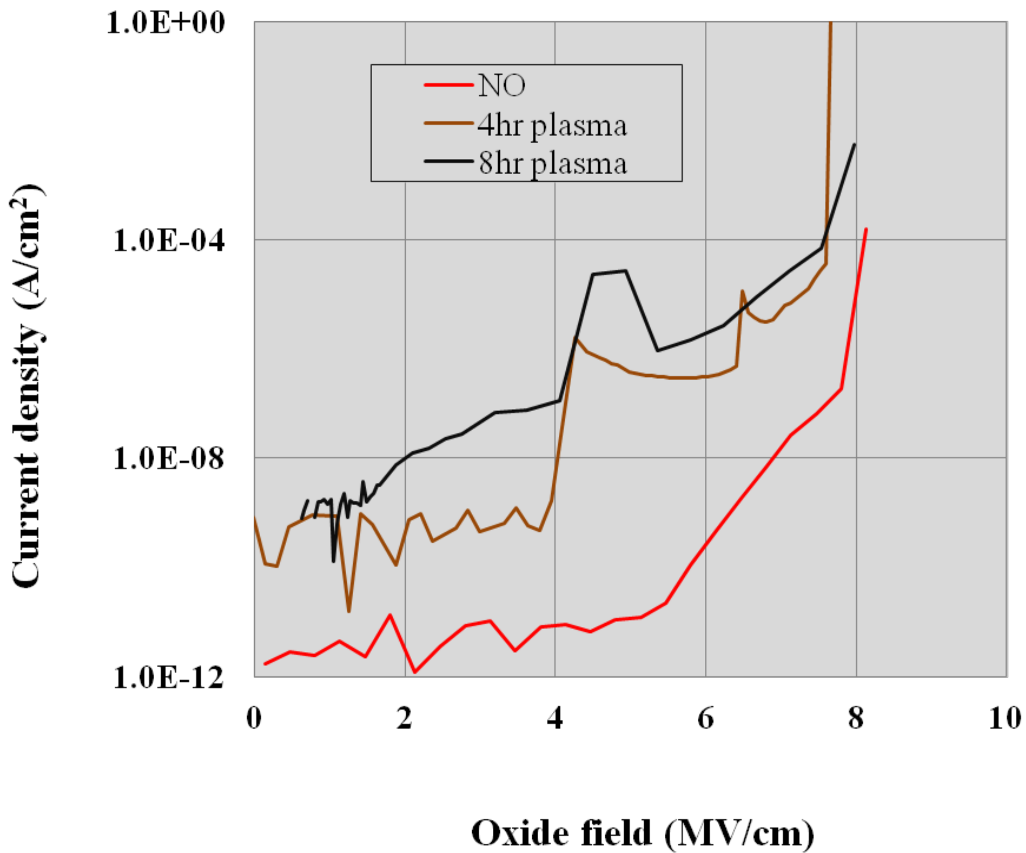


Figure 5.7: Breakdown characteristics of MOS-Cs after 8hr N2P-passivation. The red curve is for a standard NO device.

5.4 Low carbon MOSFET

Oxidation of SiC liberates a significant amount of carbon that contributes to the degradation of the inversion channel mobility [8,9,10]. Standard passivation processes that use NO and/or N_2O produce additional oxidation. We can call a MOSFET fabricated with thermal oxidation and NO passivation a "standard" MOSFET, and with this device, it is difficult to control interface traps due to excess carbon. In a new "low carbon" MOSFET fabrication process, carbon liberation is limited to the greatest extent possible. The thermal oxide is replaced by a deposited oxide and the N2P process is used for the passivation. Eight hours of plasma

Table 5.8: Comparison of processing steps for "low carbon" and standard MOSFETs.

	Processing step	Standard FET	Low carbon FET
1	30nm thermal SiO_2 prior to Mo deposition for S/D implant	Yes	Replace 1150C thermal SiO_2 w/ 650^oC TEOS
2	~ 150^oC O_2 plasma ashing for carbon cap removal after implant activation anneal	Yes	Yes
3	30nm thermal oxidation after ashing	Yes	Skip
4	Gate oxide growth - 75nm 1150^oC thermal SiO_2	Yes	Replace with 75nm 650^oC TEOS
5	Passivation - 2hr NO at 1175^oC	Yes	N_2 plasma (4hr, 1160^oC) + 2hr recovery (no plasma)

passivation grows only 1-2nm of thermal oxide (due to exposure to highly reactive atomic oxygen produced by decomposition of residual O_2 in the plasma furnace) compared to around 10nm during NO passivation. Table 5.8 compares the standard and low carbon MOSFET processes. Oxidation in step 1 is part of the nitrogen implantation process to form the MOSFET source and drain. Step 3 oxidation is performed make sure that there is no residual carbon left from the carbon cap layer (baked photoresist) used to protect the SiC surface during the implant activation anneal. This oxidation step is omitted for the low carbon MOSFET which is instead subjected to low temperature plasma ashing (~ 150C) for a longer time to remove residual carbon. In step 5, NO passivation for a standard FET is replaced by nitrogen plasma passivation.

References

[1] G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, R. K. Chanana, Robert A. Weller, S. T. Pantelides, Leonard C. Feldman, O. W. Holland, M. K. Das, and John W. Palmour, *IEEE Elec. Dev. Lett.* 22, 176 (2001).

[2] G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, M. Di Ventra, R.K. Chanana, S. T. Pantelides, Leonard C. Feldman, and R. A. Weller, *Appl. Phys. Lett.* 77, 3601 (2000).

[3] T. Kimoto, Y. Kanzaki, M. Noborio, K. Hiroaki, M. Hiroyuki, *Jap. J. Appl. Phys.* 44, 1213 (2005).

[4] W. J. Schaffer, G.H. Negley, K. G. Irvine, and J. W. Palmour, *MRS Proc.* 339, 595 (1994).

[5] E.H. Snow and B.E. Deal , *J Electro. Soc.* 113, 263 (1966).

[6] Y. K. Sharma, A. C. Ahyi, T. Issacs-Smith, X. Shen, S. T. Pantelides, X. Zhu, J. Rozen, L.C. Feldman, Y. Xu, E. Garfunkel, and J.R. Williams, *Mat. Sci. For.* 717 – 720, 743 (2011).

[7] Y. K. Sharma, A. C. Ahyi, T. Issacs-Smith, X. Shen, X. Zhu, L.C. Feldman, and J.R. Williams, *Solid-State Electron.* 68, 103 (2012).

[8] X. Zhu, A.C. Ahyi, M. Li, Z. Chen, J. Rozen, L. Feldman, and J. R. Williams, *Solid-State Electron.* 57,76 (2011).

[9] G.V. Soares, I. J. R. Baumvol, L. Hold, F. Kong, J. Han, S. Dimitrijev, C. Radtke, and F. C. Stedile, *Appl. Phys. Lett.* 91, 041906 (2007).

[10] S.T. Pantelides, R. Buczko, M. Di Ventra, S. Wang, G. Kim, S.J. Pennycook, G. Duscher, L.C. Feldman, K. Mcdonald, R. K. Chanana, R. A. Weller, J. R. Williams, G. Y. Chung, C. C. Tin, and T. Isaacs-Smith, *MRS Proc.* 640, H3.3 (2000).

[11] S. T. Pantelides, S. Wang, A. Franceschetti, R. Buczko, M. Di Ventra, S. N. Rashkeev, L. Tsetseris, M. H. Evans, I. G. Batyrev, L.C. Feldman, S. Dhar, K. Mcdonald, R. A. Weller, R. D. Schrimpf, J. R. Williams, G. Y. Chung, T. Isaacs-Smith, S. R. Wang, G. Duscher, L.M. Porter, *Mat. Sci. For.* 527 – 529, 935 (2006).

[12] X. Shen, M. P. Oxley, Y. Puzyrev, B. R. Tuttle, G. Duscher, and S. T. Pantelides, *J. Appl. Phys.* 108, 123705 (2010).

[13] A. F. Basile, S. Dhar, J. Rozen, X. Chen, J. R. Williams, L. C. Feldman, P. M. Mooney, *MRS Proc.*1246, B09-02 (2010).

[14] Jong-Pi Wey, Master thesis, Auburn University (1989).

[15] R. M. Lawless, *Development and characterization of a rmote plasma assited nitridation system*, B.S. thesis, Auburn University (2004)

[16] R.W. McCullough, *J. Vac. Sci. Technol. A* 14,152 (1996).

CHAPTER 6

Summary and future work

6.1 Summary

Metal oxide semiconductor field effect transistors (MOSFETs) in silicon carbide (SiC) have the potential of low specific on-resistance for high power operation due to inherent material qualities like high breakdown field, 2.5–3 MV/cm, wide bandgap, 3–3.2 eV, and large thermal conductivity 4–5 W/cm-K. The poor electrical quality of the interface (4H-SiC/SiO_2) currently prevents the utilization of SiC to its full potential. Although the standard NO passivation process has made the SiC power MOSFET a reality, there is still much room for improvement. For this research effort, we studied alternative ways to passivate traps/defects at the interface – (1) phosphorus (P) passivation and (2) nitrogen plasma (N2P) passivation.

Passivation with phosphorous is more effective in reducing interface traps compared to NO. The interface trap density (D_{it}) near conduction band edge (E_c – E = 0.2eV) is around $2x10^{-11}eV^{-1}cm^{-2}$. Mobility is 2.5 times higher, at around $80cm^2/V.s$ after P-passivation. Phosphorus transforms SiO_2 to phosphosilicate glass (PSG) which is a polar material, and polarization charge is source of flat band / threshold voltage instability in MOS devices. These devices can be stabilized significantly by using composite gate stacks fabricated with a thin PSG layer (< 10nm) capped with an unpassivated deposited oxide (~ 60nm). FETs fabricated in this manner show a mobility of around $70cm^2/V.s$. Hence, by reducing the thickness of the PSG layer, we can stabilize the device and at the same time keep the beneficial effect of phosphorus passivation of the interface.

In addition to the PSG process, additional interface trap reductions (compared to NO) can also be accomplished using nitrogen plasma passivation (N2P). Plasma passivation is an alternative way to introduce nitrogen at the interface compare to the NO process. Four N2P

shows “NO-like” D_{it} and mobility (for both thermal/deposited oxides devices). With an 8hr N2P process, we are able to achieve a trap density which is 2.5 times lower than compared to NO. The reason for higher tarp passivation with 8hr process is the increased areal density at the interface. The 4hr N2P and the standard NO processes give nitrogen coverage of $6x10^{14}$ cm^{-2} at the interface, while the 8hr N2P process gives $1.5x10^{15}$ cm^{-2}. This results in improved passivation of tarps at the interface. The interface trap density after eight hours of nitrogen plasma passivation at E_c - E = 0.2eV is $2x10^{11}cm^{-2}eV^{-1}$. If we scale the mobility with D_{it} then, with 8hr N2P process, we should able to achieve mobility of around $90cm^2$/V.s. This is comparable to the best result that we have obtained with phosphorous, but likely without the problem of polarization in the oxide layer.

Oxidation of SiC liberates a significant amount of carbon that may contribute to the degradation of the inversion channel mobility. The 8hr N2P process grows only 1-2nm of thermal oxide (due to exposure to highly reactive atomic oxygen produced by decomposition of residual O_2 in the plasma furnace) compared to around 10nm during NO passivation. We can combine 8hr N2P process with a deposited oxide to study the role of carbon in degrading the mobility of MOSFETs. This is called a “low carbon” MOSFET fabrication process in hich carbon liberation is limited to the greatest extent possible.

6.2 Future work

6.2.1 Phosphorus passivation

Thin PSG experiments results have shown that P-passivation has the potential to succeed as an effective passivation process, but there are still additional experiments that should be carried out.

1) Optimize the thickness of the PSG layer so that we can get higher mobility (> $70 cm^2/V.s$) without compromising D_{it}.
2) BTS experiments for higher electric fields (1.5MV/cm) and longer times (> 3hr) to check the reliability of the oxide after passivation.
3) Explore other elements from group V of the periodic table like - arsenic (As) and antimony (Sb). The chemistry for these elements is likely similar to the chemistry of phosphorous, but unlike phosphorous they may not react with SiO_2 to form glass.
4) Combine P passivation with H_2 passivation.
5) Study the effect of P passivation on the carbon face of 4H-SiC.

6.2.2 Nitrogen plasma passivation

Future experiments N2P passivation can include:

1) Eight hour nitrogen plasma passivation for MOSFET fabrication with thermal oxides. Lower D_{it} values already measured for MOS capacitors suggest a mobility of around $90 cm^2/V.s$.
2) Explore whether the 8hr N2P process is transferable to devices with deposited oxides?
3) Fabricate and characterize "low carbon" MOSFETs.
4) Further optimization of the plasma process – (a) to get higher nitrogen concentration and (b) to improve the yield.
5) For this study, the plasma passivation process was performed at 1160^oC. We need to do some experiments at lower temperature (~ 900^oC).
6) BTS experiments to check the oxide stability after plasma passivation.