

**The Effects of Thermal Aging on the Mechanical Behavior of Fine Pitch Electronics Packages**

by

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## Abstract

The direction of Electronics packaging industry is to design smaller packages with higher complexity while focusing on Sn-Ag-Cu as the alloy of choice for lead free electronics assembly. While performance capabilities have increased, thermo-mechanical reliability is a significant concern for harsh environment applications. The assemblies may be subjected to shock and vibration during day to day usage or while shipping and handling. The Inter-Metallic-Thickness which is formed during the reflow soldering process dictates the performance characteristics of the solder joint. In case of most electronics which are heavily subjected to thermal cycling due to frequent use and idleness causing fatigue, solder joint and interface failure of the component, where as portable electronics and critical equipments on Air craft's and land vehicles are subjected to repeated vibration and drop causing fatigue. The solder joint failure can be attributed to the structural dynamics of the product. It is necessary to understand the effect of time and temperature on the SAC solders joints.

This research uses a collection of fine pitch electronics packages to match a wide variety of packages available and test vehicles were built. These Test vehicles were subjected to Isothermal aging at 55°C over a period of 6, 12 and 24 months and then subjected to vibration and shock to understand the rate of reliability deterioration. The test was conducted in a step stress manner with the primary objective being the study of rate of deterioration of the two commonly used SAC alloys over time.

This dissertation deals with the challenges posed in the manufacturing of the fine pitch electronic parts due to bridging and solder paste printing process as well as the challenges posed by the solderability issue of ImSn boards at Continental Electronics, Huntsville, Alabama. It also deals with the issues caused by non standard test boards for the respective tests.

The effect of temperature over time on the mechanical behavior was compared between two SAC alloys 305 and 105 and with the recent thermal cycling data to identify and the differences in the behavior of the SAC alloys. The results shed light on the serious problems with SAC alloy reliability. This research shows clear reliability issues with using SAC alloy solder for harsh environment applicants. In addition it provides necessary data for the modeling of solder joint reliability to gain a deeper understanding of their behavior and approaches to address the issue.

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# Chapter 1

## Introduction

### 1.1 Origin and evolution of Solder

Solder is derived from old French, *soudure*, which means fasten together. Its use in English as a noun meaning “a fusible metallic alloy used for uniting less fusible metal surface or parts” dates to 1350. Lead was first obtained as a by-product of silver production, during cupellation of lead from ores. The softness and malleability of lead were later recognized. Lead was used as a setting agent to fix posts in ground and lock mortised stones. Mesopotamians [3000 B.C.] used lead to join copper pieces [1]. Egyptian King Tutankhamun’s tomb [1350 B.C.] consisted of the first manufactured solder, although debatable among scholars. Solders containing alloys of lead and tin were found from surviving artifacts and literary source of the Roman Imperial Period. Analysis of solder joints have revealed that both tin-rich and lead-rich alloys were used. Soldering was used to join the lead strips in stained glass of the five prophet’s window in Augsburg Cathedral that dates from late 11<sup>th</sup> century. Soldering was well established since Newcomen’s discovery of the effectiveness of the internally condensed steam engine in 1708, attributes to faulty repair of a blowhole in the cast bronze cylinder, a design that was not suppressed until Watt developed the separate condenser 70 years later [2]. In the 20<sup>th</sup> Century modern practices developed with the improvement of extraction techniques

which gave rise to exotic metal at affordable cost along with the alloy phase diagrams paving the path for diversity in alloy making today.

## 1.2 Soldering

It is a process of wetting the mating surfaces by a molten filler metal with or without the use of fluxing agent, forming a metallurgical bond between the filler metal and the two mating surfaces. In the process, the molten metal erodes the mating surfaces but the extent is usually microscopic ranging less than 100 $\mu$ m or 4000 $\mu$ in. In order to be recognized as Soldering the filler metal has to melt below 450°C or 840°F, else it would be considered Brazing [3].

- Soldering operation involves heating of the filler metals and mating surfaces above ambient temperature.
- Service temperature of the assembly must be lower than the melting temperature of the filler metal.
- It is not necessary to clean the mating surface as fluxes are capable of removing most oxides and organic films. Fluxes might have setbacks like leaving a residue behind and being corrosive.
- Joints tend to be strong if well filled, unless embrittling phase are produced.

## 1.3 Eutectic and Non Eutectic

The term *eutektos* comes from Greek, meaning 'Easily Melted'. A eutectic or eutectic mixture is a composition of two or more components in a ratio that has the lowest melting point, and when components simultaneously crystallize from molten



solution, this temperature is called the Eutectic Temperature. The proper ratios for a eutectic are obtained from the eutectic point on the phase diagram. They have sharp melting points, and phase transformation occurs abnormally. Some alloys don't have any eutectic point and alloys such as gold-silver. Non-Eutectic are alloys that when freezing, one component of the alloy crystallizes at one temperature and the other at a different temperature. These alloys exhibit a plastic melting range, the phase transformation is understood by drawing a line in the diagram, and each point on the line describes the composition at a given temperature [4-5].

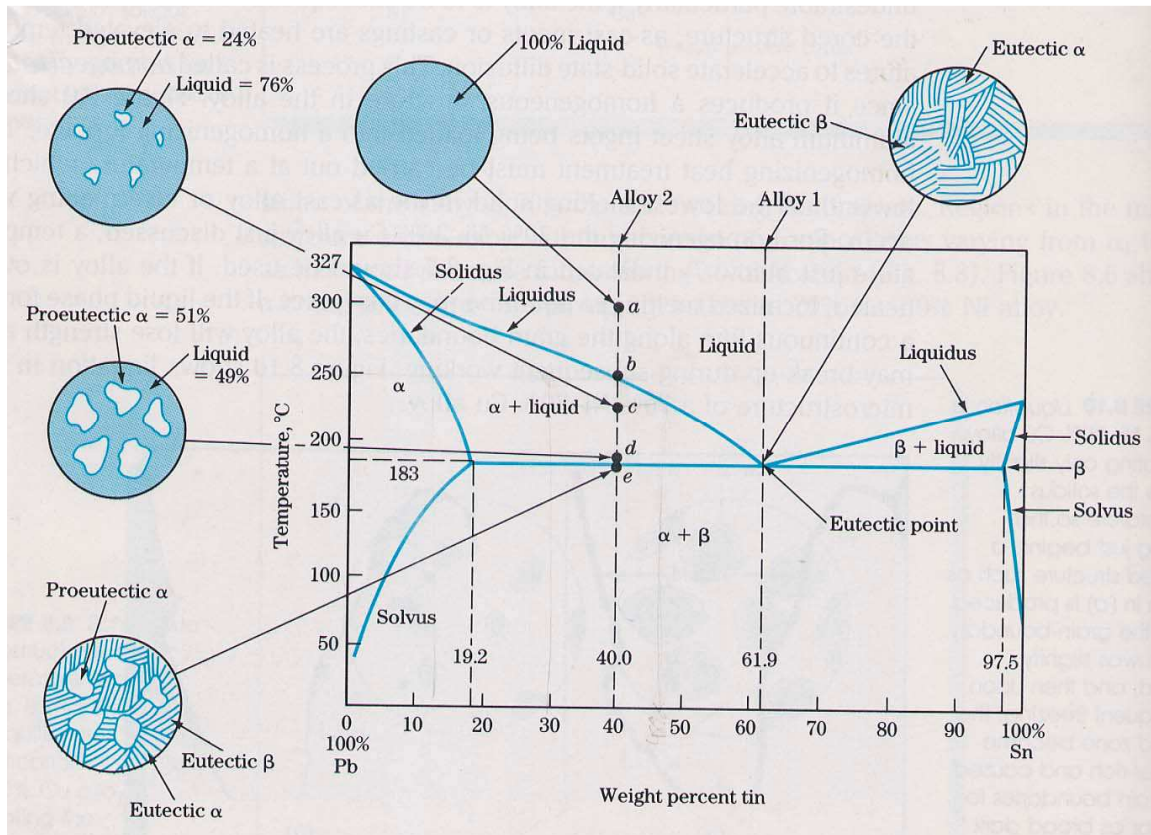


Figure 1.1 Eutectic phase diagram [6]

## 1.4 Solder Characteristics

For solder to be used in electronics packaging industry it has to meet requirements from thermal, electrical and mechanical conditions. Many of these characteristics are discussed herein.

### 1.4.1 Surface Energy and Tension

The concept is well represented in Figure 1.2, The atom at position A is inside a solid formation when compared with atom at position B which is at the surface. The atom at A has a balanced array of neighboring atom with respect to B which is lacking neighbor atoms at the surface and has unsaturated bonds. The potential Energy at B is higher than at A. The energy possessed by atoms at the surface constitutes surface energy. In liquids due to this energy it tends to draw up into spears. A sphere has the smallest surface –to– volume ratio of any shape is an indication of surface energy is larger than its volume energy. When a liquid spreads the volume remains constant and the change occurs only in surface energy, the surface is in a state of tension and is called surface tension [7-8].

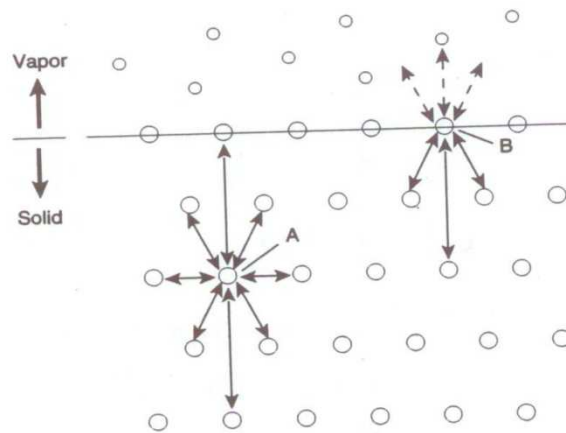


Figure 1.2 Simplified diagram of Surface Energy [2]

## 1.4.2 Wetting and Contact Angle

A liquid tend to spread over a solid surface until the three surface tensions are balanced [7-8].

- Between the liquid droplet and solid substrate.
- Between the liquid droplet and the atmosphere.
- Between the substrate and the atmosphere.

$$\gamma_{SL} = \gamma_{SV} - \gamma_{LV} \cos\theta \quad (\text{Eq1.1})$$

Where

$\gamma_{SL}$ - Surface tension between solid and liquid

$\gamma_{SV}$ - Surface tension between solid and vapor or atmosphere

$\gamma_{LV}$ - Surface tension between liquid and vapor or atmosphere

$\theta$  - Contact angle between the liquid and surface

Equation 1.1 is known as Wetting or Young's equation. The force which is responsible for the spread of the liquid over solid is the imbalance in surface tension due to  $\theta > 90^\circ$  which corresponds to the condition  $\gamma_{SV} > \gamma_{SL}$ . If  $90^\circ < \theta < 180^\circ$  liquid droplets will not spread. Thus the contact angle is the factor determining quality of wetting, with the decrease of  $\theta$  wetting increases.

$$\cos\theta = \frac{\gamma_{SV} - \gamma_{SL}}{\gamma_{SL}} \quad (\text{Eq1.2})$$

From Equation 1.2 wetting is increased by decreasing  $\theta$  as  $\cos\theta$  increases.  $\cos\theta$  is maximized by:

- Increasing  $\gamma_{SV}$

- Decreasing  $\gamma_{SL}$
- Decreasing  $\gamma_{VL}$

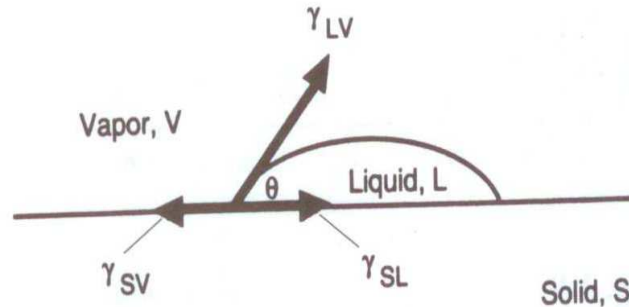


Figure 1.3 Surface Tension forces on a liquid [2]

### 1.4.3 Fluid flow

Contact angle enables the surface energy to be determined and the force that acts to fill the joint gap with liquid. The flow rate into the joint under this force is controlled by its viscosity [9].

- All surfaces are smooth and perfectly clean.
- Flow is laminar and not turbulent.

### 1.4.4 Strength

The purpose of joints is usually to form metallic bonds between components. The cohesive strength between parent material and the filler metal results from attractive force of the constituent atoms in them. Each atom tends to occupy a location where the net force is zero. When it is strained due to the application of external load, atoms move from equilibrium and an opposing stress is setup in the metallic crystal. This attractive force between the atoms that share the same electron cloud increases with the distance between

them to a maximum and decreases when failure occurs. A metallic cleavage would propagate across the crystallographic plane where the interatomic forces are the weakest.

### **1.4.5 Metallurgical Stability**

To have a stable joint the peak operating temperature of the assembly should not exceed 70% of the melting point of the filler material. Strength of all metals decrease as melting temperature is approached; the phases that are formed during solidification in a joint are unstable at elevated temperatures.

### **1.4.6 Tin Lead solder Metallurgical Stability**

Tu and Zeng [10] reviewed six aspects of reliability of Pb-free solders:

- (1) Interfacial reactions between Pb-free solder and thick metallization of bond-pad on the substrate-side,
- (2) Interfacial reactions between Pb-free solder and thin-film under bump metallization on the chip side,
- (3) The growth of a layered intermetallic compound by ripening in solid state aging of solder joints,
- (4) A long range interaction between chip-side and substrate-growth on Pb-free finish on Cu lead frame
- (5) Electro-migration in flip chip solder joints and finally
- (6) Sn whisker growth on Pb-free finish on Cu leadframe.

## 1.5 Solder for Electronics

In the world of mass production, electronics soldering is performed primarily in two methods, wave soldering and reflow soldering. Wave soldering is a process where electronics components are held in place with adhesives on the PCB and passed over a container of liquid solder where solder adheres and fills the through holes. It is typically used for all through-hole devices. Reflow soldering is a process where the pads are printed with a sticky mixture of powdered solder and flux. The designated electronic components are placed on the pads and the whole assembly is passed through a zone by zone temperature controlled oven. The flux activates to clean the pads, then the solder "Reflows" on, wets under controlled condition to provide soldering.

The solder joints between the parts and pads provide electrical, thermal and mechanical continuity in the assembly. The joints property determines the overall function of the assembly. The Sn-Pb solder composition is compatible with most substrate materials and devices. The effect of lead on tin is more pronounced than most other materials [11-16].

- Tin-Lead mixture (63Sn-37Pb) does not have a phase change; it melts at 183°C.
- Lead has an effect on the surface tension of the tin-lead mixture.
- Allotropic transformation prevented by lead on tin when it is cooled below 13°C which effects the structural integrity as the volume increases by 26%.
- Lead improves the diffusion of copper and tin in liquid state aiding in the intermetallic bonds.

Due to these factors the use of tin-lead solder is preferred and refined over a period of time in the field of electronics packaging. But in recent times concerns have been raised due to the adverse health effect lead has on humans and on the environment.

### **1.5.1 Need for Lead Free in Electronics**

Lately governments have become stricter regarding the handling of waste material. If a worker is not properly monitored and is exposed to elevated lead level, the lead could be carried on his clothing, leading to contamination in home which is potential problem. All types of wastes generated from a soldering operation; solder, wipes and packing containers have some recycling value, others have to be discarded as hazardous waste. During the process there are effluent wastes during cleaning, where solder balls and heavy metal salts are washed off. Governments are still pushing for removal of lead from products as some are being disposed in landfills, such as radios, televisions and other products [11-17].

- Legislation: WEEE Directive, Lead Tax Bill HR-2479.
- Liability Risk: Worker exposure, End product disposal.
- Manufacturing Waste: Surface mount, Hot air solder coat.
- Water Treatment: OA Process Water, General Process Water.

## **1.6 Lead-free solders**

Most solders originate from a binary alloy system. An additive is added to that composition to suppress or enlighten a certain quality, sometimes leading to the

quaternary element. The major need for additives are to lower melting point and increase reliability along with wettability [18].

### **1.6.1 Sn-Bi**

In this system there is significant solubility of Bi in Sn, up to 22% of Bi in Sn at the eutectic temperature of 139°C, but due to this, cracking might occur at slow cooling and precipitate in the Sn phase as the alloy cools. It has been a promising replacement for Sn-Pb. This solder has equivalent properties to that of 63Sn-37Pb and suitable for low temperature application. When the concentration of Bi is increased, the liquidus temperature decreases from 232°C, at pure tin to 130°C at 58% Bi [19-20]. This low melting point creates issues for electronics that operate at elevated (over 125°C) temperatures.

### **1.6.2 Sn-Ag**

In this system the liquidus temperature decreases from 232°C to 221°C at 3.5% Ag. There is negligible solid solubility of Ag in Sn, in the microstructure of the eutectic alloy features  $\beta$ -tin phase with dendritic globules and inter-dendritic regions with a eutectic dispersion of  $\text{Ag}_3\text{Sn}$  precipitates within  $\beta$ -tin matrix. It has poor wetting properties in reflow soldering applications which prevents it from wider use. With a small addition of Zn, it improves the solidification microstructure by introducing finer and uniform dispersion of  $\text{Ag}_3\text{Sn}$  [21].



### **1.6.3 Sn-Zn**

In this system with zinc at 9%, the eutectic composition has a melting point of 198°C, which is closer to the 183°C of Sn-Pb. It can even be reduced to 192°C with addition of Bi. Alternating rich phases of Zn and Sn can be found on the lamellar microstructure. The Sn-Zn composition is fairly reactive since both components react with copper to form intermetallic phases. Zn has high oxidation potential which leads to corrosion problems. It also reacts with the flux to form hard paste [22].

### **1.6.4 Sn-Cu**

In this system, at 0.7% Cu, a eutectic composition is reached at a temperature of 227°C. This is mostly preferred for wave soldering as its inexpensive. Sn-Cu has one of the least desirable mechanical properties. It is not suitable for air reflow as it results in rough and textured fillets. It is also prone to whisker growth [22].

### **1.6.5 Sn-In**

In this system, at 49% tin it is eutectic at a temperature of 120°C. Due to low melting point it is used in Surface mount application. The price of indium metal is higher than silver and not available in plenty, hence it not used as much. Sn-In is used where there is a problem of gold scavenging by tin rich solders [23-24].

### **1.6.6 Tin in lead-free solders**

Tin has an ability to wet and cover a range of metals. Its melting point is 231°C and it has allotropic transformation at 13°C. White tin has a body centered tetragonal

crystal structure and stable at room temperature. Gray tin, which has a diamond cubic crystal structure, is thermodynamically stable below 13°C. The transformation which takes place at 13°C from white tin to grey tin at 13°C is known as “Tin Pest” which results in an increase in volume by 26%, which may induce a cracking in the tin structure. Some elements have been reported to have a suppressing capability of the phase transformation. Tin poses a reliability risk in electronic circuitry as it is prone to tin whiskers which is a growth of fine wire shaped single crystals [25-29].

### **1.6.7 Tin-Silver-Copper Alloys**

In order to replace the lead based solders for over the years, many alloys have propped up but there is still no quick fix replacement suitable for all the application. Sn-Ag-Cu (SAC) based alloys derived from Sn-Ag and Sn-Cu based mixtures have been the most promising. There are many SAC alloys developed and used by major electronics manufacturers. Different parts of the globe have been fond of different composition and have been widely adopted. SAC396 (95.5Sn-3.9Ag-0.6Cu) is very popular with U.S. companies; EU has SAC387 (95.5Sn-3.8Ag-0.7Cu) as its prime solder. Japan has the widely accepted SAC305 (96.5Sn-3.0Ag-0.5Cu) as its choice [30-36].

## **1.7 SAC Alloys characteristics and Application**

SAC alloys tend to have an edge over other lead-free solders with mechanical and solderability properties provided they have lower melting point and tolerance for lead contamination. SAC has been used in soldering BGA packages for many years. In a

survey conducted by Soldertec, about 70% of the market for reflow lead-free solders is one or the other form of SAC alloys. Though SAC is sort after, it is not perfect [30-36].

- Excessive buildup of intermetallic formed at the interface between the solder joints and copper pad lead to reliability problems.
- Cost of lead free solders are high, Ag is roughly 150 times the cost of lead, Copper is twice the cost of lead. Though Ag and Cu are very less, a typical SAC solder is twice the cost of Sn-Pb.
- Higher melting point than Pb solders.

Soldertec's survey has SAC which consist 3.0-4.0% of Ag and 0.5-1.0% Cu which is near eutectic as the most popular. The melting point is 217°C, which is lower than the 96.5Sn–3.5Ag binary eutectic alloy at 221°C. In the SAC system, the addition of Cu both lowers the melting temperature and improves the wettability [30-36].

### **1.7.1 Challenges in switching to Lead-Free**

The need for Lead free solders has led to development of a relatively large number of solder alloys, some of them are binary, ternary and quaternary alloys. Over 70 alloys have been identified in the literature. Most of them rich in tin, silver are prominent as a constituent. Some concern for the manufacturers regarding the lead free solder is [37-40]:

- 1) Similar characteristics now and over time compared to tin-lead.
- 2) The selected elements will have no negative environmental impact nor or in the future.

- 3) Melting temperature must be as close as that of 63Sn-37Pb, preferably below 200°C.
- 4) Similar mechanical, thermal and electrical conductivity.
- 5) Easy to repair.
- 6) Low cost and compatible with existing process.
- 7) Future availability of base material.

### **1.7.2 Challenges in the process of Lead-Free**

In flip chip packages, the process and materials used are synchronized for Sn-Pb solder alloy which includes underfill and flux chemistry. The purpose of under fill is to reduce the shear load on the solder joints and inelastic strain in the solder which leads to better life of the solder joints. A new set of database is to be created for lead free let alone the different types of lead free as each has different melting points which are considerably higher than Sn-Pb. The potential of cracking in the low-K Inner layer dielectric caused by large stress loading in flip chip packages because of the mismatch in the CTE of Si die and substrate which needs better understanding.

To complicate matters the demand for fine pitch BGA packages have risen in recent times especially in mixed metallurgy with Sn-Pb and Pb free solder joints. In BGA assembly processes, the most commonly used solder alloy is SAC which has a melting point of 34-38°C higher than the Sn-Pb solder. With SAC solder balls puts the PCB on higher reflow temperature which could result in underfill to die interface delamination and pop corning effects are expected to rise [41-43].

### **1.7.3 Challenges in Reliability of Lead-Free**

One of the most important factors in a solder joint is the reliability of the joint. This concern has attracted a lot of research effort to develop mathematical models and test methods to accurately predict the life span and mode of failure in the joint. The stress on the solder joint is a crucial factor which is taken in to account on the prediction model of the components. Hua [44] has categorized the stresses in a package into three,

- 1) Mechanical Stress due to coefficient of thermal expansion difference between the package and material.
- 2) Chemical stress due to interface chemical reaction.
- 3) Current Stress from high current density.

Most models deal with only one of the stresses based on the assumption that dominant stress is at operation. This approach is valid for Sn-Pb packages, however for a Pb-free package, with the increase in melting point and/or current density, the solder joint failure can be caused by either or a combination of the stresses. Hence it is difficult to accurately predict the solder joint reliability without understanding the interaction of these stresses.

## **1.8 Transition**

Beginning with the ban of lead by the European Union, the need for the lead free soldering technique is taking place all over the world. Though it is crucial to make the transition from Sn-Pb to Pb-free, there are critical issues which have raised concerns and are yet to be addressed due to the incomplete infrastructure for the Pb free soldering

technology. The industry is in an interim stage highlighted by mixture of Pb-free solder with Pb-coated components and vice-versa. It is considered as a bridge for gap between Sn-Pb and Pb-free Soldering [49].

### **1.8.1 Interim Stage**

In the early transition phase, consumer electronics manufacturers converted their products to be lead-free quickly to comply with environmental regulations and avoid a marketing disadvantage. The interim stage exists due to the fact that Pb-free soldering is still evolving; the industry is still fine tuning the Pb-free alloys and suitable technical protocols for the soldering process. But some lead-free components/packages were not available because components manufacturers were slow in responding to the lead-free transition or there was insufficient demand initially. Thus tin-lead components were assembled with lead-free solder paste. This would be termed a forward compatibility situation. To address the problem of component suppliers and OEMs to avoid having production lines dedicated for Pb-free components and Pb components, in the late transition phase, many component manufacturers had migrated to lead-free production. Since the demand for tin-lead components was low, component manufacturers did not want to carry both Sn-Pb and lead-free production lines due to the cost concerns. Therefore, some components, such as memory modules, are no longer being made available in Sn-Pb finish. The most important of all is the exemption of telecommunications, avionics and high-end servers which are designed to meet long term field reliability or to survive harsh environments from the requirement for Pb-free solder

alloys [45, 46]. The manufactures of these products want to continue to be built with conventional Sn-Pb solder paste because the reliability of SAC or lead-free solder joints for these high reliability applications is still unknown. This scenario, soldering of lead-free components with Sn-Pb paste, is known as the backward compatibility situation [47, 50, and 51].

### 1.8.2 Mixed formulation challenges

Reliability and material concerns arise when Sn-Pb and Pb-free materials and process are crossed. The main concern is there is a temperature difference of about 34°C between SAC's eutectic temperature of 217°C and that of Sn-Pb is 183°C [49]. Mixed formulation can be achieved by two ways,

- 1) Forward Compatibility,
- 2) Backward Compatibility.

“Forward Compatibility” is the process where Pb-free paste and parts with Sn-Pb surface finish parts and solder balls are fused together [49, 53, and 54]. Backward compatibility is the process which involves Sn-Pb paste and parts with Pb-free surface finish parts and solder balls are assembled together [52].

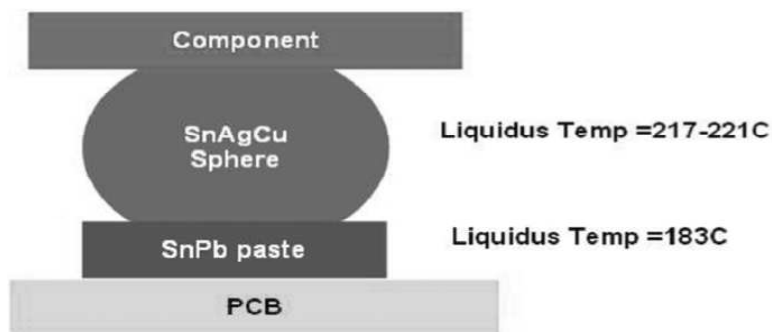


Figure 1.2 Schematic of BGA/CSP Backward Compatibility [47]

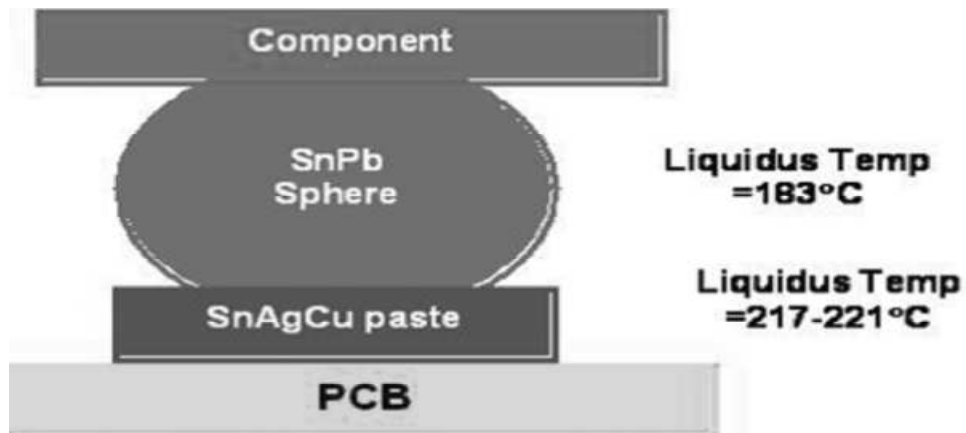


Figure 1.3 Schematic of BGA/CSP Forward Compatibility [47]

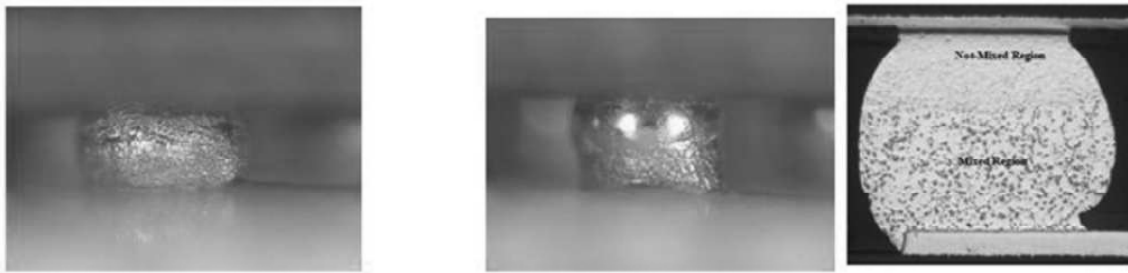


Figure 1.4 Comparison of different reflow profiles in backward compatibility (a) Using a SnAgCu reflow profile; (b) using a SnPb reflow profile [48]

### 1.8.3 Mixed formulation joints

The secondary alloying process takes place when SAC and Pb are merged in the reflow soldering which gives rise to different microstructures,

- 1) Fully mixed joint
- 2) Partially mixed joint

The homogeneity of a mixture's structure is based on Pb diffusion and is influenced by Pb concentration, peak reflow temperature, time at peak, soldering environment and the solder composition [55].



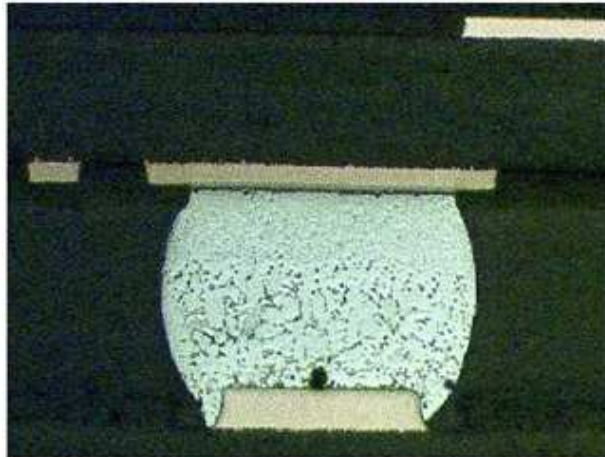


Figure 1.5 Partially Mixed Solder Joint [48]

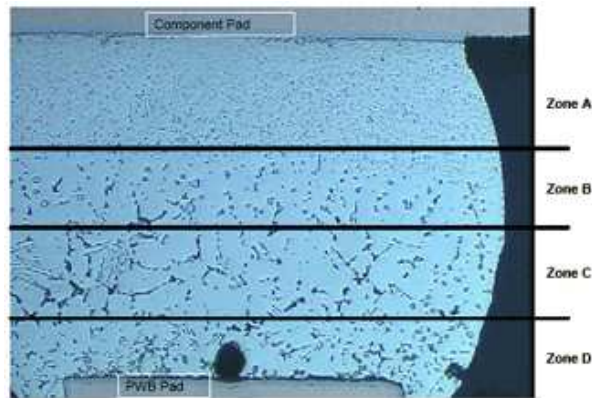


Figure 1.6 Partially Mixed Solder by Zone classification [48]

Zone	Microstructure Observed
A	Tin Matrix, Fine Blocky & platelet Intermetallic phase
B	Tin Matrix, Large Blocky & platelet Intermetallic phase
C	Tin Dendrite Matrix, Interdendritic Phases, Fine Blocky & platelet Intermetallic phase
D	Tin Dendrite Matrix, Interdendritic Phases, & platelet Intermetallic phase, Solder joint crack

Table 1.1 BGA Solder Joint Zone Microstructure

In the above mixed formulation solder joint, Zone A consist of the original SAC alloy. Since it is furthest from the Sn-Pb paste, under SEM EDX scanning it is found to have fine blocky intermetallic phases composed either of tin/copper or tin/silver. The intermetallic phases were identified as  $\text{Cu}_6\text{Sn}_5$ ,  $\text{Ag}_3\text{Sn}$  and  $\text{Ni}_3\text{Sn}_4$ . Zone B consist of tin matrix, the fine intermetallics were replaced with large blocky intermetallic phases composed of  $\text{Cu}_6\text{Sn}_5$  and  $\text{Ag}_3\text{Sn}$  but no  $\text{Ni}_3\text{Sn}_4$ . Zone C has significant microstructural changes; tin matrix is replaced with dendritic solidification. Large blocky intermetallic phases are composed of  $\text{Cu}_6\text{Sn}_5$  and  $\text{Ag}_3\text{Sn}$ . A fine platelet intermetallic phase of  $\text{Ag}_3\text{Sn}$  along with 96.5Sn/3.5Ag eutectic phase is found in the interdendritic regions. In the interdendritic region, Pb deposits are also found. Zone D consists of tin matrix, sporadic tin dendrite occurrence, platelet and blocky intermetallics and regions of Pb.

Some studies show enhanced mechanical and reliabilities in solder joints formed by mixing SAC and Pb, whereas other studies report deteriorate performance. Two major topics on debate are:

- 1) What are the minimum peak temperature and time above liquidus (TAL) for backward assembly?
- 2) How to achieve the desired mixed alloy homogeneity and reliability?

High temperatures are usually used in reflowing Pb-free solders to obtain a homogenous microstructure in the joint which could result in reliability concerns of the package. Hua, et al. [53,56] found that reliability and process risks are high for backward solder joints when peak temperature of the reflow profile is less than  $217^\circ\text{C}$  as inhomogeneous microstructure resulting from the partially collapsed SAC solder ball. A

peak temperature of 235°C is needed to obtain acceptable reliability in solder joints of backward compatibility, Theuss, et al [57]. But it was reported that backward solder joints with fully mixed microstructure can be achieved with a peak reflow temperature of about 210C with 20 to 30 seconds for certain paste to ball weight ratio, Nandagopal [45, 58].

### 1.9 Mechanical Properties of solder joint

The purpose of solder alloy joint is to provide electrical, mechanical and thermal integrity in electronics assembly. Various failure mechanisms are presented in the Figure 1.7. Most of the failures are caused by fatigue or fracture which causes distortion in the functionality before visible breaking. These failures are associated with mechanical behavior of solder alloys under certain thermal environments and are called thermo-mechanical failure [59].

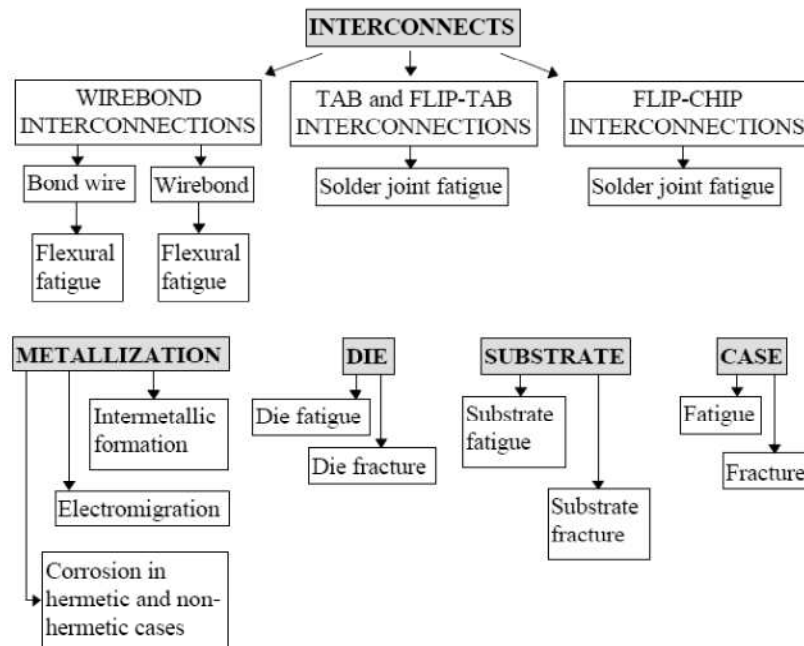


Figure 1.7 Failure Mechanisms in Microelectronic Packaging [59]

## 1.9.1 Coefficient of Thermal Expansion

When an electronic component is powered to function, it generates heat. Due to this heat, there will be thermal expansion of the components. When there is a mismatch between the coefficient of thermal (CTE) expansion of the component and the material used to construct the assembly, stresses are induced. If the CTE of all the material in the assembly are the same they expand and contract together provided a good heat transfer in the assembly, there will be no thermal stress induced. But almost all of the packages have a mismatch due to the wide array of materials used in present day electronic packaging. When the component is power off it cools and again expands when it is switched on, this result in cyclic stresses in the joints. It is important to know the spatial and temporal distribution of the cyclic stress, which usually takes the form of solder joint shearing. The range of temperature variation, the component configuration and solder joint distribution, the solder joint geometry, solder alloy elastic-plastic and creep constitutive relationship.

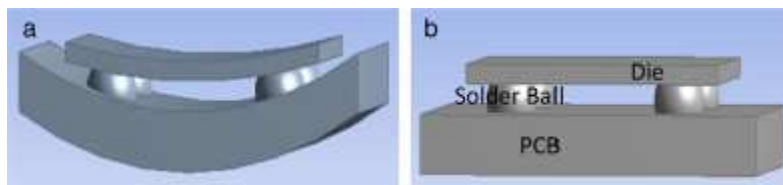


Figure 1.8 a) Cyclic Stress Induced by CTE Mismatch after expansion, b) before expansion

## 1.9.2 Tensile Properties

The solder joints in an electronic assembly are one which is usually subjected to tensile loading when the assembly is subjected to flexing. In order to determine the limit to which a joint can be subjected to tensile deformation before it can sustain a failure, the

tensile properties of the alloy such as yield strength, ultimate tensile strength and elastic module are important.

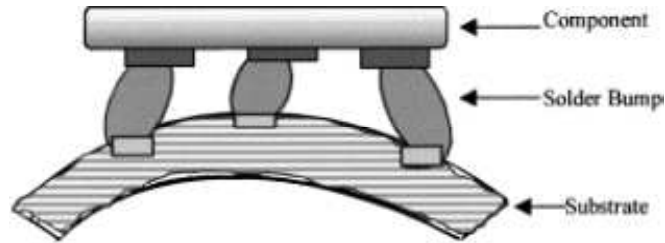


Figure 1.9 Tensile loading [36]

Materials strength is defined as the load it could undergo without deformation, which is determined by tensile test results in the form of a stress-strain graph. Engineering stress-strain graphs are widely used over true stress-strain graph as engineering stress-strain graph provides the means for obtaining data about a material's tensile strength without regard for the material's physical size or shape [60].

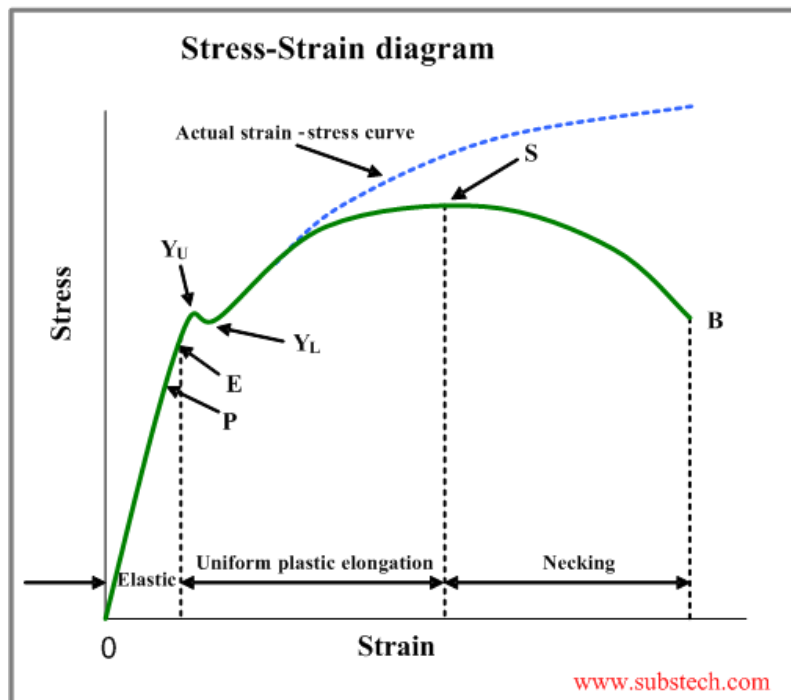


Figure 1.10 Stress-Strain relationships

In the above graph, the blue line represents the true stress- strain curve. Strain is the ratio of increase in dimension to the original dimension. Tensile stress is the ratio of the tensile load  $F$  applied to the specimen to its original cross-sectional area  $S_0$ , Eq. 1.1. The initial straight line (OP) of the curve characterizes proportional relationship between the stress and strain. The stress value at the point P is called the limit of proportionality; this behavior conforms to the Hook’s Law.  $E$  is a constant, known as Young’s Modulus or Modulus of Elasticity. The line OE in the Stress-Strain curve indicates the range of elastic deformation, upon removal of the load at any point of this part of the curve results in return of the specimen length to its original value. The elastic behavior is characterized by the elasticity limit which is the stress value at the point E. A point where the stress causes sudden deformation without any increase in the force is called yield limit. The highest stress (point YU), occurring before the sudden deformation is called upper yield limit. The lower stress value, causing the sudden deformation (point YL) is called lower yield limit. As the load increase, the specimen continues to undergo plastic deformation and at a certain stress value its cross-section decreases due to “necking”. At the point S in the Stress-Strain Diagram, the stress reaches the maximum value, which is called ultimate tensile strength.

$$\sigma = \frac{F}{S_0} \quad \text{Eq.1.1}$$

### 1.9.3 Shear Properties

Due to mismatch in the coefficient of thermal expansion, solder joints are subjected to shear stress in an electronic assembly when they are powered on and off. The

silicone die and substrate are subjected to shear stress generated by mismatch in CTE are shown in Figure. Now the shear properties of the solder alloy such as the shear modulus and shear strength become important [61].

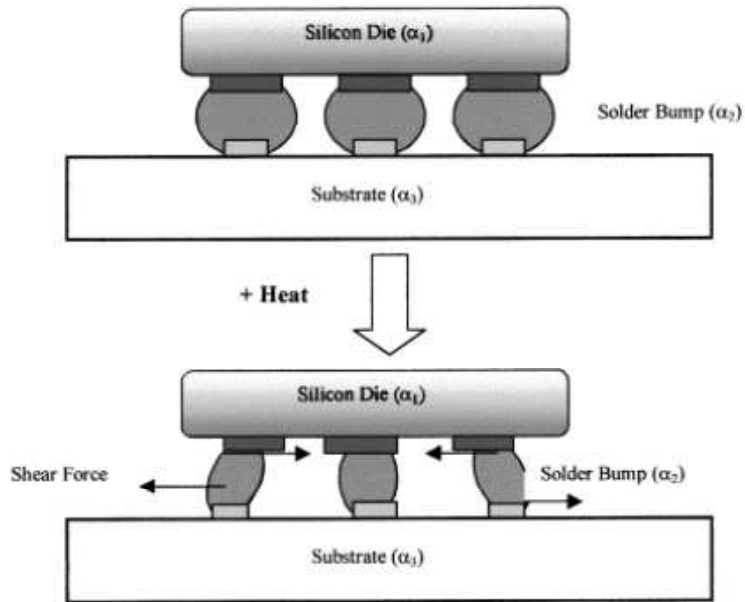


Figure 1.11 Solder Joints Subjected to Shear Strain due to CTE Mismatch [36]

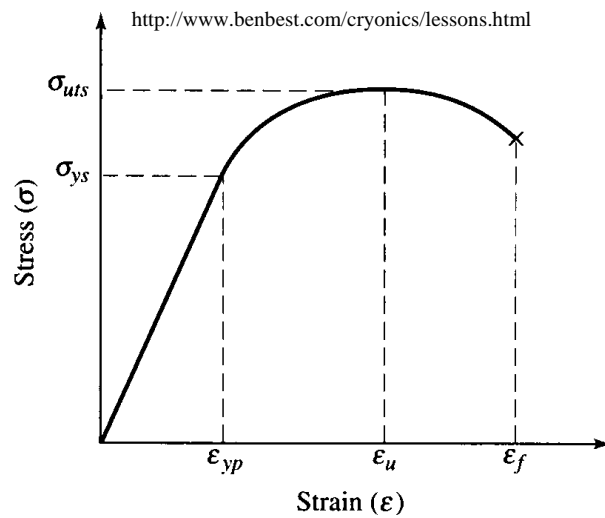


Figure 1.12 Solder state under shear load

When a material is subjected to shear load, it behaves in a linear-elastic manner and exhibit a proportional limit  $\sigma_{ys}$ . Until ultimate shear stress  $\sigma_{uts}$ , strain hardening will take place. The shear strength drops when the material fractures. The point at which material fractures is called fracture strength. Due to CTE mismatches and thermal differences caused by either power switching or the environment, electronic assemblies often undergo combined shear deformation, warpage, and distortion. Under such circumstances, solder joints are usually subjected to a combination of shear and tensile loading.

#### **1.9.4 Creep Properties**

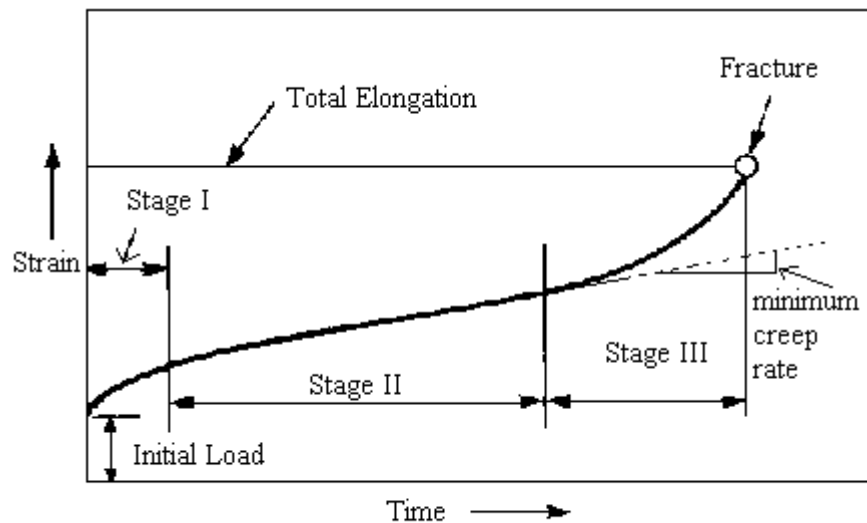
When electronic assemblies are subjected to long periods of constant high temperature, the solder joints are subjected to creep. This type of deformation is one of the major types of failure modes of solder joints for electronic packaging modules [62]. When a material is subjected to a constant load over a period of time at a constant temperature, deformation takes place; this type of permanent deformation which is time-dependent is called creep. In other words creep is a measure of time needed for a material to fail under constant load and temperature [61].

From a creep test, strain is measured against time and for the creep curve we can see that the failure takes place in three stages.

- Stage 1: Primary creep is a period of primary transient creep, in this period the resistance to creep increases until stage2 due to strain hardening which reduces deformation.



- Stage 2: It is known as steady state creep; in this period it is found that the rate of creep is roughly constant as strain hardening and recovery softening reaches a dynamic balance. At higher temperature, strain hardening is associated with subgrain formation caused by the rearrangement of dislocations. Recovery softening is related to thermally activated cross-slip and edge dislocation climb [60].
- Stage 3: In the tertiary creep stage, necking takes place which results in the reduction of the cross sectional area. This accelerated creep may be related to weakening metallurgical instabilities such as intercrystalline fracture and corrosion [60].



<http://www.materialsengineer.com/CA-Creep-Stress-Rupture.htm>

Figure 1.13 Different stages of creeps

### 1.9.5 Fatigue

Fatigue is the failure resulting from the application of cyclic stress. It is often considered as one of the most critical failure category. Solder joint fatigue failure is

attributed primarily to stress brought about by temperature swings and mismatch between the coefficients of thermal expansion of materials. Before the actual fatigue fracture, solder joints undergo cyclic deformation from the cyclic stresses as the temperature alternates between low and high value. This usually takes place at stress levels lower than the material's yield stress. In general fatigue is huge factor responsible for failure of engineering materials. This type of failure is usually caused by localized stress concentrations. In regions where localized stress becomes much greater than the average stress and cycled, micro-cracks will initiate and lead to stress concentrations at crack tips or boundaries. Higher stress leads to crack propagation into the material; this crack causes reduction in the cross-sectional area of the material. At a point it won't be able to withstand the load exerted and fracture occurs, this fracture is called Fatigue fracture. Most material, when subjected to load, will deform. When the load is reversed the material regains the original form to some extent. Hence there is relatively little plastic deformation which is cumulative and leads to unexpected failure. Ductile materials often behave like brittle materials when subjected to fatigue [60].

Fatigue crack growth takes place in three stages. These include: initiation and transient crack growth; steady state crack growth; and crack interaction and saturation [3<sup>rd</sup> stage crack growth].

- Stage 1: Crack initiation and transient growth

Cracks are formed in the regions where the stress is concentrated, indents, interior corners, dislocation slopes and micro-cracks initiate.

- Stage 2: Steady state crack growth

Along the crystal planes which have higher shear stress, cracks propagate which has flat surface, and cracks propagate perpendicular to the applied stress, they grow by repetitive blunting and sharpening at the tip of the crack featuring rough surface.

- Stage 3: Interaction and Saturation

Cracks grow to attain a point where one crack crossed the other causing wider cracks to propagate rapidly to ultimate failure.

Summary based on Manufacturability and Reliability manufactures are interested is given in the below table.

<b>Manufacturability</b>	<b>Reliability</b>
Melting/liquidus temperature	Electrical conductivity
Wettability (of copper)	Thermal conductivity
Cost	Coefficient of thermal expansion
Environmental friendliness	Shear properties
Availability and number of suppliers	Tensile properties
Manufacturability using current processes	Creep properties
Ability to be made in balls	Fatigue properties
Copper pick-up rate	Corrosion resistance
Recyclability	Oxidation resistance
Ability to be made into paste	Intermetallic compound formation

Table 1.2 Performance Characteristics of solder alloys

## 1.10 Objectives of the Study

The object of the study is to compare the effect of duration of isothermal aging on the mechanical reliability of Fine-Pitch electronic Packages between Lead-free and Tin-Lead paste. Following Steps were taken to achieve the objective:

- Developed assembly procedure to build TV-7 Test boards with fine pitch components.
- Aged test boards at Isothermal temperature of 55C over a period of 6, 12, 24 months.
- Overcame testing difficulty and developed test method to conduct vibration testing along with vibration profile.
- Setup drop test instruments and Came up with a reasonable test profile to conduct drop test.
- Compared the reliability different packages built using SAC and Sn-Pb paste.

## **1.11 Overview of the Dissertation**

The dissertation follows the following pattern:

- Chapter 1: Introduction
- Chapter 2: Literature survey
- Chapter 3: Selection of Test Vehicle, Parts and process
- Chapter 4: Manufacturing challenges and solutions
- Chapter 5: Vibration Challenges, approaches and solutions
- Chapter 6: Shock Challenges
- Chapter 7: Conclusion

## **Chapter 2**

### **Literature Review**

#### **2.1 Introduction**

Tin-Lead solder has been the champion of electronics packaging industry for many decades; 63Sn-37Pb is one of the most extensively researched solder materials. In recent past, due to many reasons, the industry has been forced to move away from solder containing lead. Research on Lead-Free solders has grown exponentially in both industries and academic fields in an effort to develop a substitute for Tin-Lead and create a database of the material behavior. Though some reports on lead free solders already exist there remains a variation.

The variations observed are due to many causes. One issue is the fact that properties are primarily tested on dog bone test sample or bulk solder specimen, which are greatly different from solder joint formed by a BGA. A uniform microstructure has to be archived to start with in order to produce repeatable results. All the test samples are to be subjected to similar test conditions in order to compare with each other and the method of data collection has to be consistent.

From the bulk of the past literature, it is noted that isothermal aging for SAC alloys is limited to both temperature and the period of aging. Aging of solder materials affects both mechanical properties and the microstructure. In an electronic device, the solder joint undergoes aging and thermal cycling as the device heats up and cools down frequently. The study of solder material undergoing isothermal aging for a longer period will help reduce the discrepancies in the current database and help understand the change

in microstructure and mechanical behavior of the solder alloys at various intervals of time. Due to a variety of lead-free solder joints in real world electronic packages and package variables introduced due to die size, package size, ball count, pitch, mold compound and substrate material, it is difficult to obtain mechanical from dog bone samples.

Accelerated testing is a method of testing solder and solder joints for reliability. One of the most common failures is thermo-mechanical solder fatigue failure, which is important for those applications whose service lifetime is expected to be a few year. Most common temperature range adopted for cycling varies by the field of application.

<b>Application</b>	<b>Operating Temperature</b>
Consumer	0°C to + 70°C
Industry	-40°C to 85°C
Automotive	-40°C to +125°C
Military	-55°C to +125°C

Table 2.1 Typical Thermal Operating Environments [63]

Most solder alloys have high homologous temperature even in room temperature, unlike eutectic tin-lead, the microstructure and mechanical behavior of SAC series alloys degrade over time at room temperature. The degradation is especially more rapidly during elevated temperature.

Electronic devices are subjected to long periods of constant elevated temperatures; the solder joints provide not only electrical connections but also mechanical support on the printed circuit board (PCB). The solder joints between the

package and the PCB experience the highest susceptibility to failure under harsh environmental loading conditions and upon failure the device is not useable. The CTE mismatches between the PCB and the IC components generate large cyclic deformations, which in turn produce complex stress/strain conditions and eventually lead to solder joint failure. Due to the high homologous temperatures solder joints experience during operation, solder alloys usually exhibit complicated creep-plasticity interactions and significant temperature-strain rate dependent material characteristics. The microstructure and mechanical behavior of solder alloys can change significantly over time during long term isothermal aging [64]. Even though some researches begin to study the isothermal aging on solder joints, more accelerated tests and field data are necessary before drawing conclusions about the long-term reliability of lead-free solder material and the trend of effects of thermal aging on different package designs.

## **2.2 Effect of Aging on Solder**

Solder material undergoes different types of Aging, the solder material is usually obtained in the form of bulk solder, solder paste and solder balls. The manufactures store the components for a period. During manufacturing assembly, the solder alloys are exposed to elevated temperature, which results in aging of the second level solder joints [64]. The mechanical properties of the dog bone solder bars are different from solder joints including the aging effects. It was found that at room temperature there are effects of aging by Lampe [65]. Up to 20% of the shear strength and hardness is lost after 30 days of storage at room temperature. In 1956, Medvedev [66] observed 30% loss of tensile strength for bulk Sn-Pb stored at room temperature for 450 days at the same time

there was a loss of 23% loss of tensile strength for solder joints stored at room temperature for 435 days. Hence studies should be performed which match the specific operating conditions of the actual solder joints. The aging effect on specific operating condition and solder joint is different to test. Lee et al. also observed that in 3 days room temperature aging after reflow, shearing stress of solder joints decreased by up to 10 % [67,68],

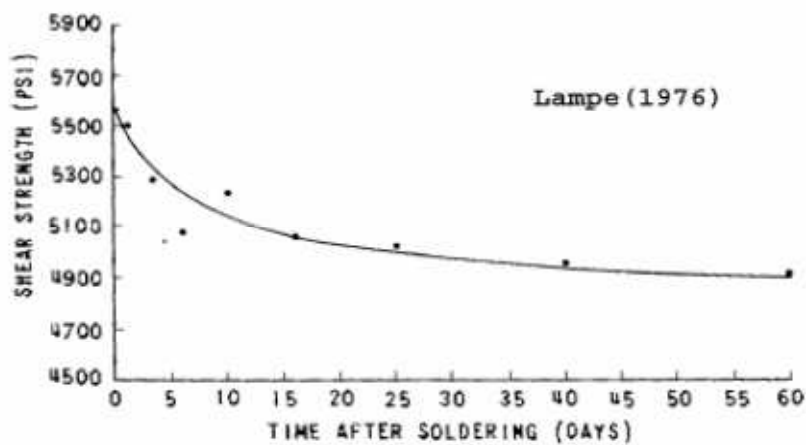


Figure: 2.1 Effect of Aging at Room temperature for Sn-Pb solder [65]

Xiao studied stress-strain curve of SAC396 after different period of aging at room temperature and showed a loss of ultimate tensile strength up to 25 % over days [69, 70]. At elevated temperature of 180, it was observed that there was quick softening of the material during the first 24 hours followed by a gradual hardening with time.

### 2.2.1 Effect of Thermal Aging on Solder

The solder behavior is influenced by external factors like applied strain rate, temperature and mechanical loads over a duration of time [71-73]. Some physical influence like size and cooling methods can have a significant effect as well. For SAC



alloys it has been demonstrated before, that time and temperature are some of the most critical factors which influence the solder performance as time progresses [65, 74, 75, 76, 77-80]. The aged specimens were also found to creep much faster than un-aged ones by a factor of up to 20 times for both SAC305 and SAC405 solder alloys [81]. At room temperature, Sn3.9Ag0.6Cu alloy softens with time but at 180°C it reaches its minimum flow strength after a day of aging [76]. It starts to harden as it is aged more, which is thought to be caused by the dispersion of Ag<sub>3</sub>Sn particles in to Sn crystals which were free of any intermetallic precipitates. SAC432, SAC396 and SAC387 are few alloys which exhibit a reduction in their flow strength with increasing test temperatures after aged at 125°C for 24 hours, and their degree of strength is highly dependent on their composition [77].

Studies [82, 83-85] have been performed to understand the degradation of BGA ball shear strength with elevated temperature aging at 125°C or 150°C. It has been documented that microstructure coarsening and intermetallic layer growth take place during the aging period. Chiu found significant reductions in drop reliability when aged at elevated temperature [82], the formation of voids and coalesce were the dominant mechanism for solder joint strength and board level reliability degradation. Ma, et al. [78] observed that the evolution and saturation of Young's modulus, yield strength, and ultimate strength of a series of SAC alloys under various aging conditions. He developed a linear-exponential model to describe the material property evolution. Aging effects on creep resistance in terms of secondary creep strain rate were also reported by him. Xiao, et al. [75] reported that SAC396 has much lower absolute creep rates compared with

eutectic Sn-Pb and tied the increase in creep resistance to the finely dispersed intermetallic compound (IMC) precipitates in the Sn matrix. Aging effects on primary creep were found to be more dramatic than on secondary creep [80].

Miyazawa and Ariga [86-88] observed significant hardness losses and microstructural coarsening for Sn-Pb, Sn-Ag, and Sn-Zn eutectic solders stored at 25°C for 1000 hours, whereas Chilton [89] observed a 10-15% decrease in the fatigue life of single SMD joints after room temperature aging.

### **2.2.2 Effect of Thermal Aging on Microstructure of Solder**

The formation of inter-metallic layer is beneficial, since an inadequate inter-metallic thickness may indicate insufficient bond formation between the component lead and the solder, and the solder and the board pad. An either very thin or excessively thick inter-metallic layer connotes greater solder attachment failure potential. A desired inter-metallic thickness is 1 to 5 microns. Over time, the inter-metallic layer may grow. Thermal cycling should show accelerated aging growth of the inter-metallic thickness. Too great an inter-metallic thickness is detrimental to joint reliability since the joint may become more brittle.

High strain rate brittle fracture can be encountered in soldering with Pb-free solder to all electronic substrates including OSP Cu, ENIG, matte Ni and sputtered Au/Ni. The interfacial IMC formed is determined by the phase equilibria of the high Sn solder and the substrate, In soldering Cu with a SAC alloy,  $\text{Cu}_6\text{Sn}_5$  is the equilibrium phase at the Sn rich solder interface while  $\text{Cu}_3\text{Sn}$  is in equilibrium with the substrate. The

quantity of IMC formed is a function of soldering time and temperature and subsequent aging conditions. The degree to which a particular soldered interface is susceptible to brittle failure depends on the composition of the IMC.  $\text{Cu}_3\text{Sn}$  is the more brittle of the two binary CuSn IMC's. The thickness of the IMC and the presence of defects as Kirkendall voids, incipient cracks or residual stress between IMC layers. Drop/shock performance can be improved by controlling the initial IMC formation, its subsequent development through device life and the IMC defects.

The effect of thermal aging is widely studied due to the dramatic changes in the microstructure and mechanical properties that result. Recent research has revealed that the addition of transition metals to Sn-Ag-Cu alloys provided a marked improvement in microstructural modification and mechanical properties and has attracted considerable attention. Aging softening has also been observed for solder subjected to elevated temperature aging. Pang et al. [98] measured microstructure changes, intermetallic layer growth, and shear strength degradation in SAC single ball joints aging at elevated temperature. Zhang looked into the effects of solder ball metallurgy and the intermetallic compound thickness at the solder-copper interface [93]. The effect of the pad surface finish has also been researched; HASL pad finish thermal reliability performance was superior over immersion nickel and palladium based pad finishes for BGA packages [90]. A lower level of silver content in the SAC compositions has been shown a significant improvement in their board level reliability in drop/shock testing. In contrast, researchers have shown that higher silver content SAC alloys have enhanced thermal reliability [91, 92]. The SAC alloy performance has been compared with conventional

leaded solder compositions [94]. Experimental studies conducted have shown that a significant enhancement in SAC based solder-joint reliability can be achieved by using compliant plastic substrates.

When the grain structure is coarser, there are fewer grain boundaries to block the dislocation movement, causing a loss of strength of the material. From experimental data, Hall and Petch independently found that the yield strength of a polycrystalline material is inversely proportional to its grain size [60], as shown in Equation 2.1:

$$\sigma_y = \sigma_i + kd^{-0.5} \quad (2.1)$$

Here  $\sigma_y$  is yield strength of the polycrystalline material,  $\sigma_i$  is the material constant, which represents the overall resistance of the lattice to dislocation movement;  $k$  is a constant which measures the contribution of hardening due to grain boundaries; and  $d$  denotes the grain size. The Hall-Petch theory states that increasing grain size degrades the strength of materials. The increasing grain size will cause the amount of grain boundaries to decrease, and with fewer grain boundaries to resist the movement of dislocations the hardening contribution due to grain boundaries will be diminished, and the material loses strength. The grain and phase structure coarsening is promoted by the self-diffusion of atoms, interstitials, and vacancies. According to the diffusion fundamental equation, Equation 2.2 [60],

$$D = D_0 \exp\left(-\frac{Q}{RT}\right) \quad 2.2$$

Where

$D$  = diffusivity,

$D_0$  = a constant that is independent of temperature,

R = the Boltzmann constant,

Q = the activation energy, and

T = the absolute temperature.

Higher temperatures will increase the diffusivity of the atoms, interstitials and vacancies, leading to grain growth. Under normal conditions, the atoms reach an equilibrium position to balance the attraction and repulsion forces. When an external force is applied within the elastic region no interatomic bonds are broken, and only the balance of the attraction and repulsion forces changes. Consequently, microstructural changes have little effect on the value of the true modulus. In engineering practice, the apparent elastic modulus is obtained from the slope of the stress-strain curves and includes time-dependent inelastic deformations such as creep. Creep is strongly dependent on the dislocation movement and grain size. Coarser grains will cause more dislocation movement, and thus lead to more severe creep deformation. The contribution of plastic deformation to the apparent elastic modulus will therefore increase with increasing grain size. This is why isothermal aging can cause a reduction in the apparent elastic modulus.

The aging effects on the microstructures of 63Sn-37Pb, Sn-3.5Ag and SAC405 solder balls on Cu/Ni/Au surface finish were investigated by Fan [95]. The thickness of the IMC layers all increased with aging time and temperature. 63Sn-37Pb has the larger diffusion coefficient and the IMC thickness grow rapidly.

Li et al [96, 97] studied the microstructure of flip-chip packaging with SAC387 solder joints aged at different temperature. The morphology of interfacial IMC  $(\text{Cu,Ni})_6\text{Sn}_5$  remained unchanged during aging, but its thickness increased considerably by a volume diffusion mechanism. The Sn IMCs existed as plate-like or as small particles around the  $\beta$ -Sn dendrites in the bulk solder. Two different Sn coarsening processes take place under high temperature aging: first, small Sn particles directly coarsened into pebble-like phases and second the plate and lamella  $\text{Ag}_3\text{Sn}$  phases broke up into small parts and then coarsened into pebble-like phases.

According to the working draft of IPC-9703, there are eight different failure modes expected from a drop test [99]. These are shown in Figure 2.2. Previous studies [100-103] show that the onset of failure will occur at the corner joints of BGA packages, either due to a fracture at the BGA package/IMC interface, or fracture at the PCB metal/IMC interface. The studies all showed that reliability and performance of Sn-Pb was superior to LF.

Farris reported from his drop test of LF CSP's that the SEM indicated the intermetallic layer thickness were 1-1.3 micron on board side and 1.3-2 on the component side for the outer row of solder joints. To investigate the extent of cohesive failure resulting from the drop tests, the dye penetrant test was performed and 58% showed trace failure under the pad and 12% solder joint on board side. There were no solder joint failures at the component side. The following relation was derived:

		Electrical failure	
		Yes	No
Resin cracking under pads	Yes	72%	19%
	No	6%	3%

Table 2.2: Relation of Failure Modes from Drop Testing by Farris

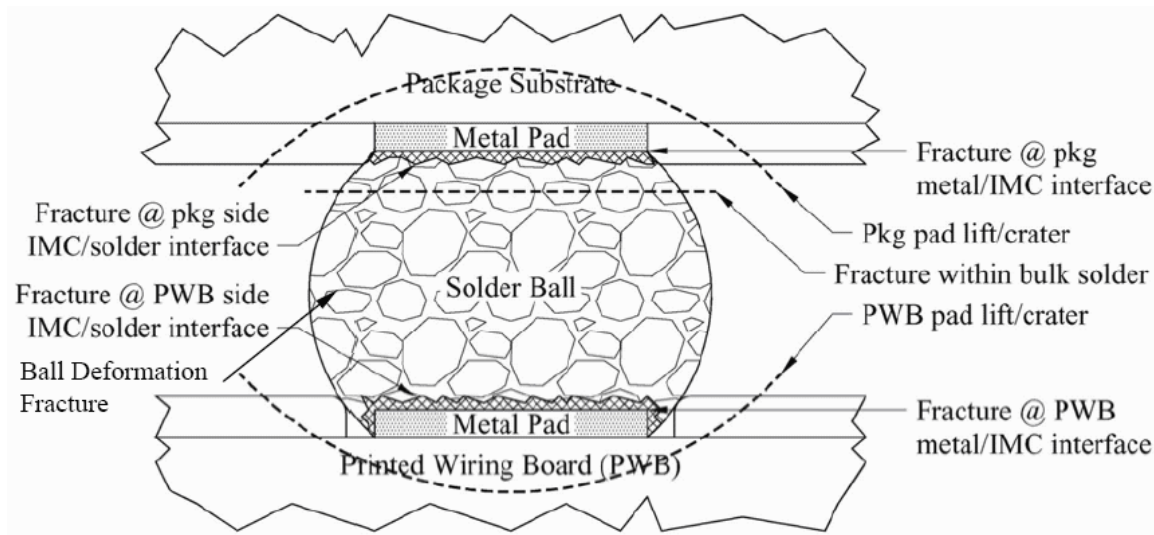


Figure 2.2: Expected Failure Modes from Drop Testing [99]

### 2.3 Effects of Kirkendall voiding

Kirkendall voids have been reported at the solder/Cu interface by many. The interdiffusion of copper particles and tin particles give rise to voids at the joints. The process of Kirkendall void formation can be classified into two stages, (1) Cu atoms leave the Cu pad and diffusion towards the solder, which generated vacancies near the Cu<sub>3</sub>Sn layer. (2) The vacancies coalesce into voids with time and higher temperature.

Chiu et al. [82] reported tests of ball grid arrays with Sn-Ag-cu solder balls with copper pad, thermal aged at 100°C, 125°C, 150°C, and 175°C for 3, 10, 20, 40 and 80 days. It was found extensive Kirkendall voids at the interface of solder joint to copper substrate. The voiding process was noted even at 100C, and after 10 days aging at 125°C. The performance of drop/shock test degraded 80%. Higher temperature generates more voids during the same aging time.

Date et al. [104] reported after 500 hours of aging at 150°C a lot of voids were observed in Cu<sub>3</sub>Sn phase at the interface between solders and Cu. As the aging time increased, transition from ductile to brittle associated with the fracture inside the solder to within the interfacial intermetallic compound phase was reported.

Ahat el al [105] studied the interface microstructure and shear strength of 96.5Sn-3.5Ag and 63Sn-36Pb-2Ag on Cu after aging at 150°C for 0, 50, 250, 500 and 1000 hours. The volume of voids formed in the Cu<sub>3</sub>Sn phase increased with the ageing time. The shear strength of both Sn-Ag and Sn-Pb-Ag decreased with the aging time. It was also noted that the fracture mode changed from the mixture of solder and IMC at zero aging time, to complete fracture within IMC layer after 1000 h aging.

Mei et al. [106] studied the conditions for voids formation and voids effects on the electronic reliability. Voids were found in high, low and even zero densities in samples of different cases after aging either for 20 days at 125°C or for 5 days at 145°C. Voids were seen in thermal cycled assemblies. It seemed that the Cu plating process and the small concentration of Ni in either the solder or the substrate influences the void density and distribution.

## **2.4 Drop/Shock Testing methods**

Solder joint reliability in electronic products for harsh mechanical environments such as drop impact is conducted using experimental techniques at the board level and the product level. Product level drop tests on completed products provide a more realistic scenario of the level of shock experienced by the solder interconnections. Product level



evaluation of drop and shock reliability depends on experimental methods. The most realistic shock tests would be product-level tests on the complete product to assess its performance under drop impact. But these tests are very expensive. Board level drop testing mimics the real-life drop impact conditions and are more controllable as compared to product level drop tests. The board level testing does not take into account the interaction between the PCB, plastic casing and other internal components of the product. The standardized JEDEC drop tests do not take into account the various drop orientations with which the product may strike the impacting surface or multiple impacts due to rebounding. Shock response experienced by the PCB in product level drop can be used to set up the board level drop to reproduce the real time conditions that the package components and solder joints undergo during actual drop. In order to address these issues, extensive experimental tests are carried out to understand the variations in the dynamic responses of the PCB subject to board or product level drop.

A product level and board level drop tests on a mobile phone and its PCB was carried out by Lim et al. [107]. The test vehicle was gripped in various orientations and allowed to have an impact under gravity from desired heights using a drop tower. Results indicated additional levels of deformation of the PCB in case of product level drop due to severe rebound impact. The drop impact responses of various mobile phones and personal digital assistants were carried out at various orientations from a drop height of one meter and accelerations, strains and impact forces were measured. The maximum PCB strains and accelerations were recorded in product level drop in the horizontal direction. Wu et al. [108] carried out product level drop tests on a customized drop tester

equipped with a drop control mechanism to control drop orientation and achieve a high degree of reliability.

Xie et al. [109] performed free fall board level and product level drops of area array LGA packages and measured the accelerations at the board and package side. It was found that the accelerations obtained in case of phone drop were much lower than those in the corresponding board level drop. The FEA results showed higher values for PCB warpage and maximum plastic strain in the solder joints in case of product level drop.

Lall et al. [110, 111] performed a controlled drop test of BGA and CSP packages from different heights in the vertical direction. Strain gages were mounted at the various component locations at both at PCB side and the package side, the Strain and continuity data obtained during the drop event with the help of a high-speed data acquisition system, the data was recorded at the rate of around 5 million samples per second. Failure analysis of the failed test specimen showed solder joint failures at the package and board interfaces and copper-trace cracking.

It has been reported from a product level drop test that a horizontal drop orientation gives the largest impact responses. Wong et al, identified three board-level drop impact characteristics; (a) elongation and bending of interconnection due to differential flexing of PCB and package, (b) inertia force from electronic packages, and (c) longitudinal stress wave from impact. Due to the variation in stiffness of the IC package and the PCB where it is being mounted onto, it results in different flexing of a package and the PCB when the board is subjected to a horizontal drop impact. In a package mounted at the center of the PCB, this differential flexing has caused the corner

solder joints to experience a larger tensile stress that leads to detrimental failure. Inertia force of the body is the second driver for interconnection failure. During free fall, the IC package travels at the same velocity with the PCB mounted on it. Upon horizontal impact, an IC package with a larger size and mass will experience a larger inertia force where

$$\text{Force} = \text{Mass} \times \text{Acceleration}$$

As a result, the solder interconnects falls apart when the impact force reaches a threshold limit. The location of the package on a PCB plays a part in the solder interconnect strength. The PCB adjacent to the supports could experience up to a thousand times (1000g) acceleration and a package near to it could also experience the same acceleration. For a package at the center on the same PCB, its acceleration could only be in the range of hundreds of gravitational acceleration. Thus given the same mass, interconnects in the package placed near the support will be subjected to a larger tensile stress and eventually more prone to impact failure. The high magnitude of longitudinal stress waves transmitted from the support to the adjacent interconnects may induce failure in it.

## **2.4 Effect of design on Drop/Shock Reliability**

For improved drop/shock performance, researchers have investigated the effects of various lead-free solder alloy composition on their reliability. SAC alloy compositions with low silver content have been shown to be resistant to high strain rates under mechanical shock and to have improved drop reliability [92, 112]. By lowering the silver

content of SAC alloys, an increase in their creep rate has been noticed. It has been suggested by Song [113] that adding Ni to SAC alloys to improve their drop reliability. It has also been shown that an improvement in their drop performance can be achieved by using SAC interconnects on Ni/Cu/Au surface finishes [114]. Solder joint reliability has been shown to enhance with UBM/penetration layer/SnAg lead free solder bump structures [115].

Chiang suggested two reflow passes as a means to achieve better reliability characteristic of BGA type packages with reference to thermal performance. A twofold increase in their characteristic life when subjected to thermal cycling due to significant reduction of plastic strain, the energy density and the Von-Mises stress at the solder joint was shown. An improvement in the solder joint reliability of perimeter array packages over area array packages has been documented. Charles reported that low standoff height and large fillets increases the fatigue life under power cycling. The large fillet angles serve to reduce the high magnitudes of stress concentrations as they result in an increased the net cross-sectional area within the joint. The corner solder balls are more susceptible to fail in drop/shock scenarios hence the layout of solder balls is very critical since it affects the load distribution on critical solder ball.

## **2.5 Vibration Durability**

The characteristics of the stress from vibration loading are low amplitude and high frequency, while those from cyclic thermal loading are high amplitude and low frequency. Vibration loading is important because it is commonly encountered during the

service life of many classes of electronic products. However, compared to thermal cycling durability, analysis of vibration durability is more complex and has received less attention in the literature. Compared to thermal cycling durability, the fatigue data for vibration is much less. Like the temperature cycling testing, most reported vibration tests have generally been a comparison of Pb-free assemblies subjected to currently accepted product qualification test levels. Unfortunately, the testing was time-terminated and not run until a significant portion of part failures occurred. In order to have a full understanding of the vibration fatigue properties, durability test and simulation have been conducted for Pb-free assemblies and compared with Pb-based solder alloy benchmark. Among all the empirical work in vibration fatigue, Steinberg [116], who is probably the best known in the area of PCB vibration fatigue, proposed a simple rule of thumb for designing PCB's in a vibration environment.

If the maximum deflection of the PCB is less than a critical value,  $d$ , the component mounted at the center of the board has a life of at least  $10^7$  cycles under sinusoidal vibration or  $2 \times 10^7$  cycles under random vibration.

$$d = \left( \frac{0.00022B}{ct\sqrt{L}} \right) \quad 2.3$$

Where:

$B$  = the length of the PWB edge parallel to the component located at the center of the board (in.)

$L$  = length of component (in.)

$t$  = thickness of PCB (in.)

$c = 1.0$  for standard DIP, 1.26 for DIP with side brazed leads, 1.0 for pin-grid array with four rows of pin (one row extending along the perimeter of each edge), and 2.25 for a leadless chip carrier.

Liu [117] and Wong [118] performed experiments and analysis for High Cycle Fatigue vibration in BGA package. Their experimental system provides controls for varying the cycling frequency and magnitude of the applied load. The failure of solder interconnects in BGA specimens were recorded by direct visual monitoring method. In all test cases, BGA interconnect failure was observed to be the result of crack initiation and propagation along the nickel/solder interface between the BGA solder ball and the ENIG plating on the copper pads of the PBGA substrate.

Zhang [91, 93] has reported that the fatigue curve of Pb free SAC obtained from lap-shear testing, has a smaller slope than Sn37Pb solder. Thus, Sn67Pb was found to be more robust at low load levels (high-cycle-fatigue) while SAC was more robust at high load levels, with a cross-over at intermediate stress levels.

Yang et al [119-121] conducted several studies on PBGA vibration reliability, including modal analysis of board, vibration reliability characterization under out-of plane excitation. Yu [122] and Shah [123] simulated the dynamic behavior of electronic package and reliability of BGA solder joints. Tu [124] examined the effect of intermetallic compounds on vibration fatigue of  $\mu$ BGA solder joint. Kim et al [125] proposed a new method for evaluating the high-cycle fatigue strength of BGA packages with Pb-free and Pb solder due to vibration. By attaching a weight and inducing a mixed

mode stress in the package and on the joints. The test frequency used in the test was 15-25 Hz which did not affect the solder joint fatigue strength.

## **2.6 Failure Analysis**

Failure analysis provides significant insight on the mechanisms that causes the deterioration in reliability of electronic packaging. Prediction of failure was investigated using fracture mechanics [126], von-mises stress [127], and board-strain based damage index [128]. Failure of the interconnects occurs at the interface close to the device or board side as these are the highest stressed locations in the joint. The extent of damage and failure modes varies for different alloy systems. The impact failure modes of SnPb solder were predominated by bulk failures as the bulk solder deformation absorbs some of the impact strain and cracks through solder rather than through the interfacial intermetallic. Lead-free solder, on the other hand, exhibits a mixture of IMC and bulk failure that occur along the bond interface [129]. The imposed strain in the SnAgCu joints moves away from the bulk solder into the lower strength brittle IMC as the apparent strength of the solder increases at higher strain rates [130]. Comparison of the failure modes of SAC alloys indicated that crack propagation through the bulk solder was more in SAC105, due to a lower elastic modulus, than brittle IMC layer in SAC405. Failures at the intermetallic layer on the package side and the laminate beneath the pad location on the board side were predominant in SAC305 [131].

In the Table 2.2, a total of 14 fatigue models have been characterized [132].

<b>Fatigue Model</b>	<b>Model Class</b>	<b>Parameters</b>	<b>Coverage</b>	<b>Applicability</b>
Coffin-Manson	Plastic strain	Plastic strain	Low cycle fatigue	All
Total Strain	Plastic + elastic strain	Strain range	High and low cycle fatigue	All
Solomon	Plastic shear strain	Plastic shear strain	Low cycle fatigue	All
Engelmaier	Total shear strain	Total shear strain	Low cycle fatigue	Leaded & leadless, TSOP
Miner	Superposition (plastic and creep)	Plastic failure & creep failure	Plastic shear and matrix creep	PQFP, FCOB
Knecht & Fox	Matrix creep	Matrix creep shear strain	Matrix creep only	All
Syed	Accumulation of creep strain energy	gbs energy and mc energy	Implies all coverage	PBGA, SMD, NSMD
Dasgupta	Total strain energy	Energy	Joint geometry accounted for	LLCC, TSOP
Liang	Stress/strain energy density based	Energy	Constants from isothermal low cycle fatigue tests	BGA and leadless joints
Heinrich	Energy density based	Energy	Hysteresis curve	BGA
Darveaux	Energy density based	Damage + energy	Hysteresis curve	PBGA, leadless
Pan	Strain energy density	Strain energy density and plastic energy density	Hysteresis curve	LCCC
Stolkarts	Damage accumulation	Damage	Hysteresis curve & damage evolution	All
Norris & Landzberg	Temperature and frequency	Temperature frequency	Test condition vs. use conditions	All

Table 2.2: Summary of solder joint fatigue models [132]



## **Chapter 3**

### **Selection of Test Vehicle, Parts and Process parameter**

#### **3.1 Why Fine Pitch BGA?**

The need for compact devices is on the rise due to customers desires for small but multifunctional devices. The majority of the electronics OEM market is moving towards miniaturization with higher level functional integrity. The best examples of this are the new smart phones, mobile and wireless devices. Whether the industry is prepared or not, the fine and ultra-fine pitch chip scale packages, micro BGA's and other active devices are being adapted by designers of next generation of thinner, faster and sleeker portable devices. The packaging trends for hand held devices are 0.3mm or less ultra-fine pitch BGA's in the future. Number of electronics sub-assembly houses and OEMs are forging ahead using earlier generation knowledge without knowing the consequences and how it affects the reliability along with the complication factor of being lead free.

#### **3.2 Purpose of the study**

From previous studies and tests provide an idea of how time and temperature affect the reliability of solder joints under different condition. Fine pitch lead free packages have started to enter critical everyday instruments but the knowledge of the combined effect has only scratched the surface of the reliability effect. The need to know more in a reliability standpoint is higher than ever. The mechanical properties of SAC alloys have shown to change at elevated temperature, but a time conscious approach is in need to study the effect and to get a better understanding.

### 3.3 Test Board

The substrate material selected for the test vehicle chosen was FR-406. FR-4 is a grade assigned to substrates which has glass reinforced epoxy laminates; it is composed of woven fiberglass cloth with an epoxy resin binder that is flame resistant or self-extinguishing. The material is known to retain mechanical and electrical insulating qualities in both dry and humid environments. It has a glass transition temperature of around 170°C. The dimension of the test board chosen is 3.94 X 2.64 inch with a thickness of 0.062 + 0.007 inch measured laminate to laminate. Figure 3.1 shows the dimension of the board along with the tooling holes drilled. The copper is distributed in four circuit layer to provide typical CTE for thermal cycling test. The copper on each of the layer is ½ oz.

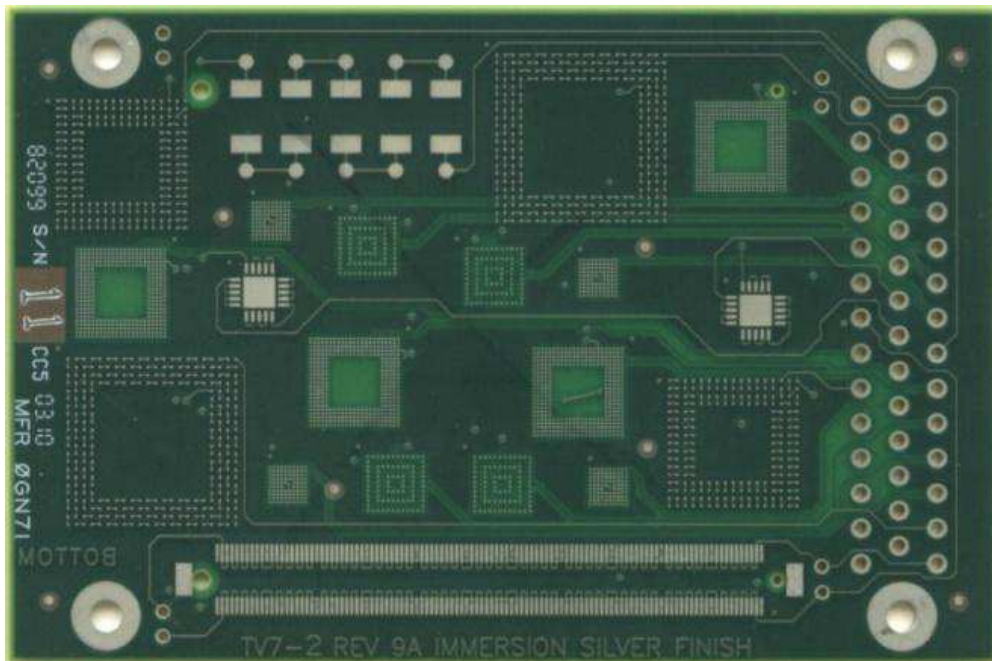


Figure 3.1 Finished TV7 Test board

The manufacturer applied the standards ANSI Y14.5M-1982. The rigid printed wire board conformed to the requirements of IPC-6011 and IPC-6012 type 3 class 3. The prepreg material used complied to IPC-4101 and in accordance with IPC-2222. The copper plating for holes, pads and conductors are as per IPC-6012 Table 3-2 Class 3. Minimum conductor width is specified at 0.003 inch and the same for conductor feature spacing. Solder mask material and application is per IPC-6012. The TV7 boards have non-solder mask defined pads. The exposed copper was covered with Immersion Silver for a set of 500 test boards and Immersion Tin for a set of 250 boards. Figure 3.2 shows the layer arrangement, Figure 3.3 is completely finished board.

### **3.4 Part and process parameter Selection**

The parts chosen to go on the Test Vehicle was provided by Practical Components. These packages have a “dummy” die to emulate real world parts. With a daisy chain laid through the substrate to help in sampling for reliability in an accelerated life test. They are intended to be monitored for continuity in order to study the reliability of the joints.

The test vehicle consists mostly of active components of various size and pitch. It included PBGA's, QFN's and CSP's. The only passive component used is a 2512 resistor. The BGA components were of both lead and lead free terminations. The lead free terminations consisted of Sn-1Ag-0.5Cu and Sn-3Ag-0.5Cu for BGA's. The Lead components were of 63Sn-37Pb formulation. The passive resistor were Sn terminated.

The fine pitch BGA's consisted of four different sizes and three different formulations (SAC105, SAC305 and 63Sn-37Pb), 19mmX19mm, 15mmX15mm, 10mmX10mm and 5mmX5mm. The QFN was 5mmX5mm with tin terminations. The CSP's were of 7mmX7mm with 2 layers of solder balls of SAC305. The resistors selected were of 0.25''X0.12'' and used in a daisy series of 5 a side, they had tin terminations. This was mainly incorporated to act as a control factor to match with previous studies. The complete matrix of components selected is summarized in the following table.

Package	Body Size (mm)	Die size (mm)	Ball/Lead Count	Pitch (mm)	Ball Alignment	Alloy		
						Sn-Pb	SAC105	SAC305
CABGA	19X19	12X12	288	0.8	Perimeter	X	X	X
CTBGA	15X15	12.7X12.7	208	0.8	Perimeter	X	X	X
CVBGA	10X10	5.0X5.0	360	0.4	Perimeter	X	X	X
CVBGA	5X5	3.2X3.2	97	0.4	Full Array	X	X	X
CTBGA	7X7	5.9X5.9	84	0.5	Perimeter	X		X
MLF	5X5	4.5X4.5	20	0.65	NA	X		
Resistor	6.3X3.2	6.3X3.2	2	NA	NA	X		

Table 3.1 Component Matrix

### 3.4.1 Assembly Selection

The test intended to build around 750 TV7 test board, 500 of them with Immersion Silver plating and 250 of them with Immersion Tin. Some test boards were populated on both sides and some on one side only. The reason for this type selective assembly was the limited availability of components. According to the type and number of parts which went on the test board, they are classified into 8 groups, LF1-4 and Pb1-4. The boards were built in a way that they had different number and arrangement of parts on top and bottom side of the board. A summary of order is given in the table below:

Parts	Pb1	Pb2	Pb3	Pb4/Connector
19mm SnPb	2	1	1	0
15mm SnPb	2	1	1	0
10mm SnPb	2	1	1	0
5mm SnPb	2	1	1	0
CSP SnPb	1	0	1	0
MLF	1	0	0	0
Resistor	5	5	5	5
Connector	0	0	0	1

Table 3.2 Component Matrix for Pb series

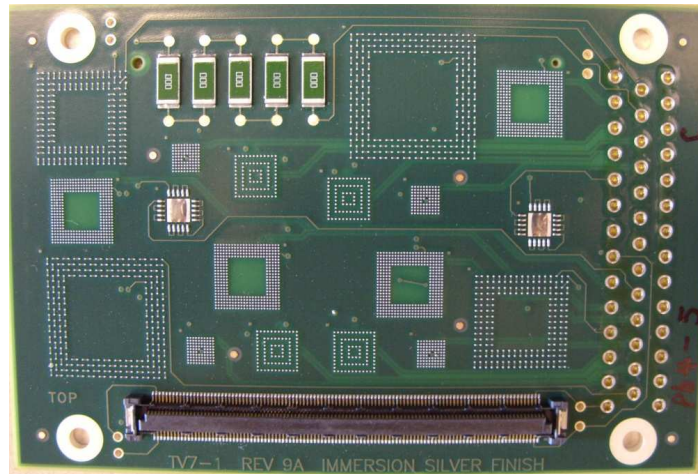


Figure 3.2 Pb4/Connector board

Parts	LF1	LF2	LF3	LF4/Connector
19mm 305	1	1	1	0
19mm 105	1	1	1	0
15mm 305	1	1	1	0
15mm 105	1	1	1	0
10mm 305	2	2	1	0
10mm 105	2	2	1	0
5mm 305	2	2	1	0
5mm 105	2	2	1	0
CSP 305	2	0	0	0
MLF	2	0	0	0
Resistor	5	5	5	5
Connector	0	0	0	1

Table 3.3 Component Matrix for LF series



Figure 3.3 LF1 assembly

### 3.4.2 Solder Paste Selection

Among the two types plating finishes only Immersion Silver boards were used for Sn-Pb paste. All the tin boards were assigned for Lead-Free Paste. Type 3, Kester EP256 paste was used for Tin-lead assembly and Senju 305 of M31-GRN360-KV series was used for Lead-free assembly. Both were of no clean type. The properties and characteristics are summarized in the following table:

Property	Kester EP256	Test Method	Senju M31-GRN360-KV Series	Test Method
Alloy Composition	Sn63-Pb37		Sn95.75:Ag3.5: Cu0.75	
Flux Type	ROL0	J-STD-004	ROL0	J-STD-004
Flux Content	10%		11.5%	JIS Z 3197
Cleaning Type	No Clean		No Clean	

Table 3.4 Comparison of Solder Properties

### 3.4.3 Stencil Selection and screen printer parameter.

The stencils for TV7 were electroformed, to go with MPM up2000 HiE screen printer. The screen printer had two metal squeegee, with one pass for a print and alternating squeegee for following boards in alternating direction. The printer was set for on contact print with a force of 10Psi. The following table has the stencil specification:

Material	Stainless Steel
Aperture type	Electroformed
Stencil Thickness	0.004 inch
Size	24X24 inches
Step Type	Single
Frame Border	Poly

Table 3.5 Stencil description

### 3.4.4 Surface Mount Assembly Process

The assembly of test boards was performed at Continental Electronics, Hunstville, AL. The whole process took place in the prototyping lab, which consisted of screen printer, placement machines and a reflow oven. All the parts were ordered in trays. Since there were fine pitch parts involved, Assembleon MG-1 was used, hence the fine pitch parts were taped and reeled, and hence Universal GSM-1 was used to handle the rest of the parts in trays. The components that were reeled were all the 5 and 10 mm BGA's, MLF's and CSP's. The resistors came in reels. The bigger parts, 15 and 19 mm BGA's were in trays. Both the machines were programmed in a way that the machines had



separate files for Pb1-4 and LF1-4. This was made just to ensure that there were no mishaps of misplacing wrong parts. The placement of parts were checked after the reflow profile was finalized by X-rays and URSA scoping. The problems faced and necessary changes made are discussed in the following chapter.



Figure 3.4 Continental Prototype Lab

### **3.4.5 Reflow process**

The reflow was performed using a 13 zone Rehm V7 convection oven. In order to attain a good profile which meets the suggested parameters of solder paste like time of soak and time above liquidus temperature, Slim KIC 2000 was used. One test board was assembled and reflowed at a profile used for a different board and it was used to arrive at a profile for the test boards. The thermocouples of Slim KIC 2000 were placed deep inside parts and in the board. This was done by drilling fine holes that it did not crack the part, the holes were on the part and underneath the part. The test board used for profiling was fully populated in order to mimic the thermal mass of what was to be built.



Figure 3.5 Reflow Oven

The same process was carried out for both lead and lead free boards and respective profile were attained as shown in the figure below after free fine tuning to meet all the critical parameters like soak time, time above liquidus and peak temperature. In order to ensure the profile was good several tests were done like URSA scoping and popping a part. The problems and approaches are discussed in the following chapter.

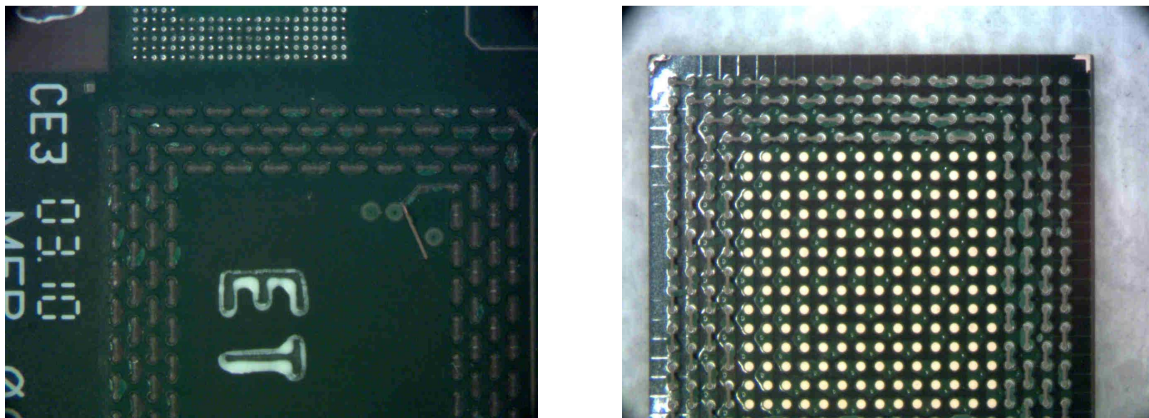


Figure 3.6 Right 19mm lead package and its respective pad on left

In order to make sure the bonding is good, the parts are pulled of the boards and it is seen that the pulled off part contains the daisy chain traces from the boards. This ensures the profile is creating a good solder joint.

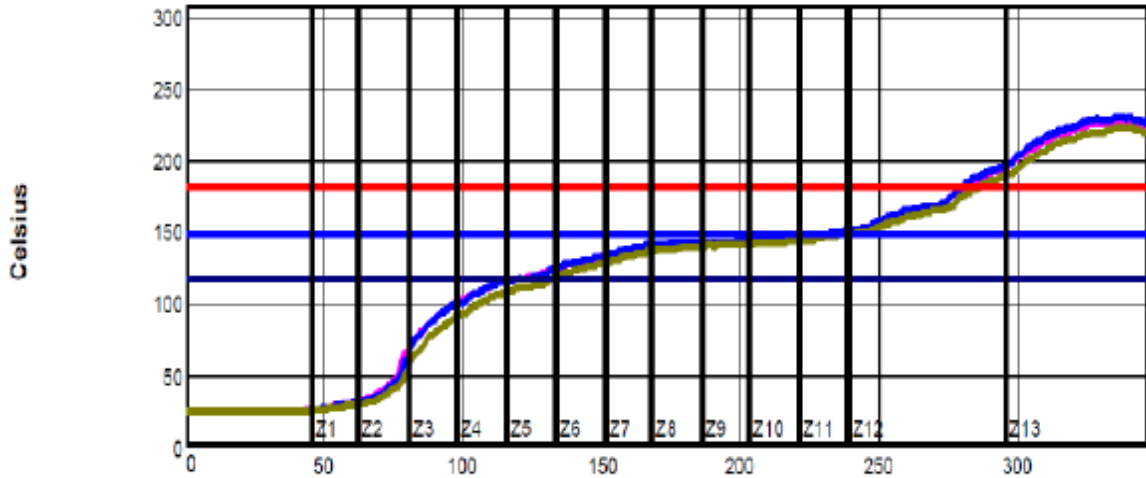


Figure 3.7 Sn-Pb solder profile

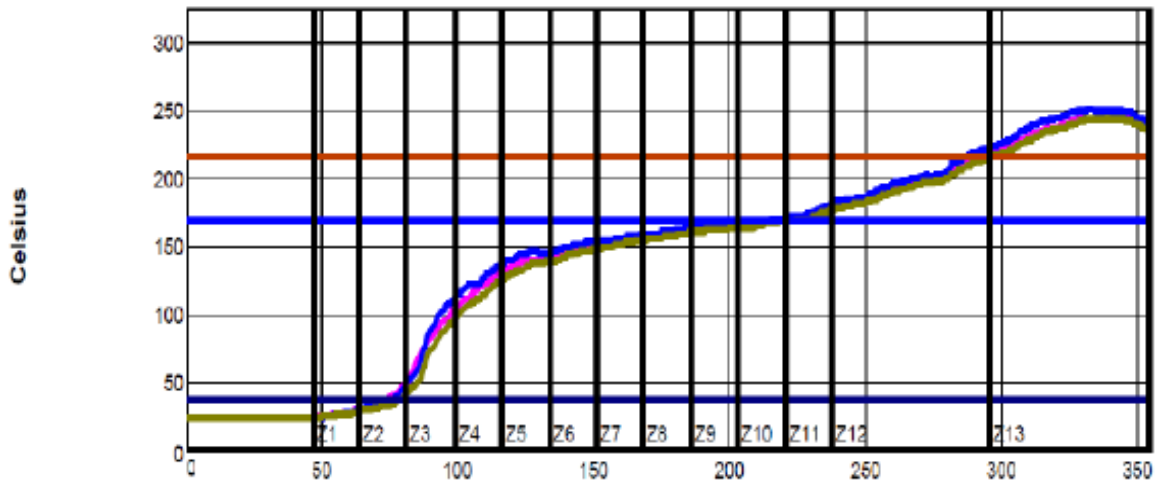


Figure 3.8 SAC solder profile

## Chapter 4

### Assembly challenges and Solutions

#### 4.1 Placement issues and approaches

The test boards after reflow were X-rayed in order to check the exact placement and ball on pad location. In some cases it was found that the solder balls were of location and the process of placement was fined tined in order to get the right location.

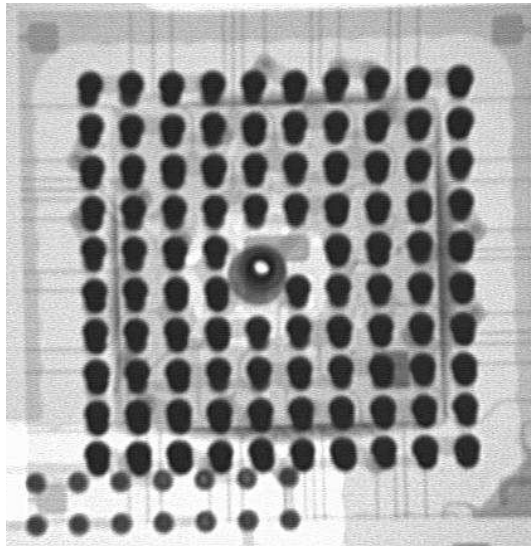


Figure 4.1 X-ray image to check location



Figure 4.2 URSA scope image to check location

One more factor which was contributing to the issue was there were two types of machines, one took the component height and other was pressure to place a component. The heights were provided from the part diagram and fed. There was still some issue with one part where the height was not exactly to that of the diagram, hence it was being dropped off from a height on to the pads and did not sit properly. This was later fixed by manually measuring the part height. The machine which used the pressure was a trial and error method where too much pressure would make the test board flex and the component jump out of place when released.

## 4.2 Screen Printing Issues and approaches

Initially when the boards were printed with paste, visual inspection found that there was uneven distribution of paste on the board. It was concluded that the aperture size on the stencil was not large enough to allow sufficient amount of paste on to the board. Some pads had more than sufficient amount of paste while others had very less in order to make a traditional solder joint.

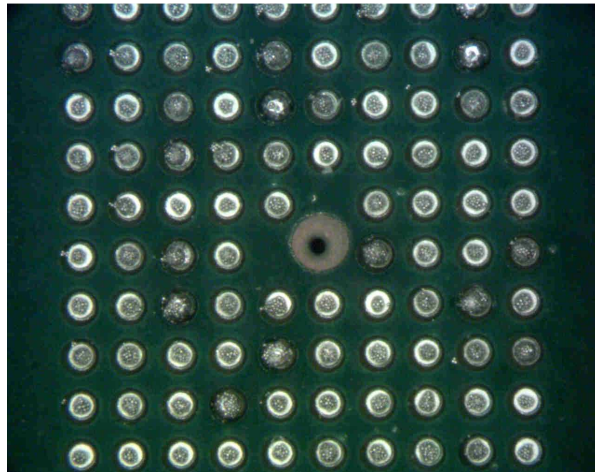


Figure 4.3 Insufficient paste on pads



To fix the problem, the apertures size on the stencil was opened up to allow more paste to be deposited on the board. This in turn led to an interesting effect of bridging, which was caused by deposition of too much paste on the pads. The most affected in the process were the 0.4 mm pitch components. The Figure 4.4 shows bridging after the paste print but this was overcome by frequent wiping of the stencil between prints.

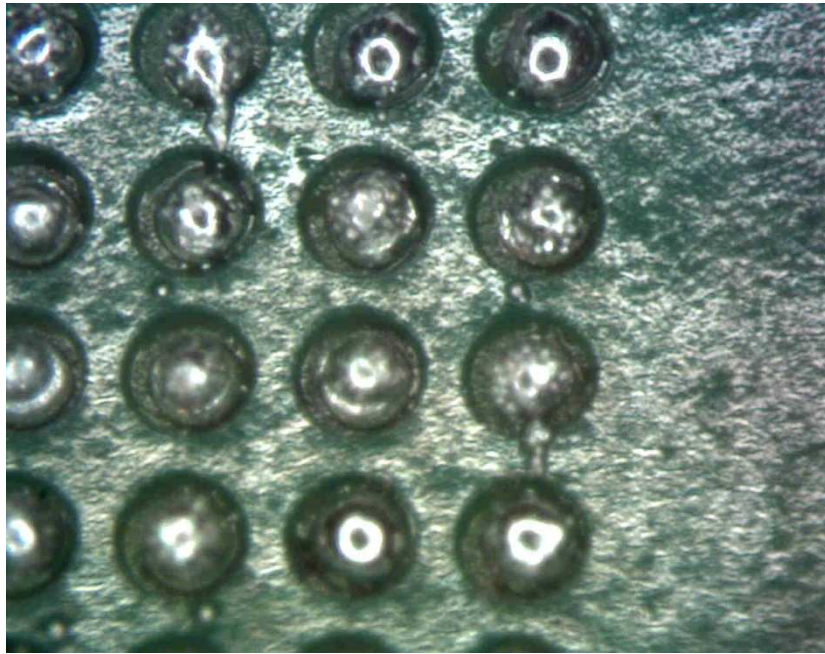


Figure 4.4 Bridging after screen printing

After overcoming the issue, parts were placed, reflowed and X-rayed, where extensive bridging was found as in Figure 4.5. To overcome the issue it was decided not to print the 0.4 mm pitch parts but to flux them with tacky flux and have parts placed. The flux was applied with a brush and the amount of flux combined with the weight of the low part caused it to float and skew in the reflow oven. The figure 4.6 shows the effect of too much flux. The brushes used to apply the flux were changed so only a fine amount was applied.

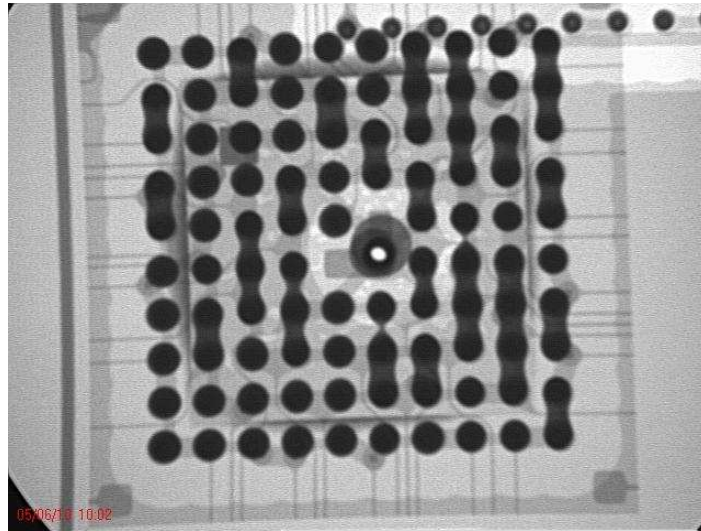


Figure 4.5 Bridging after reflow process due to excess paste

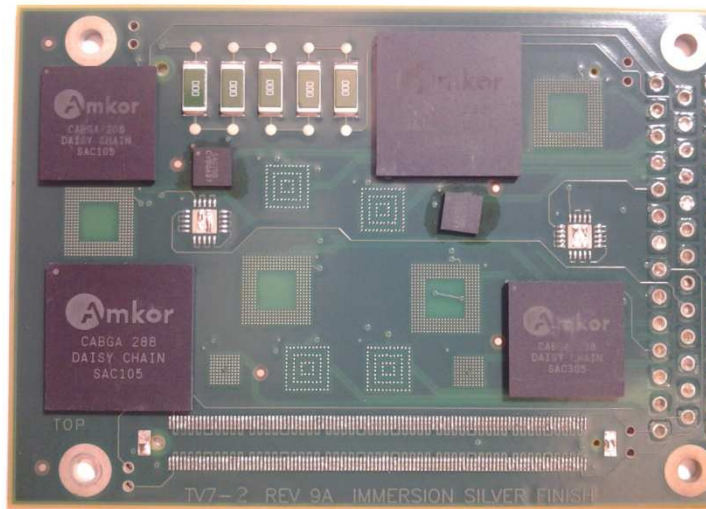


Figure 4.6 Skewing of parts due to excess flux

### 4.3 Reflow Issues and Approach

To arrive on a profile which would comply with the parameters of the solder paste and make a good joint is a trial and error process. During this process the problem faced was head and pillow effect where the solder ball from the component did not collapse to

mix with the solder paste as shown in Figure 4.7. This was the result of insufficient time above liquidus temperature.

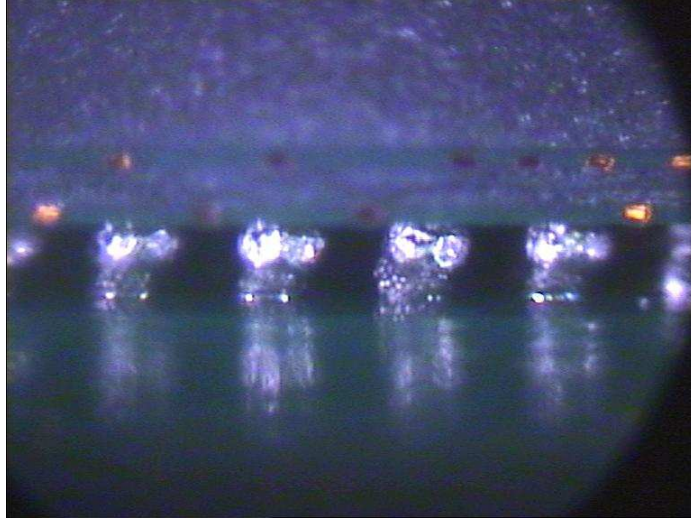


Figure 4.7 Failure of collapse of solder ball

This was overcome by increasing the temperature of zones which contributed to time above liquidus temperature, also by slowing the chains to give more soak time to arrive at the final profiles with properties mentioned below the graph. The collapse of solder balls was achieved as in Figure 4.8.

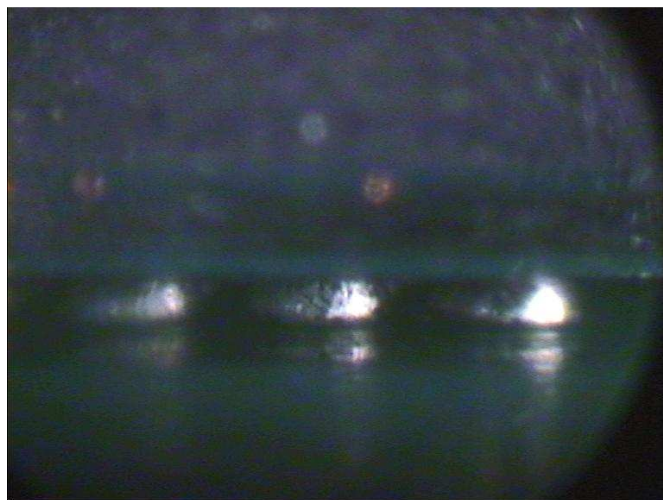


Figure 4.8 Collapse of solder ball



#### 4.4 Immersion Tin board Challenge

Immersion Tin is one of the widely used plating finishes and double side Immersion Tin has always faced problems [96, 48]. When the assembly on side 1 was taking place after all the above challenges were addressed, there were very few issues. When side two was being assembled, Immersion silver boards had significantly less issues than to Immersion Tin. For the Tin boards there was very little solder joint strength after reflow. Some components were falling of the board or could be picked off by using fingers.

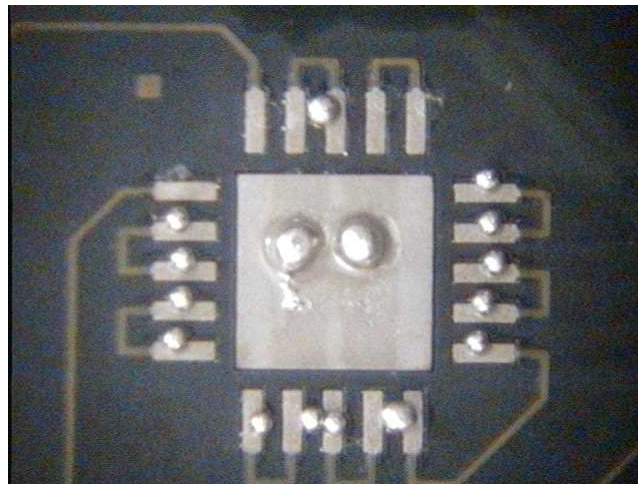


Figure 4.9 Solder Creeping on pads of QFN

Initially it was thought that the reflow temperature for the second side was not correct, however when Immersion silver boards were built, there no issues. This prompted a closer look at the tin boards. When solder is placed on a pad and reflowed, it usually spreads all over the pad evenly. In the case of Immersion Tin boards there was creeping of solder as in Figure 4.9 and 4.10.

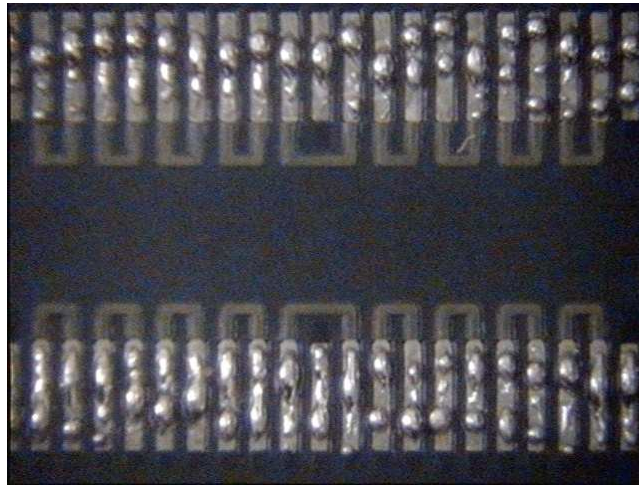


Figure 4.10 Solder Creeping on pads of connector

To check, a test board was taken and flooded it with flux and used a heat gun to melt the solder. The solder did melt and spread when the flux and air flow was present but started to creep up when both flux and hot air was absent. [96] reported that the plating thickness can give rise to failure. With insufficient thickness IMC decreases affecting solderability.

To rule out oxidation which can affect the solderability, Auger electron spectroscopy was used to analyze the test boards. This true surface technique allows detection of all elements of the periodic table present except for the material H located within the first 50 Å of the surface to a sensitivity of 0.01 atom%. A comparison study was done by testing a board which had under gone reflow once and a board reflowed twice, performed were under Lead Free profile. It was observed that there was significant Cu presence, which might be due to increased inter diffusion between Sn and Cu to form an intermetallic compound during the higher temperatures employed for the Lead Free reflow profiles.

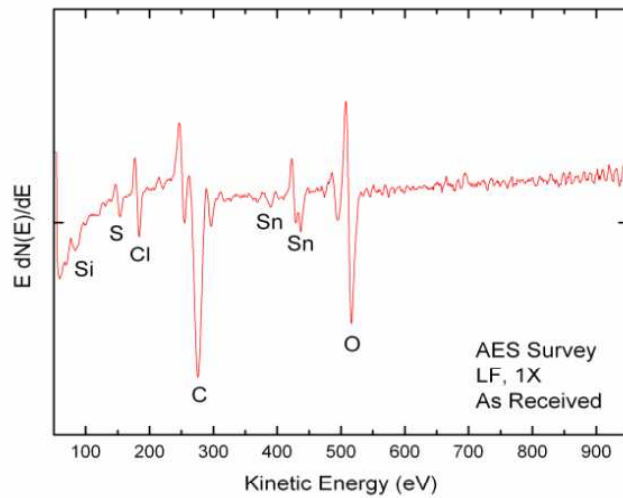


Figure 4.11 AES Spectral for once reflowed board

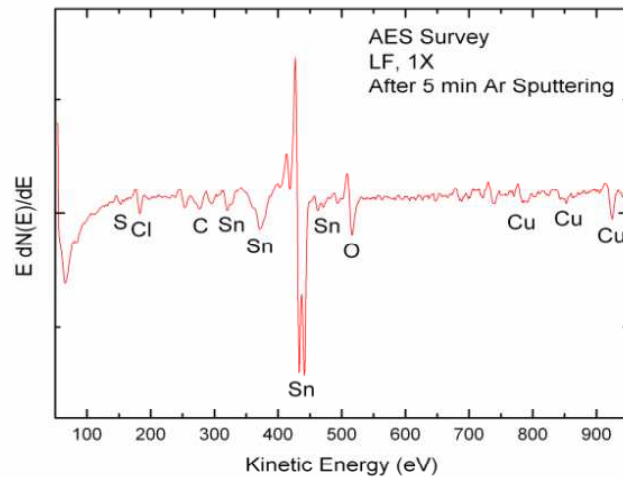


Figure 4.12 AES Spectral for once re-flowed board after sputter cleaning

The test was carried out by sputter cleaning with Argon for 5 minutes and the AES was performed. The following graphs were obtained as in Figure 4.13 and 4.14. There were significant less oxide present; this was due to the fact that after the reflow of side one and the boards were not stored inside humidity chambers. Humid conditions can

greatly accelerate oxide growth through creation of tin hydroxides. Contaminants present could also break down self limiting nature of tin oxides and accelerated oxide growth.

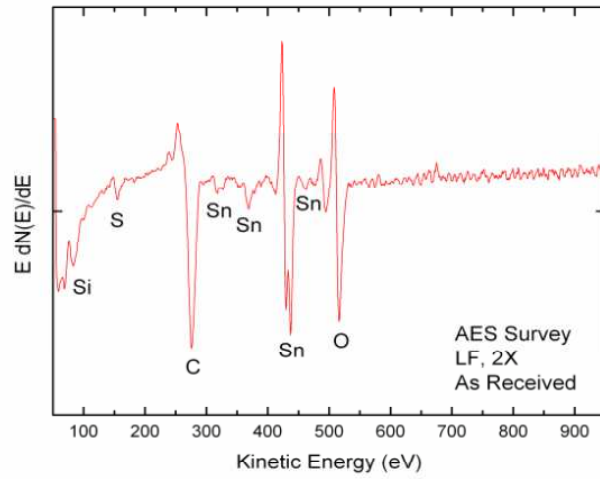


Figure 4.13 AES Spectral for twice reflowed board

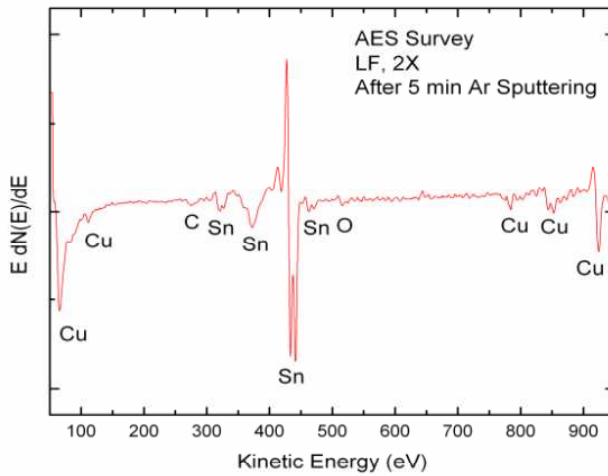


Figure 4.14 AES Spectral for twice reflowed board after sputter cleaning

## Chapter 5

### Vibration Challenges, Approaches and Solution

#### 5.1 Introduction

The Electronic component vibration durability has been studied and several damage laws have been developed to predict the solder joint life time. The mechanical behavior of lead free solders has not been completely understood due to the variation in the total time to failure. Very few laws have been proposed with respect to Lead free solder.

Random Vibration can be represented in frequency domain by power spectral density function. The amplitude is actually  $G_{\text{RMS}}^2/\text{Hz}$ , where RMS is root-mean-square. The unit for acceleration is  $G_{\text{RMS}}^2/\text{Hz}$  versus frequency. The acceleration can also be represented by metric units  $(\text{m}/\text{sec}^2)^2/\text{Hz}$ . In a pure sinusoidal function peak is equal to  $\sqrt{2}$  RMS. But random vibration is complex, the relationship between its peak and RMS value is not straight forward. The peak value in a random vibration is typically 3 to 4 times the RMS value. Power spectral density is over all square by bandwidth.

#### 5.2 Initial Profile and issues

The original profile selected for the test was a complete sine sweep. The frequency ranged between 5 and 500Hz. The test was designed to be a combined environment test, where the test boards were set in a temperature chamber and subjected to vibration. After this they would be thermal cycled for 250 cycles and again they would be put back in the combined environment chamber and the test would continue till 5000

thermal cycles were attained. During the combined environment chamber test the boards will be subjected for vibration for three 15 minutes vibration sessions under the profile over 4 hours while the temperature will be cycled between -25°C and 85°C. During thermal cycling the boards will be cycled between -40°C and 85°C.

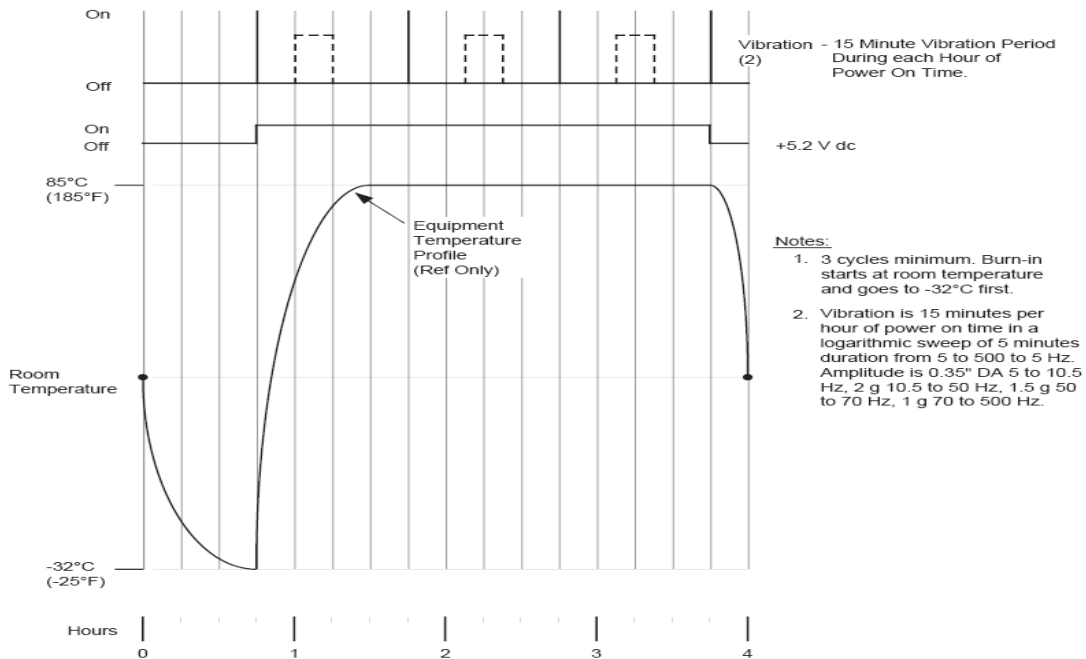


Figure 5.1 Original Vibration profile for TV7

The no aging boards were subjected to 1 cycle of the Combined Environmental Chamber; it was decided to test a small sample size before proceeding with it. Under the original profile, without the thermal cycling the test boards were subjected to vibration for about 15000 minutes which yielded no failures.



Figure 5.2 Fixture capable of testing 8TV7 boards

### 5.3 Alternative approaches

The original profile was altered to cover up to 2200Hz; still it failed to generate failures after 15000 minutes. Various axis and methods of fastening the boards was tried with no result. The test boards were subjected to vibration in X and Y axis which did not yield and result. Hence MIL-STD-810F, Method 514.5 was adopted. Starting from Level 1 till Level 7 which was the machine max was tried. All the levels were random vibration profile and after 17000 minutes of vibration, it yielded 30% failure. During this time many components were falling off the test boards where it ripped the daisy chain from inside the test boards, which was a clear indication that the solder joints were not being stressed but the substrate.



In order to figure out the frequency response required to stress the solder joints the natural frequency of excitation for each components were found using laser measurement and they all ranged between 4050 -5100Hz where the maximum capability of the equipment was 2200Hz.

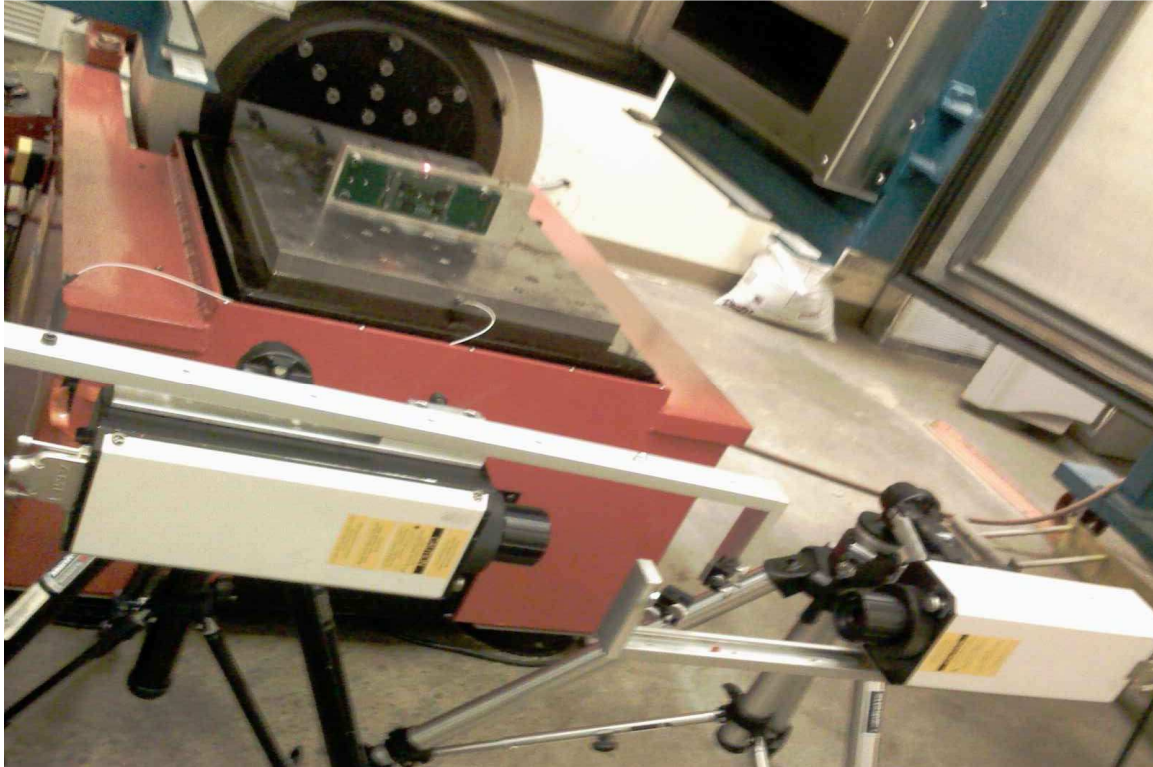


Figure 5.3 Laser measurements to determine natural frequency

To reduce the natural frequency of the components, addition of weights was tried in order to alter the extraction frequency which yielded promising results. It also posed the task of adding weights to the components equally. Attaching weights to the parts on top was the primary approach but it was difficult to maintain a uniform ratio as we moved to the smaller components since the surface area was reduced. Maintaining the weights to the middle of the component was important as shifting the weights to one quadrant of the



component would produce an undesired effect or failure which would be difficult to identify and explain, hence it was abandoned. The second approach was to add a liquidus die on top of each component. Repeatability of the process was again under question and it also had to be abandoned.

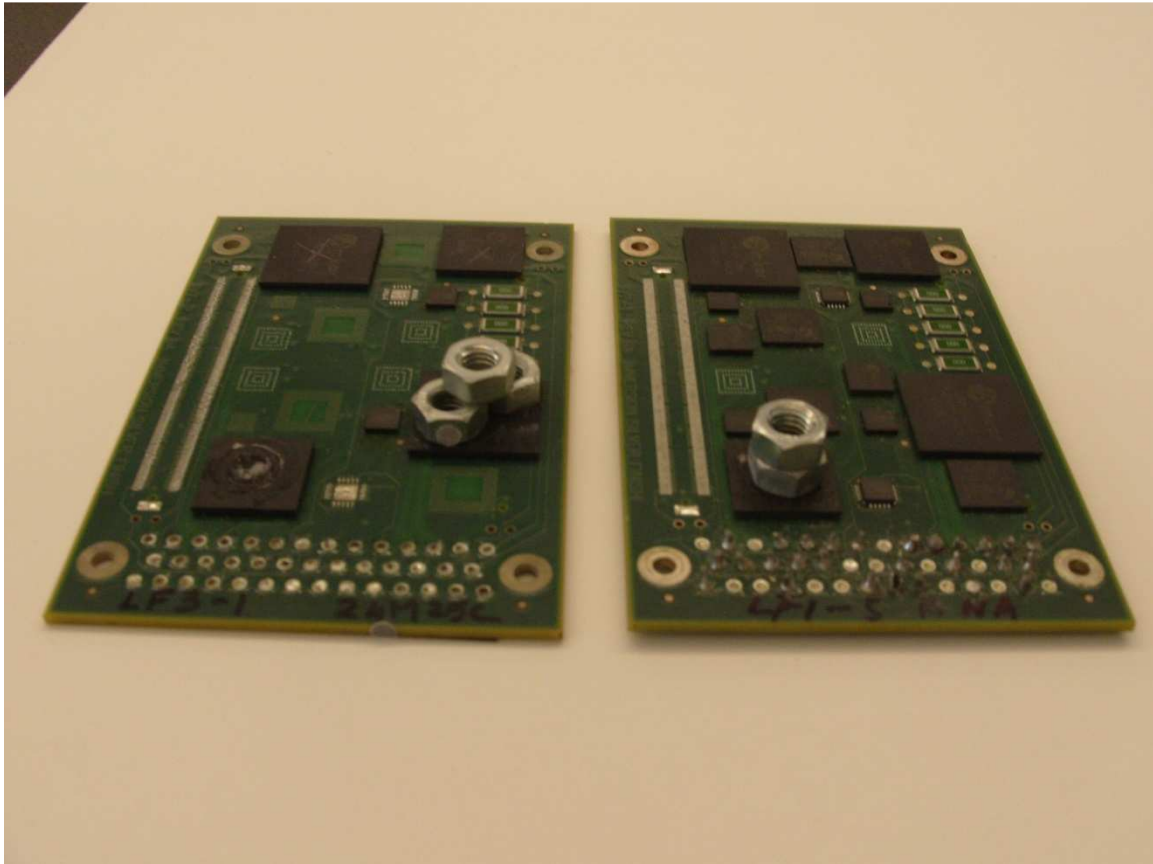


Figure 5.4 Addition of weights

## 5.4 Amplifying Vibration

Inspired by metal backed boards, the approach was turned towards fixing TV7 test boards on metal plate and then subject to vibration.



Figure 5.5 TV7 board on Metal plate

To proceed with this method the vibration level selected was Level 5 and it was subjected for vibration for a period of 600 minutes and at the end of the period it yielded no failures but deformation was noticed at the clamping points. The metal was too soft to transfer the vibration on to the TV7 board or the TV7 boards were too stiff to be flexed by the metal plate. It was clear that a stiffer material was needed as a backing material for the TV7 boards. To overcome the stiffness issue another PCB was used which had a thickness of 0.089 inches which was more than the TV7 board which was 0.062 inches.

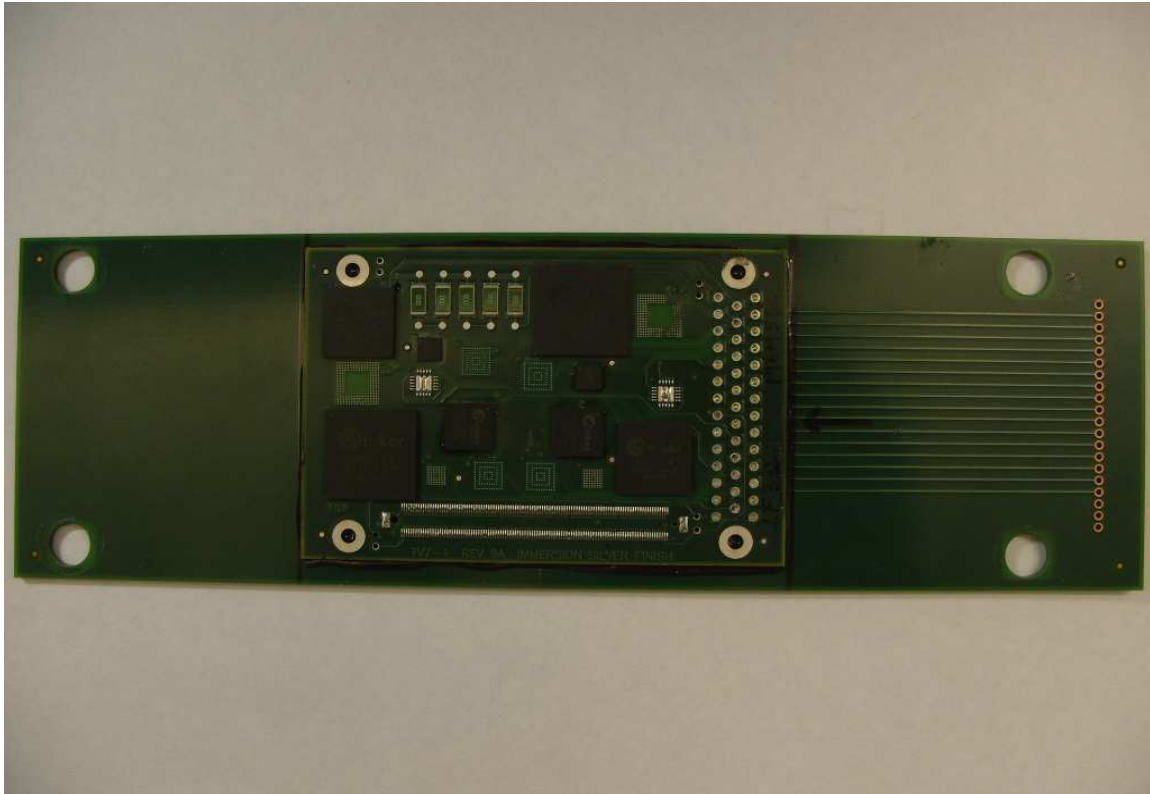


Figure 5.6 TV7 board on another PCB

## 5.5 Fastening Material

When tested with PCB as backing material, the glue which was holding the TV7 board to the other PCB gave up. This prompted to look into other formulation of glue to hold the test board. Quick drying glue was not the solution since some of the strongest glue failed. It was concluded it needed a two part epoxy to hold them together. Various two part epoxy was used but none were capable of holding up for more than 4 hours. After testing different types of two part epoxy, a suitable epoxy was identified with a cure time of 4 hours. It was Anchor Tite Automotive/RV engine gasket sealant which had a strength of 2500lbs/in and a flexibility rate of 30% elongation which was shock and

vibration resistant. The adhesive had a cure color of black. This two part epoxy was capable of surviving 10 hours of vibration at level 5 with little to no compromise in strength. It was important for the epoxy to behave uniformly for the entire length of test to be repeatable. This was checked using laser measurement system by looking into frequency of the board at it was vibrating at the 1<sup>st</sup> hour and at the 10<sup>th</sup> hour. Unfortunately Anchor had discontinued product number 15204. Thus we had to settle for a similar type of epoxy, product number 15206, which had strength of 1000 psi and was best when cured under water. It had a cure time of 4 hours, can be handled after 24 hours, but it has a full cure time of 1 week. This epoxy had a light yellow cure color and a longer cure time when cold. When tested for its durability to withstand 10 hours of vibration it developed cracks at corners by the 9<sup>th</sup> hour under machine max ranging to 2200Hz at 20G<sub>REMS</sub>.

## **5.6 Fastening and cure method**

All the TV7 test boards selected for vibration test had to be single sided since it had to be stuck to the PCB. The TV7 board had few holes close to the components, they had to be plugged in order to prevent the epoxy from seeping through the holes and make contact with the component. The same epoxy was used to plug the holes, they were applied by finger just enough to cover the hole. It was left to cure for 4 hours before being fastened to the longer PCB. The longer PCB board had holes on them and they had to be plugged by soldering to prevent the epoxy from escaping and being wasted. Both contact surfaces of longer PCB and TV7 boards were roughened with 320 grit sand paper

to create a rough surface for better result. The PCB centre was marked from the clamping points. The epoxy was mixed in batches and applied evenly on both the surfaces. Then they were mated and the curing was done in 3 phases. Phase 1: During this phase the curing for 24 hours was done at room temperature with evenly distributed weights on them. In the second phase it was cured at 55°C for 10 hours with no weights and in the 3<sup>rd</sup> phase, rest of the 134 hours was spent in room temperature. All test boards had a minimum cure time of 7 days before subjecting to vibration.

### 5.7 Displacement amplitude, peak and phase change

As the TV7 board was not designed by any standard for Vibration test, the displacement amplitude of the TV7 and the QFN boards was found. The displacement was measured using laser's and was in  $\mu\text{m}$ .

Location	Displacement Amplitude ( $\mu\text{m}$ )
A	96.12
B	77.87
C	41

Table 5.1 Displacement Amplitude of QFN

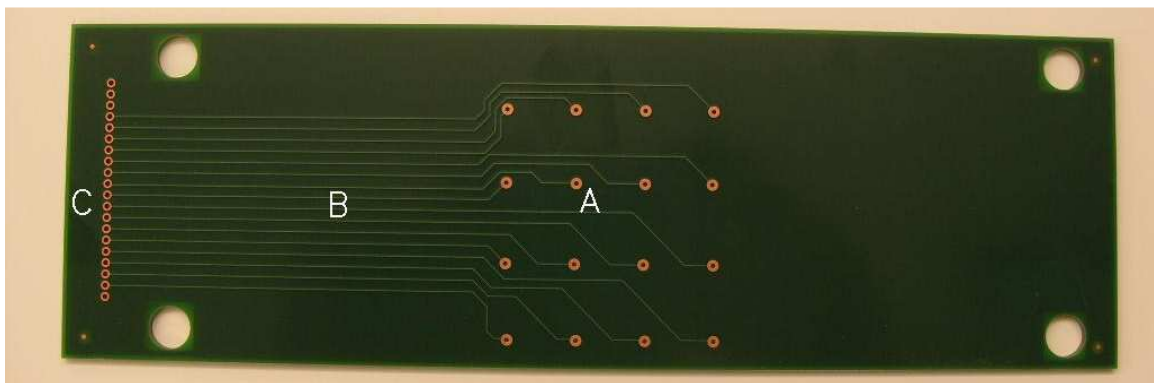


Figure 5.7 Three locations on QFN chosen

Location	Displacement Amplitude ( $\mu\text{m}$ )
A	56.18
B	52.42
C	35.2

Table 5.2 Displacement Amplitude of TV7

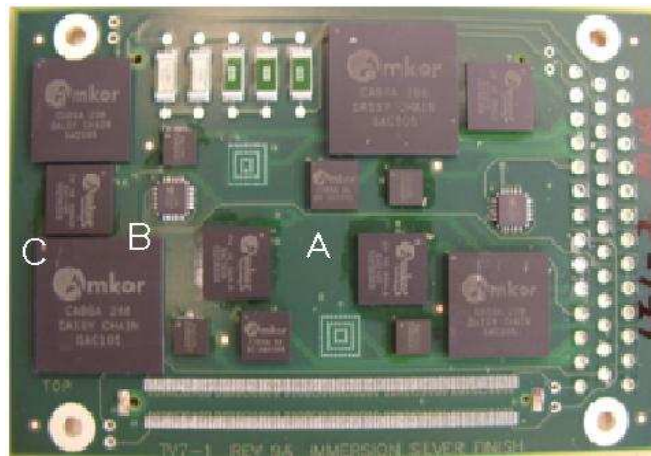


Figure 5.8 Three locations on QFN chosen

When the TV7 was used to find the phase change, there was no clear phase change; this was one of the findings which prompted to look for different solution. But when the TV7 was attached to a QFN and tested there was a phase change seen with peaks.





Figure 5.9 Laser Measurement System (a)

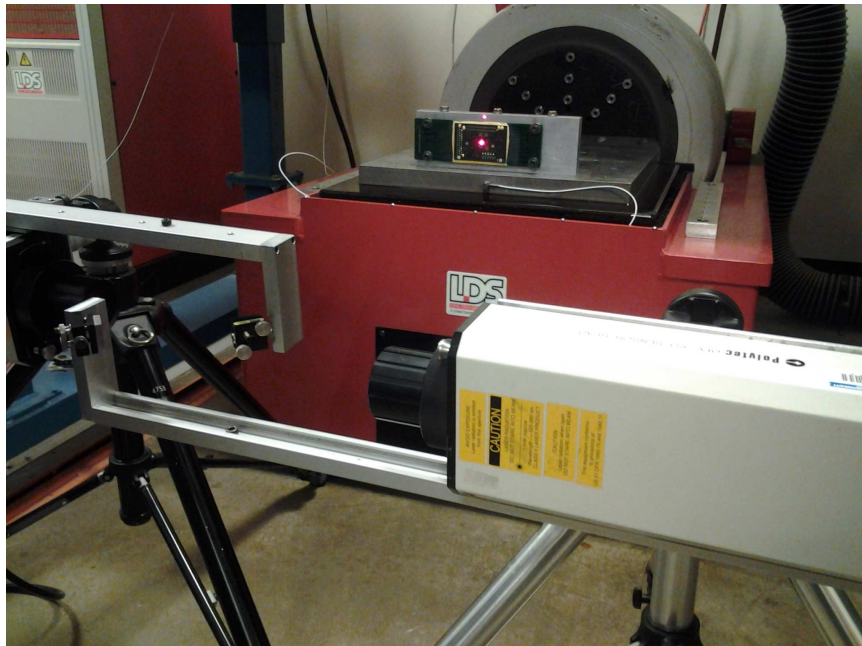


Figure 5.10 Laser Measurement System (b)

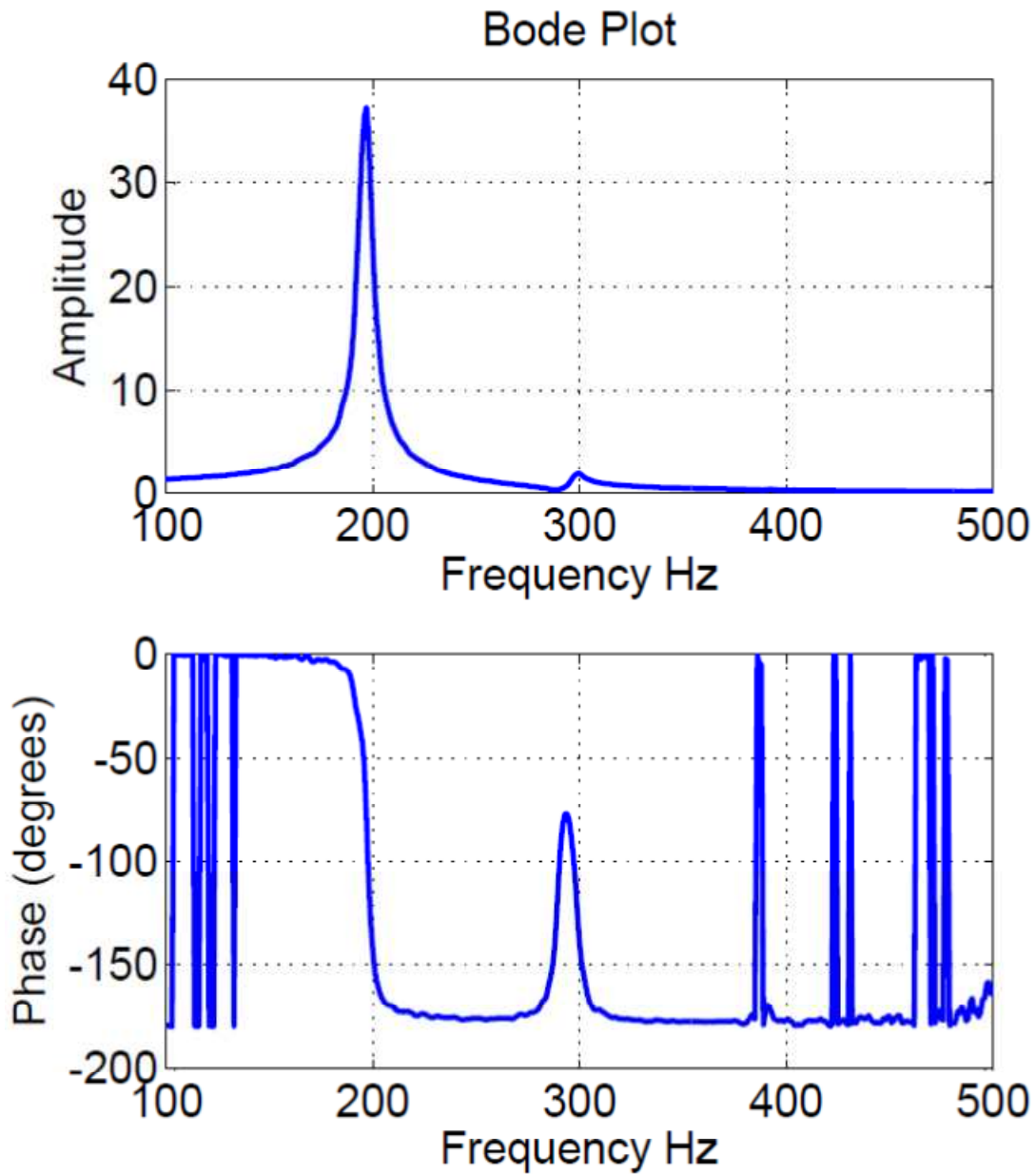


Figure 5.11 Peak and Phase change -1

From the above figure we can see there is a clear phase change of  $180^\circ$  at the peak which denotes that there is flexure of the circuit board which was not seen in just TV7 board. This phase change was confirmed by repeated tested to conform that it happens on multiple samples where the TV7 board is fixed on QFN board.



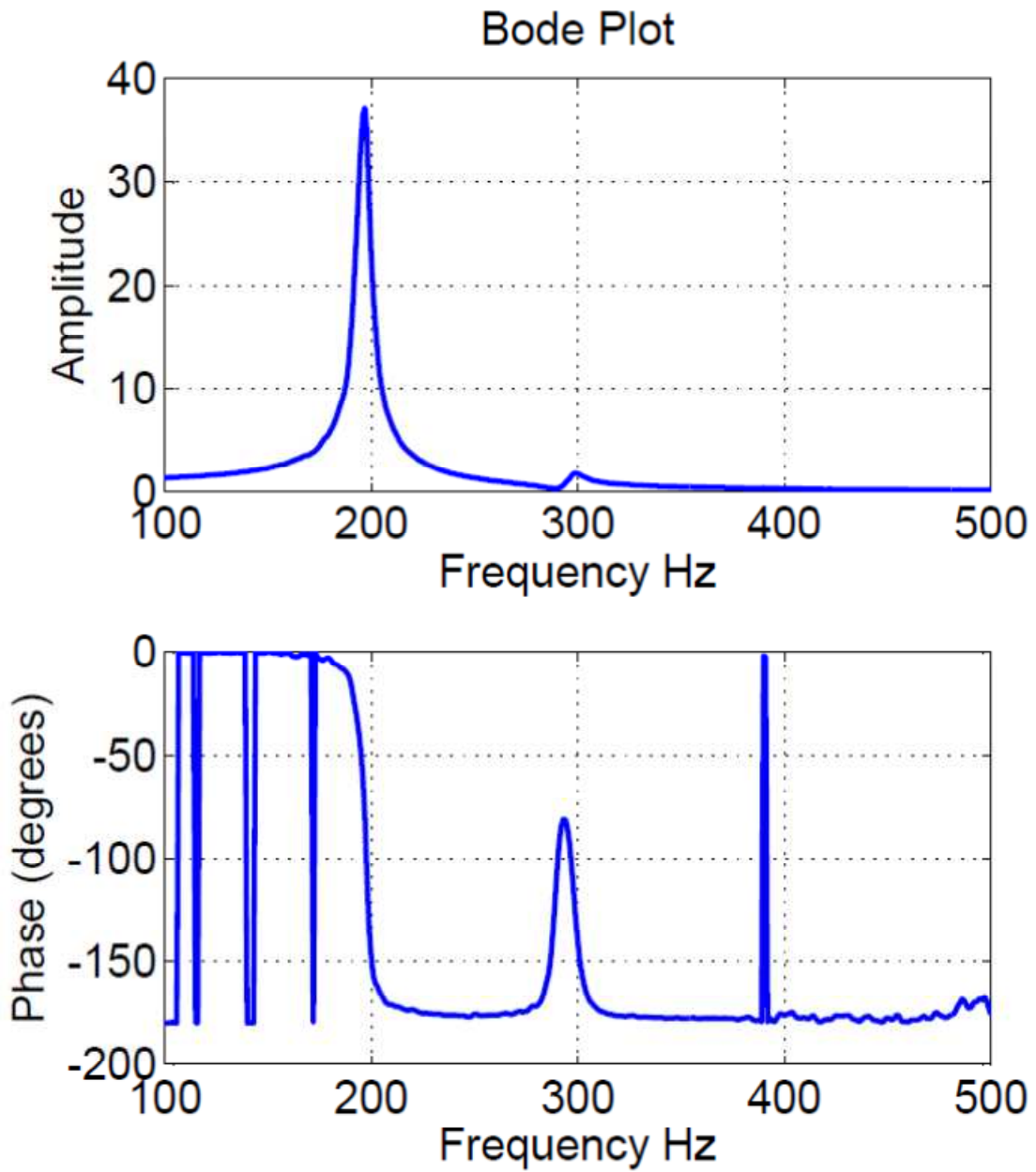


Figure 5.12 Peak and Phase change -2

## 5.8 Vibration Profile and Testing

As the original profile developed for the TV7 test boards were not capable of stressing the solder joints, MIL-STD-810F, Method 514.5 was the basis for the profile. The step stress test is much more suitable since a test conducted at  $10G_{RMS}$  would take hundreds of hours to fail the same number components through a step stress test. Moreover the 24 month ages boards would not survive that long of a test due to substrate weakening. The shape of the power spectral density curve for each stress level would excite all major resonances by random vibration input. The power spectral density curves present in the MIL-STD-810F, Method 514.5 were bases but not duplicated. There are 7 levels in the profile, each lasting 60 minutes and then moving to the next level.

Level 1	Level 2	Level 3
20-50Hz @ +6.0dB/octave	20-50Hz @ +6.0dB/octave	20-50Hz @ +6.0dB/octave
50-1000Hz@0.067G <sup>2</sup> /Hz	50-1000Hz@0.0984G <sup>2</sup> /Hz	50-1000Hz@0.134G <sup>2</sup> /Hz
1000-2000Hz @ -6.0dB/octave	1000-2000Hz @ -6.0dB/octave	1000-2000Hz @ -6.0dB/octave
2000Hz @ 0.0167 G <sup>2</sup> /Hz	2000Hz @ 0.0245 G <sup>2</sup> /Hz	2000Hz @ 0.0334 G <sup>2</sup> /Hz
Composite = 9.9G <sub>RMS</sub>	Composite = 12.0G <sub>RMS</sub>	Composite = 14.0G <sub>RMS</sub>

Level 4	Level 5	Level 6
20-50Hz @ +6.0dB/octave	20-50Hz @ +6.0dB/octave	20-50Hz @ +6.0dB/octave
50-1000Hz@0.175G <sup>2</sup> /Hz	50-1000Hz@0.2215G <sup>2</sup> /Hz	50-1000Hz@0.2734G <sup>2</sup> /Hz
1000-2000Hz @ -6.0dB/octave	1000-2000Hz @ -6.0dB/octave	1000-2000Hz @ -6.0dB/octave
2000Hz @ 0.0436 G <sup>2</sup> /Hz	2000Hz @ 0.0551 G <sup>2</sup> /Hz	2000Hz @ 0.0682 G <sup>2</sup> /Hz
Composite = 16.0G <sub>RMS</sub>	Composite = 18.0G <sub>RMS</sub>	Composite = 20.0G <sub>RMS</sub>

Level 7
50-2200Hz@0.067G <sup>2</sup> /Hz
Composite = 24G <sub>RMS</sub>

Table 5.3 Different levels of TV7 vibration profile

Above table represents the seven different levels that were used, Level 7 is different from other levels since it does not have a slope in the profile. And the frequency has been changed to cover from 50Hz to 2200Hz. This profile was included just to make sure all the frequency is covered at least for one hour at a high stress.

## 5.9 Testing

The testing was performed in batches, where each batch consisted of 6 boards. Due to the shaker table layout and the axis needed to be tested on the TV 7 board's only three fixtures could be mounted. Given the limited time to test the samples on hand, it was mounted in a way where there were two boards on each fixture, one facing the operator and the other facing the shaker. The fixture was designed to have 3 through holes to bolt the fixture to the shaker table.

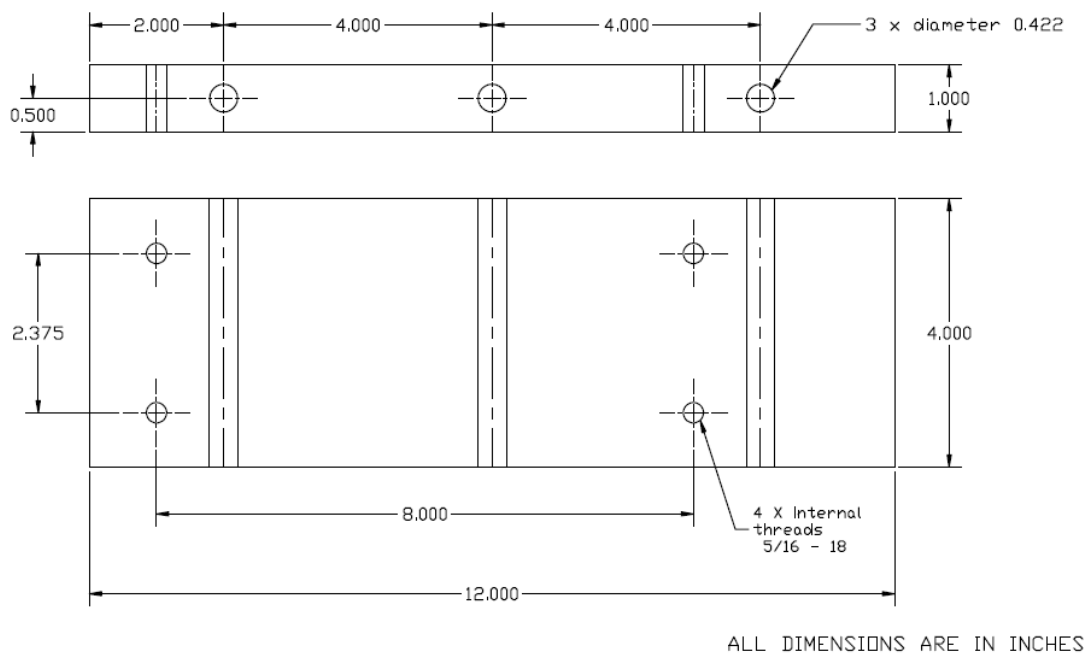


Figure 5.13 Vibration Fixture

The test boards were probed every ten minutes for the whole duration of 7 hour testing. They were probed traditionally with a millimeter and the criterion for failure was when there was a complete failure. Some components failed but their circuit closed in the later part of the test, but the failure occurrence was recorded when they failed to pass the criteria the first time.

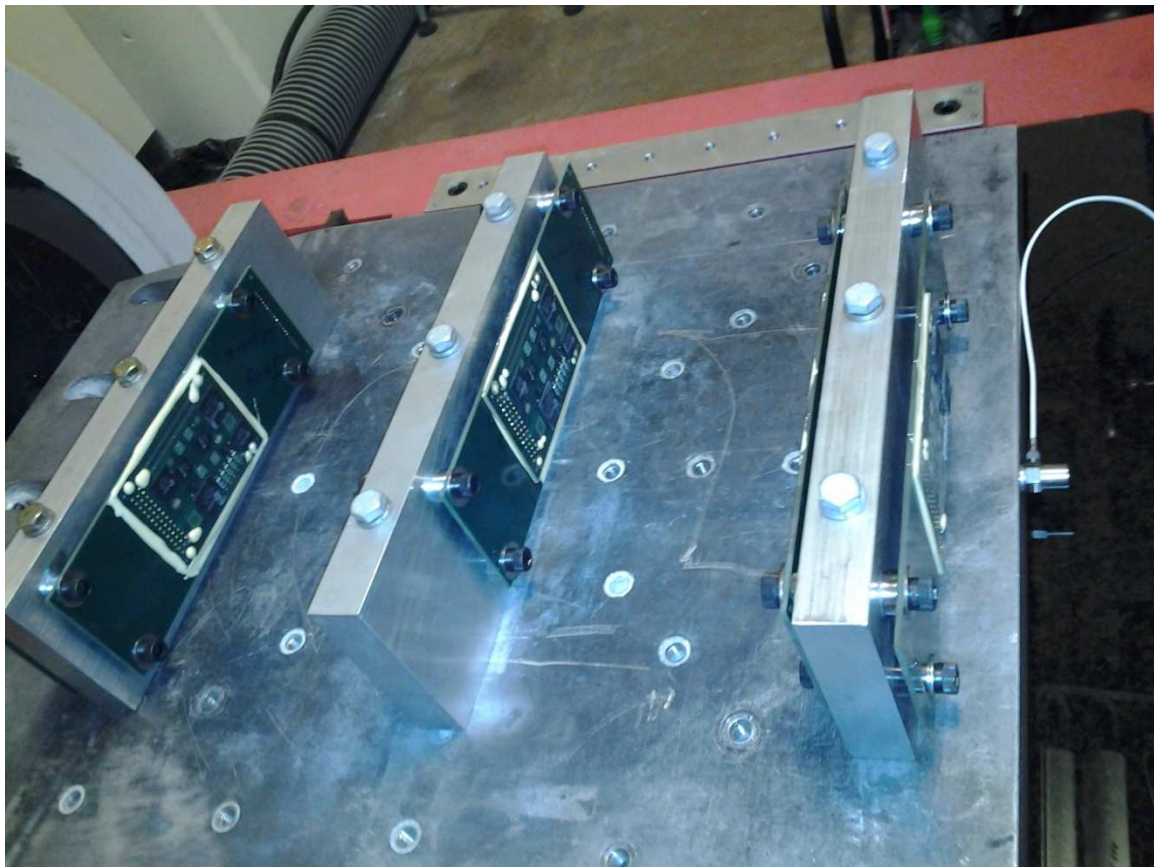


Figure 5.14 Vibration setup

## 5.10 Characteristic life of SAC105, SAC305 and SnPb

For comparing the performance of the solder joints after aging, the baseline should have been solder joints subjected to similar environment with no time spent at 55°C, but due to unavoidable circumstances, the 6 month aged samples are considered as baseline for comparison.

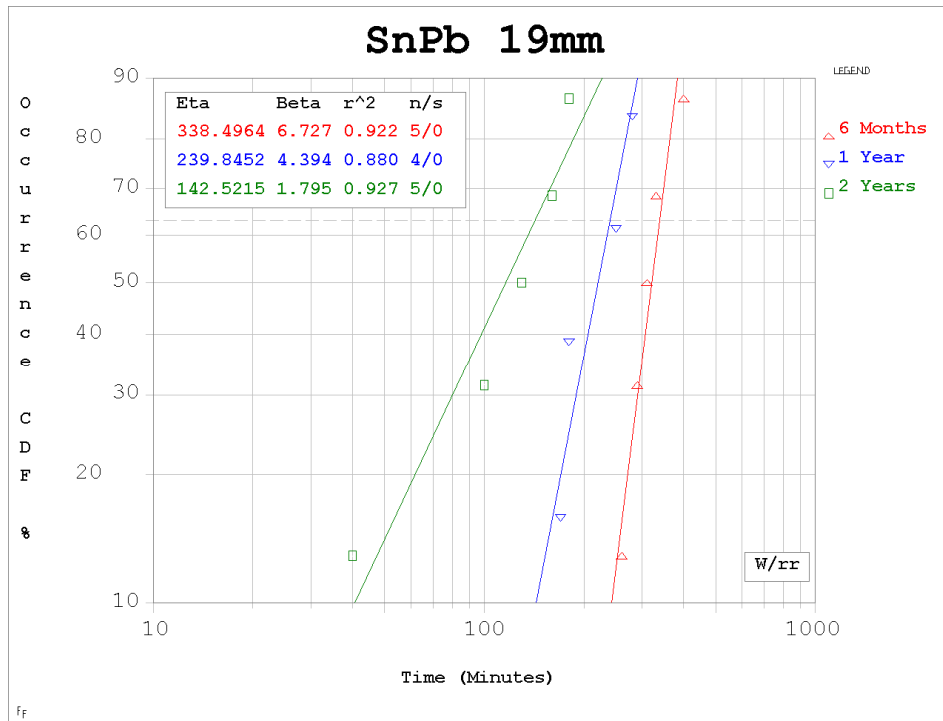


Figure 5.15 SnPb 19mm Weibull plot

When comparing the 19mm packages of the tin-lead paste from Figure 5.15, it can be seen that the 55C aging has a negative impact on the joints. Considering the 6months as baseline, there is a deterioration in characteristic life of 29.14% after 12 months of aging and 57.89% after 24 months. The deterioration between 12 and 24 months is 40.57%. There is a greater rate of degradation in characteristic life between 12 and 24 than 6 and 12 months of aging.

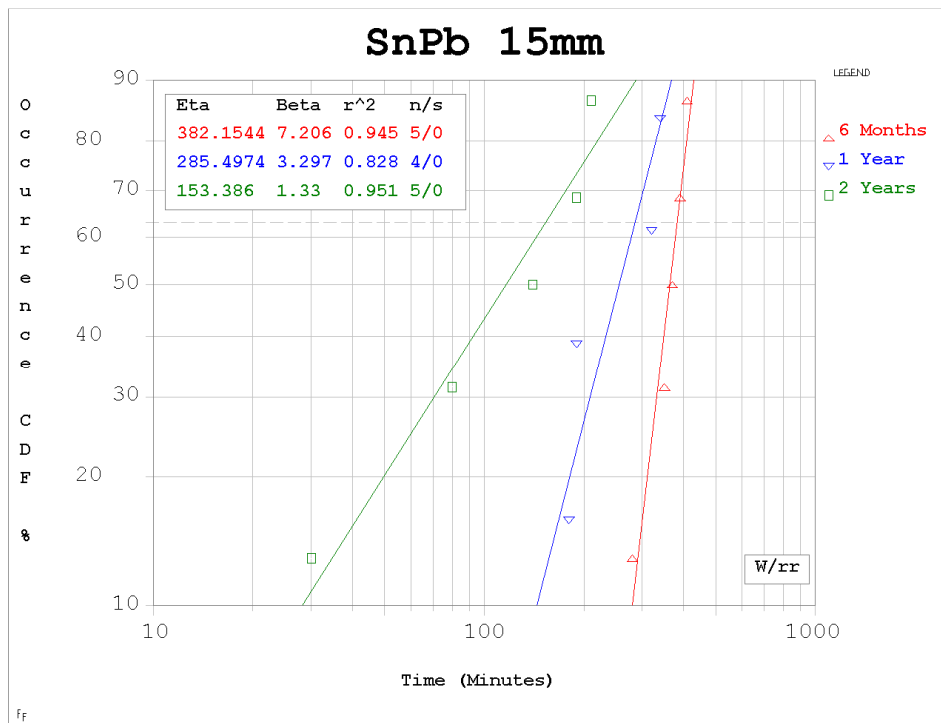


Figure 5.16 SnPb 15mm Weibull plot

In the 15mm packages from Figure 5.16, similar effect is observed. 25.29% degradation in characteristic life is observed between 6 and 12 months. Between 12 and 24 months it is found to be 46.27% which is in line with 19mm packages. Comparing with 6 months after 24 months there is a degradation of about 59.86%. Due to the design issue with the 10mm package, the comparison is not possible. In the 6 months aged boards, there were no failures of 5mm packages, but there was a difference of 5.56% between the 12 and 24 month aged boards. Which is very significantly less and only a total of 4 part failures were observed at 12 months and 6 at 24 months.

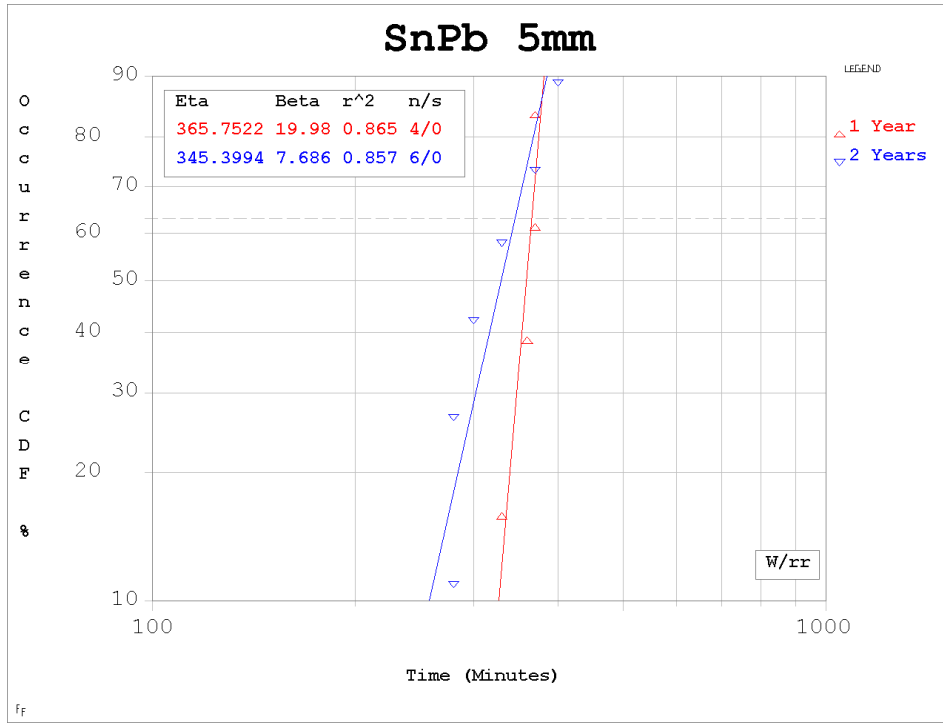


Figure 5.17 SnPb 5mm Weibull plot

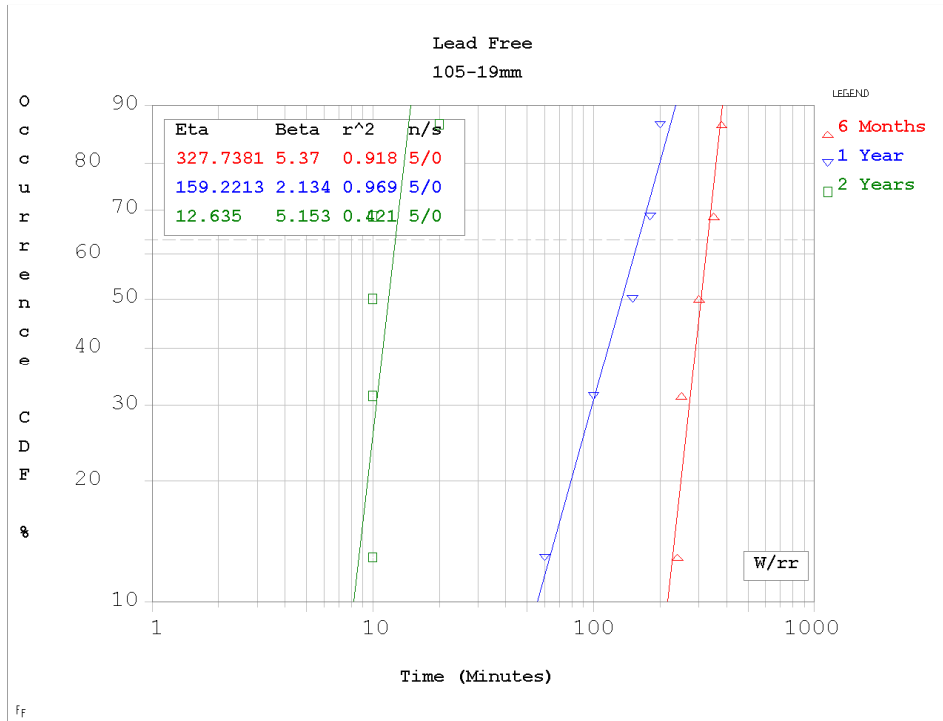


Figure 5.18 SAC105 19mm Weibull plot

Looking at lead free solders performance for the similar environment and aged boards, a huge difference is observed, the characteristic life of SAC 105 19mm packages characteristic life dropped from 327.73 minutes at 6months to 159.22 minutes at 12months and worse to 12.64 minutes at 24months. A percentage difference of 51.41% in characteristic life is observed between 6 and 12 months and 92% between 12 and 24 months. It is to be noted that the drop in reliability is 96% between 6 months and 24 months.

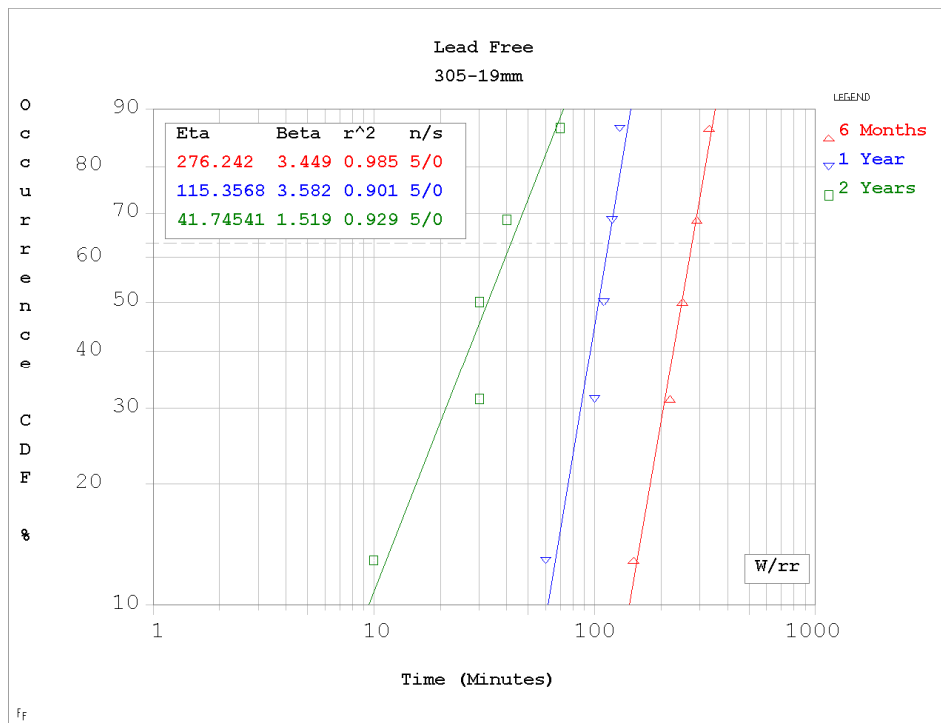


Figure 5.19 SAC305 19mm Weibull plot

In Figure 5.19, comparing SAC305 19mm package, the degradation of characteristic life from 6 months to 12 months is 58.24% while the drop between 12 and 24 months is 63.81%. But the degradation of characteristic life from 6 to 24 months is 84.88% which is a good 12% less than SAC105's performance for the same time period.



Comparing the SAC105 15mm package at different aging in Figure 5.20, a similar pattern is found in relation to the SAC105 19mm package. The characteristic life is reduced by about 35.53% between 6 and 12 months, 85% between 12 and 24 months while 90.36% at 24 months from 6 months.

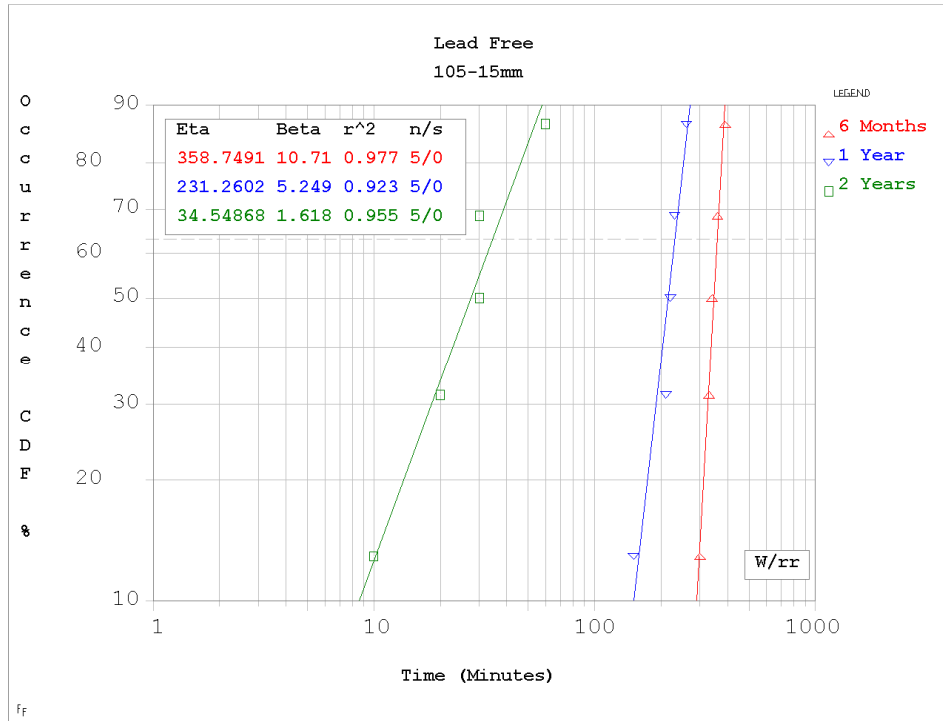


Figure 5.20 SAC105 15mm Weibull plot

Comparing the SAC305 15mm package at different aging in Figure 5.21, at 12 months the characteristic life dropped by 35.61% from 6 month, which is the same amount for SAC105 15mm package. At 24 months the rate of deterioration from 6 months is 67.66%.

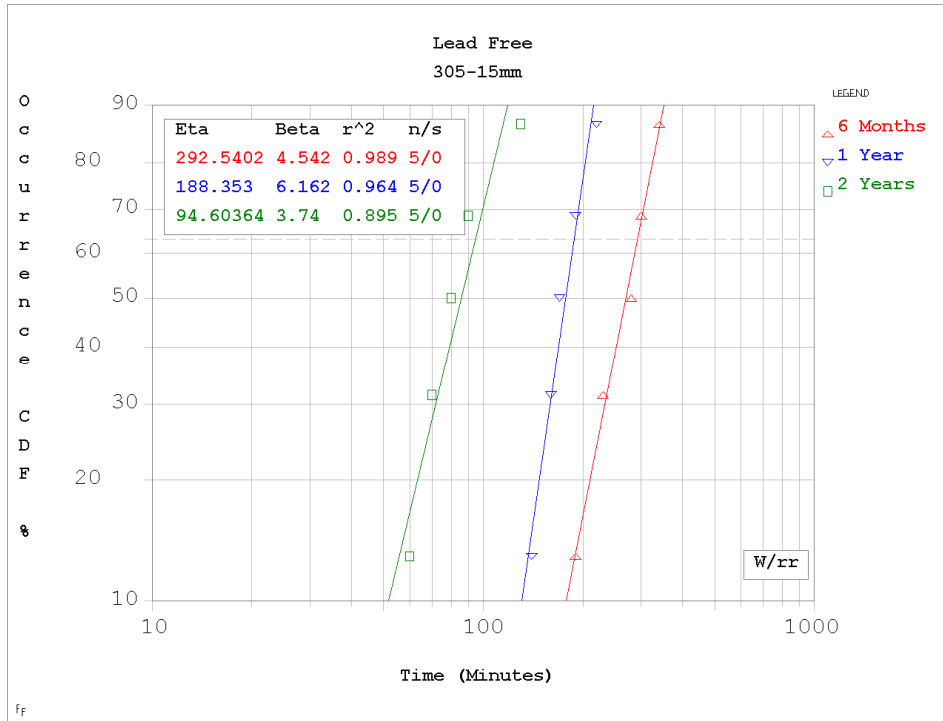


Figure 5.21 SAC305 15mm Weibull plot

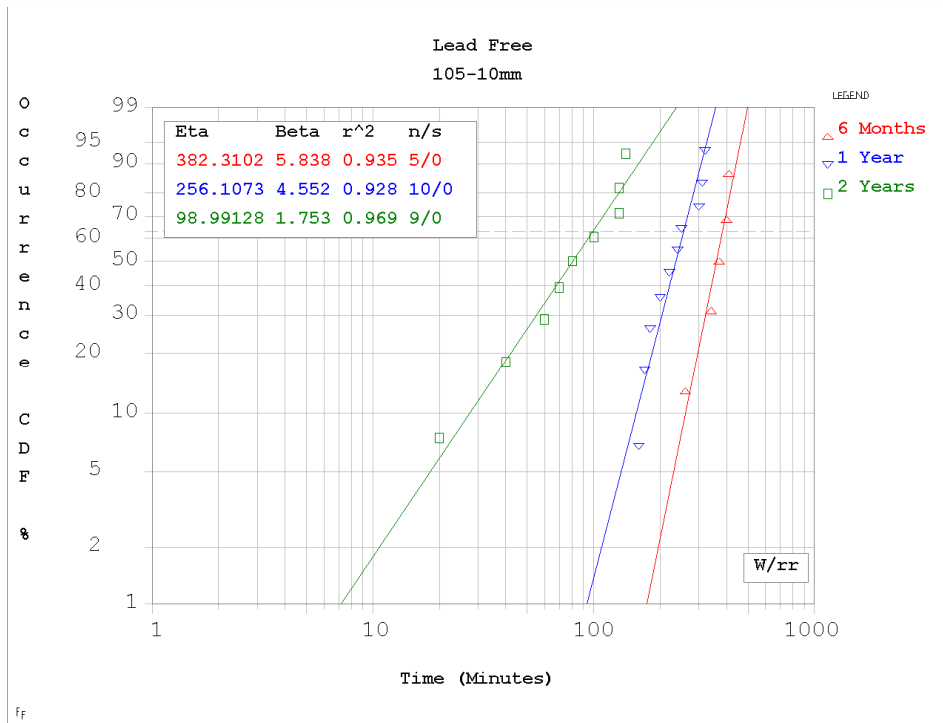


Figure 5.22 SAC105 10mm Weibull plot

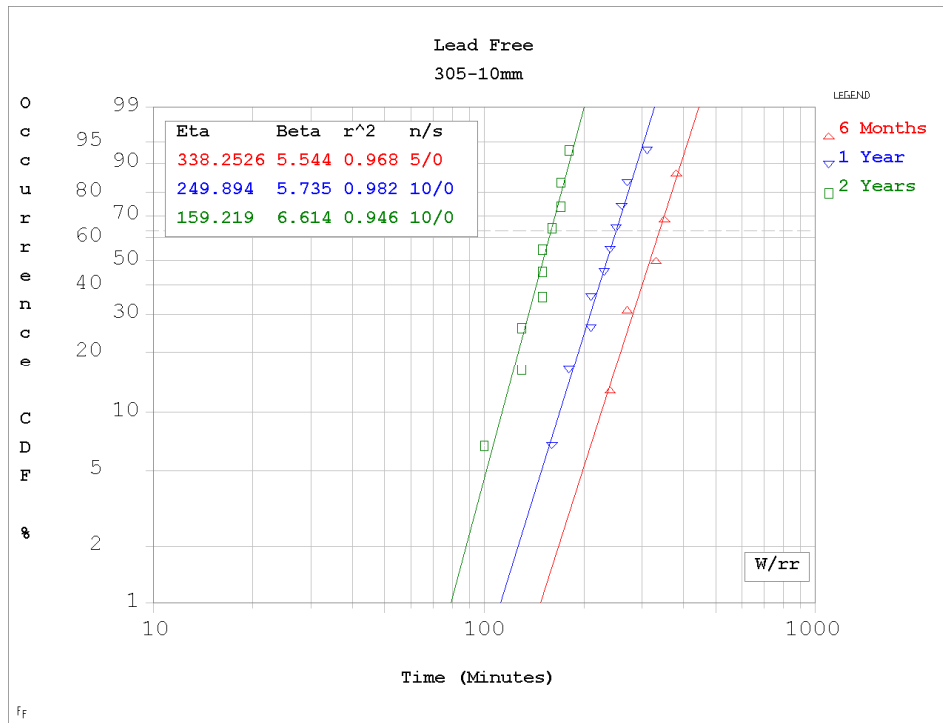


Figure 5.23 SAC305 10mm Weibull plot

Comparing SAC105 10mm packages in Figure 5.22, the characteristic life is reduced by 33% from 6 to 12 months, and a 61.34% from 12 to 24 months, while 74.1 is the change in characteristic life between the 6month and 24 month solder joint performance. Similarly in SAC305 packages, characteristic life is reduced by 26.12% between 6 months and 12 months while 36.28% between 12 and 24 months. An overall drop of 52.92% is seen between 6 months and 24 months. The 5mm packages had no failures at 6 and 12 months, with very few failures at 24 months, the only a reasonable way of looking at them is a comparison between SAC105 and 305 at 2 years. There is a 11% characteristics life time difference, SAC 305 being better.

## 5.11 Deterioration rate of SAC105 VS SAC305

It can be seen that the SAC105 and SAC305 deteriorate at different rates. To start off, SAC105's performance is better at 6 months and the rate of drop in reliability is much higher than that of SAC305. It can be observed that the SAC305 out performs SAC105 at 24months.

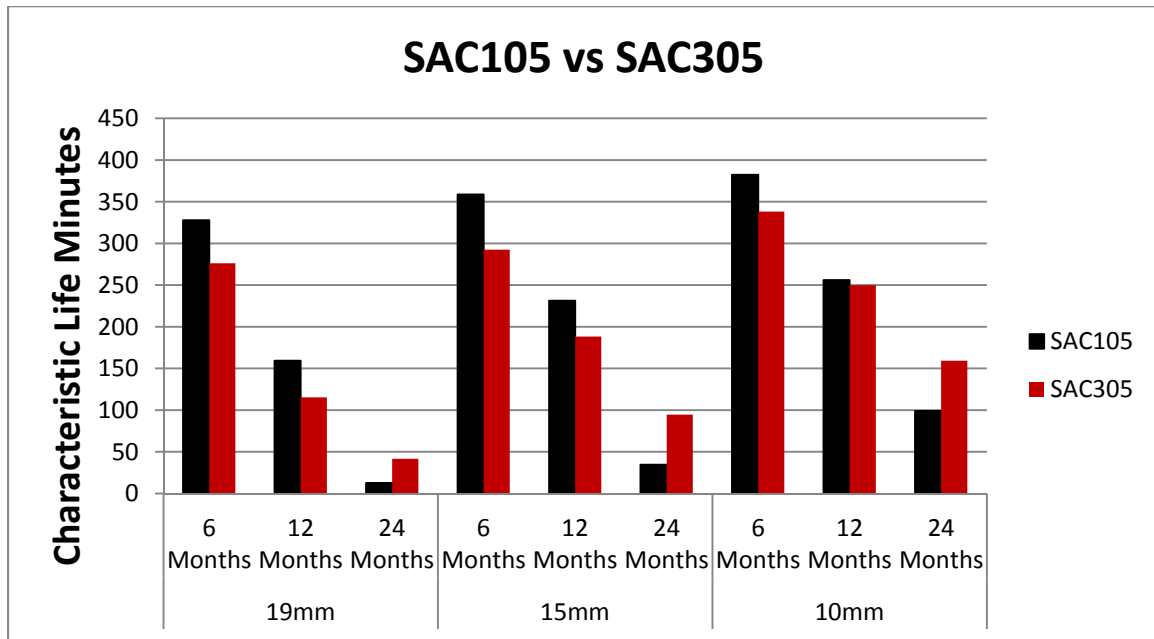


Figure 5.24 Deterioration of SAC105&305 at 6, 12 and 24 months

It is can be observed in the 19mm packages as well in the 15mm packages where SAC305 has a better characteristic life than that of SAC105 at 24 months and not 12 months. In the 10mm packages the crossover where the life characteristic of SAC 305 is on par with SAC105 is at 12 months and at 24 months SAC305 has a clear advantage.

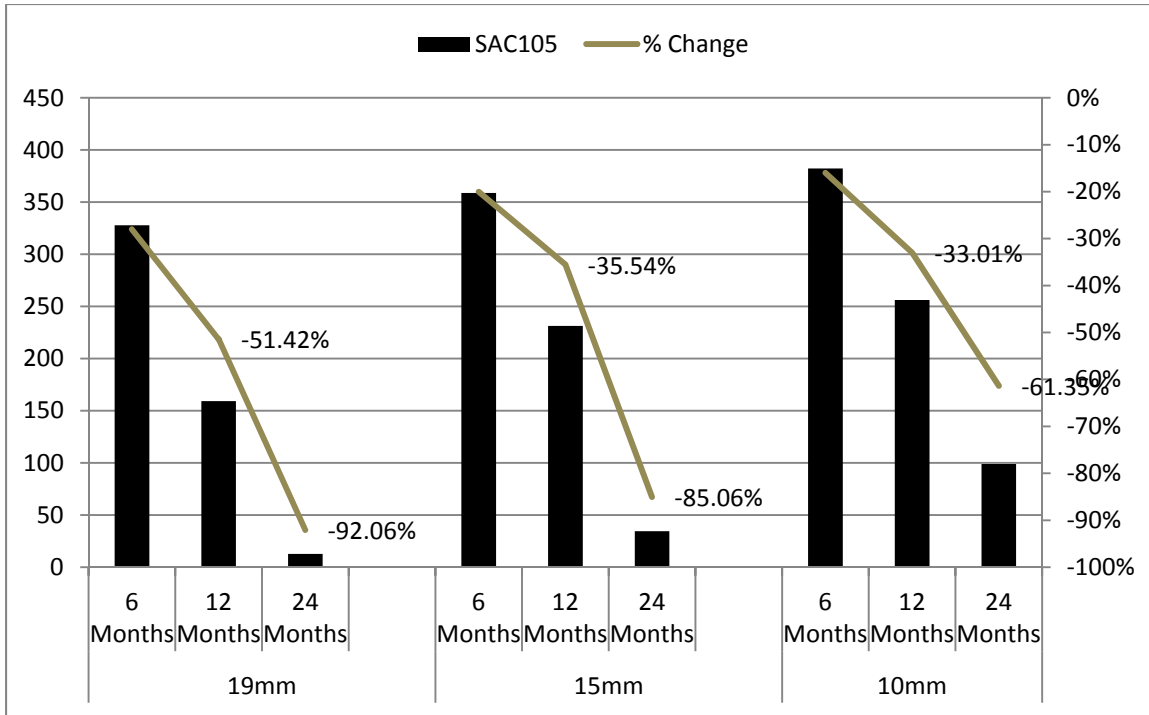


Figure 5.24 Percent Deterioration of SAC105

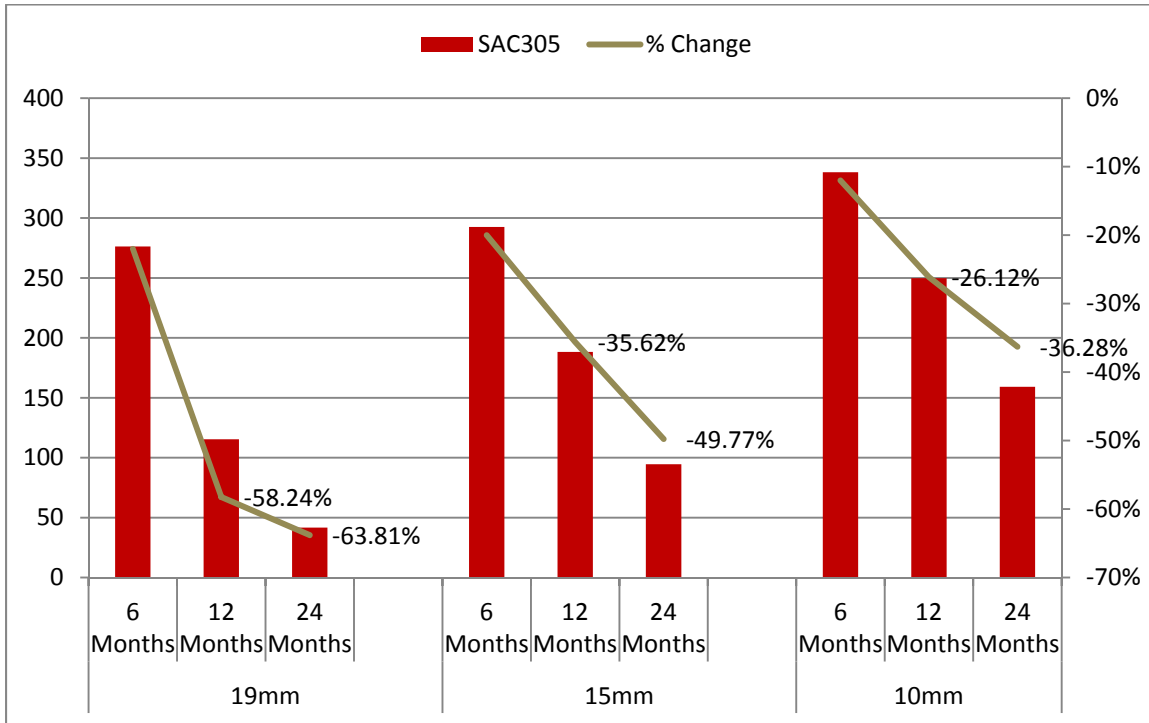


Figure 5.24 Percent Deterioration of SAC305

## 5.12 Failure mode

The cross sections of the samples revealed that the cracks occur at the intermetallics. Interestingly majority of the cracks were present at the intermetallics of chip and solder ball contrary to the pad and solder ball intermetallics, but there were instances where cracks of both types were found adjacent to each other. They are shown in Figure 5.25 & 5.26 for 19mm SAC 105 package and in Figure 5.27 & 5.28 for 19mm SAC 305 package.

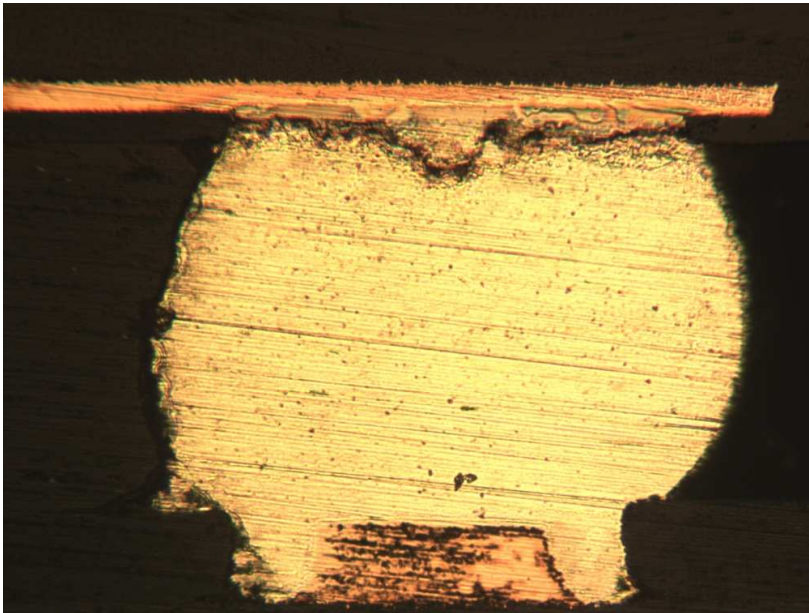


Figure 5.25 24 month aged 19mm SAC 105, crack at chip

From the cross sections it is seen that the failure mode is consistent irrespective of the solder joint, these mode have already reported, it is to be noted that in SAC 105 the crack propagation is more in bulk solder than at the Intermetallic which is the case in SAC 305.

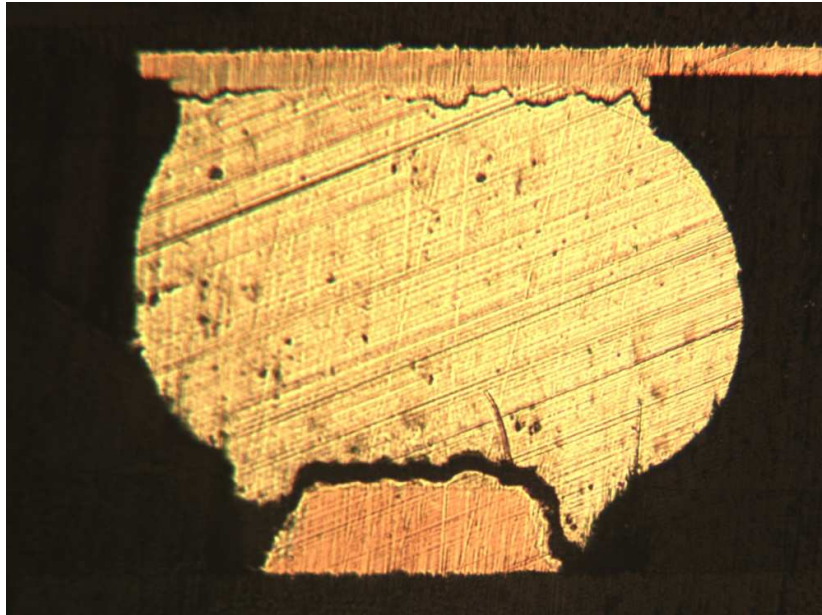


Figure 5.26 24 month aged 19mm SAC 105, crack at pad

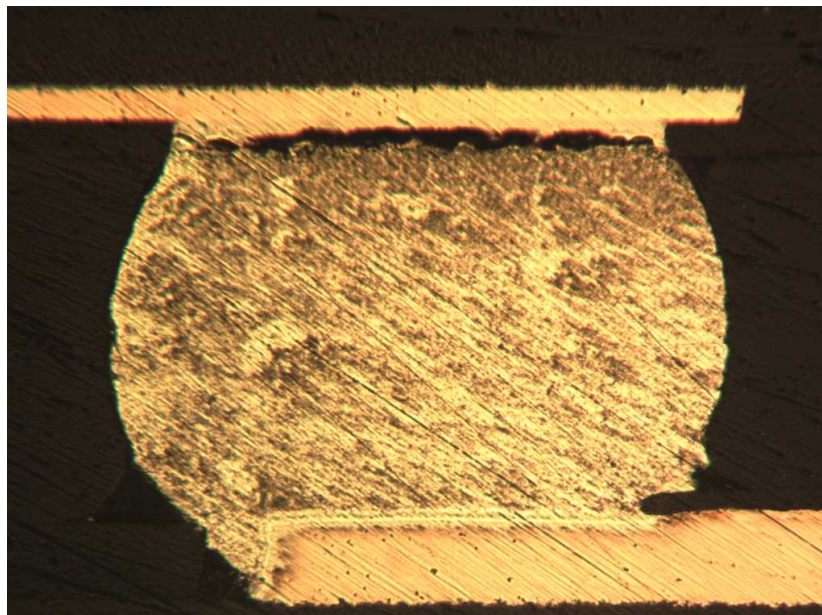


Figure 5.27 24 month aged 19mm SAC 305, crack at chip

The crack propagation in SAC 105 is more complex than SAC 305. This could be due to the low elastic modulus of SAC 105. Low silver alloys were designed specifically to enhance the stress performance through higher plastic energy dissipation ability. Low



elastic modulus of SAC 105 leads to high plastic energy dissipation in the solder during crack propagation, though the crack may not propagate in the solder, the plastic deformation in the adjacent solder will take up more energy during interfacial crack propagation. The higher stress performance of low silver solder is credited to plastic energy dissipation ability and increased bulk compliance.

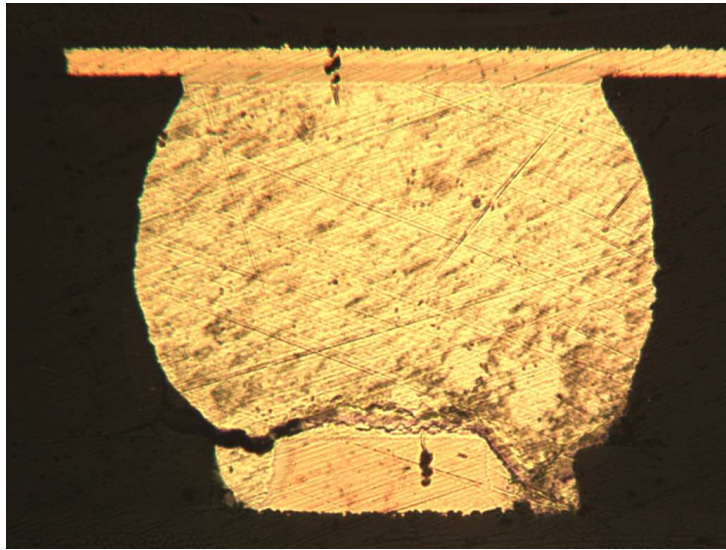


Figure 5.28 24 month aged 19mm SAC 305, crack at pad

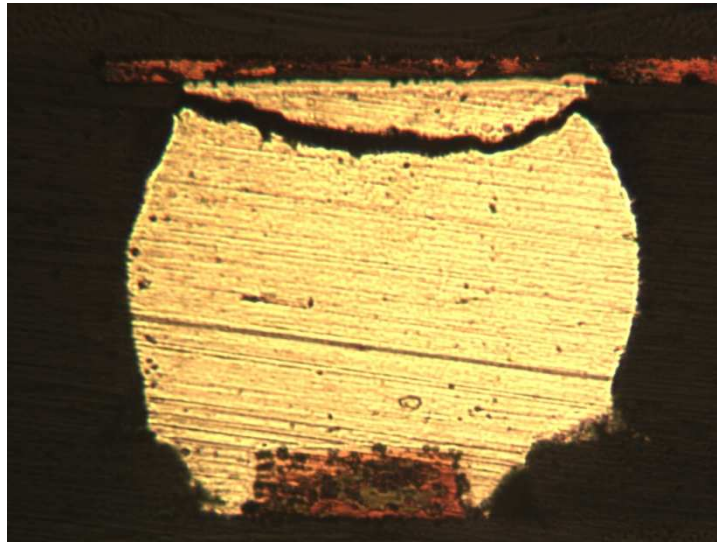


Figure 5.29 24 month aged 19mm SAC 105, crack in bulk solder



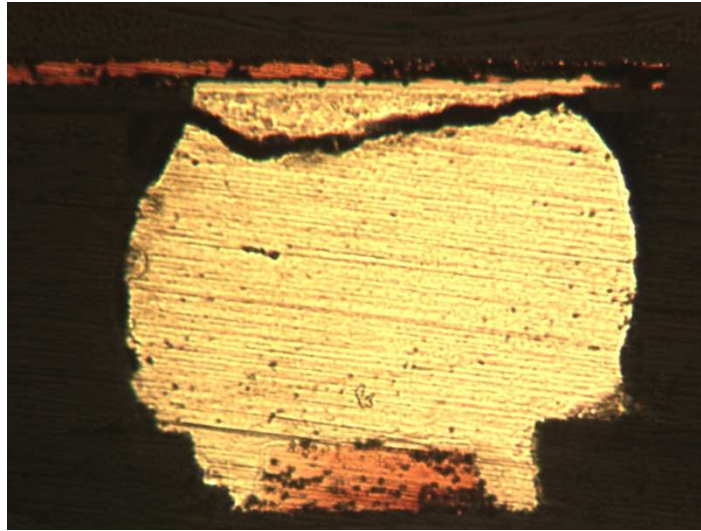


Figure 5.30 24 month aged 19mm SAC 105, crack in bulk solder -2

Solder	Elastic Modulus E [GPa]	Tensile Strength [MPa]	Elongation [%]
SAC 105	47	45	46
SAC 305	51	53	46
SAC 405	53	53	35

Table 5.4 Material Properties of SAC alloys

The outcome of the test is that there is a change in the behavior of SAC 105 when aged and SAC 305 turns out to be better than SAC 105 after 2 years of aging though SAC 105 was believed to be better for the application due to the lower percentage of Silver which would make the SAC 105 softer than SAC 305 to accommodate the stress caused in the application. The crack initiation points and direction within the solder joint are dependent on the location and type of package.

### 5.13 Vibration vs Thermal performance of SAC105 and 305

In Thermal cycling test, different aging temperatures were taken into account, but for mechanical tests only 55°C was chosen. Hence, in order to make a comparison, data of ImAg and SnPb boards, aged at 55°C are compared with the same. In thermal cycling test, data is available for no aged, 6 months and 12 months.

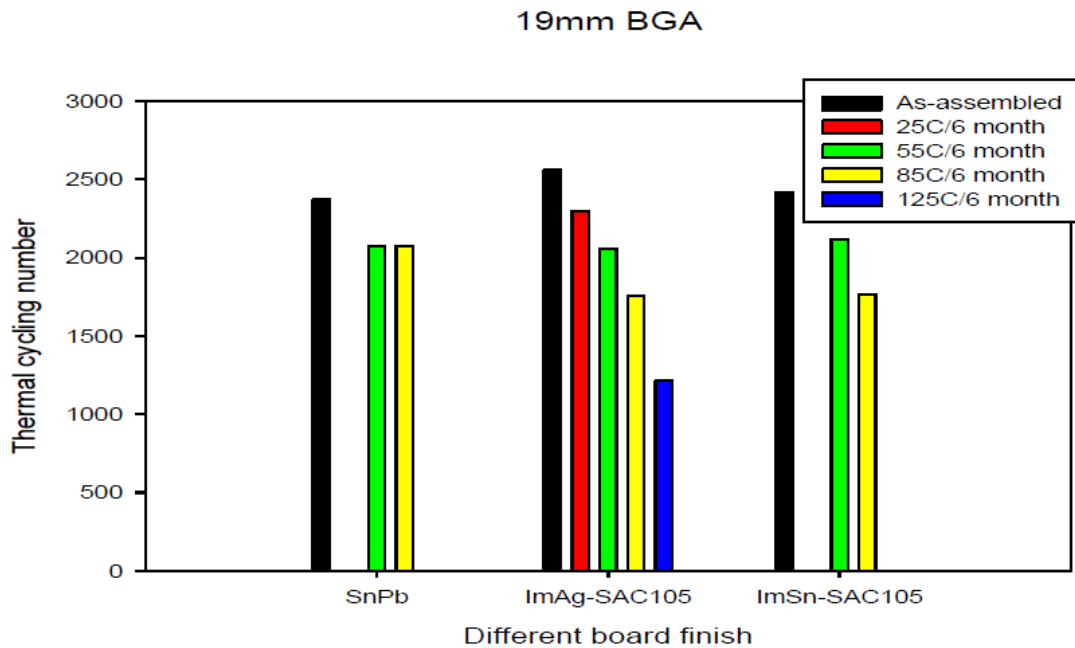


Figure 5.31 Weibull Characteristic lifetime at different aging conditions for 19mm SAC105 BGA

It can be observed that the SAC305 is better than the SAC105, the degradation is much more pronounced at a higher temperature than at lower temperature, but a general trend can be seen in SAC alloys but not so evident with SnPd solders. It is a trend irrespective of the plating finish it can be seen.

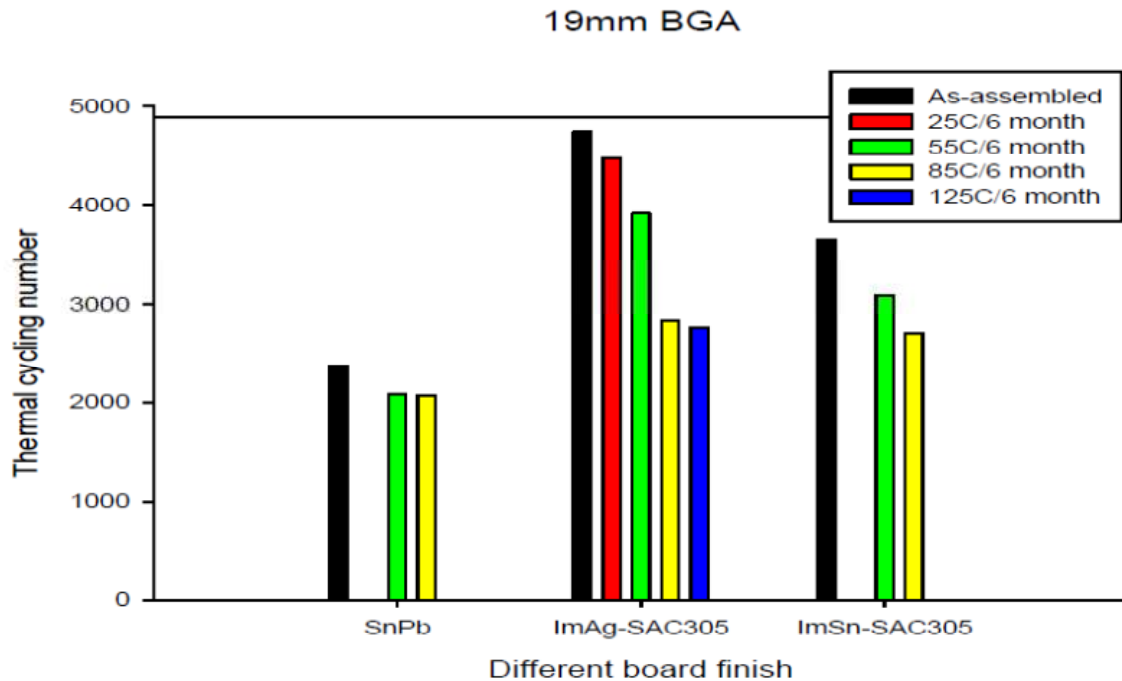


Figure 5.32 Weibull Characteristic lifetime at different aging conditions for 19mm

#### SAC305 BGA

By comparing the vibration and thermal cycling side by side for ImAg board finish aged at 55°C where the thermal cycling was carried out between -40°C and 125°C with 30 minute ramp and 15 minute soak time, the SAC 305 performs better than SAC105 and no major trend in cross over taking place.

The pattern observed is in vibration the SAC305 gains on aging and has better reliability, but in thermal cycling the SAC305 consistently has a better performance than the SAC105, traditionally SAC 305 are designed for thermal applications and low Ag solder like the SAC105 is designed for shock and vibration applications.

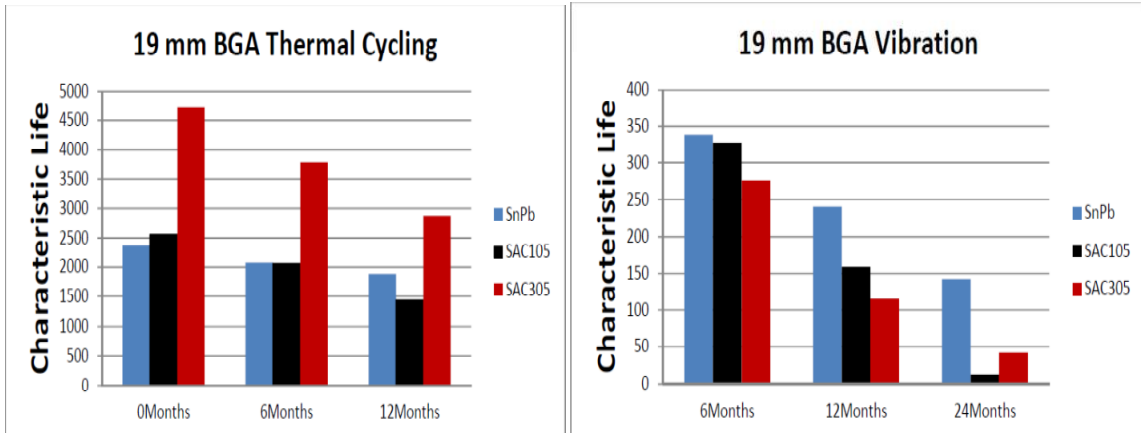


Figure 5.33 Weibull Characteristic lifetime of 19mm BGA Thermal vs Vibration

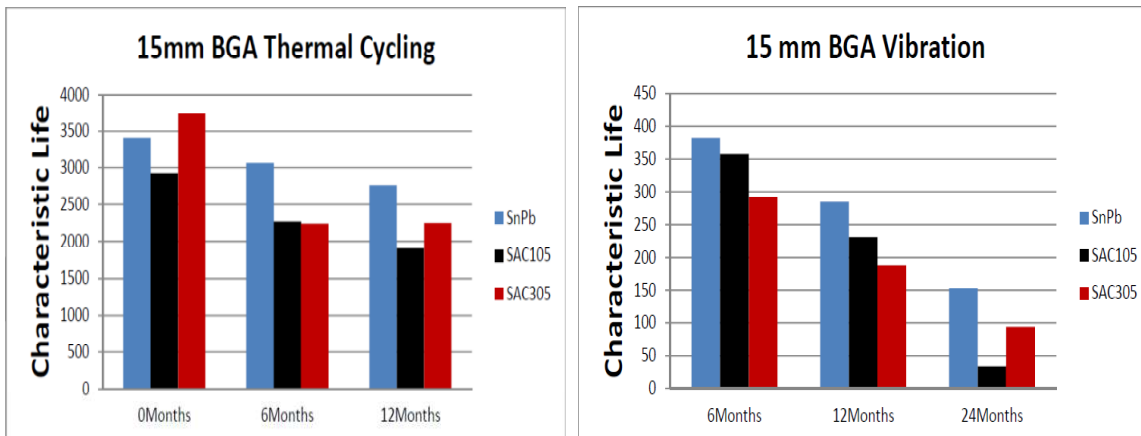


Figure 5.34 Weibull Characteristic lifetime of 15mm BGA Thermal vs Vibration

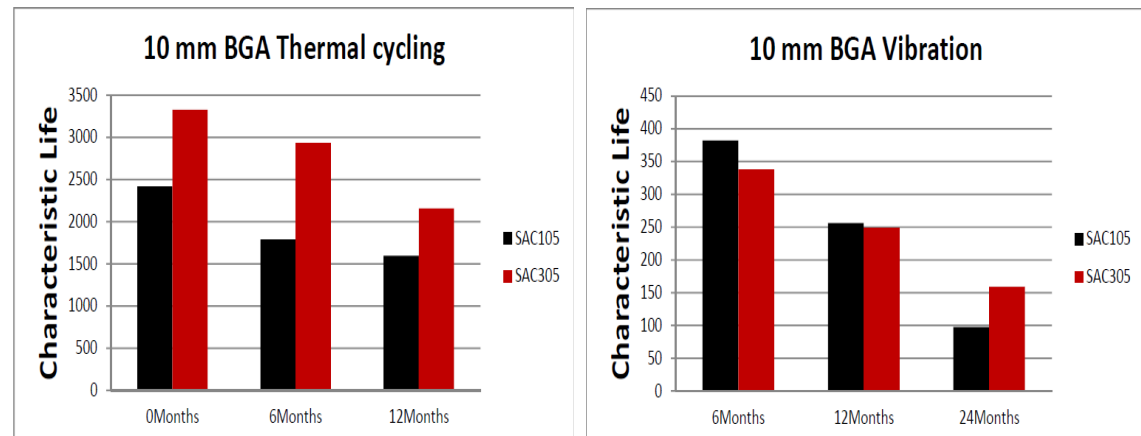


Figure 5.35 Weibull Characteristic lifetime of 10mm BGA Thermal vs Vibration

Percentage difference in Characteristic life Vibration vs. Thermal cycling.		19mm			15mm			10mm		
		0-6 Months	6-12 Months	12-24 Months	0-6 Months	6-12 Months	12-24 Months	0-6 Months	6-12 Months	12-24 Months
Vibration	SnPb	-	29%	41%	-	25%	46%	-	-	-
	SAC105	-	51%	92%	-	35%	85%	-	33%	62%
	SAC305	-	58%	64%	-	36%	50%	-	26%	36%
Thermal Cycling	SnPb	12%	9%	-	10%	10%	-	-	-	-
	SAC105	20%	30%	-	22%	16%	-	26%	11%	-
	SAC305	20%	24%	-	40%	2%	-	12%	27%	-

Figure 5.36 Percentage differences of Weibull Characteristic lifetime Thermal vs Vibration for ImAg plated boards aged at 55°C

When comparing the percentage drop in Characteristic life time it can be seen that the drop in life time for vibration is much higher than the thermal cycling though there is step stress profile adapted for vibration test. It can be seen that the drop in characteristic life slows down in the Thermal cycling for 6 to 12 months than the 0 to 6 months. Looking at 6 to 12 month drop, the percent drop of SAC305 is less than SAC105; the SAC 305 seems to be affected less by aging.

The matrix is incomplete for many reasons, the 0 – 6 months data on the vibration are not present because of the design issue they had to be mounted on back of a larger board for the test to be performed. Since no aged boards are populated on both side of the TV7 it is not possible to mount them on the backing board. The 10mm SnPb data is not present because of the patten issue in the components; they are not present for Vibration Thermal Cycling. In the Thermal cycling test the 12 to 24 month data is not present since the test for 24 month aged boards have not started yet. Once they are filled in it would yield a better comparison of the rate of deterioration.

	6Months		12Months		24Months	
	$\eta$	1st failure	$\eta$	1st failure	$\eta$	1st failure
19 MM						
SnPb	338.49	260	239.84	170	142.52	40
SAC105	327.73	240	159.22	60	12.635	10
SAC305	276.242	150	115.35	60	41.74	10

Table 5.1 19mm first failure

Looking at the first failure, there a dramatic decrease in the time taken for the first failure at time progresses, another difference is the time taken for the first failure between the SAC105 and SAC305.

	6Months		12Months		24Months	
	$\eta$	1st failure	$\eta$	1st failure	$\eta$	1st failure
15 MM						
SnPb	382	280	285	180	153	30
SAC105	358	300	231	150	34	10
SAC305	292	190	188	140	94	60

Table 5.2 15mm first failure

	6Months		12Months		24Months	
	$\eta$	1st failure	$\eta$	1st failure	$\eta$	1st failure
10 MM						
SAC105	382	260	256	160	98	20
SAC305	338	240	249	160	159	100

Table 5.3 10mm first failure

From table 5.1, 5.2 and 5.3 time taken by the SAC305 to yield a failure at 24 months is considerably higher than that of SAC105; moreover, the total time taken for the failure had rapidly reduced.

# Chapter 6

## Shock Testing

### 6.1 Introduction

The drop reliability performance of Lead free solders have been one of the key focus for mobile and handheld electronic products as Lead Free typically show increased brittle solder joint failures than that of Tin-Lead solders. The development of newer technologies and press for smaller gadgets had placed a higher demand on the enhanced performance and improved reliability. The smaller size requirements have made electronics appliances more susceptible for shocks. There are various test methods for studying the impact response such as product level drop, board level drop, component level strength test and so forth. There are extensive research investigating the effect of surface finish, different composition of lead free solder and both on the reliability of lead free solders. The board level reliability is shown to be better with low Ag content solder.

Wong et al. [133] numerically investigated three significant factors that contribute towards the solder joint failure. 1) Out of plane bending causing normal and shear stresses in the interconnects, 2) inertial forces, and 3) shock stress waves transmitted due to impact. Inertial forces play an important role if the mass of the components is large; otherwise, the PCB bending dominates and constitutes the primary source of failure. Roggeman [134,135] presented a comparative study of various SAC (105, 205, 305 and 405) and Sn-Pb alloys, and concluded that impact reliability decreases as we go up the

SAC family in terms of silver content, except for certain special cases with specific pad metallurgy on each side of the joint.

## **6.2 Shock Setup**

To test the TV7 test boards Lansmont M23 drop tester was used. Initial testing was done to check the receptivity of the machine as it was moved from Henkel facility and installed at Auburn University. This was done when the desired g force of 1500 was attained at 0.5ms impact width, 20 consecutive measurements were taken. The 20 readings have a range of 49g's. This was only 4% of indented profile since it has to be taken into account that regular news paper was used to vary the pulse width of 0.5ms. The standard impact of 1500g's with a shock period of 0.5ms was according to the JEDEC spec JESD22-B111. Standoffs and screws were also according to the standards. The drop fixture was designed in a way to handle 6 test vehicles at a time to reduce the time incurred in testing. The test fixture is as shown in figure 6.2.

## **6.3 Shock Test Procedure and observation**

The test boards were subjected to 1500g's for a total of 50 drops and then the g force was increased to 2000g's for another 50 drops, finally it was subjected for 50 more drops at 2900g's. The test boards were probed with a regular millimeter at a interval of 5 drops. During initial testing the failures happened just before the components fell off the board. It was observed that the daisy chain was ripped off from the substrate. The bigger components fell off first followed by the next smaller package. But the pattern of having the daisy chain intact was seen for all the components irrespective of the package size.



The components facing the drop were the first to fall off followed by the packages on the side facing away from the direction of the drop. It could be identified from the type of failures attained that the solder joints were not being subjected to stress since the prime objective is to study the behavior pattern of these alloys under different aging time. The parts which were ripped off the board are shown in figure 6.1.

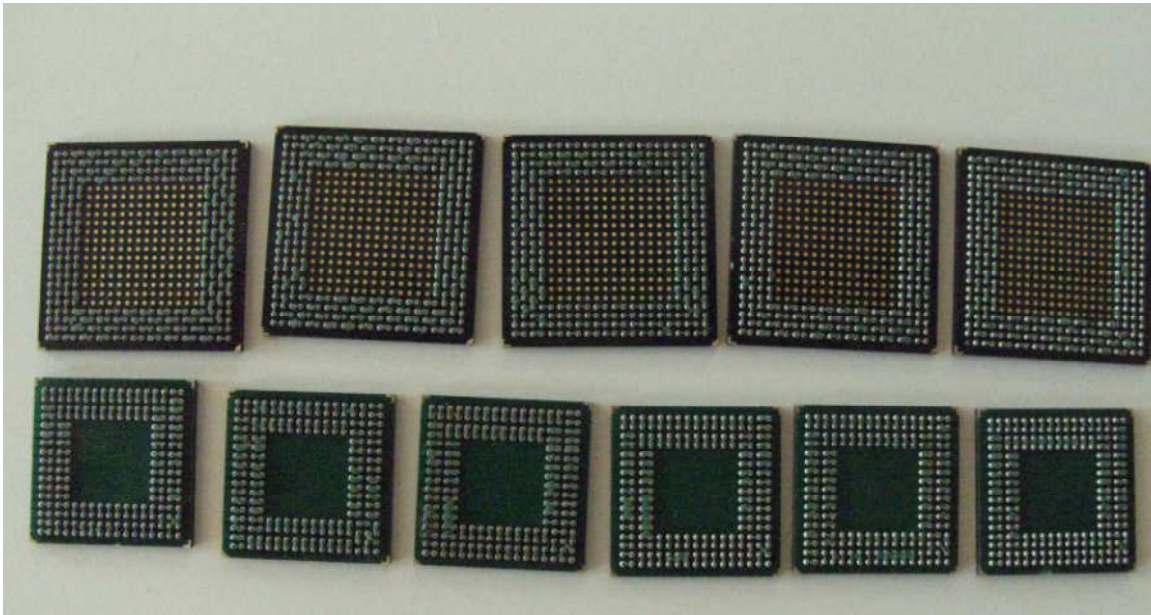


Figure 6.1 TV7 19 & 15 mm parts after drop test

These failures were majorly caused by the inertia forces of the components and the out of plane bending was not achieved. To overcome this, another test was performed with a change in fixture. The test board was held in a vertical position at 90 to the direction of the drop with an intention of stressing the joints. Thus the fixture in figure 6.3 was tested.

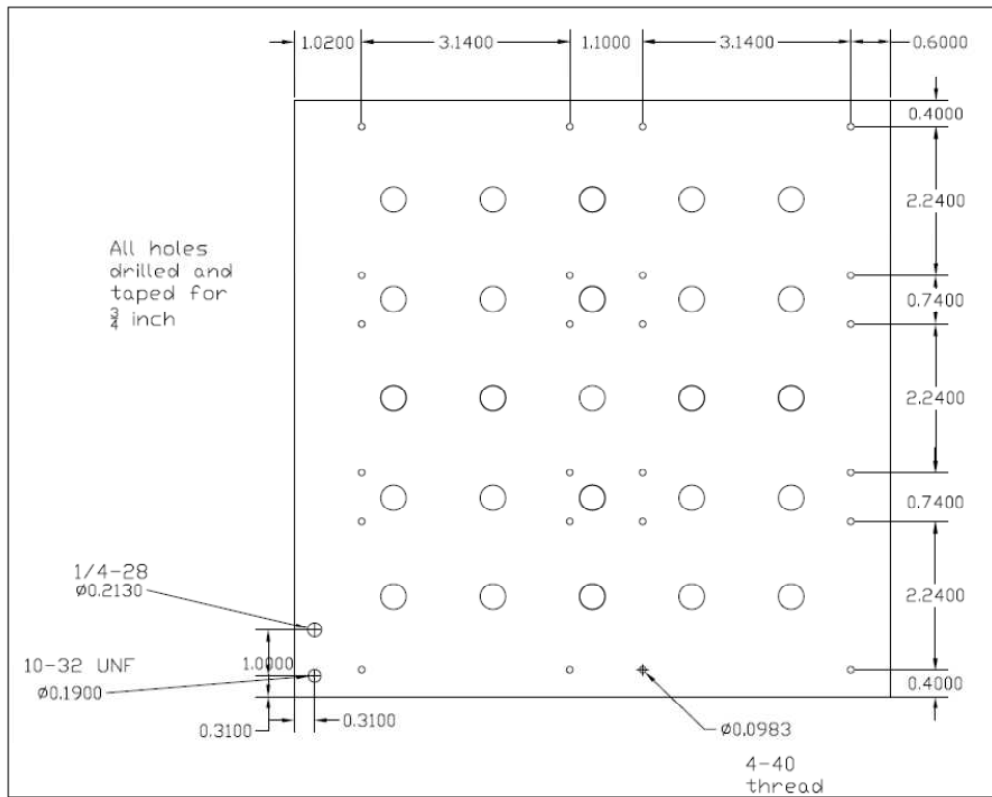


Figure 6.2 Horizontal Drop test fixture



Figure 6.3 Vertical Drop test fixture

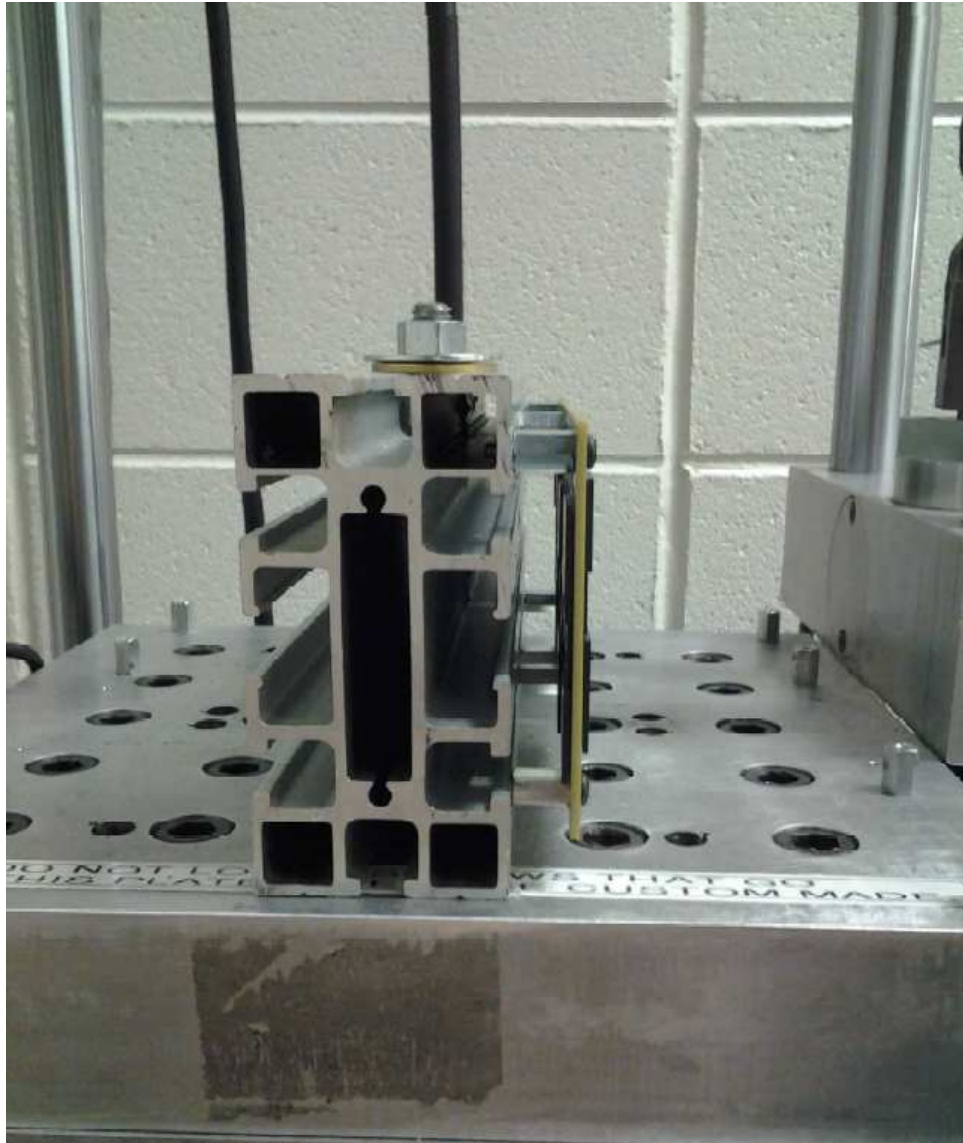


Figure 6.4 Vertical Drop test fixture - 2

The intention of a change in angle was to use the inertia force to act on the solder joints but the results were the same, the components were ripped off the board. On closer examination of the test boards the reason for this behavior can be concluded from the previous vibration test experience. This particular test vehicle, which was not designed to be subjected to any particular mechanical test other than thermal test, the dominant factor

happens to be the test board which resists any bending to cause out of plane bending. More over the degradation of the substrate is assumed to be pronounced at near the copper traces since all the parts were ripped of the board. The test boards not being to JEDEC standard can be one of the major reasons for the inability to conduct the drop test.

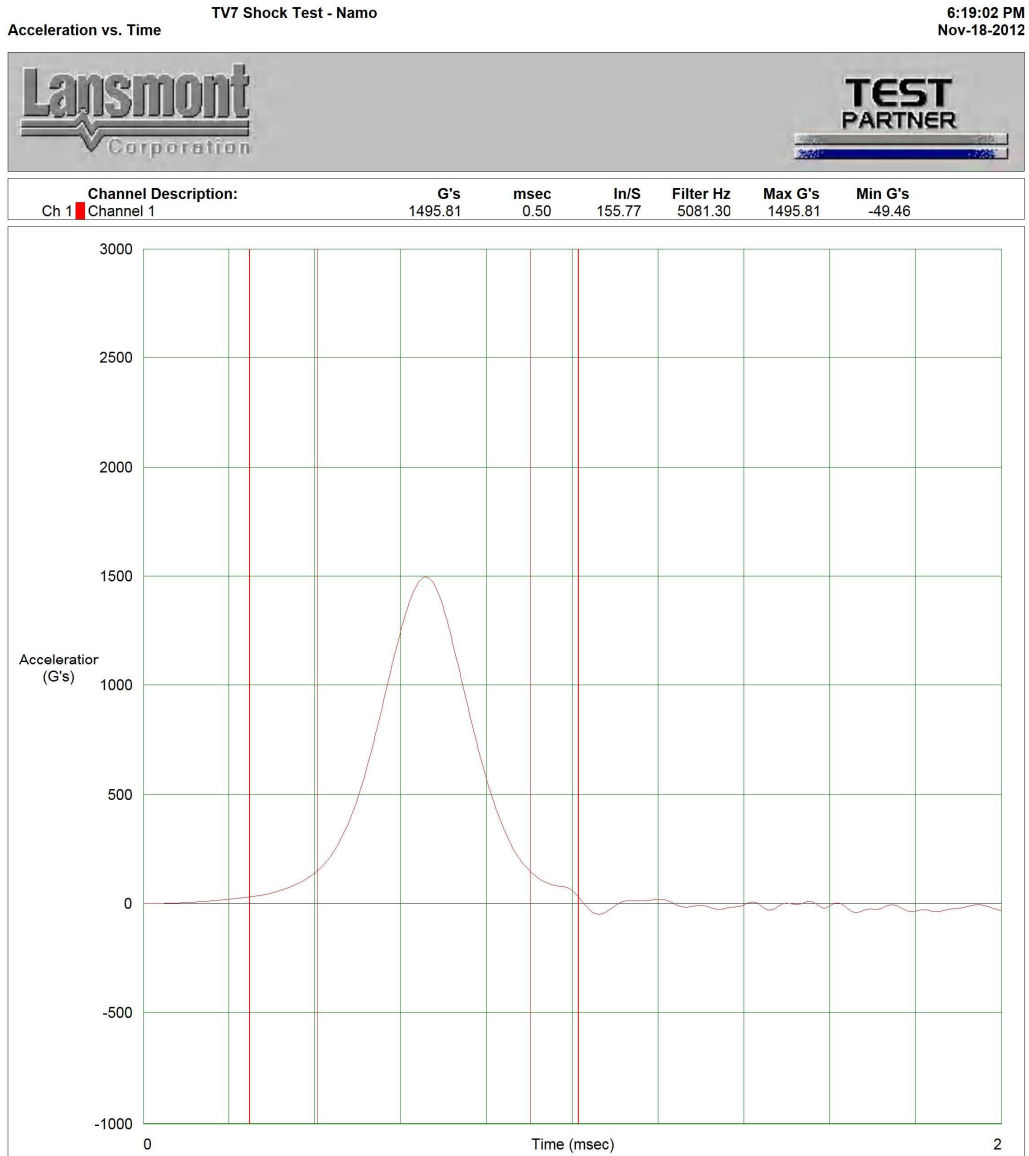


Figure 6.5 Table input graph at 1500g's

## Chapter 7

### Conclusion and Future Work

#### 7.1 Vibration Test

The vibration test data have yielded some very interesting trends. By comparing part by part it displays a shift in the performance of the SAC alloys and the rate of deterioration for time period is also revealed. In the 19mm packages, the drop in characteristics life of SAC105 drops by 51% from 6 to 12 months and a higher drop of 92% from 12 to 24 months. This increase in percent drop is consistent for other packages like the 15mm and 10mm, in 15mm for 6 to 12 months the drop is 35% and from 12 to 24 is 85%, in 10mm the drop from 6 to 12 months is 33% and from 12 to 24 months is 62%. This rampant increase is not noticed in SAC305 where the rate of drop in the Characteristic life much milder. The SAC305 has a 58% reduction in characteristic life time for 6 to 12 months which is on par with the SAC105 for 19mm package; similarly the same is noticed with 15mm and 10mm package. But for 12 to 24 months it is only 64% compared to 92% of SAC105, again similar pattern is observed for 15mm and 10mm packages, which indicated that aging effect on SAC305 is less pronounced than compared to SAC105.

By comparing with Thermal cycling where the data for 12 to 24 months is yet to be collected, but in 0 -6 months and 6 – 12 months, the percentage drop is much lower. Though step stress not present in Thermal Aging, the rate of deterioration between SAC105 and SAC305 illustrates that the performance of SAC 305 is better.

The Weibull plots show that there is shift in the performance of SAC solders as it is aged. At one year aging the SAC105 lost its advantage it had over SAC 305 at 6 months and at 24 months it performed worse than the SAC 305. This could be due to reduction in ductility of the low Ag solder over time. Since the failure modes were consistent it could be attributed to the intermetallics.

The Future work involved in this should try to address:

- The type of intermetallic and its behavior needs to be understood as time progresses and different surface plating is suggested.
- More importance have been given to the intermetallics at the pad and bulk solder joint, but in vibration it is observed that the crack origin have be found at both the chip/bulk solder interface and pad/bulk solder interface.
- The comparison matrix is not complete without the no aging data, if the slot is filled with data it would give a better understating of how much the reliability is affected by thermal aging.
- To overcome the effect of SAC105 issue, other mixed alloys have to be looked into along with different plating.
- Change in the design to overcome the issues currently faced, like no phase chance since the objective is to study the joint behavior.
- To keep all test boards identical in order to reduce the variability in stress due to components not present on pad, this would help give the ability to make a location and part by part comparison more efficiently.

## 7.2 Shock Test

The necessity to conduct a shock test is to stress the solder joints and study the behavior of SAC105 and SAC305 alloys at different aging but it was not accomplished. The inability to cause stress at the solder joints might very well be due to the fact that the test boards were not designed as per JEDEC standards. Since the JEDEC standard requires the test board mounting holes to be at least 105 mm apart and the TV7 test board had 79.75mm pitch and 56.9mm instead of 71mm. Moreover the test boards were not built identical to each other due to the limited availability of the components. With some parts missing the stress aging on one particular board is not the same on another board with one less or too many components.

To make use of the existing boards

- To explore the option of under filling perimeter array components and stay clear of solder joints which would make them more rigid but still could be stress at the chip/bulk solder interface.
- To explore the option of doing a bend test with a fixed Newton's applied in cycle with a curved arm to bend at an angle

In the future test to yield more comparable data

- Having a test board according to JEDEC drop standard to eliminate the issue of board being the dominant factor.
- Have all boards built with identical number of parts to have identical stress at each sample of the test matrix, and look into mixed alloys and doping option with different plating to address effects of aging.

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# Appendix A1

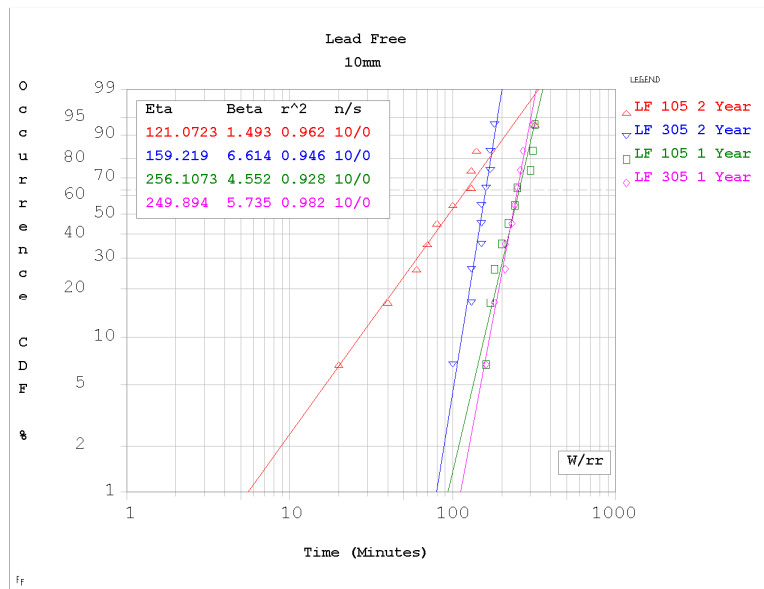


Figure A1.1 Weibull plots 10mm BGA SAC105vs305 at 12 months and 24 months

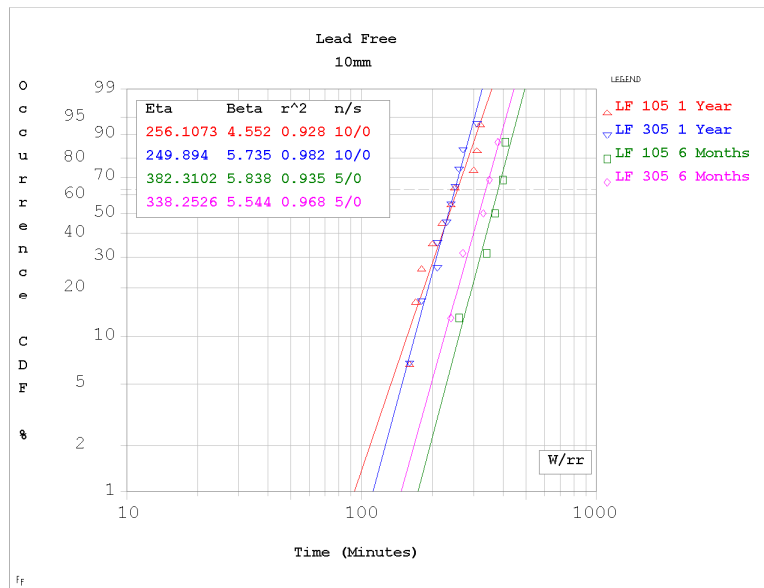


Figure A1.2 Weibull plots 10mm BGA SAC105vs305 at 6 months and 12 months

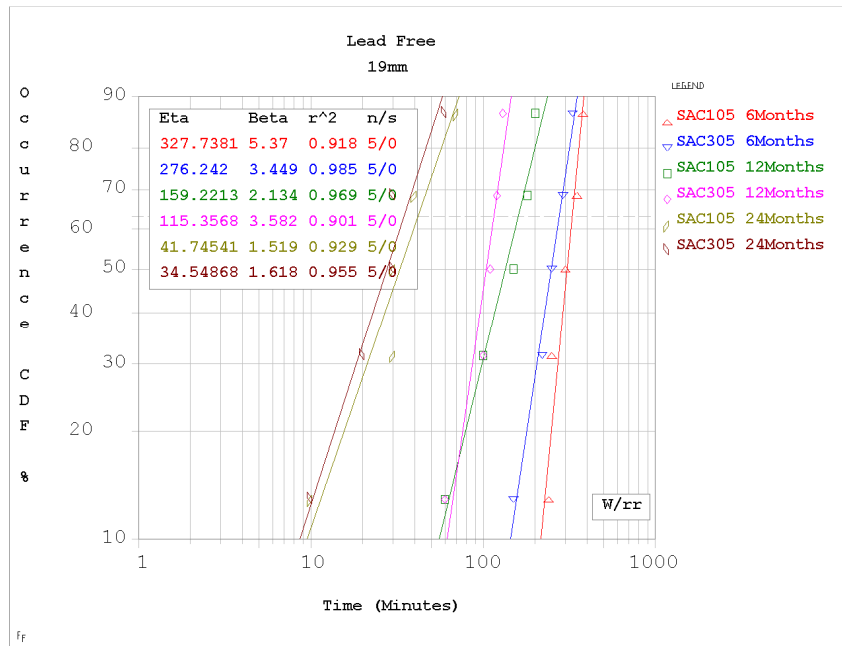


Figure A1.3 Weibull plots 19mm BGA SAC105vs305 at 6, 12 and 24 months

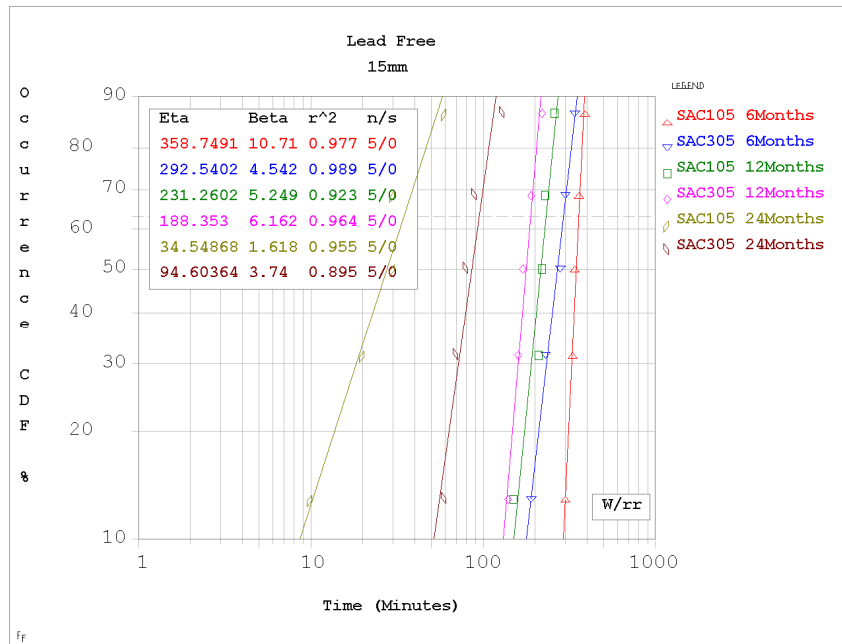


Figure A1.4 Weibull plots 15mm BGA SAC105vs305 at 6, 12 and 24 months

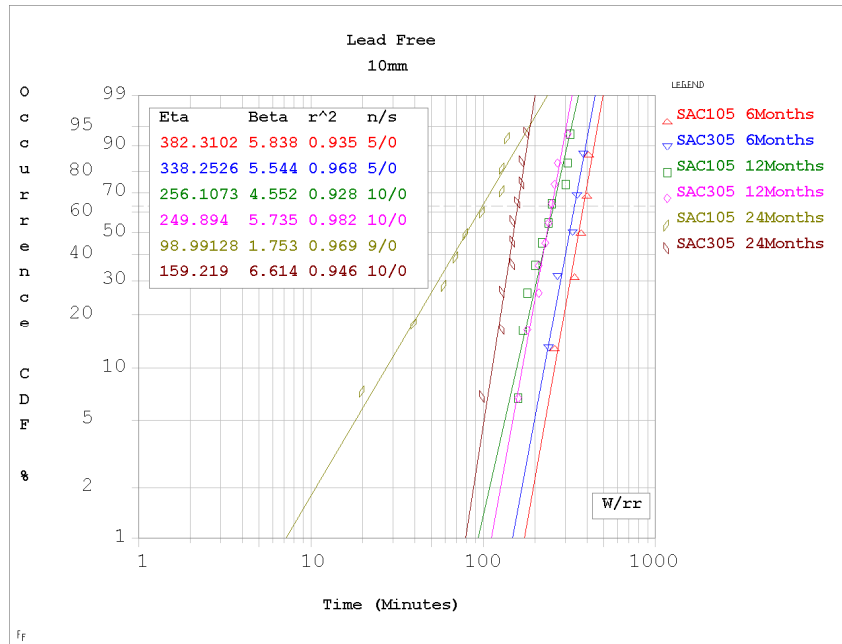
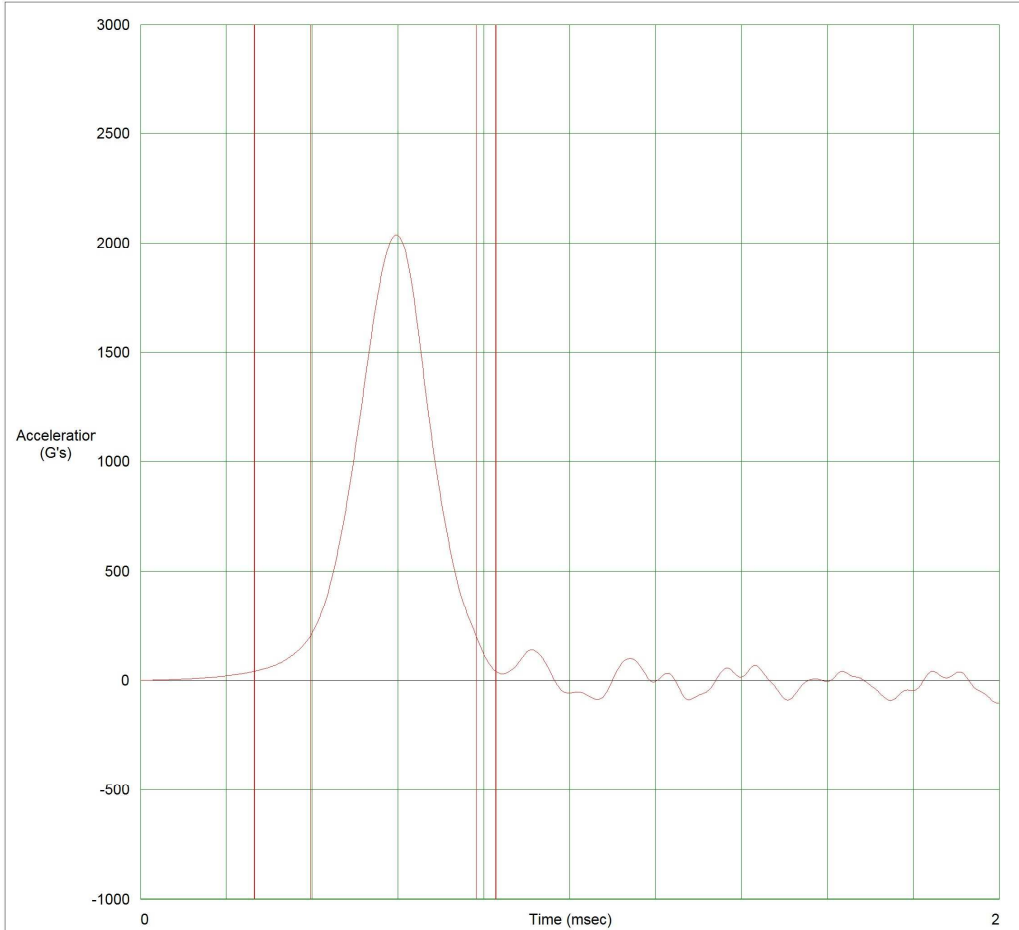


Figure A1.5 Weibull plots 10mm BGA SAC105vs305 at 6, 12 and 24 months



Channel Description:	G's	msec	In/S	Filter Hz	Max G's	Min G's
Ch 1 Channel 1	2038.15	0.39	165.47	6476.68	2038.15	-105.08



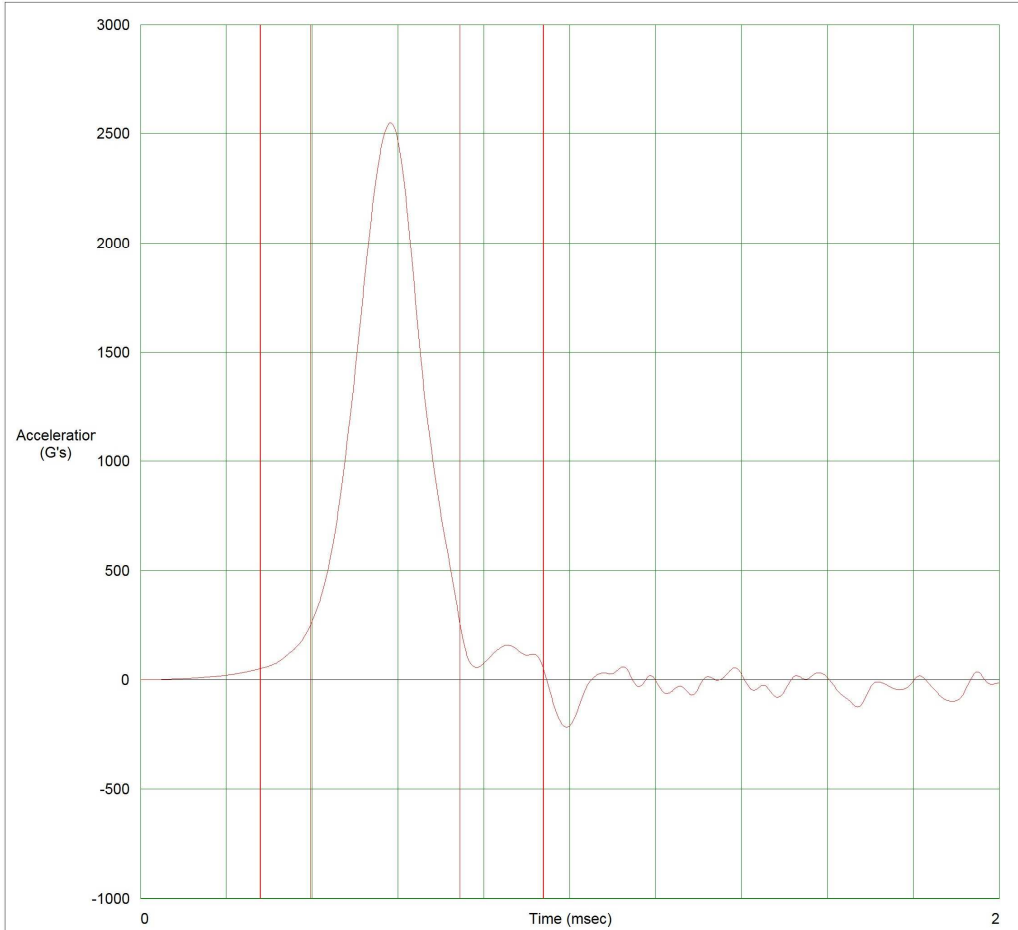
CHANNEL #1 = TABLE INPUT  
CHANNEL #2 = TABLE INPUT 2

Figure A1.6 Table input at 2000g's



TEST PARTNER

Channel Description:	G's	msec	In/S	Filter Hz	Max G's	Min G's
Ch 1 Channel 1	2548.95	0.35	195.52	7225.43	2548.95	-215.75



CHANNEL #1 = TABLE INPUT  
CHANNEL #2 = TABLE INPUT 2

Figure A1.7 Table input at 2500g's