Modeling and Reliability Characterization of Area-Array Electronics Subjected to High-G Mechanical Shock Up To 50,000G and Finite Element Analysis of Package on Package (PoP) Components for Warpage During Reflow

by

Kewal Patel

A thesis submitted to the Graduate Faculty of
Auburn University
in partial fulfillment of the
requirements for the Degree of
Master of Science

Auburn, Alabama
May 5, 2013

Keywords: Electronic package, High-G, Shock, Micro-coil spring (MCS), Warpage, Package on Package (PoP)

Approved by

Pradeep Lall, Chair, Thomas Walter Professor of Mechanical Engineering
Jeffrey C Suhling, Quina Distinguished Professor of Mechanical Engineering
George T. Flowers, Professor of Mechanical Engineering and Dean of Graduate School

Abstract

Electronics in aerospace applications may be subjected to very high g-loads during normal operation. A novel micro-coil array interconnect has been studied for increased reliability during extended duration aerospace missions in presence of high-g loads. Ceramic area-array components have been populated with micro-coil interconnects. The micro-coil spring (MCS) is fabricated using a beryllium copper wire post plated with 100 μin of Sn63Pb37, 50 mils in height with a diameter of 20 mils. Board assemblies have been subjected to high g-loads in the 0°, horizontal orientation. The board assemblies are daisy chained. Damage initiation and progression in the interconnects has been measured using in-situ monitoring with high speed data acquisition systems. Transient deformation of the board assemblies has been measured using high-speed cameras with digital image correlation.

Multiple board assemblies have been subjected to shock tests till failure. Peak shock pulse magnitudes range from 1,500g typical of JEDEC standard, to very high g-levels of 50,000g. Board assemblies have been tested at different orientations. The MCS interconnects are daisy chained and failures are measured using electrical continuity. A finite element model using explicit global to local models has been used to study interconnect reliability under shock loads. Models have been correlated with experimental data. The reliability performance of micro-coil interconnects has been

compared to column interconnects. Results have shown that the micro-coil spring array has a higher reliability than the ceramic column grid array (CCGA). Failure modes have been determined for both interconnect types.

Additionally, this study investigates the area of package warpage. Package-on-Package (PoP) assemblies may experience warpage during package fabrication and later during surface mount assembly. Excessive warpage may result in loss-of-coplanarity, open connections, misshaped joints, and reduction in package board-level reliability (BLR) under environmental stresses of thermal cycling, shock and vibration. Previous researchers have shown that warpage may be influenced by a number of design and process factors including underfill properties, mold properties, package geometry, package architecture, board configuration, underfill and mold dispense and cure parameters, and package location in the molding panel.

In this study, warpage has been measured using shadow moiré interferometery and an optical full-field measurement technique called DIC or digital image correlation. Finite element models have been created and correlated with experimental data to create a baseline model. Investigation on the effects of materials selection, package dimensions, and material properties has been conducted by altering the baseline finite element model. The material properties (CTE1, CTE2, E1 and E2) have all been varied for each material found in the PoP package including the epoxy molding compound, the substrate core, and the die. The effects of die thickness and geometry have also been investigated. A sensitivity analysis has been performed to determine the relative influences each parameter has on package warpage.

Acknowledgements

I am forever indebted to my parents without whom I would never have been given such a fortunate opportunity to create a better future for myself. For their unwavering love, continued support, and constant encouragement, I thank my mother, Sumitra Patel, and father, Suresh Patel. I am proud to say that their hard work and unwillingness to give up has greatly inspired me. I would also like to thank my sister, Swayam Patel, and brother, Mital Patel who were always there to lend an ear to my complaints and give me words of encouragement.

I would like to thank my advisor and teacher, Dr. Lall, under whom I was given the honor and privilege to conduct research. His keen insight, innovative ideas, and deep interest in the research inspired and helped me greatly in completing my research. Special thanks to Dr. Suhling under whom I took several courses. Dr. Suhling's broad knowledge and insight was a great help in my completion of this degree. I would also like to thank Dr. Flowers for not only serving on my committee but also for his candid advice and honest appraisal.

It is great honor to be able to work with individuals who are not only my colleagues but also my friends. For their support and friendship I would like to thank my friends and colleagues: Ryan, Geeta, Prashant, Vikalp, Mahendra, Dinesh, Sandeep,

Peter, Jordan, Hao, Jerry, Kazi, and many others who are not mentioned here. I would also like to greatly thank my friends outside of the lab of which there are too many to list.

Table of Contents

Abstract ii

Acknowledgements iv

List of Figures viii

List of Tables xiii

1. Introduction 1

1.1 What is electronic packaging? 1

1.2 Reliability issues at the second level of interconnection 4

1.3 Shock Testing of Electronic Packages 6

1.4 The Finite Element Method (FEM) 9

1.5 Digital Image Correlation (DIC) 10

1.6 Thesis Objective 14

2. Literature Review 16

2.1 Drop and Shock Testing 16

2.2 Finite Element Modeling of Transient Events 19

2.3 Digital Image Correlation (DIC) 20

2.4 Package Warpage 21

3. Modeling and Reliability Characterization of Area Array Electronics Subjected to High-G Mechanical Shock Up To 50,000g at Multiple Orientations 24

3.1 Introduction 24

3.2 Test-Vehicles 26

3.3 Experimental Set-up 30

3.4 Benchmark Testing 38

3.5 MCS vs. CCGA: Reliability Analysis 48

3.6 Failure Analysis 56

3.7 Finite Element Analysis Approach 65

3.8 Finite Element Analysis Results 74

4. Finite Element Analysis and Evaluation of Warpage for Package-on-Package (PoP) Components 85

4.1 Introduction 85

4.2 Test Vehicles 89

4.3 Experimental Set Up 92

4.4 Finite Element Analysis 95

4.5 Material Properties and Dimensions Effects on Warpage 103

4.6 Warpage Sensitivity Analysis 114

5. Summary, Conclusions, and Future Work 123

Bibliography 126

List of Figures

Figure 1-1: Electronic packaging hierarchy 2

Figure 1-2: Different layers of common electronic package 5

Figure 1-3: Warpage based solder joint failures 6

Figure 1-4: JEDEC acceleration pulse 8

Figure 1-5: FEA approximation 10

Figure 1-6: Deformation tracking 11

Figure 1-7: DIC experimental set up 13

Figure 2-1: JEDEC test apparatus 18

Figure 2-2: Warpage sign convention 22

Figure 2-3: Test apparatus set up 23

Figure 3-1: Test Board 27

Figure 3-2: Schematic of the MCS Interconnect 28

Figure 3-3: Column Interconnect 29

Figure 3-4: Drop Test Setup 30

Figure 3-5: 1500g board deformation (a) undeformed (b) negative deflection (c) positive deflection 31

Figure 3-6: Drop test repeatability 32

Figure 3-7: Dual Mass Shock Amplifier (DMSA) 33

Figure 3-8: Standard drop test set up vs. high-g test set up 35

Figure 3-9: Custom drop fixture for vertical drop testing 37
Figure 3-10: Drop test set-up for vertical orientation 38
Figure 3-11: Peak deflection close up 39
Figure 3-12: Board deflection for benchmark test 40
Figure 3-13: Board deflection side view 41
Figure 3-14: Detailed board deflection 42
Figure 3-15: 40,000g (a) Un-deformed (b) Deformed 43
Figure 3-16: Strain comparison 1500g vs 50,000g 44
Figure 3-17: High-G acceleration test levels 45
Figure 3-18: MCS deformation for a 2000g drop 46
Figure 3-19: MCS deflection close-up 47
Figure 3-20: Column interconnect deformation for a 2000g drop 48
Figure 3-21: Strain comparison for high-g test levels 49
Figure 3-22: CCGA horizontal orientation high-g reliability results 50
Figure 3-23: MCS horizontal orientation high-g reliability results 50
Figure 3-24: Effect of G-loading on MCS interconnect reliability 51
Figure 3-25: Effect of G-loading on CCGA interconnect reliability 52
Figure 3-26: Micro-Spring Coil Vs Column Interconnect reliability at 30,000g 52
Figure 3-27: Micro-Spring Coil Vs Column Interconnect reliability at 40,000g 53
Figure 3-28: Micro-Spring Coil Vs Column Interconnect reliability at 50,000g 53
Figure 3-29: CCGA vertical orientation failure results 55
Figure 3-30: MCS vertical orientation failure results 55
Figure 3-31: Effect of G-level on MCS interconnect reliability 56

Figure 3-32: MCS Failure Mode-1 57
Figure 3-33: MCS Failure Mode-2 58
Figure 3-34: CCGA Failure Mode-2 59
Figure 3-35: CCGA Failure Mode-1 60
Figure 3-36: Column Failures 61
Figure 3-37: MCS Failure Mode-1 for vertical orientation 63
Figure 3-38: MCS Failure Mode-2 for vertical orientation 64
Figure 3-39: Global-Local submodeling 66
Figure 3-40: Global model 67
Figure 3-41: Global model FEA set up 67
Figure 3-42: MCS Array Submodel 68
Figure 3-43: Detail MCS interconnect FEA model 69
Figure 3-44: SPRINGA element 70
Figure 3-45: CCGA Array Submodel 71
Figure 3-46: Detail CCGA interconnect 72
Figure 3-47: B31 element 73
Figure 3-48: Global model FEA time history 74
Figure 3-49: Displacement for 30,000g: DIC vs. FEA 75
Figure 3-50: Displacement for 40,000g: DIC vs. FEA 76
Figure 3-51: Displacement for 50,000g: DIC vs. FEA 76
Figure 3-52: FEA vs. Experimnetal Strain - 30,000g 77
Figure 3-53: FEA vs. Experimental Strain - 40,000g 78
Figure 3-54: FEA vs. Experimental Strain - 50,000g 79

Figure 3-55: CCGA Von-mises stress contour 80
Figure 3-56: CCGA stress components 81
Figure 3-57: MCS deflection time history 82
Figure 3-58: MCS stress components during compression 83
Figure 3-59: MCS stress components at max deflection 84
Figure 4-1: A common PoP configuration 86
Figure 4-2: Warpage phenomenon schematic 87
Figure 4-3 : Warpage sign convention 87
Figure 4-4: Test vehicle 1 package architecture 90
Figure 4-5: Test vehicle 2 package architecture 90
Figure 4-6: Temperature profile for reflow 92
Figure 4-7: Experimental set up 93
Figure 4-8: Digital image correlation for a 3D case 94
Figure 4-9: DIC Out-of-plane displacement contour 95
Figure 4-10: Test Vehicle 1 Package Type A FEM 96
Figure 4-11: Test Vehicle 2 Package Type A FEM 97
Figure 4-12: Quarter symmetry nodal constraints 98
Figure 4-13: Quarter symmetry Z-displacement result 99
Figure 4-14: Fully symmetrical warpage representation at 250C 100
Figure 4-15: Warpage at key temperatures 101
Figure 4-16: Experimental warpage Vs. FEA warpage 102
Figure 4-17: Warpage for substrate core CTE variation 103
Figure 4-18: Warpage for substrate core E variation 104

Figure 4-19: Warpage for core thickness variation 105
Figure 4-20: Warpage for silicon die CTE variation 106
Figure 4-21: Warpage for die E variation 107
Figure 4-22: Warpage for die thickness variation 108
Figure 4-23: Warpage for die dimension variation 109
Figure 4-24: Warpage for mold CTE1 variation 110
Figure 4-25: Warpage for mold CTE2 variation 111
Figure 4-26: Warpage for mold E1 variation 112
Figure 4-27: Warpage for mold E2 variation 113
Figure 4-28: Warpage for mold thickness variation 114
Figure 4-29: Warpage comparison below T_g 116
Figure 4-30: Sensitivity analysis: percent change from baseline warpage below T_g 117
Figure 4-31: Warpage comparison above T_g 119
Figure 4-32: Sensitivity analysis: percent change from baseline warpage above T_g 120
Figure 4-33: Sensitivity analysis for warpage comparison above and below Tg 122

List of Tables

Table 4-1: Range of values examined..... 88

Table 4-2: Test vehicle 1 package specifications 90

Table 4-3: Test vehicle 2 package specifications 91

Table 4-4: Silicon orthotropic material properties..... 106

1. Introduction

1.1 What is electronic packaging?

Over the past few decades, technology has become more integrated into the daily lives of the human population. Cell phones have become common place whereas they used to be a novelty less than twenty years ago. This trend of electronic integration is not only occurring at the consumer level but almost in every industry. With such an increased reliance on electronics, the cost, manufacturing, and reliability of electronic devices has become a key area of concern. Computational functionality of devices has grown at a rapid pace especially with the creation of the integrated circuit chip.

Electronic packaging is an art based on science of placing and interconnecting different levels of electronic systems. The process of electronic packaging begins with the creation of integrated circuits on a semiconductor material. Silicon, due to its semiconductor nature, is often used in electronic devices. The first step in the process of creating a silicon based integrated circuit chip involves the cutting of silicon wafer into smaller pieces to form what is called the "chip". The chip is housed in a chip container or carrier. Interconnections between the chip and the carrier are made using wire bonds made of a conductive material such as gold. Tiny solder bumps have also been developed used a means of interconnection between the chip and carrier. The assembly

consisting of the chip and its carrier is called a first level package. The second level package consists of one or more chip carriers connected to a printed circuit board (PCB). Printed circuit boards have conductive wire traces that are routed throughout the board to create an electrical connection between different electrical components. The third level package consists of several PCBs connected to a bus or motherboard. The PCBs are interconnected using edge connectors that allow communication between the multiple PCBs. The hierarchy of packages used in electronic packaging can be seen in Figure 1-1.

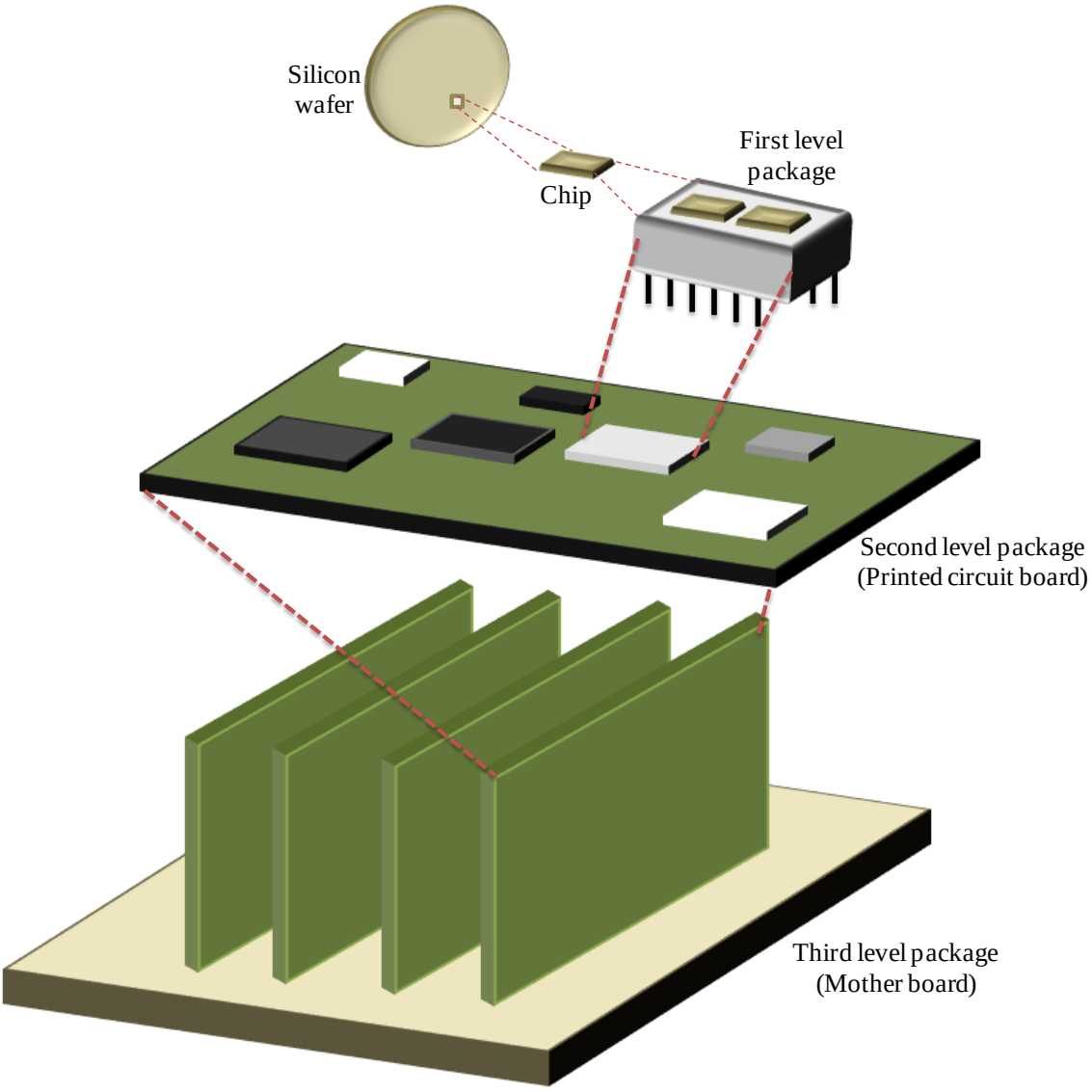


Figure 1-1: Electronic packaging hierarchy

The reliability of the secondary level interconnects is a key area of concern. Second level electronic packages are generally attached to PCBs either as through-hole components or surface mounted components. Most early forms of electronic packaging used through-hole connectors to make the connection from first level electronics (the chip carrier) to second level electronics (the PCB). The chip is generally attached on top of a metallic lead frame. The lead frame is bent to form pin connectors which are pressed through a hole in the PCB.

Increasing demands for miniaturization and functionality brought about the creation of surface of mounted devices (SMD). Surface mount technology (SMT) involves placing the components on the surface of the board using landing pads and solder attachments instead of using a through hole interconnect. The number of inputs and outputs are greatly increased since both sides of the boards can be used and a higher density of interconnects can be placed on the board. The earlier forms SMDs utilized perimeter based leads. Some examples of perimeter based lead packages are the small outline package (SOP) and the quad flat package (QFP). These surface mount devices often used gull wing interconnects based of a metallic lead frame as a means of interconnection. Finer lead pitch could be achieved by using gull wings interconnects. Another type of electronic package developed for SMT applications is the area array package type. Area array packages utilize the area under the package for interconnection purposes. Copper pads on the package side are often connected to landing pads on PCB using solder interconnects. Common area array package types that use solder interconnects include the ball grid array (BGA) and the column grid arrays (CGA). Recently, increasing demands for higher functionality and performance have resulted in

the development of even newer packaging types such as stacked-chip packages, 3D packages, and chip on board packages (COB). These increases in functionality and performance have also resulted in more concerns about reliability.

1.2 Reliability issues at the second level of interconnection

Many reliability issues exist for the second level of interconnection and are more present than ever with the creation of the high functionality technologies such as package on package (PoP), chip on board (COB), and stacked die packages. Electronic packages are often exposed to many different environments and loadings. Failures in electronic packages may be the result of thermal, mechanical, electrical, or manufacturing issues. Thermally induced failures in electronics packages often occur due to a mismatch in the coefficients of thermal expansion (CTE). Electronic packages are made up of different layers of materials including the molding compound, a laminate substrate, a silicon die, silicon adhesive, and solder interconnects. Figure 1-2 is a cross section schematic showing the different layers of a common type of electronic package, the ball grid array (BGA). Failure in the BGA often occurs at the solder ball level due to the large mismatch in the CTE between the silicon die and the printed circuit board (PCB). The die has a much lower CTE compared to the PCB and will expand more slowly compared to the PCB which results in thermally induced stresses occurring in the solder ball interconnect. This becomes more of problem in electronic packages exposed to thermal cycling environments where temperatures change from very high to very low. The thermal cycling of electronic packages can cause fatigue and often times failures in the electronic package.

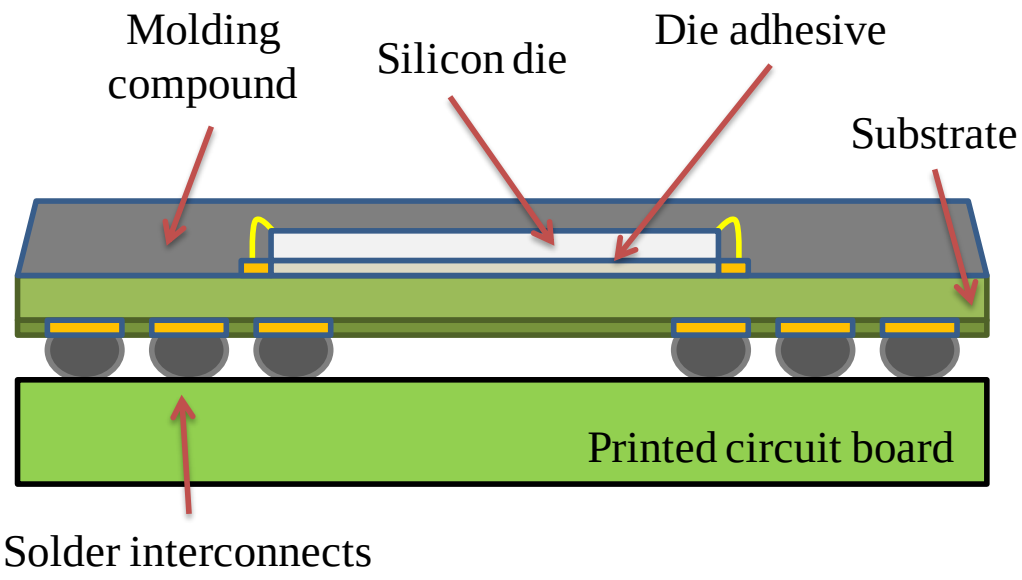


Figure 1-2: Different layers of common electronic package

Defects and failures may occur at the manufacturing level as well. One of the key concerns with the creation of surface mounted devices is the issue of co-planarity. Co-planarity is the relative out of plane distance between the printed circuit boards the solder interconnects. Although the PCB and electronic package may appear to be flat, small bumps and flaws often exist. Permanent warpage of the printed circuit board and electronic package may occur due to thermal processing. As a result of warpage, faulty solder joints may occur during the manufacturing process. Figure 1-3 shows an exaggerated schematic where solder joints have not been properly attached to the printed circuit board as a result of warpage in the electronic package.

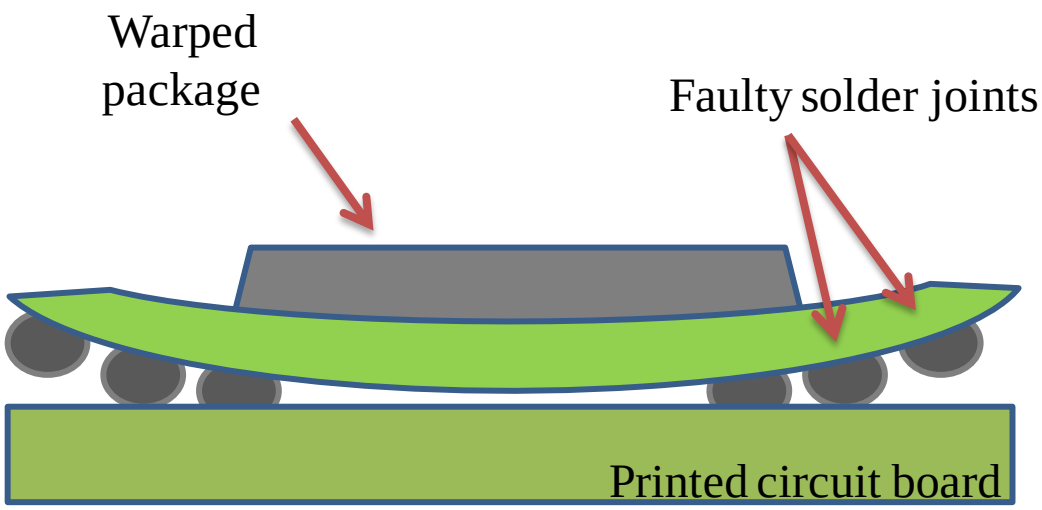


Figure 1-3: Warpage based solder joint failures

Mechanical failures may occur due to mishandling of electronic components during operation. The dropping of a cell phone and the crashing of car are examples of scenarios where the electronic package may fail due to mechanical loads. Electronic components must be able to withstand the vibration and shock that occurs during these types of events to ensure high reliability and continued functionality. In certain applications such as military operations, avionics, and space travel, the vibration and shock is expected. For these applications ultra-high reliability components are required since failure of electronic packages may result in loss of money or even lives. In this study, reliability concerns are investigated for ultra-high level reliability components under high-g loading.

1.3 Shock Testing of Electronic Packages

Electronic packages exposed to mechanical shocks often fail at the secondary level of interconnection. Failure may occur in the electronic package if the electronic

packages have not been tested for reliability under those test conditions. To determine the reliability of electronic packages during actual shock events, controlled testing in a laboratory environment is required. One way of testing for shock reliability is by performing drop tests. Drop tests are performed using drop towers where electronic assemblies are mounted and dropped from a certain height in order to achieve the desired impact level.

The Joint Electron Device Engineering Council (JEDEC) has developed a guideline for performing drop tests to ensure the repeatability of the drop test. One such classification is outlined in the JEDEC standard, JESD22-B111. This standard defines the drop test according to the change in acceleration occurring during the impact event. The desired acceleration pulse should be in the shape of a half-sine wave and consist of a specified pulse duration time. The standard also dictates that the electronic assemblies need to be in free fall. Figure 1-4 shows the desired pulse shape specified by the JEDEC standard.

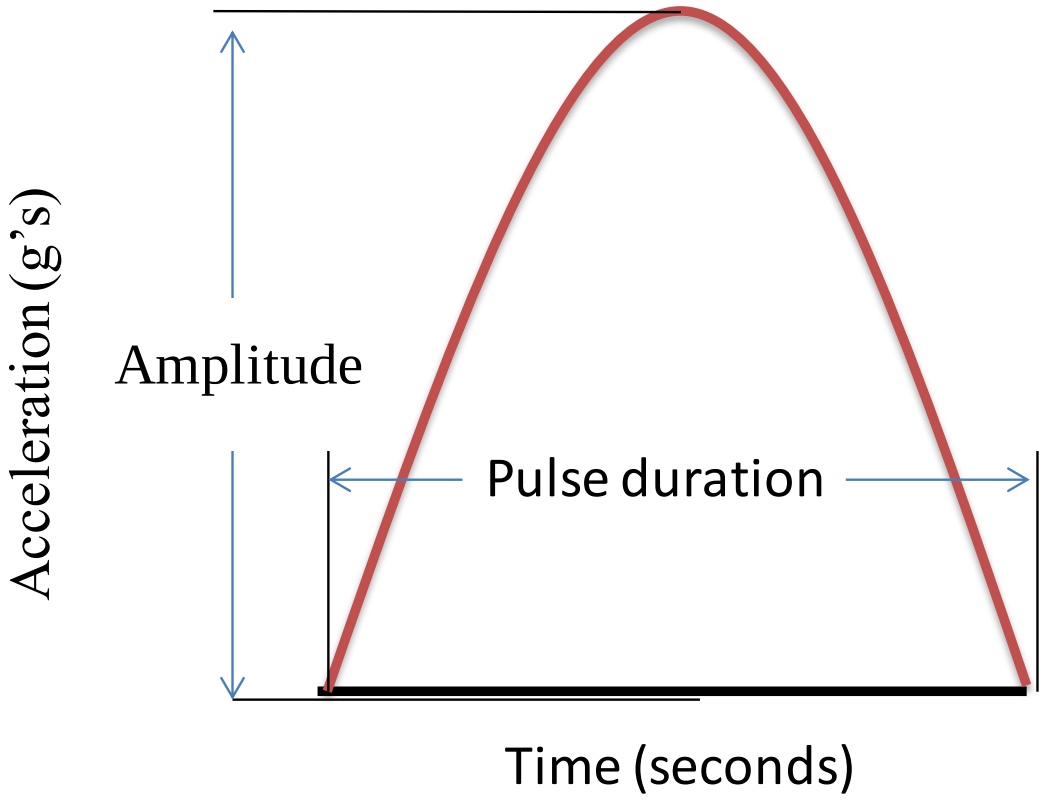


Figure 1-4: JEDEC acceleration pulse

The shape and pulse duration of the acceleration reading is dependent on many things including the electronic package mass, the pulse shaping material, the lubrication of the guide rods, height of the drop distance, and the acceleration of the package. These variables must be controlled in order to achieve a repeatable acceleration reading for every test case. Consumer grade electronic packages are often tested at a 1,500g acceleration level. Ultra-high reliability electronics require testing at higher g-levels. Testing at high-g levels has not been extensively explored in research. Very little literature exists on the reliability of electronic packages exposed to ultra high-g levels. In this study, ultra-high reliability components are tested at very high-g levels to determine the shock level reliability.

1.4 The Finite Element Method (FEM)

Finite element modeling is an attempt to mathematically represent a real-world occurrence. Equations can often times be used to determine a closed form solution to a problem. More complex problems may be harder to solve. The finite element method can be used to approximate the actual solution to a problem. Mathematical solutions are most desired in scenarios where experimental testing is either impossible or not cost effective. Finite element analysis is a technique that makes the analysis of complex structures possible. Finite element analysis involves the discretization of continuum models into discrete finite element sections governed by specific material models. Individual finite elements can be visualized as small pieces of a larger structure. The points of connection between different elements are called nodes. The arrangement of elements to form a complete structure is usually called a "mesh" scheme. The finite element method uses algebraic equations to solve for unknown variables at the nodal locations. The unknown variable can be any number of things including spatial location, temperature, stress, and strain. The unknowns for each element are solved in a peace-wise function to determine a field-value solution for the entire body. At best, the finite element solution is an approximation of the actual solution, but results can be improved by using appropriate element types and increased mesh density. Figure 1-5 is a schematic showing the steps used for a simple finite element analysis. Finite element modeling of transient events, such as drop events, is very challenging due to the instantaneous response that is required of the model. In this study, finite element analysis is used to explore stress and strain values that could not be experimentally determined.

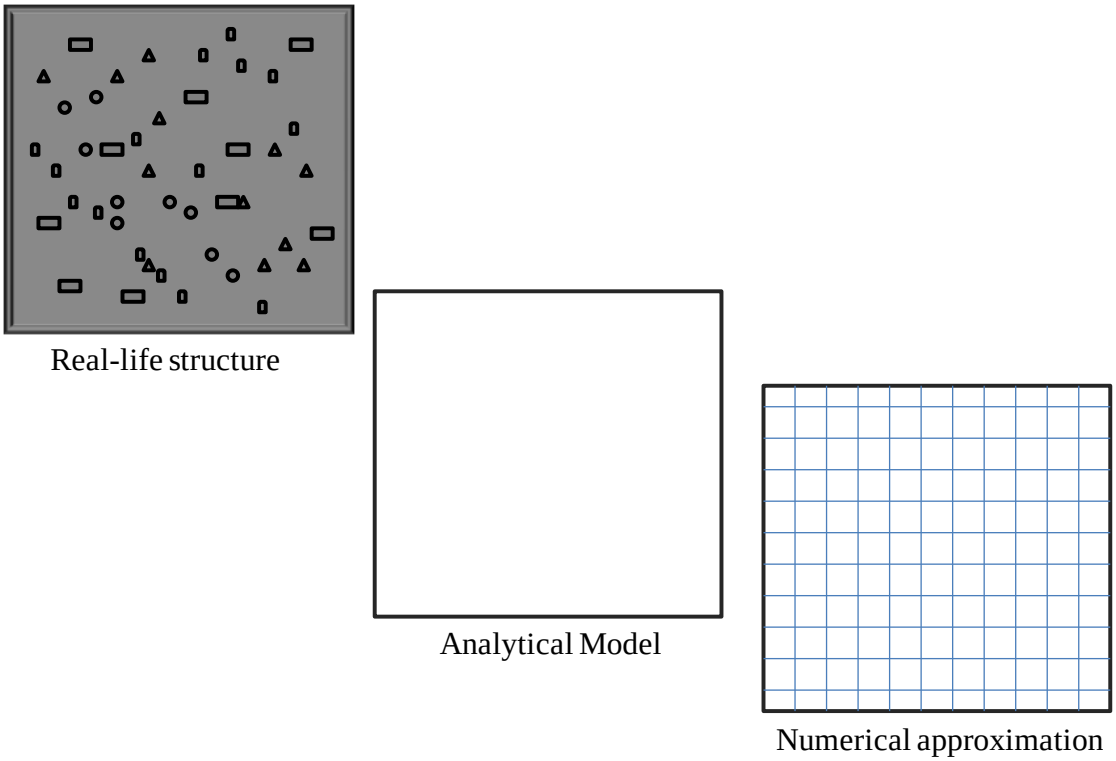


Figure 1-5: FEA approximation

1.5 Digital Image Correlation (DIC)

Digital image correlation is a non-contact, optical method for measuring deformation of an object. Traditionally, strain gages have been used to measure deformation during transient events. Digital image correlation is superior to traditional strain gages for applications where contact with the specimen in not desired or where full field data is desired. The image processing technique works by comparing undeformed and deformed images and calculating the deformation based on pixel movement. Gray value patterns in small subsets of the deformed and undeformed images are determined. Figure 1-6 shows a schematic of the deformation and pixel tracking occurring during a digital image correlation analysis. Specimens are usually coated in white paint and

speckle coated with black spots. The tracking of pixels is much easier when distinct pixel recognition is possible. An example of speckle coated specimen is also shown in Figure 1-6.

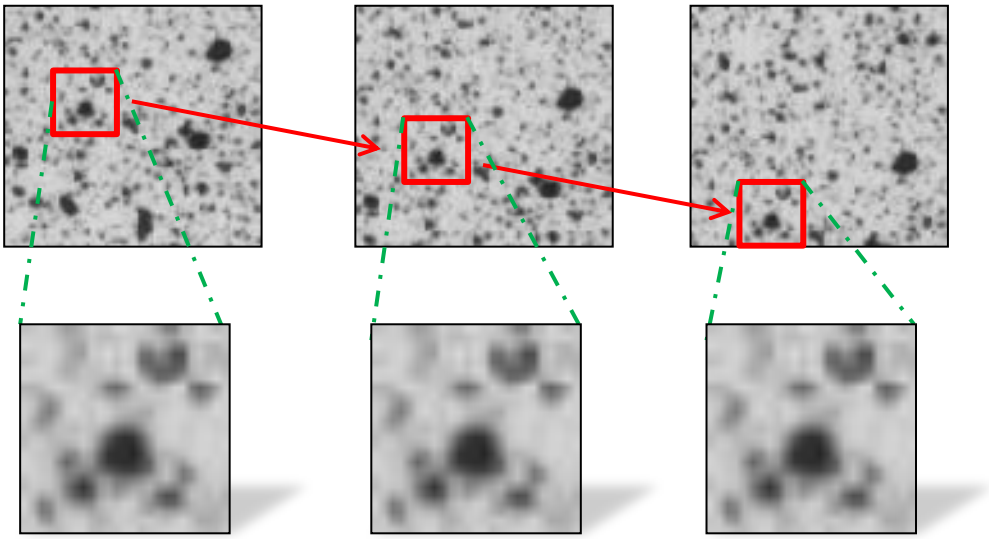


Figure 1-6: Deformation tracking

The deformation results obtained from DIC can be used to determine the full-field strain state of the specimen. Strain measurements using traditional strain gages can be used as a way to correlate and verify the accuracy of the digital image correlation analysis. Calculation of strains is of great importance during transient events such as drop and shock. Images must be captured in the specimen during testing. This can be a difficult task during transient events since the occurrence of deformation occurs under such a short period of time. High speed cameras operating at very high frame rates must be used in order to capture the deformation of such events accurately. Two dimensional deformations can be calculated using DIC and only one camera. Capturing of three dimensional deformations requires the use of two cameras. Calibration of these cameras must be performed before testing. The resulting full field data from the DIC analysis can

be used to evaluate localized strain and deformation values at certain points on the deformation contour. Figure 1-7 shows a schematic of the processes of performing a digital image correlation analysis for a 3D deformation state. Previously the feasibility of using DIC for transient strain measurements in electronic assemblies has been demonstrated [Lall 2007a-e, 2008a-d]. In this study, digital image correlation is used to calculate the strains during high g-level drop testing and to observe thermally induced package deformation in high temperature environments.

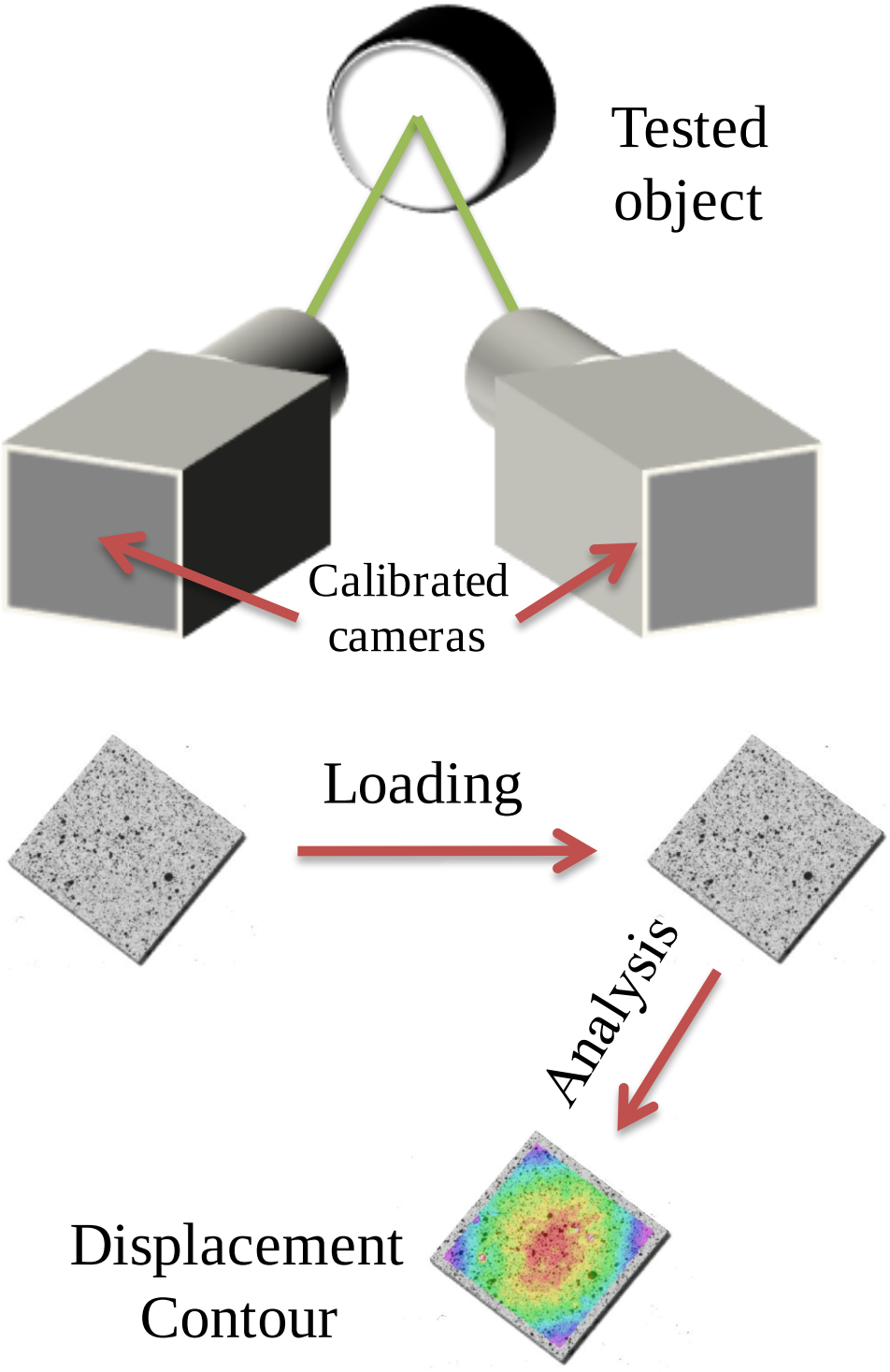


Figure 1-7: DIC experimental set up

1.6 Thesis Objective

The research presented in this thesis studies the impacts of environmental effects on reliability of electronic components. The primary focus of the paper is on the reliability of second level solder interconnects. The reliability of second level interconnects is a major area of concern. Solder joints will often fail due to cracking, shearing, and fatigue. This study aims to investigate the reliability of a new, novel type of interconnect called the micro-coil spring and compare the reliability performance of the micro-coil spring a more common interconnect type, the solder column interconnect. This study also investigates the effects of materials selection, manufacturing dimensions, and temperature conditions on package warpage. Both investigations utilize the finite element method to explore conditions which are not experimentally feasible.

Chapter 2 investigates the current state of art for the various techniques used in this study. The section outlines the available literature pertaining to this research topic. Since a major portion of this study deals with the reliability of second level interconnects, much of the reviewed literature in this section relates to the investigation of second level interconnect reliability. Literature pertaining to reliability of second level interconnects during drop and shock events is outlined. Board-level reliability of common solder interconnects such as BGAs are outlined in particular. This section also outlines the current state of art for package warpage measurement and control. Techniques used in this study, such as digital image correlation (DIC) and the finite element method (FEM), are outlined as well.

Chapter 3 presents a study investigating the reliability of a novel type of interconnect, the micro-coil spring (MCS), during drop and shock testing. The primary aim of the study is to compare the reliability of the MCS interconnect with that of a more industry standard interconnect, the column grid array. The chapter describes the tests carried out to determine the reliability of each interconnect type. Reliability of the interconnects under very high g-loads is reported. Also, the effect of board orientation on reliability is investigated. Failure analysis of the parts is conducted to determine the modes of failure for both types of interconnect. Finally, the stress concentrations on the interconnect level is investigated using the finite element method.

In chapter 4, a study investigating the warpage of package on package (PoP) components is presented. Optical methods of measurements such as digital image correlation (DIC) and shadow moiré interferometery are used to measure the warpage of the package during the test. The study investigates the effects of various process conditions and materials selections on warpage. In particular, the study aims to determine the warpage during reflow temperatures. Finite element models are analyzed and correlated with experimental values. The finite element models are used to determine the effects that material properties and package architecture have on warpage. Lastly, a sensitivity analysis is presented to determine the influence each parameter has on package warpage. In the concluding section, Chapter 5, a summary of the studies performed in this thesis is presented and the scope of possible future work is also presented.

2. Literature Review

2.1 Drop and Shock Testing

Electronics may often be subjected to drop and shock conditions during normal operation. Portable electronics are extremely susceptible to experiencing drop events especially in the current age of cell phones and tablets. These devices are often dropped during handling. The shock may result in the failure on electronics. Previously, researchers have conducted tests on consumer grade electronics to show that the angle of impact is an important parameter to consider for reliability testing of a product [Liu 2005, Seah 2002, Lall 2006b]. One of the most susceptible locations of failure is the second level of interconnects. It is important to understand and characterize not only the dynamics involved during a shock even but also the failure mechanisms. Accurate testing of electronic components can give important insight into a product's reliability. This can be a critical aspect of ensuring long term survivability. The effect of component position, drop orientation, package type, number of screws mounted on PCB, PCB bending, solder material, drop height, PCB size and shape, and flatness of contact surface on reliability during drop testing have been evaluated by researchers [Tee 2004]. Other researchers have also investigated the variability of reliability with drop height, tightness of screw, number of screws, and number of pulse shaping layers [Luan 2003].

The JEDEC drop test specified by the JESD22-B111 standard is a common drop tests performed for electronic devices. The JEDEC standard specifies the drop test by according to the pulse shape and board configuration. One of the most commonly used test conditions is the JEDEC Condition B (1500 Gs, 0.5 millisecond duration, half-sine pulse), as listed in JESD22-B110 Table 1 or in JESD22-B104-B Table 1 [JEDEC 2003]. The test standard specifies that the test vehicle should be mounted with the package side facing downwards to create a more critical loading condition [Yeh 2004]. The standard states that the drop orientation should be horizontal or at zero degrees during the drop test. Figure 2-1 shows the schematic of a drop test as specified by the JEDEC JESD-B111. Although the standard is widely used, researchers have pointed out that the standard has certain limitations such as too many redundant loading conditions. Researchers have pointed out that the redundant loading conditions may result in reduced sample sizes. It has been shown that this limitation can be overcome by using an alternative board design with only one loading condition and large sampling size [Zhao 2007].

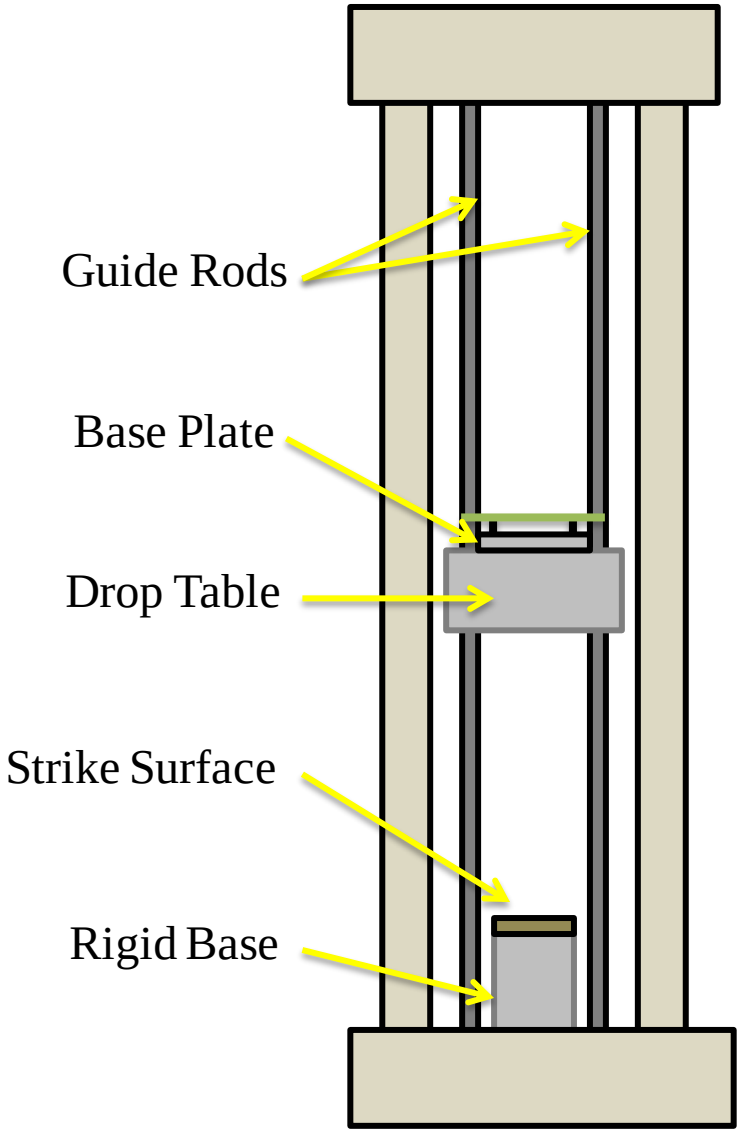


Figure 2-1: JEDEC test apparatus

Drop testing at high-g levels above the JEDEC standard is a relatively new area of research. Testing of electronic components at higher g-levels is meant for ultra-high reliability components. High g-levels on the drop tower are achieved by using an attachment fixture called the dual mass shock amplifier (DMSA). Previously researchers have conducted high-g level testing of electronic components using the DMSA with successful results [Douglas 2009-2010, Meng 2012]. These studies have shown that the

DMSA is a viable option for high-G level testing of electronic components. The studies have also shown that finite element modeling of the high-g transient is possible.

2.2 Finite Element Modeling of Transient Events

Finite element modeling is used in situations where experimental testing of products is either too complex or too costly. The FE method has been used to predict the areas of stress concentrations and strain values in solder interconnects. Normally strain measurements at the second level of interconnection are impossible due to the small size of solder interconnects. The finite element method allows insight into the stress state and possible failure mechanisms of the solder joints. Predicted failure modes can be compared to actual failure modes to determine the validity of the finite element model. The results obtained from the finite element analysis can be correlated with experimental results at the board level to ensure that the model is accurately simulating the event.

Prediction of transient dynamic events has previously been investigated using equivalent layers models [Gu 2005], smeared property models [Lall 2004, 2005], conventional shell with Timoshenko-beam element Model and the continuum shell with Timoshenko-beam Element Model [Lall 2006a,b, 2007a - E , 2008a – d], implicit global models [Irving 2004, Pitaressi 2004], global-local sub-models [Tee 2003, Wong 2003, Zhu 2001, 2003, 2004] and implicit transient analysis with Input-G Method [Luan 2004]. Material deformation under high strain rates, previously, has been incorporated in simulation frameworks using linear-elastic models and elastic-plastic models [Lall 2004, 2005, 2006a-c, 2007a-e, 2008a-d, Xie 2002, 2003, Wu 1998, 2000] for interconnects.

The primary driver in failure of second level interconnects in electronic components during transient events is the flexing and bending of the PCB. Researchers have used the finite element method to examine the plastic strain occurring in solder joints during a drop and shock event and have used a plastic damage criterion to identify the location of potential failure points in BGA assemblies [Zhu 2005]. Chip scale packages (CSP) have also been evaluated using finite element analysis to show that the critical location during testing is the corner copper wire [Wang 2004]. Since bending is the driving factor behind failure during drop events, researchers have explored using three-point and four-point bending tests to develop a reliability model of chip scale packages under curvature load conditions [Shetty 2003].

2.3 Digital Image Correlation (DIC)

Because of their small size, it is not always feasible to place measurement devices directly on test specimens. Test samples may be subjected to extreme loads and temperatures that affect the measurement accuracy of surface mounted measurement techniques such as a strain gage. Non-contact measurement techniques may be preferred over contact methods in situations where either the test specimen is unable to be accessed physically or the test conditions are too severe to allow direct contact with the specimen. Digital image correlation (DIC) is an optical, non-contact, technique that can be used to measure deformation of objects. DIC works by tracking a geometric location on an image and determining the relative displacement of the location based on deformed images. DIC has a huge advantage over normal point measurement techniques such as strain gages since it is capable of extracting full field deformation and strain data.

Previously researchers have evaluated the effects of speckle pattern creation on accuracy of extracting the deformation values and strain value [Zhou 2001, Amodio 2003, Srinivasan 2005].

DIC has been used in electronic packaging to calculate full field deformations and deformation gradient in electronics [Lall 2007c, 2008b-d, 2009, Miller 2007, Park 2007a,b, 2008]. Digital image correlation also been employed for evaluation of stresses and strain in flip-chip dies under thermal loading [Kehoe 2006], to study deformations in printed circuit assemblies for mobile devices [Lall 2007, Miller 2007, Park 2007], material characterization [Park 2007] and for calculating stresses in solder interconnects of BGA packages under thermal loading conditions [Zhou 2001, Yogel 2001, Zhang 2004, Zhang 2005, Sun 2006]. DIC has also been used for evaluating elastic modulus of underfill materials at elevated temperatures during four-point bending tests [Park 2007a, Shi 2007]. DIC based strain measurements technique has been demonstrated to be useful for transient strain measurement in electronic assemblies, in the presence of rigid body motion [Lall 2007, 2008].

2.4 Package Warpage

Warpage of both the electronic package and printed circuit board have become a critical area of concern since the widespread use of surface mount technology in electronics. Co-planarity issues will often occur because of warpage. Electronic packages with co-planarity issues can cause faulty solder joint connections. Warpage in electronic packages may occur as a result of manufacturing processes and thermal loading. The handling of components during the manufacturing process often leaves a residual stress in the electronic package that causes warpage of the package. This is often

true of epoxy molded components where the molding compound tends to shrink quicker that the substrate resulting in a smiley face up warpage configuration. Warpage may also occur during thermal loading because of the mismatch in CTEs between the different layers of the electronic package. The mismatch can cause certain layers of the electronic package to expand faster than others. This mismatch causes warpage to occur. This behavior is of critical importance during high temperature operations such as solder reflow where inadequate co-planarity can easily result in a faulty solder joint.

The JEDEC standard JESD22-B112A defines warpage according the convex or concave shape of the warped package. Warpage is typically measured along the diagonal of the electronic package. The standard specifies the positive or negative sign convention of the warpage value according to the shape of the warpage. A convex warpage has a positive value while a concave warpage has a negative value. The sign convention specified in the test standard is shown in Figure 2-2. Warpage measurements can be taken using various techniques including shadow moiré, digital image correlation (DIC), laser reflection, and projection moiré [JEDEC 2011]. The standard defines the measurement conditions for digital image correlation (DIC). Digital image correlation uses a two camera system in conjunction with glass window thermal chamber. A schematic showing the experimental apparatus prescribed by the JEDEC standard is shown in Figure 2-3.

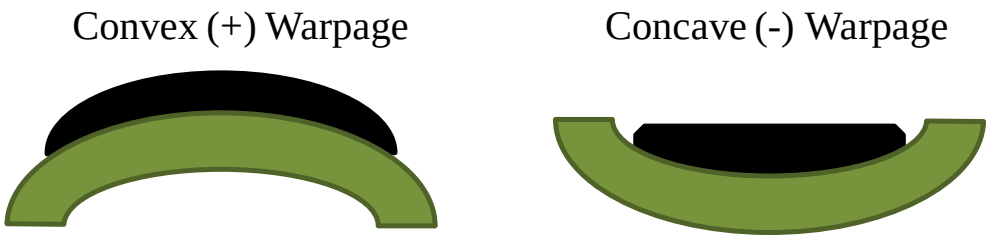


Figure 2-2: Warpage sign convention

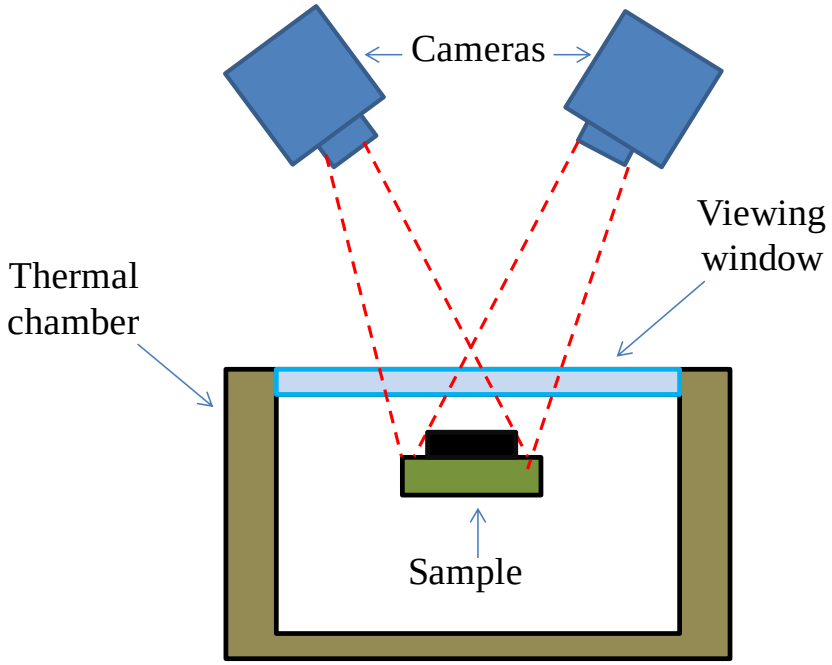


Figure 2-3: Test apparatus set up

Researchers have examined the effects of the injection mold cure time (IMC) and post mold cure time (PMC) on warpage using visco-elastic finite element models [Amagai 2010]. Researchers have shown that materials selection is critical for warpage control. The multiple layers of the electronic package including the mold, substrate, die, and die attach all play a key role in the effect of warpage. Research has been done to study the effects of the epoxy molding compound, die attach, die thickness, and mold cap thickness on warpage [Carson 2007]. Studies have also shown that the shadow moiré technique is an accurate method of measuring warpage in electronic packages [Yen 2008]. Digital image correlation (DIC) has shown to be an accurate form of measurement for thermal warpage occurring in an electronic package [Blackshear 2010]. Finite element modeling has been proven effective in predicting the variation of warpage with respect to different material properties such as substrates, molding compound, and die attach [Tzeng 2007, Sun 2008].

3. Modeling and Reliability Characterization of Area Array Electronics Subjected to High-G Mechanical Shock Up To 50,000g at Multiple Orientations

3.1 Introduction

Electronics in aerospace, avionics, and military applications may be subject to very high g-loads. Ultra-high reliability components are necessary for long-term human presence in space. Conventional drop towers have a limit of 5,000g. To facilitate the need for higher g-levels, an additional fixture that will allow up to 100,000g called the dual-mass shock amplifier (DMSA) has been used. The DMSA increases the mass and inertia-loading imparted by the table to create a larger amplitude pulse. Failure is analyzed at the second level of interconnects. Second-level interconnect reliability is a major area of concern in the electronics industry. During drop testing, components can often fail due to pad cratering, solder joint failure, underfill fillet failures, chip cracking, and copper trace failure.

System-level reliability response is influenced by various factors such as the shock height, orientation of shock, and variations in product and board design [Lim 2002, 2003]. The complex physical architecture typical of electronic products makes it necessary to test solder joint reliability and dominant failure interfaces in various orientations at the product level. The small size of the solder interconnections makes it difficult to mount strain gages at the board-joint interface in order to measure field

quantities and derivatives of field quantities such as displacement and strain. In the current assembly, the addition of the micro-coil interconnect increases the interconnect compliance, and is intended to decouple the component from the printed circuit board. It is expected that the interconnect design will enable the airborne and space electronics to survive the accelerations encountered during launch, separation and re-entry.

Prediction of transient dynamic events has previously been investigated using equivalent layers models [Gu 2005], smeared property models [Lall 2004, 2005], conventional shell with Timoshenko-beam element model and the continuum shell with Timoshenko-beam Element Model [Lall 2006[a,b], 2007[a-e], 2008[a-d]], implicit global models [Irving 2004, Pitaressi 2004], and global-local sub-models [Tee 2003, Wong 2003, Zhu 2001, 2003, 2004]. Material deformation under high strain rates, previously, has been incorporated in simulation frameworks using linear-elastic models and elastic-plastic models [Lall 2004, 2005, 2006a-c, 2007a-e, 2008a-d, Xie 2002, 2003, Wu 1998, 2000] for interconnects.

Digital image correlation (DIC) has been used in the electronics industry in the past for various applications. DIC has been used to measure deformation gradient and full field displacement in electronic assemblies subjected to drop and shock [Lall 2007[b], 2008[a,b], Miller 2007, Park 2007[a,b], 2008], damping ratio on the surface of the board [Peterson 2008] examination of velocity rotation, bending on portable products subjected to impact test [Scheijgrond 2005], stresses in solder interconnects of BGA packages under thermal loading [Bieler 2006, Rajendra 2002, Sun 2006, Xu 2006, Yogel 2001, Zhang 2005, Zhou 2001], stresses and strain in flip-chip die under thermal loading [Kehoe 2006]. In this study, DIC is used to calculate deformation of the board

assemblies during the drop event.

A JEDEC form factor board has been tested. In addition to the micro-coil spring (MCS) components, the packages tested include leaded components, micro-lead frame components, ball grid arrays, through-hole components, transistors, plastic grid arrays, and ceramic grid arrays. The focus of the paper will be the reliability of the ceramic MCS grid array. Assemblies have been subjected to varying g-levels at a 0°, horizontal orientation. Benchmark tests are run to determine appropriate test levels. In consumer products, the JEDEC drop-test [JESD22-B111 2003] is used to address board-level reliability of components, which involves subjecting the board to a 1500g, 0.5 ms pulse in the horizontal orientation. In this study, the three test levels used for the horizontal orientation include 30,000g, 40,000g, and 50,000g. Continuity has been monitored in-situ using daisy chained components and a wheat-stone bridge configuration. Transient strains and displacements are measured using high speed cameras in conjunction with DIC software. Reliability-performance for MCS interconnects subjected to the various high g-levels is determined and compared to solder column interconnects. Failure modes are determined.

3.2 Test-Vehicles

A JEDEC form factor test board is used with dimensions 132mm×77mm×1.5mm. The component layout is different than a traditional JEDEC form-factor test board and has been modified to accommodate the components in the end application. The test board has a total of 32 components with 14 unique component types. The test board and component types are shown in Figure 3-1.

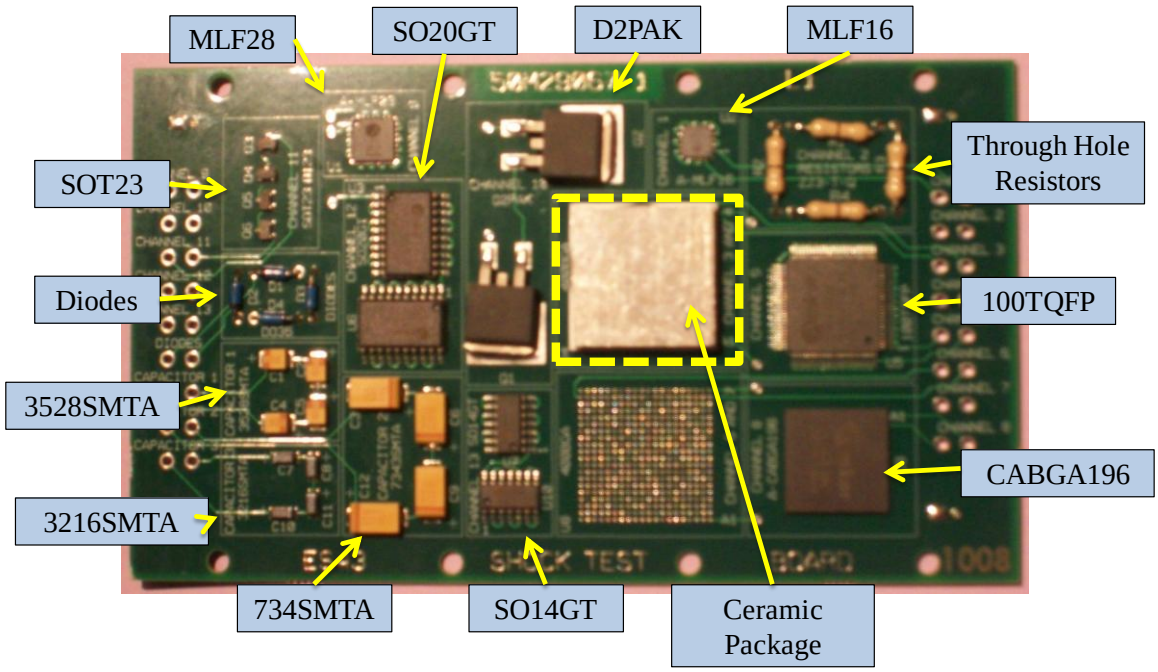


Figure 3-1: Test Board

Two types of board assemblies have been manufactured. Only the interconnect type for the ceramic package is changed between the two-types of board assemblies. In board assembly-A, the ceramic area array package is populated with a micro-coil springs, while the other assembly, termed as board assembly B has solder column interconnects. The component with the micro-coil springs and the component with ceramic columns has a 20x20 array of interconnects with a pitch of 1 mm. The MCS are fabricated using a 3.4 mil diameter beryllium copper core wire post plated with 100 µin of tin lead (Sn63Pb37). The springs have a diameter of 20 mils and are 50 mils in length. The coils have a pitch of 10 mils. There are two to three closed coils at the ends of the springs. A 6-mil stencil has been used to attach the MCS at both the PCB and ceramic sides. Tin-lead solder stenciled on the printed circuit board has been used to attach interconnects [Strickland 2011]. A side by side schematic of spring dimensions and the actual MCS interconnect is shown in Figure 2. The solder columns are made with Sn5Pb95 and are attached with

Sn10Pb90 using an 8-mil stencil. The two different alloys of tin-lead solder have different melting temperatures. The melting temperature of the column solder is high so the actual column of solder does not melt during reflow processes. They have a height of 87 mils and a diameter of 18 mils. The solder column interconnect is shown in Figure 4. An aluminum mass is attached to the ceramic substrate to simulate the mass of an active ceramic package.

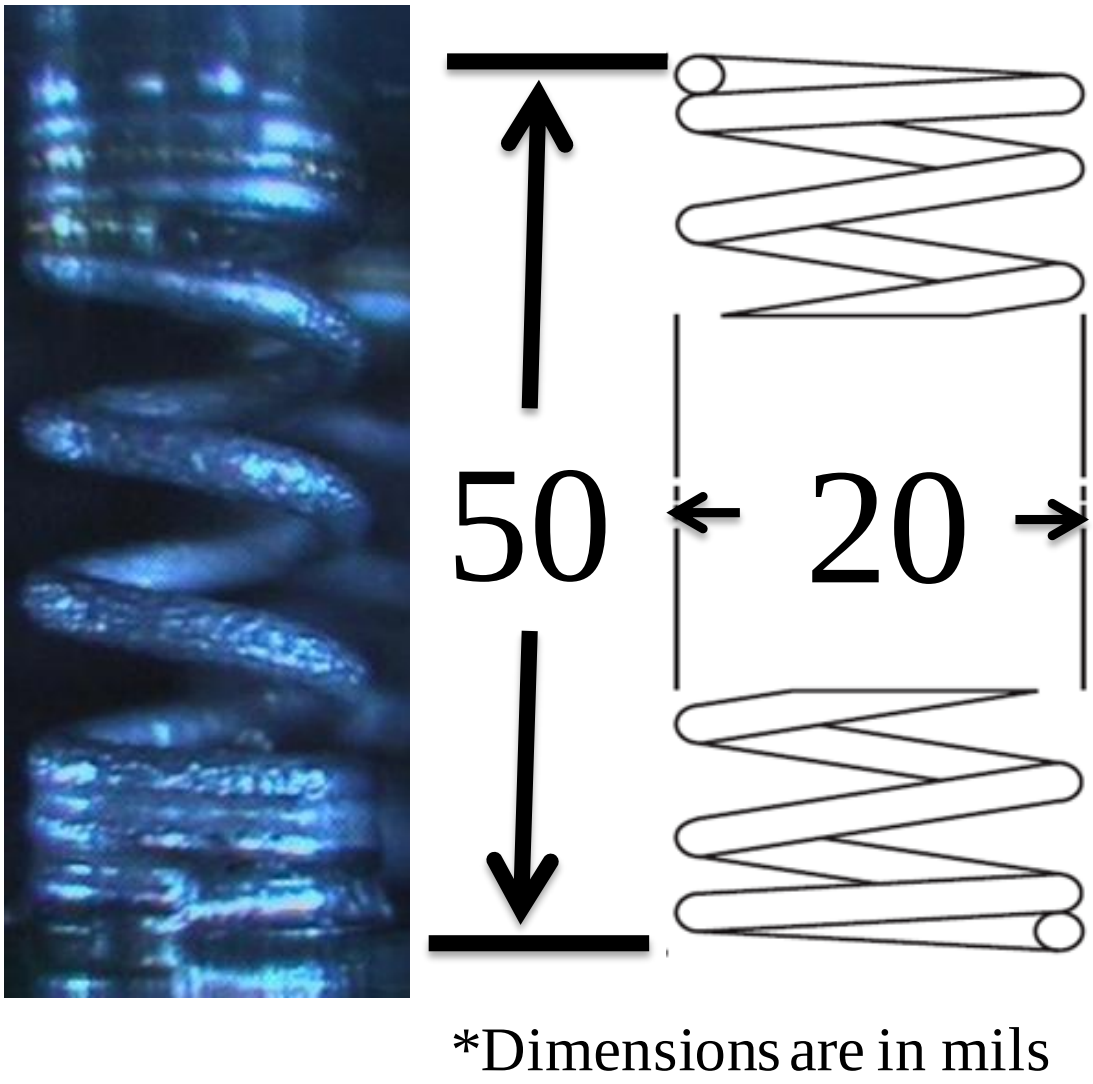


Figure 3-2: Schematic of the MCS Interconnect

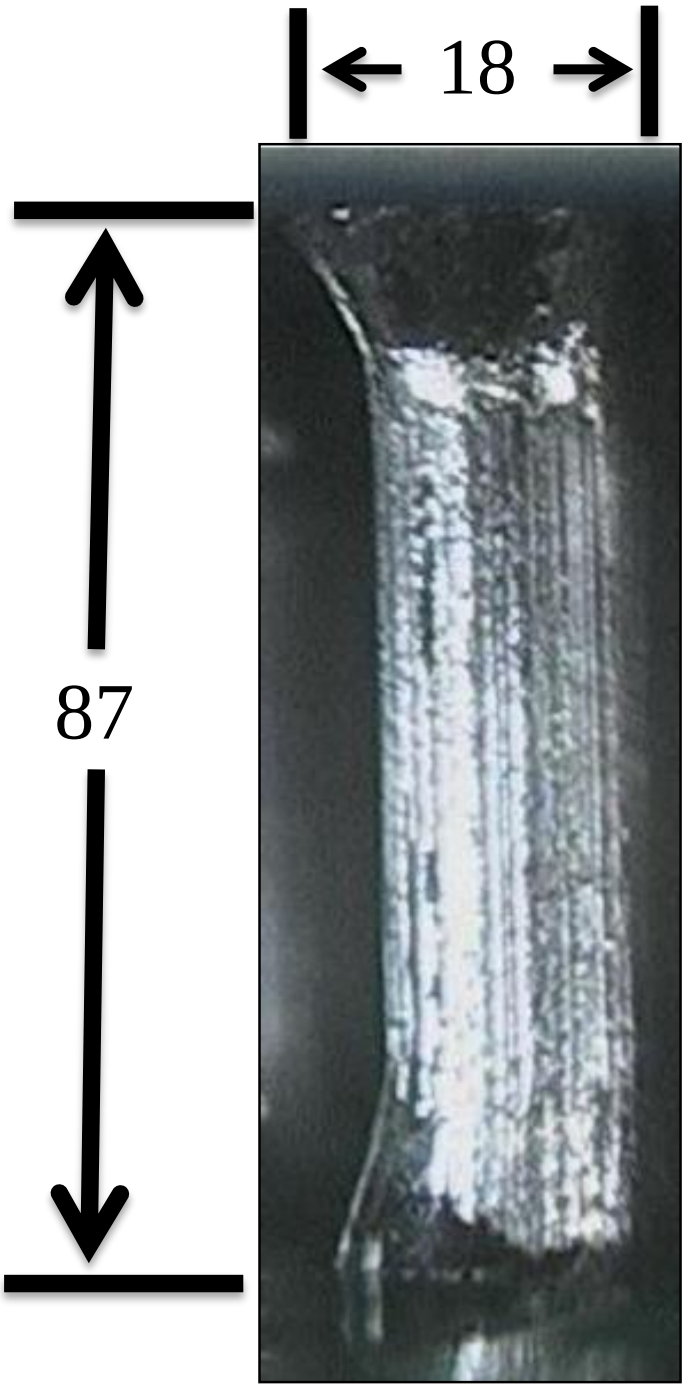


Figure 3-3: Column Interconnect

3.3 Experimental Set-up

Previously, test assemblies have been subjected to 1500g, half millisecond pulses in accordance with the JESD22-B111 test standard [Lall 2004, 2006[a], 2006[b]]. Proper pulse shape has been achieved through adjusting both the drop height and pulse shaping material between the two surfaces. The Lansmont Model-23 drop tower is used for the drop tests. Figure 3 shows a test vehicle mounted on the drop tower and a schematic of the high speed camera acquisition system. High speed cameras have been used to monitor the transient deformation of the board during a 1500g drop test. Figure 3-5 shows the deformation of the board captured by the high speed camera. High speed camera images are also used for DIC.

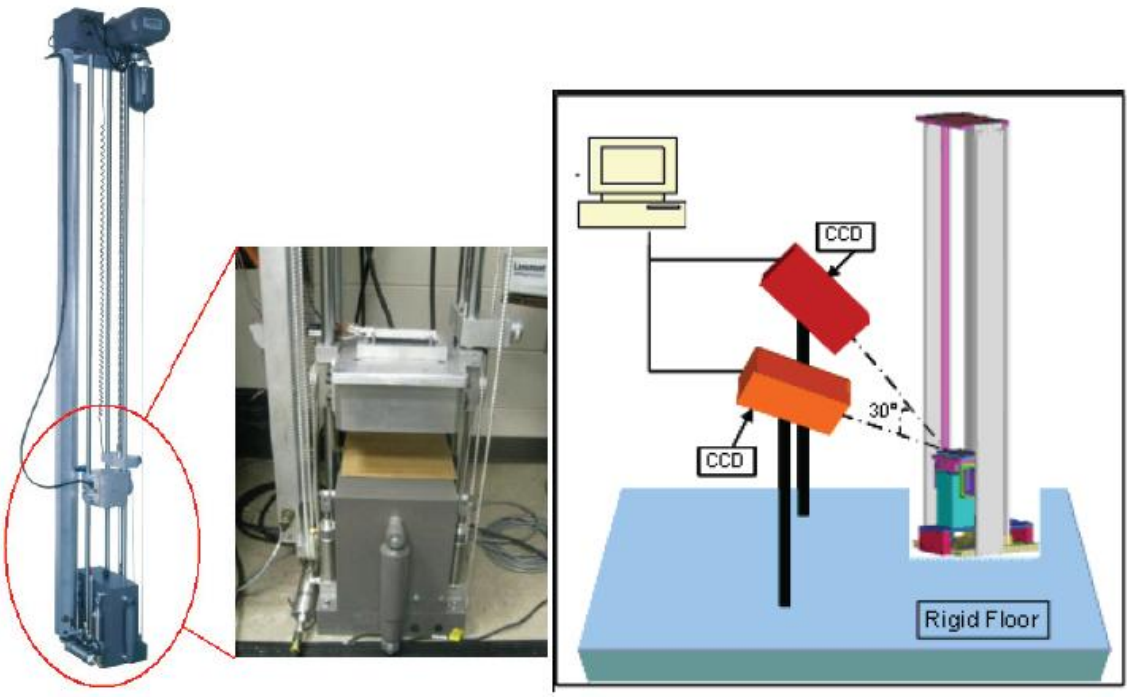


Figure 3-4: Drop Test Setup

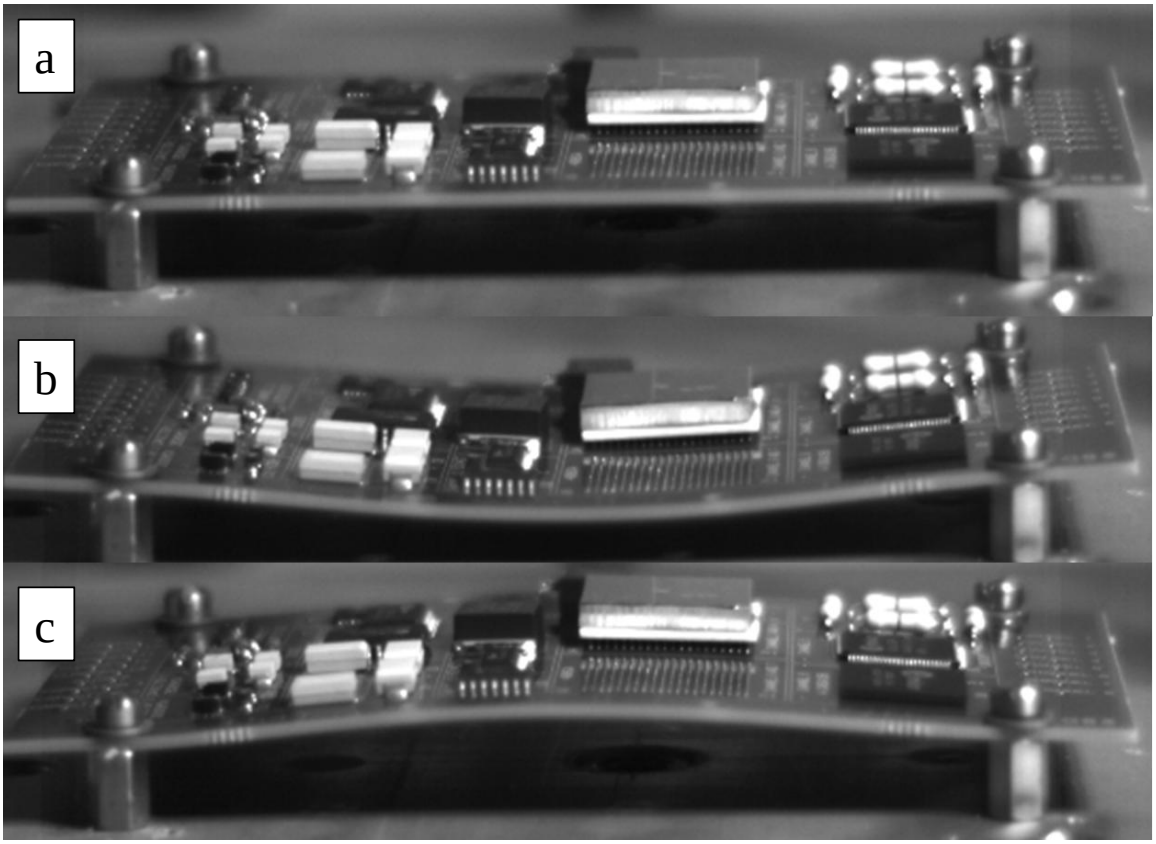


Figure 3-5: 1500g board deformation (a) undeformed (b) negative deflection (c) positive deflection

Daisy chained packages are monitored using a high-speed data acquisition system at a high sampling rate. The drop event is also simultaneously monitored with high speed video cameras operating up to 15,000 frames per second. Failures are defined in accordance with the IPC-SM785 standard. A Wheatstone bridge configuration is used to monitor the continuity of the packages. The repeatability of the drop test has been verified. Figure 3-6 shows the repeatability of the pulse shape during multiple drop tests. There is only a 4% error between the first drop and the 250th drop.

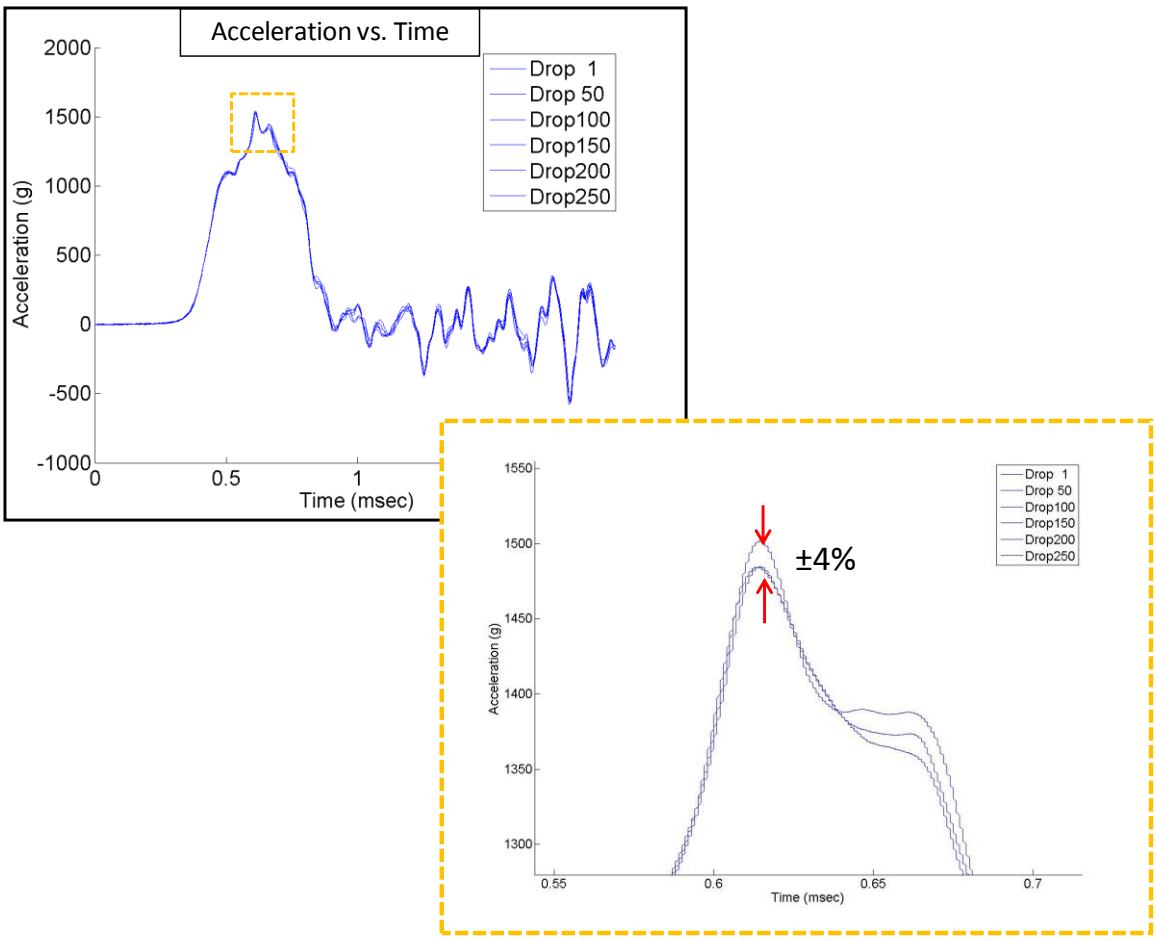


Figure 3-6: Drop test repeatability

Horizontal Orientation High-G Experimental Set-up using a DMSA

To achieve g-levels above 5000g, a special fixture termed the Dual Mass Shock Amplifier (DMSA) has been used for this test. A schematic of the DMSA can be seen in Figure 3-7. In this paper, the DMSA has been used at magnitudes up to 50,000g. The base fixture is attached to the drop tower table using connectors. Acceleration is monitored for the secondary drop table. Pulse shaping materials are used to achieve the desired pulse shape and peak acceleration for the base fixture and the secondary table. The pulse duration of a high-g drop test is much shorter than a 1,500g test. During a

high-G test, bungee cords are used to accelerate the test vehicle to impact instead of allowing a free fall drop. Test boards are mounted on the secondary drop table on the DMSA. The initial impact of the base table reverses the velocity of the base fixture while the secondary table keeps falling down. The second impact occurs when the base fixture and secondary drop table collide. Dampers and springs are used to control the motion of the secondary drop table. The guide rods on the DMSA are lubricated before each drop test session to ensure consistent accelerations are achieved.

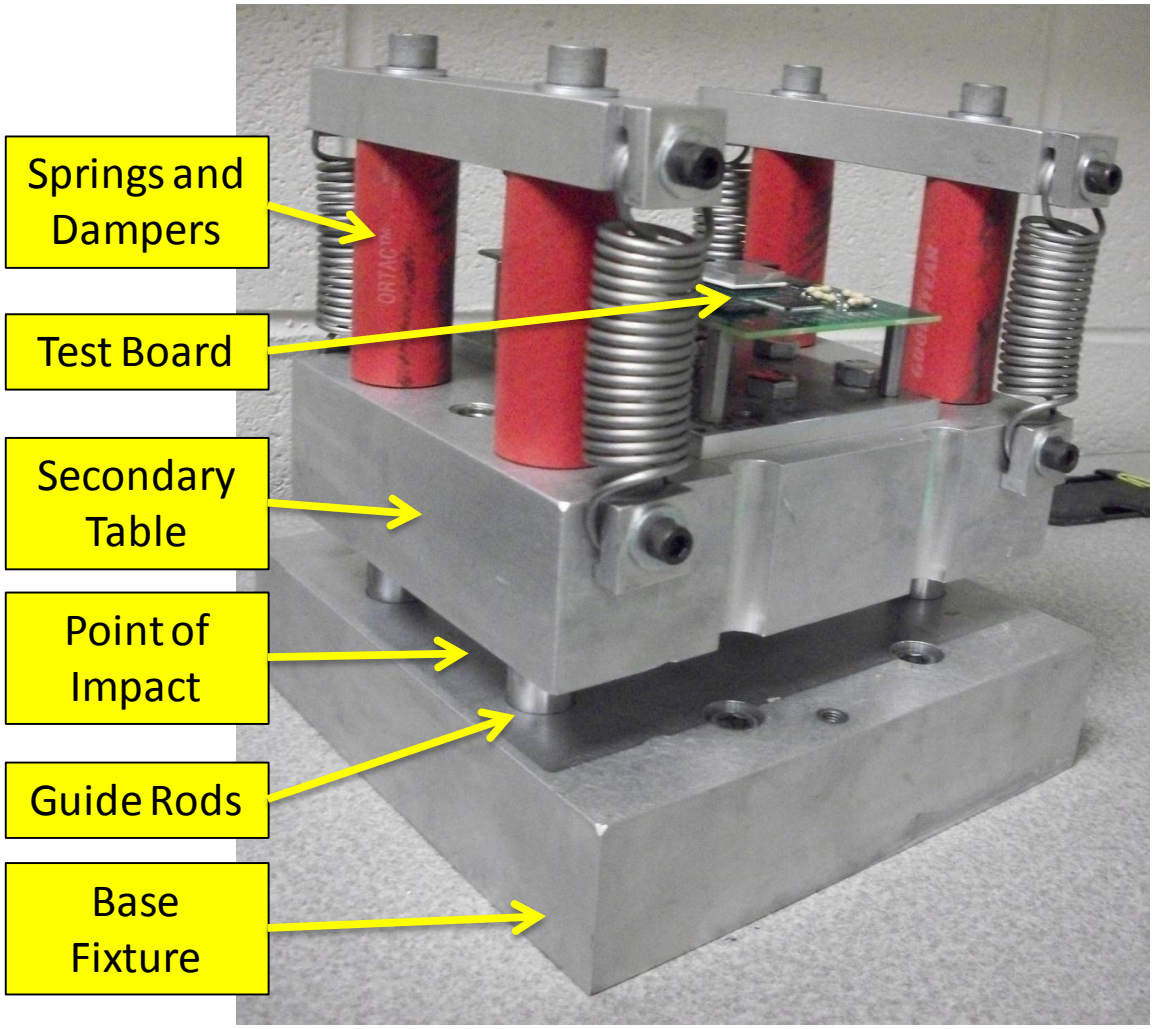


Figure 3-7: Dual Mass Shock Amplifier (DMSA)

Figure 3-8 shows a schematic comparison between a standard drop test and a high-G drop test using a DMSA. A standard drop tower set up consists of three main components: base table, seismic table, and pulse shaper. The high-g setup includes a secondary drop table with springs and dampers attached. The secondary drop table requires its own pulse shaping material. Previously, g-levels above 5,000 could not be achieved due to the limitations of the drop tower. According to the manufacturer, there is a risk of shearing connectors if threshold levels are exceeded. The DMSA has been developed to allow testing above 5,000g without risk of mechanical failure in the drop tower. Brown, conical, plastic pulse shapers have been used to reduce the g-level on the base table at the initial impact. The secondary impact occurring between the secondary drop table on the DMSA and the base table of the drop tower is where the higher g-levels are achieved.

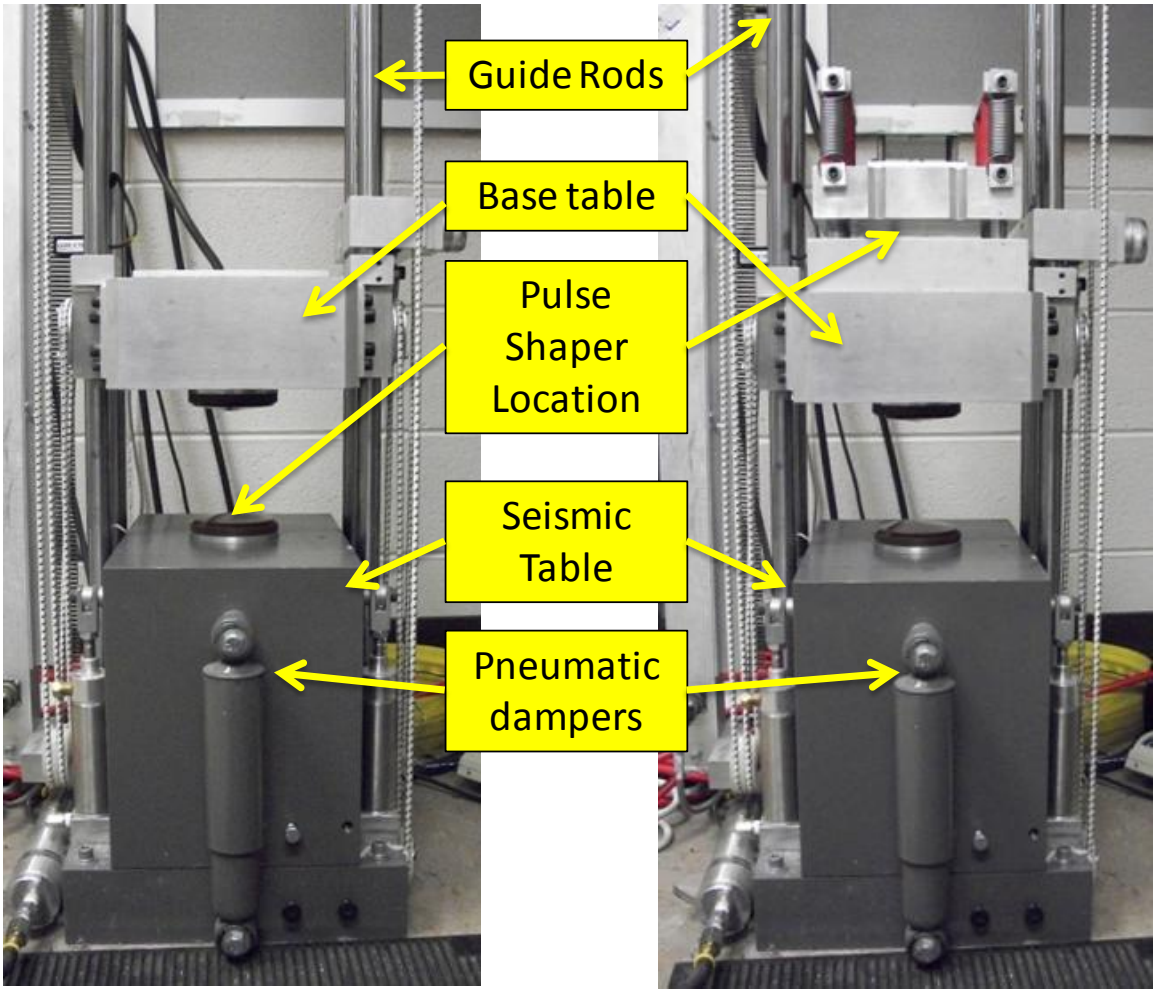


Figure 3-8: Standard drop test set up vs. high-g test set up

Vertical Orientation Experimental Set-up

Drop testing for components in the vertical orientation is achieved by using a custom built fixture. The experimental set up is the same as a JEDEC standard 1500g with the exception of using a specialized fixture. The fixture allows for the mounting of JEDEC form factor board assemblies in the vertical, 90° orientation. The fixture is shown in Figure 3-9. As shown in the figure, the drop direction is still the same as a horizontal orientation test but the board orientation is different. The board is mounted using stand-off screw holes. A mounting hole for an accelerometer has also been threaded into the fixture to allow monitoring of the acceleration during drop test. The test levels used for this orientation are 2000g, 2250g, and 2500g. Pulse shape and peak acceleration is achieved by adjusting the drop height and pulse shaping material. A schematic of the drop test set up for the vertical orientation with the custom built fixture is shown in Figure 3-10.

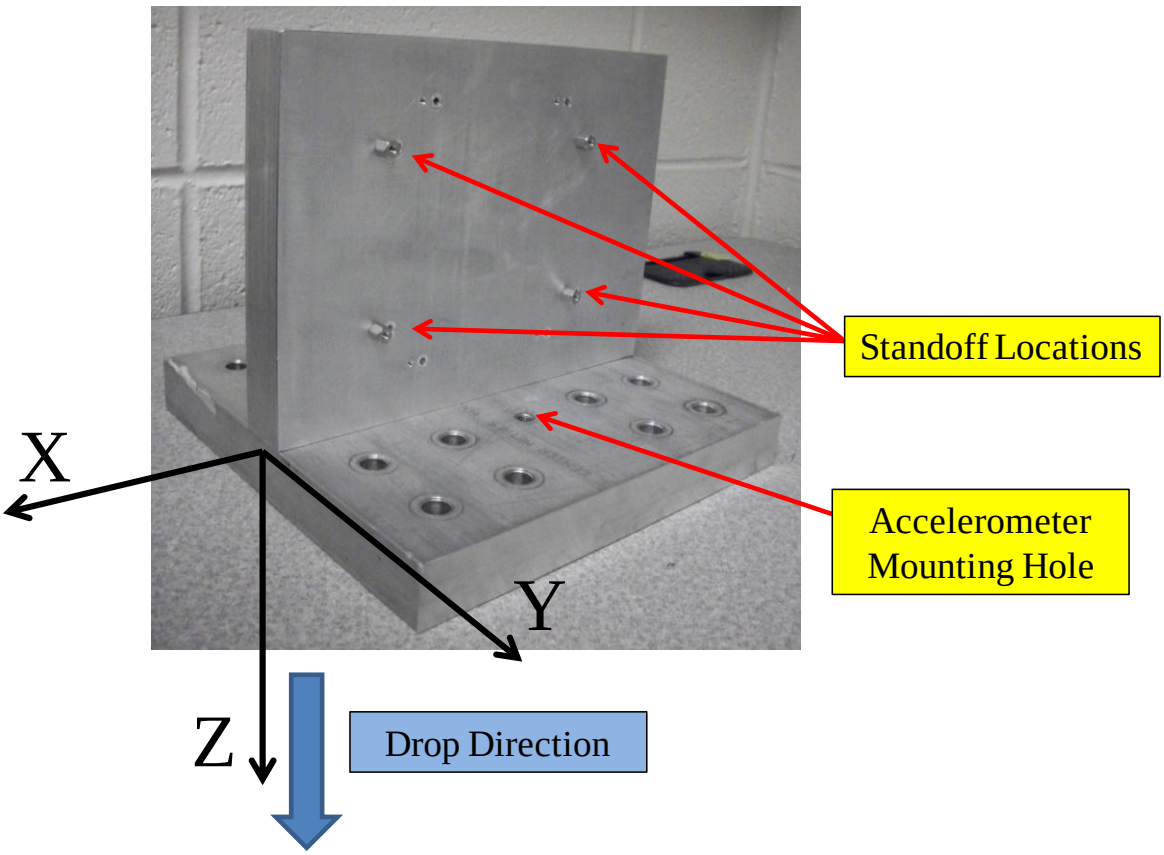


Figure 3-9: Custom drop fixture for vertical drop testing

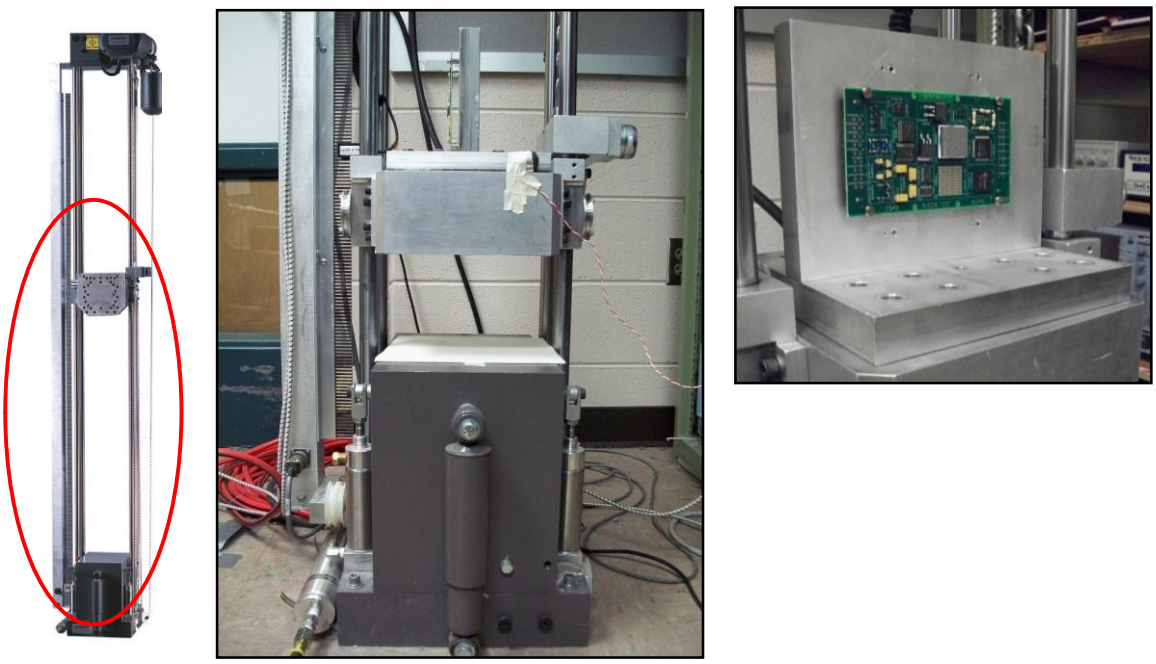


Figure 3-10: Drop test set-up for vertical orientation

3.4 Benchmark Testing

Benchmark tests are performed to determine the appropriate levels to perform the drop tests. Criteria examined during benchmark tests include strain, package continuity, and deflection. Package continuity is monitored using a high speed data acquisition system in conjunction with a wheat stone bridge configuration. Deflection contours are observed with DIC. High speed cameras are used to observe package deflection during a high-G drop. The test levels used for the horizontal orientation benchmark test are 10,000g, 20,000g, 30,000g, and 40,000g.

Horizontal Orientation Benchmark Testing

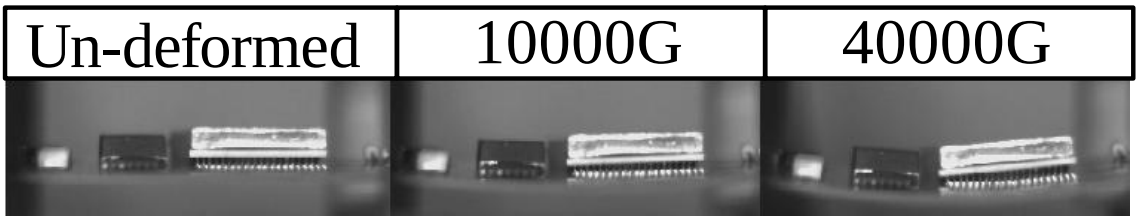


Figure 3-11: Peak deflection close up

High speed cameras were used to capture the deflection occurring during the benchmark tests for the horizontal orientation. Figure 7 is a close-up captured image of the peak deflection for the minimum and maximum levels of the benchmark tests, 10,000g and 40,000g respectively. The board deflection at 40,000g is much higher and will result in higher strains at the board level and the secondary interconnect level. Figure 8 and Figure 9 show a comparison of the transient deformation of the board assembly at shock-levels between 10,000g to 40,000g. There is a progressive increase in board deflection as the shock level is increased from the minimum to the maximum. Significantly higher deflections are observed at 40,000g. Figure 10 shows a detailed sequential break down of the deflection occurring during a 40,000g drop test. Figure 10a shows the initial deformation that occurs in the negative direction while Figure 10b shows the reverse deflection that occurs immediately after the initial deflection. Figure 11 shows the board mounted on the DMSA during 40,000g test. The un-deformed state is pictured in Figure 11a and the maximum board deflection is pictured in Figure 11b. Figure 11a and Figure 11b are also pictured side by side to show the large deflection occurring during these drop tests. High speed videos confirm that larger deflections occur during the 40,000g drop test compared to the standard 1,500g JEDEC drop test.

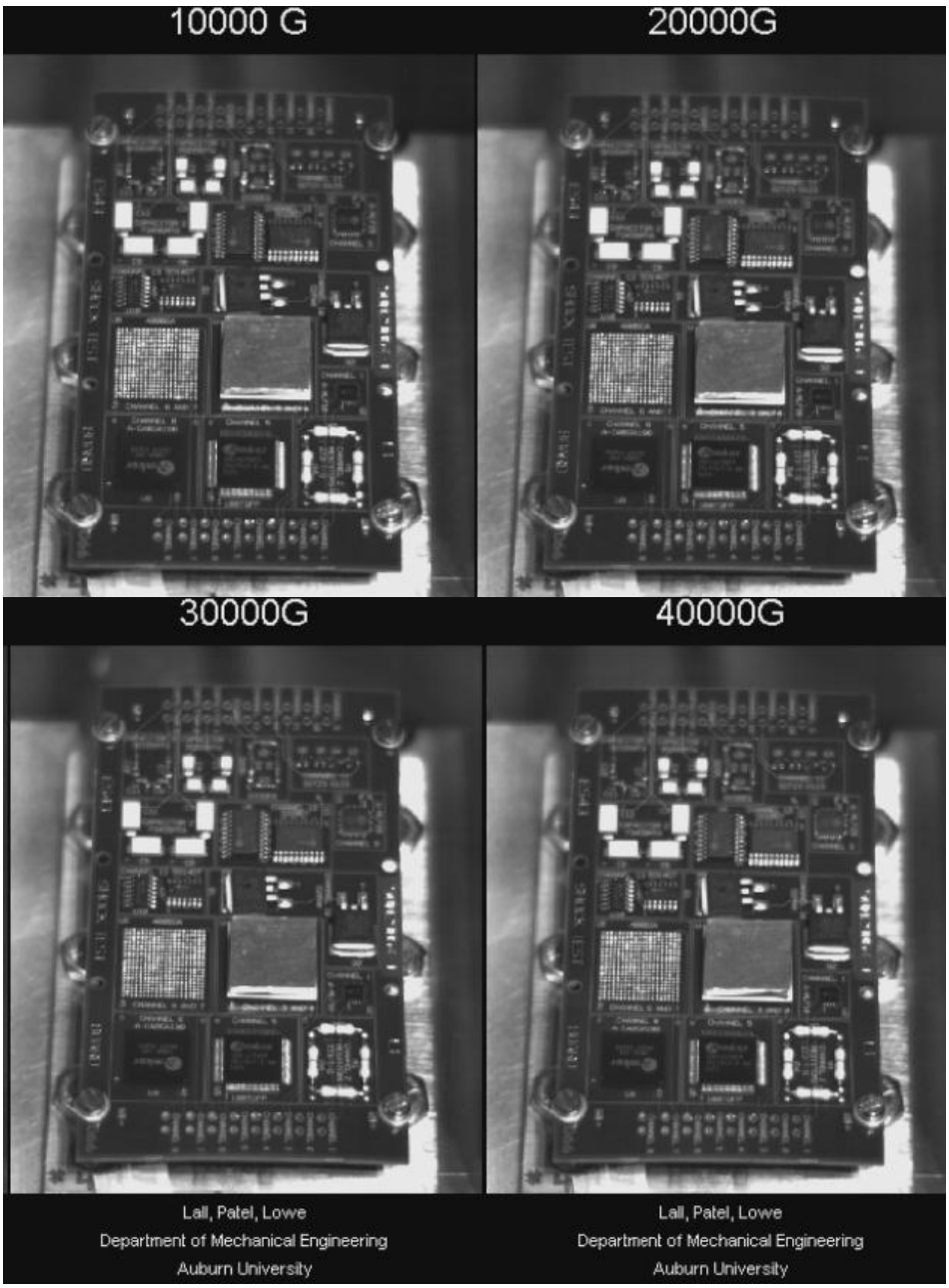


Figure 3-12: Board deflection for benchmark test

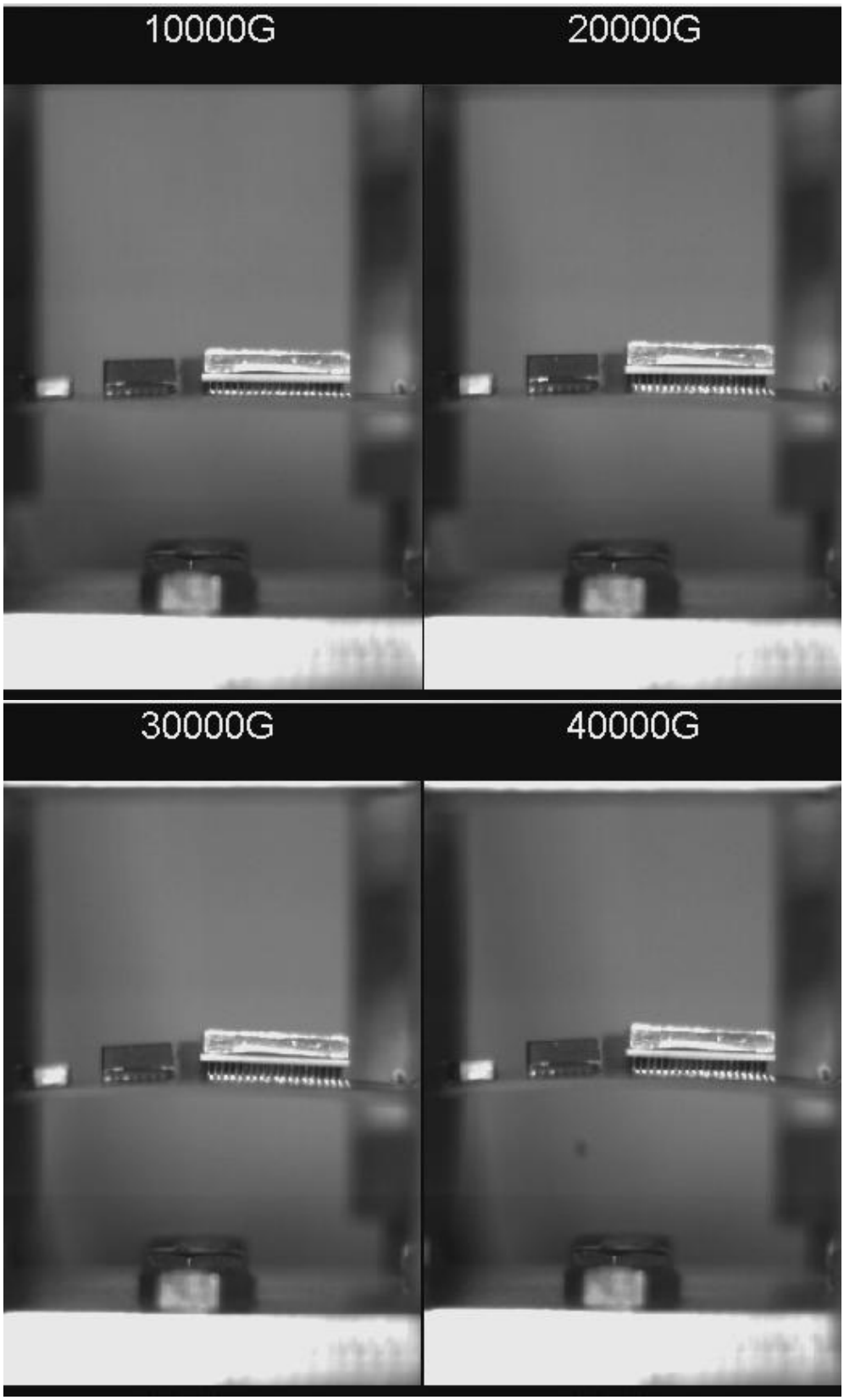


Figure 3-13: Board deflection side view

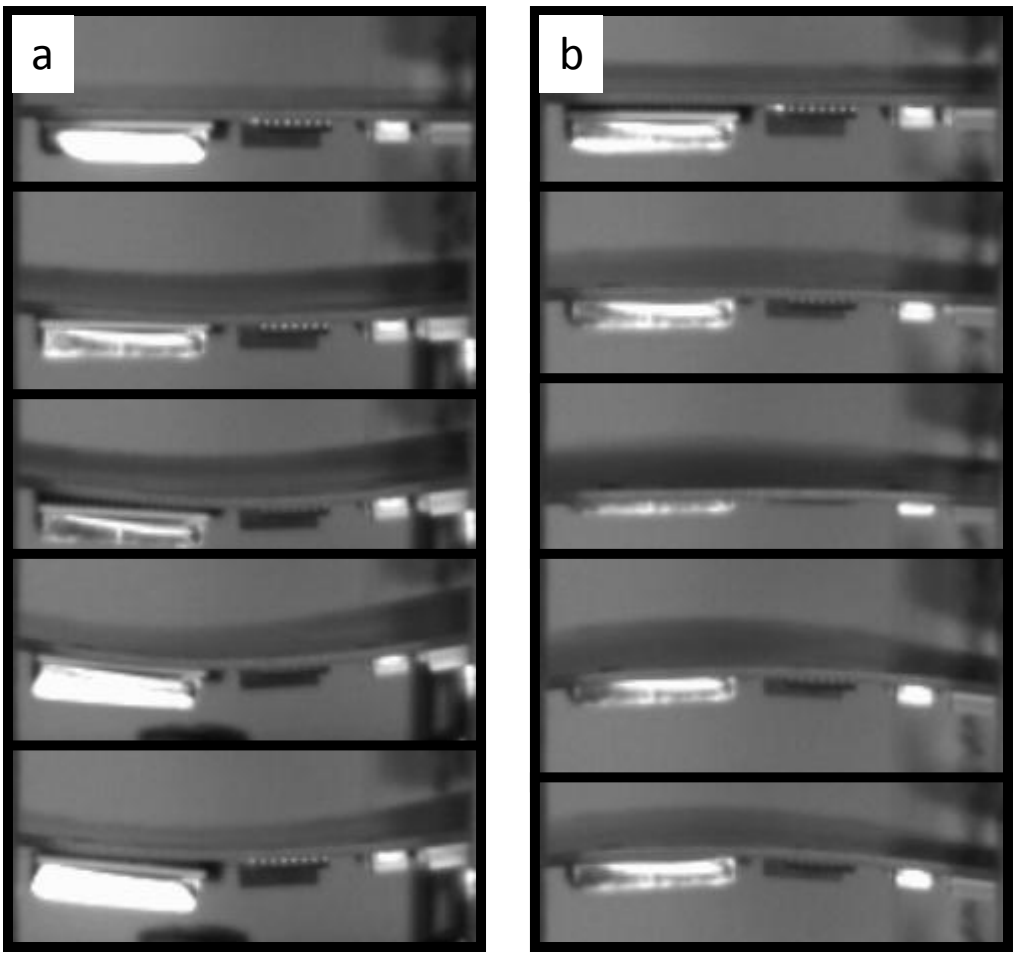


Figure 3-14: Detailed board deflection

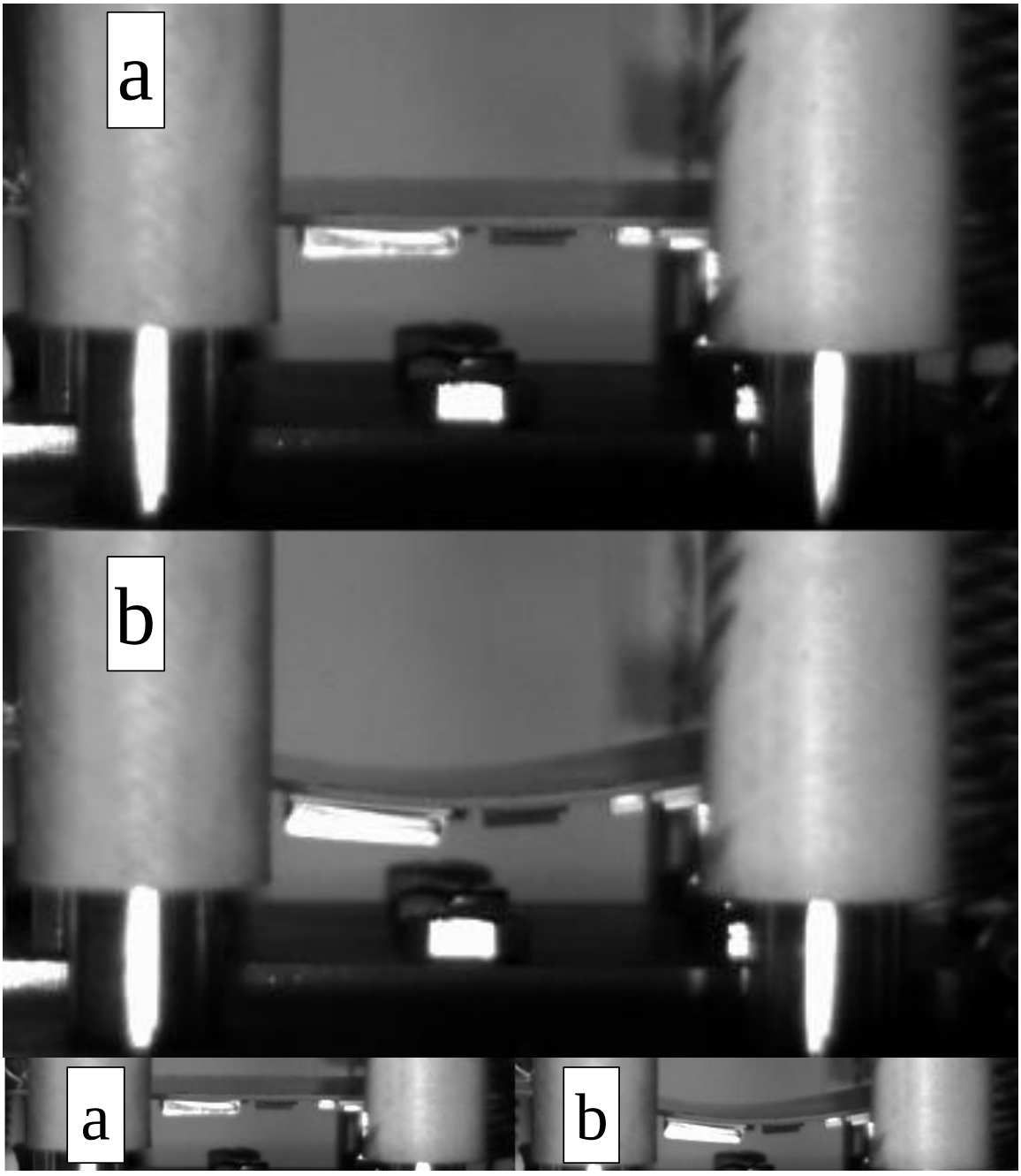


Figure 3-15: 40,000g (a) Un-deformed (b) Deformed

Deformation on the board is measured using a strain gage. The strain gage is mounted at the center of the printed circuit board on the bottom side, the side with no components. The strain gage has been mounted at this position since the maximum board level strains occur at the center of the printed circuit board. The effect of high-g testing on strain value has been evaluated by comparing strain values between a JEDEC standard 1500g drop test and a high-g drop test of 50,000g. The strain comparisons show that a much larger strain occurs during the 50,000g test. Figure 3-16 shows the strain levels observed at the center of the test board on the PCB on the bottom side for the two drop test configurations. Strain is measured along the length of the board. Significantly higher strains are observed for the high-g test case. The printed circuit board is experiencing nearly twice the amount of strain during the high-g drop.

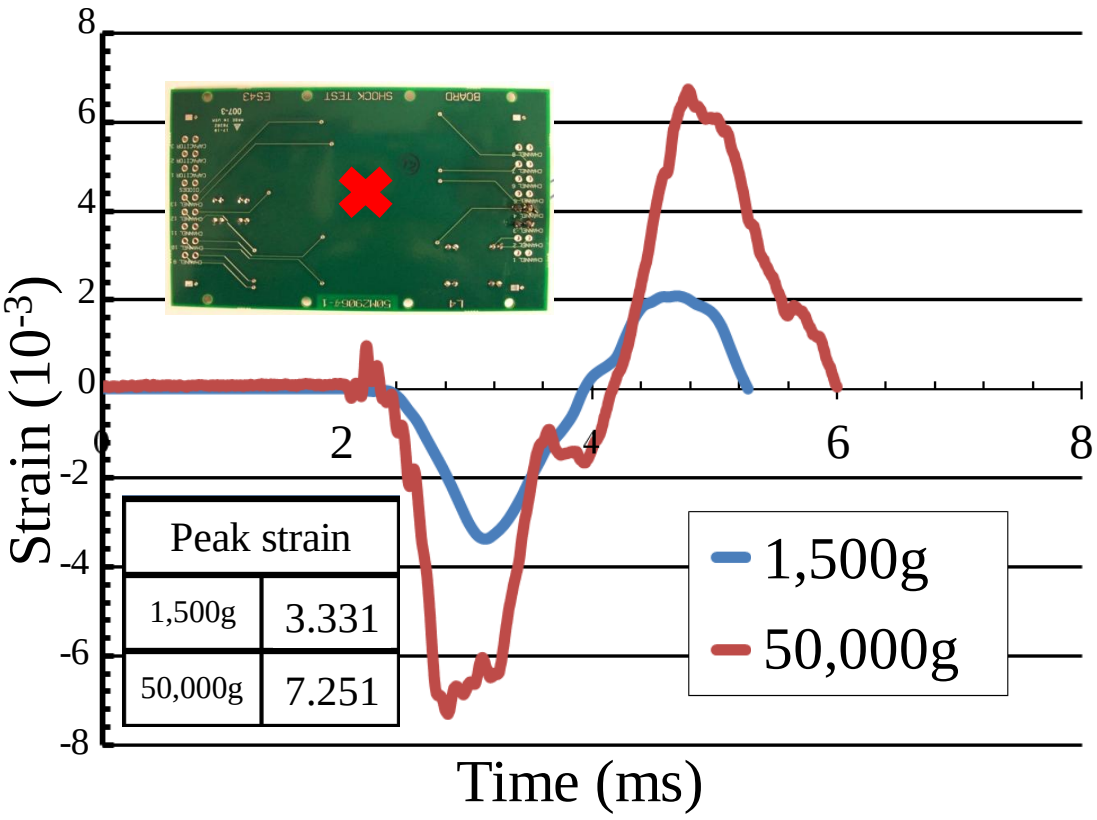


Figure 3-16: Strain comparison 1500g vs 50,000g

The benchmark results are used as standard to determine the appropriate test levels. The height limitations of the drop tower will allow a maximum testing level of 50,000g. Accordingly, the maximum test level used for this study is 50,000g. A low-level and mid-level shock event has been used to study the effects of g-loading on interconnect reliability. The low, mid, and high shock levels are 30,000g, 40,000g, and 50,000g respectively. A plot showing the acceleration of the fixture at each test level is shown in Figure 3-17.

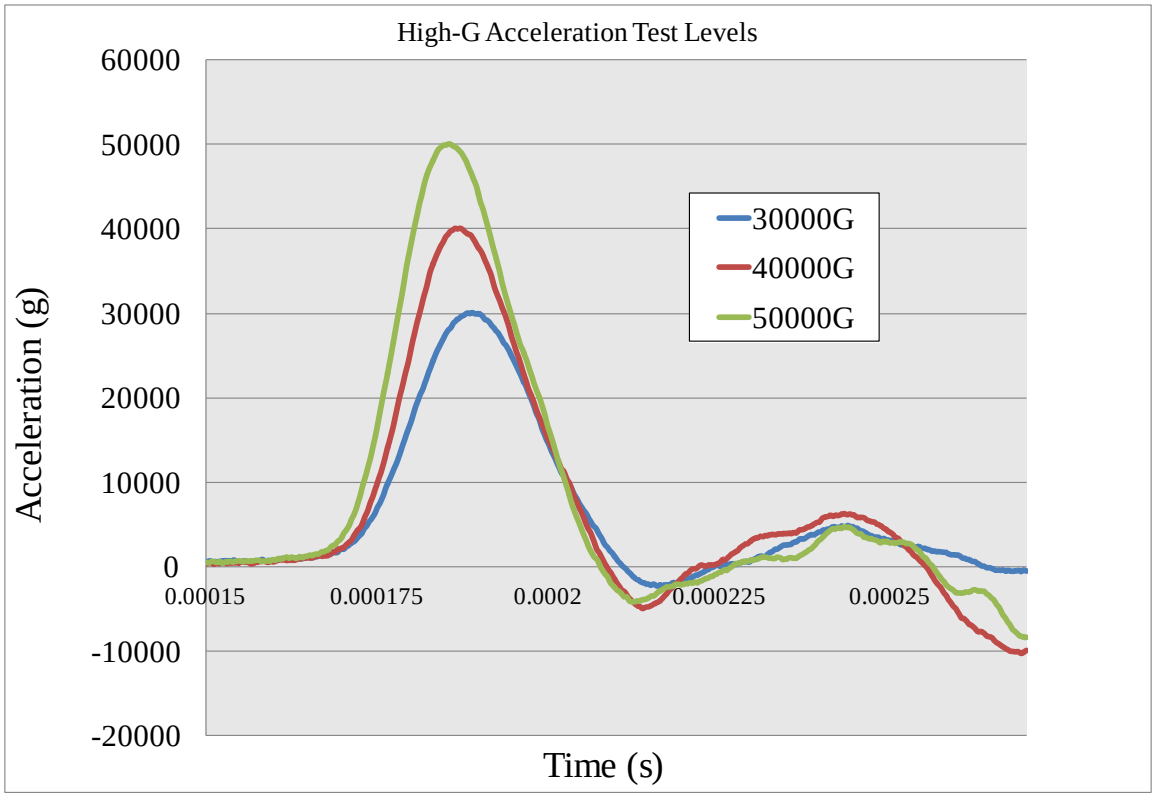


Figure 3-17: High-G acceleration test levels

Vertical Orientation Benchmark Testing

High speed cameras were used to capture the deflection of the packages during the benchmark tests for the vertical orientation. A zoom lens attachment is used to observe the deformation of the micro-coil spring and column interconnects. Large deflections were observed in the micro-coil spring interconnect ceramic package. Figure 3-18 shows captured frames depicting one cycle of deflection for the MCS interconnects during a 2000g vertical orientation drop test. Figure 3-19 shows a close-up view of the MCS interconnects along with a schematic showing the direction of the spring during each phase. Compression and extension of the springs is observed. Figure 3-20 shows the deflection of the column interconnects for a 2000g drop in the vertical orientation. Very little deflection is observed.

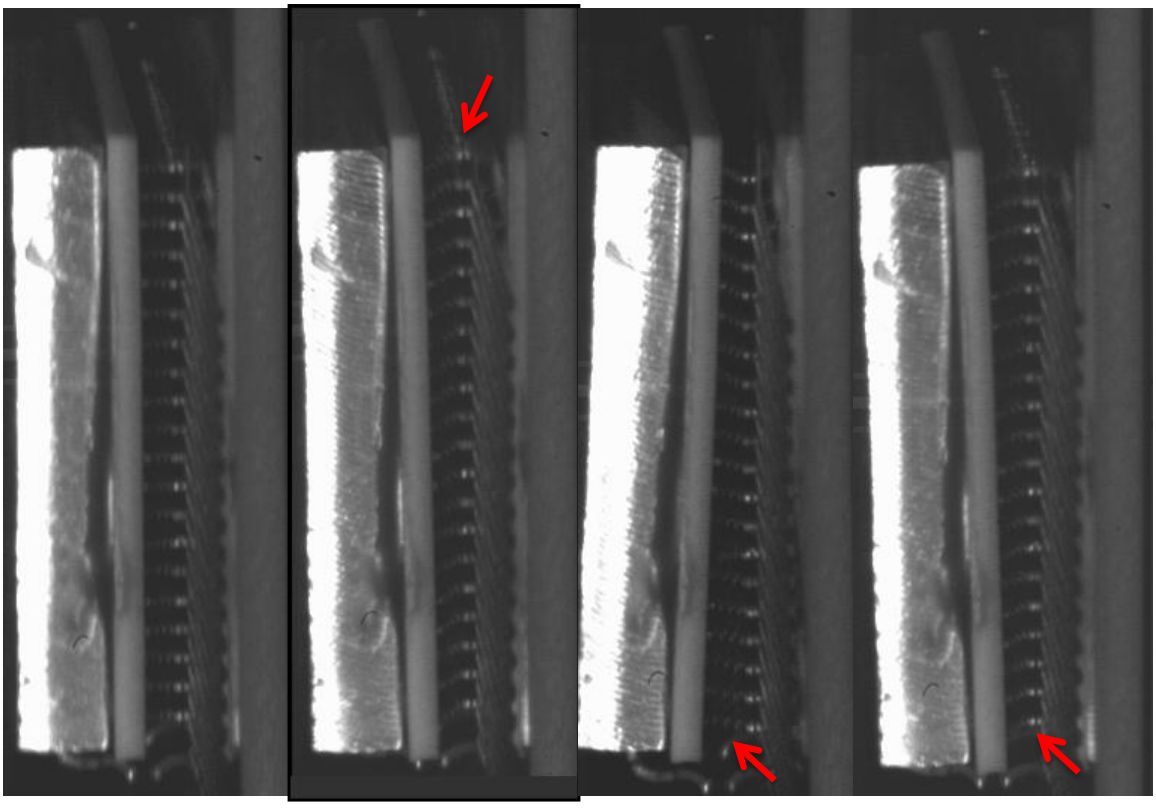


Figure 3-18: MCS deformation for a 2000g drop

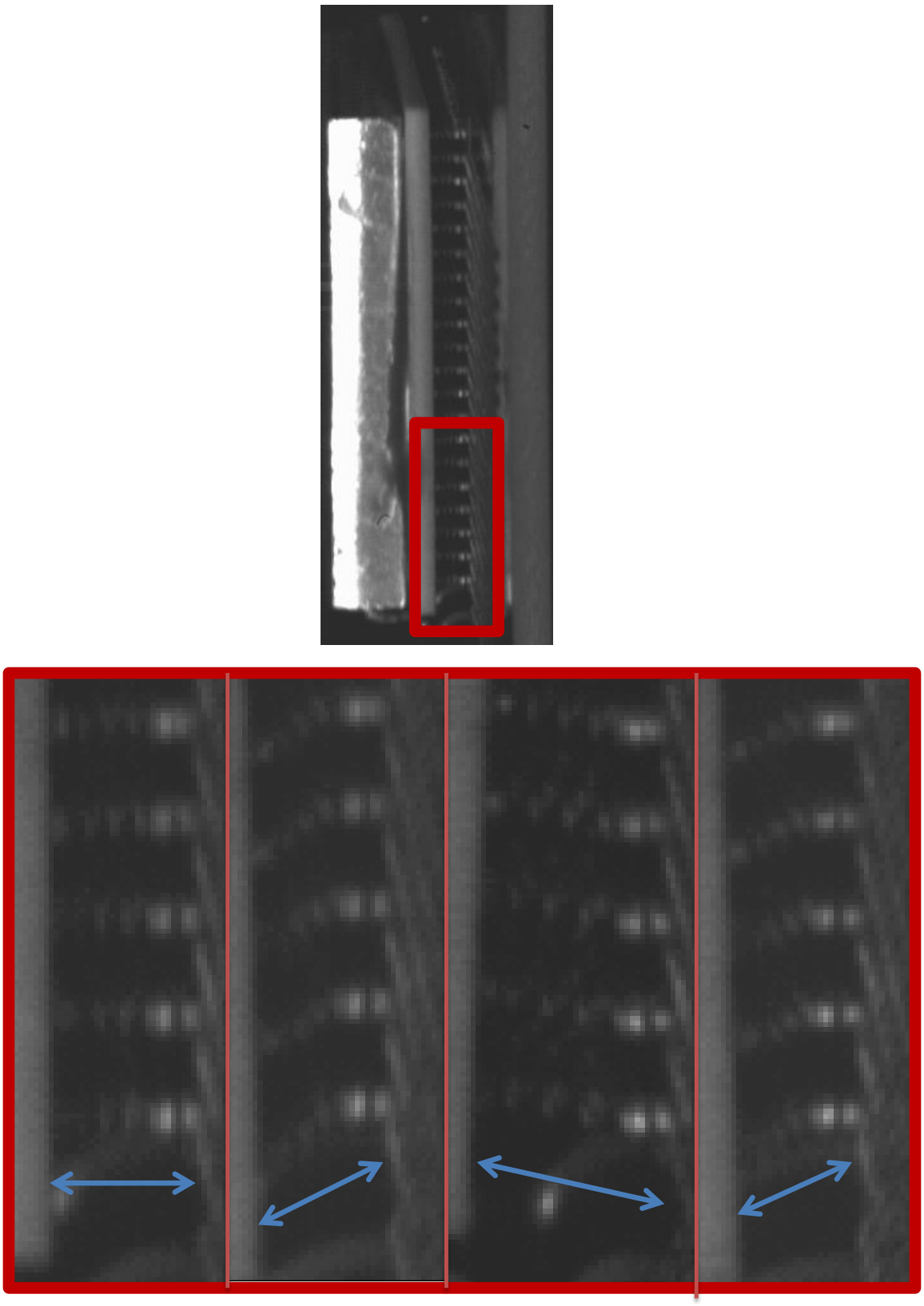


Figure 3-19: MCS deflection close-up

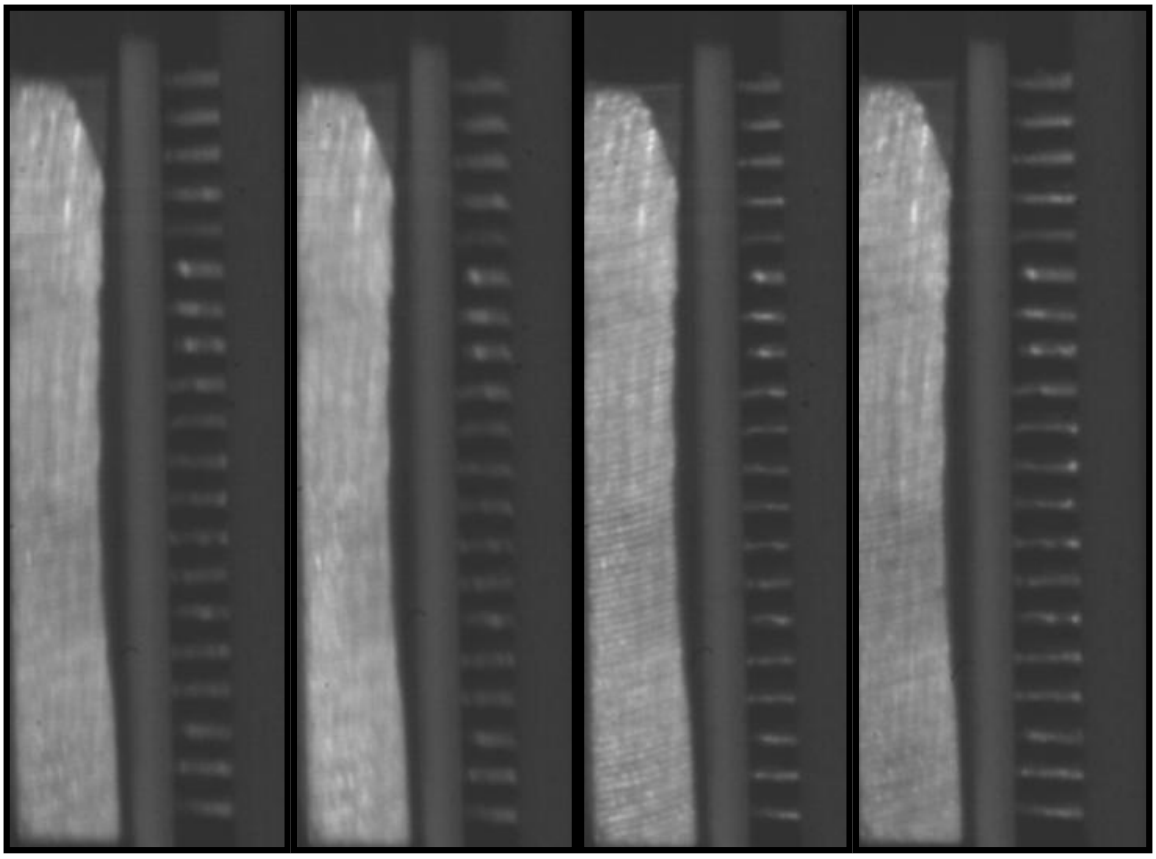


Figure 3-20: Column interconnect deformation for a 2000g drop

3.5 MCS vs. CCGA: Reliability Analysis

Strain comparisons have been made for the different test levels to determine the effect g-loadings have on strain levels for the printed circuit board. The strains are measured at the center of the board on the bottom side. The strain gage is oriented along the length of the board to measure strain along the x-direction. Measurements have been taken at the center of the board since the largest strains will occur at this location during a drop event. Peak strain values have been reported on a table in the figure as well. The peak strain values increase as the test levels increase.

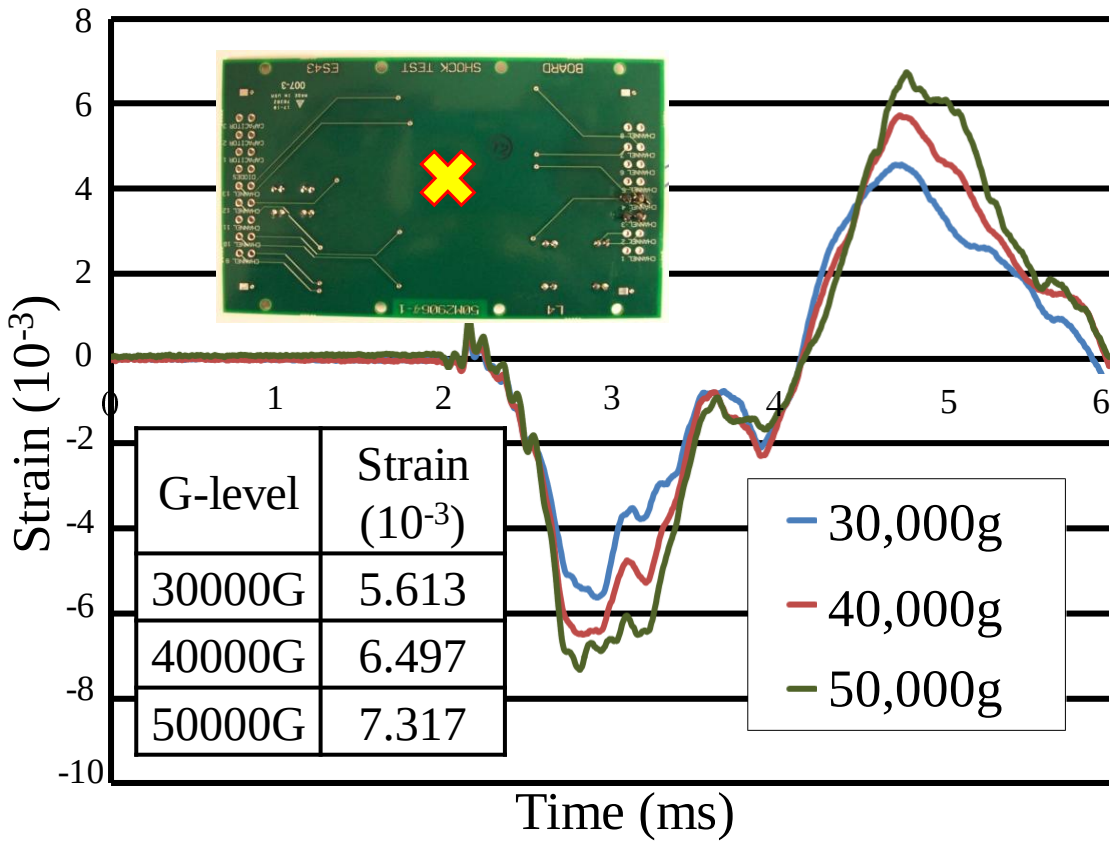


Figure 3-21: Strain comparison for high-g test levels

Horizontal Orientation Reliability Results

Reliability of both the MCS and the CCGA board assemblies have been analyzed using daisy chained in conjunction with a high speed data acquisition system. Resistance of the packages has been monitored using a modified wheat stone bridge configuration. The failures have been defined using the IPC-SM785 standard. The failure data for both board assemblies have been reported in table format in Figure 3-22 and Figure 3-23. The failures have been reported for the low, mid, and high test levels. Each cell in the table represents a tested sample. Five samples have been tested for each test level with a total

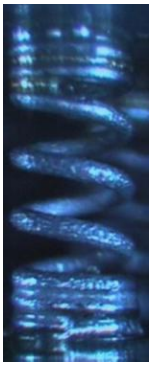
of fifteen samples tested for each board assembly. Better reliability is generally seen for the MCS board assembly although there is some variance in the failure data.

CCGA

G-level	Drops to Failure				
30,000g	4	7	9	8	8
40,000g	7	5	5	4	6
50,000g	4	4	4	5	4

*Failure is defined as an open circuit in the daisy chain using IPC-SM785 standard

Figure 3-22: CCGA horizontal orientation high-g reliability results



MCS

G-level	Drops to Failure				
30,000g	30	21	36	43	31
40,000g	13	10	17	20	26
50,000g	11	1	10	7	5

*Failure is defined as an open circuit in the daisy chain using IPC-SM785 standard

Figure 3-23: MCS horizontal orientation high-g reliability results

ANOVA analysis has been performed to report a graphical representation of the reliability of each board assembly. Figure 3-24 shows the number of drops to failure for the MCS package. The number of drops to failure decrease with the increase in g-level from 30,000g to 50,000g. Figure 3-25 shows the number of drops to failure for the CCGA. The number of drops to failure decrease with the increase in g-level from 30,000g to 50,000g. A one-way ANOVA analysis has been performed to compare the reliability of the MCS package versus the CCGA package. Figure 3-26 shows the

ANOVA analysis performed for the 30,000g test level. The plot shows that the micro-coil spring interconnect outperform the column interconnect at this test level. Figure 3-27 shows a similar one-way ANOVA plot for the 40,000g test level. Similarly, the plot show that the MCS interconnect has greater reliability at this test level. Figure 3-28 shows the one-way ANOVA analysis performed for the 50,000g test level. The MCS interconnect outperforms the CCGA. The micro-coil spring outperforms the column interconnect at every g-loading between 30,000g and 50,000. The micro-coil interconnect has higher shock survivability at the highest g-level tested of 50,000g compared to the column interconnect at the lowest g-level tested of 30,000g.

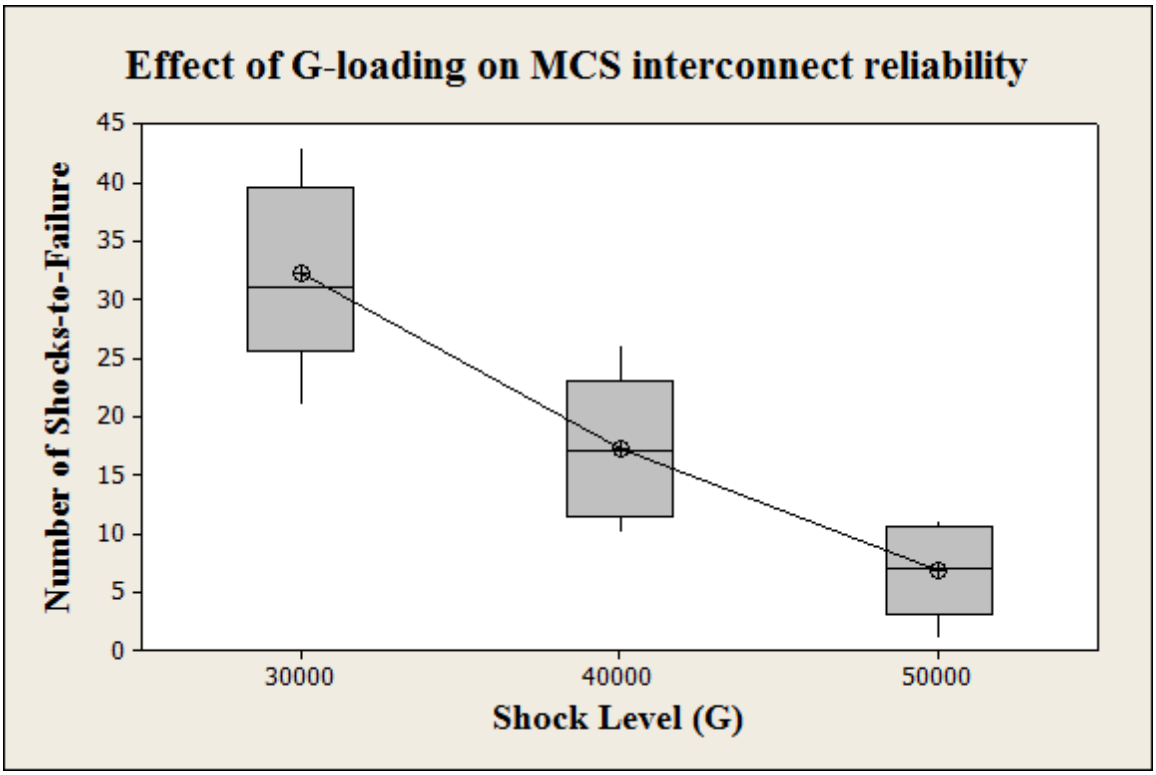


Figure 3-24: Effect of G-loading on MCS interconnect reliability

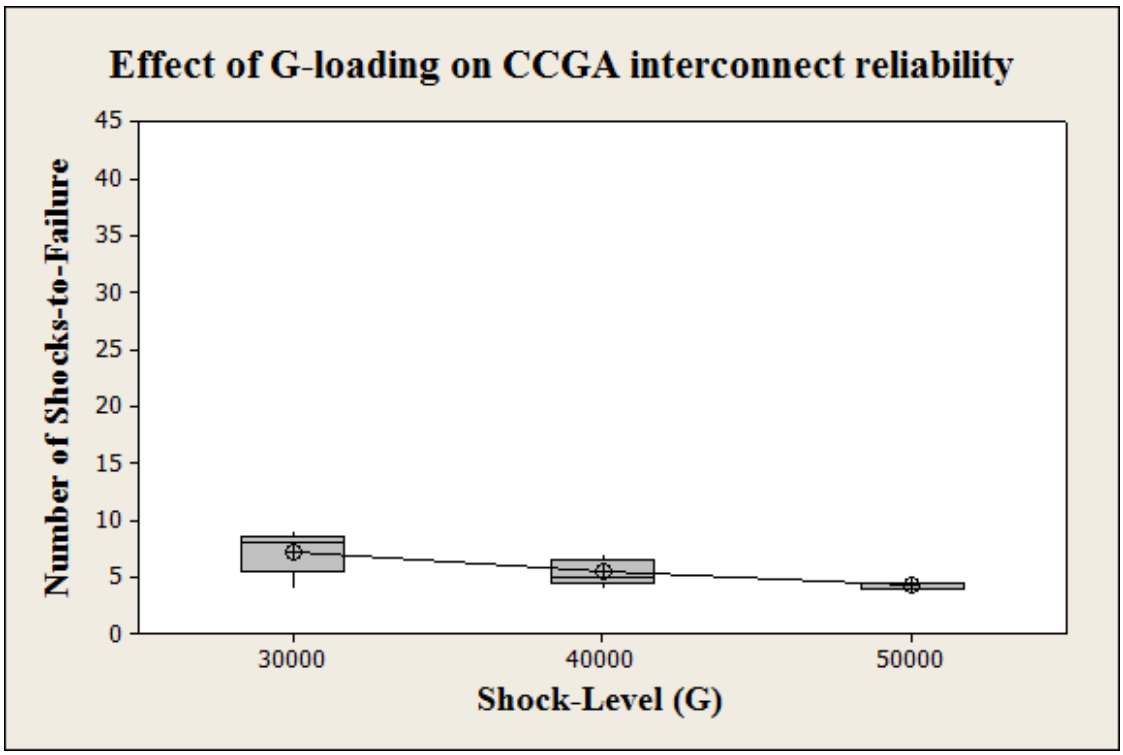


Figure 3-25: Effect of G-loading on CCGA interconnect reliability

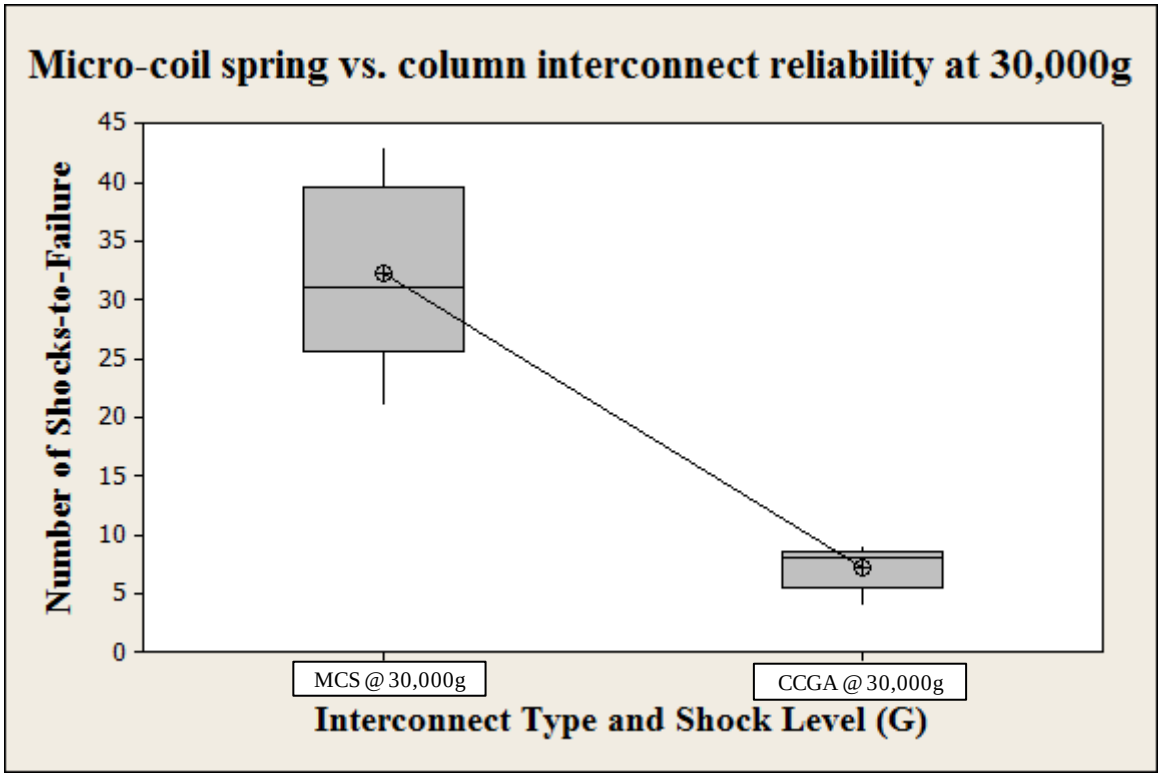


Figure 3-26: Micro-Spring Coil Vs Column Interconnect reliability at 30,000g

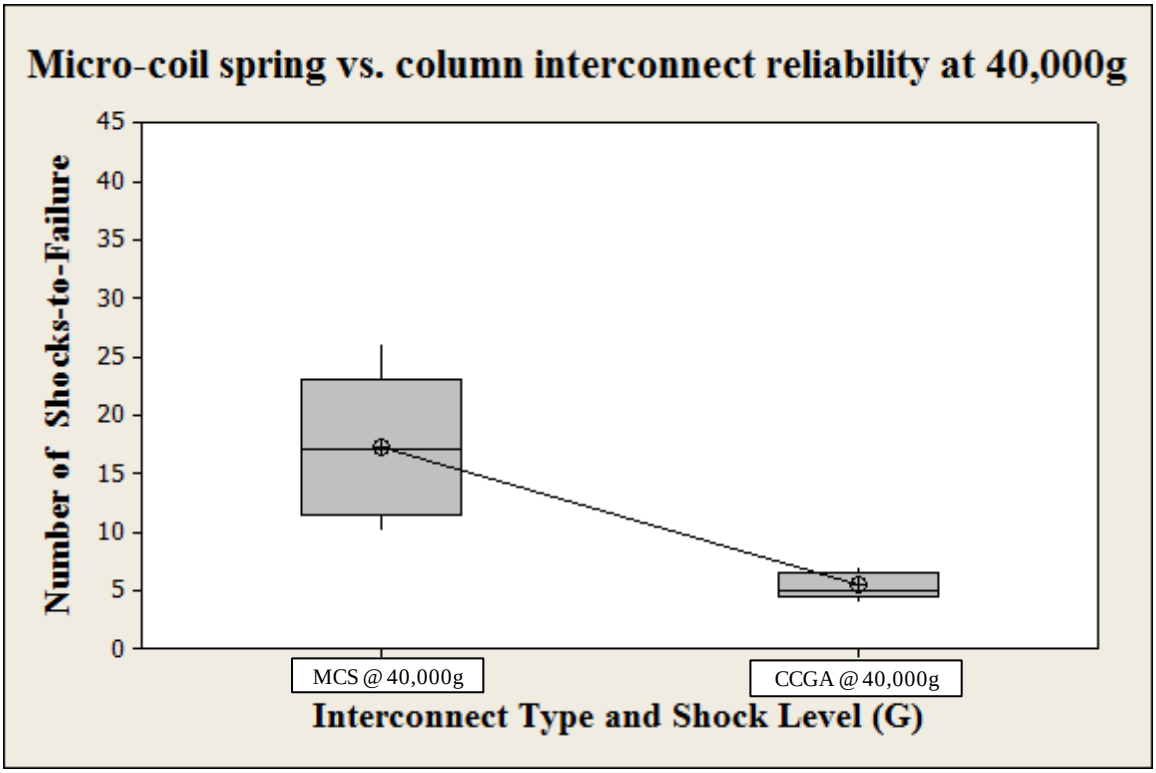


Figure 3-27: Micro-Spring Coil Vs Column Interconnect reliability at 40,000g

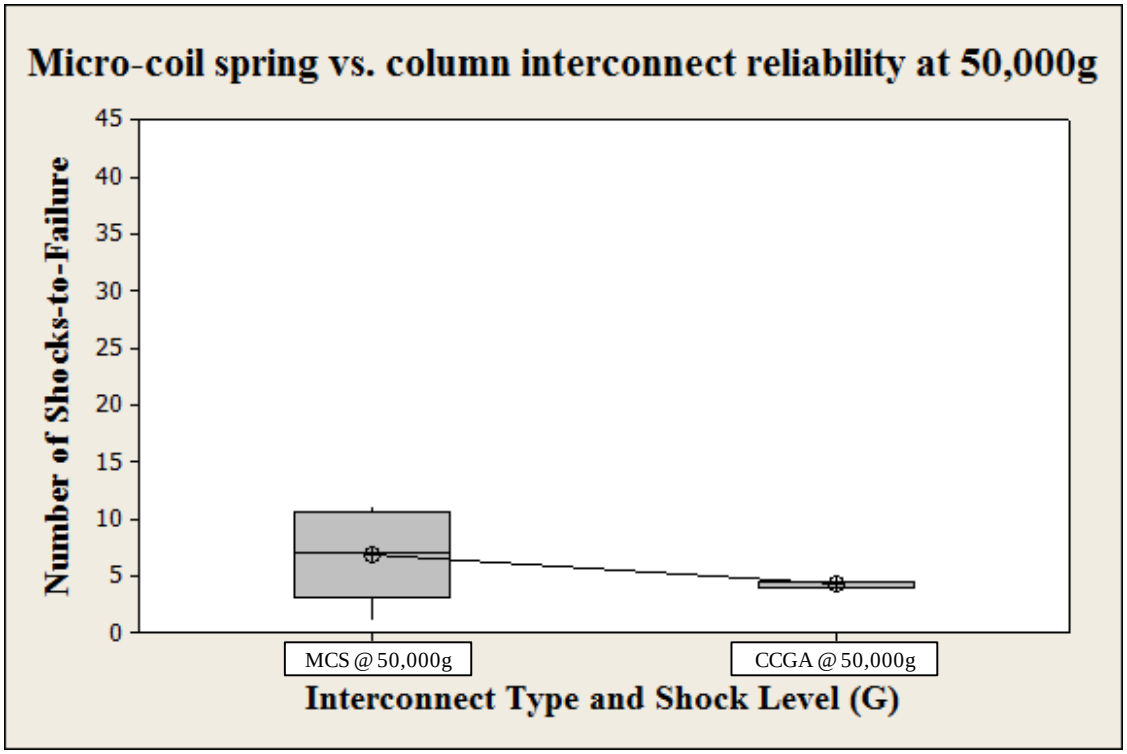
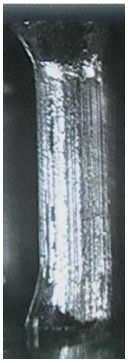


Figure 3-28: Micro-Spring Coil Vs Column Interconnect reliability at 50,000g

Vertical Orientation Reliability Results

Reliability of both the MCS and the CCGA board assemblies have been analyzed using daisy chained in conjunction with a high speed data acquisition system. Resistance of the packages has been monitored using a modified wheat stone bridge configuration. The failures have been defined using the IPC-SM785 standard. The failure data for both board assemblies have been reported in table format in Figure 3-29 and Figure 3-30. The failures have been reported for the low, mid, and high test levels. Each cell in the table represents a tested sample. Five samples have been tested for each test level with a total of fifteen samples tested for the MCS board assembly. Only two board assemblies are tested for the CCGA board assembly. Much better reliability is observed for the CCGA board assembly. Testing is conducted up to 120 drops for two test samples. Failure does not occur for the CCGA. The MCS board assemblies are more susceptible to failure in the vertical orientation. The full test matrix is examined for the MCS board assembly.

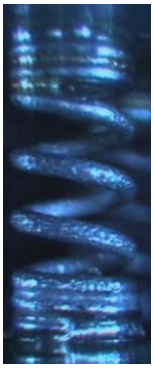


CCGA

G-level	Drops to Failure
3,000g	DNF @ 120 drops for two boards

*Failure is defined as an open circuit using IPC-SM785 standard

Figure 3-29: CCGA vertical orientation failure results



MCS

G-level	Drops to Failure				
2,000g	7	7	4	2	4
2,250g	4	3	3	2	1
2,500g	1	1	1	1	1

*Failure is defined as an open circuit using IPC-SM785 standard

Figure 3-30: MCS vertical orientation failure results

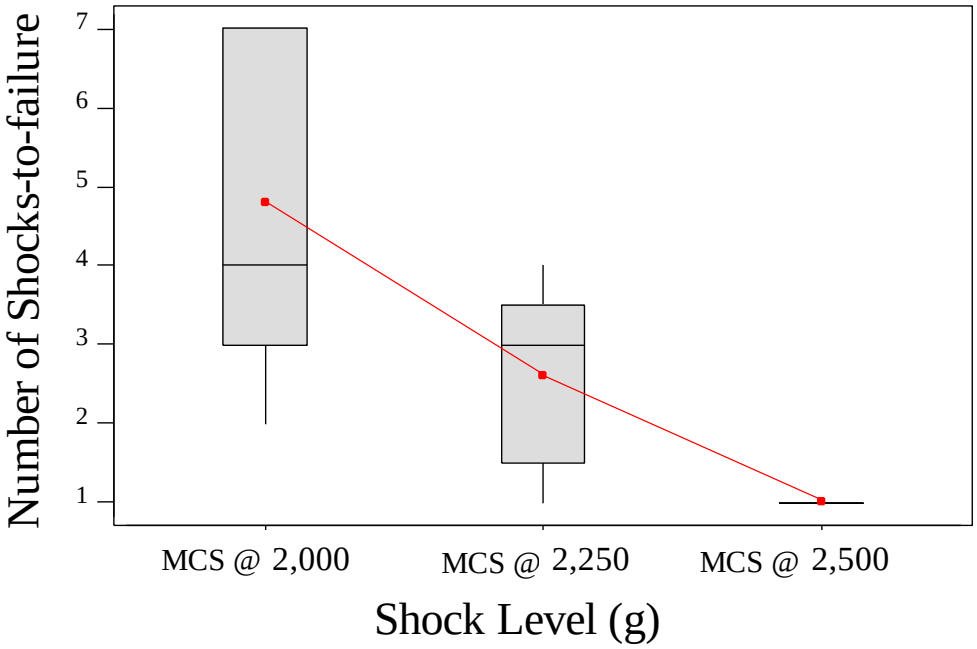


Figure 3-31: Effect of G-level on MCS interconnect reliability

3.6 Failure Analysis

Horizontal Orientation Failure Modes

Failed MCS packages have been analyzed using a high powered optical microscope. The predominant failure mode occurs due to shear shearing of the beryllium copper coil (Figure 3-32 and Figure 3-33). Failure analyses of the column interconnect shows that necking has occurred resulting in a brittle failure. The failures occur in the column near the PCB interface as shown in Figure 3-34 to Figure 3-36.

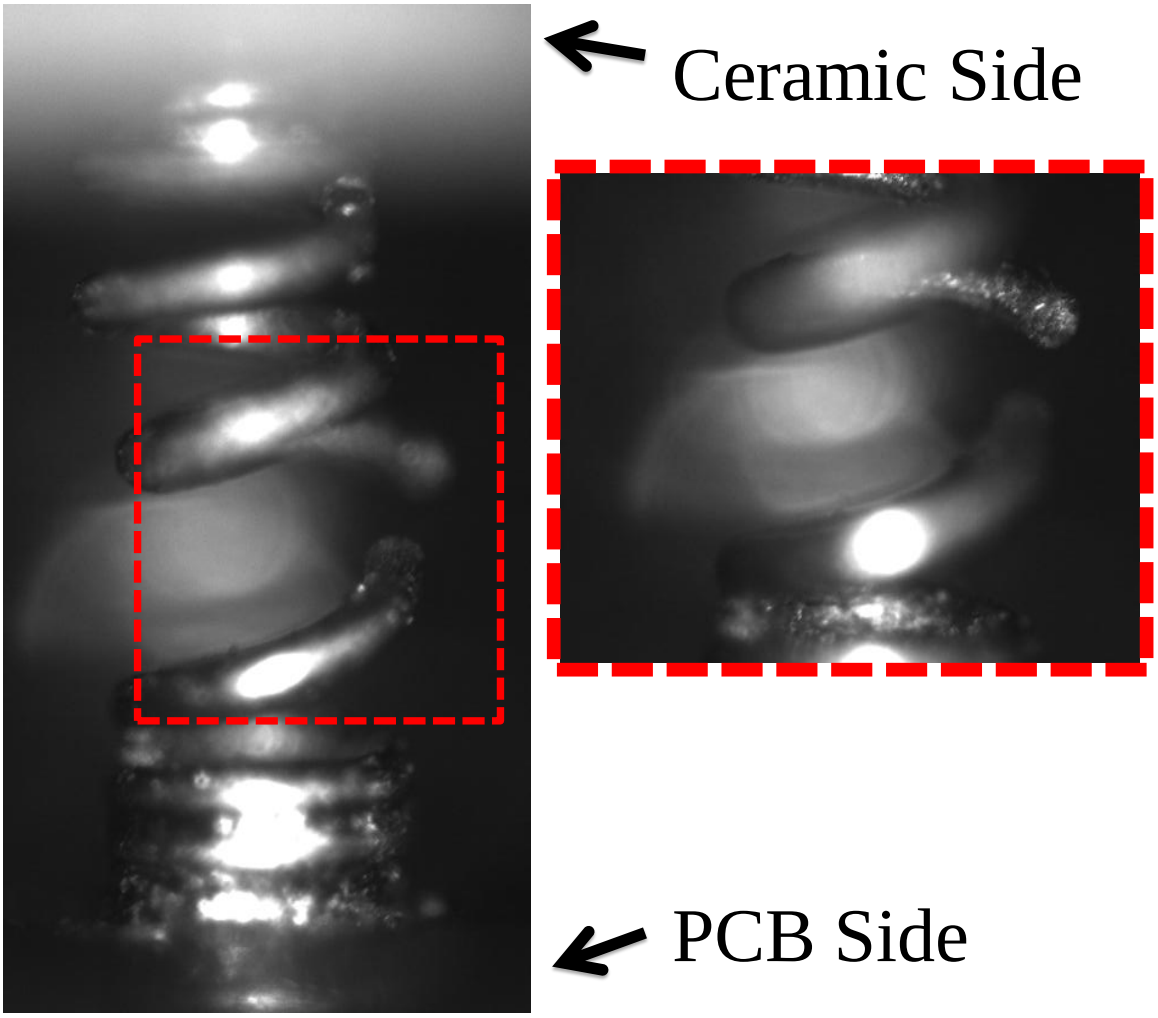


Figure 3-32: MCS Failure Mode-1

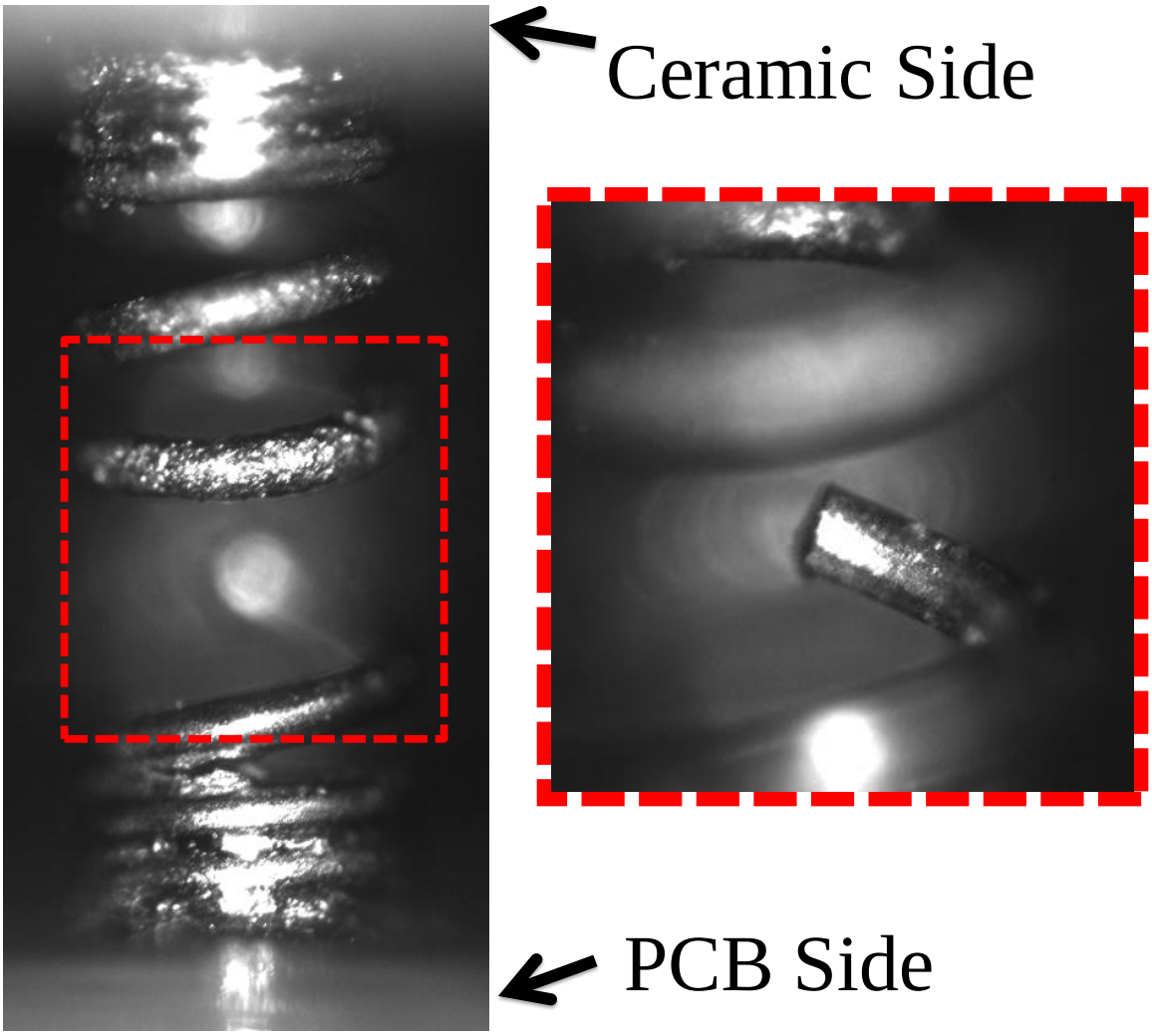


Figure 3-33: MCS Failure Mode-2

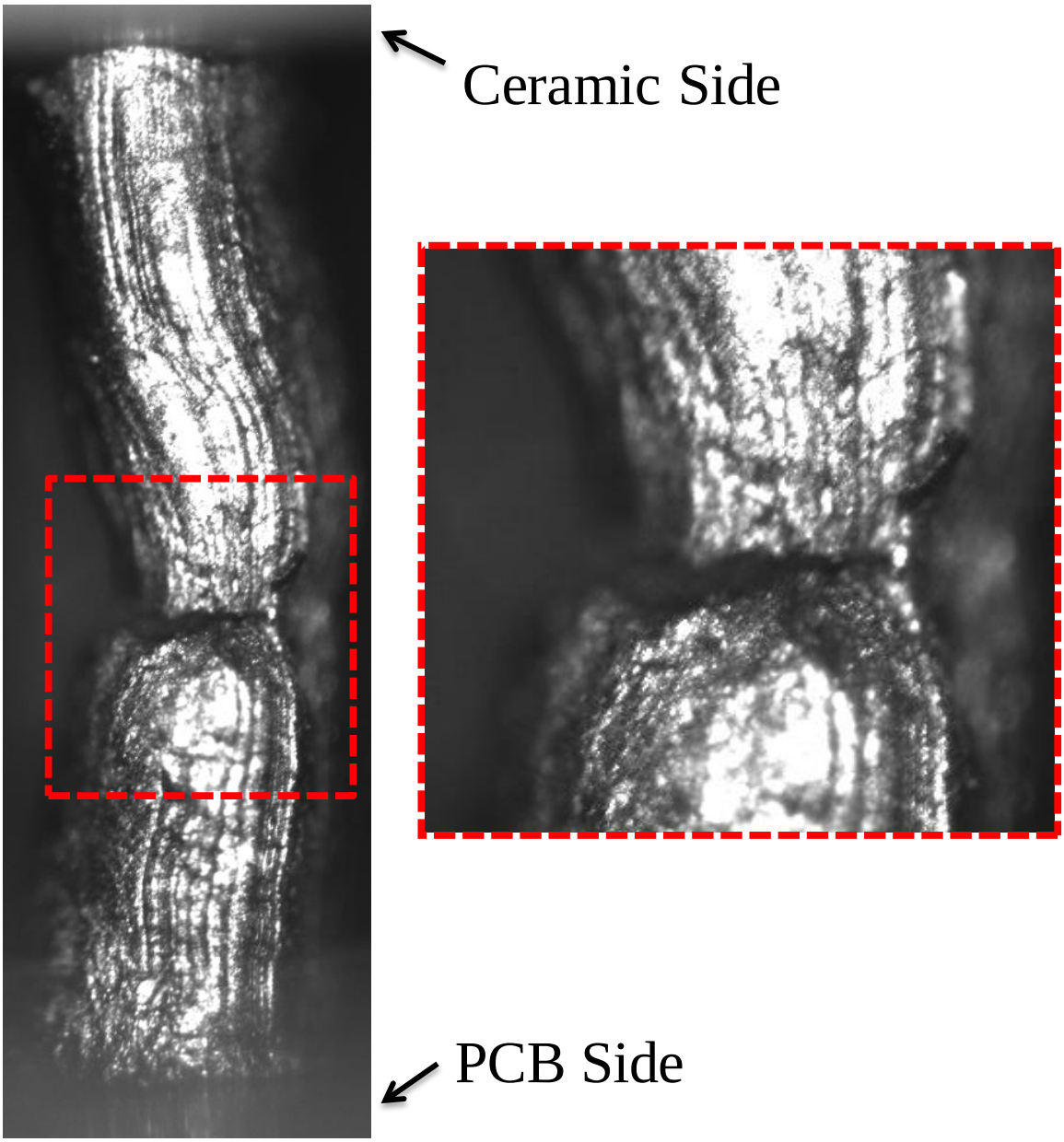


Figure 3-34: CCGA Failure Mode-2

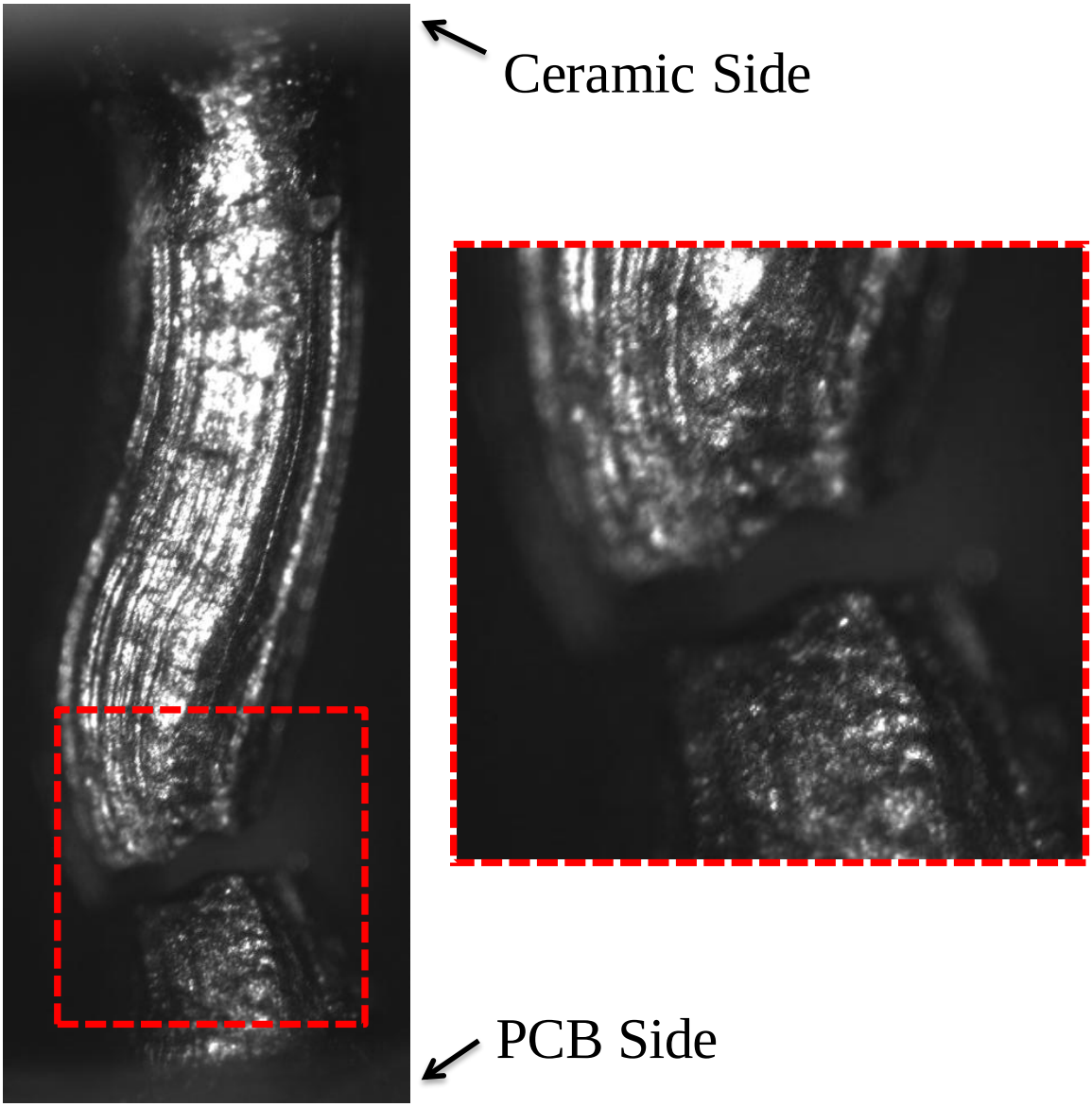


Figure 3-35: CCGA Failure Mode-1

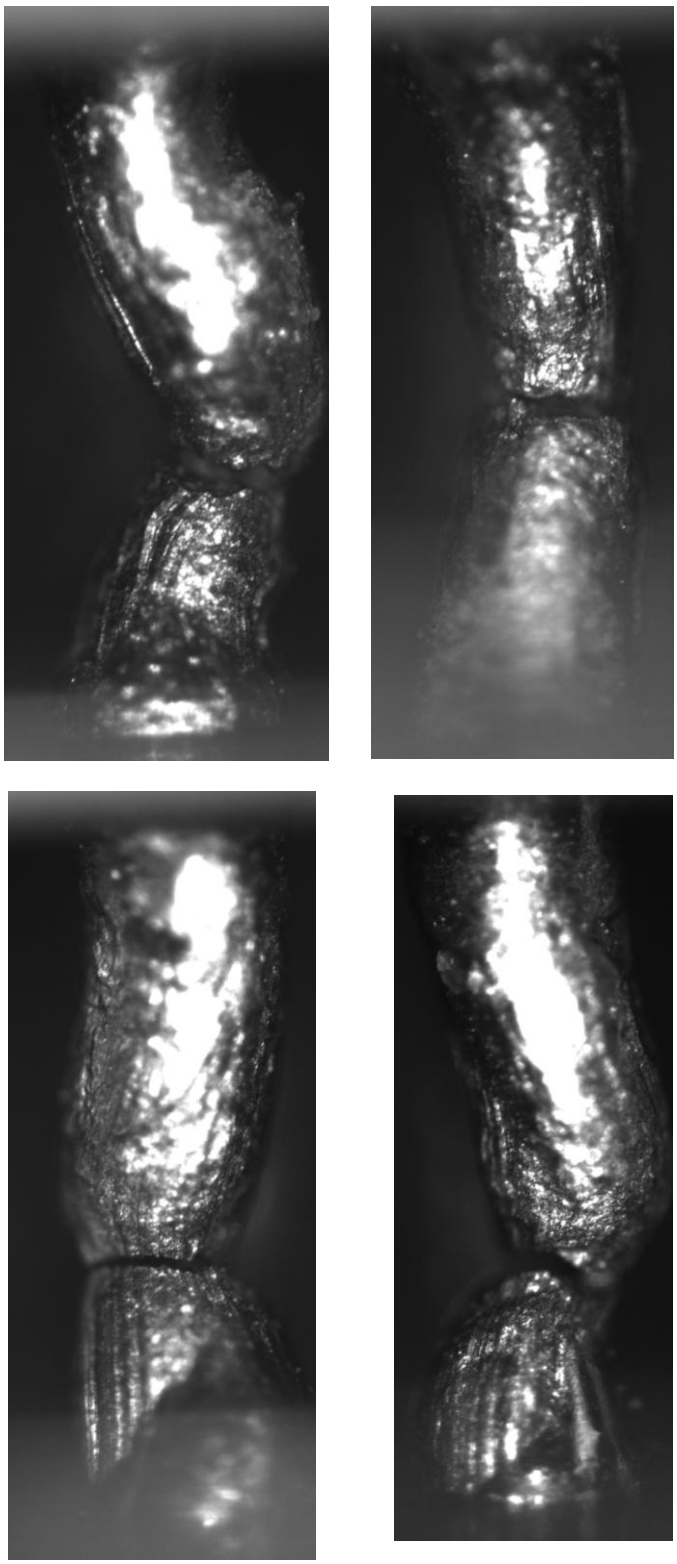


Figure 3-36: Column Failures

Vertical Orientation Failure Modes

Failed MCS packages have been analyzed using a high powered optical microscope. The dominant failure mode occurs near the solder attachment point. The failure occurs at the ends of the spring near the solder. Figure 3-37 and Figure 3-38 are images showing the predominant failure modes. A zoomed in view of the failure is also shown in the figures. Failure occurs directly through the spring. Failures occur on either the PCB side or the ceramic side but all observed failures occur near the solder attachment point and through the beryllium spring itself instead of through the solder interconnect.

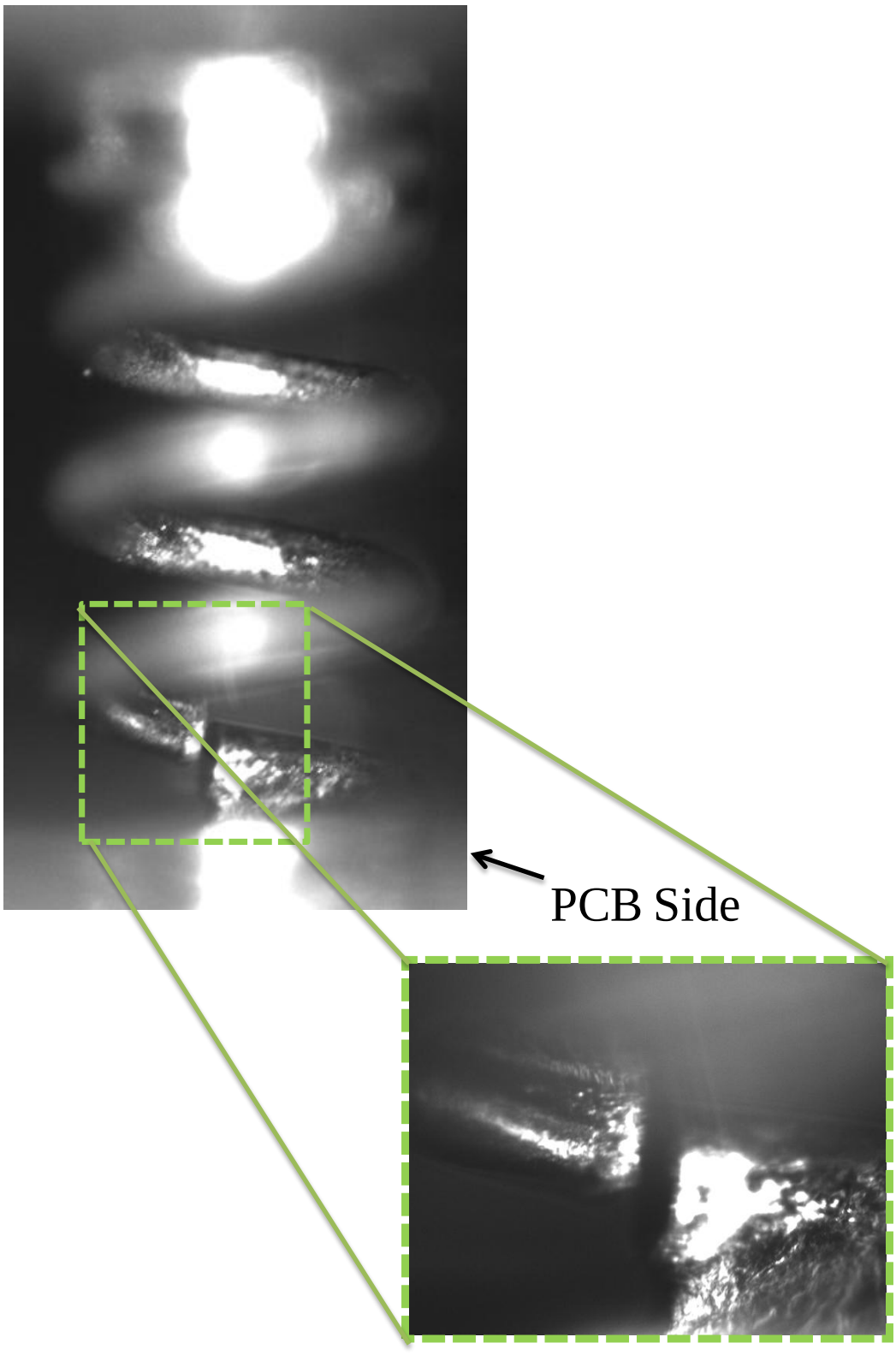


Figure 3-37: MCS Failure Mode-1 for vertical orientation

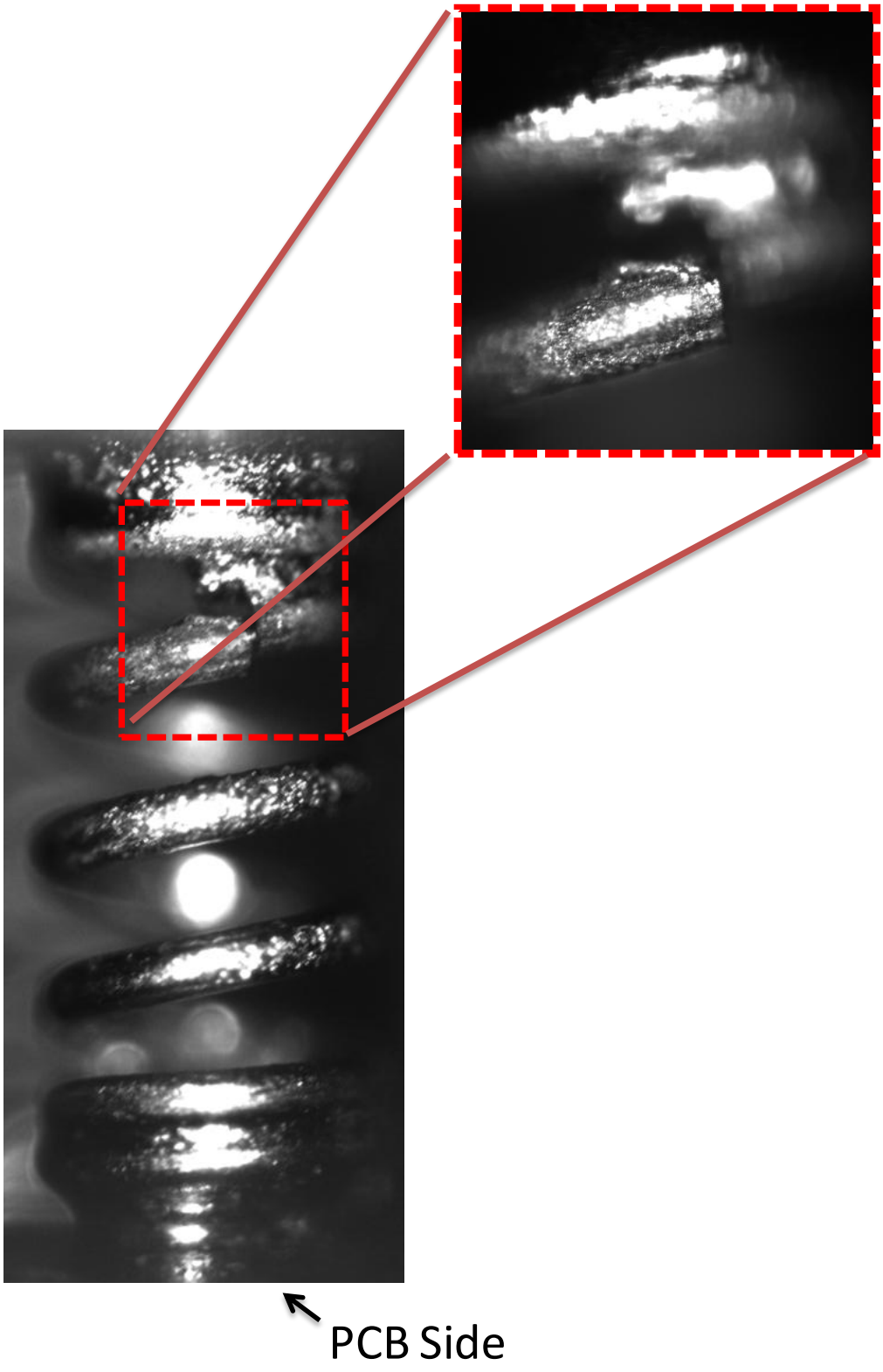


Figure 3-38: MCS Failure Mode-2 for vertical orientation

3.7 Finite Element Analysis Approach

Explicit finite element models have been developed to simulate to drop impact of the board. Response of the printed circuit board has been simulated and correlated with results obtained from experimental data. Figure 3-39 shows a schematic of the typical approach of using a global-local submodeling. Global-local submodeling requires two models. The global model is meshed coarsely using a smeared property approach [Lall 2004, 2005]. Local models are meshed finely with greater detail. Displacement boundary conditions extracted from the global model are used as inputs to analyze the local model. The global model is validated and correlated with experimental strain values. It is meshed using a reduced integration solid element type, C3D8R. The global model used for the analysis is shown in Figure 3-40. The global model is analyzed using approximated elements for the base plate and the standoff screws. The impact region is modeled as a rigid surface to reflect the rigidity of the actual impact surface. A R3D4 rigid element is used. The rigid element is bounded in all directions and is strictly there to serve as a contact region between the two surfaces. The finite element analysis set up is shown in Figure 3-41.

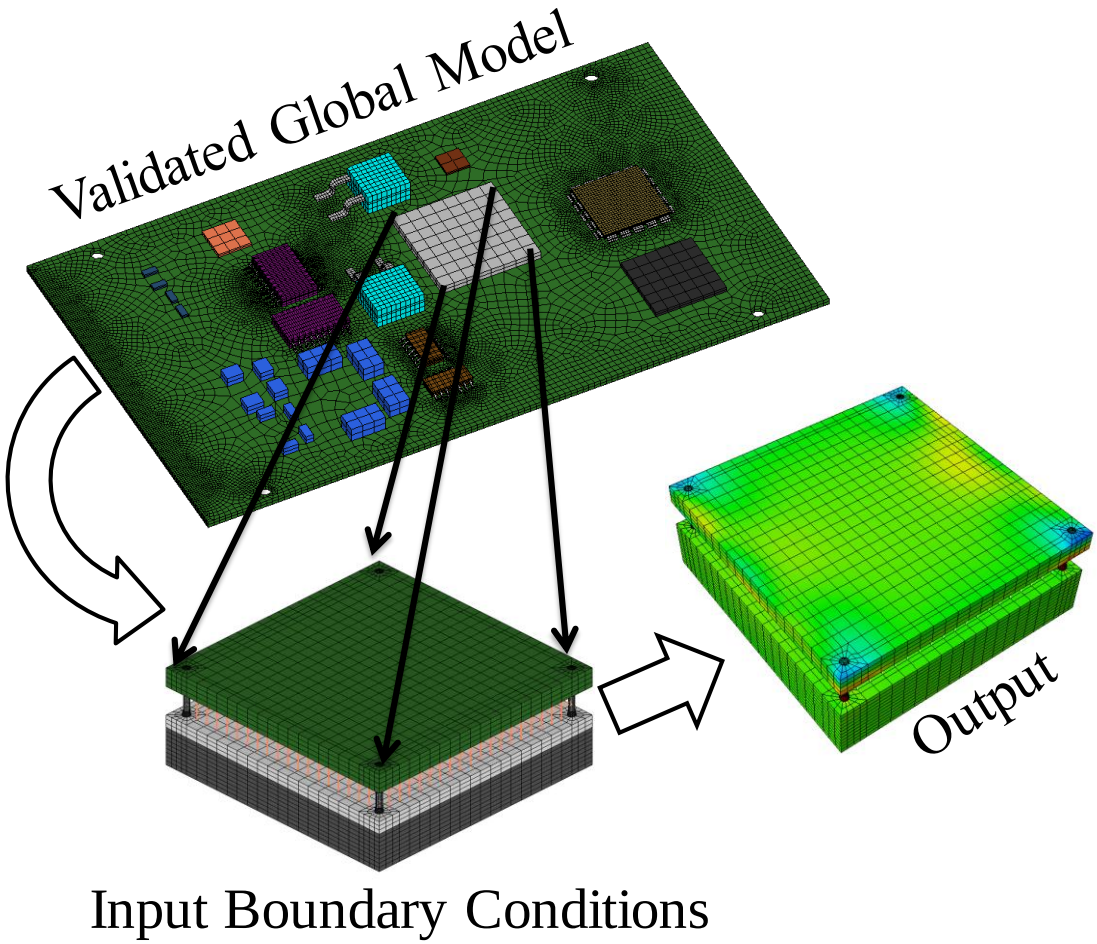


Figure 3-39: Global-Local submodeling

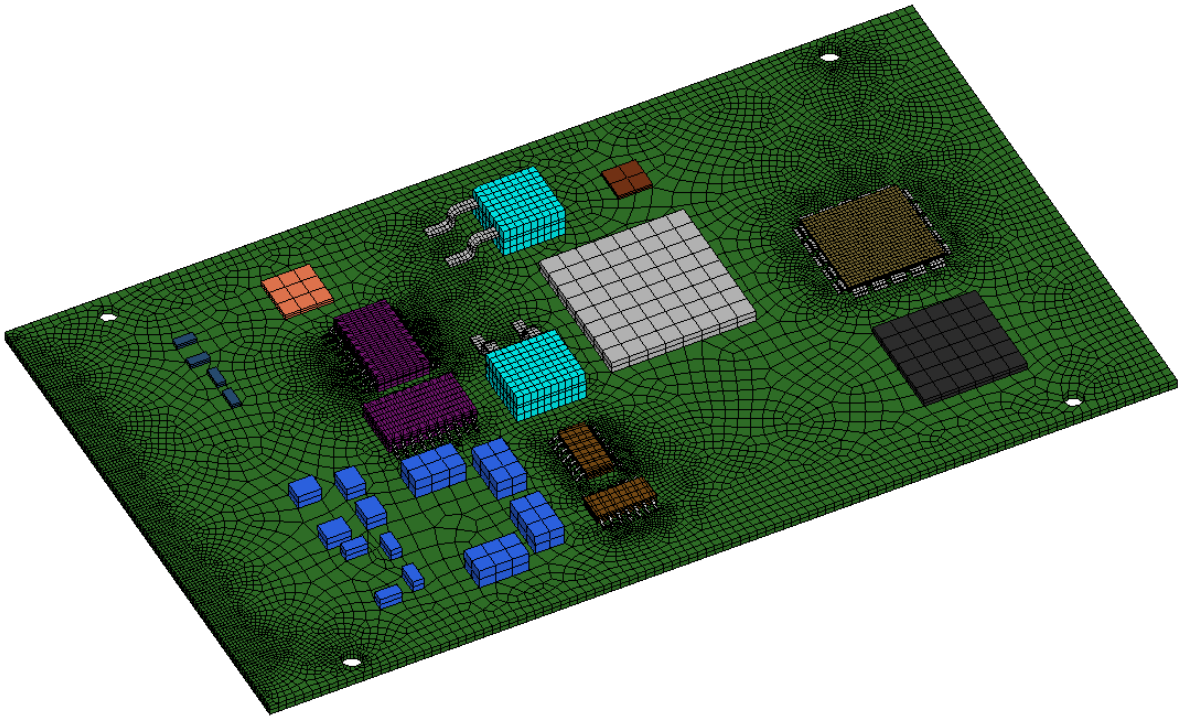


Figure 3-40: Global model

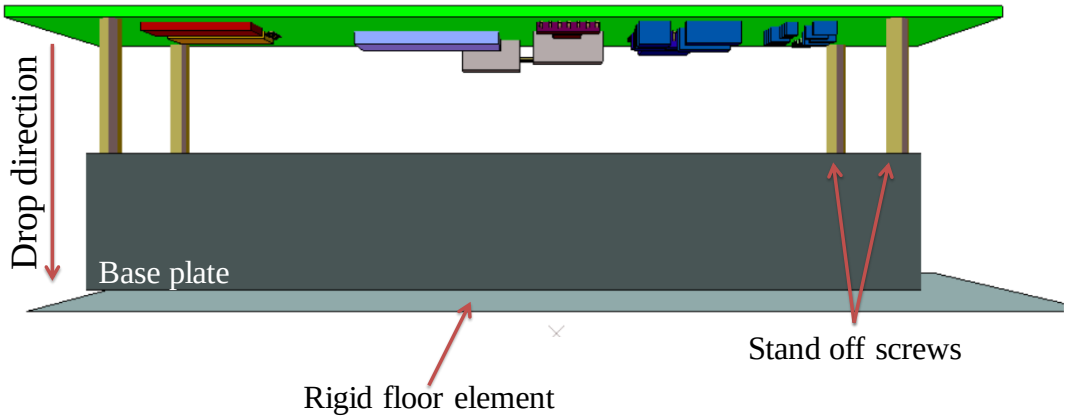


Figure 3-41: Global model FEA set up

The submodel for the MCS board assembly has been created using C3D8R solid elements and SPRINGA spring elements. The MCS array is modeled fully including the ceramic substrate and aluminum mass. To reduce computational time and focus on

interconnects susceptible to failure, only the corner interconnects have been modeled in detail. The springs are de-featured and modeled using square cross sections instead of circular cross sections. This has been done to save computational time and allow for the aligning of different mesh densities in the finite element model. The rest of the area array interconnects have been approximated using spring elements. In the past, Timoshenko beams have been used in conjunction with conventional shell elements and continuum shell elements [Lall 2006[a,b], 2007[a-e], 2008[a-d]]. A similar approach is taken in this study using spring elements. The MCS array finite element submodel is shown in Figure 3-42. The detailed finite element model of the MCS interconnect is shown in Figure 3-43.

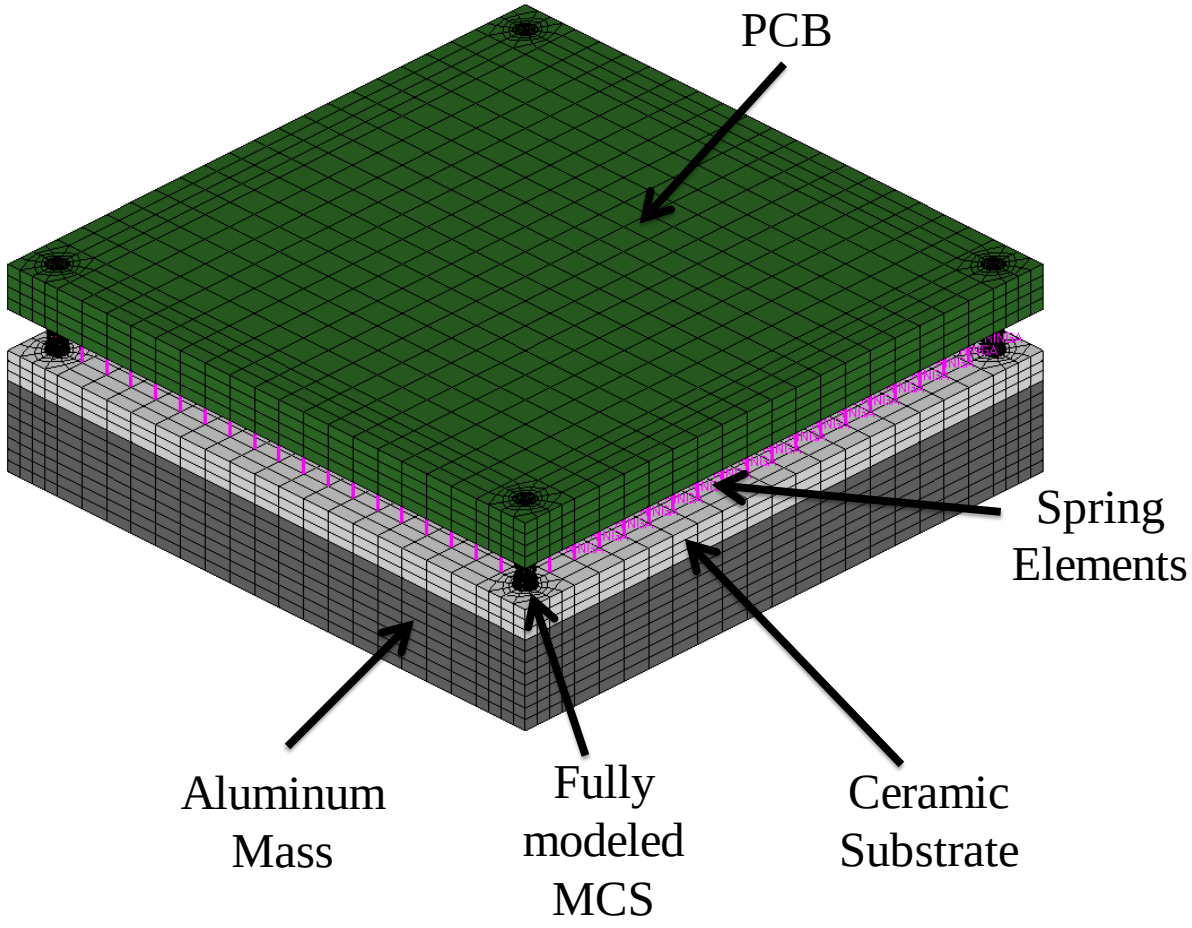


Figure 3-42: MCS Array Submodel

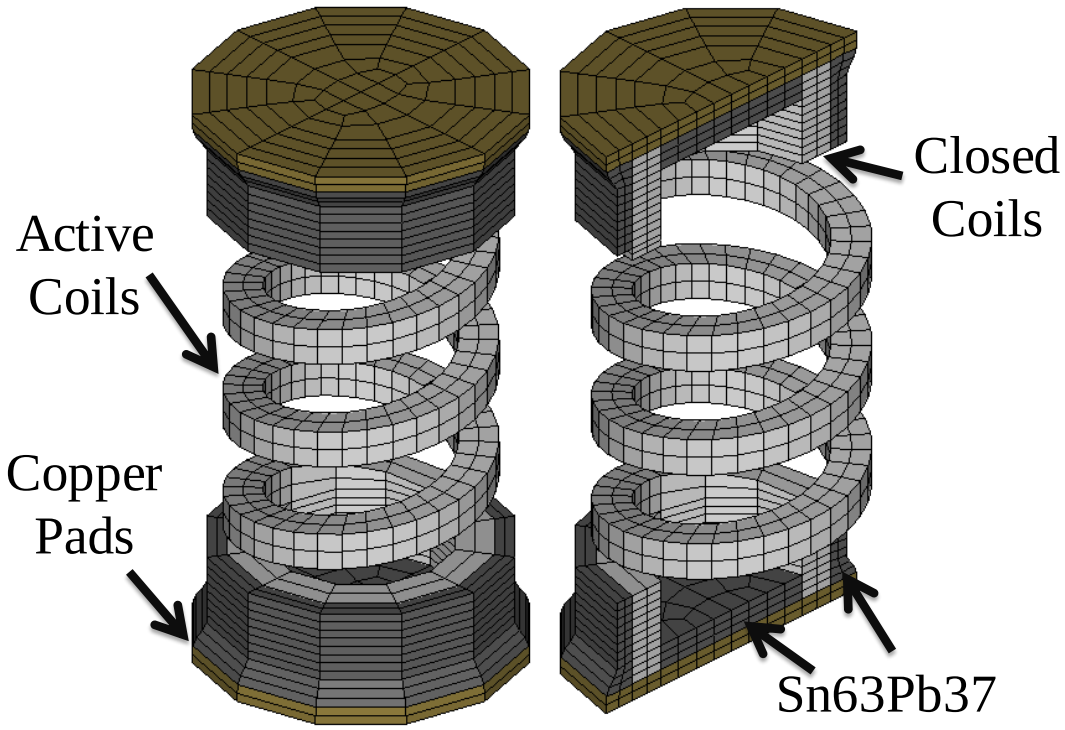


Figure 3-43: Detail MCS interconnect FEA model

The axial spring element, SPRINGA, requires two geometrical nodes. SPRINGA elements are unidirectional and will only have a line of action according to the two specified nodes. The only input required is the spring constant. The spring constant for the MCS interconnect is approximated using Equation 3.1 where D is defined by the Equation 3.2

$$k = \frac{Gd^4}{8D^3\eta} \tag{3.1}$$

$$D = D_{outer} - d \tag{3.2}$$

G is the shear modulus, d is the wire diameter, D is the mean diameter, D_{outer} is the spring diameter, and η is the number of active coils. The shear modulus is approximated using the material properties of beryllium copper. A single element cross section of a SPRINGA element is shown in Figure 3-44.

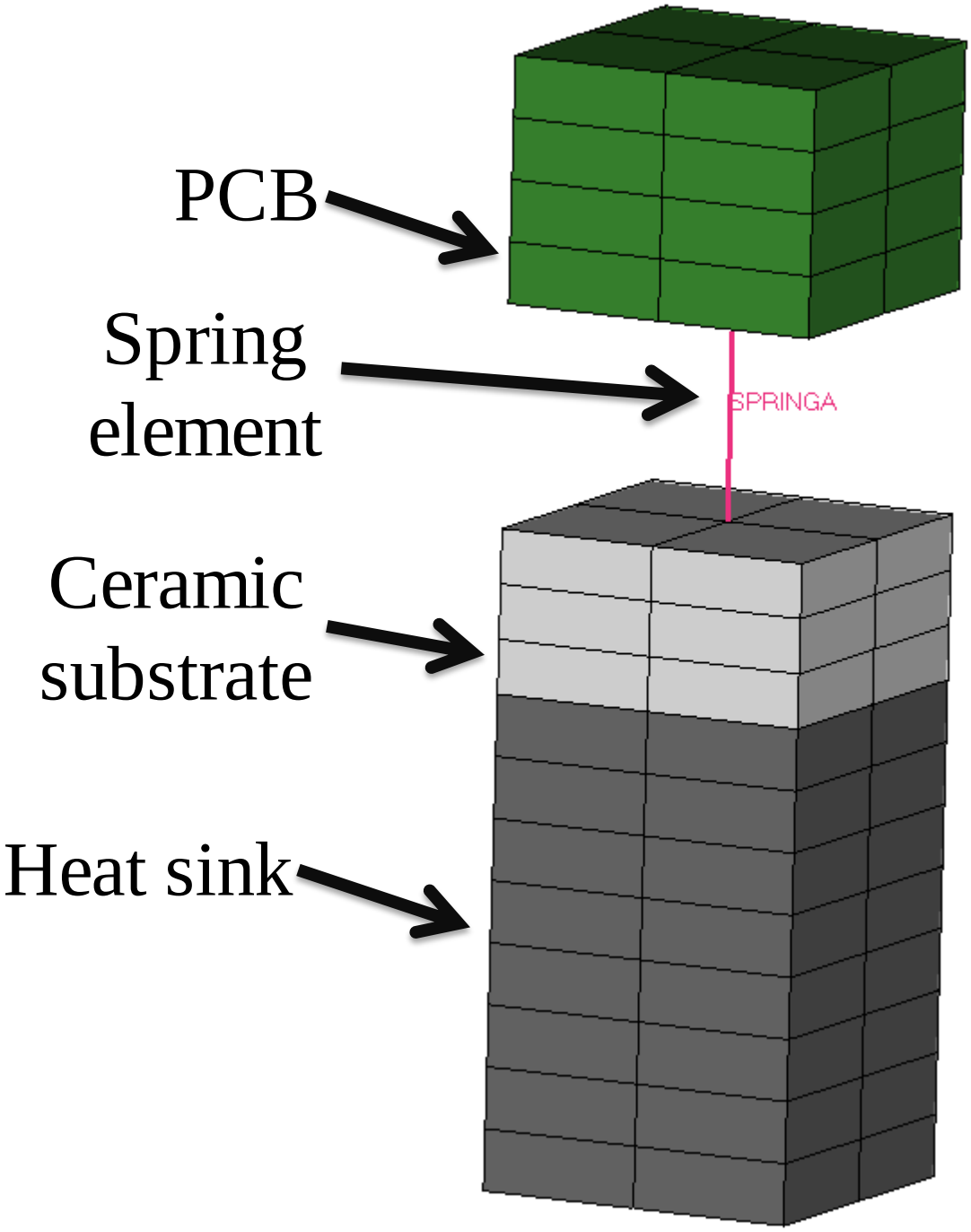


Figure 3-44: SPRINGA element

The submodel for the CCGA board assembly has been created using C3D8R solid elements and B31, Timoshenko beam elements. The column array is modeled fully including the ceramic substrate and aluminum mass. To reduce computational time and

focus on interconnects susceptible to failure, only the corner interconnects have been modeled in detail. In the past, Timoshenko beams have been used in conjunction with conventional shell elements and continuum shell elements [Lall 2006[a,b], 2007[a-e], 2008[a-d]]. The same approach has been used in this study. The CCGA array finite element submodel is shown in Figure 3-45. The detailed finite element model of the MCS interconnect is shown in Figure 3-46.

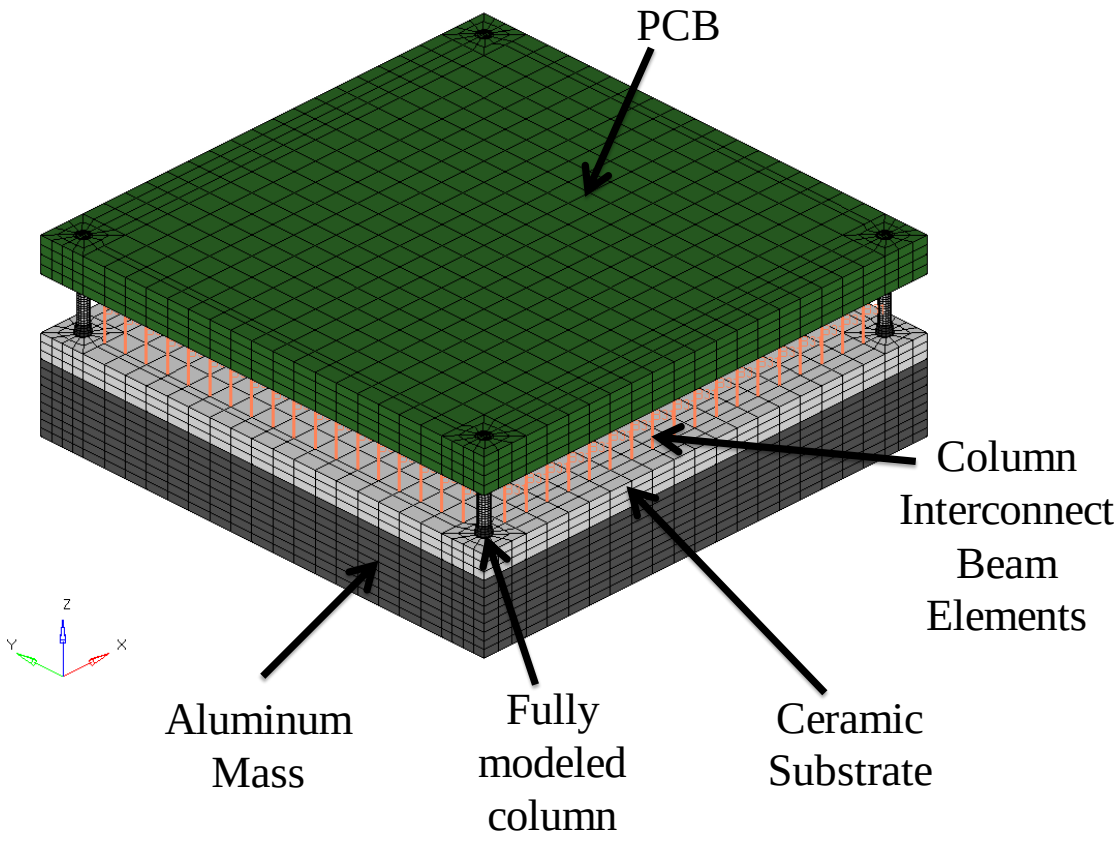


Figure 3-45: CCGA Array Submodel

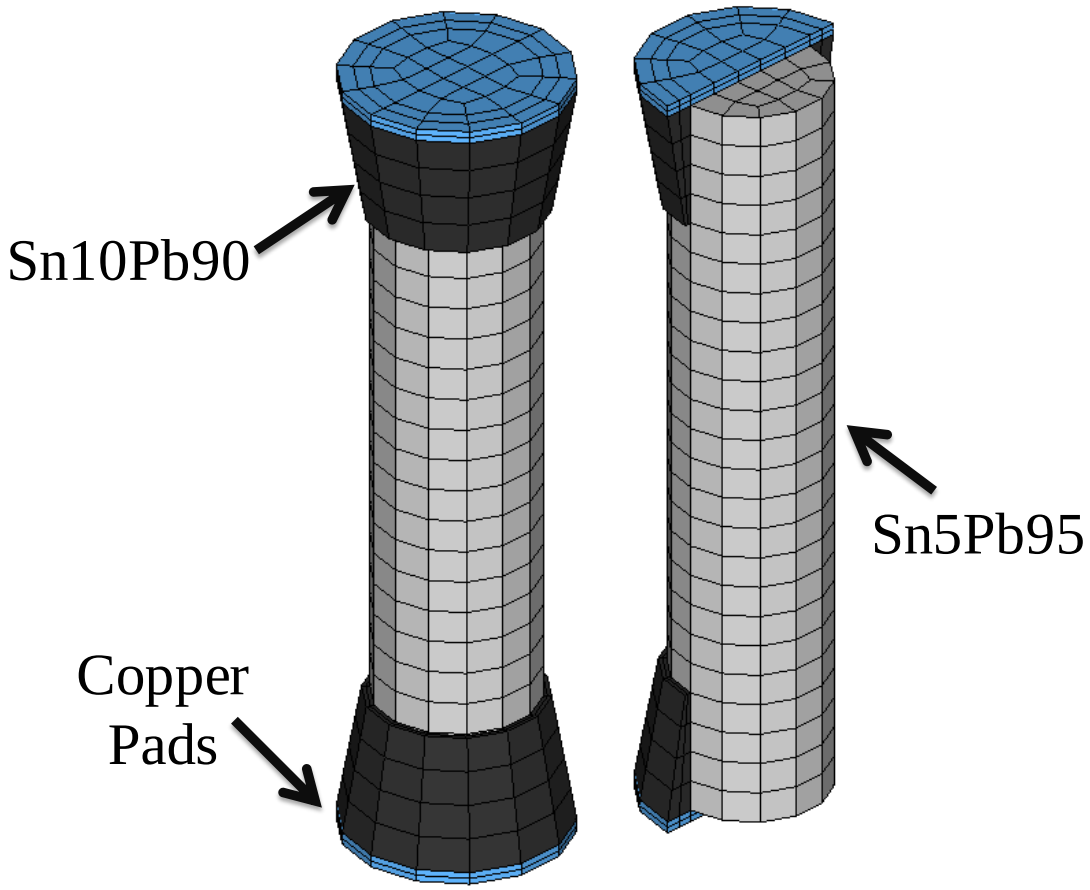


Figure 3-46: Detail CCGA interconnect

The Timoshenko beam element, B31, requires two geometrical nodes. It is a linear beam with all motional degrees of freedoms active. The beam cross section has been defined using a circular cross section with an identical radius to the detailed CCGA interconnect model. The material properties have also been kept the same between the detailed CCGA model and the beam element model. A schematic showing a single beam cross section is shown in Figure 3-47.

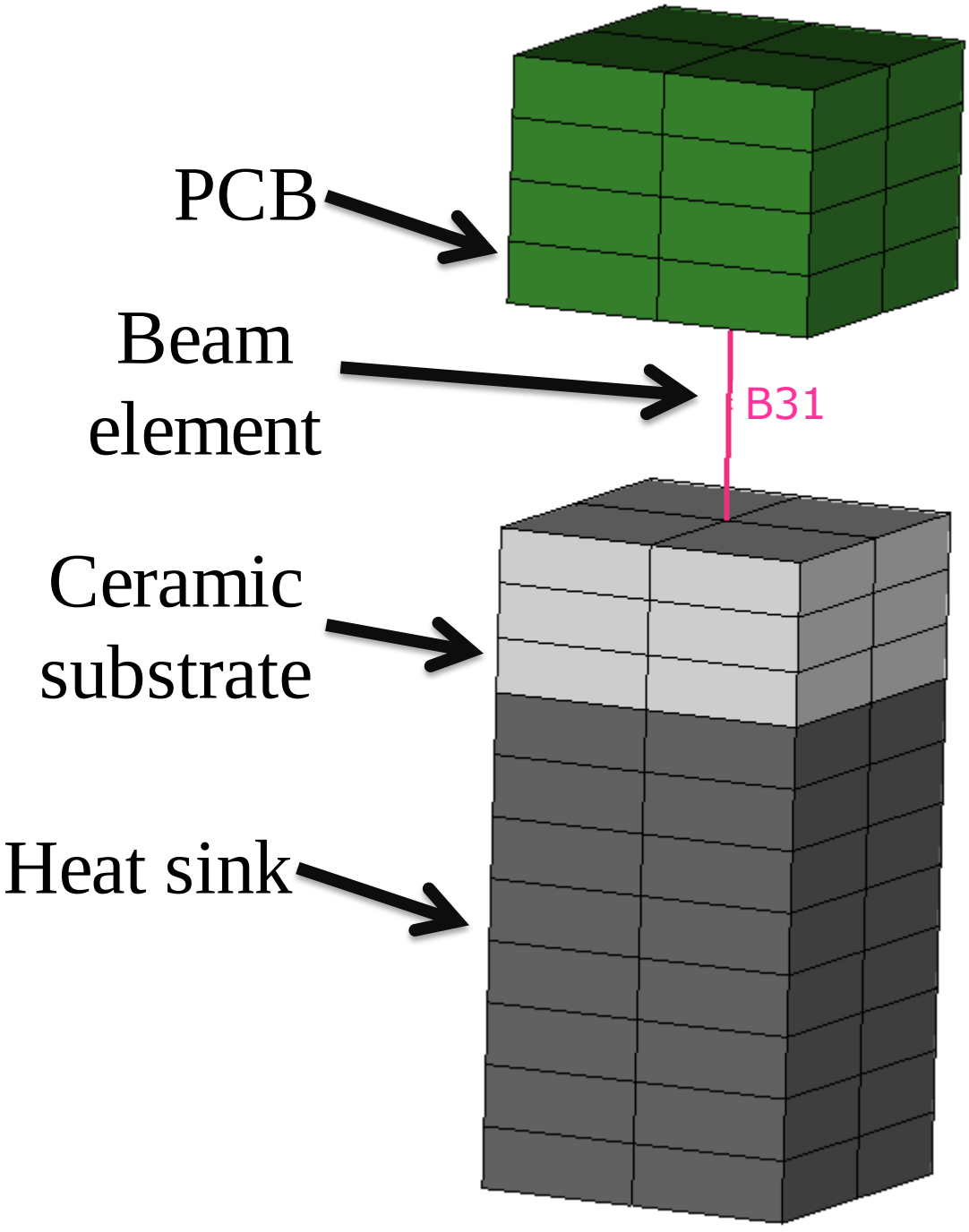


Figure 3-47: B31 element

3.8 Finite Element Analysis Results

Global Model FEA Results

The global finite element model is analyzed using an Abaqus solver. The model is analyzed as an explicit and dynamic problem. Strains extracted from the finite element analysis are correlated with experimental strain values. The global model shows good correlation. A time history of the finite element analysis is shown in Figure 3-48. The key frames of the analysis show the initial downward deflection and the rebounding upward deflection that occurs.

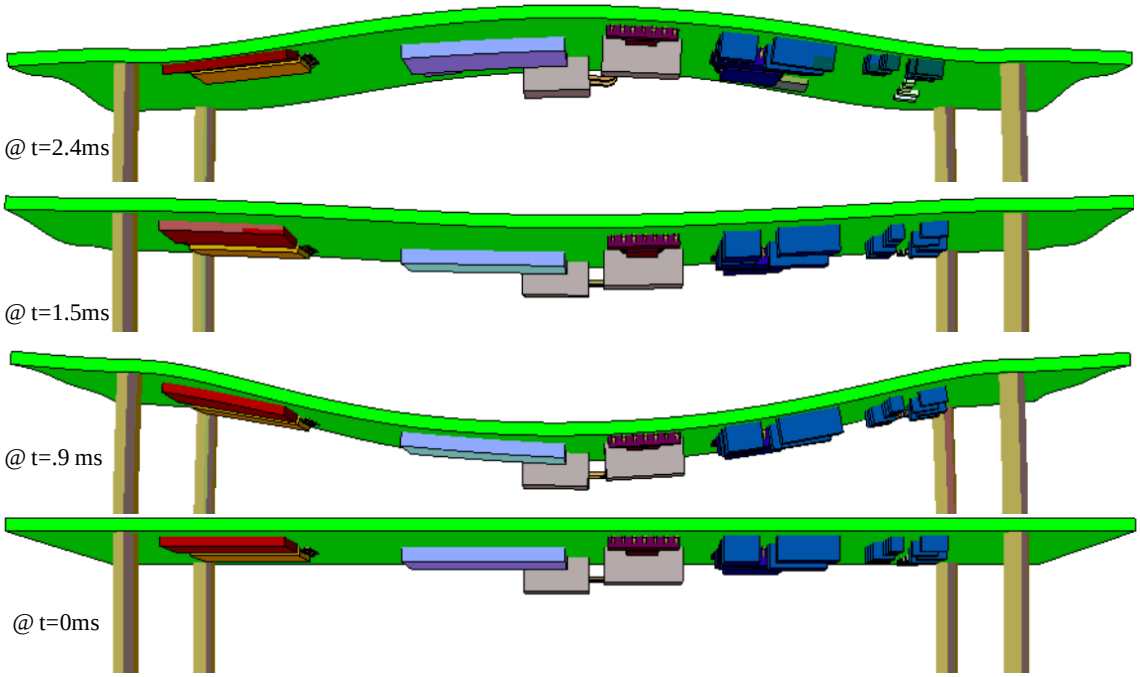


Figure 3-48: Global model FEA time history

Global finite element models are correlated using experimental results obtained from DIC. The out of plane deflection contour is correlated for each of the three test levels. Figure 3-49 through Figure 3-51 show a comparison between FEM and DIC for out of plane deflection. The results show that the FEA deflection contours correlate well with the experimental DIC contours. Strain values have also been correlated. Strain is measured on the bottom side at the center of the test board along the length of the board. The results show a very good correlation between experimental strain data and simulation strain data. Plots showing the correlation results for each of the test levels are shown in Figure 3-52 through Figure 3-54.

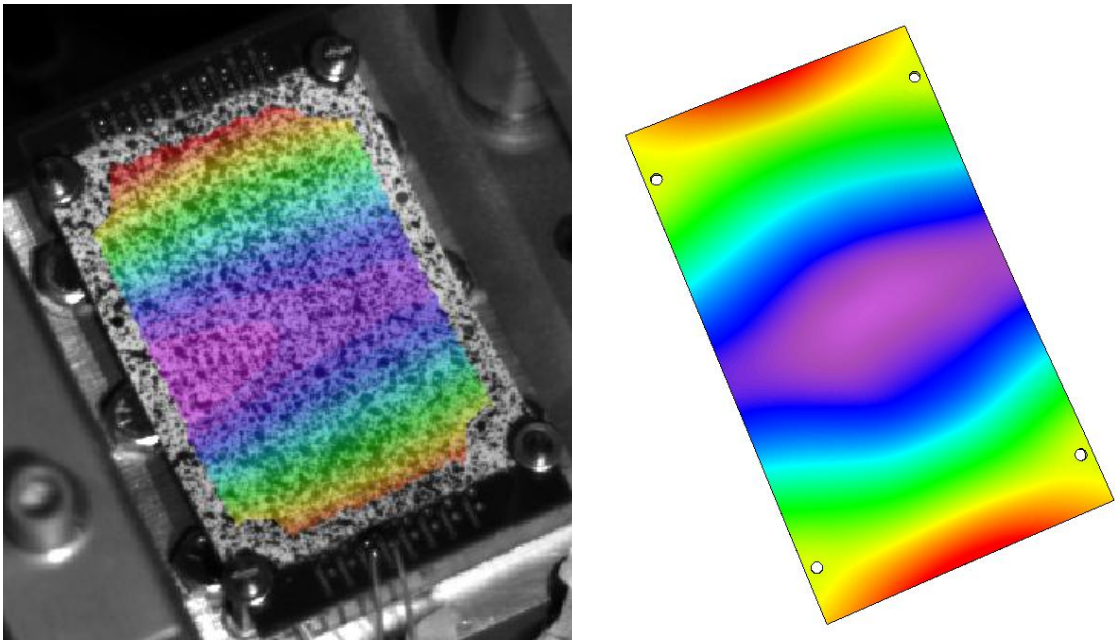


Figure 3-49: Displacement for 30,000g: DIC vs. FEA

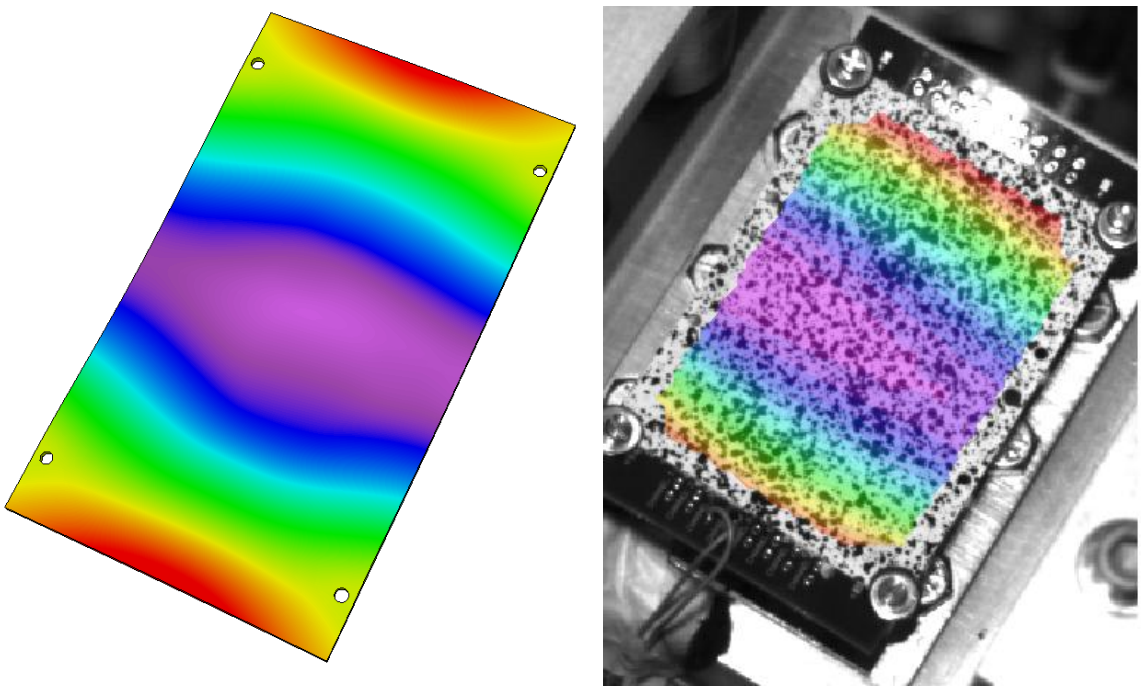


Figure 3-50: Displacement for 40,000g: DIC vs. FEA

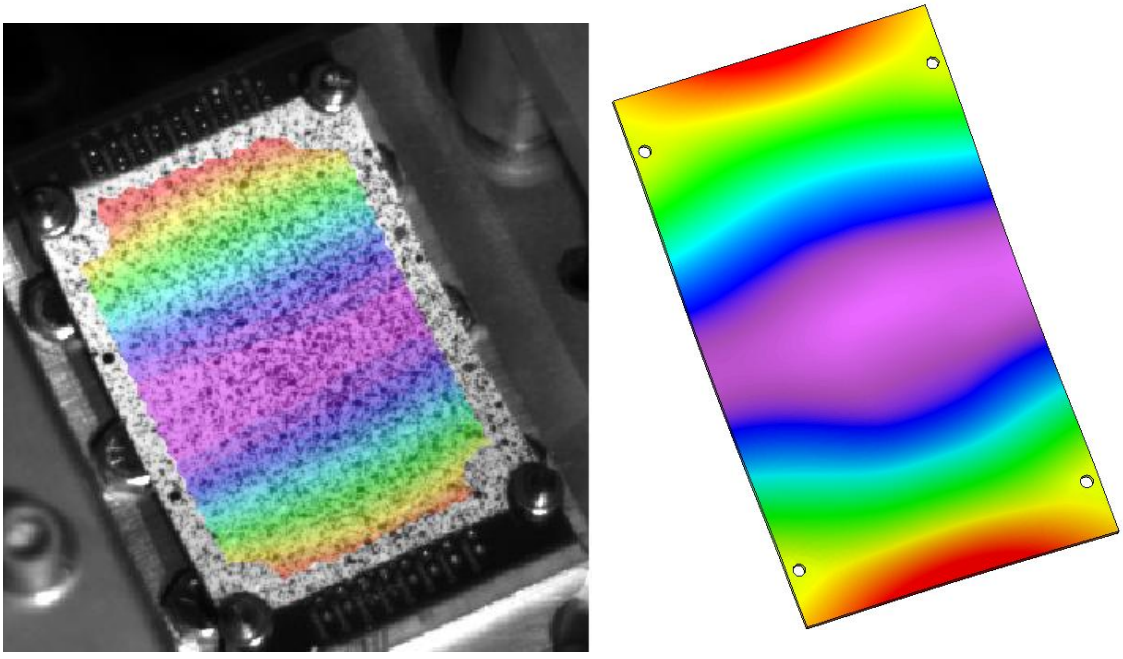


Figure 3-51: Displacement for 50,000g: DIC vs. FEA

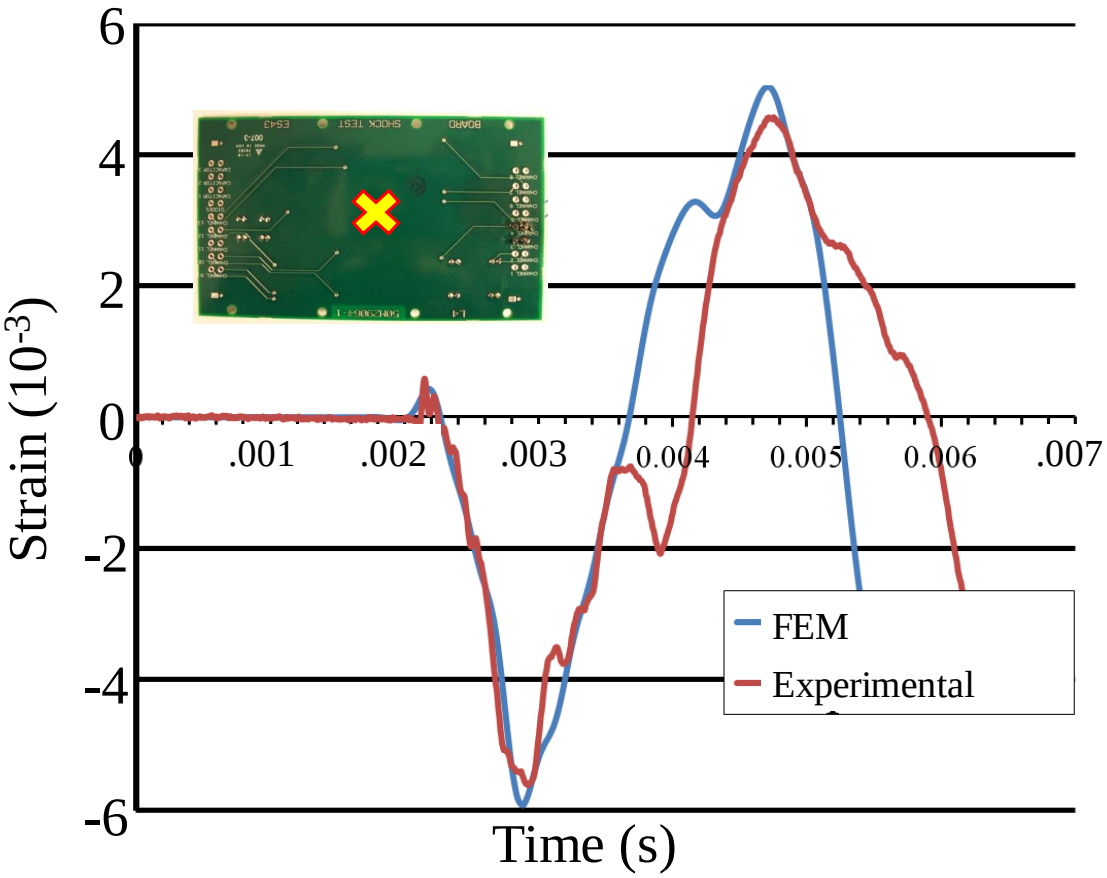


Figure 3-52: FEA vs. Experimnetal Strain - 30,000g

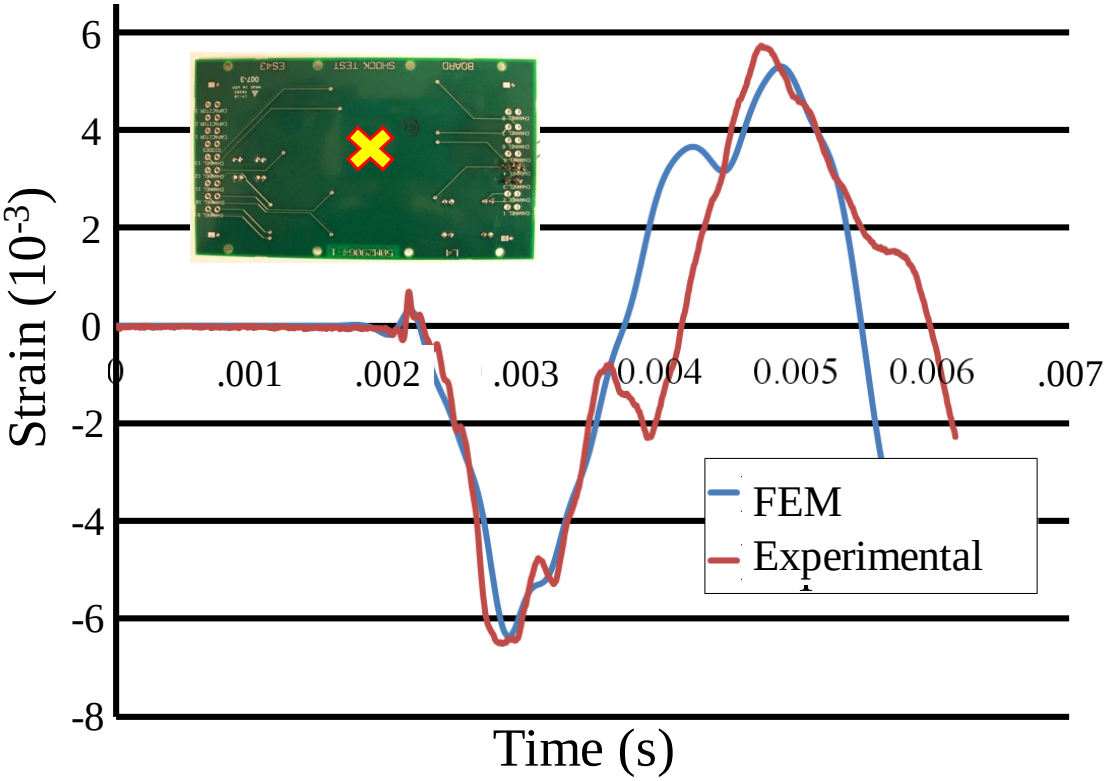


Figure 3-53: FEA vs. Experimental Strain - 40,000g

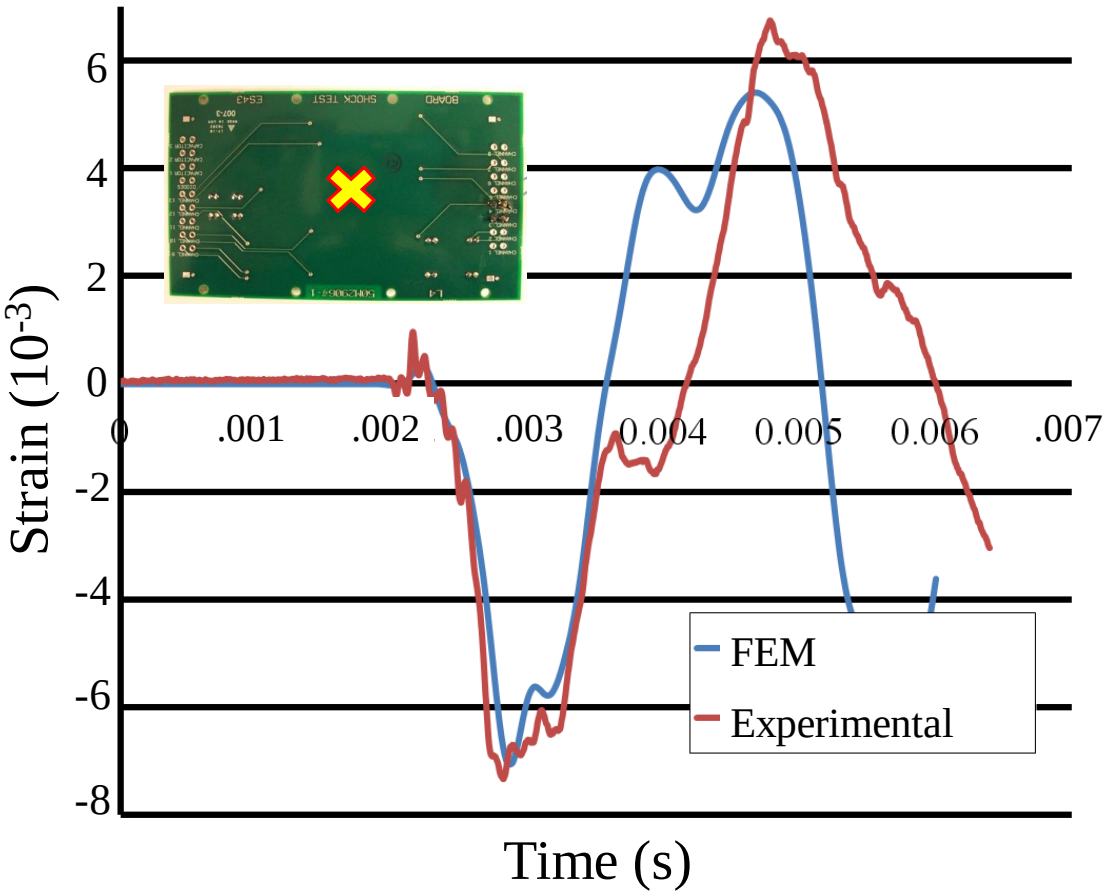


Figure 3-54: FEA vs. Experimental Strain - 50,000g

Sub-model Finite Element Analysis Results

The submodel for CCGA is analyzed using a global local modeling approach. A time history of the Von-mises stress is shown in Figure 3-55. Analysis of the individual stress components shown in Figure 3-56 shows that the highest stress values occur in the out of plane Z direction. This correlates well with the necking that occurs during both failure modes.

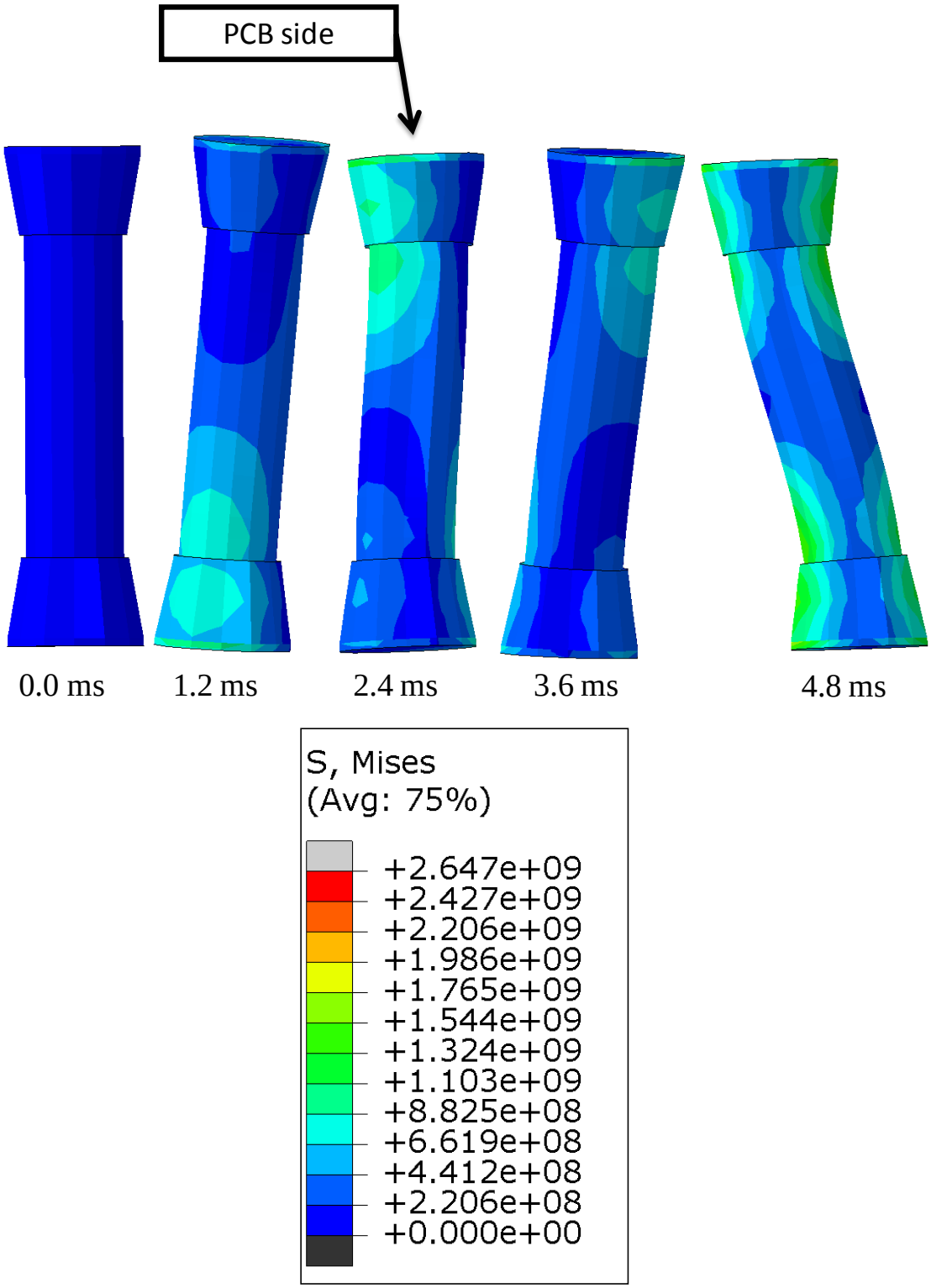


Figure 3-55: CCGA Von-mises stress contour

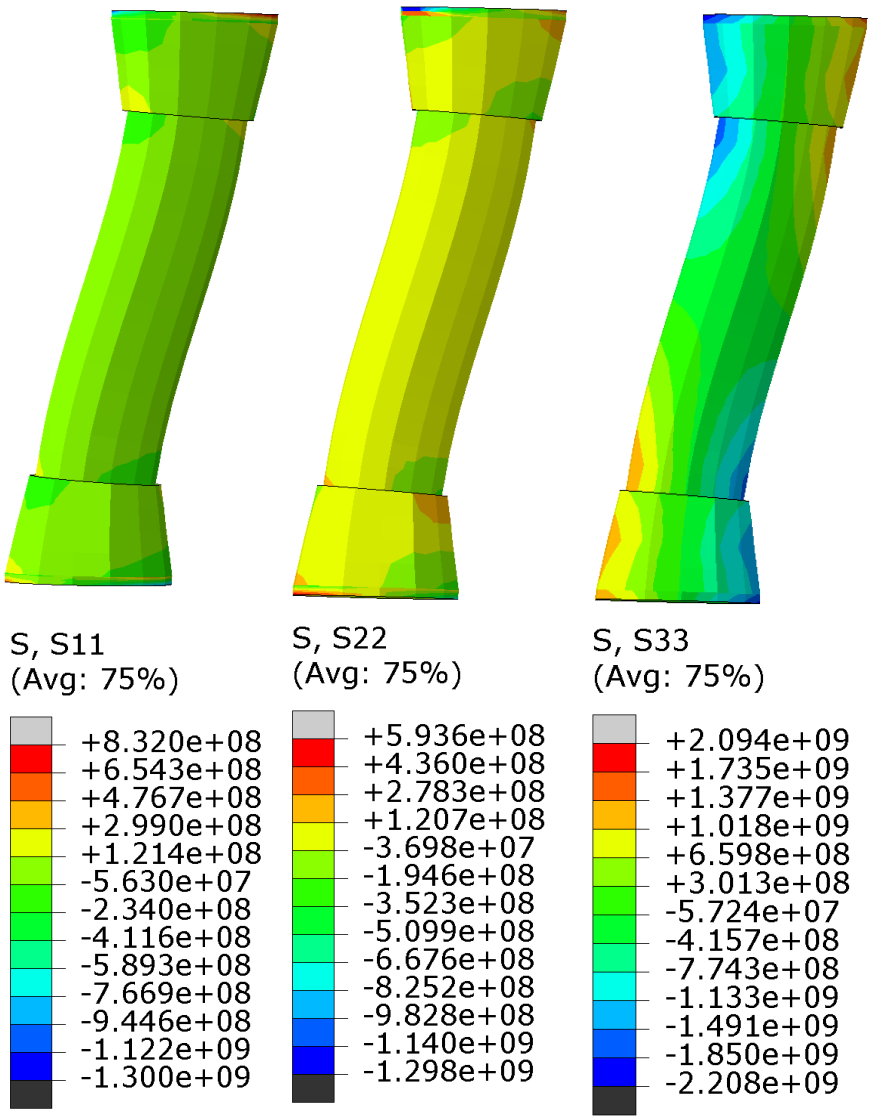


Figure 3-56: CCGA stress components

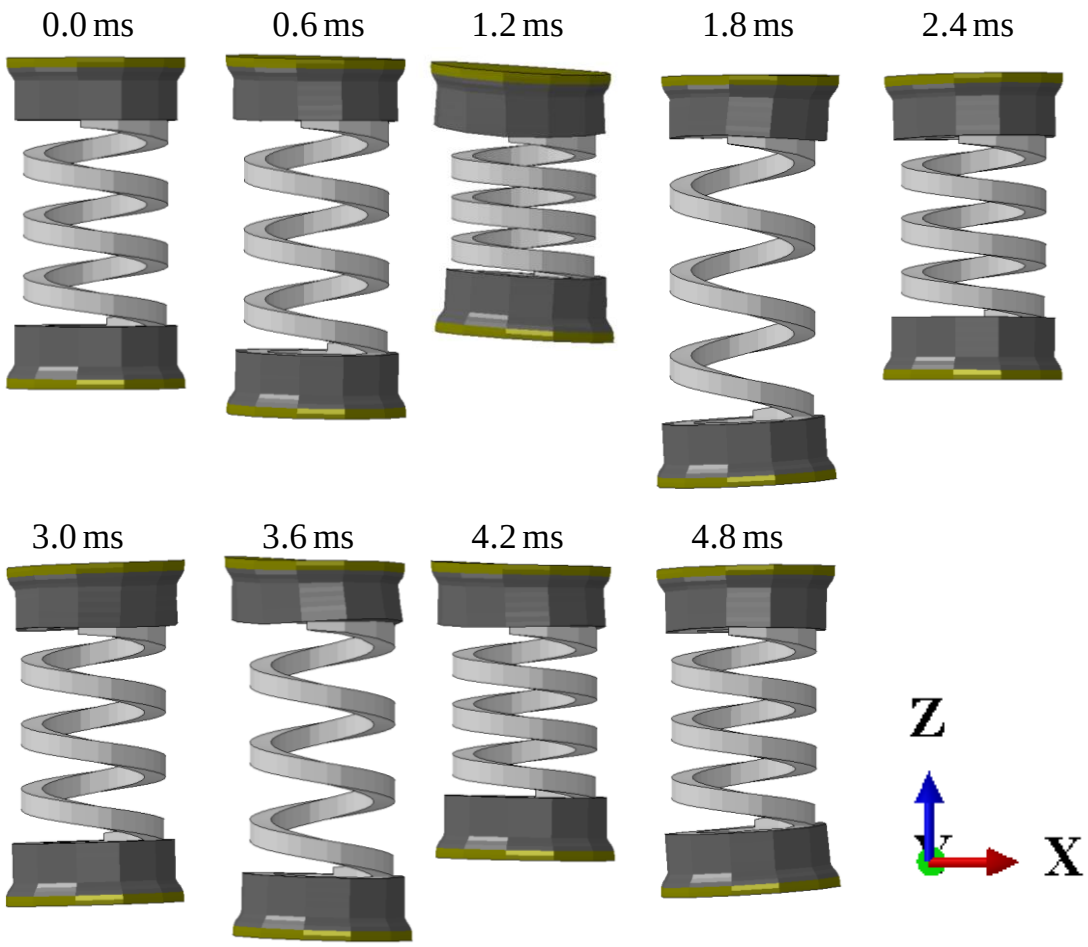


Figure 3-57: MCS deflection time history

Figure 3-58 shows the stress contours that occur while the coil is in compression. Model predictions indicate that the failure is likely to occur in the coils of the MCS. This correlates well with the failure analysis. Figure 3-59 shows the stress contours that occur at the maximum coil deflection. Results show that the shear stresses in the coil are the highest in magnitude. Similar to the compression contours, stress concentrations occur only for the two shear stress contours. Similarly, according to the simulation, failure is likely to occur in the coils of the MCS. This again correlates well with failure analysis.

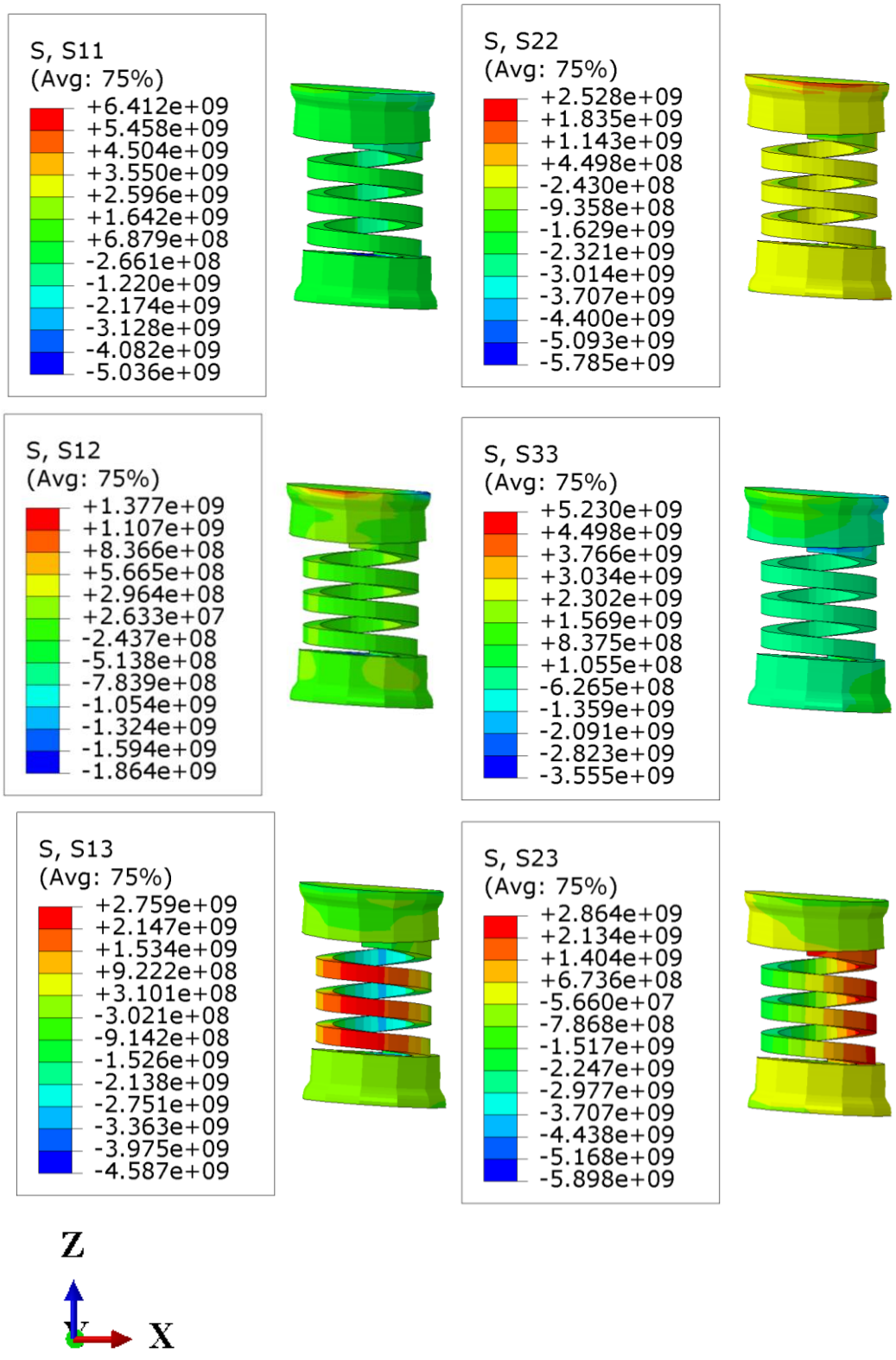


Figure 3-58: MCS stress components during compression

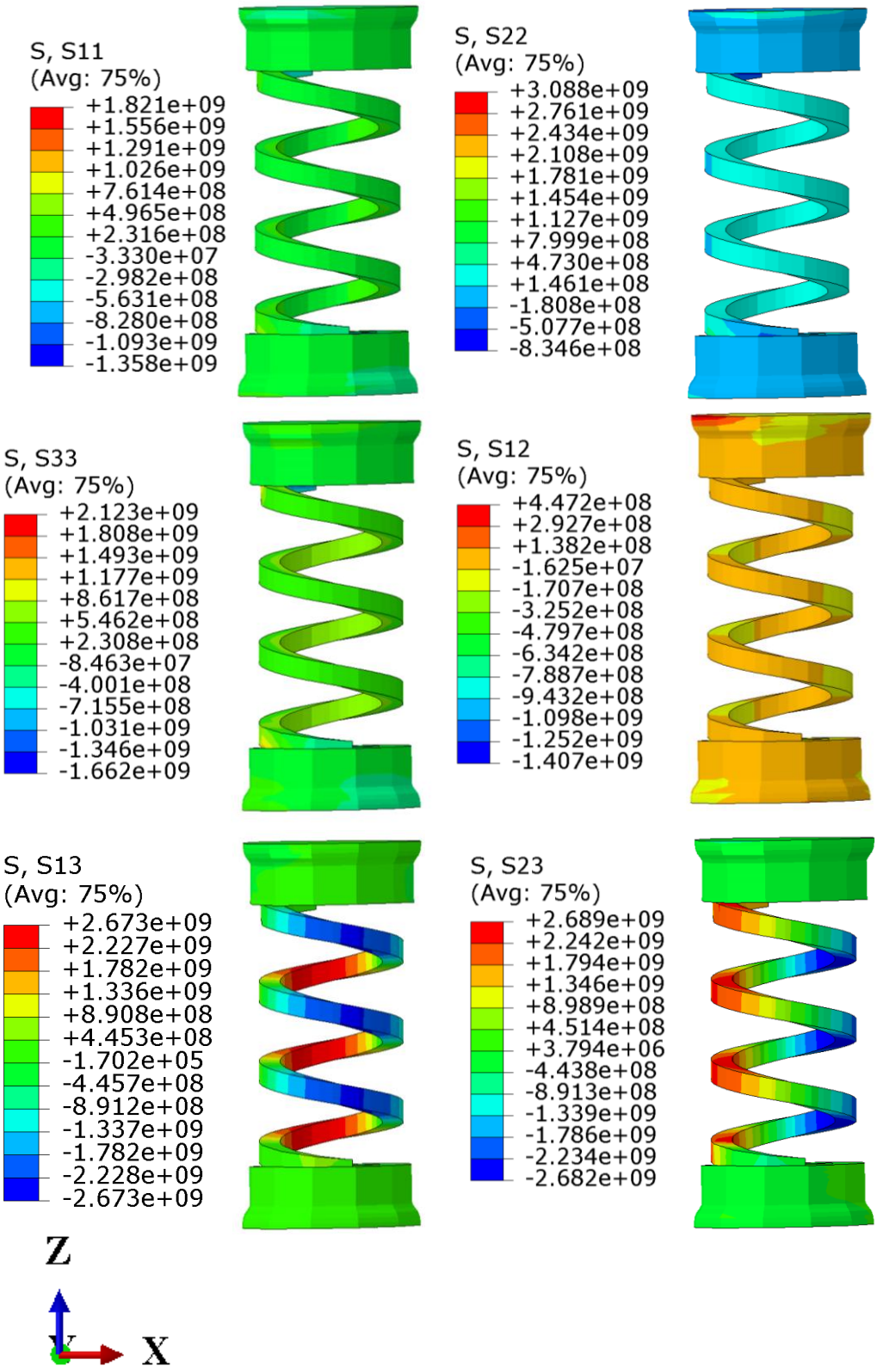


Figure 3-59: MCS stress components at max deflection

4. Finite Element Analysis and Evaluation of Warpage for Package-on-Package (PoP) Components

4.1 Introduction

The demand for increases in I/Os and decrease in package size has created a trend of using 3D packaging architectures. Three-dimensional packages utilize space in the out-of-plane direction to decrease the amount of board space used while still increasing the number of inputs and outputs. One of the more common package architectures used in 3D packaging technology is the PoP (Package on Package) component type. In this configuration, two or more packages are generally stacked on top of each other with one of the packages generally being a logic type and the other being memory type. A schematic of a common PoP configuration is shown in Figure 4-1. For proper board-level assembly, great care must be taken to ensure co-planarity exists between the stacked packages. This is of greatest concern during the reflow process where a large amount of warpage occurs due to high temperatures.

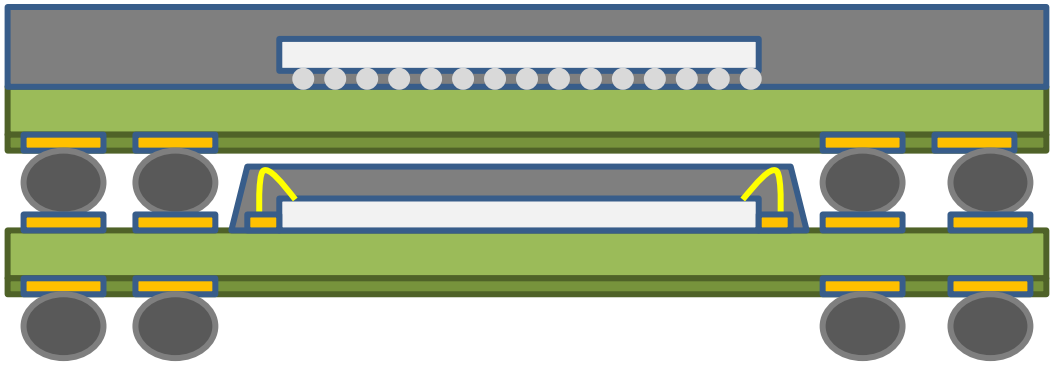


Figure 4-1: A common PoP configuration

Warpage is defined as the out of plane displacement that occurs in electronic components due to processing conditions, material properties selection, and package architecture. In the past, studies have been performed to examine the warpage that occurs in packages during reflow processes [Yen 2008, Lin 2008, Sun 2008]. A mismatch in the CTE of the various layers of the package such as the die, the mold, and the substrate results in either a positive or negative warpage. Slower expansion of the mold and faster expansion of the substrate results in the smiley face up warpage. More expansion of the mold and less expansion of the substrate may result in a smiley face down warpage. A schematic showing this phenomenon is shown in Figure 4-2. The mismatch of the CTE is of greatest concern when the package is exposed to higher temperatures such as those of a reflow environment. Warpage is characterized as positive or negative according to the shape it produces from a 2D perspective. The sign convention used for this study is shown in Figure 4-3. Smiley face down is defined as a positive warpage while smiley face up is defined as a negative warpage.

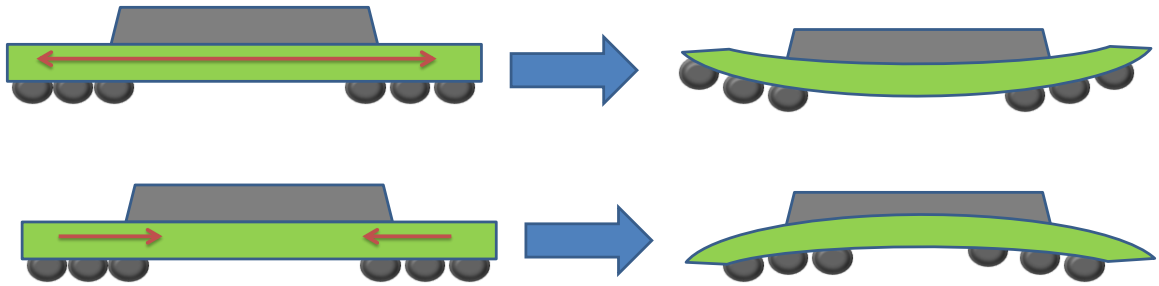


Figure 4-2: Warpage phenomenon schematic

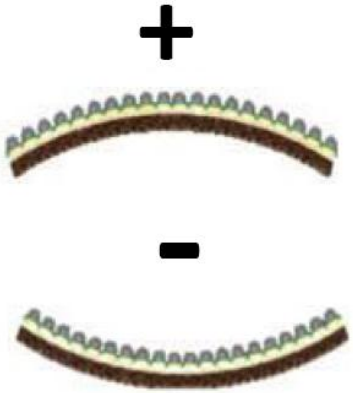


Figure 4-3 : Warpage sign convention

Since electronic packages are more susceptible to warping at high and low temperatures, warpage during a solder reflow environment is an important factor to consider. Conventionally, shadow moiré interferometery is used to measure the warpage of a package during temperature changes. In this study, an image processing technique called DIC, digital image correlation, is also used. In the past, DIC has been used to measure full field displacement and deformation in electronics subjected to drop events [Lall 2007b, 2008a,b, Miller 2007, Park 2007a,b, 2008], the damping ratio on the surface of a board [Peterson 2008], bending on portable products subjected to impact testing [Scheijgrond 2005], solder interconnect stresses under thermal loadings for BGA package

types [Bieler 2006, Rajendra 2002, Sun 2006, Xu 2006, Yogel 2001, Zhang 2005, Zhou 2001], and stresses and strains under thermal loading for flip-chip dies [Kehoe 2006].

Warpage values are greatly affected by process conditions, material properties and package architecture. Previously researchers have analyzed the effects of material properties on package warpage using finite element analysis [Amagai 2010, Sun 2008]. For this study, the effects of process conditions are assumed as an initial condition and the effects of material properties and package architecture are examined in detail using FEA. Table 4-1 shows the ranges of package architecture and material properties that have been examined.

Table 4-1: Range of values examined

Parameter	Values
Package Dimensions	12-14 mm
EMC Thickness	0.2-0.3 mm
Substrate Thickness	80-120 µm
EMC CTE1	10-16 ppm/C
EMC CTE2	34-74 ppm/C
EMC E1	18-26 GPa
EMC E2	0.6-3 GPa
Substrate CTE	3-7 ppm/C
Substrate Elastic Modulus	25-35 GPa
Chip Dimensions	7-10 mm
Chip Thickness	50-150 µm
Chip CTE	2-3 ppm/C
Chip Elastic Modulus	140-170 GPa

In this study, finite element modeling has been used to determine the effects of various input values on warpage. The examined values include variations on material properties and package dimensions. The material properties examined include the properties of the epoxy molding compound, the core material found in the substrate, and the die material. Material properties such as the coefficients of thermal expansion (CTE) and the elastic modulus (E) of each compound have been varied to see the effect it has on warpage. Geometric architecture values have also been varied to examine the effects that layer thickness has on warpage. The thickness of the epoxy molding compound, the substrate core, and the chip has been varied to study to effects it has on warpage. Another influential factor on warpage may be the effects of die dimensions. Die dimensions have been varied within a reasonable range to determine the effects it has on warpage.

4.2 Test Vehicles

Two different package types are used as test vehicles for this study. Test Vehicle-1 is a PoP package which utilizes copper landing pads for 3D stacking. The package architecture is shown in Figure 4-4 and the package specifications are shown in Table 4-2.

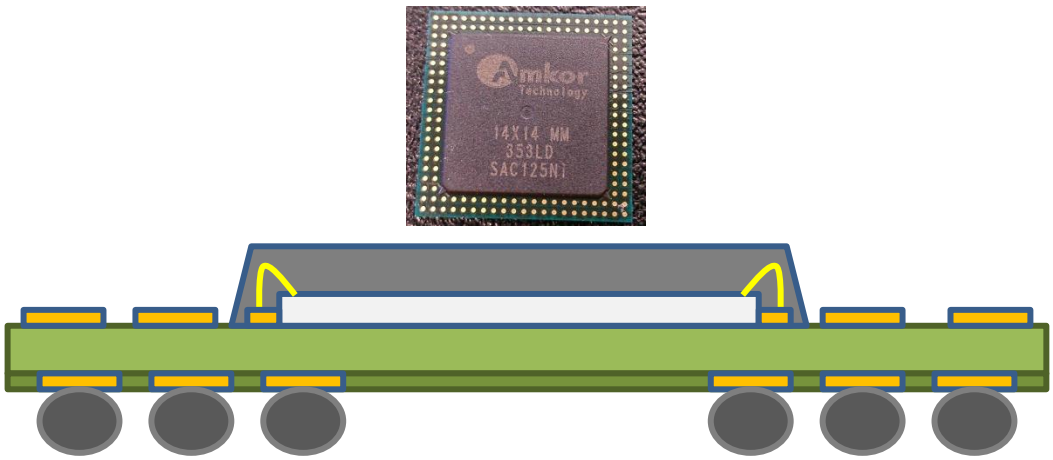


Figure 4-4: Test vehicle 1 package architecture

Table 4-2: Test vehicle 1 package specifications

	Package-A	**Package-B**
Package Size	12mm x 12mm	14mm x 14mm
Package Thickness	0.6mm	0.6mm
Die Size	7mm x 7mm	8.9mm x 8.9mm
Die Thickness	100 µm	100 µm
Footprint Bottom Side	0.5mm Pitch, 305 I/O 23x23 Matrix 4 rows, 12NC, A1 Ball	0.5mm Pitch, 353 I/O 26x26 Matrix 4 rows, 12NC, A1 Ball

Test Vehicle-2 is a PoP package that uses through mold via (TMV) technology for 3D stacking. The package architecture for Test Vehicle-2 is shown in Figure 4-5 and the package specifications are shown in Table 4-3.

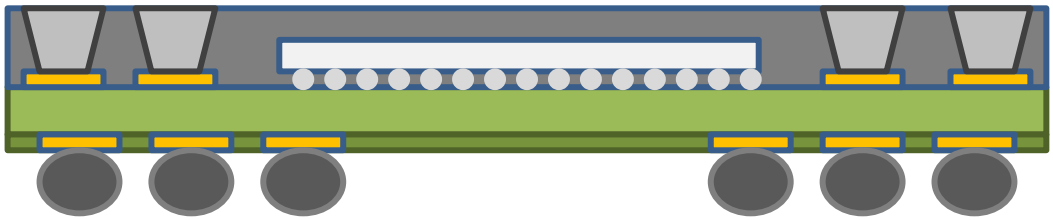


Figure 4-5: Test vehicle 2 package architecture

Table 4-3: Test vehicle 2 package specifications

	Package-A	**Package-B**
Package Size	12mm x 12mm	14mm x 14mm
Package Thickness	0.6mm	0.50mm - 0.57mm
Die Size	8.47mm x 8.24mm	9mm x 9mm
Die Thickness	60 - 100 μm	100 μm
Footprint Bottom Side	0.4mm Pitch, 559 I/O 28x28 Matrix, De-Populated	0.5mm Pitch, 325 I/O

4.3 Experimental Set Up

A conventional lead-free reflow oven is used for this study. Test vehicles have been exposed to a lead-free reflow temperature profile to simulate the temperature changes present during an actual reflow process. The reflow profile has a peak temperature of 250 °C. The temperature profile used for this experiment is shown in Figure 4-6.

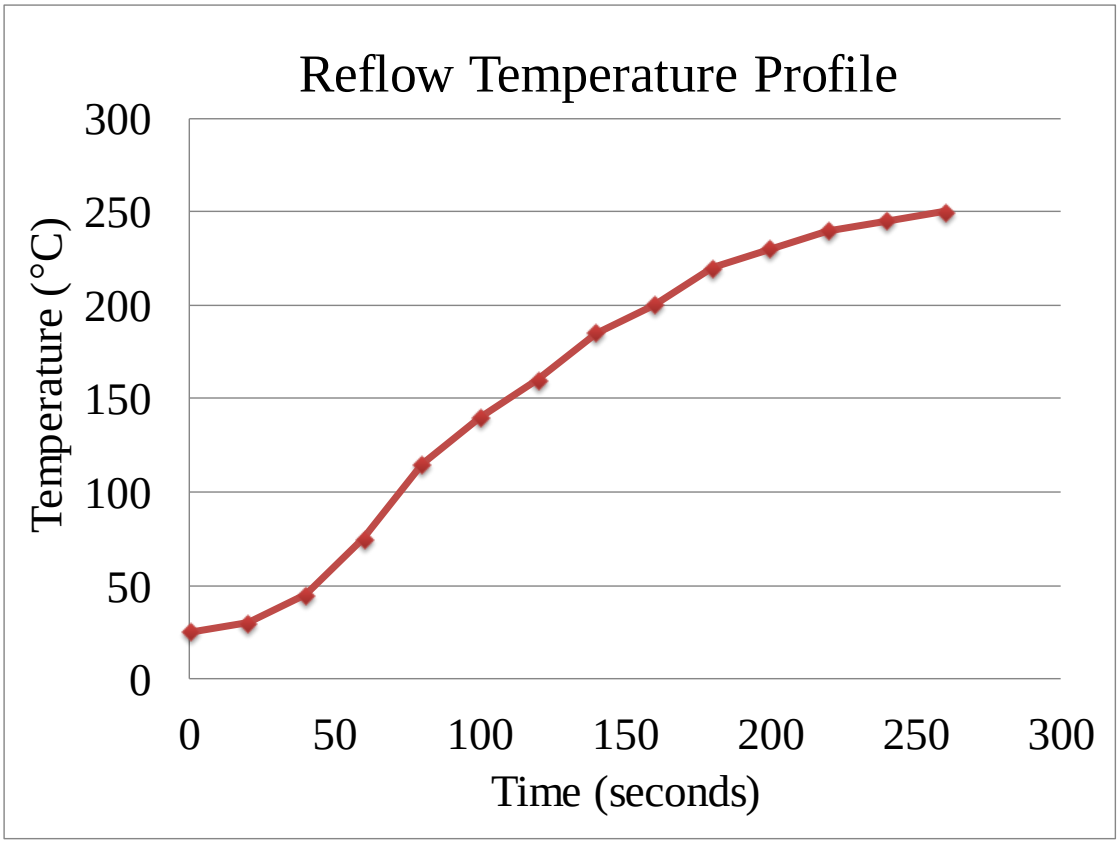


Figure 4-6: Temperature profile for reflow

A glass window installed on top of the lead free reflow oven allows for visual inspection of components while reflow is occurring. Two high resolution low speed cameras simultaneously capture images of the test specimen while the package is being subjected to the reflow temperature profile. Figure 4-7 is a schematic showing the experimental set up used in this study.

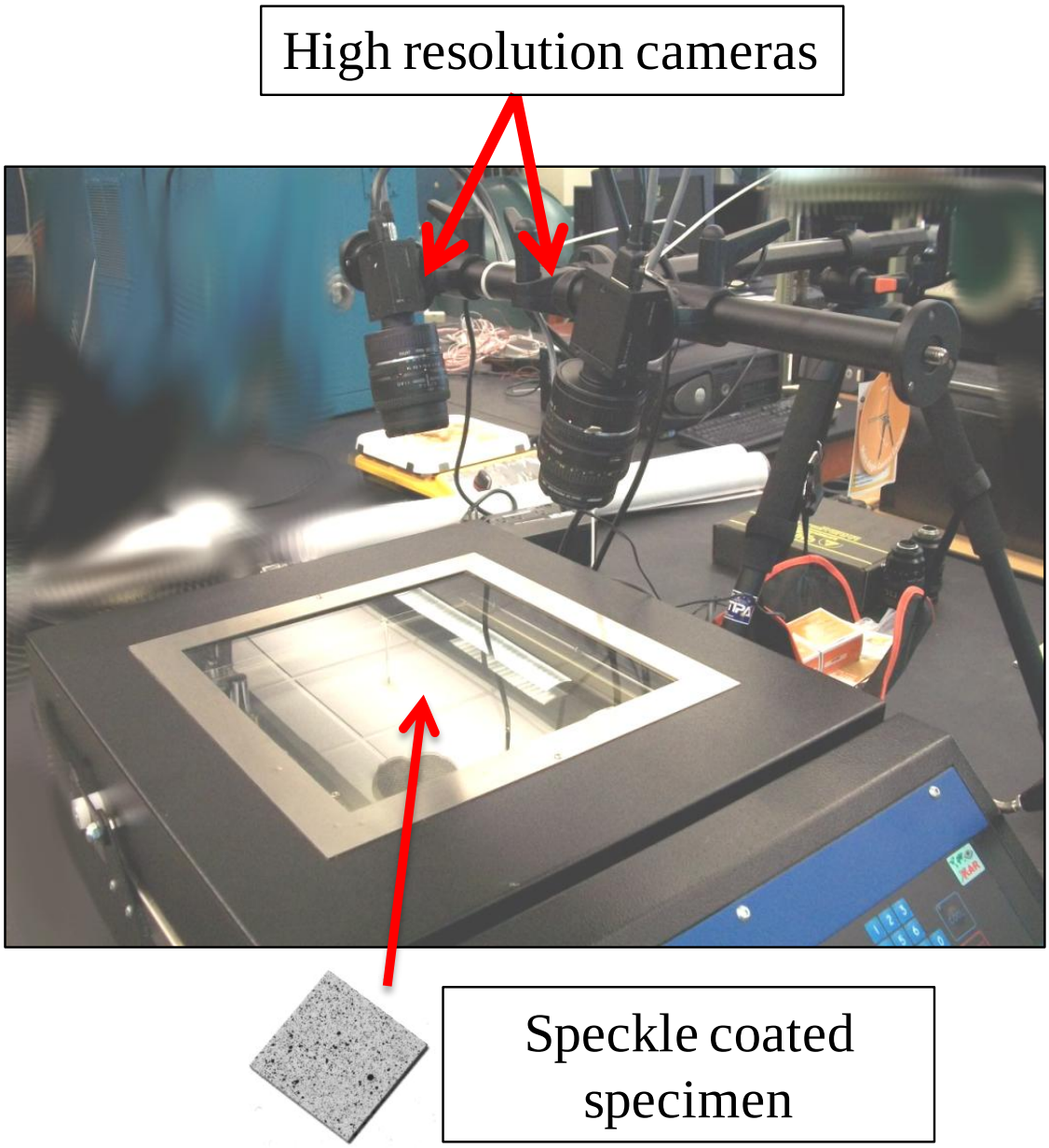


Figure 4-7: Experimental set up

An optical method, digital image correlation (DIC), has been used to measure the warpage in packages during reflow. The usability of DIC for displacement measurements in electronic assemblies has been shown [Lall 2007[a-e], 2008[a-d]]. Digital image correlation is a technique that uses speckle patterns on the surface of the test specimen to trace a geometric point during deformation. This information is then used to

determine the out of plane deformation. The specimens must be de-balled to provide a flat surface for speckle coating processes. Figure 4-8 is a schematic showing the principle of DIC for a three dimensional case.

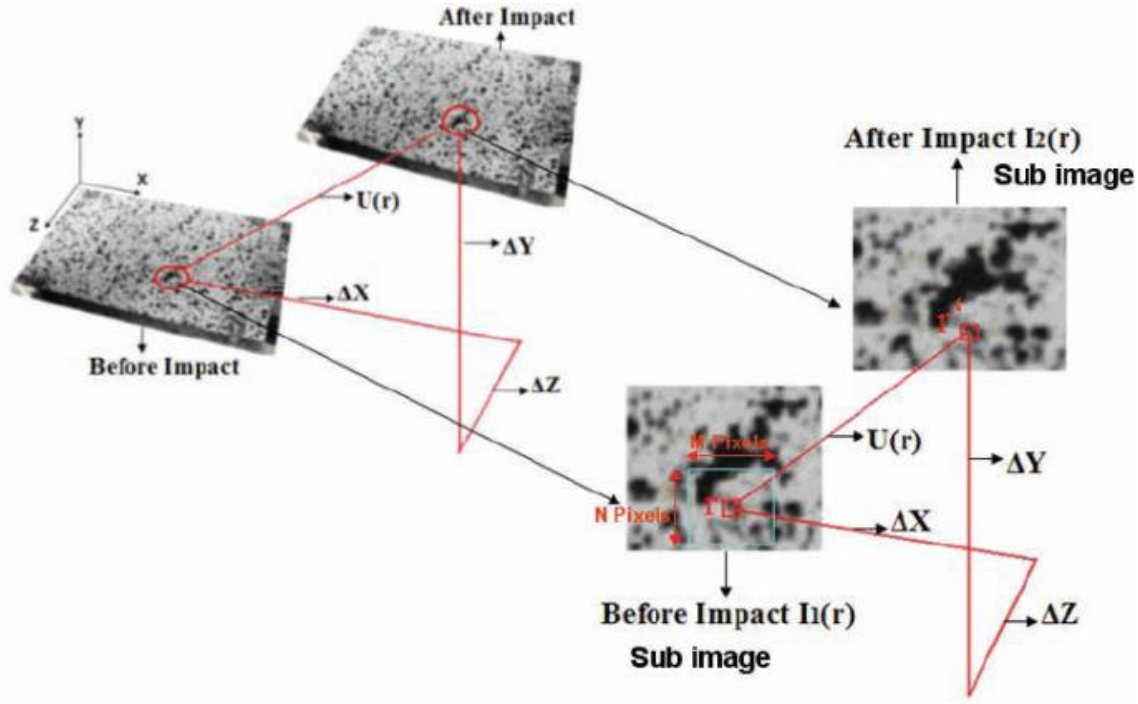


Figure 4-8: Digital image correlation for a 3D case

A full field displacement contour is obtained from image processing. Warpage is typically measured from the corners of the package to the center. This same convention is used for this study. Figure 4-9 shows a representative warpage contour along with the diagonal along which warpage is measured.

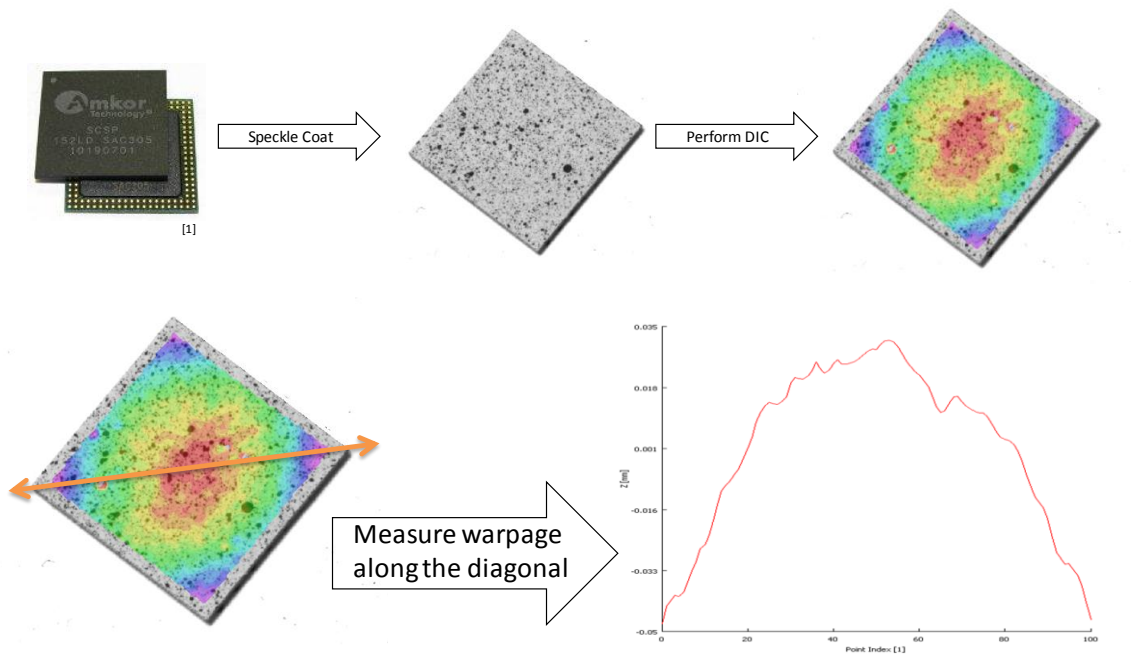


Figure 4-9: DIC Out-of-plane displacement contour

4.4 Finite Element Analysis

Finite element analysis is performed to determine the effects of material properties and package architecture on warpage. Test vehicle 2, package type A is modeled. Detailed models of all layers are considered including the epoxy molding compound (EMC), silicon die, copper layers, prepreg, and laminate core. Isotropic and homogeneous properties are assumed. The effects of through mold vias are also considered and have been modeled as well. Solder balls have not been included in the model to reflect the effects of de-balling that has been used for the experimental portion. Figure 4-11 shows the finite element model of the TMV package.

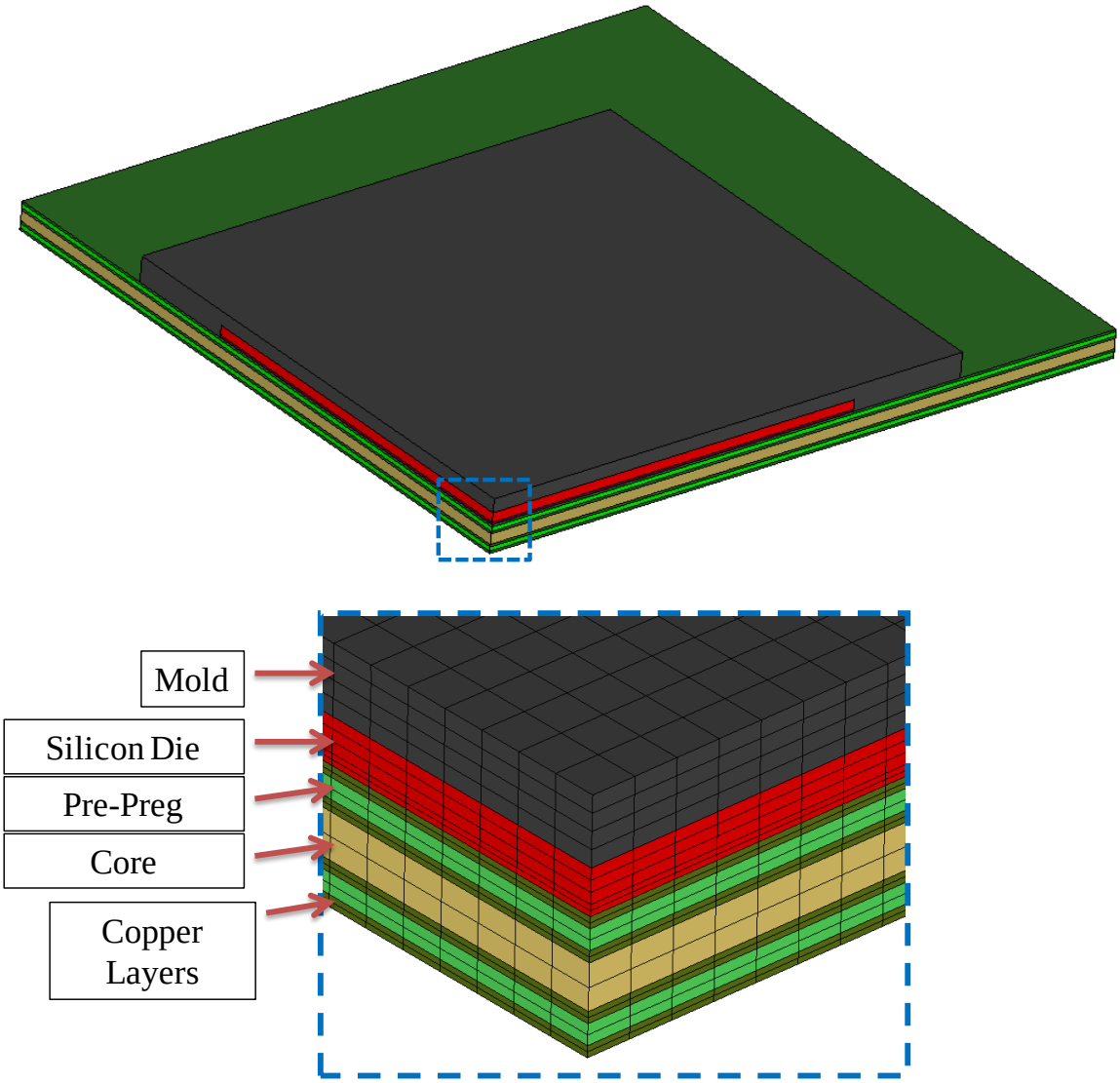


Figure 4-10: Test Vehicle 1 Package Type A FEM

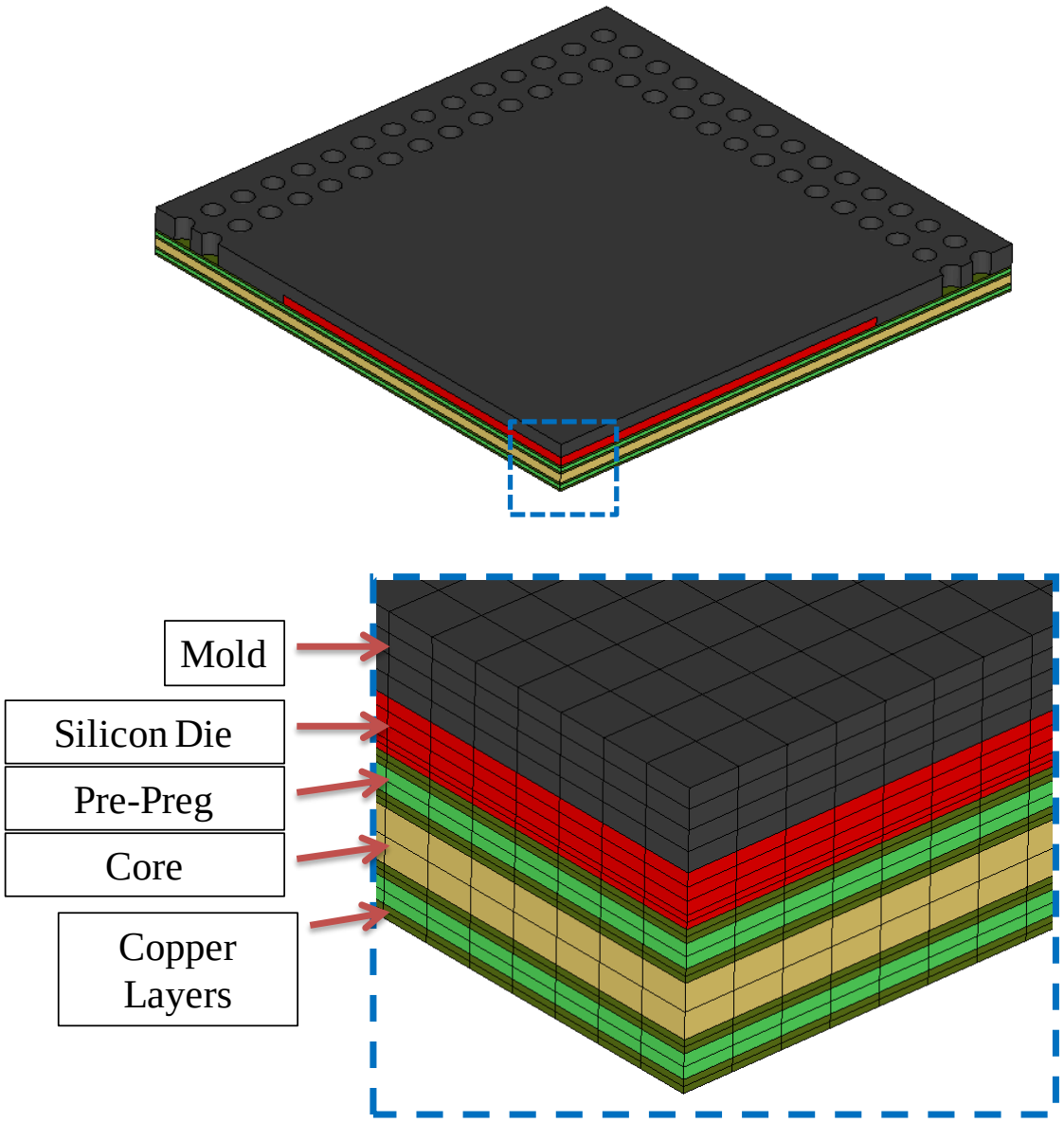


Figure 4-11: Test Vehicle 2 Package Type A FEM

The model is analyzed using C3D8R solid elements. A static thermal analysis is performed using ABAQUS. Temperature boundary conditions are prescribed to reflect the reflow temperature profile used during experimentation. Material properties are determined using a dynamic-mechanical analyzer (DMA) and a thermo-mechanical analyzer (TMA). Changes to material properties above and below the glass transition temperature (T_g) have been accounted. Visco-elastic effects are ignored for this study. Perfect adhesion between layers is assumed. A quarter symmetry model is used. As shown in Figure 4-12, quarter symmetry constraints are applied by constraining displacement in the X direction for nodes on the ZY plane and the Y direction for nodes on the XZ plane.

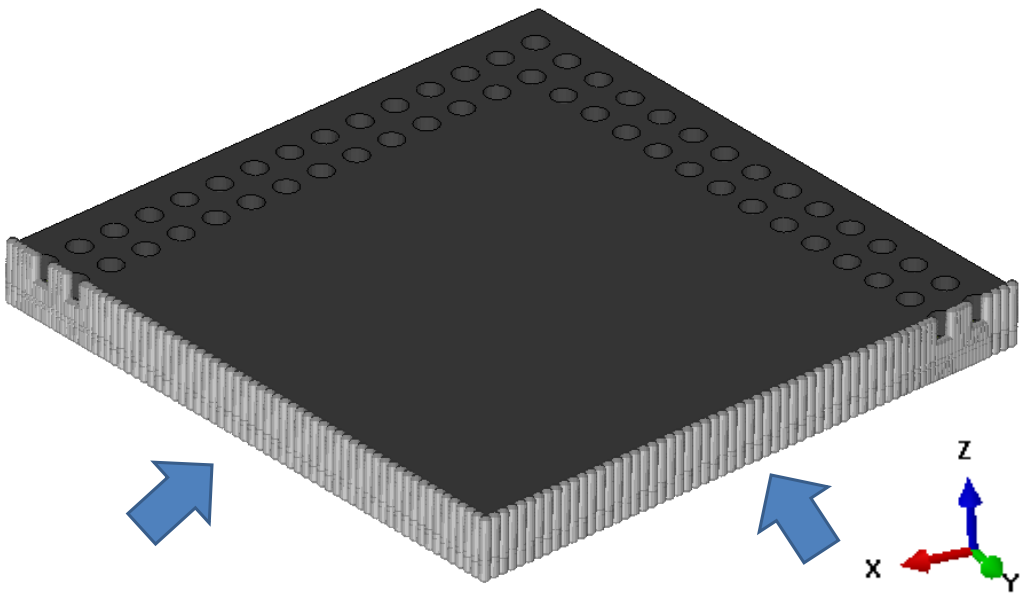


Figure 4-12: Quarter symmetry nodal constraints

The effects material property selection and package architecture have on package warpage are investigated. A baseline finite element analysis is defined using material

properties obtained from the TMA and DMA. Material properties are varied from the baseline values to determine the effects material selection has on warpage during reflow. As with the experimental data, warpage is measured along the diagonal from the corner to the center of the package. The results from the finite element analysis are shown in Figure 4-13. Figure 4-14 shows a contour plot of the out of plane displacement for the finite element analysis at 250 °C for a fully symmetrical case. The quarter symmetry model results are rotated to create the full model results. Figure 4-15 shows the contour plot at key temperatures.

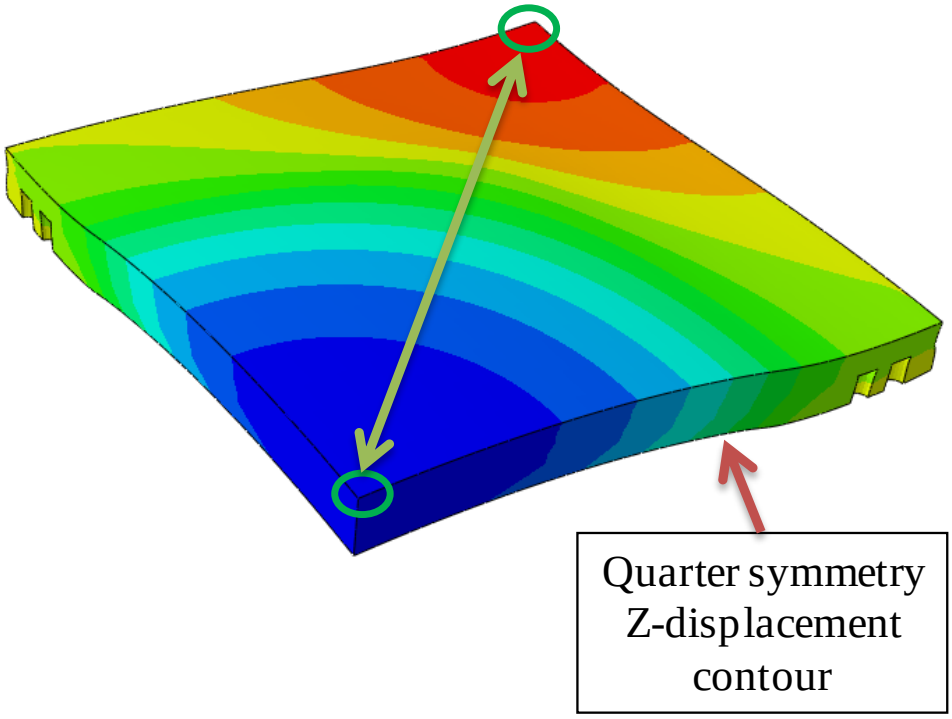


Figure 4-13: Quarter symmetry Z-displacement result

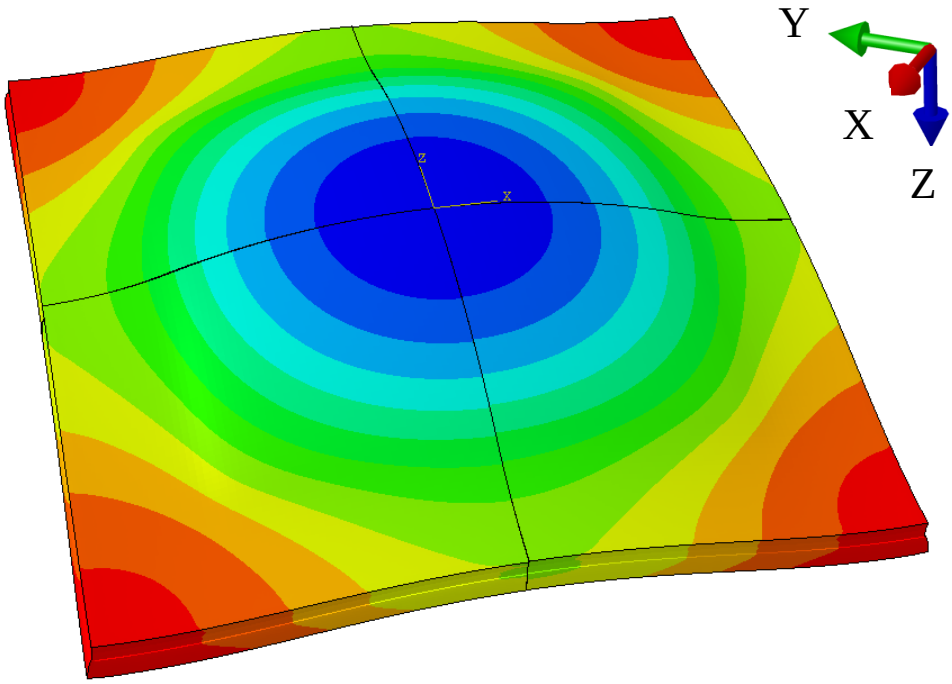


Figure 4-14: Fully symmetrical warpage representation at 250C

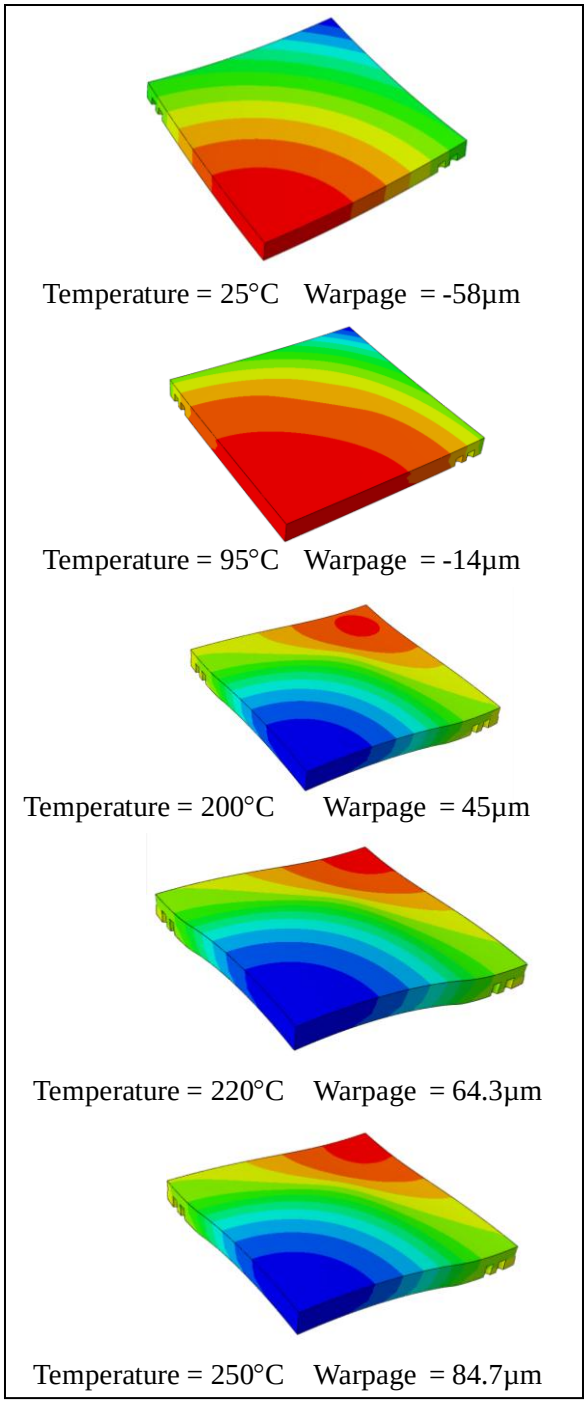


Figure 4-15: Warpage at key temperatures

The finite element results are correlated with experimental warpage values. Warpage has been measured from room temperature to the peak reflow temperature. Figure 4-16 shows a plot of the correlation between the baseline experimental data and the baseline finite element analysis. There is good correlation.

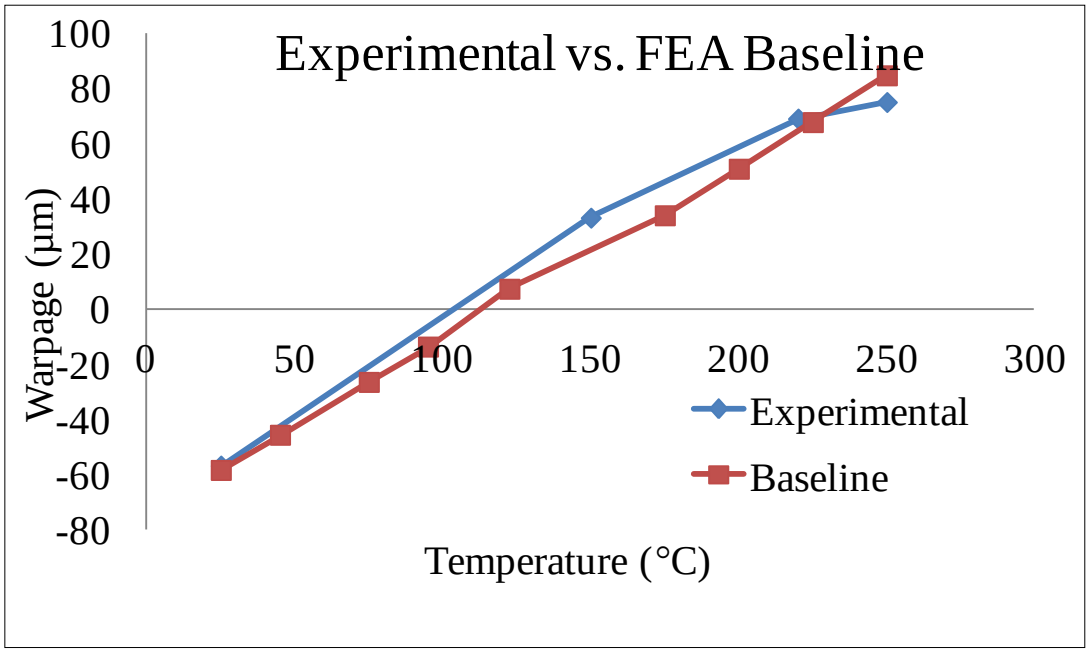


Figure 4-16: Experimental warpage Vs. FEA warpage

The effect of material property selection has on warpage is investigated by varying material property values such as CTE and elastic modulus in the finite element analysis. The effects of package architecture on package warpage has also been investigated by varying characteristics of the package architecture including package length, package width, package thickness, die thickness, die length, die width, and core thickness.

4.5 Material Properties and Dimensions Effects on Warpage

Core Properties Variation

Figure 4-17 shows the effects of core CTE variation. The trend shows that increasing the CTE of the core material will results in a higher warpage at the peak temperature. The opposite is true for the variation of the core elastic modulus. Figure 4-18 shows that as the elastic modulus of the core material increases, the warpage decreases at the peak temperature. Figure 4-19 shows a trend of decreasing warpage at peak temperature as the thickness of the core material is increased.

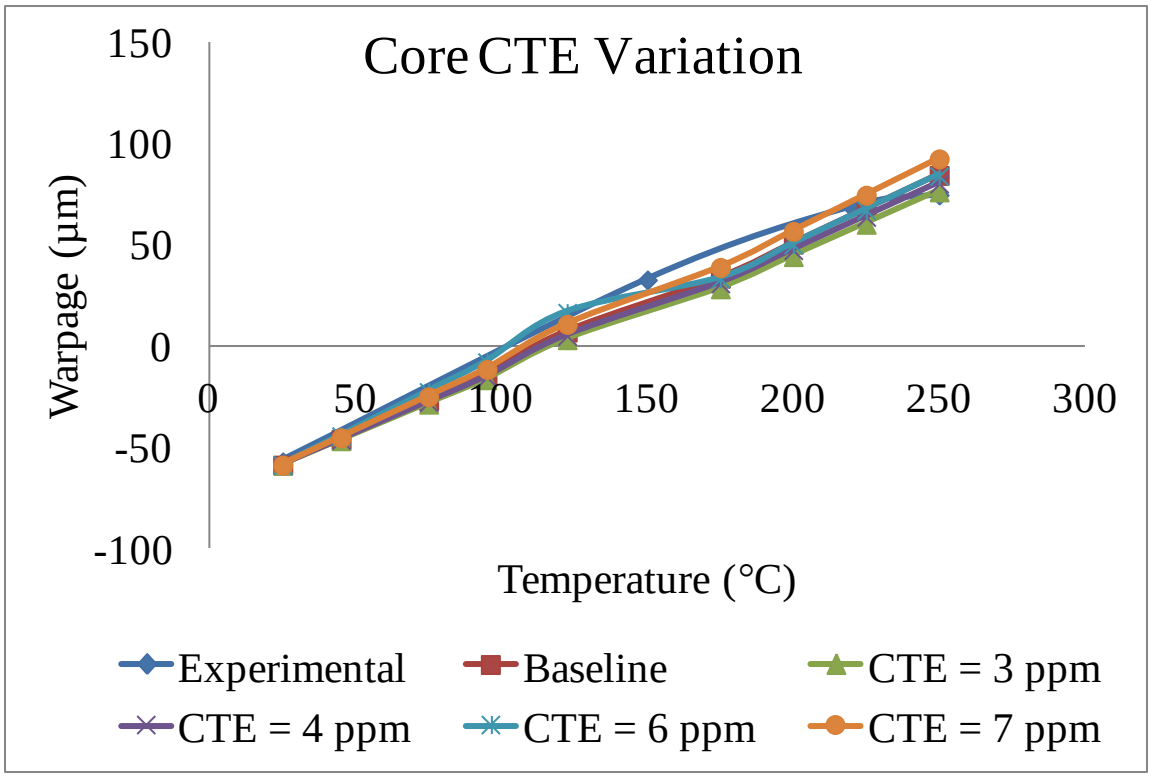


Figure 4-17: Warpage for substrate core CTE variation

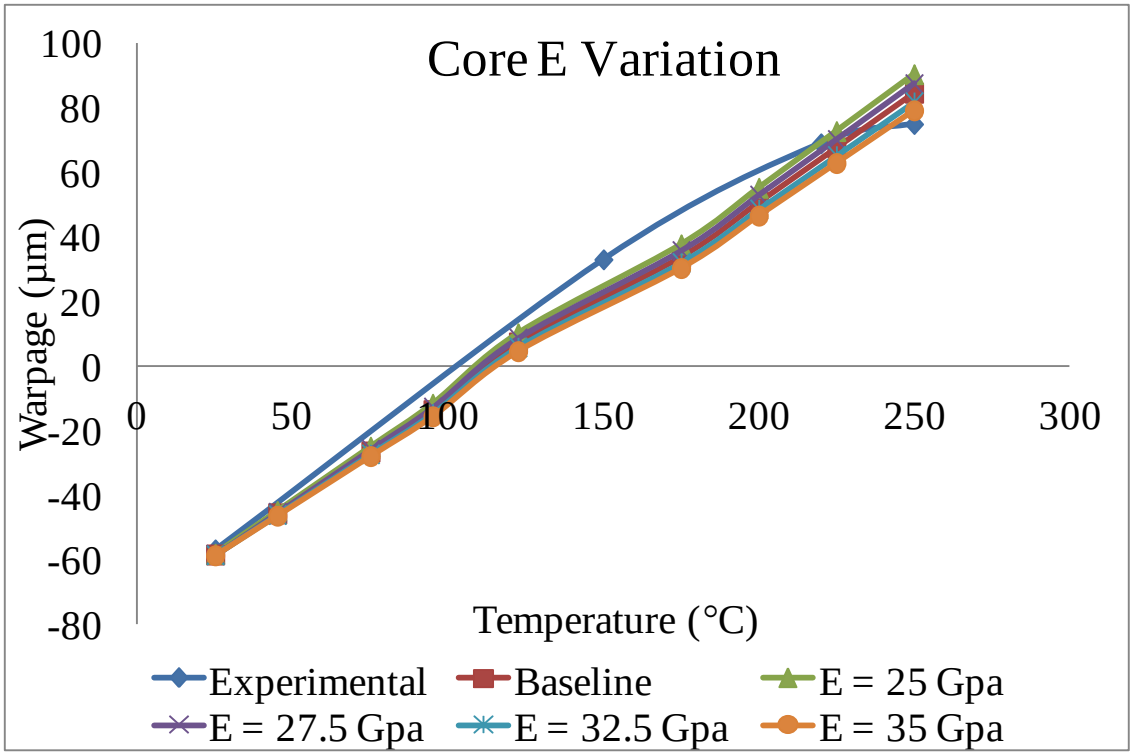


Figure 4-18: Warpage for substrate core E variation

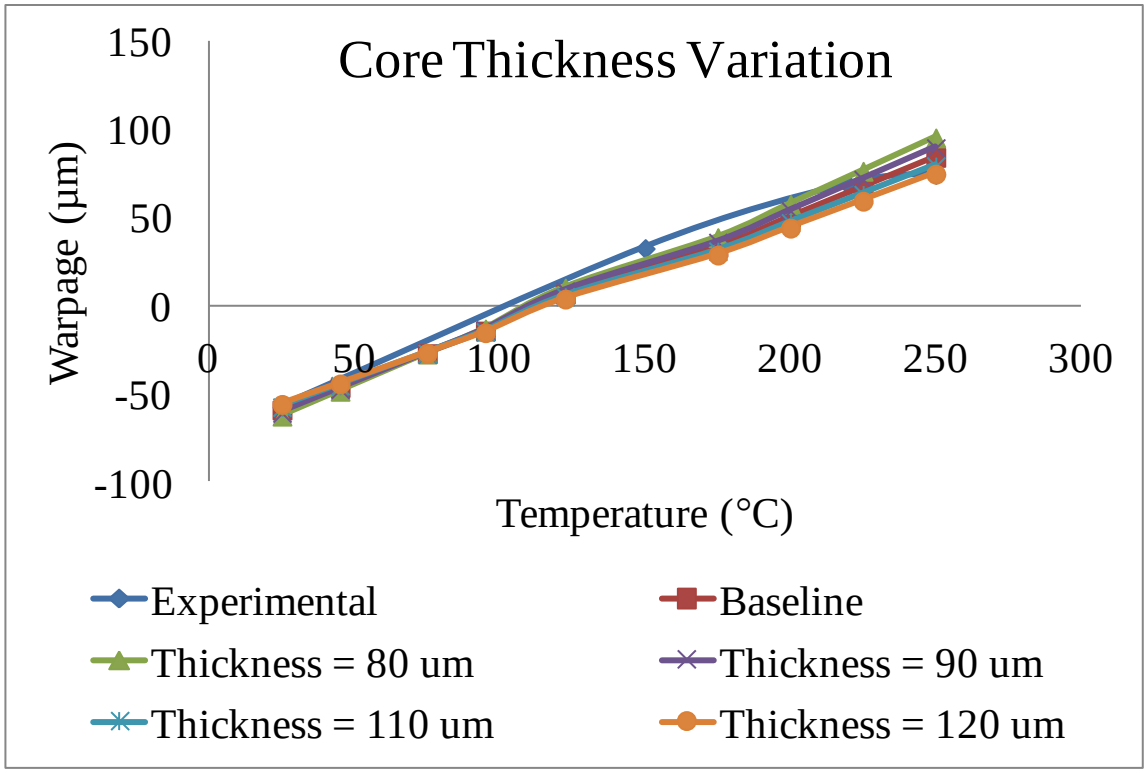


Figure 4-19: Warpage for core thickness variation

Silicon Die Properties Variation

Figure 4-20 shows that a very small change occurs in the warpage at the peak temperature as the CTE of the silicon die is changed. There is very little change from the variation since the range of values for the CTE of silicon is very small. The elastic modulus of silicon has a larger range of values. Figure 4-21 shows an increasing trend of warpage at peak temperature as the elastic modulus increases. The orthotropic properties of silicon are shown in Table 4-4. A large change in warpage from die thickness variation is shown in Figure 4-22. The trend shows that increases in die thickness will results in high warpage values. Figure 4-23 shows a positive trend in warpage as the dimensions of the die are increased.

Table 4-4: Silicon orthotropic material properties

Direction	Elastic Modulus	Units
[100]	129.5	GPa
[110]	168.0	GPa
[111]	186.5	GPa

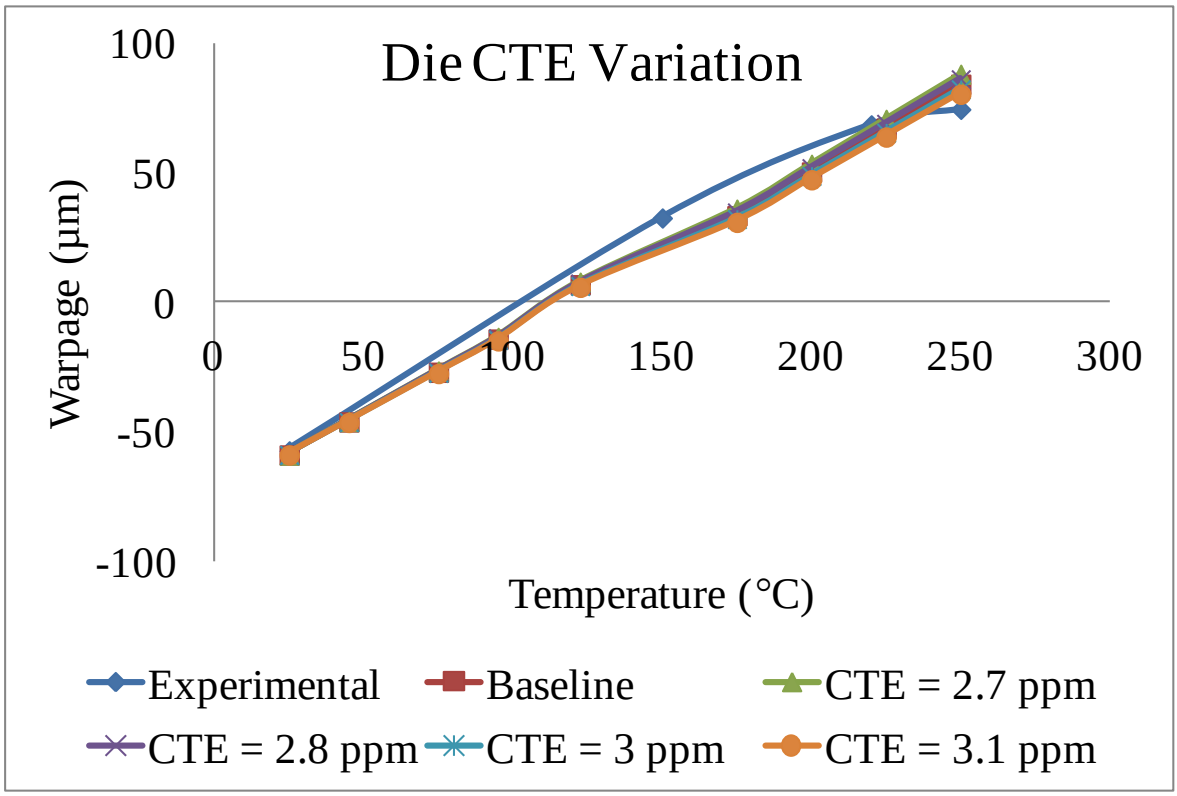


Figure 4-20: Warpage for silicon die CTE variation

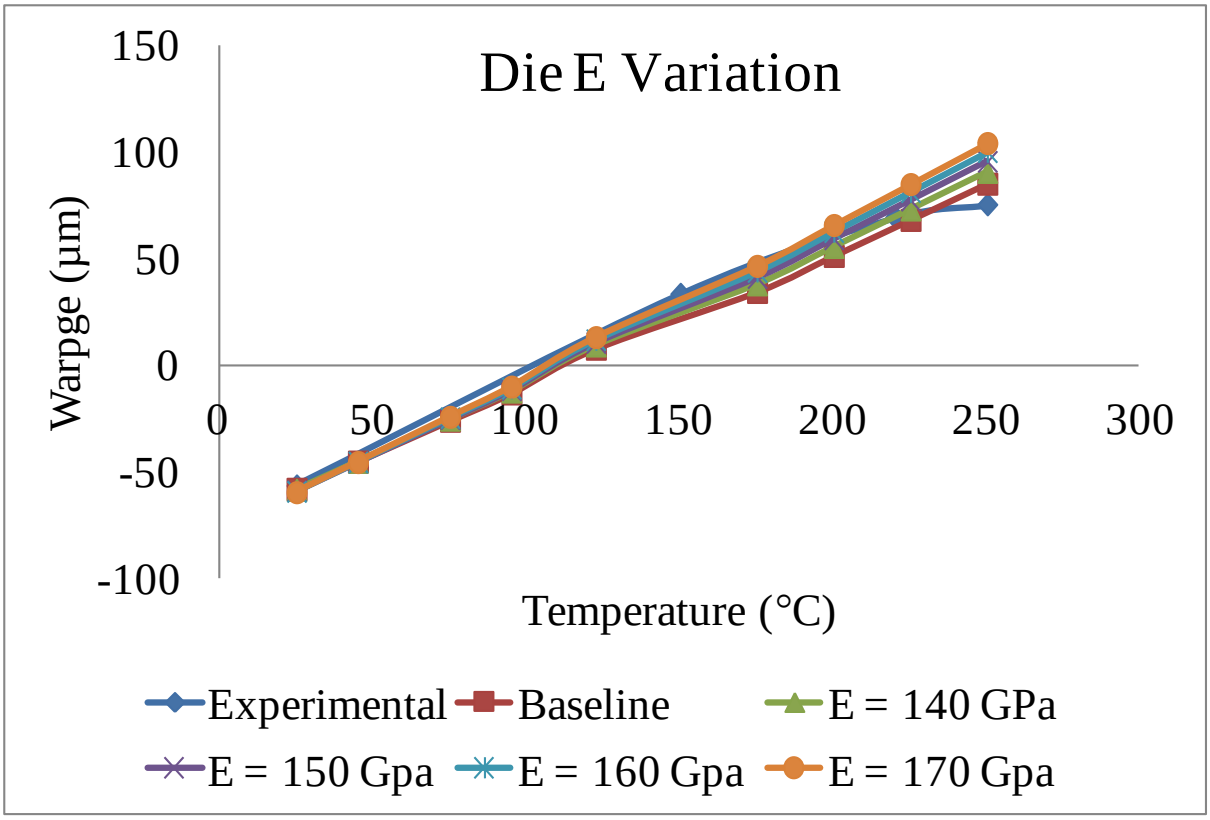


Figure 4-21: Warpage for die E variation

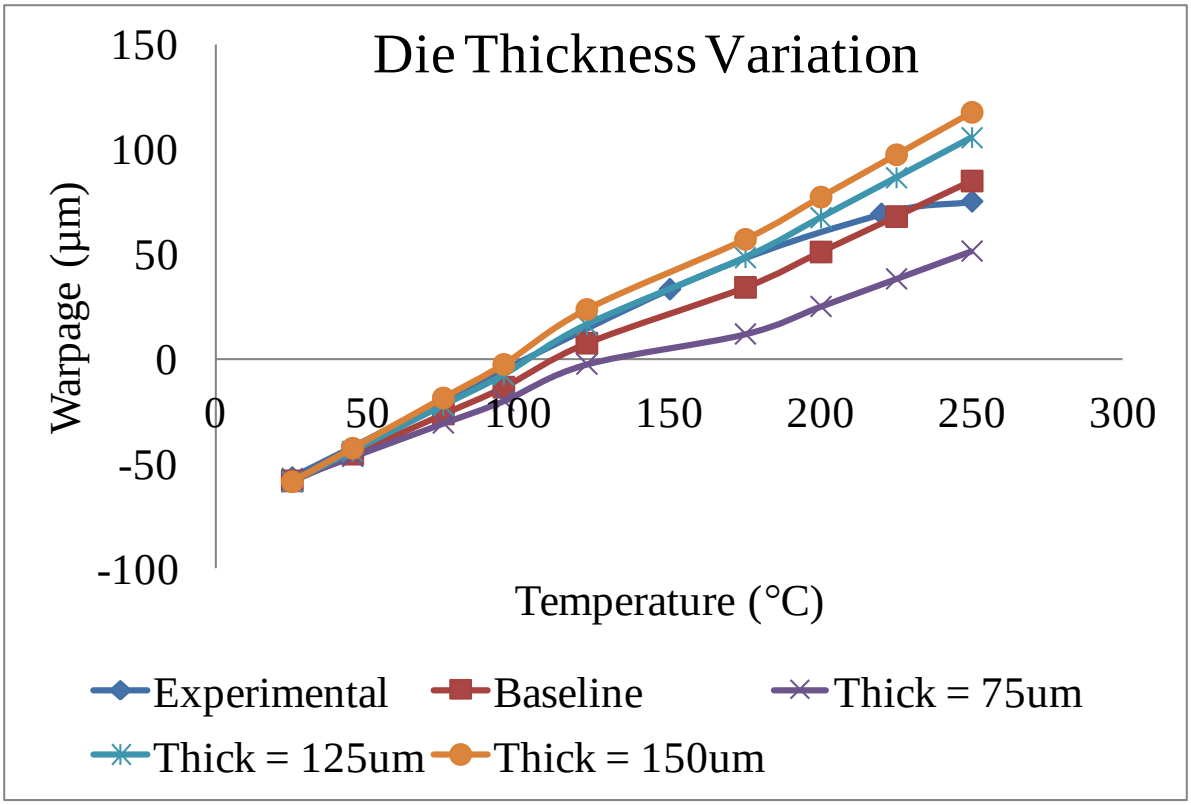


Figure 4-22: Warpage for die thickness variation

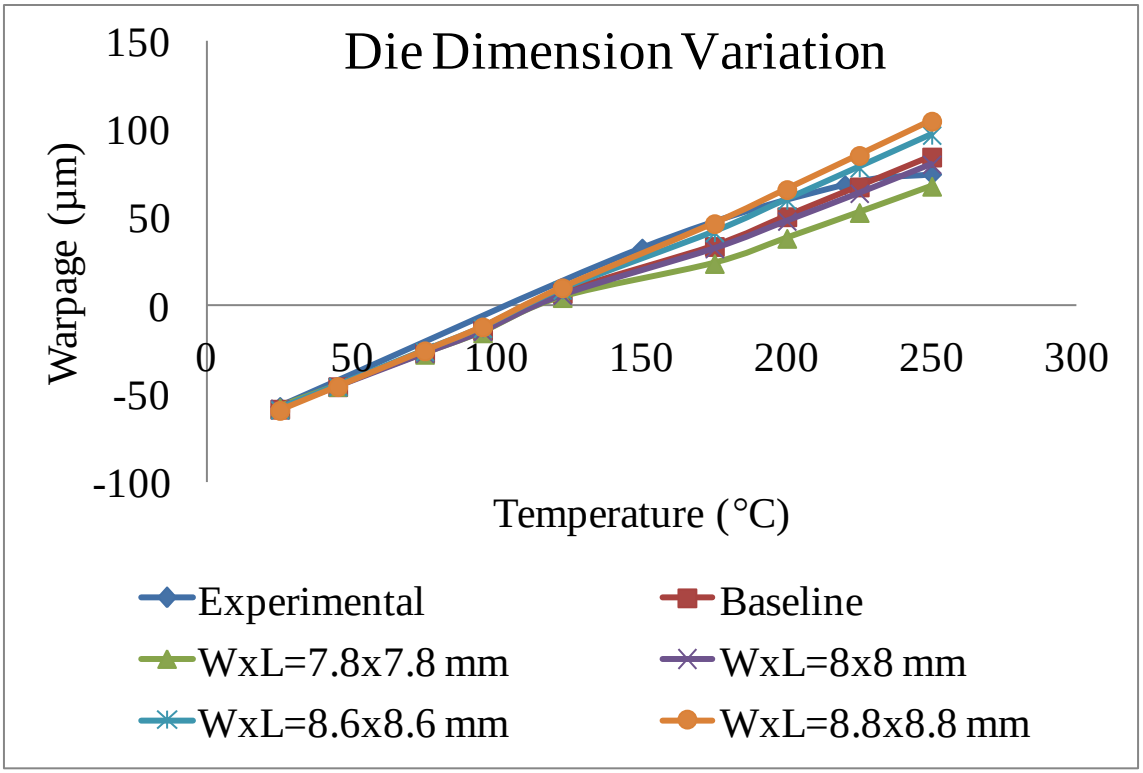


Figure 4-23: Warpage for die dimension variation

Mold Properties Variation

Figure 4-24 and Figure 4-25 show a decreasing trend in warpage for both cases where the CTE above and below liquidus temperature (T_g) is increased. Figure 4-26 shows a very small change in warpage below the T_g for change in Mold E1. Conversely, the warpage shows large variation with changes in Mold E2. A decreasing trend of warpage as E2 is increasing is shown in Figure 4-27 An increase in the thickness of the epoxy molding compound is shown to have a decrease in warpage in 4-28.

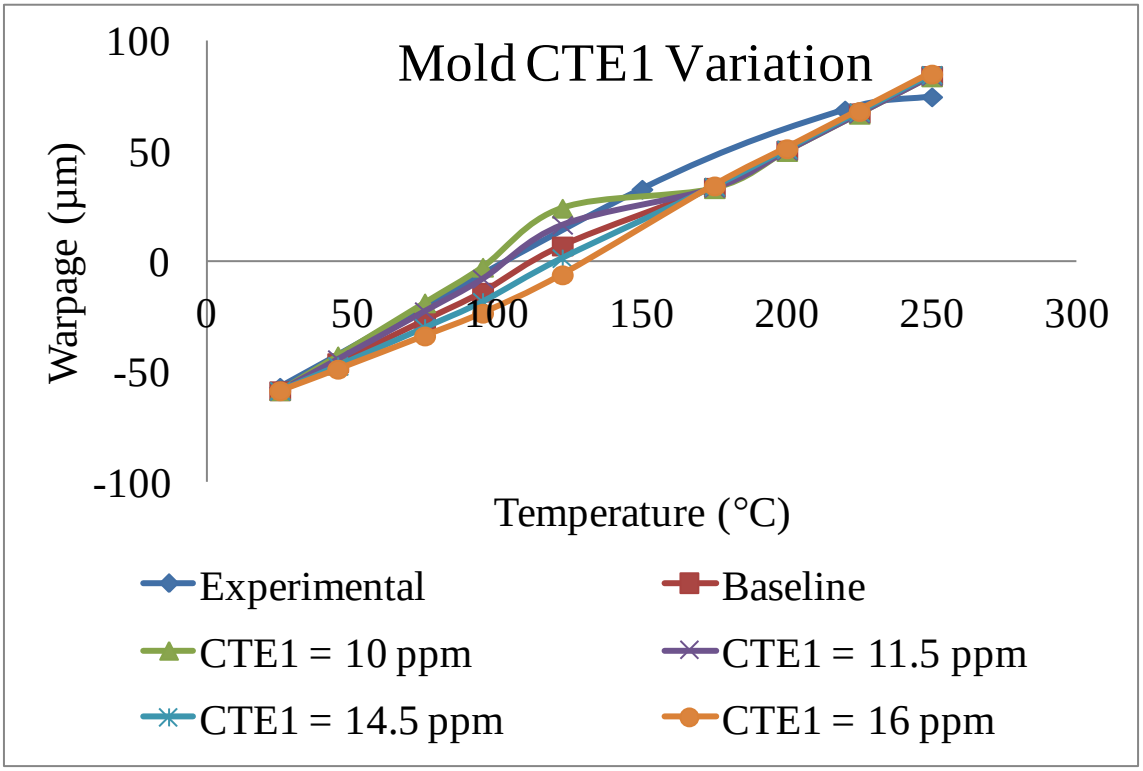


Figure 4-24: Warpage for mold CTE1 variation

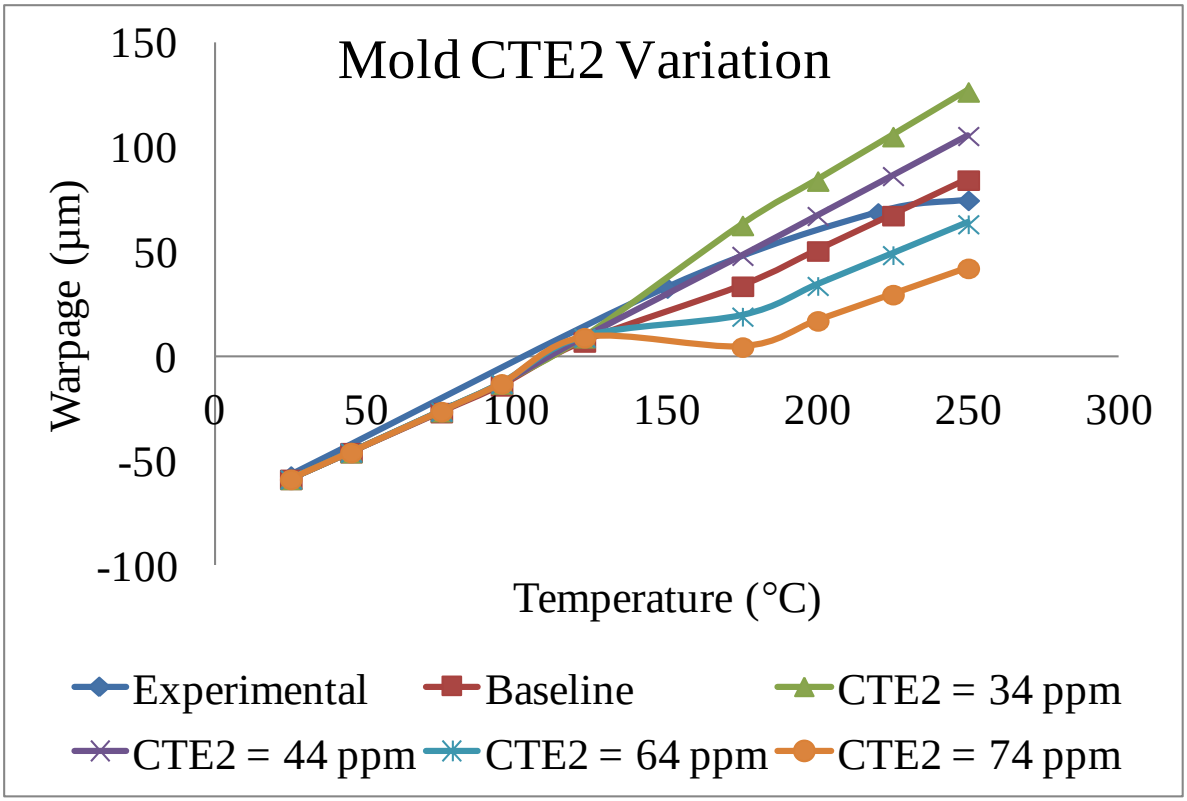


Figure 4-25: Warpage for mold CTE2 variation

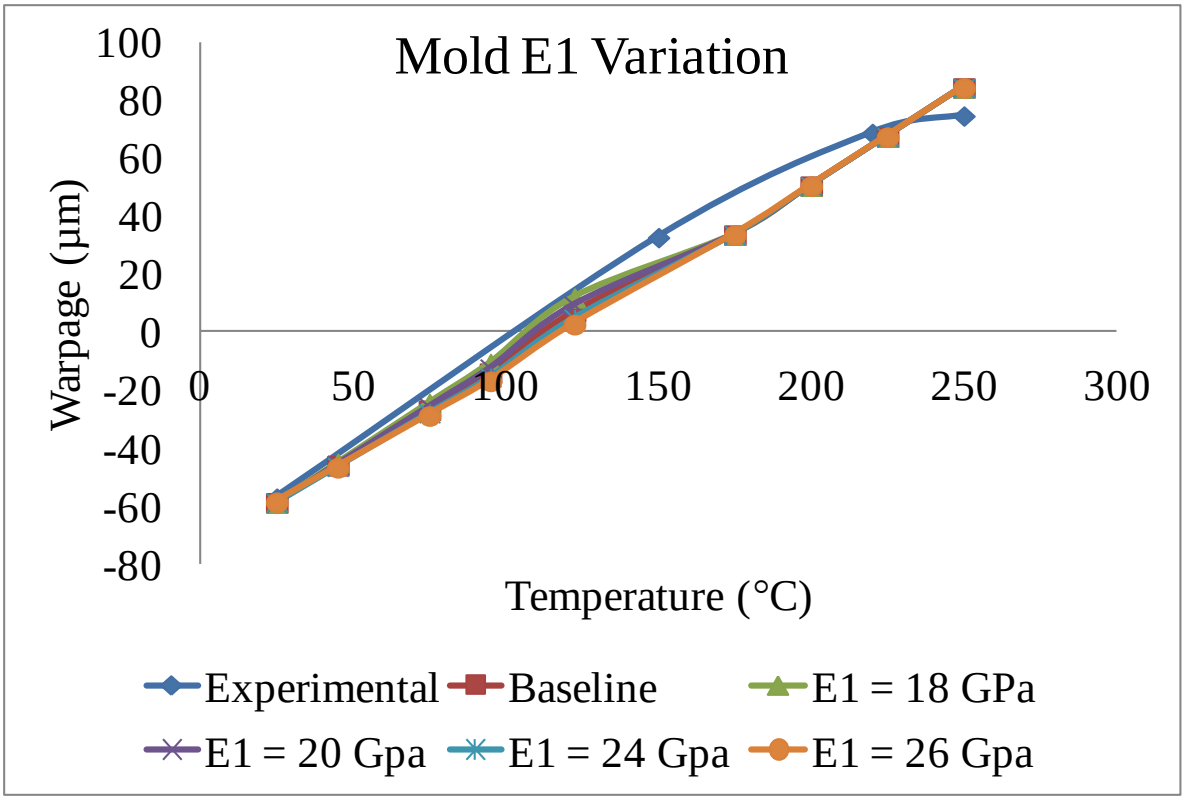


Figure 4-26: Warpage for mold E1 variation

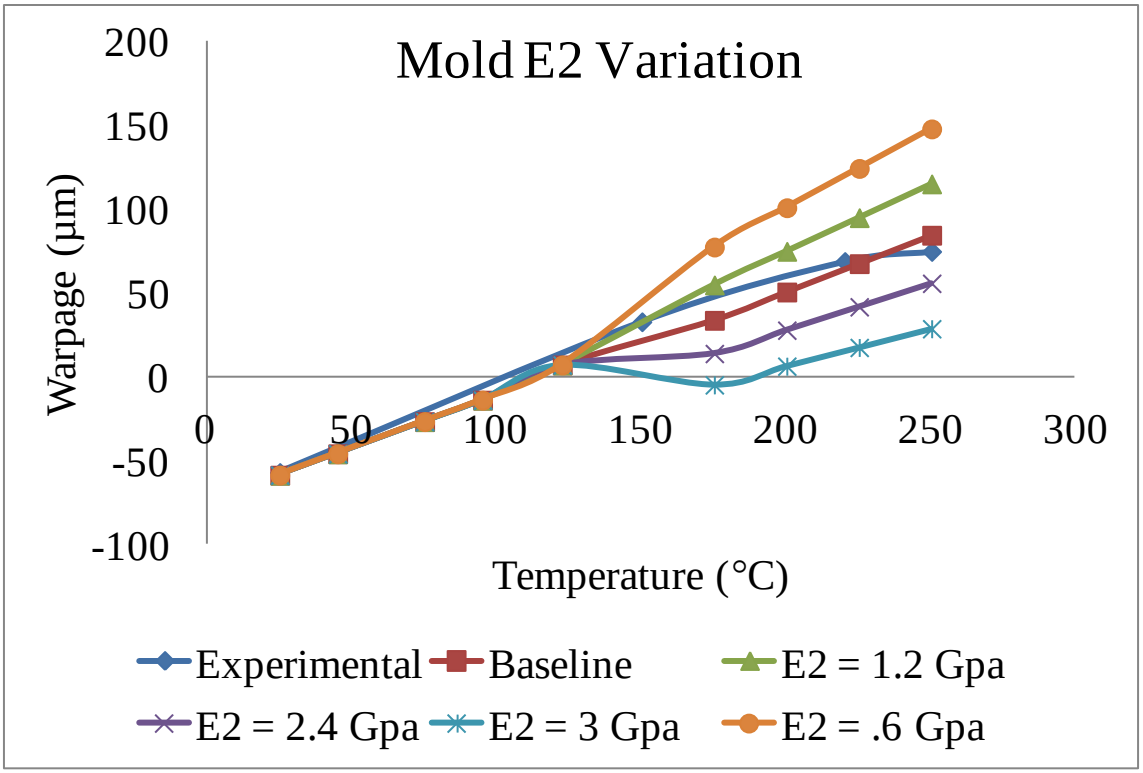


Figure 4-27: Warpage for mold E2 variation

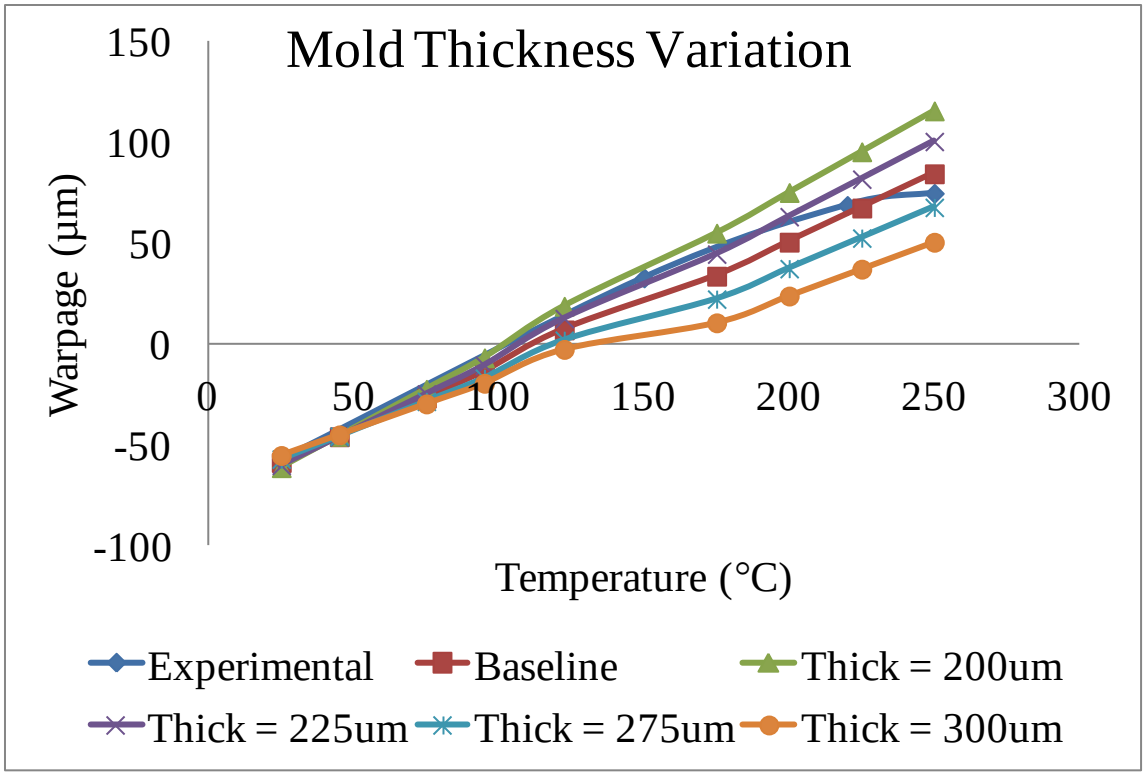


Figure 4-28: Warpage for mold thickness variation

4.6 Warpage Sensitivity Analysis

A sensitivity analysis of warpage for the PoP package is performed. The analysis is performed by using the baseline finite element model results has a reference point. Figure 4-29 is a plot showing the warpage values for each material property at a temperature below the glass transition temperature. The reported warpage values occur at the temperature of 75°C. The red dashed line in the figure indicates the warpage value of the baseline model. Warpage values which are near the dashed line indicate that the variance of that material property value in particular is not influential. Warpage values that are either larger or smaller than the baseline value indicate that the material property in particular has an influence on warpage below the glass transition temperature. To

better illustrate this point, a sensitivity plot is shown in Figure 4-30. This figure shows the percent change each material property variation has from the baseline warpage value. The percent change is calculated by subtracting the baseline warpage value from the varied warpage value and dividing that value by the baseline value. The sensitivity plot shows that the coefficient of thermal expansion of the epoxy molding compound below the glass transition temperature has a very large effect on package warpage. The EMC thickness and die thickness are also very influential to package warpage below the glass transition temperature.

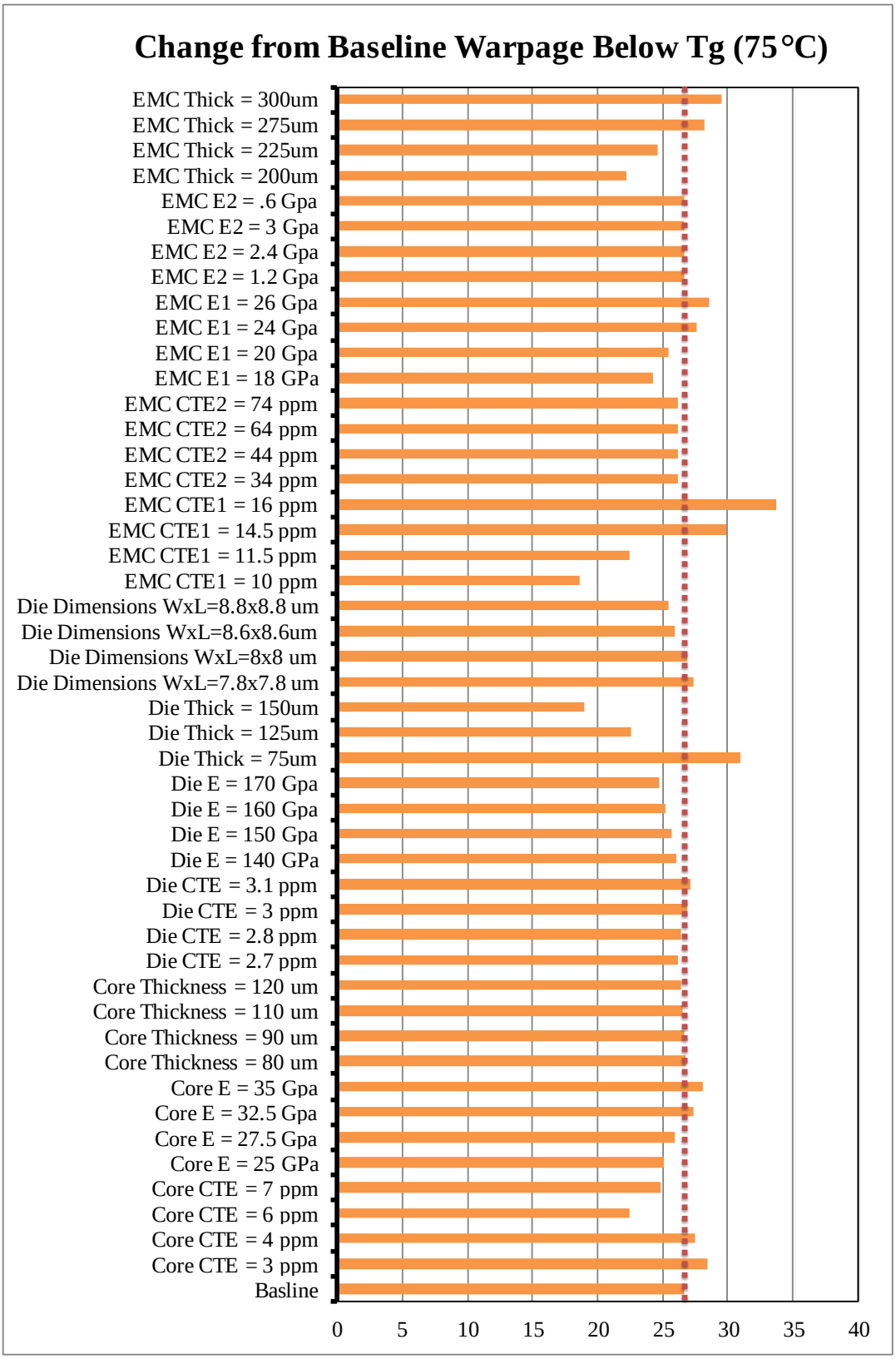


Figure 4-29: Warpage comparison below T_g

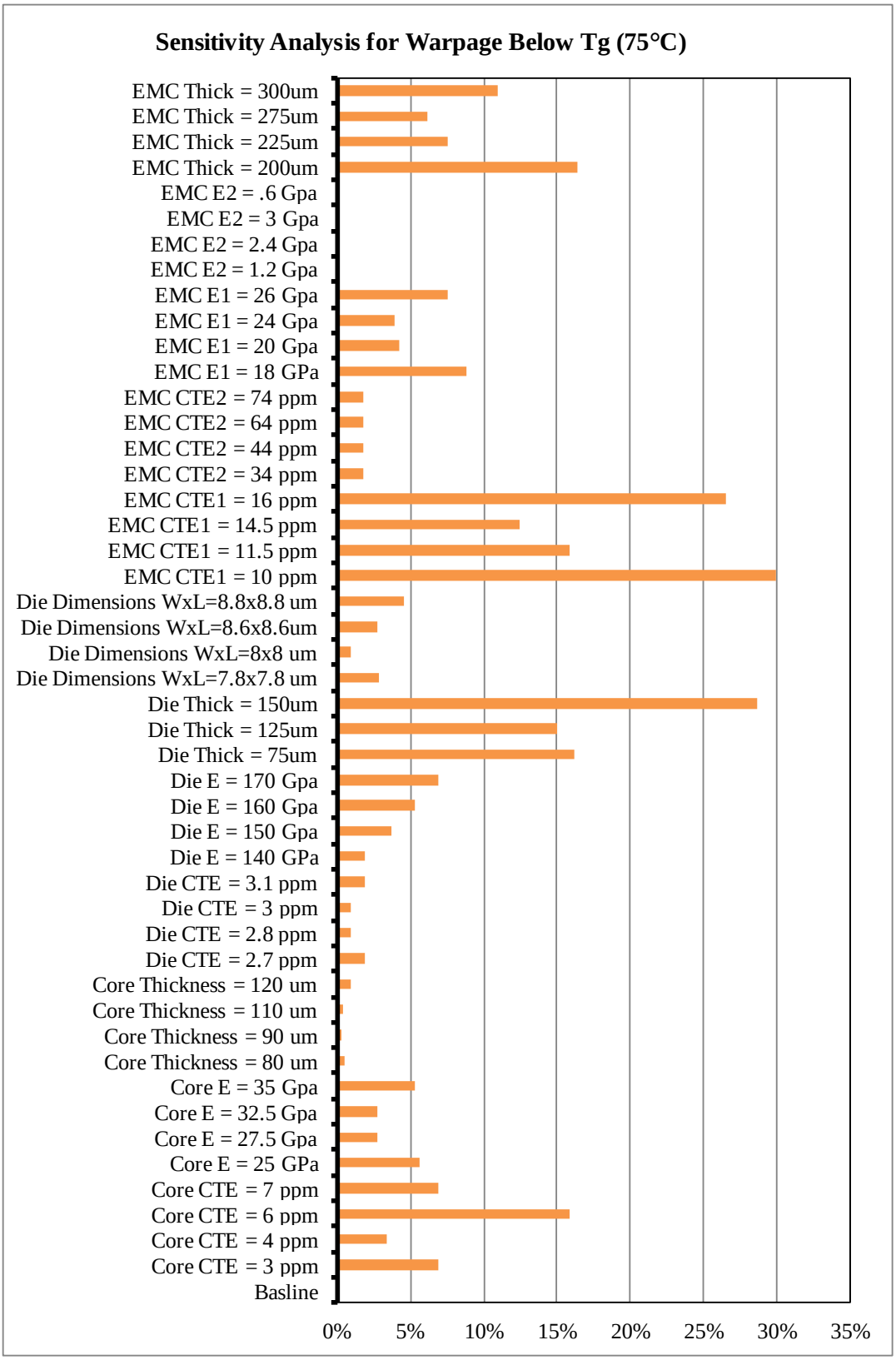


Figure 4-30: Sensitivity analysis: percent change from baseline warpage below T_g

A similar approach has been used to analyze the sensitivity of material properties and package dimensions above the glass transition temperature. Figure 4-31 is a plot showing the warpage values for each material property at a temperature above the glass transition temperature. The reported warpage values occur at the temperature of 250°C. Similar to the plots shown for the warpage values below the glass transition temperature, the red dashed line in the figure indicates the warpage value of the baseline model. Warpage values which are near the dashed line indicate that the variance of that material property value in particular is not influential. Warpage values that are either larger or smaller than the baseline value indicate that the material property in particular has an influence on warpage below the glass transition temperature. To better illustrate this point, a sensitivity plot is shown in Figure 4-32. From the sensitivity plot, it can be seen that elastic modulus of the epoxy molding compound above the glass transition temperature has a very large effect on package warpage. The EMC thickness, die thickness, and EMC CTE2 are also large contributors to package warpage above the glass transition temperature.

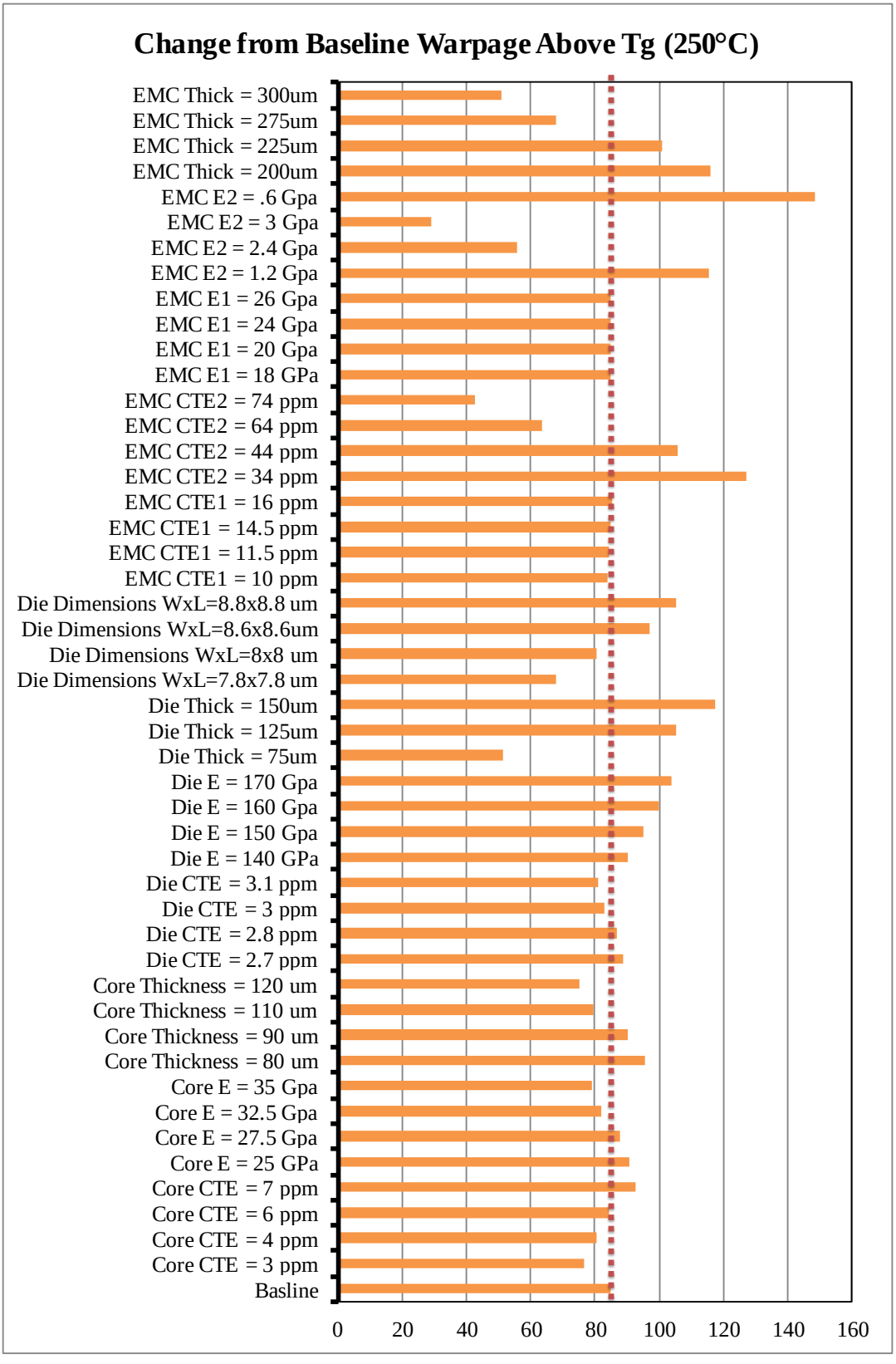


Figure 4-31: Warpage comparison above T_g

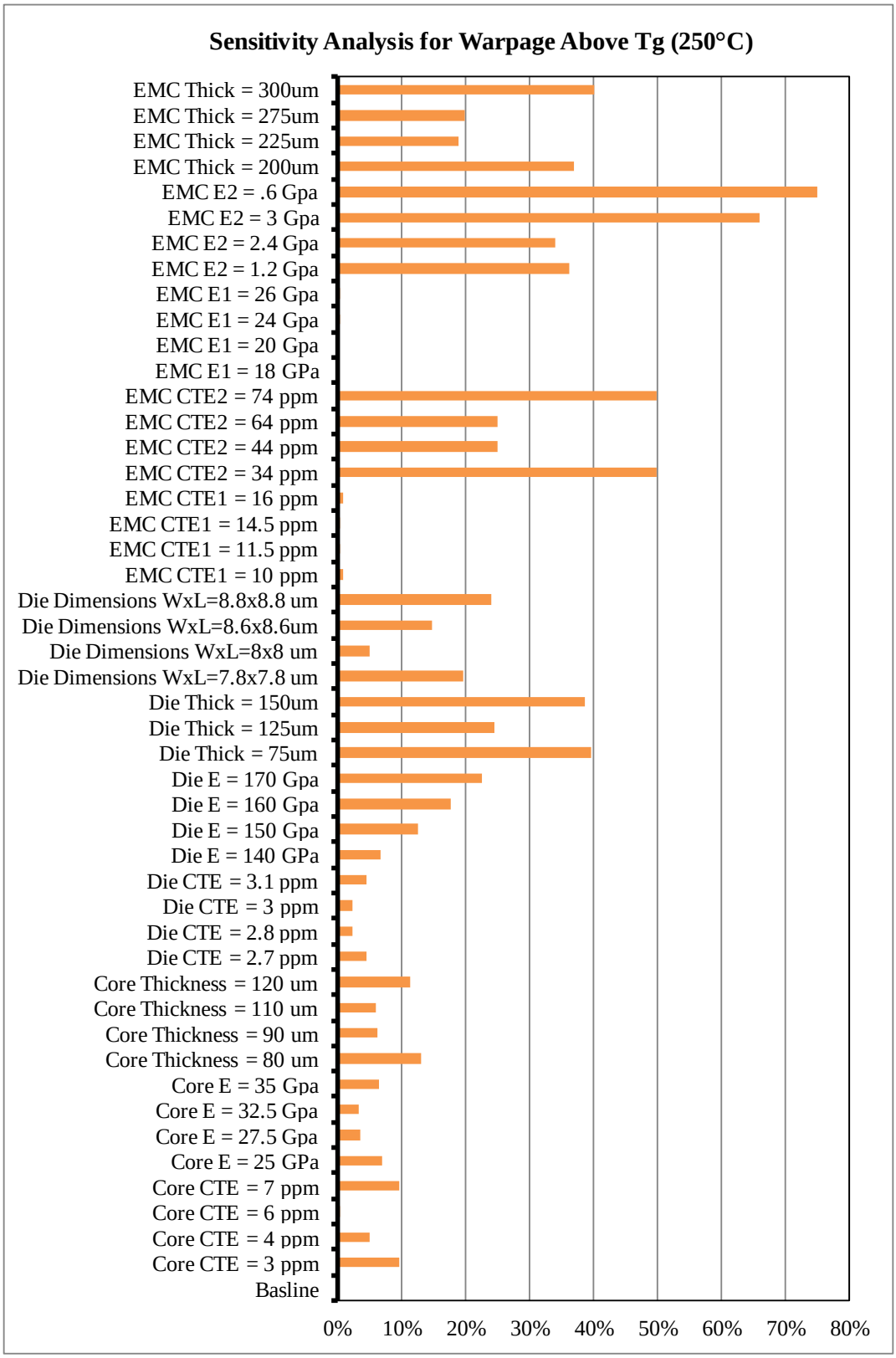


Figure 4-32: Sensitivity analysis: percent change from baseline warpage above T_g

To better analyze the effects of each material property above and below the glass transition temperature, a sensitivity plot containing warpage results from above the glass transition temperature and below the glass transition temperature is shown in Figure 4-33. The figure shows that certain material properties play a larger role in package warpage than others. The epoxy molding compound material properties and dimensional properties have the greatest influence on package warpage both above and below the glass transition temperature. The coefficient of thermal expansion of the silicon die has the least effect on package warpage. This is largely due to the fact that thermal properties of silicon have very little variation. The effects of silicon die elastic modulus are greater although still very small. The silicon die dimensions are very influential to warpage above the glass transition temperature and the die thickness is influential to warpage both below and above the glass transition temperature. The effects of substrate core material properties on warpage are low. It should be noted that the material properties above and below the glass transition temperature mainly influence warpage at those temperatures. For example, the coefficient of thermal expansion of the epoxy molding compound below the glass transition temperature does not have a large influence on warpage of the package above the glass transition temperature. With that in mind, the glass transition temperature is shown to play a critical role in package warpage with respect to temperature.

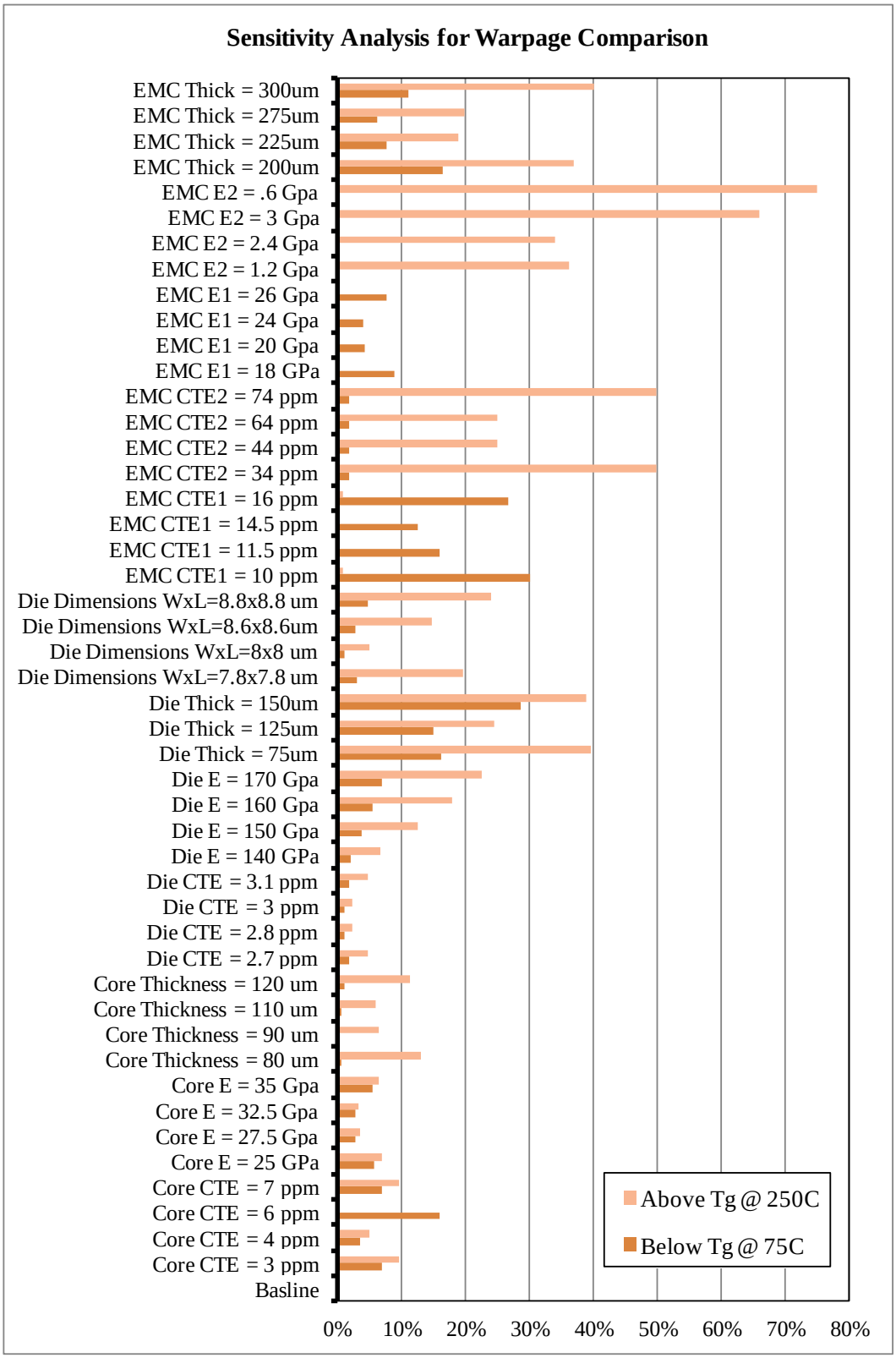


Figure 4-33: Sensitivity analysis for warpage comparison above and below Tg

5. Summary, Conclusions, and Future Work

The primary focus of this study has been to evaluate the reliability of second level interconnect devices subjected to various environmental conditions. The main motivation behind this study is to ensure that electronic systems subjected to these environmental effects during real-world applications are capable of survival. The conditions examined in this study include drop and thermal. This study also addressed the feasibility of using FE models in place of experimentation to examine test conditions which are either too costly to perform experimentally or simply too time consuming. Since such importance has been place on the finite element analysis section of this study, it is important to understand the risks and cautions one should expect and realize the various effects and variables that may cause error.

In Chapter 3, the effects of drop and shock tests on second level solder interconnects was shown. High-G drop tests were performed on a JEDEC form factor test board. A ceramic MCS grid array package was tested for shock survivability. The shock survivability of the MCS package was compared with a CCGA package. Benchmark tests were performed to determine the appropriate test levels. High speed cameras were used to observe board deflections. Reliability of the MCS in a 0° horizontal orientation was measured for three different test levels: 30,000g, 40,000g, and 50,000g. Reliability of the interconnects at the vertical orientation was also considered at three different test levels:

2000g, 2250g, and 2500g. The failure modes have been studied with optical microscopy. High speed cameras were used to capture and analyze board deflection during testing. Digital image correlation (DIC) was used to extract deformation contours. Finite element models were created using a global local modeling approach. Models showed good correlation with experimental strain and displacement. Detailed local models showed good correlation with observed failure modes.

Possible future work with this study would be to examine the effects an intermediate orientation such as a 45° orientation on the reliability of the micro-coil spring. This study revealed that the micro-coil spring is incredibly susceptible to failure at the 90° orientation but very robust compared to the CCGA at the horizontal orientation. It may also be interesting to investigate the effect of micro-coil manufacturing position on reliability. In the current configuration, there was no method made in placing the micro-coil spring array in an orientation that would optimize performance. Future work could involve creating a specimen in which the micro-coil spring is placed at a fixed rotational angle. It could be expected that the stress concentration location would change depending on how the springs are located. Lastly, a symmetrical loading condition in which the electronic package is placed at the center of the board could result in more consistent reliability performance. The current configuration creates asymmetric displacement loads since the package of interest is not directly at the center of the board.

In Chapter 4, a study investigating the warpage of a package on package (PoP) components was presented. Optical methods of measurements such as digital image correlation (DIC) and shadow moiré interferometery were used to measure the warpage

of the package in-situ during the test. The study investigated the effects of various process conditions and materials selections on warpage. In particular, the study aimed to determine the warpage during temperatures close to reflow temperature levels. The study presented a finite element analysis approach to investigating the effects of various parameters on warpage. The effects of material properties variation was shown including variation of the coefficient of thermal expansions and elastic modulus of the epoxy molding compound, the substrate core material, and the silicon die material. The coefficient of thermal expansion both below and above the glass transition temperature was investigated. The elastic modulus above and below the glass transition temperature was also investigated. The finite element models were also used to investigate the effects of package architecture on warpage. The study presented warpage variation with respect to mold thickness, die thickness, and die length and width. Lastly, a sensitivity analysis was performed to determine the influence of each parameter on warpage. The sentitivty analysis showed that the epoxy molding compound had a large influence on warpage values both above and below the glass transition temperature.

In the future, examination of the effects of different material properties and process conditions could be done experimentally rather than through the use of a finite element model. This would improve the real world accuracy since the finite element analysis requires some assumptions. In this study, only reflow temperatures are investigated. However, electronics may be exposed to temperatures much higher or lower than reflow cycles. It would be interesting to see how much warpage changes at extremely high and low temperatures on electronic assemblies.

Bibliography

Amagai, M., Yutaka S., A study of package warpage for package on package (PoP), Proceedings of 60th Electronic Components and Technology Conference, pp.226-233, June 2010.

Amodio, D., Broggiato, G., Campana, F., Newaz, G., Digital Speckle Correlation for Strain Measurement by Image Analysis, Experimental Mechanics, Vol. 43, No.4, pp. 396-402, 2003.

Bieler, T., Jiang, H., Influence of Sn Grain Size and Orientation on the Thermo mechanical Response and Reliability of Pb-free Solder Joints, Proceedings of the 56th ECTC, pp. 1462- 1471, May 2006.

Blackshear, E., Lombardi, T., Pompeo, F., Audet, J., Kim, K., Jeong, Y., Miyazawa, Y., Advanced laminate carrier module warpage considerations for 32nm pb-free, FC PBGA package design and assembly. Proceedings of the 61st Electronic Components and Technology Conference , pp. 523-529, 2011

Carson, F., Lee, S. M., Vijayaragavan, N., Controlling Top Package Warpage for POP Applications. Proceddings of 57th Electronic Components and Technology Conference, pp. 737-742, 2007

Cook, E.R., Jacoby, G.C. Jr., Tree-ring-drought relationships in the Hudson Valley, New York. Science, Vol. 198, pp.399-401, 1977.

Douglas, S., Meng, J., Akman, I., Yildiz, M., AI-Bassyiouni, A. Dasgupta, The Effect of Secondary Impacts on PWB-Ievel Drop Tests at High Impact Accelerations, Proceedings of 12th EuroSimE, pp. 1-6, 2011.

Draper, N.R. Smith, H., Applied regression analysis, 2nd edition, New York: John Wiley, and Sons. p709, 1981.

Fritts, H.C.; Blasing, T.J.; Hayden, B.P.; Kutzbach, J.E., Multivariate techniques for specifying tree-growth and climate relationships and for reconstructing

anomalies in paleoclimate, Journal of Applied Meteorology, Vol. 10, pp. 845-864, 1971.

Gunst, R.F.; Mason, R.L., Regression analysis and its application: a data-oriented approach, New York: Marcel Dekker, 402 p., 1980.

Gu, J., Lim, C. T., Tay, A. A. Y., Equivalent Solder Joint and Equivalent Layer Models for the Simulation of Solder Column Failure under Drop Impact, Proceedings of the 6th Electronic Packaging Technology Conference, pp. 547-552, 2004.

Gu, J., Lim, C. T., Tay, A. A. Y., Modeling of Solder Joint Failure due to PCB Bending during Drop Impact, Proceedings of the 6th Electronic Packaging Technology Conference, pp. 678-683, 2004

Gu J., Cooreman, S., Full-Field Optical Measurement For Material Parameter Identification With Inverse Methods, WIT Transactions on The Built Environment, Vol. 85, 2005.

Gu, J., Lim, C. T., Tay, A. A. Y., "Simulation of Mechanical Response of Solder Joints under Drop Impact Using Equivalent Layer Models", Proceedings of the 55th Electronic Components and Technology Conference, pp. 522-529, 2005.

Hong, B.Z., Ray, K. S., Ceramic Column Grid Array Technology with Coated Solder Columns. Proceedings of the 50th Electronic Components and Technology Conference 2000. pp. 1347-1353, May 2000

Irving, S., Liu, Y., Free Drop Test Simulation for Portable IC Package by Implicit Transient Dynamics FEM, Proceedings of the 54th ECTC, pp. 1062 - 1066, 2004.

JEDEC Standard JESD22-B111, Board Level Drop Test Method of Components for Handheld Electronic Products, July 2003.

JEDEC Standard. Package warpage measurement of surface-mount integrated circuits at elevated temperature. JESD22-B112A; October 2009.

Kehoe, L., Lynch, P., Guenebaut, V., Measurement of Deformation and Strain in First Level C4 Interconnect and Stacked Die using Optical Digital Image Correlation, Proceedings of the 56th ECTC, pp. 1874-1881, May 2006.

Lall, P., Panchagade, D., Liu, Y., Johnson, W., Suhling, J., Models for Reliability Prediction of Fine-Pitch BGAs and CSPs in Shock and Drop-Impact, Proceedings of the 54th ECTC, pp. 1296-1303,2004.

Lall, P., Panchagade, D., Choudhary, P., Suhling, J., Gupte, S., Failure Envelope Approach to Modeling Shock and Vibration Survivability of Electronic and MEMS Packaging, Proceedings of the 55th ECTC, pp. 480-490, 2005.

Lall, P., Choudhary, P., Gupte, S., Health Monitoring for Damage Initiation & Progression during Mechanical Shock in Electronic Assemblies, Proceedings of the 56th ECTC, San Diego, California, pp.85-94, May 30-June 2, 2006a.

Lall, P., Gupte, S., Choudhary, P., Suhling, J., Solder-Joint Reliability in Electronics Under Shock and Vibration using Explicit Finite-Element Sub-modeling, Proceedings of the 56th ECTC, pp. 428 - 435, 2006b.

Lall, P., Choudhary, P., Gupte, S., Suhling, J., Hofmeister, J., Statistical Pattern Recognition and Built-In Reliability Test for Feature Extraction and Health Monitoring of Electronics under Shock Loads, 57th Electronics Components and Technology Conference, Reno, Nevada, pp. 1161-1178, May 30-June 1, 2007a.

Lall, P., Gupte, S., Choudhary, P., Suhling, J., Solder-Joint Reliability in Electronics Under Shock and Vibration using Explicit Finite Element Sub-modeling, IEEE Transactions on Electronic Packaging Manufacturing, Volume 30, No.1, pp. 74-83, January 2007b.

Lall, P., Panchagade, D., Iyengar, D., Shantaram, S., Suhling, J., Schrier, H., High Speed Digital Image Correlation for Transient-Shock Reliability of Electronics, Proceedings of the 57th ECTC, Reno, Nevada, pp. 924-939, May 29 June 1, 2007c.

Lall, P. Panchagade, D., Liu, Y., Johnson, W., Suhling, J., Smeared Property Models for Shock-Impact Reliability of Area-Array Packages, ASME Journal of Electronic Packaging, Volume 129, pp. 373-381, December 2007d.

Lall, P., Hande, M., Bhat, C., Islam, N., Suhling, J., Lee, J., Feature Extraction and Damage-Precursors for Prognostication of Lead-Free Electronics, Microelectronics Reliability, Volume 47, pp. 1907-1920, December 2007e.

Lall, P., Shirgaokar, A., Drake, J., Moore, T., Suhling, J., Principal Component Regression Models for Life Prediction of PBGAs on Copper Core and No-Core Assemblies, iTHERM '08, Orlando, Florida, pp. 770-785, May 28-31, 2008.

Lall, P., Choudhary, P., Gupte, S., Suhling, J., Health Monitoring for Damage Initiation and Progression during Mechanical Shock in Electronic Assemblies, IEEE Transactions on Components and Packaging Technologies, Vol. 31, No.1, pp. 173-183, March 2008a.

Lall, P., Panchagade, D., Choudhary, P., Gupte, S., Suhling, J., Failure-Envelope Approach to Modeling Shock and Vibration Survivability of Electronic and MEMS Packaging, IEEE Transactions on Components and Packaging Technologies, Vol. 31, No.1, pp. 104-113, March 2008b.

Lall, P., Iyengar, D., Shantaram, S., S., Gupta, P., Panchagade, D., Suhling, J., KEYNOTE PRESENTATION: Feature Extraction and Health Monitoring using Image Correlation for survivability of Lead-free Packaging under Shock and Vibration, Proceedings of the 9th International Conference on Thermal, Mechanical, and Multi-Physics Simulation and Experiments in Micro-Electronics and Micro-Systems (EuroSlME), Freiburg, Germany, pp. 594-608, April 1618,2008c.

Lall, P., Iyengar, D., Shantaram, S., Pandher, R., Panchagade, D., Suhling, J., Design Envelopes and Optical Feature Extraction Techniques for Survivability of SnAg Lead-free Packaging Architectures under Shock and Vibration, Proceedings of the 58th Electronic Components and Technology Conference (ECTC), Orlando, Florida, pp. 1036-1047, May 27-30, 2008d.

Lall, P., Shirgaokar, A., Arunachalam, D, Principal Component Analysis Based Development of Norris-Landzberg Acceleration Factors and Goldmann Constants for Leadfree Electronics, Proceedings of the 58th Electronic Components and Technology Conference, May 2009

Lim, P.M., K. T., Seah, S. K. W., Tackling the Drop Impact Reliability of Electronic Packaging, ASME InterPAK, Maui, pp. 1 - 9, July 2003

Lin, W. Lee M.W., PoP/CSP warpage evaluation and viscoelastic modeling, 58th Electronics Components and Technology Conference, pp.1576-1581, 27-30 May 2008

Luan, J., Tee, T. Y., Novel Board Level Drop Test Simulation using Implicit Transient Analysis with Input-G Method, Proceedings of the 6th Electronic Packaging Technology Conference, pp. 671-677, 2004.

Luan, J., Tee, T., Effect of Impact Pulse Parameters on Consistency of Board Level Drop Test and Dynamic Responses, Electronic Components and Technology Conference, pp. 665-673, 2005.

Luan, J., Goh, K., Baraton, X., A Novel Methodology for Virtual Qualification of IC Packages under Board Level Drop Test, Electronic Component and Technology Conference, pp-1212-1217, 2008

Mansfield, E.R. Webster, J.T.; Gunst, R.F., An analytic variable selection technique for principal components regression, Applied Statistics. Vol. 6, pp. 34-40, 1977.

Massey, W., Principal component regression in exploratory statistical research, Journal of the American Statistical Association, 60, pp.234-246, 1965.

Meng, J., Mattila, T., Dasgupta, A., Sillanpaa, M., Jaakkola, R., Luo, G., Andersson, K., Drop qualification of MEMS components in handheld electronics at extremely high accelerations., Thermal and Thermomechanical Phenomena in Electronic Systems, pp. 1020-1027, May 2012

Miller, T., Schreier, H., Reu, P, High-speed DIC Data Analysis from a Shaking Camera System, Proceedings of the SEM Conference, Springfield, Massachusetts, June 2007.

Park, S., Reichman, A., Kwak, J., Chung, S., Whole Field Analysis of Polymer Film, Proceedings of the SEM Conference, Springfield, Massachusetts, June 4-6, 2007b. 554 2009 Electronic Components and Technology Conference

Park, S., Shah, C., Kwak, J., Jang, C., Pitarresi, J., Transient Dynamic Simulation and Full-Field Test Validation for A Slim-PCB of Mobile Phone under Drop Impact, Proceedings of the 57th ECTC, Reno, Nevada, pp. 914923, May 29 - June 1, 2007a.

Park, S., Al-Yafawi, A., Yu, D., Kwak, J., Lee, J., Goo, N., Influence of Fastening Methods on the Dynamic Response and Reliability Assessment of PCBS in Cellular Phones Under Free Drop, Proceedings of the ITherm, Intersociety Conference on Thermal and Thermo-mechanical Phenomena, Orlando, Florida, pp.876-882, May 28-31, 2008.

Peterson, D., Cheng, C., Karulkar, P.C., Characterization of Drop Impact Survivability of a 3D-CSP Stack Module, Proceedings of the 58th Electronic Component and Technology Conference, Orlando, Florida, pp. 1648-1653, May 27-30, 2008.

Pitaressi, J., Roggeman, B., Chaparala, S., Mechanical Shock Testing and Modeling of PC Motherboards, 54th Electronics Components and Technology Conference, pp. 1047 - 1054, 2004.

Rajendra, Pendse, D., Zhou, P., Methodology For Predicting Solder Joint Reliability In Semiconductor Packages, Microelectronics Reliability, Vol. 42, pp. 301-305,2002.

Strickland, S.M, Hester J.D, Gowan A.K, Montgomery R.K, Geist D.L., Micro coil Spring Interconnects for Ceramic Grid Array Integrated Circuits, 2011

Scheijgrond, P.L.W., Shi, D.X.Q., Driel, W.D.V., Zhang, G.Q., Nijmeijer H., Digital Image Correlation for Analyzing Portable Electronic Products during Drop Impact Tests, 6th International Conference on Electronic Packaging Technology, pp. 121 - 126, 2005.

Shetty, S., Reinikainen, T., Three- and four-point bend testing for electronic packages. Journal of Electronic Packaging, pp. 556-561, 2003.

Srinivasan, V., Radhakrishnan, S., Zhang, X., Subbarayan, G., Baughn, T., Nguyen, L., High Resolution Characterization of Materials Used In Packages through Digital Image Correlation, ASME InterPACK, July 1722, 2005.

Sun, Y., Pang, J., Shi, X., Tew, J., Thermal Deformation Measurement by Digital Image Correlation Method, Proceedings of ITherm Conference, pp. 921-927, May 2006.

Sun, P., Leung, V. K., Xie, B., Ma, V. W., Shi, D. Q., Warpage reduction of package-on-package (PoP) module by material selection & process optimization. In Electronic Packaging Technology & High Density Packaging, 2008

Tee, T. Y., Luan, J., Pek, E., Lim, C. T., Zhing, Z., Advanced Experimental and Simulation Techniques for Analysis of Dynamic Responses during Drop Impact, Electronic Components and Technology Conference, Las Vegas, Nevada, pp. 1088-1094, June 1-4, 2004.

Tee, T. Y., Ng, H. S., Lim, C.T., Pek, E., Drop Impact and Impact Life Prediction Model for QFN Packages, Journal of SMT, Volume 16, Issue 3, pp. 31-39, 2003.

Tee, T. Y. , Hun Shen Ng, Chwee Teck Lim, Eric Pek , Zhaowei Zhong , Board Level Drop Test and Simulation of TFBGA Packages for Telecommunication Applications, Proceedings of the 53rd ECTC, pp. 121-129, 2003.

Tzeng, Y. L., Kao, N., Chen, E., Lai, J. Y., Wang, Y. P., Hsiao, C. S., Warpage and stress characteristic analyses on package-on-package (POP) structure. Proceedings of 9th Electronics Packaging Technology Conference, pp. 482-487, December 2007

Wang, Y. Y., Wang, F., & Chai, T. C. (2004, December). Finite element modeling of CSP package subjected to board level drop test. In Electronics Packaging Technology Conference, 2004. EPTC 2004. Proceedings of 6th (pp. 684-688).

Wong, E. H., Lim, C. T., Field, J. E., Tan, V. B. C., Shim, V. P. M., Lim, K. T., Seah, S. K. W., Tackling the Drop Impact Reliability of Electronic Packaging, ASME InterPAK, July 6 -11, Maui, pp. 1 - 9,2003.

Wu, J., Global and Local Coupling Analysis for Small Components in Drop Simulation, 6th International LSDYNA Users Conference, pp. 11:17 - 11:26, 2000.

Wu, J., Song, G., Yeh, C., Wyatt, K., Drop Impact Simulation and Test Validation of Telecommunication Products, InterSociety Conference on Thermal Phenomena, pp. 330- 336, 1998.

Xie, D., Minna A., Dongkai S., Hoang P., Geiger, D., Sammy Y., Life Prediction of Lead free Solder Joints for Handheld Products, Telecom Hardware Solutions Conference, Plano, Texas, USA, May 15-16, 2002.

Xie, D., Minna Arra., Yi, S., Rooney, D., Solder Joint Behavior of Area Array Packages in Board-Level Drop for Handheld Devices, Proceedings of the 53rd ECTC, pp.130-135,2003

Xu, L., Pang, H., Combined Thermal and Electromigration Exposure Effect on SnAgCu BGA Solder Joint Reliability, Proceedings of the 56th ECTC, pp. 1154-1159, May 2006.

Yen, F., Chen, E., Lai J.Y., Wang Y.P., The Introduction of Warpage Improvement Guidelines for BGA's Performance within SMT Temperature Profile, Microsystems, Packaging, Assembly & Circuits Technology Conference, pp.278-282, October 2008.

Yogel, D., Grosser, V., Schubert, A., Michel, B., MicroDAC Strain Measurement for Electronics Packaging Structures, Optics and Lasers in Engineering, Vol. 36, pp. 195-211,200l.

Zhao, J., Liu, F., Zhou, X., Zhou, H., Jing, J., Zhao, M., Improvement of JEDEC Drop Test in SJR Qualification through Alternative Test Board Design, Electronic Components and Technology Conference, pp. 946-950, 2007.

Zhang, Y., Shi, X., Zhou, W., Effect of Hygrothermal Aging on Interfacial Reliability of Flip Chip on Board (FCOB) Assembly, Electronic Packaging Technology Conference, pp. 404-409, 2004.

Zhang, F., Li, M., Xiong, C., Fang, F., Yi, S., Thermal Deformation Analysis of BGA Package by Digital Image Correlation Technique, Microelectronics International, Vol. 22, No.1, pp. 34-42,2005.

Zhang, Y., Cai, Z., Suhling, J., Lall, P., Bozack, M., The Effect of Aging Temperature on SAC Solder Joint Material Behavior and Reliability, Electronic Component and Technology Conference, pp99-112, 2008.

Zhou, P., Goodson, K. E., Sub-pixel Displacement and Deformation Gradient Measurement Using Digital Image- Speckle Correlation (DISC), Optical Engineering, Vol. 40, No.8, pp 1613-1620, August 200l.

Zhu, L., Submodeling Technique for BGA Reliability Analysis of CSP Packaging Subjected to an Impact Loading, InterPACK Conference Proceedings, 2001.

Zhu, L., Marccinkiewicz, W., Drop Impact Reliability Analysis of CSP Packages at Board and Product System Levels Through Modeling Approaches, Proceedings of the ITherm Conference, pp. 296 - 303, 2004.

Zhu, L., Modeling Technique for Reliability Assessment of Portable Electronic Product Subjected to Drop Impact Loads, Proceedings of the 53rd ECTC, pp. 100-104, 2003.