Through Silicon Vias Using Liquid Metal Conductors for Reworkable Electronics

by

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Abstract

The design and fabrication of liquid metal interconnects (vias) for reworkable 2.5D device integration is presented in this work. We discuss the implementation of a fully reworkable test module and a partially reworkable module using Asahi glass AL-X as bonding adhesive. The liquid metal under study is eutectic gallium indium (78.6% Gallium, 21.4% Indium) alloy with a melting temperature of approximately 15.7 °C. The liquid metal is subsequently used to fill a silicon interposer with 200 μm pitch hollow vias. Electrical contact is made to the liquid metal vias through the top and bottom with complementary daisy-chain metallization that provide insight into electrical shorts and opens. This liquid metal interconnect technology can be integrated with existing interposer technologies, including capacitors and traditional (solid metal) through-silicon vias (TSVs) as a via last process.

DC and RF simulations are also presented to determine the performance of the liquid metal vias. Preliminary DC measurements under varying temperature were also performed which indicate the lowest operating temperature to be -13.15 °C before electrical contact is lost. The highest temperature tested was 80 °C with no apparent mechanical failures. The resistance of a transition with two liquid metal vias was determined to be 0.37 mΩ at room temperature.

Acknowledgments

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Chapter 1

Introduction

Liquid metals such as mercury have traditionally been used for non-destructive and rapid electrical characterization of semiconductor devices [11–13]. Other applications of mercury have been explored by researchers, such as electrostatic [14, 15] and pneumatic activated switches [16], but the use of mercury in electronics has been limited due to toxicity concerns. Meanwhile, eutectic alloys of gallium are less toxic, exhibit higher conductivity ($\sigma = 3.4 \times 10^4$ S/cm) [17] when compared to mercury ($\sigma = 1.041 \times 10^4$ S/cm) [9] and are also present in the liquid phase at room temperature. Applications of eutectic gallium indium (EGaIn) include flexible electronics [5, 6, 8] and RF devices such as a microstrip resonator [18] and a tunable metamaterial filter [19].

Research in addressing reworkability in Integrated Circuit (IC) packaging has been investigated by a few research groups [1, 20, 21]. For example, Palo Alto Research Center (PARC) has studied spring-based interconnects [20] that accommodate thermal stresses and provide reworkability by being rematable and easy to disassemble. A more conventional approach to reworkable interconnects with high pin count (> 1000) was undertaken by Aggarwal, et al., with what they term as nano-interconnects [21]. Their interconnect structure consist of tin copper (Sn-Cu) with a pitch of 50 μm that are 25 μm wide and 20 μm tall. Although this research group does not provide electrical performance or reworkability information.

These technologies offer an improvement in thermal stresses, reworkability, and demonstrate high interconnect density. Complementary to the aforementioned reworkable interconnects, liquid metal conductors are an alternative reworkable device integration technology that can also accommodate thermal stresses and provide high interconnect density.

Our research efforts are focused on using EGaIn as a non-solid (at room temperature) interconnect in interposer technology that permits complete replacement of the connected modules in case of failure or upgrade. These liquid metal vias are compatible with silicon and glass based interposers with no inherent limitation on via pitch or diameter. Liquid metal vias can also be integrated with existing interposer technologies, such as capacitors, and traditional (solid metal) vias. A benefit of using a non-solid via is that it can accommodate thermal stresses induced by the substrate. The sole requirement for liquid metal via formation is such that the liquid metal should be able to adhere to the surface of the via trench.

In our research, we quantify the electrical performance of our liquid metal through silicon vias (TSVs) by simulation and measurement. Our measurements consist of two-point probe direct current (DC) measurements. We are able to perform failure analysis on snake and comb structures to determine electrical opens and shorts. These structures also provide estimates on via yield and provide insight to possible failure mechanisms. A top view representation of the snake and comb structure used in our device testing is shown in Fig.1.1. The through lines allow us to measure a varying number of vias. Meanwhile, the open line allows us to determine whether there is isolation between contact chains.

Our test modules consist of a silicon interposer with 2500 liquid metal TSVs. Electrical contact is made to the liquid metal from both the top and bottom by a daisy-chain metallization that complement each other. Two distinct designs were studied in this work. A completely reworkable module that consists of an array of 75 μm tall with a 200 μm pitch gold coated pads, in which the top and bottom die assemblies can be removed. In the half-reworkable module, the bottom and top pads are 5 μm and 75 μm tall pads respectively. The pin diameter for the top pads is 50 μm and the bottom pad diameter is 150 μm in both modules. In the half-reworkable module, the interposer die is bonded to the bottom die with Asahi glass AL-X 2010 low-k dielectric. Schematic cross-sections of the fully reworkable module and half reworkable module assembly are shown in Fig.1.2a-1.2b.

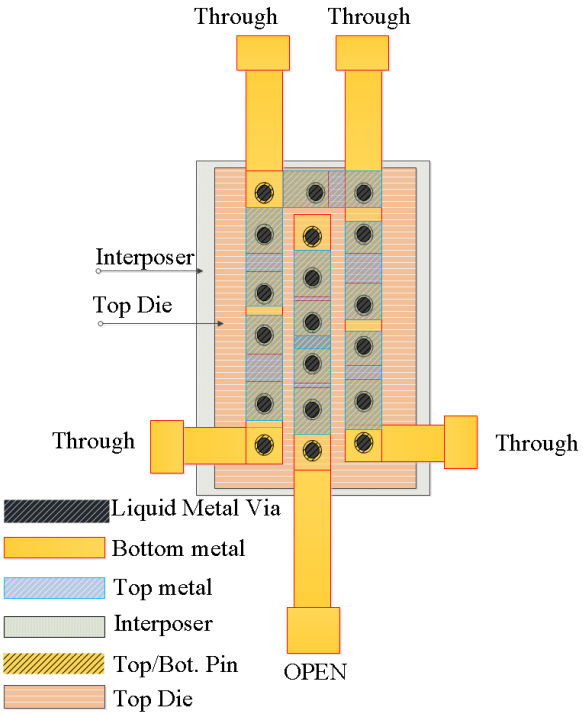
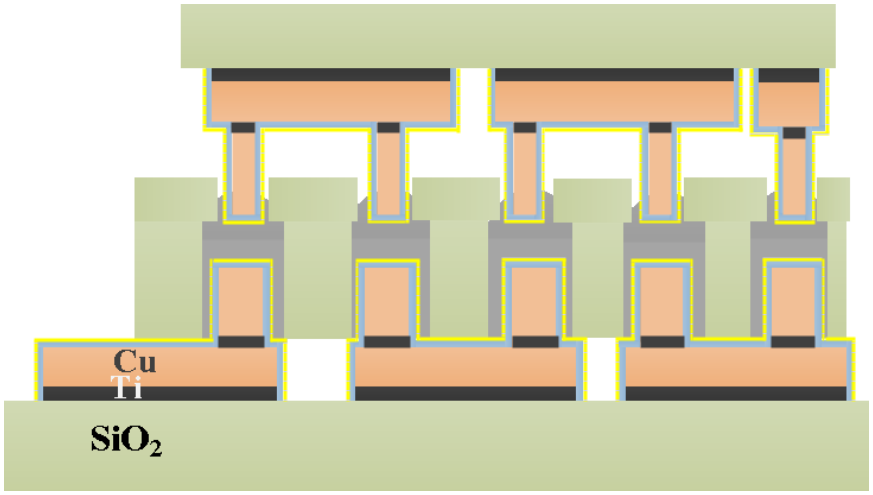
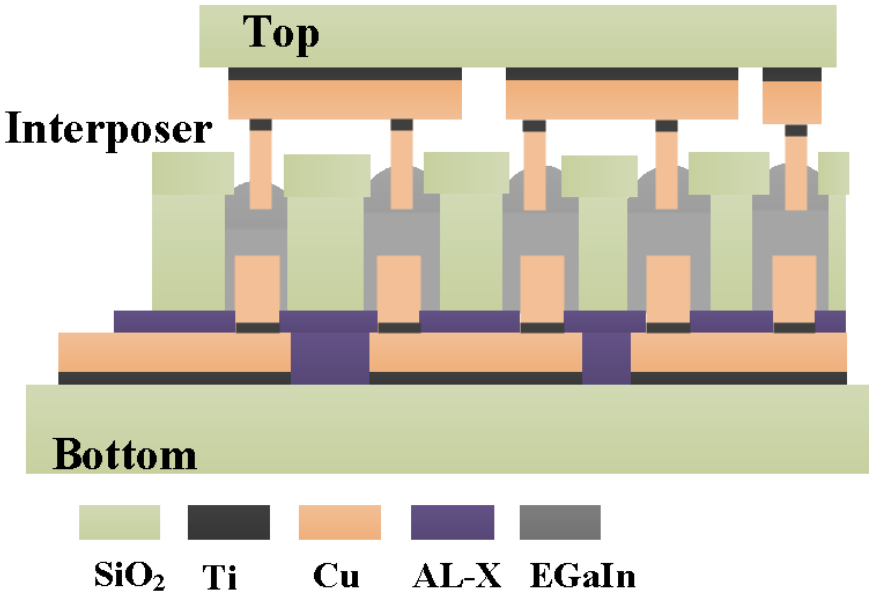


Figure 1.1: Schematic top view of snake and comb structure used in measuring electrical opens and shorts.

In the following sections we describe in greater detail the fabrication of the reworkable liquid metal via technology, the electrical performance after rework and the electrical performance at temperature range from -13.15 °C to 80 °C with modest changes in resistance.



(a)



(b)

Figure 1.2: Schematic cross section of liquid metal filled vias in an interposer die. (a) Completely reworkable module and (b) Half-reworkable module.

1.1 Literature Review

In this section we discuss reworkable interconnect technology and applications of liquid metal. To the best of our knowledge, this work is the first to implement EGaIn as a non-solid interconnect (via) for reworkable 2.5D integration. The predominate applications for EGaIn are found to be in flexible substrate technologies involving PDMS. In contrast, reworkable interconnects have been primarily implemented on rigid substrates with unique metallurgy and geometric designs.

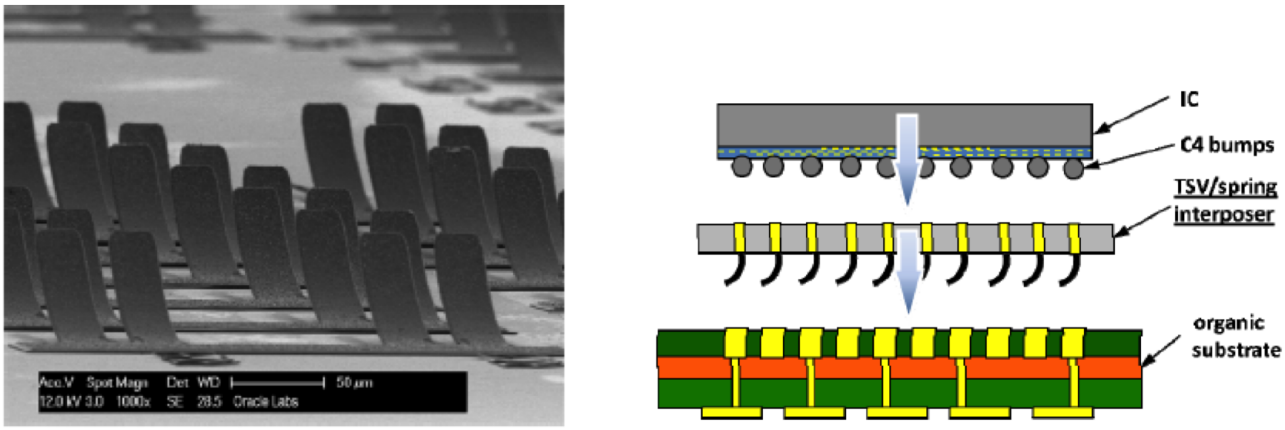
1.1.1 Reworkable Interconnects

Device reworkability becomes more important as device complexity and technological advancements lead to a higher cost of ownership. In the case of chip upgrade or failure, few solutions currently exist. Significant strides have been made by some research groups in this area.

One such example dates to 1996 and has continually been improved on [1, 20, 22–24], is a novel spring-based interconnect consisting of Molybdenum Chromium (MoCr) alloy with a ratio of $Mo_{0.08}Cr_{0.2}$ that is coated with gold to improve the conductivity of the spring. The springs are 100 μm long and 30 μm wide with a thickness of 3.5 μm and a height of 45 μm above the surface [1]. Due to a stress gradient in the metal alloy, the springs show 30 μm of z-compliance. The resistance for an individual interconnect is between 70-100 mΩ [24]. This technology has been demonstrated on organic, ceramic, and silicon substrates. Spring-based interconnects implemented on a silicon interposer is shown in Fig.1.3. Reworkability was demonstrated on a silicon substrate with up to 10 mating cycles with resistance changes not varying more than 5% [20].

1.1.2 Z-Compliant Interconnects

Similar implementations to PARC's spring-based interconnects have been studied by other researchers that provide a z-compliance with the potential to provide reworkability. The



(a) (b)

Figure 1.3: Palo Alto Research Center spring-based interconnects. (a) SEM of MoCr springs and (b) schematic of springs integrated on an interposer [1].

different technologies all define their own terminology to describe their interconnect, such as G-Helix [2], Mechanically Flexible Interconnects (MFI) [3], and FlexConnects [4], which are a 2nd generation version of the G-Helix. The goal of these different interconnect structures is to provide mechanical robustness and low impedance connectivity. For comparison, each technology is summarized in Table 1.1. To illustrate the difference in design, schematics are shown in Fig.1.4.

Interconnect Technology	Resistance	Mechanical Compliance
PARC Springs	70-100 mΩ [24]	No mention
g-Helix	43.63 mΩ [2]	10.149 mm/Newton [2]
MFI	No Mention	25 mm/Newton (Max) [3]
FlexConnects	50 mΩ [4]	6.47 mm/Newton [4]

Table 1.1: Z-Compliant Interconnect Comparison

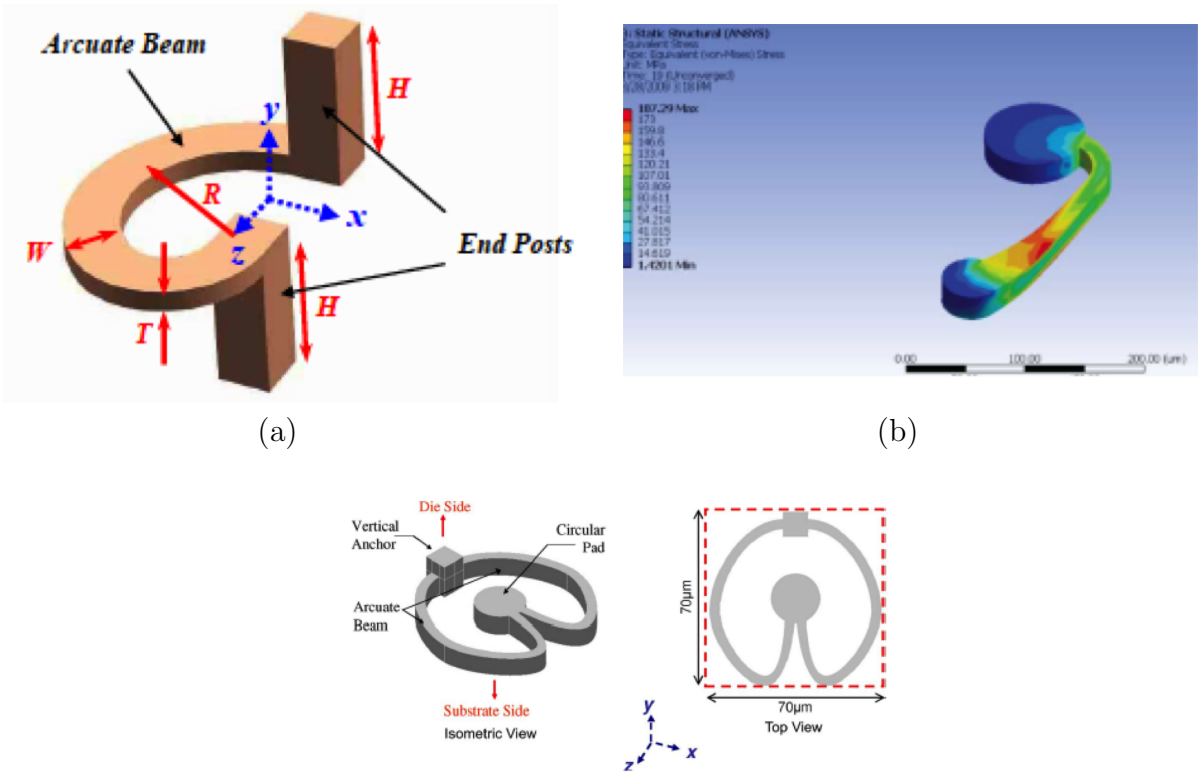
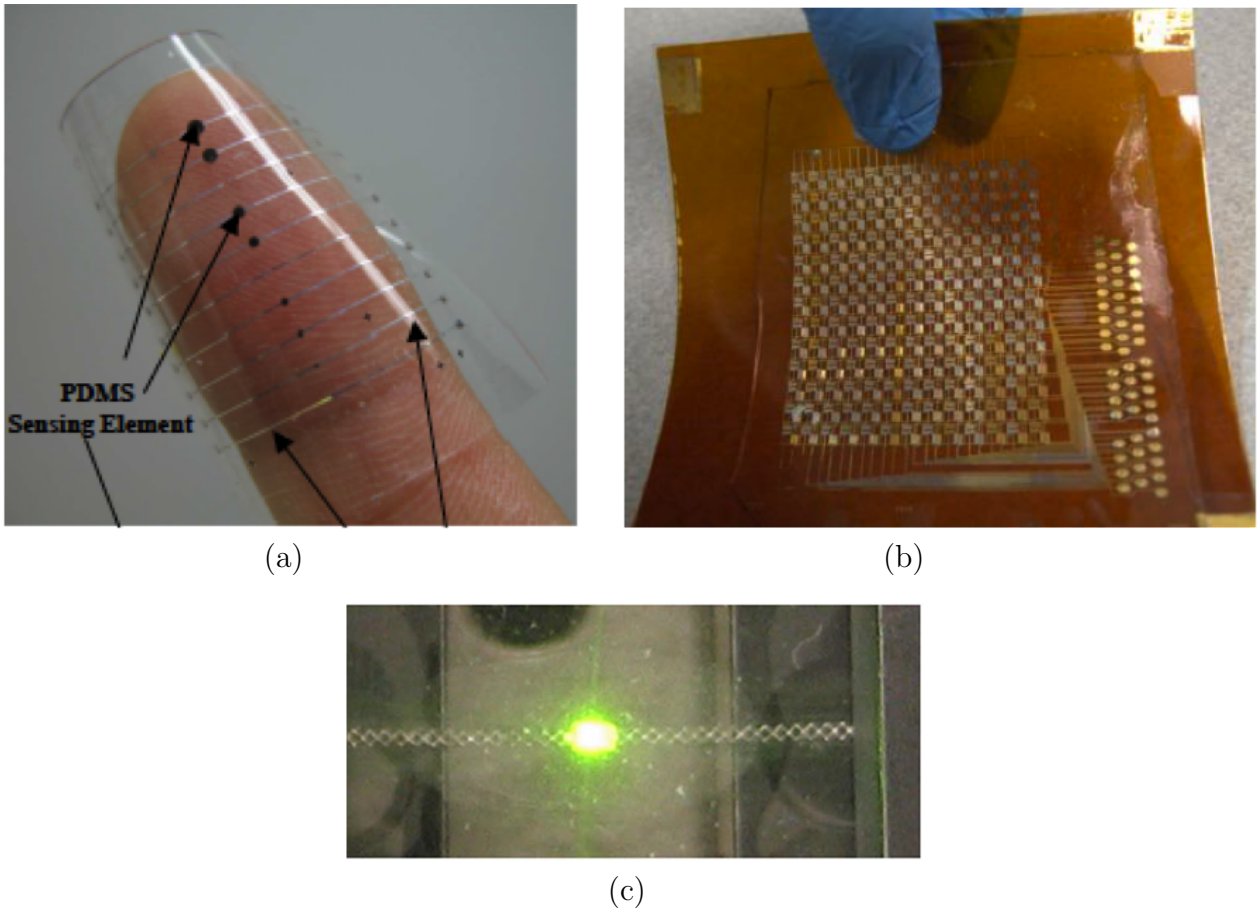


Figure 1.4: Summary of different interconnect structures (a) g-Helix [2], (b) MFI [3], and (c) FlexConnects [4].

1.1.3 Liquid Metal Flexible Interconnects

A prevalent application for liquid metal has been in flexible electronics. EGaIn at room temperature is in the liquid state, which allows is it to conform to the vessel it is contained in. Most flexible electronics based on liquid metal employ a Polydimethylsiloxane (PDMS) mold to define the electrical contact cavity where the liquid metal resides [5–7].

For instance, Hu et. al., use PDMS to define microfluidic channels that are filled with Gallinstan (68.5% Ga, 21.5% In, 10% Sn) that makes electrical contact to a carbon nanotube sensing element [5]. The purpose of this device is to detect changes in temperature and force. The Gallistan serves as a lateral interconnect that conforms to the microfluidic channel. Contact to the sensing element is not lost during changes in temperature or application of force. Similar implementation was pursued by Kim et. al., in which they use eutectic gallium indium (75.5 %Ga, 24.5 % In) encased in a PDMS mold, which is used as a stretchable interconnect with different linewidths and shapes [6]. They demonstrated a maximum variation of 0.24 Ω for a biaxial stretchable interconnect when stretched at 100% of its original length. Using the same concept of encasing the liquid metal, Surapeni et. al., implemented a ground-based sensor that measures changes in capacitance on a kapton film to determine shear and normal pressure [7]. A selection of different liquid metal sensors is shown in Fig.1.5. The implementation of liquid metal into a flexible mold for flexible electronics has been the predominate application found in literature.



(a) (b)

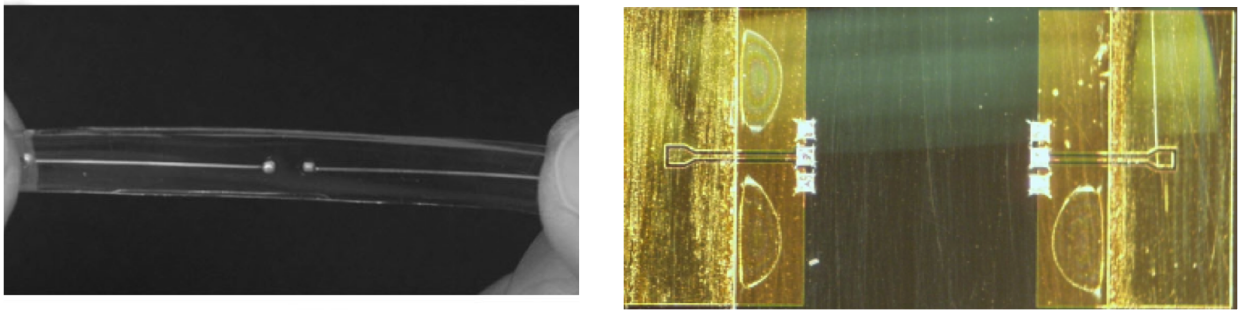
(c)

Figure 1.5: Comparison of different liquid metal flexible interconnect implementations such as a (a) flexible sensor skin [5], (b) multi-axial strechable interconnect [6], and a (c) self-repairing ground reaction sensor [7].

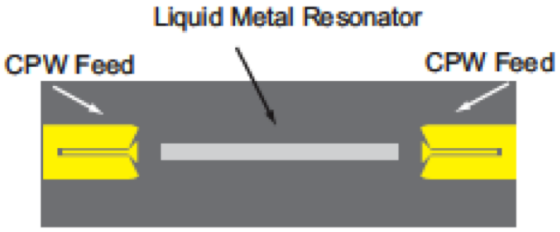
1.1.4 Liquid Metal RF Devices

RF devices based on liquid metal technology have been demonstrated to be a promising technology by some researchers. This is evident by the implementation of RF devices employing EGaIn in an antenna [8], microstrip resonator [18], and a coplanar waveguide [10] among others.

For example, So et. al., implemented a liquid metal based antenna that uses microfludic channels to define a dipole antenna in PDMS substrate [8]. The antenna can be mechanically tuned and is sensitive to strain. In addition, the antenna's resonant frequency can be shifted based on the amount of stretching introduced into the substrate. Meanwhile, Liu et. al.,



(a) (b)



(c)

Figure 1.6: Summary of different liquid metal RF devices (a) flexible dipole antenna [8], (b) resonator [9], and (c) coplanar waveguide [10].

implemented a half wavelength microstrip resonator on a silicon substrate. They used a gold adhesion layer to define the liquid metal regions. This group studied different resonator lengths in order to extract the conductivity of the liquid metal. Alike to Liu's liquid metal resonator, Wood et. al., studied liquid metal interconnects using a coplanar waveguide on a silicon substrate. The interconnect was defined using SU-8 polymer and filled with liquid metal via a syringe [10]. The authors of this work note the insertion loss of the transition was less than 0.5 dB at 20 GHz and below. These different RF devices based on liquid metal demonstrate the potential of this material.

1.1.5 Summary

A brief introduction was presented on the different interconnect structures found in literature. We discussed reworkable interconnects by PARC and a series of z-compliant interconnects fabricated by other researchers. The purpose of these different interconnect

structures is to provide either reworkability and/or better thermal match to different substrate material. We also discuss in this section liquid metal DC and RF devices. In terms of DC devices, the predominate application of liquid metal has been in flexible electrodes. Meanwhile, RF devices that implement liquid metal have been fabricated on flexible and rigid substrates. Applications of liquid metal discussed include an antenna, a microstrip resonator, and vertical interconnects in a mold. The review of reworkable interconnect and liquid metal technology served as a motivator to use liquid metal in reworkable electronics as a non-solid interconnect.

Chapter 2

Fabrication of Liquid Metal Test Modules

The procedure for fabricating a complete die assembly is described in this section. The device structure consists of a bottom die, a silicon interposer, and a top die. The bottom die consists of pads that are 100 μm in diameter with a 200 μm pitch. Meanwhile, the top die incorporates pads that are 40 μm in diameter with the same 200 μm pitch. Two different modules were studied, a completely reworkable die in which the top and bottom die are removable and a half-reworkable die, in which only the top die is removable. The metallurgy for the completely reworkable die consists of gold/nickel pads and for the half-reworkable die, the pad metal is copper.

2.1 Bottom and Top Wafer Process

The fabrication process for both the bottom and and top wafer overlap in several steps. The key difference between the two are in the contact pad area and the daisy-chain metallization that complements each other. Silicon wafers are used as-is from the manufacture without any additional cleaning procedures performed. The wafers crystallographic orientation is <100> p-type with a thickness of 500 μm $\pm$ 25 μm. An overview of the process flow with schematic representations is shown below. A detailed traveler of the process can be found in Tables B.1-B.3.

2.1.1 Electrical Isolation From Substrate

Electrical isolation from the semiconducting substrate is acheived through the growth of a thin oxide. The process consists of loading wafers into the oxidation furnace shown in Fig.A.7. Wafers are then oxidized in pyrogenic steam at 1000 °C for 2 hours. This yields

an oxide thickness of 650 nm on both the front and backside of the wafers. The furnace temperature is ramped from an idle temperature of 400 °C to 1000 °C at a rate of 10 °C/min. When the temperature reaches 1000 °C, pyrogenic steam is introduced into the chamber by flowing hydrogen and oxygen in a two to one ratio respectively. The oxidation profile used in this process is shown in Fig.2.1.

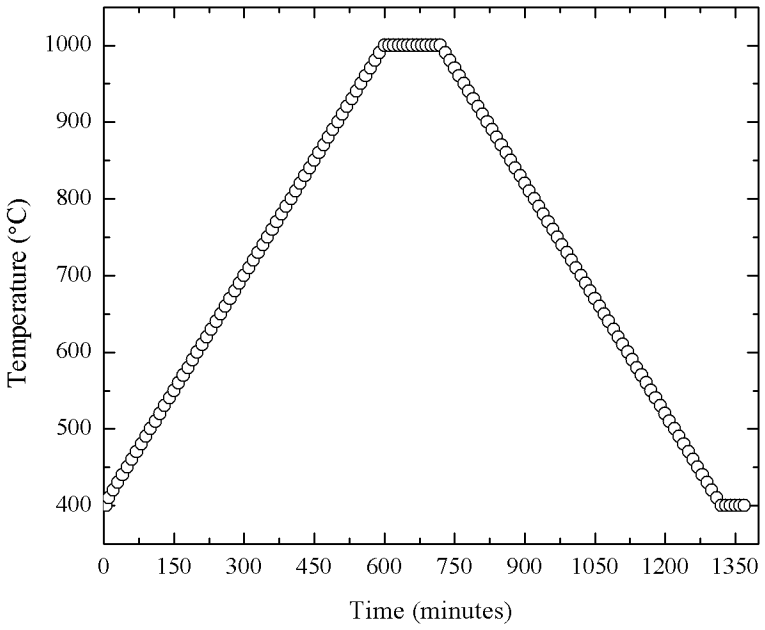


Figure 2.1: Two hour oxidation profile under pyrogenic steam.

2.1.2 Snake and Comb Contacts

Electrical contacts are defined photolithographically with AZ-9245 positive-tone photoresist. The photoresist is spun at a speed of 2200 RPM to achieve a thickness of 5 μm. A brewer science programmable spin-coater, shown in Fig.A.3 is used. Following the photoresist spin coating step, the wafers are then softbaked for 90 seconds on a hotplate set to 110 °C to harden the resist. After the softbake step, wafers are exposed under UV light for 12 seconds. A Karl Suss MA6/BA6 mask aligner (shown in Fig.A.4) is set on channel 2 with an exposure energy of 12.5 mJ/cm^2. The exposed regions are developed away with a ratio

of 150 mL of water to 50 mL of AZ-400K. Immediately following the development, wafers are loaded onto a matrix plasma descum system shown in Fig.A.5. The plasma power is set to 150 Watts for 30 seconds, which is then repeated twice for a total plasma exposure of 60 seconds. A two step process is used to let the wafers cool down between plasma exposures. Any residual photoresist left in the exposed areas is removed by the plasma exposure. This photoresist layer is used to define our base metal layer. The contact metal consists of 1000 Å of titanium for adhesion to the underlying silicon dioxide and 2000 Å of copper. The base metal snake and comb design mask is shown in Fig.A.15 for the bottom die and in Fig.A.18 for the top die metal layer. The photoresist is then removed by rinsing in acetone, methanol, water, and dried with nitrogen air. This step is shown in Fig.2.2a.

2.1.3 Completely Reworkable Module: Pads on the Snake and Comb

A copper seed layer is deposited over the previously defined snake and comb. This seed layer consists of 1000 Å of titanium and 2000 Å of copper. The seed layer establishes electrical conductivity across the entire wafer. This step is shown schematically in Fig.2.2b. This step is required in order to be able to electroplate copper pads onto the base metal. Lithographically we define the regions we wish to have electroplated. Following the seedlayer deposition, wafers are transferred to a dehydration bake oven shown in Fig.A.1 for 30 minutes to grow a thin copper oxide on the surface. The copper oxide reduces reflections during UV exposure. We then define regions on the snake and comb to be copper electroplated with AZ-125-NXT-10A negative-tone photoresist. The photoresist is spun at a rate of 600 RPM to achieve a thickness of approximately 110 μm, followed by an edge bead removal at 500 RPM with Edge Bead Remover (EBR) 70/30 for 20 seconds. Edge bead is the accumulation of photoresist at the edge of the wafer. If the edge bead is not removed, the wafer will get stuck onto the mask during exposure. The wafers are then softbaked in the 135 °C oven for 30 minutes (shown in Fig.A.2). The mask used for electroplating the pads is shown in Fig.A.16. The exposure time is 6 minutes and the unexposed areas are developed in AZ

300 MIF for 4 minutes. The photoresist serves as a soft-mask to allow plating only in the developed regions. We then electroplate the copper pins to our desired height of either 60 μm for the bottom wafer or 80 μm for the top wafer. The electroplating bath recipe used is outlined in Table C.1. Prior to electroplating, the wafers are dipped into a solution of 2% hydrochloric acid to remove the copper oxide from the regions we wish to electroplate.

Following the electroplating step, the photoresist is removed with a bath of AZ-400T photoresist stripper that is heated to 80 °C. After sitting in solution for 30 minutes, the wafer is transferred to another bath under the same conditions. Following the photoresist removal, a quick rinse in acetone, methanol, and water.

The subsequent step involves etching the underlying seed layer. The seed layer etchant for removing copper is listed in Table C.2. After the copper has been removed, the wafer is rinsed in water and submerged into buffer oxide etchant to remove the underlying titanium. The resulting electroplated pads on the base metal is shown schematically in Fig.2.2c. After the electroplating step was completed, the samples were sent out to Component Surfaces to be nickle/gold plated in order to improve the wetting of the liquid metal on the pads. This step is shown schematically in Fig.2.2d.

2.1.4 Half Reworkable Module: Pads on the Snake and Comb

A significant number of steps parallel the process of the completely reworkable module. For clarity, we discuss each step of the process and delve into more detail on the steps that are different.

Once the snake and comb layer has been defined, a copper seed layer is deposited for electroplating purposes, which consists of 1000 Å of titanium and 2000 Å of copper. This process is shown schematically in Fig.2.2b. Following the seedlayer deposition, wafers are transferred to a dehydration bake oven shown in Fig.A.1 for 30 minutes to grow a thin copper oxide on the surface. We define regions on the snake and comb to be copper electroplated with AZ-9245 positive-tone photoresist. The photoresist is spun at a rate of 22000 RPM

to achieve a thickness of 5 μm. The wafers are then softbaked on a hotplate at 110 °C for 90 seconds. We then expose the wafers for 12 seconds and develop in 1:3 ratio of AZ400K to water respectively. The mask used is the same as the reworkable interposer, which is shown in Fig.A.16. After exposure and development, any residual photoresist is removed by a plasma exposure at 150 Watts for 60 seconds. After plasma exposure, wafers are rinsed in 2% hydrochloric acid to remove the oxide from the regions we wish to electroplate. Contact pads are then electroplated to a height of 4 μm. The photoresist is then removed with acetone and methanol, followed by a DI water rinse and dried with nitrogen. After the photoresist has been removed, the wafers are then copper and titanium etched to leave behind copper pads on the base snake and comb.

2.1.5 Half Reworkable Module: AL-X Definition

In the half reworkable module, we use Asahi glass AL-X-2010 for electrical isolation between pads and as bonding adhesive. After the copper pads have been electroplated, the wafers are transferred to the dehydration bake oven for 30 minutes. Following the dehydration step, an adhesion promoter (AP903) is spun on for 30 seconds at a rate of 2500 RPM. The adhesion promoter is then baked onto the substrate at 100 °C for 90 seconds. After the adhesion promoter has been applied, AL-X-2010 is spun at 3000 RPM for 30 seconds to yield a thickness of 5 μm. The AL-X is then softbaked at 60 °C for 90 seconds. Wafers are then exposed in proximity mode for 30 seconds and developed with PS-201 on the spin coater. The mask design used in this process is shown in Fig.A.17. The exact development is more involved and thus described in greater detail in the traveler found on Table B.1 and shown schematically on Fig.2.2e.

After the AL-X has been developed on the wafer, it is left uncured and diced into individual modules. A top view image depicting the AL-X after exposure is shown in Fig.2.5. The assembly process is discussed in the module assembly section.

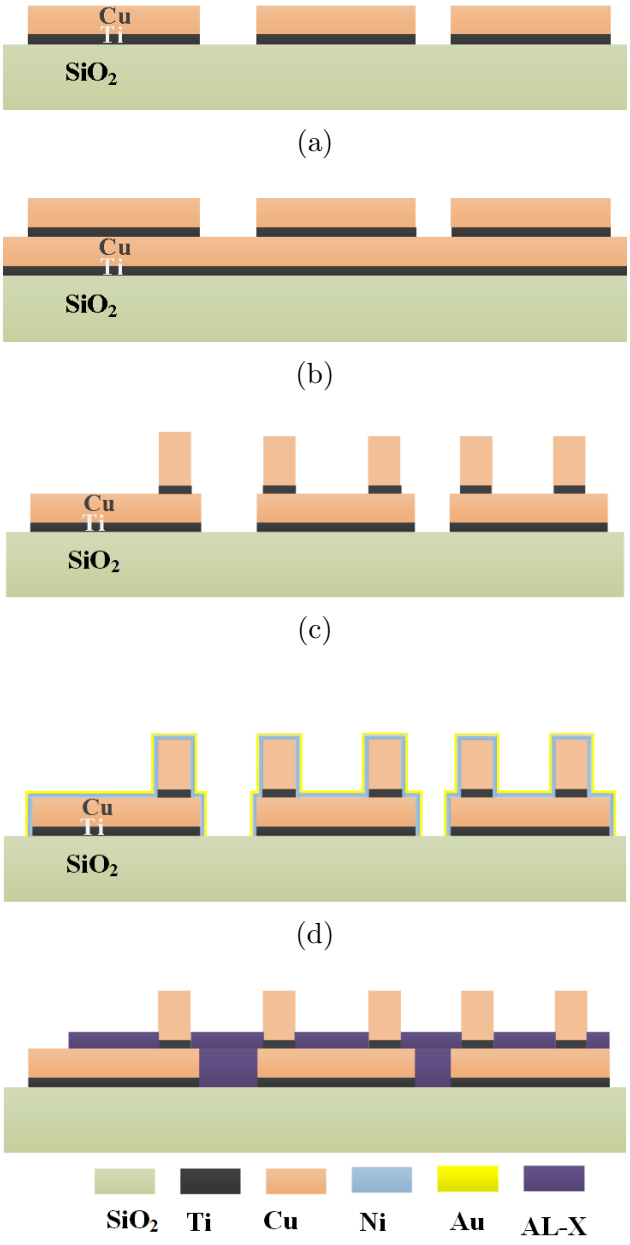


Figure 2.2: Schematic process flow for the bottom and top wafer. (a) Snake and comb pads defined (b) Seed layer deposition (c) Electroplated copper pillars (d) Ni/Au electroless plating for completely reworkable die (e) AL-X spin-on step for the half-reworkable module.

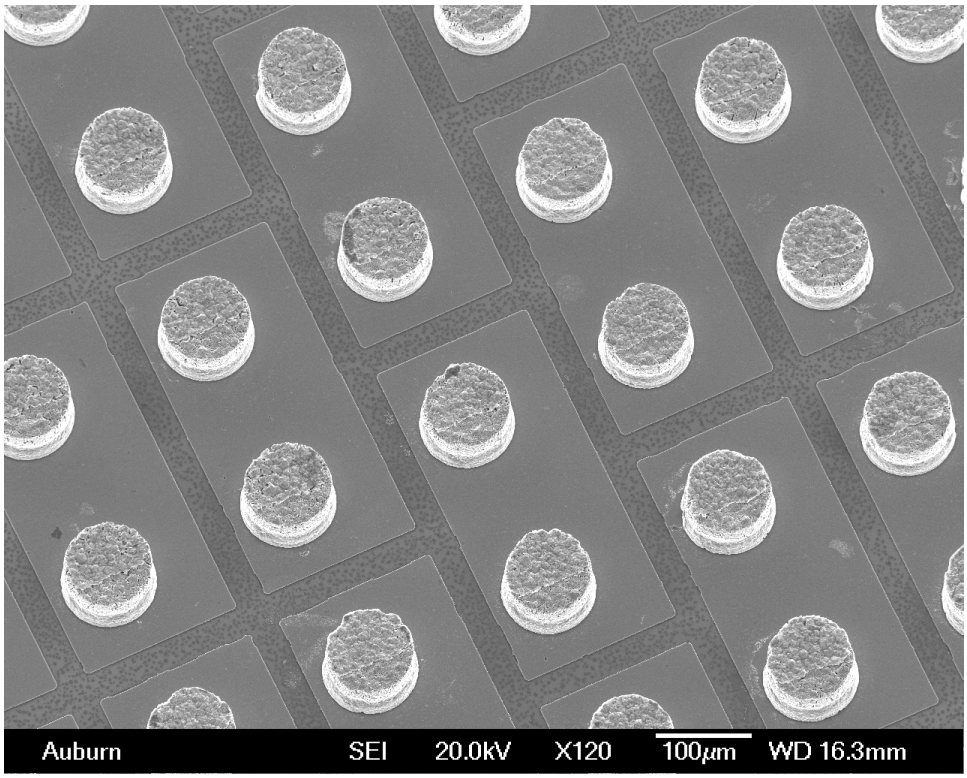


Figure 2.3: SEM imagery of bottom chip copper pads.

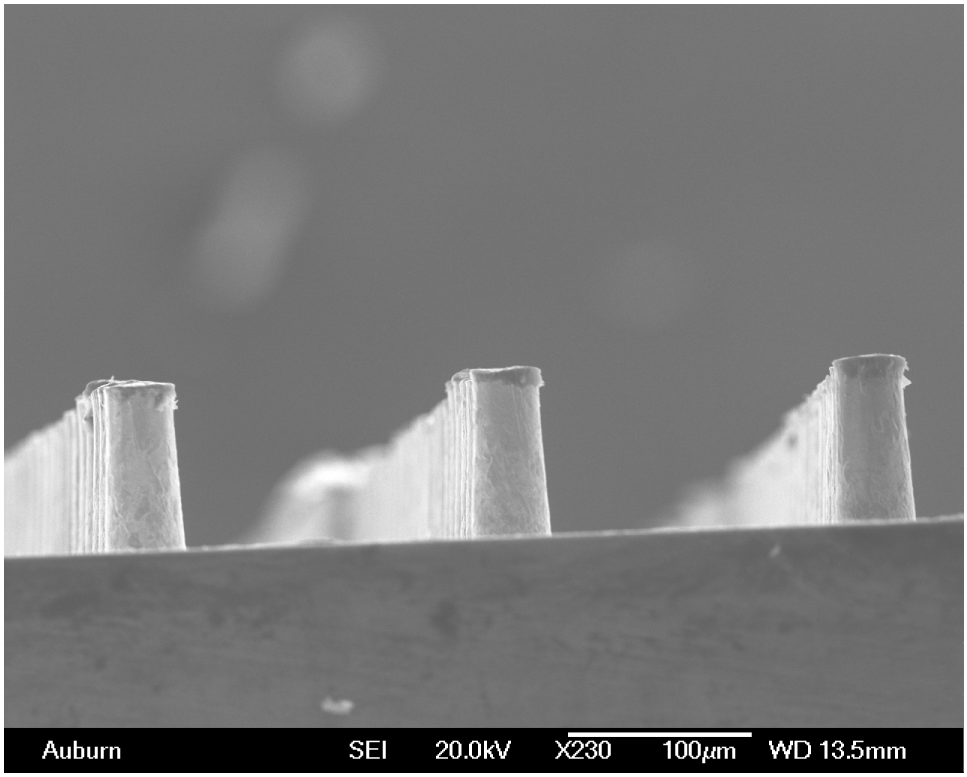


Figure 2.4: SEM imagery of top chip copper pins.

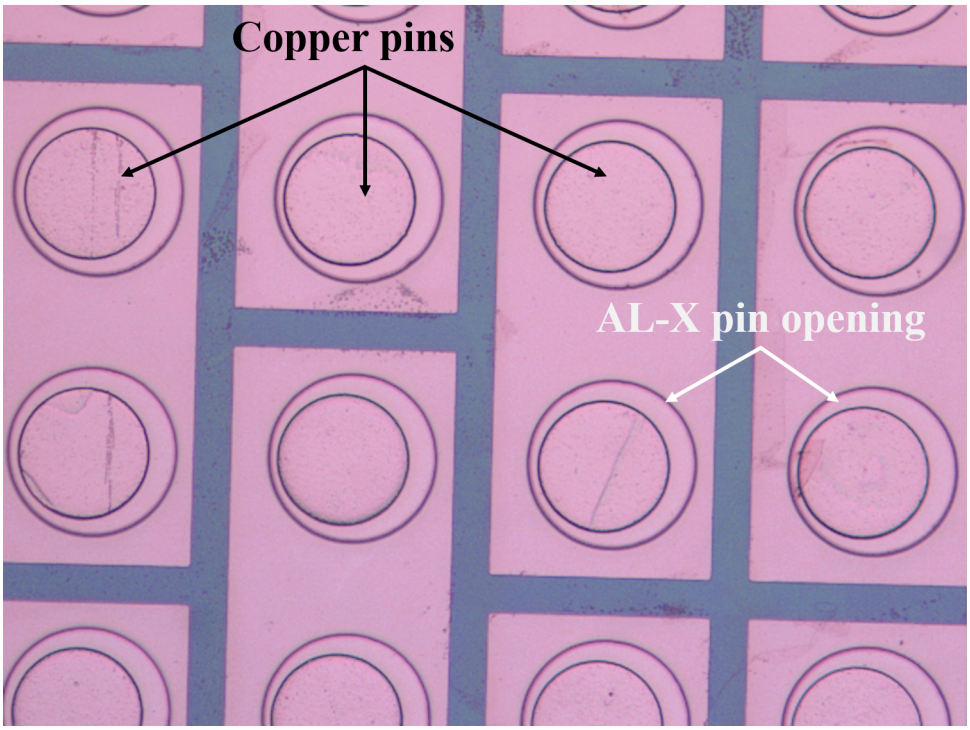


Figure 2.5: AL-X post-exposure top view image.

2.2 Low-k Dielectric Passivation and Bonding Studies

Asahi Glass AL-X 2030 was studied as a photoimageable adhesive for the assembly of a half-reworkable module. Test coupons were fabricated that had dimensions of 20.3 mm × 20.3 mm with 10 μm of AL-X. These samples were then bonded at different temperatures to oxidized silicon dies that were 8.5 mm × 8.5 mm. For these tests, the bonding load was kept constant at 1000 grams. The bonding and temperature profile for one test coupon is shown in Fig 2.6. After bonding, the samples were cured in a nitrogen ambient oven.

Analysis of the bond was performed with Confocal Scanning Acoustic Microscopy (CSAM). In CSAM analysis, we look for voids and particulate intrusion in the bond regions. Following CSAM analysis, we perform a shear test to study the strength (i.e. quality) of the bond. With the CSAM data and the shear testing results, we gain insight to how well the test coupons were bonded. A test coupon that was post-shear tested is shown in Fig.2.7. The results of the shear tests for different test coupons is shown in Table 2.1. CSAM imagery is shown in Fig.2.8a for a 90 °C bonded die and a 130 °C bonded die in Fig.2.8b. CSAM images of the other tested samples can also be found in Figs.A.12-A.14. In the 90 °C bonded die, we note a lot of grey spots, these indicate uneven curing of the film. For comparison, the 130 °C bonded die does shows a relatively uniform film.

Bond Temperature (°C)	Load (kg)	Shear Result
90	49	Sheared
110	> 40	Die cracked
130	> 40	Die cracked
150	> 40	Die cracked
170	> 40	Die cracked
190	> 40	Die cracked

Table 2.1: Shear Testing Results.

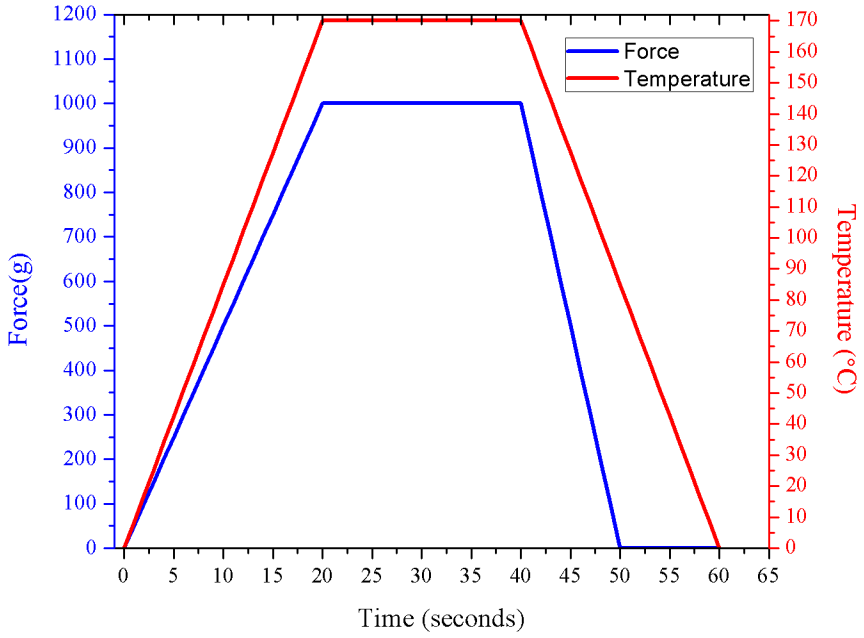


Figure 2.6: AL-X load and temperature profile used in these studies.

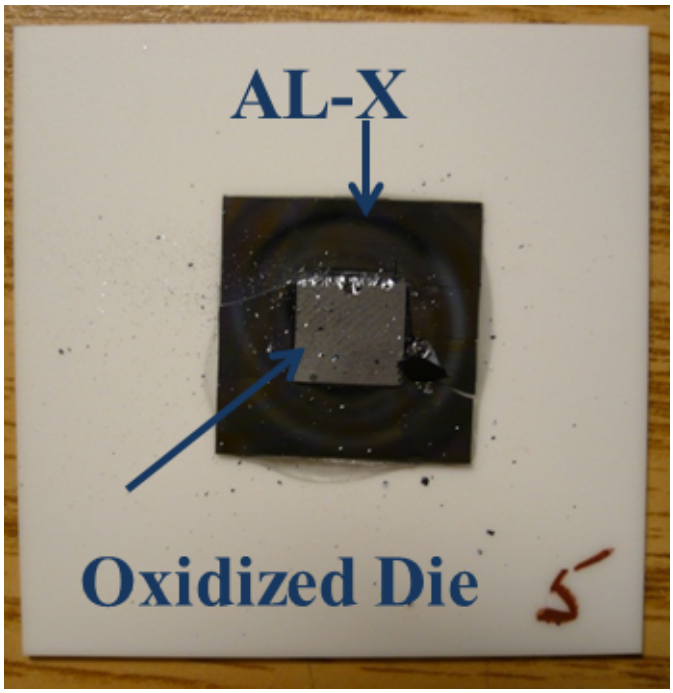
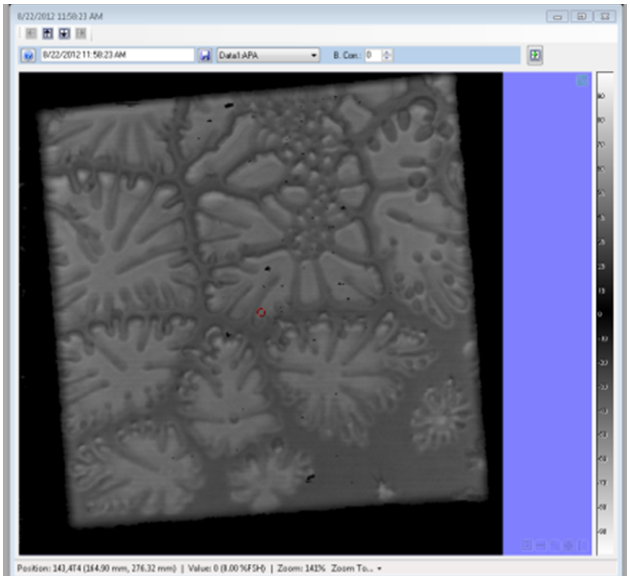
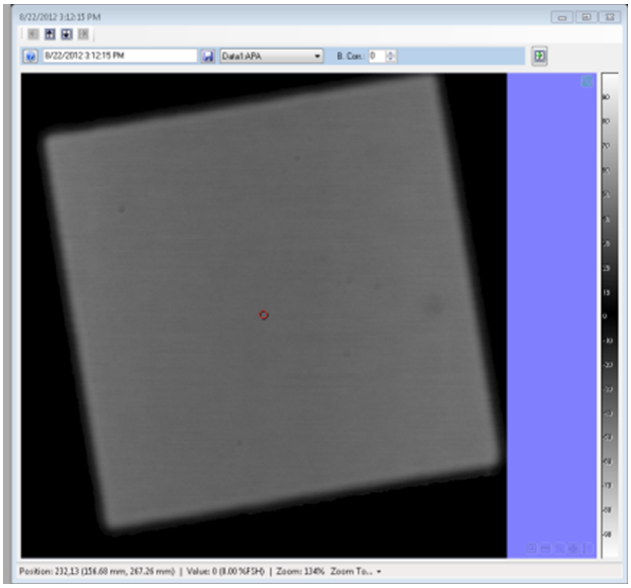


Figure 2.7: Test coupon post-shear mounted on a ceramic carrier.



(a)



(b)

Figure 2.8: CSAM imagery of a test coupon bonded at (a) 90 °C and at (b) 130 °C . The white outlines indicate voids in the AL-X layer for the 90 °C cured sample.

2.3 Interposer Wafer process

In the fabrication of the silicon interposer, we use p-type <100> wafers that are 200 μm thick and are double-side polished. Due to the thickness of these wafers, some additional processing steps are required. A detailed procedure is outlined below.

2.3.1 Top and Bottom Via Etch

The top via is defined photolithographically with AZ-5214 positive-tone photoresist. The photoresist is spun at a speed of 1000 RPM to achieve a thickness of 3.5 μm. The wafers are then softbaked at 110 °C to harden the resist. Following the softbake step, the wafers are then exposed for 10 seconds and developed in AZ-400K with a ratio of 1:3 of developer to water respectively. The mask design is shown in Fig.A.20 and Fig.A.21 for the top and bottom vias respectively. Any residual photoresist left in the exposed areas is cleared by a short 60 second plasma clean at 150 Watts.

After the vias are defined, the interposer wafer is then mounted onto a silicon carrier wafer. The carrier consists of a 2 μm thick photoresist layer that has not been softbaked. This photoresistive layer serves as a temporary adhesive. The interposer is then mounted onto the photoresist coated wafer. The wafer is then softbaked in the 90 °C oven for thirty minutes. This step is the most critical, the interposer must be well mounted on the carrier, with no gaps present. If their are any air pockets between the wafer, it is possible that it may dismount during subsequent processing that requires the wafer to be under vacuum.

After the wafer is mounted onto the carrier, it is transferred to an STS Advanced Silicon Etcher (ASE) shown in Fig.A.6. A Bosch process recipe is loaded on the ASE to etch 50 μm deep cavities into the silicon. Photolithographically, the width of the via is defined as 1000 μm for the top via. The top wafer is then unmounted by leaving it in an acetone bath overnight. Following the acetone bath, the wafer is rinsed in methanol and water and dried with nitrogen air. The backside of the wafer is then patterned and mounted on the carrier using the same procedure as before. The wafer is then etched 150 μm deep with a cavity

that is 150 μm wide. After processing, the wafers are then left in an acetone bath to dissolve the photoresist and rinsed in methanol, followed by water and dried. The wafers are then transferred to the oxidation furnace and oxidized at 1000 °C for 2 hours in pyrogenic steam.

2.4 Via Filling Procedure

Several different procedures were attempted prior to finding a process that led to satisfactory and repeatable via filling. The difficulty with working with EGaIn lies in that it readily forms an oxide in air, which alters its wetting properties. Some of the processes attempted are briefly discussed in this section. We also delve into a deeper discourse into the process that has led to successful via filling.

2.4.1 Via Filling Endeavors

Our initial trials filling hollow vias with EGaIn involved using a Dimatix DMP-2831 piezoelectric inkjet printer, as shown in Fig.2.9. The cartridge consists of a silicon printhead and a plastic reservoir. The cartridge was filled with EGaIn from a syringe. Our first attempt consisted of printing a pattern of different line widths which was unsuccessful. After analyzing the print head, we determined the piezoelectric actuator was unable to dispense EGaIn because the liquid metal was wetting the silicon-based print head. Modifications were made to the print head itself, such as back-filling the cartridge with nitrogen and heating the cartridge. These additional modifications did not resolve the issue.

Other methods were also explored, such as applying a compressive force to fill the vias in the interposer. The instrument used is shown in Fig.2.10. A petri dish was partially filled with liquid metal and a die was set on the surface. The arm would press down on the interposer die and liquid metal would be forced into the openings. This method was unsuccessful and a vacuum filling method was pursued. This is discussed in further detail in the following section.

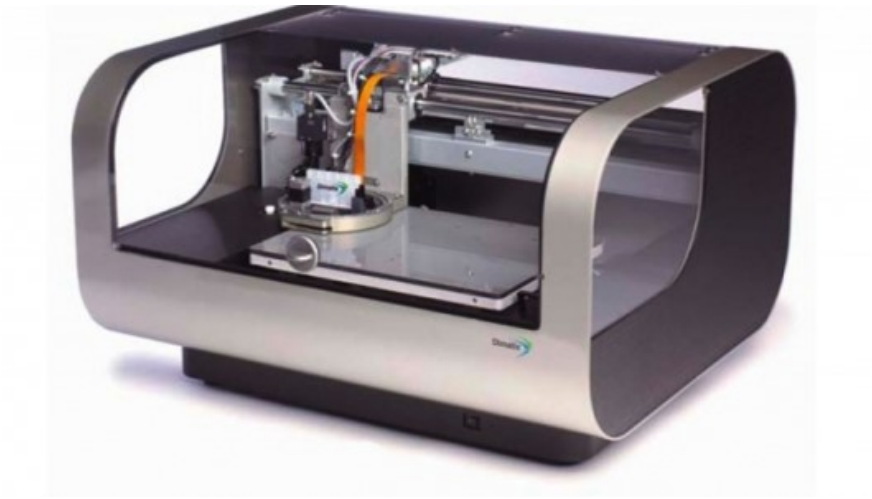


Figure 2.9: Dimatix DMP-2831 printer studied for via filling.

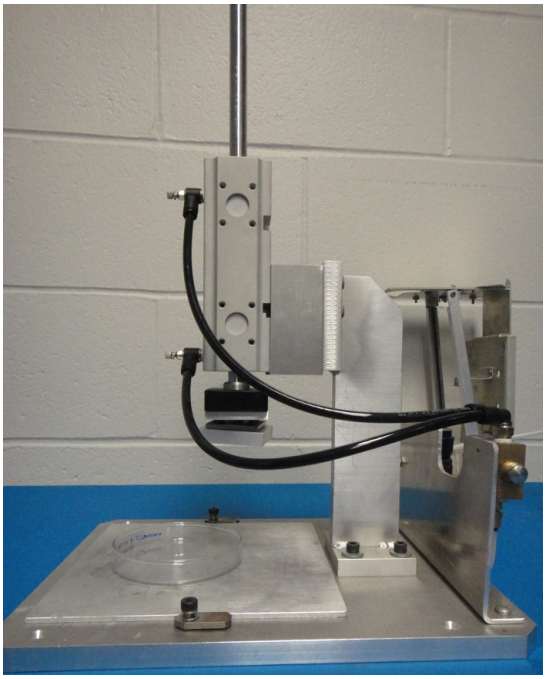
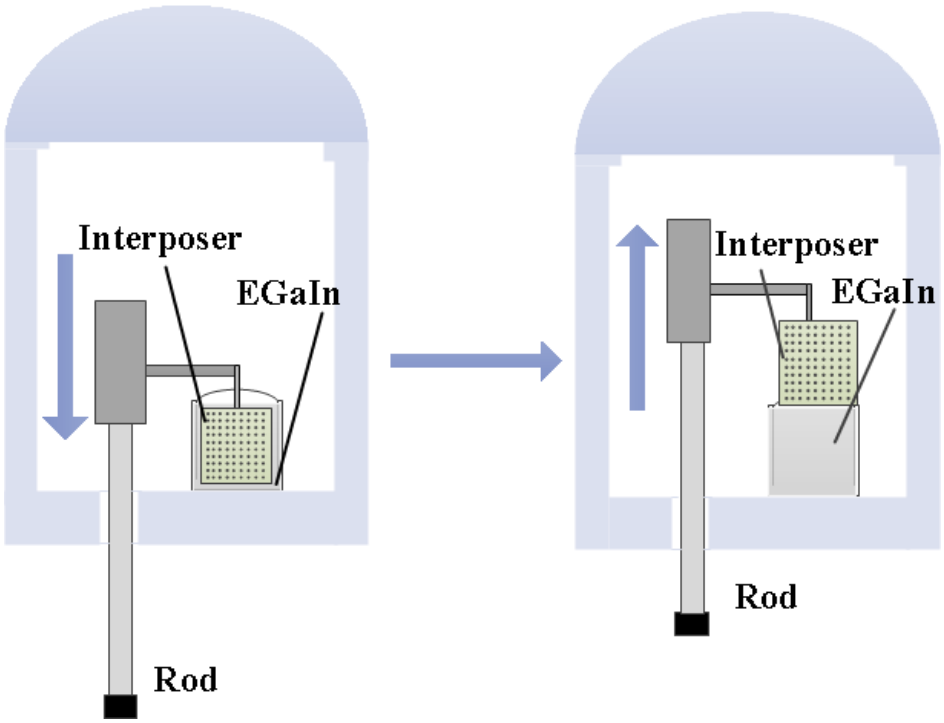


Figure 2.10: Compression tool used to force liquid metal into via openings.

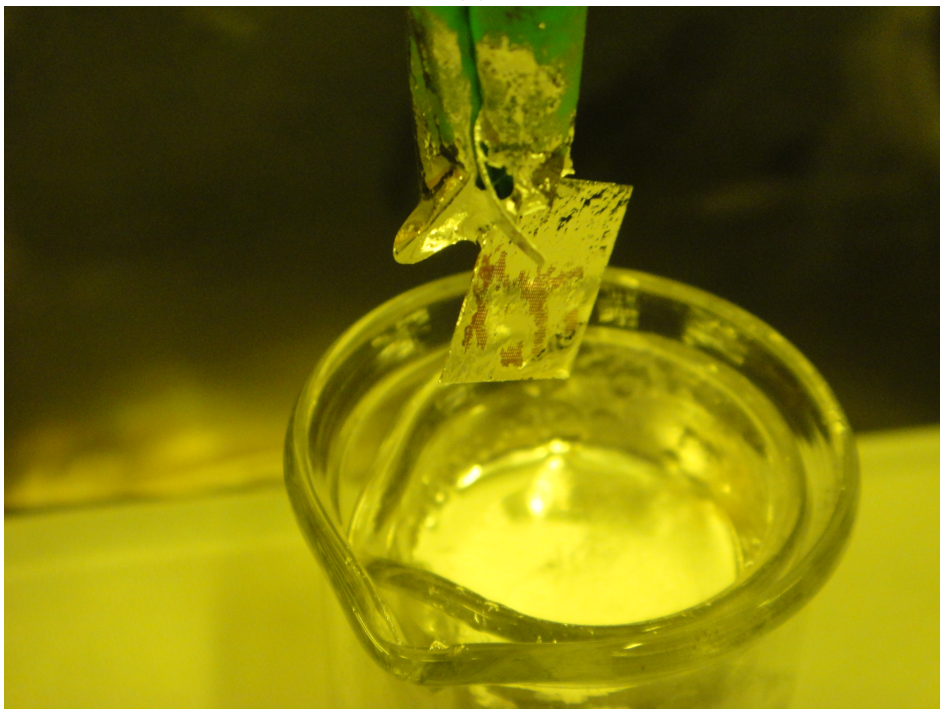
2.4.2 Via Filling Under Vaccum

Via filling under vacuum consists of loading an interposer die onto a custom holder that is inside a bell jar. The holder allows vertical travel under atmospheric and vacuum pressure. The sample is loaded under atmospheric pressure and lowered into a beaker that has been previously filled with EGaIn. The chamber is then pumped down to a pressure of $\sim$ 724 mmHg. We wait for the chamber to equilibrate at this pressure for 20 minutes. The chamber is then slowly backfilled with nitrogen. The holder is then raised vertically until the sample has been completely removed from the beaker. A schematic representation of this process is shown in Fig.2.11a. A die that has undergone this process is shown in Fig.2.11b. The beaker itself consists of EGaIn (78.6 % Gallium, 21.4 % Indium) from Sigma-Aldrich (# 495425-25G) filled to 20 mL in a 40 mL beaker. The EGaIn is used as-is, which exhibits a thin oxide at the surface. We are able to break through this oxide when we lower the die into the liquid metal filled beaker.

Following the via filling procedure, the die is unloaded from the holder and the surface is cleaned with a swab that has been previously immersed in Fantastik brand cleaner. The die is then transferred to a Phoenix PCBA X-ray machine to analyze the percentage of via filling. If the via yield is less than 90%, the process is repeated again. An X-ray of a half-assembled die is shown in Fig.2.12. Each sphere represents a single liquid metal via.



(a)



(b)

Figure 2.11: (a) Schematic representation of chamber used to fill interposer vias. The interposer die is clipped onto a custom holder. The rod moves in the vertical direction under vacuum and atmosphere.(b) Interposer die post-filled in atmosphere.

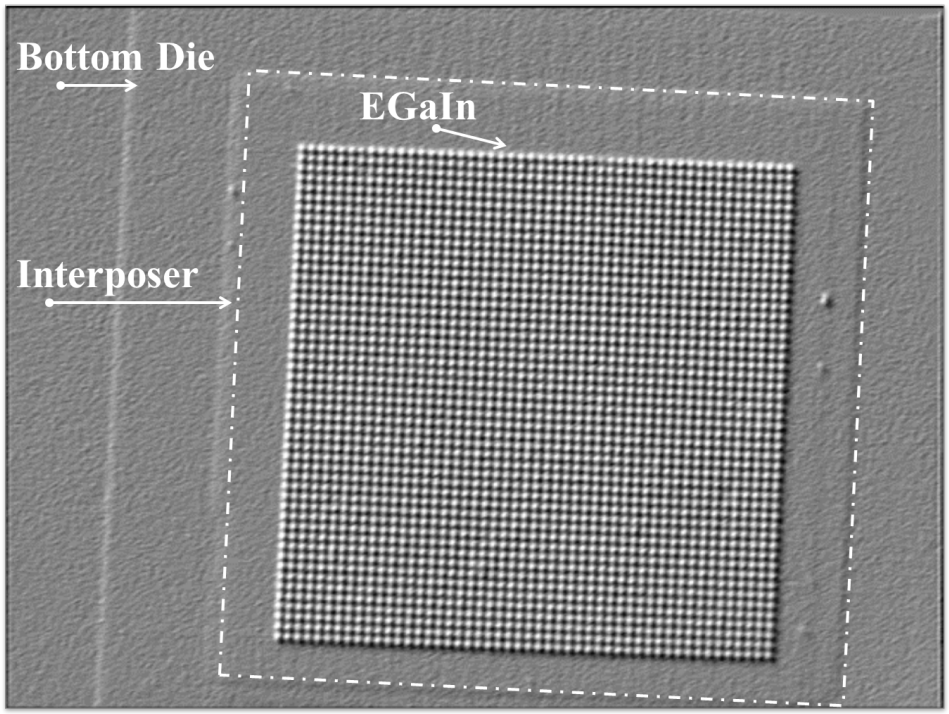


Figure 2.12: Half-assembled die with liquid metal vias prominent as spheres. Via yield higher than 90% is shown.

2.5 Module Assembly of a Fully Reworkable die

Assembly is performed using a Suss Microtech FC150 flip chip bonder, shown in Fig.A.8. An initial alignment calibration is performed, prior to any bonding, to ensure the bonding arm and the substrate camera are parallel to each other. This step involves adjusting X, Y, and θ by following the on-screen guide. After calibration is complete, samples are loaded onto the substrate stage and onto the bonding arm. The relative position of the samples once loaded onto the bonder are shown in Fig.2.13. After the samples are loaded, a second alignment procedure is performed between the top and bottom die. With the dual optics, we are able to precisely align the top chip and the substrate to a 1 μm tolerance. In our process, we align a liquid metal filled interposer with a bottom die. Alignment can also be performed with the top die and an interposer. The assembly procedure is independent of order.

Following the alignment, the two dies are brought into contact with a load of 1000 grams. Schematically this is shown in Fig.2.14. The load profile used in this process is shown in Fig.2.15. We ramp the load to 1000 grams within the first 15 seconds and keep this load for 35 seconds, we then remove the load from the sample and the bonding arm releases the vacuum hold on the top die, while maintaining vacuum on the bottom die.

After the insertion of the bottom die into the interposer via openings, we inspect the die for any excess liquid metal on the surface. Any excess liquid metal on the surface of the die is cleaned with Fantastik cleaner and a cleanroom cloth. We then proceed to load the top die into the bonding arm and the bottom half-assembly on the substrate table. We then align the top die to the via openings of the interposer die and repeat the same load profile. A post-bonded fully assembled die is shown in Fig.2.17.

2.6 Module Assembly of a Partially Reworkable die

Once the AL-X has been exposed and developed on the wafer, it is then diced into individual test coupons for assembly. The interposer die is loaded onto the bonding arm and the bottom die is loaded onto the chuck tooling. The die is then bonded with a load of 1000 grams and heated concurrently to 110 °C. Following bonding, the samples are transferred to a nitrogen ambient oven and cured. The bonding and heating profile used are shown in Fig.2.6, with difference in the bonding profile is the temperature set point, which is set to 110 °C during the force application.

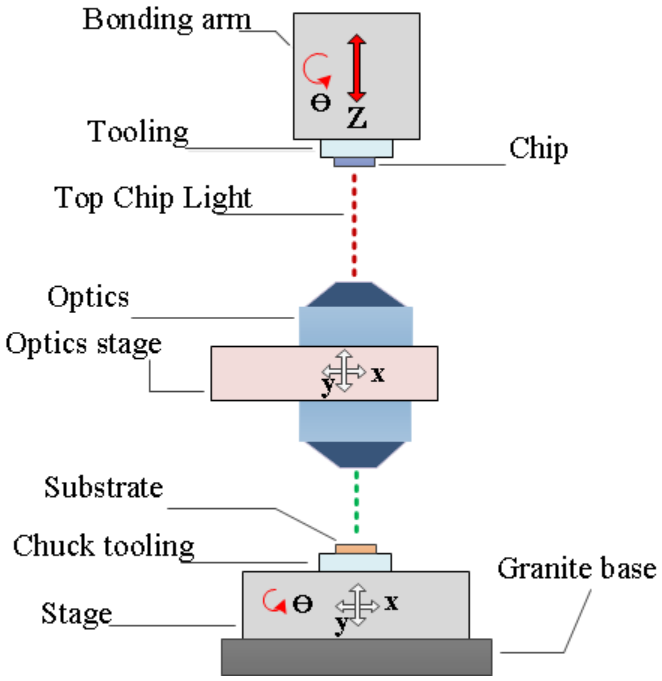


Figure 2.13: Schematic of Alignment Procedure on the FC-150.

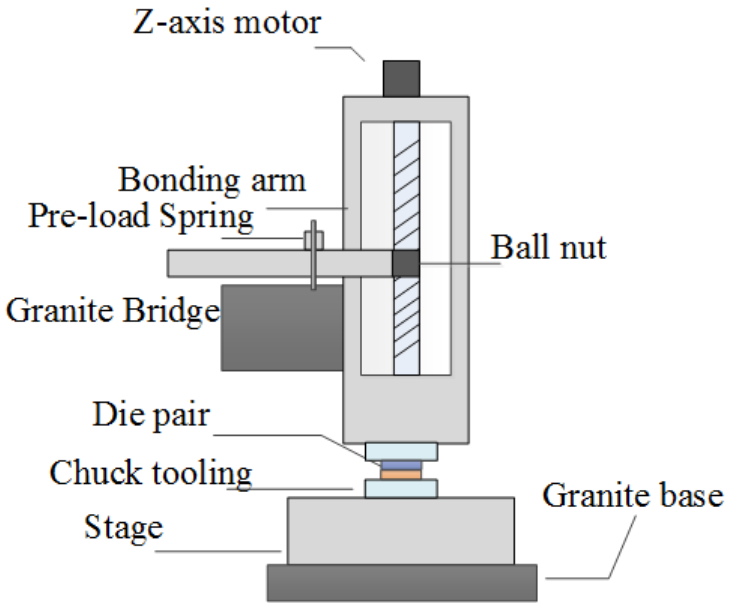


Figure 2.14: Schematic of Bonding Procedure on the FC-150.

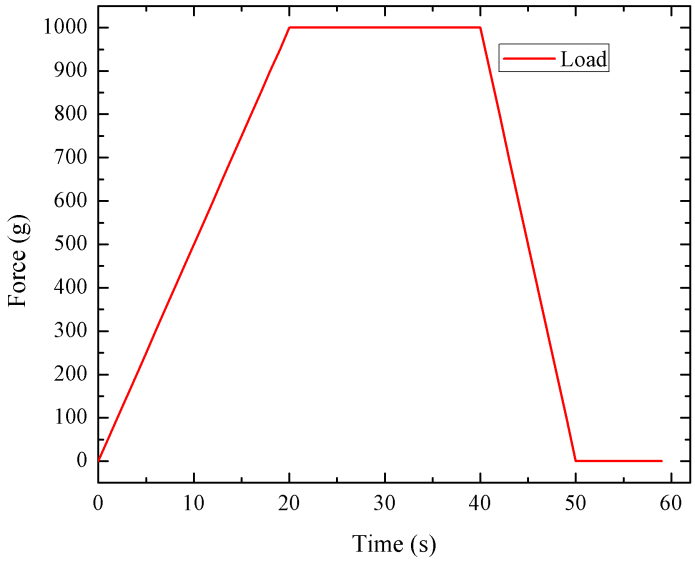


Figure 2.15: FC-150 bonding profile used for assembling modules.

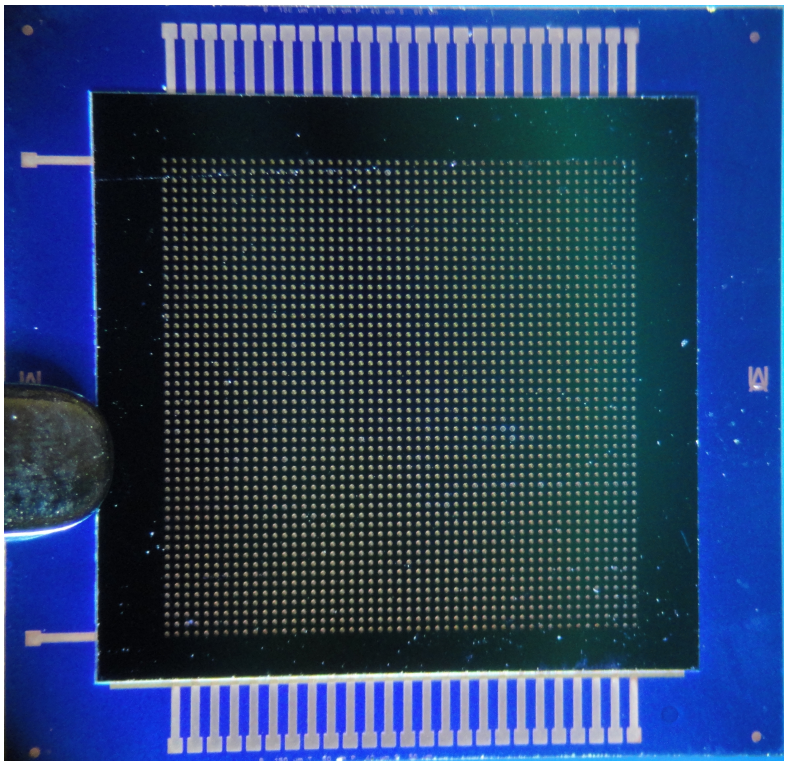


Figure 2.16: Half-assembled Module.

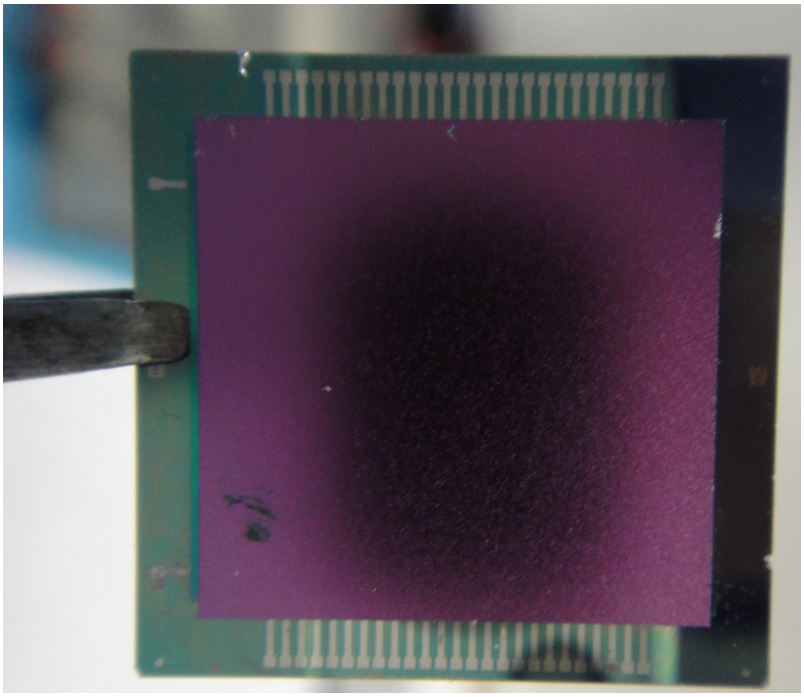


Figure 2.17: Fully assembled Module.

Chapter 3

DC Characterization

Current-Voltage (I-V) measurements were performed on a Keithley 4200-SCS parameter analyzer (shown in Fig.A.9). Two point probe measurements were performed on electrical shorts and opens to determine via yield. We also performed reworkability tests by removing the top die and reinserting it. Measurements were then repeated to document any changes in resistance. Simulations were also performed using Quartus Q3D Extractor version 12 to determine the impedance and inductance of the liquid metal vias as a function of frequency.

3.1 Low Frequency Simulations

Frequency sweeps were performed from 0-100 MHz to determine the impedance and inductance of the liquid metal vias. The contact pad metallurgy consists of .1 μm of titanium and .2 μm of copper. The conductivity of the metals used in simulation are shown in Table 3.1. A one transition simulation with two vias with the current density vectors overlaid on the model is shown in Fig.3.1.

We compare the DC resistance extracted from simulation as a function of the number of transitions to our as-fabricated devices. We simulate up-to five transitions and perform a linear-best fit to our data. Thus, we can extrapolate the resistance to any number of transitions. In our fabricated devices, the minimum number of transitions we can measure is two and the theoretical maximum is 600 transitions. A plot showing the resistance versus the number of transitions obtained from simulation is shown in Fig.3.2. From this data, we gather that the total resistance should be 68.7 mΩ/transition for fifty vias in series with twenty five transitions, which compares favorably to our measurement of 31 mΩ/transition for twenty-five transitions.

Metal-type	Conductivity (S/m)
Copper (Cu)	5.8×10^7
Titanium(Ti)	1.82×10^6
Eutectic Gallium Indium (EGaIn)	3.4×10^6

Table 3.1: Conductivity of Metals Used in Q3D Simulation.

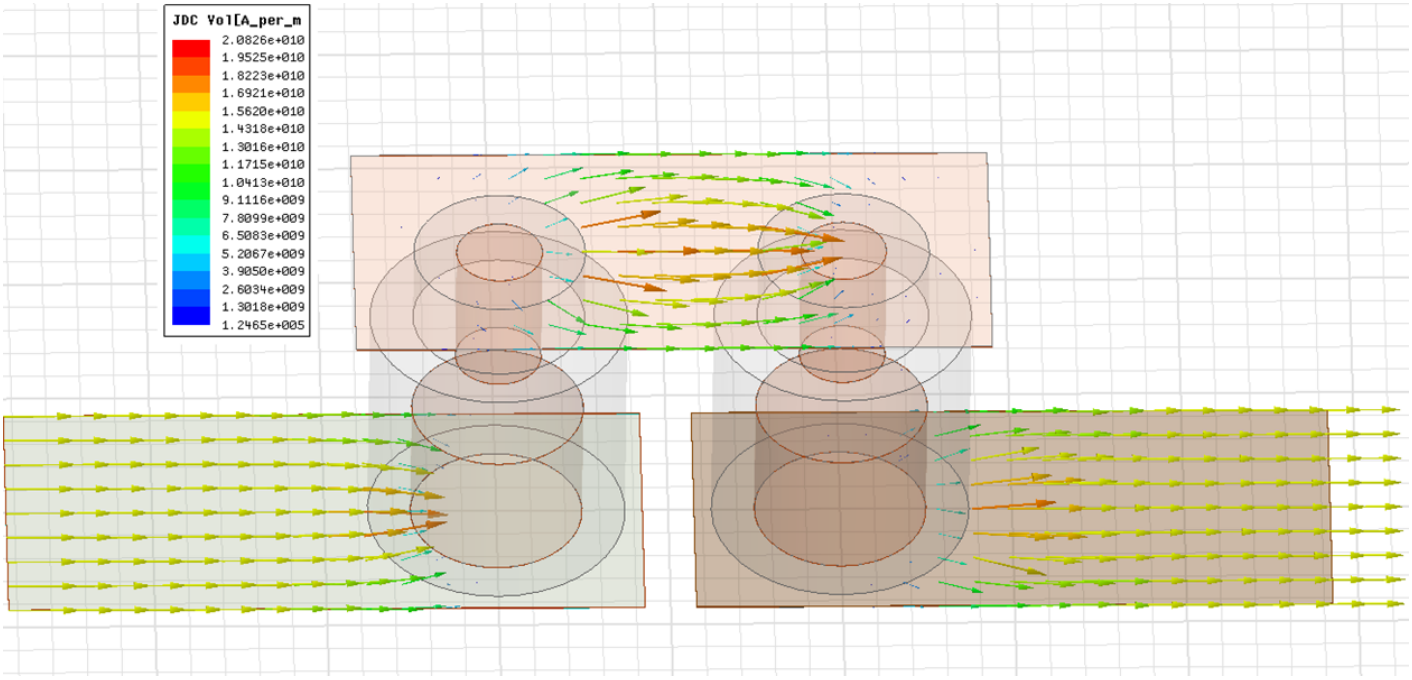


Figure 3.1: Q3D model used in simulation for one transition and two liquid metal vias in series.

We also study the total impedance and inductance of our structure as a function of frequency. We note as the frequency increases, the impedance increases (due to the skin effect) and inductance decreases. A plot of resistance and inductance as a function of frequency for varying number of transitions is shown in Fig.3.3 and in Fig.3.4 respectively. In particular, we note that the resistance and inductance increase as the number of transitions is increased.

In order to study the effects of the lateral materal and via size on the inductance, we build a simple model (shown in Fig.3.5) consisting of a single liquid metal via on a contact pad. We vary the dimensions of both independently to determine which component has the greatest effect on the inductance. Our initial parametric sweeps involved decreasing the pad size while keeping the liquid metal via diameter constant and in the same location.

The resulting inductance for different lengths is shown in Fig.3.6a. In this simulation, the via diameter is kept constant at 75 μm and the pad length is swept from 350 - 370 μm, meanwhile the inductance does not increase significantly. Meanwhile, as the via radius is decreased by 10μm , we note a higher change in inductance when the via radius is 55 μm. We attribute the much higher inductive change to the fact that a smaller via size causes the effective length of the lateral metallization to be larger. This is because the current has to travel a larger length to reach the via. Thus, although the via size does affect the inductance, it the lateral metallization that is the predominate factor that contributes to the higher inductance. In order to confirm that the lateral metal is a higher contributor to the total inductance, we sweep the radius of a single via. The model used is shown in Fig.3.7, we sweep the radius from 55-95μm and discern from Fig.3.8 that increasing the via radius leads to the lowest inductance. Thus, the lateral metallization has the largest impact on the inductance and therefore to minimize the lateral metal length should be reduced.

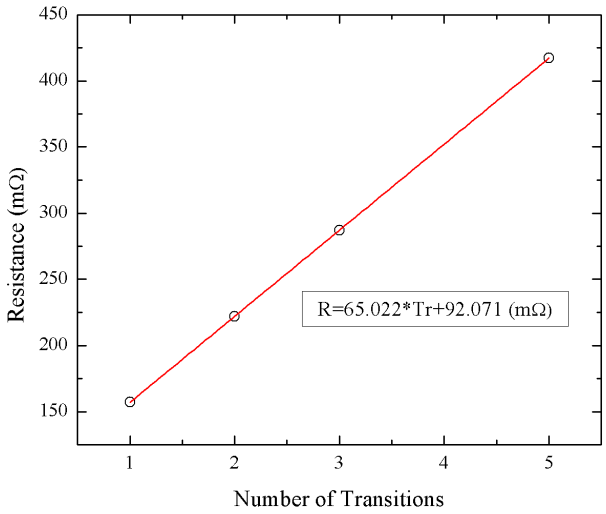


Figure 3.2: Resistance versus the number of transitions. A linear best-fit on the data for up to five transitions.

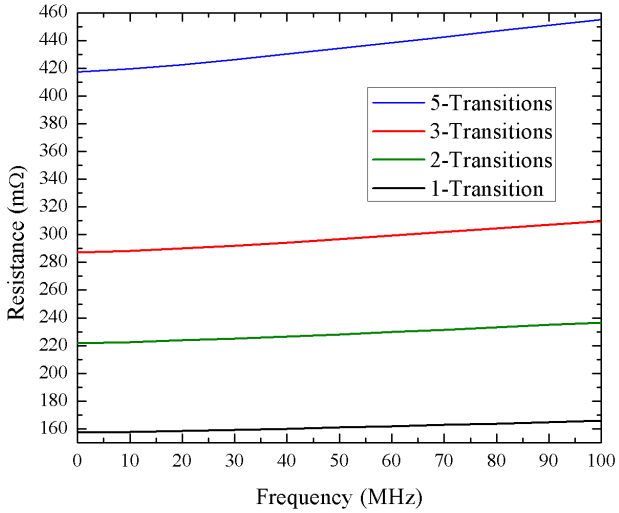


Figure 3.3: Resistance versus frequency plot for varying number of transitions (one to five transitions). The resistance increases about 10 mΩ from DC to 100 MHz for each transition.

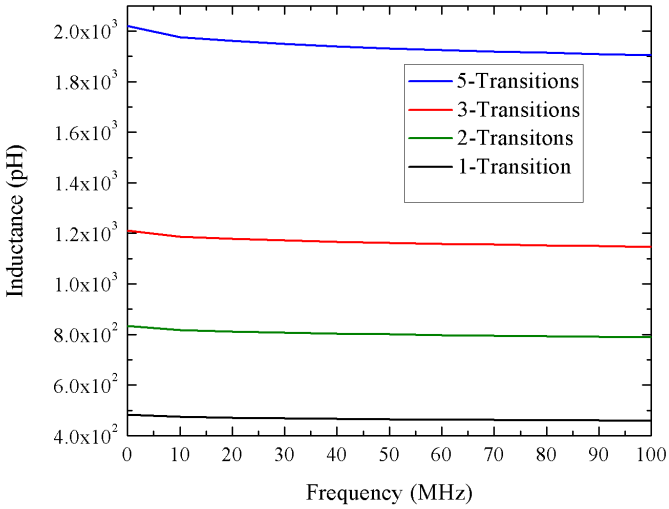


Figure 3.4: Inductance versus frequency for varying number of transitions (one to five transitions). The inductance decreases about 10 pH from DC to 100 MHz for each transition.

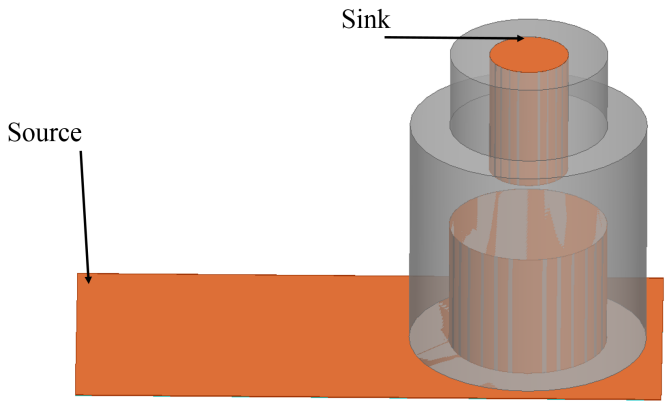
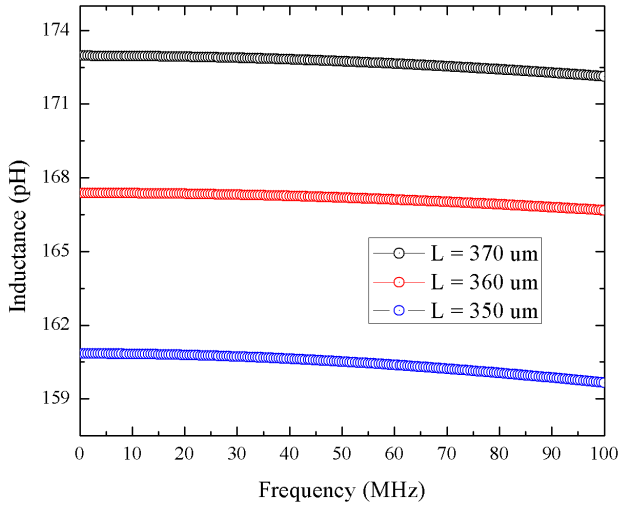
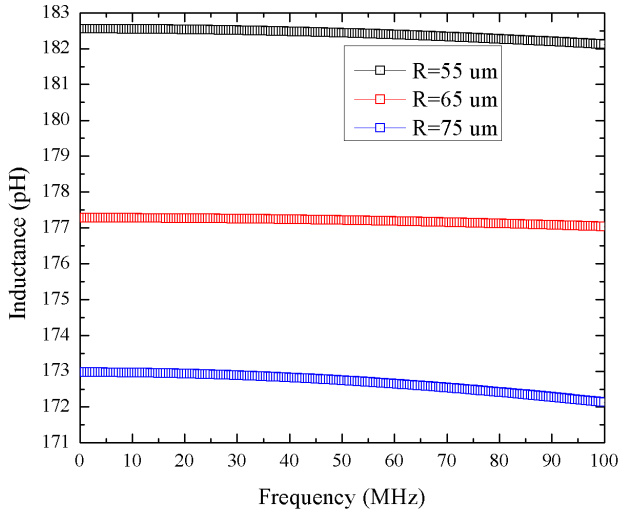


Figure 3.5: Model used to study the effects of varying the via diameter and pad length. A current source is applied at the edge of the pad and the ground is defined as the top of the pin.



(a)



(b)

Figure 3.6: The effects on inductance when (a) pad length is swept and via diameter is kept constant at 75 μm and (b) via diameter is swept and pad length is kept constant at 370μm increased.

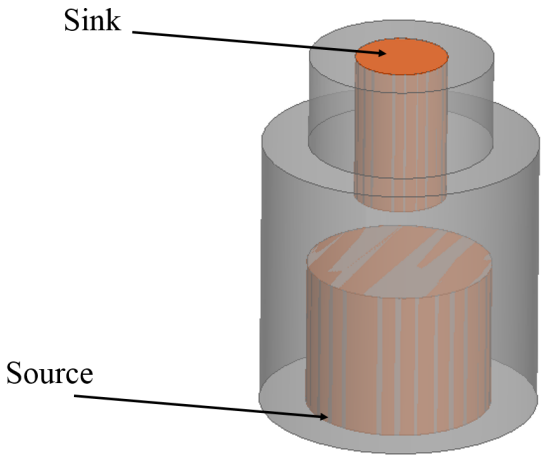


Figure 3.7: Q3d via model with source assigned to the bottom pin and sink assigned to the top pin.

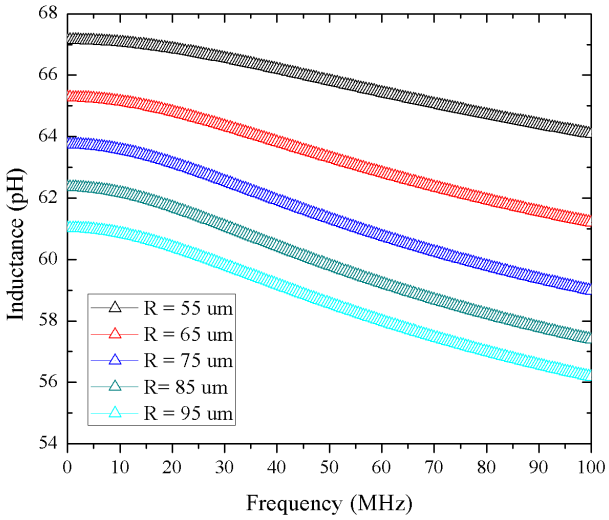


Figure 3.8: The effect of inductance as the via radius is increased from 55 to 95 μm.

3.2 As-assembled Module

In order to determine the resistance of the liquid metal vias, we eliminate the contribution in resistance from the contacts themselves. We therefore determined the total resistance (R_T) for a single transition (two vias), twenty-five transitions (fifty vias), twenty-six transitions (fifty one vias) and fifty transitions (one hundred vias). The resultant plot of total resistance versus number of transitions allows us to extrapolate the contact resistance by a linear-fit and exclude its contribution to the liquid metal resistance. From Fig.3.9, we determine the contact resistance to be approximately 8.64 Ω.

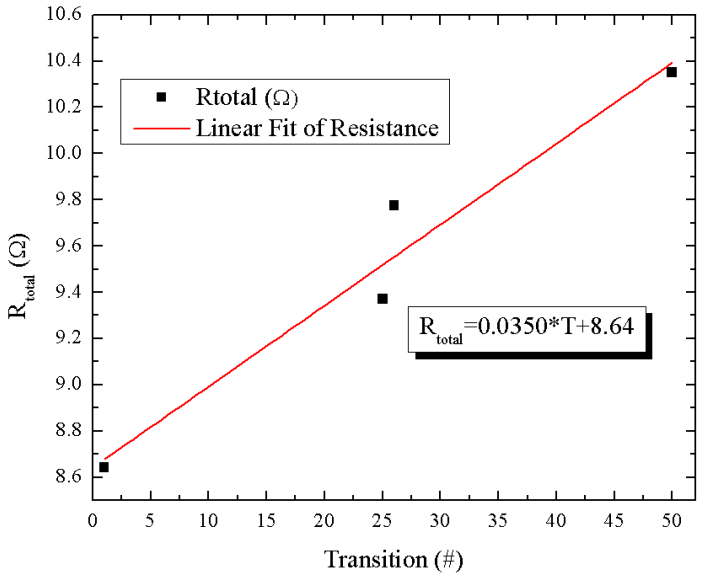


Figure 3.9: Resistance versus the number of transitions. A linear best-fit on the data for 2, 25, 26, and 50 transitions. The contact resistance is determined to be approximately 8.64Ω. The r^2 value of the linear-fit is 95.2%.

Our I-V measurements indicate a resistance of 0 .37 mΩ for 1 transition, 29.19 mΩ for twenty-five transitions, 43.6 mΩ for twenty-six transitions, and a resistance of 34.19 mΩ for fifty-transitions for an as-assembled die. We stipulate the reason the resistance is higher for the twenty-six transitions than for the fifty-transitions is due to laterally shorting that is present. We delve further into this issue at the end of this chapter.

3.3 Reworkability Testing

In our reworkability tests, we disassemble our modules by hand. A small amount of force with tweezers was applied to remove the top and bottom die from the interposer. Reassembly is performed on an FC150 with a load of 500 grams applied. Optical microscopy images were taken of a top die, after partial disassembly of our test module. As shown in Fig.3.10, we note the liquid metal wets the pins.

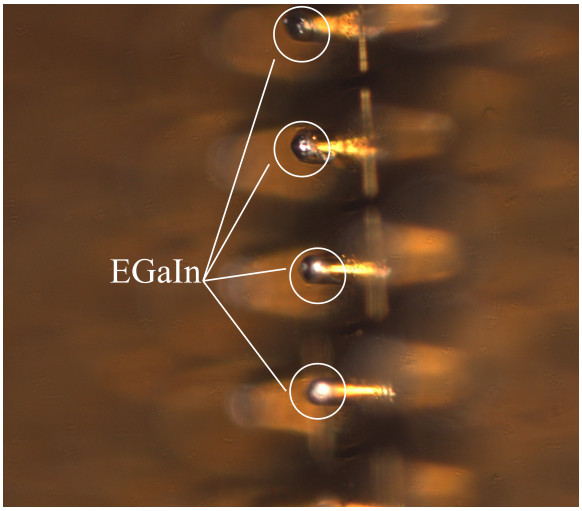


Figure 3.10: Liquid metal wetting of gold coated pins.

Current-voltage measurements were performed on twenty-five and fifty via array of liquid metal via chains. Thirteen different pad sites were measured on the die after assembly with a 4.0 Ω or less change in resistance. Measurement results for some of the test sites are shown on Table 3.2. Based on our measurements we calculate the average resistance $\bar{R}$ for a single liquid metal via and the standard deviation σ_R for the thirteen different pad sites. Our results are shown on Table 3.3, which indicate that the resistance is increasing due to the removal of liquid metal from the previous die attachment.

3.4 Temperature Studies

EGaIn exhibits a phase-change behavior from liquid to solid at a transition temperature below 15.7 °C. As the temperature is increased, the viscosity of the liquid metal changes. We

		Resistance (Ω)		
# of Transitions	# of Vias	Initial	New Top	Δ R
25	50	.719	2.61	1.89
25	50	.490	2.49	2.0
25	50	.761	4.63	3.86
50	100	1.26	3.18	1.92
50	100	1.17	2.04	.335
50	100	2.10	2.44	.333

Table 3.2: Resistance Measurements After Re-Assembly.

	$\bar{R}$ (mΩ)	σ_R (mΩ)
Initial	20.26	10.03
New Top	44.05	24.76

Table 3.3: Average Resistance For A Single Liquid Metal Via.

therefore measure the resistance of our samples at a temperature range from -43.15 °C to 80 °C. There are no apparent mechanical failures at these temperature ranges. At temperature below -33.15 °C, electrical contact is lost. I-V measurements for a fifty-via array indicate a proportional change in resistance with respect to temperature. Similar trends are noted for a two and a one hundred via array. The resistance trends are shown in Fig.3.11.

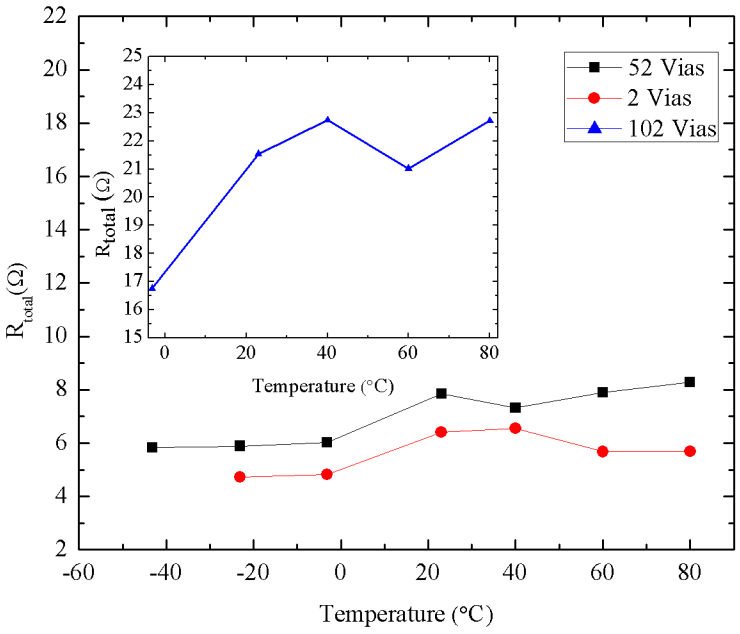


Figure 3.11: Resistance changes with varying temperature.

3.5 D.C. Characterization Conclusion

To summarize our results, DC simulations and preliminary measurements were made of the liquid metal vias. DC simulations indicate that the best-case resistance for the liquid metal vias is approximately 92 mΩ. We anticipate this resistance to be much higher because this model does not account for surface roughness and liquid metal volume variability. Although DC measurements were performed on different via arrays, their is shorting occurring between adjacent snake and comb across some pad sites. This has led to variations in the DC resistance. We can infer from our initial measurements that the via resistance could potentially be in the Ω range or less.

In our reworkability studies, we note that changes in resistance are occurring after removing and replacing the top die that weren't within measurement error. This indicates the removal of the die itself is removing liquid metal from the hollow via. With respect to how much liquid metal and how pronounced this problem is, we would need to perform X-ray computed tomography (X-ray CT), which would provide insight into this phenomenon. X-ray CT would provide a 3D map of how the pins and the liquid metal via interact inside the interposer itself before and after removal of the top die.

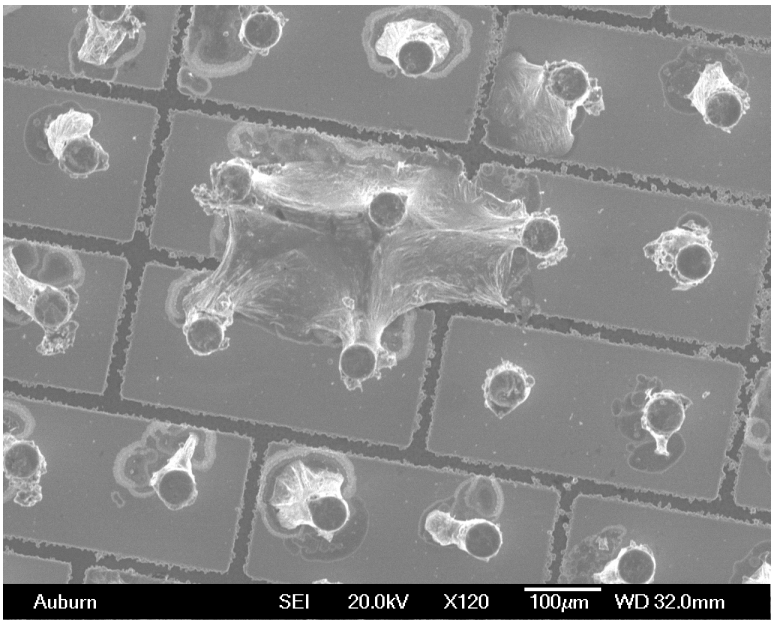
We also studied the effects of temperature on the liquid metal vias, we tested our samples from -43.15 °C to 80 °C. Foremost, we gathered from our temperature studies that below -43.15 °C, the module fails mechanically but not permanently. We lose electrical conductivity. Any temperatures below this, we lose electrical conductivity. We stipulate that this might be due to the liquid metal outside the via openings contracting. After the module reaches room temperature, the module resumes conductivity.

Chapter 4

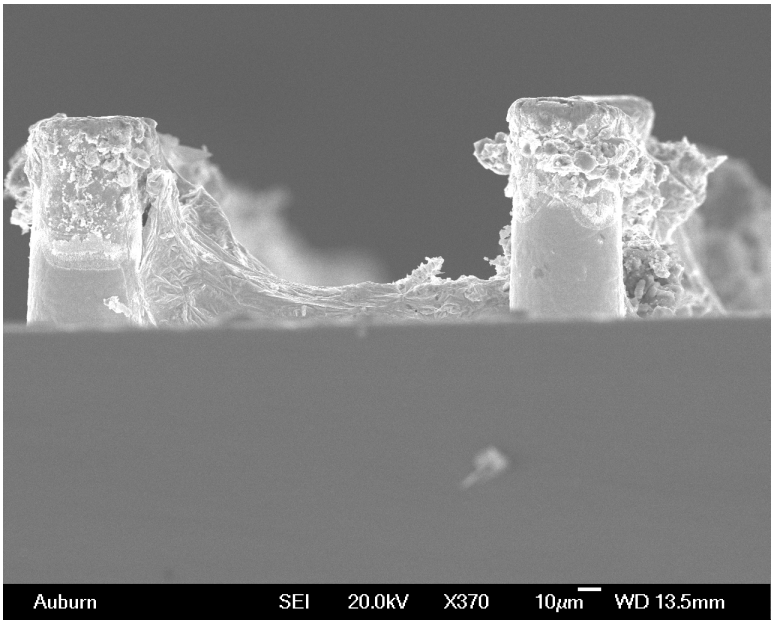
Failure Mechanisms and Yield

In this section we discuss the fabrication challenges associated with liquid metal vias. The predominate problem in our completely re-workable module design is via shorting. In the via filling process, the hollow via is filled in vacuum completely through, thus when the pins are inserted, the liquid metal is forced out of the via opening, leading to electrical shorts between contact pads. This phenomenon occurs on some of the pads, but not all. A Scanning Electron Microscopy (SEM) image of a typical short is shown in Fig.4.1a-4.1b. In the top view image, we note the adjacent pads are encased in liquid metal that resembles a web. Meanwhile, the side view picture illustrates the adjacent shorting that is occurring. Possible solutions will be discussed in the future work section.

With respect to via filling and yield, the process is quite successful. We are able to fill over 90% of the hollow vias under vacuum. Although the process is quite repetitive and slow, this can be improved by replacing the house vacuum used with a roughing pump.



(a)



(b)

Figure 4.1: SEM images of the top die pins. (a) Top view of local shorting occurring and (b) side view of the pins coated in liquid metal.

Chapter 5

Liquid Metal RF Coplanar Waveguide

5.1 Coplanar Waveguide Theory

A coplanar characteristic impedance depends on the dielectric thickness (h), the spacing (s) between the grounds and the signal line, as well as the width (w) of the signal. Schematically, the different dimensions relevant in the calculation of the characteristic impedance (Zo) is shown in Fig.5.1. The derivation of the characteristic impedance equation is dependent on elliptic integrals and thus only the main equations are referenced from [25]. We can infer from equations 5.1-5.6 the following information. The characteristic impedance is a function of the spacing and width of the line when air is on the surface of the coplanar waveguide. Furthermore, the effective dielectric constant is a ratio dependent on the substrate dielectric constant and the dielectric constant of the medium above the coplanar waveguide. For our simulations, we used a impedance calculator that can be found that employs the equations outlined below.

$$Z_0 = \frac{1}{(c \times C_{air} * \sqrt{(\epsilon_{eff})}} = \frac{30\pi}{\sqrt{\epsilon_{eff}}} \frac{K(k'_o)}{K(K_o)} \tag{5.1}$$

$$\epsilon_{eff} = \frac{C_{CPW}}{C_{air}} = 1 + \frac{(\epsilon_{r1} - 1)}{2} \frac{K(k_1)}{K(k'_1)} \frac{K(k'_0)}{K(k_0)} \tag{5.2}$$

$$k_0 = \frac{S}{(S + 2W)} \tag{5.3}$$

$$k'_0 = \sqrt{1 - k_0^2} \tag{5.4}$$

$$k_1 = \frac{\sinh(\pi S/4h)}{\sinh([\pi(S+2W)]/4h)} \tag{5.5}$$

$$k_1' = \sqrt{1-k_1^2} \tag{5.6}$$

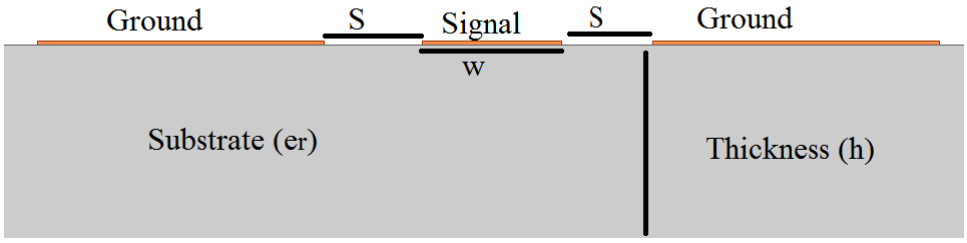


Figure 5.1: A coplanar waveguide characteristic impedance depends on the relative permittivity (ϵ_r) of the substrate, the width (w) of the signal line, the thickness of the dielectric (h), and the spacing between the signal and ground line noted as (s).

5.2 RF Simulations

A coplanar waveguide with varying size liquid metal vias was simulated in High Frequency Structural Solver (HFSS) version 13.02 and drawn in HFSS version 15.0. Frequency sweeps were performed from 5-35 GHz. A coplanar waveguide on silicon with 3 μm thick copper metal traces that are 55 μm apart from the signal line. The width of the ground lines are 205 μm with a length of 1027 μm. Similarly, the signal line is 100 μm wide and 1027 μm long. The HFSS model is shown in Fig.5.2. The frequency response of the coplanar waveguide, indicating less than -20dB return loss and less than -1dB insertion loss, is shown in Fig.5.4a and in Fig.5.4b respectively.

Based on the results from the standard coplanar waveguide model, we designed a coplanar waveguide transition. The model is shown in Fig.5.3. The liquid metal vias are 90 μm

in diameter and the pins are 80 μm in this model. The liquid metal vias are 200 μm tall, which is the thickness of the interposer and the copper pins are 14 μm tall. RF simulations were performed on different liquid metal via sizes with diameters simulated from 90 μm, 45 μm and 52 μm to better understand the impact of the via diameter on the performance. At each liquid metal via size, the copper pin diameters were decreased in size in order provide a 10 μm misalignment tolerance.

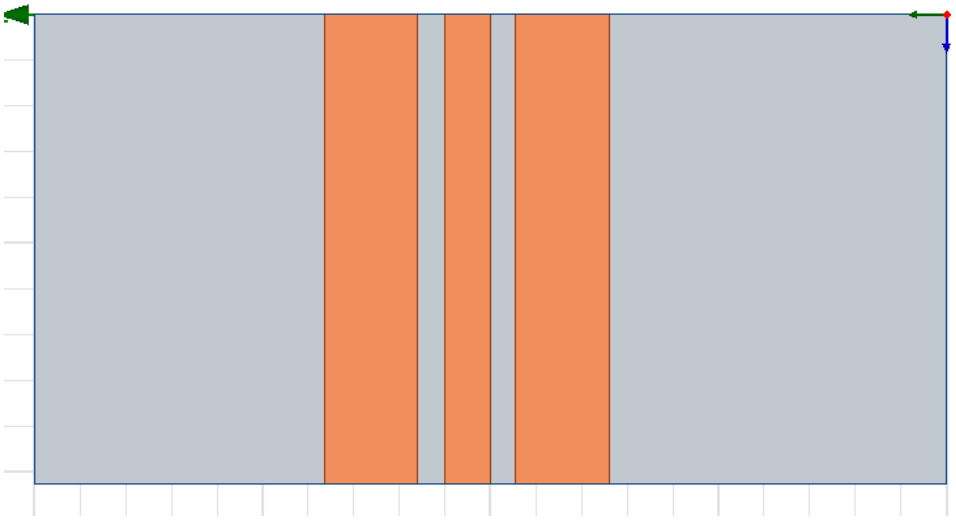


Figure 5.2: Top view image of the CPW model in HFSS. Line spacing between adjacent grounds is 55 μm. The width of the ground lines are 205 μm and the signal line is 100 μm wide.

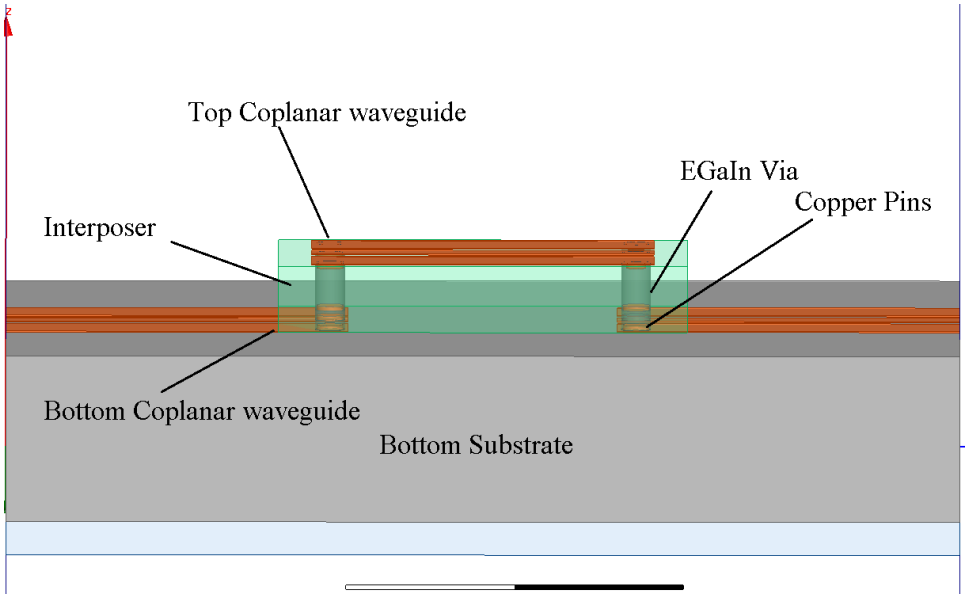
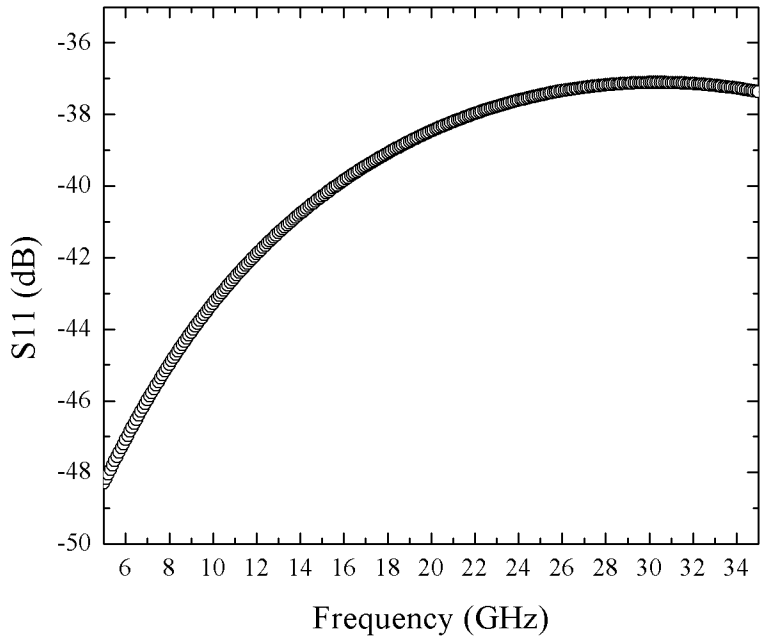
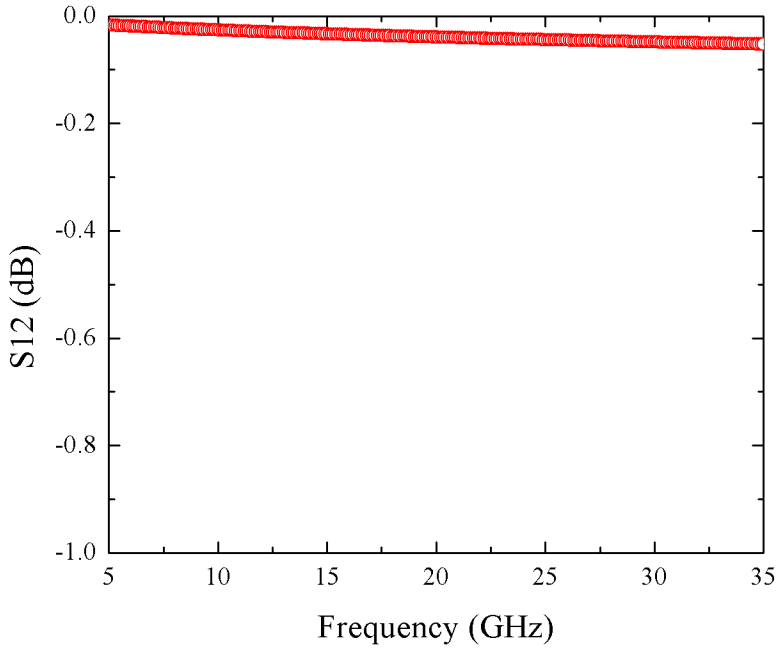


Figure 5.3: Side view image of coplanar waveguide with copper pads. Liquid metal vias are in the silicon interposer and the top and bottom coplanar waveguides make electrical contact by pins.

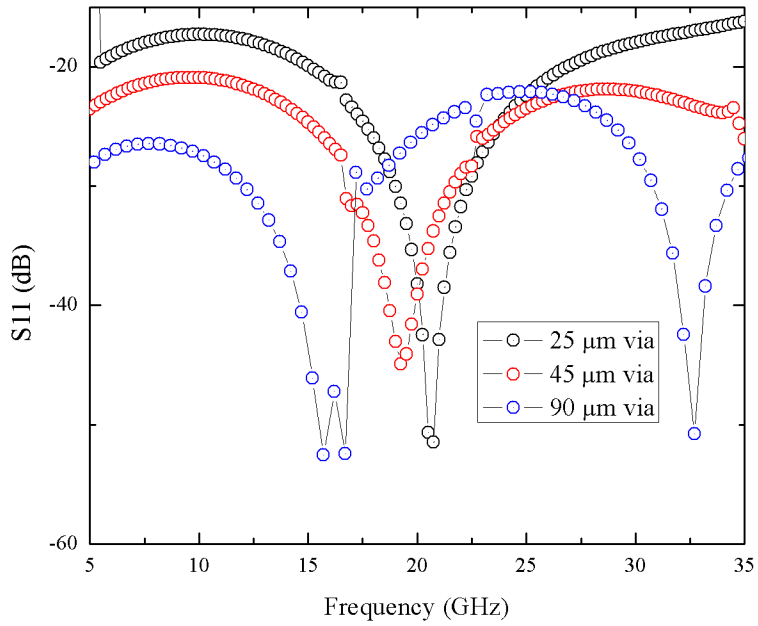


(a)

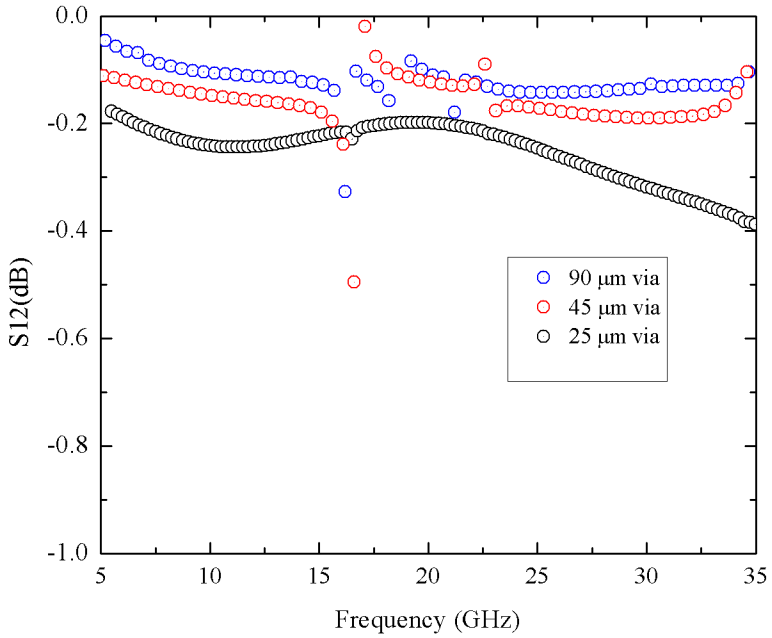


(b)

Figure 5.4: Frequency response for coplanar waveguide from 5-35 GHz. (a) Return and (b) Insertion loss.



(a)



(b)

Figure 5.5: Frequency response for liquid metal vias on a coplanar waveguide from 5-35 GHz. (a) Return and (b) Insertion loss.

Chapter 6

Conclusion and Future Work

In this work we discussed the design and fabrication of liquid metal vias in a silicon interposer. We described the process for via filling in vacuum and demonstrated a high via yield, which is confirmed through X-ray imagery. Two different types of modules were explored that led to insight to the liquid metal properties. A half-reworkable module, in which the interposer is bonded with AL-X to a bottom die, was studied. Early results with the half-reworkable module indicated via shorting and therefore a completely reworkable die was also explored. Similar issues were discovered with this implementation and SEM imagery confirmed that shorting was also occurring during the module build. From our preliminary DC measurements, we can infer that the resistance is quite reasonable, in the mΩ range. Furthermore, the variation we notice during measurement is due to shorting between snake and comb by some of the pad sites. In addition, we also performed DC measurements under varying temperature. We gather from these measurements our lowest operating range is -33.15 °C. In addition, we also studied reworkability properties of our liquid metal via interposer by removing the top die and replacing it, indicating that conductivity is present.

With respect to simulations, DC and RF simulations show promising results for liquid metal vias. DC results indicate resistance for liquid metal vias to be in the mΩ range, and RF performance indicate reasonable insertion loss from 0-40Ghz of about -1.0 dB.

In terms of future work, we are studying different methods to resolve the liquid metal shorting. Possible solutions include electroplating shorter pins, implementing containment structures, pre-wetting the pins with liquid metal and inserting them into an unfilled interposer. Our current approach involves using shorter copper pins that are 14 μm tall and surrounded with an AL-X boundary that is 10 μm tall and larger radius, which would serve

as a liquid metal reservoir. Based on results of this test, we will proceed further in testing other alternatives.

Based on our RF simulations, we are in the process of creating a mask design for testing different coplanar waveguide designs using liquid metal vias. We are interested in studying varying lengths, and number of transitions. This will provide significant insight into the liquid metal via performance.

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Appendices

Appendix A

Processing Equipment

Figure A.1: 120 °C Dehydration Oven

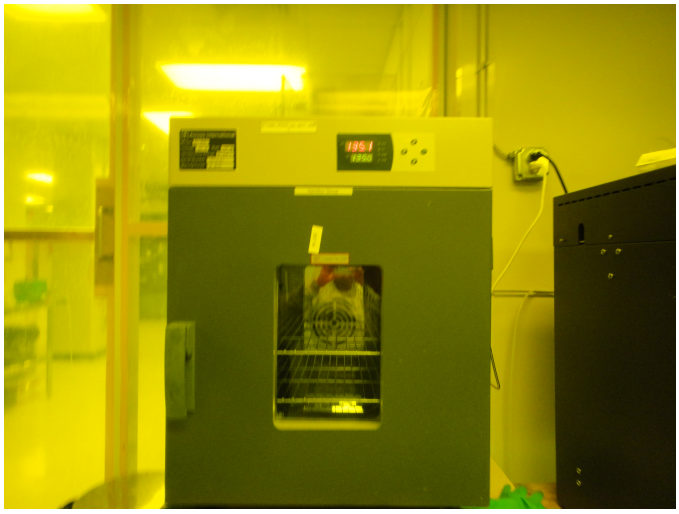

Figure A.2: 135 °C Softbake Oven for AZ-125-NXT-10A

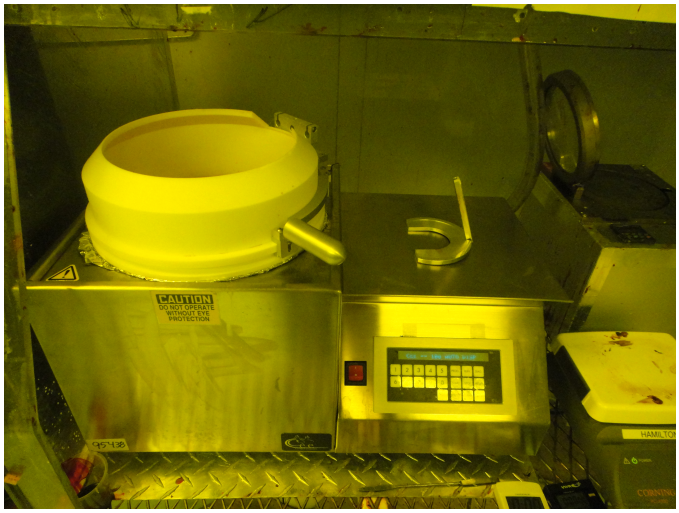

Figure A.3: Brewer Science Spin Coater

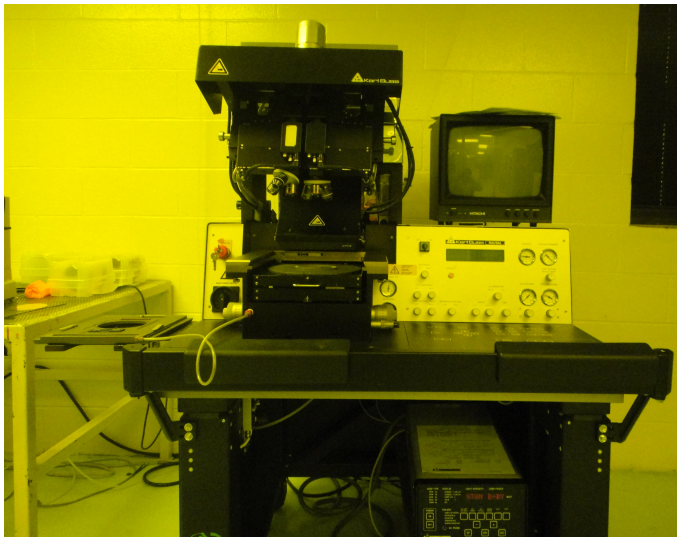

Figure A.4: Karl-Suss MA6/BA6 mask aligner

Figure A.5: Matrix O_2 plasma descum

Figure A.6: STS Advanced Silicon Etcher

Figure A.7: Oxidation Furnace

Figure A.8: Karl-Suss FC-150 Flip-Chip Bonder

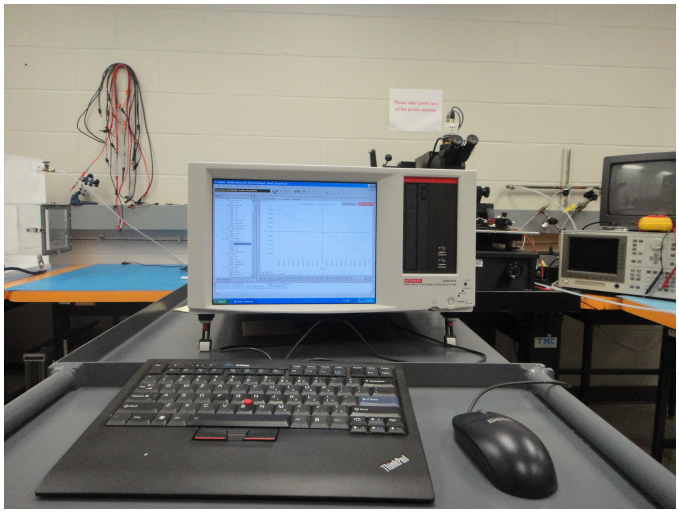

Figure A.9: Keithley 4200-SCS parameter analyzer.

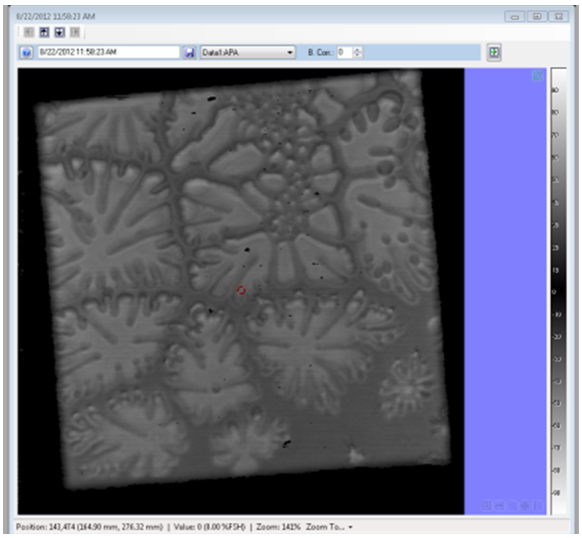

Figure A.10: CSAM image of AL-X bonded coupon at 90 °C

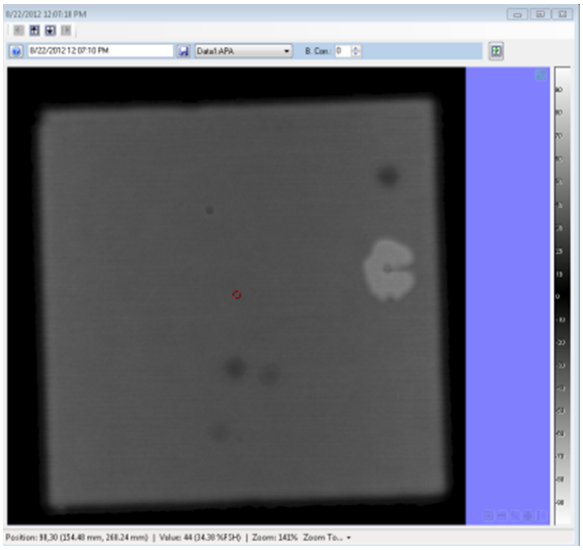

Figure A.11: CSAM image of AL-X bonded coupon at 110 °C

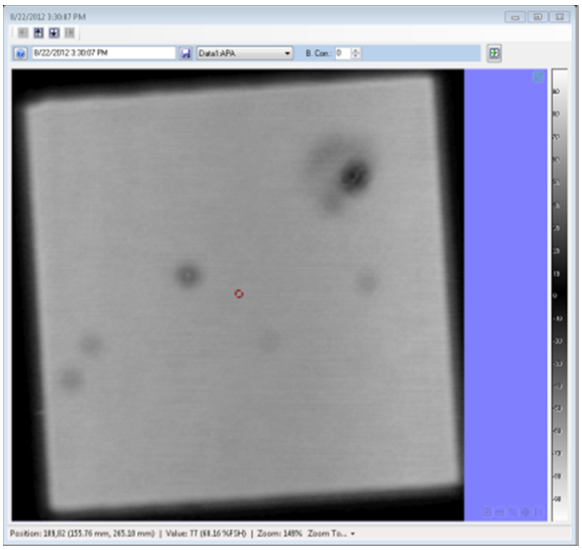

Figure A.12: CSAM imae of AL-X bonded coupon at 150 °C

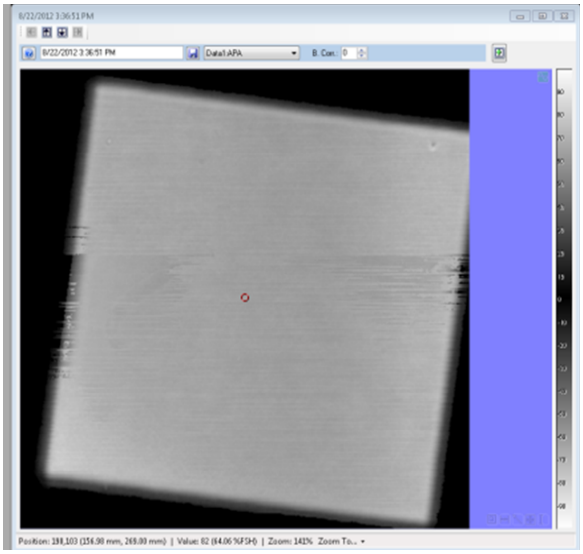

Figure A.13: CSAM image of AL-X bonded coupon at 170 °C

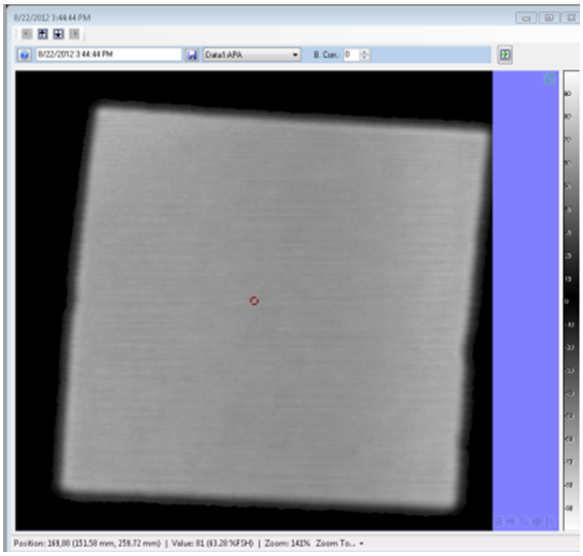

Figure A.14: CSAM image of AL-X bonded coupon at 190 °C

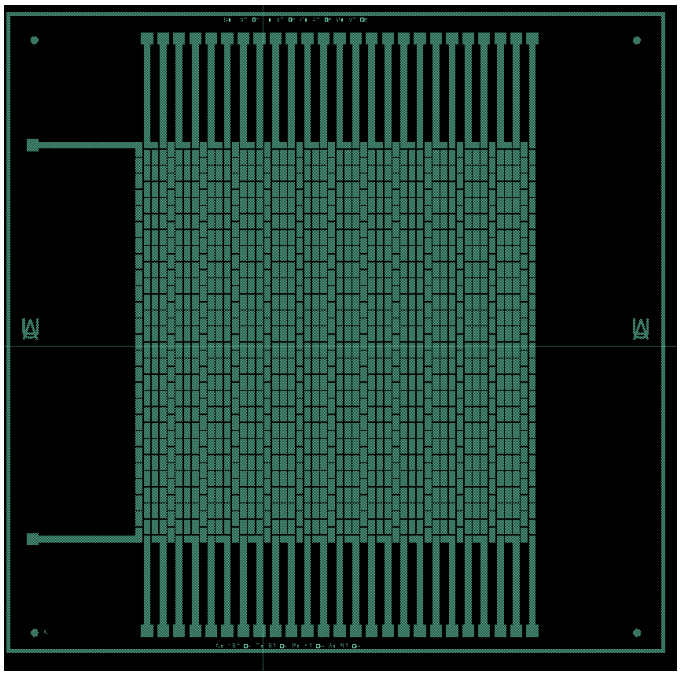

Figure A.15: ADS layout for the first metal layer on the bottom chip with the snake and comb defined.

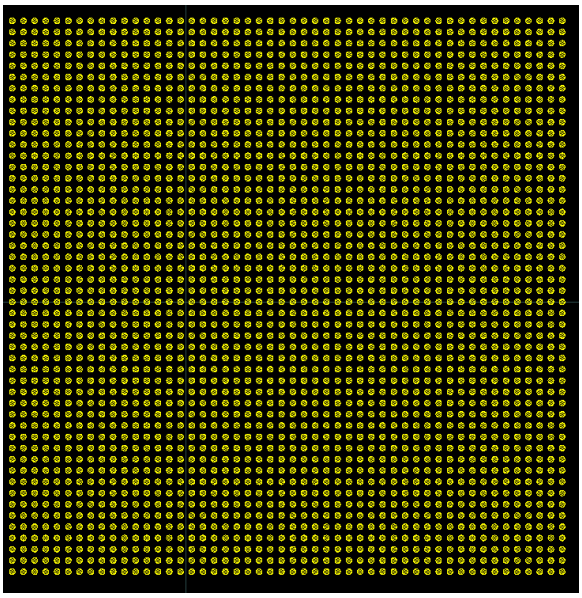

Figure A.16: ADS layout for the electroplated pads that are on the base metal.

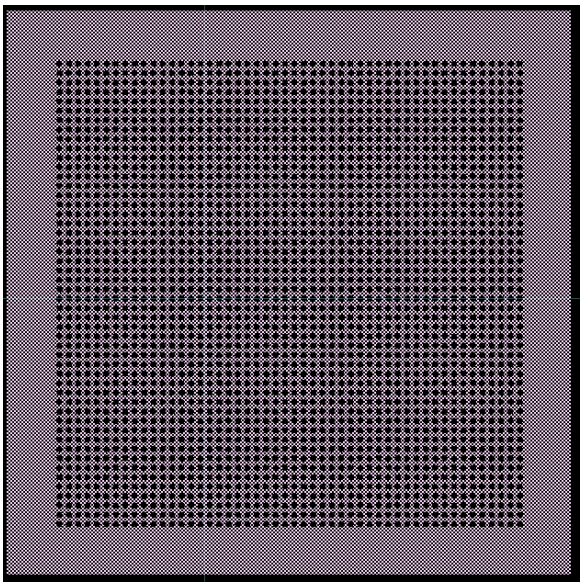

Figure A.17: ADS layout for the AL-X layer that electrically isolates adjacent pads.

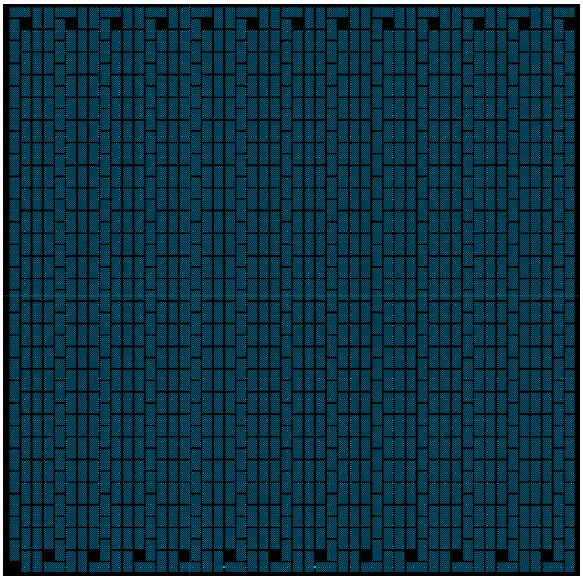

Figure A.18: ADS layout for the first metal layer on the top chip. The base metal complements the snake and comb of the bottom metal layer.

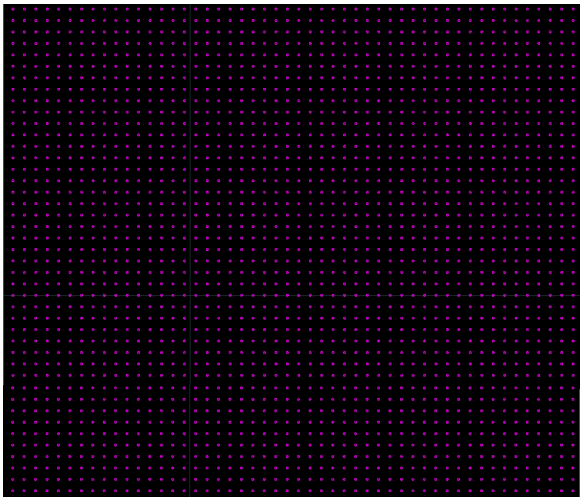

Figure A.19: ADS layout for the top chip pins.

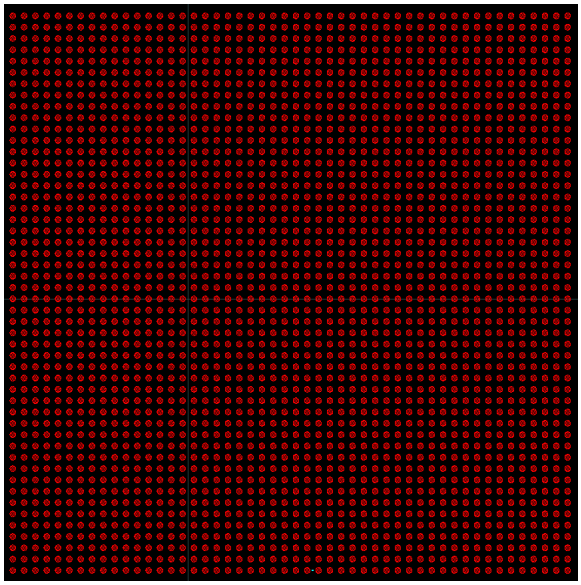

Figure A.20: ADS layout for the top via on the interposer. The via diameter is 100 μm

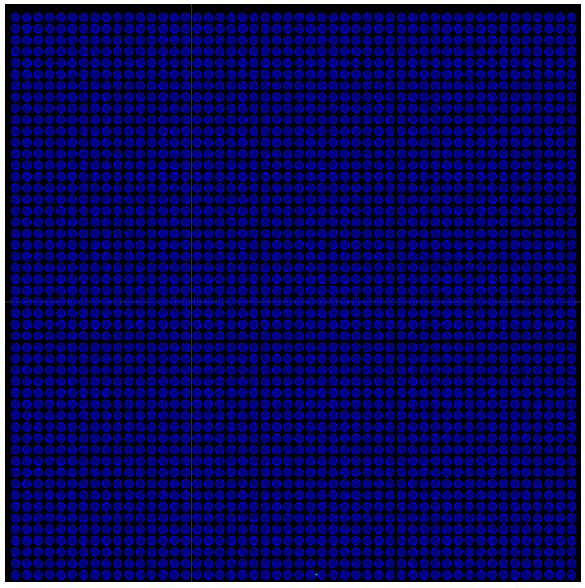

Figure A.21: ADS layout for the bottom via on the interposer. The via diameter is 150 μm

Appendix B

Traveler

Step No.	Process	Parameters	Remarks
		Snake and Comb Definition	
1	Oxidation	Two Hour Oxidation in Pyrogenic Steam at 1000°C	Profile: George120
2	Dehydration Bake	Dehydration Oven at 120°C for 30 minutes	Skip if wafers just came out the furnace
3	HMDS Coat	Place in HMDS beaker for 10 minutes	HMDS is found in an amber bottle
4	Spin Coat	PR: AZ9245 settings: 1. 1700 RPM t=5s @ 500 RPM/s 2. 2200 RPM @ 1000 RPM/s t=25s	Expected thickness: ~ 5 μm
5	Soft Bake	Temp of hotplate: T=110°C 1. Hold wafer above hotplate for 10 seconds 2. Put on hotplate for 90 seconds	
6	Mask Alignment	Exposure time: 12 seconds Alignment gap: 25μm	Mask: substrate_snake_comb
7	Development	3:1 DI Water: AZ 400k. Agitate solution prior to placing wafer in solution. Rinse in DI water and N_2 blow dry	Develop for 2 mins. Ratio: 150 mL of DI water, 50 mL Developer
8	Plasma Descum	150 W for 30 seconds. Repeat twice.	
9	PR Thickness	Use Profilometer and measure across a pad	Thickness:
10	Metal Deposition	2 Minutes ion milling. 1. 1000 Å Ti 2. 2000 Å Cu Deposition rate: 2 Å/s	
11	Lift-Off	Place wafers into acetone bath over night. Sonicate in acetone the next-day to assist in lift-off	
12	Surface Clean	Rinse in Methanol, Isopropanol and DI water	Verify all PR is gone
13	Metal Thickness	Measure on profilometer across a pad	Thickness:
		Cu Via Definition	
14	Seed Layer	2 Minutes ion milling. 1. 1000 Å Ti 2. 2000 Å Cu	Deposition rate: 4Å/s
15	Dehydration Bake	Dehydration Oven at 120°C for 30 minutes	
16	HMDS Coat	Place in HMDS beaker for 10 minutes	HMDS is found in an amber bottle
17	Spin Coat	PR: AZ9245 settings: 1. 1700 RPM t=5s @ 500 RPM/s 2. 2200 RPM @ 1000 RPM/s t=25s	Expected thickness: ~ 5 μm
18	Soft Bake	Temp of hotplate: T=110°C 1. Hold wafer above hotplate for 10 seconds 2. Put on hotplate for 90 seconds	
19	Mask Alignment	Exposure time: 12 seconds Alignment gap: 25μm	Mask: substrate_via
20	Development	3:1 DI Water: AZ 400k. Agitate solution prior to placing wafer in solution. Rinse in DI water and N_2 blow dry	Develop for 2 mins. Ratio: 150 mL of DI water, 50 mL Developer
21	Plasma Descum	150 W for 30 seconds. Repeat twice.	
22	Cu Oxide removal	2% Hydrochloric (HCl) acid for 10 seconds	100 mL H_2O : 2 mL HCl

Step No.	Process	Parameters	Remarks
23	Cu Electroplating	Current = 40 mA for 40 mins.	Expected thickness $\sim$ 3 μm
24	PR Removal	Place wafers in Acetone and agitate untill all the PR is gone Follow with Methanol, and Water rinse. N_2 blow dry.	
25	Cu seed layer removal	Solution of: 1 Acetic Acid:1 Hydrogen Peroxide: 18 Water 10 mL Hydroge Peroxide 10 mL Acetic Acid 180 mL H_2O	
26	Ti seed layer removal	Place in Buffered Oxide Etchant Rinse in DI water for 2 minutes and N_2 blow dry.	Etch time: $\sim$ 2-3 mins.
		AL-X Application	
27	Dehydration Bake	Dehydration Oven at 120°C for 30 minutes	
28	Adhesion Promoter	AP903 -Spin speed: 2500 RPM @ 1000 RPM/s time = 30s.	
29	Soft Bake	Hot plate @ 100 °C for 90 seconds	
30	Spin Coat	AL-X-2010 settings: 1. 500 RPM t=5s @ 500 RPM/s 2. 3000 RPM @ 1000 RPM/s t=30s 3. Dispense (PS-201) EBR at edge of wafer speed: 1. 500 RPM t=20s @ 500 RPM/s	Expected thickness: $\sim$ 5 μm
31	Soft Bake	Hot plate @ 60 °C for 90 seconds	
32	Mask Alignment	Exposure time: 20 seconds Proximity Exp. gap: 25μm	Mask: substrate_ALX
33	Development	1. Dispense PS-201 @ 200 RPM, t=10s. 2. Dwell for 10 secs. 3. Dispense PS-201 @ 200 RPM, t=10s. 4. Dwell for 10 secs. 5. Dispense PS-201 @ 500 RPM, @ t=10s. 6. Spin @ 2000 RPM, t=30s.	Ramp rates are: 500 RPM/s

Table B.1: Bottom Wafer Process Flow with AL-X

Step No.	Process	Parameters	Remarks
		Snake and Comb Definition	
1	Oxidation	Two Hour Oxidation in Pyrogenic Steam at 1000°C	Profile: George120
2	Dehydration Bake	Dehydration Oven at 120°C for 30 minutes	Skip if wafers just came out the furnace
3	HMDS Coat	Place in HMDS beaker for 10 minutes	HMDS is found in an amber bottle
4	Spin Coat	PR: AZ9245 settings: 1. 1700 RPM t=5s @ 500 RPM/s 2. 2200 RPM @ 1000 RPM/s t=25s	Expected thickness: ~ 5 μm
5	Soft Bake	Temp of hotplate: T=110°C 1. Hold wafer above hotplate for 10 seconds 2. Put on hotplate for 90 seconds	
6	Mask Alignment	Exposure time: 12 seconds Alignment gap: 25μm	Mask: substrate_snake_comb
7	Development	3:1 DI Water: AZ 400k. Agitate solution prior to placing wafer in solution. Rinse in DI water and N_2 blow dry	Develop for 2 mins. Ratio: 150 mL of DI water, 50 mL Developer
8	Plasma Descum	150 W for 30 seconds. Repeat twice.	
9	PR Thickness	Use Profilometer and measure across a pad	Thickness:
10	Metal Deposition	2 Minutes ion milling. 1. 1000 Å Ti 2. 2000 Å Cu Deposition rate: 2 Å/s	
11	Lift-Off	Place wafers into acetone bath over night. Sonicate in acetone the next-day to assist in lift-off	
12	Surface Clean	Rinse in Methanol, Isopropanol and DI water	Verify all PR is gone
13	Metal Thickness	Measure on profilometer across a pad	Thickness:
		Cu Via Definition	
14	Seed Layer	2 Minutes ion milling. 1. 1000 Å Ti 2. 2000 Å Cu	Deposition rate: 4Å/s
15	Dehydration Bake	Dehydration Oven at 120°C for 30 minutes	
16	HMDS Coat	Place in HMDS beaker for 10 minutes	HMDS is found in an amber bottle
17	Spin Coat	PR: AZ9245 settings: 1. 1700 RPM t=5s @ 500 RPM/s 2. 2200 RPM @ 1000 RPM/s t=25s	Expected thickness: ~ 5 μm
18	Soft Bake	Temp of hotplate: T=110°C 1. Hold wafer above hotplate for 10 seconds 2. Put on hotplate for 90 seconds	
19	Mask Alignment	Exposure time: 12 seconds Alignment gap: 25μm	Mask: substrate_via
20	Development	3:1 DI Water: AZ 400k. Agitate solution prior to placing wafer in solution. Rinse in DI water and N_2 blow dry	Develop for 2 mins. Ratio: 150 mL of DI water, 50 mL Developer
21	Plasma Descum	150 W for 30 seconds. Repeat twice.	
22	Cu Oxide removal	2% Hydrochloric (HCl) acid for 10 seconds	100 mL H_2O : 2 mL HCl

Step No.	Process	Parameters	Remarks
23	Cu Electroplating	Current = 40 mA for 40 mins.	Expected thickness $\sim$ 3 μm
24	PR Removal	Place wafers in Acetone and agitate untill all the PR is gone Follow with Methanol, and Water rinse. N_2 blow dry.	
25	Cu seed layer removal	Solution of: 1 Acetic Acid:1 Hydrogen Peroxide: 18 Water 10 mL Hydroge Peroxide 10 mL Acetic Acid 180 mL H_2O	
26	Ti seed layer removal	Place in Buffered Oxide Etchant Rinse in DI water for 2 minutes and N_2 blow dry.	Etch time: $\sim$ 2-3 mins.

Table B.2: Bottom Wafer Process Flow

Step No.	Process	Parameters	Remarks
		Snake and Comb Definition	
1	Oxidation	Two Hour Oxidation in Pyrogenic Steam at 1000°C	Profile: George120
2	Dehydration Bake	Dehydration Oven at 120°C for 30 minutes	Skip if wafers just came out the furnace
3	HMDS Coat	Place in HMDS beaker for 10 minutes	HMDS is found in an amber bottle
4	Spin Coat	PR: AZ9245 settings: 1. 1700 RPM t=5s @ 500 RPM/s 2. 2200 RPM @ 1000 RPM/s t=25s	Expected thickness: ~ 5 μm
5	Soft Bake	Temp of hotplate: T=110°C 1. Hold wafer above hotplate for 10 seconds 2. 110° hotplate for 90 seconds	
6	Mask Alignment	Exposure time: 12 seconds Alignment gap: 25μm	Mask: chip_snake_comb
7	Development	3:1 DI Water: AZ 400k. Agitate solution prior to placing wafer in solution. Rinse in DI water and N_2 blow dry	Develop for 2 mins. Ratio: 150 mL of DI water, 50 mL Developer
8	Plasma Descum	150 W for 30 seconds. Repeat twice.	
9	PR Thickness	Use Profilometer and measure across a pad	Thickness:
10	Metal Deposition	2 Minutes ion milling. 1. 1000 Å Ti 2. 2000 Å Cu Depoistion rate: 2 Å/s	
11	Lift-Off	Place wafers into acetone bath over night. Sonicate in acetone the next-day to assist in lift-off	
12	Surface Clean	Rinse in Methanol, Isopropanol and DI water	Verify all PR is gone
13	Metal Thickness	Measure on profilometer across a pad	Thickness:
		Cu Pin Definition	
14	Seed Layer	2 Minutes ion milling. 1. 1000 Å Ti 2. 2000 Å Cu	Deposition rate 4Å/s
15	Dehydration Bake	Dehydration Oven at 120°C for 30 minutes	
16	Spin Coat	PR: AZ-125-NXT-10A settings: 1. Dynamic Dispense: 200 @ 500 RPM/s RPM t=30s 2. Spread: 600 RPM @ 500 RPM/s t=25s 3. EBR: 300 RPM @ 500 RPM/s (1.5 mL EBR) t=20s	
17	Soft Bake	Put in 135°C Oven t=35 mins. Let it sit out for 12 hours	
18	Mask Alignment	Exposure time: 60 seconds w/a 30 sec. wait $\times$ 5 WEC Type: Proximity, Contact: Spacer Al. gap: 170μm Exp. gap: 150 μm	Mask: chip_pin
19	Development	AZ 300 MIF Agitate solution prior to placing in wafer	Develop for 4 minutes
20	Plasma Descum	150 W for 30 seconds. Repeat twice.	
21	Cu Oxide removal	2% Hydrochloric (HCl) acid for 10 seconds	100 mL H_2O : 2 mL HCl

Step No.	Process	Parameters	Remarks
21	Cu Electroplating	Current = 20 mA for 320 mins.	Expected thickness $\sim$ 100 μm
22	PR Removal	Place wafers in Acetone and agitate untill all the PR is gone. Follow with Methanol, and Water rinse. N_2 blow dry.	
23	Cu seed layer removal	Solution of: 1 Acetic Acid:1 Hydrogen Peroxide: 18 Water 10mL Acetic Acid 10 mL Hydroge Peroxide 180 mL H_2O	
24	Ti seed layer removal	Place in Buffered Oxide Etchant Rinse in DI water for 2 minutes and N_2 blow dry.	Etch time: $\sim$ 2-3 mins.

Table B.3: Top Wafer Process Flow

Step No.	Process	Parameters	Remarks
		Top via etch: 50μm deep	
1	Dehydration Bake	Dehydration Oven at 120°C for 30 minutes	Skip if wafers just came out the furnace
2	HMDS Coat	Place in HMDS beaker for 10 minutes	HMDS is found in an amber bottle
3	Spin Coat	PR: AZ5214 settings: 1. 1000 RPM t=30s @ 1000 RPM/s	
4	Soft Bake	Temp of hotplate: T=110°C 1. Hold wafer above hotplate for 10 seconds 2. Put on hotplate for 90 seconds	
5	Mask Alignment	Exposure time: 10 seconds Alignment gap: 25μm	Mask: interposer_top_hole
6	Development	3:1 DI Water: AZ 400k. Agitate solution prior to placing wafer in solution. Rinse in DI water and N_2 blow dry	Develop for 2 mins. Ratio: 150 mL of DI water, 50 mL Developer
7	Plasma Descum	150 W for 30 seconds. Repeat twice.	
8	Post Bake	Temp of hotplate: T=120°C 1. Hold wafer above hotplate for 10 seconds 2. Put on hotplate for 60 seconds	
9	PR Thickness	Measure photoresist thickness across different locations	PR thickness:
10	Top Via Etch	STS Etcher Profile: Army New etch rate: .8 μm/cycle. Run profile for 63 cycles	Measure Via depth:
11	PR Removal	Rinse in Acetone, Methanol, Isopropanol and DI water	Verify all PR is gone
		Bottom via etch : 150 μm deep	
12	Dehydration Bake	Dehydration Oven at 120°C for 30 minutes	
13	HMDS Coat	Place in HMDS beaker for 10 minutes	HMDS is found in an amber bottle
14	Spin Coat	PR: P4620 t=60s settings: 1.4000 RPM t=30s @ 500 RPM/s	
15	Soft Bake	Temp of hotplate: T=110°C 1. Hold wafer above hotplate for 10 seconds 2. Put on hotplate for 120 seconds. T=110°C	
16	Mask Alignment	Exposure time: 8 seconds Alignment gap: 25μm	Mask:interposer_bottom
17	Development	3:1 DI Water: AZ 400k. Agitate solution prior to placing wafer in solution. Rinse in DI water and N_2 blow dry Ratio: 150 mL of DI water, 50 mL Developer	2 minute development time
18	Plasma Descum	150 W for 30 seconds. Repeat twice.	

Step No.	Process	Parameters	Remarks
19	Bottom via etch	Etch for 500 cycles	
20	PR Removal	Rinse in Acetone, Methanol, Isopropanol and DI water	Verify all PR is gone

Table B.4: Interposer Process Flow

Appendix C

Plating Solution Chemistry and Copper Etchant Recipe

Chemical Symbol	Chemical Name	Ratio	Amount for 2L
H_2O	Water	-	Fill up to 1000 mL of Water
$CuSO_4 \cdot 5H_2O$	Copper Sulfate Pentahydrate	60 grams/L	120 grams
H_2SO_4	Sulfuric Acid	56 mL/L	112 L
HCl	Hydrochloric Acid	(1/10) ratio in water	10 mL Water: 1 mL of HCL. Transfer 4 mL of solution
	SC MD (Brightener)	8 mL/L	16 mL
	SC Lo 70/30 (Suppressor)	2 mL/L	4 mL
H_2O	Water	-	Fill with water up-untill 2000mL

Table C.1: Redistribution Layer (RDL) Plating Solution Chemistry

Chemical Symbol	Chemical Name	Typical Amount
H_2O	Water	180 mL
$C_2H_4SO_4$	Acetic acid	10 mL
2(HO)	Hydrogen Peroxide	10 mL

Table C.2: Copper Seed Layer Etchant