Low Phase Noise Voltage-Controlled Oscillators for Wide-Band Frequency Synthesis

by

Hechen Wang

A thesis submitted to the Graduate Faculty of
Auburn University
in partial fulfillment of the
requirements for the Degree of
Master of Science

Auburn, Alabama
December 14, 2013

Keywords: voltage-controlled oscillators (VCO), wide-band, phase noise, capacitor array, Gilbert mixer

Approved by

Fa Foster Dai, Chair, Professor of Electrical and Computer Engineering
Bogdan M. Wilamowski, Co-Chair, Professor of Electrical and Computer Engineering
Michael Hamilton, Assistant Professor of Electrical and Computer Engineering

Abstract

Noise-bandwidth trade-off is a challenge issue in modern voltage-controlled oscillator (VCO) designs. Wide-tuning VCOs usually suffer degraded phase noise. A mixer based tuning range enhancement technology is proposed in this thesis that allows a VCO to be able to generate wideband frequency tuning in the range from 2.4GHz to 8.4GHz without penalizing its phase noise. The wide tuning is achieved by covering three frequency bands centered at 2.5GHz, 5GHz and 7.5GHz, respectively, in which each band obtains 15.4% tuning range. Using the proposed mixer based frequency generation technique, tuning range of the frequency synthesizer can be significantly increased while the phase noise is controlled within a reasonable range.

To achieve good phase noise performance, a VCO should be biased at constant current that is compensated against temperature and supply voltage variations. A bandgap reference (BGR) circuit with the 2^{nd} order temperature-coefficient compensation as well as the power supply rejection is thus developed.

The VCO radio frequency integrated circuit (RFIC) was implemented in a 0.18 μm SiGe BiCMOS technology. Measured results from the wideband VCO prototypes demonstrate the wide tuning range capability as well as the low phase noise. The phase noise of the proposed VCO was measured as -124.4dBc/Hz, -119.1dBc/Hz and -108.8dBc/Hz at 1 MHz offset, respectively.

Acknowledgments

The work presented in this thesis could not have happened without the help and support of many people.

I'd like to start by thanking my advisor Doctor Fa Foster Dai. He has been a constant motivating force and positive influence on the work that is presented in this thesis. I have learned a phenomenal amount over the last one and a half year, and owe much of my education to Dr. Dai's personal tutelage.

I would like to thank my co-advisor Doctor Bogdan M. Wilamowski and for his constant motivation and guidance. This work would not have been possible without his constant encouragement and support.

I owe my committee, Doctor Michael Hamilton a debt of gratitude for taking the time to meet with me during the course of this work, and for reading this thesis.

My colleagues in my group provided a great deal of technical assistance, and also enriched my experience with their friendships.

I would like to thank my parents, Hong Wang and Hongyan Wang, for their love, support, and encouragement through these many years of graduate school.

Table of Contents

List of Figures

List of Abbreviations

VCO	Voltage-Controlled Oscillator
QVCO	Quadrature Voltage-Controlled Oscillator
RF	Radio Frequency
BGR	Bandgap Reference
BJT	Bipolar Junction Transistor
TC	Temperature Coefficient

Chapter 1

Introduction

1.1 Background and Motivation

The use of wireless products has been rapidly increasing all these years. In order to meet consumer's demand, designers are trying to place different application modules into mobile terminal device. Multi-standard is required to avoid the interference of various wireless communications. For each standard, the carrier frequency is located at individual frequency band within the radio communication spectrum (3 kHz to 300 GHz) [1]. Traditional approach is to arrange different local oscillator for each standard which is not meet nowadays dominant design criteria, characteristics such as low power consumption, small size, and low cost.

As a result, wide band voltage control oscillator is one of the suitable answers to those demands.

1.2 Area of Focus

Voltage control oscillator is one of the most important parts in frequency

synthesis design. And VCO's performance directly affects the frequency synthesis output quality. For multi-standard design, tuning range of the VCO is the key indicator. This paper will present several ways to increase the tuning range

Phase noise is another important characteristic in VCO design. Traditionally, there is a trade-off between tuning rang and phase noise by using varactors. Capacitor array and mixer based frequency doubler and tripler are used in this work to resolve the dilemma.

To further improve the performance a bandgap reference circuit with higher order temperature coefficient compensation and power supply rejection technique is designed to shield the VCO operation environment from temperature variation and interference on the power supply.

1.3 Organiztion of Thesis

The remaining chapters in this thesis provide further analysis, implementation details and testing (simulation) results. They are organized into four chapters. Chapter 2 presents the VCO fundamental principles. Chapter 3 analyzes several VCO performance improvement techniques. In Chapter 4 focuses on wide band low phase noise VCO design, including method analyzing, prototype circuit designs and testing results. In Chapter 5 an approach to introduce 2^{nd} order temperature coefficient is adopted to basic bandgap reference and a power supply rejection improvement technique is presented. The last Chapter draws conclusions describing the overall design of the prototype.

Chapter 2

Fundamentals of Oscillator Designs

Most of the wireless communication systems need an appropriate frequency reference to operate. Oscillators play a critical role in this area, providing the periodic signals needed for frequency conversion.

In the front-end of a typical receiver, the antenna output is amplified by a low noise amplifier (LNA), and then mixed with a local oscillator (LO). The mixing process translates the modulated radio frequency (RF) signal to a lower intermediate frequency (IF). Normally, the IF frequency is fixed in a certain communication system, which is $\boldsymbol{IF = f_{RF} - f_{LO}}$ (assuming a low-side LO is being used).

To achieve the high-accuracy requirement, phase-locked loop (PLL) is adopted commonly. Using negative feedback, PLL frequency synthesizer has the ability to precisely detect the phase of an incoming signal within a certain bandwidth while simultaneously scaling its frequency. A typical analog PLL circuit diagram is showing below. The PLL consists of a phase-frequency detector (PFD), charge-pump (CP), loop filter (LF), voltage controlled oscillator (VCO) and divider.

Voltage controlled oscillator (VCO) is the key element of the PLL and it has a huge impact on its overall performance. In particular, VCO employed in PLL must meet stringent phase noise requirements, caused by the priority contribution of PLL out band noise. And with the intention of cover RF signal's bandwidth, VCO should have a certain tuning range, especially for multi-standard system.

2.1 Oscillator Types

There are different oscillator types for specific applications to meet their different requirements. Crystal oscillator, LC-tank oscillator and ring oscillator is three commonly used oscillators.

Crystal oscillators are often used for low noise frequency synthesis at MHz frequency ranges. Due to the extremely high quality factor, crystal oscillators can provide excellent frequency stability with extremely low noise phase. However, this type of oscillators has limited output frequency and tuning range, and is not suitable for integration, which forced them to be used off-chip for most of the RF applications.

Although ring oscillator and LC-tank oscillator can both operate at high frequency, due to the structure difference, their performance has great discrepancy, and used in different applications.

2.1.1 Ring Based Oscillator

A ring oscillator is a device composed of an greater than three odd number of inverters(even number is acceptable if differential inverter is adopted). The inverters, are attached in a chain, and the output of the last inverter cell is feedback into the first

cell. The frequency of oscillation becomes $1/2n\tau$, where n is the number of inverter cells, and τ is the delay due to each cell.

By adjusting the delay of each inverter cell (changing supply voltage or capacitor value), ring oscillator can achieved a large tuning range easily. And without employ integreted passive inductors and capacitors, they occupy much smaller layout area compare to LC-tank oscillators. However, not including resonance restriction in the feedback loop, phase noise performance of this kind of oscillators cannot satisfy the RF communication requirement. Most common application field for ring oscillator is in digital circuits to establish clock reference for logic blocks.

2.1.2 LC Based Oscillator

With the LC-tank restriction, LC based VCO exhibits superior phase noise performance judge against to ring oscillator. Thus, this work focuses on resonator-based or LC VCOs. The following sections will introduce the basic concept of LC based oscillator.

2.2 LC Based Oscillator Models

2.2.1 LC Tank Basics

An LC circuit, also referred as resonant circuit, or LC-tank circuit, generally constructs of an inductor, represented by the letter L, and a capacitor, represented by the letter C, in series or in parallel. One or more resistive components are often included for modeling the resonator losses. When connected together, they act as an electrical resonator, storing and giving off energy oscillating at its resonant frequency.

An idealized LC circuit contains no resistance which means there is no energy dissipation in the tank. However, any practical implementation of an LC circuit will include loss resulting from non-zero resistance within the components and connecting wires, especially in the case involving integrated components. Thus, in the simplest case, LC tanks are represented as series or parallel RLC networks. The tank impedances of the networks are:

$$\boldsymbol{Z = \frac{1}{1/R + j(\omega C - 1/\omega L)}} \tag{2.1a}$$

$$\boldsymbol{Z = R + j(\omega L - 1/\omega C)} \tag{2.1b}$$

For a certain case, the reactive terms in (2.1) cancel out at one frequency, called the resonance frequency:

$$\boldsymbol{\omega_0 = \frac{1}{\sqrt{LC}}} \tag{2.2}$$

At $\boldsymbol{\omega_0}$, the tank impedance is purely resistive and is equal to R, and the phase of the impedance response is exactly zero. For series RLC networks, this scenario is exactly opposite. Hence, the parallel and series RLC are the dual of each other.

LC-tanks are used either for producing signals at a particular frequency in a positive feedback loop, or picking out a signal at a certain frequency from a multi-tune signal. They are widely used in many signal processing electronic devices, particularly radio frequency communication equipment, used in circuits such as oscillators, filters, tuners and mixers [4].

2.2.2 Devices for LC VCO and Parasitics

Since there always contains resistance in the LC-tank, the quality factor, or Q

factor, is raised to indicate the loss in an oscillator or resonator, or equivalently, characterizes a resonator's bandwidth relative to its center frequency. By definition, the Q of a network is defined as:

$$Q = \omega \frac{Energy\ stored}{Average\ power\ dissipated} \tag{2.3}$$

The Q factor can approximate to the following equation:

$$Q = \frac{f_r}{\Delta f} = \frac{f_\omega}{\Delta \omega} \tag{2.4}$$

where f_r is the central resonant frequency, Δf is the 3dB (half-power) bandwidth. From this definition, we can observe that there is a trade-off between spectrum purity and system bandwidth. The LC-tank that you want to build a wide bandwidth filter is not suitable for high performance VCO design.

In an ideal series RLC circuit, the Q factor is:

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}} = \frac{\omega_0 L}{R} \tag{2.5}$$

for a parallel RLC circuit, the Q factor is the inverse of the series case:

$$Q = R\sqrt{\frac{C}{L}} = \frac{R}{\omega_0 L} \tag{2.6}$$

Q factor is a very important quantity because it often determines the phase noise performance of LC VCOs.

2.2.3 Oscillation Theorem

Since every LC resonator contains resistance, energy store in the tank will soon dissipate through the resistor. In order to maintain the oscillation, adding negative

resistance through a positive feedback to resonator is needed.

Every LC oscillator can be treated as a feedback network as shown Fig. 2.1. And there are some criteria must be fulfilled in order for the system acting as an oscillator.

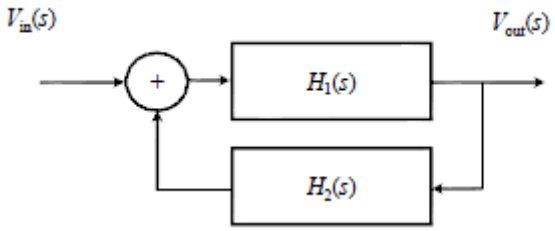


Figure 2.1. Block diagram of a basic oscillator.

In the block diagram, H1(s) represents an amplifier and H2(s) represents a feedback network that is fed the signal from the output of the amplifier to its input. The transfer function for this system is:

$$\frac{\boldsymbol{V_{out}(s)}}{\boldsymbol{V_{in}(s)}} = \frac{\boldsymbol{H_1(s)}}{\boldsymbol{1 - H_1(s)H_2(s)}} \tag{2.7}$$

The above equation indicates that the system will oscillate when denominator approaches to zero, in other words, the open-loop gain should larger or equal to 1, which is:

$$\boldsymbol{H_1(j\omega)H_2(j\omega) = 1} \tag{2.8}$$

This condition often further divides into two sections, magnitude criterion and phase criterion, which is commonly referred as *Barkhausen Criterion*.

The magnitude criterion for oscillation states that the gain of the oscillator loop must equal to 1. In practice, the loop gain has to be greater than one for the oscillator to startup and for the oscillation amplitude to grow. The amplitude will eventually be saturated due to the device nonlinearity. Reducing the open loop gain to one, one can

obtain the minimum gain required for starting oscillation, namely,

$$|\boldsymbol{H_1(j\omega)||H_2(j\omega)| = 1.}$$

(2.9)

The phase criterion for oscillation states that the phase shift of the oscillator loop must be a multiple of 2π, namely,

$$\boldsymbol{\angle H_1(j\omega)\angle H_2(j\omega) = 2n\pi,}$$

(2.10)

where n is an integer. This means that signals at a certain point in the oscillator are summed with the same place. If the phase shift were to be an odd multiple of π, the signals would have opposite phases and cancel each other.

2.2.4 VCO Topologies

Considering the above oscillation principle, an active circuit is attached to the LC-tank as shown in Fig. 2.2, where Q1 is a bipolar transistor that produces trans-conductance to generate the needed negative impedance for oscillation. A feedback circuit is added between the output and the input of the oscillator.

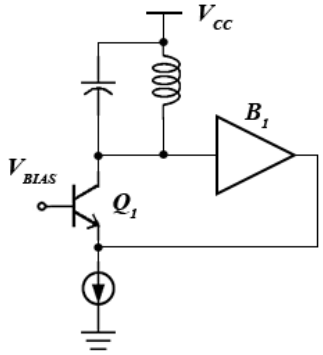


Figure 2.2. LC-tank oscillator.

A straightforward topology able to do this is the following circuit known as Colpitts oscillator. The transistor associates with capacitor feedback path establishing the negative resistance.

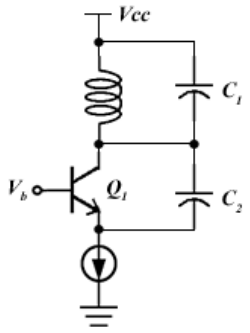


Figure 2.3. Colpitts oscillator.

In its simplest form, the transistor emitter is connected to the junction between C1 and C2. The total effective capacitance shunting the tank inductor is:

$$C_{eff} = \frac{C_1 C_2}{C_1 + C_2} \tag{2.11}$$

and the circuit will oscillate at a frequency:

$$f_0 = \frac{1}{2\pi\sqrt{LC_{eff}}} \tag{2.12}$$

Cross-coupled oscillator is another commonly adopted topology. The partial circuit is shown Fig. 2.4. The feedback loop is established by an emitter follower. Then twisting the circuit into a reciprocal topology forms a cross-coupled oscillator.

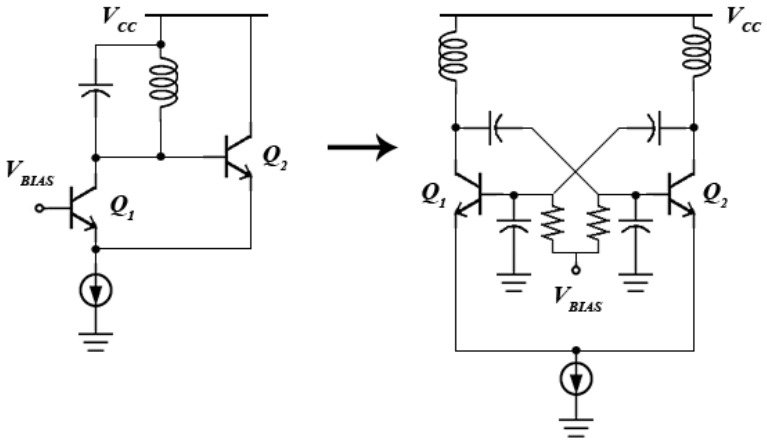


Figure 2.4. Cross-coupled oscillator.

2.3 Issues in LC VCO Design

2.3.1 Phase Noise

Ideally, the spectrum of an oscillator is an impulse located at a single frequency. Whereas for an actual oscillator, the spectrum exhibits “skirts” around the center or “carrier”. This undesirable power distribution around the center oscillation frequency is known as phase noise. To quantify phase noise, we consider a unit bandwidth at an offset $\Delta\omega$ with respect to ω_0, calculate the noise power in this bandwidth, and divide the result by the carrier power.

To understand the negative effect of phase noise, consider a generic receiver as depicted in Fig. 2.5 where the receiver consists of a low noise amplifier, a band-pass filter, and a down-conversion mixer. The local oscillator (LO) providing the carrier signal for mixer is embedded in a frequency synthesizer.

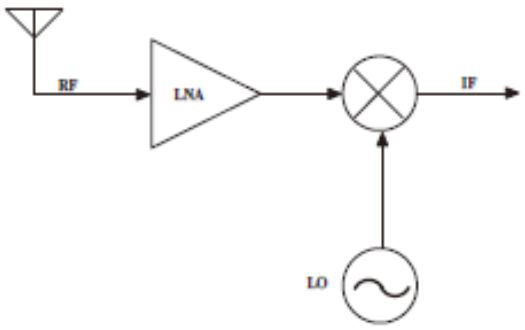


Figure 2.5. Block diagram of a typical receiver front-end.

As shown in Fig. 2.5, when trying to receive a signal in one channel in the presence of a stronger signal in an adjacent channel, consider as interference. In ideal case, the signal band of interest is convolved with an impulse and thus translated to a lower frequency with no change in its shape and the frequency difference between these two tones remains the same as it in RF band.

In reality, however, LO always contains phase noise. When the two signals are mixed with the LO, the IF band consists of two overlapping spectra, with the wanted signal suffering from significant noise due to the interference, thereby reducing the signal-to-noise ratio (SNR) of the desired signal at IF. This phenomenon is often referred to as reciprocal mixing, and limits how close together channels can be placed. Similarly, in a transmitter, LO phase noise is modulated onto the desired signal, resulting in unwanted energy being transmitted outside of the desired band.

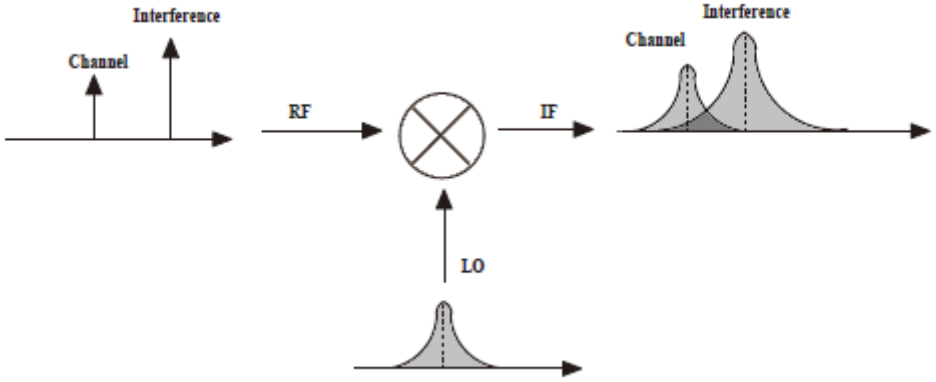


Figure 2.6. Phase noise effect in frequency conversion.

2.3.2 Tuning Range

Most of wireless communication standards contain several frequency channels within a certain bandwidth. To cover all these channels, a tunable oscillator is required, which means the output frequency is a function of a control input, usually a voltage signal. An ideal VCO is a circuit whose output frequency is a linear function of its control voltage as shown in Fig. 2.7

$$f_{out} = f_0 + K_{VCO}V_{con} \tag{2.13}$$

In the expression, f_0 is the oscillation frequency at $V_{con} = 0$ and K_{VCO}

represent the gain or sensitivity of the VCO circuit. The achievable adjusting range, $f_2 - f_1$ is called the VCO's frequency tuning range.

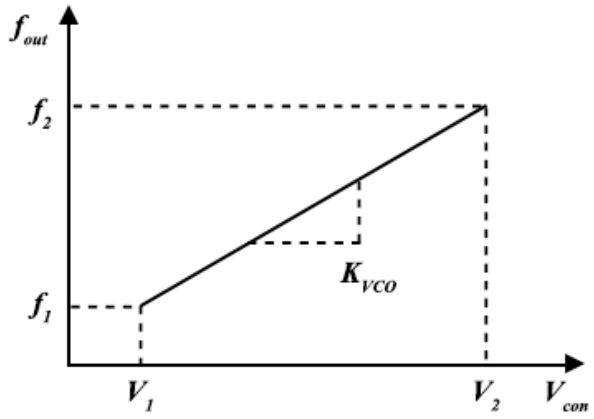


Figure 2.7. VCO tuning gain.

Frequency tuning is required not only to cover the whole application bandwidth but also to compensate for variations of the center frequency of the VCO that are caused by the process, voltage and temperature variation. The oscillation frequency of an LC-tank VCO is approximately equal to $f_{VCO} = 1/2\pi\sqrt{LC}$. In the equation, the inductor and capacitor values are the only two parameters can be varied to tune the oscillation frequency. Varactors are commonly used components for VCO design to adjust the capacitor value of the oscillation tank providing approximate linear voltage to frequency ratio.

Nowadays, due to the demands of multi-standard wireless communication, traditional tuning methods are no longer adequate. The requirement VCO's tuning range has been raised to an extreme level. Designers are putting more efforts to extend the bandwidth of frequency synthesizers to meet. Many novel approaches and techniques have been developed.

Chapter 3

Techniques for LC VCO Performance Improvement

Bandwidth and phase noise are two crucial parameters for VCO designs. The importance of these two parameters has been discussed in chapter 2. By following the traditional approaches, designers are facing a trade-off between VCO's bandwidth and phase noise. Since the requirement VCO's tuning range has been raised to a new level, this problem becomes more conspicuous these days.

This chapter focuses on the methods to improve VCO's performance. Several adopted techniques trying to increase bandwidth and optimize phase noise have presented in this chapter.

3.1 Techniques for Improving Tuning Range

The oscillation frequency is determined by the formula:

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{3.1}$$

which indicates that the way to adjust output frequency is nothing less than changing

the value of capacitor or inductor in the LC resonator. Generally, in practical, the variation of inductance is hard to implement with integrated components. Therefore designers put more attention on capacitance variation.

Three tuning range improvement methods adopted by this work are introduced in the following sections.

3.1.1 Varactor

Varactors used as voltage-controlled capacitors are reverse-biased p-n junctions. No current flows, but since the thickness of the depletion zone varies with the applied bias voltage, the capacitance of the diode can be made to vary.

Generally, the depletion region thickness is proportional to the square root of the applied voltage, and capacitance is inversely proportional to depletion region thickness. Thus, the capacitance is inversely proportional to the square root of applied voltage. This characteristic let it become the first choice for VCO design.

Despite having a modest maximum-to-minimum capacitance ratio (Cmax/Cmin) that worsens as the supply voltage scales, p-n junction varactors are adequate for applications with limited tuning needs. With proper layout techniques, the Q factor of varactor is acceptable as long as the junction is prevented from reaching its forward-biasing condition.

3.1.2 Capacitor Array

The trade-off between bandwidth and phase noise is mostly caused by the varactor. By using a larger varactor can achieve broader tuning range, however, Q factor of the resonator will degenerate simultaneously leading to a poor phase noise.

Moreover, larger varactor is more sensitive to amplitude fluctuations, which cause the AM-FM conversion of phase noise. As a result, enlarging varactor's dimension is unacceptable when the bandwidth requirement extends to a certain level.

To further increasing tuning range, instead of adjusting the value of one capacitor, we can change the number of capacitors parallel connected in resonator. Capacitor array is common in digitally controlled oscillator (DCO) design. It is controlled by several control bits, which can turn on or off switches to change the number of parallel connected capacitors in the oscillation resonator, thus varying oscillator output frequency.

Generally, there are two ways to arrange the capacitor array, binary weighted arrangement and thermometer or unary arrangement. Binary weighted arrangement selects the capacitor dimension ratio as a geometric sequence. It achieves larger tuning range, however, the large dimension difference between each capacitor turns out to inaccuracy. Relatively, thermometer arrangement is using identical capacitor dimension, more accurate, limited tuning range.

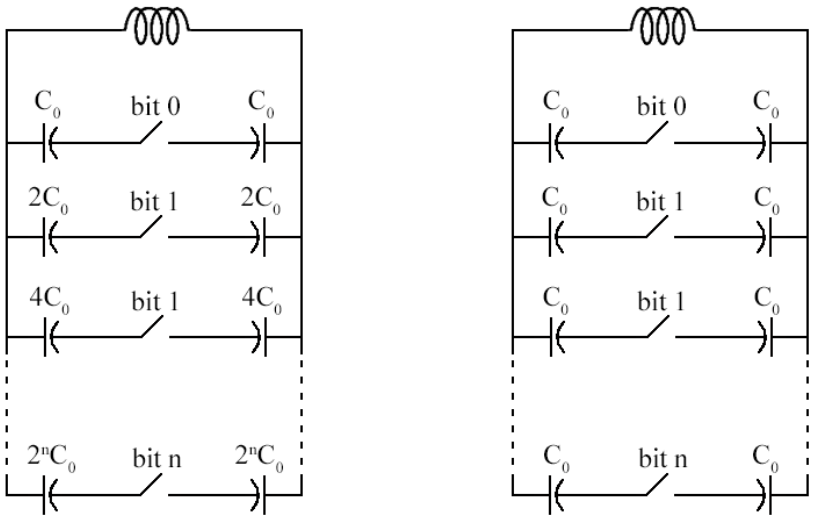


Figure 3.1. Two different capacitor array arrangements.

To ensure a symmetric operation environment for the resonator, each control bit connected with two identical dimension opposite placed capacitors. These two arrangement are presented in Fig 3.1 respectively.

Capacitor array can greatly change the capacitance in the LC resonator discretely. The combination of varactors and capacitor array leads to a continuous tuning range. The interval of capacitor array is covered by the varactor variation. To insure a continuous tuning range tuning bands are overlapped.

3.1.3 Mixer Based Frequency Doubler and Tripler

Although capacitor array can greatly increasing the tuning range, it still has limitation. Due to the capacitance nature, the dimension of integrated capacitor is hard to follow the scaling process. Transistors' critical dimension is shrinking over the years, while the capacitor size remains the same. Integrated capacitors consuming considerable area on chips, so it is extravagant to place large capacitor array on chip in today's semiconductor industry.

Multi-standard requires a bandwidth cover several gigahertz, which is unrealistic by simply using varactors and capacitor array. At this stage, traditional methods are inadequate to perform a good result, new topologies or techniques need to be used. Frequency multiplier is one of a choice.

Implemented with non-linearity circuits, frequency multiplier distorts the original signal and generates higher order harmonics of the signal. By extracting for instance the 2^{nd} or 3^{rd} order harmonics and suppressing unwanted signal through a bandpass filter, a frequency doubler or tripler is constructed, which is the most commonly used

multiplier in frequency synthesizers.

With frequency multiplier, the VCO's tuning range is greatly increased. However, the drawbacks are also obvious, additional active non-linear circuits consuming lots of power, and constructing bandpass filter requires passive elements, inductors and capacitors, which occupy tremendous on-chip area.

3.2 Techniques for Improving Phase Noise

The definition of phase noise is given by the following express:

$$\boldsymbol{L_{total}\{\Delta\omega\} = 10log\left[\frac{P_{sideband}(\omega_0 + \Delta\omega, 1Hz)}{P_{carrier}}\right]} \tag{3.2}$$

The equation indicating phase noise ($\mathcal{L}$ (f)) is typically expressed in units of dBc/Hz, and it represents the noise power relative to the carrier contained in a 1 Hz bandwidth centered at a certain offsets from the carrier.

To model VCO's phase noise, an empirical fitting formula is developed by D. B. Leeson [6] as

$$\boldsymbol{S_{VCO}\{\Delta f\} = 10log\left\{\frac{FkT}{2P_s}\left[1 + \left(\frac{f_0}{2\Delta f \cdot Q_L}\right)^2\right]\right\}\left[1 + \frac{f_c}{|\Delta f|}\right]} \tag{3.3}$$

In the equation, K is Boltzmann constant; T is absolute temperature; P is signal power; Q stands for tank loaded quality factor; and F is introduced model the noise factor of the circuit.

According to Leeson's equation, the oscillation amplitude and the Q factor of resonator are two important quantity directly related to the phase noise. As in the denominator, increasing those two quantities can lead to a better phase noise

performance.

3.2.1 Quality Factor of LC-Tank

The quality factor in an oscillation resonator is related to the parasitic resistance of inductors and capacitors. Capacitors' parasitic resistance is negligible compared with integrated inductors. Unlike discrete inductors, integrated inductors are implemented in one-dimensional plane. Suffering from substrate loss, limited dimension and fixed non-circular the Q factor is below 20 at gigahertz range in general.

Consequently, integrated inductor needs to be designed carefully to ensure an acceptable Q factor. Typical the foundry provided on-chip spiral inductor structures consist of multiple square or octagonal spiraling turns forming its coils. The top metal layer is generally preferred for its lower parasitic capacitance to the substrate, and thus higher self-resonance frequency. The number of coils needs to be limited, normally less than 3 turns, to reduce the resistance and avoiding other adverse effects. Enlarging coil width to reduce parasitic resistance and limiting interval to provide a similar environment are two experimental integrated inductor parameter settings to perform a reasonable Q factor.

3.2.2 Output Amplitude

Leeson's equation indicates that the signal power is inversely proportional to phase noise. Thus, increasing output amplitude can improve phase noise. Enlarging the current is one simple way to achieve better phase noise. However, blindly increasing current is not desirable when take power consumption into consideration.

Besides, oversized output amplitude will influence the bias of varactors in the resonator, which may lead to a negative impact on phase noise.

Chapter 4

Implementation of Mixer Based Quadrature LC VCO

Wireless communication receivers require multiple QVCOs in different frequencies with relatively low phase noise to achieve a high performance. LC-tank VCOs have a superior phase noise performance. However, they require bulky passive resonators and different frequency corresponding to different size of inductors and capacitors, which consume lots of area on the limited chip surface.

The combination of a low-frequency VCO and a frequency multiplier to achieve high frequency and wide bandwidth had been widely adopted for broadband PLL applications. In general, it will be a tradeoff between the tuning range and phase noise when design a VCO. A wide tuning range requires a large size of varactor, generally results in degradation of the quality factor of the LC-tank. However frequency multiplier can relieve this tradeoff. At low frequency range will become easier than that are operated at high frequency range. Diode varactors can have a wider tuning capability and a better quality factor when they are operating at comparatively low

frequencies. And a 2-bit band switch (capacitor array) is implemented in the QVCO to achieve a wider tuning range.

For the frequency multiplier design, a nonlinear differential amplifier, Gilbert cell mixer, has been proposed as a frequency tripler in this design, using the fundamental frequency and the signal of frequency doubler (2nd harmonic frequency obtained at the virtual ground of the QVCO differential cores).

The building block diagram of our proposal shows in Fig. 4.1. I/Q fundamental frequency generates by the QVCO core. The second harmonic frequency of the QVCO output frequency is obtained at the common node (differential virtual ground) of the cross-coupled differential pair.

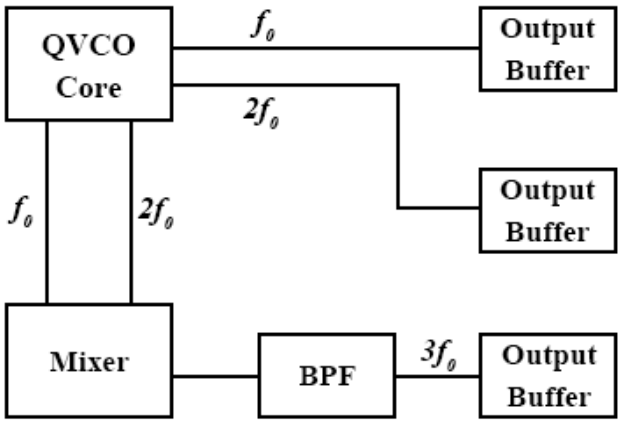


Figure 4.1. Proposed triple band frequency generation scheme.

By mixing the differential fundamental frequency signals ($\boldsymbol{f_{vco+}}$ and $\boldsymbol{f_{vco-}}$) with the second harmonic ($\boldsymbol{2f_{vco}}$), produce an upper frequency terms and a lower frequency term ($\boldsymbol{2f_{vco} \pm f_{vco}}$) at the output nodes of a BPF (band-pass filter) loaded differential mixer. The BPF load is formed by an inductor as well as two capacitors that peaks at frequency 3fvco and filters out other frequencies. By doing so, it accomplishes the desired frequency doubling and tripling.

4.1 Quadrature LC VCO Core Design

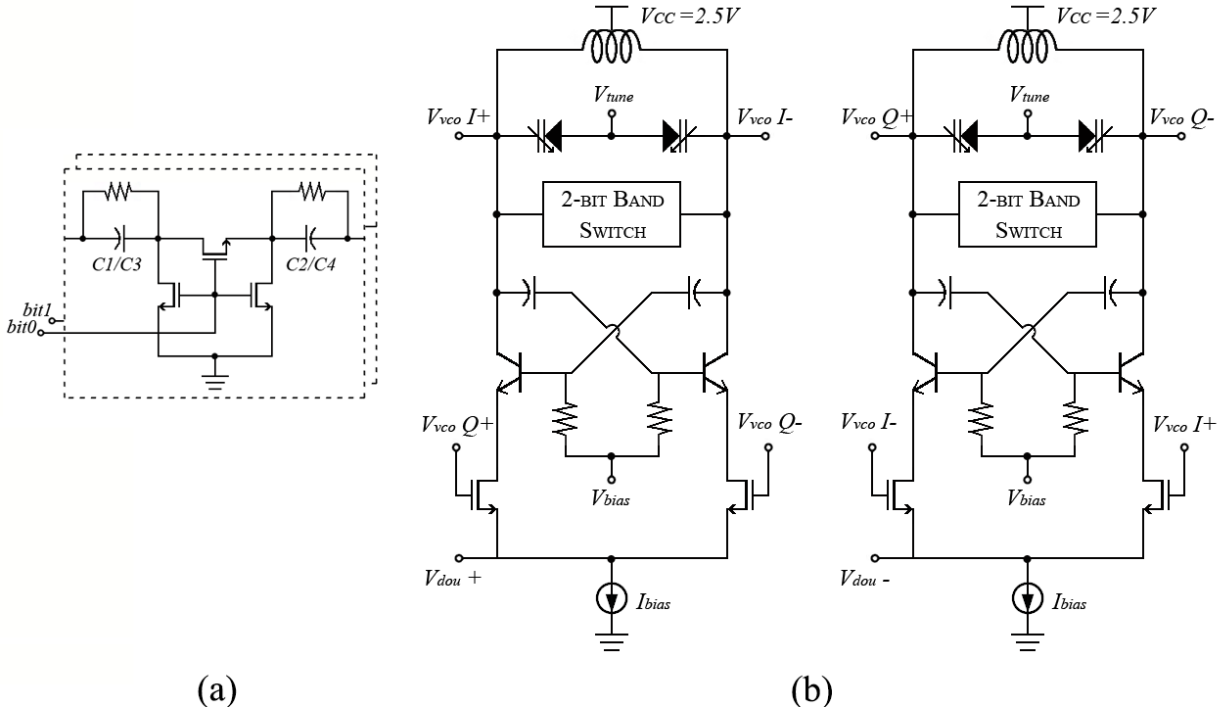


Figure 4.2. Proposed QVCO core. (a) 2-Bits sub-band switch. (b) BS-QVCO core.

4.1.1 Bottom-Series QVCO Core

The QVCO core shows in the Fig. 4.2(b), the main transistors are using BJT to obtain a better current efficiency. Larger the magnitude of the signal wave to improve the phase noise performance. A tradeoff between the magnitude and saturation region should be carefully concerned when settles the transistors' size ,the bias voltage and current. If the main transistors are operated in the saturation region, will introduce the noise to the LC-tank, and will directly impact the phase noise of VCO.

The resonant tank is build with a three turns differential inductor and two limited sized varactors to improve the phase noise performance. This work uses bottom-series MOSFET coupling (BS-QVCO) to achieve a relatively low phase noise with lower power consumption [7][8].

4.1.2. Sub-Band Switching

As mention before, the tradeoff between tuning range and phase noise dominate the size of the varactor, which means we cannot increasing VCO's tuning range by increasing the size of the varactor. In order to widen the tuning range without affecting the phase noise, this work introduced a 2-bit sub-band switch controlled capacitor array to the LC-tank core to change the resonant frequency instead of using a large varactor. The circuit is shown in Fig. 4.2(a).

The capacitor array is built by four capacitors. And the capacitance ratio is $(C_1 = C_2) : (C_3 = C_4) = 1 : 2$. Each bit contains two identical capacitors to compensate the PVT variations. In this way, we can get four different frequency bands. The size of these control MOSFET transistors is relatively large to reduce the parasitic resistance. The function of these resistors parallel with the capacitors is to prevent the p-n junction forward biasing.

4.2 Frequency Doubler and Tripler Design

To enlarge the VCO's range, the frequency doubler and tripler are adopted. By using non-linear circuits, higher order harmonics are generated from the fundamental signal. Through certain carefully designed filter, 2^{nd} and 3^{rd} order harmonics are picked to form frequency doubler and tripler respectively.

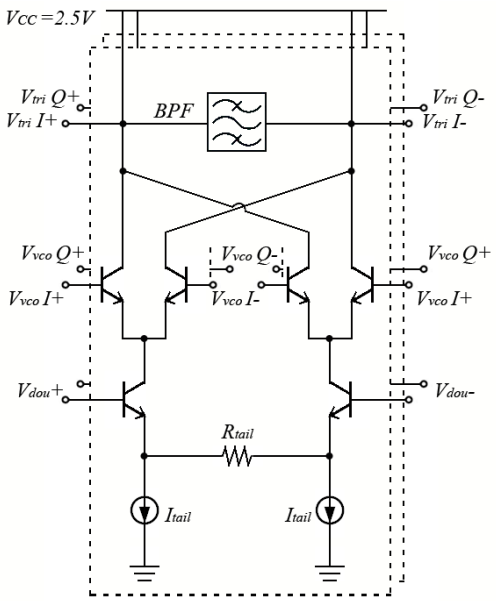
4.2.1 2nd Order Harmonic Extraction in Cross-Coupled VCO

The doubling frequency is obtain at the virtual ground of the differential pair which only cancels all the odd order's harmonics and the even order harmonics left.

Generally, using CMOS as the oscillation transistors, the signal at common mode is very weak. However, by using BJT transistors, which have less parasitic capacitors than MOSFET, as the main transistors we can have relatively strong signal coming from the common node. The amplitude of this node is 254mV or –5.95dBm based on the simulation result.

4.2.2 Frequency Tripler Mixer Design

About the tripling frequency, many designs are using single balanced mixer to construct the frequency multiplier [9], which is easy to build. However, when the frequency goes higher, the signal will leak through the substrate, and will corrupt the signal. The mixer may self mixing or mix with other unwanted signals and turn out to be undesired results.



(c)

Figure 4.3. Gilbert cell based frequency tripler.

In order to have a low noise and accurate I/Q tripling signal, a Gilbert mixing cell is introduced, which has a high common-mode rejection ratio can suppress the port

leakage. The two signals coming from the frequency doubler (common node of the QVCO) are differential signals, which just meet the Gilbert cells' differential inputs requirement. The doubling frequency mix with the quadrature phase fundamental frequencies will generate quadrature phase tripling frequencies.

$$3f_0\ I\ = cos(\omega t)\, cos(2\omega t) = cos(3\omega t) \tag{4.1}$$

$$3f_0\ Q = cos\left(\omega t + \frac{\pi}{2}\right) cos(2\omega t) = cos\left(3\omega t + \frac{\pi}{2}\right) \tag{4.2}$$

4.3 VCO Output Buffer Design

A 3-stage-buffer is implemented in this work to protect the LC-tank and increasing the loading capability. Without the buffer's protection, the outside variation can easily affect the LC-tank's parameter. Directly attaching the output nodes to the LC-tank also extracts current from the tank, which lowers the g_m and attenuates the signal power, and deteriorates the phase noise. The current biases of these stages are increasing stage by stage, to meet the measure condition. The first two stages are using MOSFET to properly shaping the waveform. The last stage is using BJT to have a better current efficiency. Fig 4.4 shows the circuit of the output buffer.

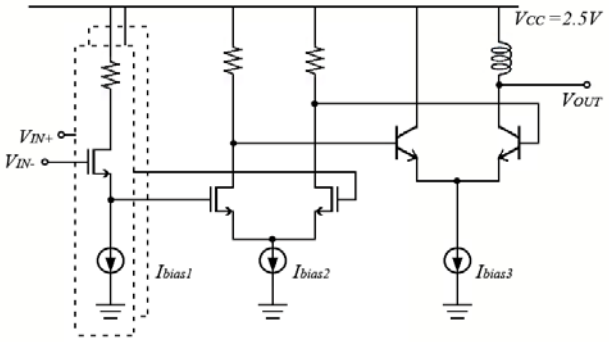


Figure 4.4. Output buffer circuit.

4.4 Experimental Results

The prototype is implemented in a 0.18μm SiGe BiCMOS process. The VCO core consumes 15mW with a 2.5V supply voltage and the frequency multiplier consumes 40mW. The Die photograph is shown below. In order to reduce the budget, this prototype is fabricated with another design aligned aside. The total prototype area including bond pads is 3.6m^2 inside the black dashed box.

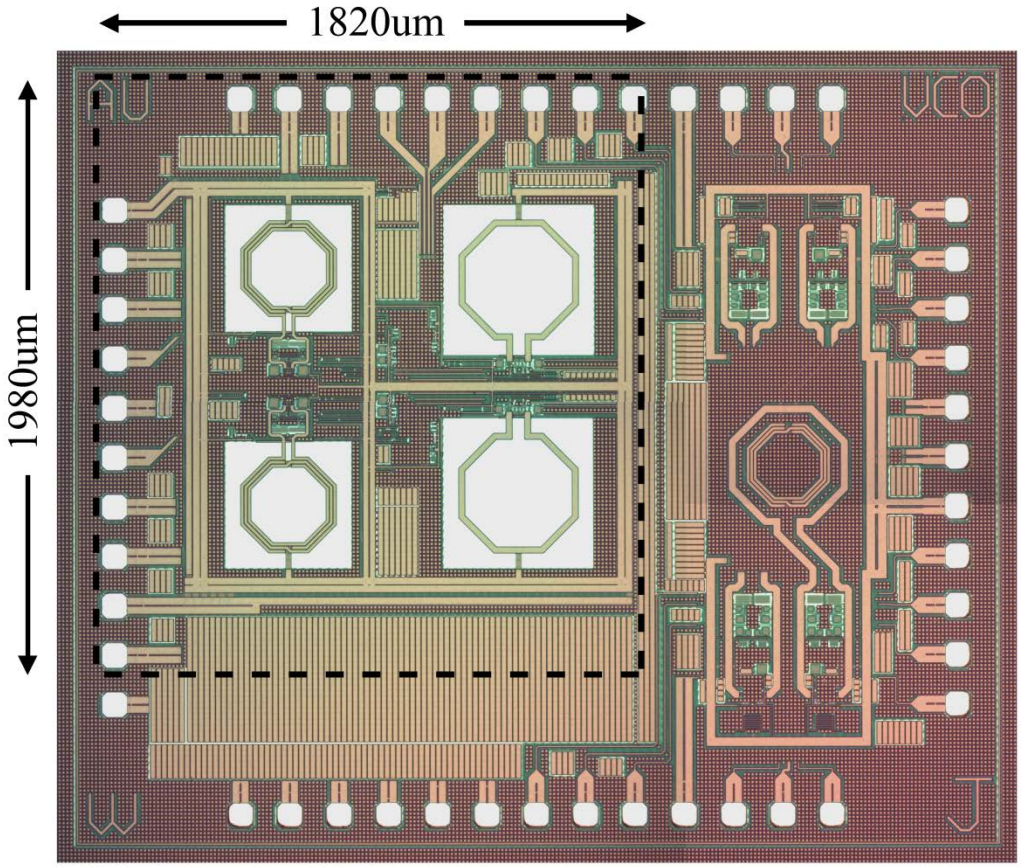


Figure 4.5. Die photograph of the prototype VCO.

4.4.1 Test Setup

The prototype VCO was measured on a test board built on standard FR4 material. The die was gold wire bonding packaged and soldered on the printed circuit board (PCB). Here shows the layout with pin map.

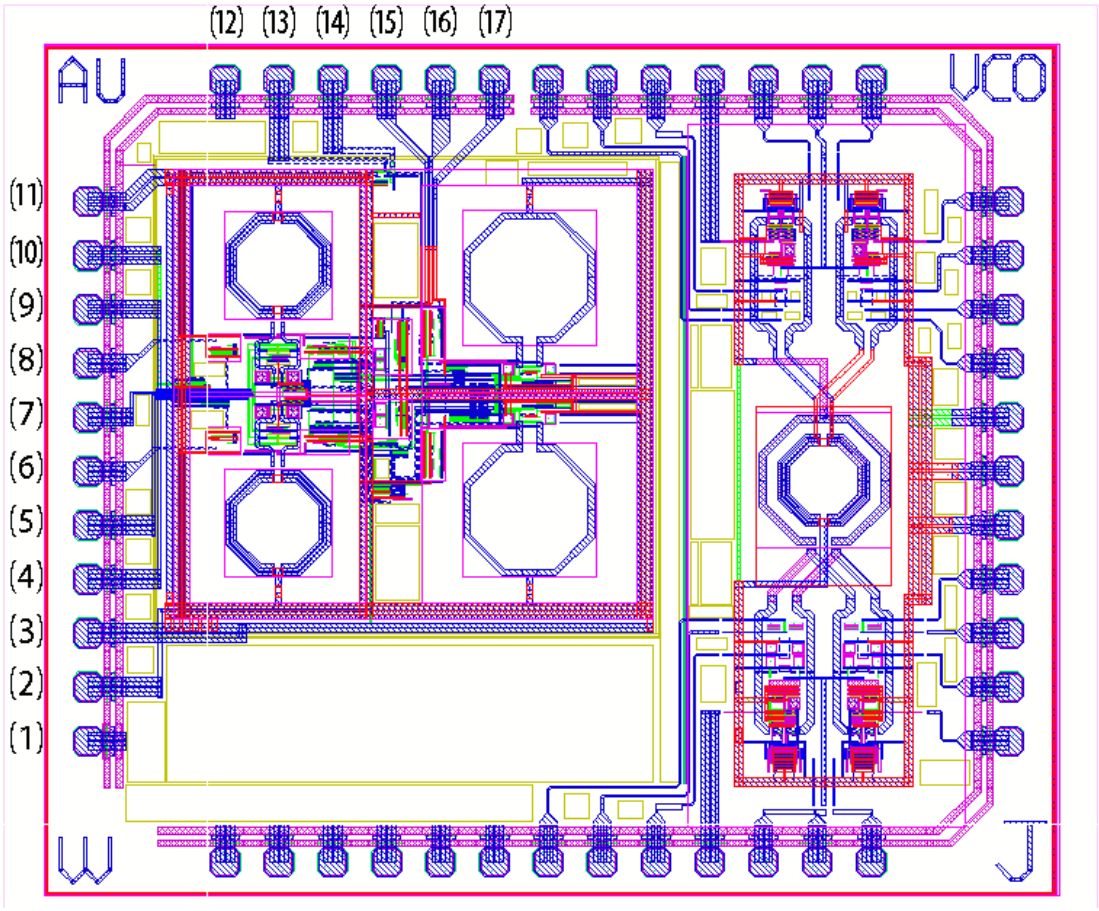


Figure 4.6. VCO layout.

Table 4.1: VCO pin mag

(1)	NC	(2)	$9G_{CON}$	(3)	GND	(4)	V_{TUNE}	(5)	V_{BIAS}
(6)	$3G_{OUT}I$	(7)	Bit1	(8)	$3G_{OUT}Q$	(9)	Bit0	(10)	$3G_{CON}$
(11)	V_{CC}	(12)	NC	(13)	I_{DC}	(14)	$6G_{CON}$	(15)	$6G_{OUT}$
(16)	$9G_{OUT}I$	(17)	$9G_{OUT}Q$	\	\	\	\	\	\

GND, V_{TUNE}, V_{BIAS}, V_{CC} and I_{DC} are pins to provide DC bias. Pins $3G_{CON}$ and $6G_{CON}$ are the switch to turn on or off the output buffer of 2.5GHz band and 5GHz band. $9G_{CON}$ is charging for the mixer and 7.5GHz output buffer. Pins Bit0 and Bit1 are sub-bands selecting bits. The signal output pins are $3G_{OUT}I$, $3G_{OUT}Q$, $6G_{OUT}$, $9G_{OUT}I$ and $9G_{OUT}Q$. The pins named NC are dummy pins for symmetric purpose.

The front and back sides of the evaluation board is shown in Fig. 4.7

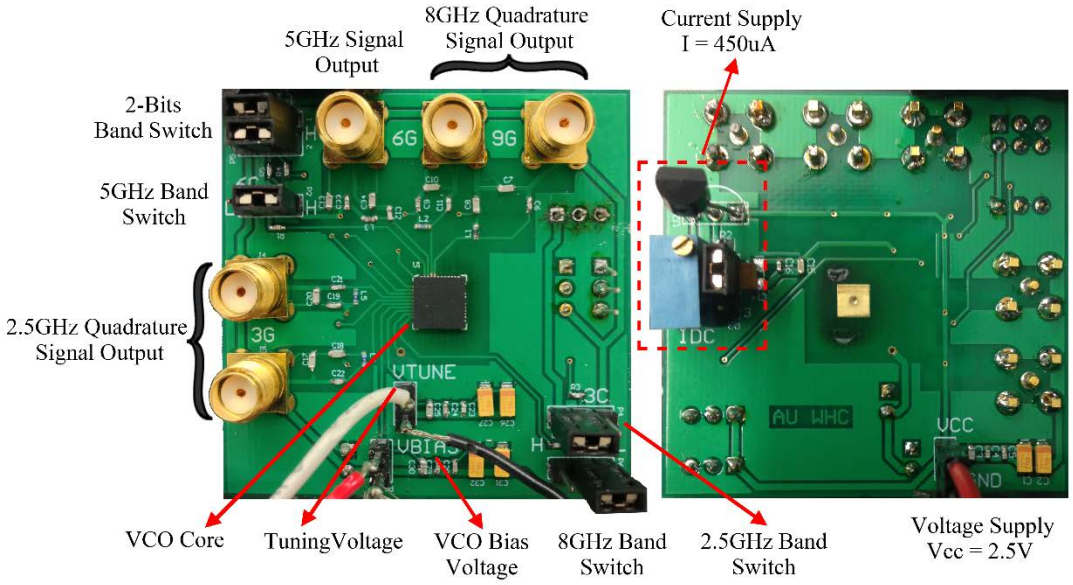


Figure 4.7. Front and back sides of the VCO evaluation board.

SMA connectors were used to provide ports for output signals measurement. Several decouple network were placed for signal outputs and DC inputs to prevent the interference. The on board current supply was built with a 3-terminal adjustable current sources LM334 and a rheostat, shown in the red dashed box above.

The setup used for the following measurements is illustrated in Fig 4.8. Agilent power supply E3631A was used as power supply for the device under test (DUT).

SMA cables were used to connect the DUT PCB to the Agilent spectrum analyzer E4446A.

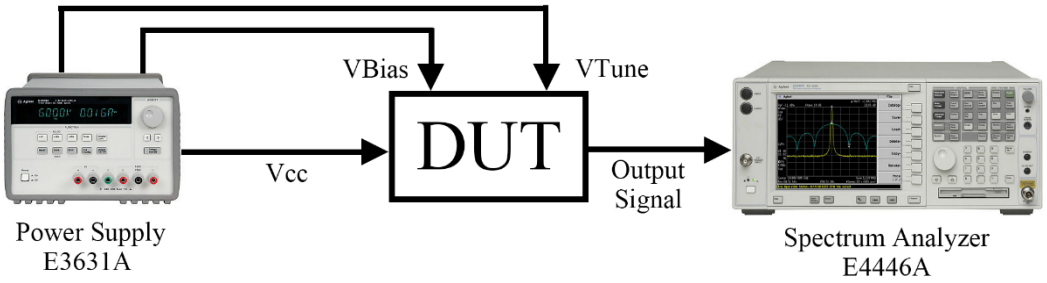


Figure 4.8. Experimental setup.

The power supply provided three independent voltages. The main voltage input Vcc set at 2.5V. The VCO bias voltage set at 1.2V. And the range of tuning voltage is 0 to 2.5V. A on board current source was built providing a constant 450uA current to the accuracy.

4.4.2 Phase Noise Measurement

Phase noise measurements were performed on an Agilent E4446A spectrum analyzer running the phase noise measurement option. Fig. 4.9 and Fig. 4.10 show the measured output spectrum of 2.5GHz band and 7.5GHz band respectively. The 2.5GHz band output spectrum is very clean. One single tune standing at 2.65GHz with an acceptable amplitude of -14.27dB. The central frequency of 7.5GHz band was designed to be 9GHz. Due to process variation and other effects, the build in bandpass filter is ineffective. As a Consequent, along with the desired 3rd order harmonic the fundamental tone and 2nd order harmonics are also survived. The inadequate -21.6dB amplitude and unwanted tunes will directly affect the phase noise performance.

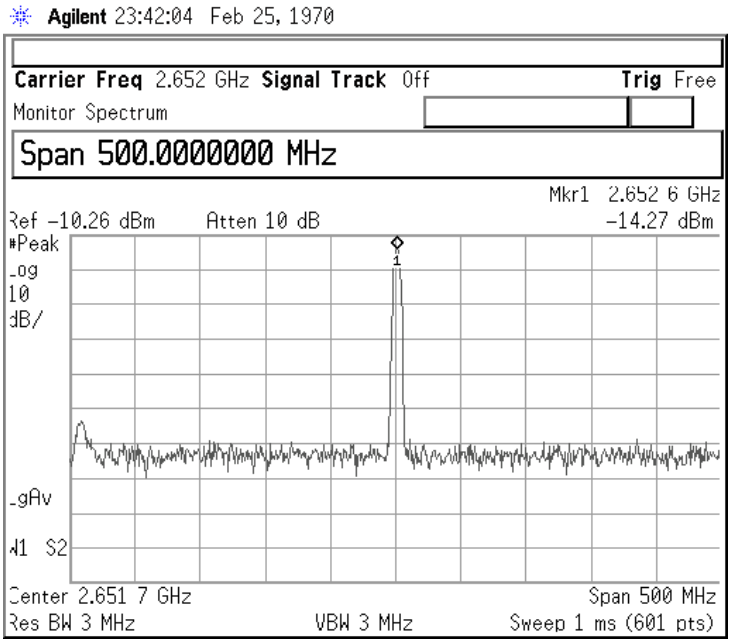


Figure 4.9. Measured output spectrum of 2.5GHz band.

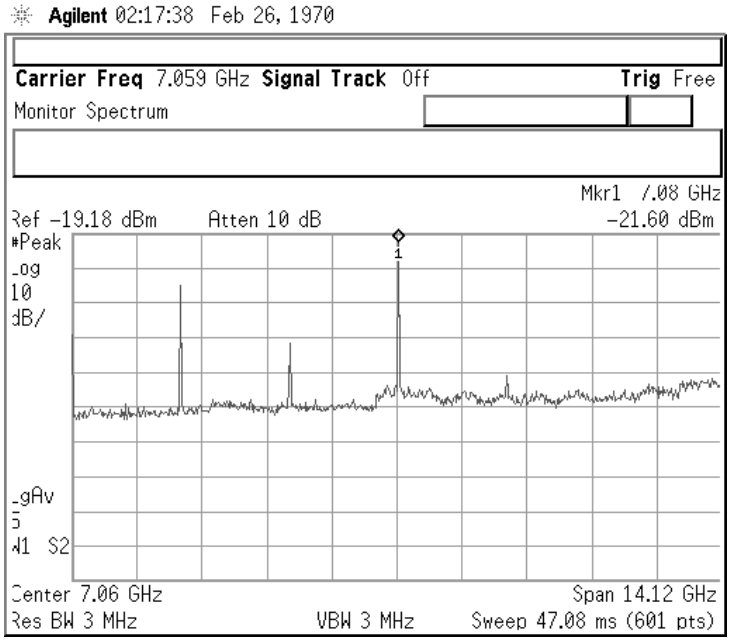


Figure 4.10. Measured output spectrum of 7.5GHz band.

Fig. 5.11 shows the measured and simulated phase noise in the 2.5GHz band, 5GHz band, and 7.5GHz band at the centre point of each band's tuning range. In the first two bands, measurements show relatively good agreement with simulations. As

analyzed above, 7.5GHz band has a large deviation from simulation result, due to the unexpected low amplitude and unmatched filter.

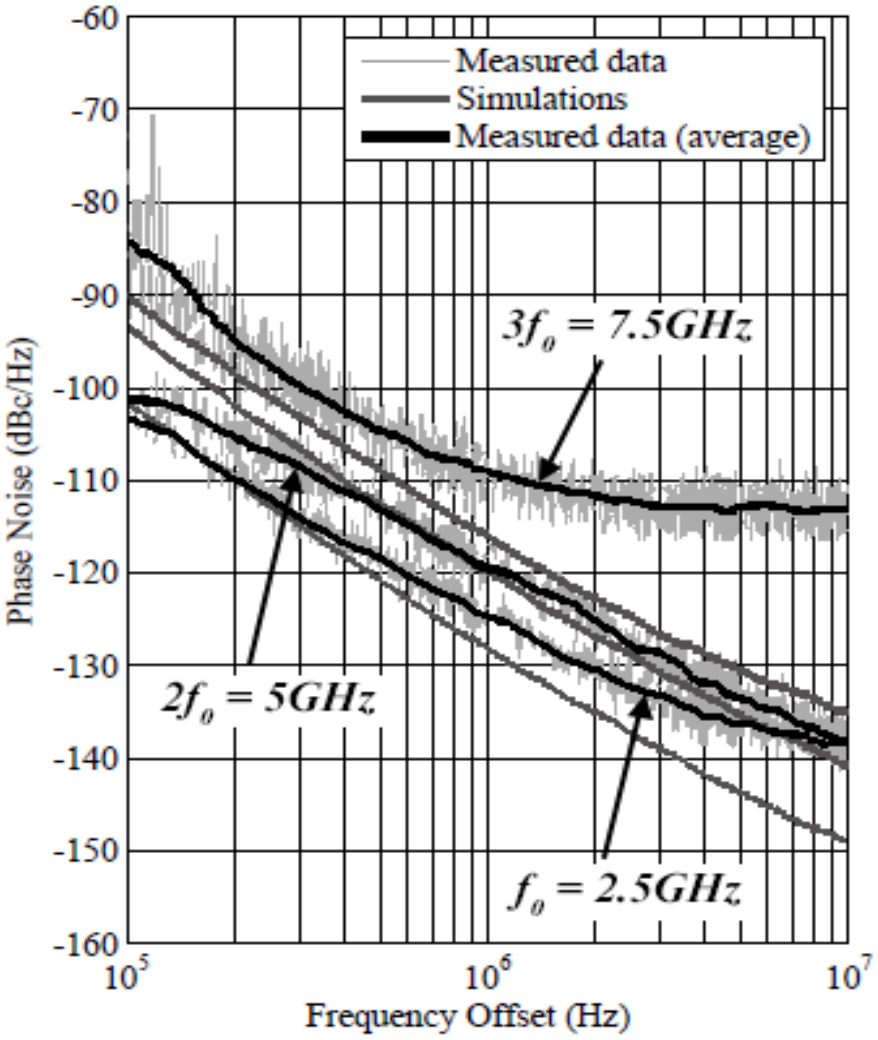


Figure 4.11. Phase Noise at 2.5, 5.0, and 7.5GHz.

4.4.3 Tuning Range Measurement

The measured tuning range is 15.4% in each three bands and tuning rang of the QVCO fundamental frequency (f_0=2.5G) is presented in Fig. 4.12. Fig. 4.13 shows the phase noise at different frequencies in fundamental frequency band. It is shown that phase noise varies erratically while tuning the varactors and switching sub-bands.

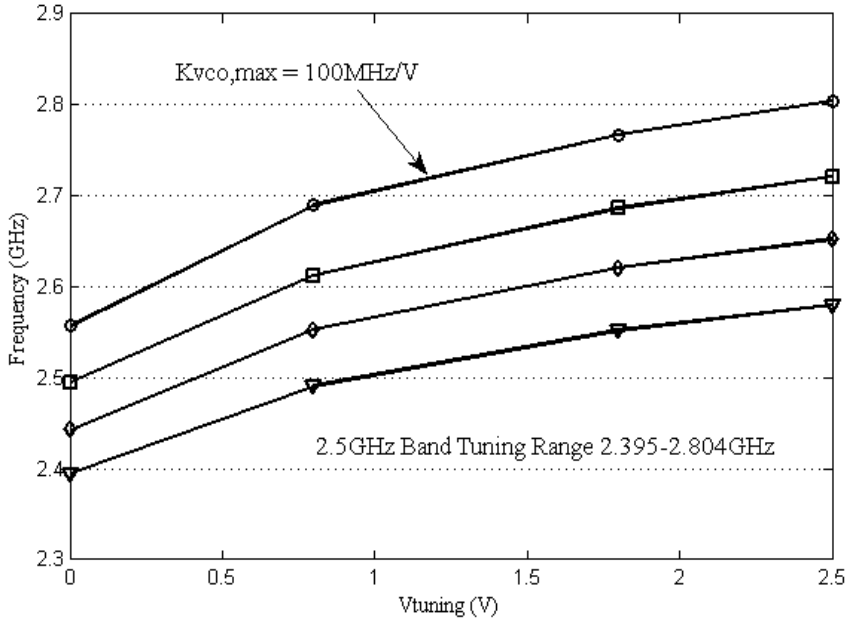


Figure 4.12. Measured tuning range of the QVCO fundamental frequency.

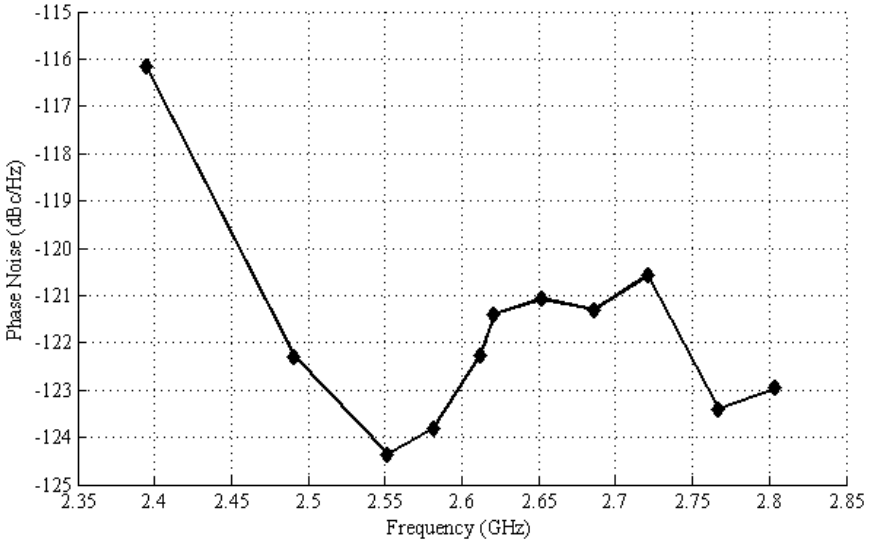


Figure 4.13. Measured phase noise versus the tuning range of the proposed circuit @1MHz offset in fundamental frequency band.

4.4.4 I/Q Mismatch Measurement

I/Q signal accuracy is a very crucial factor of a QVCO, which is very important to a RF T/RX's performance. I/Q signal output wave form of the QVCO and tripler are shown in the Fig 4.14 and Fig 4.15. I/Q mismatch is 0.9% and 1.2%.

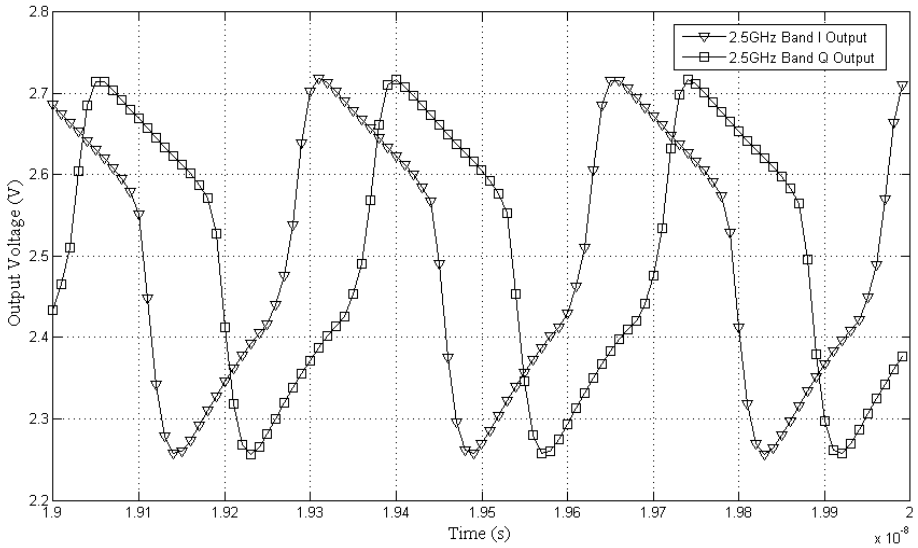


Figure 4.14. I/Q signal output wave form of the fundamental frequency band.

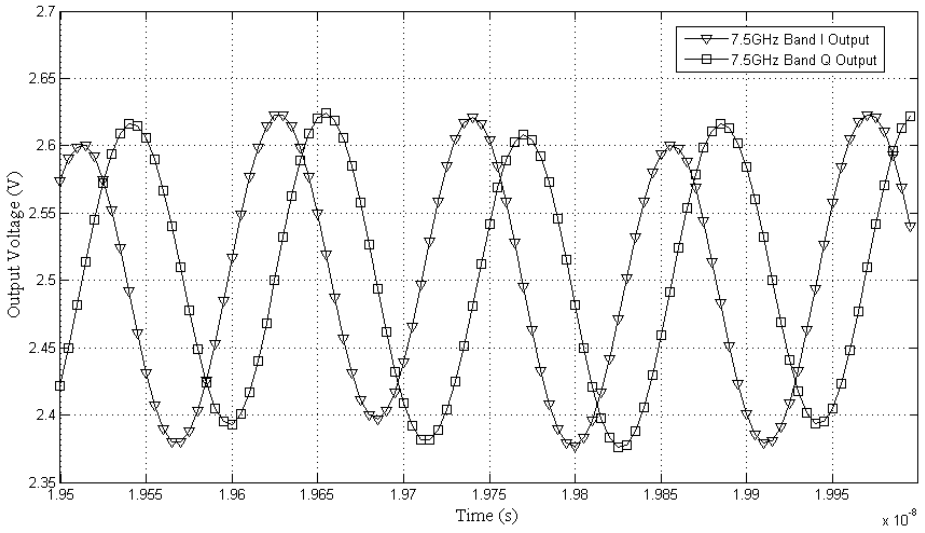


Figure 4.15. I/Q signal output wave form of the frequency tripler

4.4.5 VCO Performance Comparison

Table 4.2 summarizes the performance of the proposed QVCO and comparison with previously published QVCO work. When compared with prior art, the proposed QVCO and frequency multiplier achieves a Figure of Merit (FoM) of 182.2dB, 182.9dB and 170.4dB respectively, where the FoM is defined as [10]:

$$FoM = 10log\left[\left(\frac{f_0}{\Delta f}\right)^2 \frac{1mW}{P}\right] - L(\Delta f) \quad (4.3)$$

Table 4.2: Performance Comparison of QVCOS

Ref./Tech [µm]	Freq [GHz]	Tuning Range	PN@1MHz [dBc/Hz]	Power [mW]	FoM [dB]
[11] /CMOS 0.13	5.5	/	-117	5.28	184.58
[12] /CMOS 0.13	9.6	6.6%	-121 @3MHz	9	182.6
[13] /CMOS 0.18	10	15%	-95	14.4	163
[14] /CMOS 0.18	4.8	/	-125	22	185
This work /SiGe 0.18	2.5G 5G 7.5G	15.4% in each bands	-124.4 -119.1 -108.8	15 15 55	182.2 182.9 170.4

Chapter 5

Implementation of Bandgap Reference

The bandgap reference (BGR) has been widely used for IC designs since it was introduced by Widlar [15]. Several BGRs using Widlar BGR concept or its variants have been reported in both bipolar and CMOS processes.

Nowadays, BGRs are facing increased challenges for ultra-wide temperature application such as space application and precise analog circuit designs such as high resolution data converters. However, due to the curvature of the reference output voltage, the conventional first-order compensated BGR reference possesses limited temperature stability. An efficient technique to compensate the curvature of BGR's temperature coefficient (TC) using BJT's current gain β was proposed in [16] and will be adopted in our design.

Moreover, the BGR circuit normally suffers from power supply variations. This work presents a very simple, yet efficient circuit that improves the performance of BGR's power supply rejection ratio (PSRR) for more than 15dB.

This chapter investigates the temperature characteristics of β in both Si and SiGe processes and implement the Curvature Compensated BGRs utilizing this temperature characteristics. In the following sections, the conventional Widlar BGR is introduced and its limitations are discussed; β temperature dependences of Si and SiGe devices are analyzed; the proposed BGRs are presented. And In the last section, simulation results are summarized.

5.1 Power Supply Rejection

The BGR circuit is powered by power regulators or directly tied to the power supply, which is sensitive to power supply variations. So BGR's power supply can vary heavily and could couple unwanted signal on it, both of them may affect the output of BGR. The variation will be delivered to the BGR's output, and further influence the subsequent circuits.

Conventionally, BGR designs often use cascode transistors to separate the circuit from power supply, which provides some power supply rejection. However, cascode structure consumes more headroom, since it adds more levels of transistors, which is not suitable for low power, low voltage applications. This work propose a simple way to reduce the PSRR without adding cascode transistors.

The proposed BGR circuit is shown in Fig. 5.1 with PSRR improvement and curvature compensation technique together.

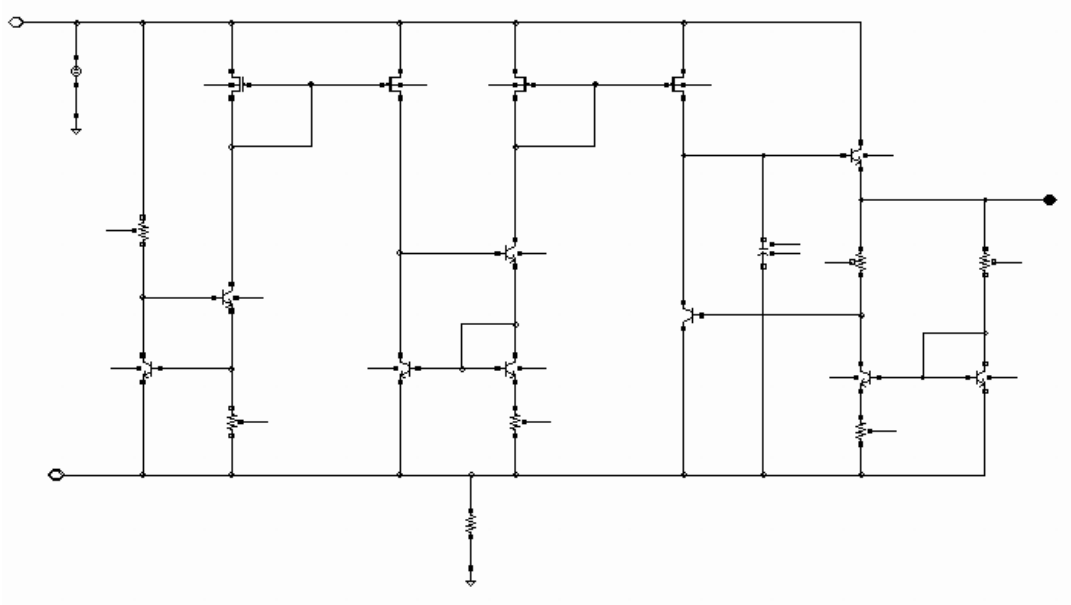


Figure 5.1. Proposed BGR circuit with PSRR improvement technique.

The proposed technique provides a constant current to the BGR by using I_C-V_{BE} relationship and the ratio of current mirror. Theoretically, this structure can improve the PSRR by 30dB without involving any op-amps. Fig. 5.2 shows the PSRR reduction effect. The voltage supply is changing from 3V to 6V, the current variation with and without PSRR improvement are differ by 5.515uA and 448.4uA respectively.

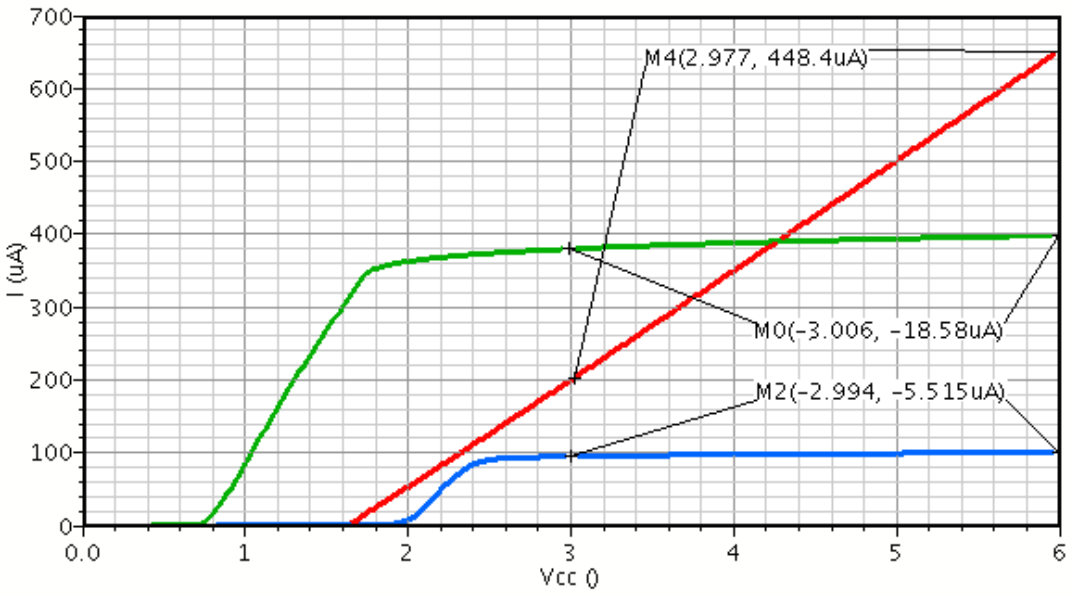


Figure 5.2. PSRR improvement simulation illustration.

5.2 Temperature Coefficient Compensation

Widlar BGR is widely used in IC design. By using first order compensation, it is barely qualified within commercial operation range. To achieve better performance, other techniques needs to be introduced.

5.2.1 Limitation of First Order Compensation

The first order temperature compensation is accomplished by the following equation:

$$V_{REF} = V_{BE} + KV_T \tag{5.1}$$

Where the VBE is a negative TC parameter, and VT is a positive TC parameter; K is a scaling factor for optimizing the compensation.

If VBE is a linear term, by adjusting the ratio of K carefully, the TC of the BGR can be compensated independently such that its temperature compensated output VREF versus the temperature should be a straight line. However, the simulation result of this first order BGR's TC turned out that the output is a parabolic curve approximately, as shown in Fig. 5.3.

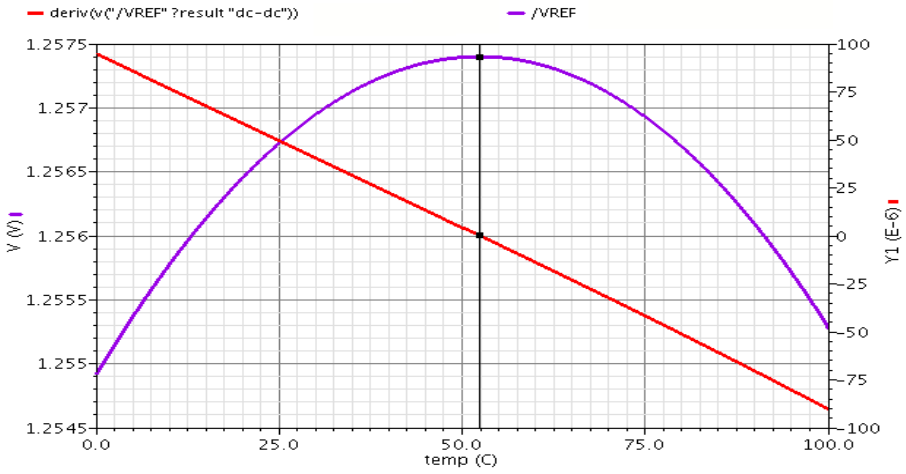


Figure 5.3. The first order BGR's output and TC.

The red line in Fig. 5.3, which is almost a straight line, is the TC curve, which is the derivative of the output curve. And only at 50 degree Celsius, the slope of the output curve becomes zero. Rest of the slope moves away from zero, which means the VREF is temperature independent only at 50 degree Celsius point, and the variation will increase when the offsets and mismatches increase. Obviously, VBE parameter must contain higher order temperature dependent terms.

The temperature characteristics of V_{BE} are studied extensively by Tsividis [17]. Considering the V_{BE} temperature dependence, we can derive the V_{REF} as:

$$\begin{aligned} V_{REF}(T) &= V_{BE}(T) + KV_T \\ &= V_G(T) + \left(\frac{T}{T_r}\right)[V_{BE}(T_r) - V_G(T_r)] \\ &\quad -(\eta - 1)\left(\frac{kT}{q}\right)\ln\left(\frac{T}{T_r}\right) + KV_T \end{aligned} \tag{5.2}$$

where V_G is the bandgap voltage of the silicon, η is the temperature dependency parameter of the silicon mobility, and T_r is a reference temperature. It is evident that the V_{BE} contains several temperature dependent parameters. Fig.5.4 shows bandgap energy $E_G = E_C - E_V$ versus temperature.

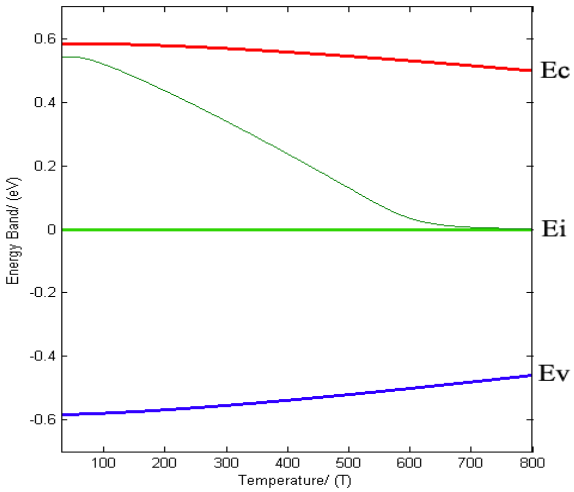


Figure 5.4. E_G versus Temperature.

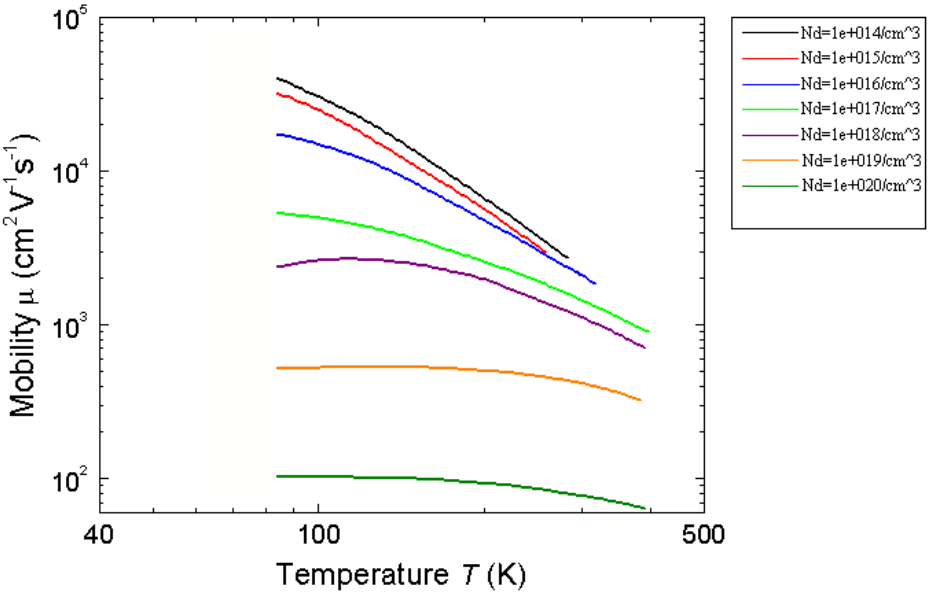


Figure 5.5: Silicon mobility versus temperature under different doping levels.

It is shown that η increases with temperature in the low temperature region, because carriers will get more energy when the temperature increases due to the impurity scattering. However, if temperature further increases, η will decrease due to lattice scattering. Also shown that the mobility η and Δη decreases with the doping level, which means heavily doped semiconductor devices has higher stability, yet its speed is lower.

5.2.2 Temperature Dependence of Current Gain β

There are many ways to cancel the higher order terms of V_{BE}. The approach adopted in this paper is to utilize the current gain of bipolar transistor β. The current gain β is a temperature dependent coefficient, and it's nonlinear, which can be used to compensate the higher order terms in V_{BE}.

5.2.2.1 Temperature Dependence of Si BJT β

Si BJT current gain β can be derived as [18], [19]

$$\beta_0 = \frac{\alpha_0}{1 - \alpha_0}$$

(5.3)

$$\alpha = \frac{\operatorname{sech}(W/L_{nb})}{1 + (D_{pe}/D_{nb})(p_{ne}/n_{pb})(W/L_{pe})}$$

(5.4)

where p_{ne}/n_{pb} is minority carrier concentration ratio

$$\frac{p_{ne}}{n_{pb}} = \frac{{n_i}^2/N_E}{{n_i}^2/N_B} = \frac{N_B}{N_E}\frac{N_C N_V \exp(-E_{GE}/kT)}{N_C{}' N_V{}' \exp(-E_{GB}/kT)}$$
$$= \frac{N_B}{N_E}\exp\left(\frac{E_{GB} - E_{GE}}{kT}\right)$$

(5.5)

where N_A is base doping level, and N_D is emitter doping level.

$$D_{pe} = \mu_e \frac{kT}{q} \quad D_{nb} = \mu_b \frac{kT}{q}$$

(5.6), (5.7)

L_{pe} is minority carrier path length in emitter, namely,

$$L_{pe} = \sqrt{D_{pe}\tau_e} \qquad \tau_e \propto \frac{{n_i}^2}{eN_D}$$

(5.8)

$$L_{nb} = \sqrt{D_{nb}\tau_b} \qquad \tau_b \propto \frac{{n_i}^2}{bN_A}$$

(5.9)

where

$${n_i}^2 \propto T^3 e^{-(E_g - \Delta E/kT)}$$

(5.10)

Thus, we can obtain the relationship between β and T as follows

$$\beta_0 \approx \frac{n_{pb}}{p_{ne}} = \frac{N_E}{N_B} exp\left(\frac{E_{GE} - E_{GB}}{kT}\right)$$

(5.11)

Let $\beta_\infty = N_E/N_B$ and $\Delta E_G = E_{GE} - E_{GB}$ we get

$$\beta(T) = \beta_\infty \, exp\left(\frac{\Delta E_G}{kT}\right)$$

(5.12)

The simulation result on Si BJT β's temperature dependence is shown below

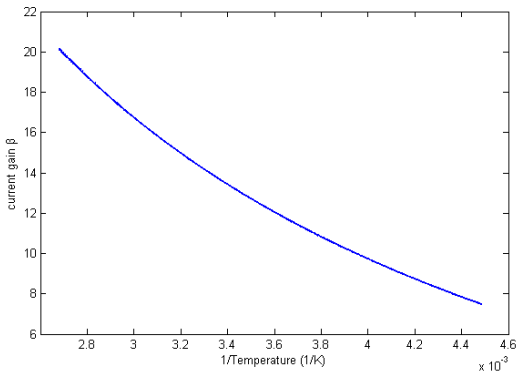


Figure 5.6. Si BJT current gain β versus 1/T.

From Fig.5.6 we can see β will increase with temperature. β_∞ is around 70, and ΔE_G is around -25meV. This simulation result is based on the Si BJT in a 0.18μm SiGe process. This is a BiCMOS process, so the Si bipolar transistor is parasitic BJT obtained in CMOS structure.

5.2.2.2 Temperature Dependence of SiGe HBT β

One of the differences between HBT and BJT is that HBT's base is heterojunction semiconductor material, which means the bandgap of the base is different from emitter and collector. Fig.5.7 shows the SiGe HBT band diagram.

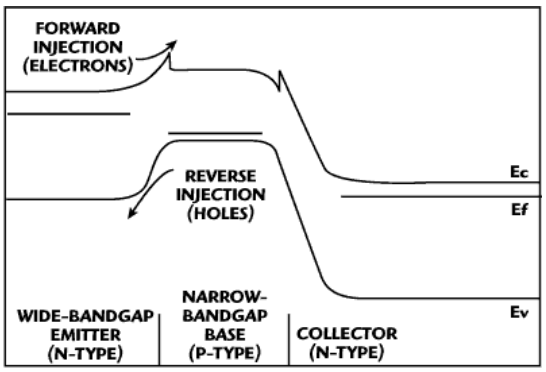


Figure 5.7. SiGe HBT energy band.

From Fig. 5.7 we can see the ΔE_G approaches to 0eV. Recall the equation (5.12), the larger ΔE_G is, the higher β will be. It is for this reason that HBT has more current gain, and has different temperature dependence.

Simulation result of Si BJT β temperature relationship is shown below

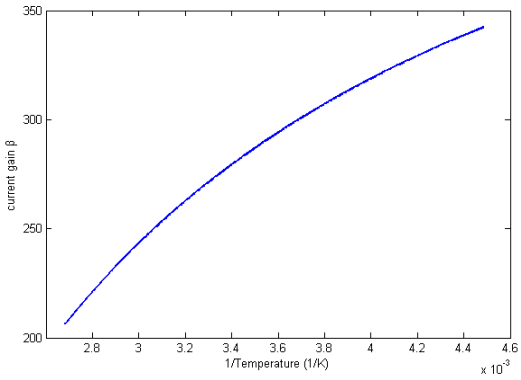


Figure 5.8. SiGe HBT current gain β versus Temperature^{-1}.

From Fig.5.8 we can see β will decrease with temperature. β_∞ is around 50 and ΔE_G is around 42meV. This simulation result is based on Si BJT in a 0.18μm SiGe process.

5.2.3 Curvature Compensation

β is a temperature dependent coefficient as we discussed above, and it's nonlinear, which can compensate the higher order terms in V_{BE}. Fig. 5.9 illustrates a simple circuit that extracts β into the output voltage V_{REF}.

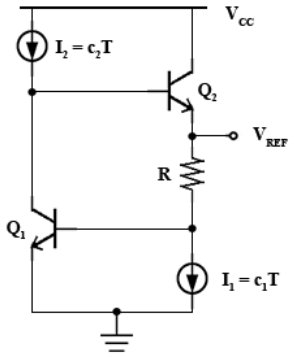


Figure 5.9. Basic curvature compensation circuit.

the two current sources I_1 and I_2 are PTAT source, so the reference voltage V_{REF} is

$$V_{REF}(T) \approx V_{BE}(T) + c_1 RT + \frac{c_2 RT}{\beta(T)}$$
$$= V_{BE}(T) + K_1 T + K_2 T\, exp\left(\frac{\Delta E_G}{kT}\right) \tag{5.13}$$

The first two terms are original first order temperature compensation. The third one is an exponential term, which can expand in Taylor series.

$$exp\left(\frac{\Delta E_G}{kT}\right) = \sum_{n=0}^{\infty} \frac{\left(\frac{\Delta E_G}{kT}\right)^n}{n!} = 1 + \frac{\Delta E_G}{kT} + \frac{\left(\frac{\Delta E_G}{kT}\right)^2}{2} + \frac{\left(\frac{\Delta E_G}{kT}\right)^3}{6} + \cdots \tag{5.14}$$

Carefully adjusting the ratio K_2, the V_{BE}'s higher order term can be greatly compensated in a large temperature range. In summary, the circuit I proposed is given in Fig. 5.10

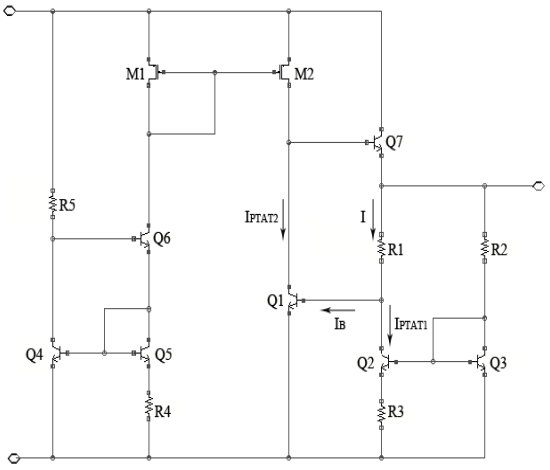


Figure 5.10. Proposed circuit.

5.2.4 Simulations Results

In Fig. 5.11, the blue curve illustrate the simulated the characteristics of Vref versus temperature for the proposed BGR circuit. It can be seen that it is not a parabolic curve anymore. The first order derivative shown in green, crosses the x axis twice. It has two zeros and one pole, which means this BGR's TC equals to zero at two points.

The average TC of the SiGe HBT BGR are simulated as 4.57 and 11.66 ppm/ºC over the commercial (0 ~70°C) and military (-55 ~125°C) temperature ranges, respectively. The power supply rejection ratio (PSRR) are -50dB under 3.3 volt supply voltage.

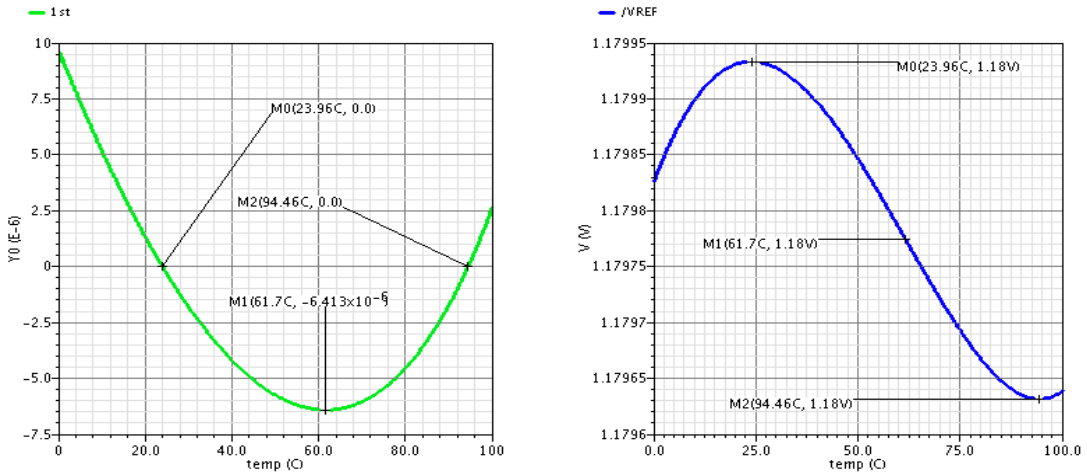


Figure 5.11. SiGe HBT based BGR output and TC curves.

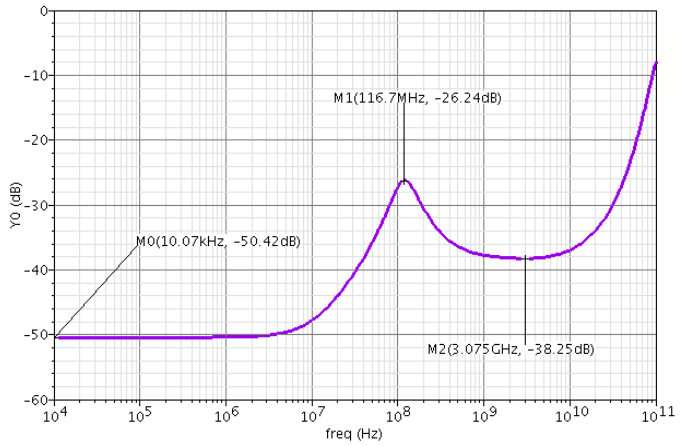


Figure 5.12. SiGe HBT based BGR output PSRR.

And for Si BJT, we can also see the compensation effect. The average TC of the Si BJT BGR are simulated as 12.33 and 54.77 ppm/ºC over the commercial (0 ~70°C) and military (-55 ~125°C) temperature range standards, respectively. The PSRR are -64dB under 3.3 volt supply voltage.

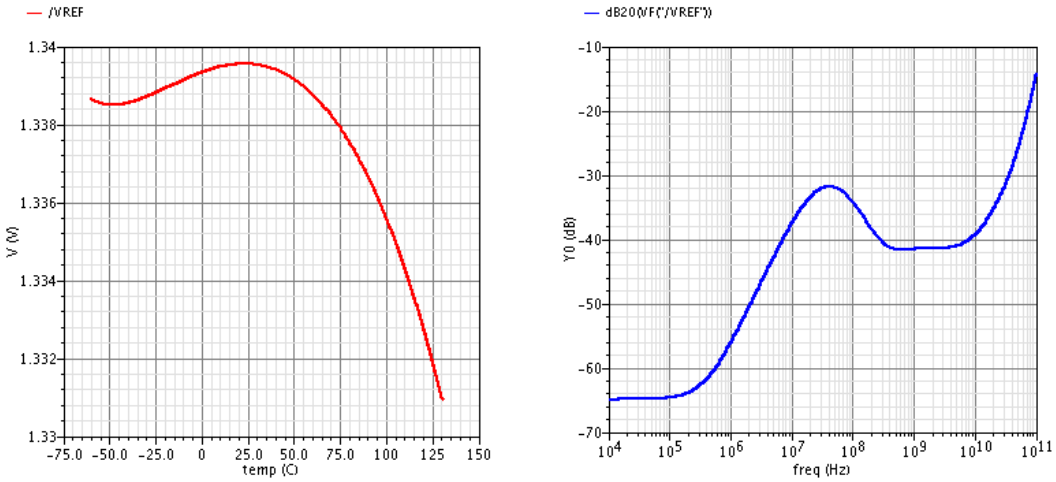


Figure 5.13: Si BJT based BGR output and PSRR

Chapter 6

Conclusions

Using a 0.18um SiGe BiCMOS technology, this thesis have presented a compact integration design consisting a mixer based low noise wide tuning range QVCO producing three frequency bands of 2.5GHz, 5GHz, 7.5GHz respectively. Bipolar transistors are used for oscillation core construction and NMOS devices for coupling. The second order harmonic of QVCO, 5GHz signal, is easy to obtain and utilize with SiGe BiCMOS process. According to the tested results, the proposed QVCO with frequency multiplier demonstrated a low-phase-noise and wide tuning range performance. For each frequency band, 15.4% tuning range is achieved. And the phase noise are -124.4dB, -119.1dB and -108.8dB respectively.

Fundamental principles of LC VCOs performance improvement techniques were introduced in Chapter 2 and Chapter 3, respectively. These chapters provide the framework supporting subsequent discussions. A mixer based VCO with a binary-weighted capacitor array was designed and tested in Chapter 4. In Chapter 5, bandgap reference circuit, an auxiliary performance improvement module, was

designed with higher order compensation concept and power supply rejection topology.

The VCO in this thesis has large gaps between each frequency band, which is inadequate in today's multi-standard requirement. Therefore one desirable extension to this work is seeking the unification of all three frequency bands. The most feasible approach is introducing a larger capacitor array to fill up the gaps between each band realizing continues tuning range.

References

[1] “United States Frequency Allocations Chart,” 2003.

[2] T. C. Weigandt, B. Kim, P. R. Gray, “Analysis of Timing Jitter in CMOS Ring Oscillator,” *Proc. of Int. Symp. Circuits and Systems (ISCAS)*, vol.4, pp.27-30, London, UK, June 1994.

[3] Ali Hajimiri, Sotirios Limotyrakis, and Thomas H. Lee, ‘‘Jitter and Phase Noise in Ring Oscillators’’, *IEEE J. Solid-State Circuits*, Vol. 34, No. 6, June 1999.

[4] Axel Dominique Berny, Robert G. Meyer, Ali Niknejad, “Analysis and Design of Wideband LC VCOs” *Electrical Engineering and Computer Sciences University of California at Berkeley*, May 12, 2006.

[5] Behzad Razavi, “A Study of Phase Noise in CMOS Oscillators”, *IEEE Journal of Solid-State Circuits*, Vol. 31, NO. 3, March 1996.

[6] D. Leeson, “A simple model of feedback oscillator noise spectrum,” *Proceedings of the IEEE*, vol. 54, no. 2, pp. 329–330, 1966.

[7] Pietro Andreani and Xiaoyan Wang, “On the Phase-Noise and Phase-Error

Performances of Multiphase LC CMOS VCOs", *IEEE Journal of Solid-State Circuits*, vol. 39, No. 11, Nov 2004.

[8] Pietro Andreani, "A 2 GHz, 17% Tuning Range Quadrature CMOS VCO with High Figure-of-Merit and 0.6Æ Phase Error", *Solid-State Circuits Conference*, 2002. ESSCIRC 2002.

[9] Pei-Kang Tsai, Tzuen-Hsi Huang, "Integration of Current-Reused VCO and Frequency Tripler for 24-GHz Low-Power Phase-Locked Loop Applications", *IEEE Transactions on Circuits and Systems—II: express briefs*, vol. 59, No. 4, April 2012.

[10] P. Kinget, B. Soltanian, S. Xu, S. Yu, and F. Zhang, "Advanced design techniques for integrated voltage controlled LC oscillators," *Proceedings of Custom Integrated Circuits Conference*, 2007, pp. 805- 811.

[11] C.-Y. Jeong and C.-S. Yoo, "5-GHz low-phase noise CMOS quadrature VCO," *IEEE Microw. Wireless Compon. Lett*, vol. 16, no. 11, pp.609–611, Nov. 2006.

[12] I. R. Chamas and S. Raman, "Analysis and design of a CMOS phase tunable injection-coupled LC quadrature VCO (PTIC-QVCO)," *IEEE J. Solid-State Circuits*, vol. 44, pp. 784–796, Mar. 2003.

[13] S. Li, I. Kipnis, and M. Ismail, "A 10-GHz CMOS quadrature LC-VCO for multicore optical applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1626–1634, Oct. 2003.

[14] S. L. J. Gierkink,S. Levantino, R. C. Frye, C. Samori, and V. Boccuzzi, "A low-phase-noise 5-GHz CMOS quadrature VCO using superharmonic coupling,"

IEEE J. Solid-State Circuits, vol. 38, no. 7, pp. 1148–1154, Jul. 2003.

[15] R. J. Widlar, "New developments in IC voltage regulators," *IEEE Journal of Solid-state Circuits*, vol. 6, pp. 2-7, Feb. 1971.

[16] Inyeol Lee, Gyudong Kim, Wonchan Kim, "Exponential Curvature-Compensated BiCMOS Bandgap References" *IEEE Journal of Solid-State Circuits*, vol. 29, no. 11, Nov 1994.

[17] Y. P. Tsividis and R. W. Ulmer, "A CMOS voltage reference," *IEEE J. Solid-state Circuits*, vol. 13, pp. 774-778, Dec. 1978.

[18] Dale Buhanan, "Investigation of Current-Gain Temperature Dependence in Silicon Transistors," *IEEE Transactions on Electron Devices*, vol. ed-16, no. 1, Jan 1969.

[19] S. M, SZE, "Semiconductor Devices Physics and Technology 2nd edition," pp.151-152.