RFIC Design for Software-Defined Radio Receiver Frontend

by

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Abstract

With the rapidly growing wireless communication standard, portable devices are expected to operate in multiple standards. Ultimately, a “Software-Defined Radio”, which is a universal RF frontend for all bands, is highly desirable. Conventional RF frontend could handle single band signal very well, but they still need bulky SAW filter at the input to filter out the interference signals from other bands, namely the “out-of-band interference” (OBI). To support multiple bands, one needs multiple RF frontend with one SAW filter for each band.

In this work, a SDR receiver frontend structure with OBI interference is proposed. Passive mixer and negative feedback was utilized for band selection and OBI suppression. A programmable bandpass characteristic was achieved at RF input of the receiver. This design was implemented in a 0.18um SiGe technology with f_T frequency at 60GHz.

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List of Abbreviations

CML	Current Mode Logic
CR	Cognitive Radio
DSB	Double Side Band
HBT	Heterojunction Bipolar Transistor
IIP3	Input Third-order Intercept Point
LNA	Low Noise Amplifier
LTI	Linear Time Invariant
LTV	Linear Time Variant
NF	Noise Figure
OBI	Out of Band Interference
P1dB	Input 1dB Compression Point
SAW	Surface-Acoustic Wave
SDR	Software Defined Radio
SiGe	Silicon-Germanium

Chapter 1 INTRODUCTION

1.1 RF frontend

The purpose of RF frontend is to upconvert the baseband signal to the higher carrier frequency band where it is more appropriate for wireless transmission through air. On the receiver side, the RF signal is downconverted to be processed by baseband circuit. Carrier frequency determines the part of spectrum occupied by the wireless transmission. Each wireless standard has its own allotted spectrum band and its channel specification as shown in the table below.

Table 1.1 Wireless standards characteristics

Standard	Frequency Range (MHz)	Channel Bandwidth	Channel Spacing	Channel Number
GSM-900	890-915	200 kHz	200 kHz	124
GSM-1800	1710-1880	200 kHz	200 kHz	374
UMTS (3G cellular)	2100	5 MHz	-	-
GPS	1575, 1227	10.23 MHz	-	154, 120
802.11a	5000	20 MHz	-	13
802.11g	2400	22 MHz	5 MHz	13

Most wireless frontend supports only one or two standards due to different spectrum band, channel bandwidth and coding scheme. With the rapidly increasing number of wireless standards, multiple frontends would be needed to support all the commonly used

networks. This imposes greater burdens on wireless devices, especially portable devices, in terms of cost, size and power consumption. An ideal substitute would be a universal RF frontend able to cover all different bands, namely the “Software-defined radio” (SDR). As the name suggests, most of the modulation and coding was done in the digital domain. These baseband processors are programmed with software. In this way, RF frontend could be configured for any type of wireless standards through software and the hardware remains fixed. The high flexibility of SDR allows for adaptive wireless system. A good example is the “Cognitive Radio” where carrier frequency and bandwidth are configured dynamically according to the current spectrum usage. For low populated area, this gives higher spectrum efficiency [1].

In the original SDR concept, the RF signal was directly digitized through a high-speed ADC after antenna at the receiver side. However, ADC performance was inherently limited at high frequency range and state-of-the-art ADC with adequate accuracy might only go as far as hundreds of megahertz, this is hardly enough to cover all the gigahertz range wireless bands. A more practical solution is to first downconvert RF signal with conventional RF frontend to a moderate frequency low enough to be sampled by ADC. Thus the requirements on ADC are greatly relaxed.

In order to cover different wireless bands, the RF frontend needs to be wideband, say from 100MHz to 6GHz. For LNA, this means it needs to be input matched and provides gain across 100MHz to 6GHz. Wideband LNA topology like common base or common emitter with feedback could support this coverage with relatively low noise figure, especially for advanced BJT structure like SiGe heterojunction bipolar transistor with a cutoff frequency of

hundreds of gigahertz. It is much more challenging to keep the linearity of the RF frontend over such a wide bandwidth. Any large power signal or blocker appearing inside this bandwidth could saturate the frontend preventing the LNA from properly amplifying the desired signal. Due to the great frequency coverage, it is very likely the frontend might be saturated by some blocker from other bands or “out-of-band interference” (OBI). This linearity problem was accounted for in conventional narrowband RF system with a dedicated discrete SAW filter at LNA input. Surface wave acoustic (SAW) filter could provide sharp filtering with very high quality factor Q. A SAW filter placed at the input could suppress all the signals outside the bandwidth. The downside of SAW filter is that its center frequency is fixed physically and it could not be integrated.

This thesis is organized as follows: chapter 2 covers different types of LNA commonly used for receiver frontend with an emphasis on LNA with negative feedback; chapter 3 presents a theoretical model for analyzing passive mixer; chapter 4 discusses the design principle for high speed frequency divider which is used for four-phase square wave signal; chapter 5 presents the novel architecture with analysis and simulation results.

Chapter 2 LOW NOISE AMPLIFIER DESIGN

2.1 Introduction

As the first stage in the frontend chain, the low noise amplifier (LNA) plays a critical role for the noise performance. Other than amplifying the weak signal from antenna, LNA also adds its own noise to the signal during the process. Decent design could give a first stage noise figure (NF) of 2-3 dB over wide bandwidth. Basic single transistor amplifier topology includes common emitter/source, common base/gate and common collector/drain. Common emitter amplifier has the highest gain with lowest NF, but it usually needs a degeneration inductor at emitter node for input matching. It usually only convers narrowband, thus it is an ideal candidate for narrowband design. Another disadvantage of CE amplifier is that the series RLC circuit formed by parasitic capacitance Cpi and degeneration inductor Le actually has an amplifying effect from the source voltage to transistor input voltage Vpi. In this way, the linearity of CE is usually inferior to other designs. Common collector or emitter follower could not provide any voltage gain; it is mainly used as an output voltage buffer. In wideband design, common base (CB) topology is usually utilized as the first stage amplifier. It is easily matched at the input: its input impedance is 1/gm and remains constant over wide bandwidth. However, the most basic CB amplifier has a NF higher than 3dB. This is inherently limited by input matching.

2.2 Noise-Cancelling LNA

One of the common structures for LNA in SDR frontend is the noise cancelling LNA. There are different types of structure for noise cancelling, but the basic idea remains the same. Noise from LNA transistors is fed into the differential input along with the signal while keeping a negative polarity with the signal. In this way, noise is cancelled at the output whereas the signal is enhanced.

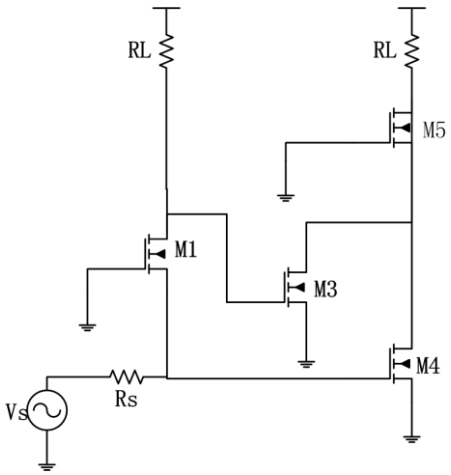


Fig. 2.1. Simplified schematics of Noise-cancelling LNA.

One of the possible implementation to noise cancelling LNA is using a CG-CS pair. The common gate branch provides 50Ohms for input matching. The common source branch presents a gate capacitance at input whose impedance is ideally infinite at low frequency. M1's channel thermal noise flows through R_s and R_1 developing a voltage of V_x and V_1 respectively with reverse polarity. V_x is further converted into current with a trans-conductance of gm_4 by M_4 and V_1 is converted into current with a trans-conductance of gm_3 by M_3. These two streams of current are recombined at the input of a current buffer M_5 where signal is added and noise from M1 is subtracted. Even though M_1's trans-conductance is fixed to 20mS for matching, we can still adjust the value of R1 along

with the trans-conductance of M_3 and M_4 to completely eliminate noise contribution from M_1 at output. Since signal has already experienced amplification at V_1, noise from M_3 can be ignored at the output. In this way, the only significant noise contributor is common source amplifier M_4. Noise from a common source amplifier could be shown to be approximately $1+\frac{\gamma}{g_m Rs}$. Without any explicit constraint, M_4's trans-conductance can be made relatively large for a low noise figure.

Another merit of this type of structure is distortion cancellation. Similar to the case of noise cancellation, distortion from M_4 can be cancelled with that from M_1 and M_3 when recombined at M_5's input. An IIP3 of 15dBm with a noise figure of 2dB was reported by utilizing this structure [2].

One of the main drawbacks from this cancelling structure is the need for accurate device parameter adjustment including gm and resistance. Accurate control over these parameters is impractical due to PVT variation and manual calibration is usually needed for optimal performance. To make matter worse, a slight deviation from optimal working condition leads to significant performance degradation.

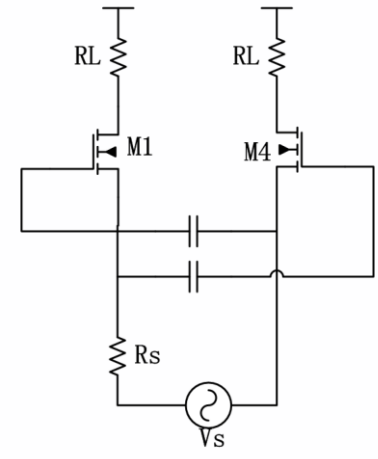


Fig. 2.2. Simplified schematics of capacitive cross coupling LNA.

Another type of structure for noise cancelling is capacitive cross-coupling technique. Careful observation could tell that this is actually the differential version of the previous structure. In fact, by removing C_1 or C_2 along with input In_n or In_p, we are left with a single-ended CS-CG pair. Due to this symmetry in the structure, only half of the noise from M_1 and M_2 is cancelled. However, since a differential input gives twice the signal strength, overall noise figure is still reduced. An apparent advantage of this structure over the previous one is that manual calibration is no longer needed since the circuit is symmetric. Even though its noise figure is relatively high compared with other approaches, capacitive cross coupling is still a popular choice for its robustness [3].

2.3 LNA with negative feedback

2.3.1 Introduction

To improve the noise performance of CB amplifier while keeping its merit of wideband, a modified structure was proposed by Francesco et al [4] as shown in figure 2.3. The tank consisting of R_p, L and C represents load on the amplifier. Instead of being AC grounded, the base node was attached to a voltage feedback signal from the output. This feedback network consisting of two capacitors C_1 and C_2 could transfer the impedance characteristic at output node to the input of LNA. When narrowband impedance is presented at the output, the LNA input would also present a narrowband characteristic.

Due to the single-ended input property of this structure, the balun at the input for a differential LNA could be omitted whose loss is directly going to increase the noise figure of LNA by a couple of dB. In addition, BJT is used instead of MOSFET since BiCMOS provides

SiGe HBT which has a higher f_t and g_m efficiency compared to MOSFET.

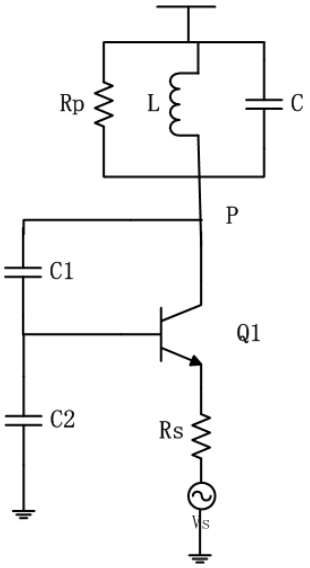


Fig. 2.3. Schematics of LNA with negative feedback.

2.3.2 Input Matching

Due to the capacitor feedback network, load impedance at node P is transferred to the input as well. Since this is voltage feedback, the capacitor network should draw little current from the output node, meaning the capacitors are usually kept to its minimum value. Define the feedback constant with capacitance ratio:

$$A_V = \frac{C_1}{C_1 + C_2} \tag{2.1}$$

Suppose load impedance presented by the parallel RLC tank at node P is Z_L, then the LNA input impedance could be shown to be:

$$Z_{in} = \frac{1}{g_m} + A_V \cdot Z_L \tag{2.2}$$

Suppose the tank has a narrowband characteristic, we could adjust the size of C_1 and C_2 to make the LNA present 50 Ohm only inside a narrow bandwidth and a nearly short for OBI

which is $1/g_m$. In this way, LNA is only matched for target frequency bands.

2.2.3 Noise Analysis

The main noise sources consist of shot noise from Q_1, thermal noise from source resistance R_S and Load impedance R_P as listed below:

$$\text{Q1 shot noise:} \quad \overline{i_{Q1}^2} = 2qI_C \tag{2.3}$$

$$\text{RS thermal noise:} \quad \overline{v_{n,rs}^2} = 4kTR_S \tag{2.4}$$

$$\text{Rp thermal noise:} \quad \overline{v_{n,rp}^2} = 4kTR_P \tag{2.5}$$

Basic common base amplifier usually has a noise figure higher than 3dB for input matching. It is required that $1/g_m$ equals to 50 Ohms. On the other hand, common base amplifier with negative feedback does not have this constraint because of the additional term in input impedance from the feedback in equation 2.2. A simplified noise figure of negative feedback LNA could be shown to be [4]:

$$\text{NF} \approx 1 + \frac{R_b}{R_S} + \frac{g_m R_S}{2\beta} + \frac{1}{2g_m R_S} + \frac{R_S}{R_L}\left(1 + \frac{1}{g_m R_S}\right)^2 \tag{2.6}$$

Above approximation stands valid when $f \ll f_T$ where f_T represents Q_1's cut-off frequency. For the HBT used in our design, a cut-off frequency of 60GHz could be easily achieved with proper biasing. In the equation, the second term represents noise from base resistance. The third and the fourth term are due to Q_1's base shot noise and collector shot noise respectively. The last term represents load resistor's thermal noise. Only base short noise and collector shot noise vary with biasing condition. Minimum noise figure is achieved

when $\frac{g_m R_S}{2\beta} = \frac{1}{2g_m R_S}$, this leads to:

$$g_m = \frac{\sqrt{\beta}}{R_S} \tag{2.7}$$

Assume an AC beta of 200 at 1GHz, we get an optimum g_m of about 280mS. Note that the absence of feedback coefficient A_V in the noise figure expression, we can make it relatively low with a high trans-conductance for Q_1 as shown below. Minimum noise figure is achieved around 300mS.

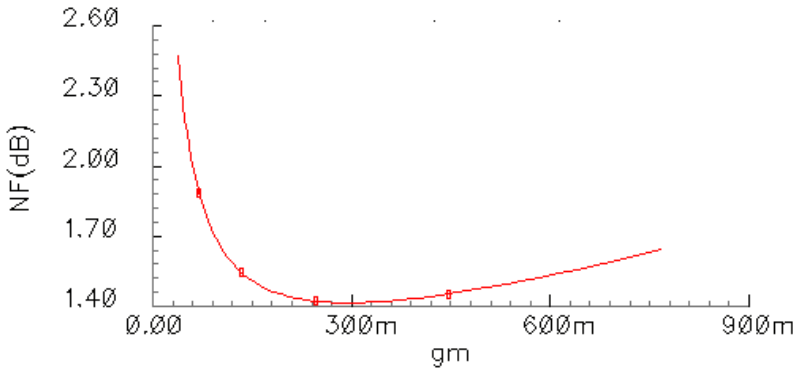


Fig. 2.4. Noise figure simulation for LNA.

2.2.3 Linearity Analysis

The input and output relationships for bipolar transistors follow an exponential pattern which is inherently a non-linear function. Non-linearity would lead to gain compression and intermodulation effects which degrades receiver's performance. This non-linearity could be analyzed with Taylor expansion, assume the output current could be expressed as:

$$i_{OUT}(t) = a_1 v_i(t) + a_2 v_i^2(t) + a_3 v_i^3(t) + \cdots \tag{2.8}$$

Common ways to evaluate receiver's linearity performance include 1dB compression point and input referred third-order intercept point (IIP3), which is defined as follows:

$$V_{P1dB} = \sqrt{0.145 \left|\frac{a_1}{a_3}\right|} \tag{2.9}$$

$$V_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{a_1}{a_3}\right|} \tag{2.10}$$

In this way, IIP3 is usually about 9dB higher than 1dB compression point. The output current from input transistor is further developed into voltage at the load resistor. For a large input signal, large output voltage might be developed which could further degrade transistor's linearity performance. As shown in figure 2.5, a lower load resistor gives a higher IIP3. As a result, it is usually preferred to filter out all large interferences in the current domain prior to converting current into voltage.

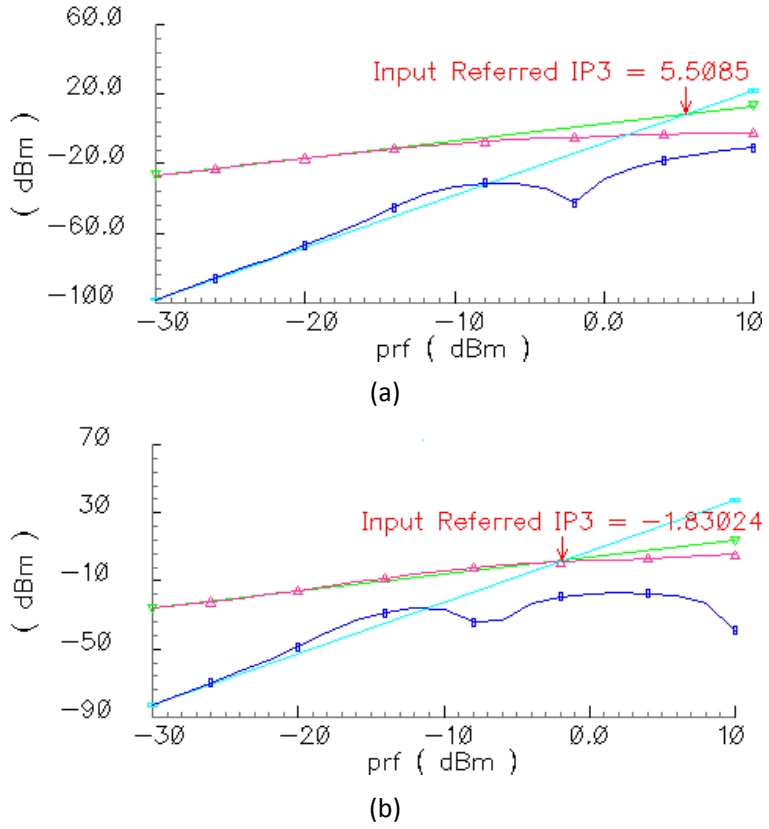


Fig. 2.5. Third-order intercept point simulation for LNA: (a)R_L=50 (b)R_L=500

2.4 Summary

In this chapter, different topologies for LNA circuit are presented with an emphasis on LNA with negative feedback which is used in the final design. The transfer characteristic from output to input of the negative feedback proves to be very useful when combined with passive mixer for OBI rejection.

CHAPTER 3 MIXER DESIGN

3.1 Introduction

As a cross stage between radio frequency signal and baseband signals, mixer could upconvert baseband signal to RF signal on the transmitter side and downconvert RF signal to baseband on the receiver side. This mixing operation is essentially carried out with a multiplication with the oscillation signal. Due to the nonlinearity of transistor amplification, signals are multiplied with LO harmonics as well. Square wave LO signals are usually applied to suppress these distortions.

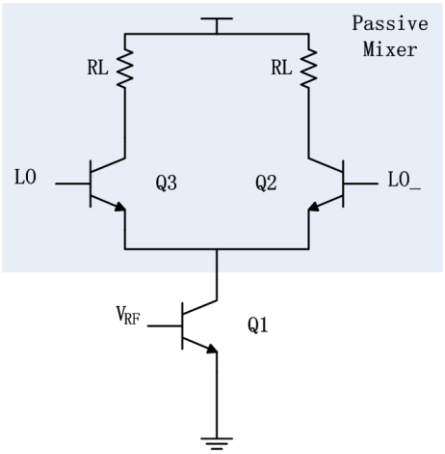


Fig. 3.1. Active and passive mixers.

There are mainly two types of mixer, either active or passive. As illustrated in figure 3.1, the main difference between these two is Q_1. For active mixer, Q_1 provides conversion gain and reverse isolation. Input voltage is converted to current at Q_1, differential pair Q_2 and Q_3 steers current between two branches. Load resistance further convert current signal into voltage signal. Components inside the box are a passive mixer which is basically an array of

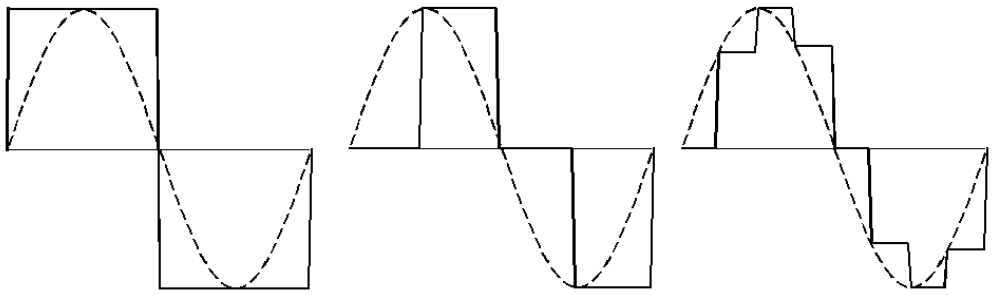
switches. Even though passive mixer doesn't have conversion gain, it avoids the nonlinearity coming along with Q_1. Passive mixer also has a couple of other merits including translational impedance which has enjoyed much focus among academics as the most promising solution to flexible SDR frontend for academic research in the recent years. In our design, passive mixer was adopted as well.

3.2 Oversampling mixer

The ideal mixing operation is done through multiplication with a sine wave. However, mixers in reality usually adopt square wave and the reason for that is linearity. Both BJT and MOSFET are inherently non-linear devices with their exponential or parabolic transfer curve. It is very challenging to guarantee both the upper level and lower level linearity in basic mixer structure as shown in figure 3.1. In order to keep nonlinearity to a controllable degree, square wave are used for LO input and the harmonics could be determined in advance. Single-balanced mixer induces all the harmonics. For double-balanced mixers where LO signal is differential all the even harmonics are rejected, but higher harmonics still reside.

Square wave mixer resembles sampler in several ways. Conventional differential mixer could be treated as a sampler with a sampling frequency f_S twice of LO frequency. This makes sense in a way that Nyquist theorem requires that sampling frequency be higher than at least twice of signal frequency. Furthermore, we can actually go beyond the basic Nyquist frequency. Through sampling at a higher frequency or oversampling, high order harmonics could suppressed. In a single sine period, we can acquire a couple of sample points and the number of which depends on the oversampling rate. By combining these samples with

appropriate weightings, we could approximate an ideal sine wave with square wave slices. Shown below are different approximations with different oversampling rate, it is obvious that the higher sample rate, the more accurate approximations become. To the extreme case where ideal sine wave is acquired, all harmonics shall be suppressed leading to truly linear mixer.



(a) (b) (c)

Fig. 3.2. Mixing with multi-phase LO. (a) M=2 (b) M=4 (c) M=8

Next we try to build a analytical model for passive mixer, part of the following derivation is based on Murphy's dissertation [5]. To study the effect of harmonic suppression of oversampling, consider an M phase mixer with an incident current i_{mixer}, its output voltage could be shown as:

$$v_{out}(t) = \sum_{x=0}^{M-1} i_{mixer}(t) K_x sw_x(t) \tag{3.1}$$

Where K_x represents weighting factors and $sw_x(t)$ is the switching function for different phases in time domain:

$$sw_x(t) = \begin{cases} 1, & \frac{(x-1)T}{M} < t < \frac{xT}{M} \\ 0, & otherwise \end{cases} \tag{3.2}$$

In the frequency domain, we can get its Fourier series coefficients:

$$\mathrm{SW}[k] = \frac{\sin\left(\frac{k\pi}{M}\right)}{k\pi} \tag{3.3}$$

$$SW_x[k] = SW[k]e^{-j\frac{2\pi kx}{M}} \tag{3.4}$$

Converting equation 3.2 into frequency domain, multiplication turns into convolution:

$$V_{out}\{\omega\} = \sum_{k=-\infty}^{\infty} I_{mixer}\{\omega - k\omega_c\} \sum_{x=0}^{M-1} K_x Sw[k]e^{-j\frac{2\pi kx}{M}} \tag{3.5}$$

By choosing a sampled version of sinusoidal waveform for weighting Kx, or more specifically:

$$\text{For I channel: } K_x = \cos\left(\frac{2\pi mx}{M}\right) \tag{3.6}$$

$$\text{For Q channel: } K_x = \sin\left(\frac{2\pi mx}{M}\right) \tag{3.7}$$

Combining these two together:

$$K_x = \cos\left(\frac{2\pi mx}{M}\right) + j\sin\left(\frac{2\pi mx}{M}\right) = e^{j\frac{2\pi mx}{M}} \tag{3.8}$$

where m is the target signal harmonics, i.e., signal around LO fundamental frequency is downconverted if m=1. Next, we could further expand Vout to be:

$$V_{out}\{\omega\} = \sum_{k=-\infty}^{\infty} I_{mixer}\{\omega - k\omega_c\} Sw[k] \sum_{x=0}^{M-1} e^{-j\frac{2\pi(k-m)x}{M}} \tag{3.9}$$

Where ω_c is LO fundamental frequency. For the inner summation:

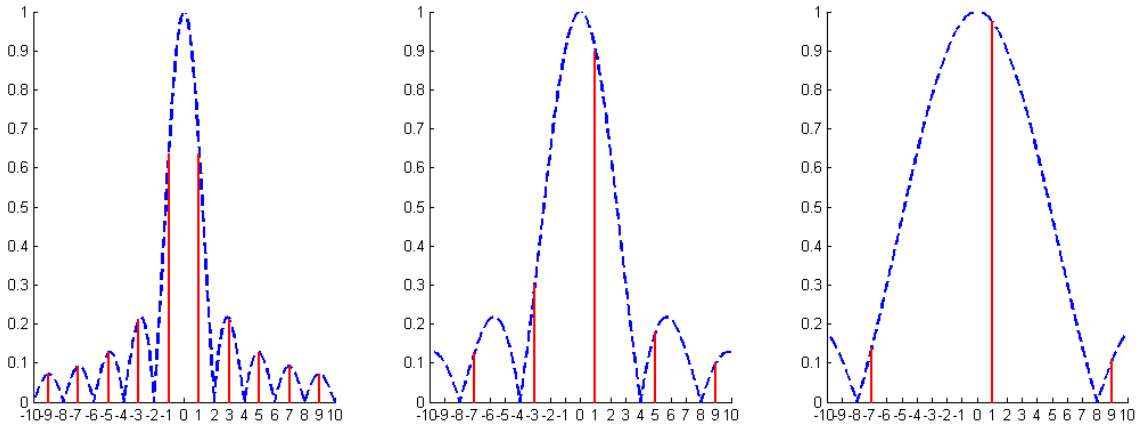
$$\sum_{x=0}^{M-1} e^{-j\frac{2\pi(k-m)x}{M}} = \begin{cases} M, & k-m = gM, g \in \mathrm{Z} \\ 0, & otherwise \end{cases} \tag{3.10}$$

Since only voltages around baseband are concerned, we could write 3.9 as:

$$V_{out}\{\Delta\omega\} = M \sum_{g=-\infty}^{\infty} Sw[m - gM] I_{mixer}\{(m - gM)\omega_c + \Delta\omega\} \tag{3.11}$$

From this expression for output voltage, we could see that the down-conversion operation shift input signal around different harmonics of LO down to baseband with weighting $S_w[k]$. Usually m=1 for down-converter and we can plot this weighting $S_w[k]$ to see the effect of oversampling on harmonics as shown in figure 3.3.

For a two-phase mixer or M=2, a conversion gain of -4dB is added to the RF signal. LSB and USB signals around all odd harmonics are downconverted to baseband. This is the case for the most basic double-balanced mixer. When M is increased to 4 which correspond to mixing with sine and cosine LO signals generating I and Q channel signal, only one of the USB and LSB around all odd harmonics is downconverted. For an even higher M of 8, the nearest harmonic is either USB or LSB of 7^{th} and 9^{th} harmonic. A conversion gain about -0.4dB is added to the RF signal for this case.



(a) (b) (c)

Fig. 3.3. Mixing coefficients for multi-phase LO: (a)M=2 (b)M=4 (c)M=8.

3.3 Four-Phase Passive Mixer

3.3.1 Linear Time-Variant Model

Now we are ready to analyze the passive mixer in a practical setting. Suppose the prior stage is converted into its Norton equivalent. The Norton current source acts as the input signal current and the Norton source resistance represents the prior stage output resistance or a loading on the Norton current source. A conceptual schematic for four-phase mixer is illustrated in figure 3.4. On-resistance of the mixer could be extracted in to the Norton source resistance as well leaving ideal switches in this analysis. A simplified baseband impedance of capacitance C_b is attached to each branch.

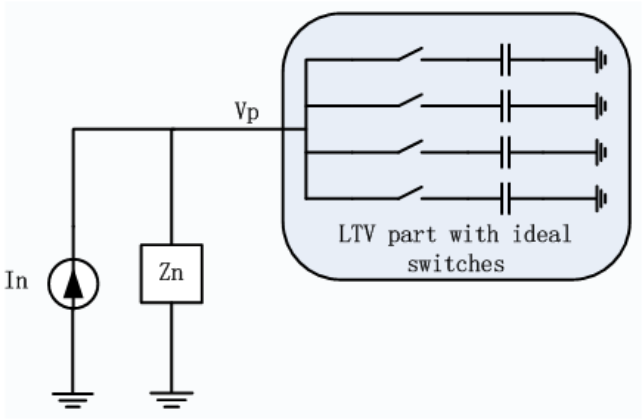


Fig. 3.4. Model for LTV analysis of passive mixer.

Next, recall the expression for V_{out} in the last section where a summation of input current at different LO harmonics multiplying a weighting of S_w, we could further utilize this result and define:

$$I_{N,fold}\{m\omega_c + \Delta\omega\} = \sum_{g=-\infty}^{+\infty} \frac{Sw[m-gM]}{Sw[m]} \cdot I_N\{(m-gM)\cdot\omega_c + \Delta\omega\} \tag{3.12}$$

$$\frac{1}{Z_{N,fold}\{m\omega_c + \Delta\omega\}} = \sum_{g=-\infty}^{+\infty} \frac{|Sw[m-gM]|^2}{|Sw[m]|^2} \frac{1}{Z_N\{(m-gM)\omega_c + \Delta\omega\}} \tag{3.13}$$

$$Z_{MX}\{m\omega_c + \Delta\omega\} = M|Sw[m]|^2 Z_{BB}\{\Delta\omega\} \quad (3.14)$$

Where $S_w[m]$ is the m_{th} Fourier coefficients of M-phase square wave switching function:

$$\mathrm{Sw[m]} = \frac{1}{M} sinc\left(\frac{k\pi}{M}\right) \quad (3.15)$$

$I_{n,fold}$ and $Z_{n,fold}$ are the folded modification of I_n and Z_n respectively: copies at LO harmonics appears in parallel with the original current or impedance with some weighting Sw. Z_{mx} is the translated version of Z_{bb}. Molnar et al [6] has proposed another solution where the entire mixer is converted into an LTI system.

Finally, mixer voltage at node P and output could be shown as:

$$\mathrm{Vp}\{\mathrm{m}\omega_c + \Delta\omega\} = I_{N,fold}\{\mathrm{m}\omega_c + \Delta\omega\}(Z_{N,fold}(\mathrm{m}\omega_c + \Delta\omega)\big|\big|Z_{MX}(\mathrm{m}\omega_c + \Delta\omega)\big) \quad (3.16)$$

$$V_{out}\{\Delta\omega\} = MSw[m]Zbb \cdot \frac{Vp\{\mathrm{m}\omega_c + \Delta\omega\}}{Z_{MX}\{\mathrm{m}\omega_c + \Delta\omega\}} \quad (3.17)$$

We can see from above equations that V_p could be expressed as the developed voltage across an equivalent load $Z_{n,fold}$ in parallel with Z_{MX} flowing with an equivalent current $I_{N,fold}$. The final output voltage combing four branches is a scaled version of voltage at node P.

3.3.2 Translational Impedance

When a passive mixer is loaded with a programmable baseband filter, the impedance of the filter would be up-converted to the LO frequency and its harmonics, presenting a programmable filter characteristics at the input of the mixer. This “Translational Impedance” [7] is mainly caused by the lack of reverse isolation for the passive mixer and similar property does not hold for active mixer for its strong reverse isolation.

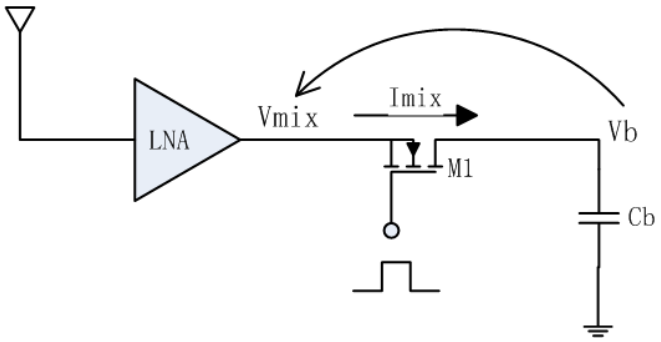


Fig. 3.5. Illustration of the translational impedance concept.

Consider a practical scenario as in figure 3.5, in the first stage, a trans-conductance LNA converts input voltage signal into a current I_{mix} which flows into the passive mixer in the second stage. This current is downconverted by the passive mixer to the baseband and again converted into voltage V_b with a simplified baseband load capacitor C_b. For input signals around LO frequency which is downconverted to DC, baseband capacitor presents very large impedance hence leading to a large voltage signal; whereas for out-of-band interferences, capacitor C_b shunts most of the current to ground. Due to the lack of reverse isolation, this baseband voltage V_b is again upconverted to LO frequency, noted by V_{mix} in the graph. Defining mixer impedance as V_{mix}/I_{mix}, this translated impedance only presents a large value at the LO frequency with the baseband filter profile being translated to RF frequency.

3.4 Summary

In this chapter, a theoretical model was established for analyzing the behavior of passive mixer. Oversampling mixer with higher sampling frequency reduces harmonic mixing and conversion loss. However, multiple phase signals put extra burden on LO generation circuit.

CHAPTER 4 HIGH SPEED FREQUENCY DIVIDER DESIGN

4.1 Introduction

Divide-by-N circuits takes an incoming square wave at frequency f_s and output a square wave with a frequency of f_s /N. Frequency divider is widely used in Phase-Locked Loops (PLL) to compare the output with the reference waveform. Phase-Frequency Detector (PFD) compares the reference signal and the divided output to generate an error signal representing the phase difference between two inputs. This error signal is further utilized to adjust Voltage Controlled Oscillator (VCO) for accurate output frequency.

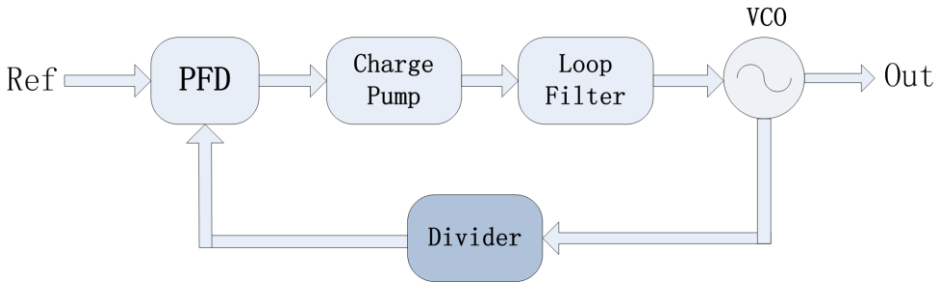


Fig. 4.1. Conceptual block diagram of a PLL.

The most basic frequency divider divide-by-2 circuit or Johnson counter can be implemented with a D-flipflop connecting its negative output to the input D port. One pulse is generated for every uprising edge or falling edge. Divide-by-2^N circuit can be implemented with N divide-by-2 circuit connected in serial. However, this leads to a relatively high phase noise or jitter since jitter in every stage is accumulated to the final output. In a synchronous design, each pulse is generated with a clock edge with a jitter performance only dependent on the clock signal. A synchronous divide-by-4 circuit could be

implemented as follows:

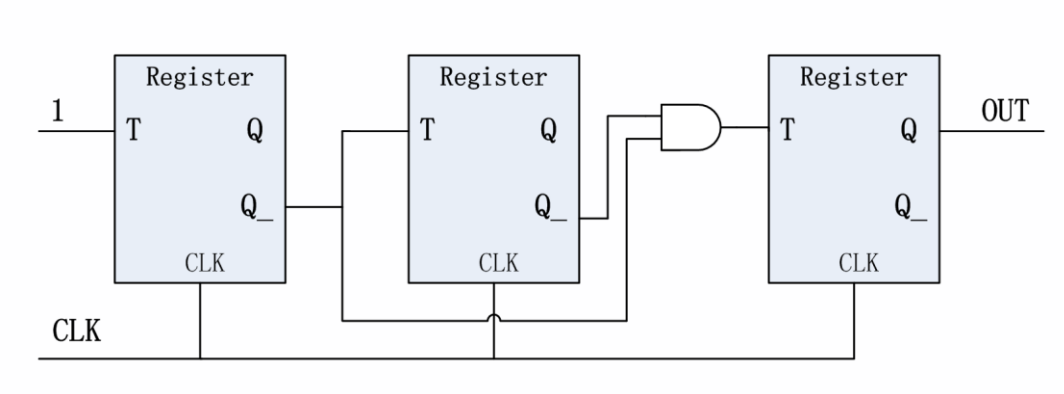


Fig. 4.2. Synchronous frequency divider.

For more variable dividing ratio, a divide-by-2/3 is usually utilized as the building blocks. Register B acts as divide-by-2 circuit. In normal mode of operation where CON* is low, register A is disabled and divider acts as a divide-by-2 circuit. When CON* is high, register A would swallow one of the pulses from register B output and register B would remain high for one extra high cycle. In this way, the entire circuit is a divide-by-3 circuit. By connecting multiple divide-by-2/3 circuits together, dividing ratio could be programmed to be multiple values.

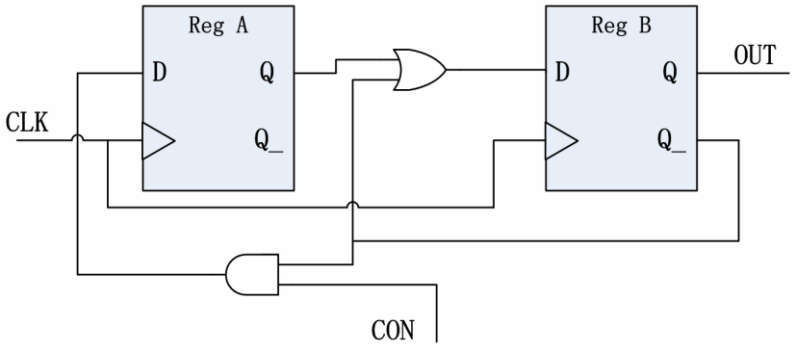


Fig. 4.3. Divide-by-2/3 divider.

4.2 Current Mode Logic

The most common implementation for digital circuit is CMOS logic. The complementary

PMOS and NMOS circuits pull the output capacitor to Vcc and ground respectively. Compared with alternative logic circuit approaches, CMOS is simpler in terms of design and control especially for Very Large Scale Integrated circuit (VLSI) design. However, for simple logic circuits, Current Mode Logic (CML) can operate at a higher speed than CMOS. Thus for high speed divider in our design, CML was adopted.

The basic building block for CML is a differential pair. Differential input voltage steers tail current between either branch to express logic high or low. Rather than rail-to-rail voltage swing in CMOS logic, the voltage swing in CML is actually controllable by the designer. The only requirement for voltage swing is to be high enough to drive the next stage. For BJT differential pair, this puts a lower limit of $4V_T$ which leads to a peak to peak value of 300mV; whereas for MOS differential pair, the lower limit depend on the relation between device size and tail current. Generally speaking, MOS pair needs a higher input swing than BJT pair.

The speed advantage of CML over CMOS bears from its difference at output node. Rather than using PMOS transistor, a load resistor is used in CML. The time constant at output node is determined by $1/R_LC_L$ and R_L is determined by the target voltage swing:

$$V_{swing} = R_L I_{tail} \tag{4.1}$$

For higher speed, we need a small load resistance and a higher tail current is needed if output voltage swing is to be fixed. In this way, a tradeoff between speed and power consumption is established. Moreover, if we compare the power consumption between CMOS and CML, higher efficiency is achieved by CML for high speed logic. Depending on the actual circuit and technology used, this boundary between CML and CMOS could be from

hundreds of MHz to several GHz [8].

4.3 A four-phase shift-register

To generate a four-phase clock square wave, we took an incoming sine wave signal four times the LO frequency. A chain of differential amplifiers reshape and buffer the signal to drive a shift-register consisting of four flip-flops in *Current Mode Logic (CML)*. The key for fast CML is to have a very small resistor as the load to achieve a low RC time constant at the output. However, to acquire same amount of voltage swing, a smaller load resistor needs a higher current. In this way, a faster CML needs more power consumption.

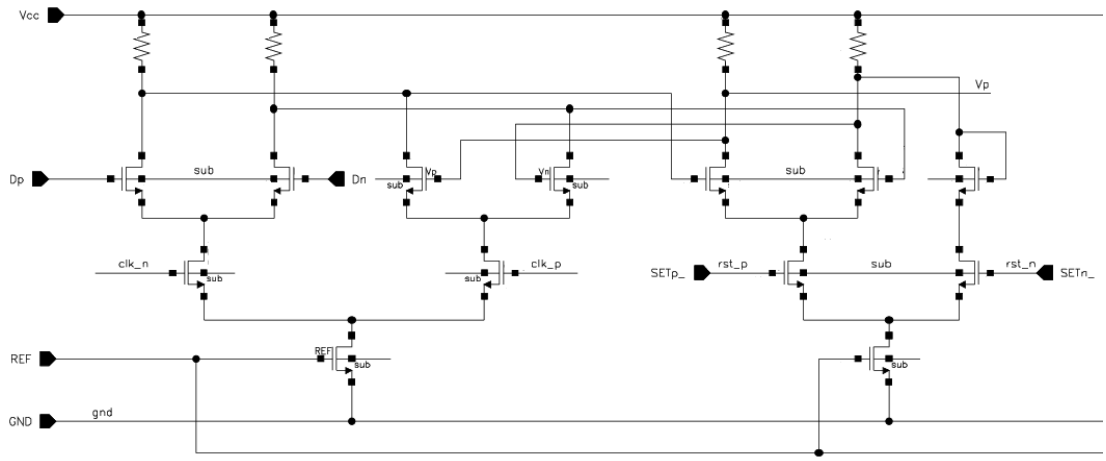


Fig. 4.4. Schematic diagram of a folded D-Latch with reset.

The basic building block D-flipflop is made up with two latches in serial. A tail current of about 1mA is chosen for each branch. For a 400mV voltage swing, a load resistor of 400 Ohms was adopted as shown in figure 4.4. One of the disadvantage of CML is that a higher amount of stacking also lead to higher requirement on voltage headroom. To reduce the layer needed, we used a folded structure to get one layer off. In our design, each level adds an extra 0.5V to the overall voltage headroom. Including the voltage swing on the load

resistor, this gives a total voltage of 1.8V. A Vcc voltage of 2V is chosen finally just to be safe.

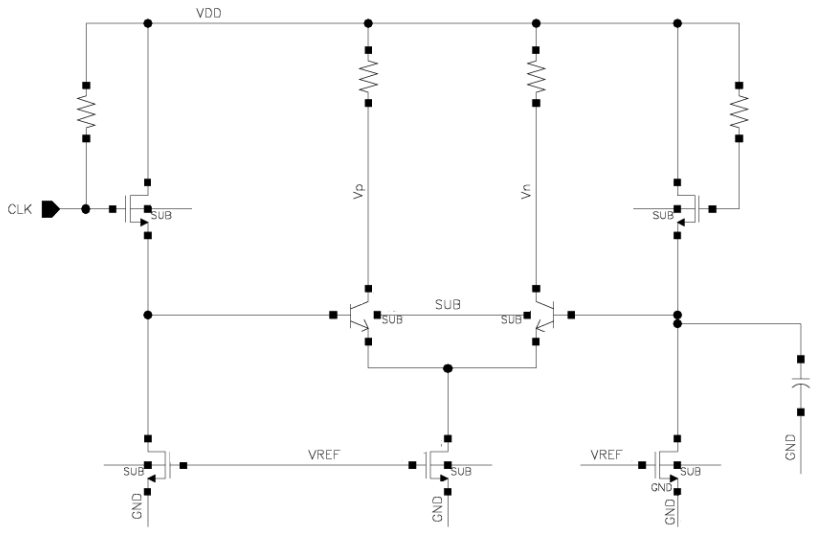


Fig. 4.5. Schematic diagram of a single to differential buffer.

As shown in figure 4.6, one of the four flipflips is pulled to high while all the others are pulled to low during startup. The high state is shifted through the chain repeatedly. A buffer which is also a differential amplifier takes the output of flipflops and converts the voltage swing to that needed by the mixer. Through using a synchronized clock circuit, the noise contribution from this division network is minimized. With some careful layout controlling the delay from the output of flipflops to the mixer, minimum overlap between different phases is achieved.

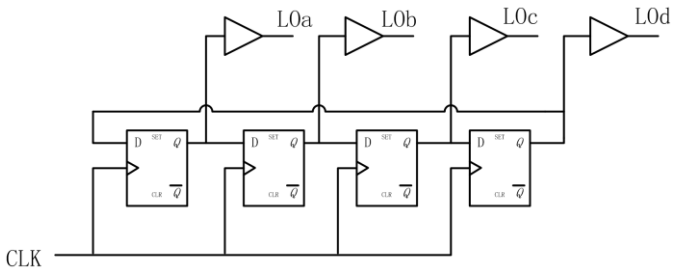


Fig. 4.6. Block Diagram of a four-phase clock generator.

4.3 Summary

This chapter introduces some of the basic design principles behind high speed frequency dividers. CML, as one of the implementation of high speed digital circuit, is readily presented. Basic tradeoff between speed and power consumption is introduced as well.

CHAPTER 5 BLOCKER TOLERANT RECEIVER FRONTEND DESIGN

5.1 Architecture Overview

Due to its good linearity with OBI suppression capability, the passive mixer has been the focus of academic research recently as the most promising solution to highly flexible SDR frontend. However, most of the proposed structures either use a mixer-first approach or a conventional LNA with input matching. The mixer-first strategy gives a relatively poor noise figure since the first stage amplification is lost. Using passive mixer with conventional structure would otherwise require a highly linear first stage LNA. The alternative approach we proposed is more like a compromise between these two types of architecture.

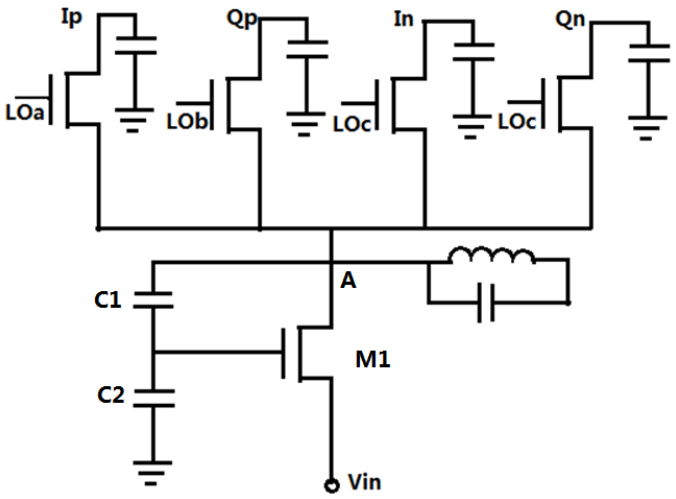


Fig. 5.1. Proposed SDR frontend schematic.

In our proposed novel structure, the filtering property of passive mixer is transferred to the input of the LNA which helps relaxing the LNA linearity requirement. As shown in figure 5.1, common gate amplifier acts as the first stage LNA. A large integrated inductor is

attached as a DC current feed for transistor M1. Parasitic capacitance at the output node is modeled with the tank capacitor. Output current from LNA is passed to a four-phase passive mixer. Due to the translated impedance from the baseband, a voltage signal would be developed at node A only around the LO frequency. The capacitor divider network further feeds it back to M1's gate.

Due to its time varying property, it is difficult to directly model the mixer with its small signal model. A possible approach is to separate the RF circuit into two parts: one for the "Linear Time Invariant" (LTI) part including the LNA; another for the "Linear Time Variant" (LTV) part including the mixer. As shown in figure 5.2, the lower LTI part consists of the LNA with its capacitive feedback; the upper LTV part consists of the mixer which is presented in chapter 3. Note that the on-resistance of the mixer switches is extracted into the LTI circuit in the analysis as well, leaving ideal switches for the LTV analysis.

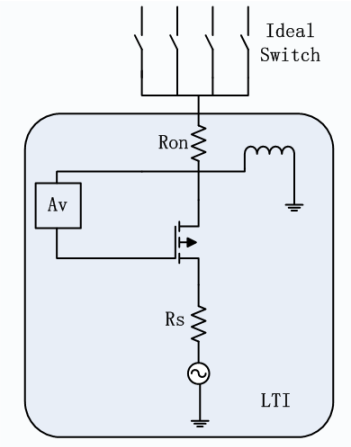


Fig. 5.2. Model for LTI analysis of the proposed architecture.

5.2 Input Matching

As discussed in chapter 2, the input impedance of the LNA can be expressed as:

$$\text{Zin} = \frac{1}{g_m} + Av \cdot Z_L \tag{5.1}$$

Thus, we can adjust the size of C_1 and C_2 such that the LNA presents a 50 Ohm impedance at the LO frequency and a small impedance ($1/g_m$) for the OBI. Hence, the LNA is only matched for the targeted frequency bands. Furthermore, this load impedance can be expressed by:

$$Z_L = Z_{mL,fold}(w)||Z_{MX}(w)$$

$$= \left(\sum_{k=-\infty}^{+\infty} \frac{1}{(4k+1)^2 Z_{mL}(w + 4kw_{LO})} \right) || \frac{2}{\pi^2} (Z_{BB}(w - w_{LO}) + Ron) \tag{5.2}$$

where:

$$Z_{mL}(\mathrm{w}) = \frac{1}{sC + \frac{1}{sL} + \frac{1}{Z_{AV}}} \tag{5.3}$$

$$Z_{AV} = \frac{1}{A_V} \left(R_S + \frac{1}{g_m} \right) \tag{5.4}$$

Here g_m is the trans-conductance of the first-stage LNA, C is the total capacitance presented at node A and L is the tank inductance. The load impedance at harmonics of LO is also relevant because baseband voltage is up-converted to all the harmonics of LO. *An intuitive way to think about this is that the baseband is driving the load impedance as well as its copies at the LO harmonics*.

5.3 Noise Analysis

Major noise contributions come from input matching transistor M_1 and mixer switching resistance R_{on}. To calculate the noise contribution from each source, we need to calculate the noise presented at the output node only considering each individual noise source. First for the source thermal noise, by converting the LTI part into its Norton equivalent circuit, the current

source I_n can be found out as:

$$I_{N,Rs} = \frac{\sqrt{4kTR_S}}{R_{on}Av + \left(\frac{1}{gm} + Rs\right)\left(1 + \frac{Ron}{ZL}\right)} \tag{5.5}$$

The Norton current source for LNA transistor channel thermal noise can be derived as:

$$I_{N,M} = \frac{\sqrt{4kTg_m\gamma}}{g_mR_{on}Av + (1 + g_mRs)\left(1 + \frac{Ron}{ZL}\right)} \tag{5.6}$$

Moreover, the thermal noise from switch on-resistance is given by:

$$I_{N,sw} = \frac{\sqrt{4kTR_{on}}}{R_{on} + Z_L||Z_{AV}} \tag{5.7}$$

The Norton equivalent source impedance can be shown to be the same for three noise sources, namely:

$$Z_N = R_{on} + Z_L||Z_{AV} \tag{5.8}$$

Now we can relate I_n to the noise presented at the output and calculate the overall noise figure correspondingly:

$$\text{NF} = 1 + \frac{\gamma}{g_mRs} + \frac{Ron}{Rs} \cdot \left(\frac{1}{gm} + Rs\right)^2 \cdot \frac{\sum_{g=-\infty}^{+\infty}\left(\frac{|Sw[m-gM]|}{|Sw[m]|} \cdot \frac{1}{Ron + Z_{L,g}||Z_{AV}}\right)^2}{\sum_{g=-\infty}^{+\infty}\left(\frac{|Sw[m-gM]|}{|Sw[m]|} \cdot \frac{1}{1 + \frac{Ron}{Z_{L,g}}}\right)^2} \tag{5.9}$$

where $Z_{L,g}$ represents the load impedance at the (m-gM)th harmonic of the LO. In the above equation, the second term represents noise from LNA and the third represents that from the mixer switches. There are three conclusions we can draw from this equation:

1. To suppress the noise from the LNA, we need to use a large transistor with large trans-conductance gm.

2. To suppress the noise from the switches, we need to guarantee a large load impedance Z_L at the LO frequency as well as its harmonics.

3. Decreasing Ron does not necessarily decrease the noise from the switches.

Interestingly the noise contributed by the mixer from its fundamental LO frequency only adds a small amount of the total noise. We can show this by plotting $(\frac{|Sw[m-gM]|}{|Sw[m]|} \cdot \frac{1}{Ron+Z_{L,g}||Z_{AV}})^2$ at different harmonics of the LO as shown in figure 5.3. The ditch in the center represents the noise contribution from LO fundamentals. Suppose using a LC tank as the load which is the case for this design, if the load impedance reduces at a faster pace than the switching coefficient $\frac{|Sw[m-gM]|}{|Sw[m]|}$ as the frequency increases, the mixer switches are likely to present a very large noise at the output due to its higher harmonics. To counter-act such effect, we need to slow down the sinking pace of the tank impedance which could be done with smaller tank capacitance and larger inductance.

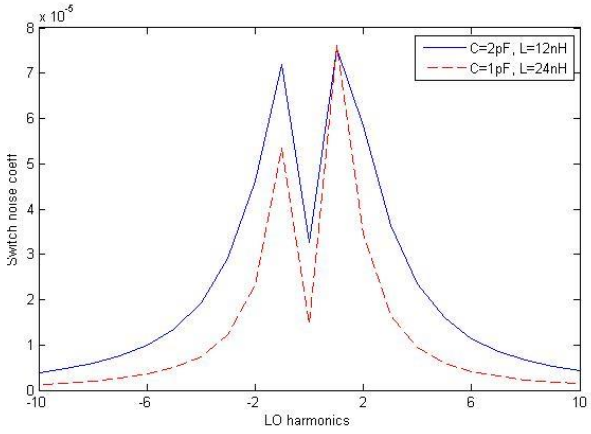


Fig. 5.3. Mixer noise coefficients.

5.4 Simulation Results

The final design was implemented in 0.18um SiGe BiCMOS technology. Shown in figure 5.4 is the layout diagram for the entire receiver frontend. An HBT with a 16/0.2 length to width ratio is used in the first stage LNA with negative feedback for both matching and amplification. The DC current is set to be 3mA to achieve a transconductance of 110mS. MOS switches used in the passive mixer have a length to width ratio of 104/0.18 to achieve an on-resistance of 30 Ohms. The total area occupied is 1.5mm^2. A supply voltage of 2V is chosen and simulation shows a power consumption of 128mW. A large inductor was used for DC current feed at LNA output node. The final inductance value is 22nH and a quality factor is simulated to be about 14. Large array of dc coupling capacitance was also used for power noise suppression.

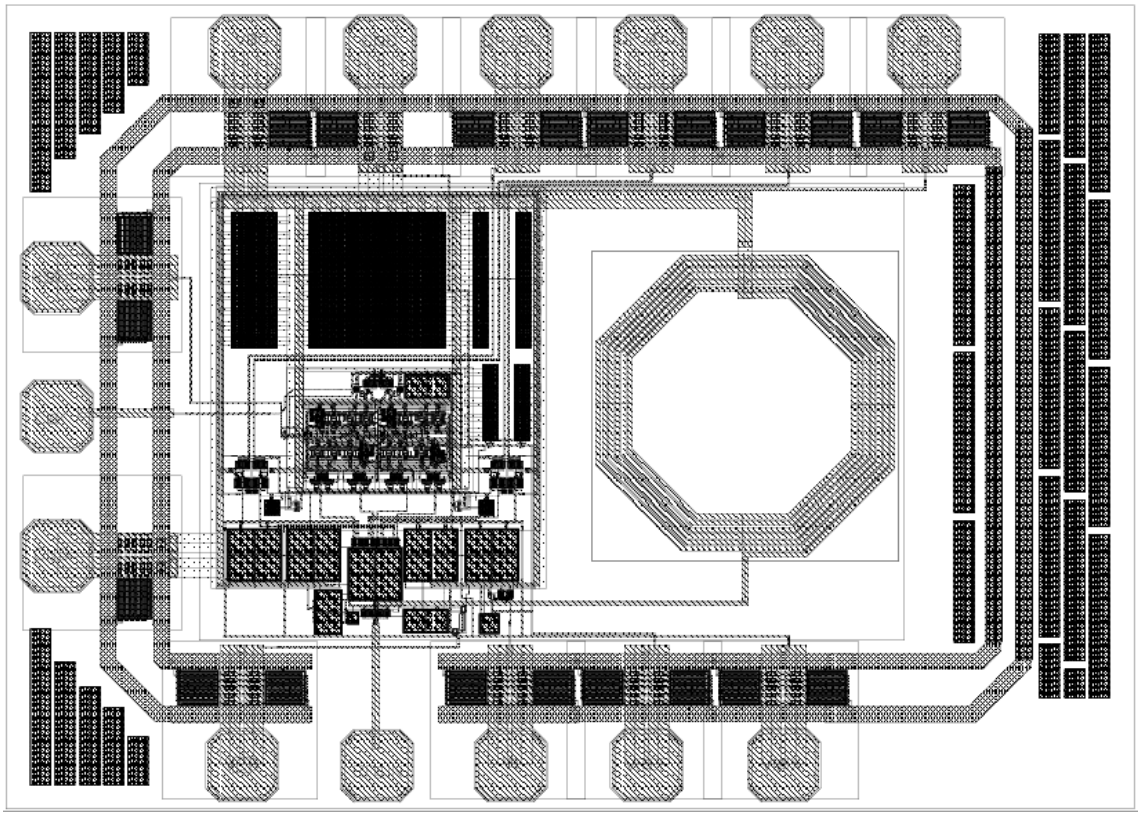


Fig. 5.4. SDR receiver layout diagram.

Circuit performance at different LO frequency was estimated with post-layout

simulation. Due to limitation from LO signal generation circuitry, the frequency divider stops working for frequency higher than 1GHz. In this way, three LO frequencies were simulated at 0.8, 0.9 and 1.0GHz respectively. A minimum noise figure of 4.28dB is achieved as shown in figure 5.5.

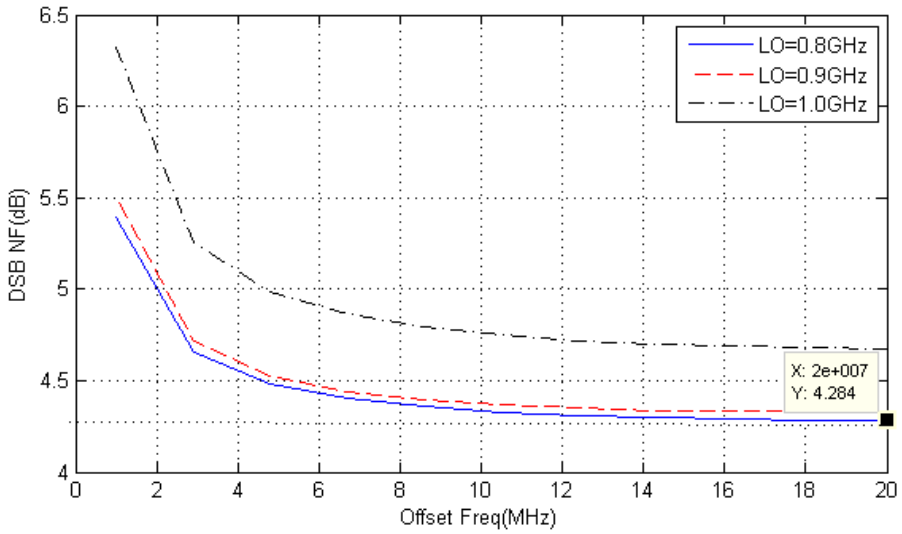


Fig. 5.5. Simulated double sideband noise figure.

The following diagram shows that receiver is indeed only matched in a limited band around LO frequency.

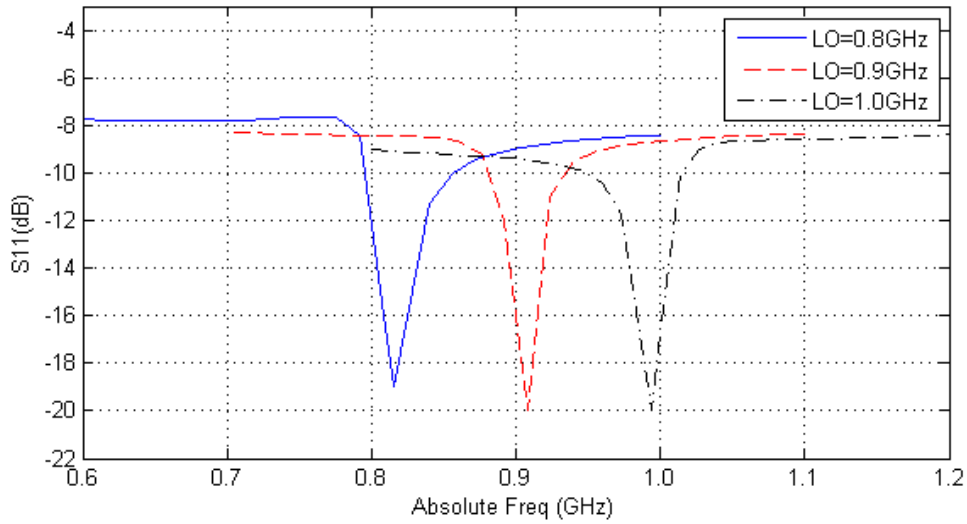


Fig. 5.6. Simulated S11 for input matching.

Shown below is the gain profile of the first stage LNA. Variable loading causes large gain to be centered around LO frequency. A filtering of 10dB is achieved.

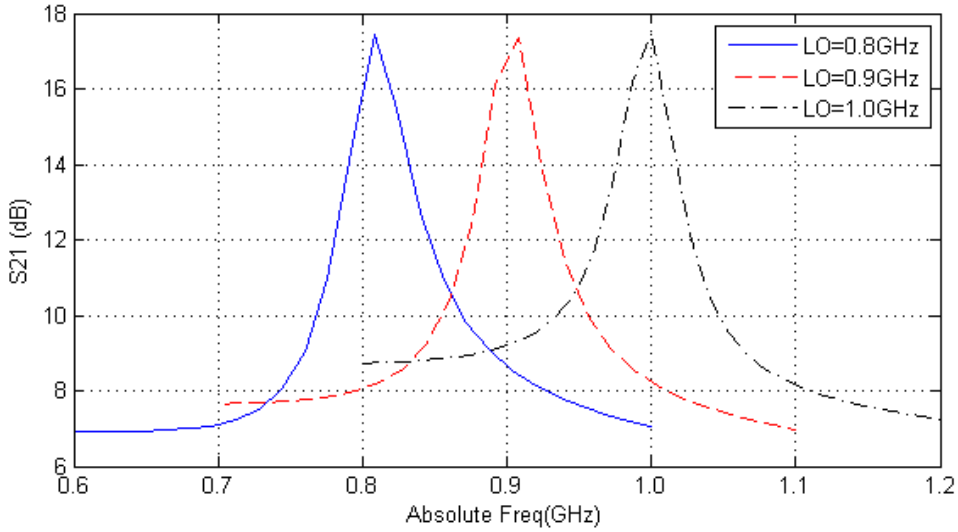


Fig. 5.7. Simulated S21 for LNA gain.

5.5 Summary

An SDR receiver inherently requires the frontend to operate over a wide bandwidth and the associated interferences could easily desensitize the frontend. To tackle this problem, a novel RF-frontend with out-of-band interferences rejection using capacitive feedback and passive mixer techniques has been presented. Simulation results demonstrate a 10dB filtering for out of band interferences with an overall noise figure of 4.3dB.

CHAPTER 6 Conclusions

In this thesis, the main objective is to improve current approaches to SDR frontend. Extensive effort was put in noise reduction, linearity improvement and interference robustness. In order to maintain the flexibility of SDR frontend for cognitive radio application, conventional filtering using SAW filter has to be discarded. Passive mixer, on the other hand, imposes one possible solution to this challenge as the filtering profile is adjustable with LO frequency. The basic principle behind passive mixer is to do the necessary filtering at baseband and upconvert the filtered signal to RF frequency, or namely the “Translation Impedance”. However, due to this down/up-conversion operation, the filtering capability is very limited due to harmonics and distortions. This could indeed be improved with oversampling mixer where harmonics mixing is reduced, but there is a limit to what a high sampling frequency mixer could achieve, say 20dB of filtering. This is still far from the desired filtering capability that SAW filter could provide.

Large power interference could be handled either as voltage or current in RF circuits. Voltage signal is limited by the upper level which is usually the power voltage level. And this upper limit usually varies from 1V to 2V for modern integrated circuits. On the other hand, current signal does not have such constraint to be flowing in the circuit. Thus it is preferred to handle interference signal in the current domain. However, a high current signal also runs the risk of significantly disrupting the operating condition or Q-point of transistor which could lead deteriorated linearity performance. It would be more beneficial to filter out all

the interference in current domain prior to any baseband processing in voltage domain.

Classic LNA-mixer pair as the very first stage in conventional receiver frontend is under much scrutinization for SDR design. Since first stage LNA presents a bottleneck for linearity, structures directly using passive mixer alone was proposed. Even though featuring a higher P1dB and IIP3 point, mixer-first approach has a relatively poor noise performance. The idea behind our design is to utilize this flexible narrowband property from passive mixer to help relaxing the linearity requirement on LNA to provide a better performance for both sensitivity and linearity. With the negative feedback from the passive mixer, input LNA is only matched at target signal band.

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