THERMO-MECHANICAL RELIABILITY MODELS FOR LIFE PREDICTION OF AREA ARRAY ELECTRONICS IN EXTREME ENVIRONMENTS

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THERMO-MECHANICAL RELIABILITY MODELS FOR LIFE PREDICTION OF AREA ARRAY ELECTRONICS IN EXTREME ENVIRONMENTS

Naveen Chandra Singh

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THERMO-MECHANICAL RELIABILITY MODELS FOR LIFE PREDICTION OF AREA ARRAY ELECTRONICS IN EXTREME ENVIRONMENTS

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VITA

Naveen Chandra Singh, son of Dr. R. S. Singh and Smt. Pratima Singh, was born on October 05, 1975, in Varanasi, Uttar Pradesh, India. He graduated in 1997 with a Bachelor of Engineering degree in Aeronautical Engineering from Punjab Engineering College, Chandigarh, India. After his baccalaureate he joined Punjab Tractors Ltd. (PTL) as a Management Trainee in July, 1997. He worked at PTL's R&D Divison on various research projects in the capacity of Research and Development Engineer for more than 5 years. In the pursuit of enhancing his academic qualification he joined the M.S. Program at Auburn University in the Department of Mechanical Engineering in Spring, 2003. Ever since he enrolled for the M.S. program at Auburn University, he has worked under the guidance of Professor Pradeep Lall, in the Department of Mechanical Engineering and the Center for Advanced Vehicle Electronics (CAVE), as a Graduate Research Assistant in the area of harsh environment electronic packaging reliability.

THESIS ABSTRACT

THERMO-MECHANICAL RELIABILITY MODELS FOR LIFE PREDICTION OF AREA ARRAY ELECTRONICS IN EXTREME ENVIRONMENTS

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The increasing functionality in modern microelectronics requires more complexity in less space and more reliability at lower cost. Demands on miniaturization have lead to the evolution of several types of area array packages like PBGA, Flex-BGA, Flip Chip CSPs etc. Area array packages have been increasingly targeted for use in harsh environments such as automotive, military and space application but the thermomechanical reliability of these packages in such environments is a concern for the electronic industry. Several approaches are available today for reliability prediction including non-linear finite element models and first-order closed form models. The first-order models as the name suggests offer limited accuracy.

In this thesis, a unique hybrid approach to reliability prediction, in order to achieve accuracy beyond the closed-form first-order approximations, has been presented. The perturbation approach presented in this paper enables higher-accuracy model prediction by perturbing known accelerated-test data-sets using models, using factors which quantify the sensitivity of reliability to various design, material, architecture and environmental parameters. The models are based on a combination of statistics and failure mechanics. In addition, parameter interaction effects, which are often ignored in closed form modeling, have been incorporated in the proposed hybrid approach. The statistics models are based on accelerated test data in harsh environments, while failure mechanics models are based on damage mechanics and material constitutive behavior.

The framework formulated from the models is intended as an aid for understanding the sensitivity of the component reliability to geometry, package architecture, material properties and board attributes in different thermal environments. The intent is to develop a decision-support system for doing trade-offs between geometry, materials and quantitatively evaluating the impact on the reliability. Convergence between the statistical model sensitivities and failure mechanics based sensitivities has been demonstrated. Predictions of the sensitivities have been validated against the experimental test data.

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CHAPTER 1

INTRODUCTION

The role of packaging [Tummala, et al. 1997] in electronic device is, signal and power distribution, heat dissipation and protection from the environment, loads and stresses. Electronic packaging may be understood as the embodiment of the electronic devices and establishment of electrical interconnection among the devices for some useful application. The advances in the semiconductor fabrication being driven into the nanometer range [Isaac, 2005], has mounted the pressure on the IC (Integrated Circuit) packaging technologies. The sophisticated packaging design solutions once considered cutting edge or deemed too costly have moved into the mainstream to meet the needs of the commercial products.

1.1 Area Array Packaging: Key to the Miniaturization of Electronics

The extreme miniaturization in the electronic devices has lead to the evolution of area array packaging technology. Due to the increase in the device density of the IC chips, the number of input-output interconnections (I/Os) for the same sized chip have grown up to an extent that the perimeter of the packaged chip is not sufficient to accommodate all the I/Os, thus driving the packaging technology towards the area array interconnection [Lau 1996, 1997] in order to accommodate the ever increasing I/Os.

Area array packaging with surface mount technology [Harper, 2004] has emerged as the solution for the problem posed by the extreme miniaturization in electronics for the high density IC packaging. The IC packaging technology [Suhling, 2003] in the past has evolved from the inline and peripheral array packages such as single inline package (SIP), dual inline package (DIP), plastic leaded chip carrier (PLCC), quad flat package (QFP) or leadless ceramic chip carrier (LCCC) to an area array packaging such as ball grid array (BGA), flip-chip, chip scale packages (CSP) and multi-chip modules (MCM). The mounting technology [Suhling, 2003] for the IC packages has evolved from the earlier plated through hole (PTH) to the current state-of-art surface mount technology (SMT).

1.2 Thermo-mechanical Reliability: A Concern for Area Array Packaging

The operation of any electronic device generates heat and with the increasing device density of the IC chips the amount of heat flux generated by the IC chips has gone to a level of 100-200 W/cm² [Nimkar, et al. 2005]. Due to this, whenever a device is switched on, the electronic components heat-up and than cool down after the device is switched off. This leads to a thermal cycling of the device and since the different packaging components have different coefficients of thermal expansion (CTE), as shown in the Figure 1.1, there is a differential in expansion of various components. This thermal expansion differential causes stresses in the various components and the continuous thermal cycling of the device due to on-off switching during it's usage life finally leads to the fatigue failure of the device. The fatigue failure of the device can occur in various different modes [Viswanadham and Singh, 1998].

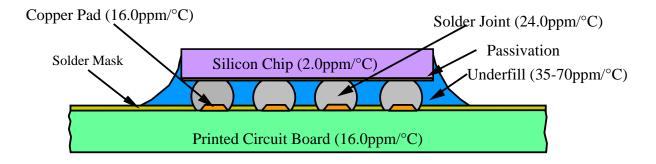


Figure 1.1 Various components of a flip-chip package with the corresponding approximate coefficients of thermal expansion (CTE) values.

One of the common failure modes in electronic packages is the 'Pop Corn Failure' which occurs during the re-flow due to the moisture content in the mold compound of the package. Ilyas and Roberts [1993] analyzed the sensitivity of the moisture in electronic package, on the package failures and attributed failure to 3 different types of cracking depending upon the moisture content, chip size, and other package dimensions. Ilyas and Roberts [1993] investigated the moisture sensitivity in several surface mount packages that included SOJ, PLCC, TQFP, and PQFP packages. Yip, et al. [1996] studied the moisture induced failures in case of Ball Grid Array packages, PBGA and TBGA packages were used in the study. It was established that 16 hours baking at 115°C essentially removes most of the moisture from the package, hence reducing possibility of the interfacial delamination and pop-corn cracking of the package. Lee, et al. [1996] analyzed and proposed a new lead frame design for improved reliability of the packages by encountering the pop corn cracking. Guzman, et al. [1996] in their study on the package cracks during the assembly process addressed various issues that lead to package cracking at the assembly stage, such as flashing of the excess plastic molding compound, lead forming operations and package singulation. Measures for eliminating the assembly induced package cracks for plastic SOIC packages were proposed.

Silicon die cracking is another failure mode that takes place due to the thermal stresses developed in the chip. The stresses might develop during the assembly stage or during the thermal cycling of the component due to the CTE mismatch within the package. Efforts as early as 1970's [Dale and Oldfield 1977] have been made to analyze the stresses developed in the plastically encapsulated devices during the assembly and use. Lau [1993] has addressed the stresses generated during the packaging processes

such as wafer preparation, oxidation, diffusion, metallization, die and wire bonding, encapsulation, re-flow and curing. Edwards, et al. [1987] evaluated shear stresses during thermal cycling and thermal shock tests in the plastic packages and found that the shear stresses are heavily concentrated at the corners and edges of the silicon die. Okikawa, et al. [1987] analyzed plastic molded LSI packages subjected to thermal cycling and found that thermal stresses cause passivation film cracks in the package. Jaegar et al. [1993, 1997] and Gee, et al. [1995] designed a test chip and piezoresistive sensor for detecting thin film cracking and measurement of stresses in the electronic packages. Suhling, et al. [1999] measured flip chip die stresses using piezoresistive test die, and Zou, et al. [1999] analyzed the die surface stress variation during thermal cycling and thermal aging raliability tests.

Thermal stresses developed due to the CTE differential during assembly or thermal cycling can also lead to interfacial delamination, which may result in package failure. Moore, et al. [1991, 1992] used C-SAM (C-Mode Scanning Acoustic Microscope) for detecting delamination in the plastic packages by polarity analysis of reflected acoustic pulses and analyzed the impact of delamination on the stress induced failures on surface mounted ICs. Doorselaer and Zeeuw [1990] developed relation between delamination and temperature-cycling induced failures in plastic packaged devices. Van Gestel, et al. [1992] compared the effect of delamination on plastic packaged devices subjected to temperature cycling test and highly accelerated stress test. Zou, et al. [1998] analyzed the effect of delamination on the die surface stresses and conducted the stress measurements delaminated and non-delaminated plastic packages.

With the shrinking interconnect size, the solder joint becomes the weakest link in the overall package reliability. It has been established from various studies and failure analyses [Harmon 1974, Engelmaier 1984, Katlowitz 1986, Hwang 1988, Solomon 1989, Tien, et al. 1989, Lau 1991, Lall, et al. 1997, 2003, 2005, Suhling, et al. 2004] that the interconnect failure due to the thermal cycling, as shown in Figure 1.2 is the most critical mode of failure in various leaded and SMT packages such as BGA and flip-chip. Solder joint failure has remained a serious concern and area of extensive research in electronic packaging reliability. Vishwanadham, et al. [1993] and Emerick, et al. [1993] looked at the solder joint reliability aspects of TSOP (Thin Small Outline Package) and proposed method for enhancement of solder joint reliability by using encapsulation. Solder alloy of various compositions have been conventionally used as the interconnect material in electronic packages, eutectic solder (Sn63 Pb37) being the most popular choice, but the RoHS (Restriction of Hazardous Substances) legislation [Iscoff, 2005] and the stringent norms of EPA (Environmental Protection Agency), has made it inevitable for the electronic industry to look for Pb-free solder alloys. Multitude of research studies [Lau, et al. 2004, Wiese, et al. 2001, Zahn 2002, 2003, Kim et al. 2003, Schubert et al. 2002] have been performed and are still underway to determine the most suitable Pb-free replacement, although no particular replacement has been so far identified for all the applications, but the SAC alloy (SnAgCu) has emerged out as the most popular choice.

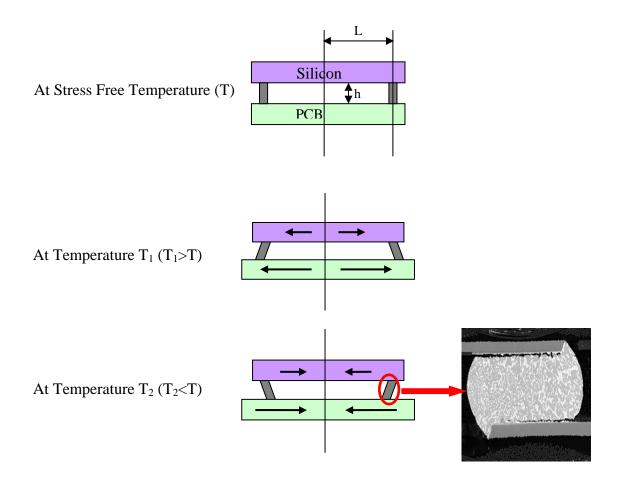


Figure 1.2 Solder joint fatigue failure due to thermal cycling

1.3 Factors Affecting Packaging Design and Selection

Today, the OEMs have several options for making selections among the COTS (commercial of the shelf) IC devices, for their product. But it is of utmost importance for the manufacturer to understand the reliability of the selected devices for the given application, because the failure of any one of the selected device would result in the failure of the whole product. In case, reliability was the only factor for consideration then one could have selected most robust components designed with very high reliability, but that's not the case. In a real situation factors like production yield, cost, size and weight also play a vital role, keeping these factors in mind the manufacturer has to be very wise and precise in his judgment for the design and selection of appropriate components.

1. Exposure to the Environment: The ever increasing use of electronics in various applications and technological areas has simplified and helped the development in those areas, but it has certainly complicated the design and development of electronic packaging, since the same device in different products calls for a different packaging technology as the environment to which the device is subjected, varies with the application. A product to be used for automotive [Adams et al. 1998, Evans et al. 1997, Jung et al. 1998, Mawer et al. 1999] or space application is subjected to much harsher vibration, shock and thermal environment as compared to the product such as a workstation [Ray, et al. 1997], microwave [Bedinger, 2000], cellular application [Sillanpaa et al. 2004] power electronics [Liu,et al. 2001] application thus requiring more robust packaging as compared to the devices to be used in the office environment desktops.

- 2. <u>Size</u>: Size of the product is another governing factor that drives the packaging technology to be used for the electronic devices. Most of the electronic products have witnessed a drastic decrease in their size, which is visible if one compares the size of the mobile phones today with those of five or ten years back. The space or size constraint also depends on the product for example the desktop computer can have much larger space for housing all the electronic devices and circuits as compared to the laptops, therefore the similar devices to be used for the laptops need to have much smaller packaging.
- 3. <u>Cost</u>: One of the most important factors driving most of the technological developments in any industry is the cost reduction. Due to the ever increasing competition in the market the seller has no option but to go for the cost reduction of the products in order to have an edge over the other competitors. The time has gone when the high factor of safeties were used, now the performance of the products can be more precisely determined thus leading to much lower safety margins and cost savings. Various technological developments in the materials and process engineering have been accomplished in the area of electronic packaging in order to reduce the cost of the final product.
- 4. <u>Product Life</u>: The product life is one of the critical factors governing the type of packaging technology to be used for the electronic devices for any particular product. Using the components having life higher than the life for which the product is designed unnecessarily adds to the cost of the product, on the other hand the life of components cannot be less than the designed life of the product, otherwise the product will fail earlier

than it's designed life. Thus the packaging technology that optimizes the life of the components with that of the product life has to be developed.

There are multiple ways in which one can analyze these factors for making appropriate selection of the components that will have optimum life. One way is to conduct accelerated experimental testing and correlate it with the field conditions. This is a very tedious and time consuming process, thus adding to the cost of the product and delaying the arrival of the product in the market. The other option is FEA based computational simulation, which is much faster, but it requires highly specialized and skilled user otherwise it is just a weapon in the hands of an incompetent user. Another viable option is to take help of closed form analytical models based on mechanics of failure or statistics for analyzing the effect of various parameters. This option provides a tool which is very quick and easy to use and does not require high skill.

CHAPTER 2

LITERATURE REVIEW

Solder joint failure due to thermo-mechanical fatigue is the most critical factor in the reliability of the area array packages [Giulio 1997, Harper 2004]. This makes the solder joint reliability analysis one of the most important and focused issue as far as the reliability and life of the electronic packages is concerned. Multitude of published literature addressing solder joint reliability and life prediction is available. Various methodologies used in these literatures for the solder joint fatigue life prediction of area array packages include, experimental techniques (accelerated thermal cycling tests), closed form models based on the theory of failure mechanics, finite element analysis (FEA) and statistics based regression models.

2.1 Experimental Techniques

Several experimental tests, such as accelerated thermal cycling, thermal shock, HAST (highly accelerated stress test) and vibration test, have been used by the researchers in the past to analyze the solder joint fatigue life for qualifying the components for different applications. Darveaux, et al. [2000] conducted several board level thermal cycle reliability tests, the packages used included Flex-BGA, TABGA (Tape Array Ball Grid Array), PBGA and µBGA. Various package and board variables were included in the test matrix, and it was found that fatigue life increased by up to 6X

as dies size was reduced, and for a given die size, fatigue life was up to 2X longer for larger packages, and solder joint fatigue life was 20% longer for 0.9mm thick test boards compared to 1.6mm thick boards. 1.6X acceleration factor between -40°C to 125°C and 0°C to 100°C was also reported.

Mercado, et al. [2000] conducted test on flip chip PBGA package for FSRAM (Fast Static RAM) application in order to analyze the effect of pad size and substrate thickness on the solder joint reliability. It was reported that C5 solder joints with larger solder pad and thicker substrates demonstrated higher reliability. Hung, et al. [2000] investigated the effect of chip size, surface finish, Au plating thickness, epoxy thickness, polyimide thickness and underfilling on the interconnect thermal cyclic fatigue life by conducting experimental test on Flex-BGA packages. Chip size, polyimide thickness and underfilling were found to have significant impacts on the joint fatigue life, epoxy thickness was found to have little effect on the joint fatigue life.

Mitchell, et al. [2004], conducted thermal cycling tests for the BLR (board level reliability) analysis of multiple stacked die chip scale package configurations, three different CSP test vehicles, 8x11mm, 13x13mm and 15x15mm, with twelve different package configurations of the 1-to-5 die stacks were evaluated. No consistent trend of BLR performance relative to die stack configuration was found.

2.2 Statistical Analysis

Researchers have used different statistical methods for the analysis of the experimental test failure data, the most common being regression analysis and Weibull distribution. Clech, et al. [1994] presented statistical analysis of thermo-mechanical wear

out failure data from 26 accelerated tests and tested the goodness-of-fit using two and three parameter Weibull and log-normal distributions. It was concluded that the three parameter Weibull treatment provides more accurate reliability projections and failure-free time prediction, potentially qualifying component assemblies that would be rated marginal or unacceptable based on conservative two parameter Weibull or log-normal analysis.

Muncy, et al. [2003, 2004] conducted thermal reliability test including air-to-air thermal cycling (AATC) and liquid-to-liquid thermal shock (LLTS) on various configurations of flip-chip on board (FCOB) packages. The failure data was then analyzed using multiple linear regression and ANOVA (analysis of variance) to determine the parameters that had influence on the reliability performance of the components in accelerated life testing, the input parameters investigated included, substrate metallization, substrate mask opening area versus the UBM area of the flip chip bump, die size, perimeter or area array flip chip interconnect pattern, underfill material, location of the die on the test board, frequency of cycling, number of I/O, and percent area voiding. A model based on regression analysis was developed in order to quantify the effect of process and design decisions on the reliability of a flip chip on board assembly. ANOVA and linear regression was performed by Perkins, et al. [2004] to develop a polynomial equation between the fatigue life and the design parameters. A full factorial design of FEA simulations performed for five design parameters and fatigue life calculated from the simulations using Coffin-Manson equation was utilized for the analysis.

2.3 Failure Mechanics Based Analytical Modeling

Some researchers have used theory of mechanics to model the electronic packages in order to analyze the thermo-mechanical reliability of the packages. This approach provides a very quick and easy to use solution for the thermo-mechanical reliability problems in electronic packages. Hall [1984], used the bi-metal thermostat analysis [Timoshenko, 1925] to calculate forces, moments, displacements of a LCCCs (leadless ceramic chip carrier) soldered to PWB (printed wire boards). The physical measurements of the strains using the strain gages was also done in order to verify the calculations from the theory. Hall, proposed a formulation of an axial symmetry model and reported that the expansion mismatch between the LCCC and the PWB was absorbed mostly by the solder shear at high temperature, and mostly by "bi-metallic" bending at low temperatures. The behavior was interpreted in terms of the mechanical properties of solder.

Bi-metal thermostat theory [Timoshenko, 1925] has been extended to the trimaterial assembly [Suhir, 1986, 1990] for calculating thermally induced stresses in adhesively bonded and soldered assemblies in microelectronics. The formulation presented in form of formulas is simple, visible and easy-to-use and can be used for calculation of the magnitude and distribution of the normal stresses acting in the assembly components, without any computerization.

The diagonal lead stiffness and the compliance of the corner-most leads along with component half-diagonal dimension in the package diagonal direction [Kotlowitz, 1988] controls majority of the cyclic load transmitted to the corner-most interconnection. Kotlowitz formulated structural models for calculating the diagonal transmitted force for

SM (surface mount) leaded components, which is a key parameter for predicting long term SM solder attachment reliability [Kotlowitz and Engelmaier, 1986, Clech, et al. 1988, 1989].

Thermo-mechanical models [Vendevelde, et al. 1998] formulated for the leadless solder interconnections in flip chip assemblies can be used for evaluating the solder joint forces and stresses in both the perimeter array and area array flip chip packages. These models are based on the equilibrium of forces and moments, compatibility of displacements and compatibility of rotation conditions. High accuracy (error low than 5%) in the calculation of forces and moments was shown in the comparison of peripheral array models and FEM simulations, however the transformation of the joint loads into stresses resulted in inaccuracy (errors about 20%). Barker, et al. [2002] used the thermomechanical models formulated by Vendevelde to analyze the shear force behavior in CSP, CBGA (ceramic ball grid array), PBGA (plastic ball grid array) and connector.

Clech, et al. [1993] found that predictive tools such as the AT&T's Figure of Merit [Clech, et al. 1989] were too erroneous when applied to the various surface mount assemblies, this lead to the development of a comprehensive surface mount reliability (CSMR) model, which was based on the correlation of 28 accelerated tests in the SM reliability database and was validated by nine accelerated test datasets. The combined effect of local and global thermal mismatches is used in the energy based fatigue law for the reliability prediction. The CSMR model was further extended to another Design-for-Reliability Tool, SRS (Solder Reliability Solution) model [Clech, 1996] which was used for the reliability predictions of LCCCs as well as area array assemblies. The validation of SRS model has been done for variety of BGA, flip chip and CSP assemblies [Clech,

2000]. The SRS model has also been used for conducting parametric studies for combinations of materials, geometry and use conditions [Clech, 1997] in case of CSP and flip chip assemblies. The solder volume effects [Clech, 1998] on the reliability of flip chip and CSP assemblies has been analyzed by introducing the solder volume correction factor in the existing SRS model and the model has been validated for flip chip assemblies, micro-BGAs and CSPs with alumina interposer.

2.4 Finite Element Based Numerical Techniques

FEA (Finite Element Analysis) has been a widely used methodology for solder joint reliability [Darveaux 1996, Syed 2001, Zahn 2002, 2003] analysis and life prediction of various electronic packages. Darvaeux [2000] analyzed the effect of simulation methodology on solder joint crack growth correlation and fatigue life prediction, ANSYS 5.6 was used for the simulation and solder joint material was modeled with Anand's viscoplastic constitutive model [Anand 1985, Brown, et al. 1989], which is a standard option in ANSYS. Johnson [1999] extended Darveaux's approach and implemented it for the finite element simulation of BGA solder joint reliability, Gustafsson et al., [2000] also used finite element modeling for the life prediction of BGA packages.

Lindley, et al. [1995] and Lall, et al. [2003] conducted solder joint reliability study on BGA and CSPs for the automotive underhood application. Yeh, et al. [1996], Popelar [1998] and Lu, et al. [2000] did parametric analysis of flip chip reliability based on solder joint fatigue modeling, via computer simulation. Time independent plastic behavior [Wiese, et al. 2002] of SnPb and SnAgCu solder alloy has been modeled and it's effect

on the FEM (Finite Element Method) simulations of electronic packages. The solder joint reliability prediction of electronic packages is sensitive to the damage volume [Vendevelde, 2003] which is used for volume averaging of plastic work in the solder joint, analysis for 7x7 area array CSP mounted on FR4 board using a quarter symmetry model was done in order to optimize the damage volume. Hossain, et al. [2004] presented strain based approach using FEM, for predicting the solder joint fatigue life with and without IMC (inter-metallic compound) layer in case of a CSP, it was found that the IMC growth significantly affect the stress distribution and inelastic strain accumulation in the solder joint.

A novel hybrid approach [Towashiraporn, et al. 2003 Shen, et al. 2001, and Uegai, et al. 2002] based on damage and fracture mechanics was proposed to predict crack trajectory and fatigue life of solder joint subjected to temperature and power cycling of 144 I/O, Sn-Pb CSP and BGA packages. Warner et al. [2004] have integrated FE stress module within CFD to predict solder joint life in case of SMT resistor, using finite element (ANSYS, FLO/STRESS) and finite volume (PHYSICA) codes. Lau, et al. [2004] developed thermal fatigue life prediction equation for lead-free (Sn4.0Ag0.5Cu) bumped WLCSP (wafer level CSP) on lead-free FR-4 PCB with ENIG (electroless nickel-immersion gold). FEM simulation based solder joint fatigue life model methodology for both 63Sn37Pb and 95.5Sn4Ag0.5Cu solder alloy has been presented by [Zahn, 2002, 2003, Kim et al. 2003, Schubert et al. 2002]. The effect of underfill on solder strains and susceptibility to delamination in SBGA (Super BGA) was studied [Pyland, et al. 2002] and it was reported that underfill does not always enhance SBGA

reliability, the properties of the underfill have a significant role in the over all reliability of the SBGA packages.

Pucha, et al. [2001] and Tunga, et al. [2003, 2004] proposed a damage metric based mapping approach for developing accelerated thermal cycling guidelines for electronic packages with both lead and lead-free solder, the percentage contribution of plastic and creep deformation to total inelastic deformation in the solder joint is considered for mapping the damage accumulation in order to develop accurate ATC (accelerated thermal cycle) for a given field condition.

2.5 Constitutive Behavior of Solder Material

Since the strength of materials models and the FEA models both require input of constitutive relation parameters and the material models for the various materials within the assembly, therefore the material characterization becomes an important aspect of life prediction process. Constitutive relations are developed by fitting the stress-strain data into various material models. Darveaux, et al. [1992] presented extensive stress-strain data on 62Sn36Pb2Ag, 60Sn40Pb, 96.5Sn3.5Ag, 97Pb3Sn and 95Pb5Sn solder joints, both shear and tensile loading were employed over a wide range of temperature and strain rate. Amagai, et al. [2002] conducted material characterization tests of Sn-Pb based and Sn3.5Ag0.75Cu, Sn-Ag based lead-free solders (63Sn37Pb, 62Sn36Pb2Ag, Sn2.0Ag0.5Cu), and fitted the data to the Anand's constitutive model that unifies both rate-dependent creep and rate independent plasticity via viscoplastic flow equation and evolution equation.

Nose, et al. [2003] analyzed the effects of temperature and starin rate on the tensile strength and inelastic constitutive relationship of Sn-Pb solders, the compositions used include 5Sn95Pb, 10Sn90Pb, 40Sn60Pb, 60Sn40Pb and 63Sn37Pb. Wiese, et al. [2001] investigated and reported the constitutive behavior of two lead-free solder (Sn96.5Ag3.5, Sn95.5Ag3.8Cu0.7) and two lead containing solder alloys (Sn63Pb37, Sn59Pb40Ag1), the experiments were conducted on both bulk specimens and flip-chip joints.

Micro-structural and mechanical characterization of 95.5Sn4Ag0.5Cu solder balls by nano-indentation was carried out by Erinc, et al. [2004]. Xiao, et al. [2004] analyzed and reported the aging and creep behavior of Sn3.9Ag0.6Cu solder alloy. Pang, et al. [2004] fitted the stress strain curves for lead free (95.5Sn3.8Ag0.7Cu) solder alloy into modified Ramberg-Osgood model and compared the results with the Anand's model. Liu, et al. [2002] measured and reported the micro-scale mechanical properties of fine feature flip-chip with lead free solders. Fan, et al. [2003] conducted mechanical characterization of board level solder (63Sn37Pb, Sn3.5Ag, Sn4Ag0.5Cu) sphere attachment on Cu with ENIG surface finish substrate. Three different modeling approaches were used [Feustel, et al. 2000] for time dependent material modeling of solder in finite element analysis (ANSYS) of flip chips: viscoplasticity (Anand's model).

2.6 Solder Joint Fatigue Failure Models and Damage Relationships

The models developed from the statistical analysis don't use any failure mechanics theory and predict life, without using any fatigue or damage relationship, but

since the statistical models are based on the experimental failure data so the failure mechanics is inherently in-built in these life prediction models. In case of failure mechanics based or FEA based models the model out put is either in form of a strain or strain energy, which is subsequently used in the damage relationship in order to predict the solder joint fatigue life. Coffin-Manson type life prediction model [Coffin 1954, Manson, et al. 1964] based on the creep strain [Syed 1990, 1997], plastic strain [Engelmaier 1983, Solomon 1986] or total inelastic strain [Pang, et al. 1997] accumulated in one thermal cycle has been traditionally used by several researchers. Guven, et al. [2003] used method based on strain energy density criterion in conjunction with the three-dimensional thermo-mechanical finite element analysis for accurate prediction of crack growth in electronic packages.

Lall, et al. [2003] modified Darveaux's model for the life prediction of CSPs and PBGA, this model is energy based and the total life in this model is divided into cycles for initiation and cycles for propagation. Recently, many researchers [Dauksher 2003, Lau 2003, Syed 2004] have analyzed components with lead-free solder and developed thermal fatigue life models for lead-free solder joint reliability prediction. Syed [2004] proposed creep strain and strain energy density based thermal fatigue life prediction models for lead-free (SnAgCu) solder joints.

Shi, et al. [1999, 2000] analyzed the effect of temperature and frequency on the low cycle fatigue (LCF) life of eutectic solder alloy and proposed a temperature and frequency-dependent fatigue life prediction model using the total strain range [2000] and energy density [1999] in the frequency-modified LCF relationship. Massiot [2004] and

Lee [2000] reviewed various creep fatigue failure models in solder material and proposed their applicability for the PBGA and chip scale packages.

2.7 Objective and Scope of the Thesis

The chief motivation behind this work has been to understand and quantify the sensitivity of component reliability to various parameters such as package architecture, geometry, material properties and board attributes. In this research task, an effort has been made to develop a tool that can serve government contractors, OEMs and 3rd party contract manufacturers for doing trade-offs between geometry and material in order to make educated selection of appropriate components for specified mission requirements.

In this thesis, library of closed form models based on the theory of failure mechanics and statistical analysis of experimental test failure data has been developed and presented. Finite element analysis (FEA) for the thermo-mechanical reliability analysis of a flip-chip has also been performed. The sensitivity of the flip-chip reliability on the various design and material parameters has been analyzed through the FEA simulations and the results have been presented.

2.8 Thesis Layout

The closed form model, based on the theory of failure mechanics and material constitutive relations, developed for the BGA packages, has been presented in Chapter 3. Chapter 4 includes the library of statistics based closed form models and the regression analysis methodology used for developing the life prediction models for the BGA packages on flex substrate. The models developed in Chapter 3 and 4 have been

validated with the experimental test data and the design guidelines for the BGA packages has been included in the Chapter 5.

The statistics based and the failure mechanics based closed form models developed for the flip-chip package in the present work have been presented in the Chapter 6, which also includes a section on the validation of the models developed with the experimental test data. Chapter 7 provides the details of the FEM analysis done on a flipchip package. Finally the conclusions based on the present study and the recommended future work is presented in Chapter 8.

CHAPTER 3

FAILURE MECHANICS BASED MODELS FOR BGA PACKAGES

Failure mechanics based models have also been referred as mathematical or analytical models in several published literatures. These models are based on the strength of materials analysis for a given package configuration with known geometry and material properties.

3.1 Overview

The package life is considered to be a function of the damage due to the inelastic strain energy that solder joint interconnect accumulates while the device undergoes thermal cycling. The accumulation of the inelastic strain energy initiates a crack in the solder joint and this crack propagates with the accumulation of the inelastic strain energy as the component keeps on undergoing thermal cycling. The component finally fails when either the solder joint cracks completely or when the crack is sufficient enough to prevent the flow of required current through the solder joint interconnection. The inelastic strain energy accumulated per unit volume per cycle, also referred as inelastic strain energy density (ISED) is given by the area enclosed within the hysteresis loop of the solder joint. The inelastic strain energy density calculation for any given package depends on various factors like the geometry and architecture of the package, material

properties, assembly stiffness, local and global thermal mismatch, hysteresis loop approximation methodology, creep and other material constitutive relations

3.2 Modeling Methodology

The flowchart shown in the Figure 3.1 describes main steps involved in the formulation and application of failure mechanics based models. In the first step the maximum shear strain in the solder joint is determined which is required as a initial guesstimate for initializing the hysteresis loop iteration. The second step involves hysteresis loop determination for both local and global thermal mismatch using various material constitutive relations.

Once the hysteresis loops are determined for both the cases then in the next step inelastic strain energy is calculated from the area enclosed within the loops. Finally the sum of the inelastic strain energy density due to both local and global thermal mismatch is used in the damage relationship for calculating the characteristic life of the package.

3.2.1 Maximum Shear Strain Calculation

The maximum shear strain in the solder joint can be calculated by the simplified DNP formula, but the DNP formula is based on several assumptions due to which it gives the upper bound of the maximum shear strain value. Since maximum shear strain value is used as the primary input for initiating the hysteresis loop iteration in order to determine the hysteresis loop for both local and global mismatch so the accuracy of the hysteresis loop is significantly impacted by the initial input of the maximum shear strain value. In the case of area array package the shear forces generated due to the thermal

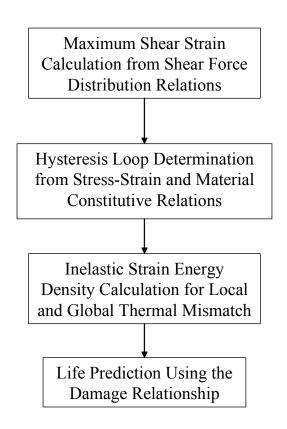


Figure 3.1 Schematic of the failure mechanics based modeling methodology

mismatch during thermal cycling of the component is shared by all the solder joints so the DNP formula which does not considers the shear force distribution among the solder joints gives a highly unrealistic value. Vandevelde, et al. [1998] proposed an analytical thermo-mechanical model to calculate thermally induced shear force in the solder balls of an area array package. In the present work, Vandevelde's [1998] approach has been used to determine γ_{max} instead of the DNP formula. Since the shear force distribution among all the solder balls for different area array configurations is taken into account in this methodology so it gives a better estimate of the γ_{max} than the DNP formula. The shear force experienced by the solder balls in an area array with 2n x 2n balls can be calculated by solving set of n linear equations from (3.1) for i = 1 to n [Vandevelde, et al. 1998]

$$(\alpha_b - \alpha_c)(\Delta T)(P)(i) = [(\phi)\sum_{k=1}^{i}\sum_{q=k}^{n}F(q)\times(P)] + F(i)\times\chi$$
 (3.1)

where

F(i) is shear force due to thermal mismatch in the ith solder joint from the center [Vandevelde, et al. 1998]

$$\varphi = \frac{\left(\frac{h_c}{2} + h_s + \frac{h_b}{2}\right)^2}{E_c I_c + E_b I_b} + \frac{1}{E_c I_c} + \frac{1}{E_b I_b}$$
(3.1.1)

$$\chi = \frac{h_c}{6 \times G_c \times P \times b_c} + \frac{h_b}{6 \times G_b \times P \times b_c} + \frac{h_s}{A_s G_s} + \frac{h_s^3}{12E_s I_s}$$
(3.1.2)

The shear strain is then calculated for the ball with maximum value of shear force F(i) using Equation (3.2) [Vandevelde, et al. 1998]

$$\gamma_{\text{max}} = \frac{2 \times (1 + v_s) \times F_{\text{max}}(i)}{E_s \times A_s}$$
(3.2)

Shear force distribution and maximum shear strain calculation procedure has been implemented in MATLABTM.

3.2.2 Hysteresis Loop Determination

The thermal cycle for hysteresis loop determination is divided into 4 sections:

- 1. Ramp up from low temperature to high temperature
- 2. Dwell at high temperature
- 3. Ramp down from high temperature to low temperature
- 4. Dwell at low temperature

The solder joint response during the temperature ramps is approximated by time independent plastic deformation relation (3.3) [Knecht and Fox, 1991].

$$\gamma_{\rm B} - \gamma_{\rm A} = \left(\frac{\tau_{\rm B}}{\tau_{\rm P}}\right)^2 \tag{3.3}$$

where

subscript A denotes the condition before ramp, B denotes condition after ramp and τ_p is plasticity parameter obtained from linear curve fitting of data in [Knecht, et al. 1991]:

$$\tau_{P}(psi) = 50588.5 - 300.23 \times T(^{\circ}C)$$
 (3.3.1)

The constitutive relation (3.4.1) given by Hall [1991] has been used for stress relaxation during the dwell period. The creep relation (3.4.2) given by Wong [1988] has been used for time and temperature dependent creep during the dwell period.

$$\gamma + \frac{\tau}{\kappa} = \gamma_{\text{max}} \tag{3.4.1}$$

$$\gamma_{\text{creep}} = A(T)\tau^{\text{m}} \tag{3.4.2}$$

where

$$\kappa = \frac{K \times h_s}{A_s} \tag{3.4.1.1}$$

K is the effective assembly stiffness calculated from the formulation given by Hall [1984] for both global and local thermal mismatch

 γ_{creep} is strain rate or the time derivative of creep strain

A(T) is temperature dependent factor derived from the data by Wong [1988] and is given by:

$$A(T) = 7.298 \times 10^{13} \frac{1}{E^{3}(T)} e^{-\frac{5412}{T(K)}}$$
(3.4.2.1)

E(T) is the temperature dependent Young's modulus of the eutectic tin-lead solder.

The first iteration is started with initial value of shear strain, $\gamma_A = \gamma_{max}/2$ and zero shear stress. The iteration is continued each time starting with the shear strain equal to the mean of residual strain, γ_F , and γ_A , of the previous iteration. The loop is stabilized and closed when the point residual strain overlaps the initial strain, which means that the value of γ_F lies in the vicinity of γ_A . The loop closure is defined by the parameter %e, given by Equation (3.5), and the loop is considered to be closed and stabilized when %e is equal to or less than 1%.

$$\%e = \frac{|\gamma_A - \gamma_F|}{\gamma_D - \gamma_A} \times 100 \tag{3.5}$$

The calculations based on the equations discussed above have been incorporated in a program in $MATLAB^{TM}$.

3.2.3 Inelastic Strain Energy Density Calculation

The hysteresis loop is determined for both the global and local thermal mismatch separately using the procedure discussed in section 3.2.2. Once the stabilized loops are determined than the area enclosed within the loops which represents the amount of inelastic strain energy density accumulated by the solder joint during one complete thermal cycle is determined using the trapezoidal rule. According to the trapezoidal rule the area under any curve given by a function f(x), as shown in the Figure 3.2, can be approximated as the summation of the 'n' trapezoids used to divide the area, [Suli, et al. 2003]

$$\int_{a}^{b} f(x)dx \approx \sum_{i=1}^{n} \frac{h}{2} (f(a+(i-1)h) + f(a+ih))$$
 (3.6)

The total inelastic strain energy per unit volume per cycle (ΔW) is given by the sum of the inelastic strain energy density per cycle due to global thermal mismatch (ΔW_G) and due to local thermal mismatch (ΔW_L) [Clech, 1996].

$$\Delta W = \Delta W_{G} + \Delta W_{L} \tag{3.7}$$

3.2.4 Life Prediction from Damage Relationship

The damage relationship relates the characteristic life of the component in terms of number of thermal cycles with the total inelastic strain energy density per cycle. This damage relationship is valid only if the failure mode of the package is solder joint

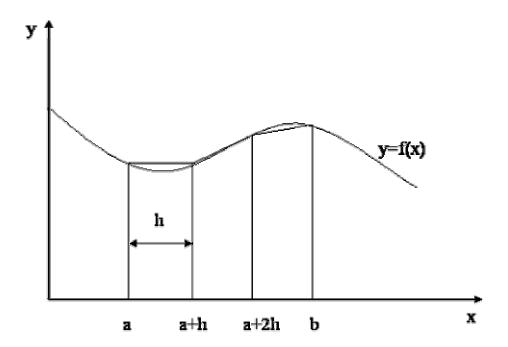


Figure 3.2 Calculation of area under the curve using trapezoidal method

cracking due to thermal cycling fatigue. The damage relationship is established from the experimental ATC failure data. This relationship depends on the solder composition and the package architecture. So, one has to be very careful while using the damage relationship while predicting failure cycles for any particular component. In the current work the damage relationships proposed by Lall, et al. [2004] and Darveaux [2000] have been used to calculate the characteristic life (α_{joint}) for life prediction of the component. The characteristic life of the component is given by Equation (3.8).

$$\alpha_{\text{joint}} = N_0 + \frac{a}{\text{da/dN}}$$
(3.8)

where

'a' is the joint diameter at the interface

$$N_0 = K_1(\Delta W)^{K_2}$$
 is the number of cycles for crack initiation

$$\frac{da}{dN} = K_3(\Delta W)^{K_4}$$
 is the crack propagation rate

The value of the constants K_1 , K_2 , K_3 and K_4 used for calculation of characteristic life cycles are given in Table 3.1.

In order to verify the model prediction one percent failure cycles predicted from the failure mechanics based closed form model for 23mm PBGA package under two different thermal cycling conditions has been plotted in Figure 3.3 against the experimental values. The two thermal cycling conditions used for the model validation are:

- 1. -50°C to 150°C with 15mins ramp and 30mins dwell
- 2. -40°C to 125°C with 15mins ramp and 30mins dwell

The model over predicts life for the -50°C to 150°C thermal cycle and under predicts for the -25°C to 125°C thermal cycle. But the trend and the 1% failure life of the package predicted by the model is consistent and lies in close proximity of the experimental values, thus validating the model predictions.

Table 3.1 Constants for the damage relationship

	K_1	K_2	K ₃	K_4
	(cycles/psi ^K ₂)		(in/cycle/psi ^K ₄)	
Lall et al. [2004]	28769	-1.53	6x10 ⁻⁷	0.7684
Darveaux [2000]	48300	-1.64	3.8x10 ⁻⁷	1.04

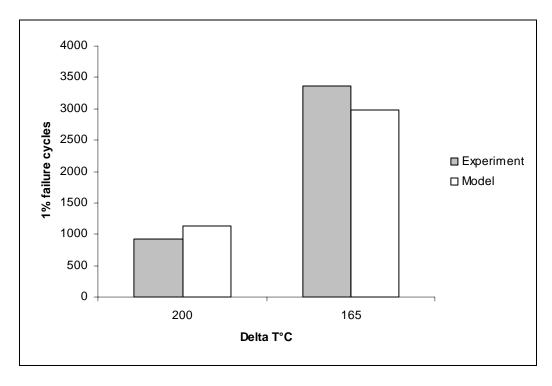


Figure 3.3 Effect of temperature condition on thermal reliability of 23mm PBGA package

CHAPTER 4

STATISTICS BASED CLOSED FORM MODELS FOR BGA PACKAGES

Multi-variable regression and analysis of variance are very powerful and useful statistical techniques for an engineer to analyze and quantify the effect of multiple independent variables on a dependent variable. This technique has been used to establish a mathematical relationship to correlate the independent variable like characteristic life or cycles to 1% failure for an electronic package with the various dependent variables which affect the life of the package. The results have been analyzed and correlated with underlying failure mechanics in order to develop meaningful closed form statistical models for application to area array package reliability. The results have been correlated with the actual experimental failure data in order to gain confidence for application of these models.

4.1 Overview

This section presents a methodology based on statistics of multi-variable regression for assessing and predicting the reliability of area array packages under harsh environments. One of the biggest advantage of this methodology is that it allows one to incorporate the effect of several non-conventional predictor or dependent variables such as board finish, pad configuration (SMD, NSMD) etc on the thermal reliability of the package..

4.2 The Perturbation Approach

A unique perturbation approach based on the statistical models developed from multivariate regression techniques has been developed and presented in the current work. The flowchart in Figure 4.1 demonstrates a broad layout of the various steps involved in the development and application of this perturbation approach.

The first step in the development of this approach has been the accumulation of the actual experimental failure database of various configurations of area array packages under accelerated thermal cycling tests. The harsh environment accelerated test database on various configurations of packages generated in-house by the researchers at the Center of Advanced Vehicle Electronics (CAVE) and the test data published by other researchers in various literatures has been accumulated. The accumulated data is then arranged in the excel spreadsheet in the form of several datasets. Number of cycles for 1% failure of the component has been used as the reliability criterion, as it is a standard thumb rule commonly followed in the automobile and aerospace industry for assessment and comparison of thermal reliability of the electronic components. Several conventional and non-conventional predictor variables which are known to have impact on the component reliability have been also included in the datasets. These parameters include Body Size, Die Size, Die to Package Ratio, Solder Ball Size (ball diameter and height), Solder Volume, Ball Pitch, Ball Count, Array Configuration (partial or full array), Underfill EMC Filler Content, Conformal Coat, Pad Size, Pad Configuration (SMD/NSMD), Solder Mask Diameter, Solder Mask Thickness, PCB Thickness, Board Finish (HASL,

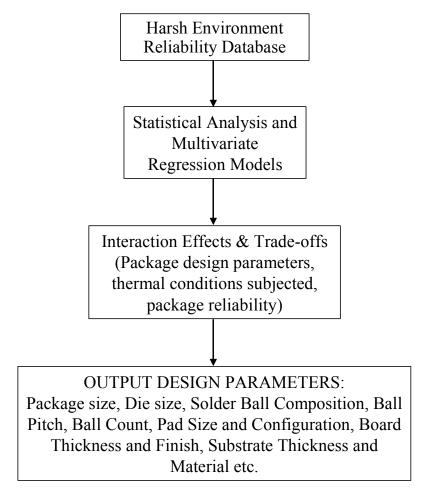


Figure 4.1 Schematic of the perturbation approach for thermal reliability assessment

OSP, Au), PCB material, Substrate material and Temperature Cycle Conditions such as ramp rate, dwell time and temperature extremities.

In the next step statistical analysis of the complete datasets has been carried out using MINITABTM (statistical analysis software). Multi-variable regression and analysis of variance techniques were employed to analyze and quantify the relative influence of the predictor variables on the thermal reliability of the package. The output of the multi-variable regression and analysis of variance is used to develop a mathematical equation which correlates the sensitivities of the predictor variables with the 1% failure cycles $(N_{1\%f})$ for a given package. The significance of the sensitivities of the predictor variables has also been analyzed in order to retain only the significant variables in the final equation. The multi-collinearity among the predictor variables in the reliability data has been analyzed using the Pearson correlation coefficient matrix of the predictor variables. The residuals have also been analyzed and verified for heteroscedasticity in the data, the residual vs fit plot has been used for the heteroscedasticity. The normal distribution of the residuals, which is one of the basic assumptions for the regression analysis, has also been ensured.

Once the mathematical equation correlating the 1% failure cycles with the various dependent parameters of the package is established and validated with the actual failure data with significant level of confidence than it can be used for perturbing a select few or all parameters against existing datasets for evaluation of various design options. This allows one to analyze the interaction effects among the various package design parameters. One can also use these models to do trade-offs with confidence within the frame of given datasets in order to achieve a specified level of thermo-mechanical

reliability for any package under a given harsh environment condition. Thus this methodology helps the user in making a final decision on the various package design parameters such as package size, die size, solder ball composition, ball pitch, ball count, pad size and configuration, board thickness and finish, substrate thickness and material etc.

4.3 Model Library

Several statistical models have been developed to predict the thermal reliability of BGAs (Flex-BGA and PBGA). The model library includes linear and non-linear models. The number of cycles to 1% failure for different configurations of area array packages has been used to predict and compare the thermo-mechanical reliability of the various configurations of the packages subjected to harsh environment conditions.

4.4 Linear Models

Multi-variable regression analysis has been done on the collected experimental failure database to generate a linear relationship between the cycles to 1% failure and the predictor variables. In this case it has been assumed that life of the package is linearly related to the various design parameters. The mathematical relation developed for linear statistical model is represented in the form of Equation (4.1)

$$N_{1\%f} = a_0 + a_1(Var1) + a_2(Var2) \dots a_n(VarN)$$
 (4.1)

where,

' $N_{1\%f}$ ' is the cycles to one percent failure or the life of any given package, also called dependent or the response variable

'Var1', 'Var2'... 'VarN' are the design parameters which influence the package life, these are also called independent or predictor variables

' a_0 ' is a constant and ' a_1 ', ' a_2 ',.... ' a_n ' are the coefficients of the design parameters and are called generalized degree of freedom in the problem definition

4.4.1 Linear Model-1

This is the basic form of a linear statistical model in which maximum number of predictor variables (parameters) had been included in the model to analyze the effect of each variable on the reliability of the package. The statistical model in form of a mathematical equation is given by Equation (4.2)

$$\begin{split} N_{1\%f} &= a_0 + a_1(\text{BodyMM}) + a_2(\text{DietoBodyRatio}) + a_3(\text{BallCount}) \\ &+ a_4(\text{BallDiaMM}) + a_5(\text{PitchMM}) + a_6(\text{PCBthkMM}) \\ &+ a_7(\text{PCBPadDiaMM}) + a_8(\text{EMCFillID}) + a_9(\text{MaskDefID}) \\ &+ a_{10}(\text{SubstrateID}) + a_{11}(\text{BoardFinishID}) + a_{12}(\Delta\Delta T) \\ &+ a_{13} \left(\frac{\partial T}{\partial t}\right) \end{split} \tag{4.2}$$

The parameters in the Equation (4.2) ending with MM indicate that the parameter has dimension of length and is measured in millimeters. The parameters ending with ID are dimensionless parameters. The various predictors used in this model were BodyMM (package body size), DietoBodyRatio (ratio of die size to body size), BallCount (number of I/Os), BallDiaMM (solder ball diameter), PitchMM (solder ball pitch), PCBthkMM (PCB thickness), PCBPadDiaMM (PCB pad diameter), EMCFillID (EMC filler content), MaskDefID (pad configuration), SubstrateID (substrate type), BoardFinishID, ΔT

(thermal cycling temperature range in °C) and $\frac{\partial T}{\partial t}$ (ramp rate in °C/min). The dimensionless variables such as EMCFillID, MaskDefID, SubstrateID and BoardFinishID were used as dummy variables and each dummy variable was assigned a numerical value.

MaskDefID toggles the mask definition between SMD and NSMD. A value of 0 corresponds to SMD and value of 1 corresponds to NSMD. EMCFillID toggles the encapsulant mold compound filler content between low and high. A value of 0 corresponds to low filler content and value of 1 corresponds to high filler content. SubstrateID toggles the substrate material between polyimide, 2 layer tape laminate and 3 layer tape laminate. A value 0 corresponds to polyimide, value of 1 corresponds to 2 layer tape and value 2 corresponds to 3 layer tape laminate. BoardFinishID toggles the board finish between Ni-Au, HASL and OSP. A value of 0 corresponds to Ni-Au, value of 1 corresponds to HASL and the value of 2 corresponds to OSP finish. The coefficient of each of the variable or the design parameter in the Equation (4.2) of this model defines the sensitivity of that parameter on the thermal reliability of the package. A negative value of the coefficient indicates a decrease in the number of cycles to 1% failure with increase in value of the variable. The numerical values of these coefficients or the generalized degrees of freedom for this model are listed in the 'Coefficient' column of the Table 4.1.

Table 4.1 Model Parameters and Analysis of Variance for Multi-variable Regression Linear Model-1

Predictor	Coefficient	SE Coeff	t-stat	p-value
Constant	3459.0	1663	2.08	0.045
BodyMM	520.2	110.2	4.72	0.000
DietoBodyRatio	-3657.1	466.9	-7.83	0.000
BallCount	-12.3	4.591	-2.69	0.011
BallDiaMM	7181.0	4853	1.48	0.148
PitchMM	-8629.0	3338	-2.59	0.014
PCBthkMM	-461.6	192.6	-2.40	0.022
PCBPadDiaMM	3086.0	4795	0.64	0.524
EMCFillID	263.9	189.5	1.39	0.173
MaskDefID	792.9	577.6	1.37	0.179
SubstrateID	14.6	116.1	0.13	0.900
BoardFinishID	-230.2	188.1	-1.22	0.230
ΔΤ	-14.3	5.049	-2.84	0.008
RampRate	-4.1	10.51	-0.39	0.700

Analysis of Variance

Source	DF	SS	MS	f	p-value
Regression	13	72832259	5602481	36.33	0.000
Residual Error	34	5243035	154207		
Total	47	78075293			

$$S = 392.7$$
 $R-Sq = 93.3\%$ $R-Sq(adj) = 90.7\%$

4.4.1.1 Model Diagnostics

The model parameters for the Linear Model-1 are listed in the Table 4.1. Analysis of the model parameters shows that the model has good R-Sq and R-Sq(adj) value which indicates that more than 90% of variation in the reliability data is explained by the regression model. High p-values of the predictor variables including, BallDiaMM = 14.8%, PCBPadDiaMM = 52.4%, EMCFillID = 17.3%, MasfDefID = 17.9%, SubstrateID = 90.0%, BoardFinishID = 23.0% and RampRate = 70.0% indicate that these variables are statistically insignificant. But from the failure mechanics theory it is known that these variables have significant effect on the package reliability. Since this statistical insignificance may be attributed to the multi-collinearity among the predictor variables in the reliability data, so the correlation coefficient matrix of the predictor variables as shown in the Table 4-2 was calculated to check the correlation coefficients for any multi-collinearity. It was found that BallDiaMM is highly correlated to PitchMM and has a correlation coefficient of 0.945 where as PCBPadDiaMM is highly correlated to PitchMM (0.78) and MaskDefID (-0.75).

Since the linear regression is based on the assumption of normal random distribution of the residuals, so it is extremely important to look at the distribution of the residuals in order to make sure that the basic assumption is not violated. It is also important to check if there is any heteroscedasticity in the data which means that the standard deviation in the distribution of the dependent variable varies with the value of the independent variable. The residual plots as shown in the Figure 4.2 are of great help in order to check whether the model complies with all these assumptions. The normal plot of the residuals shows the residuals plotted against the normal score, in case the

Table 4.2 Pearson correlation coefficient matrix for the predictor variables of the Linear Model-1

	${\tt BodyMM}$	DietoBod	BallCoun	BallDiaM	PitchMM	${\tt PCBthkMM}$	PCBPadDi	EMCFill
DietoBod	-0.352							
BallCoun	0.924	-0.229						
BallDiaM	0.568	-0.307	0.381					
PitchMM	0.708	-0.368	0.496	0.945				
PCBthkMM	0.221	-0.173	0.101	0.285	0.296			
PCBPadDi	0.580	-0.419	0.303	0.640	0.783	0.391		
EMCFill	-0.018	-0.049	-0.164	0.098	0.097	0.365	0.171	
MasfDefI	-0.342	0.333	-0.201	-0.218	-0.346	-0.280	-0.748	-0.107
Substrat	0.063	-0.001	0.233	-0.107	-0.103	0.175	-0.148	-0.184
BoardFin	-0.063	-0.058	-0.108	0.045	0.036	0.009	0.002	0.100
DeltaT	-0.518	0.441	-0.364	-0.205	-0.314	-0.179	-0.394	-0.125
RampRate	-0.199	0.227	-0.176	-0.040	-0.079	0.091	-0.006	0.017
Ma	asfDefI	Substrat	BoardFin	DeltaT				
Substrat	-0.030							
BoardFin	0.063	-0.420						
DeltaT	0.234	-0.104	0.073					
RampRate	0.109	-0.080	-0.010	0.358				

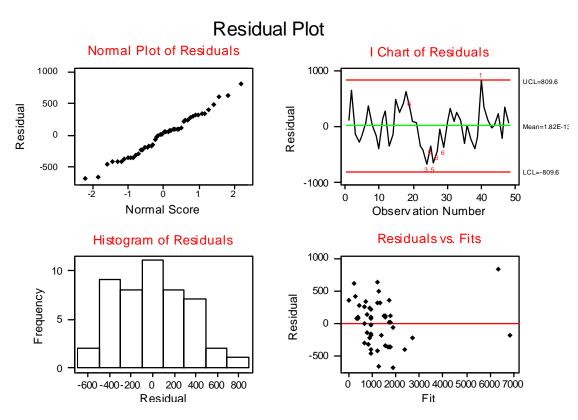


Figure 4.2 Residual plots for the Linear Model-1

residual distribution is perfectly normal than the locus of the points on the normal plot would be a straight line at an angle of 45°. The histogram of the residuals should be symmetrical bell shaped if the residual distribution is normal. The I-chart of residuals is used to verify that the residuals for all the predicted values of the model are within the control limits of 3 sigma. The residual-vs-fit plot is used to check if the failure data holds the assumption of homoscedasticity (constant variance). In case there is any heteroscedasticity than the residuals either fan out or follow some pattern as we go from the lower fits to the higher fitted values. Analyzing the residual plots of the Linear Moidel-1 it can be concluded that the distribution of the residuals is very close to normal distribution and there is no heteroscedasticity in the data, also all the residuals are within the control limits of 3 sigma (±809.6).

4.4.2 Linear Model-2

Multi-collinearity was observed in the Linear Model-1, the predictors BallDiaMM and PCBPadDiaMM were highly collinear with the predictor variable PitchMM. Linear regression was done in the Linear Model-2 using the same failure data as in the previous model but in order to remove the multi-collinearity, the variables BallDiaMM and PCBPadDiaMM were neglected from the analysis. The mathematical correlation between the number of cycles to 1% failure and the predictor variables for this model is given by Equation (4.3)

$$\begin{split} N_{1\%f} &= a_0 + a_1(BodyMM) + a_2(DietoBodyRatio) + a_3(BallCount) \\ &+ a_4(PitchMM) + a_5(PCBthkMM) + a_6(EMCFillID) \\ &+ a_7(MaskDefID) + a_8(SubstrateID) + a_9(BoardFinishID) \\ &+ a_{10}(\Delta\Delta T + a_{11} \bigg(\frac{\partial T}{\partial t} \bigg) \end{split} \tag{4.3}$$

The numerical values of the generalized degrees of freedom for this model are listed in the 'Coefficient' column of the Table 4.3.

4.4.2.1 Model Diagnostics

The model parameters for the Linear Model-2 are listed in the Table 4.3 and the residual plots are shown in Figure 4.3. In this model we notice that the R-Sq values remain almost the same so this model also explains more than 90% of the variation in the reliability data. Moreover the p-values for the constant, BallCount, PitchMM, MaskDefID, BoardFinishID and ΔT have improved significantly. But the variables SubstrateID and RampRate still remain statistically insignificant having very high p-values of 95.2% and 87.3%. Analyzing the histograms and the normal plot of the residuals for the Linear Model-2 it can be concluded that the distribution of the residuals is somewhat away from the normal distribution and the I-chart shows the residual for at least one data point to be outside the control limit of 3 sigma (±740.2). Looking at the distribution of data points in the residual-vs-fit plot it can be concluded that there is no heteroscedasticity in the data. Another linear regression after eliminating the predictors SubstrateID and RampRate was done to see the effect on the model.

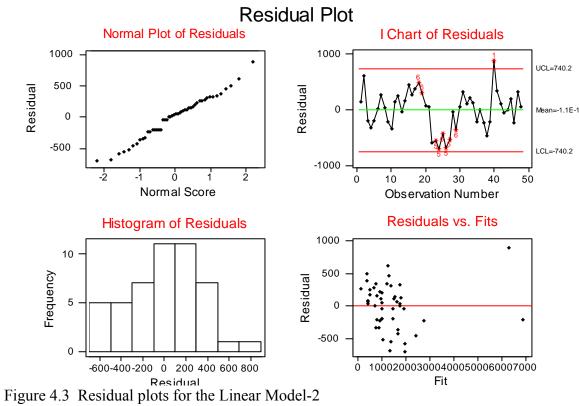
Table 4.3 Model Parameters and Analysis of Variance for Multi-variable Regression Linear Model-2

Predictor	Coefficient	SE Coeff	t-stat	p-value
Constant	4617.0	1111.0	4.16	0.000
BodyMM	506.2	94.55	5.35	0.000
DietoBodyRatio	-3674.1	468.1	-7.85	0.000
BallCount	-12.6	3.78	-3.34	0.002
PitchMM	-4149.0	1008.0	-4.12	0.000
PCBthkMM	-399.1	187.3	-2.13	0.040
EMCFillID	250.2	186.5	1.34	0.188
MaskDefID	573.8	278.4	2.06	0.047
SubstrateID	-6.9	115.5	-0.06	0.952
BoardFinishID	-256.6	187.7	-1.37	0.180
ΔΤ	-15.0	5.01	-2.99	0.005
RampRate	-1.5	9.32	-0.16	0.873

Analysis of Variance

Source	DF	SS	MS	f	p-value
Regression	11	72493777	6590343	42.51	0.000
Residual Error	36	5581517	155042		
Total	47	78075293			

S = 393.8 R-Sq = 92.9% R-Sq(adj) = 90.7%



4.4.3 Linear Model-3

Regression analysis of the Linear Model-2 indicated that the predictor variables SubstrateID and RampRate were highly statistically insignificant. Linear regression was done once again with same dataset for the formulation of Linear Model-3, but the statistically insignificant predictors were dropped out of the analysis. The mathematical correlation between the number of cycles to 1% failure and the predictor variables for this model is given by Equation (4.4)

$$N_{1\%f} = a_0 + a_1(BodyMM) + a_2(DietoBodyRatio) + a_3(BallCount) + a_4(PitchMM) + a_5(PCBthkMM) + a_6(EMCFillID) + a_7(MaskDefID) + a_8(BoardFinishID) + a_9(\Delta\Delta T)$$

$$(4.4)$$

The numerical values of the constant and other coefficients for this model are listed in the 'Coefficient' column of the Table 4.4.

4.4.3.1 Model Diagnostics

The model parameters for the Linear Model-3 are listed in the Table 4.4 and the residual plots are shown in Figure 4.4. The R-Sq and R-Sq(adj) value have increased which means that this model explains more than 91% of the variation in the data. Looking at the residual-frequency plot, it can be observed that the residuals have better normal distribution in this case as compared to the previous linear models. The I-chart shows that residual for only one data point is outside the control limit of 3 sigma (±735.6). Looking at the random distribution of data points in the residual-vs-fit plot it can be concluded that there is no heteroscedasticity in the data. Analyzing the regression

Table 4.4 Model Parameters and Analysis of Variance for Multi-variable Regression Linear Model-3

Predictor	Coefficient	SE Coeff	t-stat	p-value
Constant	4616.0	941.6	4.90	0.000
BodyMM	508.65	77.49	6.56	0.000
DietoBodyRatio	-3680.7	454.0	-8.11	0.000
BallCount	-12.7	3.0	-4.23	0.000
PitchMM	-4163.7	952.9	-4.37	0.000
PCBthkMM	-407.9	165.8	-2.46	0.019
EMCFillID	252.0	180.6	1.40	0.171
MaskDefID	573.2	267.5	2.14	0.039
BoardFinishID	-250.4	165.6	-1.51	0.139
ΔΤ	-15.1	4.42	-3.42	0.002

Analysis of Variance

Source	DF	SS	MS	f	p-value
Regression	9	72489404	8054378	54.79	0.000
Residual Error	38	5585890	146997		
Total	47	78075293			

$$S = 383.4$$
 $R-Sq = 92.8\%$ $R-Sq(adj) = 91.2\%$

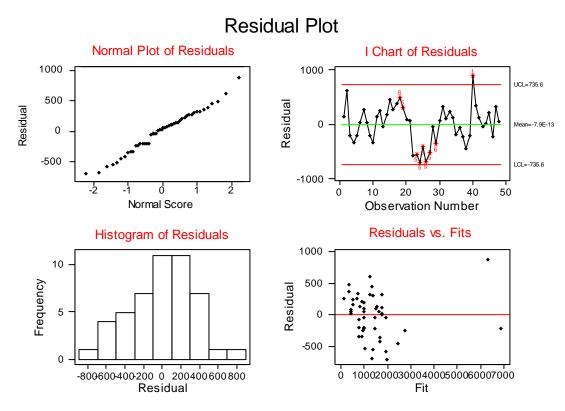


Figure 4.4 Residual plots for the Linear Model-3

results of the model and comparing with the previous model it is also observed that the R-Sq(adj) value has increased which shows that this model better explains the variation in the reliability data as compared to the previous two linear models. There is also improvement in the p-values of the predictor variables BallCount, PCBthkMM, EMCFillID, MaskDefID, BoardFinishID and ΔT as compared to the previous models. The p-values for EMCFillID(17.1%) and BoardFinishID(13.9%) are still greater than the significance level of 5%, which means they are statistically insignificant, but still these predictor variables have been retained in the model as it is known from the mechanics of failure that they have significant effect on the package reliability. Also these p-values are not too high as in case of the other variables that were dropped from the previous model.

4.5 Non-Linear Models

Multi-variable regression analysis on the collected experimental failure database was also done to generate non-linear relationship between the cycles to 1% failure and the predictor variables. In the preceding section only linear relationships were explored in order to get the best fit model. Since it is not necessary for the sensitivities of the all the dependent variables to be linearly related to the package life, so it becomes extremely important to analyze the sensitivities from the non-linear standpoint. In this case multiple variable linear regression was done using the logarithm of the dependent and independent variables that were used in the formulation of linear models, which means that the predictor variable for the non-linear models can be given by Log(Independent Variable) Thus, the final mathematical relation developed for non-linear statistical model can be represented in the form of Equation (4.5)

$$N_{1\%f} = A(Var1)^{b_1} (Var2)^{b_2} \dots (VarN)^{b_n}$$
 (4.5)

where,

' $N_{1\%f}$ ' is the cycles to one percent failure or the life of any given package, same as in case of the linear models

Var1', 'Var2'... 'VarN' are the design parameters which influence the package life, these are also called independent variables

'A' is a constant and 'b₁', 'b₂',.... 'b_n' are the indices of the design parameters

4.5.1 Non-Linear Model-1

Maximum number of predictor variables (parameters) were included in this model to analyze the effect of each variable on the reliability of the package. The statistical model in form of a mathematical equation is given by Equation (4.6)

$$N_{1\%f} = A(BodyMM)^{b_1} (DietoBodyRatio)^{b_2} (BallCount)^{b_3}$$

$$(BallDiaMM)^{b_4} (PitchMM)^{b_5} (PCBthkMM)^{b_6}$$

$$(PCBPadDiaMM)^{b_7} (EMCFillID)^{b_8} (MaskDefID)^{b_9}$$

$$(SubstrateID)^{b_{10}} (BoardFinishID)^{b_{11}} (\Delta \Delta T^{b_{12}} \left(\frac{\partial T}{\partial t}\right)^{b_{13}}$$

$$(4.6)$$

The index of each of the predictor variable or the design parameter in the Equation (4.6) of this model defines the sensitivity of that parameter on the thermal reliability of the package. A negative value of the index indicates a decrease in the number of cycles to 1% failure with increase in value of the variable. The numerical values of the generalized degrees of freedom or the indices are listed in the 'Coefficient' column of the Table 4.5.

4.5.1.1 Model Diagnostics

The model parameters for the Non-Linear Model-1 are listed in the Table 4.5. Though the model has good R-Sq and R-Sq(adj) values but several predictor variables BodyMM=30.6%, have high p-values such as BallDiaMM=38.9%, PitchMM=79.8%, PCBPadDiaMM=88.8%, EMCFillID=76.5% and RampRate=96.4%, which is beyond the acceptable limit of 5.0%. This means that all these variables are statistically insignificant, but from the failure mechanics it is well known that these variables have significant impact on the package reliability. Multi-collinearity among the predictor variables might be one of the reason for such high p-values of these variables. In order to check the collinearity among the various variables the Pearson correlation coefficient matrix was calculated as shown in the Table 4.6. Analyzing the coefficient matrix it is observed that BodyMM is highly correlated to BallCount similarly PitchMM and PCBPadDiaMM are highly correlated to BallDiaMM. The histogram and normal plot of the residuals for this model in the Figure 4.5 show that the residuals have fairly It is evident from the I-chart of the residuals that residuals normal distribution. corresponding to all the observations are within the control limit of 3 sigma (± 0.211). Since the data points in the residual-vs-fit plot are randomly scattered so there is no heteroscedasticity in the data.

Table 4.5 Model Parameters and Analysis of Variance for Multivariate Regression Non-Linear Model-1

Predictor	Coefficient	SE	t-stat	p-
LogA	4.442	1.198	3.71	0.001
LogBodyMM	-1.182	1.138	-1.04	0.306
LogDietoBodyRatio	-1.854	0.197	-9.42	0.000
LogBallCount	0.944	0.517	1.83	0.076
LogBallDiaMM	1.220	1.399	0.87	0.389
LogPitchMM	0.436	1.689	0.26	0.798
LogPCBthkMM	-0.514	0.132	-3.89	0.000
LogPCBPadDiaMM	-0.112	0.785	-0.14	0.888
LogEMCFillID	-0.009	0.030	-0.30	0.765
LogMaskDefID	0.205	0.048	4.28	0.000
LogSubstrateID	0.225	0.117	1.92	0.063
LogBoardFinishID	-0.085	0.049	-1.75	0.089
LogΔT	-1.120	0.548	-2.04	0.049
LogRampRate	-0.007	0.161	-0.05	0.964

Analysis of Variance

Source	DF	SS	MS	f	p-value
Regression	13	3.23068	0.24851	25.24	0.000
Residual Error	34	0.33478	0.00985		
Total	47	3.56545			

S = 0.09923 R-Sq = 90.6% R-Sq(adj) = 87.0%

Table 4.6 Pearson correlation coefficient matrix for the predictor variables of the Non-Linear Model-1

	${\tt LnBodyMM}$	LnDietoB	LnBallCo	LnBallDi	LnPitchM	LnPCBthk	LnPCBPad	LnSubstr
LnDietoB	-0.271							
LnBallCo	0.914	-0.025						
LnBallDi	0.649	-0.298	0.380					
LnPitchM	0.748	-0.345	0.477	0.968				
LnPCBthk	0.203	-0.196	0.082	0.259	0.267			
LnPCBPad	0.580	-0.428	0.293	0.692	0.790	0.382		
LnSubstr	0.076	0.017	0.220	-0.100	-0.097	0.188	-0.160	
LnEMCFil	-0.037	-0.066	-0.170	0.090	0.087	0.359	0.172	-0.184
LnMasfDe	-0.295	0.349	-0.165	-0.193	-0.290	-0.280	-0.683	-0.030
LnBoardF	-0.038	-0.034	-0.070	0.053	0.049	0.004	0.022	-0.420
LnDeltaT	-0.414	0.487	-0.268	-0.185	-0.269	-0.180	-0.380	-0.104
LnRampRa	-0.346	0.446	-0.240	-0.132	-0.200	-0.057	-0.226	-0.112
	LnEMCFil	LnMasfDe	LnBoardF	LnDeltaT				
LnMasfDe	-0.107							

LnMasfDe -0.107

LnBoardF 0.100 0.063

LnDeltaT -0.125 0.234 0.073

LnRampRa -0.067 0.209 0.039 0.831

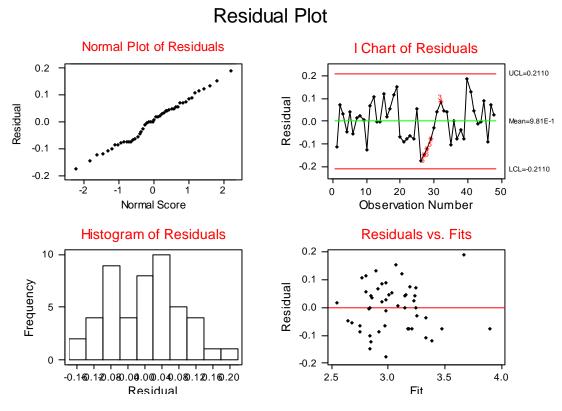


Figure 4.5 Residual plots for the Non-Linear Model-1

4.5.2 Non-Linear Model-2

It was observed that some predictor variables in the Non-Linear Model-1 were highly correlated, so regression analysis for the formulation of another non-linear model was done after dropping the variables with multicollinearity (BodyMM, PitchMM and PCBPadDiaMM) and the variables with very high p-values (SubstrateID and RampRate). The statistical model in form of a mathematical equation is given by Equation (4.7)

$$N_{1\%f} = A(DietoBodyRatio)^{b_1} (BallCount)^{b_2} (BallDiaMM)^{b_3}$$

$$(PCBthkMM)^{b_4} (EMCFillID)^{b_5} (MaskDefID)^{b_6}$$

$$(BoardFinishID)^{b_7} (\Delta \Delta T^{b_8})$$

$$(4.7)$$

The numerical values of each generalized degree of freedom or the index is listed in the 'Coefficient' column of the Table 4.7.

4.5.2.1 Model Diagnostics

The p-values for this model listed in the Table 4.7 are approximately zero for all the predictor variables, thus indicating the very high level of statistical significance of these variables. The value of R-Sq(adj) also shows improvement which means that this model fits the failure data better than the Non-Linear Model-2.

The histogram and normal plot of the residuals for this model in the Figure 4.6 show that the residuals have close to normal distribution. It is evident from the I-chart of the residuals that residuals corresponding to all the observations are within the control limit of 3 sigma (±0.2175). Since the data points in the residual-vs-fit plot are randomly scattered so the assumption of homoscedasticity (constant variance) for the regression also hold true.

Table 4.7 Model Parameters and Analysis of Variance for Multivariate Regression Non-Linear Model-2

Predictor	Coefficient	SE	t-stat	p-value
LogA	3.807	0.751	5.07	0.000
LogDietoBodyRatio	-1.739	0.153	-11.35	0.000
LogBallCount	0.416	0.083	4.99	0.000
LogBallDiaMM	0.949	0.278	3.41	0.002
LogPCBthkMM	-0.532	0.111	-4.82	0.000
LogEMCFillID	0.191	0.043	4.41	0.000
LogMaskDefID	0.258	0.063	4.10	0.000
LogBoardFinishID	-0.078	0.040	-1.93	0.061
LogΔT	-0.945	0.279	-3.39	0.002

Analysis of Variance

Source	DF	SS	MS	f	p
Regression	8	3.21641	0.40205	44.92	0.000
Residual	39	0.34904	0.00895		
Total	47	3.56545			

S = 0.0946 R-Sq = 90.20% R-Sq(adj) = 88.20%

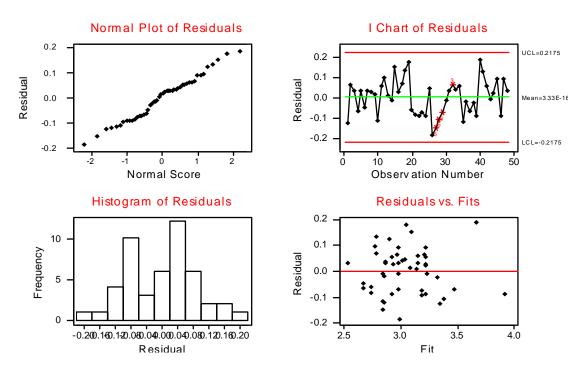


Figure 4.6 Residual plots for the Non-Linear Model-2

4.6 Model Prediction Correlation with Experimental Data

Cycles to one-percent failure values predicted by the statistical model was plotted against the actual values from the experimental database to assess the goodness of fit of the model. The best fit linear model and the non-linear model were used for the comparison of the accuracy of the prediction of these models. Figure 4.7 shows the plot for the Linear Model-3 and the Figure 4.8 shows the plot for the Non-Linear Model-2.

The straight line at 45° in these figures represents the locus of the points for which the predicted values match exactly to the experimental values. So the closer the data points are scattered to this line the better are the model predictions. On comparing both the plots it can be seen that the non-linear model gives closer and better predictions. Thus the Non-Linear Model-2 is more accurate, so this model has been selected for further validation and analyzing the sensitivity of the various design parameters on the BGA packages.

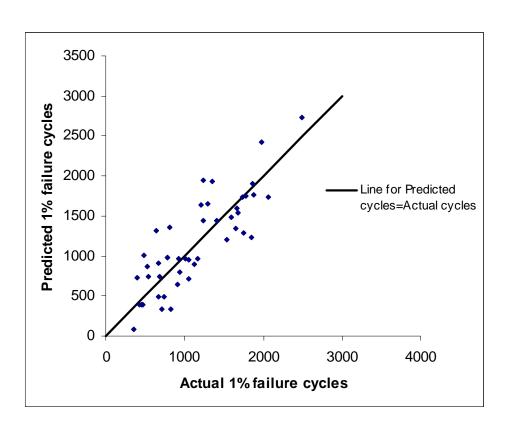


Figure 4.7 Plot of experimental vs predicted 1% cycles to failure for the Linear Model-3

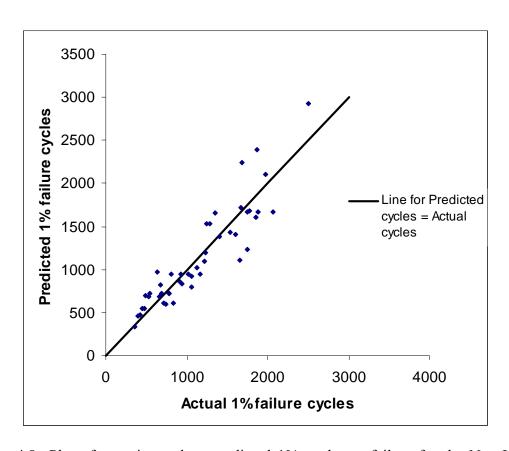


Figure 4.8 Plot of experimental vs predicted 1% cycles to failure for the Non-Linear Model-2

CHAPTER 5

MODEL VALIDATION AND DESIGN GUIDELINES FOR BGA PACKAGES

Model predictions have been correlated with the experimental data to develop confidence on the accuracy of the model. In this section the sensitivity factors developed for various design parameters from the statistics based models and the failure mechanics based closed form models have been validated against the sensitivity factors from the actual accelerated test failure data for different configurations of fine pitch ball grid array packages subjected to harsh environments. The effect of various design parameters on the reliability of the package has been analyzed and quantified, to develop guidelines for use in the designing and selection of the package architecture and board attributes for application in various harsh environments such as space application or automobile under the hood application.

5.1 Model Validation

The effect of the various design parameters on the thermal reliability of the package has been used for the model validation and for comparing the model predictions with the actual experimental failure test data. Statistics and failure mechanics based sensitivity factors quantifying the effect of design, material, architecture, and environment parameters on thermal fatigue reliability, have been used to compute life. Convergence between statistical model sensitivities and failure mechanics based

sensitivities has been demonstrated. Predictions of sensitivities have been validated against experimental test data. Non-Linear Model-2 presented in Chapter-4 (Section 4.5.2) has been used for perturbation of the failure data for validation of the predicted values.

5.1.1 Packaging Density

Packaging density of an electronic package is defined as the ratio of the die size to the package body size. It is also called die to body ratio. The reliability of a ball-grid array package generally decreases with the increase in the die-to-package ratio. This effect has been demonstrated in both rigid-substrate and flex-substrate packages. The hybrid model has been used to evaluate sensitivity to die-to-body. Packages with compliant elastomeric substrates (e.g. µBGA) may not exhibit this effect. Experimental data on thermal-fatigue reliability effect of die/body ratio on the solder joint thermal fatigue life of different sizes of BGA packages in thermal cycle of -40°C to 125°C with 15mins ramps and 15mins dwells has been correlated with the model predictions for 8 mm, 12 mm, 15 mm, 16 mm, 17 mm and 27 mm BGA packages with different die sizes. The cycles for 1% failure from the experimental data and the statistical model has been plotted against the die to body ratio of the various packages. Four layer FR-4 test boards of 0.85 mm and 1.6 mm thickness with OSP finish and SMD pads were used for the air to air thermal cycling test. The experimental data has been plotted along with the predicted values from the statistical model. The predicted values from the hybrid model follow the experimental values quite accurately and show the same trend as seen in the Figure 5.1. The sensitivity of the package reliability to the packaging ratio has been given in the

Table 5.1. The number of cycles to 1% failure for the different packages predicted by the model has also been listed along with the actual failure data.

5.1.2 Ball Count

The effect of ball count, also referred to as number of I/Os in published literature has been investigated. Experimental data indicates that thermal reliability of the BGAs increases with the increase in the ball count of the package. The experimental data used for the correlation includes 7.5 mm, 8 mm, 12 mm, 15 mm and 16 mm BGA packages. Figure 5.2 indicates a close agreement between the experimental data and the statistical model predictions. The general trend of increase in thermal reliability with the increase in the ball count can be seen from the plot, which is in agreement with the failure mechanics theory. Increase in the number of solder balls distributes stresses developed due to the thermal deformation over a larger number of solder joints reducing the stress level in the individual ball. The sensitivity of the package reliability to the ball count has been given in the Table 5.2. The number of cycles to 1% failure for the different packages predicted by the model has also been listed along with the actual failure data.

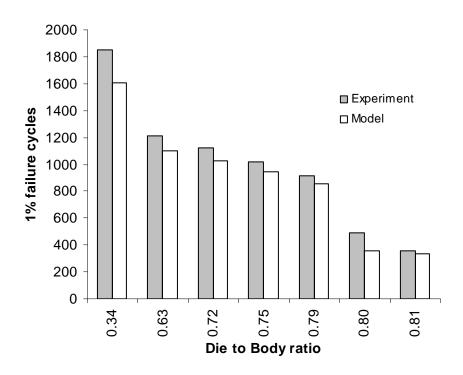


Figure 5.1 Effect of die-to-package ratio on thermal fatigue reliability of BGA subjected to -40 to 125 °C Thermal Cycle

Table 5.1 Sensitivity of the package reliability to packaging ratio and comparison of predictions from non-linear model-2 with actual failure data.

Die-to-	Ball	Ball Dia	Experiment	Model	Sensitivity Factor
Body	Count	(mm)	_		for Die-to-Body
Ratio					Ratio
0.34	40	0.45	1855	1607	
0.63	208	0.45	1215	1101	
0.72	280	0.45	1124	1027	
0.75	132	0.45	1016	946	-1.74
0.79	144	0.45	911	855	
0.80	208	0.45	491	360	
0.81	96	0.30	360	337	

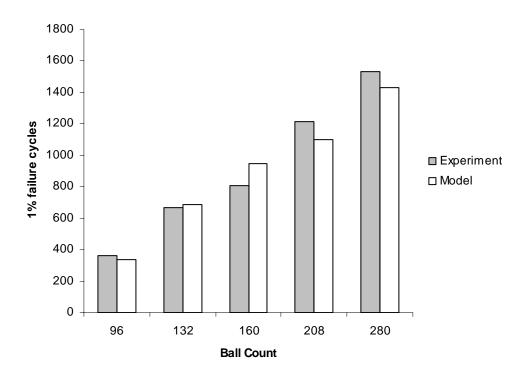


Figure 5.2 Effect of ball count on thermal fatigue reliability of BGA subjected to -40 to 125 °C Thermal Cycle

Table 5.2 Sensitivity of the package reliability to the ball count and comparison of predictions from non-linear model-2 with actual failure data.

Ball	Die-to-Body	Experiment	Model	Sensitivity Factor
Count	Ratio			for Ball Count
96	0.81	360	337	
132	0.79	667	687	
160	0.49	805	947	0.416
208	0.63	1215	1101	
280	0.72	1534	1433	

5.1.3 Ball Diameter

The solder joint ball diameter has a pronounced effect on the thermal reliability of the BGA packages. Experimental thermal reliability data has been compared with the statistical model predictions. BGA packages evaluated include solder ball diameter of 0.30 mm, 0.45 mm and 0.50 mm. The plot in the Figure 5.3 shows correlation of 1% failure cycles for BGA with variable ball diameter. Experimental data indicates that the increase in the ball diameter leads to overall better thermal reliability of the package. This trend is in compliance with the theory of failure mechanics as the increase in the solder ball diameter increases the crack area resulting in higher thermal fatigue life. The sensitivity of the package reliability to the ball diameter has been given in the Table 5.3. The number of cycles to 1% failure for the different packages predicted by the model has also been listed along with the actual failure data.

5.1.4 Board Thickness

The printed circuit board thickness also affects the thermo-mechanical reliability of the package. The decrease in reliability of a ball-grid array package with the increase in the PCB thickness is evident from the plots in Figure 5.4 and Figure 5.5. This effect is consistent from failure mechanics point of view as the increased PCB thickness leads to higher assembly stiffness, which results in higher stresses in the interconnect. This effect has been demonstrated in both rigid-substrate and flex-substrate packages. Packages with compliant elastomeric substrates (e.g. µBGA) do not exhibit this effect. Sensitivity factor has been computed from the multivariate regression model for PCB thickness in the

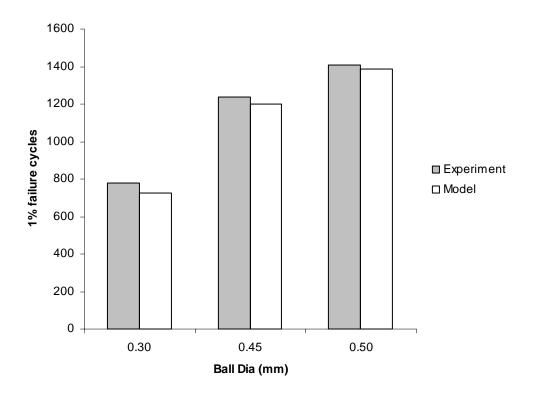


Figure 5.3 Effect of ball diameter on thermal fatigue reliability of BGA subjected to -40 to $125\ ^{\circ}\text{C}$ Thermal Cycle

Table 5.3 Sensitivity of the package reliability to the ball diameter and comparison of predictions from non-linear model-2 with actual failure data.

Ball Diameter (mm)	Experiment	Model	Sensitivity Factor for Ball Diameter
0.30	778	723	
0.45	1238	1201	0.9485
0.50	1408	1386	

range of 0.85 mm to 1.6 mm for BGA packages including 8 mm, 12 mm, 15 mm and 16 mm BGAs.

The sensitivity of the package reliability to the PCB thickness has been given in the Table 5.4. The table also shows the X-factor which is the ratio of the 1% failure cycles of a component on 1.6 mm thick PCB to that on 0.85 mm thick PCB. This basically means that it is a factor by which the life of component reduces when it is mounted on 1.60 mm thick board instead of 0.85 mm thick board.

5.1.5 Encapsulant Mold Compound Filler Content

In case of PBGAs and some other packages, to protect the silicon die from the external environment it is encapsulated in a mold compound which is usually epoxy based material. The CTE of the epoxy is much higher than the silicon, which causes very high thermal mismatch during the thermal cycling of the component. This might cause stresses to develop on the surface of the die. In order to reduce this thermal mismatch, usually a filler material with very low CTE such as silica is added to the epoxy. The thermal reliability of the BGA package decreases with the increase in the mold compound filler content. The BGA with lower amount of the mold compound filler have better thermal fatigue reliability. This trend is visible in the plots for two different 16mm BGA packages with die-to-body ratio of 0.53 in Figure 5.6 and with die-to-body ratio of 0.72 in Figure 5.7. The value of 1 indicates high filler content and the value of 10 indicates low filler content. Both the components show a decrease in the 1% failure cycles and the model predictions are in close vicinity of the experimental values which implies the correct prediction of the sensitivity of the component's thermal reliability to

EXPERIMENT 2000 1800 1600 1400 1% failure cycles 1200 D 1000 800 600 400 200 0 0.4 8.0 1.2 1.6 2 PCB thickness (mm)

Figure 5.4 Experimental data plot for BGAs (A to H) with die-to-package ratios between 0.53 and 0.81, subjected to -40 to 125 °C Thermal Cycle and PCB thickness 0.85 and 1.60mm

1800 1600 1400 1% failure cycles 1200 С D 1000 – E 800 600 _ G _ H 400 200 0 0.4 8.0 1.2 1.6 2 PCB thickness (mm)

MODEL

Figure 5.5 Model prediction plot for BGAs (A to H) with die-to-package ratios between 0.53 and 0.81, subjected to -40 to 125 °C Thermal Cycle and PCB thickness 0.85 and 1.60mm

Table 5.4 Sensitivity of the package reliability to the PCB thickness and comparison of X-factor based on predictions from non-linear model-2 and actual failure data.

S.No.	Die-to-Body	Experiment	Model	Sensitivity Factor
	Ratio	X-Factor	X-Factor	for Board Thickness
A.	0.53	0.70	0.72	
C.	0.54	0.39	0.50	
D.	0.72	0.73	0.72	
E.	0.79	0.79	0.72	-0.5322
F.	0.79	0.79	0.72	
G.	0.80	0.77	0.72	
H.	0.81	0.86	0.72	

the mold compound filler content. This trend is consistent from the failure mechanics point of view as the higher filler content mold compound will have higher elastic modulus and a lower CTE. Higher modulus of elasticity makes the package stiffer, therefore higher stresses are transmitted to the solder joints and lower CTE will increase the global thermal mismatch. Both the factors contribute to the poor solder joint thermomechanical reliability of the package.

The sensitivity of the package reliability to the EMC filler content has been given in the Table 5.5. The table also shows the X-factor values from model predictions and the experimental data. The X-factor is a factor by which the life of component reduces when the filler content in the encapsulant is increased from low to high. The X-factors from the model predictions are quite close to that calculated from the experimental data, thus validating the model sensitivity.

5.1.6 Pad Configuration

Two different solder pad configurations usually used in the electronic packages are solder mask defined (SMD) and non-solder mask defined (NSMD). Solder joint reliability in thermal fatigue increases with change in pad configuration from SMD to NSMD. This trend is visible from the 1% failure plot for 15mm, 160 I/O BGA as shown in Figure 5.8. The value of 1 indicates SMD pad configuration and the value 10 indicates NSMD pad configuration in the plot. This effect is true for both rigid-substrate and flex-substrate ball grid array packages. Packages with compliant elastomeric substrates (e.g. μ BGA) do not exhibit this effect. This trend may vary depending on the mode of failure. The package may show opposite trend in case the failure is due to the tearing out of the

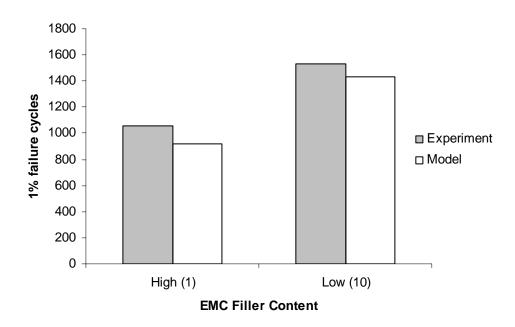


Figure 5.6 Effect of mold compound filler content on thermal fatigue reliability of 16mm BGA with die-to-body ratio 0.53, subjected to –40 to 125 °C Thermal Cycle

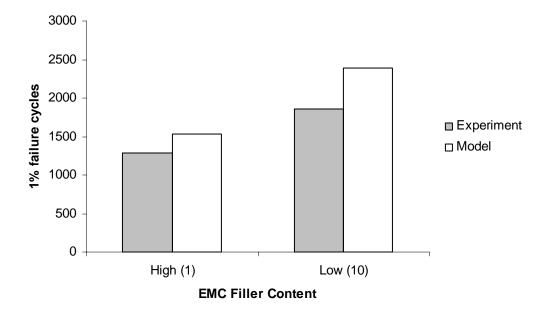


Figure 5.7 Effect of mold compound filler content on thermal fatigue reliability of 16mm BGA with die-to-body ratio 0.72, subjected to –40 to 125 °C Thermal Cycle

Table 5.5 Sensitivity of the package reliability to the EMC filler content and comparison of X-factor based on predictions from non-linear model-2 and actual failure data.

Die-to-Body Ratio	Experiment X-Factor	Model	Sensitivity Factor for EMC Fill
0.72	0.69	0.64	0.191
0.53	0.69	0.64	0.191

laminate under bending as shown by Mawer et. al.[1996]. In that case the solder mask on top of the SMD pad helps to anchor the pad to the laminate core which leads to better thermal fatigue reliability.

The sensitivity of the package reliability to the pad configuration has been given in the Table 5-6. The table also shows the X-factor values from model predictions and the experimental data for 15 mm FlexBGA package with 160 I/Os. The X-factor is a factor by which the life of component reduces when the pad configuration is changed from NSMD to SMD. The X-factors from the model predictions are quite close to that calculated from the experimental data, which validates the model sensitivity.

5.1.7 Board Finish

The most commonly used board finishes for PCBs are hot air solder level (HASL), organic surface protection (OSP) and electroless immersion gold (ENIG or Ni/Au). Experimental data from previous studies indicates that HASL and OSP are significantly more reliable than ENIG for ball grid array packages. This effect has been demonstrated in both rigid-substrate and flex-substrate packages. Packages with compliant elastomeric substrates (e.g. μBGA) may also exhibit this effect. Hung, et. al. [2000] investigated the effect of surface finish on the solder joint reliability of 12mm BGA with polyimide substrate, die-up, wire bonded and over-molded configuration. Thermal cycle of –40°C to 125°C with 15mins ramps and 15mins dwells was used for the test. FR-4 test boards of thickness 0.8mm were used in the test. As seen in Figure 5.9, out of the three surface finishes, the OSP finish boards exhibit maximum thermal

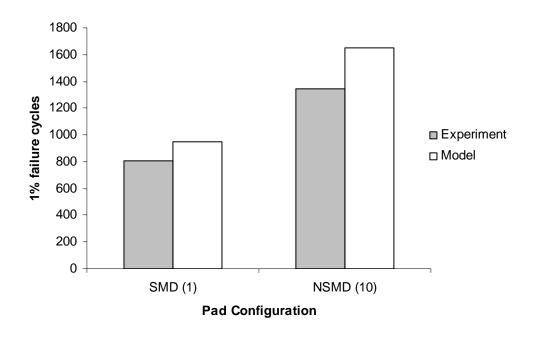


Figure 5.8 Effect of the change in mask definition from SMD to NSMD on 15mm, 160 I/O BGA thermal reliability.

Table 5.6 Sensitivity of the package reliability to the pad configuration and comparison of X-factor based on predictions from non-linear model-2 and actual failure data.

Device	Experiment X-Factor	Model X-Factor	Sensitivity Factor for Mask Definition
15mm, 160 I/O FlexBGA	0.59x	0.57x	0.2576

reliability. In the plot the value 1 for the board finish corresponds to OSP finish, 10 corresponds to HASL and 100 corresponds to Ni-Au finish. This effect of board finish on the thermal fatigue reliability is attributed to the different inter-metallic system formation for different board finishes. The different inter-metallic systems induce different failure modes thus having impact on the thermal fatigue reliability of the component. Figure 5.9 demonstrates a close agreement between the experiment and the predicted values from the statistical model.

The sensitivity of the package reliability to the board finish type has been given in the Table 5.7. The number of cycles to 1% failure for the 12 mm BGA with 132 I/Os predicted by the model for all the three board finishes has also been listed along with the actual failure data. The model predictions follow the same trend as the experimental data.

5.1.8 Temperature Cycle Condition

Temperature cycle condition affects BGA package reliability immensely. The sensitivity of the package thermal reliability to the thermal cycling temperature range has been quantified using the multivariate regression analysis in the statistical model. ΔT is the thermal cycling temperature magnitude. The cycles for 1% failure for 12mm, 132 I/O BGA with Die/Body ratio of 0.54 predicted by the statistical model has been plotted with the experimental data in the Figure 5.10. Two different temperature cycle conditions used for the comparison are:

- 1. 40°C to 125°C with 15mins of dwell, 15mins ramp
- 2. 0°C to 100°C with 30mins of dwell, 30mins of ramp.

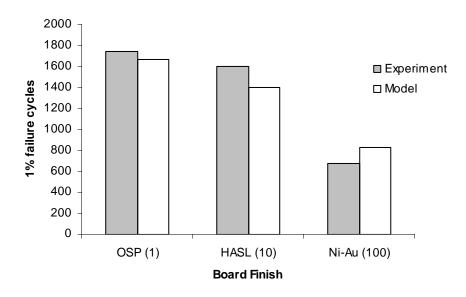


Figure 5.9 Effect of PCB pad finish on 12mm, 132 I/O BGA thermal reliability subjected to –40 to 125 °C Thermal Cycle

Table 5.7 Sensitivity of the package reliability to the board finish type and comparison of predictions from non-linear model-2 with actual failure data.

Board Finish	Experiment	Model	Sensitivity Factor for Board Finish
OSP (1)	1743	1668	
HASL (10)	1597	1403	-0.07794
Ni-Au (100)	673	828	

The sensitivity of the package reliability to the thermal cycling temperature range has been given in the Table 5.8. The table also shows the X-factor values from model predictions and the experimental data for 12 mm FlexBGA package with 132 I/Os. The experimental data validates the thermal sensitivity of the package predicted by the model.

5.2 Convergence of Statistics and Failure Mechanics Models with Actual Experimental Test Data

Convergence of model predictions from statistics and failure mechanics has been investigated. Figure 5.11 shows the effect of solder ball diameter on thermal reliability of 8mm and 12mm BGA packages under thermal cycling from –40°C to 125°C with 15 mins ramp and 15 mins dwell. Comparison of experimental data with that of predicted values for 1% failure cycles from both statistics and failure mechanics model shows good agreement. All the three values for both the packages show a same trend of increased thermal reliability with the increase in the ball diameter and lie in close vicinity of each other, thus validating the model predictions. The correlation is especially important, if one considers the vastly different approaches used in arriving at predicted life. The statistics models are based on considerations of multivariate regression and analysis of variance techniques and therefore account for mechanics of stress-strain only implicitly. The failure mechanics approach are based on mechanics-of-materials, damage mechanics, material constitutive behavior and do not address the statistical significance and distribution of parameters explicitly.

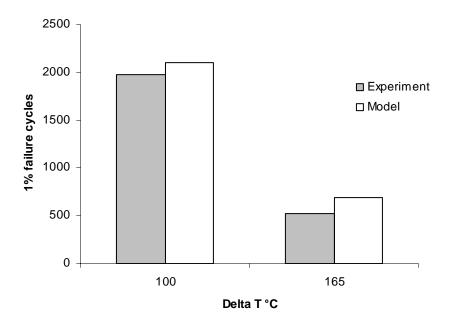


Figure 5.10 Effect of temperature cycle condition on 12mm, 132 I/O BGA thermal reliability

Table 5.8 Sensitivity of the package reliability to temperature range and comparison of X-factor based on predictions from non-linear model-2 and actual failure data.

Device	Experiment X-Factor	Model X-Factor	Sensitivity Factor for DeltaT
12mm, 132I/O FlexBGA	0.27x	0.33x	-0.9453

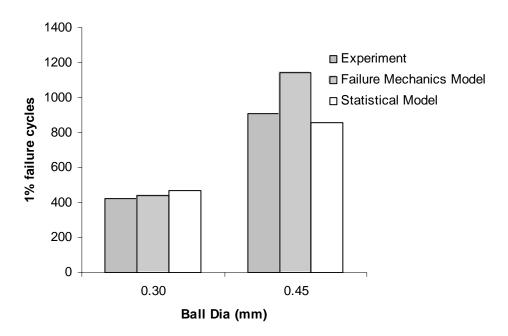


Figure 5.11 Effect of solder ball diameter on thermal reliability of 8mm and 12mm BGA packages under thermal cycle -40° C to 125° C

5.3 Design Guidelines

The sensitivities from the multi-variable regression model have been used to analyze the effect of various parameters on the solder joint reliability of the area array packages. The sensitivities derived in Chapter-4 and validated in this chapter can be used for doing the trade-offs and formulation of the design guidelines at the design and selection stage of the area array packages for various applications.

- The reliability of solder inter-connect in a ball-grid area array package generally decreases with the increase in the die-to-package ratio. This effect has been demonstrated in both rigid-substrate and flex-substrate packages.
- Solder joint thermo-mechanical reliability of the BGA packages increases with the increase in the ball count of the package.
- Increase in the ball diameter leads to overall better thermal reliability of the solder joint in the area array package.
- The solder joint thermo-mechanical reliability decreases with the increase in the PCB thickness.
- The BGA package with lower amount of mold compound filler demonstrate better solder joint thermal fatigue reliability.
- Solder joint reliability in thermal fatigue increases with change in pad configuration from SMD to NSMD.
- HASL and OSP pad finishes are significantly more reliable than ENIG for ball grid area array packages, and OSP gives better thermo-mechanical reliability than HASL.

 Thermo-mechanical reliability of the solder joint in an area array package is inversely proportional to the temperature cycle magnitude through which the package under goes thermal cycling.

CHAPTER 6

STATISTICS AND FAILURE MECHANICS BASED MODELS FOR FLIP CHIP

The term flip chip refers to the method of attachment of the silicon or the IC, in which the chip is attached upside-down and attached directly to printed circuit board or carrier substrate, typically using conductive solder bumps. Due to the large difference in the CTE of the silicon and the interposer, solder joints experience fatigue damage during the thermal or power cycling. This chapter presents the statistics based and failure mechanics based models developed in the current research for the prediction of cycles to failure. A perturbation approach to prediction of reliability of flip-chip devices in harsh environments has been investigated. The proposed approach has been shown to achieve a much higher accuracy compared to traditional first-order models by perturbing known accelerated-test data-sets using models, using factors which quantify the sensitivity of reliability to various design, material, architecture and environmental parameters. The models are based on a combination of statistical analysis and failure mechanics. The proposed approach has the potential of predicting both single and coupled factor effects on reliability, which are often ignored in closed form models. Several solder joint configurations and flip-chip architectures have been analyzed with statistical models and failure mechanics models. The results have been compared with accelerated test data.

6.1 Overview

The proposed methodology presents a turn-key solution for product managers, who are often faced with the problem of evaluating reliability trade-offs due to changes in packaging format for existing designs because of component obsolescence, die shrink, technology progression, underfills or other factors. Examples of common situations include, vendor switches the underfill on a part which has been qualified, a perimeter die is switched to an area-array die to achieve greater density, vendor thins the die from the traditional 21 mils to 10 mils to achieve higher density.

6.2 Statistics Based Modeling

In this section, statistics-based closed-form models have been developed based on multivariate regression and analysis of variance. The model parameters are based on failure mechanics of flip-chip assemblies subjected to thermo-mechanical stresses. The material properties and the geometric parameters investigated include die thickness, die size, ball count, ball pitch, bump metallurgy, underfill types (capillary-flow, reflow encapsulant), underfill glass transition temperature (Tg), solder alloy composition (SnAgCu, SnPbAg), solder joint height, bump size, and printed circuit board thickness.

An extensive flip-chip accelerated test reliability database based on the harsh environment testing conducted by the researchers at the NSF Center for Advanced Vehicle Electronics (CAVE) has been accumulated. This database has also been supplemented with the various datasets published in the literature. Range of data collected in each case is shown in Table 6.1. Each data point in the database is based on the characteristic life of a set of flip-chip devices of a given configuration tested under

Table 6.1 Scope of Accelerated Test Database.

Parameter	Data Range	
Die Size	3 mm to 12.6 mm	
Ball Count	42 to 184	
Ball Pitch	0.2 mm to 0.457 mm	
Ball Diameter	0.04 mm to 0.195 mm	
Ball Height	0.04 mm to 0.147 mm	
Solder Composition	Sn63Pb37, Sn96.5Ag3.5, Sn99.3Cu0.7, Sn95.8Ag3.5Cu0.7	
PCB Thickness	0.5 mm to 1 mm	
T _{High} in Accelerated Test	100°C, 125°C, 150°C	
T _{Low} in Accelerated Test	-55°C, -40°C, 0°C	

harsh thermal cycling or thermal shock conditions. Sensitivity of the reliability to the geometry and material parameters have been derived based on the statistical models. MinitabTM and MatlabTM have been used for the analysis. Characteristic life of the various configurations of the flip-chip packages under different accelerated testing conditions has been used as the response variable. Predictor variables include, different thermal conditions, design parameters and material attributes of the package.

The database is fairly diverse in terms of materials and geometry parameters. The flip-chip architectures contained in the database includes packages with both leaded and lead-free solder bumps. Die sizes range from 3.0mm to 12.6mm, ball counts range from 42 to 184 I/O, ball pitch ranges from 0.2 to 0.457 mm, ball diameter ranges from 0.04 to 0.195 mm, ball height ranges from 0.04 to 0.147 mm. The various solder compositions included in the database consist of Sn63Pb37, Sn96.5Ag3.5, Sn99.3Cu0.7, and Sn95.8Ag3.5Cu0.7. Accelerated test high temperatures include 100°C, 125°C, and 150°C. The low temperatures in the accelerated test include -55°C, -40°C, and 0°C.

These models in their present form can be used for reliability comparison of the flip-chip packages with different design and material attributes when subjected to different extreme environments. The perturbation approach can be used to perturb known accelerated test data sets. This approach provides higher accuracy than any first order closed form model and also allows the user analyze the interaction effects of the various parameters on the package reliability, which are often ignored in the various first order closed form modeling methodologies and addressed only using finite element models or experimental accelerated test data. The proposed form of the mathematical model is shown in Equation (6.1).

$$N_{63.2\%} = a_1 + b_1(DieSizeMM) + b_2(BallCount) + b_3(UnderfillID)$$

$$+b_4(SolderCompID) + b_5(BallDiaMM) + b_6(PadTypeID)$$

$$+b_7(DeltaT)$$

$$(6.1)$$

The parameter N_{63.2%} on the left hand side of the equation represents the characteristic life of three-parameter Weibull distribution for the flip-chip package when subjected to accelerated thermo-mechanical stresses. The parameters on the right hand side of the equation are the predictor variables or the various parameters that influence the reliability of the package. The coefficient of each of the parameter is the indictor of the relative influence of that parameter on the characteristic life of the package. In this case, parameters b_i , for i = 1 to 7 represent the sensitivities of reliability to the respective Parameter dimensions are indicated at the end of the parameter, e.g. parameters. DieSizeMM represents the die size in mm. Qualitative parameters that significantly influence the package reliability have been used as dummy variables in order to address their affect on the package reliability. Parameters ending with the ID are dummy variables. The PadTypeID varies between 0 and 1, with value 0 corresponding to solder mask defined pad and 1 corresponding to non-solder mask defined pad. A 0 value for underfillID represents non-underfill, while value of 1 corresponds to an underfilled flipchip device. The SolderCompID takes on 4 values 0, 1, 2, 3 corresponding to the four alloys in the database including, Sn63Pb37, Sn95.8Ag3.5Cu0.7, Sn96.5Ag3.5, and Sn99.3Cu0.7. The value of constant and coefficients in the model (Eq. 6.1) formulated from the statistical analysis of the failure data are listed in the Table 6.2.

6.2.1 Model Diagnostics

The p-value of a parameter in, Table 6.2, indicates the statistical significance of that parameter and the parameter with p-value less than 0.05 is considered to be statistically significant and it should have significant effect on the reliability of the package, with confidence level of more than 95.0%. All the predictor variables except the SolderCompID are statistically significant with p-values in the neighborhood of 0. SolderCompID has p-value of 0.062 which indicates 93.8% confidence level which is little less than the 95.0% confidence level but it has still been included in the model as we know from failure mechanics that the solder composition has significant effect on the thermo-mechanical reliability of the flip-chip packages. A negative value of the index indicates a decrease in cycles-to-1% failure with increase in value of the variable. The model has an R² of 99.4% indicating that a large part of the variation in the data has been explained by the model. A high f-value in Table 6.3 indicates statistical significance of difference between groups.

Normality of the distribution of residuals has been verified. Residual plots of the statistical model are shown in Figure 6.1. If we plot the residuals against the normal score of the residuals then a perfectly normal distribution is represented by a straight line at 45° on the normal plot of the residuals. The normal plot of residuals for this model indicates a fairly normal distribution of the residuals as it is quite close to a straight line at 45° (Figure 6.1). The histogram plot of residual vs frequency exhibits a nearly symmetrical bell-shape pattern, which is consistent with a sample from a normal distribution. The chart of individual observations reveals that the residuals for all the observations are within the three sigma limits of (-406.9 and 406.9) which implies that all

the data points in the analysis are fitted within the control limits of 3 sigma. We can see fairly random distribution of the residuals in the residual vs fits plot, which demonstrates the linear relationship between the predictors and the response variable in the model. If the relationship is not linear than the residuals follow some curved pattern distribution. The plot also holds the assumption of homoskedasticity (constant variance) in the data as the residuals do not fan out or show any pattern as we go from the lower fits to the higher fitted values.

Characteristic Life (63.2% failure of population) values predicted by the statistical model have been plotted against the actual values from the experimental database to assess the goodness of fit of the model. The straight line at 45° in Figure 6.2 represents the perfect fit of the predicted values. After comparing the various statistical models for the fit of the predicted values with that of actual 1% failure cycles values form the experimental data, the model with the best fit has been finally selected. The plot in the Figure 6.2 for the model show's that the predicted values are consistent with the experimental values within close tolerance.

Table 6.2 Multi Variable Regression (MVR) Model of Flip Chip

Predictor	Coeff	SE Coeff	t	P-Value
Constant	11374	1526	7.45	0
DieSizeMM	-456.18	62.32	-7.32	0
BallCount	21.994	4.413	4.98	0.001
BallDiaMM	19873	6553	3.03	0.016
PadTypeID	1781.2	261.5	6.81	0
DeltaT	-72.546	6.838	-10.61	0
PitchMM	11860	2884	4.11	0.003
BallHeightMM	-16102	4624	-3.48	0.008
SolderCompID	124.17	57.38	2.16	0.062
S		R-Sq		R-Sq(adj)
213.5		99.40%		98.80%

Table 6.3 Analysis of Variance for Data-Set.

Analysis of Variance							
Source	SS	MS	f	P			
Regression	59005565	7375696	161.84	0			
Residual Error	364599	45575					
Total	59370164						

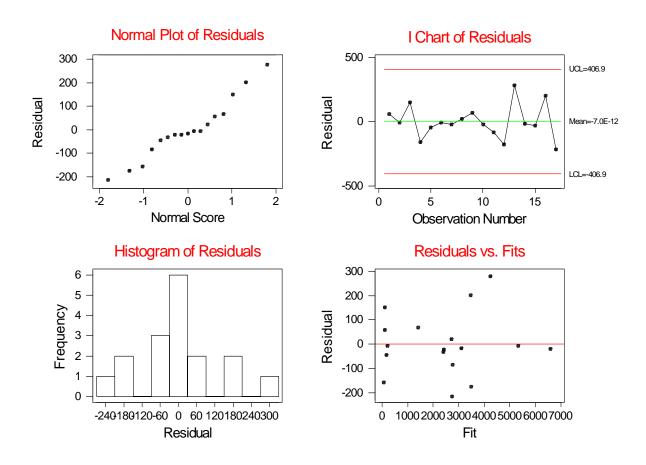


Figure 6.1 Residual plots for the diagnostics of the statistical model

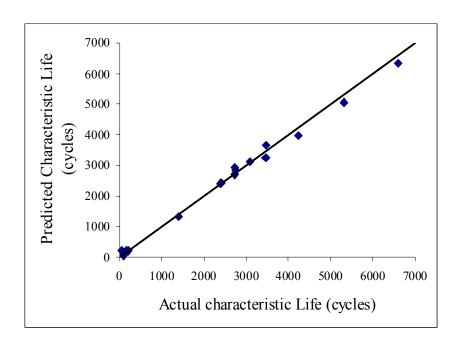


Figure 6.2 Actual vs predicted characteristic life

6.3 Failure Mechanics Based Modeling

The formulation and application of the failure mechanics based modeling methodology in the current work is based on a combination of Timoshenko beam theory [1925], and its application to tri-material assemblies [Suhir 1986, 1991], calculation of time-independent plastic deformation [Knecht 1991], calculation of stress relaxation [Wong 1991], hysteresis loop calculation [Clech 1996], life prediction [Darveaux 1992, 1995, 2000; Lall 2004]. In the first step the maximum shear strain developed in the solder joint during thermal cycling is determined which is the required input for the hysteresis loop determination. The second step involves hysteresis loop determination using the various material constitutive relations for both local and global thermal mismatch separately. Once the hysteresis loops have been determined, the total inelastic strain energy density is determined which is given by the sum of the area enclosed within the hysteresis loops for local and global thermal mismatch. Finally the characteristic life for the package is calculated from the damage relationships.

6.3.1 Shear Stresses and Strains

Previous researchers have computed the maximum shear strain in the solder joint during thermal cycling using the DNP (distance to neutral point) formula approximation, but due to the assumptions on which the DNP formula is based, it gives the exaggerated values of the maximum shear strain that are normally much higher than the actual values. The simplified form of the DNP formula usually given by Equation (2) assumes that the solder joint withstands the complete thermal expansion differential between the package

and the PCB in form of a shear strain given by γ_{max} . Bending of the package and the PCB is also completely ignored in the DNP formula [Clech, 1996],

$$\gamma_{\text{max}} = \frac{L_{\text{D}}}{h_{\text{s}}} \cdot \Delta \alpha \cdot \Delta T \tag{2}$$

Shear stresses and strain computation is based on the Timoshenko Beam theory for Bi-material assemblies [Timoshenko, 1925] and its application to flip-chip assemblies [Suhir 1986, 1990]. In order to facilitate the load distribution of the thermal mismatch, an assembly of width equal to the flip-chip pitch has been analyzed. The x-displacements at the bottom of the flip-chip and top of the substrate are respectively given by, [Suhir, 1986]

$$u_{1}(x) = \alpha_{1} \Delta t x - \lambda_{1} \int_{0}^{x} F_{1}(\xi) d\xi + \kappa_{1} \tau_{1}(x) + \frac{h_{1}}{2} \int_{0}^{x} \frac{d\xi}{\rho(\xi)}$$
(3)

$$u_{2}(x) = \alpha_{2} \Delta t x + \lambda_{2} \int_{0}^{x} F_{2}(\xi) d\xi - \kappa_{2} \tau_{2}(x) - \frac{h_{2}}{2} \int_{0}^{x} \frac{d\xi}{\rho(\xi)}$$
(4)

where, λ_i is the axial compliance for the i^{th} component, for i=1,2,3 corresponding to the flip-chip, underfill and the printed circuit board. E_i and v_i are the elastic modulus and poisson's ratio, h_i is the layer thickness and F_i is the force in the i^{th} component, [Suhir, 1986]

$$\lambda_{i} = \frac{1 - v^2}{E_{i}} h_{i} \tag{5}$$

The interfacial compliance, κ_i of the i^{th} component is given by, [Suhir, 1986]

$$\kappa_{i} = \frac{h_{i}}{3G_{i}} \tag{6}$$

and G_i is the shear modulus of the i^{th} component, ρ is the radius of curvature, $\tau_i(x)$ is the shear stress in the i^{th} interface. The relationship between forces and radius of curvature is calculated using the equilibrium equations for the underfill, the shear stresses can be represented by, [Suhir, 1986]

$$\tau(x) = \frac{\Delta \alpha \Delta t}{\sqrt{\lambda \kappa}} \frac{\sinh kx}{\cosh kl}$$
 (7)

where
$$\kappa = \kappa_1 + 2\kappa_2 + \kappa_3$$
, and $k = \sqrt{\frac{\lambda}{\kappa}}$

6.3.2 Hysteresis Loop Computation

In the current approach the reliability or the life of a package is considered to be a function of the damage due to the plastic work that the solder joint interconnect accumulates while the device undergoes thermal cycling. The accumulation of the plastic work initiates a crack in the solder joint and this crack propagates as the component keeps on undergoing thermal cycling. The component finally fails when either the solder joint cracks completely or when the crack is sufficient enough to prevent the flow of required current through the solder joint interconnection. Failure criterion for any component during the accelerated thermal cycling tests has been defined in several different ways by different researchers in the published literature. A 100% increase in the electrical resistance of the component has been commonly used as the failure criterion. The plastic work accumulated per unit volume per cycle which is also referred as inelastic strain energy density, is given by the area enclosed within the hysteresis loop of the solder joint undergoing the thermal cycling.

Loop iteration is done using the methodology by Clech [1996] until the loop converges. The thermal cycle is divided into 4 sections: (1) Ramp-up (2) Dwell at high temperature (3) Ramp-down (4) Dwell at low temperature. The solder joint response during the temperature ramps is approximated by time independent plastic deformation [Knecht and Fox,1991],

$$\gamma_{\rm B} - \gamma_{\rm A} = \left(\frac{\tau_{\rm B}}{\tau_{\rm P}}\right)^2 \tag{8}$$

where, subscript A denotes the condition before ramp, B denotes condition after ramp and τ_P is plasticity parameter obtained from linear curve fitting of data in Knecht [1991]:

$$\tau_{P}(Mpa) = 348.79 - 2.07 \times T(^{\circ}C)$$
 (9)

The constitutive relations given by Hall [1984] and Wong [1991] have been used for stress relaxation and the time dependent creep during the dwell period,

$$\gamma + \frac{\tau}{\kappa} = \gamma_{\text{max}} \tag{10}$$

$${\stackrel{\circ}{\gamma}}_{creep} = A(T)\tau^3 \tag{11}$$

where, γ_{creep} is strain rate or the time derivative of creep strain, A(T) is temperature dependent factor derived from the data by Wong [1991], and $\kappa = \frac{K \times h_s}{A_s}$ where K is effective assembly stiffness derived from the formulation given by Hall [1984] for the LCCCs

6.3.3 Life Prediction from Damage Relationship

The damage relationship relates the characteristic life of the component in terms of number of thermal cycles with the total inelastic strain energy density per cycle. This damage relationship is valid only if the failure mode of the package is solder joint cracking due to thermal cycling fatigue. The damage relationship is established from the experimental ATC failure data. This relationship depends on the solder composition. So, one has to be very careful while using the damage relationship while predicting failure cycles for any particular component. In the current work the damage relationships proposed by Lall [2004] and Darveaux [1992, 2000] have been used to calculate the characteristic life (t_{63.2%,joint}) for life prediction of the component. The characteristic life of the component has been calculated using the damage relationship given by Equation (12).

$$t_{63.2\%, joint} = N_0 + \frac{a}{da/dN}$$
 (12)

$$N_0 = K_1(\Delta W)^{K_2} \tag{13}$$

$$\frac{\mathrm{da}}{\mathrm{dN}} = \mathrm{K}_3 (\Delta \mathrm{W})^{\mathrm{K}_4} \tag{14}$$

Where, 'a' is the joint diameter at the interface, N_0 is the number of cycles for crack initiation and da/dN is the crack propagation rate. The value of the constants K_1 , K_2 , K_3 and K_4 used for calculation of characteristic life cycles are given in Table 6.4.

The above mentioned approach has been used to correlate the experimental data from accelerated test with failure mechanics model predictions for -40°C to 125°C, -55°C

Table 6.4 Constants for the damage relationship

	K_1	K ₂	K ₃	K ₄
Lall, et al. [2004]	28769	-1.53	6x10 ⁻⁷	0.7684
Darveaux [2000]	48300	-1.64	3.8x10 ⁻⁷	1.04

to 125°C and 0°C to 100°C. The correlation between the predicted and the experimental values, in addition to convergence with statistical models will be discussed later in the chapter.

6.4 Model Validation

The statistical model presented earlier in the Section 6.2 has been validated against the experimental accelerated test failure data. The effect of the various design parameters on the thermal reliability of the package has been presented. Statistics and failure mechanics based sensitivity factors quantifying the effect of design, material, architecture, and environment parameters on thermal fatigue reliability, have been used to compute life. The predictions from the statistical model have been also compared with the experimental data.

6.4.1 Die Size

The thermo-mechanical reliability of a flip-chip devices generally decreases with the increase in the die size. This effect has been demonstrated in flip-chip devices soldered to both FR4-substrate and BT-substrates. The statistical model has been used to evaluate sensitivity to die size. Wafer-level devices with compliant elastomeric substrates (e.g. µBGA) may not exhibit this effect. In addition, the model predictions focus on solder interconnect failure. If the failure mode is different, such as underfill cracking, then the failure response will be different. The cycles for 63.2% failure from the experimental data and the statistical model has been plotted against the die size of various devices. The predicted values from the statistical model follow the experimental values quite accurately and show the same trend (Figure 6.3). This trend is also

consistent from the failure mechanics standpoint, as the solder joints with larger die are subjected to much higher strains due to the increased distance from the neutral point, thus having lower reliability.

Encapsulated flip-chip packages with die sizes of 5.1mm, 6.5mm and 10mm have been used for the comparison of the model predictions with the actual test failure data. All the three packages had eutectic (Sn37Pb) solder joints of different ball diameter, pitch and pad definition and were subjected to different ATC (Table 6.5). Thus, the model is being tested for its ability to predict both single and coupled effects. Since a linear model has been used to quantify the sensitivity, so the sensitivity factor of -456.18 means that the characteristic life of a flip-chip decreases by 456 cycles when the die size increases by 1 mm and all the other parameters remaining constant. The characteristic life of the three packages plotted in the Figure 6.3 has also been listed in the Table 6.5.

6.4.2 Ball Count

The effect of ball count on thermo-mechanical reliability of the flip-chip devices has been demonstrated in the Figure 6.4. A trend of increase in the reliability with the increase in the ball count is visible, which is also supported by the failure mechanics theory. With the increase in the ball count the shear stress generated in the solder joints due to the thermal mismatch gets distributed, thus reducing the stress in the individual joint and increasing the life of the solder joint. Since this failure mechanics is only applicable in the case where the failure mode is solder joint cracking, so the trend might

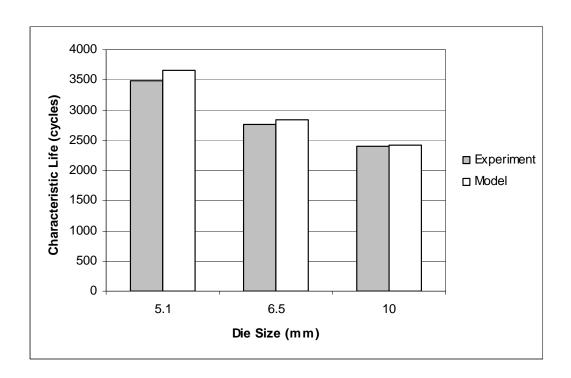


Figure 6.3 Effect of die size on thermal fatigue reliability of encapsulated flip-chip with Sn37Pb solder joints

Table 6.5 Sensitivity factor for the die size and MVR model prediction comparison with the actual failure data

Die Size	Ball	Pitch	Ball	ATC	Characteris		Sensitivity
(mm)	Count	(mm)	Dia		(cycle	s)	Factor
			(mm)		Experiment	Model	
5.1	88	0.2	0.112	-25°C to	3485	3656	
				140°C			
6.5	96	0.25	0.098	-55°C to	2764	2843	-456.18
				140°C			-430.16
10	184	0.2	0.126	-25°C to	2407	2426	
				140°C			

be different for other failure modes such as underfill delamination or copper trace cracking.

Three different encapsulated flip-chip packages with ball count of 88, 96 and 137 subjected to different ATC test condition (Table 6.6) have been used to validate the effect of ball count on the thermo-mechanical reliability predicted by the model. The three packages used for comparison had been subjected to different ATC test conditions and include different solder joint compositions and die sizes. The characteristic life predicted by the model lies in close proximity to the actual characteristic life from the experimental thermal cycling test. The sensitivity factor indicates that with an increase of every single ball in the total ball count keeping all other parameters constant the characteristic life of the flip-chip package increases by 22 cycles.

6.4.3 Underfill Characteristic

Flip-chip devices with the underfill or encapsulation show very high thermomechanical reliability as compared to the flip-chip devices without underfill. This trend hold true for both eutectic (Sn37Pb) and lead-free flip-chip devices mounted on both BT and FR-4 substrate. The main reason for this trend from thermo-mechanics standpoint is that the underfill material provides a mechanical support and shares the shear stresses generated in the solder joints due to the thermal mismatch between the chip and the board. However this trend is reversed for the case where the failure mode is trace cracking, because the application of underfill leads to much higher stresses on the Cu traces and has a peeling effect. Underfill cracking and delamination are the other failure modes commonly associated with encapsulated flip-chip devices along with solder joint

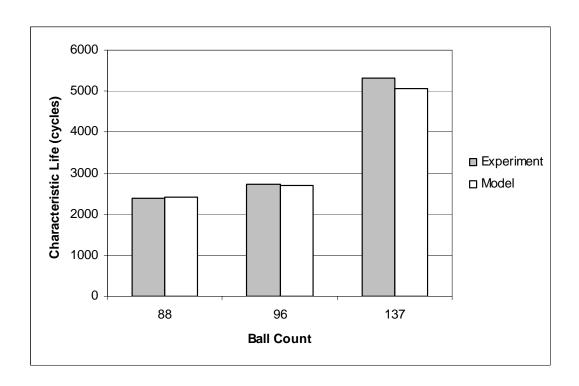


Figure 6.4 Effect of ball count on thermal fatigue reliability of encapsulated flip-chip with leaded and lead-free solder joints.

Table 6.6 Sensitivity factor for the ball count and MVR model prediction comparison with the actual failure data

Ball	Die	Pitch	Solder	ATC	Characteristic Life		Sensitivity
Count	Size	(mm)	Composition		(cycle	s)	Factor
	(mm)				Experiment	Model	
88	5.1	0.2	Sn3.5Ag	-55°C to	2383	2410	
				140°C			
96	12.6	0.46	Sn37Pb	-25°C to	2722	2697	21.99
				140°C			21.99
137	12.6	0.2	Sn0.7Cu	0°C to	5322	5048	
				140°C			

failure and Cu trace cracking. Figure 6.5 shows the comparison of actual and predicted characteristic life of 12.6mm flip-chip device with and without underfill having Sn0.7Cu solder joints, subjected to different thermal cycling conditions. Figure 6.6 shows the actual and predicted effect of the encapsulation on the flip-chip device with different die sizes subjected to thermal cycling of -40°C to 125°C.

The 30x to 40x improvement in the characteristic life of underfilled flip-chip compared to the non-underfilled flip-chip devices is partially due to the coupled effects of die size and thermal cycling conditions and cannot be attributed to absence of underfill alone. The correlation demonstrates that the model is robust enough to accurately predict coupled effects. The added advantage of the perturbation approach demonstrated here is that single effects can also be predicted for configurations which were never tested. For example, the presence of underfill alone is predicted to increase life by 1336 cycles in the configuration analyzed. The underfill factor shows a positive sensitivity versus thermomechanical reliability, indicating increase in solder-joint reliability with presence of underfill. The sensitivity factor derived to quantify the effect of the encapsulation on the thermo-mechanical reliability of the flip-chip device has been listed in the Table 6.7. The model prediction for the characteristic life of the device matches with the actual ATC test failure data within small variation.

6.4.4 Solder Joint Diameter

The thermo-mechanical reliability of the flip-chip devices is also influenced by the solder joint or bump diameter. Flip-chip with bigger bump size usually give higher reliability for the device. This trend is supported by the characteristic life plot for the

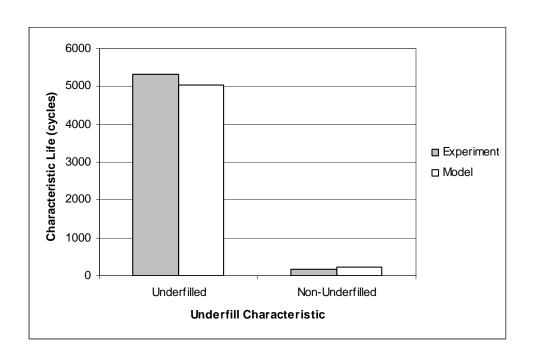


Figure 6.5 Effect of underfill on thermal fatigue reliability of flip-chip devices with 99.3Sn0.7Cu solder joints.

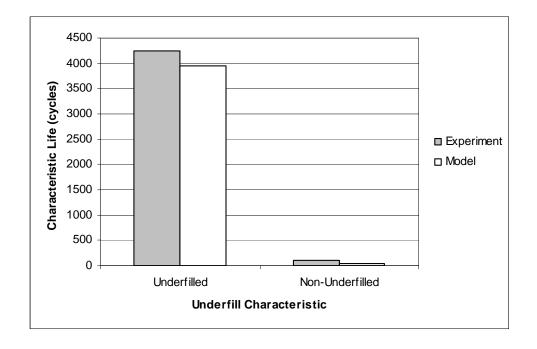


Figure 6.6 Effect of underfill on thermal fatigue reliability of flip-chip with 95.5Sn4.0Ag0.5Cu solder joints.

Table 6.7 Sensitivity factor for underfill characteristic and MVR model prediction comparison with the actual failure data

Encapsulation	Die Size	Solder Composition	ATC	Characteristic Life (cycles)		Sensitivity Factor
	(mm)	_		Experiment	Model	
Underfilled	12.6	Sn0.7Cu	0°C to	5322	5048	
			110°C			
Non-	12.6	Sn0.7Cu	-40°C to	171	213	
Underfill			140°C			1336
Underfiled	5.1	Sn4Ag0.5Cu	-40°C to	4243	3958	1330
			140°C			
Non-	12.6	Sn4Ag0.5Cu	-40°C to	101	41	
Underfill			140°C			

flip-chip device for two different ball diameters. Flip-chip with larger bumps have lower stress concentration and longer crack propagation path in the solder interconnects, thus adding to the thermo-mechanical reliability of the device. The encapsulated flip-chip used for the validation had a die size of 5.1 mm with solder joint composition of 96.5Sn3.5Ag, ball count of 88, and ball diameter of 0.1 mm and 0.12 mm respectively (Figure 6.7). The thermal cycling conditions and all other parameters are constant in both the cases (Table 6.8), so the coupled effects are not included in the life prediction. Model predictions show good correlation with experimental data.

6.4.5 Pad Configuration

Two different configurations, SMD and NSMD, are usually used for mounting the flip-chip device on the PCB. Flip-chip devices mounted on PCB with NSMD pad configuration have been shown to have higher thermo-mechanical reliability. The solder mask in the SMD pad creates a sharp edge in the solder joint which leads to a stress concentration and early failure of the joint, thus resulting in poor reliability compared to solder interconnects with NSMD pad configuration. This is true only when the failure mode is solder joint cracking under thermo-mechanical stresses. SMD pads provide a better reliability in the cases where the failure mode is peeling-off of the pad or cracking of the Cu trace, in that case the cover film over the edges of the SMD pad provides the support to the pad and restrains the pad from peeling off. This is often the case in large out-of-plane deformation, shock and vibration. Figure 6.8 shows the comparison of the characteristic life of underfilled 12.6 mm x 7.46 mm flip-chip devices with different pad configurations. The pad definition effect has been modeled with dummy variables with

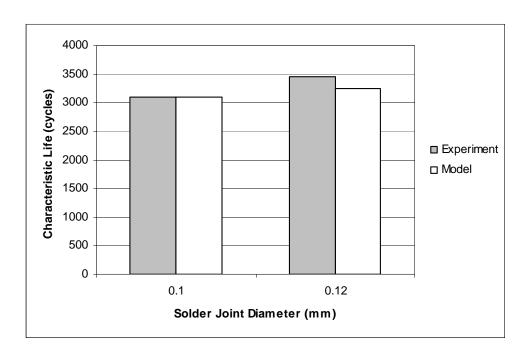


Figure 6.7 Effect of bump diameter on thermal fatigue reliability of encapsulated flip-chip with lead-free (96.5Sn3.5Ag) solder joints and die size of 5.1 mm subjected to – 40°C to 125°C thermal cycle.

Table 6.8 Sensitivity factor for the ball diameter and MVR model prediction comparison with the actual failure data

Ball	Die	Solder	ATC	Characteristic Life		Sensitivity
Dia	Size	Composition		(cycles)		Factor
(mm)	(mm)				I =	
(11111)	(11111)			Experiment	Model	
0.1	5.1	Sn3.5Ag	-25°C to	3092	3104	
		_	140°C			19873
0.12	5.1	Sn3.5Ag	-25°C to	3456	3249	198/3
			140°C			

value "0" indicating an SMD pad and value "1" indicating an NSMD pad. The factor has been shown to have positive sensitivity indicating an increased in thermo-mechanical reliability for change in pad definition from SMD to NSMD. The sensitivity factor derived to quantify the effect of the encapsulation on the thermo-mechanical reliability of the flip-chip device has been listed in the Table 6.9.

6.4.6 Temperature Cycle Magnitude

The thermo-mechanical life of the flip-chip devices, similar to other package architectures, is a function of the environment or the testing condition to which it is subjected. Magnitude of the temperature range experienced during the accelerated test is an influential parameter. The characteristic life of the package decreases with the increase in the temperature range of the ATC (Figure 6.9). Temperature cycle magnitude has a negative sensitivity factor, indicated by decrease in thermo-mechanical reliability with increase in temperature cycle magnitude. Data presented (Table 6.10) includes coupled effects of other parameter variations such as, die size, ball diameter, ball count and cycle time. The predicted values for characteristic life calculated based on the statistical model match the experimental values from the ATC test very accurately.

6.5 Convergence of Statistics and Failure Mechanics Models with Actual Experimental Test Data

Convergence of model predictions from statistics and failure mechanics has been investigated. Figure 6.10 shows the effect of die size on thermal reliability of 5.1 mm, 6.5 mm, and 10 mm flip-chip devices under thermal cycling from 0°C to 100°C, –40°C

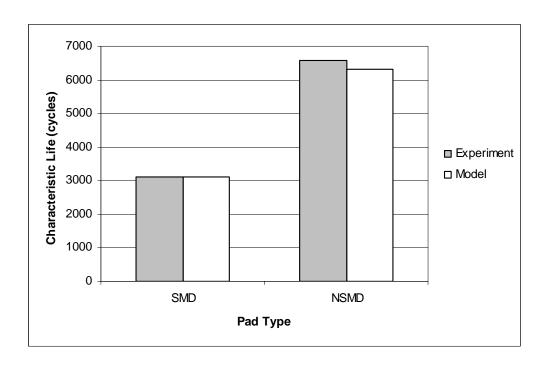


Figure 6.8 Effect of pad configuration on thermal fatigue reliability of encapsulated flipchip with die size of 12.6 mm subjected to 0°C to 100°C thermal cycle.

Table 6.9 Sensitivity factor for pad type and MVR model prediction comparison with the actual failure data

Pad	Die	Solder	ATC	Characteristic Life		Sensitivity
Type	Size	Composition		(cycle	s)	Factor
	(mm)			Experiment	Model	
SMD	12.6	Sn0.7Cu	0°C to	5322	5048	
			100°C			1781.2
NSMD	12.6	Sn37Pb	0°C to	6588	6328	1/01.2
			100°C			

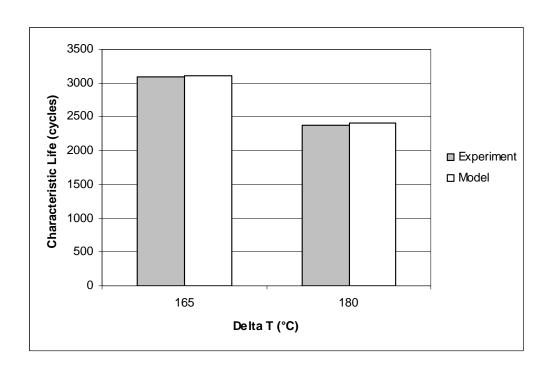


Figure 6.9 Effect of ATC temperature cycle magnitude on thermal fatigue reliability of underfilled flip-chip devices

Table 6.10 Sensitivity factor for ATC temperature range and MVR model prediction comparison with the actual failure data

ATC	Cycle	Die	Ball	Ball	Characteristic Life		Sensitivity
	Time	Size	Count	Diameter	(cycle	s)	Factor
	(mins)	(mm)		(mm)	Experiment	Model	
-25°C to	60	5.1	88	0.10	3092	3104	
140°C							-72.55
-55°C to	17	5.1	88	0.12	2383	2410	-12.33
125°C							

to 125°C, and –55°C to 125°C. Comparison of experimental data with that of predicted values for 63.2% failure cycles from both statistics and failure mechanics model shows good agreement. All the three values for both the devices show a same trend of increased thermal reliability with the increase in the die size.

The correlation can be used in building confidence during trade-off studies by arriving at consistent results in terms of reliability impact of changes in material, configuration and geometry using different modeling approaches. The correlation is especially important, if one considers the vastly different approaches used in arriving at predicted life. The statistics models are based on the two-parameter Weibull distribution, multivariate regression and analysis of variance techniques and therefore account for mechanics of stress-strain only implicitly. The failure mechanics approach are based on Timoshenko beam theory, damage mechanics, material constitutive behavior and do not address the statistical significance and distribution of parameters explicitly.

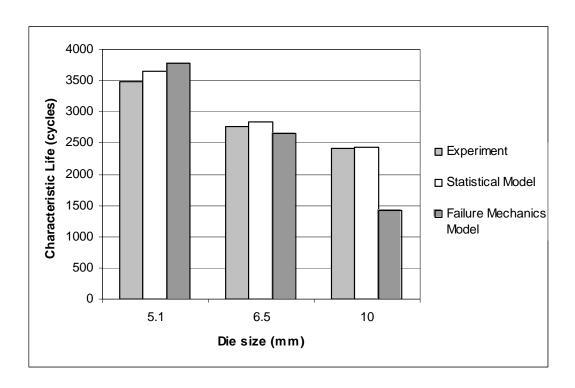


Figure 6.10 Correlation between Accelerated Test, Statistical Model, and Failure Mechanics Model

CHAPTER 7

FEM ANALYSIS OF A FLIP-CHIP PACKAGE

FEM (Finite Element Method) has been widely used for the reliability assessment and analysis of the various electronic components . Several modeling and life-prediction methodologies have been developed for electronics subjected to thermal-cycling [Lall, et al. 2003, Clech 1997, Syed 1995 and Zahn 2002] . Both 2-D (two dimensional) and 3-D (three dimensional) models have been used for the analysis [Pang 1997, Syed 2001]. Usually 3-D models have been shown to give better accuracy and more realistic results as compared to the 2-D models [Vendevelde 2003, Zahn 2003]. Depending upon the geometric and material symmetry of the actual package different configuration of 3-D models like full model, 1/4th or 1/8th symmetry model and diagonal slice model [Zahn 2003 and Pang 2001] can be used for the simulation. Use of 3-D diagonal slice model configuration is preferred over the other configurations for the fully symmetric packages due to its computational efficiency and ability to capture true boundary conditions.

7.1 Overview

In the present study 3-D diagonal slice model has been used for all of the FEA purposes. Various other parameters such as material non-linearity, element type, shape and size also affect the simulation accuracy. The finite element models used in the current work have been checked for their element shapes (aspect ratio and angles) and a

finer mesh in the region of solder bump has been employed for better accuracy. In order to capture the true nature of solder bump, time and temperature dependent non-linear constitutive model has been employed for the simulation.

Exhaustive research has been done on the solder joint reliability of various electronic packages subjected to thermal cycling. It has been established by many researchers that the fatigue life of the solder interconnect is dependent on the amount of inelastic strain energy density (ISED) accumulated by the solder joint during each thermal cycle. A correlation between the solder joint reliability and the ISED output from FEA has also been developed in the past for both leaded [Darveaux 2000] and lead-free [Syed 2004] interconnect. The ISED calculations done from the simulations run for different configuration and various thermal cycles have been used in the current work for the solder joint reliability prediction using the life prediction correlations.

Both linear and non-linear material properties have been used for analyzing the effect of various parametric variations on the reliability of the package. The parametric variations include both design parameters (geometry and material) and the thermal cycling parameters. The two failure modes analyzed for the relative comparison of reliability due to the various parametric variations include solder joint failure and copper trace cracking. Failure modes such as silicon die cracking and delamination have not been analyzed in the present study.

7.2 Model Description

3-D diagonal slice model incorporated with time and temperature dependent nonlinear and linear material properties has been developed in ANSYSTM. Four different geometries had been modeled in order to generate a total of 18 different configurations for the analysis.

7.2.1 Model Variables

Several configurations have been developed for the analysis of flip-chip solder joint integrity and Copper trace integrity. The parametric variations in the model include both geometric and material property variables. Analyses with these variations give an insight into the effect of various parameters on the flip chip reliability.

7.2.1.1 Geometry

The variations in the geometry considered in the FEA analysis. include three bump heights (low, mid and high) and two bump sizes or diameters. The exact geometric dimensions for the model construction were measured from the images of the flip-chip bump cross-section. The dimensions of the fixed parameters are given in the Table 7.1 and the dimensions of variable parameters are listed in the Table 7.2.

7.2.1.2 Material

Both eutectic (62Sn36Pb2Ag) and lead-free (Sn3.5Ag0.75Cu) solder material have been considered for the analysis. Also three different underfill materials have been considered for the analysis. The material variations used in all the 18 configurations for the simulation have been listed in the Table 7.2.

Table 7.1 Dimensions of fixed parameters used for the finite element model

Parameter	Dimension (inch)
Pad thickness	0.0007
Slice length (Si Die)	0.096
Slice length (PCB)	0.192
Slice width	0.0056
Height (Si Die)	0.028
Height (PCB)	0.0212

Table 7.2 Material variations and the dimensions of the variable geometric parameters

Test Case	Solder	Underfill	Bump Height (mils)	Bump Size (mils)
1	62Sn36Pb2Ag	UF-4	1.0 (Low)	4
2	62Sn36Pb2Ag	UF-1	2.5 (High)	4
3	62Sn36Pb2Ag	UF-4	2.5 (High)	4
4	62Sn36Pb2Ag	UF-4	2.0 (Mid)	4
5	62Sn36Pb2Ag	UF-1	1.0 (Low)	4
6	62Sn36Pb2Ag	UF-3	2.0 (Mid)	4
7	62Sn36Pb2Ag	UF-2	2.5 (High)	4
8	62Sn36Pb2Ag	UF-2	2.0 (Mid)	3
9	62Sn36Pb2Ag	UF-3	2.0 (Mid)	3
10	Sn3.5Ag0.75Cu	UF-2	2.5 (High)	4
11	Sn3.5Ag0.75Cu	UF-2	2.0 (Mid)	3
12	Sn3.5Ag0.75Cu	UF-4	2.5 (High)	4
13	Sn3.5Ag0.75Cu	UF-4	2.0 (Mid)	3
14	Sn3.5Ag0.75Cu	UF-3	2.5 (High)	4
15	Sn3.5Ag0.75Cu	UF-3	2.0 (Mid)	3
16	Sn3.5Ag0.75Cu	UF-1	1.0 (Low)	4
17	Sn3.5Ag0.75Cu	UF-1	2.0 (Mid)	4
18	Sn3.5Ag0.75Cu	UF-1	2.5 (High)	4

7.2.2 Elements Used

The model has been map meshed using brick shaped 8 noded hexahedral isoparameteric elements (Figure 7.1). Since the 8 noded hexahedral element provides better results and higher accuracy as compared to the tetrahedral elements so the hexahedral elements have been used for meshing the entire model. 2x2x2 Gaussian quadrature integration option has been used for the solution.

VISCO107 elements have been used for the solder bump and SOLID45 elements for the rest of the materials. VISCO107 has rate-dependent large strain plasticity capabilities and is used to represent non-linear behavior of visco-plastic materials. Another advantage of using VISCO107 for solder is to facilitate the constitutive modeling of the solder material using Anand's model. SOLID45 element also has large strain capabilities.

7.2.3 Mesh and Boundary Conditions

The complete meshed model had 11,850 elements in all for the models with high and medium bump height and 11,130 elements with low bump height models. Fully meshed model with the coordinate system is shown in Figure 7.2. The bump region has been finely meshed in order to get higher accuracy. The geometry of the elements has been checked for the AR (aspect ratio) and the angles as the simulations run with the model having elements with poor AR and angles can give inaccurate and misleading results.

Three different solder joints with different bump gap heights have been modeled.

The Low gap bump with height 1.0mil, mid gap bump with height 2.0mils and high gap

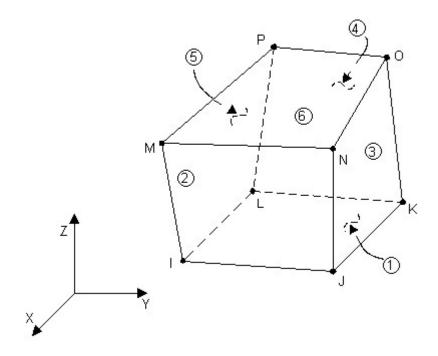


Figure 7.1 Eight noded hexahedral isoparametric element

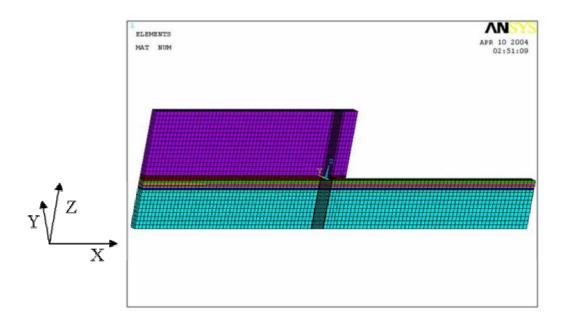


Figure 7.2 Fully meshed model with coordinate axes

bump with height 2.5mils have been modeled for the analysis. Both the Copper pads have been meshed with two element layers each. As shown in Figure 7.3 the low gap bump has been meshed with 3 element layers and the other two bump configurations have been modeled with six layers each. Since the objective of the simulation is to analyze solder joint failure so the solder joint has to be finely meshed.

Symmetry boundary conditions as described in the Figure 7.4 have been used for simulating true conditions. The boundary conditions have been applied on the nodes. The coupled boundary condition applied on the symmetry plane implies that the nodes on that surface are constrained to remain coplanar. One node on the bottom left corner of the model has been fully constrained in order to prevent the rigid body motion.

7.2.4 PCB Material Layers

Various material layers have been modeled with the geometric dimensions provided by the Vendor. For simplification the underfill fillet has not been considered for the solder joint integrity simulation but it was considered for the Copper trace integrity simulation as the fillet has significant impact on the stresses developed in the trace. A close view of the schematic of the different layers modeled has been shown in Figure 7.5. The thickness and the material properties of each layer of the PCB has been listed in the Table 7.3.



Figure 7.3 Solder bump mesh for the three different gap heights

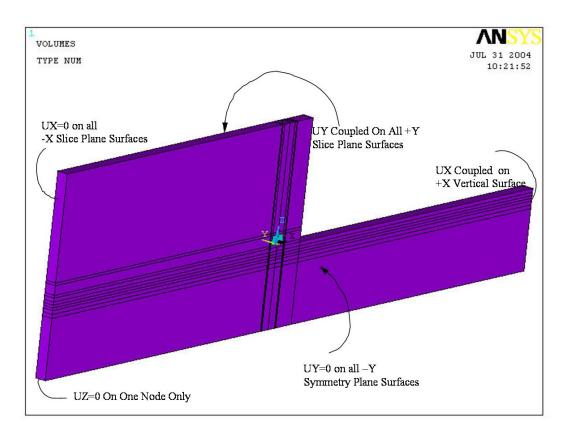


Figure 7.4 Schematic of the boundary conditions applied on the model for the simulation

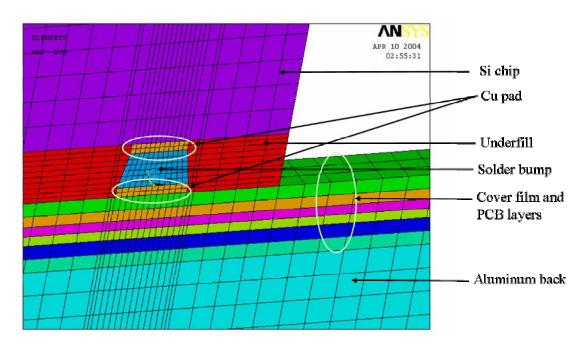


Figure 7.5 Schematic of the material layers modeled for the simulation

Table 7.3 Material properties and thickness of the PCB layers

Layer	Thickness	Material	
Material	(mils)	Properties	
Cover film	1.0	E(Kpsi)	500.38
Cover min	1.0	α	18 ppm/ ⁰ C
Adhesive 1	0.8	E(Kpsi)	105.88
runesive i	0.0	α	118 ppm/ ⁰ C
Copper	0.7	Е	9717.53
Соррег	0.7	α	17 ppm/ ⁰ C
Adhesive 2	0.7	E(Kpsi)	105.88
runesive 2		α	118 ppm/ ⁰ C
Base polyimide	1.0	E(Kpsi)	500.38
Base poryminde		α	18 ppm/ ⁰ C
Adhesive 3	1.0	E(Kpsi)	159.54
runesive 3		α	218 ppm/ ⁰ C
Aluminum	16.0	E(Kpsi)	10007.6
Mummum	10.0	α	10 ppm/ ⁰ C

7.2.5 Material Properties

7.2.5.1 Linear Material Properties

Linear isotropic material properties have been assigned to all the elements except the solder bump elements. The solder bump elements have been modeled with both linear and non-linear constitutive relations. The linear isotropic material properties assigned in the model have been listed in the Table 7.4. The non-linear constitutive relations for the solder bump has been discussed in the next section.

7.2.5.2 Non-Linear Solder Material Properties

Solder alloy is a viscoplastic material which means that it exhibits both time dependent creep and plasticity. Thus it is essential to use time and temperature dependent non-linear material model for the solder bump. Widely used and established Anand's model which is also a standard feature in ANSYSTM has been used to model both eutectic (62Sn36Pb2Ag) [Darveaux, 2000] and lead-free [Amagai et al, 2002] solder material. In the Anand's model both creep and plasticity have been coupled together with the help of flow and evolutionary equations:

Flow equation
$$\frac{d\varepsilon_p}{dt} = A(\sinh(\varsigma \sigma / s_o)^{\frac{1}{m}} \exp\left(\frac{-Q}{kT}\right)$$

$$\frac{ds_o}{dt} = \left\{ h_o \left(|B| \right)^a \frac{B}{|B|} \right\} \frac{d\varepsilon_p}{dt}$$

Evolutionary equation

where, B= 1-
$$\frac{s_o}{s^*}$$
 and $s^* = s \left[\frac{d\varepsilon_p/dt}{A} \exp\left(\frac{Q}{kT}\right) \right]^n$

Table 7.4 Linear isotropic material properties with vendor data for the underfill materials

Material	E(psi)	Poisson's ratio	CTE (per °C)
Silicon	23641000	0.278	2.50E-06
UF-1	1232800	0.25	3.30E-05
UF-2	812211	0.25	4.50E-05
UF-3	391602	0.25	6.10E-05
UF-4	449617	0.25	6.70E-05
Lead-free Solder	5729100	0.3	2.00E-05
Eutectic Solder	4163600	0.35	2.45E-05
Copper pad	18710000	0.34	1.63E-05
Cover film	500400	0.3	1.80E-05
Adhesive 1	105900	0.35	1.18E-04
Copper	9717500	0.34	1.70E-05
Adhesive 2	105900	0.35	1.18E-04
Base polyimide	500400	0.35	1.80E-05
Adhesive 3	159500	0.35	2.18E-04
Aluminum	10008000	0.3	2.30E-05

The constants of the Anand's model for the simulation have been assigned through the standard input for VISCO107 element in ANSYSTM. The value of the constants used for modeling both the eutectic [Darveaux 2000] and lead-free [Amagai, et al. 2002] solder material have been listed in the Table 7.5.

7.2.6 Inelastic Strain Energy Density

Several researchers have established inelastic strain energy density (ISED to be the damage proxy for solder joint thermo-mechanical reliability of electronic packages. Damage relationships correlating the solder joint life with the ISED accumulated per thermal cycle by the solder joint have also been developed. These relationships can be used for the life prediction of the electronic packages with solder joint cracking as the failure mode. The ISED can be calculated from the simulation. In ANSYSTM VISCO107 element has plastic work (PLWK) as a standard output, ISED has been calculated in the present study by volume averaging PLWK over the whole solder bump volume. Some researchers volume average PLWK over the few layers in the vicinity of the interface instead of the whole solder volume. Plastic work accumulated in the solder joint over the complete thermal cycle has been found to be stabilized after the first cycle. Consequently the simulation is run for only two cycles and the ISED is calculated based on the plastic work accumulated during the second thermal cycle. ISED for the solder joint is given by:

$$\Delta W_{i} (ISED) = \frac{\left(\sum_{n=1}^{total} _elements \\ \Delta W^{(n)} \times V_{n} \right)}{\left(\sum_{n=1}^{total} _elements \\ \sum_{n=1}^{total} V_{n} \right)}$$

Table 7.5 Values of the constants of Anand's viscoplastic model

Anand's constants for solder					
Pb-free			Eutectic		
Sn3.5Ag0.75Cu	ANSYS	Model	62Sn36Pb2Ag		
Value	Input	Parameter	Value	Definition	
135.72	C1	So (psi)	1800	Initial Value of Deformation Resistance	
8400	C2	Q/k (1/K)	9400	Activation Energy / Boltzmann.s Constant	
4610000	C3	A (1/sec)	4000000	pre-exponential factor	
0.038	C4	ξ	1.5	multiplier of stress	
0.162	C5	m	0.303	stain rate sensitivity of stress	
448000	C6	ho (psi)	200000	hardening constant	
150.8	C7	s^ (psi)	2000	coefficient for deformation resistance saturation value	
0.0046	C8	n	0.07	Strain rate sensitivity of saturation (deformation resistance) value	
1.56	C9	a	1.3	strain rate sensitivity of hardening	

where $\Delta W^{(n)}$ is plastic work accumulated by n^{th} element during the second thermal cycle of the simulation and it is standard output in ANSYSTM for VISCO107 element in form of PLWK and V_n volume of the n^{th} element.

7.3 Material Characterization of Underfill Materials

The material characterization of the underfill materials provided by the supplier has been performed. The stress-strain curve for five different materials has been plotted from the uni-axial tensile testing of the samples fabricated with the in house facilities (Figure 7.6) at Auburn University. The elastic modulus for the linear range has also been calculated in order to verify the vendor data. The simulations for 0-70°C ATC has been run with both the vendor data and the measured properties in order to see the impact of difference in the material properties on the plastic work accumulated in the solder joint during the thermal cycle.

7.3.1 UF-1

UF-1 is a capillary flow underfill material with highest value of elastic modulus and lowest value of CTE (coefficient of thermal expansion) among all the underfill materials tested. The stress-strain curve from the test data has been plotted in Figure 7.7. The samples were tested at the starin rate of 0.001 sec⁻¹, as the strain rates encountered during the ATC of flip-chip fall in this range.

The maximum strains encountered by the underfill during the simulation of both 0-70°C and 0-90°C thermal cycles had been measured in order to make sure that the elastic properties used for the simulations falls within the linear range. The point P₁ and



Figure 7.6 Uniaxial test specimen and the assembly equipment used for the sample preparation and cure.

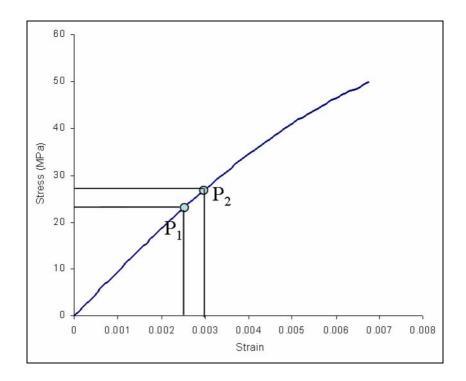


Figure 7.7 Stress-strain plot from the uniaxial tensile test for UF-1 underfill material

P₂ corresponds the maximum strains encountered by the UF-1 underfill during 0-70°C and 0-90°C ATC respectively. It can be seen that the maximum strain for 0-90° is about 3000 microns and this point falls well within the linear range of the stress-strain curve. The contour plot of the strain distribution has been shown in the Figure 7.8. This shows that the maximum strain occurs on the top edge of the underfill just below the silicon die. The elastic modulus of the UF-1 underfill material for the linear region measured from the uniaxial tensile test has been found to be 9.21 GPa which is a 8.35% higher than the value of 8.5 GPa provided by the vendor

7.3.2 UF-2

UF-2 is also a capillary flow underfill with elastic modulus lower than the UF-1 underfill and the CTE higher. The stress strain curve from the uniaxial tensile test data has been plotted in the Figure 7.9 and the test was again carried out at the strain rate of 0.001 sec⁻¹. The points P₁ and P₂ plotted on the curve indicate the maximum strain encountered during the 0-70° and 0-90°C test cycle simulation and it is seen that the maximum strain during the 0-90°C test cycle is about 5000 microns which is higher than the UF-1 underfill material but still it lies well within the linear range of the material. The elastic modulus for the linear region measured from the uniaxial tensile test is 5.22 GPa which is 6.78% lower than the value of 5.6 GPa provided by the vendor.

7.3.3 UF-3

UF-3 is a reflow type underfill material with elastic modulus lower and the CTE higher than the capillary flow underfill materials. The stress-strain curve from the

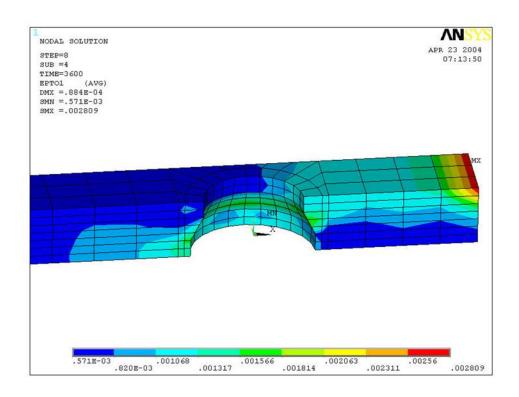


Figure 7.8 Strain distribution in UF-1 underfill with low gap height bump

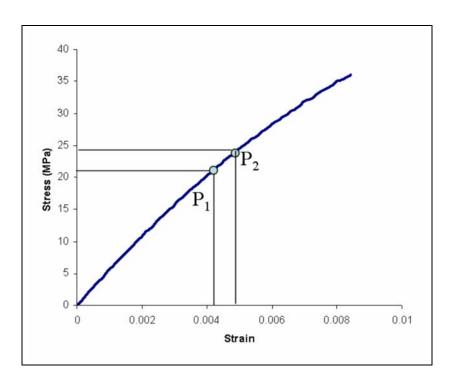


Figure 7.9 Stress-strain plot from the uniaxial tensile test for the UF-2 underfill

uniaxial tensile test data has been plotted in the Figure 7.10. It is visible form the plot that the maximum strain during the 0-90°C test cycle is around 5500 microns which lies well within the linear range of the material. The elastic modulus of the UF-3 material for the linear region measured from the uniaxial tensile test is 3.11 GPa which is 15.18% higher than the value of 2.7 GPa provided by the vendor. Figure 7.11 shows the strain distribution contour plot for the UF-3 underfill material with high bump gap height configuration.

7.3.4 UF-4

UF-4 is also a reflow type underfill material with elastic modulus lower and the CTE higher than the UF-3 underfill material. The stress-strain curve from the uniaxial tensile test data has been plotted in the Figure 7.12. It is visible form the plot that the maximum strain (5500 microns) goes just beyond the linear region of the material. But still the linear isotropic material properties have been used in the simulation for the approximation. Figure 7.13 shows the strain distribution in the UF-4 underfill material from 0-90°C thermal cycle simulation.

It is seen from the Figure 7.13 that the maximum strain in case of the UF-4 material lies at the solder bump and underfill interface edge as compared to the die and underfill interface edge in case of other underfill materials. The elastic modulus of the UF-4 material for the linear region measured from the uniaxial tensile test is 2.53 GPa which is 18.4% lower than the value of 3.1 GPa provided by the vendor.

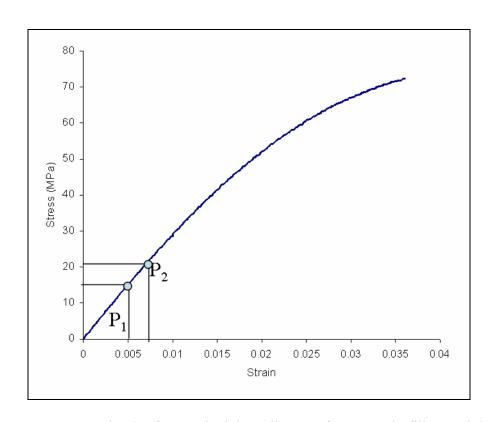


Figure 7.10 Stress strain plot from uniaxial tensile test of UF-3 underfill material

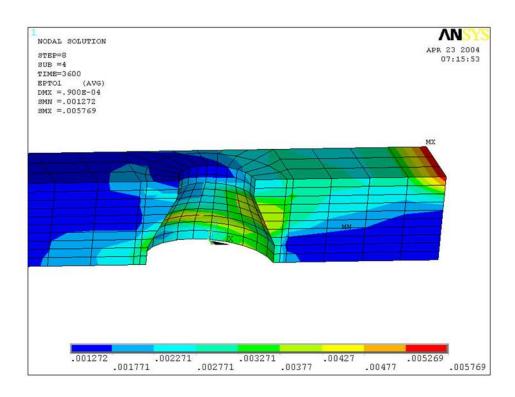


Figure 7.11 Strain distribution contour plot in UF-3 underfill material with high gap height bump configuration.

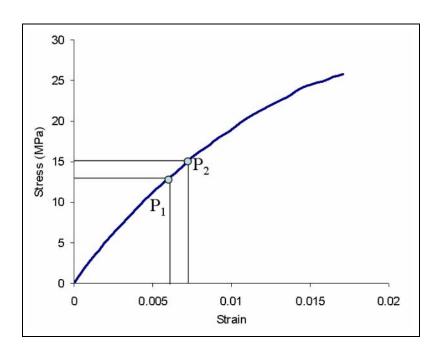


Figure 7.12 Stress strain plot from uniaxial tensile test of UF-4 underfill material

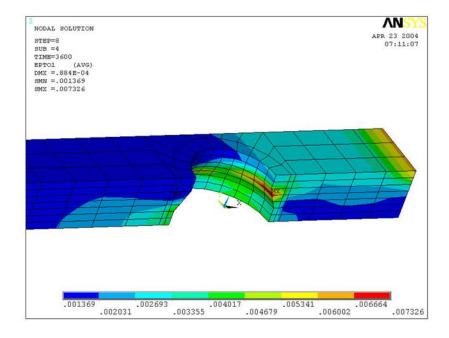


Figure 7.13 Strain distribution contour plot in UF-4 underfill material with low gap height bump configuration

7.3.6 Effect of Measured Properties on the Simulation Results

The correct input of material properties in the FEA model is vital for getting accurate results from the simulation. The simulations for 0-70°C ATC were run with both the material properties measured in house as well as with the material data provided by the vendor for the 15 different configurations provided by the vendor. Difference in the simulation results can be observed from the Table 7.6.

Since higher value of ISED for the same configuration implies lower reliability, thus except UF-1 underfill all the other three underfill give higher reliability with the vendor data. So the models will under predict the solder joint reliability in case of UF-1 and over predict in other cases if the vendor data is used in the simulation.

7.4 Solder Joint Integrity in Accelerated Thermal Cycling

The most serious concerns in the flip-chip reliability is the solder interconnect fatigue failure due to thermal cyclic loading. Due to the CTE mismatch within the various components of the flip-chip package, stresses are developed in the component whenever thermal cycling takes place. These stresses lead to the fatigue failure of the component when the thermal cycling is continued for long. It has been established through various experimental studies and field failure analysis that the solder interconnect is the most susceptible to such fatigue failures. Due to this finite element analysis and simulation of solder joint integrity becomes extremely important. In the current study simulation of 0-70°C and 0-90°C ATC along with three different field profiles has been done and presented in this chapter.

Test	Solder	Underfill	Bump Gap	Bump Size	Inelastic Strain Energy Density Per Cycle (psi)	
Case	Composition		Height	(mils)	Computed with Vendor Data	Computed with AU Data
1	62Sn36Pb2Ag	UF-4	Low	4	33.65	37.98
2	62Sn36Pb2Ag	UF-1	High	4	10.75	10.65
3	62Sn36Pb2Ag	UF-4	High	4	28.42	29.01
4	62Sn36Pb2Ag	UF-4	Mid	4	29.73	31.05
5	62Sn36Pb2Ag	UF-1	Low	4	12.49	12.13
6	62Sn36Pb2Ag	UF-3	Mid	4	25.95	26.89
7	62Sn36Pb2Ag	UF-2	High	4	16.52	16.65
8	62Sn36Pb2Ag	UF-3	Mid	3	16.89	17.11
9	62Sn36Pb2Ag	UF-3	Mid	3	28.22	27.19
10	Sn3.5Ag0.75Cu	UF-3	High	4	14.09	14.06
11	Sn3.5Ag0.75Cu	UF-3	Mid	3	15.80	15.86
12	Sn3.5Ag0.75Cu	UF-4	High	4	25.52	25.67
13	Sn3.5Ag0.75Cu	UF-4	Mid	3	29.40	30.05
14	Sn3.5Ag0.75Cu	UF-3	High	4	22.66	22.31
15	Sn3.5Ag0.75Cu	UF-3	Mid	3	26.48	25.82

Table 7.6 Simulation results for 0-70°C thermal cycle with vendor and measured data

7.4.1 0-70°C

The thermal profile shown in the Figure 7.14 has been simulated in ANSYSTM for the analysis of solder joint integrity and the comparative study in order to see the effect of various variations on the solder joint reliability. The cycle starts at the room temperature (25°C) has a dwell of 12 mins at the extreme temperatures of 0°C and 70°C and the ramp time between the extreme temperatures is 3 mins, therefore the total time period for the cycle is 30 mins. Simulations for the eighteen different configuration listed earlier in the section 2.1.2 have been run for this profile and the simulation results are listed in Table 7.7. Inelastic strain energy density averaged over the complete solder volume has been calculated as discussed in section 2.6. Since ISED is a true indicator of the damage accumulated by the solder joint, which leads to the crack initiation and finally failure of the solder joint, so it has been used as the basis for the comparison of reliability for different configurations of the flip-chip.

Figure 7.15 shows the distribution of the magnitude of the ISED accumulated in the solder joint during one complete thermal cycle for test case 1 which consist of low gap height eutectic solder bump with UF-1 underfill. It is visible that the magnitude of the ISED accumulated is maximum at the top left corner of the bump, which indicates that the crack would initiate at this location and than propagate, also there is a high ISED accumulation region at the bottom right corner of the bump which implies a possibility of secondary crack initiation in this region before the primary crack completely propagates.

Figure 7.16 and Figure 7.17 show the contour plot of the distribution of the ISED accumulated and the Von-Mises stress in the solder bump. The plots shown here are for test case 12 which consist of high gap height lead-free solder bump with UF-4

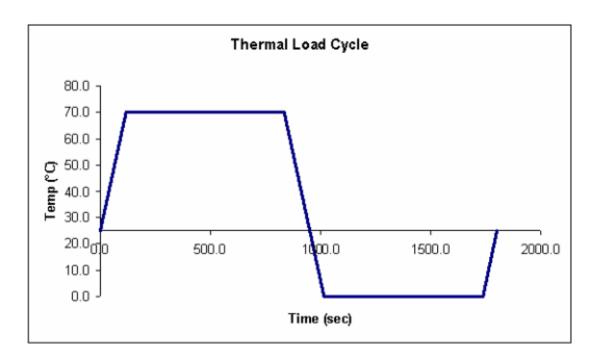


Figure 7.14 0-70°C accelerated thermal cycle profile

Table 7.7 Simulation results for 0-70°C accelerated thermal cycle

Test Case	Solder Composition	Underfill	Bump Gap Height	Bump Size (mils)	Normalized Inelastic Strain Energy Density per Cycle
1	62Sn36Pb2Ag	UF-4	Low	4	4.415
2	62Sn36Pb2Ag	UF-1	High	4	1.208
3	62Sn36Pb2Ag	UF-4	High	4	3.543
4	62Sn36Pb2Ag	UF-4	Mid	4	3.716
5	62Sn36Pb2Ag	UF-1	Low	4	1.423
6	62Sn36Pb2Ag	UF-3	Mid	4	3.487
7	62Sn36Pb2Ag	UF-2	High	4	1.964
8	62Sn36Pb2Ag	UF-2	Mid	3	2.024
9	62Sn36Pb2Ag	UF-3	Mid	3	3.550
10	Sn3.5Ag0.75Cu	UF-2	High	4	1.795
11	Sn3.5Ag0.75Cu	UF-2	Mid	3	1.890
12	Sn3.5Ag0.75Cu	UF-4	High	4	3.444
13	Sn3.5Ag0.75Cu	UF-4	Mid	3	3.890
14	Sn3.5Ag0.75Cu	UF-3	High	4	3.047
15	Sn3.5Ag0.75Cu	UF-3	Mid	3	3.483
16	Sn3.5Ag0.75Cu	UF-1	Low	4	1.045
17	Sn3.5Ag0.75Cu	UF-1	Mid	4	1.012
18	Sn3.5Ag0.75Cu	UF-1	High	4	1.000

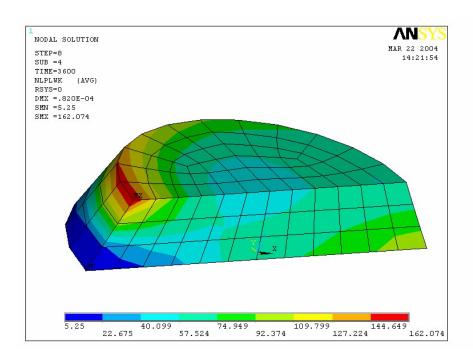


Figure 7.15 Contour plot of nodal values of ISED in the solder bump for test case 1

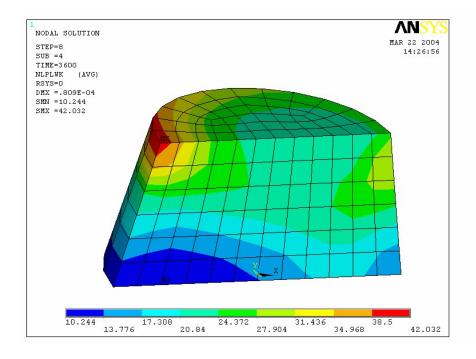


Figure 7.16 Contour plot of the nodal values of the ISED accumulated in the solder bump for test case 12

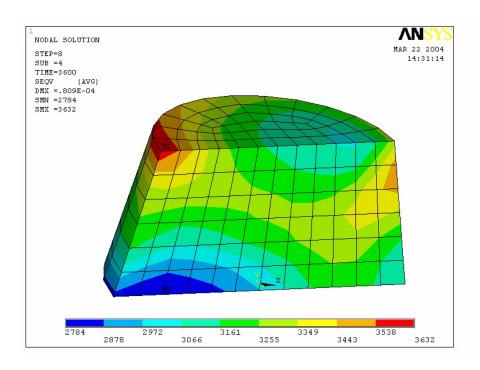


Figure 7.17 Contour plot of the nodal values of the Von-Mises stress in the solder bump for test case 12

underfill. It is visible that the distribution for both the ISED accumulated and the Von-Mises stress remains more or less the same but in this case it can be observed that the region for the secondary crack has shifted from the bottom right (test case-1) to the top right. This shift in the secondary crack location may speed up the failure, as now the primary crack does not have to travel until the other end in order to cause a failure. It is also seen that the contour plot of ISED follows almost the stress contour.

7.4.1.1 Effect of Solder Joint Material Composition

It is visible form the Figure 7.18 that the value of ISED accumulated per cycle for eutectic solder bump is higher as compared to the lead-free bump for the capillary flow UF-1 underfill material for both high gap and low gap height bumps. For eutectic solder bumps the difference in the ISED accumulated between the high and low gap height bump is higher as compared to the lead-free solder bumps.

The eutectic solder bumps have higher value of ISED than the lead-free bumps in case of UF-2 underfilled flip-chip also for both the mid and high gap height bumps. But the difference in the value of ISED between mid and high gap for UF-2 is higher in the case of lead-free bumps. For both the re-flow encapsulant materials the ISED accumulated in the solder joint per cycle is less for the lead-free bump. UF-4 is more sensitive to the solder joint composition as far as the solder joint reliability is concerned.

7.4.1.2 Effect of Underfill Composition

Solder joint reliability is also sensitive to the undefill material, a trend of higher reliability with the capillary flow encapsulants as compared to the re-flow encapsulants is

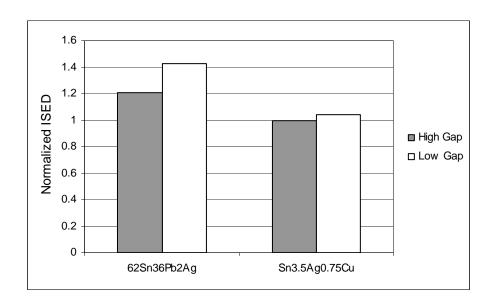


Figure 7.18 Normalized ISED for UF-1 underfill material with low and high gap height bump diameter 4 mils

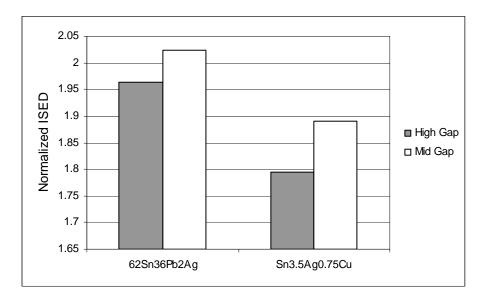


Figure 7.19 Normalized ISED for UF-2 underfill material with mid (3 mils) and high (4 mils) gap height and bump diameter 4 mils

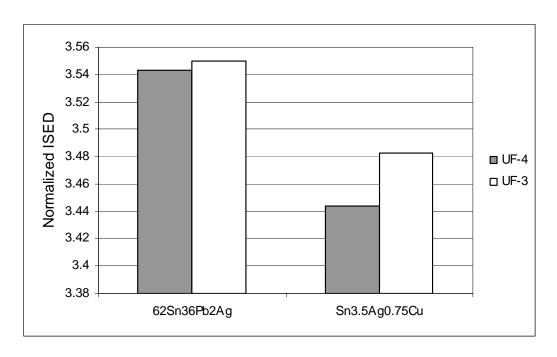


Figure 7.20 Normalized ISED for UF-4 (4 mils) and UF-3 (3 mils) underfill material with high and mid gap height solder bumps respectively

visible form the Figure 7.21 to Figure 7.23. Figure 7.21 shows the comparison of ISED for three different underfill materials with eutectic solder bumps.

The value of ISED is higher for the re-flow encapsulants in the case of lead-free solder bumps also (Figure 7.22 and Figure 7.23). UF-4 has the highest value of ISED accumulated per cycle in the solder joint and the UF-1 capillary flow encapsulant has the lowest. This implies that the flip chip encapsulated with the UF-1 underfill will have maximum solder joint reliability.

7.4.1.3 Effect of Bump Gap Height

Figure 7.24 shows the normalized ISED accumulated by the eutectic solder joint of three different gap heights for a flip-chip with UF-4 encapsulant. Trend of increasing ISED with decreasing gap height is observed. It is also observed that the ISED increases more drastically when the solder bump height is reduced from mid gap height to low gap height as compared to the change from high gap height to mid gap height. Figure 7.25 shows the normalized ISED in case of lead-free solder with capillary flow underfill. Same trend is also observed for the lead-free solder bumps with both reflow and capillary flow encapsulant.

7.4.1.4 Effect of Bump Size

Two different bump sizes have been used for the simulation of the 18 configurations. The solder bump with the bigger size (4 mils) have lower ISED value and thus higher reliability. Flip-chip with eutectic bumps and UF-3 re-flow

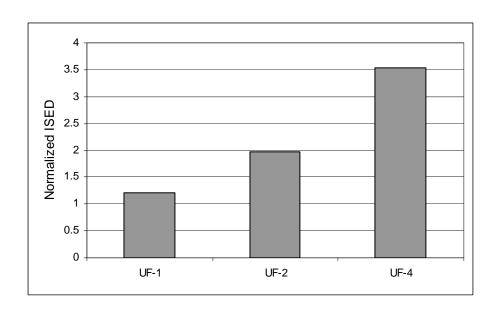


Figure 7.21 Normalized ISED for high gap height 4 mils eutectic solder bump with different underfill materials

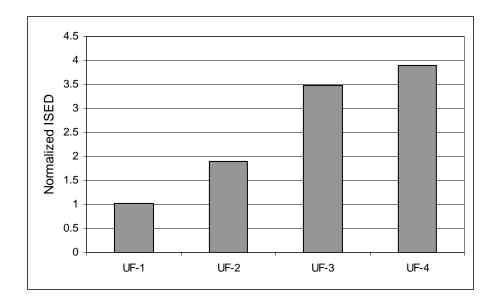


Figure 7.22 Normalized ISED for mid gap height 3 mils lead-free solder bumps with different underfill materials

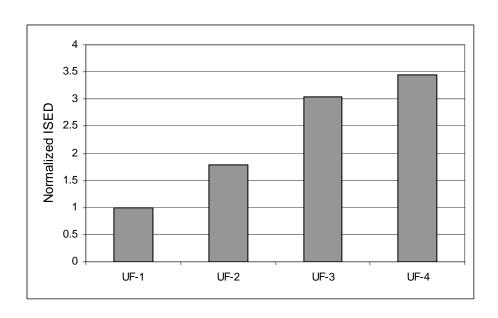


Figure 7.23 Normalized ISED for high gap height 4 mils lead-free solder bumps with different underfill materials

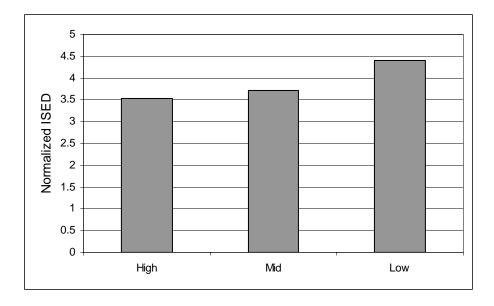


Figure 7.24 Normalized ISED for 4 mils eutectic solder bumps with UF-4 underfill material and different gap heights

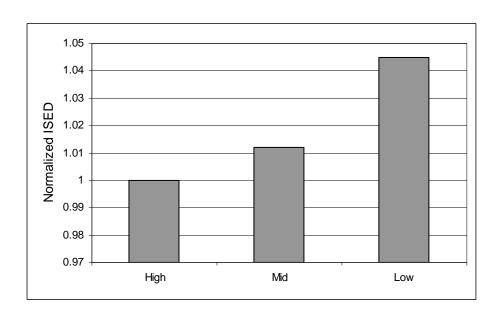


Figure 7.25 Normalized ISED for 4 mils lead-free solder bumps with UF-1 underfill material and different gap heights

encapsulant has been used (Figure 7.26) to show the effect of the bump size on the thermal reliability.

7.4.1.5 Summary

- Lead-free solder have lower ISED compared to eutectic tin-lead solder for all
 investigated underfills. However, this does not necessarily mean that lead-free
 solder will have better reliability as the damage relationships for the two different
 solder materials will be different.
- Increase in gap height lowers ISED for both eutectic and lead-free solders, this means that the flip-chip with higher gap height will have higher reliability.
- For the underfills investigated, capillary flow underfills exhibit lower ISED as compared to the reflow encapsulant for both eutectic as well as lead-free solders.
- Increase in the bump size lowers the ISED for both eutectic and lead-free solders.

7.4.2 0-90°C

Thermal profile shown in Figure 7.27 has been simulated for the analysis of solder joint reliability when the flip-chip is subjected to 0-90°C ATC. The cycle starts at the room temperature (25°C) has a dwell of 12 mins at the extreme temperatures of 0°C and 90°C and the ramp time between the extreme temperatures is 3 mins, therefore the total time period for the cycle is 30 mins.

Simulations for the eighteen different configuration have been run for this profile and the simulation results are listed in Table 7.8. Since the UF-4 underfill material has a Tg (glass transition temperature) in the range of 70-75°C, so the it behaves very

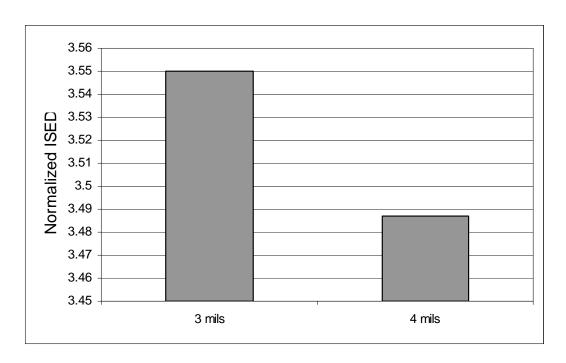


Figure 7.26 Normalized ISED for mid gap height eutectic solder bumps with UF-3 underfill with different bump diameter

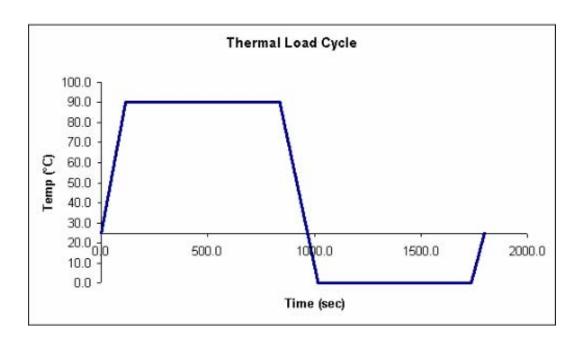


Figure 7.27 0-90°C accelerated thermal cycle profile

differently as compared to the other underfill materials whose Tg is above 90°C. The normalized ISED listed in the Table 7.8 has been evaluated considering the Tg of UF-4 above 90°C so that the Tg does not affect the relative comparison of the reliability of various configurations. The effect of Tg of the underfill material on the solder joint reliability has been analyzed separately.

7.4.2.1 Effect of Solder Joint Material Composition

It is observed form the Figure 7.28-7.31 that the lead-free solder bumps accumulate higher ISED per cycle as compared to the eutectic solder bumps for all the configurations. Thus there is a reversal in the trend for the 0-90° ATC as compared to the trend for 0-70°C. This however does not necessarily mean higher reliability for the lead-free solder bumps, as the reliability prediction depends on the damage relationship which is different for both the solder compositions. This means that inspite of higher ISED value the flip-chip with lead-free bump might exhibit higher reliability.

7.4.2.2 Effect of Underfill Composition

The reliability trend for the underfill composition when the flip-chip is subjected to 0-90°C ATC remains the same as in case of 0-70°C ATC. Figures 7.32, 7.33 and 7.34 exhibit the trend of increased value of normalized ISED from capillary to re-flow encapsulant for various configurations of the flip-chip.

Table 7.8 Simulation results for 0-90°C accelerated thermal cycle

Test Case	Solder Composition	Underfill	Bump Gap Height	Bump Size (mils)	Normalized Inelastic Strain Energy Density per Cycle
1	62Sn36Pb2Ag	UF-4	Low	4	3.354
2	62Sn36Pb2Ag	UF-1	High	4	0.931
3	62Sn36Pb2Ag	UF-4	High	4	2.678
4	62Sn36Pb2Ag	UF-4	Mid	4	2.780
5	62Sn36Pb2Ag	UF-1	Low	4	1.093
6	62Sn36Pb2Ag	UF-3	Mid	4	2.710
7	62Sn36Pb2Ag	UF-2	High	4	1.489
8	62Sn36Pb2Ag	UF-2	Mid	3	1.548
9	62Sn36Pb2Ag	UF-3	Mid	3	2.732
10	Sn3.5Ag0.75Cu	UF-2	High	4	1.653
11	Sn3.5Ag0.75Cu	UF-2	Mid	3	1.720
12	Sn3.5Ag0.75Cu	UF-4	High	4	2.834
13	Sn3.5Ag0.75Cu	UF-4	Mid	3	3.204
14	Sn3.5Ag0.75Cu	UF-3	High	4	2.346
15	Sn3.5Ag0.75Cu	UF-3	Mid	3	2.940
16	Sn3.5Ag0.75Cu	UF-1	Low	4	1.115
17	Sn3.5Ag0.75Cu	UF-1	Mid	4	1.030
18	Sn3.5Ag0.75Cu	UF-1	High	4	1.000

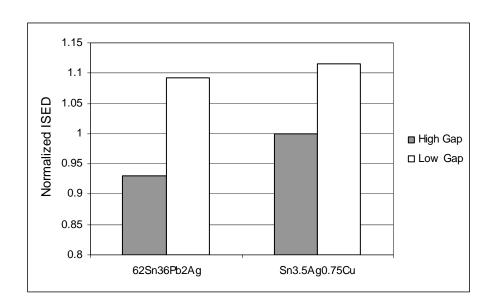


Figure 7.28 Normalized ISED for UF-1 underfill material with low and high gap height 4 mils solder bumps

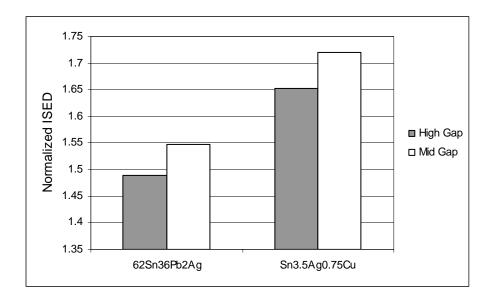


Figure 7.29 Normalized ISED for UF-2 underfill material with mid (3 mils) and high (4 mils) gap height 4 mils solder bumps

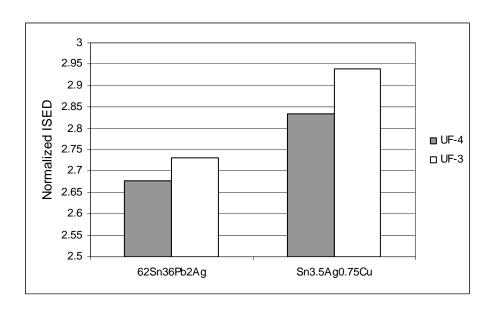


Figure 7.30 Normalized ISED for UF-4 (4 mils) and UF-3 (3 mils) underfill material with high and mid gap height solder bumps respectively

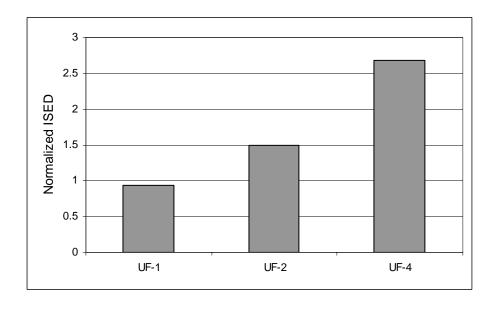


Figure 7.31 Normalized ISED for high gap height 4 mils eutectic solder bump with different underfill materials

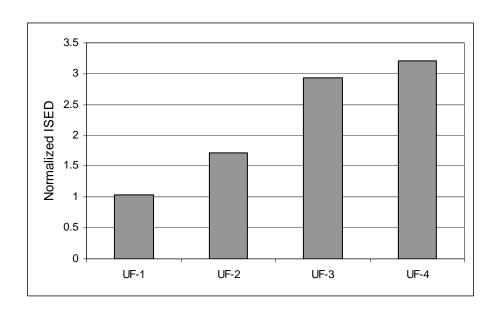


Figure 7.32 Normalized ISED for mid gap height 3 mils lead-free solder bumps with different underfill materials

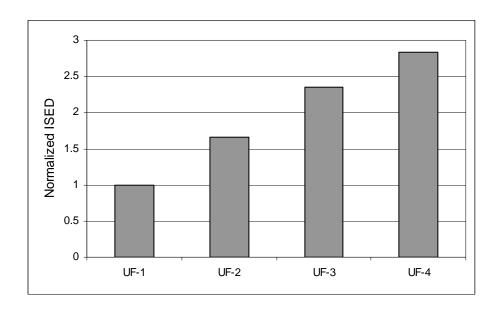


Figure 7.33 Normalized ISED for high gap height 4 mils lead-free solder bumps with different underfill materials

7.4.2.3 Effect of Bump Gap Height

It is observed from the Figure 7.34 and 7.36 that the normalized ISED is much more sensitive to bump height in case of lead-free solder bumps as compared to the eutectic solder bumps. However, the effect of bump height on the solder joint reliability for both eutectic and lead-free solder in the case of 0-90°C ATC remains the same as in case of 0-70°C ATC. The ISED value decreases with the increase in the bump gap height.

7.4.2.4 Effect of Bump Size

The 4 mil bump exhibits higher reliability than the 3 mil bump which was also true in case of 0-70°C ATC. Also the bump with larger size will have larger crack length so it will take longer for the crack to propagate throughout the solder joint before the failure occurs. Thus both the effects will be coupled and will add up to the solder joint reliability. The effect of bump size on the normalized ISED of the solder joint is shown in the Figure 7.36.

7.4.2.5 Summary

- For 0-70°C ATC the eutectic solders had higher ISED as compared to the leadfree solder, but in the case of 0-90°C ATC a reversal in the trend has been observed. The lead-free solder has higher ISED as compared to the eutectic solder.
- Decrease in gap height increases the ISED and this has greater impact on the leadfree solders for both capillary flow and re-flow underfill materils.
- Increase in the bump size reduces the ISED.

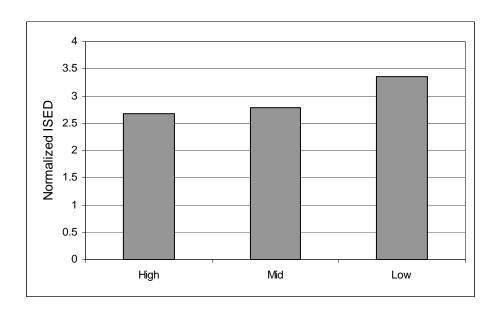


Figure 7.34 Normalized ISED for 4 mils eutectic solder bumps with UF-4 underfill material and different gap heights

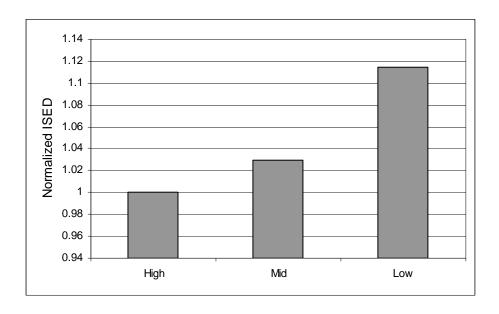


Figure 7.35 Normalized ISED for 4 mils lead-free solder bumps with UF-1 underfill material and different gap heights

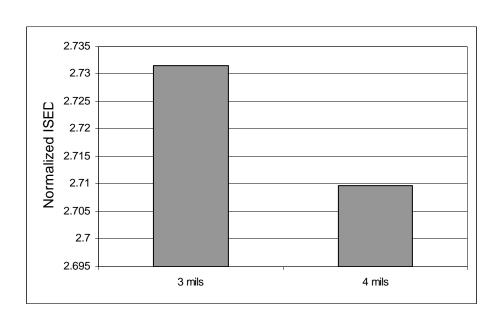


Figure 7.36 Normalized ISED for mid gap height eutectic solder bumps with UF-3 underfill with different bump diameter

7.4.3 Effect of Tg (glass transition temperature) of the Underfill Material

Material properties like CTE and elastic modulus change drastically once the working temperature of the material rises beyond the Tg of that material. The material properties of the underfill have a very significant impact on the solder joint reliability, thus it is advisable to use the underfill material which has Tg above the working temperature of the component. UF-4 has a Tg in the range of 70-75°C therefore simulations for special test cases of the UF-4 with modified properties were run in order to understand the effect of Tg on the solder joint reliability.

Four different material models listed in the Table 7.10 have been considered for the analysis. The material model D represents the actual behavior of the UF-4 underfill. Model C represents the behavior of UF-4 in case the Tg of UF-4 is above 90°C. The results from the simulation are listed in the Table 7.9, which shows that the ISED value for the UF-4 reduces to 0.18X if the Tg of the UF-4 material is above 90°C for the 0-90°ATC. The simulation run for the various temperature ranges show that there is drastic increase in the ISED once the operating temperature goes above the Tg range. The increase of the maximum temperature from 70°C to 75°C leads to a increase in the ISED value by 5.4X.

Table 7.9 Simulation results for the analysis of the effect of Tg on solder joint reliability

Temp	Material	Normalized
Cycle	Model	ISED
0-90°C	A	206.63
0-90°C	В	64.4
0-90°C	C	51.85
0-70°C	D	33.65
0-75°C	D	182.02
0-80°C	D	191.75
0-85°C	D	257.49
0-90°C	D	289.72

Table 7.10 Material model data used for simulation

	1	4	В		С		D	
Temp	CTE	Е	CTE	E (Gpa)	CTE	E (Gpa)	CTE	Е
(°C)	(ppm)	(Gpa)	(ppm)		(ppm)		(ppm)	(Gpa)
25	67	3.1	67	3.1	67	3.1	67	3.1
50	67	3.1	67	3.1	67	3.1	67	3.1
70	67	3.1	67	3.1	67	3.1	67	3.1
75	281	3.1	100	3.1	67	3.1	281	0.74
80	281	3.1	100	3.1	67	3.1	281	0.74
90	281	3.1	100	3.1	67	3.1	281	0.74

7.4.4 Field Profiles

Three different field profiles acquired by the hard drive manufacturer for different field applications were used for the simulation and the analysis of solder joint reliability. Simulations were run with all the three field profiles. Again the ISED has been used as the index of the damage for comparison for relative solder joint reliability comparison.

7.4.4.1 Profile 1

Profile 1 is an averaged thermal duty cycle for 4 hrs of writing and 30 minutes of reading. The temperature profile shown in the Figure 7.37 has been simulated for the analysis. This thermal cycle has a 4 hour dwell at the high temperature of 87°C and two quick ramp-up of 1sec from 63°C to 87°C and 2 seconds from 87°C to 63°C and has a slow ramp of 30 minutes from 63°C to 58°C. Since the UF-4 material has Tg in the range of 70-75°C which is below the operating range of the field profile so for the configurations with UF-4 underfill material test cases were run with the actual material model i.e. Tg in the range of 70-75°C and the ideal case with Tg above the operating range. The values in the parenthesis in the results table are for the ideal test case, in which the Tg of the UF-4 is considered to be above the operating range of 87°C. The simulation result for the profile-1 for all the 18 configurations has been listed in the Table 7.11.

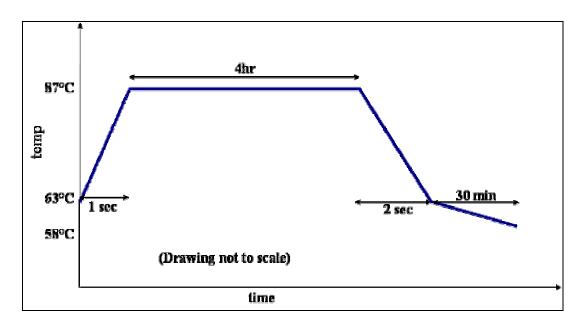


Figure 7.37 Temperature profile of the averaged thermal duty cycle 1

Table 7.11 Simulation results for field profile 1

Test Case	Solder Composition	Underfill	Bump Gap Ht.	Bump Size (mils)	Normalized Inelastic Strain Energy Density per Cycle
1	62Sn36Pb2Ag	UF-4	Low	4	434.6 (13.5)
2	62Sn36Pb2Ag	UF-1	High	4	3.89
3	62Sn36Pb2Ag	UF-4	High	4	345.28 (11.12)
4	62Sn36Pb2Ag	UF-4	Mid	4	360.98 (11.7)
5	62Sn36Pb2Ag	UF-1	Low	4	4.59
6	62Sn36Pb2Ag	UF-3	Mid	4	11.19
7	62Sn36Pb2Ag	UF-2	High	4	6.87
8	62Sn36Pb2Ag	UF-2	Mid	3	7.10
9	62Sn36Pb2Ag	UF-3	Mid	3	11.37
10	Sn3.5Ag0.75Cu	UF-2	High	4	3.47
11	Sn3.5Ag0.75Cu	UF-2	Mid	3	3.99
12	Sn3.5Ag0.75Cu	UF-4	High	4	332.39 (6.52)
13	Sn3.5Ag0.75Cu	UF-4	Mid	3	352.32 (8.22)
14	Sn3.5Ag0.75Cu	UF-3	High	4	5.90
15	Sn3.5Ag0.75Cu	UF-3	Mid	3	7.38
16	Sn3.5Ag0.75Cu	UF-1	Low	4	1.98
17	Sn3.5Ag0.75Cu	UF-1	Mid	4	1.90
18	Sn3.5Ag0.75Cu	UF-1	High	4	1.89

7.4.4.2 Profile 2

Profile 2 is an averaged thermal duty cycle for 10 minutes of writing, 2 minutes of reading and 8 minutes of rest. The temperature profile shown in the Figure 7.38 has been simulated for the analysis. This thermal cycle has a 10 minute dwell at the high temperature of 82°C, 2 minute dwell at 58°C and 8 minute dwell at 50°C with ramp time of 1 seconds from each dwell temperature to the next dwell temperature. The temperature profile shown in the Figure 7.38 has been simulated for the analysis and the simulation result for this profile is listed in Table 7.12.

7.4.4.3 Profile 3

Profile 3 is a very short time duration profile. It provides highly accelerated testing in terms of time as the number of ATC that a component undergoes while thermal cycling with Profile 3 is very high for a given period of time. The temperature profile shown in Figure 7.39 has been used for the simulation purpose. There are two dwell periods in this profile at a high temperature of 82°C and low temperature of 50°C respectively. Ramp time of 1 second has been used for going from one dwell temperature to the other. The result from the simulations run for all the 18 test cases has been listed in the Table 7.13. The normalized ISED per cycle values indicated in the parenthesis are for the ideal case of UF-4 underfill material considering that the Tg of the UF-4 is above the maximum temperature of 82°C during the thermal cycling.

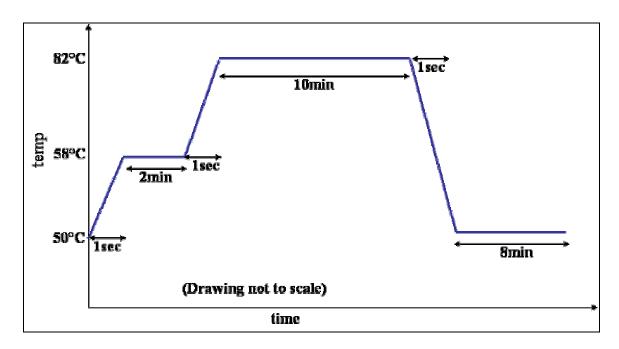


Figure 7.38 Temperature profile of the averaged thermal duty cycle 2

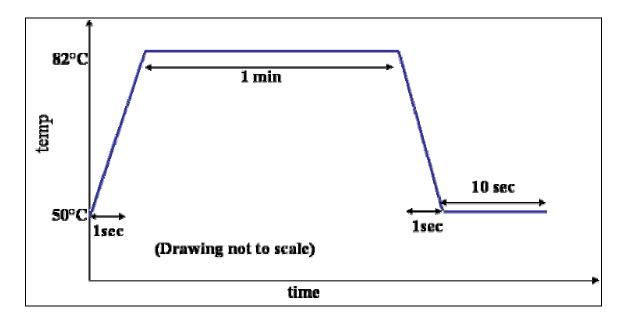


Figure 7.39 Temperature profile of the averaged thermal duty cycle 3

Table 7.12 Simulation results for the field profile 2

Test Case	Solder Composition	Underfill	Bump Gap Height	Bump Size (mils)	Normalized Inelastic Strain Energy Density per Cycle
1	62Sn36Pb2Ag	UF-4	Low	4	358.55 (13.54)
2	62Sn36Pb2Ag	UF-1	High	4	3.97
3	62Sn36Pb2Ag	UF-4	High	4	281.46 (11.72)
4	62Sn36Pb2Ag	UF-4	Mid	4	322.17 (12.17)
5	62Sn36Pb2Ag	UF-1	Low	4	4.59
6	62Sn36Pb2Ag	UF-3	Mid	4	11.43
7	62Sn36Pb2Ag	UF-2	High	4	6.52
8	62Sn36Pb2Ag	UF-2	Mid	3	6.81
9	62Sn36Pb2Ag	UF-3	Mid	3	11.94
10	Sn3.5Ag0.75Cu	UF-2	High	4	3.17
11	Sn3.5Ag0.75Cu	UF-2	Mid	3	3.67
12	Sn3.5Ag0.75Cu	UF-4	High	4	258.96 (6.83)
13	Sn3.5Ag0.75Cu	UF-4	Mid	3	311.62 (8.51)
14	Sn3.5Ag0.75Cu	UF-3	High	4	6.17
15	Sn3.5Ag0.75Cu	UF-3	Mid	3	7.64
16	Sn3.5Ag0.75Cu	UF-1	Low	4	1.59
17	Sn3.5Ag0.75Cu	UF-1	Mid	4	1.58
18	Sn3.5Ag0.75Cu	UF-1	High	4	1.57

Table 7.13 Simulation results for the field profile 3

Test Case	Solder Composition	Underfill	Bump Gap Height	Bump Size (mils)	Normalized Inelastic Strain Energy Density per Cycle
1	62Sn36Pb2Ag	UF-4	Low	4	224 (4.71)
2	62Sn36Pb2Ag	UF-1	High	4	1.23
3	62Sn36Pb2Ag	UF-4	High	4	221 (4.62)
4	62Sn36Pb2Ag	UF-4	Mid	4	223 (4.65)
5	62Sn36Pb2Ag	UF-1	Low	4	1.40
6	62Sn36Pb2Ag	UF-3	Mid	4	4.41
7	62Sn36Pb2Ag	UF-2	High	4	2.30
8	62Sn36Pb2Ag	UF-2	Mid	3	2.60
9	62Sn36Pb2Ag	UF-3	Mid	3	5.09
10	Sn3.5Ag0.75Cu	UF-2	High	4	1.12
11	Sn3.5Ag0.75Cu	UF-2	Mid	3	1.36
12	Sn3.5Ag0.75Cu	UF-4	High	4	204 (2.73)
13	Sn3.5Ag0.75Cu	UF-4	Mid	3	222 (3.63)
14	Sn3.5Ag0.75Cu	UF-3	High	4	2.63
15	Sn3.5Ag0.75Cu	UF-3	Mid	3	3.45
16	Sn3.5Ag0.75Cu	UF-1	Low	4	0.64
17	Sn3.5Ag0.75Cu	UF-1	Mid	4	0.58
18	Sn3.5Ag0.75Cu	UF-1	High	4	0.58

7.4.4.4 Relative Damage Index

Relative damage index gives the indication of the comparative damage inflicted per cycle on the solder joint by the three different field profiles. The Figures 7.41 to 7.44 show the plot of the relative damage index for the three field profiles for different configurations of the flip-chip. It is observed that for most of the configurations the damage done by the filed profile 1 is the highest and the damage done by the profile 3 is the lowest. The reason behind this being the difference in the dwell period among the profiles. Profile 1 has the maximum dwell period as compared to the other two profiles. Since the solder joint creeps during the dwell period which results in the accumulation of the non-linear plastic work, thus the ISED accumulated by the solder joint due to the profile 1 is maximum. This means that the profile 1 will have the highest acceleration factor in terms of life in cycles, however this does not mean that the profile 1 will have the highest acceleration factor in terms of the time.

The life prediction in the section 5 shows that the solder joint life in terms of time is lowest for the profile 3. In spite of the lowest damage index value of the profile 3 it accumulates highest damage in terms of time because the ISED accumulates itself in the solder joint after every consequent cycle and since the cycle time for profile 3 (1 min 12 secs) is minimum as compared to the profile 1 (4 hrs 30 mins 3 secs) and profile 2 (20mins 3 secs) so the component is subjected to much higher number of cycles in case of profile 3 as compared to the other two profiles. This results in accumulation of higher amount of ISED in case of profile 3 for the same period of time, which means that the components would take more number of cycles to fail when subjected to profile 3 but still in terms of time the profile 3 will cause failures much earlier than the other 2 profiles.

Table 7.14 Simulations results for evaluation of relative damage index of the three field profiles provided by the vendor

Underfill	Solder	Solder Bump Size		nailzed Inc Energy I (psi)	Tg effect	
		(mils)	Profile Profile Profile 1 2 3			
UF-2	Sn3.5Ag0.75Cu	4	2.70	2.61	1.00	
UF-3	Sn3.5Ag0.75Cu	4	4.61	4.73	2.24	
UF-4	Sn3.5Ag0.75Cu	4	5.13	5.23	2.32	$Tg > 87^{\circ}C$
UF-4	Sn3.5Ag0.75Cu	4	213.36	188.13	157.31	$Tg = 70-75^{\circ}C$

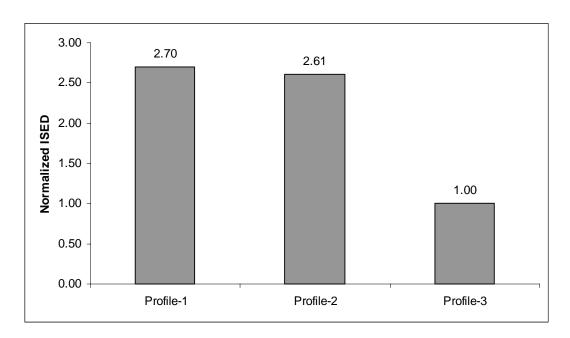


Figure 7.40 Relative damage index of the three field profiles for the lead-free solder bumps with high gap height, bump size 4 mils and UF-2 capillary flow encapsulant

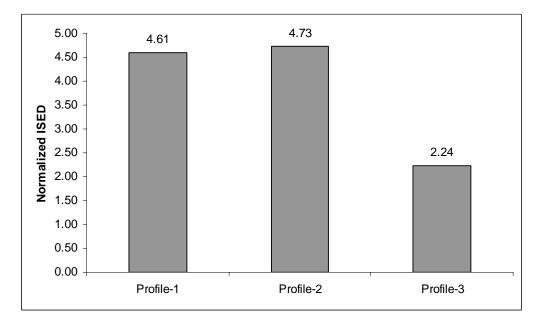


Figure 7.41 Relative damage index of the three field profiles for the lead-free solder bumps with high gap height, bump size 4 mils and UF-3 re-flow encapsulant

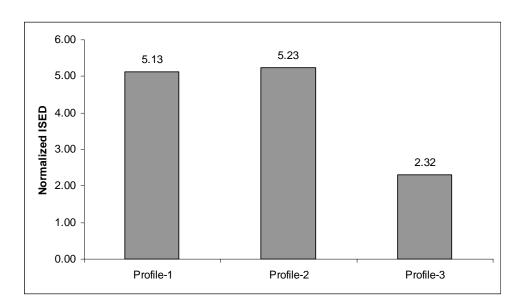


Figure 7.42 Relative damage index of the three field profiles for the lead-free solder bumps with high gap height, bump size 4 mils and UF-4 re-flow encapsulant with Tg assumed to be above 87°C

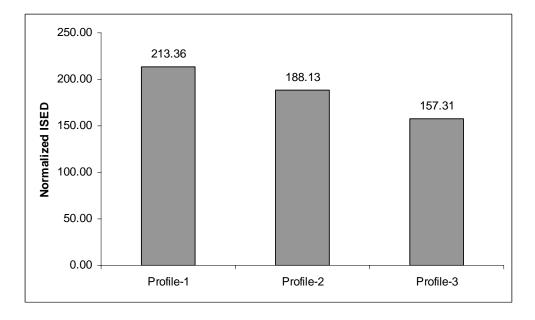


Figure 7.43 Relative damage index of the three field profiles for the lead-free solder bumps with high gap height, bump size 4 mils and UF-4 re-flow encapsulant with Tg assumed to be in the range of 70-75°C

7.5. Life Prediction and Field Life Correlation with ATC Life

Life prediction is a very essential part of the product design and manufacturing for the upfront reliability assessment in order to manufacture robust assemblies that will meet product life requirements. Modeling and ATC tests are employed for this purpose. Finite element modeling and analysis has been used in the current work in order to analyze the solder joint reliability and copper trace integrity.

7.5.1 Theory

Development of life prediction modeling involves several steps as mentioned below:

- Determination of accurate thermal cycle (ATC) in order to simulate the field condition and same failure mechanism as encountered in the field. Energy partitioning method has been used in the FEA for the determination of the correct ATC.
- Acquisition of actual test data on the components subjected to ATC with the
 various failure mechanisms encountered. Actual test failure data provided by the
 Vendor has been used to determine the constants and the scaling factors for the
 life prediction.
- Constitutive equations and, material properties for the applicable range of stressstrain conditions. Constitutive equations from the published literature and the material properties measured at Auburn University has been used in the present study.

- Simulations for calculating the ISED for the life prediction of the solder joints has been done in ANSYSTM using a 3-D diagonal slice model as described in section
 2.
- Development of the correlation between the damage parameter and life of the package.
- Determination of correct acceleration factor correlating the field life to the ATC life. Mapping based on the statistical analysis has been used in order to determine the correct acceleration factors.

7.5.2 Energy Partitioning Methodology

Determination of accurate ATC and correct acceleration factor for the experimental testing for the thermo-mechanical reliability assessment of the electronic package is extremely important. The flow chart in the Figure 7.44 describes the methodology used for the energy partitioning for determination of correct ATC. Different ATCs induce different failure modes in the component, it is extremely critical to match failure mode induced in the ATC to the failure mode encountered in the field application for the accurate life prediction. In case the failure mode induced in the ATC is different than the one encountered in the field application, then there is no way to predict actual life of the component based on the ATC testing and it's not possible to establish a correlation between the field life and the life of the component subjected to ATC. The damage or the strain energy accumulated in the solder joint during it's life which causes it to crack and finally fail can be divided into two portions, one due to the

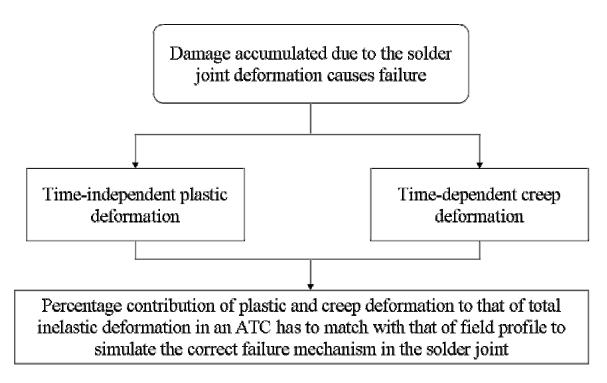


Figure 7.44 Energy partitioning methodology flowchart

time independent plastic deformation and the second due to the time dependent creep deformation.

The philosophy behind the application of energy partitioning methodology for development of field life correlation and solder joint life prediction is that in order to induce the same failure mode in the ATC as encountered in the field, the ratio of the ISED accumulated due to both time dependent plastic and time independent creep deformation has to remain the same. The energy partitioning methodology allows to separate the contribution of both the factors, thus enabling the user to determine the ratio of both the contributions towards the total ISED. Thus by matching the ratio one can determine the correct ATC for the accelerated testing of a component.

In order to separate the effect of plastic and creep deformation, a separate creep model and plasticity model have to be used in ANSYSTM instead of the Anand's viscoplasticity model. Anand's model combines both the effects in form of evolution and flow equations, preventing the user from separating the two effects.

<u>Time Dependent Creep Model</u> The Garofalo's equation (7.1) has been used as a constitutive model for the solder in the simulation for representing the time dependent creep.

$$\dot{\varepsilon} = A[\sinh(\alpha\sigma)]^n \exp\left(\frac{-Q}{RT}\right)$$
 (7.1)

The constants in the Garofalo equation used for both the 62Sn36Pb2Ag solder and the lead-free solder (Sn3.5Ag0.75Cu) have been listed in the Table 7.15.

Time Independent Plasticity Model The time independent plasiticity of the solder joint has been modeled in ANSYSTM using the linear and non-linear MISO (multilinear isotropic hardening) option. The MISO option is preferred for the large strain cycling. The MISO option allows user to specify up to 20 temperature-dependent stress-strain curves. The uniaxial behavior is described by a piece-wise linear total stress-total strain curve, starting at the origin, with positive stress and strain values. The curve has to be continuous from the origin through 100 (max) stress-strain points. The slope of the first segment of the curve must correspond to the elastic modulus of the material and no segment slope should be larger. No segment can have a slope less than zero. The data collected from the uniaxial tensile test conducted at Auburn University has been used for modeling both the linear elastic and multilinear isotropic hardening. Figure 7.45 shows the linear elastic modulus used for the simulation in ANSYSTM.

The MISO data for the eutectic solder has been input for the three different temperatures, T1= -25°C, T2= 25°C and T3= 85°C. The plot of the stress-strain data input in the ANSYSTM for the three temperatures has been shown in the Figure 7.46.

Temperature dependent non-linear elastic modulus has been used for the lead-free solder material, Figure 7.47 shows the plot of the elastic modulus data input in the ANSYSTM for the simulation. The MISO data for the lead-free solder has been input for the five different temperatures, T1= 0°C, T2= 25°C, T3= 50°C, T4= 75°C and T5= 100°C. The plot of the stress-strain data input in the ANSYSTM for all the five temperatures has been shown in the Figure 7.48.

Table 7.15 Constants used for the time dependent creep model of the solder

Solder Alloy	A	α	n	Q
62Sn36Pb2Ag [Zahn 2003]	10	0.001379	2.0	5401.2
Lead-free [Wiese, et al. 2001]	277984	1.688E-4	6.41	6500.0

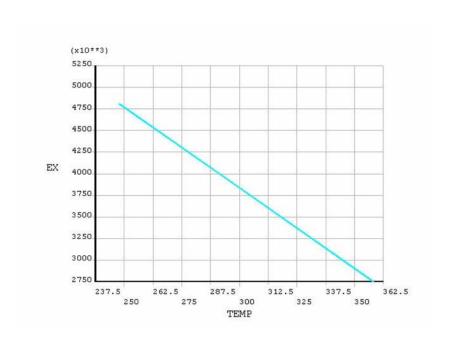


Figure 7.45 Temperature dependent linear elastic modulus of the eutetctic solder material

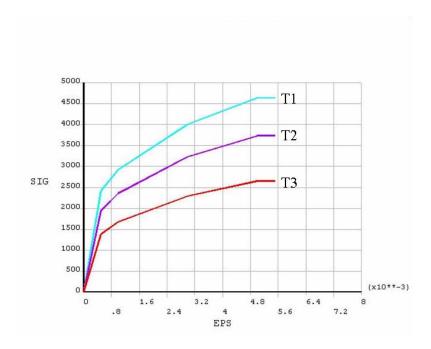


Figure 7.46 Temperature dependent stress-strain data for modeling multilinear isotropic hardening of the 62Sn36Pb2Ag solder material

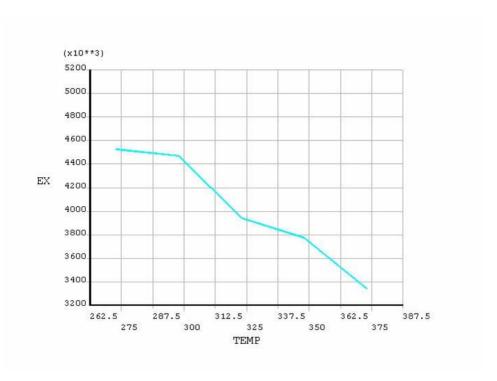


Figure 7.47 Temperature dependent linear elastic modulus of the lead-free solder material

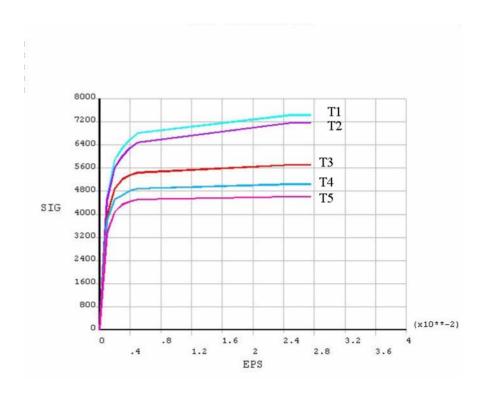


Figure 7.48 Temperature dependent stress-strain data for modeling multilinear isotropic hardening of the lead-free solder material

7.5.2.1 Hysteresis Loop

The shear stress-strain data from the simulation has been plotted to analyze the hysteresis loops for solder joint with both the capillary flow and re-flow encapsulants, when subjected to the three field profiles. The hysteresis loop shows the amount of the non-linear plastic work accumulated by the solder joint during the thermal cycle. The ISED accumulated by the solder joint during the thermal cycle is given by the area enclosed within the hysteresis loop for that cycle. Hysteresis loop also shows the manner in which the solder joint behaves when subjected to the thermal cycle. The vertical line region in the hysteresis loop shows the stress relaxation taking place during the dwell periods of the cycle. This is the region where the creep takes place within the solder joint. The region of horizontal or the inclined line shows the plastic deformation happening during the ramps.

The stress-strain data during the thermal cycling of the flip-chip has been taken from the simulation run in ANSYSTM. The top left corner element with the maximum strain has been used for the output of the stress-strain data. Hysteresis loop has been plotted from this stress-strain data for all the three field profiles. Figure 7.49a, 7.50b and 7.50c shows the hysteresis loop plot for the capillary flow encapsulant subjected to field profile 1, 2 and 3 respectively. Figure 7.50a, 7.50b and 7.50c show the hysteresis loop plot in the case of re-flow encapsulant. It is visible form the hystersis loops for both the capillary flow and the re-flow underfill materials that the plastic work or the ISED accumulated per cycle in the solder joint is maximum for the profile 1 and minimum for the profile 3.

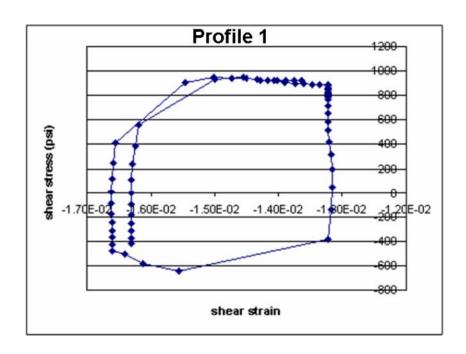


Figure 7.49a Hysteresis loop for the Sn3.5Ag0.75Cu solder bump with UF-2 capillary flow encapsulant subjected to field profile 1

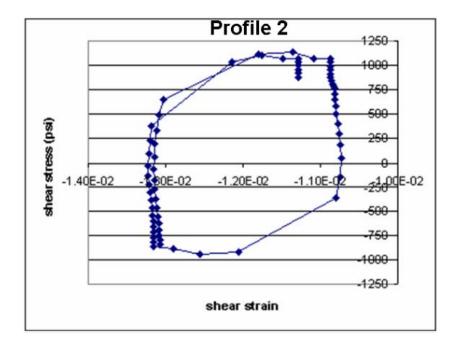


Figure 7.49b Hysteresis loop for the Sn3.5Ag0.75Cu solder bump with UF-2 capillary flow encapsulant subjected to field profile 2

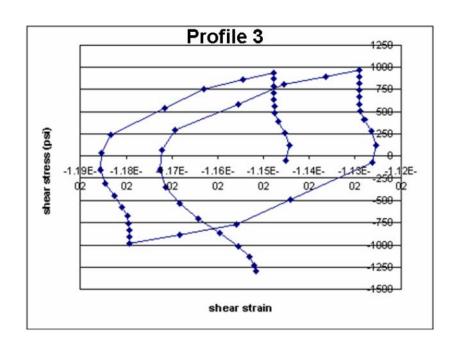


Figure 7.49c Hysteresis loop for the Sn3.5Ag0.75Cu solder bump with UF-2 capillary flow encapsulant subjected to field profile 3

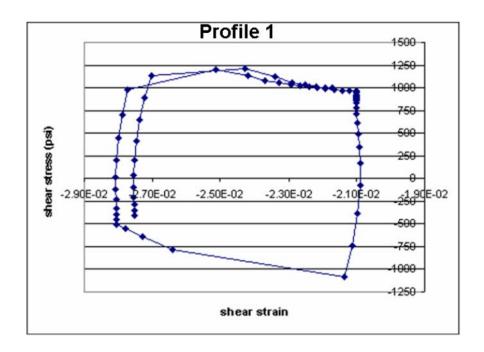


Figure 7.50a Hysteresis loop for the Sn3.5Ag0.75Cu solder bump with UF-4 reflow encapsulant subjected to field profile 1

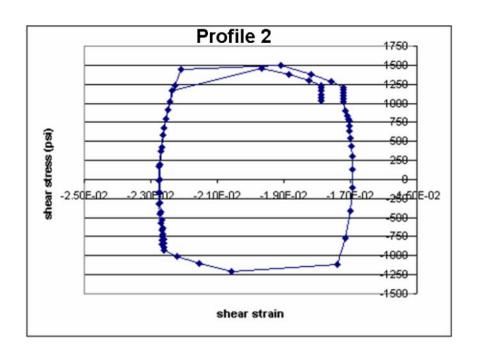


Figure 7.50b Hysteresis loop for the Sn3.5Ag0.75Cu solder bump with UF-4 reflow encapsulant subjected to field profile 2

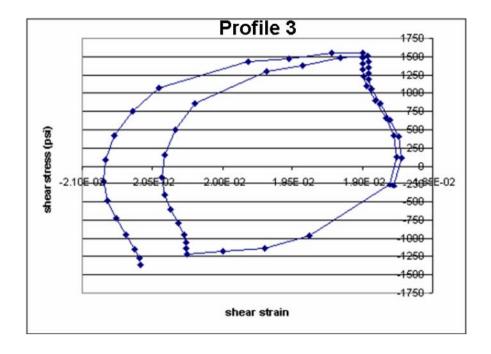


Figure 7.50c Hysteresis loop for the Sn3.5Ag0.75Cu solder bump with UF-4 reflow encapsulant subjected to field profile 3

7.5.3 Fatigue Life Prediction Models

Fatigue life prediction models, also known as the damage relationships have been used to correlate the life of the solder joint to the strain energy density or the strain (plastic, creep or total strain) accumulated during each ATC.. Several strain energy and strain based life prediction models for the eutectic solder have been used by the researchers in the past and published in the literature. The life prediction models developed for the lead-free solder are very few.

7.5.3.1 Eutectic (SnPbAg) Solder

Some of the fatigue life prediction models for eutectic solder published in the literature are listed below:

1. Engelmaier's [1983] Model based on total shear strain range

$$N_f = \frac{1}{2} \left[\frac{\Delta \gamma_T}{0.65} \right]^{-\left(\frac{1}{c}\right)}$$

Ductility exponent, $c = -0.442 - 6 \times 10 - 4 \text{(Tmean)} + 1.72 \times 10 - 2 \text{Ln}(1+v)$

where, Tmean is the mean temperature and v is the cycling frequency

2. Solomon's [1986] low cycle fatigue model based on plastic shear strain range

$$N_p = \left[\frac{1.36}{\Delta \gamma_p}\right]^{\left(\frac{1}{0.5}\right)}$$

3. Knecht and Fox's [1991]model based on creep shear strain range

$$N_c = \frac{8.9}{\Delta \gamma_c}$$

Pang's [1997] model based on Miner's superposition rule of creep-fatigue 4. interaction

$$N_T = \left[\left(\frac{1}{N_c} \right) + \left(\frac{1}{N_p} \right) \right]^{-1}$$

5. Morrow's energy based fatigue model modified by Spraul, et al. [2004]

$$N_f = C_1 (\Delta W)^{c_2}$$

where,
$$C_1 = 537.15$$
, $C_2 = -1.0722$

Shi et al's [2000] frequency modified model based on total strain range 6.

$$N_f v^{(h-1)} = \left[\frac{C}{\Delta \varepsilon_t}\right]^{\left(\frac{1}{m}\right)}$$

where,

$$m = 0.731 - (1.63 \times 10 - 4)T + (1.392 \times 10 - 6)T2 - (1.15 \times 10 - 8)T3$$

$$C = 2.122 - (3.57 \times 10 - 3)T + (1.329 \times 10 - 5)T2 - (2.502 \times 10 - 7)T3$$

$$h = 0.919 - (1.765 \times 10 - 4)T - (8.634 \times 10 - 7)T2$$

$$v = 0.0139$$

7. Shi et al's [1999] frequency modified model based on Morrow's energy model

$$N_f v^{(h-1)} = \left[\frac{C\Delta\sigma}{\Delta W}\right]^{\left(\frac{1}{m}\right)}$$

where,
$$m = 0.7$$
, $C = 1.69$, $h = 0.9$

$$C = 1.69$$
.

$$h = 0.9$$

8. Darveaux's [2000] energy based model with CAVE modified constants

$$N_e = N_0 + \frac{a}{da/dN}$$

where,

'a' is the joint diameter at the interface

$$N_0 = K_1(\Delta W)^{K_2}$$
 is the number of cycles for crack initiation

$$\frac{da}{dN} = K_3 (\Delta W)^{K_4}$$
 is the crack propagation rate

The value of the constants K_1 , K_2 , K_3 and K_4 used for calculation of characteristic life cycles are given in Table 7.16.

7.5.3.2 Lead-free (SnAgCu) Solder

Some of the fatigue life prediction models for lead-free solder published in the literature are listed below:

1. Shi et al's [2000] frequency modified Coffin-Manson model based on total strain range fitted by Pang [2004]

$$N_f v^{(h-1)} = \left[\frac{C}{\Delta \varepsilon_t}\right]^{\left(\frac{1}{m}\right)}$$

where,
$$m = 0.93$$
, $C = 12.9$, $h = 0.95$,

2. Shi et al's [1999] frequency modified model based on Morrow's energy model fitted by Pang [2004]

$$N_f v^{(h-1)} = \left[\frac{C}{\Delta W} \right]^{\left(\frac{1}{m}\right)}$$

where,
$$m = 0.877$$
, $C = 1487.3$, $h = 0.82$

3. Morrow's energy based fatigue model fitted by Lau et al. [2004]

$$N_f = C_1 (\Delta W)^{c_2}$$

where,
$$C_1 = 18.15$$
, $C_2 = -1.96$

Table 7.16 Constants for the damage relationship

	K_1	K_2	K ₃	K_4
	(cycles/psi ^K ₂)		(in/cycle/psi ^K ₄)	
Lall, et al. [2004]	28769	-1.53	6x10 ⁻⁷	0.7684
Darveaux [2000]	48300	-1.64	3.8x10 ⁻⁷	1.04

7.5.4 Field Profile Based Fatigue Life Prediction

Solder joint fatigue life prediction for all the eighteen configurations for the three different field profiles provided by the vendor has been done. The experimental failure data for the Profile 3 provided by the vendor (Table 7.17) has been used for the Weibull plot and calculation of constants and scaling factors for the fatigue life prediction for all the three profiles. UF-4L and UF-4H is for the re-flow (UF-4) encapsulant with low and high gap height respectively. VAR1 and VAR2 indicate UF-4 underfill material with different size of filler material. The solder joint fatigue life prediction for the test cases with eutectic bumps has been done using both Darveaux's model modified with CAVE constants as well as Morrow's model. In case of lead-free alloy predictions using only Morrow's model has been presented.

7.5.4.1 Profile-1

Table 7.18 lists the predicted life from the simulation results for all the 18 test cases subjected to profile-1.

7.5.4.2 Profile-2

The solder joint fatigue life prediction from the simulation, for the 18 test cases when subjected to field profile 2 has been listed in Table 7.19.

7.5.4.3 Profile-3

Life prediction in the case of field profile 3 has been listed in Table 7.20.

Table 7.17 Failure data for profile 3 provided by the vendor

Test Case	No. of Failures	Total Units in Test	Characterstic Life (Hrs)	Characterstic Life (Cycles)
UF-1	0	8	-	-
UF-2	0	8	-	-
UF-4L	6	6	790	39500
UF-4H	5	5	675	33750
VAR1	8	8	249	12450
VAR2	8	8	441	22050

Table 7.18 Predicted life for all 18 test cases for field profile 1

Test Case	Scaled Fatigue Life Based on Darveaux's Model with CAVE Constants		Scaled Fatigue Life Based on Morrow's Model	
	cycles hours		cycles	hours
1	2036	9163	1620	7288
2	120915	544117	254340	1144528
3	2416	10874	2073	9327
4	2337	10519	1976	8893
5	101148	455168	212992	958462
6	41001	184507	81922	368651
7	66415	298870	138221	621993
8	54934	247206	133425	600415
9	33741	151838	80533	362397
10			124250	559125
11			109929	494680
12			2273	10230
13			2160	9721
14			78006	351027
15			64103	288464
16			203231	914539
17			210716	948223
18			211694	952622

Table 7.19 Predicted life for all 18 test cases for field profile 2

Test Case	Scaled Fatigue Life Based on Darveaux's Model with CAVE Constants		Scaled Fatigue Life Based on Morrow's Model	
	cycles hours		cycles	hours
1	2036	11748	3916	9953
2	120915	591334	197111	1244242
3	2416	14082	4694	12902
4	2337	12725	4242	11162
5	101148	505743	168581	1064958
6	41001	200879	66960	400397
7	66415	350293	116764	730957
8	54934	287174	95725	697634
9	33741	160631	53544	382088
10			672521	224174
11			591457	197152
12			14149	4716
13			12029	4010
14			375020	125007
15			310930	103643
16			1231714	410571
17			1238548	412849
18			1245464	415155

Table 7.20 Predicted life for all 18 test cases for field profile 3

Test Case	Scaled Fatigue Life Based on Darveaux's Model with CAVE Constants		Scaled Fatigue Life Based on Morrow's Model	
	cycles hours		cycles	hours
1	33458	669 (790)	33266	665 (790)
2	4588994	91780	8821451	176429
3	33778	676 (675)	33716	674 (675)
4	33572	671	33426	669
5	3920391	78408	7678171	153563
6	1055782	21116	2243723	44874
7	2180067	43601	4509119	90182
8	1703533	34071	3953683	79074
9	788387	15768	1923949	38479
10			3349661	66993
11			2825215	56504
12			34945	699
13			32334	647
14			1584396	31688
15			1248814	24976
16			5471989	109440
17			5965388	119308
18			5965388	119308

7.6 Copper Trace Integrity

Copper trace failure mode is another critical failure mode in the flip-chip devices and other electronic packages. Since the copper trace has negligible effect on the solder joint reliability so the copper trace was ignored in the solder joint integrity analysis.

7.6.1 Model Description

A copper trace of 0.7mils thick and 2 mils wide has been added to the 3-D diagonal slice model. Four models with low gap height bump and 4 mils pad have been generated for all the four different underfill materials for the copper trace integrity analysis. For the simplicity of the model the underfill fillet was initially not considered in the model (Figure 7.51). Later an underfill fillet (Figure 7.52) was also added for the accuracy of the result.

7.6.2 Von-Mises Stress Comparison for Different Underfill Materials

The Von Mises stress contour plot (Figure 7.53) in the case of the model without underfill fillet shows the stress concentration in the copper trace in the region outside the underfill away from the die edge. The actual copper trace failure however occurs at the die edge just below the underfill fillet. Since the FEA without the underfill fillet was not able to simulate the actual failure thus the model was recreated with an underfill fillet for the better results.

Simulation with the underfill fillet showed the high stress region below the underfill fillet, which is also the location of failure in field and experimental testing. This generates the confidence in model. The values of maximum Von Mises stress from the

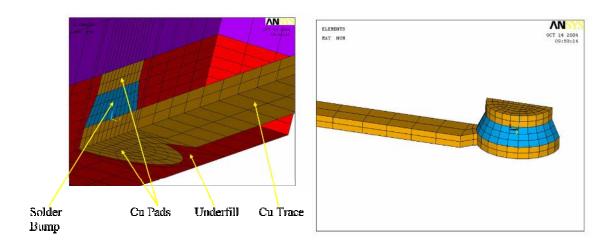


Figure 7.51 Close-up view of the flip-chip model with the copper trace, without underfill fillet

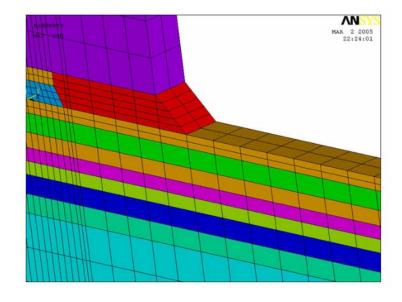


Figure 7.52 Close-up view of the flip-chip model with the copper trace with underfill fillet

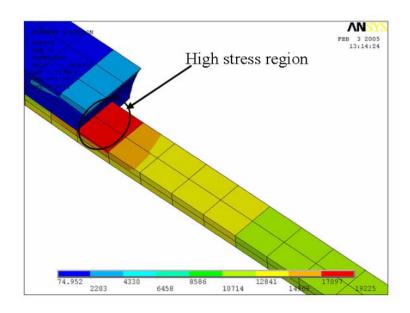


Figure 7.53 Von Mises stress contour plot of the copper trace without underfill fillet

Table 7.21 Maximum Von Mises stress from the model with fillet and without fillet

Underfill	Max Stress (Psi)		
Material	Von Mises		
	with fillet	w/o fillet	
UF-1	35821	40057	
UF-2	35577	38073	
UF-3	34092	34604	
UF-4	34344	34945	

simulation run without fillet is higher by approximately 10% than the values of the model with fillet.

Figure 7.54 and 7.57 show the stress contour plots for the models with fillet for 0-70°C ATC, it is visible form the plots that the high stress region occurs just below the underfill fillet in all the cases. Von Mises stress has been used for the plots and the comparison of stresses because Von Mises stress is the failure criterion for the failure of ductile materials under fatigue

In all 16 simulations have been run for two different ATC profiles for all the four underfill materials with eutectic as well as lead-free solder bumps. The results have been listed in Table 7.22 The results indicate that there is hardly any difference in the value of max. stress of the copper trace between the eutectic and the corresponding lead-free cases, the stresses for lead-free being slightly higher than the eutectic cases.

The ultimate tensile strength of oxygen free electronic copper is in the range of 32054 to 65993 psi and the tensile yield strength is in the range of 10008 to 52940 psi. Thus the copper trace failure is predicted for all the test cases in case of the -55 to 125°C ATC but it may not fail when the flip-chip is subjected to 0-70°C ATC.

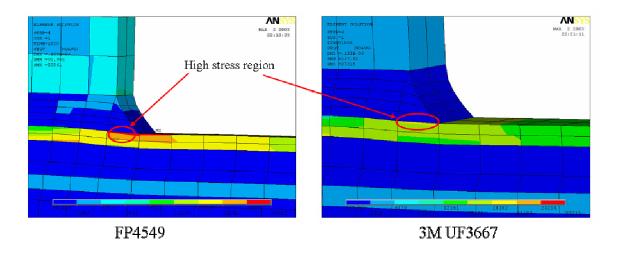


Figure 7.54 Stress distribution contour plot for UF-2 (capillary flow) and UF-3 (re-flow) underfill

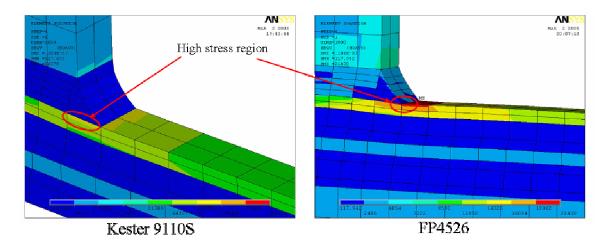


Figure 7.55 Stress distribution contour plot for UF-4 (re-flow) and UF-1 (capillary) underfill

Table 7.22 Simulation results for two different ATCs

Underfill Material	Max Stress (Psi) Von Mises		Max Stress (Psi) Von Mises	
	0-70°C		-55 to	125°C
	Eutectic	Lead-free	Eutectic	Lead-free
UF-1	35821	35802	85718	85626
UF-2	35577	35575	83444	83372
UF-3	34092	34166	67691	68195
UF-4	34344	34396	65031	65594

7.7 Summary and Recommendations

This section gives a briefing on the methodology of using the life prediction models and life prediction calculation for the solder joint reliability. Recommendations on the selection of the accelerated test methodologies is also provided at the end of the section. The solder joint life acceleration factors depend on various parameters:

- The ATC (accelerated thermal cycle) selected for the field life prediction.
- The field profile for which the life is to be predicted.
- Material, geometry and assembly parameters.
- Duty cycle in terms of average number of field cycles that the component is subjected to during it's application on a per day basis.

These factors have to be kept in the mind while performing any life prediction calculations. One has to be extremely careful and wise while using the modeling and simulation tools, as if not wisely used it may give the user a set of completely irrelevant results which may prove fatal in the design and selection of component instead of helping the designer.

7.7.1 Development of PCB and Drive Level Tests

Calculation of Acceleration Factors

For the simplicity of understanding the various steps involved in the solder joint life prediction calculation for a sample test case has been demonstrated for the test case-1 with field profile-3. The acceleration factor has also been calculated for the ATC 0-90°C based on the field profile-3.

Since the UF-4 material has Tg below the maximum temperature (82°C) of the profile-3 so the weighted average of the ISED has been used to calculate the scaled ISED and used for the life calculation. The weight factor (WF) of 2 and the scaling factor (SF) of 10 for the profile 3 has been used in the calculation.

SISED (
$$\Delta$$
W) = (WF)*(SF)*(ISED)
= 2*0.1*4.71
= 0.942 psi

Now from Darveaux's model modified with CAVE's constants, as mentioned in section 5.3.1

$$N_0 = K_1(\Delta W)^{K_2}$$

$$= 25768 \text{ cycles}$$

$$\frac{da}{dN} = K_3(\Delta W)^{K_4}$$

$$= 4.73E-7$$

$$N_e = N_0 + \frac{a}{da/dN}$$

$$= 34226 \text{ cycles}$$

If we assume that the flip-chip encounters 20 averaged thermal duty cycles of profile 3 per day than the field life of the component would be 1711 days or 4 yrs and 8.3 months.

Now using the same calculations with appropriate values of the constants and ISED for 0-70°C ATC, the characteristic life (N) comes out to be 8854 cycles. This means that 8854 cycles of 0-70°C test cycles correspond to 4yrs 8.3 months of drive level

field life. Since the cycle time for 0-70°C ATC is 30 mins therefore the characteristic life is 4427 hrs or 184 days.

Thus the acceleration factor (AF) for $0-70^{\circ}$ PCCA level test cycle w.r.t. drive level field profile 3 is 9.3X (AF = 1711 / 184) in terms of time. Similarly the calculations can be done for any drive level profile and PCB level accelerated test using any of the life prediction models for which the results are presented in section 5.4.

7.7.2 Recommendations for the PCB Level Accelerated Test

The following recommendations can be made for the accelerated test methodologies at the PCB level to predict solder joint reliability based on the finite element analysis.

- Before selecting the accelerated test cycle for the thermo-mechanical testing of the component it is extremely critical to make sure that the failure mode and the mechanism in the ATC testing remains identical as failure mode and mechanism encountered in the field application.
- In the present study it is observed that for the UF-4 underfill material the ISED accumulated in the solder joint increases drastically for the thermal cycles having maximum temperature above the Tg (70-75°C).
- It is extremely important to check the maximum temperature encountered by the solder joint in the field application and select a underfill material which has Tg above the maximum field temperature.
- The ATC should also be selected so that the maximum temperature in the test cycle is not above the Tg of the underfill material.

• 0-70°C ATC is recommended for the comprehensive accelerated testing of the flip chip with all the underfill materials. The solder joint failure for the 0-70°C test cycle remains independent of the Tg of the underfill material for all the capillary flow and re-flow underfills. However 0-90°C ATC can be used for the testing of flip-chips with the capillary flow underfills.

7.7.3 Recommendations for the Drive Level Stress Test

Three drive-level test profiles (Profile 1, Profile 2, Profile 3) provided by the vendor as shown in Figures 7.38, 7.39, 7.40, have been investigated in this study. The hysteresis loops and energy partitioning in the profiles was investigated (Figures 7.50, 7.51). Model predictions indicate that significant plastic work per cycle can be obtained by using a much accelerated profile 3. It is hypothesized that, a large portion of the plastic work is accumulated during the ramps, enabling compression of time during the accelerated test. Therefore, profile 3 is recommended over profiles 1 and 2.

In general, the high temperature for profile 3, which is presently at 82°C, should be lower than the glass transition temperature for the underfill. In the current study the Tg for UF-1, UF-2, and UF-3 is above 82°C, but not for the UF-4 underfill. Due to this it is recommended that the high temperature should be reduced to 70°C as the Tg of UF-4 is in the range of 70°C-75°C. This may not be a concern, if the UF-4 material is improved such that the glass transition temperature becomes significantly higher than 82°C.

CHAPTER 8

SUMMARY AND CONCLUSIONS

In this work, the decision-support models for deployment of area array devices under various harsh thermal environments have been formulated. The devices for which the decision-support models can be used include both flip chip and flex substrate ball grid array packages. Separate set of models have been formulated for the BGA packages and flip-chip packages. The sensitivities of reliability to design, material, architecture and environment parameters have been developed and validated with the experimental data. The model predictions for various parametric variations show the similar trends in the effect on the reliability of the packages of various configurations. The sensitivities developed in this paper can be used to analyze quantitatively the impact of various design parameters on the reliability of area array packages in harsh environments.

Hybrid modeling methodology presented in this paper provides a technique to perturb accelerated test data and evaluate trade-offs. The methodology developed in this work provides an extremely cost effective and time effective solution for doing trade-offs and the thermo-mechanical reliability assessment of the area array devices subjected to extreme environments. Thus, providing a turn key approach, for making trade-offs between geometry and materials and quantitatively evaluating the impact on reliability. Accuracy greater than normally achieved by 1st order models has been demonstrated. Convergence between the experimental, statistical and failure mechanics based model

results validates the application of these models to compare the reliability of the different area array packages with various parametric variations.

The broad conclusions that can be drawn from the present analysis of BGA packages are:

- The reliability of the BGA package is highly sensitive to the die-to-body ratio
 (also known as package density) and the life of the package decreases with the
 increase in the die-to-body ratio.
- The thermo-mechanical reliability increases with the increase in the ball count (number of I/Os).
- Solder joint diameter also has a great influence and the reliability of the package increases with the increase in the solder joint diameter.
- Increase in the PCB thickness decreases the package reliability.
- Higher encapsulant mold compound filler content in the package provides better thermo-mechanical reliability.
- NSMD pad configuration imparts higher reliability to the package as compared to the SMD pad configuration.
- Increase in the temperature range of the thermal cycle reduces the solder joint life of the package.

The conclusions from the statistics and failure mechanics based analysis of the flipchip package are as follows:

• The thermo-mechanical reliability of flip-chip devices generally decreases with the increase in the die size.

- Increase in the solder joint diameter increases the reliability of the package.
- The thermo-mechanical reliability of the package increases with the increase in the number of I/Os.
- The encapsulation of a flip-chip has a huge bearing on the reliability of the package. The encapsulated flip-chip exhibits characteristic life upto 30x to 40x as compared with the non-encapsulated flip-chip.
- Flip-chip with NSMD pad configuration exhibits better reliability as compared to the flip-chip with SMD pads.
- Increase in the temperature range of the thermal cycle reduces the solder joint life of the flip-chip.

FEA model for flip-chip solder joint reliability and copper trace integrity has been developed and presented in this work. Damage based methodology for flip-chip solder joint reliability prediction has also been presented which has been used for the development of appropriate accelerated thermal cycle for the experimental testing and developing field life correlation. Solder joint reliability analysis for both leaded (62Sn36Pb2Ag) and lead-free (95.5Sn4.0Ag0.5Cu) solder alloy has been done and presented in this work.

The finite element analysis of the flip-chip done in the current work leads to below mentioned conclusions:

For 0-70°C ATC the eutectic solders had higher inelastic strain energy (ISED) accumulation per cycle as compared to the lead-free solder, but in the case of 0-90°C ATC a reversal in the trend has been observed. The lead-free solder has higher ISED as compared to the eutectic solder.

- Decrease in gap height increases the ISED and this has greater impact on the leadfree solders for both eutectic and lead-free solders
- Increase in the bump size reduces the ISED.
- For the underfills investigated, capillary flow underfills exhibit lower ISED as compared to the reflow encapsulant for both eutectic as well as lead-free solders.
- The simulation shows that there is drastic increase in the ISED once the operating temperature goes above the Tg range of the underfill material
- The simulation for the copper trace integrity test shows that the failure mode might shift to the copper trace cracking for the -55 to 125°C ATC. This implies that -55 to 125°C ATC should be used for the accelerated testing only if the failure mode in field mode is copper trace cracking.
- The underfill fillet plays a significant role in reducing the Cu trace stresses and the effect of solder alloy used for bumping is negligible.

There is still a scope of further improvement in these models and validation with wider database of experimental results. Formulation of similar design-support models with more extensive accelerated test failure database with the methodology presented in this work is desired. The models presented in this paper should not be used for absolute solder joint life prediction, rather they should be used as a tool for educated evaluation of relative thermal reliability performance of ball grid array and flip-chip packages up-front in the design phase or during the selection of a package for specified mission requirements.

BIBLIOGRAPHY

- Adams, R. M., A. Glovatsky, T. Lindley, J. L. Evans and A. Mawer, "PBGA Reliability Study for Automotive Applications", *Proceedings of the 1998 SAE International Congress and Exposition*, Detroit, MI, pp. 11-19, February 23-26, 1998.
- Amagai, M., Watanabe, M., Omiya, M., Kishimoto, K and Shibuya, T., "Mechanical Characterization of Sn-Ag Based Lead-Free Solders", *Transactions on Microelectronics Reliability*, Vol. 42, pp. 951-966, 2002.
- Anand, L., "Constitutive Equations for Hot-Working of Metals", *International Journal of Plasticity*, Vol. 1, pp. 213-231, 1985.
- Barker, D. B., Mager, B. M. And Osterman, M. D., "Analytic Characterization of Area Array Interconnect Shear Force Bahavios", *Proceedings of ASME International Mechanical Engineering Congress and Exposition*, New Orleans, LA, pp. 1-8, November 17-22, 2002.
- Bedinger, John M., "Microwave Flip Chip and BGA Technology", *IEEE MTT-S International Microwave Symposium Digest*, v 2, pp 713-716, 2000.
- Brown, S. B., Kim, K. H. and Anand, L., "An Internal Variable Constitutive Model for Hot Working of Metals", *International Journal of Plasticity*, Vol. 5, pp. 95-130, 1989.
- Clech, Jean-Paul and Augis, J. A., "Temperature Cycling Structural Response and Lifetime Prediction of Surface Mounted Leaded Assemblies", *Proceedings of 1986 International Electronics Packaging Society Conference*, Dallas, TX, pp. 305-325, November 7-9, 1988.
- Clech, Jean-Paul, "Flip-Chip/CSP Assembly Reliability and Solder Volume Effects", *Proceedings of Surface Mount International Conference*, San Jose, CA, pp. 315-324, August 23-27, 1998.
- Clech, Jean-Paul, "Reliability Challenges and Modeling of Modern Soldered Assemblies", *Proceedings of Symposium on Design and Reliability of Solders and Solder Interconnections*, Orlando, FL, pp. 367-375, February 9-13, 1997.

- Clech, Jean-Paul, "Solder Joint Reliability of CSP Versus BGA Assemblies", *Proceedings of SMT ESS Hybrid 2000 Conference*, Nuremberg, Germany, pp. 19-28, June 27-29, 2000.
- Clech, Jean-Paul, "Solder Reliability Solutions: A PC based design-for-reliability tool", *Proceedings of Surface Mount International Conference*, San Jose, CA, pp. 136-151, Sept. 8-12, 1996.
- Clech, Jean-Paul, "Solder Reliability Solutions: From LCCCs to Area-Array Assemblies", *Proceedings of NEPCON West* '96, Anaheim, CA, pp. 1665-1680, February 1996.
- Clech, Jean-Paul, "Tools to Assess the Attachment Reliability of Modern Soldered Assemblies", *Proceedings of NEPCON West '96*, Anaheim, CA, pp.35-45, February 23-27, 1997.
- Clech, Jean-Paul, Kotlowitz, R. W., Engelmaier, W. and Augis, J. A., "Surface Mount Solder Attachment Reliability Figures of Merit Design-for-Reliability Tools", *Proceedings of Surface Mount and Related Technologies Conference*, SMART V, Technical Paper SMT V-48, New Orleans, LA, January 9-12, 1989.
- Clech, Jean-Paul, Manock, J. C., Noctor, D. M., Bader, F. E. and Augis, J. A., "A Comprehensive Surface Mount Reliability Model: Background, Validation and Applications", *Proceedings of Surface Mount International Conference*, pp. 363-375, 1993.
- Clech, Jean-Paul, Tervalon, M. J. and Augis, J. A, "Reliability Evaluation of 25-Mil and 50-Mil Pitch Surface Mounted Plastic Leaded Packages", *Proceedings of 1989 International Electronics Packaging Society Conference*, San Diego, CA, pp. 754-768, September 11-14, 1989.
- Clech, J-P., Noctor, D. M., Manock, J. C., Lynott, G. W. and Bader, F. E., "Surface Mount Assembly Failure Statistics and Failure-Free Times", *Proceedings of the 44th Electronic Components and Technology Conference*, IEEE, Washington, D. C., pp. 487-497, May 1-4, 1994.
- Coffin, L. F., "A Study of the Effects of Cyclic Thermal Stresses on a Ductile Metal", *Transactions of ASME*, Vol. 76, pp. 931-950, 1954.
- Dale, J. R. and Oldfield, R. C., "Mechanical Stresses Likely to be Encountered in the Manufacture Use of Plastically Encapsulated Devices", *Microelectronics and Reliability*, Vol. 16, pp. 255-258, 1977.
- Darveaux, R., "Effect of Simulation Methodology on Solder Joint Crack Growth Correlation," *Proceedings of the 50th Electronic Components and Technology Conference*, Las Vegas, Nevada, pp.1048-1058, May 21-24, 2000.

- Darveaux, R., "How to use Finite Element Analysis to Predict Solder Joint Fatigue Life", *Proceedings of the VIII International Congress on Experimental Mechanics*, Nashville, Tennessee, June 10-13, pp. 41-42, 1996.
- Darveaux, R., and Banerji, K., "Constitutive Relations for Tin-Based Solder Joints," *IEEE Transactions on Components, Hybrids and Manufacturing Technology*, Vol. 15, No. 6, pp. 1013-1024, 1992.
- Darveaux, R., Banerji, K., Mawer, A., and Dody, G., "Reliability of Plastic Ball Grid Array Assembly", *Ball Grid Array Technology*, J. Lau, ed., McGraw-Hill, Inc. New York, pp. 379-442, 1995.
- Darveaux, R., Heckman, J., Syed, A. and Mawer, A., "Solder Joint Fatigue Life of Fine Pitch BGAs-Impact of Design and Material Choices", *Transactions on Microelectronics Reliability*, Vol. 40, Issue 7, pp. 1117-1127, July 2000.
- Dauksher, W. and Lau, J., "Lead-Free Solder Joint Reliability of Photonic Device Under Transient and Steady State Loadings", *Proceedings of 2003 ASME International Mechanical Engineering Congress*, Washington, D. C., pp. 281-289, November 15-21, 2003.
- Doorselaer, K. V. and de Zeeuw, K., "Relation Between Delamination and Temperature-Cycling Induced Failures in Plastic Packaged Devices", *Proceedings of 40th Electronic Components & Technology Conference*, IEEE, Las Vegas, NV, pp. 813-820, 1990.
- Edwards, D. R., Heinen, K. G., Martinez, J. E. and Groothuis, S., "Shear Stress Evaluation of Plastic Packages", *Proceedings of 37th Electronic Components & Technology Conference*, pp. 84-95, 1987.
- Emerick, A., Ellerson, J., McCreary, J., Noreika, R. and Vishwanadham, P., "Enhancement of TSOP Solder Joint Reliability Using Encapsulation", *Proceedings of the 43rd Electronic Components & Technology Conference*, Orlando, FL, pp. 187-192, June 1-6 1993.
- Engelmaier, W., "Fatigue life of leadless chip carrier solder joints during power cycling," *IEEE Transactions on Components, Hybrids, Manufacturing Technology*, Vol. 6, pp. 52–57, September, 1983.
- Engelmaier, W., "Functional Cycles and Surface Mounting Attachment Reliability", *ISHM Technical Monograph Series*, pp. 87-114, 1984.
- Engelmaier, W., "Test Method Considerations for SMT Solder Joint Reliability", *Proceedings of International Electronics Packaging Society Conference*, Baltimore, MD, pp. 360-369, October 29-31, 1984.
- Erinc, M., Schreurs, P. J. G., Zhang, G. Q., Driel, W. D. van and Geers, M. G. D, "Microstructural and Mechanical Characterization of 95.5Sn4.0Ag0.5Cu Solder Balls

- by Nano-Indentation", *Proceedings of 5th International Conference on Thermal and Mechanical Simulation and Experiments in Microelectronics and Microsystems*, pp. 443-448, 2004.
- Evans, J.L., R. Newberry, L. Bosley, S. G. McNeal, A. Mawer, R. W. Johnson and J. C. Suhling, "PBGA Reliability for Under-the-Hood automotive Applications", *Proceedings of InterPACK '97*, Kohala, HI, pp. 215-219, June 15-19, 1997.
- Fan, J-W, Kuo, C-T and Yip, M-C, "Mechanical Characterization of Board-Level 63Sn37Pb and Lead-Free Solder Sphere Attachment on Cu-Pad/Ni/Au Surface Finish Substrates", *Proceedings of the 53rd Electronic Components & Technology Conference*, New Orleans, LA, pp. 712-717, May 27-30, 2003.
- Feustel, F., Wiese, S. and Meusel, E., "Time-Dependent Material Modeling for Finite Element Analyses of Flip Chips", *Proceedings of the 50th Electronic Components and Technology Conference*, Las Vegas, Nevada, pp. 1548-1553, May 21-24, 2000.
- Gee, S. A., Johnson, M. R. and Chen, K. L., "Test Chip Design for Detecting Thin Film Cracking in Integrated Circuits", *Transactions on Components, Packaging and Manufacturing Technology*, Part B Advanced Packaging, Vol. 18(3), pp. 478-484, 1995.
- Giulio, D-G, Relibility of Electronic Packages and Semiconductor Devices, McGraw-Hill, New York, 1997.
- Gregor, M. and Munier, C., "A Review of Creep Fatigue Failure Models in Solder Material-Simplified Use of a Continuous Damage Mechanical Approach", *Proceedings of 5th International Conference on Thermal and Mechanical Simulation and Experiments in Microelectronics and Microsystems*, pp. 465-472, 2004.
- Gustafsson, G., Guven, I., Kradinov, V., Madenci, E., "Finite Element Modeling of BGA Packages for Life Prediction", *Proceedings of the 50th Electronic Components and Technology Conference*, Las Vegas, Nevada, pp. 1059-1063, May 21-24, 2000.
- Guven, I., Kradinov, V., Madenci, E. and Tor, J. L., "Solder Joint Life Prediction Model Based on the Strain Energy Density Criterion", *Proceedings of the 53rd Electronic Components & Technology Conference*, New Orleans, LA, pp. 214-220, May 27-30, 2003.
- Guzman, J. C. de, Epistola, E. and Mena, M. G., "Elimination of Assembly Induced Package Cracks in Plastic SOICs", *Proceedings of 46th Electronic Components & Technology Conference*, Orlando, FL, pp. 92-106, May 29-31, 1996.
- Hall, P. M., "Forces, moment, and displacements during thermal chamber cycling of leadless ceramic chip carriers soldered to printed boards", *IEEE Transactions on Components, Hybrids and Manufacturing Technology*, Vol. 7, No. 4, pp.314-327, December 1984.

- Harmon, G. G., "Metallurgical Failure Modes of Wire Bonds', 12th Annual Proceedings, Reliability Physics, pp. 131-141, 1974.
- Harper, C. A., *Electronic Packaging and Interconnection Handbook*, McGraw-Hill, 4th Edition, New York, September, 2004.
- Hossain, M. M. and Agnofer, D., "Strain Based Approach for Predicting the Solder Joint Fatigue Life with the Addition of Intermetallic Compound Using Finite Element Modeling", *Proceedings of 2004 Inter Society Conference on Thermal Phenomena*, Las Vegas, NV, pp. 358-367, June 1-4, 2004.
- Hu, J. M., Barker, D., Dasgupta, A. and Arora, A., "Role of Failure-Mechanism Identification in Accelerated Testing", *Proceedings of Annual Reliability and Maintainability Symposium*, pp. 181-188, 1992.
- Hung, S. C., Zheng, P. J., Lee, S. C., Ho, S. H. and Chen, H. N., "Thermal Cycling Fatigue of the Interconnect of a Flex-Type BGA", *Proceedings of 50th Electronic Components & Technology Conference*, IEEE, Las Vegas, NV, pp. 1384-1391, 2000.
- Hwang, J. S., "Solder Joint Failure Phenomena", *Proceedings of the National Electronic Packaging and Production Conference*, *NEPCON East* '88, pp. 305-322, 1988.
- Ilyas, Q. S. M. and Roberts, B., "Moisture sensitivities of SM packages, structural analysis in microelectronics and fiber optics", *ASME*, *EEP* Vol. 7, pp. 145-156, 1993.
- Isaac, J., "Packaging Trends: Automating IC Packaging", *International Magzine for Electronic Packaging Applications*, Advanced Packaging, pp. 12, November 2005.
- Iscoff, R., "Going Green and Lead-Free: The Race is On!", *Chip Scale Review*, Vol. 9, No. 6, pp. 32, August-September, 2005.
- Jaegar, R. C., Suhling, J. C., Carey M. T., and Johnson, R. W., "A Piezoresistive Sensor Chip for Measurement of Stress in Electronic Packaging", *Proceedings of 43rd Electronic Components & Technology Conference*, pp. 686-692, 1993.
- Johnson, Z., "Implementation and Extension to Darveaux's Approach to Finite Element Simulation of BGA Solder Joint Relibility", *Proceedings of 49th Electronic Components & Technology Conference*, San Diego, CA, pp. 1220-1229, June 1-4, 1999.
- Jung, E., Heinricht, K., Kloeser, J., Aschenbrenner, R. and Reichl, H., "Alternative Solders for Flip Chip Applications in the Automotive Environment", *Proceedings of IEMT-Europe*, Berlin, Germany, pp. 82-91, 1998.
- Kim, D., Mawer, A, Masada, G. Y. and Moon, T. J., "Modeling and Analysis of Crack Growth in SnPb and SnAgCu Solder Joints in PBGA Packages: Part I-Crack Initiation", *Proceedings of 2003 ASME International Mechanical Engineering Congress*, Washington, D. C., pp. 251-260, November 15-21, 2003.

- Kim, D-H, Elenius, P. and Barret, S., "Solder Joint Reliability and Characteristics of Deformation and Crack Growth of Sn-Ag-Cu Versus Eutectic Sn-Pb on a WLP in a Thermal Cycling Test", *IEEE Transactions on Electronics Packaging Manufacturing*, Vol. 25, No. 2, pp. 84-95, April, 2002.
- Knecht, S., and L. Fox, "Integrated matrix creep: application to accelerated testing and lifetime prediction", *Chapter 16, Solder Joint Reliability: Theory and Applications*, ed. J. H. Lau, Van Nostrand Reinhold, pp. 508-544, 1991.
- Kotlowitz, R. W. and Engelmaier, W., "Impact of Lead Comlpaince on the Solder Attachment Reliability of Leaded Surface Mounted Devices", *Proceedings of 1986 International Electronics Packaging Society Conference*, San Diego, CA, pp. 841-865, November 17-19, 1986.
- Kotlowitz, R. W. and Engelmaier, W., "Impact of Lead Compliance on the Solder Attachment Reliability of Leaded Surface Mounted Devices", *Proceedings of International Electronics Packaging Society Conference*, San Diego, CA, pp. 841-865, November 17-19, 1986.
- Kotlowitz, R. W., "Comparative Compaliance of Reperesentative Lead Designs for Surface Mounted Components", *Proceedings of International Electronics Packaging Society Conference*, Dallas, TX, pp. 908-948, November 7-10, 1988.
- Lall, P., Islam, N. and Suhling, J., "Prognostication and Health Monitoring of Leaded and Lead Free Electronic and MEMS Packages in Harsh Environments", *Proceedings of 55th Electronic Components & Technology Conference*, IEEE, Orlando, FL, pp. 1305-1313, May 31-June 3, 2005.
- Lall, P., Islam, N., Suhling, J. and Darveaux, R., "Model for BGA and CSP Reliability in Automotive Underhood Applications", *Proceedings of 53rd Electronic Components and Technology Conference*, New Orleans, LA, pp.189 –196, May 27-30, 2003.
- Lall, P., Islam, N., Rahim, M. K. and Suhling, J., "Prognostics and Health Management of Electronic Packaging", *IEEE Transactions on Components and Packaging Technologies*, Accepted for Publication, Available on IEEE Explore, 2005.
- Lall, P., Islam, N., Shete, T., Evans, J., Suhling, J. and Gale, S, "Damage Mechanics of Electronics on Metal-backed Substrates in Harsh Environments", *Proceedings of 54th Electronic Components & Technology Conference*, IEEE, Las Vegas, NV, pp. 704-711, June 1-4, 2004.
- Lall, P., Islam, N., Rahim, M. K., Suhling, J. and Gale, S., "Leading Indicators-of-Failure for Prognosis of Electronic and MEMS Packaging", *Proceedings of 54th Electronic Components & Technology Conference*, IEEE, Las Vegas, NV, pp. 1570-1578, June 1-4, 2004.

- Lall, P., Islam, N, Suhling, J., Darveaux, R., Model for BGA and CSP in Automotive Underhood Environments, *IEEE Transactions on Components and Packaging Technologies*, Volume 27, Number 3, pp. 585-593, September 2004.
- Lall, P., Singh, N, Suhling, J., Strickland, M. and Blanche, J., "Thermal Reliability Considerations for Deployemnet of Area Array Packages in Harsh Environments", *Proceedings of 2004 Inter Society Conference on Thermal Phenomena*, Las Vegas, NV, pp. 259-267, June 1-4, 2004.
- Lall, P., Singh, N, Suhling, J., Strickland, M. and Blanche, J., "Decision-Support Models for Thermo-Mechanical Reliability of Leadfree Flip-Chip Electronics in Extreme Environments", *Proceedings of 55th Electronic Components & Technology Conference*, IEEE, Orlando, FL, pp. 127-136, May 31-June 3, 2005.
- Lall, P., Singh, N, Suhling, J., Strickland, M. and Blanche, J., "Thermo-mechanical reliability tradeoffs for deployment of area array packages in harsh environments", *IEEE Transactions on Components and Packaging Technologies*, Vol. 28, Issue 3, pp. 457-466, September 2005.
- Lall, P., Pecht, M. and Hakim, E, *Influence of Temperature on Microelectronic and System Reliability*, CRC Press, Inc., Sep. 1997
- Lau, J. H. and Dauksher, W., "Reliability of an 1657CCGA (Ceramic Column Grid Array) Package with 95.5Sn3.9Ag0.6Cu Lead-Free Solder Paste on PCBs (Printed Circuit Boards)", *Proceedings of 2003 ASME International Mechanical Engineering Congress*, Washington, D. C., pp. 202-208, November 15-21, 2003.
- Lau, J. H., Ball Grid Array Technology, McGraw-Hill, New York, 1995.
- Lau, J. H., Dauksher, W., and Vianco, P., "Acceleration Models, Constitutive Equations and Reliability of Lead-Free Solders and Joints", *Proceedings of the 53rd Electronic Components & Technology Conference*, New Orleans, LA, pp. 229-236, May 27-30, 2003.
- Lau, J. H., Shangguan, D., Lau, D. C. Y., Kung, T. T. W. and Lee, S. W. R., "Thermal-Fatigue Life Prediction Equation for Wafer-Level Chep Scale Package (WLCSP) Lead-Free Solder Joints on Lead-Free Printed Circuit Board (PCB)", *Proceedings of 54th Electronic Components & Technology Conference*, IEEE, Las Vegas, NV, pp. 1563-1569, June 1-4, 2004.
- Lau, J. H., Solder Joint Reliability: Theory and Applications, Van Nostrand Reinhold, 1991.
- Lau, J. H., *Thermal Stress and Strain in Microelectronics Packaging*, Van Nostrand Reinhold, 1993.
- Lau, J.H., Flip Chip Technologies, McGraw Hill, New York, 1996.

- Lau, J. H. and Pao, Y-H, Solder Joint Reliability of BGA, CSP, Flip Chip, and Fine Pitch SMT Assemblies, McGraw-Hill, New York, 1997.
- Lee, C., Chen, W. T. and Pape, H., "A New Lead Frame Design for Improved Popcorn Cracking Performance", *Proceedings of 46th Electronic Components & Technology Conference*, Orlando, FL, pp. 78-91, May 29-31, 1996.
- Lee, W. W., Nguyen, L. T. and Selvaduray, G. S., "Solder Joint Fatigue Models: Review and Applicability to Chip Scale Packages", *Transactions on Microelectronics Reliability*, Vol. 40, pp. 231-244, 2000.
- Lindley, T. R., "BGA Solder Joint Reliability Study for Automotive Electronics", *Proceedings of the 1995 International Conference on Multichip Modules*, Denver, CO, pp. 126-133, April 19-21, 1995.
- Liu X.S., S. Haque, and G.-Q. Lu, "Three-dimensional Flip-Chip on Flex Packaging for Power Electronics Applications," *IEEE Transactions on Advanced Packaging*, Vol. 24, pp. 1-9, Feb. 2001.
- Liu, C., Geggel, M., Conway, P. and Hendrilksen, M., "Micro-Scale Mechanical Properties of the Feature Flip-Chip with Lead Free Solders", *Proceedings of International Symposium on Electronic Materials and Packaging*, pp. 259-266, 2002.
- Lu H., Bailey C., Cross M., "Reliability Analysis of Flip Chip Designs via Computer Simulation", *Journal of Electronic Packaging*, Transactions of the ASME, Vol. 122, No. 3, pp. 214-219, September 2000.
- Manson, S.S. and Hirschberg, M.H., *Fatigue: An Interdisciplinary Approach*, Syracuse University Press, Syracuse, NY, pp. 133, 1964
- Mawer, A., N. Vo, Z. Johnson and W. Lindsey, "Board-Level Characterization of 1.0mm and 1.27mm Pitch PBGA for Automotive Under-Hood Applications", *Proceedings of the 49th Electronic Components and Technology Conference*, San Diego, CA, pp. 118-124, June 1-4, 1999.
- Mawer, A., Cho, D. and Dareaux, R., "The Effect of PBGA Solder Pad Geometry on Solder Joint Reliability", *Proceedings of SMI*, pp. 127-135, 1996.
- May, D. J. R, "Trapezoidal Rule", Web Resource, http://metric2.ma.ic.ac.uk
- Mercado, L. L., Sarihan, V., Guo, Y. and Mawer, A., "Impact of Solder Pad Size on Solder Joint Reliability in Flip Chip PBGA Packages", *IEEE Transactions on Advanced Packaging*, Vol. 23, No. 3, August 2000.
- Mitchell, D, Zahn, B. and Carson, F., "Board Level Thermal Cycle Reliability and Solder Joint Fatigue Life Predictions of Multiple Stacked Die Chip Scale Package Configuration", *Proceedings of 54th Electronic Components & Technology Conference*, IEEE, Las Vegas, NV, pp. 699-703, June 1-4, 2004.

- Moore, T. M. and Kelsall, S. J., "The Impact of Delamination of Stress Induced and Conatmination Related Failure in Surface Mounted ICs", *Proceedings of the 30th Annual International Relaibility Physics Symposium*, IEEE, San Diego, CA, pp. 169-176, 1992.
- Moore, T. M., "Reliable Delamination Detection by Polarity Analysis of Reflected Acoustic Pulses", *Proceedings of International Symposium for Testing and Failure Analysis*, pp. 49-54, 1991.
- Muncy, J. V. and Baldwin, D. F., "A Component Level Predictive Reliability Modeling Methodology", *Proceedings of 2004 SMTA International Conference*, Chicago, IL, pp. 482-490, September 26-30, 2004.
- Muncy, J. V., Lazarakis, T. and Baldwin, D. F., "Predictive Failure Model of Flip Chip on Board Component Level Assemblies", *Proceedings of 53rd Electronic Components & Technology Conference*, IEEE, New Orleans, LA, May 27-30, 2003.
- Muncy, J. V., Predictive Failure Model For Flip Chip On Board Component Level Assemblies, *Ph. D. Dissertation*, Georgia Institute of Technology, Atlanta, GA, January, 2004.
- Nimkar, N. D., Bhavnani, S. H. and Jaeger R. C., "Benchmark Heat Transfer Data for Microstructured Surfaces for Immersion-Cooled Microelectronics", IEEE Transactions on Components and Packaging Technologies, Accepted for future publication, Issue 99, 2005.
- Nose, H., Sakane, M., Tsukada, Y. And Nishimura, H., "Temperature and Strain Rate Effects on Tensile Strength and Inelastic Constitutive Relationship of Sn-Pb Solders", *ASME Journal of Electronic Packaging*, Vol. 125, pp. 59-66, March 2003.
- Okikawa, S., Sakimoto, M., Tanaka, T., Sato, T., Toya, T. And Hara, Y., "Stress Analysis of Passivation Film Crack for Plastic Molded LSI Caused by Thermal Stress", *Proceedings of International Symposium for Testing and Failure Analysis*, pp. 75-81, 1987.
- Pang, H. L. J., Kowk, Y.T. and SeeToh, C. W., "Temperature Cycling Fatigue Analysis of Fine Pitch Solder Joints", *Proceedings of the Pacific Rim/ASME International Intersociety Electronic and Photonic Packaging Conference, INTERPack* '97,Vol. 2, pp. 1495-1500, 1997.
- Pang, J. H. L., Prakash, K. H. And Low, T. H., "Isothermal and Thermal Cycling Aging on IMC Growth Rate in Pb-Free and Pb-Based Solder Interfaces", *Proceedings of 2004 Inter Society Conference on Thermal Phenomena*, Las Vegas, NV, pp. 109-115, June 1-4, 2004.
- Pang, J. H. L., Xiong, B. S. and Che, F. X., "Modeling Stress Strain Curves for Lead-Free 95.5Sn-3.8Ag-0.7Cu Solder", *Proceedings of 5th International Conference on*

- Thermal and Mechanical Simulation and Experiments in Microelectronics and Microsystems, pp. 449-453, 2004.
- Pang, J. H. L., Xiong, B. S. and Low, T. H., "Creep and Fatigue Characterization of Lead Free 95.5Sn-3.8Ag-0.7Cu Solder", *Proceedings of 2004 Inter Society Conference on Thermal Phenomena*, Las Vegas, NV, pp. 1333-1337, June 1-4, 2004.
- Pascariu G., Cronin P, Crowley D, "Next-generation Electronics Packaging Using Flip Chip Technology", *Transactions on Advanced Packaging*, Nov.2003
- Perkins, A. and Sitaraman, S. K., "Predictive Fatigue Life Equations for CBGA Electronic Packages Based on Design Parameters", *Proceedings of 2004 Inter Society Conference on Thermal Phenomena*, Las Vegas, NV, pp. 253-258, June 1-4, 2004.
- Popelar S. F., "Parametric Study of Flip Chip Reliability Based on Solder Fatigue Modeling: Part II-Flip Chip on Organic", *Proceedings of SPIE: The International Society for Optical Engineering*, v 3582, pp 497-504, 1998.
- Pucha, R. V., Pyland, J and Sitaraman, S., "Damage Metric-Based Mapping Approaches for Developing Accelerated Thermal Cycling Guidelines for Electyronic Packages", *International Journal of Damage Mechanics*, Vol. 10, pp. 214-234, July 2001.
- Pyland, J., Pucha, R. V., Sitaraman, S. K., "Thermomechanical Reliability of Underfilled BGA Packages", *IEEE Transactions on Electronics Packaging Manufacturing*, Vol. 25, No. 2, pp. 100-106, April 2002.
- Ray, S.K., Quinones, H., Iruvanti, S., Atwood, E., Walls, L., "Ceramic Column Grid Array (CCGA) Module for a High Performance Workstation Application", *Proceedings of 47th Electronic Components and Technology Conference*, pp 319-324, 1997.
- Schubert, A., Dudek, R., Auerswald, E., Gollhardt, A., Michel, B. and Reichel, H., "Fatigue Life Models for SnAgCu and SnPb Solder Joints Evaluated by Experiments and Simulation", *Proceedings of 53rd Electronic Components and Technology Conference*, New Orleans, LA, pp. 603-610, May 27-30, 2003.
- Schubert, A., Dudek, R., Doring, R., Walter, H., Auerswald, E., Gollhardt, A. and Michel, B., "Thermo-Mechanical Reliability of Lead-Free Solder Interconnects", *Proceedings of 8th International Symposium on Advanced Packaging Materials*, pp. 90-96, 2002.
- Schubert, A., Dudek, R., Walter, H., Jung, E., Gollhardt, A., Michel, B., and Reichl, H., "Reliability Assessment of Flip Chip Assemblies with Lead-Free Solder Joints", *Proceedings of 52nd Electronic Components and Technology Conference*, San Diego, CA, pp. 1246-1255, May 28-31, 2002.

- Schubert, A., Walter, H., Dudek, R. and Michel, B., "Thermo-Mechanical Properties and Creep Deformation of Lead-Containing and Lead-Free Solder", *Proceedings of International Symposium on Advanced Packaging Materials*, pp. 129-134, 2001.
- Shen, L., Yi, S., Caers, J., Zhao, X. and Zhang, K., "A Damage Parameter Based on Fracture Surface for Fatigue Life Prediction of CSP Solder Joints", *Proceedings of International Symposium on Electronic Materials and Packaging*, pp. 412-416, 2001.
- Shi, X. Q., Pang, H. L. J., Zhou, W. and Wang, Z. P., "A Modified Energy-Based Low Cycle Fatigue Model for Eutectic Solder Alloy", *Journal of Scripta Material*, Vol. 41, No. 3, pp. 289-296, 1999.
- Shi, X. Q., Pang, H. L. J., Zhou, W. and Wang, Z. P., "Low Cycle Fatigue Analysis of Temperature and Frequency Effects in Eutectic Solder Alloy", *International Journal of Fatigue*, pp. 217-228, 2000.
- Sillanpaa, M., and Okura, J.H., "Flip chip on board: assessment of reliability in cellular phone application", *IEEE Transactions on Components, Packaging and Manufacturing Technology*, Vol.27, Issue:3, pp. 461–467, Sept.2004.
- Solomon, H. D., "Fatigue of 60/40 solder," *IEEE Transactions on Components, Hybrids, Manufacturing Technology*, Vol. 9, pp. 423–432, Dec. 1986.
- Solomon, H. D., "Low Cycle Fatigue of Surface Mounted Chip Carrier Printed Wiring Board Joints", *Proceedings of 39th Electronic Components & Technology Conference*, IEEE, Huston, TX, pp. 277-292, May, 1989.
- Suhir, E., "Thermal Stress Failures in Microelectronic Components–Review and Extension", Vol. 1, Chapter 5, in *Advances in Thermal Modeling of Electronic Components and Systems*, ed. A. Bar-Cohen and A. D. Kraus, Hemisphere Publishing Co., pp. 337-412, 1990.
- Suhir, E., "Calculated Thermally Induced Stresses in Adhesively Bonded and Soldered Assemblies", *Proceedings of the International Symposium on Microelectronics*, Atlanta, Georgia, pp. 386-392, Oct. 1986.
- Suhling, J C., *Mechanics of Electronic Packaging*, Class Notes of the Course MECH 6310, Spring Semester, 2003.
- Suhling, J. C., Jaegar, R. C., Wilamowski, B. M., Lin, S. T., Mian, A. K. M. and Cordes, R. A., "Design and Calibration of Optimized (111) Silicon Stress Sensing Test Chips", *Proceedings of INTERPack* '97 Kohala HI, pp. 1723-1730, June 15-19, 1997.
- Suhling, J. C., Johnson, R., Mian, A. K. M., Rahim, M., Zou, Y., Ellis, C., Ragam, S., Palmer, M. and Jaegar, R., "Measurement of Backside Flip Chip Die Stresses using Piezoresistive Test Die", *Proceedings of 32nd International Symposium on Microeletronics, IMPAS*, Chicago, pp. 298-303, October 26-28, 1999.

- Suhling, J., Gale, H. S., Johnson, W., Islam, M. N., Shete, T., Lall, P., Bozack, M., Evans, J., Seto, P., Gupta, T. and Thompson, R., "Thermal Cycling Reliability of Lead Free Chip Resistor Solder Joints", *Soldering and Surface Mount Technology Journal*, Vol. 16, No. 2, pp. 77-87, 2004.
- Suli, E. and Mayers, D. F., An Introduction to Numerical Analysis, Cambridge University Press, August, 2003.
- Syed, A. R., "Thermal Fatigue Reliability Enhancement of Plastic Ball Grid Array (PBGA) Packages", *Proceedings of the 46th Electronic Components and Technology Conference*, Orlando, FL, pp. 1211-1216 May 28-31, 1996.
- Syed, A. R., "Thermal Fatigue Reliability Enhancement of Plastic Ball Grid Array (PBGA) Packages", *Proceedings of the 46th Electronic Components and Technology Conference*, Orlando, FL, pp. 1211-1216, May 28-31, 1996.
- Syed, A., "Factors Affecting Creep-Fatigue Interaction in Eutectic Sn/Pb Solder Joints", Proceedings of the Pacific Rim/ASME International Intersociety Electronic and Photonic Packaging Conference, INTERPack '97, Vol. 2, pp. 1535-1542, 1997.
- Syed, A., "Predicting Solder Joint Reliability for Thermal, Power and Bend Cycle within 25% Accuracy", *Proceedings of 51st Electronic Components & Technology Conference*, IEEE, Orlando, FL, pp. 255-263, May 29-June 1, 2001.
- Tien, J. K., Hendrix, B. C., Bretz, B. L. And Attarwala, A. I., "Creep-Fatigue Interactions in Solders", *Proceedings of 39th Electronic Components & Technology Conference*, IEEE, Huston, TX, pp. 259-263, May, 1989.
- Timoshenko, S. P., "Analysis of Bi-Metal Thermostats", *Journal of the Optical Society of America*, Vol. 11, September 1925.
- Towashiraporn, P. and Subbarayan, G., "A Hybrid Fracture-Damage Model for Computationally Efficient Fracture Simulations in Solder Joints", *Proceedings of 53rd Electronic Components and Technology Conference*, New Orleans, LA, pp.462-469, May 27-30, 2003.
- Tummala, R. R., Rymaszewski, E. J. and Klopfenstein, A. G., *Microelectronics Packaging Handbook Technology Drivers Part 1*, Chapman and Hall, New York, 1997.
- Tunga, K., Kacker, K., Pucha, R. V., Sitaraman, S. K., "Accelerated Thermal Cycling: Is it Different for Lead-Free Solder?", *Proceedings of 54th Electronic Components & Technology Conference*, IEEE, Las Vegas, NV, pp. 1579-1585, June 1-4, 2004.
- Tunga, K., Pyland, J., Pucha, R. V., Sitaraman, S. K., "Field-Use Conditions Vs Thermal Cycles-A Physics-Based Mapping Study", *Proceedings of the 53rd Electronic Components & Technology Conference*, New Orleans, LA, pp. 182-188, May 27-30, 2003.

- Uegai, Y., Kawazu, A., Wu, Q., Matsushima, H., Yasunaga, M. and Shimamoto, H., "New Thermal Fatigue Life Prediction Method for BGA/FBGA Solder Joints with Basic Crack Propagation Study", *Proceedings of 52nd Electronic Components and Technology Conference*, San Diego, CA, pp. 1291-1296, May 28-31, 2002.
- Van den Crommenacker, J., "The System-in-Package Approach", *IEEE Transactions on Communications Engineer*, Vol 1, No. 3, pp. 24-25, June/July, 2003.
- Van Gestel, R., de Zeeuw, K., van Gemert, L. And Bagerman, E., "Comparison of Delamination Effects Between Temperature Cycling Test and Highly Accelerated Stress Test in Plastic Packaged Devices", *Proceedings of the 30th Annual International Relaibility Physics Symposium*, IEEE, San Diego, CA, pp. 177-181, 1992.
- Vandevelde, B., Christiaens F., Beyne, Eric., Roggen, J., Peeters, J., Allaert, K., Vandepitte, D. and Bergmans, J., "Thermomechanical Models for Leadless Solder Interconnections in Flip Chip Assemblies", *IEEE Transactions on Components, Packaging and Manufacturing Technology*, Part A, Vol.21, No. 1, pp.177-185, March 1998.
- Vandevelde, B., Gonzalez, M., Beyne, E., Zhang, G. Q. and Caers, J., "Optimal Choice of the FEM Damage Volumes for Estimation of the Solder Joint Reliability for Electronic Package Assemblies", *Proceedings of 53rd Electronic Components and Technology Conference*, New Orleans, LA, pp.189 –196, May 27-30, 2003.
- Vendevelde, B, Beyne, E., Zhang, K. G. Q., Caers, J. F. J. M., Vandepitte, D. and Baelmans, M., "Solder Parameter Sensitivity for CSP Life-Time Prediction Using Simulation-Based Optimization Method", *IEEE Transactions on Electronic Packaging Manufaturing*, Vol. 25, No. 4, pp. 318-325, October 2002.
- Vishwanadham, P., Stenett, M. A., and Haggett, R. A., "Second Level Assembly and Reliability Aspects of Thin Small Outline Packages", *Proceedings of 1993 ASME International Electronic Packaging Conference*, Vol. 2, pp. 1127-1134, September-October 1993.
- Vishwanadham, P. and Singh, P., Failure Modes and Mechanisms in Electronic Packages, Chapman and Hall, New York, 1998.
- Warner, M., Parry, J., Bailey, C. and Lu, H., "Solder Life Prediction in a Thermal Analysis Software Environment", *Proceedings of 2004 Inter Society Conference on Thermal Phenomena*, Las Vegas, NV, pp. 391-396, June 1-4, 2004.
- Weisstein, E., W., "Trapezoidal Rule", From MathWorld--A Wolfram, Web Resource, http://mathworld.wolfram.com/TrapezoidalRule.html
- Wen, S. and Keer, L. M., "Damage Based Fatigue Criterion for Solders in Electronic Packaging", *Proceedings of 2004 Inter Society Conference on Thermal Phenomena*, Las Vegas, NV, pp. 184-191, June 1-4, 2004.

- Wiese, S., Rzepka, S. and Meusel, E, "Time-Independent Plastic Behavior of Solders and It's Effects on FEM Simulations for Electronic Packages", *Proceedings of 8th International Symposium on Advanced Packaging Materials*, pp. 104-111, 2002.
- Wiese, S., Schubert, A., Walter, H., Dudek, R., Feustel, F., Meusel, E. and Michel, B., "Constitutive Behavior of Lead-Free Solders vs Lead-Containing Solders-Experiments on Bulk Specimens and Flip Chip Joints", *Proceedings of 51st Electronic Components & Technology Conference*, IEEE, Orlando, FL, pp. 890-902, May 29-June 1, 2001.
- Wong, B., D. E. Helling and R. W. Clark, "A creep rupture model for two phase eutectic solders", *IEEE Transactions on Components, Hybrids and Manufacturing Technology*, Vol.2, No. 3, pp. 284-290, Sep. 1988.
- Wong, B., Helling, D. E. and Clark, R. W., "A Creep-Rupture Model for Two-Phase Eutectic Solders", IEEE Transactions on *Components, Hybrids and Manufacturing Technology*, Vol. 2, No. 3, September 1988.
- Wong, C. P., Rao, Y., Qu, J. and Wu, S. X., "Creep Behavior Characterization of Some New Materials for high Density Interconnect Substrates Using Dynamic Mechanical Analyzer (DMA)", *Proceedings of International Symposium on Advanced Packaging Materials*, pp. 73-76, 1998.
- Xiao, Q., Nguyen, L. and Armstrong, W. D., "Aging and Creep Behavior of Sn3.9Ag0.6Cu Solder Alloy", *Proceedings of 54th Electronic Components & Technology Conference*, IEEE, Las Vegas, NV, pp. 1325-1332, June 1-4, 2004.
- Yeh C., Zhou W. X., Wyatt K., "Parametric Finite Element Analysis of Flip Chip Reliability", *International Journal of Microcircuits and Electronic Packaging*, Vol. 19, No. 2, pp. 120-127, 1996.
- Yip, L., Massingill, T. and Naini, H., "Moisture Sensitivity Evaluation of Ball Grid Array Packages", *Proceedings of 46th Electronic Components & Technology Conference*, Orlando, FL, pp. 829-835, May 29-31, 1996.
- Zahn, B. A., "Finite Element Based Solder Joint Fatigue Life Predcitions for a Same Die Size-Stacked-Chip Scale-Ball Grid Array Package", *Proceedings of International Electronics Manufacturing Technology Symposium*, pp. 274-284, 2002.
- Zahn, B. A., "Solder Joint Fatigue Life Model Methodology for 63Sn37Pb and 95.5Sn4Ag0.5Cu Materials" *Proceedings of the 53rd Electronic Components & Technology Conference*, New Orleans, LA, pp. 83-94, May 27-30, 2003.
- Zou, Y., Suhling, J. C., Jaegar, R. C. and Ali, H., "Three-Dimensional Die Surface Stress Measurements in Delaminated and Non-Delaminated Plastic Packaging", *Proceedings of 48th Electronic Components & Technology Conference*, Seattle, WA, pp. 1223-1234, May 25-28, 1998.

Zou, Y., Suhling, J. C., Jaegar, R. C., Lin, S. T., Benoit, J. T. and Grzybowski, R. R., "Die Surface Stress Variation During Thermal Cycling and Thermal Aging Reliability Tests", *Proceedings of 49th Electronic Components & Technology Conference*, San Diego, CA, pp. 1249-1260, June 1-4, 1999.

APPENDIX A

List of Symbols

α Coefficient of thermal expansion

γ Shear strain

κ Interfacial complaince

λ Axial complaince

v Poisson's ratio

ξ Dimensional parameter

τ Shear stress

A Area, mm²

BGA Ball grid array

CTE Coefficient of thermal expansion

DF Degrees of freedom

E Modulus of elasticity, MPa

EMC Encapsulant mold compound

f (mean square of residual error) / (mean square of regression error)

F Shear force

G Shear modulus

h Height, mm

I Cross-sectional moment of inertia

N Number of thermal cycles

NSMD Non-solder mask defined

p-value p-value of the coefficient

P Pitch

PCB Printed circuit board

R-sq Multiple coefficient of determination

R-sq(adj) R-sq adjusted for degrees of freedom

S Standard deviation

SE Coeff Standard error of the coefficient

SMD Solder mask defined

t-stat t-statistic of the coefficient

u Displacement

ΔT Thermal cycling temperature differential (°C)

ΔW Inelastic strain energy density

Subscripts

1%f 1% failure life

63.2% Characteristic life

b PCB

c Component

s Solder ball