Reducing ATE Test Time by Voltage and Frequency Scaling

by

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Abstract

During wafer sort, the fabricated chips are subjected to tests that verify if they meet the design specification. Test application time plays a critical role while verifying large volume of dice in a given period of time. These tests are carried out on an automatic test equipment (ATE). The time spent on the ATE directly affects the final cost of the device. Hence it is paramount to reduce test application time such that the device can be verified reliably while keeping the test time to a minimum. While reducing test application time is important, power dissipation is also important while considering reduction in test time. Power dissipation is often a trade off when deciding the test frequency and becomes a major limiting factor.

One of the major approaches to test time reduction during circuit design is to implement multiple scan chains. This approach reduces test time drastically when compared to a same device implemented using a single scan chain. Other approaches involve manipulating test hardware and test patterns to reduce test time and testing many dice in parallel.

The objective of this thesis is to obtain an optimum solution to the trade off and the feasibility of such approaches which can lead to new test methods in hardware and software. The problem is approached in two ways (i) by scaling the supply voltage, and (ii) by scaling the test frequency. Additionally, the two methods can be combined to reduce test time further. These methods can be used in tandem with existing methods to provide additional gain in test time reduction.

The proposed methodologies are verified by simulation and through experiments. The experiments were carried on the Advantest T2000GS ATE located at Auburn University, Alabama. The simulations were performed using ISCAS'89 benchmark circuits and results show up to 50% reduction in test time.

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Chapter 1

Introduction

1.1 VLSI Testing

An abstract form of testing is to observe the response of a device to known inputs under desired environmental conditions. For instance, consider a test to see how good a microwave oven works; here the oven will be considered as the device under test (DUT). To test the operation of the oven, one might try to cook some dish using the microwave oven for a preferred duration of time, where the dish becomes the test input and the time is the duration of test. If the food is cooked well, then the microwave oven operates as desired and thus it passes the test. If it did not cook well then either the microwave oven is faulty (if the food or the container is not hot), or it needs more time (if the food is warm but seems under cooked), i.e., insufficient test input, or the type of food cannot be cooked under the current conditions (if a bowl of rice is cooked without adding water), i.e., error in the process. Similarly, in very large scale integrated circuit testing (or simply VLSI testing), once the circuit is designed, it is tested for the correctness of operation. If the circuit fails the test it may be due to a fault in the design. Either the test was wrong to begin with, or if the design is fabricated then there might have been an error in the process, or the design could have been wrong, or the conditions under which it was tested were wrong. The role of testing is to verify if the design is free of manufacturing defects and the role of diagnosis is to identify the source of the failure [15].

1.1.1 Levels of Testing

The testing and diagnosis of the device can be classified into four types based on the purpose of each test [15]. The order in which they are performed is called as the test flow

and normally is considered as a standard procedure to make sure that the design performs as intended and to capture any anomalies early.

Simulation

This is the first stage of testing where the design netlist is verified using computer programs called simulators. The netlist is a file that contains the structure of the design written in languages such as SPICE or VHDL. The simulators verify the correctness of these netlist by applying inputs and observing the output.

Characterization Test

The characterization test is done during the initial part of the design after fabrication, called the "silicon bring up", before it is sent to production. In this phase the industry designing the device obtains a sample of chips from a foundry that fabricates them. During this step the design is verified and debugged for the correctness of operation and whether the initial sample meets all the specifications of the manufacturer. Functional tests are run and elaborate AC and DC measurements are performed. The thoroughness of the tests during this phase may involve probing internal nodes and the use of specialized tools using electron beam to observe the activity within the device. The step helps in identifying the correct operating limits for the device. These are obtained by performing tests under various voltage and frequency ranges and plotting the results as a *Shmoo plot*, which provides a graphical display of the sample over the operating range [15].

Production Test

Once the chips pass the characterization test, they are sent to be produced in mass volumes. In the production test phase, the tests are less extensive but they still have to meet the manufacturer's specifications. During this phase the test time and hence the test cost plays a paramount role. To minimize the test time, a high coverage of faults is targeted

with minimum vectors possible. Since the chip is already designed and fabricated in mass volume the diagnosis of a failing chip is not performed, and only the pass/fail decision is made [15]. Binning of the dice based on the failing specifications is also done in this stage to maximize yield.

Burn-In Test

The next phase in test flow is the burn-in test phase. The main idea of this test is to accelerate the age of the device. Due to various process variations the produced chips may not be identical. Though the process is controlled, some of these variations are unavoidable. It is found that once the devices are produced some fail early while others do not. Burn-in helps to accelerate the life of the chip by putting the device under test (DUT) at very high temperatures. During this test, the production tests are performed at very high temperatures and voltages. The test targets two types of failures, namely, infant mortality failures and freak failures. In infant mortality failure, the DUT fails very early due to weak resistive lines that burn out easily at a slightly accelerated environment. In freak failure, the DUT works properly as a good chip during normal conditions but fails after a very long time. Such devices are identified by putting the DUT through long hours of burn-in [15].

Incoming Inspection

Once the chips pass the burn-in tests they are sold to various systems manufactures who integrate several components together on a board into one system. During that process, each component is tested to check correctness of operation and the thoroughness of the test can vary based on the system designed. The main idea during this phase is to minimize the effort of replacing an individual defective component after it is integrated into the system [15]. For instance, a faulty graphics card integrated into a laptop and shipped to the customers, ended in recall and a significant loss was incurred by the device manufacturer and component manufacturer [6].

At each step of tests described above, the design is verified for certain mismatches. These mismatches can be termed as defects, errors, or faults. A defect is defined as the unintended difference in the hardware structure from the actual design, an error is a mismatch in the output signal caused by the defect present in the design and a fault is the abstract form of the defect causing that error [15]. For instance, a device could have a process defect such as a weak interconnect between two logic gates, which may produce an error in the output signal and the test engineer will conclude that some fault in the design caused this erroneous output.

1.1.2   Fault Models

There are two basic types of testing, called functional and structural testing. In functional testing, the circuit is tested for correct functional operation by giving functional vectors and verifying if the circuit works. In a structural test, the circuit is verified for any structural anomalies due to fabrication process errors. The structural tests are performed at every level of test described earlier and the test patterns may not have a functionally meaningful output. The structural test is performed based on certain fault models which describe the types of faults targeted. These fault models help to develop algorithms that enable the structural test. Some fault models generally used are given below.

Gate Level Stuck-at Fault Model

In a gate level stuck-at fault model, an input or an output signal line is considered to be stuck at a value 0 or 1 due to the defect in the design. In these tests the signal line is driven with a value opposite to the value being tested. For instance, to test an input line for a value stuck at 0, an input of 1 is applied on that line and the output is observed. If the line is not stuck at 0 then the output will be the expected value for the input value of 1 [15, 29]. The work in this thesis mainly uses the stuck-at fault model for all experiments since it is the simplest fault model.

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Transition Delay Fault Model

Delay fault models checks if the DUT meets the timing specifications. Resistive opens or shorts on interconnects can cause the signal to transition after a delay. In a transition delay fault model, the delay of a transition is measured by forcing a transition on the desired pin and observing that transition at the output. The transition fault model is similar to the stuck-at fault model in the sense that the stuck-at fault takes an infinite amount of time to transition. The difference with the two fault models are that, unlike stuck-at fault models, the transition delay fault model is detected by a vector pair in which the first vector initializes the pins to a value while the second vector cause the transition. In the transition fault model the transition is observed at any path the signal takes, irrespective of whether the path is a short or long path and the test passes if the transition is observed at the output within the specified timing threshold [15, 29].

Path Delay Fault Model

Path delay models are also called as lumped delay fault models. In this fault model, the delay of each gate in the path, if summed up, is claimed to cause more delay in a signal when traveling through that path. In contrast to the transition fault model, the test engineer has the flexibility of choosing the path the signal should take. This could ensure that every path in the design meets the timing constraints [15, 29].

Bridging Fault Model

A bridging fault represents a short between two or more signal lines. The logic value on the signal can be modeled as a 1-dominant (OR Bridge), where a signal value of '1' on one line forces the signal on the neighboring line to be '1', or a 0-dominant (AND bridge), where a signal value of '0' on one line forces the signal on the other line to be '0' [15, 29].

Transistor Level Stuck-at Fault Model

In a transistor level stuck-at fault model the DUT is verified for stuck-open or stuck-short in the transistor. A stuck-open transistor fault would cause the transistor to behave as a dynamic level-sensitive latch, while a stuck-short fault would produce a direct path between the power supply line V_{DD} and the ground line. These faults are not accurately modeled in the gate stuck-at fault model due to the complementary structure of nmos and pmos transistors in the complementary metal oxide semiconductor (CMOS) circuits. To monitor the stuck-short faults, a steady state current is supplied, this test is termed as I_{DDQ} test. To monitor a stuck open fault two vectors are applied. The first vector sensitizes the line to the opposite value, while the second vector propagates the value to an observing point [15, 29].

1.2 Designs for Test

Test circuits can be combinational or sequential circuits. In a combinational circuit there are no registers, such as a D-type flip-flop (DFF) to hold a previous value and hence is a simpler design. Due to the absence of state sensitive registers, testing combinational circuit is straight forward and the automatic test pattern generator (ATPG) will generate test patterns that will sensitize and propagate the fault to the output. In contrast, sequential circuits have registers that hold previous values until there is a change in the values and update the output on the next clock pulse, as shown in Figure 1.1, where the PI and PO are the primary inputs and primary outputs. The combinational logic consist of logic gates and the DFF are D-type flip-flops.

1.2.1 Scan-Based Tests

Since registers are state sensitive, the correct output depends on their current state, which is determined by past values. An ATPG will have to create time frames with the preferred past states to generate sequential ATPG vectors and can be cumbersome to do so.
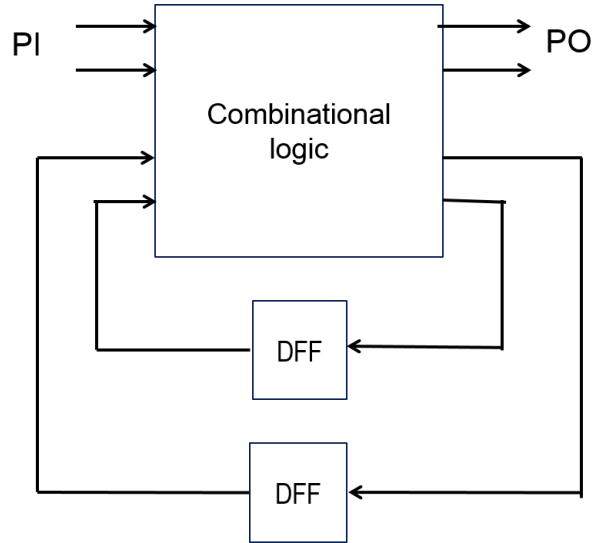
Figure 1.1: Illustration of a sequential circuit with 4 flip-flops.

Due to this reason a sequential circuit is generally converted into a combinational circuit by connecting the registers serially into a serial shift register. The user can then set the register in the preferred state by shifting in the input values, and observe the response by shifting out the values. This type of test methodology is known as scan-based test; it helps to convert a complex sequential circuit into a more manageable combinational circuit. Figure 1.2 illustrates this method, where the registers are connected serially using a multiplexer with one input coming from the combinational logic and the other input coming from the scan input (SI) or from the previous register. The test vectors are serially shifted (scanned) in through the scan input (SI) pin and serially shifted (scanned) out through the scan output (SO) pin. The DUT operates in the normal mode when the scan-enable (SE) pin is '0' and is switched to test mode by driving the SE pin high [29]. The work presented in this thesis uses scan-based methodology to synthesize the register transfer level (RTL) benchmark circuits.

1.2.2 Built-In Self Test

Though scan-based test is widely used, one of the disadvantages of scan-based test methods is that, for a given fault coverage, the volume of test patterns generated by the ATPG can be very large for industrial circuits. Since automatic test equipment (ATE)

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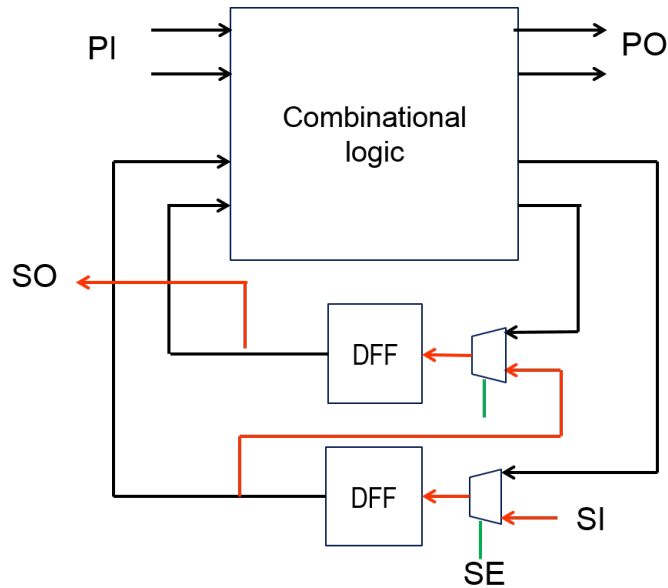
Figure 1.2: Illustration of a sequential circuit with 4 flip-flops connected into a serial shift register.

has limited storage size, very large volumes of patterns can have serious overhead. The built-in self test (BIST) helps to mitigate this problem by incorporating a pattern generator along with the device under test (DUT), with little area overhead. It comprises a test pattern generator (TPG) built using a linear feedback shift register (LFSR), and output response analyzer (ORA) built using multiple input signature register (MISR) [60]. The ORA compacts the output responses from the DUT to form a "signature" which is compared with the "signature" from a known good circuit. The patterns are generated by providing an initial seed to the LFSR. Though the patterns generated by the LFSR may not be as random as in a scan-based test, they can be changed by varying the seed supplied to the LFSR. Random patterns help to capture hard-to detect faults by "chance", thereby providing high fault coverage in short time [29].

1.2.3   Compressor-Decompressor

In the current VLSI trend, designs have hundreds of thousands of sequential elements. When these elements are connected together to form a single shift register, also known as
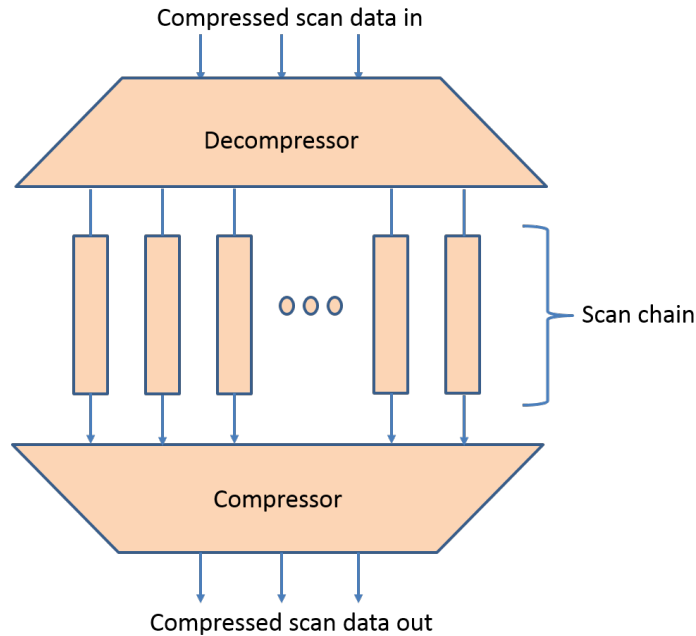
Figure 1.3: Illustration of a compressor-decompressor logic connected to multiple scan chains.

a single scan chain, the number of cycles needed to shift the input values through the scan chain could be large. To minimize this, the single scan chain is normally broken down into multiple smaller scan chains. Though the time to shift the values through the scan chains can be significantly reduced, the number of scan-in pins is increased. Since an ATE has limited amount of pins available, in order to drive the large number of pins on the chip, designs include a hardware circuit pair called compressor-decompressor, or in short codec. The job of the decompressor is to expand and broadcast the input values from the ATE or LFSR to multiple scan inputs within the circuit. The job of the compressor is to get the values from multiple scan out pins and shorten the length of the pattern before sending it to the ATE for storing or analysis. Figure 1.3 illustrates the compressor decompressor architecture of the Synopsys DFTMAX adaptive scan technology [8]. The decompressor is built using a multiplexer which can be used to switch from a 1:1 mode or broadcast mode shown in Figure 1.4, while the compressor is built using an exclusive OR (XOR) tree as shown in Figure 1.5. As the number of input pins for the decompressor increases the test circuit will have more controllability and hence the high test coverage can be obtained with fewer

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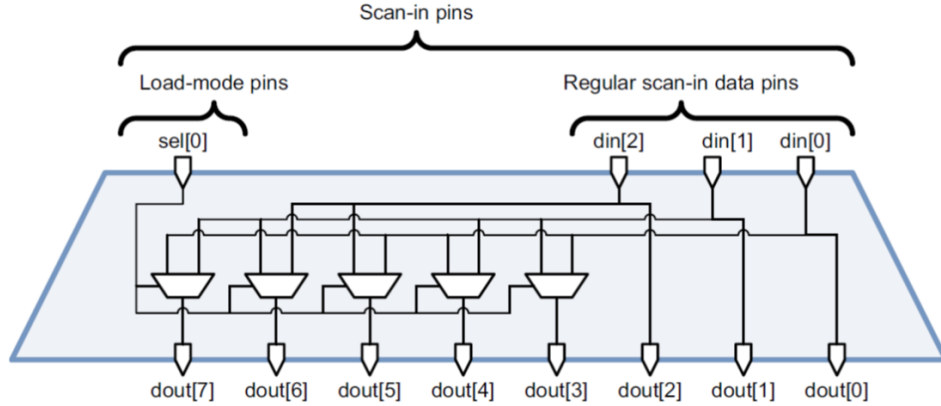
Figure 1.4: Illustration of a decompressor logic built using multiplexor [8].
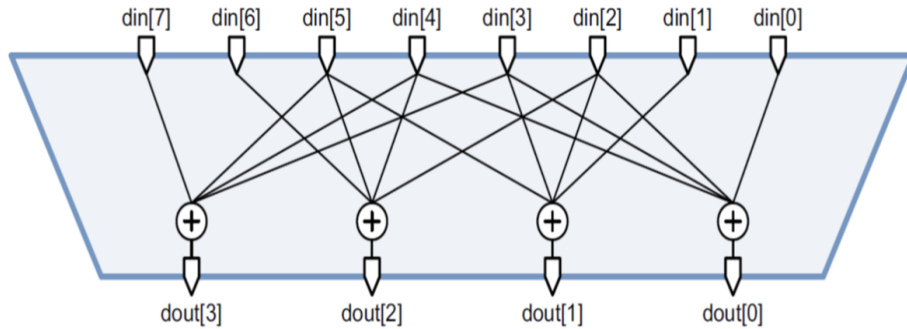
Figure 1.5: Illustration of a compressor built using XOR logic [8].

test patterns. As the output of the compressor increases, the length of the fault signature increases, thus providing better resolution to the signature, thereby reducing undesirable aliasing, where a faulty signature resembles the good signature [8, 29].

1.2.4 SerDes

Though codecs are used with partitioned scan chains to minimize pin count, there may be more pin limitations, like having only one SI pin per chip. This necessitates the need for a separate functional block that takes in the test pattern serially and drives the scan inputs of the chip in parallel. This functional block is known as a serializer-deserializer logic, or in short, SerDes. The SerDes functional block contains a serial to parallel converter and a parallel to serial converter. Besides other applications, the use of SerDes has been suggested

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for reducing the hardware area and power required for on-chip communication [33, 34]. In test application, patterns are normally shifted at high speed through the deserializer shift registers and then shifted at a slower speed through the scan chain. Likewise, the patterns in the serializer registers are shifted out at a high speed [16, 41, 52].

1.2.5 Analog Bus

Similar to SerDes, possibility exists for using analog signal transmission of test data [61]. It has been suggested that n-bit digital data can be converted into an analog voltage by a digital-to-analog converter (DAC), transmitted over a single wire, and then converted back to n digital bits by an analog-to-digital converter (ADC). Such scheme, as suggested for on-chip communication, reduces hardware and is shown to reduce power as well, though it must be carefully designed to limit noise related errors.

1.3 Prior Work

Most digital VLSI circuits today are tested using the scan-based method [15]. This reduces the complexity of testing sequential circuits to that of testing combinational circuits. As mentioned earlier in the scan method, flip-flops are loaded and unloaded through a shift register mechanism for testing faults in the combinational logic. Custom system-on-chip (SoC) designs containing microprocessors, digital signal processors and memories use large numbers of clock cycles during scan-based tests. This directly impacts the final cost of the chip [15]. In the era of low power devices that contain more than a billion gates, long test times have become a critical concern.

While the large size of a device is one reason for long test times, the main limiting factor for test speed is the power dissipated during test due to signal transitions in the circuit. Test power dissipation is known to be $2\times$ the functional power dissipation in central processing units (CPU) [47] and $4\times$ the functional power dissipation in graphic processing units (GPU) [69]. If the power dissipated during tests go beyond the rated power of the

device then it is possible for a good device to fail or even be damaged. Several approaches have been investigated and implemented to reduce the total power dissipation of the circuit under test (DUT); however, these methods generally lengthen the test time [42]. Hence, in the current semiconductor industry, where devices continue to get denser and smaller, both test power and test time must be addressed together.

Earlier approaches to reduce test time used pattern overlapping [20,23] and reusable scan chains [36] to eliminate unwanted scan chain operations through similar patterns to reduce the scan shift process. Reduction in test time depends on the availability of such patterns. Scan chain partitioning also reduces test time significantly but increases the number of scan input pins. Bonhomme et al. [13] and Chalkia et al. [17] proposed methods that can overcome this problem while achieving similar test time reduction as in multiple scan chains. Test time reduction for multi-core SoC designs requires power-constrained scheduling of tests [21, 22, 37]. Recent proposals by Sheshadri et al. [57–59] optimize SoC test schedules by selecting supply voltage and clock frequency.

Shanmugasundaram and Agrawal [53–56] proposed a technique to reduce test time in power-constrained built-in self test (BIST) circuits. They implemented an activity monitor that increases the clock frequency if the monitor records low activity in the chain, otherwise it decreases the frequency. The method achieves $20 - 50\%$ reduction in test time in BIST circuits with little area overhead. Hashempour et al. [32] implemented a system that uses both BIST and ATE in an effort to reduce test time on the ATE. The methodology identifies all "easy-to-detect" faults using BIST and then uses ATE to identify the "hard-to-detect" faults.

Implementing parallel testing, where multiple dice are tested in parallel, has also reduced test time when testing large volumes of dice. One noted disadvantage of such methods is that the time between two tests, also called as indexing time, becomes an overhead when one tester probe has to wait until the other probe completes its test. This can be mitigated by employing an aperiodic probe method, where in a dual-probe tester system, when one

probe detects a faulty die it has the flexibility to check other dice for a good die by gross fault tests until the other probe finishes its lengthy tests [27, 45].

This work presented in this thesis focuses on reducing the test application time and can work in tandem with above mentioned procedures. The test time reduction is achieved by implementing two methods: (1) by scaling supply voltage and (2) scaling test frequency. The methods are investigated mathematically to obtain dependencies and then each method is verified through simulations and experimentation on test equipment, such as Advantest T2000GS entry level ATE for the method using scaled frequency and National Instruments ELVIS [2] board test equipment for the method using scaled supply voltage. The research as it appears here has been presented as posters [63, 64] and discussed at technical forums [10, 11, 65–68].

Chapter 2

VLSI Test Equipment and Procedure

An undergraduate or a graduate student majoring in Electrical and Computer Engineering would have several lab sessions dealing with digital and/or analog circuits. During those lab courses the student would use numerous transistors and integrated circuits to understand the practical applications of what they studied. Students implement the circuit on a circuit board by plugging in and interconnecting components. They then supply input values through a computer or a voltage source connected to the board and observe the output on an oscilloscope or simply on an LED. The output is then verified on the monitor against the output they pre-calculated according to the instructions in their lab manual. If the output matches then they claim that the circuit works and move on, else their circuit does not work and they analyze it closely to fix the faults. This is the most basic form of testing, where for a given circuit a set of input patterns is applied and the output response of that circuit is verified by comparing with known response. If the response matches then the circuit is good, else the circuit is bad and the test engineer then finds the source of the problem and attempts to fix it using diagnostic tools.

In an industry the testing happens from the day the chips are designed using a hardware description language (HDL) until the day the chips are shipped out. In the first half of the chip's design life, the software tools play a major role in test and debug of the design. Here the design is constantly verified for different process corners, such as power, voltage, and timing, using a transistor-level model. However, once the design is fabricated, it is more challenging to meet the required process corners for which the chip is being designed. During this second half of the chip's life in the industry, automatic test equipment (ATE), or simply the tester, plays an important part in making sure that the chip has the expected design and
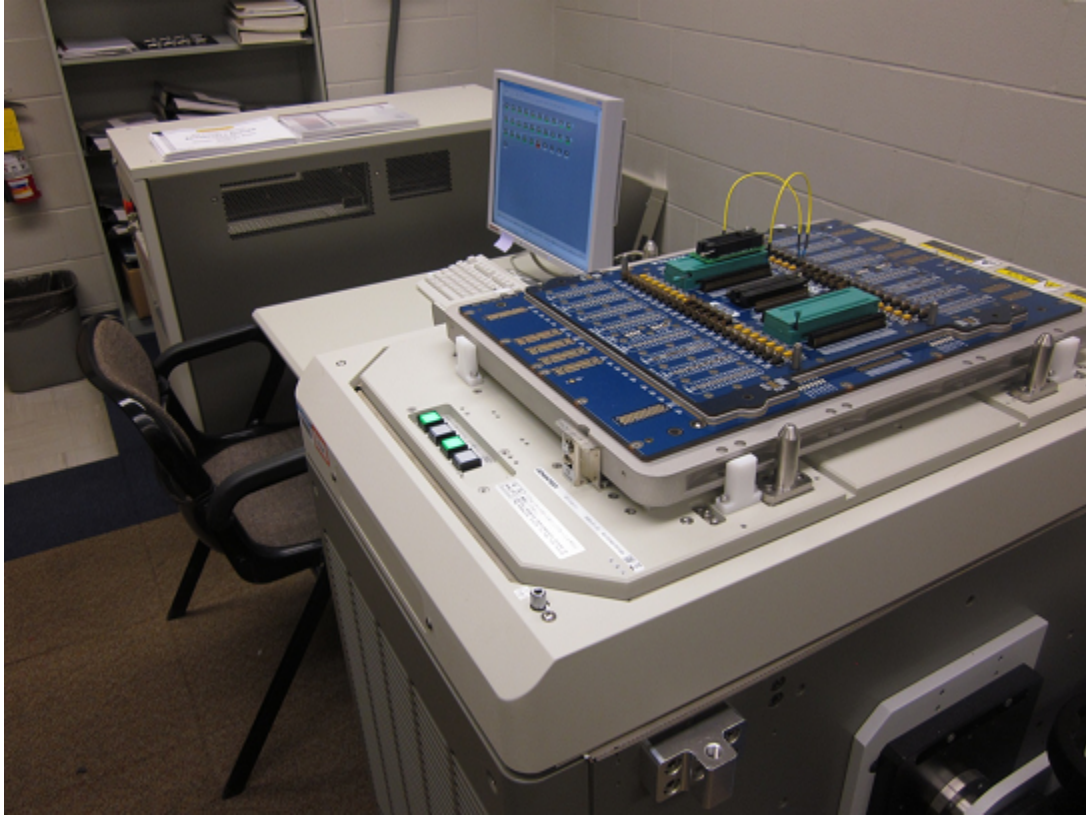
Figure 2.1: Advantest T2000 ATE at Auburn University, Alabama.

is capable of operating with the desired performance. The basic function of the ATE is to drive the inputs with the test patterns and then monitor the output response from the chip.

2.1 Advantest T2000GS ATE

Auburn University, Alabama, houses the automatic test equipment (ATE)- Advantest Model T2000GS, shown in Figure 2.1. The ATE is an entry level system manufactured by Advantest and can perform digital, mixed signal and RF tests. The test equipment consists of three units, the mainframe, a user interface console and a test head.

Mainframe

The mainframe, shown separately in Figure 2.2, supplies the main system power. It also houses the system controller, site controller and the bus matrix. The system controller

Figure 2.2: Mainframe of Advantest T2000GS at Auburn University.

provides the tools and applications required by the test engineer to verify and debug the device under test (DUT) placed on the test head. It controls the user interface, such as keyboard and mouse connected to the system controller. Any information related to the test plan, such as test patterns and test program are stored in the system controller. The site controllers communicate with different modules placed in the test head. It executes the test program on the DUT or test site.

Test head

The test head, shown in Figure 2.3, consists of different modules used to test the DUT. The modules in the test head include a 500mA device power supply module (DPS 500mA), 250MHz Digital module (250MDM) and a sync generator. The sync generator provides the capability of generating multiple time domains or frequencies for the digital module. It

Figure 2.3: Test head of the Advantest T2000GS with an FPGA on the loadboard.

generates the synchronization clock to synchronize the clock with the patterns. The DPS 500mA module has 32 channels and supplies the power to the DUT. The 250MDM consists of 32 I/O channel digital logic to drive and observe the signal on the DUT I/O pins.

2.1.1   Test Programming

Once the device under test (DUT) is fabricated, it is tested to sort good and bad chips in the wafer. For the tester to accurately test the DUT, the test engineers have to provide the tester with three main inputs, namely the test program, the test vectors and the analog test waveform [15]. The production test pattern can be generated by the test software tools such as Mentor graphics Tessent Fastscan [7] or Synopsis Tetramax. Most of the testers in the industry are compatible with the test pattern format called standard test interface

language (STIL) [3, 40] test pattern file. It is the language used to define the test vectors applied to the DUT. The STIL files contain the following information required for the ATE:

1. Definition of each signal pin in the signal block,

2. Timing and waveform information in the timing block,

3. DC signal levels which are applied and expected, and

4. Definition of test patterns.

The test program contains a sequence of instructions that describes the test flow, the patterns to be used and the test environment condition. Once the test program is loaded the tester uses its test pattern generator (TPG) and the frame processor to generate test patterns and the clock, respectively.

The Advantest T2000GS ATE uses a native Open Architecture Test System (OPEN-STAR) Test Programming Language or OTPL for short. It is a modular programming solution that enables user to write procedures dealing with various aspects of the test individually that can later be used with the test plan to obtain a complete test program. Apart from T2000s OTPL, the test plan can also be written using C++ though this requires complete knowledge of the test system and the test object model.

To test a device on the T2000GS ATE the user will have to describe the DUT and the type of test to be performed. Unlike the STIL file, in OTPL the timing information and the definition of each signal are defined separately from the pattern file. To take advantage of the modular programming of T2000, several files are created. These are described next.

Pin Description File

This file defines the signal and power pins available on the DUT and associates each pin with the resource type in the test system. For instance, any I/O signal pin is specified with digital pin resource or "dpin" and the power pins are specified with digital power supply

500mA or "dps500mA" resource. Within each resource definition, the pins can be grouped and labeled for better readability. This file is typically named with a .pin extension.

Socket File

This file specifies the mapping between the DUT pins and the ATE connectors. This file does not offer any grouping of the pins and does a general mapping of each pin with the ATE connectors. Every signal pin is specified in this file and the corresponding ATE connectors can be found in the resource folder.

Specification File

The device specifications, such as the supply voltage range, current range, timing and slew rate are specified in this file. The specifications are defined as a variable with a data type that indicates the type of specification (voltage, current or time) to provide more readability and consistency across other files. Each variable can be specified with a range of values, such as min, max and typical. The range is user defined, and the range for each specification specified in the same order by separating values with commas.

Levels File

The levels file specifies the voltage and current levels at each signal and power pin. The values at each pin can be either fixed or assigned a variable name from the specification file. In this file the levels can be specified common to a group in the pin description file or to an individual pin.

Timing and Timing Map File

The timing description related to the test clock period and the behavior of the signal (waveform) at each pin or pin group is specified in the timing file. Each timing group can be specified with 4 periods and up to 8 waveforms. The input value specified in the pattern file

must be in relation to the values specified in the timing waveform, i.e., if the input values such as 'X' or 'Z' indicating a don't care bit or high impedance, respectively, are specified in the pattern file, the signal behavior for those values must be specified in the timing file.

Test Condition File

The preferred type of operating condition for a given test is specified in the test condition file. It includes the type of voltage levels and their specifications, and the timing information for the test. Every test can be provided with a unique test condition. The test condition for every test can be unique and can either have new specification or use the range from the specification file.

Pattern File

The pattern file has the test patterns or test vectors to be applied during functional tests. The OTPL allows several types of pattern descriptions, such as algorithmic pattern generation (ALPG) , SCAN pattern generation, or a simple pattern list that specifies the values at each input and output pins. The tester's pattern generator will generate the signals based on the values specified in the pattern file and timing behavior provided in the timing file.

Test Plan File

This is the main file that organizes the test flow and calls all the test condition and resource files. Every test flow can also be provided with an option of binning, which logs the failed device and the levels at which the failure occurred. The patterns that each test will use, is also called from this file.

2.1.2   Test Data Analysis

Analyzing the test data helps to identify or sort the good chips from the bad ones. From the bad chips the test engineer can understand the fabrication process and fine tune the process for the next design to minimize the defects. The analysis also provides information about the design weaknesses [15]. The data also provide information on the quality of the test that indicates how thorough the test has been in sorting good chips. A chip that fails can easily be sorted as faulty, however if the chip passes it may be a case that it had passed for the given test model but can fail in some other scenario.

Process variations play a key role in the discrepancies that occur during fabrication. It is quite possible that in the same wafer different chips may have, say, different operating frequencies due to process variations. Failure mode analysis of the failing chips can provide information to improve the fabrication process. Normally chips failing due to process variations have similar failing patterns.

The T2000GS offers several graphical user interface (GUI) tools of which the logic analyzer and the oscilloscope are used in this work. The logic analyzer provides a digital representation of the signal activity during the test and the oscilloscope represents an analog representation of the signal. The oscilloscope provides the tools to measure signal characteristics such as rise and fall times, voltage and current values. These tools also provide indication of the expected and observed values and the time at which the event is observed.

2.2   Time and Cost Relationship

Test time depends on the type of test conducted on the ATE. There are two categories of tests that are performed called the parametric tests and the functional tests. Parametric test are performed with slow speeds and the test time depends on the number of pins that are tested. Functional tests are performed at higher speeds than parametric tests and the test time depends on the number of vectors applied and the frequency at which they are

Table 2.1: State of art IMA Tester Cost Analysis Data [62]

ATE Purchase Price	$985K
Depreciation	20% [27]
Maintenance	4%
Operating Cost	10% [15]
Production weeks/yr	52
Production days/week	7
Production shifts/day	3
production hours/shift	8
Devices per slot	7000
Good devices test time	5 seconds
Bad devices test time	0.3 seconds
Yield	98%

applied. Testing cost can be defined as the cost incurred for the amount of time spent on the tester. This cost can be quantified as [15],

$$Running\ cost\ =\ Depreciation\ +\ Maintenance\ +\ Operating\ Cost$$

Consider the test data example given in Table 2.1. Using the data in the table we can calculate the test cost for a single chip.

$$Running\ Cost\ =\ \$985,000(0.2\ +\ 0.04\ +\ 0.1)\ =\ \$334,900$$

$$Tester\ usage\ =\ weeks/yr\ *\ days/week\ *\ number\ of\ shifts\ *\ hours/shift\ *\ 3600\ sec$$

$$Tester\ usage\ =\ 52\ *\ 7\ *\ 3\ *\ 8\ *\ 3600\ seconds$$

$$\Rightarrow Tester\ usage\ =\ 31,449,600\ seconds$$

$$Testing\ cost\ =\ \frac{Running\ cost}{Tester\ usage}\ cents/second$$

$$Testing\ cost\ =\ \frac{334,900}{31,449,600}\ =\ 10\ cents/second$$

$$Total\ test\ time\ =\ Total\ time\ for\ good\ devices\ +\ Total\ time\ for\ bad\ devices\ seconds$$

$$Total\ test\ time\ =\ 7000\ (0.98\ *\ 5\ +\ 0.02\ *\ 0.3\ )\ =\ 34,342\ seconds$$

$$Total\ cost\ =\ Total\ test\ time\ *\ testing\ cost$$

$$Total\ cost\ =\ 34,342\ seconds\ *\ 10\ cents/second\ =\ 343,420\ cents$$

$$Cost\ per\ die\ =\ \frac{Total\ cost}{Number\ of\ good\ dice}\ =\ 50\ cents$$

$$Cost\ per\ die\ =\ \frac{343,420}{(7000\ *\ 0.98)}\ =\ 50\ cents$$

Though parallel testing dominates the industry, cost of testing will still be significant owing to the volume of chips produced and the number of parallel sites available to run these tests. Having many parallel sites is also added to the cost of tester as a whole and involves maintenance costs. Hence reducing test time reduction is still a major concern in testing.

Test Time Theorem and Applications

In the previous section we saw how test time affects the cost of a single chip. In this section we lay the foundation for the proposed methods by stating a theorem for minimum test time.

3.1 Test Time Theorem

Theorem. *For power constrained testing where the peak power during any clock cycle must not exceed $P_{PEAKfunc}$, the test time (TT) has a lower bound,*

$$\frac{E_{TOTAL}}{P_{PEAKfunc}} \leq TT = \frac{E_{TOTAL}}{P_{AVG}} \tag{3.1}$$

where E_{TOTAL} is the total energy and P_{AVG} is the average power consumed by the test.

Proof:

Consider a test that runs for N clock cycles and for cycle i, we define:

T_i as period of the clock cycle,

E_{di} as dynamic energy consumed during the cycle,

P_{li} as leakage power dissipated during the cycle, and

E_i as total energy consumed during the cycle.

Then, test time and total energy are given by,

$$TT = \sum_{i=1}^{N} T_i \tag{3.2}$$

$$E_{TOTAL} = \sum_{i=1}^{N} E_i = \sum_{i=1}^{N} (E_{di} + T_i \times P_{li}) \tag{3.3}$$

In particular, for a periodic clock test, $T_i = T_{test}$, i.e., all clock cycles have the same period T_{test},

$$TT = N \times T_{test} \tag{3.4}$$

The equality in equation (3.1) follows from the standard definitions of energy and power. P_{AVG} is the rate of energy usage, averaged over the test duration TT. Therefore, total energy is $E_{TOTAL} = TT \times P_{AVG}$.

To prove the lower bound, the power constraint that each clock cycle must satisfy is examined. The clock cycles are assumed to have different periods and thus a conventional periodic clock would be a special case. Thus,

$$\frac{E_{di}}{T_i} + P_{li} \leq P_{PEAKfunc}, \ \forall \ 1 \leq i \leq N \tag{3.5}$$

or

$$T_i \geq \frac{E_{di} + T_i \times P_{li}}{P_{PEAKfunc}}, \ \forall \ 1 \leq i \leq N \tag{3.6}$$

Hence, from equations (3.2) and (3.3),

$$TT \geq \frac{1}{P_{PEAKfunc}} \sum_{i=1}^{N} (E_{di} + T_i \times P_{li}) = \frac{E_{TOTAL}}{P_{PEAKfunc}} \tag{3.7}$$

This proves the lower bound on test time in equation (3.1). ∎

Leakage power plays an interesting role. Notice that in inequality (3.6), T_i appears on both sides. For given $P_{PEAKfunc}$ as clock period T_i is increased to satisfy the power constraint, the right hand side also increases, though at a slower rate because of small P_{li}. The minimum period for i^{th} clock cycle is,

$$T_i = \frac{E_{di}}{P_{PEAKfunc} - P_{li}} \qquad (3.8)$$

To determine T_i we must know dynamic energy E_{di} and leakage power P_{li}, both of which are functions of the input vector applied to the circuit in clock cycle i. For now, let us neglect the leakage power and thus equation (3.8) will take a simpler form,

$$T_i = \frac{E_{di}}{P_{PEAKfunc}} \approx \frac{E_i}{P_{PEAKfunc}} \qquad (3.9)$$

For a given set of test patterns generated by an automatic test pattern generator (ATPG), the total energy consumed during test remains unchanged irrespective of how tests are applied. The total test time is dependent only upon the average power consumed. In order to reduce the test time, it is required that the test be run with the smallest clock period possible while dissipating power less than the rated power. Since the minimum period is limited by the critical path delay of the DUT, test time is dependent on both the rated power and the structural delay of the circuit. The two constraints that determine the minimum test clock period can be defined as follows,

1. Power Constraint - A test is power constrained if the minimum test clock period is limited by the maximum rated power for the circuit. We define this period as $T_{power} = E_{MAX(test)}/P_{PEAKfunc}$ where $P_{PEAKfunc}$ is the maximum power dissipated during functional operation or the rated maximum for the DUT and $E_{MAX(test)}$ is the maximum energy dissipated during any test cycle.

2. Structure Constraint - A test is structure constrained if the minimum test clock period is limited by the structural (critical path) delay of the DUT. We define the fastest clock as $f_{structure} = 1/T_{structure}$ where $T_{structure}$ is the structure constrained clock period.

Based on the above definitions, the minimum test clock period would have to satisfy both power and structure constraints, i.e.,

$$T_{test} = max\{\ T_{structure},\ T_{power}\} \tag{3.10}$$

In a power constrained test, the test clock period is $T_{power} > T_{structure}$, that is,

$$T_{test} = T_{power} = \frac{E_{MAX(test)}}{P_{PEAKfunc}} \tag{3.11}$$

Substituting equation (3.11) in equation (3.4) we get the total test time for power constrained test as;

$$TT_{min} = N \times \frac{E_{MAX(test)}}{P_{PEAKfunc}} \tag{3.12}$$

Equation (3.12) can also be represented as

$$TT_{min} = \frac{E_{TOTAL}}{E_{AVG}} \times T_{synch} = \frac{E_{TOTAL}}{P_{AVG}} \tag{3.13}$$

3.2   Applications of Test Time Theorem

In section 3.1, it was shown that for a given rated power, test time is limited by the total energy dissipated during test. Conventionally, energy can be reduced by modifying the test vectors. For instance, to increase the probability of identifying a fault with a given pattern set, the automatic test pattern generator (ATPG) uses "0's" and "1's" randomly to fill the "don't care" bits during pattern generation. However it causes excessive switching in the scan chain during scan shift and thus increases the shift power. This effect can be avoided by conservatively filling the "don't care" bits with adjacent fill, where the "don't care" bits are filled with the same value of the bits adjacent to it, or with only "0's" or only "1's". Since this procedure is done mainly to reduce power, for a given allowable power the ATPG normally increases the number of test patterns to achieve the desired test coverage.

Thus this increases test time and often is the trade off. Now the question is whether test time can be reduced using a given set of vectors, rated power, and the critical period for the device under test (DUT). Based on the theorem stated earlier, we describe two scenarios in this section and examine the feasibility of reducing test time with the given constraints.

3.2.1 Periodic Clock Test

The first scenario considers a test using a fixed clock period for every cycle during test. This is the conventional method of testing and let us name it as *periodic clock test*, where every cycle has the same period as its neighboring cycle. Now to minimize the test time of a periodic clock test, let us assume a test with N clock cycles with a period T_{test} and frequency $f_{test} = 1/T_{test}$. As described in 3.1 the test clock period is constrained by rated power and the critical path delay of the circuit. Based on equations (3.10) and (3.11) the test clock period is limited by,

- $T_{structure}$ - the critical path delay which limits the minimum period,

- $E_{MAXtest}$ - the maximum cycle energy dissipated for a given set of vectors

- $P_{PEAKfunc}$ - the maximum allowable rated power for the device under test (DUT).

In a power constrained test, the maximum power that any cycle can dissipate is limited to $P_{PEAKfunc}$, hence $P_{PEAKfunc}$ can be assumed as a constant. Then based on equation (3.11) we infer that the only way to minimize T_{test} is to minimize the numerator $E_{MAXtest}$. Since for a given test the test vectors are practically unchanged, the switched capacitance during the test will not vary and thus the energy dissipated during any cycle will be proportional to the quadratic value of the supply voltage applied to the DUT during test. So reducing the supply voltage can significantly reduce the energy during test. Doing so, we now have lot of head room between the power dissipated during test and the allowable peak power. If we want to maintain the same power dissipation, $P_{PEAKfunc}$, the frequency of the test must be increased. The new test clock period T_{test} can be obtained using the equation (3.11) with

the energy dissipated at the new supply voltage. This way the test time can be reduced using the new power constrained test clock period at the new voltage.

The idea of using the low supply voltage and increasing the frequency would work very well if not for one caveat, when the voltage is reduced the gates tend to switch slower due to the now increased time in charging the load capacitance. This indicates that the critical path delay can increase and in worst case change the critical path. Assuming that there is no change in the critical path, when the voltage is reduced the critical path delay increases. From equation (3.10), the test clock period is structure constrained if $T_{structure} > T_{power}$, and any reduction in voltage will increase the delay and hence the test clock period must increase. Hence it should be ensured that the voltage cannot be low enough that the power constrained test clock period is shorter than the structural delay. The optimum supply voltage should be such that the test clock period $T_{test} = T_{power} = T_{structure}$. Thus for a periodic clock testing at optimum voltage,

$$P_{PEAKfunc} = \frac{E_{MAXtest}}{T_{structure}} \tag{3.14}$$

and the minimum test time for a periodic clock test is given by

$$TT_{sync} = N \times T_{structure} \tag{3.15}$$

Figure 3.1 illustrates the minimum test time as a function of supply voltage. if a test is performed at the nominal supply voltage, e.g., 1.8V for 180nm CMOS technology, the test clock period is limited by the maximum power dissipated by the DUT during any clock cycle. If the rated power is lower than the maximum power dissipated during test the test clock period must be wide enough to ensure that the test power does not exceed the rated power. If we reduce the voltage then the $E_{MAXtest}$ reduces and $T_{structure}$ increases. Based on equation (3.11) if the power dissipated is held constant to $P_{PEAKfunc}$ then the test clock period decreases. Repeating the experiment several times at each voltage level, as long as

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Figure 3.1: Minimum test time as a function of supply voltage (V_{DD}) for N-cycle periodic clock test. For a minimum test time TT_{sync} supply voltage is V_{sync} which is lower than the nominal voltage V_{nom}.

the test is still power constrained, we achieve a reduction in test time. At a certain supply voltage $V_{synch} < V_{nom}$, the energy dissipated becomes low enough that the test is no longer power constrained and the structural delay of the circuit starts to dominate the test clock period. Thus, Figure 3.1 can be partitioned into two regions, the region on the right side indicates that the test time is power constrained and region on the left side indicates that the test time is structure constrained. The minimum value of test time occurs at the boundary of the two regions. The voltage at this boundary is the optimum voltage at which the test will be fastest. Any reduction in voltage beyond V_{synch}, i.e. in the structure constrained region, will increase the test time significantly.
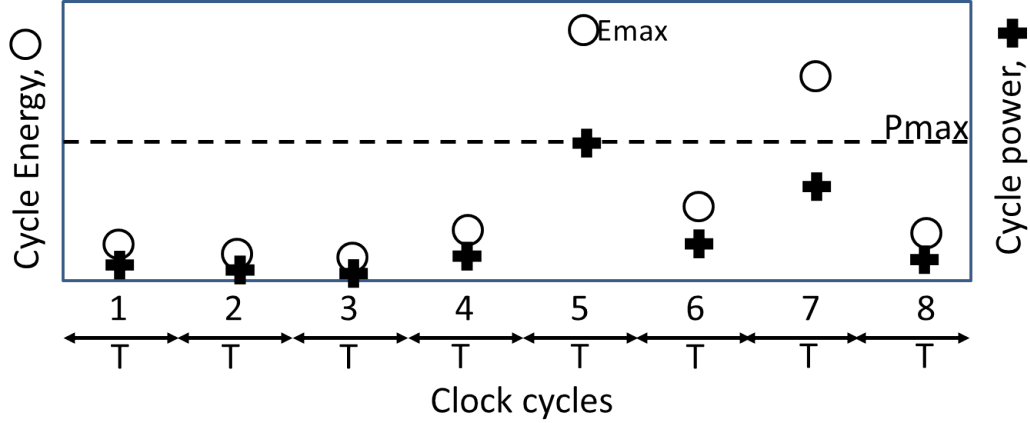
Figure 3.2: Illustration of test power and test energy for every test cycle using periodic clock. The test clock period is determined by the cycle dissipating the maximum power.

3.2.2 Aperiodic Clock Test

In Section 3.2.1 we considered the scenario where the clock period was fixed and thus the power constrained test clock period was determined by the maximum power dissipated during test. Then according to a theorem in Section 3.1 the periodic clock test serves as the upper bound of test time. In the second scenario, the goal is to achieve the lower bound for test time in the theorem.

Consider the illustration in Figure 3.2, which shows the energy and power dissipated during a given test of N cycles ($N = 8$, here). The power constrained test clock period in a periodic clock test is determined by the cycle that consumes the most power. Though the maximum power is now limited within the allowed rated power for the DUT, there will be some cycles that dissipate lower power than the maximum power. Hence, in a power constrained test scenario equation (3.13) may not be the optimum solution for the minimum test time, since the denominator can be small if there are many cycles consuming lower power. This means that the power constrained test time can be reduced if the denominator can be larger. In mathematics, the arithmetic mean of any positive valued function is maximum when all the values in that function have the value equal to the maximum value in the function. Thus, we infer that in order to increase the value of P_{AVG}, every cycle should

31
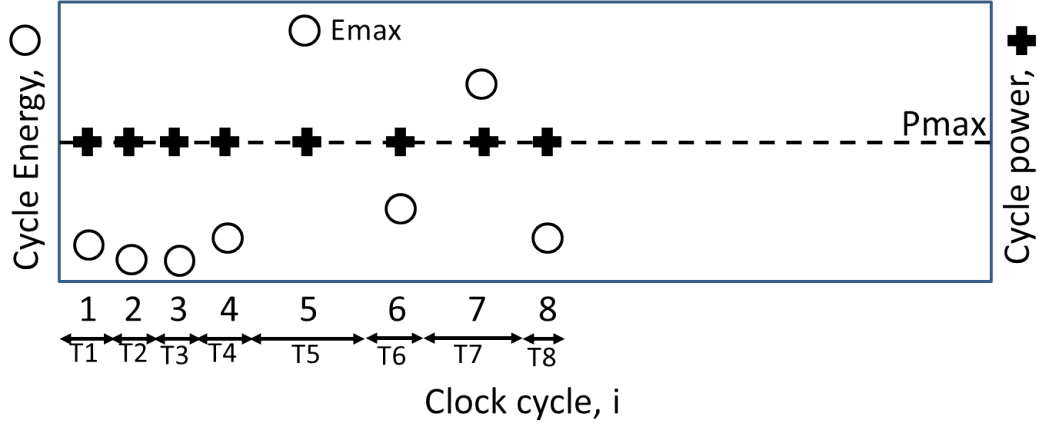
Figure 3.3: Illustration of test power and test energy for every test cycle using aperiodic clock. The test clock period for every cycle is determined by the power dissipated during that cycle.

consume the same power equal to the rated maximum power for that device, i.e., each cycle will now dissipate the same maximum power equal to the rated power $P_{PEAKfunc}$. This is achieved by using *aperiodic clock test* where the period of each clock cycle can be unique and may differ from the period of the neighboring cycle. This is illustrated in Figure 3.3, where every cycle has a unique period that is determined by the amount of power dissipated during that cycle.

Though the period of each cycle is determined by the power dissipated during that cycle, the resulting period must not cause any setup or hold time violations. Hence the minimum clock period allowed is limited to the critical delay of the circuit. The period for each cycle in a aperiodic clock test will then be given by,

$$T_i = \max\{T_{structure}, \ \frac{E_i}{P_{PEAKfunc}}\} \tag{3.16}$$

where E_i, $i = 1, 2, 3, \cdots, N$, is the energy consumption during the ith clock cycle, and T_i is the test clock period of the ith cycle and it must not be shorter than $T_{structure}$. Notice that since the energy is independent of the chosen time period, the device still dissipates

the same amount of energy for the given test vectors as in the periodic clock test. Equation (3.16) indicates that each cycle can be structure constrained or power constrained based on the energy dissipated during that cycle, i.e., the cycle is structure constrained if $E_i \leq P_{PEAKfunc} \times T_{structure}$ and the cycle is power constrained, if $E_i > P_{PEAKfunc} \times T_{structure}$. For instance, in Figure 3.3 since energy E_5 and E_7 are high, cycles T_5 and T_7 will definitely be power constrained. However, because energy E_1 to E_3 are low the corresponding cycles could be structure constrained. Revisiting equation (3.6), we can notice that in an aperiodic clock test the leakage energy during the cycles with shorter time period will be lower. The test time for an aperiodic clock test is bounded by,

$$\sum_{i=1}^{N} \max\{T_{structure}, \frac{E_i}{P_{PEAKfunc}}\} \leq TT_{async} \tag{3.17}$$

$$TT_{async} \leq TT_{sync} = N \times \frac{E_{MAXtest}}{P_{PEAKfunc}} \tag{3.18}$$

Equation (3.17) is true when there are a mix of low power and high power test cycles, and the equality in equation (3.18)will occur when all the cycles dissipate same amount of energy. While from equation (3.18) we can conclude that at any given voltage it is possible that, as long as the test is power constrained, the time taken by an aperiodic clock test will be lower than the time taken by a periodic clock test. So, as described for periodic clock test, there should be an optimum voltage at which the aperiodic clock test is fastest. The optimum voltage for an aperiodic test can in fact be inferred by back tracing from the optimum voltage of a periodic test.

Consider the plot in Figure 3.4, which is an extension of the illustration in Figure 3.1. Here the point 'A' indicates the optimum voltage V_{synch} at which the periodic clock test is fastest. If we increase the voltage from point 'A' then the test will become power constrained, and hence, as we discussed earlier, using a periodic clock test will have a mix of low and high power cycles and the clock period will be based on the cycle that consumes most power. If
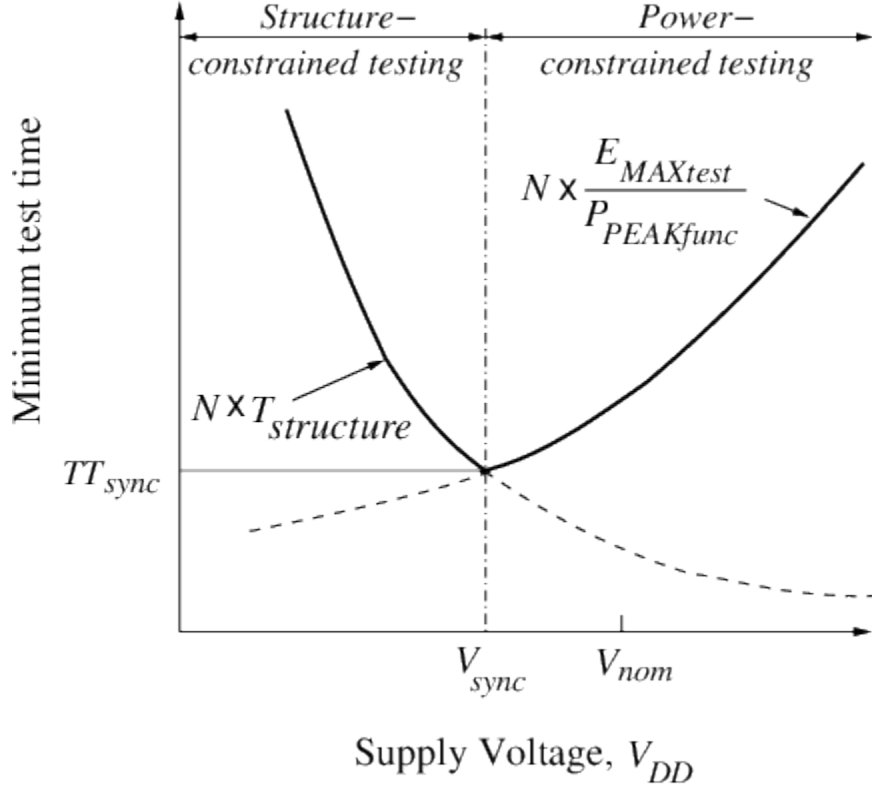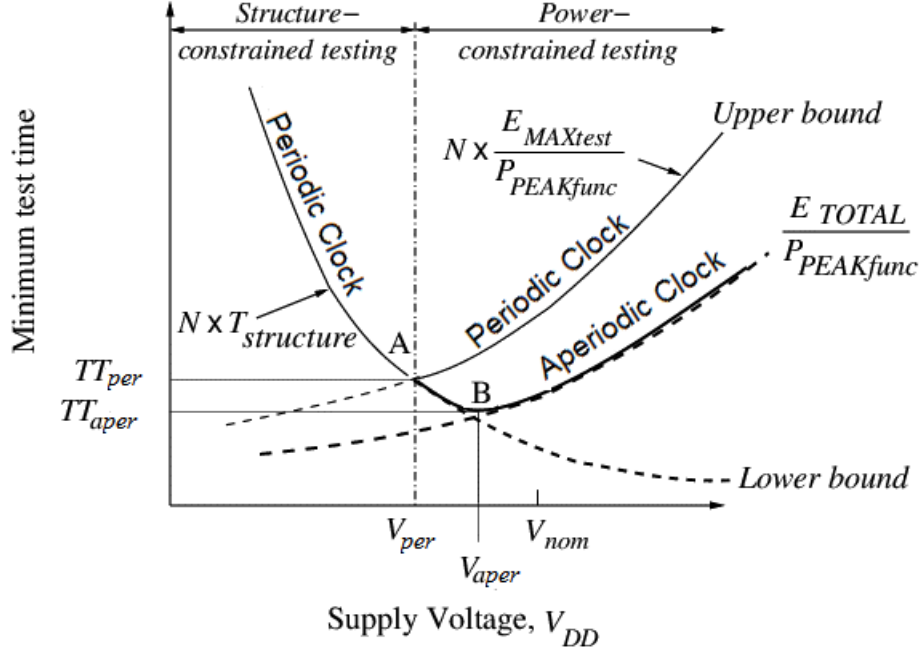
Figure 3.4: Minimum test time as a function of supply voltage (V_{DD}) for N-cycle aperiodic clock test. For a minimum test time TT_{sync} supply voltage is V_{sync} which is lower than the nominal voltage V_{nom}.

we use an aperiodic clock test beyond point 'A', because there is a mix of low power and high power cycles, the low power cycles will use the structural period for the test to run periodically, while the cycles with higher power will be expanded aperiodically to dissipate same amount of power. In the region between point 'A' and point 'B' there will be a mix of structure constrained and power constrained cycles and the test is mostly dominated by the structure constrained cycles. The minimum test time for an aperiodic clock test will be at the supply voltage at which there are more structure constrained cycles than power constrained cycles, and the structural delay is at the minimum. This point is shown in the figure as V_{async}, which is the optimum aperiodic supply voltage, and $V_{asynch} > V_{synch}$ always. From Figure 3.4 we can imply that the periodic clock test at the optimum voltage will be a special case of aperiodic test when every cycle of the aperiodic clock test is structure constrained.

In the following chapters we will discuss more about the applications of the theorem with experimental example on a benchmark circuit and provide enough evidence to support the theorem with transistor level simulation results using several benchmark circuits.

Chapter 4

Scaling Supply Voltage to Reduce Periodic Clock Test Time

4.1 Low Voltage Tests

Testing at low voltage has several advantages. Hao and McCluskey [31] have shown that manufacturing defects such as interconnect bridging and gate-oxide shorts become more visible (testable) at reduced voltage. Such defects are the main causes for early life failures and reliability issues in circuits but they often escape the test at nominal voltage [18,19,31]. When the voltage is reduced, the resistance of the short does not change and the voltage drop across these resistive shorts becomes high. According to Chang and McCluskey [18,19] the voltage at which these defects are detected lies between $2V_{TH}$ to $2.5V_{TH}$. Roehr [49] indicates that for a reasonable yield, the voltage can be obtained through statistical analysis of min-VDD tests on a large sample of chips. Reducing power supply has a quadratic effect on the dynamic power dissipation, hence it is an attractive option in testing, especially during scan shift operation [24]. For instance, a test pattern set that causes a lot of signal transitions in the device under test (DUT), due to random fill to obtain better fault coverage with fewer vectors, can perform the test at lower power supply voltages and avoid the power dissipation to exceed the rated power for the DUT.

A cited disadvantage of reduced voltage testing is the possible change in critical paths [18], which can force an increase in the test clock period. Qian *et al.* [46] have suggested novel timing tests as an alternative solution to the conventional logic tests to identify gate oxide defects at very low power supply.

4.2 Reduced Supply Voltage Test

As indicated in Section 4.1, testing at low voltages has its advantages and disadvantages. It was mentioned in Section 3.1 of Chapter 3 that the speed of a test is constrained by power dissipated by the DUT during test and the structural delay of the DUT. With regards to power, reducing the power supply has significant advantage over lowering the test power. In fact, even slightly lowering the voltage can have significant reduction in dynamic power dissipation and even more reduction in gate oxide and sub-threshold leakage power dissipation [35]. With respect to test time reduction, reducing power could enable us to increase the speed of testing, thus maintaining the same power dissipation. However, by reducing the supply voltage the gates switch slowly, thus increasing the critical path delay and sometimes a change in critical path. Hence, the question arises, how low can the voltage be reduced? In this section we will examine the lowest possible voltage without changing the critical path.

The operational speed of a circuit is characterized by the time taken for a signal to propagate from one register to the next through a combinational path. The accumulated delays of individual gates in a path through which the signals propagate determine the total delay of that path. The path that has the longest delay becomes the *critical* path, and any path with a delay less than the critical path is considered as a *non-critical path*. The propagation delay of a gate represents the time to charge and discharge the load capacitor. When the gate switches, it operates in the saturation region and the drain current is directly proportional to the square of the difference in gate-source voltage and the threshold voltage. More generally, in the region of saturation, the drain current can be shown to be directly proportional to $(V_{GS} - V_{TH})^{\alpha}$ [51], where α is the velocity saturation index. The relation between gate delay and supply voltage is shown quantitatively by Sakurai and Newton [51] and by Nose and Sakurai [43]. A simplified proportionality relation between delay and supply voltage is given by Sakurai [50] and is shown below,

$$t_d \propto \frac{K \times V_{DD}}{(V_{DD} - V_{TH})^\alpha} \qquad (4.1)$$

According to Sakurai and Newton [51] the velocity saturation index α ranges from 1 to 2 based on the channel length. Several methods [14, 51] can be used to find a value for α. For the work presented in this thesis, the value of α is found to be near 2. However, the experiments can be performed for any value between 1 and 2 based on the available technology.

To determine the accuracy of the delay calculated using equation (4.1), the delay obtained by triggering the critical path of a DUT can be compared with the calculated delay value using equation 4.1. In this experiment, the s298 ISCAS'89 benchmark circuit is synthesized using $180nm$ CMOS technology and we assume that the test is not power constrained, i.e., the test is only limited by the structural delay of the circuit. It was observed that the critical path determined by the Leonardo Spectrum [7] static timing analysis (STA) tool was a false path and hence a path was chosen between the two registers of the critical path. Using an ATPG tool, such as Mentor graphics Fastscan [5], a path delay vector set was obtained for a path with 6 out of 7 gates specified in the critical path. The initial path delay, measured using SPICE, was used to calculate the value of the constant K in the equation (4.1). With an assumption that the critical path will not change as the voltage reduces, the value for the delay was calculated using equation (4.1) for every voltage reduced from the nominal voltage of 1.8V down to 0.6V in steps of 0.1V. The new value was used as the new clock period and the SPICE simulation was performed again. If the expected transitions occurred in the path chosen, then the path delay was noted for that voltage. If the expected transitions did not occur, then the test clock period was increased and the test was repeated.

Figure 4.1 shows the comparison of the calculated and measured values for minimum test time at each voltage reduction. The measurement assumes that the test is only structure constrained and hence the test runs at the functional speed. From the results it was observed that the delay calculated using the α power law equation (4.1) was in correspondence with
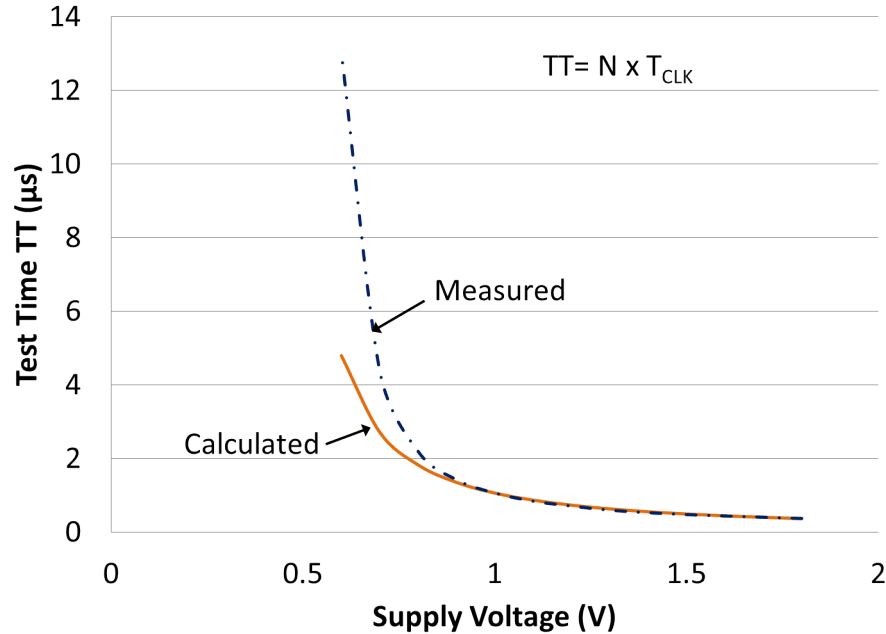
Figure 4.1: Comparison of the test time measured using SPICE simulations with the delay calculated using α power law using s298 ISCAS'89 benchmark circuit. The test clock period is chosen as the functional period assuming that the test is not power constrained.

the measure values while reducing the supply voltage by up to half of the nominal supply voltage, beyond which the clock period had to be increased to obtain the expected results. So the experiment provides evidence that it is safe to assume that the critical path will not change for small reductions in supply voltage and for a given value of K and α the delay can be found using the approximation in equation (4.1). As it will be described in the following sections, this conclusion helps to obtain the optimum voltage for test time reduction in periodic clock test.

4.3 Optimum Supply Voltage

4.3.1 SPICE Experiment

In Chapter 3 it was stated that in a power constrained test, the test clock period is limited by the maximum allowable power of the circuit. In general test clock period can be

related as

$$P_{MAXtest} = \frac{E_{MAXtest}}{T_{power}}$$

$$\Rightarrow T_{power} = \frac{E_{MAXtest}}{P_{MAXtest}} = \frac{C_L \times V_{DD}^2}{P_{MAXtest}} \tag{4.2}$$

where T_{power} is the test clock period at a given peak power limit $P_{MAXtest}$, $E_{MAXtest}$ is the maximum energy dissipated by any clock cycle during the entire test, and C_L is the total switched capacitance in clock cycle that consumes most energy due to rising signal transitions. Since the technique is implemented for stuck at fault tests, the signal transitions in both scan shift and capture are accounted for to find the cycle with maximum switching activity.

The maximum allowable power of the device is usually the maximum power dissipated during its functional operation for which the hardware is designed. Hence in a power constrained tests, the maximum allowable power during test must not exceed the maximum power dissipated during functional operation, i.e. $P_{MAXtest} \leq P_{PEAKfunc}$. The power constrained test clock period T_{power} is,

$$T_{power} \geq \frac{C_L \times V_{DD}^2}{P_{MAXfunc}} \tag{4.3}$$

The leakage power dissipation depends on the current flow in the circuit when it is in the steady state. Hence the power dissipation due to leakage will remain the same during test as during functional operation [29]. Since the strategy is to lower the voltage and shrink the test clock period, the net effect will be to reduce the leakage power as well as leakage energy per cycle during the test. In the following analysis, the dynamic power, which is a function of both signal transitions and short circuit power, is considered to dominate the total power dissipation.

In this section we aim to find the best voltage at which a power constrained test can run with minimum test time without exceeding the peak power or violating the critical path delay constraint of the circuit. As mentioned in the previous sections the test time can be

reduced while limiting the power by reducing the supply voltage. However, there exists a point where the voltage will not be enough to charge the output load capacitance within the right amount of time. Thus the value at the output will be wrong. At this point the circuit is considered structure constrained and the test time is now dependent on the critical path delay of the circuit. The gate delay of the circuit can be characterized by using the α power law delay model in equation (4.1) proposed by Sakurai [51] [50]. This allows expressing the smallest structure constrained test clock frequency as,

$$T_{critical} \geq K \times \frac{V_{DD}}{(V_{DD} - V_{TH})^{\alpha}} \tag{4.4}$$

where K is a proportionality constant, which depends upon the critical path structure, timing margin, etc., and α is the velocity saturation index. If the test is only structure constrained then the total test time can be given as

$$TT_{structure} = N \times T_{critical} \tag{4.5}$$

where $TT_{structure}$ is total test time using structure constrained clock period T_{CLK} in an N cycle test.

To minimize the test time we find the smallest test clock period, T_{opt}, that will satisfy the power constraint (4.3) and critical path constraint (4.4). Thus, at any given voltage the optimum test period is given by

$$T_{opt} = \max\{\min T_{power}, \min T_{critical}\} \tag{4.6}$$

then the minimum test time will be,

$$TT_{min} = max(TT_{power}, \ TT_{structure}) \tag{4.7}$$

The optimum voltage at which a power constrained test will run with the fastest clock and in least overall test time will be the voltage at which both TT_{power} and $TT_{structure}$ are equal.

An experiment to identify the optimum voltage was performed on the s298 sequential benchmark circuit. In order to observe the peak power dissipated by the circuit during test, as well as the critical path delay, scan vectors generated by the ATPG for stuck-at fault tests were combined with the vectors generated to trigger the critical path. The critical path obtained by the static timing analysis (STA) tool for the DUT was found to be a false path and hence the next longest path was found to be having a delay of 0.77ns, including the setup time. This path was considered in the experiments and correspondingly the value for K was calculated. Simulations were performed using Nanosim SPICE simulator [4] tool by varying the voltage from 1.8V down to 0.6V in steps of 0.1V. The peak energy dissipated and the critical path delay were measured at each voltage point. Using equations (4.2) and (4.5), the values for test times were calculated and the maximum of the two values is the total time as given by equation (4.7).

Figure 4.2 shows the graph for the simulated and calculated results to find the optimum voltage points. The point labeled minimum V_{DD} is the cross point at which the power-constrained test clock period and the critical path delay of the circuit are approximately the same. Reducing the voltage beyond this point increases the test time as the critical path delay increases above the power-constrained clock period. Hence, the test must slow down. The dotted line, labeled "measured", shows the result from simulation. The best voltage is 1.07V with a total test time of approximately $1\mu s$ and a test clock frequency of 532MHz is the same as the functional frequency. The minimum of the "measured" curve exactly coincides with the cross-over point of the two calculated curves from equations (4.2) and (4.5). This validates the calculation of the best supply voltage for minimum test time is obtained from equation (4.7). Thus, the SPICE simulation, which is expensive for a large circuit, is not required for many voltages. Once E_{Max} and t_{pd} have been obtained at one
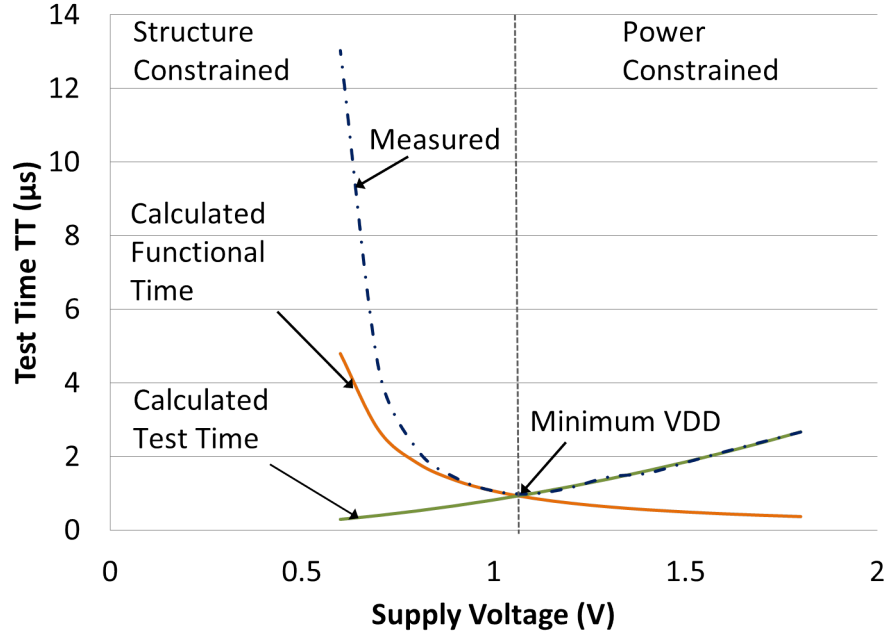
Figure 4.2: Simulation and experimental test time plots to find the optimum voltage for s298 benchmark circuit.

voltage (say, nominal voltage or 1.8V in our example), both equations (4.2) and (4.5) can be characterized. The optimum voltage can also be obtained directly for a given value of K, α, switched capacitance C_L and the rated power for the device $P_{PEAKfunc}$.

4.3.2 Polynomial Equation to Obtain Minimum Supply Voltage

From equation (4.3) we observe that as the voltage is reduced T_{power} reduces. But from equation (4.4) $T_{critical}$ increases as the voltage is reduced. Thus if we plot equations (4.3) and (4.4) with respect to voltage, as the voltage reduces the two functions will cross each other at a point. The voltage V_{DDopt} at which the test time is minimum must satisfy:

$$T_{opt} \;=\; T_{power} \;=\; T_{critical} \tag{4.8}$$

This relation was evident in Figure 4.2. To obtain a straight forward solution for the optimum voltage problem we make the following assumptions in our analysis:

1. Variation in threshold voltage V_{TH} due to changes in supply voltage is not drastic and V_{TH} is assumed to be constant for the supply voltage interval of interest.

2. The critical path remains unchanged as supply voltage changes. Thus, the value of K is assumed to be independent of the supply voltage.

We equate the right hand sides of equations (4.3) and (4.4) according to (4.8) and substitute $V_{DD} = V_{DDopt}$:

$$T_{opt} = \frac{C_L \times V_{DDopt}^2}{P_{MAXfunc}} = \frac{K \times V_{DDopt}}{(V_{DDopt} - V_{TH})^\alpha} \tag{4.9}$$

We make two useful observations about the test conducted at supply voltage V_{DDopt} that satisfies equation (4.9):

- For shortest test time, the test clock period T_{opt} is the minimum allowed by the critical path delay at V_{DDopt}.

- The maximum power for a test cycle, $C_L \times V_{DDopt}/T_{opt}$, equals the peak power specification $P_{MAXfunc}$.

These observations help us experimentally find the optimum test time parameters. To analytically obtain V_{DDopt} we derive a polynomial equation:

$$V_{DDopt}^{\frac{1}{\alpha}+1} - V_{TH} \cdot V_{DDopt}^{\frac{1}{\alpha}} - \left(\frac{K \times P_{MAXfunc}}{C_L}\right)^{\frac{1}{\alpha}} = 0 \tag{4.10}$$

or

$$V_x^{\alpha+1} - V_{TH} \cdot V_x - \gamma = 0 \tag{4.11}$$

where $V_x = V_{DDopt}^{\frac{1}{\alpha}}$ and $\gamma = \left(\frac{K \times P_{MAXfunc}}{C_L}\right)^{\frac{1}{\alpha}}$

Since $\alpha = 1$ when the device is completely velocity saturated and $\alpha = 2$ if the device has no velocity saturation [50, 51], equation (4.11) is a polynomial of degree three or lower,

which is solvable. Knowing the voltage V_{DDopt} for the shortest test time, the corresponding shortest test clock period can be obtained from (4.9) as,

$$T_{opt} = \frac{C_L \times V_{DDopt}^2}{P_{MAXfunc}} \tag{4.12}$$

The optimum test frequency is then

$$f_{opt} = \frac{1}{T_{opt}}$$

Here f_{opt} is the highest power constrained test frequency.

The polynomial equation (4.11) can be solved using any mathematical solver such as MATLAB. The values for K, α, $P_{MAXfunc}$ and effective maximum switched load capacitance C_L during any test cycle can be obtained through simulation at nominal voltage.

4.3.3 Solving for V_{DDopt}, f_{opt} and TT_{opt}

The optimum voltage V_{DDopt} will be the minimum voltage at which the test can run fastest without exceeding the maximum power limit of the device and without being structurally constrained due to an increase in the critical path delay because of scaling the supply voltage.

Let us solve for the optimum voltage V_{DDopt} using equation (4.11) for the s298 IS-CAS'89 sequential benchmark circuit synthesized for scan test in TSMC 180nm technology. The DUT is synthesized using Mentor Graphics Leonardo Spectrum tool [7]. The nominal voltage for this technology is 1.8V and the threshold voltage is 0.39V. The critical path delay obtained through static timing analysis (STA) using Leonardo Spectrum [7] was 1.5ns or 666MHz. To find V_{DDopt} using equation 4.11 we need values for the proportionality constant K, maximum allowable power limit $P_{MAXfunc}$ and the maximum switched capacitance C_L, that will determine γ.

The alpha power law model given in equation (4.4) is an approximate method to find the critical path delay for any circuit for a given supply voltage and threshold voltage. The value for α, the velocity saturation index, in equation (4.4) ranges between 1 and 2 [50, 51] and can be found using methods described in [14] and [51]. It can also be obtained from a simple curve fitting to delay values at different voltages for a chain of inverters. In our experiment for 180nm technology, the value for α was found to be 2 using the latter method.

We can now rewrite equation 4.4 to find the value for K as follows:

$$K = T_{critical} \times \frac{(V_{DD} - V_{TH})^\alpha}{V_{DD}}$$

To trigger the critical path for observing the delay we obtained a path delay vector set using Mentor Graphics Fastscan [5] for the path used in section 4.3.1. The STA for this path was given as 0.77ns including setup time. Post synthesis timing simulation of the DUT using Mentor Graphics Modelsim with a period of 0.77ns, was found to pass the test. The value for the proportionality constant K for this path was calculated to be 0.85. The value of K depends on the critical path of the circuit, hence based on assumption 2 in Section 4.3.2, the value of K is kept constant.

The maximum allowable power limit for a circuit is normally given as a specification in the datasheet. In a power-constrained test the power dissipated during test must be kept under that limit. In the absence of a known power limit for our DUT, we determined the maximum allowable power by simulating 1,000 random patterns in functional mode and measured the power dissipated per cycle using Synopsys Nanosim transistor level simulator at the nominal voltage of 1.8V and a frequency of 500MHz. The maximum power over the entire functional operation is assumed to be the upper bound for the power during test. For the DUT in this example the upper bound was measured as 1.2mW.

The next unknown in equation (4.10) is the maximum switched capacitance C_L. It is defined as the effective switched load capacitance of the circuit during maximum rising signal

Table 4.1: Parameter values for s298 benchmark synthesized in 180nm CMOS technology ($V_{DD} = 1.8$V, $V_{TH} = 0.39$V, Critical Delay $= 0.77$ns).

Parameter	Value
$P_{MAX(func)}$	0.0012W
C_L	2.04pF
K	0.85
α	2

transitions caused by any test cycle. Energy consumed during that cycle is,

$$E_{MAXtest} = C_L \times V_{DD}^2$$

where C_L = maximum switched capacitance of the test pattern that causes the most rising signal transitions. Therefore,

$$C_L = \frac{E_{MAXtest}}{V_{DD}^2}$$

The value of $E_{MAXtest}$ can be obtained by simulating the test patterns at any arbitrary (slow) frequency f and measuring the maximum power $P_{PEAKfunc}$ for a clock cycle, i.e.,

$$E_{MAXtest} = \frac{P_{PEAKfunc}}{f}$$

where f is any frequency slower than the maximum allowed by the critical path.

Once the value for $E_{MAXtest}$ is obtained, C_L can be obtained from the equation above. For the DUT in this example the value for C_L is obtained as 2.04pF. Table 4.1 summarizes the values obtained in this manner. Substituting these values into the expression for γ following equation (4.11) we get $\gamma = 0.7158$ and the equation becomes,

$$V_X^3 - 0.39V_X - 0.7158 = 0$$

We use a numerical solver in MATLAB to find the roots for V_X. We obtain 3 roots, two complexes and one real. Since the supply voltage is a real number, it is logical to consider only the real root and discard the two complex roots. Solving for V_{DDopt} from V_X we get
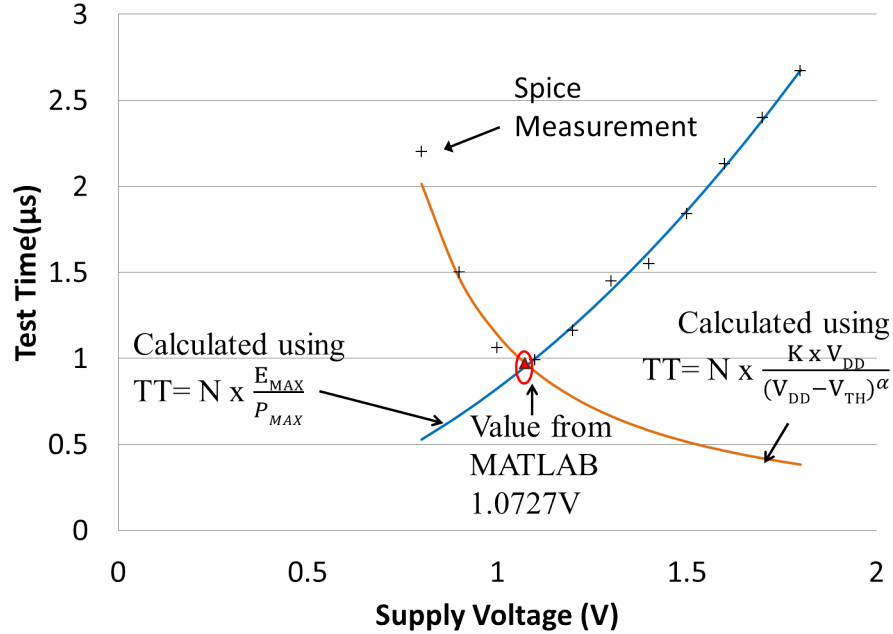
Figure 4.3: Simulated and calculated curves using test period and functional period at various voltages. The direct approach using MATLAB (circled) matches the cross point of the curves obtained analytically using the periods calculated from equations (4.3) and (4.4) and the results obtained from SPICE ("plus" data points) in [66].

$V_{DDopt} = 1.0727$V. This is the optimum voltage at which the test can run at maximum speed would better. Since at this voltage the test is still power constrained, we can calculate T_{opt} from equation (4.3) where $T_{test} = T_{opt}$ which gives us $T_{opt} = 1.95ns \Rightarrow f_{opt} \approx 512$MHz.

The total test time for the DUT can be calculated as

$$TT_{opt} = N \times T_{opt}$$

where N is the total number of test cycles. For the DUT in this example $N = 498$, hence the total test time is $TT_{opt} = 0.971\mu$s.

Figure 4.3 shows the calculated test time plots using equations (4.3) and (4.4), at various voltages for the s298 benchmark circuit. The circled data point indicates the optimum voltage value obtained from the numerical analysis. The values measured from SPICE at various voltages in Section 4.3.1 are shown in the curve "Spice Measurement". It is readily observed

Table 4.2: Optimum V_{DD} for reduced test time of ISCAS'89 benchmark circuits.

Circuit name	Total scan test cycles	Peak per cycle power (W)	Nominal voltage (1.8V) test		Optimum voltage test			Test time reduction (%)
			Test freq. (MHz)	Test time (μs)	Supply voltage (Volts)	Test freq. (MHz)	Test time (μs)	
s298	450	0.0012	216.3	2.08	1.1	562	0.8	61.5
s298	498	0.0012	187	2.66	1.07	512	0.971	63.0
s298	540	0.0012	184	2.92	1.07	529	1.02	65.0
s382	704	0.0029	292	2.41	1.44	457	1.54	36
s713	810	0.0015	137.28	5.9	1.33	249.23	3.25	45.0
s1423	6975	0.0045	135.9	51.3	1.6	148.4	47.0	13.0
s1423	6975	0.0030	90.58	77	1.49	132.1	52.7	31.5
s13207	62237	0.0213	168	369	1.62	208.8	298	19.2
s15850	101708	0.240	67.35	1510	1.30	128.9	789	47.7
s38584	224113	0.350	88.54	2531	1.30	172.3	1300	48.6

from the graph that the numerical analysis to obtain the optimum voltage is in accordance with the SPICE measurement.

4.4 Results

The procedure described in this section was repeated for several ISCAS'89 benchmark and the results are tabulated in Table 4.2. It gives the results based on Nanosim transistor level [4] simulation. The values slightly differ from [66]; the difference is the number of cycles and the peak power used. The vectors and the power values are chosen such that they are consistent throughout this document. Though the results vary, for the given peak power and vectors, both results are valid. In the SPICE simulations, the optimum voltage is obtained through transistor level simulations for closely spaced voltages to find the point before the circuit becomes structure constrained. In Table 4.2 it was observed that, if the value for the chosen $P_{PEAKfunc}$ is closer to the power dissipated during test, then the reduction obtained in test time using reduced voltage is not much. This is because, when the power dissipated by the test is closer to the rated power, the test runs at a speed closer to the functional speed and any reduction in supply voltage makes the test structure constrained. This is

seen in circuits s1423 and s15850. On the other hand, if the power dissipated during test is significantly greater than the rated power then significant reduction in test time is observed, as in s298 and s382. Most circuits today have the test power $2\times$ the functional power in CPUs [47] and $4\times$ the functional power in GPUs [69], hence significant reduction in test time is attainable.

Using the polynomial method explained in Section 4.3.2, the optimum voltage was obtained analytically for the same benchmark circuits used in the SPICE experiments described above. The results shown in Table 4.3, correlate well with the simulation results in Table 4.2. Thus knowing the design specifications such as, the velocity saturation index α, proportionality constant K, maximum allowable power $P_{PEAKfunc}$, and the maximum switched capacitance C_L obtained from the maximum energy cycle, using the polynomial equation (4.11) the optimum voltage can be obtained in less time. Note that to solve the polynomial equation (4.11) for a given $P_{MAXfunc}$, we need to simulate the circuit only once at the nominal voltage to find the constants. For instance if the optimum voltage using SPICE simulations is achieved after 10 simulations, the time taken to obtain the optimum supply voltage and test time using the numerical analysis, is reduced by $\frac{1}{10}$.

It should be noted that since the test patterns generated for periodic test was able to find all faults in the optimum V_{DD} tests, the defect and fault coverage for stuck-at tests should be the same as in periodic test at nominal voltage.

4.5 Peak Power and Critical Path Frequency Measurements

The scenario described in this chapter was used to perform experiments on a FPGA configured with a benchmark circuit. The motive of this experiment is to experimentally observe the effect of scaling supply voltage on power and frequency. Due to the absence of a method to measure power on the fly using the Advantest T2000GS ATE, a bench test equipment by National Instruments [2] is used.

Table 4.3: Analytically obtained V_{DDopt} and f_{opt} for minimum scan test time of ISCAS'89 circuits in 180nm CMOS ($\alpha = 2$, $V_{TH} = 0.39$V).

Circuit name	Propor- tionality constant K ($\times 10^{-9}$)	Maximum switched capaci- tance C_L (pF)	Total scan test cycles N	Peak per cycle power $P_{MAXfunc}$ (W)	Nominal voltage 1.8V test		Optimum voltage test			Test time reduc- tion (%)
					Test freq. (MHz)	Test time (μs)	Supply V_{DDopt} (Volts)	Test freq. f_{opt} (MHz)	Test time (μs)	
s298	0.85	1.76	450	0.0012	216.3	2.08	1.1	562	0.8	61.5
s298	0.85	2.04	498	0.0012	187.0	2.66	1.073	512	0.971	63.0
s298	0.85	2.06	540	0.0012	184.0	2.92	1.07	529	1.02	65.0
s382	1.75	3.07	704	0.0029	292.0	2.41	1.44	434	1.54	36.0
s713	2.79	3.36	810	0.0015	132.28	5.90	1.34	249.23	3.25	45.0
s1423	6.38	10.22	6975	0.0045	135.9	51.30	1.66	158.5	44	14.2
s1423	6.38	10.22	6975	0.0030	90.58	77.00	1.49	131.7	52.9	31.2
s13207	4.64	38.9	62237	0.0213	168	369	1.62	208.8	298	19.2
s15850	5.12	109	101708	0.0240	67.35	1510	1.31	128.9	789	47.7
s38584	4.03	156.8	224113	0.0350	88.54	2531	1.31	172.4	1300	48.6

4.5.1 Hardware Setup

National Instruments ELectronic Virtual Instrumentation Suite II+ (NI ELVIS) [2] serves equally well as a bench-top test instrument and prototyping board. We used NI ELVIS to measure peak power per cycle and the maximum circuit test frequency for a given supply voltage. The circuit used for the measurements was the Altera DE2 Field Programmable Gate Array (FPGA) board [12]. The DE2 board houses an Altera Cyclone-II 2C35 FPGA. Benchmark circuit s298 was programmed on this FPGA. Figure 4.4 shows the test setup for the power and maximum test frequency measurements. The DE2 board was powered through the variable power supply available on NI ELVIS. For the s298 circuit, all inputs and outputs, including scan-in and scan enable, were configured as external pins of the DE2 board. These pins were in turn connected to the programmable digital Input/Output (IO) pins available on NI ELVIS. The test program was written in LabVIEW [1] on a PC, and the test patterns were sent to NI ELVIS through a Universal Serial Bus (USB) connection. Stored test patterns were then applied to the circuit under test (in our case the DE2 board) from NI ELVIS, and the response was captured and compared for every test vector.
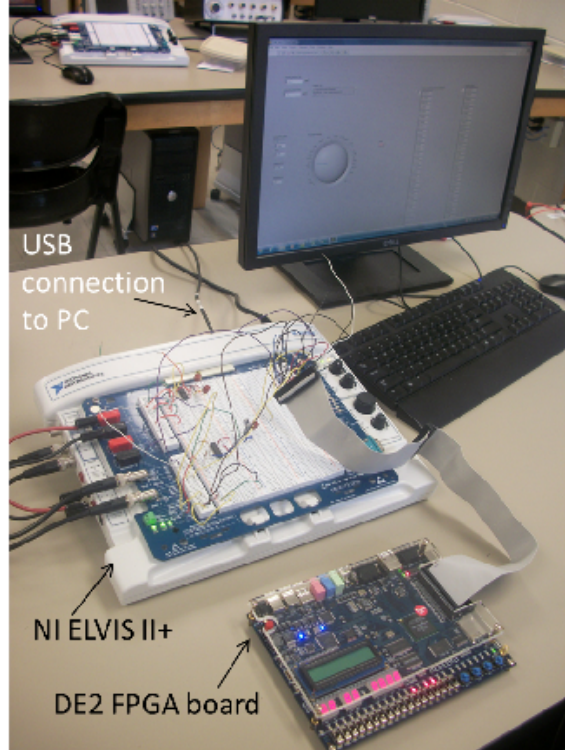
Figure 4.4: Test setup for measuring peak power per cycle and maximum test frequency for an Altera DE2 FPGA board (with all its peripherals) using the NI ELVIS II+ bench-top prototyping board.

4.5.2 Peak Power and Frequency Measurements

Figure 4.5 shows the peak power per cycle and maximum test frequency, plotted as a function of the supply voltage. As the DE2 board comprises a number of peripherals, like the seven-segment display, several LEDs, several different IO drivers, etc., the absolute power numbers measured from the supply voltage and current product will be dominated by these peripheral components rather than the actual circuitry on the FPGA. We, therefore, corrected the measured supply-power by removing the steady state power component in each cycle. The remaining power component, which is the switching (or dynamic) power, is presumably dominated by CMOS circuitry on the FPGA. The dynamic power curve is shown in blue with circular markers at the measured voltage points on the graph in Figure 4.5. We found that the peak dynamic power per cycle increases as a square of the supply voltage in the range of 1.8V–5.4V, well in agreement with theory. For supply voltages below 1.8V, even very

51
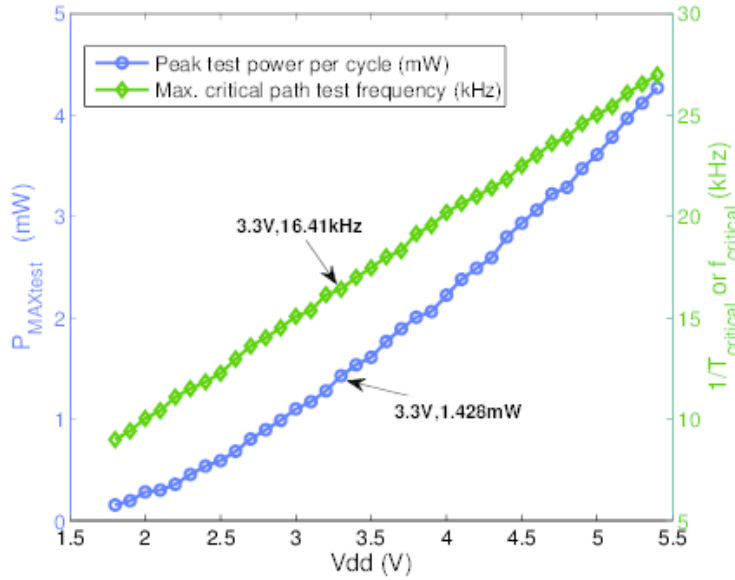
Figure 4.5: Measured values of maximum power consumed per cycle (in blue) and maximum test frequency (in green) plotted as a function of the supply voltage for the Altera DE2 FPGA board tested using NI ELVIS II+ bench-top prototyping board. Switching power is dominated by the CMOS circuitry contained on the board. The FPGA itself is programmed with the function of s298 benchmark with scan.

low test frequencies result in erroneous outputs, which is plausible since the nominal voltage specified for the board is 3.3V, and one or more of the IO drivers may not be operational at voltages below 1.8V. Even though the commonly used nominal supply voltage for CMOS logic circuits at the 90nm technology node is about 1.2V, we could only control the supply to the DE2 FPGA board in the range 1.8V to 5.4V. Because these tests are destined for s298 circuit implemented on the FPGA chip and were applied through edge connectors and other logic on the board, the whole process ran essentially like a board test rather than a chip test.

The maximum test frequency, in practice, is limited by the structural critical path delay of the circuit; however, in the current setup, it is limited by the speed of the IO drivers on the FPGA board and the maximum allowable sampling frequency of NI ELVIS. The maximum test frequency at each supply voltage also corresponds to frequency at which maximum power per cycle is dissipated. This curve is shown in green with diamond markers at the

measured voltage points in Figure 4.5. The maximum operating frequency at each supply voltage step was found by starting at an initial frequency and increasing it until the point where the circuit output no longer matches the ideal output. The highest frequency at which the circuit output matches the ideal output is taken as the peak operating frequency.

4.5.3 Minimizing Test Time for Given Peak Power Limit

For a circuit under test with a given peak power limit, $P_{MAXfunc}$, the experimental data of Figure 4.5 readily gives both the supply voltage V_{DDopt} and test frequency f_{opt} that minimize the test time of the power constrained test. This is done by using the two observations made following equation (4.9). For example, suppose we have a peak power limit $P_{MAXfunc} = 0.5$mW. At the nominal supply voltage of 3.3V, the test power dissipation is 1.428mW and maximum structural clock frequency is 16.4 kHz. To keep the test power under 0.5mW, the test must be run at $16.4 \times 0.5/1.428 = 5.74$kHz. From Figure 4.5, for $P_{MAXtest} = P_{MAXfunc} = 0.5$mW, we should lower V_{DD} to $V_{DDopt} = 2.5$V, which gives a test frequency of $f_{opt} = 12.5$kHz. Thus, test time will be reduced by a factor $5.74/12.5 = 0.46$.

Chapter 5

Dynamic Scaling of Test Clock Period

5.1 Aperiodic Clock Test

In Chapter 4 it was proposed that, for a periodic clock test where the test clock period is held constant throughout the test, the test time can be reduced by choosing an optimum supply voltage that is lower than the nominal supply voltage. While using a periodic clock test, at any voltage the dynamic power dissipation for a given test pattern set is not constant and randomly varies throughout the test, based on the switching activity caused by the test patterns during each cycle. If every cycle in a periodic clock test can be modified such that the power remains constant and within the allowed limit for the entire test by choosing unique clock periods, then it will be possible to reduce test time significantly. This method of testing is termed as the *aperiodic clock* test, where the period of each cycle can be different from the period of its neighboring cycle. This was briefly described in Section 3.2.2. In an aperiodic clock test, it is possible for every clock cycle in a test to be either structure constrained or power constrained. The test clock period of an aperiodic test can be given by,

$$T_i \;=\; max\{T_{structure}, \frac{E_i}{P_{PEAKfunc}}\} \tag{5.1}$$

For the stuck-at fault tests, the capture cycle will also be at the same clock period as the scan shift cycles; hence the period for the capture cycle can also be reduced based on the power dissipated during that cycle. When considering delay testing, based on whether we use single clock capture (Launch-on Shift) or double clock capture (Launch-on Capture), test cycle period for the shift cycles can be modified and the capture cycles can be left unaltered, since the capture cycles uses functional clock period to identify delay faults.

Using equation (5.1) the total test time for an aperiodic clock test can be given as,

$$TT_{asynch} = \sum_{i=1}^{N} max\{T_{structure}, \frac{E_i}{P_{PEAKfunc}}\} \qquad (5.2)$$

where TT_{asynch} is the aperiodic test time for a test with N cycles.

5.1.1   A Circuit Example

We examine the proposed aperiodic clock test using an ISCAS'89 sequential benchmark circuit. For simplicity, let us choose the s298 benchmark circuit that contains 14 flip-flops, 3 primary inputs and 6 primary outputs. The circuit is synthesized using Mentor Graphics Leonardo Spectrum [7] with TSMC 180nm technology. The Spectrum tool also provides the critical path delay via static timing analysis (STA) of the circuit. More accurate critical path delay information can be obtained after the routing of the circuit with inserted scan chains. Statistical static timing analysis (SSTA) can also be used to consider process variations during delay calculations [9,28]. All flip-flops in the circuit were daisy chained to form a single scan chain, using Mentor Graphics DFT Advisor. Once the scan chain was inserted, a set of deterministic ATPG test vector patterns for stuck-at faults were generated using Mentor Graphics Tessent Fastscan [5]. A transistor level simulation was performed using Synopsys Nanosim [4] at the nominal voltage of 1.8V. The transistor level description of the netlist was generated using Mentor Graphics Design Architect and the SPICE file was imported into Nanosim. Using Nanosim the energy dissipated per cycle during the entire test was measured. Based on the report obtained through transistor level simulation, we determined the test period for each cycle. For each cycle the test period would be constrained both by structure, as given by STA, and by maximum rated power. The maximum rated power depends on the functional characteristics, physical design, packaging, etc., and is part of the specification of the circuit. In the absence of available data, for our analysis we measured the maximum power in functional mode through simulation of 1,000 random vectors, which
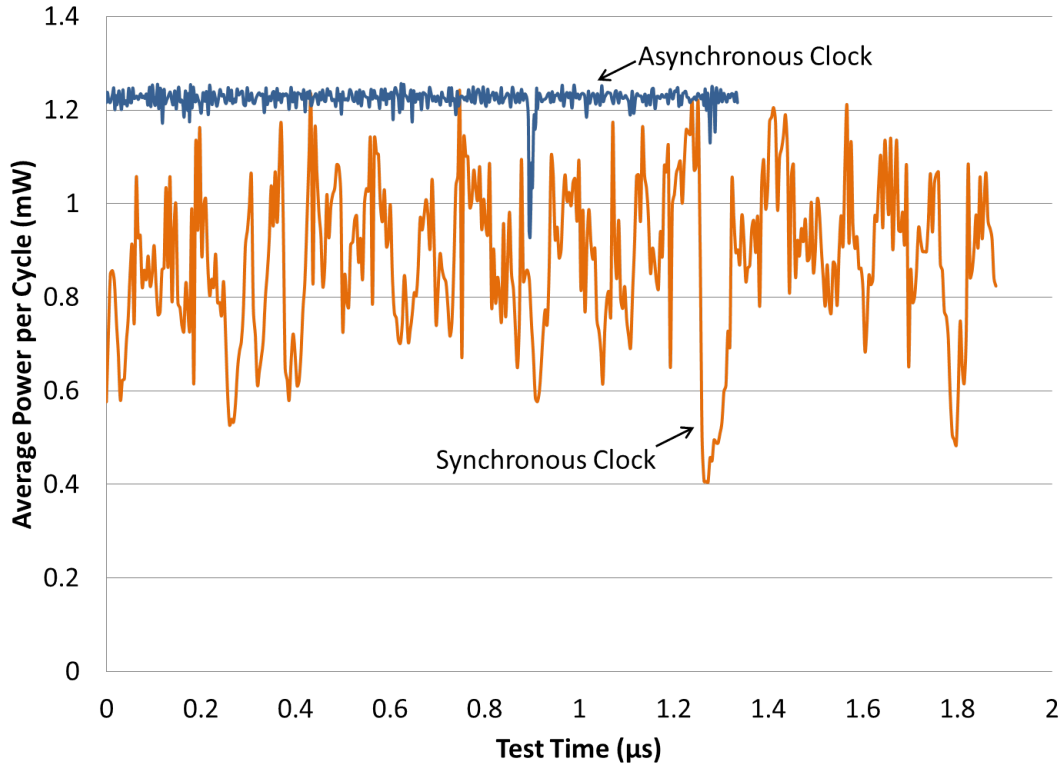
Figure 5.1: Periodic and aperiodic clock simulation of 450-cycle scan test of ISCAS'89 bench-mark circuit s298. Periodic test clock frequency is 240MHz and test time is $1.87\mu s$. Aperiodic clock test time is $1.31\mu s$.

was 1.23mW. Once the time period for each cycle was obtained the circuit was simulated again to calculate the power dissipated during each test cycle.

Figure 5.1 shows the simulation results for the s298 benchmark circuit. The plot compares the test performed using periodic (fixed) and aperiodic (varying) clock periods. The x-axis shows time as test was run and the y-axis shows the power dissipated during each test cycle. As observed from the figure, when a periodic clock is used the power dissipated during each cycle does not reach the maximum rated power at most cycles. Hence the test clock periods for cycles dissipating less power can be safely reduced until the cycle power is close to the rated power. This effect is seen in the simulation results using the aperiodic clock. When the particular cycle dissipates low power, the period is reduced such that the power for that cycle increases to a value closer to the rated power. However, while trying to

do so if the period becomes shorter than the critical path delay then the period is set to the value of the critical path delay. Thus, we ensure that the power constrained period is small without violating any timing constraints. This limitation on the minimum period will force the circuit to dissipate significantly less than the rated power and hence the "dips" in the aperiodic clock plot.

In this example, the total test time with the periodic clock was $1.87\mu s$ and the test time with the aperiodic clock was $\approx 1.31\mu s$. This represents a reduction of 30%. Greater reduction is achievable if the average power of the entire test is significantly lower than the maximum power. Thermal analysis [70] and characterization of test power can be performed to determine a safe operating point for testing and the test can be modified appropriately, such that if the thermal issues are a concern, the method can be used at the safe operating point.

5.1.2 Simulation Results

Table 5.1 shows the simulation results for several ISCAS'89 benchmark circuits using the procedure described in Section 5.1.1. All circuits were synthesized using TSMC 180nm technology. The nominal supply voltage for this technology is 1.8V. For s298 three different sets of test patterns were used for each circuit to observe the effect of test power while reducing test time. This is discussed later in this section.

Column 2 of Table 5.1 shows the number of scan test clock cycles used for each circuit. This is determined by the number of flip-flops in the scan chain and the total number of vectors, along with one cycle per vector for capture. Since vectors were generated for stuck at faults, only one capture cycle is used for response capture at the end of each test. The maximum rated power ($P_{PEAKfunc}$) shown in column 3 is normally given in the circuit datasheet. However, for these benchmark circuits we obtained a value by simulating the DUT in functional mode at its fastest frequency for 100 random vectors. In some cases the power value thus obtained might be closer to the power calculated during test, but employing an

Table 5.1: Scan test time for ISCAS'89 circuits in TSMC 180nm technology.

Circuit name	Total scan test clock cycles	Per cycle peak power $P_{PEAKfunc}$ (W)	Max per cycle Energy $E_{MAX(test)}$ (pJ)	Total energy of test E_{TOTAL} (nJ)	Periodic clock Freq-uency (MHz)	Test time (μs)	Asynch-ronous clock test time (μs)	Test time reduction %
s298	450	0.0012	5.71	1.83	216.34	2.08	1.48	28.5
s298	498	0.0012	6.61	1.83	187.2	2.66	1.49	44.0
s298	540	0.0012	6.68	1.89	184.9	2.92	1.54	47.2
s382	704	0.0029	9.96	4.69	100	2.41	1.62	32.7
s713	810	0.0015	10.9	4.22	137.28	5.9	2.83	52.0
s1423	6975	0.0045	33.14	166.68	135.96	51.3	39.8	22.4
s1423	6975	0.0030	33.14	166.68	90.58	77	55.6	28.0
s13207	62237	0.0213	126.3	660	168.66	369	312.2	15.0
s15850	101707	0.0240	213.8	2610	67.35	1510	1088.0	27.8
s38584	224112	0.0350	609.8	9470	88.54	2531	2101.5	17.0

aperiodic clock to reduce test time can still be shown. Column 4 shows the maximum energy ($E_{MAXtest}$) dissipated due to signal transitions in the clock cycle that consumes the most energy. Column 5 shows the total energy (E_{TOTAL}) consumed by the entire test. These were obtained by simulation as discussed in Section 5.1.1. For the s1423 an additional experiment was performed with a value of 0.030mW, which is less than the simulated peak value, to observe the effect of power on test time reduction without a change in the energy dissipation.

Columns 6 and 7 give the test frequency and test time for the periodic clock test. The periodic clock period T_{POWER} is obtained from equation (3.11), using the data from columns 3 and 4. The test frequency in column 6 is $\frac{1}{T_{POWER}}$. The total test time for the periodic clock, in column 7, is calculated using equation (3.15). Column 8 shows the total test time taken when an aperiodic clock is used and the corresponding test time reduction over that of column 7 for periodic clock is given in column 9.

An interesting observation here is that aperiodic to periodic test time ratio for power constrained testing is the ratio of average energy to the maximum energy per cycle. For example, consider s298 in the first row of Table 5.1. Average energy per cycle is $E_{AVG} = 1.83$nJ$/498 = 4.067$pJ. The ratio $E_{AVG}/EMAX(test) = 4.067/5.71 = 0.71$ is about the

same as the test time ratio 1.48/2.08. In cases where a significant number of clock cycles are structure constrained the test time ratio may move toward unity. If every cycle consumes significantly low energy compared to a few cycles that consume very high energy, then it is possible to achieve a large reduction in test time. This is because, based on equation (5.1) all low energy cycles will only be limited by the critical path delay and only those cycles that consumes high energy will run at the slowest clock period. On the other hand, if the number of cycles consuming very high energy is significantly larger than the number of cycles consuming low energy then the reduction in test time will be less. This effect was examined for the $s298$ circuit in Table 5.1. Using alternative sets of vectors with one test pattern having high energy consuming cycles and the rest of the patterns consuming low energy, the test time reduction improved from 28% to 47% for s298.

Once again, since the test patterns generated for periodic test was able to find all faults in aperiodic test, the defect and fault coverage for stuck-at fault test should be the same as in periodic test.

5.1.3 Test Programming on ATE at Nominal Voltage

Experimental Setup

The aperiodic clock technique was experimentally verified on the Advantest T2000GS ATE at Auburn University. The ATE can be operated at a maximum speed of 250MHz and has 128 bi-directional tester channels. The power supply to the DUT is provided by the ATE through a digital power supply module DPS500mA, which has a power supply range of -2 to $8V$ and a output current range up to 500mA. The test plan is programmed using the native *Open architecture Test system Programming Language*, in short OTPL. Provisions to place a chip on the tester head are available. For our experiments with benchmark circuits, we used a Xilinx Spartan 3 FPGA $XC3S50$ soldered on a printed circuit board. The DUT used for our experiment was the s298 benchmark circuit with daisy chained mux-type scan

flip-flops configured on the FPGA. The FPGA is configured on the run by the ATE using the bit file generated by the Xilinx ISE tool [39].

The ATE has a frame processor and a pattern generator, which are synchronized with the rate generator. The rate generator generates a fixed rate clock pulse and triggers the pattern at the start of each pulse. Based on the waveform set by the frame processor and the corresponding pattern value, the pattern is applied to the DUT mounted on the tester head. The test plan for the FPGA consists of three steps. The first two steps account for the configuration of the FPGA using the ATE. In the first step, the FPGA is powered by the ATE with a supply voltage of 2.5V and the configuration memory is cleared during this process. The second step downloads the bit file generated by Xilinx ISE using a slave serial mode. In this mode, the configuration data is provided through the DIN input pin of the FPGA and clocked externally using the ATE. A successful configuration of the FPGA is indicated by a High output value on the DONE pin. The third step performs the functional test on the DUT now configured on the FPGA.

External Test

The clock period required for the scan-based functional test is determined prior to the external testing. Certain limitations of the tester framework set only allow 4 unique clock periods can be provided for each test flow this limits the granularity in its variations. Hence, the periods for each test cycle are obtained through simulations and split into four groups. The latency of the analog measurement modules is included in the selected period. The longest cycle period corresponds to the pulse width determined by the cycle during which we achieve maximum switching. The shortest period corresponds to the lowest test period using which we achieve significant reduction in test time. Each test cycle is assigned to a period that is closer to, but not less than, the required period for that cycle.

Based on the periods obtained earlier, synchronization with the rate generator is controlled by specifying the periods in the test program using a timing block. The timing block

has information about the rates at which the pattern should be applied at each input and the behavior of the signal at each pin corresponding to the value in the pattern file. Since the patterns are applied at the start of each period, the pulse provided by the rate generator is not used as a clock to the scan circuit of the DUT, but instead it is used to synchronize the pattern generation. The clock pin is considered as an input pin and the duty cycle is set to 50% of the period set by the rate generator. This way we avoid any race conditions caused during the application of the inputs at the start of the each period of the rate generator. The pattern for each cycle contains the signal value needed at each input pin and the response to be observed at each output pin. The period for each cycle is specified by mapping the cycle with the waveform information that is uniquely defined to match one period.

ATE Results

The proposed method was applied by the ATE to the s298 benchmark circuit configured on the Xilinx. We simulated 36 deterministic combinational ATPG patterns used for simulation of the s298 circuit in Table 5.1 row 3. The cycle times required for each period were obtained through a *perl* script based on the energy consumption per cycle reported by Nanosim [4]. Though in this work the energy is obtained using NanoSim, power can be calculated per cycle during the actual test on the ATE by implementing a microcontroller on the test head. The minimum clock period that was used with the DUT was 100ns. For clarity of our experiment, the clock periods obtained through simulation were multiplied by 100. Four unique clock periods were then obtained such that we achieve significant reduction in test time. Figure 5.2 shows the test clock periods on the y-axis for each corresponding test cycle on the x-axis. The horizontal broken (red) lines show the four unique test cycle periods. A test cycle will use the test clock in the dotted line just above the period as shown in Figure 5.2. For the periodic clock test the maximum period in Figure 5.2 will be used as the fixed clock period.
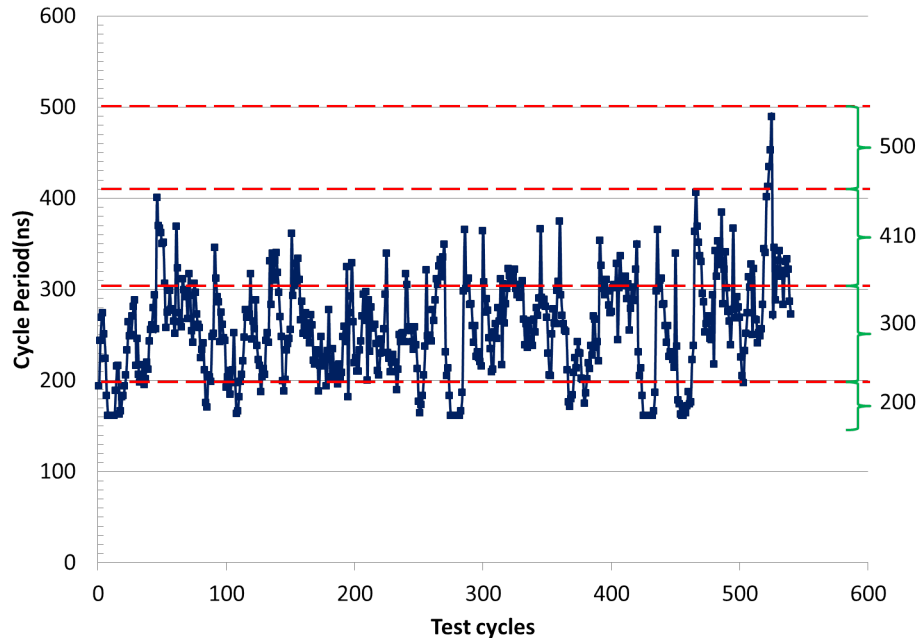
Figure 5.2: Aperiodic clock for 540-cycle scan test of s298 for a power budget of 1.23mW. Horizontal broken lines indicate four test clock periods available from the T2000GS ATE. Period used for a test cycle was the nearest higher ATE clock period.

The four clock periods used in this experiment were determined from a visual inspection of the plot in Figure 5.2 and are not optimal. It is possible to algorithmically find the best clock periods for any given number of periods that an ATE may support [30].

The waveforms for the ATE tests are shown in Figures 5.3 and 5.4, as viewed in the logic analyzer of the Advantest T2000GS system. The two figures have the same time scale. Figure 5.3 shows 33 cycles (13 to 46) which account for two scan sequences of the periodic clock test using a 500ns clock. The cycle number is indicated in the first row, followed by the period for each cycle as indicated above the first waveform. The labels on the left side of each waveform correspond to scan out, scan in, scan enable, three primary inputs and clock pins. The value expected at the scan out signals are indicated by X, L or H, at the beginning of each period and the strobe instants at which the output response is verified are indicated by downward/upward triangles, placed at the end of each period. The strobe points are located such that there is enough time for the signal to settle after a clock pulse is applied. The input waveforms are indicated along with the pattern that is applied at

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Figure 5.3: Periodic clock: ATE result for 540-cycle scan test of s298 benchmark circuit. Waveform shows 33 test cycles (cycles 13 through 46) of 500ns clock. Signals shown are scan-out, scan-in, scan enable, three primary outputs and clock. Green triangles under scan-out waveform are matching strobes.

the start of that period. A '1' pattern for the clock during each period indicates that the clock is turned on and based on the 50% duty cycle for the clock during that period, the corresponding waveform is generated by the frame processor. The test pattern used in this experiment is a deterministic test pattern generated by Fastscan ATPG for stuck-at faults having lower power cycles than high power cycles. For the periodic clock test of Figure 5.3, which used a fixed clock period of 500ns for the entire test, the total time for 540 cycles was 270μs.

Figure 5.4 shows the ATE waveforms using an aperiodic clock with periods, 500, 410, 300 and 200 ns, as selected for each cycle based on the corresponding activity it produces in the DUT. The test clock period is determined from Figure 5.2. Thus, the peak activity in the DUT is the same for both periodic and aperiodic clock tests. Both Figures 5.3 and 5.4 show the waveforms for a time interval of 16.5μs. Because the aperiodic clock test runs at varying clock period, more cycles are run in this time. Hence, in Figure 5.4 we observe 58 cycles (13 to 71) within the same time frame of $16.5\mu sec$ as 33 cycles (13 to 46) for the periodic clock test. The total test time for 540 cycles is now 157.7μs, which corresponds to a reduction of $\approx 38\%$ over the periodic clock test time.
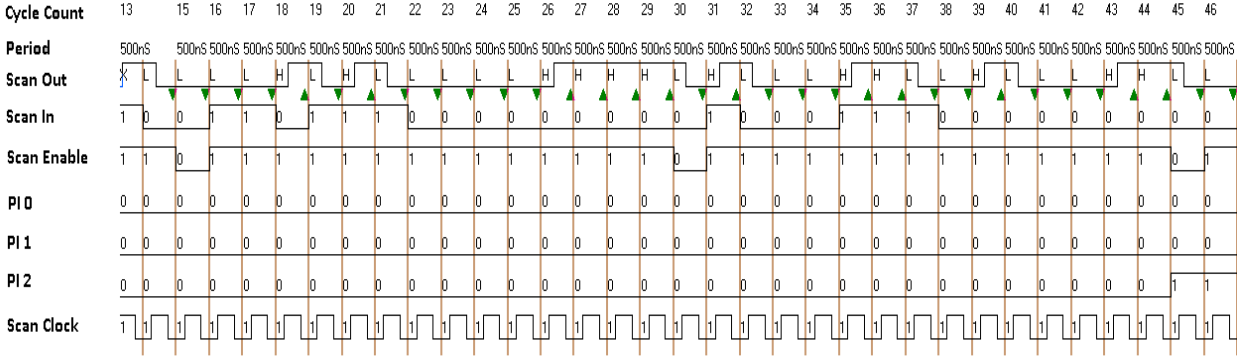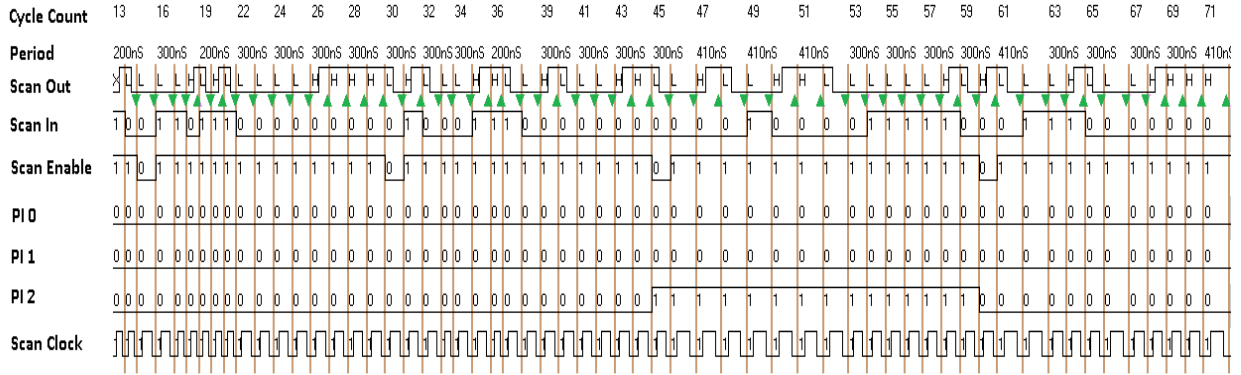
Figure 5.4: Aperiodic clock test: ATE result for 540-cycle scan test of s298 benchmark circuit. Waveforms shows 58 test cycles (cycles 13 through 71) taking the same time as taken by 46 cycles of periodic clock test in Figure 5.3. Clock periods used were 200, 300, 410 and 500 ns as shown in Figure 5.2. Signals shown are scan-out, scan-in, scan enable, three primary outputs and clock. Green triangles under scan-out waveform are matching strobes.

This test time reduction is dependent on the relative clock schedules between periodic and aperiodic clock tests and hence can be compared with 47.2% reduction reported for the 540 cycle test of s298 in Table 5.1. There are two reasons for ATE time saving being lower. Firstly, the granularity of clocks, i.e., four ATE clocks versus individual clock for each vector and secondly, the selection of the four ATE frequencies was ad-hoc and we believe a better selection can improve the test time reduction.

5.2   Optimum Voltage for Aperiodic Clock Test

We saw in the previous section that by using an aperiodic clock test, it is possible to reduce test time at nominal voltage. However, is it possible to reduce the test time further? In this section we examine the possibility of an optimum test time for aperiodic clock test at which the test can run the fastest.

The reduced voltage approach discussed in chapter 4 can be extended to further reduce the aperiodic clock test time. From equation (4.2), the period for power constrained cycle is proportional to the voltage used for test. Hence the width of the power constrained period can be reduced to improve the test time by reducing the voltage for the test. However,

there are a few points to consider when using aperiodic clock tests. First, some cycles in the aperiodic clock test may have already been compressed to the minimum period permitted by the structure constraint and as the supply voltage is reduced for test the critical path delay increases. Thus, as the voltage is reduced, more cycles become structure constrained. With further reduction in power supply, the voltage is further reduced and the test starts to lose its aperiodic clock property and becomes fully periodic. However, at some voltage before the test becomes periodic most of the cycles will be structurally constrained except for a very few cycles that are power constrained. The point at which the test still retains the aperiodic clock property will be the optimum test time for aperiodic clock test. Figure 3.4 illustrates this effect and is an extension of Figure 3.1. Based on equation (3.17) and (3.18), the aperiodic clock test time is bounded by the slowest frequency of the periodic clock test, limited by the power constraint and the fastest frequency limited only by the structure constraint. Point A represents the optimum voltage for periodic clock test. From point A, if the supply voltage is increased in steps such that $V > V_{synch}$ then some cycles start becoming power constrained, so those cycles have to be expanded to accommodate the power dissipation within the rated power. An optimum voltage for the aperiodic clock test, V_{asynch}, will lie in the region A-B at a point where the structural delay is lower and the test has more structure constrained cycles than power constrained cycles.

Analysis of this method is performed on the s298 benchmark circuit. The circuit was synthesized in 180nm technology using Leonardo Spectrum [7] and the scan chains were inserted using Mentor Graphics DFT Advisor. We used deterministic vectors generated by Fastscan [5] for stuck-at faults test, which also include one path delay vector to trigger the critical path of the device. The aperiodic clock test was performed for decreasing power values and the corresponding test times were noted. Figure 5.6 shows the results, plotted with test time on the y-axis and supply voltage on the x-axis. At each voltage we estimate the critical path delay using the alpha power law approximation [50, 51]:
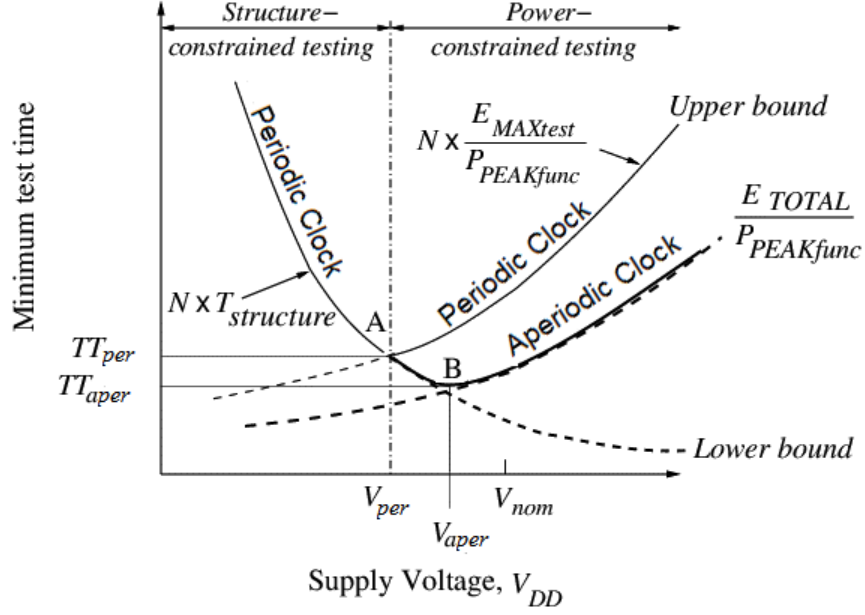
Figure 5.5: Aperiodic clock test time as a function of supply voltage showing the minimum test time voltage, V_{async}.

$$T_{structure} = K \times \frac{V_{DD}}{(V_{DD} - V_{TH})^\alpha} \tag{5.3}$$

A few assumptions were made when solving for the critical path delay,

1. Critical path does not change as voltage is reduced; found valid for small voltage changes.

2. Threshold voltage does not vary.

The maximum rated power was found by simulating the circuit at nominal voltage for 1000 random vectors in the functional mode. The resulting maximum power was noted to be 1.23mW. The value for the velocity saturation index α was found to be 2 by curve fitting the delay of a chain of inverters at different voltages with those obtained through simulation. Once the value of alpha is known, the value for K for the s298 benchmark, found using the delay obtained through STA in the section 4.3.1 at nominal voltage. The value for K is found to be 0.85. We can now find the delay of the critical path at every voltage step.
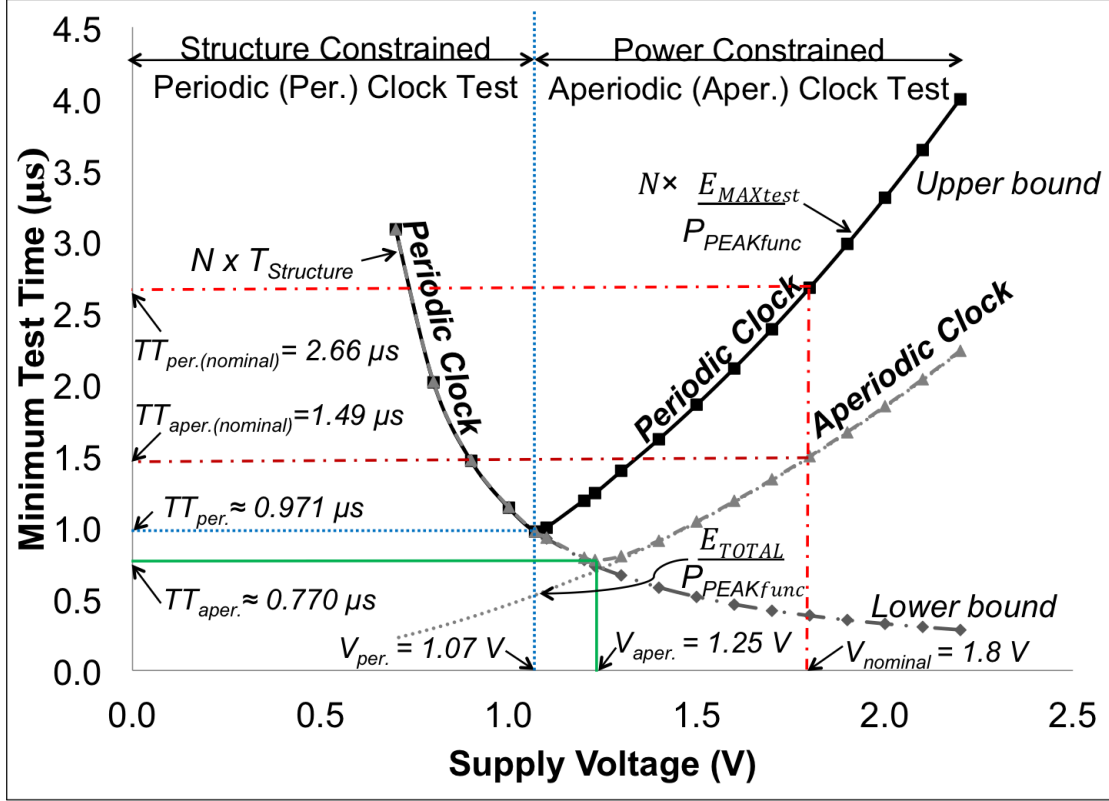
Figure 5.6: Minimum periodic and aperiodic clock test times for s298 circuit after selecting suitable supply voltages.

The method to calculate the aperiodic clock period at each voltage was based on the explanation provided in Section 5.1. At the optimum voltage of $V_{async} = 1.25$V, the corresponding minimum aperiodic clock test time using this method is found to be $TT_{asynch} = 0.77\mu$s, which is a 71% reduction in test time compared to the test time ($TT_{Nominal}$) of 2.66μs using periodic clock at the nominal voltage of 1.8V, as shown in Figure 5.6.

5.2.1 Simulation Results

Table 5.2 shows the optimum voltage for aperiodic clock test obtained through simulation. All circuits were synthesized using TSMC 180nm CMOS technology using Mentor Graphics Leonardo Spectrum [7]. The scan chains were inserted and stitched into a single scan using DFT Advisor. Patterns used in this experiment were the same set of patterns used in periodic clock test experiment in chapter 4 and for the aperiodic experiment in

Table 5.2: Optimum voltage V_{DDopt} for minimum aperiodic clock scan test time of ISCAS'89 circuits in 180nm CMOS ($\alpha = 2$, $V_{TH} = 0.39$V).

Circuit name	Proport-ionality constant K ($\times 10^{-9}$)	Maximum switched capaci-tance C_L (pF)	Total scan test cycles N	Peak per cycle power $P_{MAXfunc}$ (W)	Nominal voltage (1.8V) test		Optimum voltage test		Test time reduc-tion (%)
					Test clock freq. (MHz)	Test time (μs)	Supply V_{DDopt} (Volts)	Test time (μs)	
s298	0.85	1.76	450	0.0012	216.0	2.08	1.20	0.72	65.4
s298	0.85	2.04	498	0.0012	187.0	2.66	1.25	0.77	71.0
s298	0.85	2.06	540	0.0012	184.9	2.92	1.25	0.81	72.2
s382	2.18	3.07	704	0.0029	292:	2.41	1.59	1.37	43.5
s713	3.31	3.36	810	0.0015	137.28	5.9	1.62	2.49	57.7
s1423	6.38	10.22	6975	0.0045	135.9	51.3	1.82	39.7	26.7
s1423	6.63	10.23	6975	0.0030	90.6	77	1.55	49.5	35.7
s13207	4.64	38.9	62237	0.0213	168	369	1.7	281	23.8
s15850	5.22	109	101707	0.0240	67.35	1510	1.43	702	53.5
s38584	4.03	156.8	224112	0.0350	88.54	2531	1.41	1290	49.0

Table 5.1. The patterns were generated for stuck-at fault model using Mentor Graphics Tessent Fastscan [5]. The critical path delay for the structure constraint was obtained using the static timing analysis (STA) tool of Leonardo Spectrum. The α power law model in equation (5.3) was then used to calculate the path delay value at each supply voltage to set the structure constraint for the aperiodic clock period. The critical path is assumed to be constant and hence the initial value for the proportionality constant was obtained at the nominal voltage at the velocity saturation value $\alpha = 2$.

Column 1 of Table 5.2 shows the ISCAS'89 benchmark circuits used for this experiment, column 2 gives the proportionality constant used to calculate the delay at each voltage using the α delay law model. The maximum allowable power used in these experiments is shown in column 5. The maximum power chosen here is measured by simulating each circuit in normal mode with 1000 random patterns and measuring the maximum power over the entire test. Columns 6 and 7 show the test clock frequency and total test time for a conventional test using a periodic clock period at the nominal voltage of 1.8V. Column 8 shows the optimum test supply voltage for an aperiodic clock test and the corresponding test time at

the optimum voltage is given in column 9. Finally the reduction in test time by using an aperiodic clock under reduced supply voltage over the periodic clock at nominal voltage is shown in column 10. The results show significant reduction in test time when compared to the methods discussed earlier. Since, the calculated delay is pessimistic, in a practical setting more reduction in test time is possible.

Table 5.3: Test times for various methods normalized with respect to that of the conventional method (nominal 1.8V supply and periodic clock).

| Circuit | Nominal Voltage 1.8V | | Periodic clock | | Aperiodic clock | |
Name	Periodic clock	Aperiodic clock	Optimum voltage	Reduction ratio	Optimum voltage	Reduction ratio
s298	1	0.52 - 0.71	1.07 - 1.1	0.35 - 0.38	1.20 - 1.25	0.27 - 0.34
s382	1	0.67	1.44	0.63	1.59	0.56
s713	1	0.48	1.33	0.55	1.62	0.42
s1423	1	0.72	1.49	0.68	1.55	0.64
s13207	1	0.84	1.62	0.80	1.70	0.76
s15850	1	0.72	1.30	0.52	1.43	0.46
s38584	1	0.83	1.30	0.51	1.41	0.49

Table 5.3 summarizes the test time reduction using the proposed methods, normalized with the conventional method using a periodic clock at the nominal voltage of 1.8V for CMOS 180nm technology. Summarizing the results, it is evident that for most of the circuits the test time is reduced significantly ($> 30\%$) by either reducing the power supply or by scaling the frequency.

Chapter 6

Discussion

6.1 Adapting to At-Speed Testing

Timing related defects are often targeted during at-speed testing. This necessitates the need for clock pulses generated at functional speeds. Due to high costs of automatic test equipment (ATE) and the growing clock speeds, implementing at-speed testing using ATEs will not be economical [15], due to this reason at-speed clocks during capture cycles are generated internally using phase lock loops (PLL) that generates clock pulses with fixed frequency that can be a multiple of a reference slow clock [38]. On chip PLLs also serve another purpose; to eliminate clock skews [48].

In the case of at-speed testing the use of aperiodic clock can be restricted only to improve scan shift timing, since the majority of test time is taken while shifting. Besides, during at-speed the capture cycle (and the launch cycle for launch on capture) already run at functional speed. The slow clock during scan shift can be supplied by the ATE or generated internally using a divide by N counter. In the case where the clock for scan shift is generated within the chip, modifications can be done to the architecture such that the tester chooses the clock to be used. To describe the feasibility of this procedure let us consider the serdes architecture used in [52], where a deserializer is used to shift patterns at high speed from the tester and the internal scan chain shifts patterns at a slow speed. The shift clock to the internal scan chains is a slow clock with a frequency that is a fourth of the ATE clock. This slow clock could be generated by implementing a simple divide by N counter. With aperiodic clock, the divide by N counter could be designed to produce the required four clocks.. The ATE can then be used to send the bits that sets the value for N and the corresponding output is used as clock. When the pattern is shifted out, the output from the scan chains is

fed to the serializer module which shifts out the pattern to the ATE at high speed. Since the patterns from the ATE and to the ATE are shifted at the same speed, there should not be any conflict due to internal aperiodic clock when comparing the output with the expected value. It is to be noted that, while choosing the clock period for the aperiodic test, any additional delay constraints due to long interconnects during scan shift that is considered for timing closure will be added to the structure constraint in the aperiodic clock. Further analysis will be done in future works that explores this feasibility.

6.2 Adapting to Process-Voltage-Temperature Variations

As technology scales to small feature sizes intra-die and inter-die variations in the operational parameters of the chips are more pronounced. These variations can be due random or systematic defects due to fabrication process and can often affect the timing during voltage and temperature changes. Testing the circuit under test (CUT) under different process-voltage-temperature (PVT) corners, namely *worst, typical*, and *best* cases, identifies the reliability of the chip and its operating range [44]. Such testing normally checks for the functionality of the device at each corners. Designers and process engineers often determine these corners and the corresponding delays are characterized to the chips structural constraints [25, 26]. The CUT is tested at these corners for its functionality and therefore corner testing is more critical during timing based tests. Hence, during corner testing the concern is for the CUT to meet the timing specification of the capture cycle. The shift cycle (and launch cycle in case of launch on shift) must include the interconnect delay and the setup and hold time constraints imposed due to these variations. Using the proposed method with the corner testing would account the same constraints when determining the structural constraint for the test clock period and while finding the optimum voltage during scan shift at each of these corners. The voltage can then be switched to the corner voltage during the capture cycles either internally if the chip has a dynamic voltage regulator [24] or externally by the ATE.

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Further analysis will be performed in future extensions of this work to analyze the effect of process variations in obtaining the optimum values in aperiodic test and voltage at each corners and explore the feasibility to increase the supply voltage dynamically for capture cycle using ATE.

Chapter 7

Conclusion

Advanced technologies for CMOS VLSI design for low power applications require power constrained tests that could result in longer test time and high testing costs. New methods are required to reduce test time while conforming to the allowable power. In this work, employing scan-based test, ISCAS'89 benchmark circuits were simulated for the maximum energy dissipated using periodic clock period. Different methodologies such as scaling down supply voltage and scaling up the frequency were shown to help reduce test time. Results have shown that a reduction of more than 50% is attainable in some cases. Maximum reduction in test time is observed when the peak energy dissipated by the circuit is significantly greater than the average energy dissipated. The feasibility of aperiodic clock test was demonstrated on an ATE. The results presented in this work suggests that a test engineer can have multiple options to reduce test time based on the available hardware and improvements in tester framework and hardware can help reap full benefits of the proposed methods.

It was shown that by reducing the power supply voltage at which a DUT is tested the test time can be reduced. Future investigations should involve the use of the proposed method for delay testing with the focus of finding the correlation of low voltage timing measurements with actual nominal voltage of the delay. Effects of leakage power that occur in advanced technologies will also have to be investigated in the future. We believe that the methods presented here will remain beneficial. The dynamic power considered in this work, was the cycle-average peak power, which also includes the instantaneous peak within a clock cycle. Although smoothing due to suitable design of power grid and decoupling capacitors may justify the use of cycle-average, any possible issues related to power supply noise and coupling effects will have to be examined in the future.

Future analysis would include process variations when finding aperiodic clock periods for a DUT. Such an analysis would be beneficial for the proposed method and we believe that it will not be a limitation in determining optimum clock periods. System on chip (SoC) testing could have severe test time and power problems when multiple cores are tested in parallel. There will be benefits if core tests are optimized by aperiodic clock periods. However, the distributions of clocks through the test access mechanism (TAM) of SoC and test program details have to be analyzed in the future. Such limitations may not be encountered when using reduced power supply voltage with periodic clock test. Since the netlist used in this work did not have information on wiring delay after place and route, the work presented in this thesis assumes that the critical path delay on the scan path and functional path to be similar. However, the critical path for scan mode may have very little logic but it is not optimized for delay in the physical design, future work will have to examine the issue in depth.

The work presented in this thesis uses an ad-hoc method to group clock periods used on the ATE, future work can investigate different non-linear algorithms that could provide the optimum values for the clock periods. The test programming used in the Advantest T2000GS ATE is not a conventional one and the method have to be adapted to the STIL format [3, 40], which is more commonly used in the industry. Some circuits include a dual voltage logic that can operate at different voltage levels. With that in mind, a dynamic voltage mechanism can be devised in the same way as the aperiodic clock, where the voltage for each cycle will be determined by the amount of energy dissipated during that cycle. At the cost of some added complexity to the test set up the added degree of freedom will further reduce the test time. It is suggested that such a scheme should be studied in the future.

The clock signal during test may be generated in several possible ways. The clock may be supplied directly by the ATE. Alternatively, it may be generated by a phase lock loop (PLL) circuit on the device under test (DUT) with a synchronizing signal provided from the ATE. In the first case the control of the clock frequency would be done by the test program.

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However, the manipulation of test clock frequency would be more complex in case of test compression where the test data transmission rate between ATE and DUT would differ from the internal clock on DUT. Such schemes require serious study. Another important issue is the distribution of clock on DUT. Typically, a clock tree is designed to correctly transmit the functional clock or any fixed rate slower clock. However, faster clock as may be used for reduced voltage periodic test or variable clock rates used for aperiodic test would require a careful study of the time constant of the clock distribution network.

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