Planar Magnetics Design for Low Voltage High Power DC-DC Converters

by

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Abstract

Planar magnetic technology is widely used in a variety of applications from telecommunications to power electronics. In particular, the use of planar inductors and transformers in power electronics have burgeoned as a result of increasing switching frequencies. However, the design and construction of these magnetic structures becomes more difficult as switching frequencies increase. At high frequencies, the skin and proximity effects contribute significantly to a component's total loss. Thus, methods for analyzing the various losses inherent to planar magnetic components were discussed in detail. The air gap necessary for planar inductor design was characterized and discussed in depth. The core geometry, core material, number of turns and gap width affect the inductance of a planar inductor. All of these factors must be carefully considered when designing and building an inductor.

A multitude of planar inductors were designed for use in a 12-1 V synchronous buck converter configuration. A simple testing method was proposed that allowed quick and accurate comparison of the various inductors. The inductors were fully characterized through the efficiency of the overall buck converter. Limitations for the developed inductors were found to be core saturation and discontinuous mode operation.

Finite element analysis (FEA) was performed to investigate the current distribution throughout the windings. It was quickly concluded that 2D analysis was not sufficiently accurate; consequently, all FEA modeling was performed with the 3D solver. From this analysis, the gap location with respect to the windings was determined to be critical to the level of current imbalance. As such, a conclusion was reached that the windings should be located as far from the gap as possible. A more ideal solution, if available, is the utilization of cores having the air gap located at the top of the middle leg.

The most suitable planar inductor determined through preliminary testing was integrated in the most efficient buck converter design. The planar inductor buck converter board performed comparably with a similar board utilizing COTS inductors. A peak efficiency of 94.7% was achieved at the a load current of 6 A. The optimal load current rating of each buck converter phase was determined to be 12 A. For this load current level, the planar inductor performed best at 400 kHz with an efficiency of 92%. The DC resistance of the planar inductor was about 1.5 mΩ, which caused the efficiency of the component to fall off more quickly than the 1 mΩ COTS inductors.

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Chapter 1

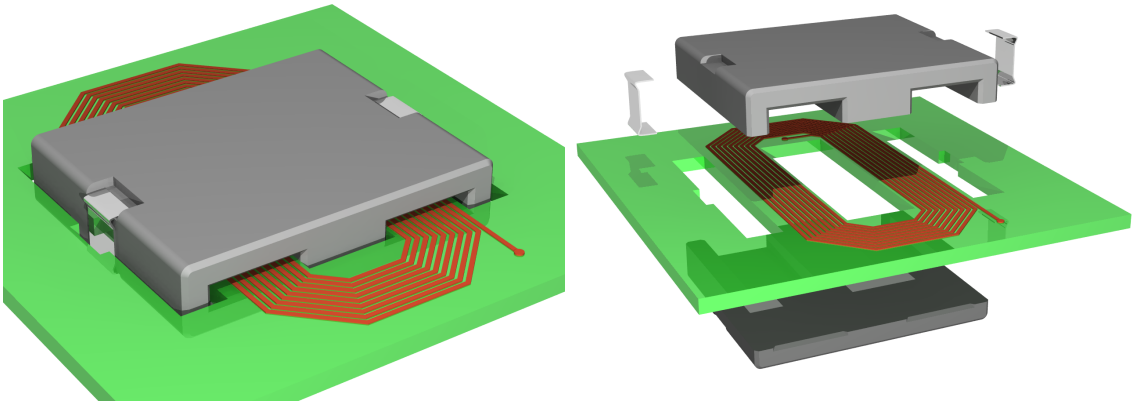
Introduction

The growth in supercomputer facilities and data centers over the past decade has engendered an increased demand for high density and high efficiency power supplies [1]. As a further requirement, modern processors require a power supply with stringent transient performance to ensure the required voltage upheld [2],[3]. Consequently, modern switched-mode power supplies (SMPS) have seen an increase in operating frequency to accommodate load demands. This push towards higher operating frequencies gives rise to benefits as well as drawbacks from a design perspective. A decrease in the size of the magnetic component is a natural consequence of increasing the operating frequency. However, additional losses are introduced as a result of the skin and proximity effects at these higher frequencies.

Planar magnetic technology (Figure 1.1) has benefited greatly from the advancements in electronics manufacturing. Low profile windings have been around for some time. However, before the advent of printed circuit board (PCB) technology, the construction of planar windings was difficult, time-consuming, and for the most part, not economically viable. As the cost of PCB fabrication has fallen, the technology has began to supplant itself not only in power electronics, but also in fields such as communications and power distribution.

Planar magnetic technology offers a number of advantages that mitigate many of the problems inherent to conventional magnetic devices [4],[5]. An overview of the technology and its candidacy for power electronic applications will be presented as follows:

- Magnetic components for power electronics
- Benefits and limitations of planar magnetics
- Commercially available planar cores

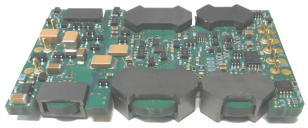


(a) Diagram of planar inductor (b) Diagram in exploded view

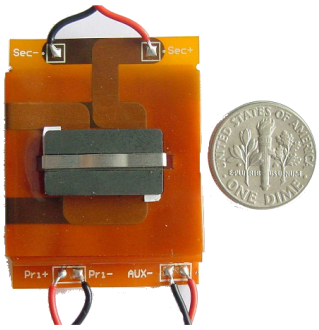
Figure 1.1: Planar structure

1.1 Overview of Planar Magnetic Components

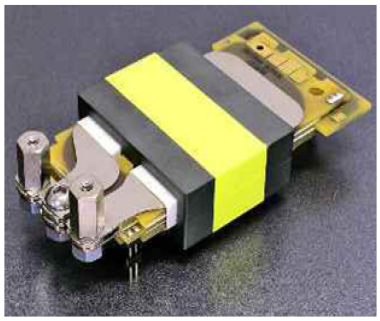
Planar magnetic technology is present in a variety of applications ranging from power electronics to wireless communication systems [1]. Several approaches to "planar" windings have been utilized in order to best suite the application. Perhaps the most common planar technology involves standard PCB techniques with various winding structures (Figure 1.2a). Various winding techniques have been explored over the years [6],[7]. Flexible substrates such as polyimide are often used for electronics that have unusual packaging constraints (i.e. cameras, cell phones)[8]. This technology can be easily extended to planar magnetics as shown in Figure 1.2b. For high current applications where ohmic losses must be minimized, a hybrid approach employing PCB technology and stamped copper traces is often a suitable approach (Figure 1.2c). For certain applications, the cost associated with PCB fabrication may preclude the use of these methods. In such cases, windings may be "hand-made" and stacked accordingly while making use of an insulator. Vertically and horizontally oriented examples are presented in Figure 1.2d and Figure 1.2e, respectively. RF applications also make use of planar windings for magnetic components (Figure 1.2f). Often, an air core is sufficient to achieve the necessary inductance since the operating frequency is generally much higher than in power electronic applications.



(a) Standard multilayer PCB

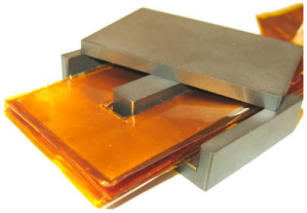


(b) Flexible multilayer PCB

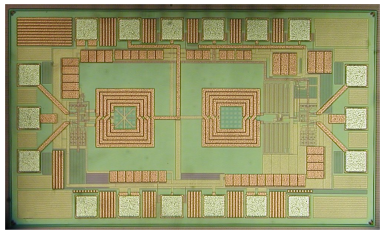


(c) Hybrid PCB with copper stamping

(d) Vertical windings



(e) Copper foils with Kapton taper



(f) Air core RF inductor

Figure 1.2: Examples of planar magnetic technologies

1.1.1 Benefits

Planar magnetic technology exhibits a variety of advantages over conventional wire-wound magnetic components. Some of the prominent benefits as related to power electronics are as follows:

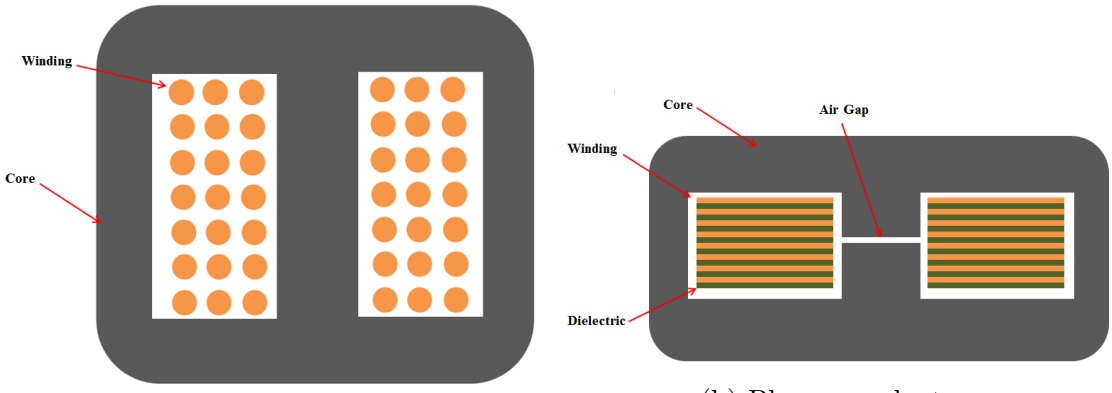
- **Low profile** - The required core volume of an inductor to avoid magnetic saturation is a strong function of the current. For this reason, the volume of the core for a given application is often a fixed value. Consequently, the overall volume of the planar and conventional magnetic components will be roughly equal. However, a larger footprint is often accepted to achieve a reduction in the height of the component.

- **Implementation and repeatabilty** - Modern PCB technology allows for arbitrary design of the winding and interleaving structure. This is a particularly important point when considering large scale integration and the need for consistent component

characteristics. Additionally, printing the windings directly onto the PCB removes the losses inherent to the soldered terminations required for surface mount devices (SMD).

- **Thermal characteristics** - Although the volume of planar and conventional magnetic devices are often similar, planar technology tends to provide a higher surface-to-volume ratio. This affords the structure a greater ability to dissipate the heat from ohmic and core losses.

- **Reduced AC losses** - In general, SMPS applications operate at switching frequencies ranging from hundreds of kilohertz to a couple megahertz. However, a significant amount of the total energy lies in the upper level harmonics. As a result, the skin effect often contributes to additional losses in conventional round-wire components. The flat windings inherent to planar inductors and transformers can reduce these high frequency losses dramatically. Various investigations into this subject have shown PCB windings can provide a 90% reduction in AC resistance. The winding geometries for conventional and planar structures are presented in Figure 1.3.



(a) Conventional round conductors

(b) Planar conductors

Figure 1.3: Comparison of winding structures

1.1.2 Limitations

Some limitations are often associated with planar magnetic technology. Most can be worked around with appropriate design procedures. The most prominent limitations are:

- **Limited number of turns** - Conventional winding structures have a much easier time achieving a large number of turns. Due to the nature of PCB technology, achieving multiple turns often equates to additional layers. If the total number of layers is fixed, the dc resistance of the component will suffer in order to achieve the necessary turns ratio or inductance. This preventative cost is being mitigated as PCB fabrication costs continue to fall.

- **Large footprint** - The low profile structure attained through planar technology comes at the cost of a larger footprint. This can be problematic if board space for an application is limited. However, in many cases, the board size will be constrained in the normal (z) direction as well as the horizontal (xy) direction. As mentioned previously, the low profile characteristic of planar technology can be exploited in these situations.

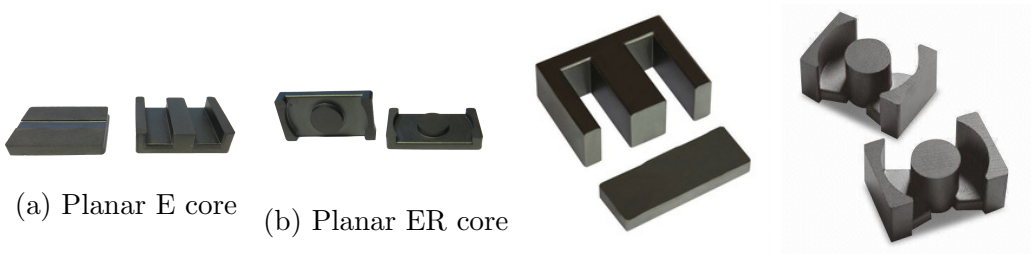
- **Low window utilization** - Planar technologies based on rigid PCB techniques will often possess a relatively low window utilization factor. The dielectric layers associated with PCB technologies take up a considerable amount of the available window. The hybrid approach mentioned previously is an example of a work around for this limiting factor.

1.2 Planar Cores

Magnetic cores for use in planar magnetics are available in a variety of industry standard core sizes, geometries, and materials. The extensive adoption of planar technology has driven the development of application specific magnetic core materials and shapes. The type of core will differ greatly with the application; therefore, this discussion will be restricted primarily to power electronics applications.

1.2.1 Geometry

The most common core geometry within the power electronics realm is the planar E core and its variants. The planar E core, shown in Figure 1.4a, is the easiest to integrate into a PCB. However, the rectangular shape of the legs are not ideal for achieving a uniform flux density. The planar ER core (Figure 1.4b) has a number of advantages over the standard planar E core. Although it is slightly more difficult to implement in a PCB, the flux density is more evenly distributed through the legs due to the optimized leg shapes. Additionally, the dc resistance associated with these cores is reduced due to the shorter winding lengths. For high current applications where a hybrid PCB with stamped copper is utilized, the standard E core (Figure 1.4c) is often used to provide the necessary height. The planar Q core, shown in Figure 1.4d, is similar to the planar ER core, but is more efficient with respect to distributing flux evenly throughout the volume [9].



(a) Planar E core (b) Planar ER core (c) E core (d) Planar Q core

Figure 1.4: Core Geometries

1.2.2 Material

A variety of magnetic materials with considerable differences are available, making the choice of material a critical design step. Metal alloy, powdered metal, and ferrite are the primary material classes for power electronic applications. Metal alloy materials are tape wound cores that have extremely high permeability and saturation flux density. Unfortunately, the resistivity of the material is such that eddy current losses are unacceptable above

400 Hz. For this reason, they are generally not viable candidates for most SMPS applications, which often operate at over 100 kHz. Powdered metal cores have a much lower permeability than metal alloy cores due to non-magnetic sections distributed throughout the structure. Although these materials often have high saturation flux densities, they are still quite lossy at SMPS frequencies. Ferrite materials are predominantly the best option for SMPS applications. Many ferrite materials are formed through a mixture of iron oxide with manganese and zinc or nickel. The MnZn ferrites are generally used for frequencies up to 2 MHz. NiZn ferrites were developed to have much higher resistivity, making them suitable for applications up to several hundred MHz. The saturation flux density of ferrites is considerably lower than in metal alloys and powdered metal materials; thus, core saturation is often a limitation of ferrite materials. [10],[9].

Chapter 2

Planar Magnetic Component Design and Loss Characteristics

2.1 Loss Mechanisms

Inductor losses can generally be subdivided into two categories: core loss and winding loss. Core loss involves hysteresis loss as well as eddy current formation within the core material itself. Winding loss is often spoken of in terms of AC and DC losses. DC losses are determined by the DC resistance of the winding and the magnitude of the DC component. AC losses occur as a result of the skin and proximity effects.

2.1.1 Winding Loss

For the vast a majority of SMPS applications, winding losses will make up the majority of the total component losses. One reason for this is the large DC offset inherent to filter inductor applications. Consequently, the associated loss mechanisms must be carefully considered throughout the design process. AC winding losses are the result of eddy currents forming within the windings. These eddy currents can form due to the skin and proximity effects as well as fringing magnetic fields. The skin and proximity effects are mechanically similar. Additional eddy currents often form as the result of air gap location. Both situations will be considered.

Skin and Proximity Effects

The skin effect and proximity effect increase the equivalent resistance of a trace by altering the current distribution within the winding. Both work under the same principle and have the potential to cause current imbalance in the windings. Consider a conductor

carrying current i(t) as shown in Figure 2.1. According to Lenz's law, the magnetic flux produced by the eddy currents will oppose the flux due to the current i(t). It follows that the net result of the original current combined with the eddy currents alters the current distribution.

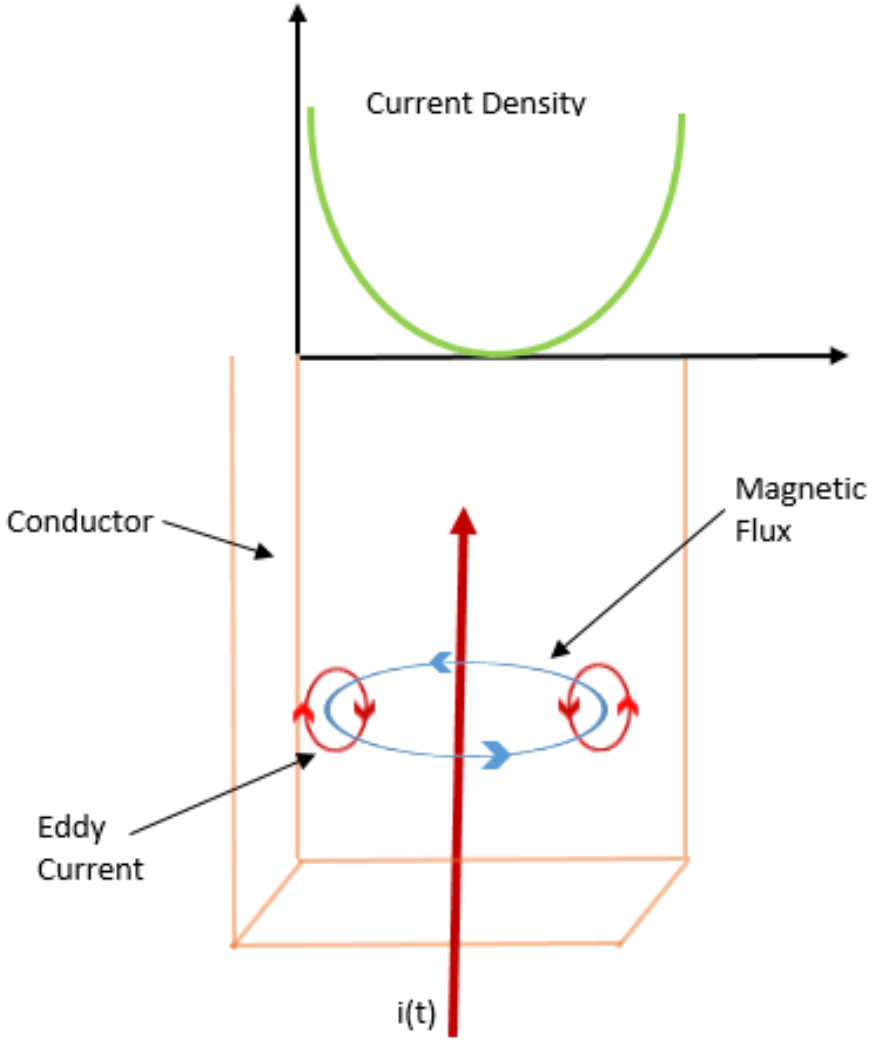


Figure 2.1: Eddy current formation in a conductor

The precise current distribution can be solved for using Maxwell's equations, but is often evaluated empirically by means of the skin depth, δ. The skin depth is a decaying function in frequency and is given by

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}} \tag{2.1}$$

where ρ is the resistivity, μ is the permeability, and f is the frequency. It should be noted that resistivity of a material is a function of temperature. The dependence of ρ on temperature, T, is given as

$$\rho(T) = \rho_0[1 + \alpha(T - T_0)] \tag{2.2}$$

where α is a temperature coeficcient.

2.1.2 Gapping

Power inductors and filter inductors found in SMPS often require a discrete gap in order to maintain a predictable inductance. The size and location of the gap can substantially change the performance of the inductor. With regard to SMPS, the size of the gap is determined by two criteria. First, the effective permeability, μ_e, is controlled through the size of the gap. In turn, this limits the maximum flux density for a given load current. The second function of the gap is to control the amount of ripple current allowed by the design specification. These functions are naturally conflicting and an iterative process is often needed to find the appropriate gap size [11],[12].

The location of the gap is also of great importance. A review of magnetic circuits will assist in clarifying this point. For an inductor, the total reluctance of the magnetic component is given as the ratio of magnetomotive force (mmf) to total magnetic flux

$$\mathcal{R} = \frac{\mathcal{F}}{\phi} \tag{2.3}$$

where $\mathcal{F}$ is the mmf given as

$$\mathcal{F} = \oint \mathbf{H} \cdot d\mathbf{l} \tag{2.4}$$

and ϕ is the total magnetic flux given as

$$\Phi = \iint_S \mathbf{B} \cdot d\mathbf{S}. \tag{2.5}$$

For a material with a high permeability, $\mu_r >> 1$, the total reluctance of the magnetic circuit is given as

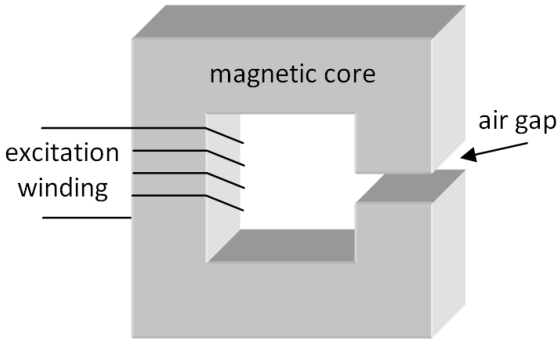
$$\mathcal{R} = \frac{l}{\mu_r \mu_0 A}. \tag{2.6}$$

The addition of a small air gap ($\mu_r = 1$) introduces a high reluctance element into an otherwise low reluctance path. Analogous to Ohm's law, the majority of the energy is stored within the high reluctance air gap [13]. However, due to the sharp discontinuity in path reluctance, the magnetic flux tends to "bow out" causing significant fringing fields in the area of the gap. Shown in Figure 2.2b is the ideal formation of the magnetic flux through the air gap. The more realistic formation of these fields is shown in close proximity to planar windings in Figure 2.2c. The formation of eddy currents as a result of these fringing fields is shown in Figure 2.2d according to Lenz's law. The orientation of these fringing fields can be particularly detrimental to performance. As shown in Figure 2.2c and Figure 2.2d, the incident fields are roughly normal to the surface of the winding. This particular orientation will form the strongest possible eddy currents within the windings according to

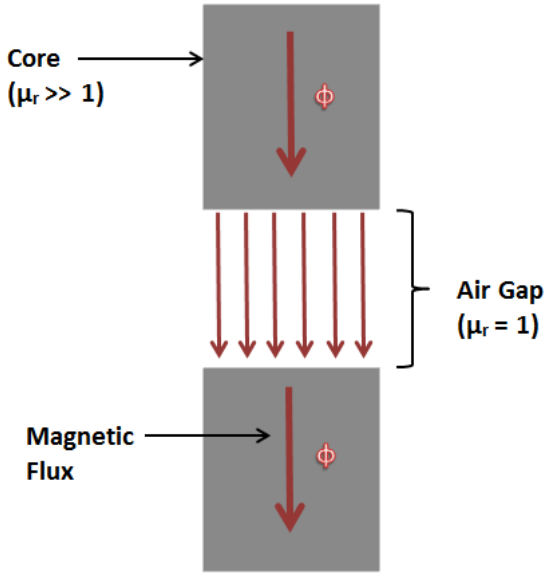
$$\nabla \times \mathbf{H} = \mathbf{J} + \frac{\partial \mathbf{D}}{\partial t}. \tag{2.7}$$

The formation of eddy currents will have the overall effect of crowding the current within the trace. The direction of the eddy currents shown in Figure 2.2d indicate that distinct regions of current imbalance will develop. The middle of the trace will have a reduction in current density due to the canceling effect of the eddy currents. However, the regions of the trace in close proximity to the gap will experience a much higher current density. This phenomena

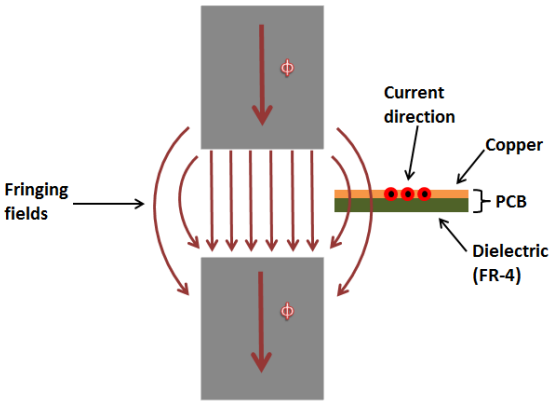
will be explored further when finite element method (FEM) simulations of planar magnetic devices are presented.



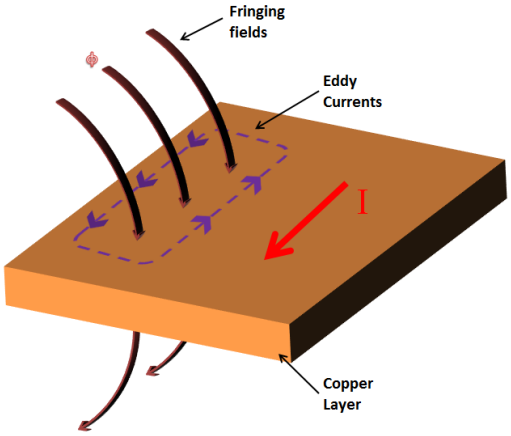
(a) Magnetic circuit with an air gap



(b) Ideal flux fields through the air gap



(c) Fringing fields incident on copper traces



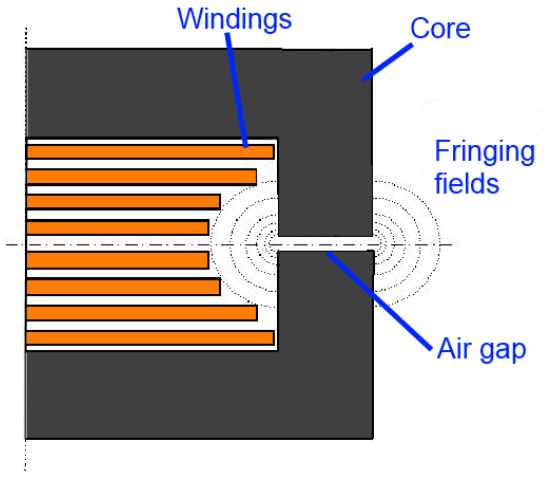
(d) Development of eddy currents within the trace

Figure 2.2: Eddy current formation

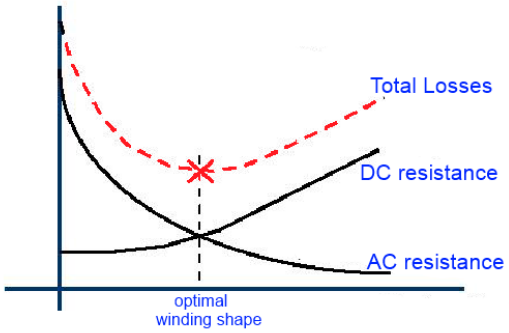
Improved Winding Configuration

Altering the shape of the windings is one approach investigated in [14],[15] to combat the strong eddy currents that tend to form on any conductor near the air gap. This method

essentially accepts a higher DC resistance to reduce the overall resistance through reduction in AC losses. Several optimal structures have been proposed; however, they all work under an optimization principle, where an optimal winding structure is one that minimizes the overall winding resistance [6] as shown in Figure 2.3.



(a) Diagram of shaped windings around fringing flux



(b) Optimizing curve for shaped windings

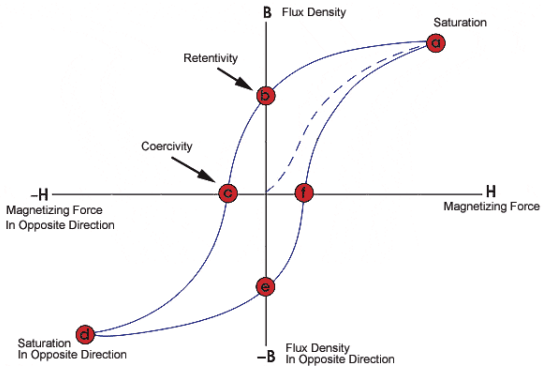
Figure 2.3: Filter inductor current waveforms

2.1.3 Core Loss

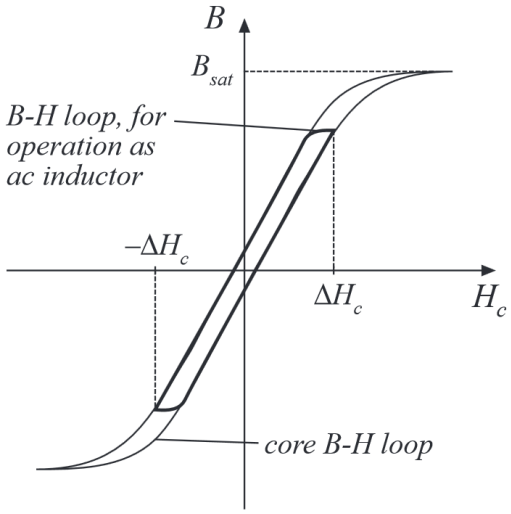
Core losses in inductors can vary greatly with the application. Tape-wound metal alloys generally have the highest core losses of any material class. Ferrite materials are usually considered to have the lowest core losses. Although most SMPS utilize ferrite materials, the characteristics of the system can increase the hysteresis losses in the core dramatically.

A typical B-H curve is shown in Figure 2.4a. In general, an inductor will operate over a certain region of the loop - ideally avoiding the saturation region. Figure 2.4b depicts the B-H loop for operation as an ac inductor. The operating loop will always be symmetric about the H-axis if there is no DC bias. Figure 2.4c illustrates a filter inductor which is often used in SMPS applications. This particular inductor has a large DC current component with a smaller superimposed AC component. The area of the minor B-H loop will increase as the AC component of the current increases. Since power loss in a core material is a function of

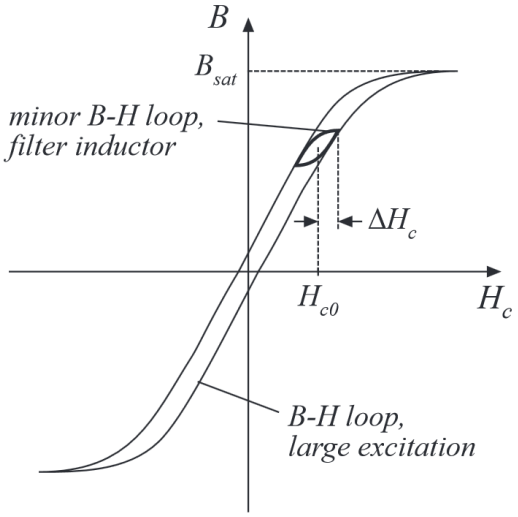
B-H loop area, it should be noted that core losses in filter inductors can be quite small if the percentage current ripple is small. However, a smaller ripple current often will require a larger inductance. Consequently, the reduction in core losses are often accompanied by an increase in winding loss [16].



(a) Full B-H curve path



(b) B-H loop

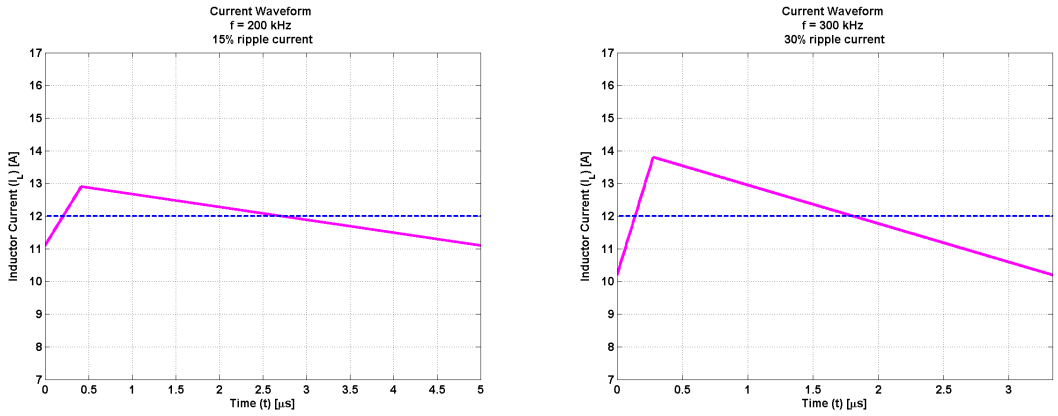


(c) Minor B-H loop

Figure 2.4: Comparison of minor and major BH loops

The ability to model core loss empirically is an invaluable tool in characterizing the performance of an inductor. Traditional empirical formulas lacked the ability to handle arbitrary waveforms. In the case of a filter inductor, the waveform is essentially a triangle

waveform with a DC offset. Two examples of typical filter inductor current waveforms are presented in Figure 2.5. Several new methods have been developed in order to more accurately calculate core loss due to non-sinusoidal waveforms [17].



(a) Filter inductor current waveform with 15% current ripple

(b) Filter inductor current waveform with 30% current ripple

Figure 2.5: Filter inductor current waveforms

Steinmetz's Equation

The first empirical model used to describe core loss was Steinmetz's equation (SE). In this model, the frequency and peak flux density were used to estimate the loss within the core. The constants k, α, and β are material dependent curve-fit parameters used to describe the power loss density as shown in Equation 2.8.

$$P = k f^{\alpha} \hat{B}^{\beta} \tag{2.8}$$

Various problems arose from this model when applied to power electronic applications. The SE description of core power loss was difficult to apply over a large frequency range as the material parameters displayed variation. Second, and more important, this model ignores the effect of a DC bias within the circuit. Many inductors used in power electronic applications carry a significant DC bias in addition to the AC component. For these reasons,

an improvement in core power loss calculations was desperately needed for power electronic applications.

Modified Steinmetz's Equation

A modified Steinmetz's equation (MSE) was developed by Albach, Durbau and Brockmeyer [18] that included a term based on the varying magnetic field within the core. An equivalent frequency provides a weighted average of the time varying magnetic field as shown in Equation 2.9.

$$f_{eq} = \frac{2}{\Delta B^2 \pi^2} \int_0^T (\frac{dB}{dt})^2 dt \tag{2.9}$$

The power loss density can then be found by using Equation 2.10.

$$P = k f_{eq}^{\alpha-1} \hat{B}^{\beta} f_r \tag{2.10}$$

Although this provided considerable improvement over the original Steinmetz equation, the assumptions about the kind of averaging used to determine the equivalent frequency leads to limited accuracy.

Generalized Steinmetz Equation

To combat the limitations of the MSE, Li, Abdallah and Sullivan [19] developed the generalized Steinmetz equation (GSE). The GSE (Equation 2.11) was developed on the premise that the instantaneous power loss is a function of the instantaneous magnetic field and its derivative.

$$P(t) = k \left| \frac{dB}{dt} \right|^a |B(t)|^b \tag{2.11}$$

The GSE was determined to not provide any significant advantage over the previously developed MSE. In some cases, the results were even more inaccurate than the modified Steinmetz equation.

improved Generalized Steinmetz Equation

Due to the lack in accuracy of the GSE and MSE, it became apparent that the entire hysteresis path was critical to determine the core loss. Venkatachalam, Sullivan, Abdallah and Tacca [17] determined that an appropriate relationship to describe instantaneous power loss could be stated in the form shown in Equation 2.12.

$$P(t) = k(\Delta B)^w \left|\frac{dB}{dt}\right|^z \tag{2.12}$$

From this, it was determined that the original Steinmetz parameters α and β could be fit into Equation 2.12 in the form

$$P(t) = \frac{1}{T}\int_0^T k_1 \left|B(t)\right|^{\beta-\alpha} \left|\frac{dB}{dt}\right|^\alpha \tag{2.13}$$

The parameter k_1 is calculated as

$$k_1 = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi} |cos\theta|^\alpha |sin\theta|^{\beta-\alpha} d\theta} \tag{2.14}$$

This result provides the most accurate estimation of core loss for arbitrary waveforms. The iGSE utilizes the hysteresis path as well as the time derivative of that path to quantify core loss.

2.2 Design Procedure

The design and implementation of planar inductor is an involved process that requires careful consideration of several key factors. A flow-chart defining a general algorithm for designing planar inductors is shown in Figure 2.6.

- **Circuit parameter definition:** Although it may seem rudimentary, a thorough understanding of the circuit is critical for developing magnetic components. Understanding overall system requirements is particularly important when building power converters since the inductor is very influential over the output waveform. Faulty design of the magnetic component can lead to poor system performance and may also damage the load.

- **Core material and geometry:** A variety of core material and geometry combinations are available to the designer from a multitude of manufacturers. Most materials have one or two characteristics that separate them from other material, such as core loss, high flux, etc. It is important to recognize the most pertinent issue in a design in order to fully exploit the characteristics of the core material.

- **Turns and gap width:** The number of turns and the gap width control the inductance and flux density of the structure. They must always be designed for in tandem to avoid core saturation and high winding losses. In general, a minimum gap is required to keep the core out of the saturation region. However, a larger gap will reduce the inductance. Thus, multiple turns can be added to increase the inductance. An unavoidable increase in DCR will usually be the result of increasing the number of turns. Consequently, both gap and the number of turns must be optimized for any given design.

- **Winding configuration:** One approach that enables the designer to make use of more turns without increasing the DC resistance is through a parallel turn structure. This, in essence, reduces the resistance of a structure by a factor equal to the number of parallel windings used. However, implementing parallel windings necessitates the use of high layer-count boards, which will often increase the cost of production. If space is not at a premium, multiple two-layer boards can be stacked to effectively implement a parallel winding structure without raising the cost of production significantly.

- **FEM Optimization:** FEM optimization can be very helpful in determine the flux distribution throughout a core. Additionally, the current distribution of arbitrary structures can be accurately solved with this tool. Methods and techniques associated with FEM analysis are presented in detail in Chapter 4.

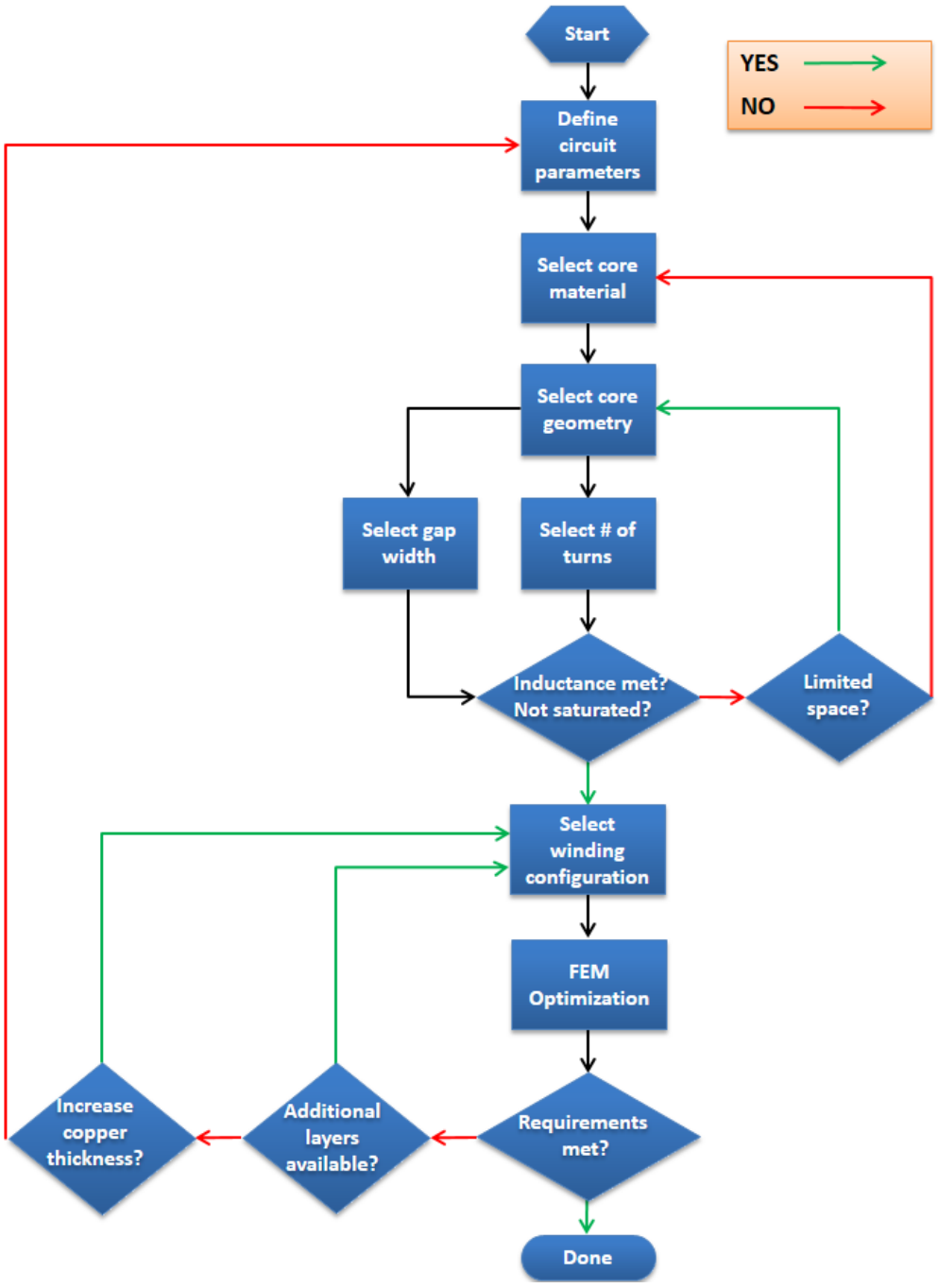


Figure 2.6: Planar filter inductor design process

Chapter 3

Initial Testing in Buck Converter Configuration

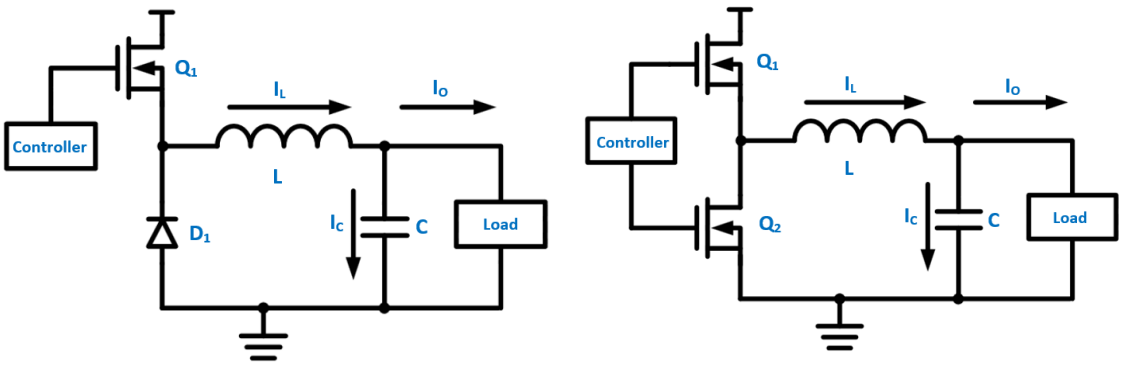
3.1 DC-DC Buck Converter

The buck converter is a common type of switch-mode converter used to step down a voltage. Its most common application is in power conversion for processor applications. Modern processors often operate between 0.8 V and 1.2 V. Efficiently converting a 12 V input voltage to about 1 V is a problem that has received widespread attention within the power electronics realm. A variety of aspects must be considered to effectively and efficiently perform power conversion. A suitable controlling algorithm must be developed for the converter switching. As switching speeds increase, board layout becomes a very influential factor on the efficiency of the buck converter. Utilizing appropriate switching devices is also important to minimize losses, particularly as switching frequency increases.

The filter inductor often provides a large percentage of the losses within the converter. Consequently, any improvements that can be made to the magnetic component can greatly increase the overall converter efficiency.

3.1.1 Overview

Buck converters can be classified into two distinct categories: asynchronous and synchronous. The asynchronous type offers decreased complexity at the cost of lower efficiency. The synchronous implementation requires the control of an additional switch, but often possess a higher conversion efficiency. The asynchronous and synchronous buck converter schematics are shown in Figure 3.1a and Figure 3.1b, respectively.



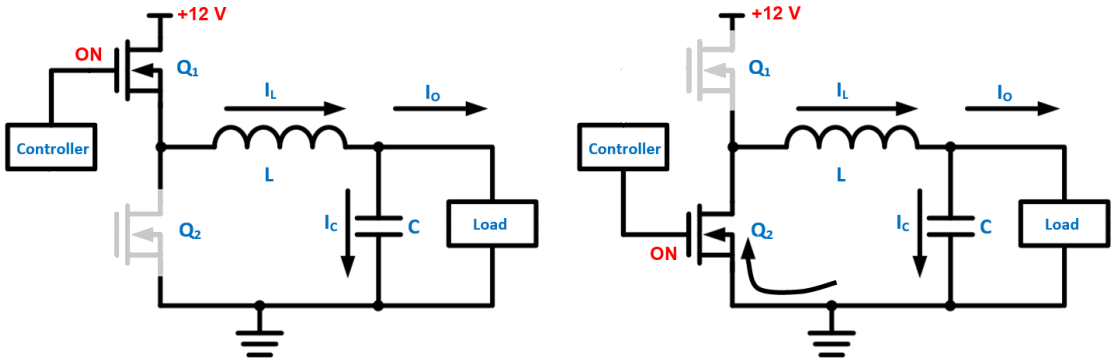
(a) Asynchronous buck converter

(b) Synchronous buck converter

Figure 3.1: Buck converter types

3.1.2 Operation

In order to fully understand the role a filter inductor plays in a buck converter application, it is necessary to observe the entire conversion algorithm. The synchronous buck converter has two states that each occur during one switching cycle. For a given duty cycle, D, and switching period, T, the switching FET denoted by Q_1 is "ON" for $D \cdot T$ seconds. For the remainder of the period, $(1 - D) \cdot T$, the synchronous rectifier denoted by Q_2 is "ON". These two states are portrayed in Figure 3.2a and Figure 3.2b.

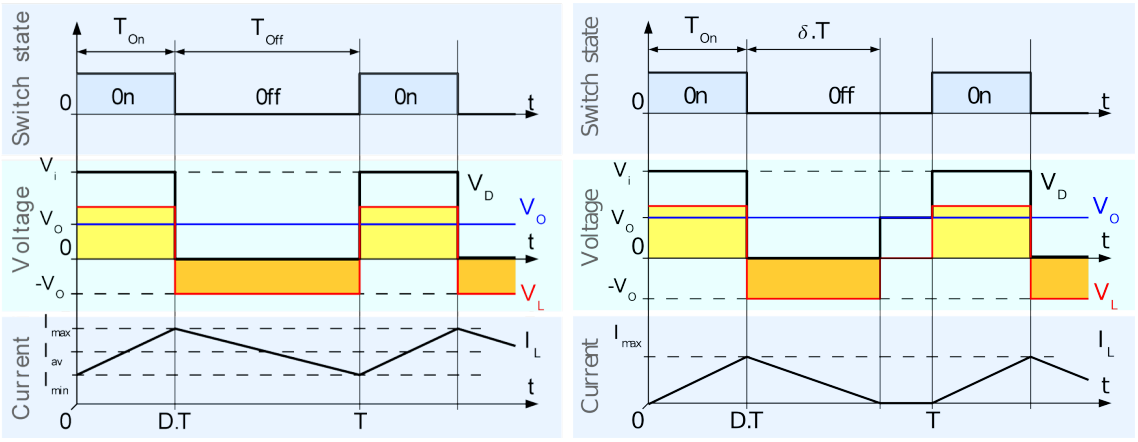


(a) Synchronous buck converter in the first state

(b) Synchronous buck converter in the second state

Figure 3.2: Buck converter states

A buck converter has two distinct modes of operation: continuous and discontinuous. These modes simply refer to the nature of the output current waveform. Continuous conduction mode (CCM) refers to a mode where the inductor current, I_L, is conducting over the entire period. When in discontinuous conduction mode (DCM), there exists a portion of the switching period in which I_L goes to zero. The two distinct modes of operation are shown in Figure 3.3. DCM often occurs when the amount of energy being drawn by the load drops below a certain point. Insufficient inductance can also cause a buck converter to operate in DCM.



(a) Continuous conduction mode (CCM) (b) Discontinuous conduction mode (DCM)

Figure 3.3: Buck converter operation modes

The required duty cycle for a buck converter is simply the ratio of input and output voltages.

$$D = \frac{V_O}{V_{In}} \tag{3.1}$$

For notational purposes, time constants t_{on} and t_{off} will be used to define the lengths of time that Q_1 is closed and open, respectively.

$$t_{on} = D \cdot T \tag{3.2}$$

$$t_{off} = (1 - D) \cdot T \tag{3.3}$$

The energy stored in an inductor is given as

$$E = \frac{1}{2} L \cdot I_L^2 \tag{3.4}$$

During the first operating state between $t = 0$ and $t = t_{on}$, the inductor current I_L is increasing. Thus, from Equation 3.4, it can easily be seen that the energy stored is increasing. During the second state, the inductor current is decreasing; thus, the inductor is dissipating energy. A simple analysis of the operating states shown in Figure 3.2 will reveal that the inductor voltage, V_L, takes on two possible values over the entire period. For the first state, shown in Figure 3.2a, the inductor voltage will be equal to $V_o - V_{in}$. During the second state, shown in Figure 3.2b, the inductor will be $-V_o$, neglecting the voltage drop across the switch Q_2. Consequently, the change in current through the inductor will be linear according to the fundamental relationship between current and voltage in an inductor.

$$V_L = L \frac{dI_L}{dt} \tag{3.5}$$

During the first state when Q_1 is closed and Q_2 is open, the increase in current through the inductor is given as:

$$\Delta i_{L_{on}} = \int_0^{t_{on}} \frac{V_L}{L} dt = \frac{(V_{in} - V_o)}{L} t_{on} \tag{3.6}$$

The decrease in inductor current when Q_1 is open and Q_2 is closed is given as:

$$\Delta i_{L_{off}} = \int_0^{T - t_{off}} \frac{V_L}{L} dt = -\frac{V_o}{L} t_{off} \tag{3.7}$$

Equations 3.6 and 3.7 define the AC component of the inductor current I_L. It can be noted from Figure 3.2 that the average inductor current is equal to the average output current, I_o. With this knowledge, the minimum and maximum values of the output current can be

solved for explicitly.

$$I_{o_{max}} = \bar{I_L} + \frac{\Delta i_{L_{on}}}{2} \tag{3.8}$$

$$I_{o_{min}} = \bar{I_L} + \frac{\Delta i_{L_{off}}}{2} \tag{3.9}$$

Combining Equations 3.6 - 3.9 and assuming a load resistance of R yields

$$I_{o_{max}} = \frac{V_o}{R} + \frac{1}{2}\left[\frac{(V_{in} - V_o)}{L} t_{on}\right] \tag{3.10}$$

$$I_{o_{min}} = \frac{V_o}{R} + \frac{1}{2}\left[-\frac{V_o}{L} t_{off}\right] \tag{3.11}$$

At this point, it is possible to utilize Equations 3.10 and 3.11 to determine the boundary conditions between continuous and discontinuous current modes. Using Equations 3.1 - 3.3, Equation 3.10 can be simplified as

$$\begin{aligned}
I_{o_{max}} &= \frac{V_o}{R} + \frac{1}{2}\left[\frac{(\frac{V_o}{D} - V_o)}{L} t_{on}\right] \\
&= \frac{V_o}{R} + \frac{1}{2}\left[\frac{V_o(\frac{1}{D} - 1)}{L} t_{on}\right] \\
&= \frac{V_o}{R} + \frac{1}{2}\left[\frac{V_o(\frac{1}{D} - 1)}{L} D \cdot T\right] \\
&= \frac{V_o}{R} + \frac{1}{2}\left[\frac{V_o(1 - D)}{L} T\right] \\
&= V_o\left[\frac{1}{R} + \frac{(1 - D)}{2Lf}\right]
\end{aligned}$$

Likewise, Equation 3.11 can be simplified in a similar fashion.

$$\begin{aligned} I_{o_{min}} &= \frac{V_o}{R} + \frac{1}{2}\left[-\frac{V_o}{L}(1-D)\cdot T\right] \\ &= \frac{V_o}{R} + \frac{1}{2}\left[-\frac{V_o(1-D)}{L}T\right] \\ &= V_o\left[\frac{1}{R} - \frac{(1-D)}{2Lf}\right] \end{aligned}$$

The obvious boundary condition for the buck converter to remain in CCM is $I_{o_{min}} = 0$. This can be seen graphically in Figure 3.3b. In the majority of converter designs, the input and output voltage as well as the load resistance will be specified. From this, it is possible to solve for a critical inductance value, L_c, to keep a buck converter operating at switching frequency, f, in continuous current mode.

$$I_{o_{min}} = 0 = \bar{I_L} + \frac{\Delta i_{L_{off}}}{2} \tag{3.12}$$

$$= V_o\left[\frac{1}{R} - \frac{(1-D)}{2L_c f}\right] \tag{3.13}$$

The critical inductance in Equation 3.13 can be solved for as a function of converter switching frequency, f.

$$L_c = \frac{(1-D)R}{2f} \tag{3.14}$$

Inductors are inherently large and lossy components, traits undesirable in power conversion processes. Thus, it is preferable to minimize the required inductance as much as possible. Equation 3.14 illustrates the relationship between critical inductance, duty cycle, load resistance, and frequency. From a practical design perspective, switching frequency is often the only variable that can be arbitrarily chosen. The duty cycle depends on the conversion ratio of output to input voltage. The resistance is dependent on the load requirements and will often vary depending on the activity of the load. Increasing the switching frequency

will reduce the inductance necessary to remain in continuous current mode. However, high frequency losses within the core and windings as well as switching losses will increase with operating frequency. High performance loads such as modern processors often require stable input current levels. This stipulation is much more strict than simply keeping a converter in CCM. Consequently, a central goal in converter design is minimizing current ripple. From Equation 3.6, the required inductance for maintaining a maximum current ripple, ΔI, is given as

$$L_{min} = \frac{D(V_{in} - V_o)}{f\Delta I_{max}} \tag{3.15}$$

In addition to low input current ripple, modern processors also demand a rapid transient response ability of the power supply. In other words, they require the ability to quickly switch between an idle state and a full-load state while maintaining the appropriate load voltage, V_o. The *transient response recovery time*, T_{trr}, is the worst case slew rate for a converter. Worst case in this sense implies a switch from an idle state of 0 A to a full load state of I_{pk} A.

$$T_{trr} = \frac{LI_{pk}}{V_o} \tag{3.16}$$

From Equations 3.15 and 3.16, a design trade-off becomes overt. A minimum inductance is necessary to satisfy rigorous load demands. However, transient capabilities are undermined by this increase in inductance. Increasing the switching frequency will reduce the minimum inductance and the T_{trr} concurrently. However, this method results in higher core losses and increased AC resistance through the windings.

3.1.3 Multi-Phase Architecture

Multi-phase buck converter implementations provide numerous benefits over single phase designs. Ohmic losses in single phase buck converters become unacceptable at high current levels. Dividing the current load among multiple phases allows each individual phase to operate more efficiently.

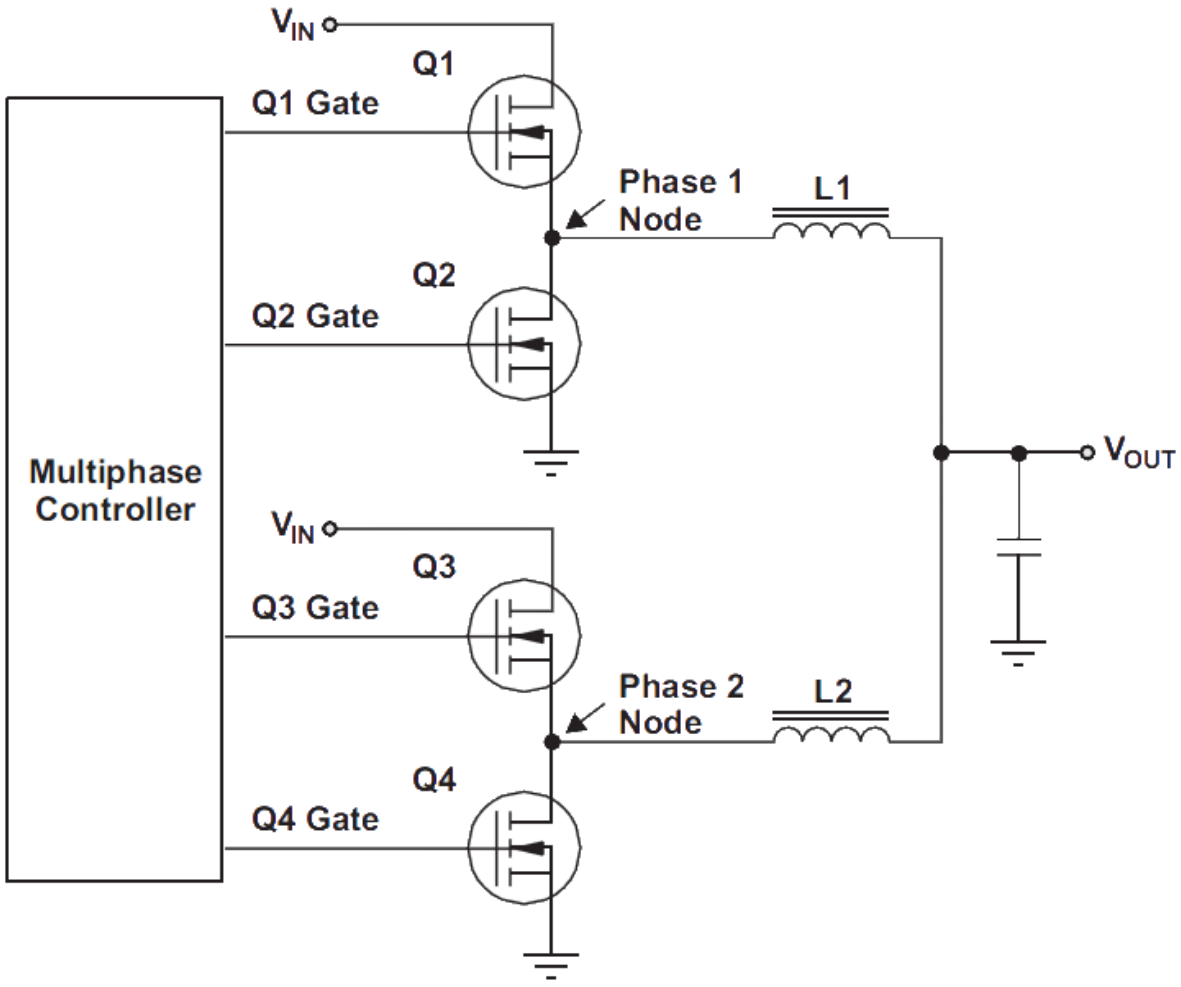


Figure 3.4: Multi-phase buck converter with two phases

Perhaps the most valuable aspect of a multi-phase implementation is its effect on current ripple and transient response time. For a given switching frequency, increasing the inductance will increase the transient response time of the system. However, a multi-phase buck implementation can reduce the necessary inductance for a given ripple level and in doing so, reduce the transient response recovery time. This is achieved through running multiple buck converters in parallel with equivalent time spacing in between phase switching. This has the effect of adding the individual ripple components out of phase. In doing so, the effective ripple current is reduced.

To illustrate this point, consider a three phase synchronous 12-1 V buck converter. The system must supply 36 A at 1 V with a maximum allowable ripple current of 3 percent. Performing this with a single phase converter presents two problems. The first problem is that of excessive copper losses. Designing an efficient buck converter to supply over 25 A is nearly impossible without the use of expensive techniques such as copper plating. In addition, a maximum current ripple of three percent is difficult to achieve while maintaining acceptable transient properties. To mitigate these problems, a multi-phase buck converter with three phases can be used.

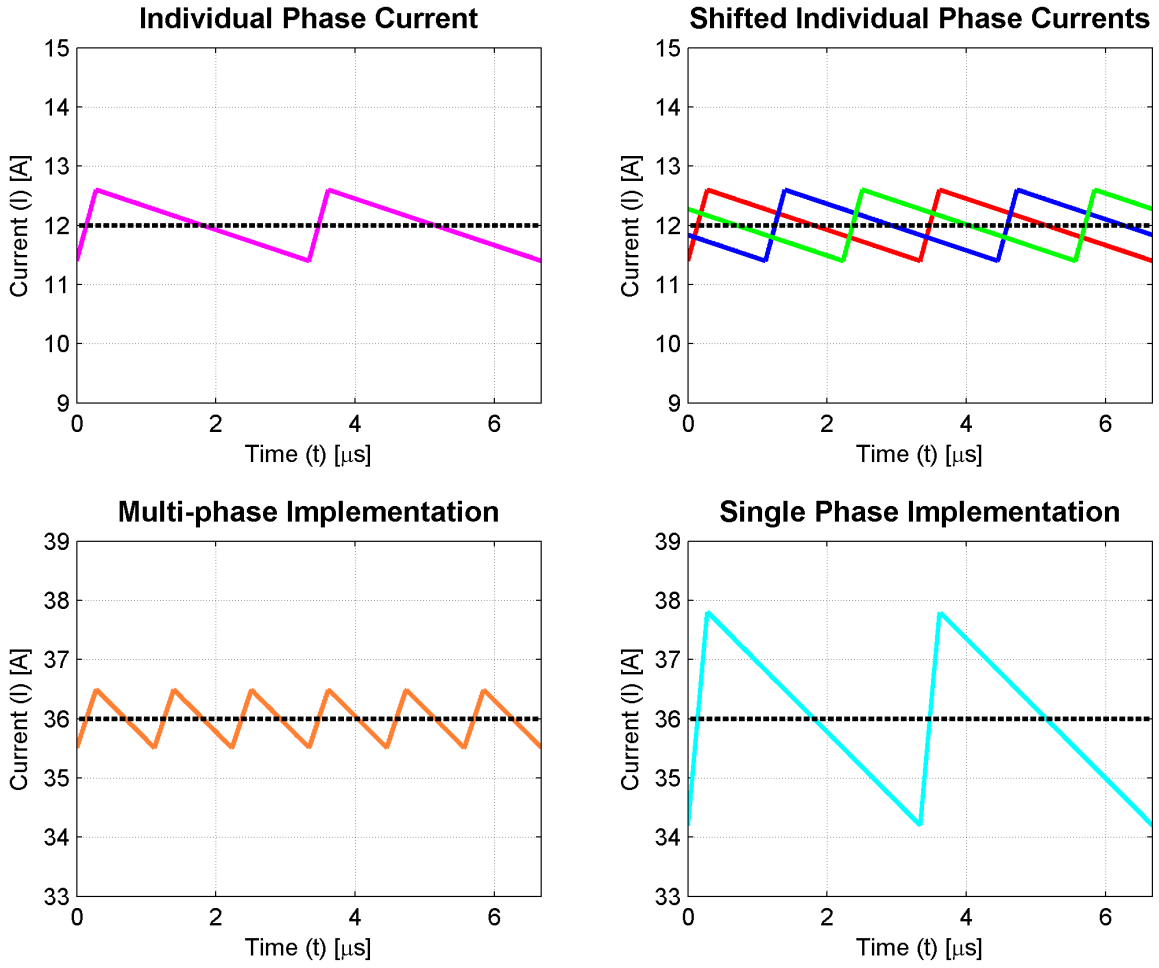


Figure 3.5: Comparison between single-phase and multi-phase buck converters

To minimize the current ripple, each phase should switch at evenly spaced intervals within the switching period. Figure 3.5 depicts how the phases are spaced over a period. Depending on the number of phases in the system, an appropriate phase delay is applied to each phase preventing the current ripple from adding constructively. This effectively reduces the overall current ripple of the system. A single phase implementation with a 10 percent ripple is presented as a benchmark. In this particular example, the multi-phase buck converter with three phases each having a 10 percent ripple current contributed to a total converter ripple current of only 2.74 percent. In general, the multi-phase ripple current percentage will be that of each individual phase divided by the number of phases.

$$\% \text{ ripple} \approx \frac{\text{phase ripple } \%}{\#\text{ of phases}} \tag{3.17}$$

Equation 3.17 works under the assumption that the phases are optimally spaced. The transient response of the multi-phase buck converter will improve as a result of the reduced inductance. For a system with N phases, the minimum inductance per phase can be reduced by a factor of N and still meet the desirable ripple current. Furthermore, from Equation 3.16, the transient response recovery time will decrease by a factor of N.

3.2 Buck Converter Integration and Initial Testing

In many ways, the most challenging aspect of developing a planar inductor for use in buck converters is the testing methodology. The designer has two broad categories of testing available: integrated and stand-alone. In addition, empirical and numerical methods should be utilized to minimize the amount of hardware testing. The buck converter being developed had specifications outlined in Table 3.1.

Parameter	Value
Output Voltage	1 V
Input Voltage	12 V
Output Current	12 - 25 A
Output Ripple Current	15 %
Switching Frequency	100 - 500 kHz

Table 3.1: Buck converter specifications

3.2.1 Testing Strategy

Although printed circuit board technology offers a variety of benefits, the cost and turn-time associated with prototyping are distinct drawbacks. The buck converter being developed underwent multiple board iterations over relatively short periods of time. Integrating a planar inductor into each of these board designs would be time and cost preventative under most budgets. Consequently, a testing strategy was developed that sacrificed performance for modularity. Eight different winding structures were considered for use in the buck converter. The developed system relies on "swappable" boards to get fast and consistent experimental results. The testing strategy involves connecting the buck converter to swappable inductor cards as shown in Figure 3.6.

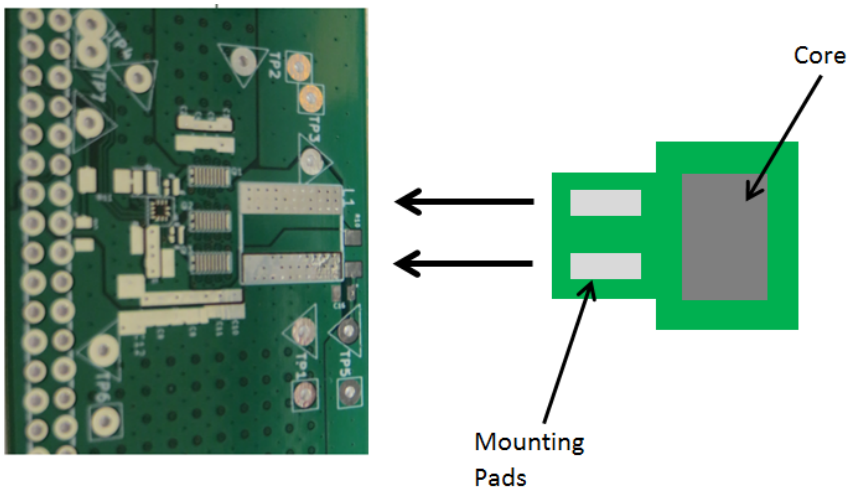


Figure 3.6: Swappable inductor board concept

The use of these cards allows may inductors to be considered. Eight different inductor boards with varying winding strategies and cores were designed. Figure 3.7 shows the various breakout boards. The boards were designed for use with four different core geometries, shown in Figure 3.8 [20],[21],[22]. For each geometry, one and two turn implementations were developed. This strategy allows for arbitrary creation of a variety of inductors, all possessing different characteristics.

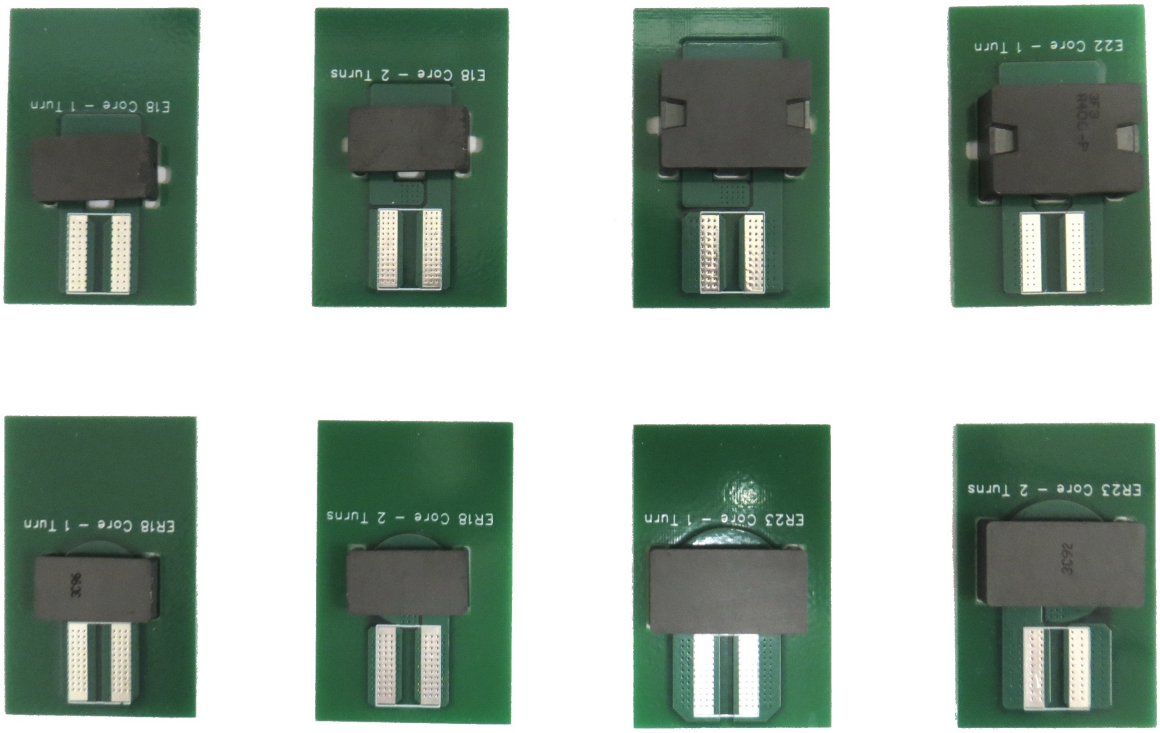
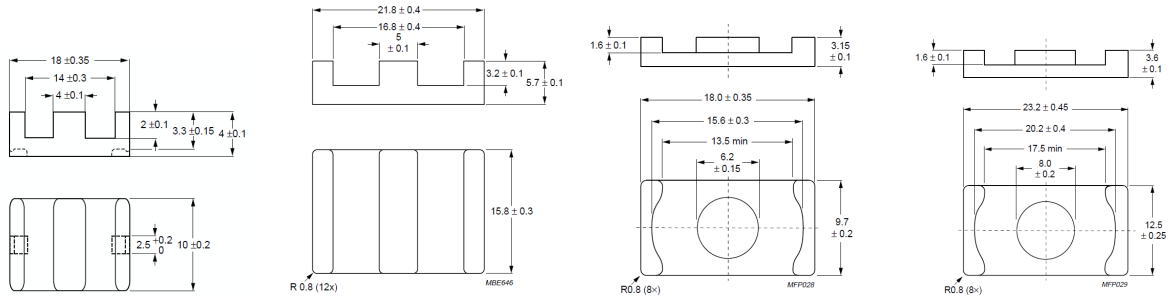


Figure 3.7: Inductor breakout boards. Cores: E18 (top left), E22 (top right), ER18 (bottom left) ER23 (bottom right)



(a) E18 geometry (b) E22 geometry (c) ER18 geometry (d) ER23 geometry

Figure 3.8: Ferroxcube® planar core diagrams

Mounting

The contacts used to interface between the buck converter and inductor breakout board were not able to be mounted directly. Interface pins were necessary to connect the two boards; this is shown in Figure 3.9. Although these connections contribute a fair amount of DC resistance to the inductor structure, the added resistance will be consistent across all testing. Thus, when comparing the various inductors tested in this way, the properties of the inductor can be extrapolated. Another non-ideal consequence of this testing method was the introduction of a loop through the mounting bars. This additional loop seemed to cause a small amount of current ripple in addition to what was expected from the buck converter design.

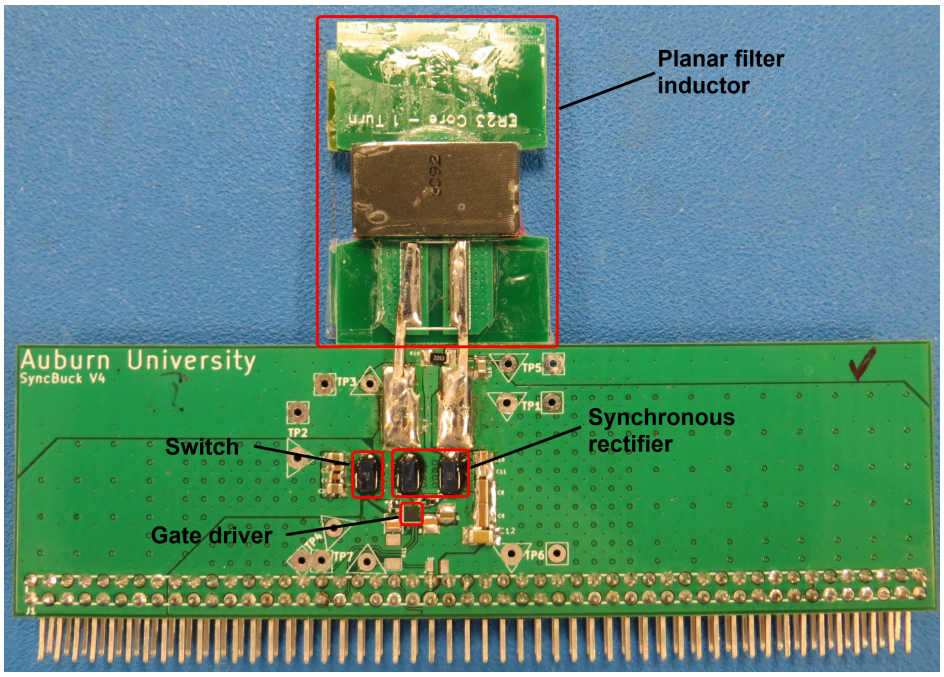


Figure 3.9: Inductor mounting strategy

Gapping

The ability to achieve and control the inductance of a planar magnetic structure is paramount in power electronic applications. The inductance of planar ferrite core inductors is determined by the number of turns, the core material and the air gap, with the latter

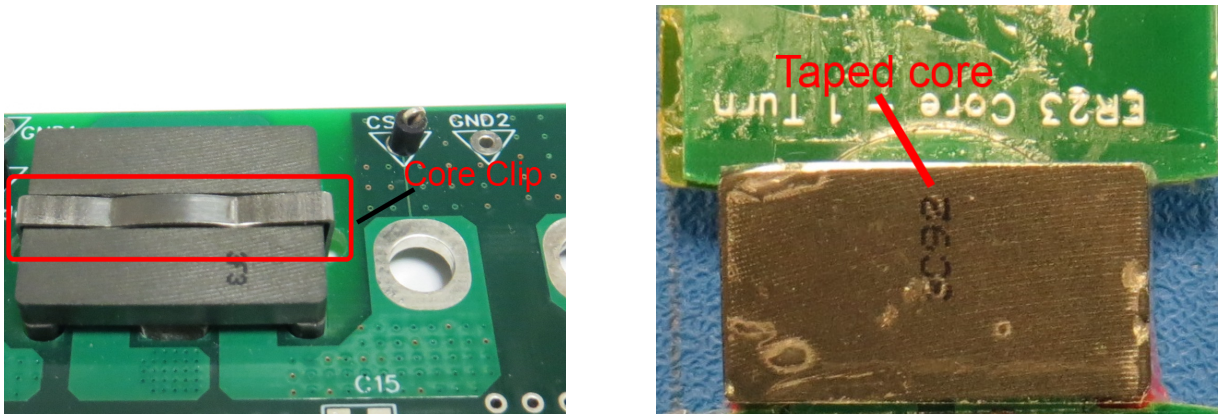
being the most critical. Various methods are available for achieving a certain air gap width. The most accurate gap widths are custom cut by the manufacturer or a third party vendor. For high performance and mass production applications where parameter control is critical, machining is the preferable gapping method. For prototyping and iterative design situations, the cost associated with machine gapping makes the method impractical. A cheaper but still relatively accurate method for gapping is the use of a spacer. Shim stock plastic is a low-cost material that comes in a plethora of thicknesses making it ideal for ferrite gapping. Its relative permeability, μ_r, is approximately one, giving it identical magnetic properties to that of air. A couple of factors must be considered if using sheet plastic as a gapping material. Some flexibility as to where the gap can be located is lost when using plastic fillers. A single gap in the middle post is not possible with this strategy. Instead, the gap must extend across all three legs of the core. A comparison between the gap types is illustrated in Figure 3.10. It should be noted that the width of the distributed gap in Figure 3.10b is half the width of the machined middle leg gap in Figure 3.10a. However, the effective reluctance of the cores will be identical.

(a) Machined middle leg gap with air fill (b) Distributed gap with a plastic filler

Figure 3.10: Types of gaps for ferrite cores

Another consideration when utilizing plastic fillers is the core assembly pressure. Machined cores generally have clamps that apply the proper amount of pressure for a seamless and consistent reluctance path; an example is shown in Figure 3.11a. Cores that do not have custom gaps often have no clamp for holding the two pieces together. The core requires a certain amount of holding pressure outlined by the manufacturer to ensure the specifications

are met. There are a couple ways achieve the proper holding pressure for unmachined cores, with none of them being perfect. Many sources suggest employing an adhesive between the core halves. Although this provides sufficient holding pressure, the exact width of the gap becomes unpredictable with the added adhesive. Additionally, this method makes removing the cores a laborious if not impossible task. The approach taken in this research was to simply tape the cores together very tightly. If done correctly, the pressure applied by the tape is sufficient to maintain a consistent reluctance path throughout the core. An example of a taped core is shown in Figure 3.11b.



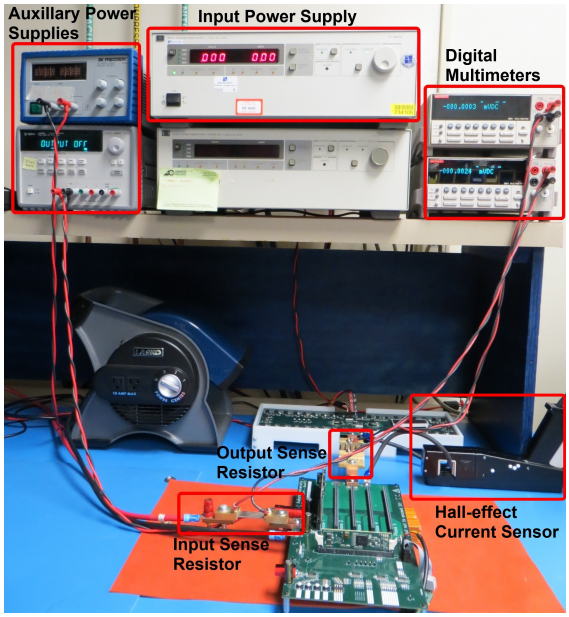
(a) Core pressure applied by metal clip

(b) Core pressure applied by tape

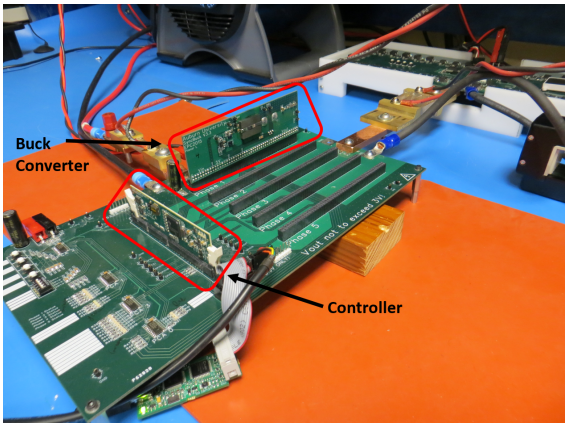
Figure 3.11: Methods for applying appropriate core holding pressure

Testing Setup

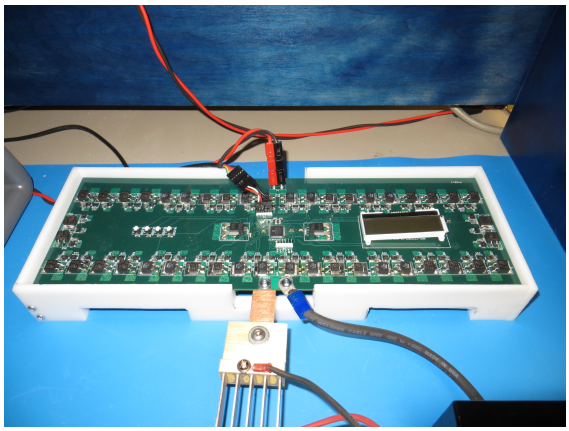
The performance of each inductor was characterized by the efficiency of the overall buck converter. The losses due to the various components of the buck converter were well-documented through simulation and experimental results. Consequently, the performance of various inductors could be characterized indirectly by observing changes in buck converter efficiency. A complete and comprehensive analysis of a buck converters performance necessitates the collection of efficiency data over a wide range of switching frequencies and load currents. To expedite this collection process, an automated tester was developed to sweep a specified range of operating conditions and record efficiency data.



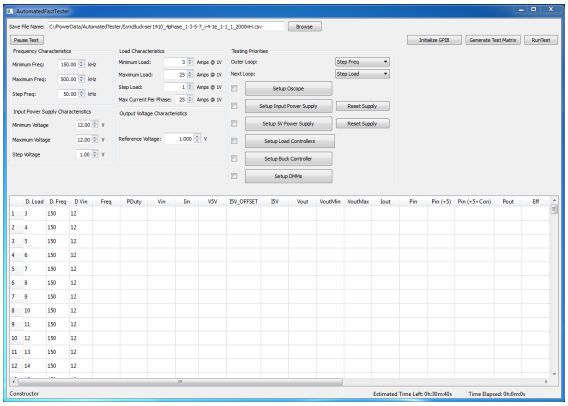
(a) Overall test setup



(b) Carrier Board



(c) Electronic load board



(d) Graphical user interface

Figure 3.12: Buck converter test setup

The automated tester was comprised of four primary components. The system in its entirety is shown in Figure 3.12a. Various power supplies are used to provide the input power to the buck converter as well as auxiliary power to the control circuitry. The carrier board, shown in Figure 3.12b, interfaces up to five buck converter phases with the control circuitry. The electronic load board, shown in Figure 3.12c, dynamically controls the load current. To verify the the current being drawn by the load, two independent methods are employed to ensure accuracy. The sense resistors and hall-effect current sensor are outlined

in Figure 3.12a. A simple GUI, pictured in Figure 3.12d, was created to allow the user to specify sweep ranges for operating frequency as well as output current.

3.2.2 Inductance Design

Achieving a precise inductance when building an inductor by hand can be very challenging. The core geometries available for planar magnetics are not conducive to determining what the inductance of a structure will be through a closed-form expression. Most of the closed for expressions for determining the inductance of a structure are suitable only for simple geometries (i.e., loops, squares, etc.). When considering inductors with multiple turns, flat traces, and unusual geometries, a precise determination of the inductance of a structure is often a difficult problem. Fortunately, core manufactures provide empirical data to assist the designer in achieving a target inductance. Core saturation is an additional factor that must be considered when developing filter inductors. Saturation can be defined in two ways. Graphically, it is defined as the point in the B-H curve where the slope is zero or the point at which the B-H curve becomes nonlinear. The latter definition is often referred to as soft saturation.

The inductance of a planar magnetic structure is controlled by three factors: the core material and geometry, the number of turns and the gap width. The ferrite core materials designed for power electronics all have similar material permeability. Thus, the volume of the core heavily dictates the available inductance. The number of turns has the largest effect on the inductance. However, an optimal inductor design will use a minimum number of turns to reduce the winding resistance as much as possible. The gap width also has a large influence on the inductance. Further, the gap width in conjunction with the number of turns must be optimized to prevent the core from saturating. The inductance factor is an empirical value provided by the core manufacturer to quickly determine the inductance of a structure. The total inductance of a magnetic structure can be determined by multiplying the inductance factor, A_L by the number of turns squared, N^2.

Gap Width Determination

Manipulating the magnetic component's inductance through gap width variation is conducive to quickly prototyping and testing inductors. The windings often associated with planar magnetics are located on PCB substrates, making them difficult to change quickly. However, the spacer method of inductor gapping discussed previously provides a quick and simple way to vary the inductance of a planar component. Core manufacturers provide empirical data that assists with achieving a certain inductance by altering the gap width.

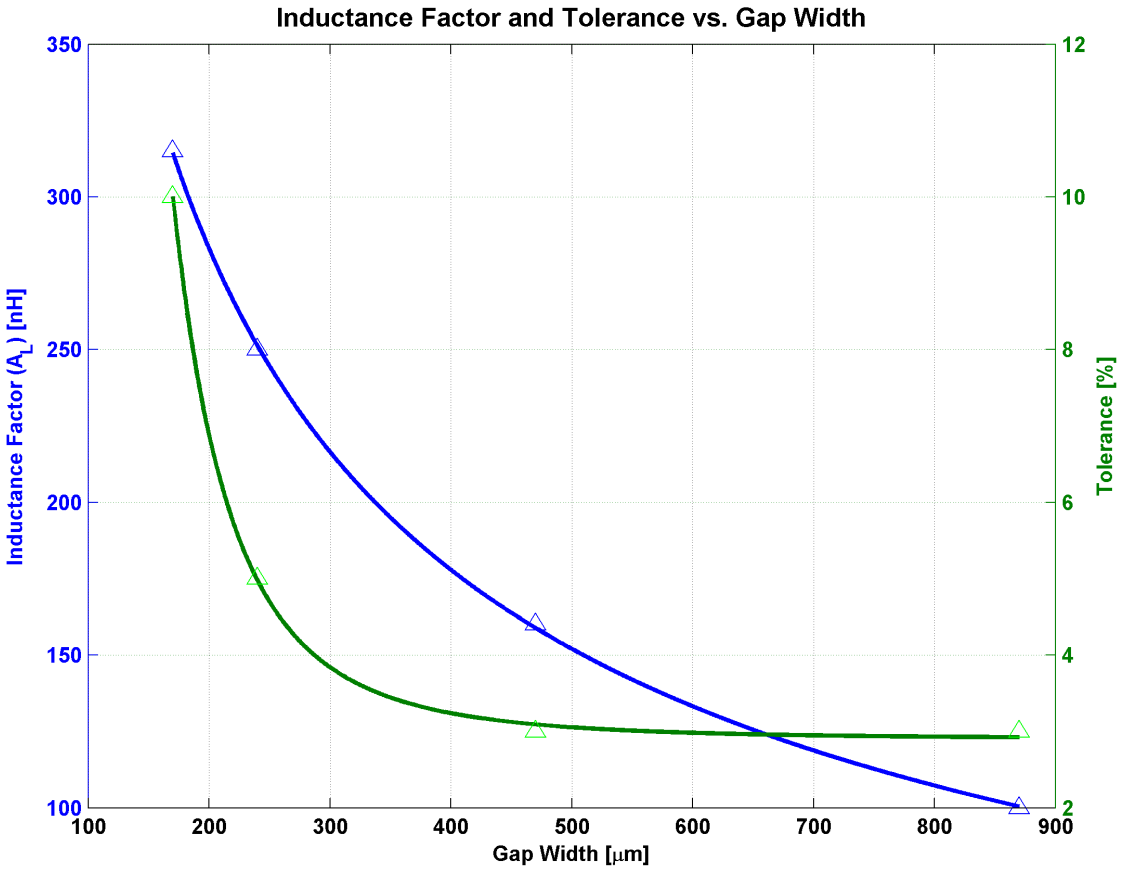


Figure 3.13: Relationship between gap width, inductance factor, and inductance tolerance

Figure 3.13 illustrates some of the key points regarding the gap width of an inductor. The ability to precisely control the inductance is inversely related to the gap width. In other words, the ability to form a precise inductance is more difficult as the gap is made smaller.

This is a consequence of permeability variations within the core material. The relationship between effective permeability and relative permeability is given as

$$\mu_{eff} = \frac{\mu_c}{1 + \mu_c \cdot \frac{l_g}{l_c}} \tag{3.18}$$

where μ_c is the relative permeability of the core, l_g is the gap width and l_c is the effective length of the core. As the ratio of $\frac{l_g}{l_c}$ gets smaller, variations of the core permeability are amplified. This point is illustrated by the green curve in Figure 3.13.

3.3 Efficiency Results

Efficiency data was collected on around 50 planar inductor variations that translated into thousands of data points and efficiency curves. For brevity, a couple of inductors that form a representative sample are presented here for comparison.

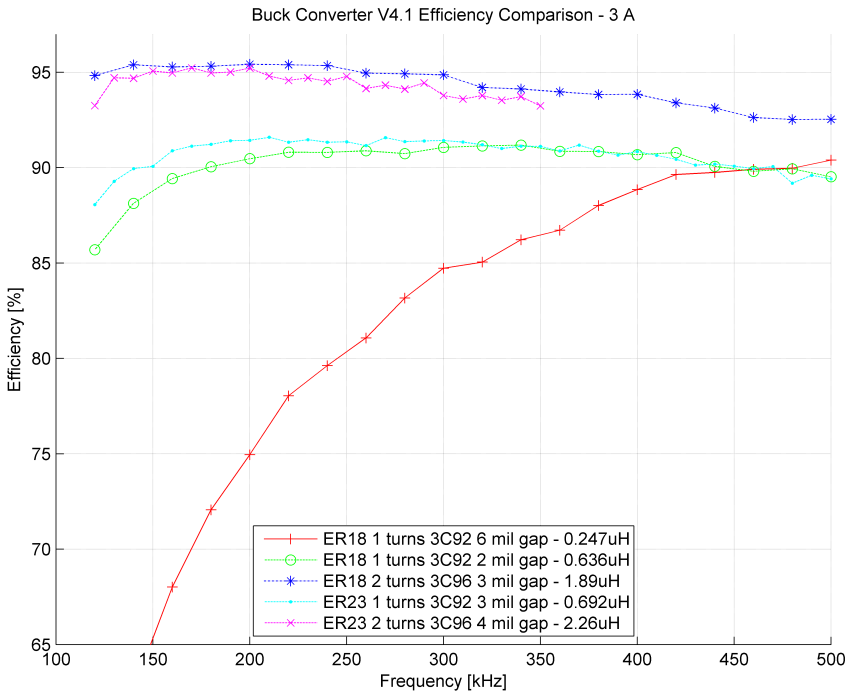


Figure 3.14: Buck Converter V4.1 Efficiency comparison - 3A

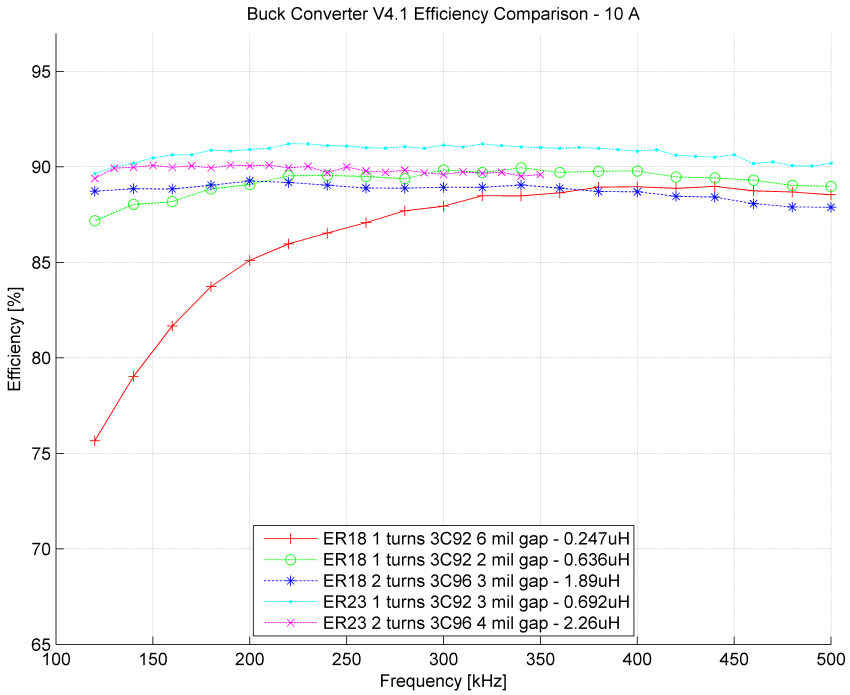


Figure 3.15: Buck Converter V4.1 Efficiency comparison - 10A

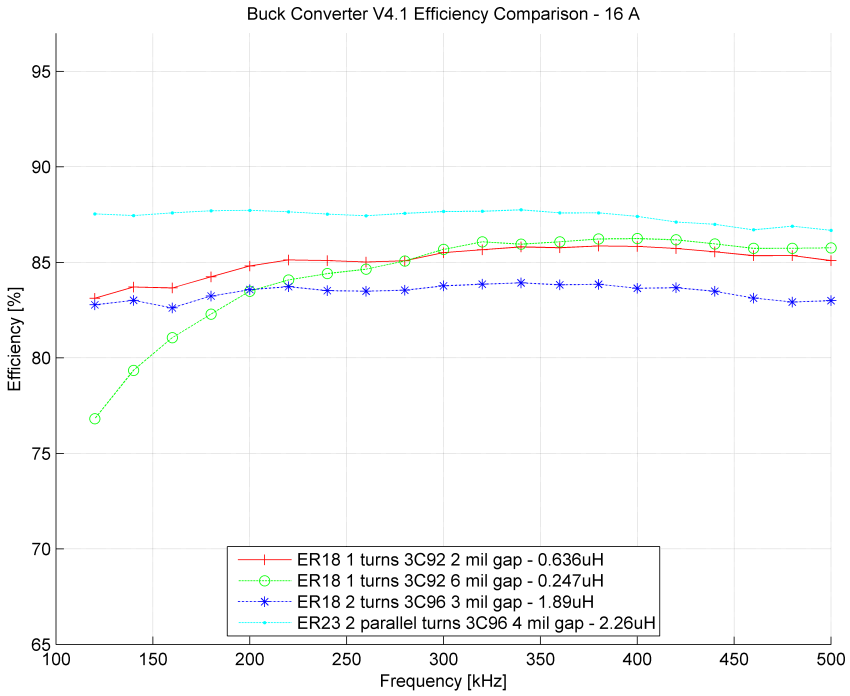


Figure 3.16: Buck Converter V4.1 Efficiency comparison - 16A

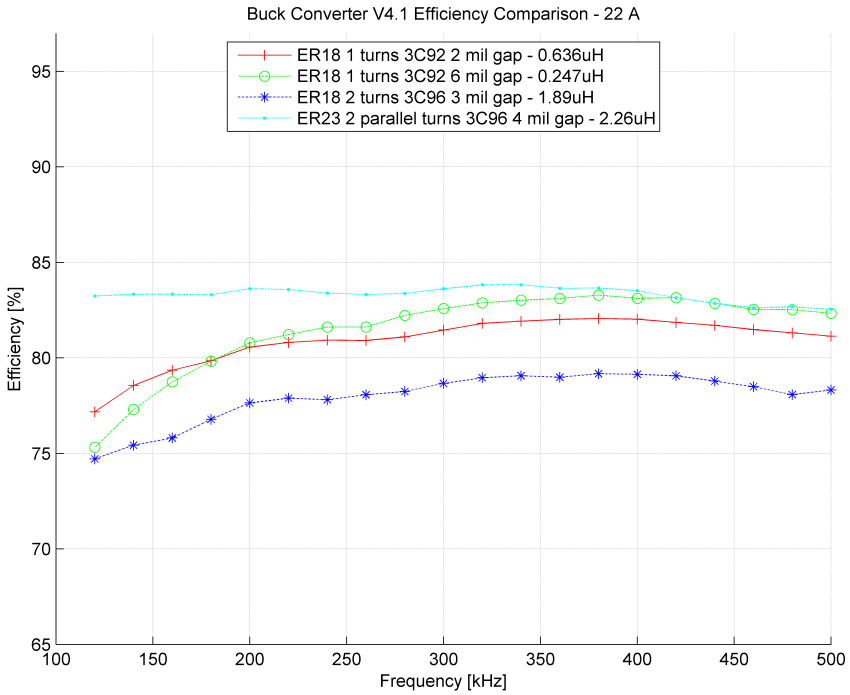


Figure 3.17: Buck Converter V4.1 Efficiency comparison - 22A

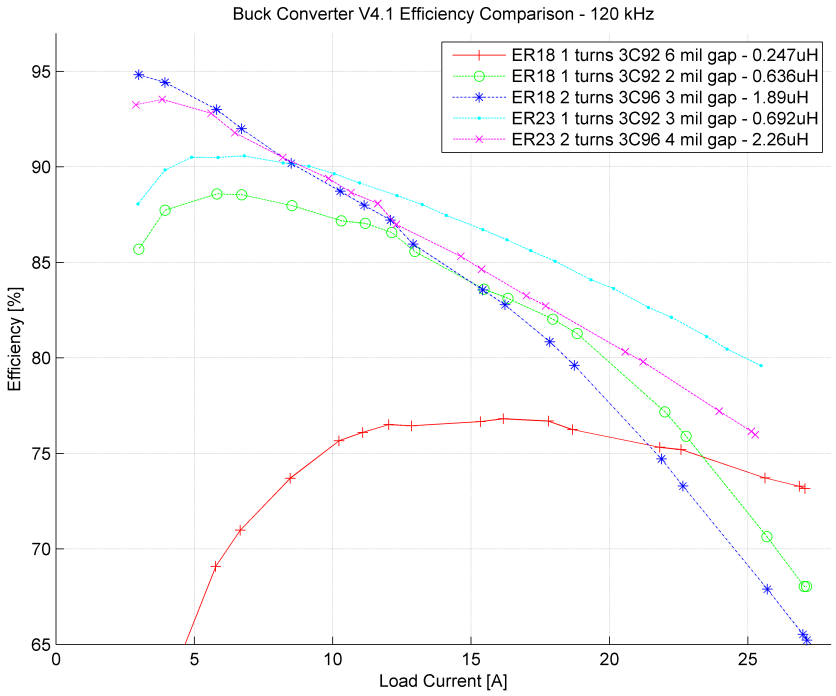


Figure 3.18: Buck Converter V4.1 Efficiency comparison - 120kHz

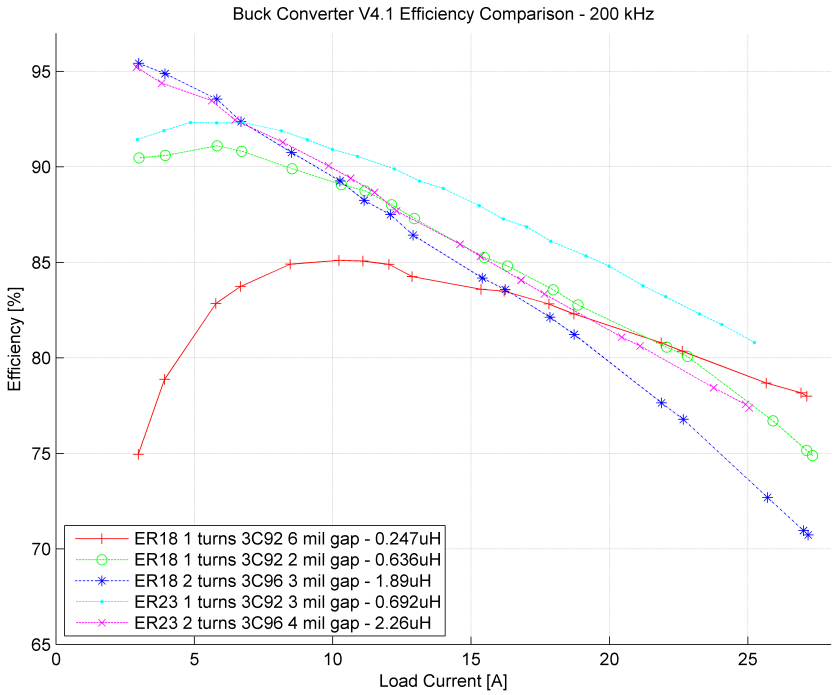


Figure 3.19: Buck Converter V4.1 Efficiency comparison - 200kHz

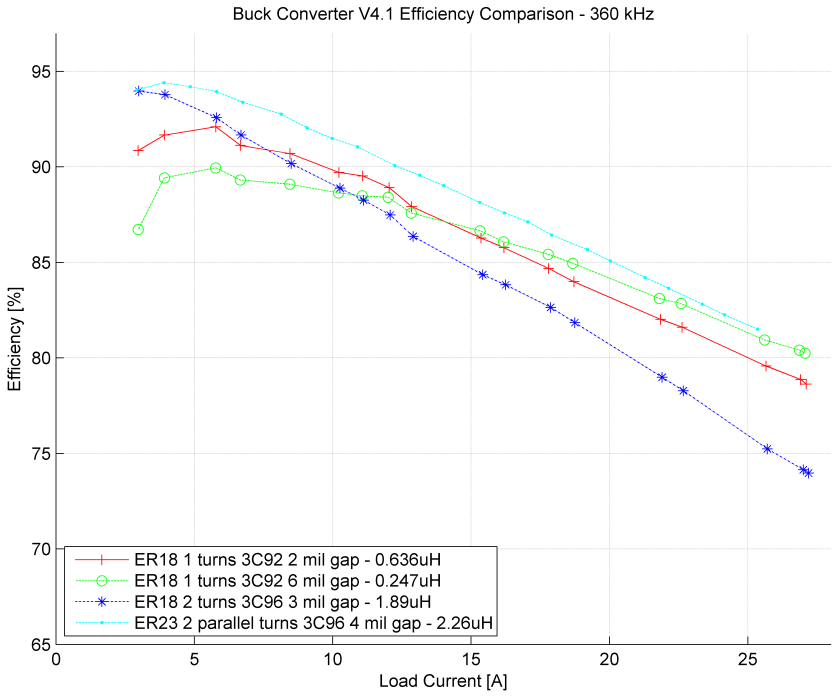


Figure 3.20: Buck Converter V4.1 Efficiency comparison - 360kHz

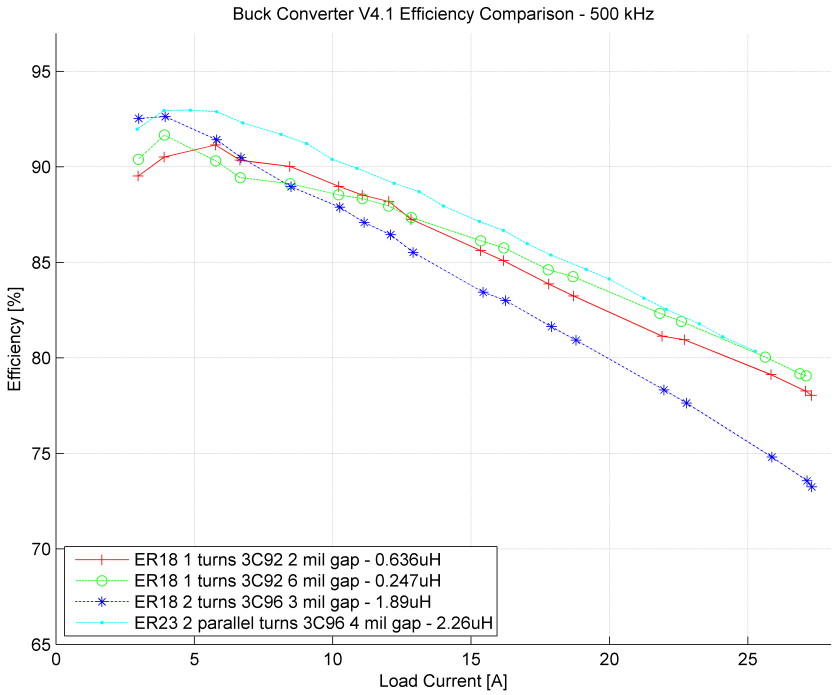


Figure 3.21: Buck Converter V4.1 Efficiency comparison - 500kHz

Figure 3.14 depicts a critical pitfall of not providing enough inductance for a given design. The red trace represents the efficiency of a 1-turn inductor providing about 247 nH. This inductor has an extremely low efficiency measurement at low switching frequencies. This is a result of the large ripple current forcing the converter into DCM, as discussed in Section 3.1.2. Since the load current in this case is so low, the ripple inductance must also be very small to avoid being pushed into DCM. As the switching frequency increases, the efficiency increases as a result of a smaller ripple current. This point can be further emphasized by observing the next largest inductances represented by the green and teal lines. Both of these inductors have a slightly larger inductance than the first one, but still not enough to avoid DCM completely. In contrast, the inductors represented by the blue and purple lines provide about 2 μH of inductance and operate in CCM over the entire frequency range.

Figures 3.15 - 3.17 depict the same inductors at progressively higher load currents. Some additional insight can be extracted by observing this progression. First, as the load current increases, a larger ripple current is required to force the converter into saturation. Hence, the low frequency efficiency results for the 250 nH inductor are not as bad. Second, the efficiency of the inductors operating in CCM decreases due to additional ohmic losses. This point is clearly illustrated by observing the ER18, 2 turn inductor. It provided the highest efficiency when operating at lower loads; however, its efficiency dropped off more quickly than the others since it had the highest DC resistance of the compared inductors.

Figures 3.18 - 3.21 depict efficiency for the same four inductors plotted vs load instead of frequency; the same characteristics can be viewed from another angle. Another limiting factor can be faintly seen in Figure 3.18. The ER18, 2 turn inductor, in addition to having a higher DCR, also exhibits core saturation at the higher load currents. The curve begins to slope downward around 20 A, indicating the core may be slightly saturation.

Chapter 4

Finite-Element Modeling and Analysis

4.1 Overview

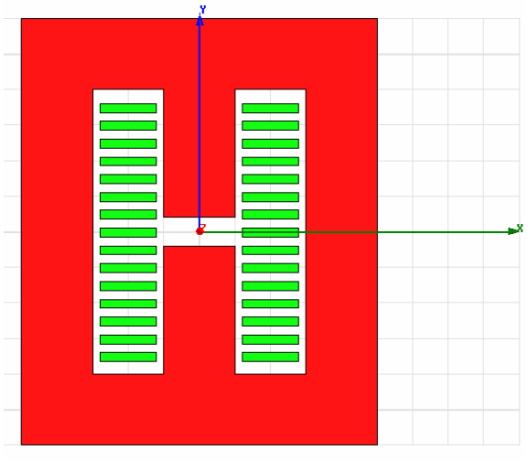
Design and analysis of magnetic components becomes increasingly difficult as the structure increases in complexity. This level of complexity is often unavoidable when developing PCB-based magnetic components [23]. The principal reasoning for the complexity is the winding structure. Multiple layers are necessary in nearly all cases to satisfy component loss constraints [24]. Consequently, an intricate method of interconnecting the various layers is often required. In most cases, this introduces a significant level of complexity when compared to common surface mount inductors such as a toroid - which has very well established closed form solutions for loss, inductance, etc.

The finite-element method (FEM) is a popular numerical technique for approximating solutions to differential equations with well-defined boundary conditions [25]. Maxwell® software developed by the Ansoft Corporation is a popular FEM suite utilized primarily for low frequency electromagnetics. The advent and widespread availability of high performance computers have made this technology accessible to most designers. This type of analysis is often employed when designing arbitrary electromagnetic structures. It uses simple variational calculus methods to minimize an error function until a specified error level is reached [26].

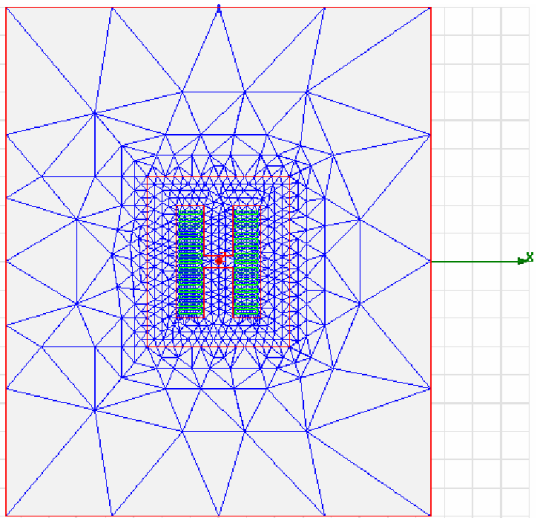
4.1.1 Mesh Operations

The most basic mechanics of an FEM solver involve partitioning the structure into a collection of tetrahedral elements (often referred to simply as elements). Modeling can be performed in 2D as well as 3D, with the latter requiring considerably greater computational

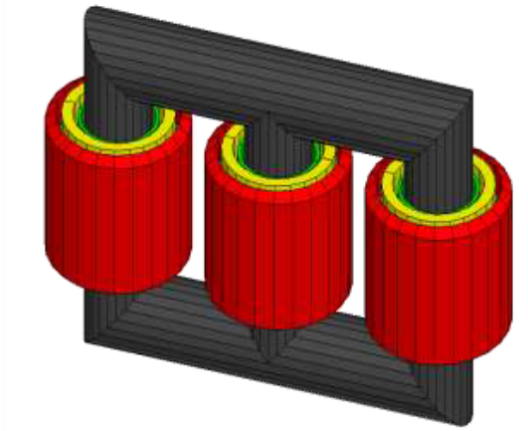
power. Figure 4.1a shows an inductor modeled in 2D with its associated mesh shown in Figure 4.1b. The general tetrahedral shape is reduced to triangles for the 2-dimensional case. It should be noted that the elements within the core (red) and the traces (green) are considerably smaller than the elements found outside the core. This provides more resolution in areas of the design that are critical to component performance. Modeling a component in 2D is often insufficient when modeling components that do not posses a significant degree of symmetry. Furthermore, a 2D model will often convey inaccurate results since it lacks so much information about the rest of the structure [27].



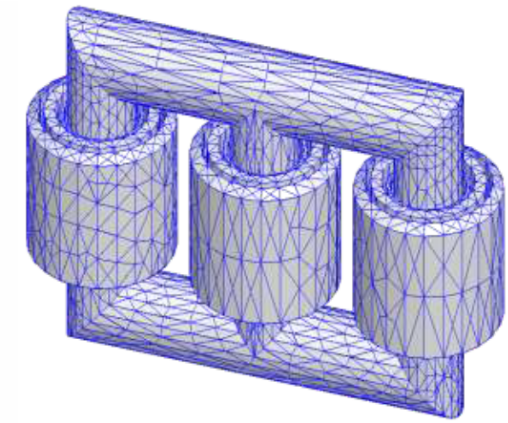
(a) Gapped inductor modeled in 2-D



(b) 2-D mesh - triangles



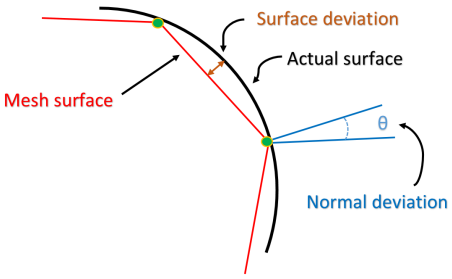
(c) Coupled inductor modeled in 3-D



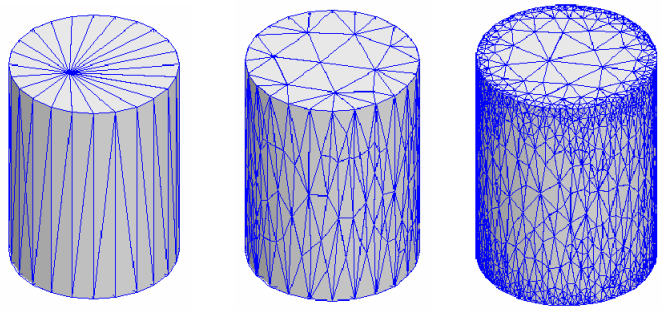
(d) 3-D mesh - tetrahedral

Figure 4.1: Examples of mesh grids in 2D and 3D solvers

A 3D modeling scheme, although more computationally intensive, delivers information about the entire structure rather than just a cross section. A 3D coupled inductor model is shown in Figure 4.1c along with its corresponding mesh grid shown in Figure 4.1d. When modeling in 3D, the meshing algorithm becomes more complicated since multiple dimensions of the tetrahedral elements must be considered. The trade-off between size, accuracy and required computing power is much more important in 3D modeling [23]. Maxwell 3D possesses an engine to adaptively assign mesh patterns to a structure based on desired values of maximum and minimum lengths and widths. Since the mesh elements are inherently restricted to linear tetrahedrals, the algorithm used to describe curved and spherical surfaces to the solver is critical. The mesh engine provided by Maxwell 3D will iteratively assign a mesh pattern to the structure, as shown in Figure 4.2b, until an acceptable approximation is found based on the tolerated amount of error depicted in Figure 4.2a.



(a) Diagram of surface errors resulting from mesh operations



(b) Adaptive mesh operations

Figure 4.2: Mesh operation on rounded surfaces

4.1.2 FEM Solvers

Maxwell 3D offers a variety of field solvers tailored to various situations. These four solvers are summarized below:

1. **Magnetostatic** - This solver computes the static (DC) magnetic fields due to DC current in conductors, permanent magnets, and static magnetic fields represented by boundary conditions. The quantity solved for is the magnetic field strength, H; current

density (J) and magnetic flux density (B) are automatically calculated from the magnetic field. Derived quantities such as energy and inductance can also be calculated.

2. **Eddy Current Analysis** - This solver computes the steady-state, time-varying (AC) magnetic fields at a given frequency, thus making this a frequency domain solution. The source of the magnetic fields can be a sinusoidal AC current sources as well as time-varying magnetic fields enforced as boundary conditions. The quantities solved for are magnetic field (H) and magnetic scalar potential (Ω). Similar to the magnetostatic solver, quantities such as current density (J), magnetic flux density (B), and inductance (L) can be solved for as well. One limitation of this solver is its inability to handle nonlinear magnetic materials.

3. **Transient Analysis** - This time domain solver computes the magnetic fields within the structure at discrete time steps. The solver formula utilizes the current vector potential in solid conductors as well as the scalar potential over the entire solution window. Excitation sources can take the form of arbitrary time-varying current within the conductors and permanent magnets. Magnetic field (H) and current density (J) are solved for initially and in turn used to find other quantities such as power loss and flux linkage.

4. **Electrostatic** - This solver computes the static (DC) electric fields. The possible sources of the static electric fields are applied potentials and charge distributions. The quantity solved for in this analysis is electric scalar potential (Φ). In turn, the electric field (E), electric flux density (D) are automatically calculated. Derived quantities such as capacitance and energy can be found from the basic field quantities.

For design and analysis of an inductor, the current density and flux density are the most pertinent pieces of information. Consequently, the magnetostatic and eddy current solvers were utilized for the analysis of the planar inductor. Since the inductor current will be a

small AC component superimposed on a larger DC component, these two solvers provided sufficient information for determining the flux density and current distribution.

Magnetostatic Solver

The magnetostatic solver provides a tool to calculate the flux density due to the DC component of the current. Filter inductors used in buck converter applications often possess a large DC current component, making this analysis all the more important. The solver computes the magnetic field in a two step process. The conductors (perfect and non-perfect) are first analysed to determine the current density, J. The current density in a conductor is proportional to the potential difference as expressed in Equation 4.1.

$$J = \sigma E = -\sigma \cdot \nabla \phi \tag{4.1}$$

Given an arbitrary volume, V, the current flow out of the volume must equal the net change in charge within the volume.

$$\int_S \mathbf{J} \cdot d\mathbf{A} = -\frac{d}{dt} \int_V \rho \, dV = -\int_V \frac{\partial \rho}{\partial t} dV \tag{4.2}$$

The surface, S, encloses the volume, V, with charge density, ρ. From the divergence theorem, the first term in 4.2 can be expressed as a divergence.

$$\int_S \mathbf{J} \cdot d\mathbf{A} = \int_V \nabla \mathbf{J} \cdot dV \tag{4.3}$$

From Equations 4.2 - 4.3, the continuity equation can be found as

$$\int_V \nabla \cdot \mathbf{J} dV = -\int_V \frac{\partial \rho}{\partial t} dV \tag{4.4}$$

This relationship holds for any volume regardless of size, shape, or location. Thus, the integration over the volume is arbitrary and can be dropped for simplification.

$$\nabla \cdot \mathbf{J} = -\frac{\partial \rho}{\partial t} \tag{4.5}$$

Since the magnetostatic solver only analyzes the DC component of the current, the charge density within a given region will not vary with time. Equivalently,

$$\nabla \cdot \mathbf{J} = -\frac{\partial \rho}{\partial t} = 0 \tag{4.6}$$

Combining the result in Equation 4.6 with Equation 4.1, a solution can be obtained in terms of electric potential, ϕ.

$$\nabla \cdot (\sigma \cdot \nabla \phi) = 0 \tag{4.7}$$

Once the current density is computed, the static magnetic fields can be calculated utilizing a system of equations derived from Gauss' law for magnetism and Ampere's law.

$$\oiint_{\partial\Omega} \mathbf{B} \cdot d\mathbf{S} = 0 \tag{4.8}$$

$$\nabla \times \mathbf{B} = \mu \left(\mathbf{J} + \epsilon \frac{\partial \mathbf{E}}{\partial t} \right) \tag{4.9}$$

In a similar fashion to Equation 4.6, the time varying term in Equation 4.9 can be set to zero in the magnetostatic case.

$$\nabla \times \mathbf{B} = \mu \mathbf{J} \tag{4.10}$$

Once a solution for the magnetic field has been found, a variety of parameters including energy storage and inductance can be computed.

$$U = \frac{1}{2} L I^2 = \frac{1}{2} \int_V H \cdot B \, dV \tag{4.11}$$

$$L = \frac{1}{I^2} \int_V H \cdot B \, dV \tag{4.12}$$

Eddy Current Analysis

The AC component of the current waveform was analyzed using the eddy current analysis tool within Maxwell 3D. This solver treats all values as phasors, precluding the inclusion of the DC component within the analysis. The solver will determine the eddy currents in all conductors. In the initial steps of the analysis, the magnetic field strength, **H**, is calculated based on the specified AC current sources and boundary conditions. Since the eddy current solver produces a frequency domain solution, it is convenient to express the relevant equations in terms of phasors. Ampere's law with a slight modification can be expressed in phasor form by:

$$\nabla \times \mathbf{B} = \mu \left(\mathbf{J} + \epsilon \frac{\partial \mathbf{E}}{\partial t} \right) \tag{4.13}$$

$$= \mu \left(\sigma \mathbf{E} + \epsilon \frac{\partial}{\partial t} \mathbf{E} \right) \tag{4.14}$$

$$= \mu(\sigma + j\omega\epsilon)\mathbf{E} \tag{4.15}$$

Equivalently, Faraday's law can be expressed in phasor form by:

$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t} \tag{4.16}$$

$$= j\omega \mathbf{B} \tag{4.17}$$

Solving for the electric field, **E**, in Equation 4.15 and combining with Equation 4.17 yields:

$$\nabla \times \left(\frac{1}{(\sigma + j\omega\epsilon)\mu} \nabla \times \mathbf{B} \right) = j\omega \mathbf{B} \tag{4.18}$$

In terms of magnetic field, **H**, Equation 4.18 becomes:

$$\nabla \times \left(\frac{1}{\sigma + j\omega\epsilon} \nabla \times \mathbf{H} \right) = j\omega\mu\mathbf{H} \tag{4.19}$$

Once the magnetic field has been determined, the AC magnetic field energy can be found as:

$$U_{Avg} = \frac{1}{4} \int_V \mathbf{B} \cdot \mathbf{H}^* \, dV \tag{4.20}$$

The skin effect is calculated for currents induced throughout the structure according to:

$$\delta = \sqrt{\frac{2}{\omega\sigma\mu_0\mu_r}} \tag{4.21}$$

The current density, **J**, is determined by means of the skin effect at various points throughout the conductor as well as the calculated magnetic field. The power loss in the conductors can in turn be calcuated as:

$$P = \int_V \frac{\mathbf{J} \cdot \mathbf{J}^*}{2\sigma} dV \tag{4.22}$$

The overall resistance of the structure can be determined using the power loss found in Equation 4.22 and the RMS current by:

$$R = \frac{P}{I_{RMS}^2} = \frac{\frac{1}{2\sigma} \int_V \mathbf{J} \cdot \mathbf{J}^* \, dV}{I_{RMS}^2} = \frac{\int_V \mathbf{J} \cdot \mathbf{J}^* \, dV}{\sigma I_{peak}^2} \tag{4.23}$$

Although the eddy current solver only provides information on the AC component of the current, these results can be combined with the analysis of the DC component in the magnetostatic solver to form a total solution. This method of analysis proved very practical to determine which current component caused limitations in various aspects of the design.

4.2 Planar Inductor Analysis

By utilizing the magnetostatic solver in conjunction with the eddy current solver, all pertinent information regarding the properties of the filter inductor in buck converter configuration can be studied. The most common problems associated with filter inductors in buck configurations seem to be core saturation and current distribution. Core saturation is most easily studied with the magnetostatic solver since it depends mostly on the DC current component. Although, if the AC current component is large enough, the core could be forced into saturation due to the flux swing. A typical filter inductor hysteresis loop can be found in Figure 2.4c. The eddy current solver is necessary to determine the current distribution throughout the traces. The unequal current distribution in an application such as this often results from fringing fields near the inductor gap.

Simulation within the Maxwell environment can be performed in 2-D and 3-D. The complexity of the inductor being analyzed precludes the use of a 2-D simulation since it requires a large degree of symmetry. The inductor chosen through testing to be integrated into the buck converter had two turns and was fitted to an ER18 core geometry. The choice was based on an estimated operating output current for each individual buck converter phase of 12 A. A ten layer board was selected to provide enough copper area for an acceptable resistance level. An overview of the model is shown in Figure 4.3. The dielectric (FR-4) was omitted from the model since it has a permeability roughly equivalent to air; thus, it would not have any great effect on the characteristics being studied. An interleaving structure was utilized to reduce inter-winding capacitance as discussed in [7], [28]. Due to the high cost of producing a ten layer board with an embedded inductor, an over-arching goal of the design was to ensure the component had a large degree of versatility. In other words, the design was aimed at providing a wide range of inductances and saturation points through gap and material manipulation only. Furthermore, the window utilization factor was kept relatively low, allowing the windings to be placed at slightly different locations relative to the core and the gap. This point is illustrated in Figure 4.4.

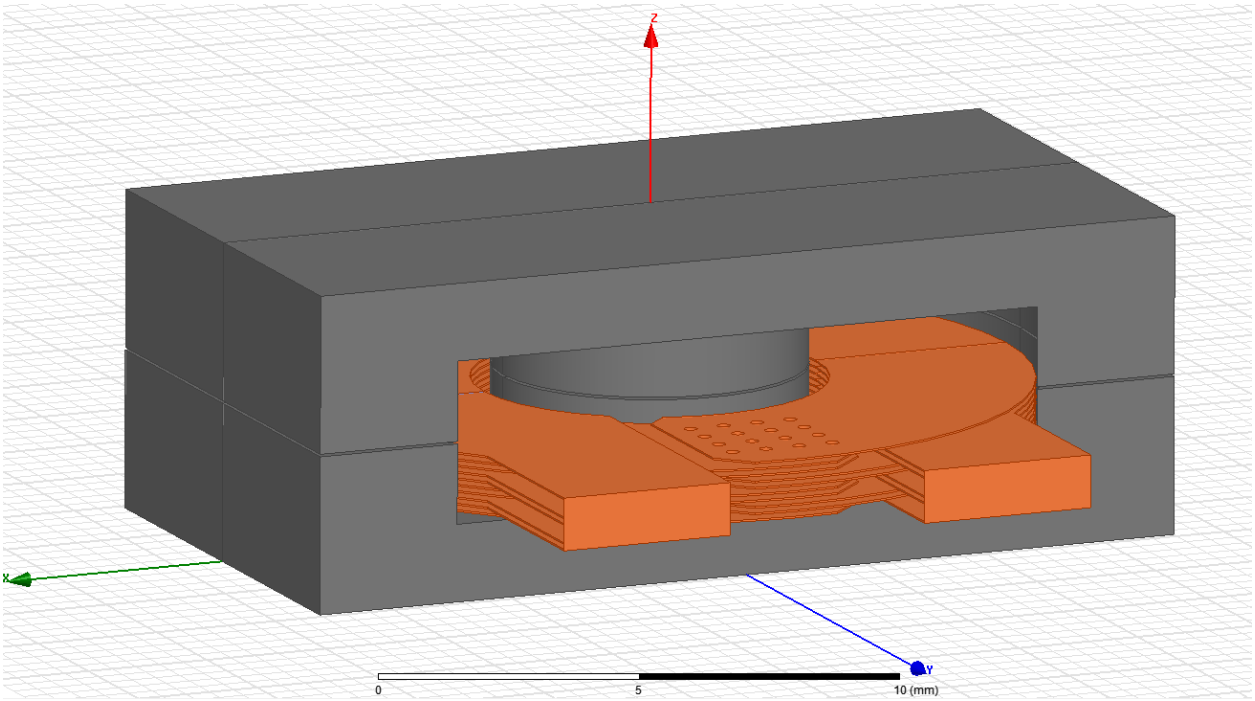
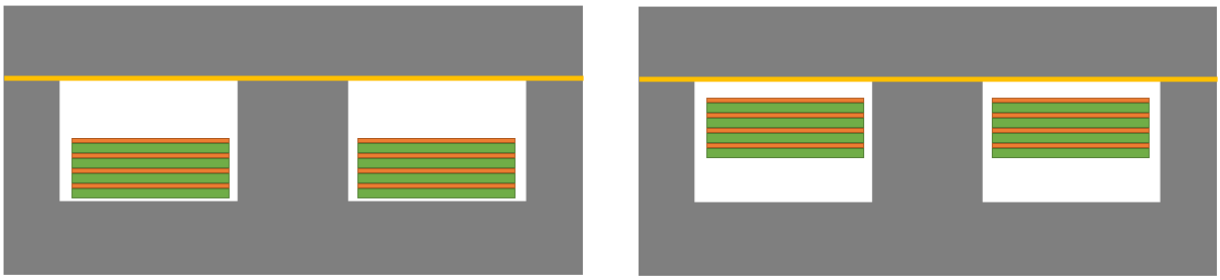


Figure 4.3: 3D inductor structure



(a) Windings positioned at the bottom of the core

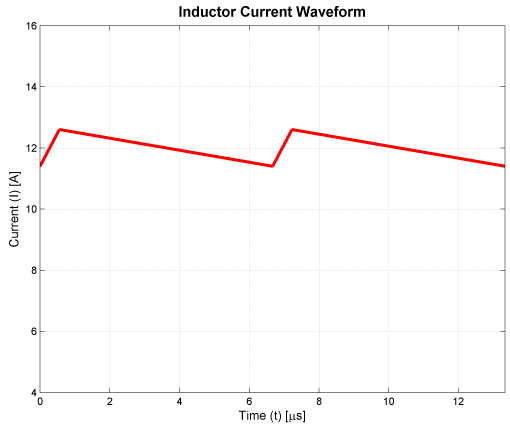
(b) Windings positioned near the gap of the core at the top

Figure 4.4: Various winding locations within the core window

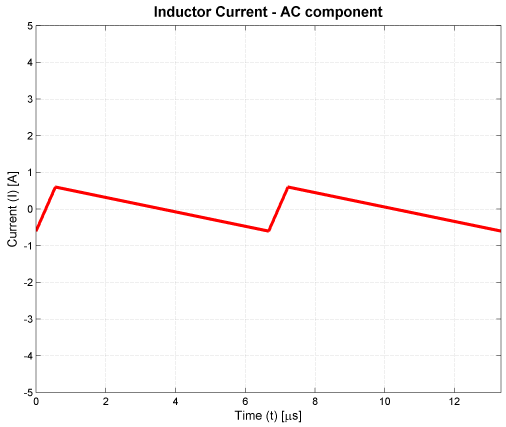
The analysis presented in the following sections outlines four distinct structure orientations. The winding structure is held constant across each model while the gap width, gap location, and winding location are manipulated. The purpose of this analysis method is to determine how each variable affects the current distribution as well as the core flux density.

For the magnetostatic analysis, all analysis was performed with a DC current of 12 A. This value was chosen as a result of the peak performance level of the overall buck converter,

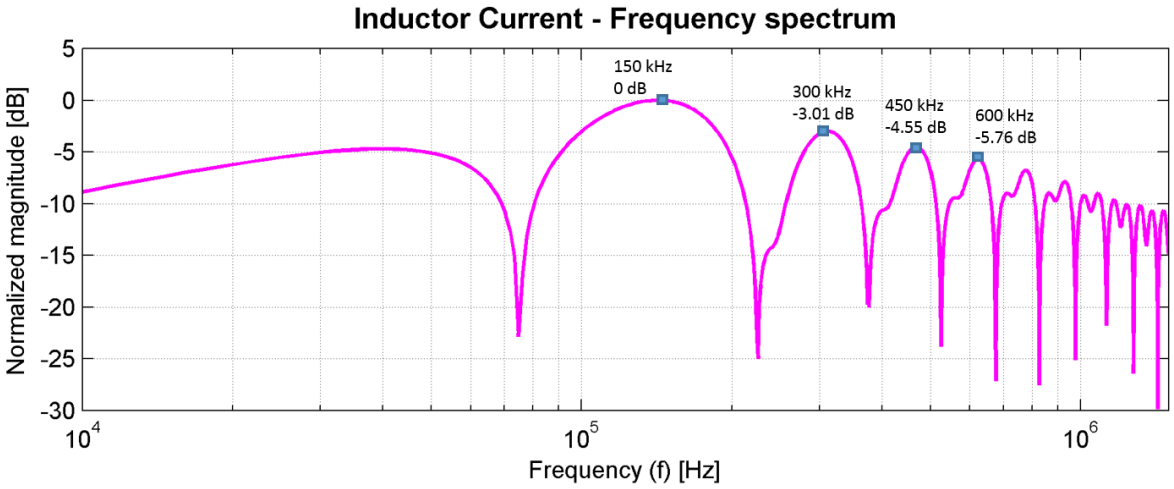
determined through extensive experimental testing. Empirical formulas describing the flux density within a core indicated the ER18 core geometries would be suitable at these current levels.



(a) Filter inductor current



(b) Filter inductor current - AC component



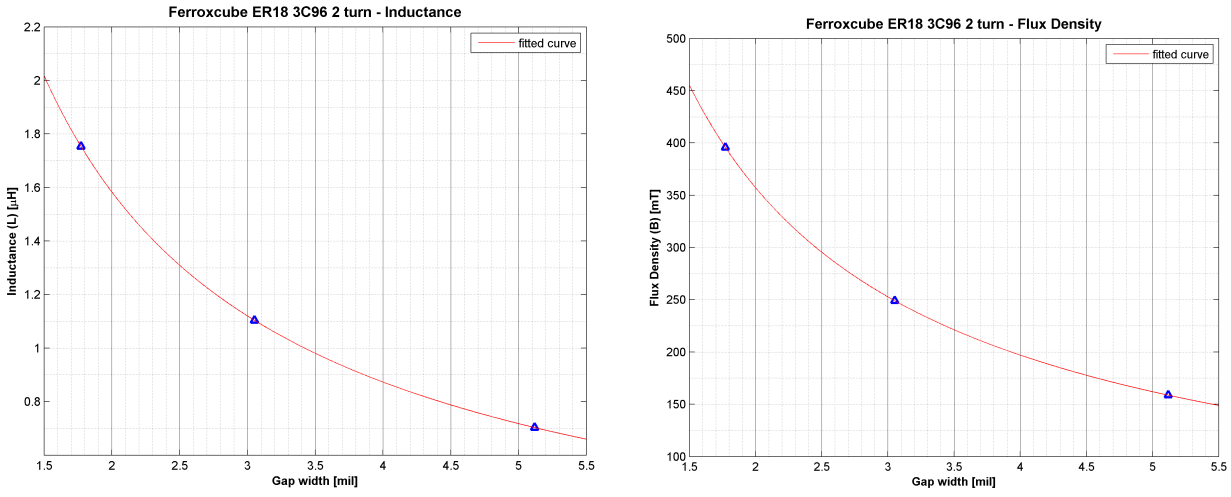
(c) Filter inductor current - Frequency spectrum

Figure 4.5: AC component extraction and frequency response

Characterizing the AC component of the inductor current is slightly more difficult due to the nature of the waveform. Since the eddy current solver is a frequency domain solution, it provides solutions in discrete frequency steps. The current waveform through the inductor is a saw-tooth wave with a DC offset as shown in Figure 4.5a. Since waveforms of arbitrary frequency content cannot be defined within the Maxwell eddy current solver environment,

analysis must be performed at individual frequencies. Clearly, since the eddy current solver does not consider DC, the effective waveform being studied was the AC component of the filter inductor current, shown in Figure 4.5b. The frequency spectrum of the AC component is illustrated in Figure 4.5c. Clearly, the majority of the energy is present within the fundamental frequency of 150 kHz. However, significant frequency content exists in the harmonics of the switching frequency. The frequency content of a typical buck converter current waveform was investigated in [4] with the conclusion that the first three harmonics are significant; as such, these components were investigated with eddy current analysis.

Four inductor configurations were analyzed within Maxwell; all inductors utilized a two turn winding structure designed to work with a Ferroxcube ER18 geometry. Preliminary testing indicated the most suitable material for this particular application was the Ferroxcube 3C96. With all else being equal, the inductance and flux density were controlled entirely by the gap width. The manufacturer provides some experimental data for estimating the inductance of a given structure. Thus, extrapolation by curve fitting was used to get an approximate inductance and flux density for the various designs. Plots of empirical data along with curve fits are shown in Figure 4.6.



(a) ER18 2-turn inductance

(b) ER18 2-turn magnetic flux density

Figure 4.6: Curve fit parameters for Ferroxcube ER18 3C96 2-turn inductor

The desired inductance for the magnetic component was between 1 and 1.5 μH. Consequently, the analysis performed utilizes gap widths of 2 and 3 mils. The saturation flux density for Ferroxcube's material 3C96 is 500 mT. The empirical estimation of flux density shown in Figure 4.6b indicates that the cores should not reach saturation.

4.2.1 Inductor #1

The first inductor configuration investigated had a 2 mil distributed gap with the windings placed in the lower region of the core away from the gap. A 3D model view of this configuration is shown in Figure 4.7. The gap width is 2 mils through each leg of the core. This configuration was estimated to provide about 1.5 μH; this can be verified by observing Figure 4.6a. The maximum flux density was estimated to be 360 mT as seen in Figure 4.6b.

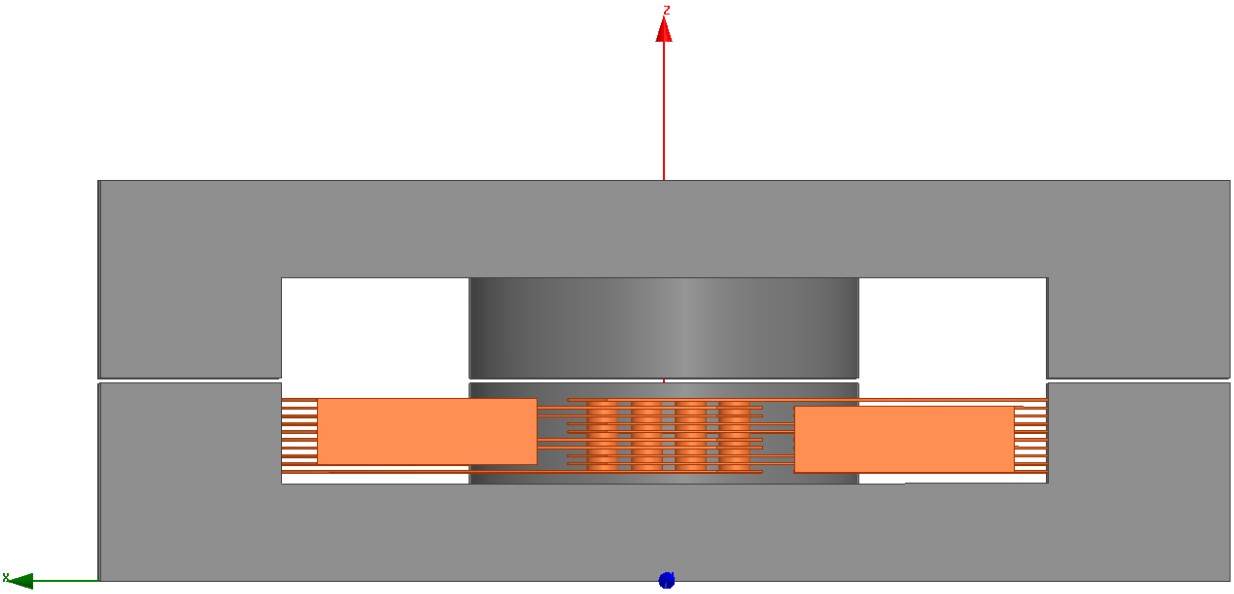


Figure 4.7: Inductor with 2 mil distributed gap and bottom winding orientation

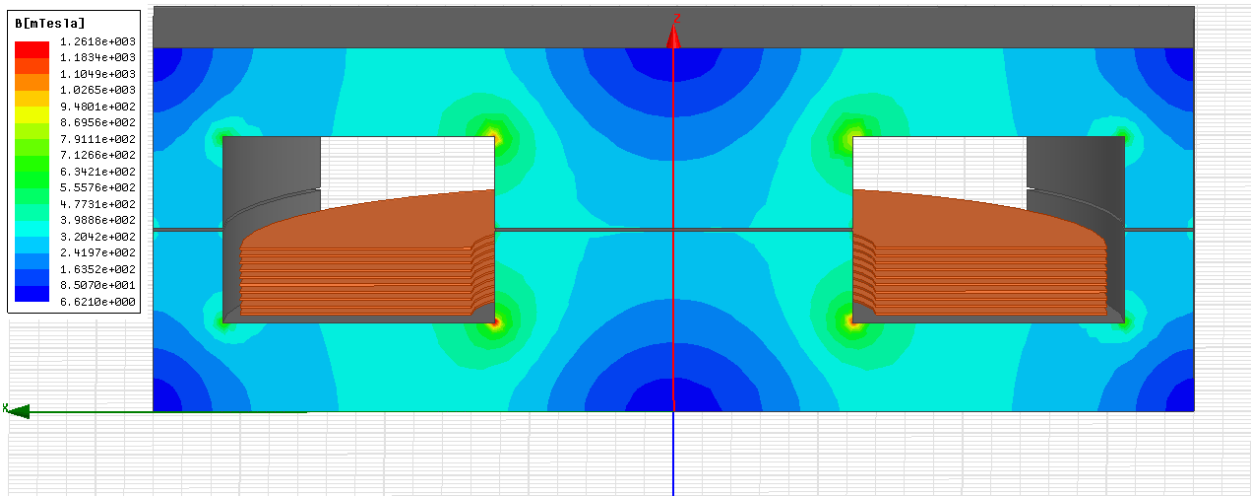
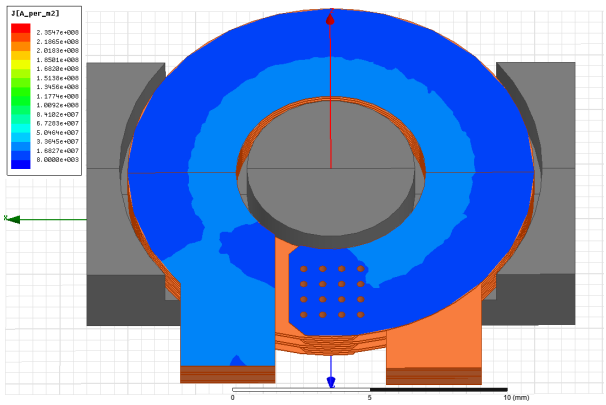


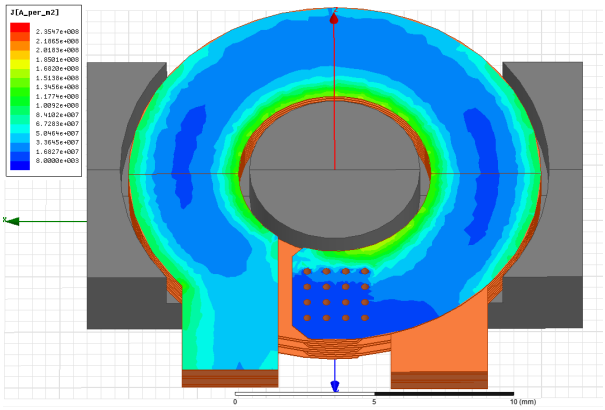
Figure 4.8: Magnetic flux density [mT] through the cross section of the core

The chief advantage of investigating flux density with a 3D FEM model is the localized information it provides. The 1-D empirical calculation is only able to offer a predicted *average* flux density. However, as can be seen in Figure 4.8, the actual flux density varies greatly throughout the core. By observing the center leg, it should be clear that the flux straddles the border of the core closest to the windings. The reason for this is simple. In a similar fashion to electric current and resistance, the magnetic flux density will be higher in paths with a lower reluctance. Several areas of the core, particularly in the corners, contain very little of the total core flux. The loop surrounding the core window, in contrast, possesses regions of flux density between 300 and 700 mT. The large flux differential throughout the core will lead to a relatively soft saturation, since different areas of the core will become saturated at different current levels.

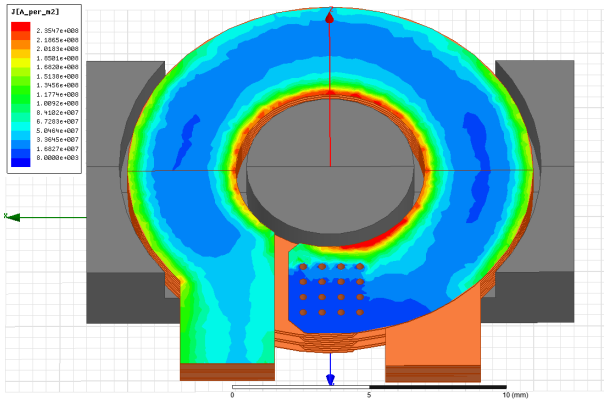
The eddy current solver helps visualize current imbalances throughout the windings. As mentioned previously, the fundamental switching frequency will be analyzed as well as the first two harmonics (300 kHz & 450 kHz). In addition, the current density at 60 Hz will be studied as a reference; given the thickness of the windings, the results obtained at 60 Hz will be approximately equivalent to the DC characteristics.



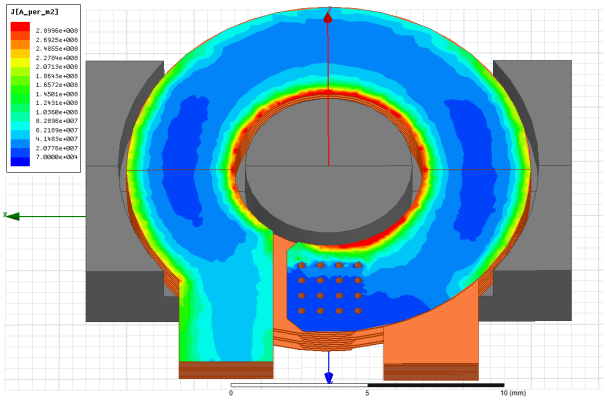
(a) Current density on top trace - 60 Hz



(b) Current density on top trace - 150 kHz



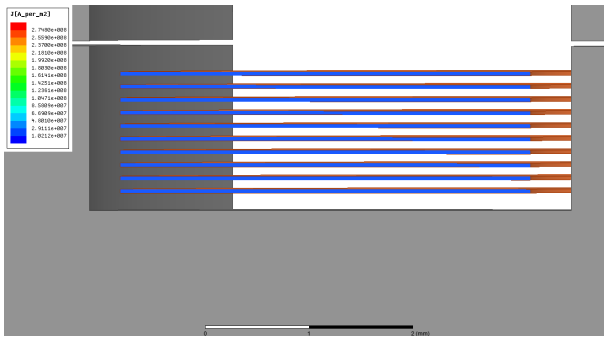
(c) Current density on top trace - 300 kHz



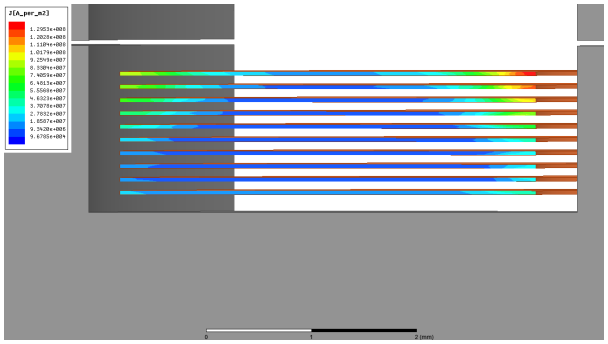
(d) Current density on top trace - 450 kHz

Figure 4.9: Current density of first 3 harmonics and DC (60Hz)

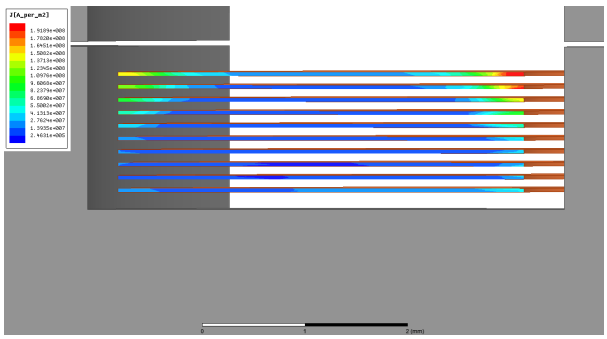
As illustrated in Figure 4.9a, the current distribution at DC (60Hz) is relatively uniform. The slight imbalance is due solely to the resistance differential between the inside and outside of the trace. At 150 kHz, the current become sightly imbalanced, as shown in Figure 4.9b. The current imbalance continues to increase in the cases of 300 kHz and 450 kHz. The most severe current "hot spots" occur near the legs of the core. From this, it can be concluded that the majority of the current imbalance is the result of fringing fields near the gap.



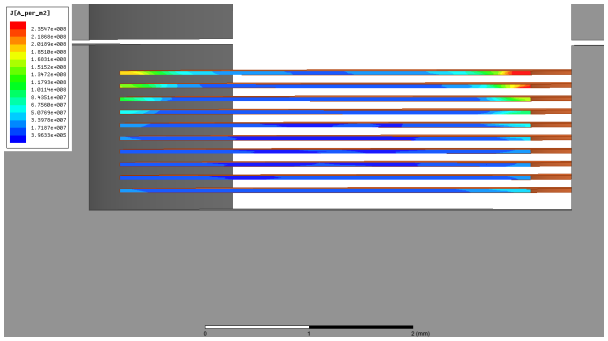
(a) Current density cross-section - 60 Hz



(b) Current density cross-section - 150 kHz



(c) Current density cross-section - 300 kHz



(d) Current density cross-section - 450 kHz

Figure 4.10: Current density viewed as cross-section of first 3 harmonics and DC (60Hz)

The cross-sectional view of the traces deliver more insight into the nature of the current imbalance. The edges of the traces have a higher current density than the middle. However, it is also clear from the cross-sectional plots shown in Figure 4.10 that the traces closer to the gap experience a larger current imbalance. Referring back to Figures 2.2c - 2.2d, it is clear the shape of the current distribution fits the shape of the fringe fields present in the gap region. Similar to the view in Figure 4.9, the imbalance intensifies with increasing frequency.

4.2.2 Inductor #2

The only change made to the inductor characterized previously involved the position of the windings relative to the gap. The windings were placed in close proximity to the gap, in

the middle of the core. The gap remained at 2 mils. A diagram of the inductor is shown in Figure

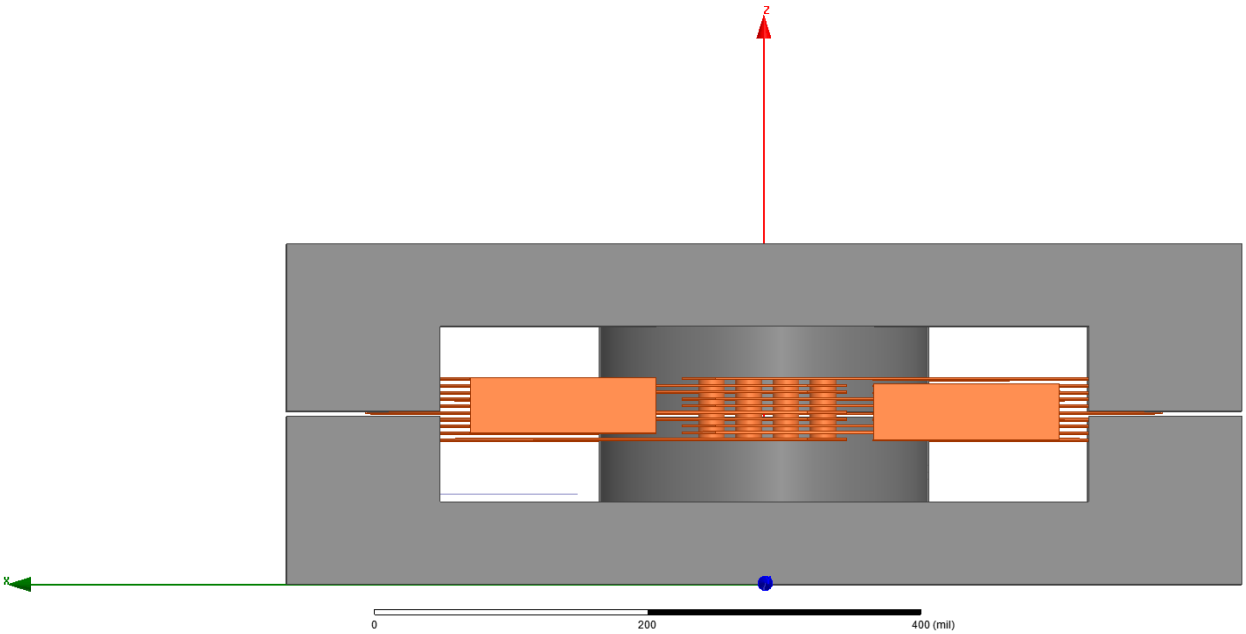


Figure 4.11: Inductor with 2 mil distributed gap and central winding orientation

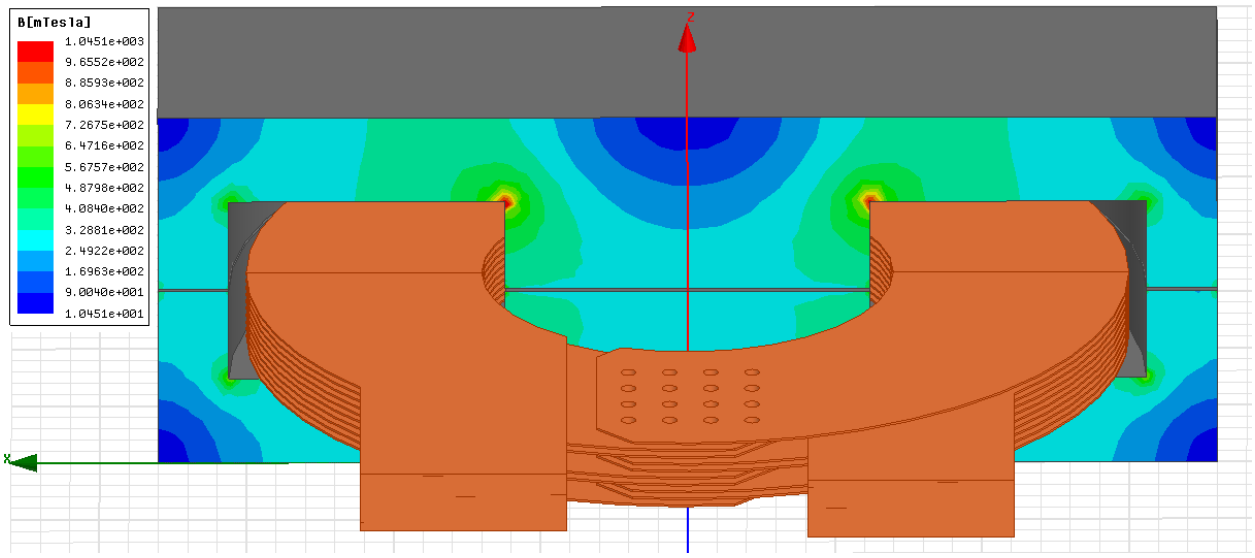
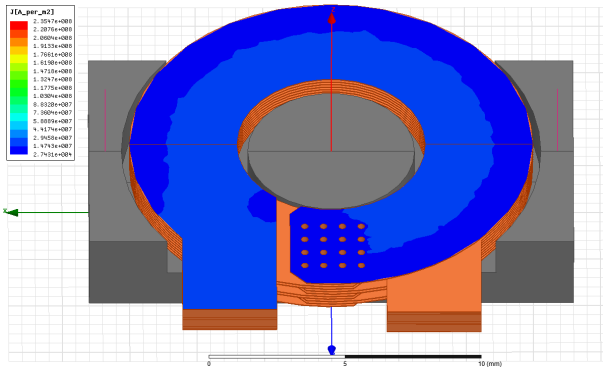


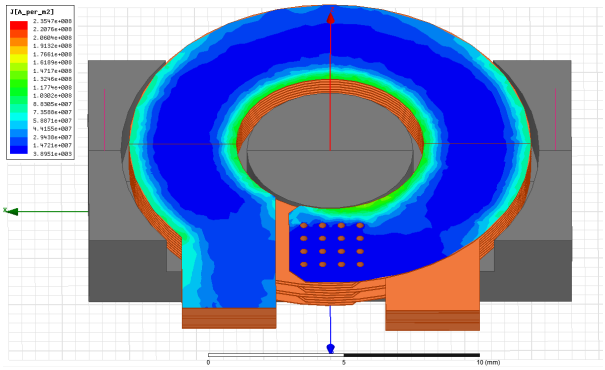
Figure 4.12: Magnetic flux density [mT] through the cross section of the core

Assuming all of the flux remains within the core, which is usually a reasonable approximation, the magnetic flux density should not depend on the location of the current

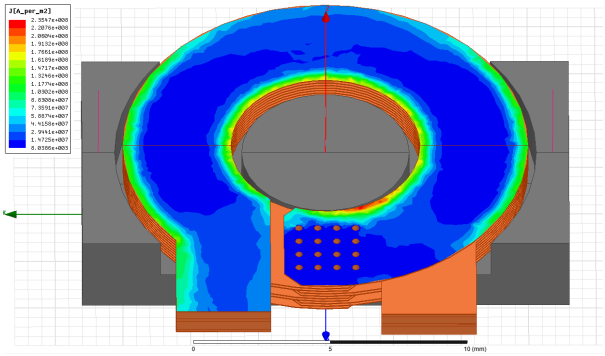
producing the flux. This point is illustrated by observing Figures 4.8 and 4.12. The flux density through the inductors with different winding locations is roughly the same.



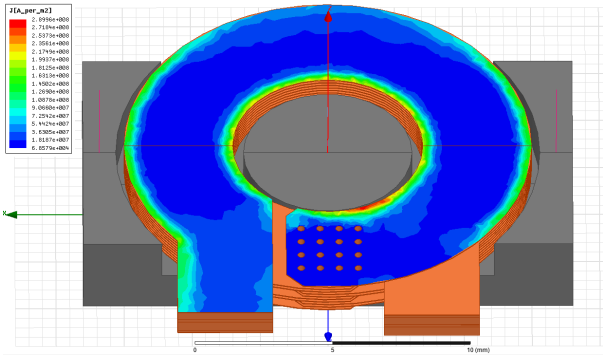
(a) Current density on top trace - 60 Hz



(b) Current density on top trace - 150 kHz



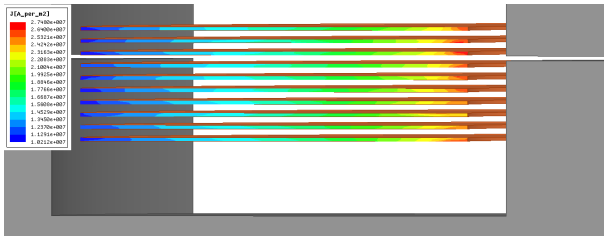
(c) Current density on top trace - 300 kHz



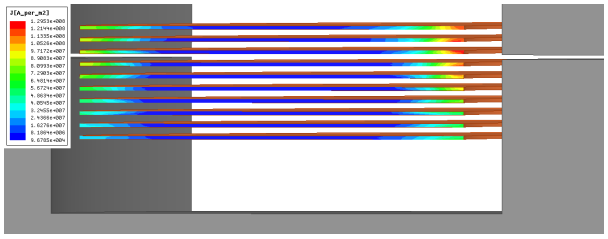
(d) Current density on top trace - 450 kHz

Figure 4.13: Current density of first 3 harmonics and DC (60Hz)

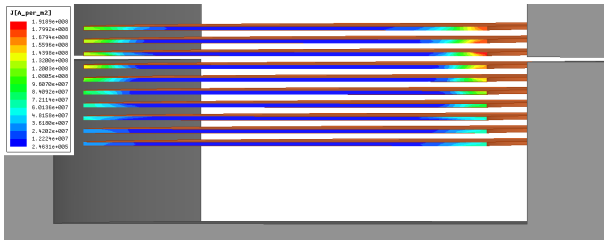
The current density of the top copper winding is shown in Figure 4.13 for DC and the first three harmonics. The current imbalance in this case appears to be less severe than the previous case. However, a closer inspection will indicate that this layer is carrying about 25% less current overall than the same layer in the previous example. The reason for this has to do with the proximity of the winding being viewed to the core gap.



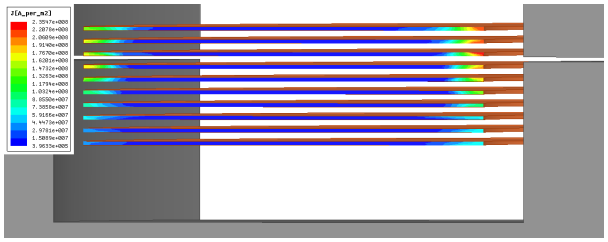
(a) Current density cross-section - 60 Hz



(b) Current density cross-section - 150 kHz



(c) Current density cross-section - 300 kHz



(d) Current density cross-section - 450 kHz

Figure 4.14: Current density viewed as cross-section of first 3 harmonics and DC (60Hz)

The cross-sectional view of the current distribution indicates the layers in which the current crowding is most severe. Much like the previous case, the current imbalance closely aligns the shape of the fringing flux fields protruding from the gap region. However, in this case, the top layer is further from the gap, meaning it will carry less current than the traces in close proximity to the gap. This phenomenon can be seen clearly in Figures 4.14b - 4.14d. A significant amount of research has gone into the optimal placement of the windings in relation to the gap. For the most part, the consensus remains that the two should be separated as much as possible. The most efficient way to accomplish a suitable spacing is by moving the gap to the top of the legs. Unfortunately, the core selected for this work is not constructed in this way. To alleviate this, another approach has been taken that alters the shape of the windings to reduce the AC resistance [7].

4.2.3 Inductor #3

The third inductor investigated, shown in Figure 4.15, had an identical winding location to the first, but the size of the gap was increased by 1 mil. By observing Figures 4.6a and 4.6b, it can be seen that the result of increasing the gap width is lower inductance as well as lower flux density. For a gap of 3 mils, the inductance is estimated as about 1.1 μH. The peak flux density should be reduced to about 250 mT.

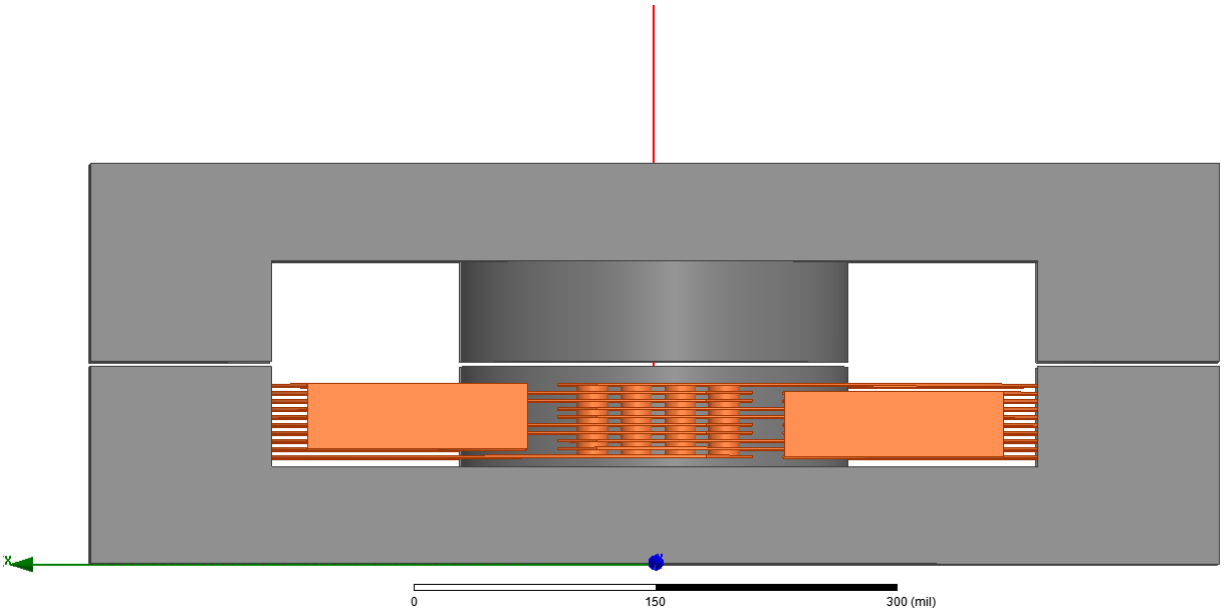


Figure 4.15: Inductor with 3 mil distributed gap and central winding orientation

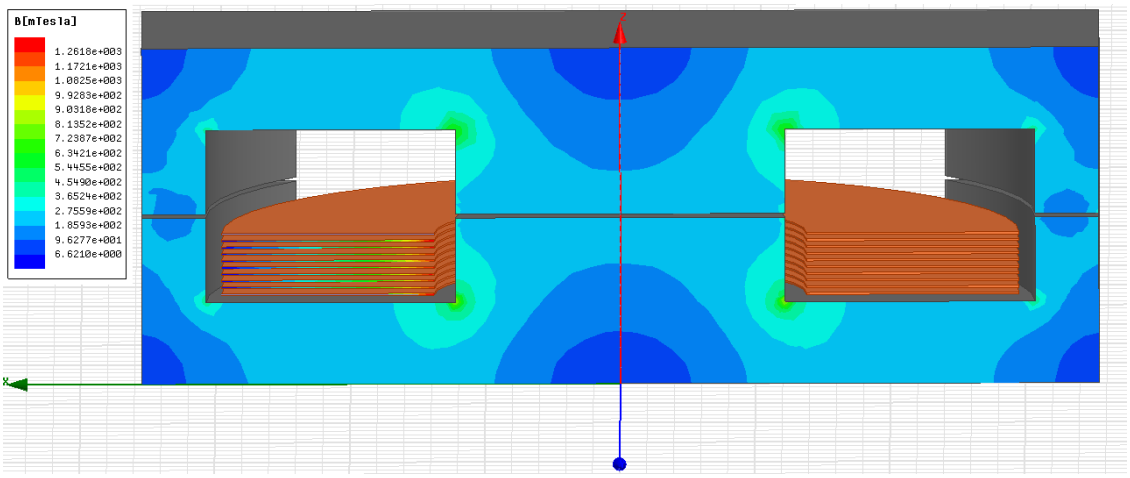


Figure 4.16: Magnetic flux density [mT] through the cross section of the core

A diagram of magnetic flux density throughout the core is illustrated in Figure 4.16. The peak flux density was found to be around 230 - 280 mT, lining up closely with the 1-D approximation. When compared to the similar inductor with a 2 mil gap, it can be seen that magnetic flux is inversely proportional to gap width. This also agrees with the 1-D formula defining flux through a material:

$$B_{pk} = \frac{\mu_0 N I_{pk}}{g + \frac{l_c}{\mu_r}} \tag{4.24}$$

where N is the number of turns, I_p is the peak current, g is the gap width, and l_c is the mean loop length of the core. The proportionality with the gap width occurs when

$$\frac{l_c}{\mu_r} << g, \tag{4.25}$$

which is most often the case when dealing with high-permeability ferrite materials. The current distribution for the 3 mil gapped inductor was nearly identical to that of the 2 mil gap. This result was intuitive since it has been established that winding location with respect to the gap is the primary driver behind current imbalance.

4.2.4 Inductor #4

The final inductor investigated with FEM analysis was a single gapped version of the first inductor. The gap was made twice as large (4 mils) and placed only on the middle leg. The inductance provided by this structure will be identical to that of the first design since the core reluctance, and hence, the effective permeability of the core, will be identical to that of the distributed 2 mil gapped inductor. A plot of the flux density within the 4 mil central gapped inductor is shown in Figure 4.18. Observing and comparing the flux density of the 4 mil central leg gapped inductor with the 2 mil distributed gap inductor shown in Figure 4.8 illustrates the similar flux characteristics. To further emphasize the equality between the two gaping methods, a 6 mil central leg gapped inductor was analyzed with the magnetic flux density displayed in Figure 4.19.

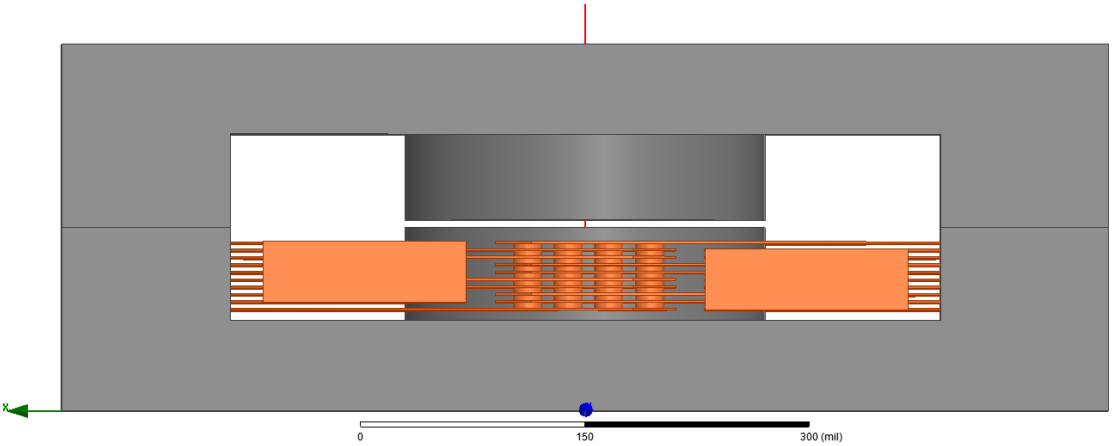


Figure 4.17: Inductor with 4 mil central leg gap and lower winding orientation

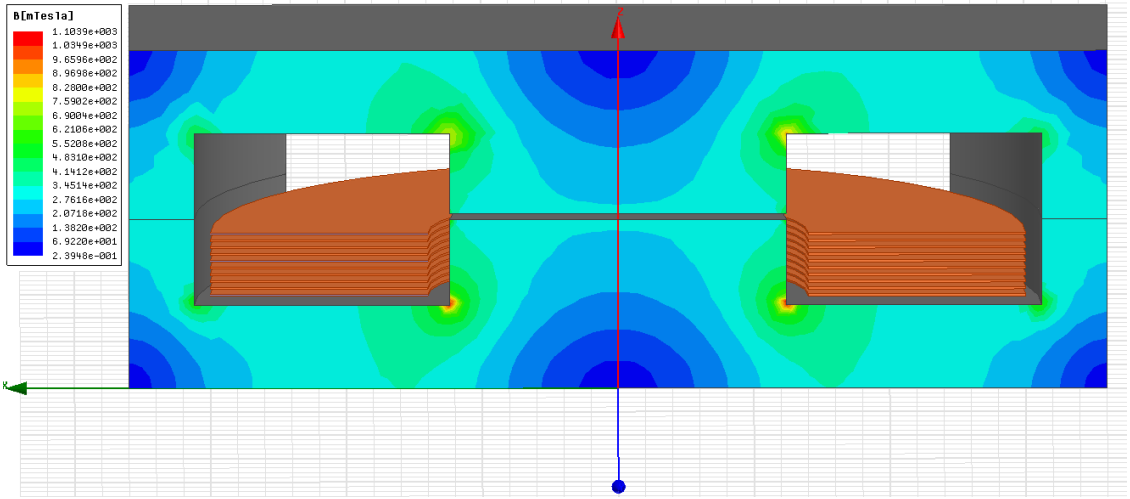


Figure 4.18: Magnetic flux density [mT] through the cross section of the core

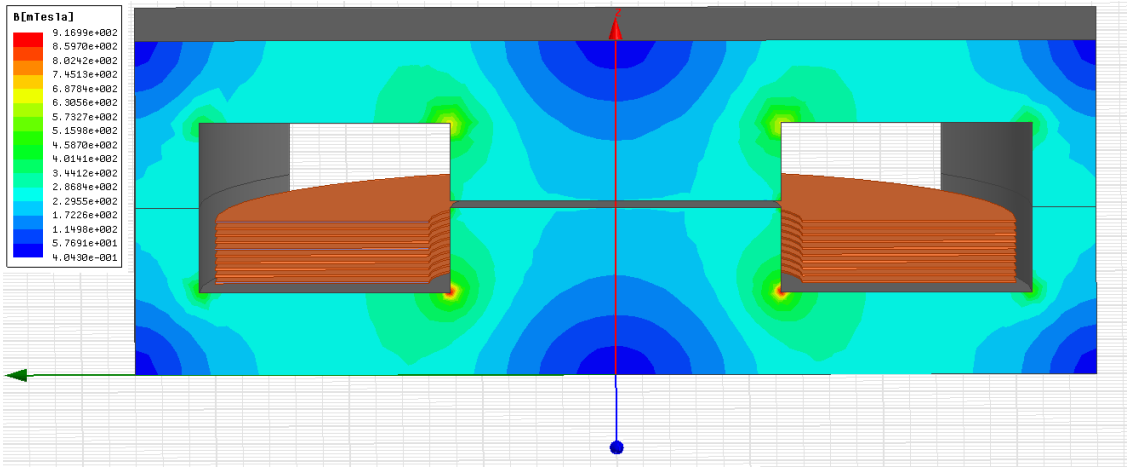
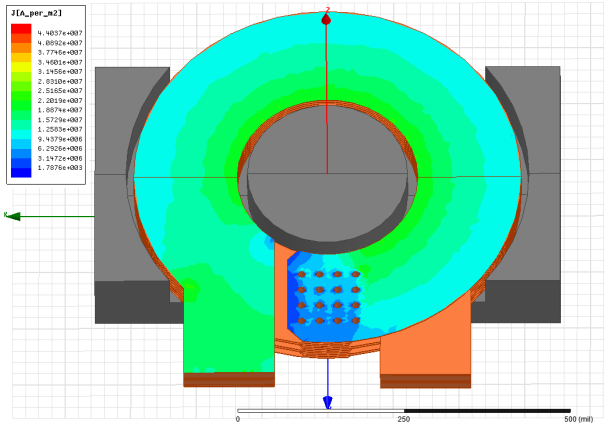
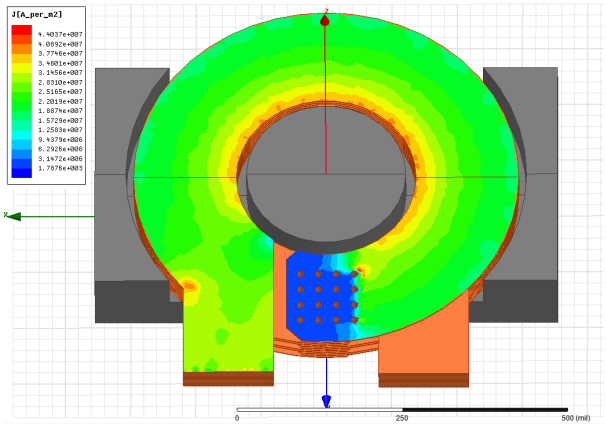


Figure 4.19: Magnetic flux density [mT] through the cross section of the core

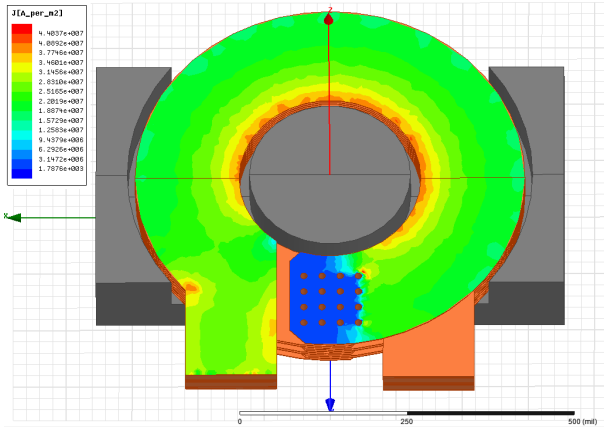
The current distribution was investigated for the 4 mil inductor. The results can be extended to the 6 mil inductor with a high degree of confidence. The current distribution of the top trace is shown for DC and the first three harmonics in Figure 4.20. The current distribution of this inductor design draws some stark contrasts with that of the previous designs with distributed gaps.



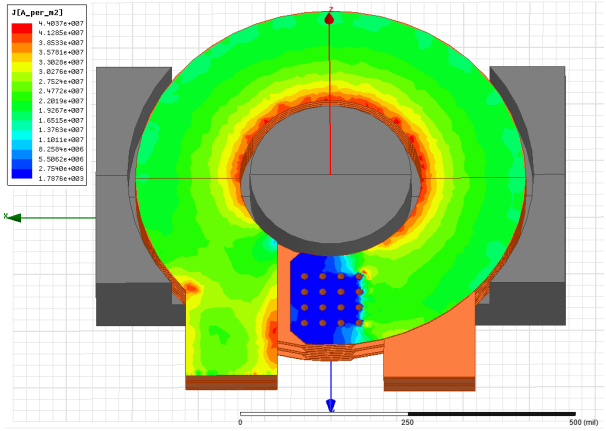
(a) Current density top layer view - 60 Hz



(b) Current density top layer view - 150 kHz



(c) Current density top layer view - 300 kHz



(d) Current density top layer view - 450 kHz

Figure 4.20: Current density viewed as cross-section of first 3 harmonics and DC (60Hz)

The first difference is the degree to which the current imbalance is occurring; with the gap only in the middle leg, the current is significantly more balanced when compared to the

previous cases. In particular, the current crowding occurs only on the inner radius of the winding. This is a direct result of the fringing fields only affecting the inside ring of the windings. Thus, the current is more evenly spread through the remainder of trace. The overall effect of the increased current balance is a reduction in AC resistance. From this, it can be concluded that a single central gap has a superior performance than a distributed gap due to a lower AC resistance. Unfortunately, a single gap core of the appropriate geometry and material was not available. From the FEM analysis, the next best design rule was to keep the traces as far away from the gap as possible. This methodology was utilized when developing the buck converter with integrated magnetics.

Chapter 5

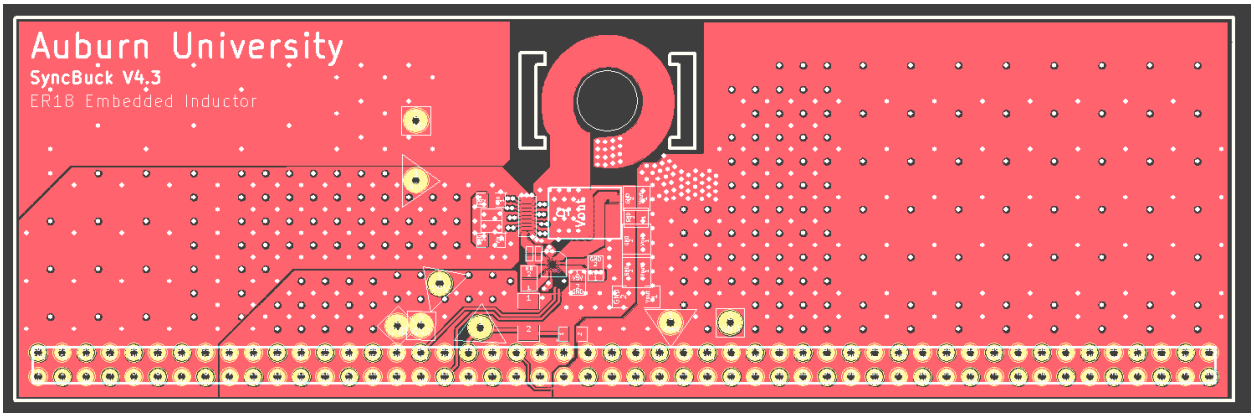
Buck Converter Efficiency Testing and Results

5.1 Board Design

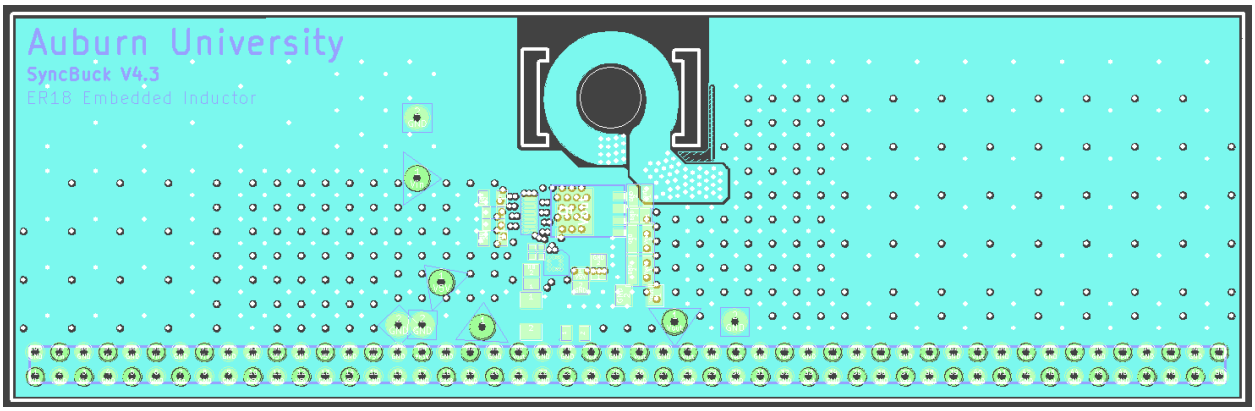
In order to implement the planar inductor into the pre-existing buck converter, a variety of design changes had to be made to the board. The most critical of these changes was increasing the number of layers. A major drawback of planar magnetics is the lack of available copper area; this problem is exacerbated when developing inductors for high current applications. The maximum number of layers available in standard PCB processes is ten. However, thicker two ounce copper was available for use on the outer layers, which made the ten layer board equivalent to a 12 layer board with one ounce layers. Keeping the number of layers no greater than ten was necessary to avoid cost prohibitive manufacturing processes required for high layer-count boards.

5.1.1 Layout

The inductor design and board layout were performed in KiCad, an open-source schematic editor and PCB layout tool. The shape of the inductor made the layout fairly difficult. Most PCB layout editors are tailored for laying out linear traces shapes. The inductor being designed was formed by a two turn loop, thus, conventional layout techniques could not be used. Small linear segments were used to approximate the round circular traces of the inductor windings. The ten layer board was made up of alternating signal and ground layers for parasitic inductance reduction. However, the inductor made use of the ground layers by inserting a cut-out in the layer. The top layer and bottom ground layer are shown in Figures 5.1a and 5.1b, respectively.



(a) Top signal layer of buck converter

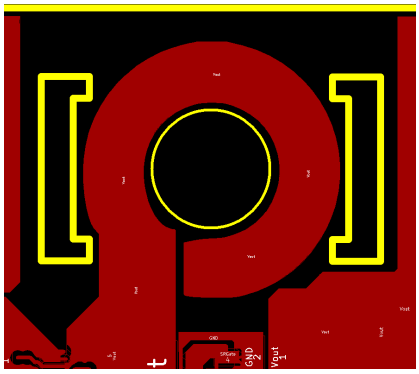


(b) Bottom ground layer of buck converter

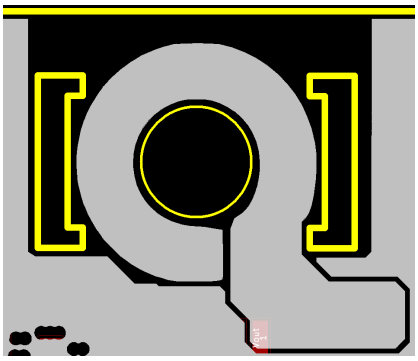
Figure 5.1: Buck converter layout

Each of the two turns was made up of five parallel turns. An interleaving structure was utilized to avoid inter-winding capacitance. The interleaving structure was a pattern of four turn configurations shown in Figure 5.2. The ground plane was altered in a fashion that avoided interfering with any high frequency traces serving as switch turn-on and turn-off circuitry. The board cut-outs, denoted as yellow lines in Figures 5.2a - 5.2d, were difficult to match precisely to the cut-out required by the core. Therefore, square approximations were made to be as close to the required cutout as possible. Additionally, this method kept board costs down, since arbitrary board cut-outs with lots of small angles are difficult and expensive to produce. Since the planar could not be built as a discrete component, the schematic needed to be modeled with the inductor as a short circuit. The effect of

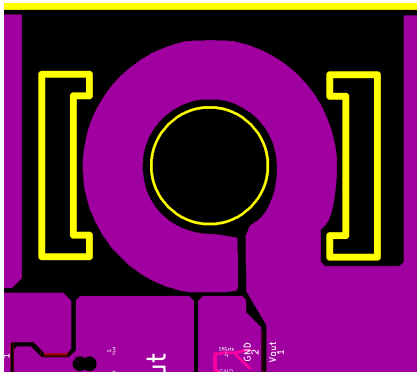
this is shown in Figure 5.2a, where the output of the switch is labeled as V_{out} due to the inductor short. This change required extra care to be taken when laying out the inductor and relocating the necessary components since many parts were now on the same net.



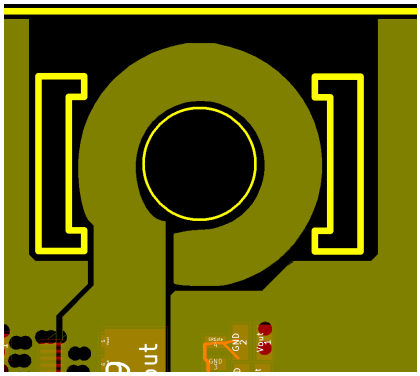
(a) Winding A - Layers 1,5,9



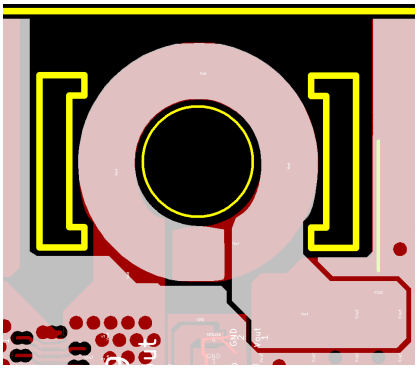
(b) Winding B - Layers 2,6,10



(c) Winding C - Layers 3,7



(d) Winding D - Layers 4,8



(e) Winding A & B superimposed

Figure 5.2: Various turn configurations used to make 2-turn inductor

5.1.2 Assembly

The un-populated PCB is shown Figure 5.3. The thickness of the board was about 1.76 mm, which left about 1.5 mm of clearance between the board and the ferrite core. The board was assembled with conventional soldering techniques for most components. However, the driver, switch, and synchronous rectifier are flip-chip devices that required specialized assembly techniques to ensure proper operation. These devices were placed utilizing a technique developed and demonstrated in [29],[30]. This method makes use of an X-ray for device alignment and a re-flow oven to cycle the solder through a specific temperature profile recommended by the manufacturer.

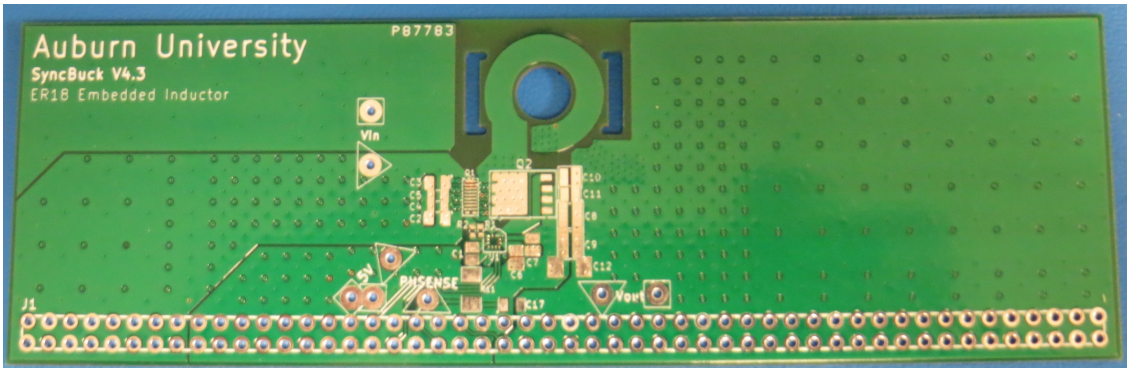


Figure 5.3: Un-populated final buck converter design with planar inductor

One critical mistake was discovered upon assembling the board. The free-wheeling diode was not included in the V4.3 buck converter design. This omission can seriously degrade the reliability of the synchronous rectifier as well as the overall efficiency. The easiest solution was determined to be bridging the switch node to the nearest ground plane, which happened to be the ground terminal of the output filter capacitors [31]. This remedy is portrayed in Figure 5.4. Another mistake, albeit much more minor, was the size of the outside core cut-outs. In previous testing, the core was able to be adhered at an appropriate pressure by wrapping tape around both pieces. The size of the outer leg cut-outs prevented this method of mounting the core. Thus, applying enough pressure to the core sides was much more difficult with this board.

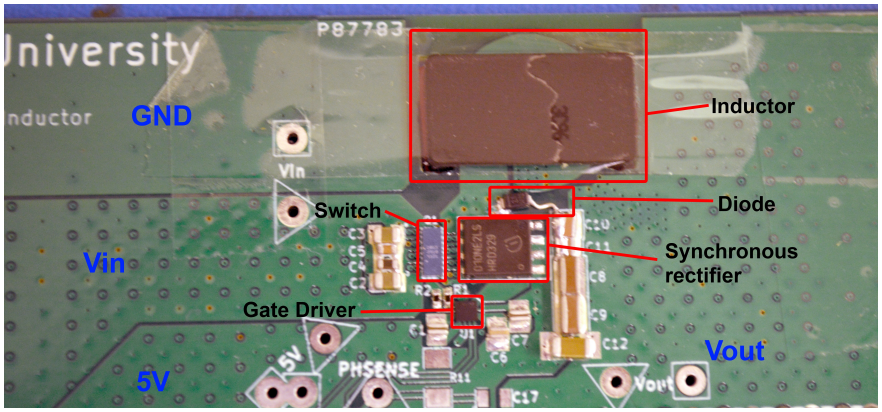


Figure 5.4: Labeled V4.3 buck converter with diode fix

5.2 Efficiency Results

The efficiency of the buck converter was tested for a current range of 4 to 25 A and a frequency range of 120 to 500 kHz. Efficiency plots over frequency and load current are shown in Figures 5.5 and 5.6, respectively.

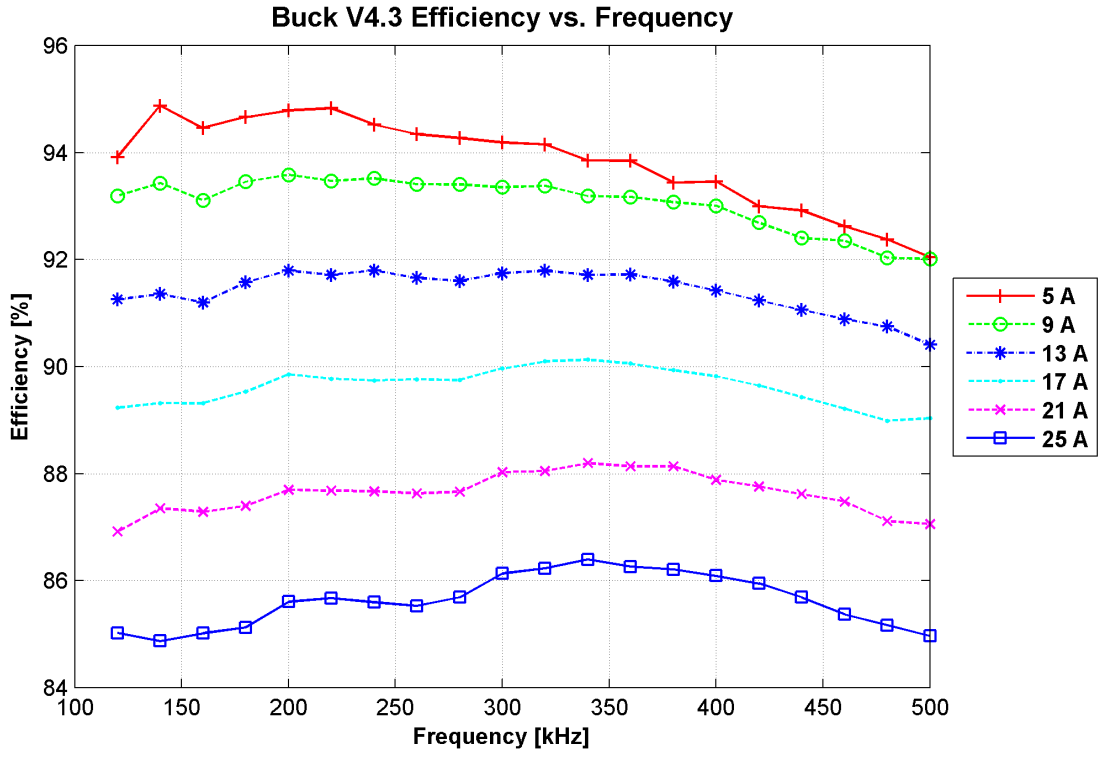


Figure 5.5: Efficiency data plotted over frequency

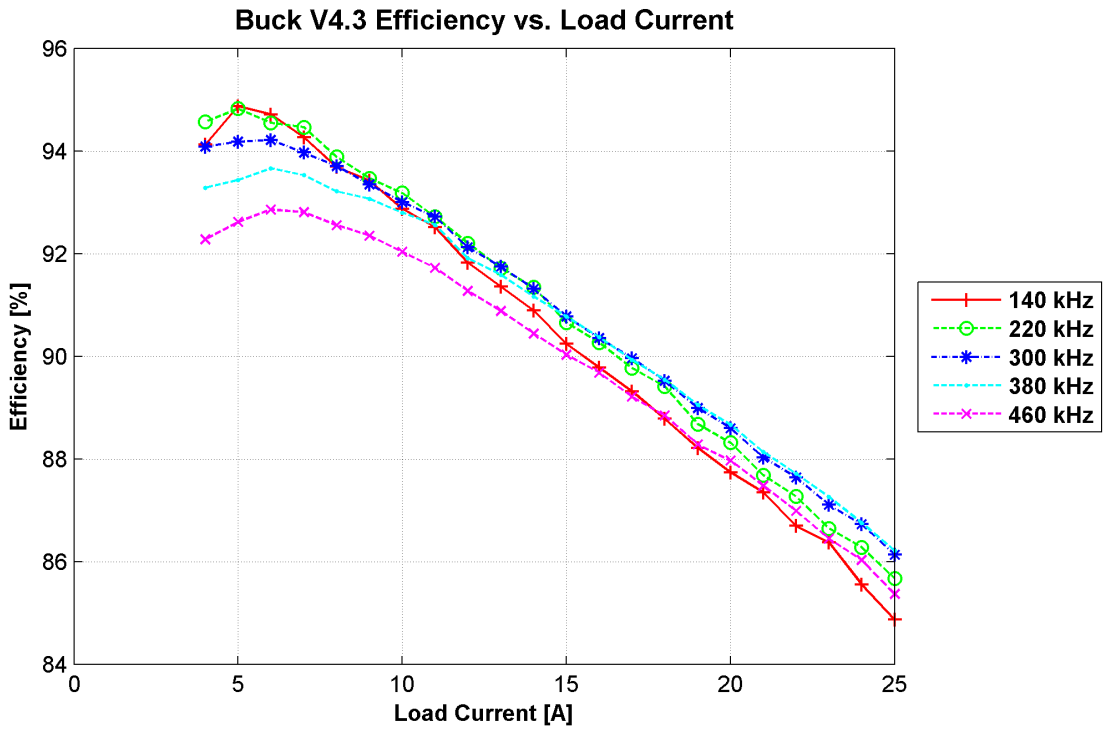


Figure 5.6: Efficiency data plotted over load current

5.3 Comparison vs. Previous Designs

The efficiency improvements brought about by the integrated planar inductor were the result of many factors. The first and most obvious improvement was the board integration and elimination of the mounting bars. This reduced the DCR of the inductor by about 2 mΩ. Another obvious improvement was the addition of six layers to the design, which more than halved the DCR of each turn. A more subtle change was the interleaving strategy and how the terminals were established between the switch node and the output node. A comparison of the buck converter V4.1 and V4.3 are shown in Figures 5.7 - 5.14. The teal line indicates the buck convert V4.3 with the integrated planar inductor.

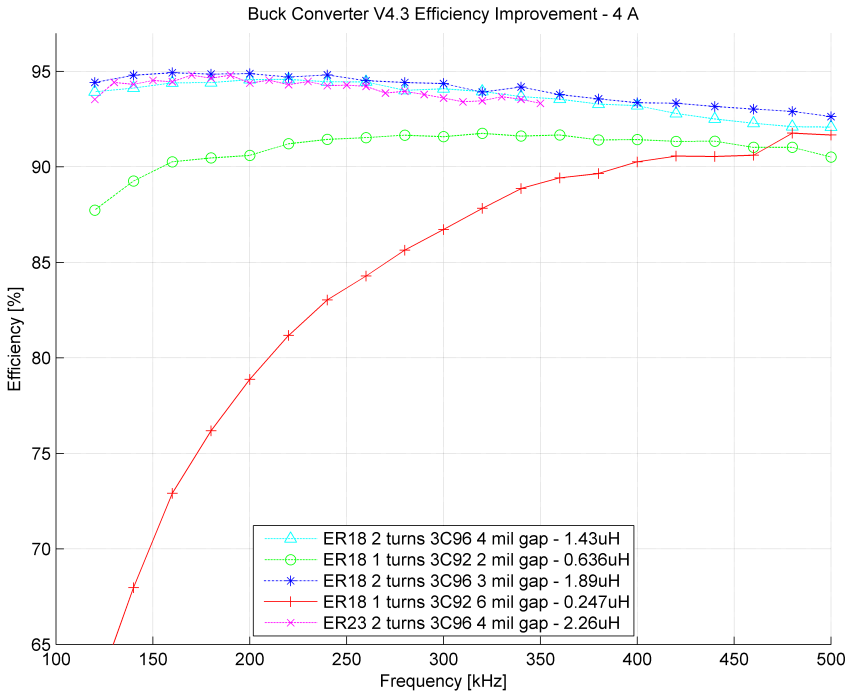


Figure 5.7: Buck Converter V4.3 Efficiency improvement - 4A

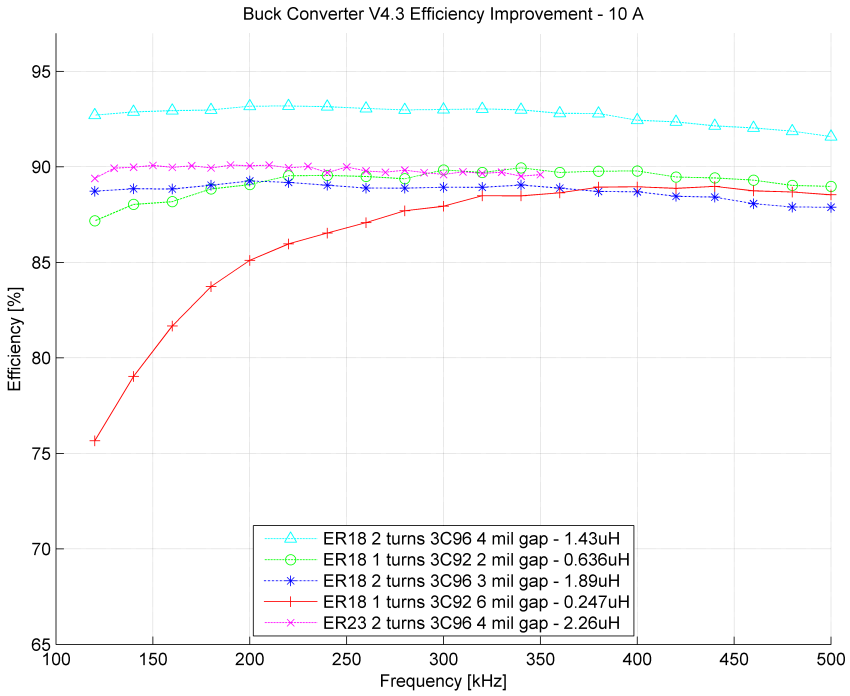


Figure 5.8: Buck Converter V4.3 Efficiency improvement - 10A

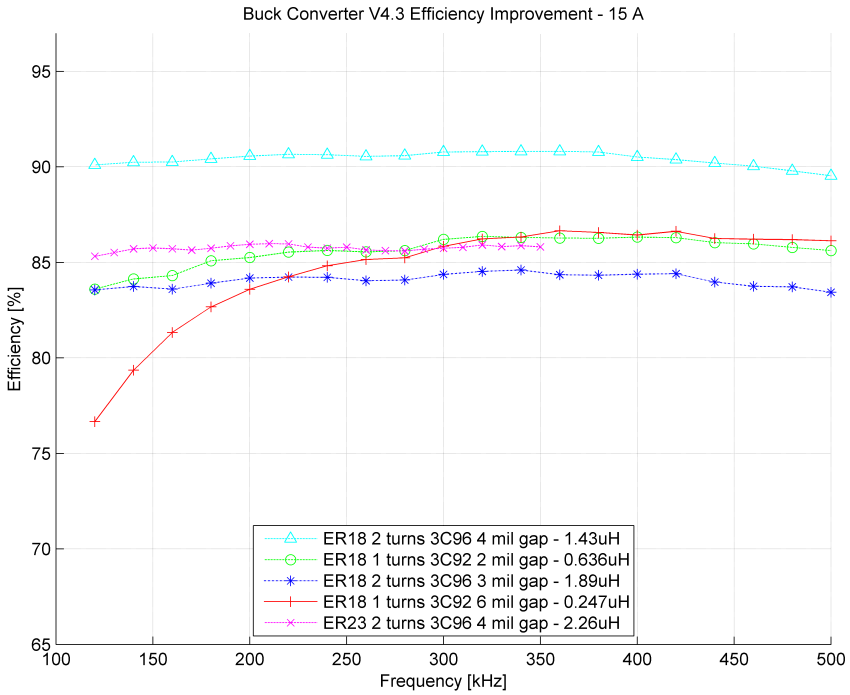


Figure 5.9: Buck Converter V4.3 Efficiency improvement - 15A

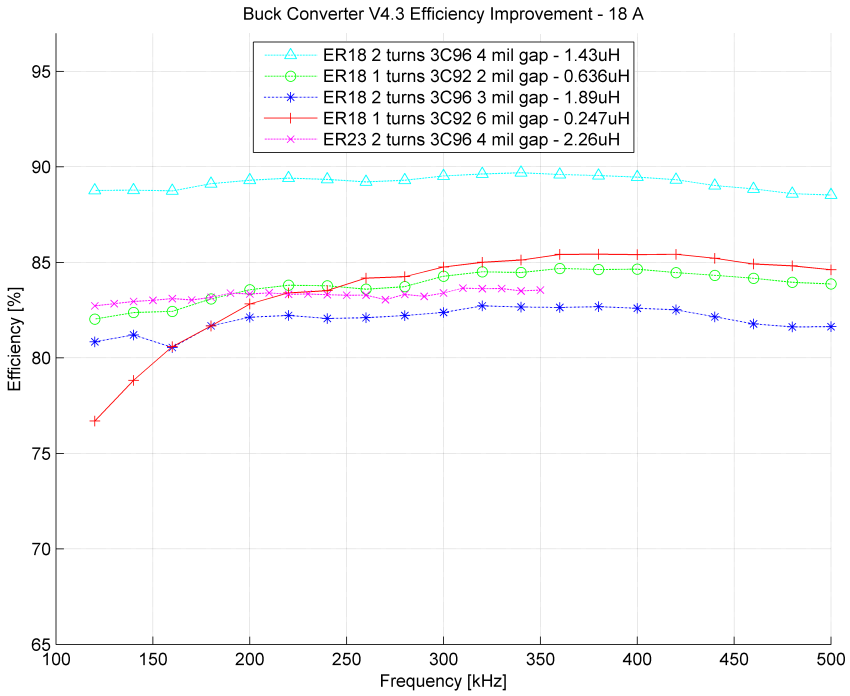


Figure 5.10: Buck Converter V4.3 Efficiency improvement - 18A

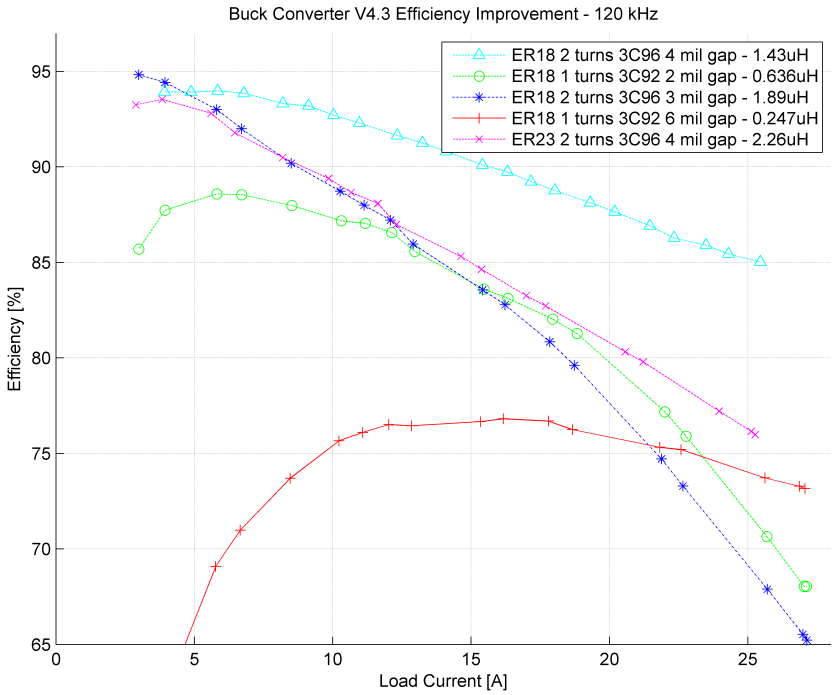


Figure 5.11: Buck Converter V4.3 Efficiency improvement - 120kHz

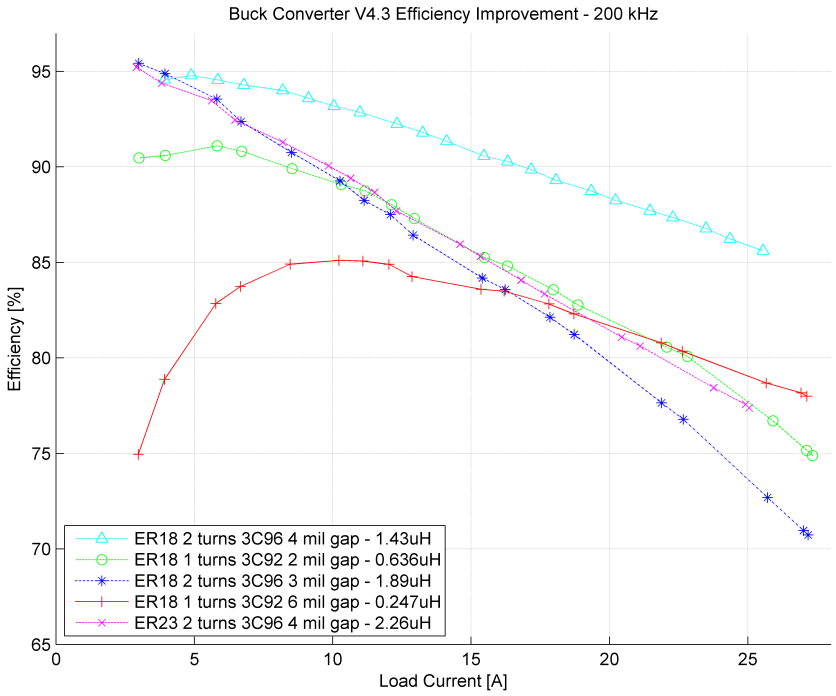


Figure 5.12: Buck Converter V4.3 Efficiency improvement - 200kHz

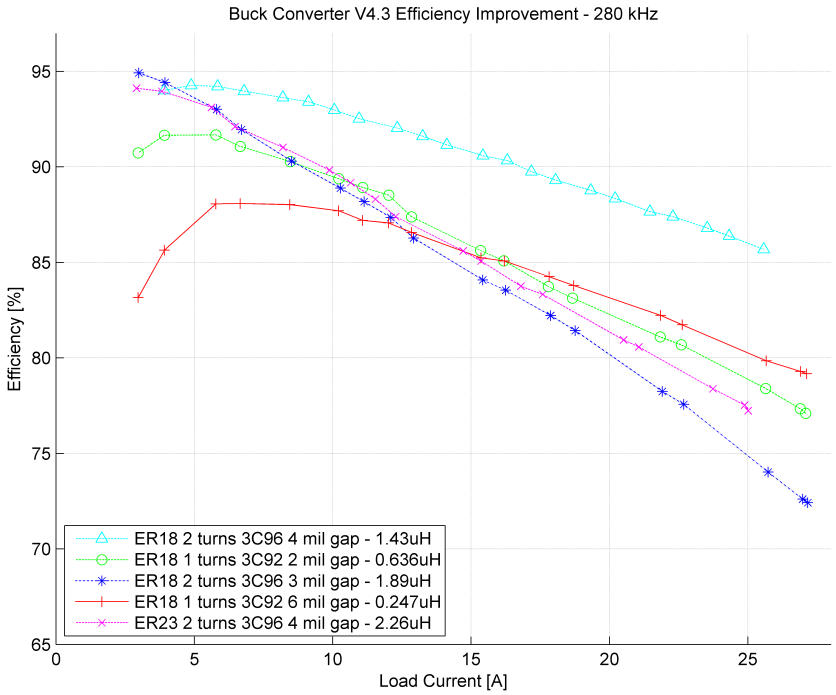


Figure 5.13: Buck Converter V4.3 Efficiency improvement - 280kHz

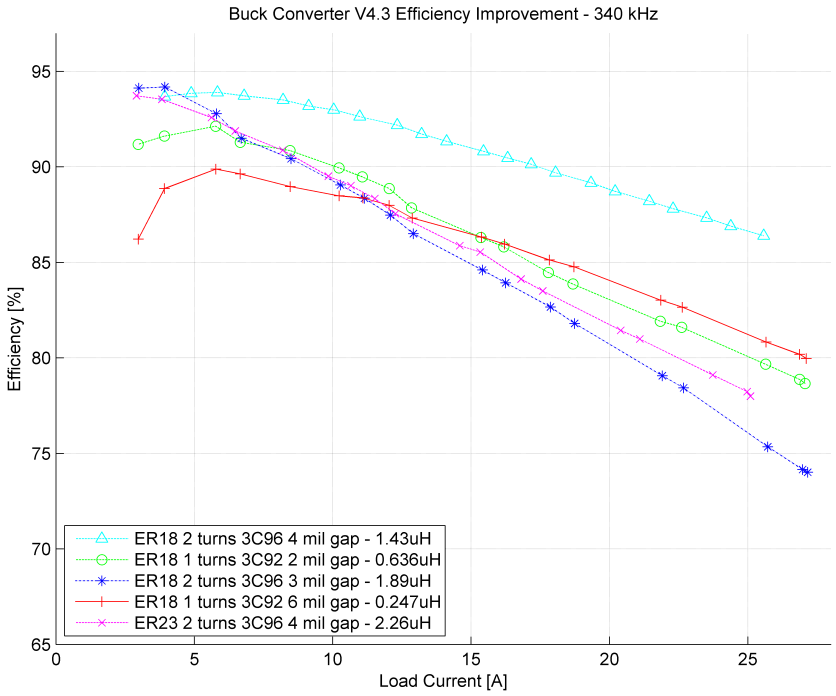


Figure 5.14: Buck Converter V4.3 Efficiency improvement - 340kHz

The efficiency improvements can be seen clearly for load currents greater than 10 A, where losses due to DCR begin to get large compared to core loss. The V4.3 board has a relatively constant efficiency over frequency since it has sufficient inductance to remain out of DCM and a low enough magnetic flux density to avoid saturation.

5.4 Comparison vs. COTS Inductors

The planar inductor board V4.3 performed competitively with many high quality commercial off-the-shelf (COTS) inductors. For illustration, two of the better COTS inductors tested are compared directly to the planar inductor at a variety of load currents and frequencies. These comparisons are illustrated in Figures 5.15 - 5.21.

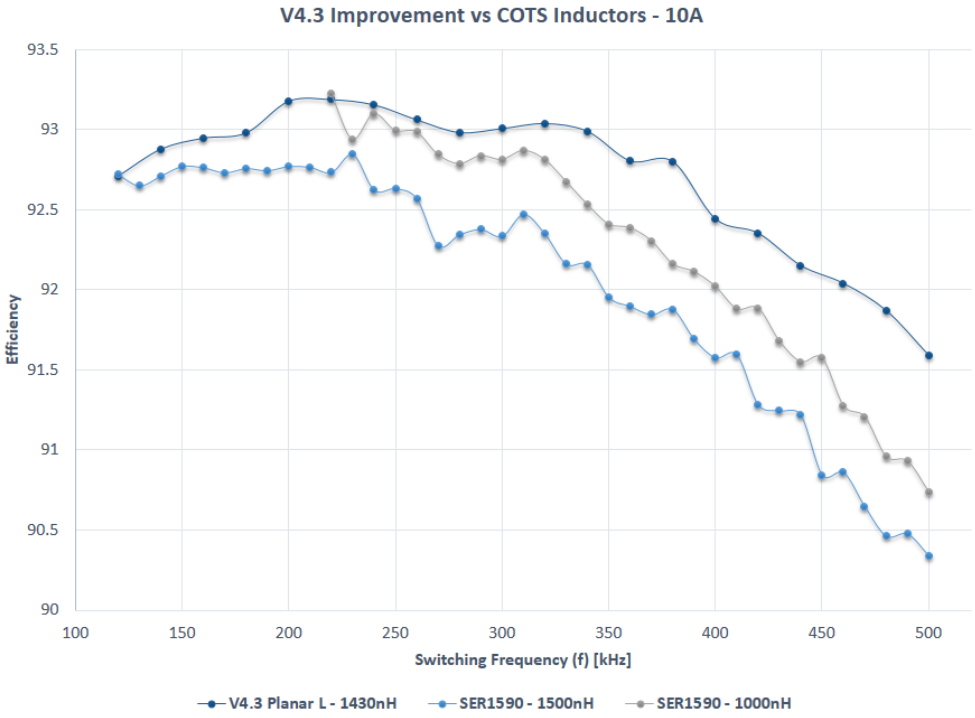


Figure 5.15: Buck converter V4.3 efficiency vs. COTS inductors - 10A

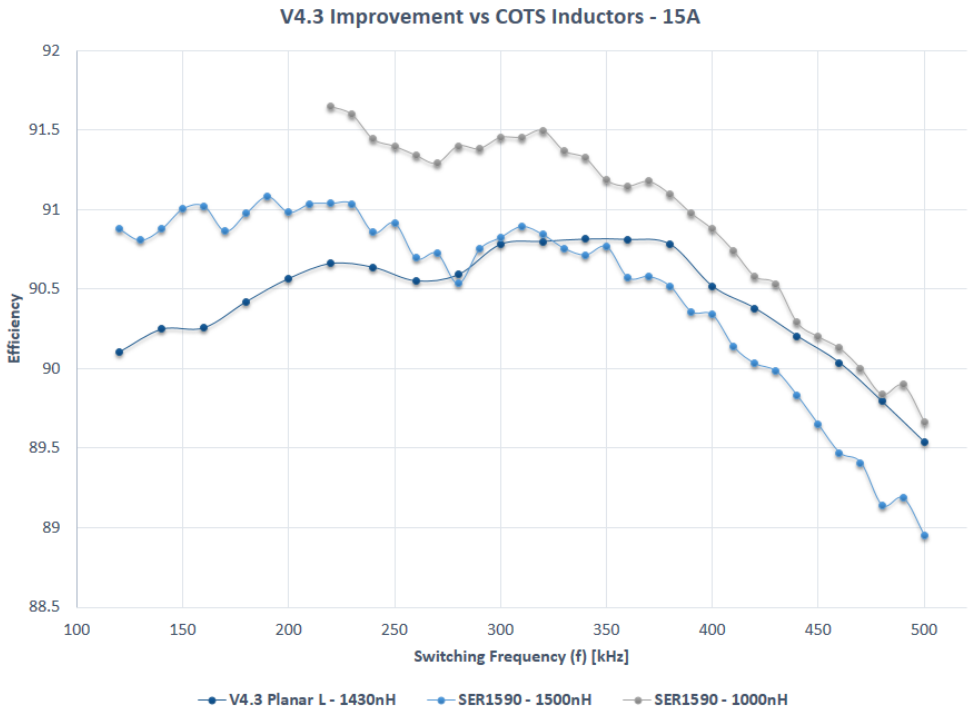


Figure 5.16: Buck converter V4.3 efficiency vs. COTS inductors - 15A

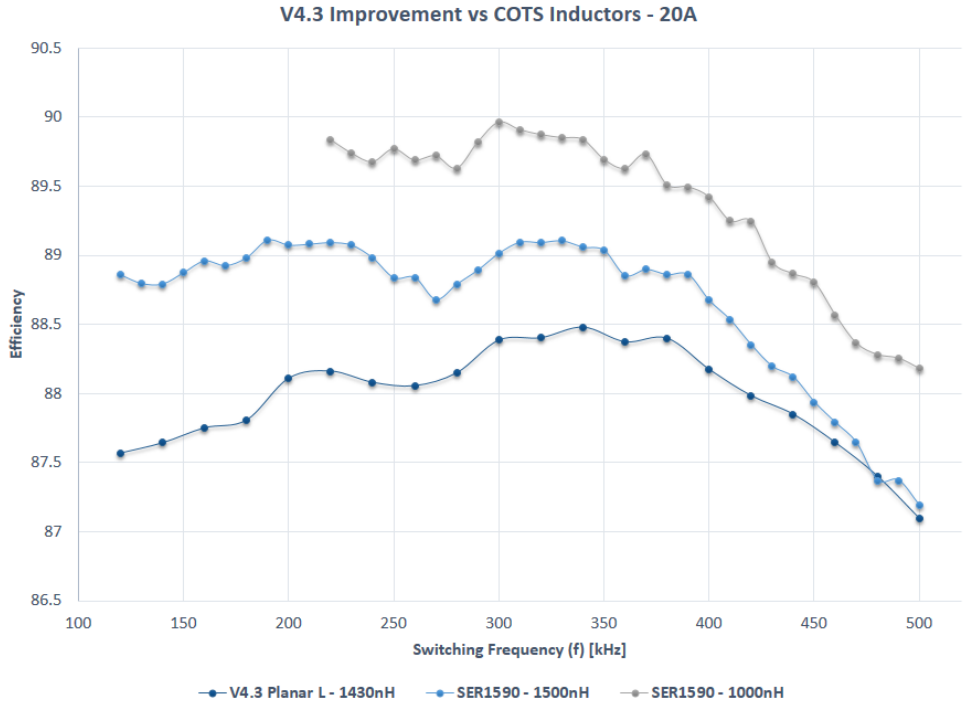


Figure 5.17: Buck converter V4.3 efficiency vs. COTS inductors - 20A

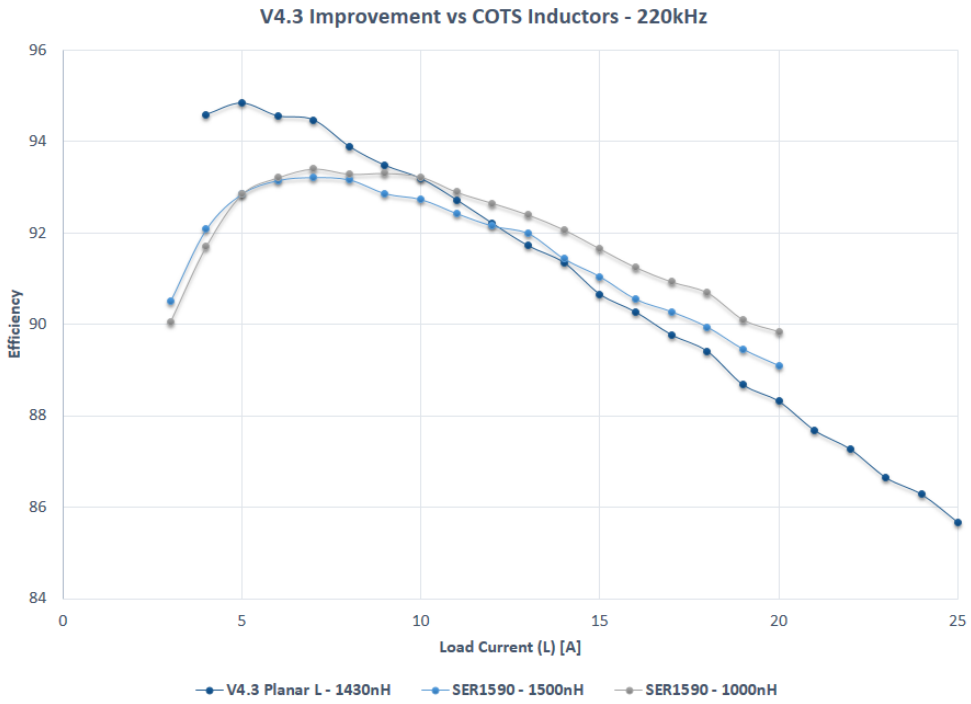


Figure 5.18: Buck converter V4.3 efficiency vs. COTS inductors - 220kHz

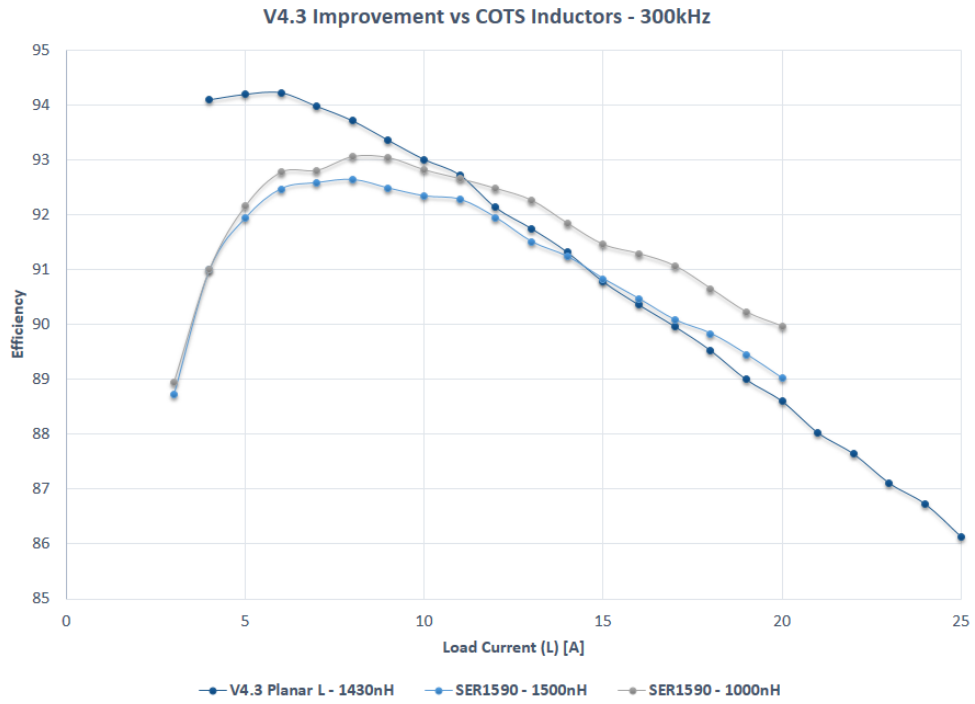


Figure 5.19: Buck converter V4.3 efficiency vs. COTS inductors - 300kHz

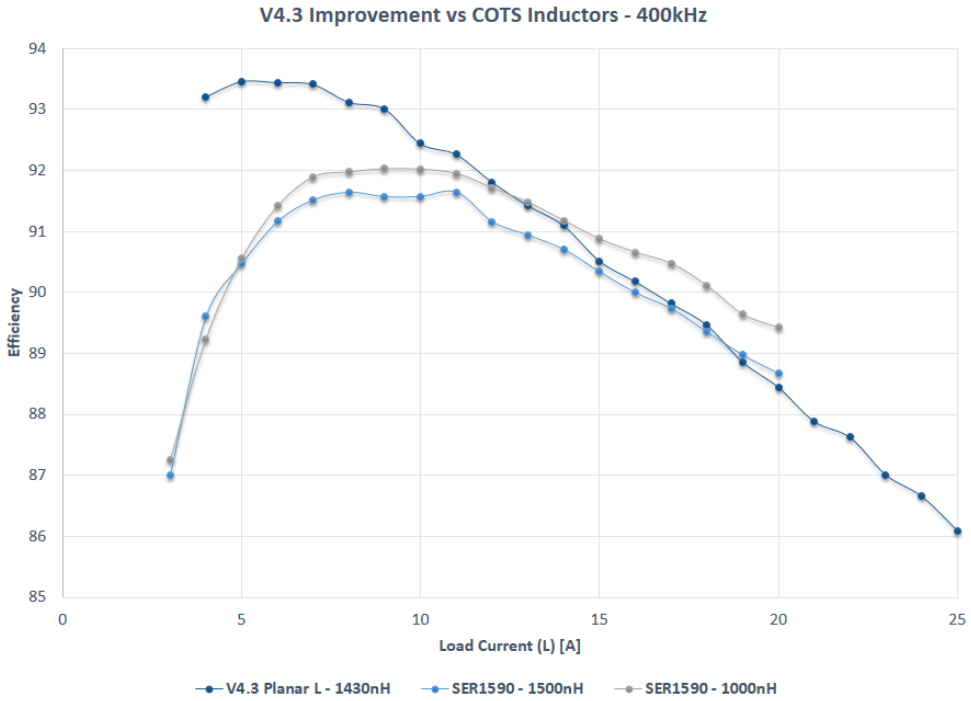


Figure 5.20: Buck converter V4.3 efficiency vs. COTS inductors - 400kHz

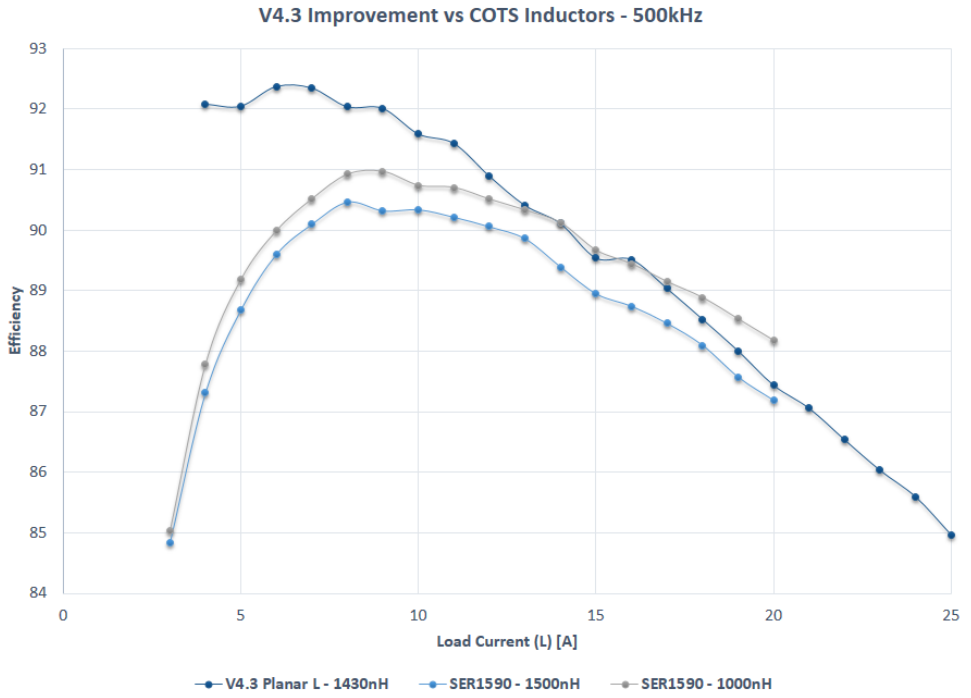


Figure 5.21: Buck converter V4.3 efficiency vs. COTS inductors - 500kHz

The planar component is most competitive with the COTS inductors at low to mid load current ranges. The reason being the 1.5 mΩ DCR of the planar component compared to the less than 1 mΩ of the COTS components. This discrepancy can be mitigated through the use of more layers and thicker copper. The planar inductors seem to have a slight advantage at higher frequencies over the COTS inductors. This is most likely a result of the flat traces, which are shaped optimally for high frequency operation. Overall, a buck converter being run at low to mid output load currents and mid to high frequencies can benefit from the planar magnetic technology. However, as load current increases, the DCR of the planar component is simply to great to compete with the surface mount COTS inductors.

Chapter 6

Conclusion and Future Work

6.1 Summary

A planar inductor was developed and integrated with a 12-1 V DC-DC synchronous buck converter. Further, the developed planar inductor was shown to perform comparably with present state-of-the-art COTS power inductors. In many cases, the developed planar inductor provided higher efficiency and a lower dependence on switching frequency when compared to COTS inductors.

An extensive review of planar magnetic technology was outlined in Chapter 1. The discussion of planar magnetic technology was restricted to power electronic applications with an emphasis on low voltage, high current DC-DC buck converters. A survey of applications which included data centers and high performance computing centers were discussed. The various loss characteristics of an inductor were outlined in Chapter 2. Unlike transformers, winding loss was shown to be the primary source of power loss within inductors. A typical design procedure was presented and outline briefly. For purposes of simplicity and testing speed, a method of quickly characterizing planar inductors was outlined in Chapter 3. Several inductors utilizing a multitude of core geometries and materials were compared. Ferroxcube's ferrite material 3C96 was determined to be the optimal material for the buck converter application at the selected switching frequency range. FEM analysis was shown to be an invaluable tool for designing and characterizing inductors. This tool becomes even more critical as the complexity of the winding structure increases. The final buck converter with an integrated inductor was presented in Chapter 5. Efficiency comparisons were illustrated for the final planar inductor and two COTS inductors. The planar inductor was shown to outperform the COTS inductors at low to mid load currents.

6.2 Future Work

Through development of the planar inductor, the principle loss mechanism was determined to be the winding resistance. This was comprised of DC and AC loss components. As such, further measures should be taken to mitigate the winding loss of the inductor. Some example of feasible approaches were discussed previously. The most promising approach for this application is the shaped winding approach discussed in [24]. This method is especially useful when working with middle gapped cores to reduce the AC winding resistance. Furthermore, the techniques proposed in Chapter 4 to analyze the AC resistance of a structure could be expanded upon.

Bibliography

[1] U. Badstuebner, J. Biela, and J. Kolar, "Design of an 99%-efficient, 5kW, phase-shift PWM DC-DC converter for telecom applications," in *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Feb. 2010, pp. 773–780.

[2] Y. Cui and L. Tolbert, "High step down ratio (400 v to 1 v) phase shift full bridge DC/DC converter for data center power supplies with GaN FETs," in *2013 IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Oct. 2013, pp. 23–27.

[3] D.-H. Kim, T. Yu, H. Kim, H. Mok, and K.-S. Park, "300V DC feed system for internet data center," in *2011 IEEE 8th International Conference on Power Electronics and ECCE Asia (ICPE ECCE)*, May 2011, pp. 2352–2358.

[4] C. Collins and M. Duffy, "Limits and opportunities for distributed inductors in high-current, high-frequency applications," *IEEE Transactions on Power Electronics*, vol. 25, no. 11, pp. 2710–2721, Nov. 2010.

[5] C. Quinn, K. Rinne, T. O'Donnell, M. Duffy, and C. Mathuna, "A review of planar magnetic techniques and technologies," in *Sixteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2001. APEC 2001*, vol. 2, 2001, pp. 1175–1183 vol.2.

[6] D. C. Pentz and I. Hofsajer, "Novel technique for shaped planar inductor winding optimization in gapped core applications," in *IEEE Power Engineering Society Conference and Exposition in Africa, 2007. PowerAfrica '07*, Jul. 2007, pp. 1–6.

[7] L. Ye, G. Skutt, R. Wolf, and F. Lee, "Improved winding design for planar inductors," in *, 28th Annual IEEE Power Electronics Specialists Conference, 1997. PESC '97 Record*, vol. 2, Jun. 1997, pp. 1561–1567 vol.2.

[8] C. Ionescu, P. Svasta, D. Bonfert, and G. Klink, "Analysis of planar inductors on flexible substrates for RFID antennas," in *2010 33rd International Spring Seminar on Electronics Technology (ISSE)*, May 2010, pp. 338–343.

[9] L. Dixon, "Magnetic core properties," Oct. 1994. [Online]. Available: www.ti.com/lit

[10] M. Rylko, B. Lyons, K. Hartnett, J. Hayes, and M. Egan, "Magnetic material comparisons for high-current gapped and gapless foil wound inductors in high frequency dc-dc converters," in *Power Electronics and Motion Control Conference, 2008. EPE-PEMC 2008. 13th*, Sep. 2008, pp. 1249–1256.

[11] M. Xingkui and C. Wei, "Winding loss mechanism analysis and the design for a new structure high-frequency gapped inductor," in *Magnetics Conference, 2005. INTERMAG Asia 2005. Digests of the IEEE International*, Apr. 2005, pp. 1073–1074.

[12] W. Chen, J. He, H. Luo, Y. Hu, and C.-C. Wen, "Winding loss analysis and new air-gap arrangement for high-frequency inductors," in *Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual*, vol. 4, 2001, pp. 2084–2089 vol. 4.

[13] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Springer, Jan. 2001.

[14] X. Huang, K. D. T. Ngo, and G. Bloom, "Design techniques for planar windings with low resistances," in *Applied Power Electronics Conference and Exposition, 1995. APEC '95. Conference Proceedings 1995., Tenth Annual*, Mar. 1995, pp. 533–539 vol.2.

[15] R. Prieto, R. Asensi, and J. Cobos, "Selection of the appropriate winding setup in planar inductors with parallel windings," in *2010 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2010, pp. 4599–4604.

[16] S. Cuk, "Basics of switched-mode power conversion: topologies, magnetics, and control," in *Advaces in Switched-Mode Power Conversion*, 2nd ed. Irvine, CA: TESLAco, 1995.

[17] K. Venkatachalam, C. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters," in *2002 IEEE Workshop on Computers in Power Electronics, 2002. Proceedings*, Jun. 2002, pp. 36–41.

[18] J. Reinert, A. Brockmeyer, and R. De Doncker, "Calculation of losses in ferro- and ferrimagnetic materials based on the modified steinmetz equation," *IEEE Transactions on Industry Applications*, vol. 37, no. 4, pp. 1055–1061, Jul. 2001.

[19] J. Li, T. Abdallah, and C. Sullivan, "Improved calculation of core loss with nonsinusoidal waveforms," in *Conference Record of the 2001 IEEE Industry Applications Conference, 2001. Thirty-Sixth IAS Annual Meeting*, vol. 4, Sep. 2001, pp. 2203–2210 vol.4.

[20] Y. Corporation, "ER18 low-profile planar core - datasheet," Sep. 2008. [Online]. Available: www.ferroxcube.com

[21] ——, "Ferrite 3F3 material specification," Sep. 2008. [Online]. Available: www.ferroxcube.com

[22] ——, "Planar ER cores and accessories," Sep. 2008. [Online]. Available: www.ferroxcube.com

[23] T. Sato, K. Watanabe, H. Igarashi, T. Matsuo, T. Mifune, K. Kawano, M. Suzuki, Y. Uehara, and A. Furuya, "3-d optimization of ferrite inductor considering hysteresis loss," *IEEE Transactions on Magnetics*, vol. 49, no. 5, pp. 2129–2132, May 2013.

[24] R. Prieto, J. Cobos, O. Garcia, P. Alou, and J. Uceda, "Using parallel windings in planar magnetic components," in *Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual*, vol. 4, 2001, pp. 2055–2060 vol. 4.

[25] R. Asensi, R. Prieto, J. Cobos, and J. Uceda, "Modeling high-frequency multiwinding magnetic components using finite-element analysis," *IEEE Transactions on Magnetics*, vol. 43, no. 10, pp. 3840–3850, Oct. 2007.

[26] S. Ito, T. Mifune, T. Matsuo, M. Suzuki, and K. Kawano, "Finite element analysis of a ferrite-core inductor with direct current bias current using an equivalent-circuit model of dynamic hysteretic properties," *Journal of Applied Physics*, vol. 115, no. 17, pp. 17A330–17A330–3, May 2014.

[27] J. Pollock and C. Sullivan, "Modelling foil winding configurations with low AC and DC resistance," in *Power Electronics Specialists Conference, 2005. PESC '05. IEEE 36th*, Jun. 2005, pp. 1507–1512.

[28] D. Perreault, J. Hu, J. Rivas, Y. Han, O. Leitermann, R. Pilawa-Podgurski, A. Sagneri, and C. Sullivan, "Opportunities and challenges in very high frequency power conversion," in *Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition, 2009. APEC 2009*, Feb. 2009, pp. 1–14.

[29] S. W. Henning, L. L. Jenkins, and C. G. Wilson, "Manual assembly of 400um bumped-die GaN power semicoductor devices," San Diego, CA, Sep. 2012, p. 10.

[30] L. Jenkins, C. Wilson, J. Moses, J. Aggas, and R. Dean, "A reliable and cost-effective assembly process for quick prototyping with GaN FETs and other flip-chip packages," in *2013 IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Oct. 2013, pp. 84–87.

[31] L. L. Jenkins, "Discussion on how to fix the diode issue with the sync-buck v4.3 board," Dec. 2013.

Appendix A

MATLAB Scripts

A.1 Efficiency plotting script

```
1
2  %% Specify comparison name
3  compName = 'Buck Converter V4.3 Efficiency Improvement';
4  fileName = 'V4_3_Improve';
5  %% Specify Y-Lim range for plots
6  YMIN = 65;
7  YMAX = 97;
8  %% Specify plot options
9
10 % Plot data markers?
11 dataMarkers = 'y';
12
13 % Save .FIG file?
14 FIGsave = 'n';
15
16 % Legend location
17 legLoc = 'SouthWest';
18 %% Cell Array of plot types
19 if dataMarkers == 'n'
20     plotStyle = {'--c' '--g' '-.b' '-r' '--m' '-b' '-k' ':r' '-y' '-g'...
21         '--b' '-c' '-y' '-m' '-k' '-b' '-r' '-k' '-g' '-c' '-y'...
22         '-r' '-g' '-b' '-k' '-c' '-m' ':m' '-b'};
23 elseif dataMarkers == 'y'
24     plotStyle = {'--c^' '--go' '-.b*' '-r+' '--mx' '-bs' '-kd' ':r^'...
25         '-yv' '-g>' '--b<' '-cp' '-yx' '-mx' '-kx' '-bx' '-r*' '-ko' ...
26         '-g*' '-c+' '-yo' '-rh' '-gp' '-bd' '-ks' '-cs' '-mv' ':mh' '-bv'};
27 else
28     error('Invalid dataMarkers specification...');
29 end
30 %% Make directory to store plots
31 wb = waitbar(0,'Setting up new directory...');
32 set(wb,'Position',[700 200 270 56.25])
33 mkdir(compName);
34 %% PLOT VS. LOAD
35
36 % Determine common frequencies
37 Lcount = length(L);
38 commF = L(1).freq_start:L(1).freq_step:L(1).freq_stop;
39 for i=2:Lcount
```

```
40      bufferF = L(i).freq_start:L(i).freq_step:L(i).freq_stop;
41      commF = intersect(commF,bufferF);
42  end
43
44  % Set up parameters for waitbar
45  stepTot = Lcount*length(commF);
46  step = 1/stepTot;
47  bar = 0;
48
49  % Cycle thru common frequencies
50  for i=1:length(commF)
51      fprintf('Plotting frequency %d kHz\n',commF(i));
52      message = sprintf('Plotting frequency %s kHz',num2str(commF(i)));
53      waitbar(bar,wb,message);
54
55      % Assemble title and file strings
56      fid = strcat(fileName,num2str(commF(i)),'kHz');
57      if dataMarkers == 'n'
58          fidPNG = strcat(fileName,num2str(commF(i)),'kHz','.png');
59          fidPNG_small = strcat(fileName,num2str(commF(i)),'kHz_small','.png');
60      else
61          fidPNG = strcat(fileName,'Markers_',num2str(commF(i)),'kHz','.png');
62          fidPNG_small = strcat(fileName,'Markers_',num2str(commF(i)),...
63              'kHz_small','.png');
64      end
65      titleStr = strcat(compName,{' - '},num2str(commF(i)),{' '},'kHz');
66
67      % Get efficiency curves for current frequency
68      for j=1:Lcount
69          % Use appropriate load and efficiency values if DMM available
70          f_buffer = L(j).data_FreqSort(:,2);
71          if L(j).DMM == 'y'
72              L_buffer = L(j).data_FreqSort(:,8);
73              Eff_buffer = L(j).data_FreqSort(:,10);
74          elseif L(j).DMM == 'n'
75              L_buffer = L(j).data_FreqSort(:,3);
76              Eff_buffer = L(j).data_FreqSort(:,5);
77          else
78              error('Corrupt data file');
79          end
80
81          % Get current load and efficiency values and sort by measured Iout
82          ind = find(f_buffer == commF(i));
83          loadVec = L_buffer(ind(1):ind(end));  %#ok<*SAGROW>
84          dataVec = Eff_buffer(ind(1):ind(end));
85          currentData = sortrows([loadVec dataVec],1);
86
87
88          % Make legend entry for current inductor
89          coreStr = L(j).CoreGeometry;
90          if isnumeric(L(j).Turns)
91              turnStr = strcat(num2str(L(j).Turns),' turns');
92          else
93              turnStr = strcat(L(j).Turns(1),' parallel turns');
```

```
94          end
95          matStr = L(j).Material;
96          gapStr = strcat(num2str(L(j).Gap),' mil gap');
97          inductance = L(j).L;
98          legendEntry = strcat(coreStr,{' '},turnStr,{' '},matStr,{' '},...
99              gapStr, {' - '},num2str(inductance,3), 'uH');
100         legendInfo{j} = char(legendEntry); %#ok<SAGROW>
101
102         % Add curve to plot
103         h = figure(1);
104         hold on;
105         plot(currentData(:,1),currentData(:,2),plotStyle{j});
106         fprintf('Plot %s added\n',char(legendEntry));
107         message = sprintf('Plot %s added',char(legendEntry));
108         bar = bar + step;
109         waitbar(bar,wb,message);
110     end
111
112     % Label plot
113     title(titleStr);
114     xlabel('Load Current [A]');
115     ylabel('Efficiency [%]');
116     xlim([0,28]);
117     ylim([YMIN,YMAX]);
118     % adjust legend location to not block curves
119     if commF(i) < 160
120         legend(legendInfo,'Location','NorthEast');
121     else
122         legend(legendInfo,'Location','SouthWest');
123     end
124     cd(compName)
125     message = sprintf('Saving PNG file - %d kHz %s/%s',commF(i),...
126         num2str(i),num2str(length(commF)));
127     waitbar(bar,wb,message);
128     grid on;
129     print(h,'-dpng','-r600', fidPNG);
130     print(h,'-dpng','-r100', fidPNG_small);
131     if FIGsave == 'y'
132         message = sprintf('Saving FIG file - %d kHz %s/%s',num2str(i),...
133             num2str(length(commF)));
134         waitbar(bar,wb,message);
135         hgsave(h,fid);
136     end
137     % return to function folder, close figure
138     cd ..;
139     close(h);
140
141     fprintf('Plot %d/%d complete - %d kHz\n',i,length(commF),commF(i));
142
143 end
144
145 fprintf('Vs. Load plot generation complete...\n\n');
146 close all;
147 clear wb;
```

```
148 %% PLOT VS. FREQ
149
150 % Round all load data to nearest integer and get common load currents
151 Lcount = length(L);
152 for i=1:Lcount
153     ind = 1;
154     Fstep = L(i).freq_stepN;
155     if L(i).DMM =='y'
156         loadCol = 8;
157     elseif L(i).DMM == 'n'
158         loadCol = 3;
159     else
160         error('Corrupt data file');
161     end
162
163     % use round to integer of average load values
164     for j=1:L(i).load_stepN
165         I_act = round(mean(L(i).data_LoadSort(ind:ind+Fstep-1,loadCol)));
166         L(i).data_LoadSort(ind:ind+Fstep-1,loadCol) = I_act;
167         ind = Fstep*j+1;
168         Ibuffer(j) = I_act;
169     end
170
171     % get common load currents
172     if i==1
173         commI = Ibuffer;
174     else
175         commI = intersect(commI,Ibuffer);
176     end
177     Ibuffer = [];   % clear load buffer
178 end
179
180 % Set up parameters for waitbar
181 stepTot = Lcount*length(commI);
182 step = 1/stepTot;
183 bar = 0;
184
185 % Plot for each common load current
186 for i=1:length(commI)
187     fprintf('Plotting load current %d A\n',commI(i));
188     message = sprintf('Plotting load current %s A',num2str(commI(i)));
189     %waitbar(bar,wb,message);
190
191     % Assemble title and file strings
192     fid = strcat(fileName,num2str(commI(i)),'A');
193     if dataMarkers == 'n'
194         fidPNG = strcat(fileName,num2str(commI(i)),'A','.png');
195         fidPNG_small = strcat(fileName,num2str(commI(i)),'A_small','.png');
196     else
197         fidPNG = strcat(fileName,'Markers_',num2str(commI(i)),'A','.png');
198         fidPNG_small = strcat(fileName,'Markers_',num2str(commI(i)),...
199             'A_small','.png');
200     end
201     titleStr = strcat(compName,{' - '},num2str(commI(i)),{' '},'A');
```

```
202
203     % Get efficiency curves for current load
204     for j=1:Lcount
205         % Use appropriate load and efficiency values if DMM available
206         if L(j).DMM == 'y'
207             I_buffer = L(j).data_LoadSort(:,8);
208             Eff_buffer = L(j).data_LoadSort(:,10);
209         elseif L(j).DMM == 'n'
210             I_buffer = L(j).data_LoadSort(:,3);
211             Eff_buffer = L(j).data_LoadSort(:,5);
212         else
213             error('Corrupt data file');
214         end
215
216         % store available frequency points in buffer
217         freqVec = L(j).data_LoadSort(1:L(j).freq_stepN,2);
218
219         % Get efficiency data for current load value
220         ind = find(I_buffer == commI(i));
221         dataVec = Eff_buffer(ind:ind+L(j).freq_stepN-1);
222
223         % Make legend entry for current inductor
224         coreStr = L(j).CoreGeometry;
225         if isnumeric(L(j).Turns)
226             turnStr = strcat(num2str(L(j).Turns),' turns');
227         else
228             turnStr = strcat(L(j).Turns(1),' parallel turns');
229         end
230         matStr = L(j).Material;
231         gapStr = strcat(num2str(L(j).Gap),' mil gap');
232         inductance = L(j).L;
233         legendEntry = strcat(coreStr,{' '},turnStr,{' '},matStr,{' '},...
234             gapStr, {' - '},num2str(inductance,3), 'uH');
235         legendInfo{j} = char(legendEntry); %#ok<SAGROW>
236
237         % Add curve to plot
238         h = figure(1);
239         hold on;
240         plot(freqVec,dataVec,plotStyle{j});
241         fprintf('Plot %s added\n',char(legendEntry));
242         message = sprintf('Plot %s added',char(legendEntry));
243         %bar = bar + step;
244         %waitbar(bar,wb,message);
245     end
246
247     % Label plot
248     title(titleStr);
249     xlabel('Frequency [kHz]');
250     ylabel('Efficiency [%]');
251     ylim([YMIN,YMAX]);
252     if commI(i)>16
253         legend(legendInfo,'Location','North');
254     else
255         legend(legendInfo,'Location','South');
```

```
256     end
257
258     cd(compName)
259     message = sprintf('Saving PNG file - %d A %s/%s',commI(i),...
260         num2str(i), num2str(length(commI)));
261     %waitbar(bar,wb,message);
262     grid on;
263     print(h,'-dpng','-r600', fidPNG);
264     print(h,'-dpng','-r100', fidPNG_small);
265     if FIGsave == 'y'
266         message = sprintf('Saving FIG file - %d A %s/%s',commI(i),...
267             num2str(i), num2str(length(commI)));
268         waitbar(bar,wb,message);
269         hgsave(h,fid);
270     end
271     cd ..;
272     close(h);
273
274     fprintf('Plot %d/%d complete - %d A\n',i,length(commI),commI(i));
275
276 end
277
278 fprintf('Vs. Frequency plot generation complete...\n');
```

A.2 Data storage script

```
clear all;
clc;
load V4_1;
cd('C:\Users\jaggas\Google Drive\Thesis\Power Project\AutomatedTester\V4_3')

%% FILE FORMAT
%
% SyncBuck_coreGeo_xtxgxxx[_doubleBoard].csv
%            ^     ^ ^  ^         ^
%            1     2 3  4         5
%
% Format Key:
%   1 - core geometry (i.e. E18, E22, ER23, ER18)
%   2 - turn number (i.e. 1 or 2)
%   3 - effective middle post gap width in mils (i.e. 2,4,6, etc)
%   4 - material (i.e. 3c96, 3f3, 3c92)
%   5 - append _doubleBoard if using stacked breakout boards
%

%% Import data files
files = dir;

for i=3:length(files)
    %% Get current file and import data
    fileH = files(i);
    fid = fileH.name;

    % get test params
    dashI = find(fid == '_');
    uScI = find(fid == '_');
    perI = find(fid == '.');
    dashSc = union(dashI,uScI);
    markers = union(dashSc,perI);
    coreGeo = fid(markers(1)+1:markers(2)-1);

    Linfo = fid(markers(2)+1:markers(3)-1);
    turns = Linfo(1);
    gI = find(Linfo == 'g');
    gap = Linfo(3:gI-1);
    material = Linfo(gI+1:end);

    if ~isempty(strfind(fid,'doubleBoard'))
        BoardStack = 2;
    else
        BoardStack = 1;
    end

    % ensure file is in csv format
    check = fid(markers(end):end);
    if strcmp(check,'.csv')
```

```
51          fprintf('%s data validated\n',fid);
52      else
53          fprintf('%s data not valid\n',fid);
54          break;
55      end
56
57      % import data
58      x = importdata(fid);
59
60      %% Select data elements to save
61      Inom = x.data(:,1);
62      freq = x.data(:,2);
63      Iout = x.data(:,14);
64      Pout = x.data(:,18);
65      Eff = x.data(:,19);
66      Eff_5V = x.data(:,20);
67      Eff_tot = x.data(:,21);
68      try
69          Iout_DMM = x.data(:,23);
70          Pout_DMM = x.data(:,27);
71          Eff_DMM = x.data(:,28);
72          Eff_DMM_5V = x.data(:,29);
73          data = [Inom freq Iout Pout Eff Eff_5V Eff_tot Iout_DMM Pout_DMM ...
74              Eff_DMM Eff_DMM_5V];
75          DMM = 'y';
76      catch
77          data = [Inom freq Iout Pout Eff Eff_5V Eff_tot];
78          DMM = 'n';
79      end
80
81      % sort data according to frequency and nominal load current
82      y.data_LoadSort = sortrows(data,1);
83      y.data_FreqSort = sortrows(data,2);
84      y.freq_start = min(freq);
85      y.freq_step = diff(y.data_LoadSort(1:2,2));
86      y.freq_stop = max(freq);
87      y.freq_stepN = (max(freq) - min(freq)) / y.freq_step + 1;
88
89      y.load_start = min(Inom);
90      y.load_step = diff(y.data_FreqSort(1:2,1));
91      y.load_stop = max(Inom);
92      y.load_stepN = (max(Inom) - min(Inom)) / y.load_step + 1;
93
94      % assemble data structure with inductor information
95      cd ..;
96      y.CoreGeometry = coreGeo;
97      if (BoardStack == 2)
98          y.Turns = strcat(turns,'P');
99          turnID = strcat('turns_',turns,'P');
100     else
101         y.Turns = str2double(turns);
102         turnID = strcat('turns_',turns);
103     end
104     y.Material = upper(material);
```

```
105     y.Gap = str2double(gap);
106     y.L = Lcalc(coreGeo,material,turns,gap);
107     y.DMM = DMM;
108 
109     % Save to Version structure
110     gapID = strcat('gap_',gap);
111     matID = upper(strcat('M',material));
112     V4_3.(coreGeo).(turnID).(matID).(gapID) = y;
113 
114     % Display current board parameters
115     fprintf('Board %d/%d saved\n',i,length(files));
116     fprintf('Core Geometry: %s\n',coreGeo);
117     fprintf('# of Turns: %s\n',turns);
118     fprintf('Board Stack: %d\n',BoardStack);
119     fprintf('Material: %s\n',material);
120     fprintf('Gap Width: %s\n',gap);
121     fprintf('DMM data available: %s\n\n',DMM);
122     cd('C:\Users\jaggas\Google Drive\Thesis\Power Project\AutomatedTester\')
123 end
124 
125 cd ..;
126 clearvars -except V4_1 V4_3
127 save V4_1;
```

A.3 Waveform generation and analysis

```
    %% Used to generate current waveforms

%% System parameters
N = 3;      % number of phases
f = 150;    % switching frequency in kHz
Idc = 12;   % dc current component
percI = 10; % percent ripple current
Vin = 12;
Vout = 1;
Nview = 2;  % number of period to view
M = 1000;   % points per period

%% Calculate waveform parameters

% switching period in microseconds
T = 1000/f;

% minimum and maximum current values
Imax = Idc + 0.5*percI/100*Idc;
Imin = Idc - 0.5*percI/100*Idc;

% duty cycle
D = Vout/Vin;

%% Build waveforms
% time
t = linspace(0,T*Nview,Nview*M);

% switch
swV1 = Vin*ones(1,ceil(D*M));
swV = repmat([swV1 zeros(1,floor((1-D)*M))],1,Nview);

% inductor voltage
L_V = swV - Vout;

% current
i1 = linspace(Imin,Imax,ceil(D*M));
i2 = linspace(Imax,Imin,floor((1-D)*M));
iWF = repmat([i1 i2],1,Nview);
Idc_line = Idc*ones(1,Nview*M);

% output voltage
Vo = iWF/Idc;

figure(1);
subplot(2,2,1);
plot(t,swV);

subplot(2,2,2);
plot(t,L_V);
```

```
51
52 subplot(2,2,3);
53 plot(t,iWF);
54
55 subplot(2,2,4);
56 plot(t,Vo);
57
58 H2 = figure(2);
59 P2 = plot(t,iWF,'LineWidth',3,'Color','r');
60 ylim([Idc-8 Idc+4]);
61 xlim([0 t(end)]);
62 xlabel('Time (t) [\mus]','FontSize',14);
63 ylabel('Current (I) [A]','FontSize',14);
64 title('Inductor Current Waveform','FontSize',16,'FontWeight','bold');
65 grid on;
66 c = get(get(H2,'CurrentAxes'));
67 c.FontSize = 14;
68 print(H2,'-dpng','-r300','InductorCurrent')
69
70 H4 = figure(4);
71 P4 = plot(t,iWF-Idc,'LineWidth',3,'Color','r');
72 ylim([-5 5]);
73 xlim([0 t(end)]);
74 xlabel('Time (t) [\mus]','FontSize',14);
75 ylabel('Current (I) [A]','FontSize',14);
76 title('Inductor Current - AC component','FontSize',16,'FontWeight','bold');
77 grid on;
78 c = get(get(H4,'CurrentAxes'));
79 c.FontSize = 14;
80 print(H4,'-dpng','-r300','InductorCurrent_AC')
81
82 %% FFT of current waveform
83
84 % downsample factor
85 L = 50;
86
87 % # of FFT points
88 NFFT = 2048;
89
90 % decimate the signal, remove the DC offset and study only the AC component
91 iD = downsample(iWF,L)-12;
92
93 % new Nyquiest frequency
94 fNyq = 0.5*M*f*1e3/L;
95
96 % take FFT and assemble frequency vector
97 ID = abs(fftshift(fft(iD,NFFT)));
98 ID = 10*log10(ID/max(ID));
99 fvec = linspace(0,fNyq,NFFT/2);
```

Appendix B
Material Specifications

3C92 SPECIFICATIONS

A low frequency, high Bsat power material for use in power inductors at frequencies up to 0.2 MHz.

SYMBOL	CONDITIONS	VALUE	UNIT
μ_i	25 °C; ≤10 kHz; 0.25 mT	1500 ±20%	
μ_a	100 °C; 25 kHz; 200 mT	≈ 5000	
B	25 °C; 10 kHz; 1200 A/m	≈ 540	mT
	100 °C; 10 kHz; 1200 A/m	≈ 460	
	140 °C; 10 kHz; 1200 A/m	≈ 400	
P_V	100 °C; 100 kHz; 100 mT	≈ 50	kW/m^3
	100 °C; 100 kHz; 200 mT	≈ 350	
ρ	DC; 25 °C	≈ 5	Ωm
T_C		≥ 280	°C
density		≈ 4800	kg/m^3

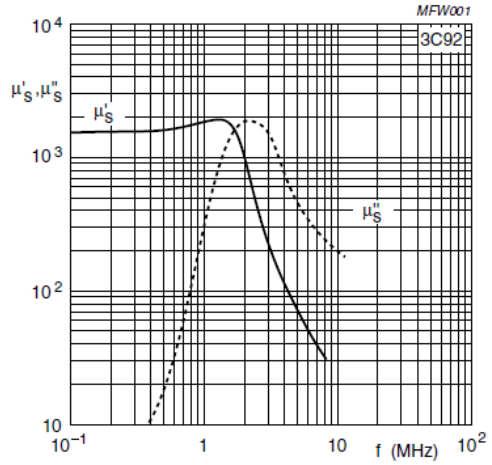


Fig.1 Complex permeability as a function of frequency.

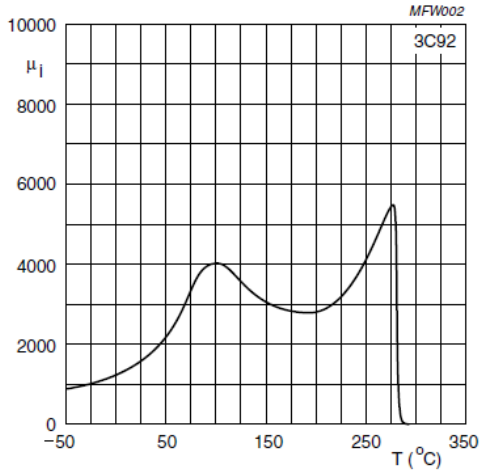


Fig.2 Initial permeability as a function of temperature.

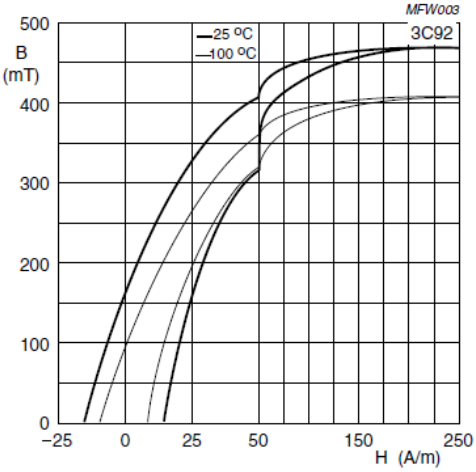


Fig.3 Typical B-H loops.

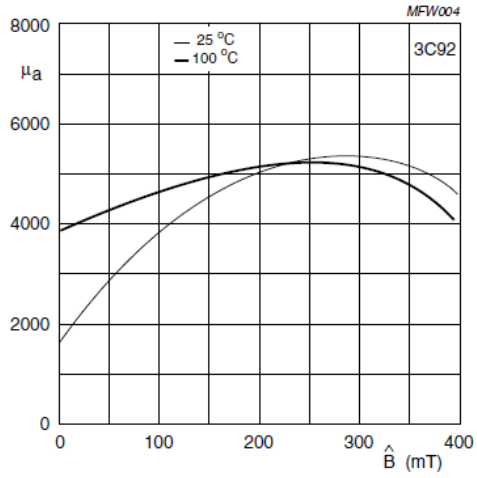


Fig.4 Amplitude permeability as a function of peak flux density.

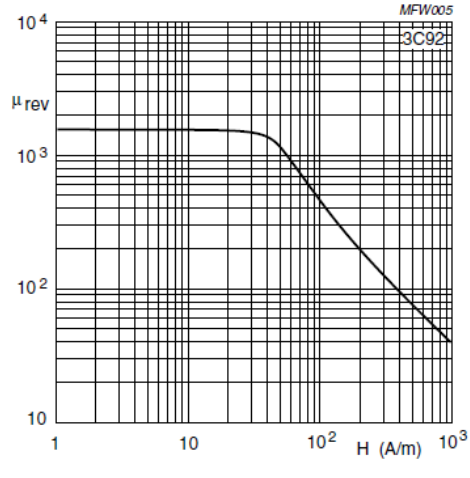


Fig.5 Reversible permeability as a function of magnetic field strength.

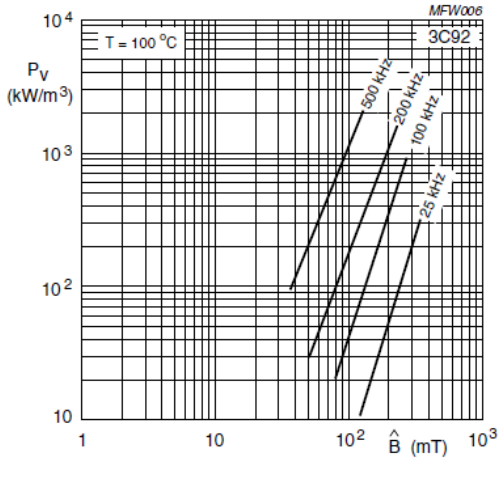


Fig.6 Specific power loss as a function of peak flux density with frequency as a parameter.

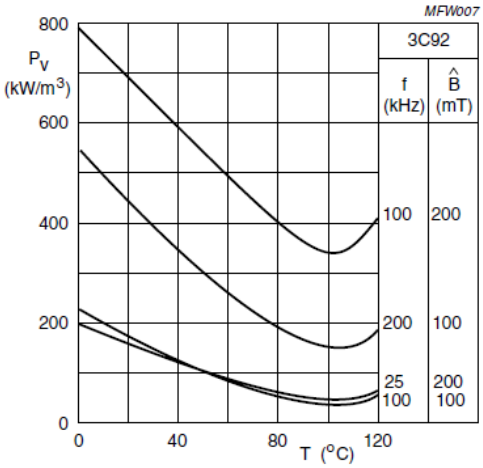


Fig.7 Specific power loss for several frequency/flux density combinations as a function of temperature.

3C94 SPECIFICATIONS

A low frequency power material for use in power and general purpose transformers at frequencies up to 0.3 MHz.

SYMBOL	CONDITIONS	VALUE	UNIT
μ_i	25 °C; ≤10 kHz; 0.25 mT	2300 ±20%	
μ_a	100 °C; 25 kHz; 200 mT	5500 ±25%	
B	25 °C; 10 kHz; 1200 A/m	≈ 470	mT
	100 °C; 10 kHz; 1200 A/m	≈ 380	
P_V	100 °C; 100 kHz; 100 mT	≈ 50	kW/m^3
	100 °C; 100 kHz; 200 mT	≈ 350	
ρ	DC, 25 °C	≈ 5	Ωm
T_C		≥ 220	°C
density		≈ 4800	kg/m^3

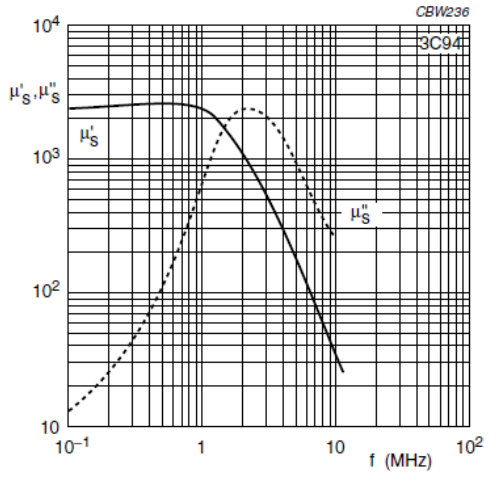


Fig.1 Complex permeability as a function of frequency.

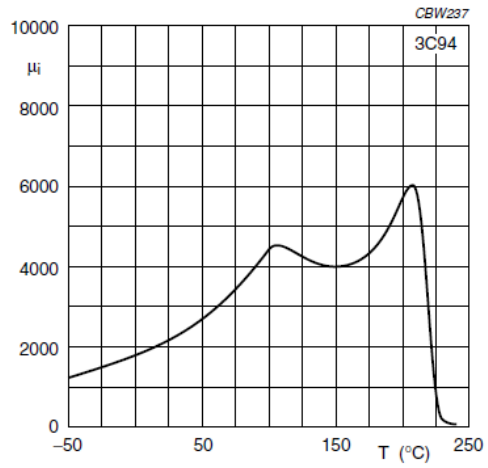


Fig.2 Initial permeability as a function of temperature.

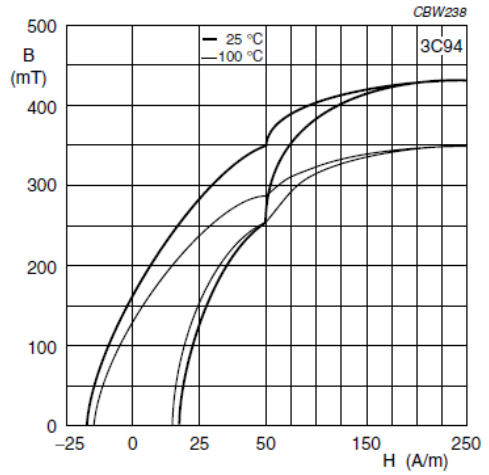


Fig.3 Typical B-H loops.

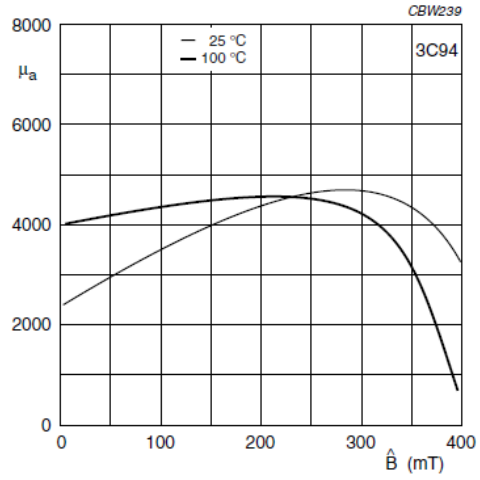


Fig.4 Amplitude permeability as a function of peak flux density.

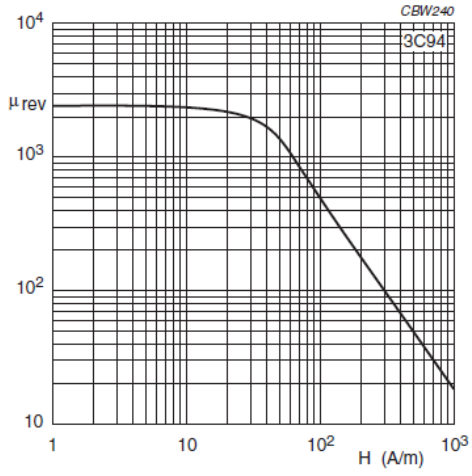


Fig.5 Reversible permeability as a function of magnetic field strength.

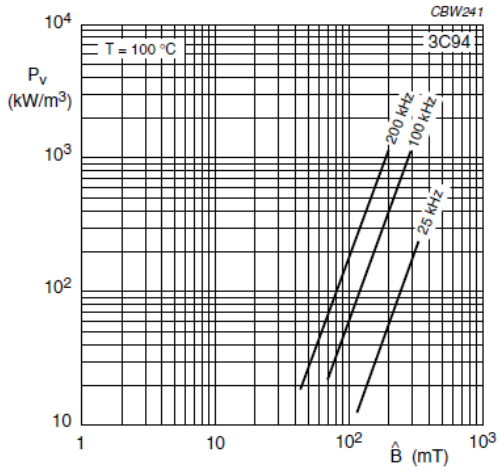


Fig.6 Specific power loss as a function of peak flux density with frequency as a parameter.

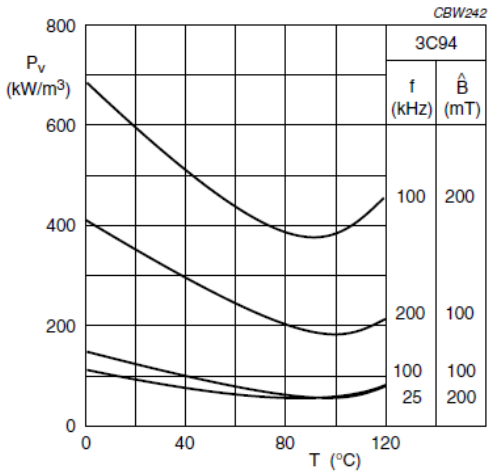


Fig.7 Specific power loss for several frequency/flux density combinations as a function of temperature.

3C96 SPECIFICATIONS

A low to medium frequency power material for use in power and general purpose transformers at frequencies up to 0.4 MHz.

	CONDITIONS	VALUE	UNIT
μ_i	25 °C; ≤10 kHz; 0.25 mT	2000 ±20%	
μ_a	100 °C; 25 kHz; 200 mT	≈ 5500	
B	25 °C; 10 kHz; 1200 A/m	≈ 500	mT
	100 °C; 10 kHz; 1200 A/m	≈ 440	
P_V	100 °C; 100 kHz; 100 mT	≈ 40	kW/m^3
	100 °C; 100 kHz; 200 mT	≈ 300	
	100 °C; 500 kHz; 50 mT	≈ 250	
ρ	DC; 25 °C	≈ 5	Ωm
T_C		≥ 240	°C
density		≈ 4800	kg/m^3

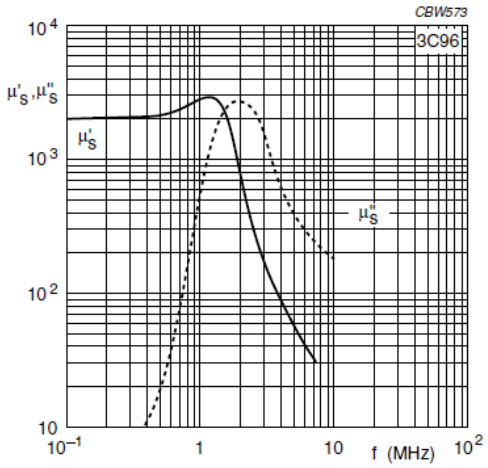


Fig.1 Complex permeability as a function of frequency.

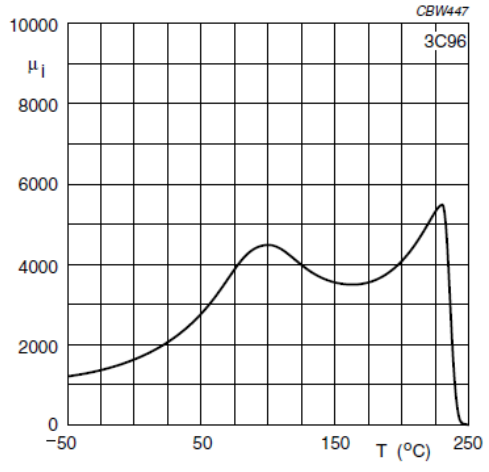


Fig.2 Initial permeability as a function of temperature.

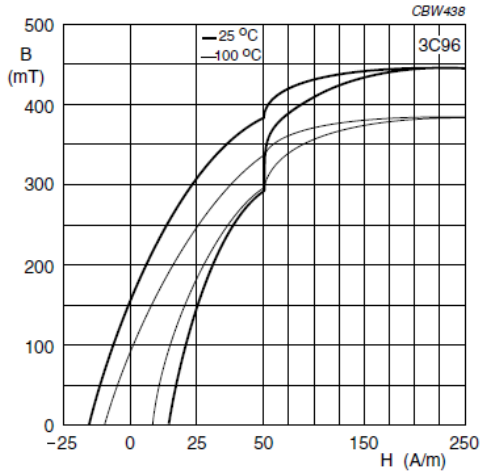


Fig.3 Typical B-H loops.

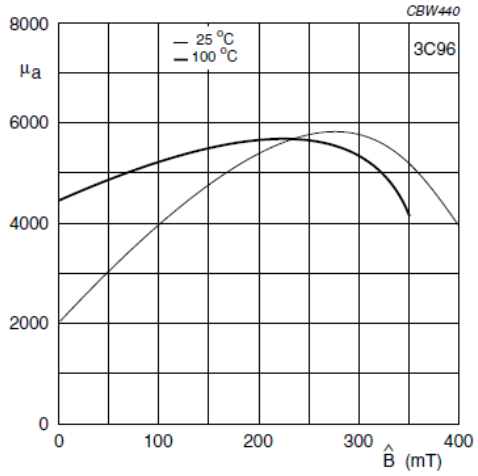


Fig.4 Amplitude permeability as a function of peak flux density.

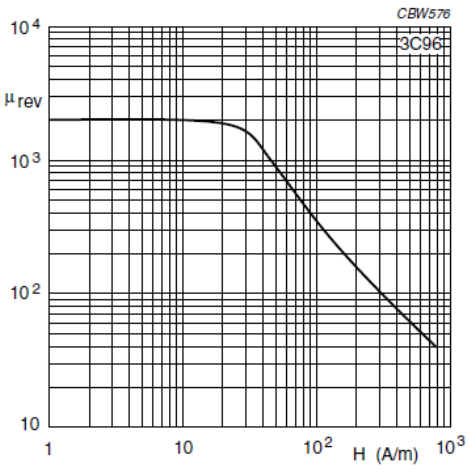


Fig.5 Reversible permeability as a function of magnetic field strength.

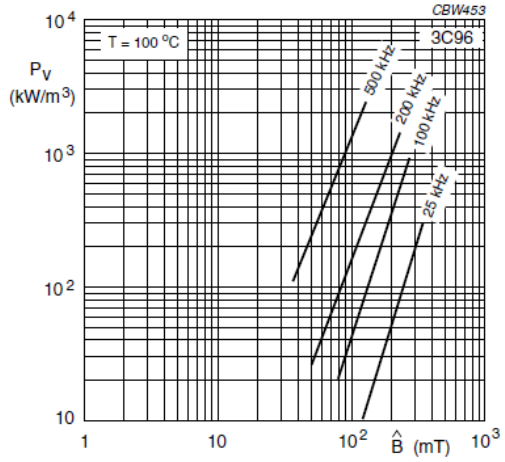


Fig.6 Specific power loss as a function of peak flux density with frequency as a parameter.

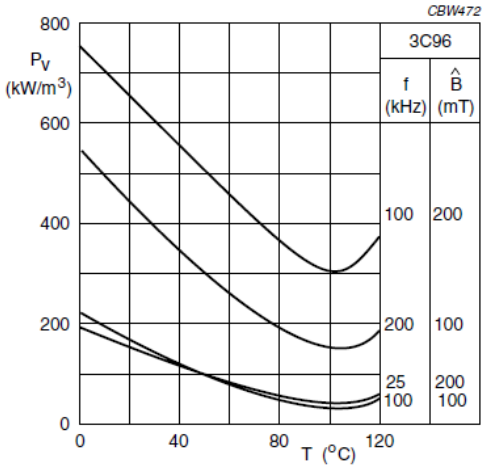


Fig.7 Specific power loss for several frequency/flux density combinations as a function of temperature.

3F3 SPECIFICATIONS

A medium frequency power material for use in power and general purpose transformers at frequencies of 0.2 - 0.5 MHz.

SYMBOL	CONDITIONS	VALUE	UNIT
μ_i	25 °C; ≤10 kHz; 0.25 mT	2000 ±20%	
μ_a	100 °C; 25 kHz; 200 mT	≈ 4000	
B	25 °C; 10 kHz; 1200 A/m	≈ 440	mT
	100 °C; 10 kHz; 1200 A/m	≈ 370	
P_V	100 °C; 100 kHz; 100 mT	≤80	kW/m^3
	100 °C; 400 kHz; 50 mT	≤150	
ρ	DC; 25 °C	≈ 2	Ωm
T_C		≥200	°C
density		≈ 4750	kg/m^3

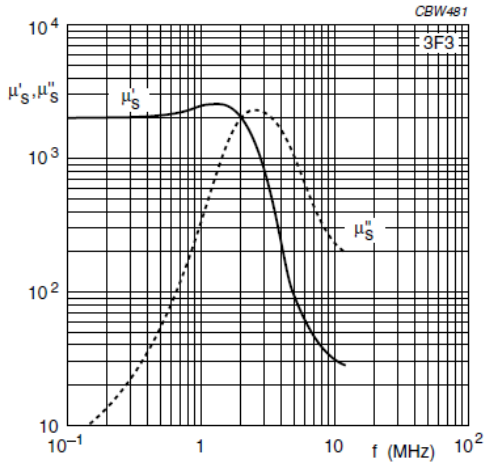


Fig.1 Complex permeability as a function of frequency.

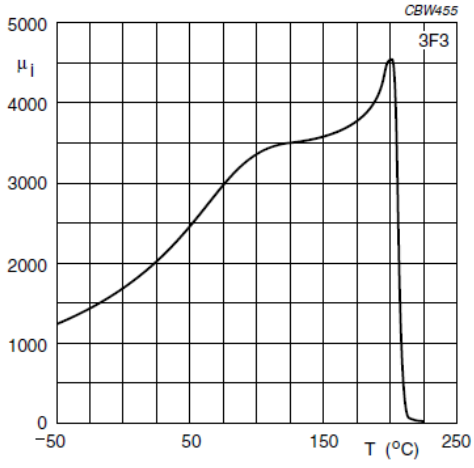


Fig.2 Initial permeability as a function of temperature.

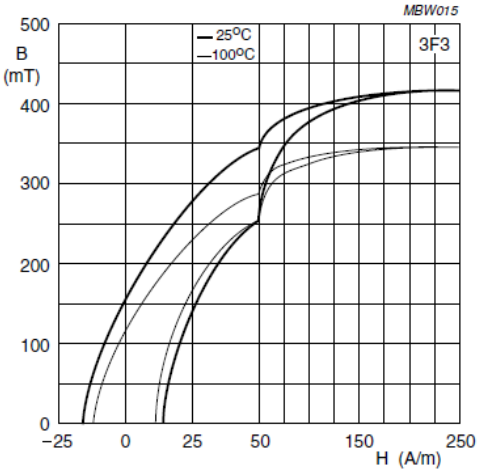


Fig.3 Typical B-H loops.

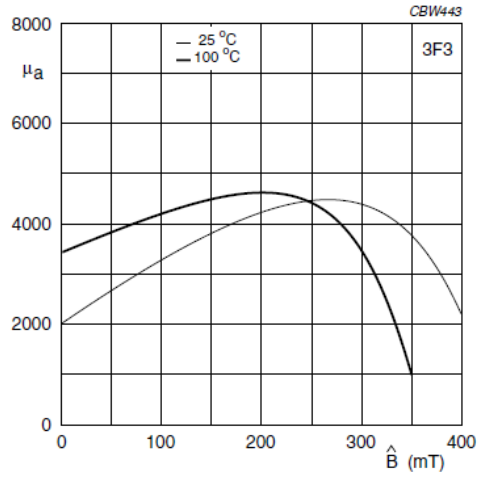


Fig.4 Amplitude permeability as function of peak flux density.

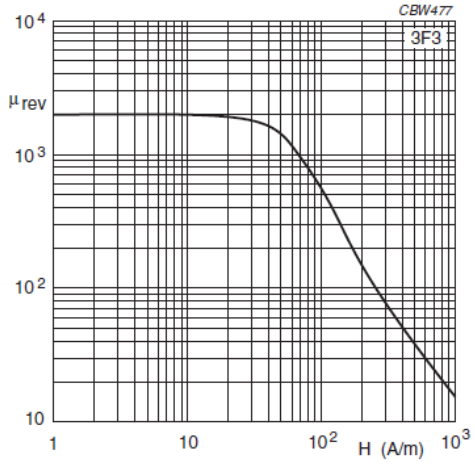


Fig.5 Reversible permeability as a function of magnetic field strength.

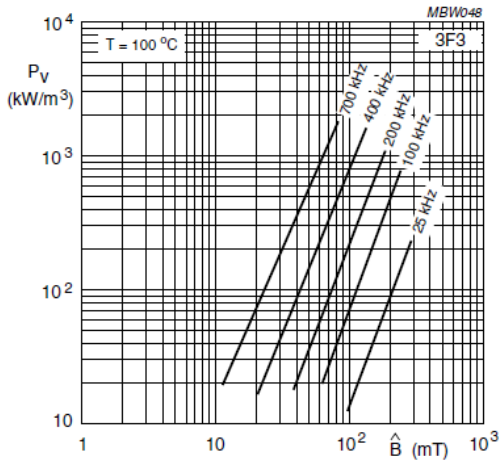


Fig.6 Specific power loss as a function of peak flux density with frequency as a parameter.

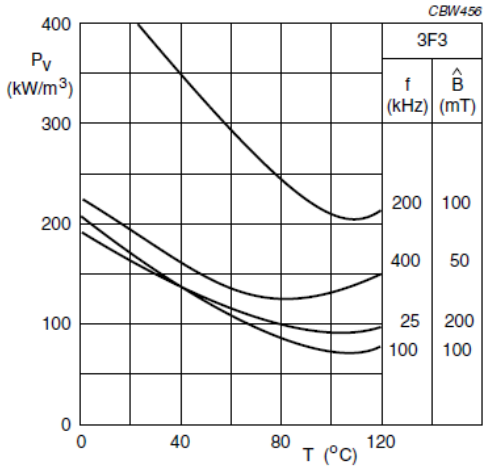


Fig.7 Specific power loss for several frequency/flux density combinations as a function of temperature.