Device Simulation of Density of Interface States of Temperature Dependent Carrier Concentration in 4H-SiC MOSFETs

by

Wei-Chung Shih

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Approved by

Guofu Niu, Alumni Professor of Electrical and Computer Engineering
Fa Foster Dai, Professor of Electrical and Computer Engineering
Bogdan Wilamowski, Professor of Electrical and Computer Engineering

Abstract

Interface traps play an important role in the SiO_2/4H-SiC interface. They are crucial issues for the current and trans-conductance in 4H-SiC MOSFET devices. In this thesis, we present a temperature and bias dependent model for simulations of trap occupation and also carrier concentration in a 4H-SiC MOSFET device. By fitting the Hall measurement data [1], we have various parameters for simulation, including the fixed oxide charge density and the interface trap density of states profile. These simulations enable us to observe temperature dependence of occupied trap densities and inversion layer carrier concentrations. In addition, bias dependence of trap density and occupation probability at different temperatures is also presented.

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Chapter 1

Introduction

1.1 Motivation

For the past 50 years, silicon (Si) has been the number one choice of semiconductor materials. It is in an almost perfect stage through extensive research and also is inexpensive to manufacture for so many years. In addition, it performs very reliably at room temperature. However, as modern electronics move to a more advanced level with increasing complexity, materials other than Si are under consideration. Several areas where Si has difficulties are in high temperature environments and high voltage conditions. In recent years, silicon carbide (SiC) has become the subject of extensive research in the area of high power and high temperature electronics. As a semiconductor and competitor to the omnipresent Si-technologies, SiC is considered superior in many applications requiring high power, temperature or frequency due to its large band gap, large dielectric breakdown field, large thermal conductivity, high saturation velocity and very low sensitivity to harsh chemical environments.

The properties of SiC have enabled the manufacturing of fabricating SiC metal-oxide-semicon-ductor field-effect transistors (MOSFETs) with significant advances in the area of working in high power, high temperature environment [4][5]. However, there are challenges in the development of SiC device: high channel resistance and low trans-conductance caused by low channel mobility and large densities of occupied interface traps at the SiC/SiO_2 interface [6][7]. Low inversion-channel mobilities have been reported for MOSFETS fabricated on Si-face 4H-SiC substrates [8][9][10] despite their high bulk mobility. These low mobilities lead to much higher on-state resistances in 4H-SiC MOSFETs [11][12]. These poor

electrical properties have been attributed to the large density of interface states (D_{it}) at the SiC/SiO_2 interface resulting in charge trapping [13].

1.2 Properties of Silicon Carbide

Compared to Si-based devices, SiC-based devices and integrated circuits can work at much higher temperatures and also much higher power. Because of the larger bandgap and superior thermal conductivity of SiC, it should be possible to use SiC-based devices at temperatures up to 500°C [14]. Table 1.1 shows a comparison of the material properties of Si and SiC.

Table 1.1: Important physical properties of Silicon and polytypes of SiC [3]

	Si	6H-SiC	4H-SiC
Bandgap(eV)	1.1	2.86	3.26
Bulk Electron Mobility (cm^2/Vs)	1500	300	900
Thermal Conductivity ($W/K \cdot cm$)	1.5	4.9	4.9
Breakdown Field (10^6 V/cm)	1	3	3
Saturation Velocity (10^7 V/cm)	1	2	2
Static Dielectric Constant	11.8	9.7	9.7

1.3 Wide Bandgap Property

The energy bandgap of 4H-SiC is 3.26eV [3], while Si has bandgap of 1.1eV at room temperature. This wide band gap property makes the electrons/holes harder to jump to the conduction band from the valence band at room temperature. Thus, even at high temperature, the generation-recombination of electrons and holes is still difficult. Moreover, Si-C bond is formed with a very strong bonding energy within a stable tetrahedral structure, which is very hard in nature. Therefore, SiC devices can sustain high radiation and can operate in extreme environment.

1.3.1 High Thermal Stability

The main problem of solid-state semiconductor power devices is heat. Si-based electronics have poor reliability in high temperature environments. On the other hand, because of the large bandgap, SiC-based devices can operate in high temperature and show a stable operation in wide range of temperature (27°C to 650°C) [15]. SiC has high thermal conductivity (4.9 W/K.cm) compared to Si (1.5 W/K.cm) [3] that results in lower junction-to-case thermal resistance. Thus, the volume and the size of the heat sink can be reduced with SiC-based power devices. Also, because SiC works in a high temperature environment, therefore, the need of an extra cooling is greatly reduced.

1.3.2 High Electric Breakdown Field and Saturation Drift Velocity

SiC has a high breakdown field (1.5∼4x10^6 V/cm) [15]. Therefore, device layer can be made thinner than Si for the same breakdown voltage rating. Because of the high breakdown field, high voltage rating power devices can be fabricated in SiC. In addition, SiC is capable to block higher voltages than Si by a factor of 10X [3] for the same thickness of material, due to its higher electric field breakdown strength.

The drift velocity of SiC poly-types (2x10^7cm/s) is twice that of Si (1x10^7cm/s) [15] and SiC also has a very small value of intrinsic carrier concentrations and negligible leakage current. Therefore, it is expected that SiC-based power devices can be operated at higher switching frequencies than Si-based power devices.

1.4 Limitations and Challenges in SiC Power MOS Device

Currently, the biggest challenge in development of SiC devices is low surface mobility at the SiC/SiO_2 interface. As described earlier, SiC-based devices and integrated circuits can

work at much higher temperatures and also much higher power, as compared to Si-based devices. However, temperature has a strong effect on the mobility and usually mobility decreases with the increase of temperature in SiC-based devices. In addition, carrier mobility has a direct effect on the channel resistivity. The channel resistance increases with the decrease of the mobility. Moreover, high gate voltage is required to turn the devices fully on which indicates that the on-resistance is dominated by the MOS channel resistance. This is mainly due to the low inversion layer mobility. The results suggest that further improvement in mobility is necessary to reduce the on-resistance.

The reason of this low surface mobility has been shown to be high densities of occupied interface traps at the SiC/SiO_2 interface [7][16]. Interface traps in SiC power MOS device are distributed randomly in energy across the band gap. A Device with a large number of trap densities will affect the performance of the device due to the loss of the carriers from the channel which results in lowering the conduction current of the SiC device. These interface traps affect the mobility of the SiC and thus cannot be ignored.

1.5 Thesis Structure

This thesis addresses the issues related to numerical simulation of a 4H-SiC device. We have extracted the density of interface states (D_{it}) profiles of the interface traps in the 4H-SiC MOSFET with different temperatures. In addition, with a 2D simulation model, the variation of occupied interface trap density with different bias in the 4H-SiC MOSFET is also investigated. By fitting the simulated curves to the experimental measured data [17][1] we can extract various parameters, including the D_{it} profiles and the fixed oxide charge densities.

This thesis is organized as follows: Chapter 2 introduces the device structure which contains the meshing, doping and gridding profiles. Chapter 3 details the device simulation concepts and 2D device simulation for temperature and bias dependent 4H-SiC MOSFET.

Chapter 4 investigates and discusses the simulation results obtained. Chapter 5 concludes the work.

Chapter 2

Device Structure

The first step in a device simulation is construction of the device. The structure of the device is created in Sentaurus Structure Editor, a TCAD tool from Synopsys, Inc. During device construction, the first step is to construct the boundary of the device. Moreover, we also need to define meshing, region and contact placement. The second step is doping the device with different doping file. This chapter gives a detailed description of the step by step construction of the device. A 2D schematic cross section of 4H-SiC MOSFET is presented for device simulation.

2.1 Region Definition and Boundary Construction

The device is divided into several different regions and layers. It is divided into the source, the drain, the substrate, the oxide and the interface regions, where the semiconductor equations are to be solved. The boundary contacts are where external voltage is applied or an artificial boundary is created. Sentaurus Structure Editor does not allow regions to overlap and has different ways to treat overlapping regions, depending on the Boolean behavior selected. Fig. 2.1 gives a 2D cross section showing the layer structures and various material regions we defined in this construction of device. The figure is not drawn to scale. The substrate consist only silicon carbide. The channel length is taken as 1um. The gate oxide thickness was built in two different scales for simulation comparison. Two oxide thickness scales are 53nm and 125nm respectively. In this work, a 4H-SiC MOSFET is designed for 2D device simulation.

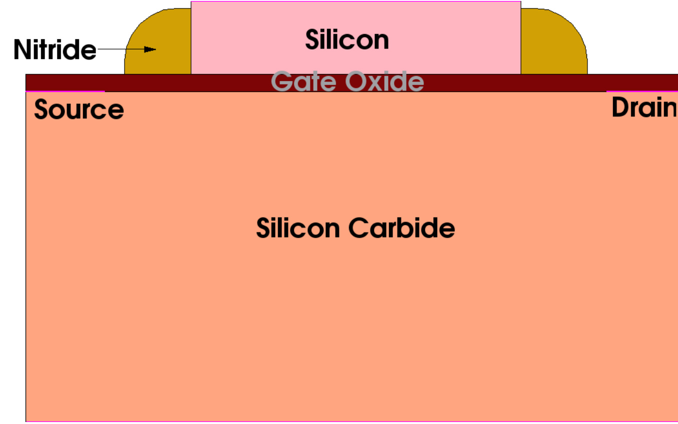

Figure 2.1: Schematic cross section showing the different materials used in construction of device.

2.2 Mesh and Doping Profile

Mesh generation is an important issue to any device simulation. In order to capture the physics of the inversion layer, the mesh is kept very fine near the SiC/SiO_2 interface. This enables us to extract detailed physics of the inversion layer. However, near the center of the device, the mesh is not too detailed as there is not much variation in these physical quantities. The finer the mesh means more nodes need to be solved.It would be unnecessary to build very fine mesh throughout the whole device. Therefore, the reduction of unnecessary nodes is also an important issue due to the tradeoff between accuracy and efficiency.

Constant doping was used for substrate and gate region while Gaussian doping implantation was used in source and drain region. Fig. 2.2 shows the doping and meshing schematic cross section of the 4H-SiC MOSFET device for simulation. The substrate region is Boron doped p-type substrate, source and drain region is doped with Arsenic. Boron doped poly-Si was used as the gate electrode. Fig. 2.3 shows the location where x-cut cutting through the schematic cross section of the 4H-SiC MOSFET device for simulation. Fig. 2.4 shows the doping concentration variation along the x-axis. A summary of the device structure and doping levels is shown in Table 2.3 and Table 2.2.

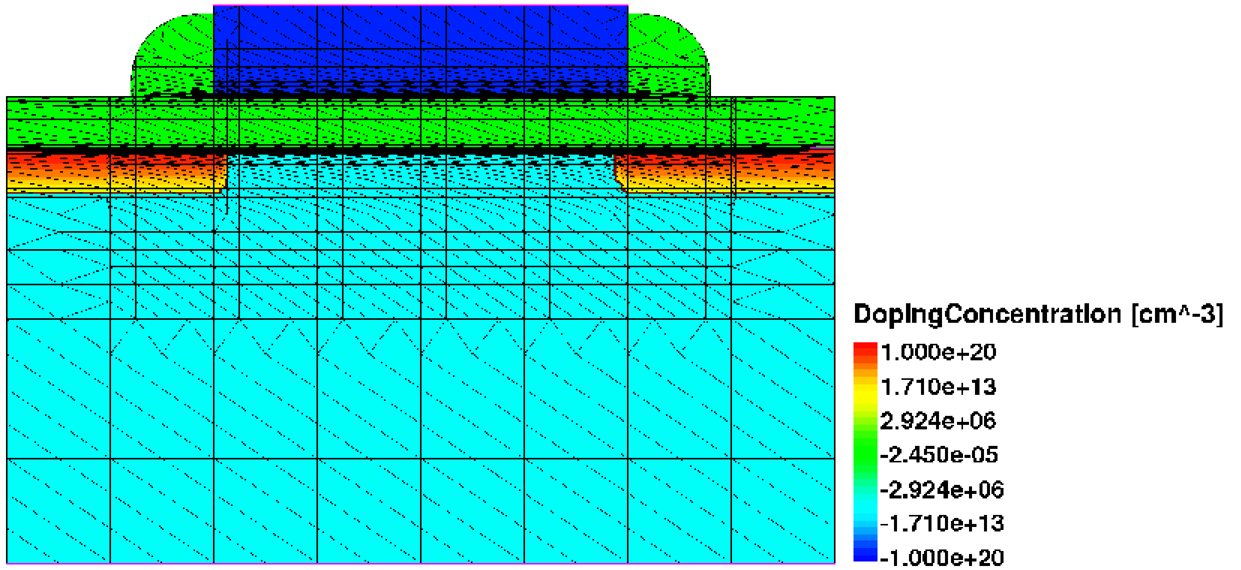

Figure 2.2: The doping and meshing schematic cross section of the 4H-SiC MOSFET.

Table 2.1: Device structure dimensions of the 4H-SiC MOSFET

	Device dimensions
Channel length	1 um
Oxide thickness	53nm/1250nm
S/D junction depth	0.1um

2.3 Parameter File

Silicon carbide crystallizes in numerous (more than 200) different modifications (polylypes). The most important are: cubic unit cell: 3C-SiC (cubic unit cell, zincblende); 2H-SiC; 4H-SiC; 6H-SiC (hexagonal unit cell, wurtzile); 15R-SiC (rhombohedral unit cell). Other polylypes with rhornbohedral unit cell: 21R-SiC 24R-SiC, 27R-SiC etc. For this thesis, the basic parameter files of 4H-SiC are listed in Table 3.1 and there are more detail parameter file in appendix A.

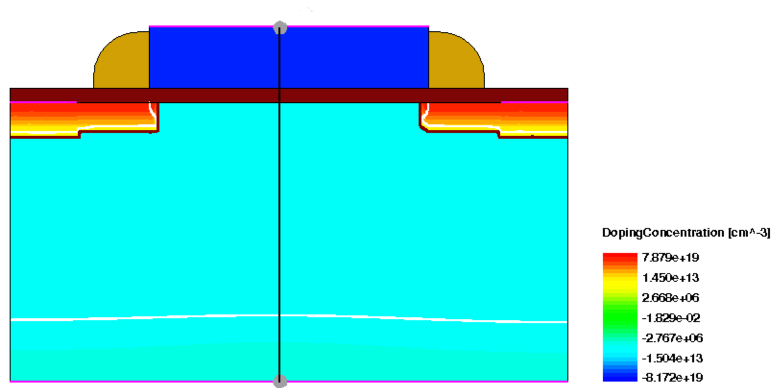

Figure 2.3: The x-cut line of doping and meshing schematic cross section of the 4H-SiC MOSFET.

Table 2.2: Doping profiles of the 4H-SiC MOSFET

Region	Doping level	Impurity
p-substrate	$4.9\text{x}10^{15}\text{cm}^{-3}$	Boron
n^+ channel	$1\text{x}10^{20}\text{cm}^{-3}$	Arsenic
p^+ gate electrode	$1\text{x}10^{20}\text{cm}^{-3}$	Boron

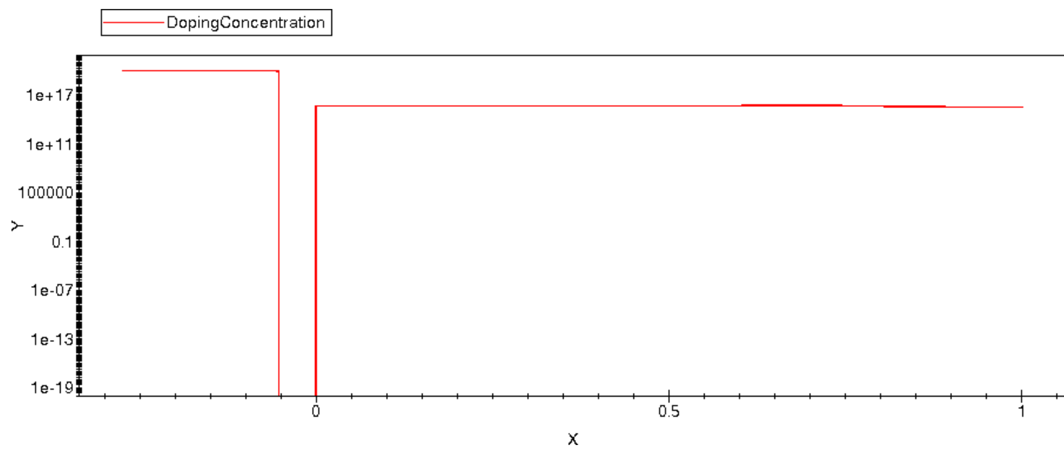

Figure 2.4: Doping concentration along X-cut of the 4H-SiC MOSFET.

Table 2.3: Basic parameter files of the 4H-SiC MOSFET

epsilon	9.66
electron affinity	3.65 eV

Chapter 3

Device Simulation

In this chapter, some important model methodologies used in this 4H-SiC MOSFET simulation will be presented. Some of the important physical model selections during simulation will also be introduced in this chapter. Moreover, later in the chapter will introduce trap specification and strategies used to evaluate the occupied interface trapped charge and the fixed oxide charge density at the SiC/SiO_2 interface.

3.1 Drift Diffusion Model Equations

The drift diffusion models are the basic building blocks for semiconductor device modeling. The drift diffusion equations consist of the Poisson's equation, the electron and hole current equations, and the current continuity equations for electrons and holes. These equations are derived from the Boltzmann transport equation by doing certain approximations. In this section, we describe these equations in brief.

Poisson Equation: The Poisson equation governs the behavior of the electrostatics in the semiconductor device. It relates the electrostatic potential, ϕ, the electron and hole concentration, n and p, respectively, to the net charge density inside the semiconductor. The Poisson equation can be written as [2]:

$$\epsilon \nabla^2 \phi = -q(p - n + N_D^+ - N_A^-) - \rho_{trap} \tag{3.1}$$

where:

- ϵ is the electrical permittivity.

- n and p are the electron and hole densities.
- q is the elementary electronic charge.
- N_D is the concentration of ionized donors.
- N_A is the concentration of ionized acceptors.
- ρ_{trap} is the charge density contributed by traps and fixed charges.

Current Equations: Current flowing inside a semiconductor is made up of two components. The diffusion component of current is due to the flow of electrons (or holes) from a region of higher concentration to a region of lower concentration. Thus, the diffusion current depends on the concentration gradient of electrons and holes. The drift component arises due to the flow of electrons (or holes) in presence of an electric field. The total electron (and hole) current is a combination of the diffusion and drift currents. From Boltzmann transport theory, $\vec{J_n}$ and $\vec{J_p}$ can be written as a function of ϕ, n, and p, consisting of drift and diffusion components, and is given as [2]:

$$\vec{J_n} = -qn\mu_n\vec{\nabla}\phi + qD_n\vec{\nabla}n \tag{3.2}$$

$$\vec{J_p} = -qp\mu_p\vec{\nabla}\phi - qD_p\vec{\nabla}p \tag{3.3}$$

where:

- μ_n is the electron mobility.
- μ_p is the hole mobility.
- D_n is the electron diffusion constant.
- D_p is the hole diffusion constant.

Current Continuity Equations: The continuity equations are based on the conservation of mobile charge. They relate the change in mobile charge concentration in time

to the gradient of the current density and the rates of generation and recombination of carriers. The continuity equations of electrons and holes are written as [2]:

$$\frac{\partial n}{\partial t} = \frac{1}{q}\vec{\nabla} \cdot J_n - U_n \tag{3.4}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\vec{\nabla} \cdot J_p - U_p \tag{3.5}$$

Here U_n and U_p represent net electron and hole recombination, respectively. $\vec{\nabla} \cdot J_n$ and $\vec{\nabla} \cdot J_p$ are the net flux of electrons and holes in and out of the specific volume. The current continuity equations state that the total current flow in or out of a volume of space is equal to the time varying charge density within that volume plus any additions due to generation or recombination that may occur.

3.2 Physical Model Selection

We solve the Drift Diffusion equations inside the device for the electrostatic potential, electron and hole concentration. In order to characterize the performance of a semiconductor device, we need to include the relevant physical mechanisms that govern transport in the device. The physical models selected in the simulation influence the accuracy of the result to a large extent. Therefore, to achieve higher accuracy of the simulation results, physical model selection is very important.

Generation and Recombination: Various mechanisms for generation and recombination are incorporated into device simulation. For SiC MOSFET simulations, two types of recombination mechanisms have been modeled. The first one we used is Shockley-Read-Hall (SRH) recombination which occurring due to trap centers. In addition, we include Auger recombination which occurring due to direct particle recombination.

Mobility Degradation at Interfaces: In the channel region of a MOSFET, carriers are subjected to scattering by acoustic surface phonons and surface roughness because the high transverse electric field forces carriers to interact strongly with the semiconductor insulator interface. This selected physical model describes mobility degradation caused by these effects. To activate mobility degradation at interfaces, we select the calculation of field perpendicular to the semiconductor-insulator interface; specify the Enormal option to Mobility [2].

Incomplete Ionization: In silicon, because the impurity levels are sufficiently shallow, most dopants can be considered to be fully ionized at room temperature, excluding indium. However, incomplete ionization must be considered when impurity levels are relatively deep compared to the thermal energy kT. This is the case for indium acceptors in silicon and nitrogen donors and aluminum acceptors in silicon carbide (SiC) [2]. For these situations, we need to include the incomplete ionization into physic models during device simulation in order to derive accurate simulation result.

3.3 Trap Specification

The effect of interface traps on the performance of SiC devices is the main interest and discussion of this work. Therefore, how we specify and define the traps during the device simulation is an important issue. Different trap types and different energetic-spatial distribution of traps defined in the device simulation are presented in this section.

3.3.1 Trap Types

Five trap types are defined [2]; they are FixedCharge, Acceptor, Donor, eNeutral, hNeutral, respectively:

• FixedCharge: traps are always completely occupied and distributed inside an insulator bulk material or at arbitrary material interfaces.

• Acceptor and eNeutral: traps are uncharged when unoccupied and they carry the charge of one electron when fully occupied.

• Donor and hNeutral: traps are uncharged when unoccupied and they carry the charge of one hole when fully occupied.

3.3.2 Trap Density-of-States (DOS) Energy Distribution

Different energetic-spatial distributions of traps defined in the device simulation are described as below [2]:

• Level represents a single energy trap level at a predefined EnergyMid position.

• Uniform represents a uniformly energy distributed trap inside a material band gap, controlled by the energy reference point, EnergyMid and EnergySig parameters.

• Exponential represents an exponentially energy distributed trap inside a material point, EnergyMid and EnergySig parameters.

• Gaussian represents an Gaussian energy distributed trap in a material band gap, controlled by the energy reference point, EnergyMid and EnergySig parameters.

• Table specifies a tabular trap energy distribution.

Equations below shows different distribution functions respectively. For a Level distribution, N0 is set as trap concentration which is given in cm^{-3} for bulk traps and cm^{-2} for interface traps. For the other energetic distributions, N0 is given in $\mathrm{eV}^{-1}\mathrm{cm}^{-3}$ for bulk traps and $\mathrm{eV}^{-1}\mathrm{cm}^{-2}$ for interface traps. Fig. 3.1 shows different trap DOS energy distributions for different trap DOS definitions [2].

$$\text{Level} : N_0, \text{ for } E = E_0 \tag{3.6}$$

$$\text{Uniform} : N_0, \text{ for } E_0 - 0.5E_s < E < E_0 + 0.5E_s \tag{3.7}$$

$$\text{Exponential} : N_0 exp(-\frac{E - E_0}{E_s}) \tag{3.8}$$

$$\text{Gaussian} : N_0 exp(\frac{(E - E_0)^2}{2(E_s)^2}) \tag{3.9}$$

$$\text{Table} : \begin{cases} N_1 & \text{for } E = E_1 \\ & ... \\ N_m & \text{for } E = E_m \end{cases} \tag{3.10}$$

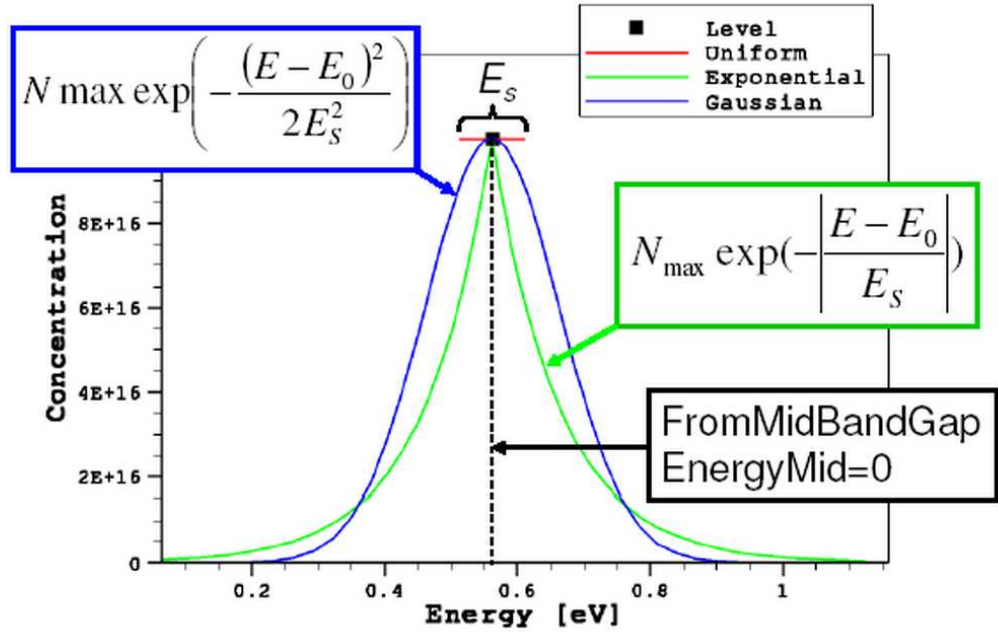

Figure 3.1: Trap DOS energy distributions for different trap DOS definitions [2].

3.4 4H-SiC MOSFET Model Parameters

In this section, the methodology of temperature depedent parameters fitting the measurement data [17][1] will be introduced and the fitting results will be presented in next

chapter. First of all, the interface trapped charge Q_{it}, as a function of surface Fermi level E_F can be approximated as [17]: where D_{it}(E) is the interface state density profile as a function of trap energy. With respect to trap energy from the conduction band edge (E_c), it is assumed to be as the following form [17]:

$$Q_{it}(E_F) = -\int_{E_1}^{E_F} D_{it} dE \tag{3.11}$$

$$D_{it}(E_c - E) = D_{it}^0 + D_{it}^1 e^{-E_c - E / \sigma}, \text{for } 0 < E_c - E < E_c/2 \tag{3.12}$$

$$D_{it}(E_c - E) = 0, \text{for } E_c - E < 0 \tag{3.13}$$

The term D_{it}^0 is a constant uniform distribution representative of D_{it} in the mid-bandgap region. The term D_{it}^1 represents a D_{it} profile decreasing exponentially from the conduction band edge. N_f is the positive fixed oxide charge which is typically located in SiO_2/4H-SiC interface. σ is a parameter in eV that dictates the sharpness of the profile. The parameters D_{it}^0, D_{it}^1, N_f, σ, and also EnergyMid and EnergySid which we mentioned in 3.3 section, are that we used for data fitting. The fitting method might not be unique while we use a better way for data fitting after numerous trials and errors. First of all, we only adjust the parameter N_f. By only changing the parameter N_f, we can shift the curve horizontally without involving the variations of the curve slope. This enables us to fit the threshold voltage in the very beginning step. Second of all, by adjusting the parameters D_{it}^1 and D_{it}^0, we can fit the slope of curves. σ, EnergyMid and EnergySid are the last step for subtle adjustment if necessary. Table 3.1 shows the parameters used for data fitting.

Table 3.1: Temperature dependent parameters used for fitting measurement data

Model fitting parameter	Trap type specification
$D_{it}^0(cm^{-2}eV^{-1})$	Uniform/ from mid bandgap
$D_{it}^1(cm^{-2}eV^{-1})$	Exponential/ from conduction band edge
$\sigma(eV)$	Dictates the sharpness of D_{it}^1
$N_f(cm^{-2})$	Fixed oxide charge
EnergyMid / EnergySid	E_s and E_0 introduced in Table 3.1

Chapter 4
Simulation Results and Interpretations

In this chapter, we will present and interpret various simulation results. First of all, we start with interpreting the results at room temperature. Free carrier concentration N_{inv} as a function of gate voltage (V_g) plot that fit the experimentally measured values [17][1] is presented in two different oxide thickness scales. In addition, the interface charge density as a function of gate voltage (V_g) plot with two different oxide thickness scales is also presented for detail interpretation. Moreover, the interface trap occupation and trap density as a function of energy plot is also presented for discussion. For temperature dependent and bias dependent analysis, we will have simulation results and plots presented in the later part of this chapter. By interpret the simulation result plots, we can see the role played by interface traps at the SiC/SiO_2 interface in 4H-SiC with different temperatures and different biases.

4.1 Simulation Methodology

As we mentioned in section 3.4, employing temperature dependent parameters allows us to fit the temperature dependence of N_{invs}. In this section, we will have comparisons of changing only one temperature dependent parameter at a time, in order to show how these temperature dependent parameters involve the variation of trap distribution and inversion layer carrier concentrtion. The results of employing different fixed oxide charge (N_f), (D_{it}), and σ are presented in this section, respectively.

Fig. 4.1 shows the simulation result of N_{inv} as a function of gate voltage with different fixed oxide charge (N_f). We can see from the plot that by only changing parameter fixed

oxide charge (N_f), we have the N_{inv} curve shift horizontally without changing the slope of the curve. In addition, the threshold voltage V_{th} decreases with increasing N_f. This is the first step for us to fit the threshold voltage V_{th}.

Fig. 4.2 shows the simulation result of N_{inv} as a function of gate voltage with different D_{it} profiles. We can see from the plot that the V_{th} of the N_{inv} curves is all the same when we only change different D_{it} profiles. The only difference of the simulation result is the slope of the curves. With increasing the D_{it} profiles, we will have decreasing slope of N_{inv} curves. This is the second step for us to fit the N_{inv} curves.

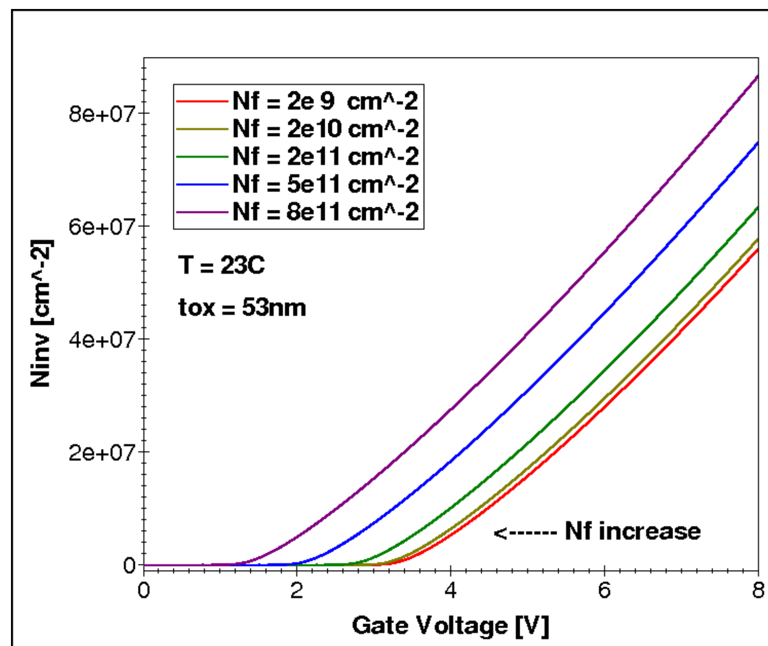

Figure 4.1: N_{inv} as a function of gate voltage with different N_f.

Fig. 4.3 shows the variation of N_{inv} curves while the σ changing is involved. It will change not only the slope of curve but also the curve will shift horizontally. In addition, we can see from Fig. 4.4 which show the trap density as a function of energy with different σ when gate bias is applied at 21V. Changing σ will also considered as one of the simulation methodologies while there is large difference that need to be fitted.

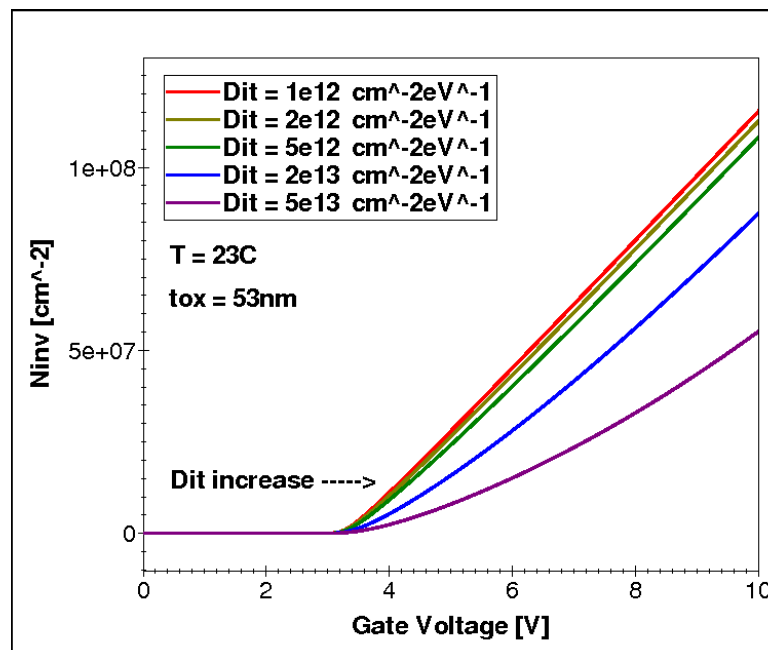

Figure 4.2: N_{inv} as a function of gate voltage with different D_{it} profiles.

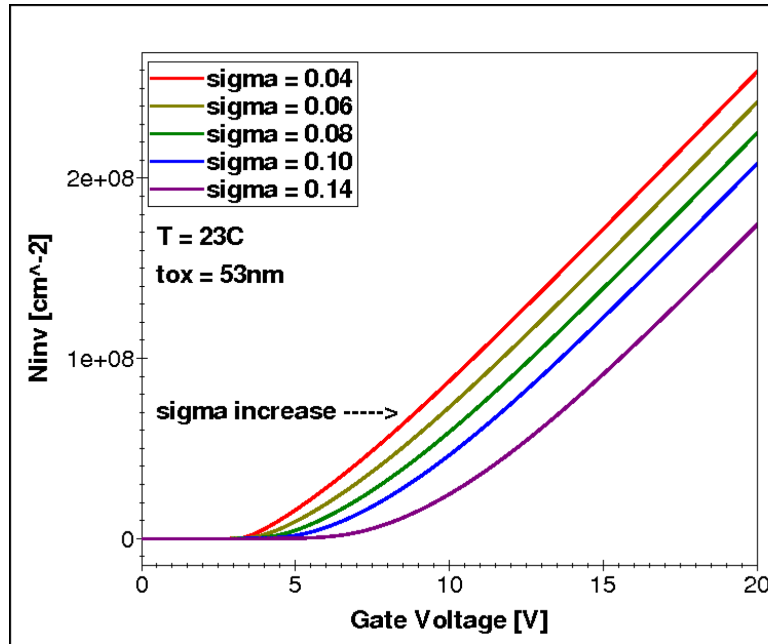

Figure 4.3: N_{inv} as a function of gate voltage with different σ.

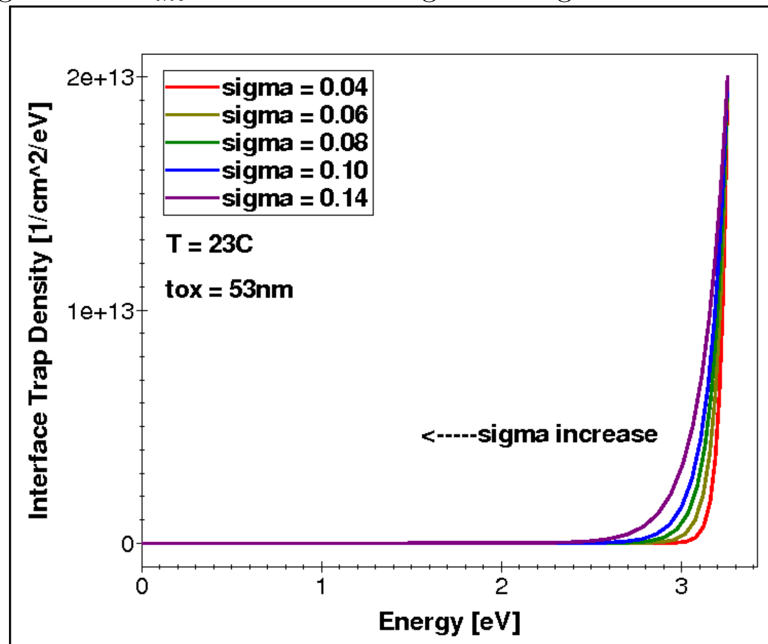

Figure 4.4: Interface trap density as a function of energy with different σ. (Vg=21V)

4.2 Simulation Results at Room Temperature

Fig. 4.5 and Fig. 4.6 show the free carrier concentration as a function of gate voltage with two different oxide thickness device structures at room temperature. They are 53 nm and 125 nm respectively. From Fig. 4.5 and Fig. 4.6 we can see due to the thicker gate oxide ($2.5X$), the slope of 125 nm oxide thickness device structure is around 25% lower than ideal charge sheet model's (CSM) slope [19] within the simulated gate bias range, while for 53 nm oxide thickness structure, the slope of the N_{inv} versus V_g curve is within 5% of the ideal model's slope in the simulated gate voltage range.

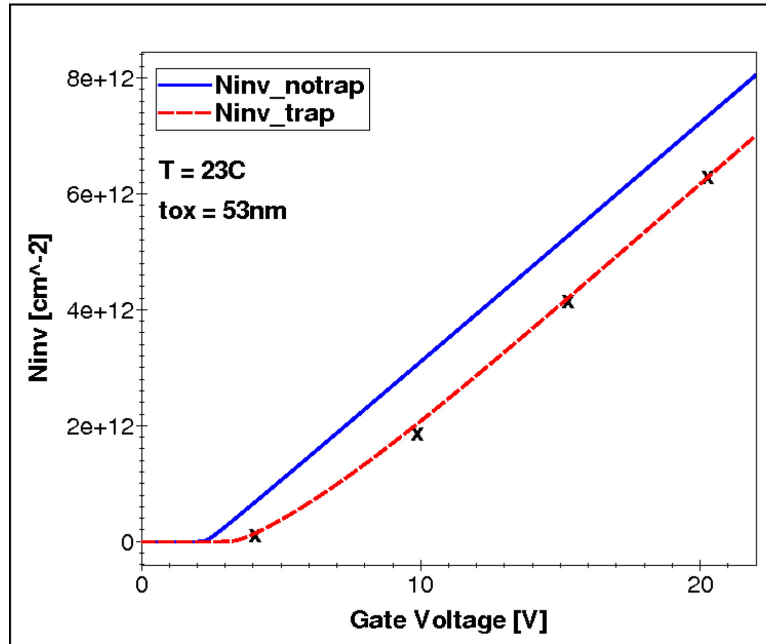

Figure 4.5: Free carrier concentration as a function of gate voltage for 53 nm oxide thickness.

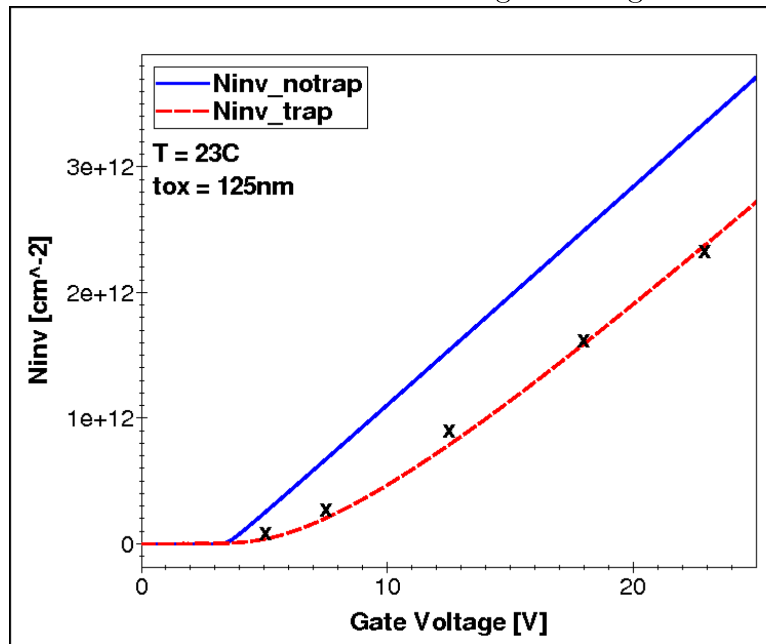

Figure 4.6: Free carrier concentration as a function of gate voltage for 125 nm oxide thickness.

Fig. 4.7 and Fig. 4.8 show interface trapped charge density as a function of gate voltage with two different oxide thickness device structures at room temperature. Two different oxide thicknesses are 53 nm and 125 nm, respectively. The solid line represents 53 nm and the dot line represents 125 nm. Fig. 4.7 is in linear scale and Fig. 4.8 is in log scale which can be seen more clearly with saturation of trapping. We can see from Fig. 4.7 and Fig. 4.8, the total number of traps in 125 nm structure is about 20% higher than 53 nm structure. Moreover, the gate voltage where the saturation of trapping occurred is different for the two structures. For 53 nm oxide thickness structure, saturation of trapping occurs around V_g=10V. For 125 nm oxide thickness structure, saturation of trapping occurs around V_g=20V. The difference of gate oxide thickness has a greater impact than the difference of D_{it} profile for the two structures [17].

Fig. 4.9 and Fig. 4.10 show the interface trapped density and occupation probability as a function of energy at room temperature with 21 V gate bias in 53 nm oxide thickness structure. We combine all different D_{it} profiles into one to show trap density and occupation probability as single curves, respectively.

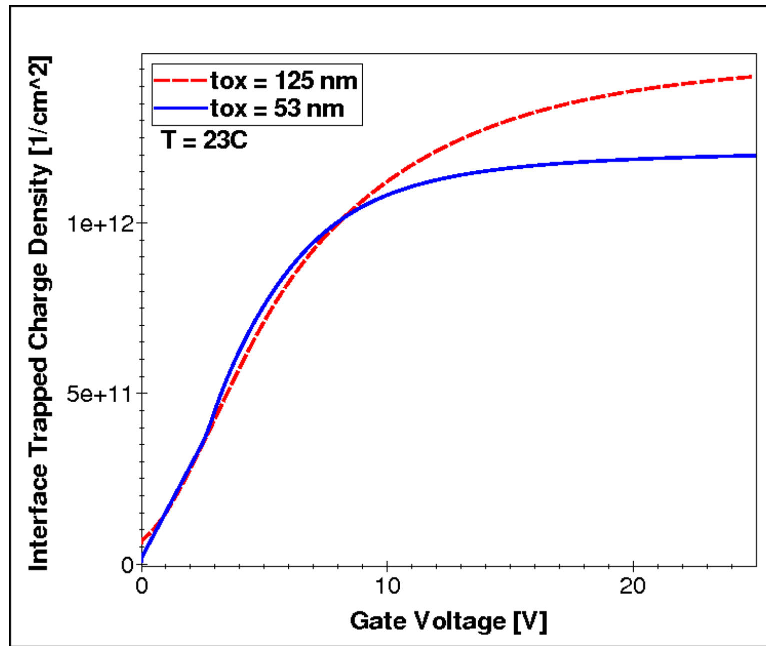

Figure 4.7: Interface trapped charge density as a function of gate voltage (linear scale).

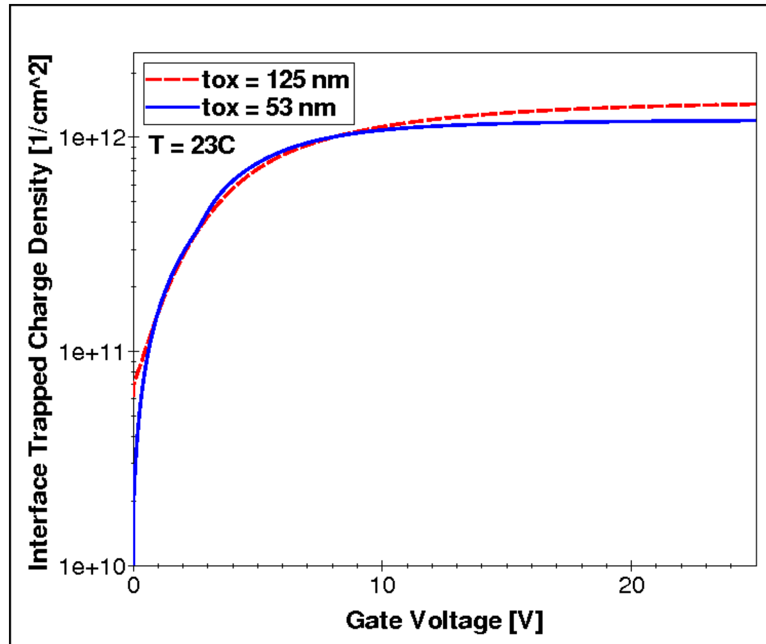

Figure 4.8: Interface trapped charge density as a function of gate voltage (log scale).

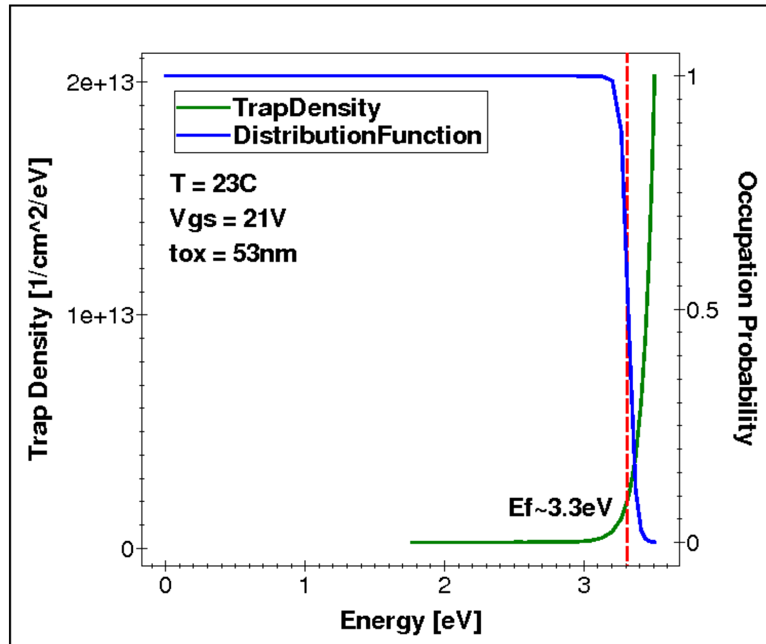

Figure 4.9: Interface trapped density and occupation probability as a function of energy at room temperature with 21V gate bias (linear scale).

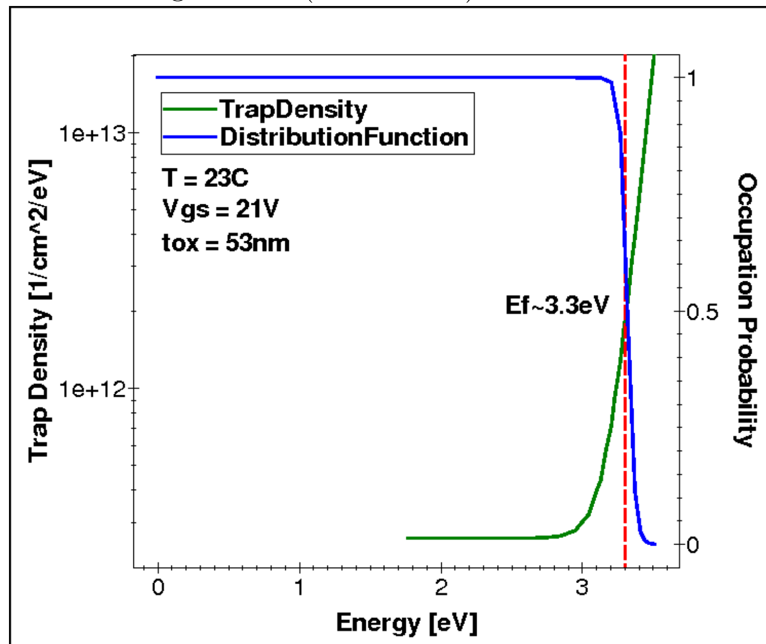

Figure 4.10: Interface trapped density and occupation probability as a function of energy at room temperature with 21V gate bias (log scale).

4.3 Temperature and Bias Dependent Model Simulation Results

In this section we will have inversion layer carrier concentration as a function of gate voltage simulation under different temperatures. In addition, we also simulate trap density distribution and trap charge density as a function of energy with different temperatures. Moreover, bias dependent trap occupation as a function of energy will be presented for observation. These are simulated under the 53 nm oxide thickness structure.

Fig. 4.11 shows inversion layer carrier concentration as a function of gate voltage at different temperatures without traps. We can see from Fig. 4.11, the inversion layer carrier concentration increases when we increase temperature; however, the increase is very small because there are no any D_{it} profiles involved in the simulation.

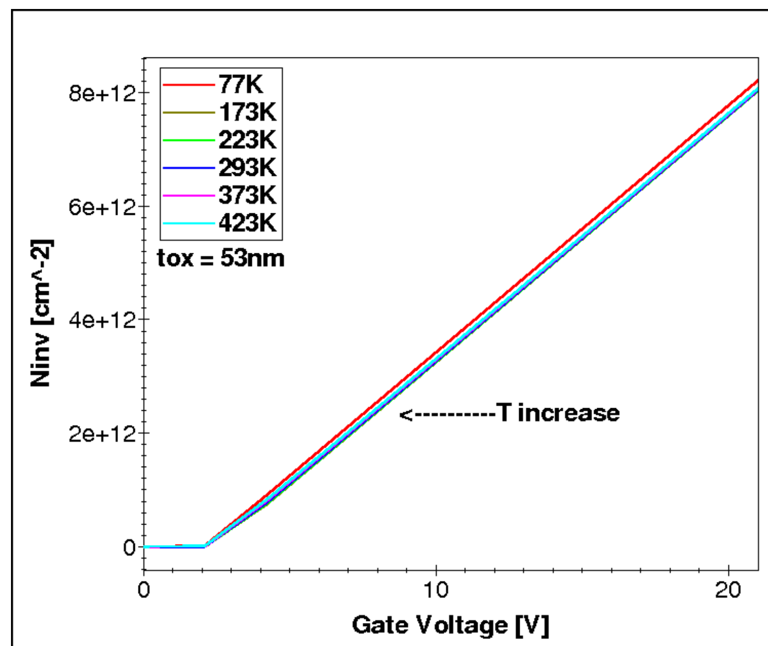

Figure 4.11: Inversion layer carrier concentration as a function of gate voltage in different temperatures without traps.

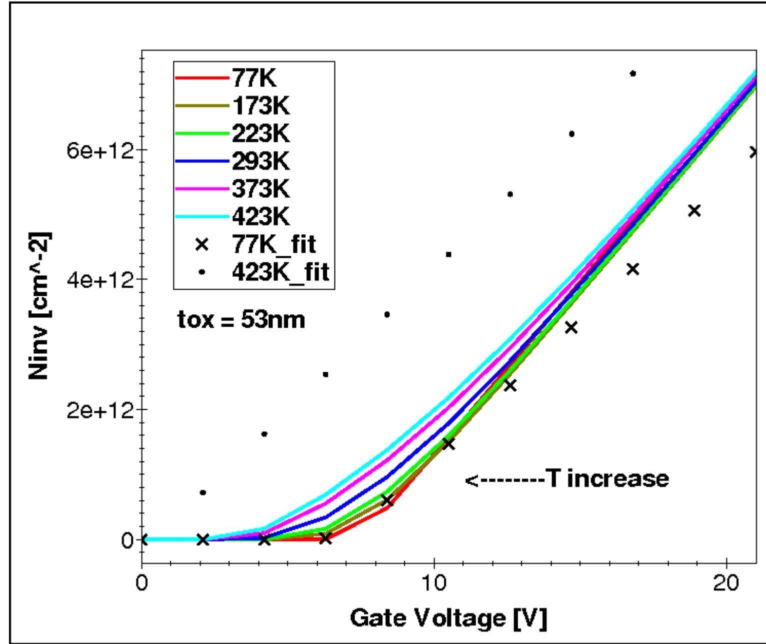

Figure 4.12: Inversion layer carrier concentration as a function of gate voltage in different temperatures with same D_{it} profile and same fixed oxide charge.

Fig. 4.12 shows the inversion layer carrier concentration as a function of gate voltage at different temperatures with traps. We have the same D_{it} profile and same fixed oxide charge with all different temperature simulation models. It still couldn't fit the CSM (Charge-sheet model) [19] curve because it is modeled without temperature dependent D_{it} profile. The dot line is the curve for 423K and the cross line is for 173K which are supposed to be fitted and we can see the discrepancy becomes larger with higher temperatures.

Fig. 4.13 shows the inversion layer carrier concentration as a function of gate voltage simulated with temperature dependent D_{it} profiles. By employing temperature dependent parameters, the curves fit the CSM data reasonably. The dot and cross lines are the data [19] we tried to fit. We can see the threshold voltage (V_{th}) increases with decreasing temperatures. Based on [1], we adjust temperature dependent parameters with larger D_{it} value when temperature decreases. At lower temperatures, higher interfacial trapped charge

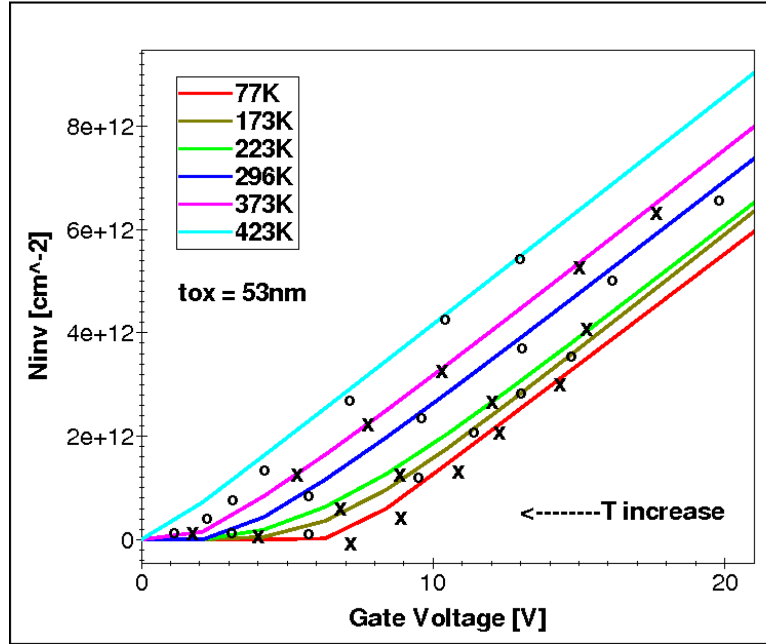

Figure 4.13: Inversion layer carrier concentration as a function of gate voltage in different temperatures simulated with temperature dependent parameters.

is observed [1]. This causes the curves to shift to the right and increases the threshold voltage (V_{th}).

Fig. 4.14 shows the interface trapped charge density as a function of V_g in different temperatures. As we discussed in Fig. 4.5 and Fig. 4.6, which is simulated only in room temperature, trapping saturation reached at different V_g for two different oxide thickness scales. The reason is mainly due to difference in oxide thickness instead of different D_{it} profiles. In Fig. 4.14, we simulate different temperatures in the same 53 nm oxide thickness structure and we can see the difference of trapping saturation V_g is not that much as Fig. 4.5 and Fig. 4.6. In addition, the trapped charge density increases rapidly when V_g is smaller than 10V while the temperature is lower as 173K and 223K.

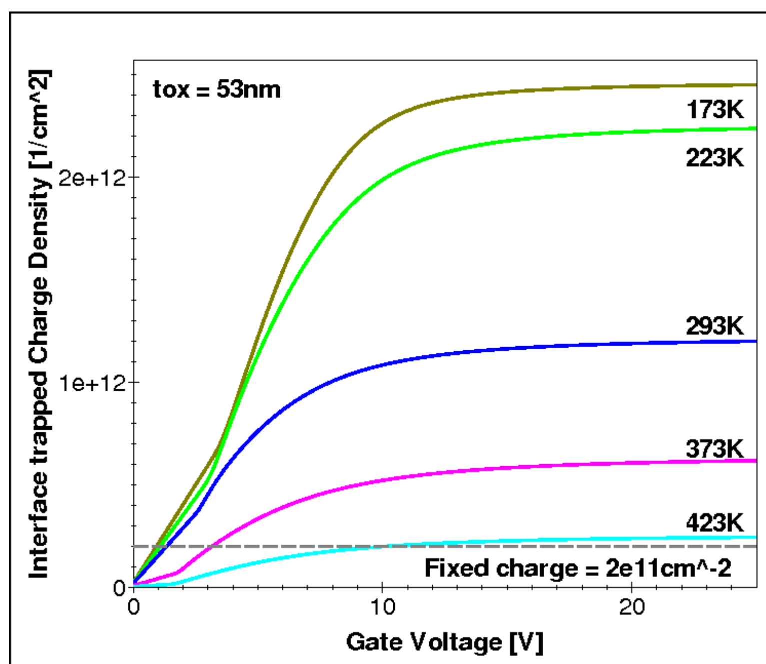

Figure 4.14: Interface trapped charge density as a function of V_g in different temperatures.

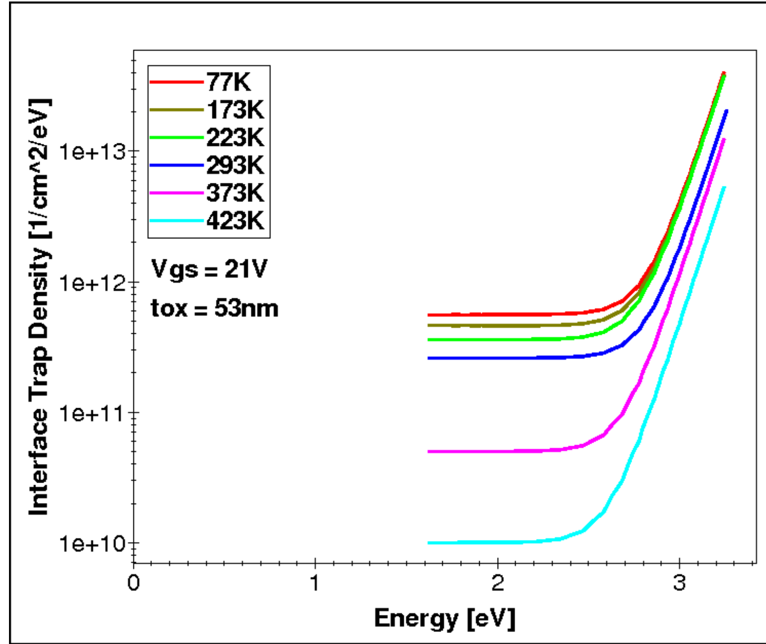

Figure 4.15: Trap density as a function of energy in different temperatures.

Fig. 4.15 shows trap density as a function of energy in different temperatures. It is simulated in the 53nm oxide thickness structure with 21V gate bias. For each temperature in this figure, we combine all the D_{it} profiles into one trap density in order to show one curve as one temperature. Once we have the trap density distribution curves for different temperature, we can simulate their occupation probability and see how they distribute in different temperatures which are shown in Fig. 4.16 and Fig. 4.17.

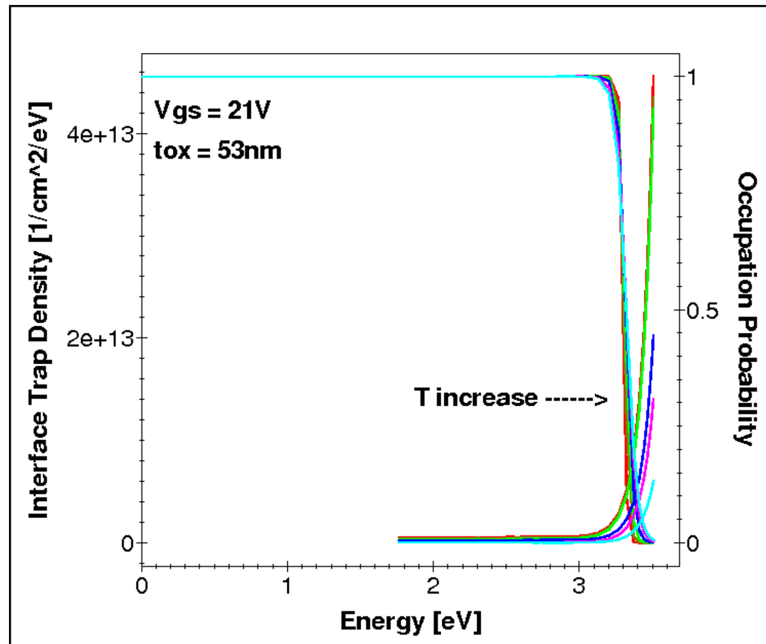

Figure 4.16: Trap density and occupation probability as a function of energy (linear scale).

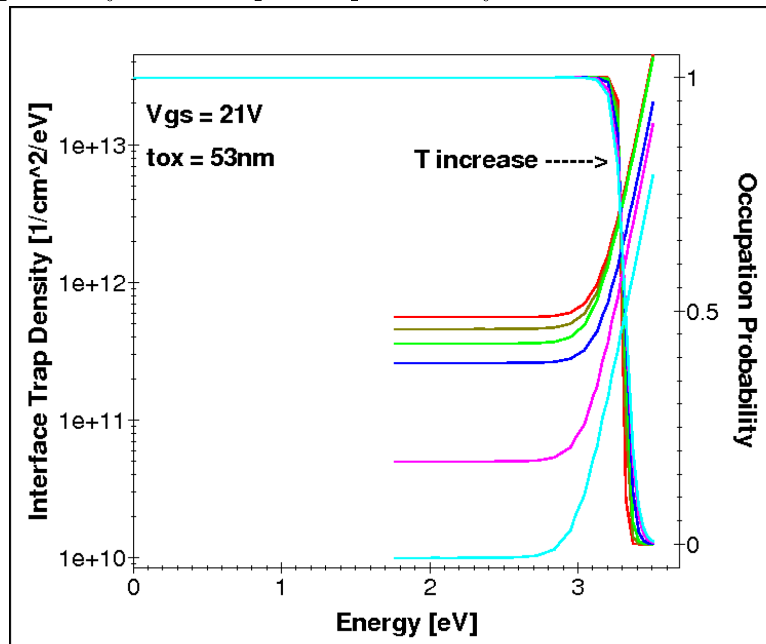

Figure 4.17: Trap density and occupation probability as a function of energy (log scale).

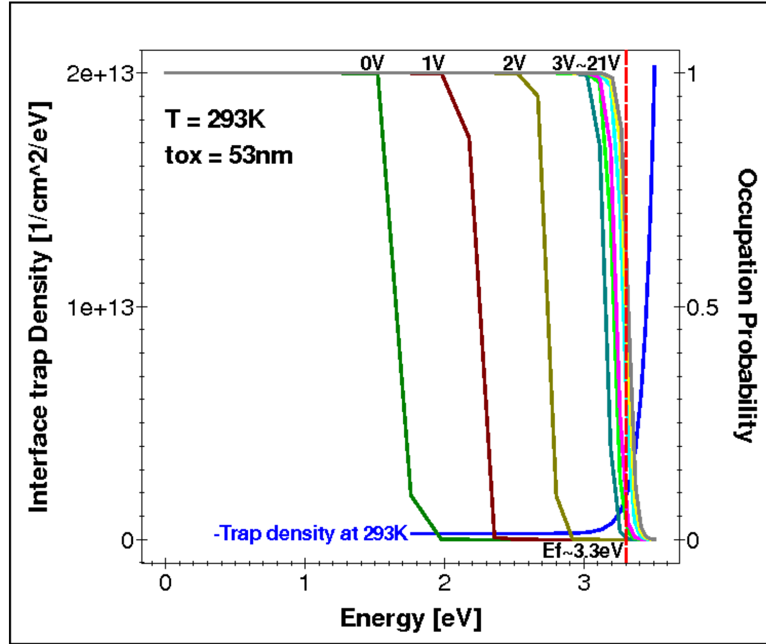

Figure 4.18: Trap density and occupation probability as a function of energy with different gate bias at room temperature.

Fig. 4.18 shows trap density and occupation probability as a function of energy with different gate bias. From the figure we can see the trap occupation move toward the conduction band edge rapidly while the gate bias increases from 0V to 3V. As gate bias increase over 3V, there is not much shift for trap occupation probability, especially when gate bias is over 7V. The occupation probability of traps are almost overlaid when gate bias is applied during 10V∼21V.

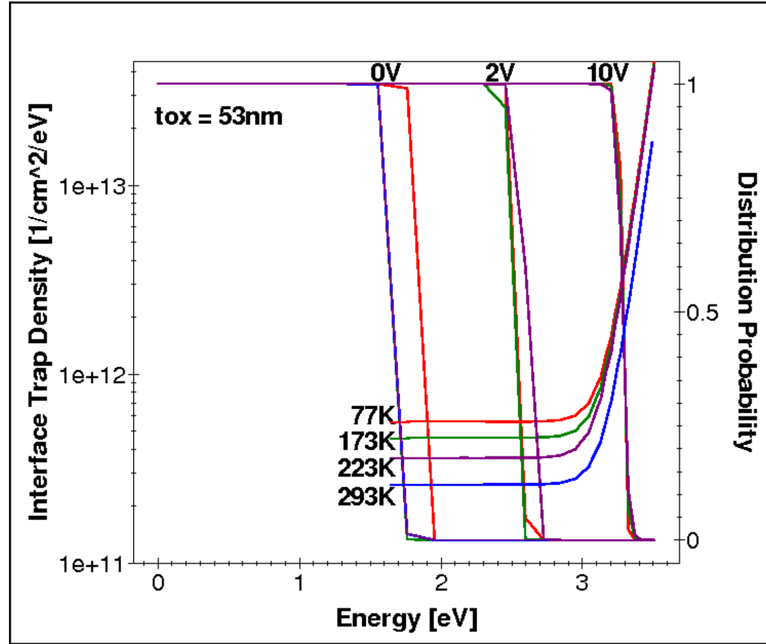

Figure 4.19: Trap density and occupation probability as a function of energy with different bias and different temperatures.

Fig. 4.19 shows trap density and occupation probability as a function of energy with different bias and different temperatures. Each color of line represents different temperatures. We can see from the figure that when gate bias is applied at 10V, the curve of occupation probability are all almost overlaid. That's the reason we don't plot out the curves of occupation probability with gate bias applied over 10V.

Chapter 5
Conclusion

We have presented simulations of 2D 4H-SiC MOSFET structures with two different oxide thicknesses, with temperature dependent interface trap parameters, we are able to fit measured inversion layer carrier concentrations as a function of gate bias at different temperatures. The variation of interface trap occupation probability with temperatures and biases are examined using simulation details.

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Appendices

APPENDIX A

2D Device Simulation Command File

```
File {
   *input files:
   Grid=    "mosfet_msh.tdr"
   Parameter="sdevice.par"
   *output files:
   Plot=   "traps_des.tdr"
   Current="traps_des.plt"
   Output= "traps_des.log"
   TrappedCarPlotFile = "itraps_trappedcar"
}

TrappedCarDistrPlot {
   MaterialInterface = "SiliconCarbide/Oxide" {
     (1 1e-8)
   }
}

Electrode {
   { Name="source"    Voltage= 0.0 }
```

```
  { Name="drain"    Voltage= 0.1 }
  { Name="gate"     Voltage= 0.0 }
  { Name="base"     Voltage= 0.0 }
}

Math{-CheckUndefinedModels}

Physics{
   Temperature=293
   Fermi
   Recombination(
      SRH(DopingDependence)
      Auger
      Avalanche(OkutoCrowell)
   )
   Aniso(
     Mobility
     Avalanche
   )
  Mobility(
      DopingDependence
      HighFieldSaturation
      Enormal(Lombardi)
```

```
      IncompleteIonization
    )
   UseNitrogenAsDopant
   IncompleteIonization
   EffectiveIntrinsicDensity(OldSlotboom)

}

Plot {
   eDensity hDensity eCurrent hCurrent
   Potential SpaceCharge ElectricField
   eMobility hMobility eVelocity hVelocity
   Doping DonorConcentration AcceptorConcentration
   eQuasiFermi hQuasiFermi
   eTrappedCharge hTrappedCharge
   eInterfaceTrappedCharge hInterfaceTrappedCharge
   TotalInterfaceTrapConcentration
   EffectiveBandGap
   ConductionBandEnergy
   ValenceBandEnergy
 }

CurrentPlot {
```

```
  eDensity(
    Integrate(Window[(0.8 0) (1.2 0.2)])
  )
  eMobility((1 1e-8))
  ElectricField/Vector((1 1e-8))
  evelocity((1 1e-8))
  ElectrostaticPotential((1 1e-8))
  eDensity((1 1e-8))
  eInterfaceTrappedCharge((1 1e-8))
  eTrappedCharge((1 1e-8))
}
```

```
*-----------------------------------------------------------
*Specifying interface fixed charge and traps

Physics(MaterialInterface = "SiliconCarbide/Oxide" ){

  Traps(
     (FixedCharge Conc=2.0e+11)
     (eNeutral     Uniform     fromMidBandGap     Conc=2.6e11
```

```
EnergyMid=0.807        EnergySig=1.615        eXsection=1e-14
hXsection=1e-14)
      (eNeutral Exponential fromCondBand Conc=2e13  EnergyMid=0
EnergySig=0.04 eXsection=1e-14     hXsection=1e-14)
       )
     }
*-------------------------------------------------------------
Math {
   Extrapolate
   RelErrControl
   CurrentPlot (IntegrationUnit = cm)
   ExitOnFailure
   TrapDLN=30
}
Solve {
*-initail solution
     Poisson
     Coupled { Poisson Electron Hole }


*-ramp gate
     Quasistationary(
      DoZero
```

```
    InitialStep= 1e-3 Increment= 1.5
    MinStep= 1e-5 MaxStep= 0.01
    Goal { Name="gate" Voltage=25}
  )
  { Coupled { Poisson  Electron  Hole }
  CurentPlot (Time = (Range=(0 1) Intervals= 20) noOverwrite) }

}
```

4H-SiC Device Simulation Parameter File

```
Material="SiliconCarbide"{
*************** Bandgap / Bandgap Narrowing / Intrinsic Density:
**************
* nieff = ni exp( deltaEg/(2 kT) ), ni = (Nc(T) Nv(T))^(1/2)
exp( -Eg/(2kT) ) *
***************************************************************
*****************
Epsilon
{ *  Ratio of the permittivities of material and vacuum

  * epsilon() = epsilon
    epsilon   = 9.66 # [1]
}


Epsilon_aniso
{ *  Ratio of the permittivities of material and vacuum

  * epsilon() = epsilon
    epsilon   = 9.66 # [1]
}




Bandgap *temperature dependent*
{ * Eg = Eg0 - alpha T^2 / (beta + T)
    alpha  = 3.206000e-02   # [eV K^-1]
    beta   = 1.0e+05 # [K]
    Eg0 = 3.285        # [eV]
```

```
    * Chi0 is electron affinity.
      Chi0   = 3.65 # [eV]
}

OldSlotboom
{ * deltaEg = Ebgn ( ln(N/Nref) + [ (ln(N/Nref))^2 + 0.5]^1/2 )
   Ebgn   = 9.0000e-03  # [eV]
   Nref   = 1.0000e+17  # [cm^-3]
}

**** Effective Densities of States: ****
*   Nc(T) = 2.540e19 ( me(T) T )^3/2   *
*   Nv(T) = 2.540e19 ( mh(T) T )^3/2   *
**** Density of State Masses: ****
eDOSMass
{
  * For effective mass specificatition Formula1 (me approximation):
  * or Formula2 (Nc300) can be used :
    Formula   = 1 # [1]
  * Formula1:
  * me/m0 = [ (6 * mt)^2 *  ml ]^(1/3) + mm
  * mt = a[Eg(0)/Eg(T)]
  * Nc(T) = 2(2pi*kB/h_Planck^2*me*T)^3/2 = 2.540e19
((me/m0)*(T/300))^3/2
   a   = 0.0625   # [1]
   ml  = 1.5  # [1]
   mm  = 0.0000e+00  # [1]
  * Formula2:
  * me/m0 = (Nc300/2.540e19)^2/3
  * Nc(T) = Nc300 * (T/300)^3/2
   Nc300  = 2.8900e+19  # [cm-3]
}

hDOSMass
```

```
{
  * For effective mass specificatition Formula1 (mh approximation):
  * or Formula2 (Nv300) can be used :
    Formula    = 1 # [1]
  * Formula1:
  * mh =  m0*{[(a+bT+cT^2+dT^3+eT^4)/(1+fT+gT^2+hT^3+iT^4)]^(2/3)
+ mm}
  * Nv(T) = 2(2pi*kB/h_Planck^2*mh*T)^3/2 = 2.540e19
((mh/m0)*(T/300))^3/2
    a   = 1 # [1]
    b   = 0 # [K^-1]
    c   = 0 # [K^-2]
    d   = 0 # [K^-3]
    e   = 0 # [K^-4]
    f   = 0 # [K^-1]
    g   = 0 # [K^-2]
    h   = 0 # [K^-3]
    i   = 0 # [K^-4]
    mm  = 0 # [1]
  * Formula2:
  * mh/m0 = (Nv300/2.540e19)^2/3
  * Nv(T) = Nv300 * (T/300)^3/2
    Nv300  = 3.1400e+19  # [cm-3]
}

*****************************  Thermal conductivity of Silicon
Carbide *******************************

Kappa
{ *  Lattice thermal conductivity

  * Formula = 0:
  * kappa() = 1 / ( 1/kappa + 1/kappa_b * T + 1/kappa_c * T^2 )
    1/kappa    = -0.0327 # [K cm/W]
```

```
   1/kappa_b = 5.5580e-04  # [cm/W]
   1/kappa_c = 7.7560e-07  # [cm/(W K)]
}


Kappa_aniso
{ *  Lattice thermal conductivity

  * Formula = 0:
  * kappa() = 1 / ( 1/kappa + 1/kappa_b * T + 1/kappa_c * T^2 )
   1/kappa   = -0.0327 # [K cm/W]
   1/kappa_b = 5.5580e-04  # [cm/W]
   1/kappa_c = 7.7560e-07  # [cm/(W K)]
}


*****************************  Mobility Models:
*******************************
* mu_lowfield^(-1) = mu_dop(mu_max)^(-1) + mu_Enorm^(-1) +
mu_cc^(-1)          *
* Variable = electron value ,   hole value     # [units]
*
**************************************************************
*****************
ConstantMobility:
{ * mu_const = mumax (T/T0)^(-Exponent)
* [Linewih and Dimitrijev]
    mumax = 950 ,    124 # [cm^2/(Vs)] [Cree] E perp c
   Exponent  = 2 ,  2   # [Cree]
}
ConstantMobility_aniso:
{ * mu_const = mumax (T/T0)^(-Exponent)
   mumax  = 700 ,    114 # [cm^2/(Vs)] [Cree] E || c - 4H-SiC
   Exponent  = 2 ,  2   # [Cree]
```

```
}

DopingDependence:
{
  * For doping dependent mobility model three formulas
  * can be used.

  * If formula=1, model suggested by Masetti et al. is used:
  * mu_dop = mumin1 exp(-Pc/N) + (mu_const -
mumin2)/(1+(N/Cr)^alpha)
  *                        - mu1/(1+(Cs/N)^beta)
  * with mu_const from ConstantMobility
* [Linewih and Dimitrijev]

   formula   = 1 ,  1   # [1]

      mumin1  = 40. ,        15.9          # [cm^2/Vs] [Cree]
      mumin2  = 40 ,       0.0000e+00     # [cm^2/Vs]
      mu1     = 0.00 ,       0.00          # [cm^2/Vs]
      Pc      = 0.0000e+00 ,  0.00          # [cm^3]
      Cr      = 2e+17 ,    1.76e+19       # [cm^3] [Cree]
      Cs      = 3.4300e+20 ,  6.1000e+20     # [cm^3]
      alpha    = 0.76 ,       0.34    # [Cree]
      beta    = 2 ,          2      # [1]

}

DopingDependence_aniso:
{
  * For doping dependent mobility model three formulas can be used.
  * Formula1 is based on Masetti et al. approximation.
  * Formula2 uses approximation, suggested by Arora.

  * If formula=1, model suggested by Masetti et al. is used:
```

```
  * mu_dop = mumin1 exp(-Pc/N) + (mu_const -
mumin2)/(1+(N/Cr)^alpha)
  *                         - mu1/(1+(Cs/N)^beta)
  * with mu_const from ConstantMobility

    formula   = 1 ,  1   # [1]

       mumin1  = 40. ,        15.9          # [cm^2/Vs] [Cree]
       mumin2  = 40 ,       0.0000e+00     # [cm^2/Vs]
       mu1     = 0.00 ,       0.00          # [cm^2/Vs]
       Pc      = 0.0000e+00 ,  0.00          # [cm^3]
       Cr      = 2e+17 ,    1.76e+19       # [cm^3] [Cree]
       Cs      = 3.4300e+20 ,  6.1000e+20     # [cm^3]
       alpha   = 0.76 ,       0.34    # [Cree]
       beta    = 2 ,          2      # [1]


}
HighFieldDependence:
{ * mu_highfield = mu_lowfield / ( 1 + (mu_lowfield E /
vsat)^beta )^1/beta
  * beta = beta0 (T/T0)^betaexp; vsat = vsat0 (T/T0)^(-Vsatexp);
   beta0  = 1.00 ,  1.213  # [R.M.]
   betaexp   = 0.66 ,  0.17   # [1]
   vsat0  = 2.10e+07 , 3e+7    # [1]  E perp c
   vsatexp   = 0.87 ,  0.52   # [1]
}

HighFieldDependence_aniso:
{ * mu_highfield = mu_lowfield / ( 1 + (mu_lowfield E /
vsat)^beta )^1/beta
  * beta = beta0 (T/T0)^betaexp; vsat = vsat0 (T/T0)^(-Vsatexp);
   beta0  = 1.00 ,  1.213  # [R.M.]
   betaexp   = 0.66 ,  0.17   # [1]
```

```
   vsat0  = 2.10e+07 ,  3e+7    # [R.M.] E || c
   vsatexp   = 0.87 ,  0.52   # [1]
}

EnormalDependence {

* electron parameters matched [Linewih and Dimitrijev]. This paper
only has data for SiO2/SiC interface on 1120
* hole parameters are Silicon defaults

       B       = 1e6 ,  9.9250e+06     # [cm/s]
       C       = 5.8000e+02 ,  2.9470e+03     #
[cm^(5/3)/(V^(2/3)s)] *1.74e5/300
       N0      = 1 ,  1      # [cm^(-3)]
       lambda  = 0.042828 ,      0.0317  # [1]
       k       = 1 ,  1      # [1]
       delta   = 5.82e+14 ,  2.0546e+14     # [V/s]
       A       = 2 ,  2      # [1]
       alpha   = 0.0000e+00 ,  0.0000e+00     # [1]
       aother  = 0.0000e+00 ,  0.0000e+00     # [1]
       N1      = 1 ,  1      # [cm^(-3)]
       nu      = 1 ,  1      # [1]
       eta     = 5.8200e+30 ,  2.0546e+30     # [V^2/cm*s]
       l_crit  = 1.0000e-06 ,  1.0000e-06     # [cm]
}


EnormalDependence_aniso{
* electron parameters matched [Linewih and Dimitrijev]. This paper
only has data for SiO2/SiC interface on 1120
* hole parameters are Silicon defaults

       B       = 1e6 ,  9.9250e+06     # [cm/s]
       C       = 5.8000e+02 ,  2.9470e+03     #
```

```
[cm^(5/3)/(V^(2/3)s)] *1.74e5/300
       N0      = 1 ,   1       # [cm^(-3)]
       lambda  = 0.042828 ,       0.0317  # [1]
       k       = 1 ,   1       # [1]
       delta   = 5.82e+14 ,  2.0546e+14      # [V/s]
       A       = 2 ,   2       # [1]
       alpha   = 0.0000e+00 ,  0.0000e+00      # [1]
       aother  = 0.0000e+00 ,  0.0000e+00      # [1]
       N1      = 1 ,   1       # [cm^(-3)]
       nu      = 1 ,   1       # [1]
       eta     = 5.8200e+30 ,  2.0546e+30      # [V^2/cm*s]
       l_crit  = 1.0000e-06 ,  1.0000e-06      # [cm]
}


*************************** Recombination Models:
******************************
* Variable = electron value ,   hole value     # [units]
*
*****************************************************************
*****************
Scharfetter * relation and trap level for SRH recombination:
{ * tau = taumin + ( taumax - taumin ) / ( 1 + ( N/Nref )^gamma )
  * tau(T) = tau * ( (T/300)^Talpha )         (TempDep)
  * tau(T) = tau * exp( Tcoeff * ((T/300)-1) ) (ExpTempDep)
    taumin = 0.0000e+00 ,   0.0000e+00    # [s]
       taumax  = 2.5000e-06 ,  0.50000e-06    # [s]
       Nref   = 3.0000e+17 ,   3.0000e+17    # [cm^(-3)]
    gamma  = 0.3 ,    0.3 # [1]  IEEE TRANS. On Elec. Dev.
Vol.41.No.6 1994
    *Talpha    = -1.5000e+00 ,  -1.5000e+00   # [1]
    *Lifetime increases as temperature increases
    *alpha was changed to fit the experimental results. [M41]
```

```
    *always use TempDep key in the input file.
    Talpha = 1.72000e+00 ,  1.7200e+00   # [1]
    Tcoeff = 2.55 ,  2.55  # [1]
    Etrap  = 0.0000e+00 # [eV]
}

Auger * coefficients:
{ * R_Auger = ( C_n n + C_p p ) ( n p - ni_eff^2)
  * with C_n,p = A + B (T/T0) + C (T/T0)^2
       *See ref. [9]
    A   = 5.0000e-31 ,   2.0000e-31   # [cm^6/s] * From
http://www.ioffe.rssi.ru/SVA/NSM/Semicond/SiC/recombination.ht
ml
    B   = 0.00    ,   0.00      # [cm^6/s]
    C   = 0.00 ,  0.00      # [cm^6/s]
}

OkutoCrowell * Impact Ionization: <1120>
{ * G_impact = alpha_n n v_drift_n  +  alpha_p p v_drift_p
  * with alpha = a (1+c(T-300)) E^gamma exp[-(b (1+d(T-300))
/E )^delta]
    a   = 2.1000e+7, 2.9600e+07     # [1/cm] * From Hatakeyama for
electron
*   b   = 1.700e+07, 1.6000e+07   # [V/cm] * From Hatakeyama for
holes
    b   = 1.700e+07, 1.4000e+07   # [V/cm] * From Hatakeyama for
holes
    c   = 0.0 ,   0.0 # [1/K]
    d   = 0         , 0         # [1/K]
    gamma  = 0 ,  0  # [1]
    delta  = 1.0 ,   1.0 # [1]
}

OkutoCrowell_aniso * Impact Ionization: <0001>
```

```
{ * G_impact = alpha_n n v_drift_n  +  alpha_p p v_drift_p
  * with alpha = a (1+c(T-300)) E^gamma exp[-(b (1+d(T-300))
/E )^delta]
   a   = 1.76e+8,    3.4100e+08      # [1/cm] * From Hatakeyama for
electron
*   b   = 3.3000e+07, 2.5000e+07    # [V/cm] * From Hatakeyama for
holes
   b   = 3.3000e+07, 2.3000e+07    # [V/cm] * From Hatakeyama for
holes

   c   = 0.0 ,    0.0 # [1/K]
   d   = 0          , 0          # [1/K]
   gamma  = 0 ,  0   # [1]
   delta  = 1.0 ,    1.0 # [1]
}


************************** Incomplete Ionization
***************************
* Nd,ion = Nd / ( 1 + g_D n/nt ); nt =  NC exp(-E_D/kT)      if Nd
< NdCrit   *
* Na,ion = Na / ( 1 + (1/g_A) p/pt ); pt =  NV exp(-E_A/kT)  if Na
< NaCrit   *
* where E_D = E_D_0 - alpha_D * (Nd + Na)^(1/3)
*
*      E_A = E_A_0 - alpha_A * (Nd + Na)^(1/3)
*
**************************************************************
*****************
Ionization
{
* p-type 4H-SiC doped with Al     : 0.191eV
* n-type 4H-SiC doped with Nitrogen: 0.065eV
   E_As_0    = 0.065   # [eV]
```

```
alpha_As  = 3.1000e-08  # [eV cm]
g_As      = 2 # [1]
Xsec_As      = 1.0000e-12  # [cm^2/sec]

E_P_0     = 0.065   # [eV]
alpha_P   = 3.1000e-08  # [eV cm]
g_P       = 2 # [1]
Xsec_P       = 1.0000e-12  # [cm^2/sec]

E_Sb_0    = 0.065   # [eV]
alpha_Sb  = 3.1000e-08  # [eV cm]
g_Sb      = 2 # [1]
Xsec_Sb      = 1.0000e-12  # [cm^2/sec]

E_B_0     = 0.191   # [eV]
alpha_B   = 3.1000e-08  # [eV cm]
g_B       = 4 # [1]
Xsec_B       = 1.0000e-12  # [cm^2/sec]

E_In_0    = 0.191   # [eV]
alpha_In  = 3.1000e-08  # [eV cm]
g_In      = 4 # [1]
Xsec_In      = 1.0000e-12  # [cm^2/sec]

E_N_0     = 0.065   # [eV]
alpha_N   = 3.1000e-08  # [eV cm]
g_N    = 2 # [1]
Xsec_N    = 1.0000e-12  # [cm^2/sec]

E_NDopant_0   = 0.065   # [eV]
alpha_NDopant    = 3.1000e-08  # [eV cm]
g_NDopant = 2 # [1]
Xsec_NDopant = 1.0000e-12  # [cm^2/sec]
```

```
    E_PDopant_0   = 0.191   # [eV]
    alpha_PDopant    = 3.1000e-08  # [eV cm]
    g_PDopant = 4 # [1]
    Xsec_PDopant = 1.0000e-12  # [cm^2/sec]

    NdCrit    = 1.0000e+22  # [cm-3]
    NaCrit    = 1.0000e+22  # [cm-3]
}

BarrierTunneling
{ * Non Local Barrier Tunneling
  * G(r) =
g*A*T/kB*F(r)*Pt(r)*ln[(1+exp((E(r)-Es)/kB/T))/(1+exp((E(r)-Em
)/kB/T))]
  * where:
  *    Pt(r) is WKB approximation for the tunneling probability
  *    g = As/A, As is the Richardson constant for carriers in
semiconductor
  *    A is the Richardson constant for free electrons
  *    F(r) is the electric field
  *    E(r) is carrier energy
  *    Es is carrier quasi fermi energy in semiconductor
  *    Em is carrier fermi energy in metal
  *    alpha is the prefactor for quantum potential correction
    g  = 2.1 ,   0.66   # [1]
    mt = 0.52 ,  0.52   # [1]

    alpha  = 0.0000e+00 ,   0.0000e+00   # [1]
}
```

```
* References :
* [1] N. D. Arora, J. R. Hauser, and D. J. Roulston, ?Electron and
Hole Mobilities in Silicon
*    as a Function of Concentration and Temperature,? IEEE
Transactions on Electron
*    Devices, vol. ED-29, no. 2, pp. 292?295, 1982.


Band2BandTunneling
{ * See Dessis manual `Band-To-Band Tunneling'
       A      = 8.9770e+20    # [cm / (s V^2)]
       B      = 2.1466e+07    # [eV^(-3/2) V/cm]
       hbarOmega      = 0.0186       # [eV]

 * Traditional models for the following keywords in input file:
 * Band2Band(E1)  : A1*E*exp(-B1/E)
 * Band2Band(E1_5): A1_5*E^1.5*exp(-B1_5/E)
 * Band2Band(E2)  : A2*E^2*exp(-B2/E)
**       A1     = 1.1000e+27    # [1/cm/sec/V]
*       A1     = 1.1000e+20    # [1/cm/sec/V]
       A1     = 1.1000e+15    # [1/cm/sec/V]
**       B1     = 2.1300e+07    # [V/cm]
*       B1     = 1.200e+07    # [V/cm]
       B1     = 2.100e+07    # [V/cm]
       A1_5    = 1.9000e+24    # [1/cm/sec/V^1.5]
       B1_5    = 2.1900e+07    # [V/cm]
       A2     = 3.5000e+21    # [1/cm/sec/V^2]
       B2     = 2.2500e+07    # [V/cm]
}
}
BarrierTunneling "NLM"
{ * Non Local Barrier Tunneling
```

```
  * G(r) =
g*A*T/kB*F(r)*Pt(r)*ln[(1+exp((E(r)-Es)/kB/T))/(1+exp((E(r)-Em
)/kB/T))]
  * where:
  *    Pt(r) is WKB approximation for the tunneling probability
  *    g = As/A, As is the Richardson constant for carriers in
semiconductor
  *    A is the Richardson constant for free electrons
  *    F(r) is the electric field
  *    E(r) is carrier energy
  *    Es is carrier quasi fermi energy in semiconductor
  *    Em is carrier fermi energy in metal
    g  = 2.1e-5 ,   0.66e-5   # [1]
    mt = 0.5 ,   0.5 # [1]
}
```