Characterization of Die Stress in Microprocessor Packaging Due to Mechanical, Thermal, and Power Loading

by

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Abstract

Microprocessor packaging in modern workstations and servers often consists of one or more large flip chip die that are mounted to a high performance ceramic chip carrier. The final assembly configuration features a complex stack up of flip chip area array solder interconnects, underfill, ceramic substrate, lid, heat sink, thermal interface materials, second level ceramic ball grid array (CBGA) solder joints, organic printed circuit board, etc., so that a very complicated set of mechanical loads is transmitted to the microprocessor chip. Several trends in the evolution of this packaging architecture have exacerbated die stress levels including the transition to larger die, high CTE ceramic substrates, lead free solder joints, higher levels of power generation, and larger heat sinks with increased clamping forces. Die stress effects are of concern due to several reasons including degradation of silicon device performance (mobility/speed), damage that can occur to the copper/low-k dielectric top level interconnect layers, and potential mechanical failure of the silicon in extreme cases.

In this work, test chips containing piezoresistive stress sensors have been used to measure the buildup of mechanical stresses in a microprocessor die after various steps of the flip chip CBGA assembly process. (111) silicon test chips were used to measure the complete three-dimensional stress state at each sensor site being monitored by the data acquisition hardware. Special test fixtures were developed to eliminate any additional stresses due to clamping effects. The developed normal stresses are compressive (triaxial compression) across the die surface, with significant in-plane and out-of-plane (interfacial) shear stresses also present at the die corners. The compressive stresses increase with each assembly step (flip chip solder joint reflow, underfill dispense and cure, and lid attachment).

The experimental observations from this study show clearly that large area array flip chip die are subjected to relatively large compressive in-plane normal stresses after solder

reflow. It was also observed that the majority of the die compressive stress is accumulated during the underfilling assembly step. Typical increases in the stress magnitude were on the order of 300% (relative to the stresses due to solder joint reflow only). As a general "rule of thumb," approximately two-thirds (66%) of the final die stress magnitudes were observed to be developed during the underfill dispense and cure, with the second largest contribution coming from the die attachment, and the smallest contribution coming from lid attachment.

A unique package carrier was developed to allow measurement of the die stresses in the FC-CBGA components during thermal and power cycling without inducing any additional mechanical loadings. Initial experiments consisted of measuring the die stress levels while the components were subjected to slow (quasi-static) temperature changes from 0 to 100 °C. In later testing, long term thermal cycling of selected parts was performed from 0 to 100 °C (40 minute cycle, 10 minute ramps and dwells) for up to 9000 cycles. After various durations of cycling, the sensor resistances at critical locations on the die device surface (e.g. die center and die corners) were recorded. From the resistance data, the stresses at each site were calculated and plotted versus time. Finally, thermal and power cycling of selected parts was performed, and in-situ measurements of the transient die stress variations were performed. Power cycling was implemented by exciting on-chip heaters on the test chips with various power levels. During the thermal/power cycling, sensor resistances at critical locations on the die device surface (e.g. die center and die corners) were recorded continuously. From the resistance data, the stresses at each site were calculated and plotted versus time.

The experimental test chip stress measurements were correlated with finite element simulations of the packaging process. A sequential modeling approach was used to predict the build-up of compressive stress. The method used incorporates precise thermal histories of the packaging process, element creation, and nonlinear temperature and time dependent material properties. With suitable detail in the models, excellent correlation has been obtained with the sensor data throughout all packaging processes.

Finally, CBGAs with the stress sensing chips were soldered to organic PCB test boards. A simulated heat sink mechanical loading was applied, and the stresses were measured as a function of the clamping force. Compressive stress increases of up to 60 MPa were observed for a 1000 N applied clamping force. The experimental test chip stress measurements were correlated with finite element simulations of the clamping process. Excellent correlation has been obtained between the predicted and measured stress changes occurring during simulated heat sink clamping.

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Nomenclature

Acronyms

AlSiC Aluminum Silicon Carbide

ALT accelerated life testing

BGA ball grid array

CBGA ceramic ball grid array

CCGA ceramic column grid array

CLGA ceramic land grid array

CMOS complementary metal-oxide-semiconductor

CSAM c-mode scanning acoustic microscopy

CSP chip scale package

CTE coefficient of thermal expansion

DAQ data acquisition system

DIMM dual in-line memory module

DNP distance to neutral point

ENIG electroless nickel immersion gold

FC-CBGA flip chip ball grid array

FC-CBGA flip chip ceramic ball grid array

FC-PBGA flip chip plastic ball grid array

FEA finite element analysis

FET field-effect transistor

FIFI far infrared Fizeau interferometry

GPIB general purpose interface bus

HiTCE high temperature coefficient of expansion

ILD interlayer dielectric

LEAP laboratory for electronics assembly and packaging

LGA land grid array

LTCC low temperature cofired ceramic

MPC multipoint constraint

PBGA plastic ball grid array

PCB printed circuit board

PGA pin grid array

PLGA plastic land grid array

PTH plated through hole

RTD resistance temperature detector

SAC tin silver copper solder

SHS simulated heat sink

SMES shadow moiré with enhanced sensitivity

SOP system-on-package

TCR temperature coefficient of resistance

TEFCBGA thermally enhanced flip chip ball grid array

TIM1 first level thermal interface material

TIM2 second level thermal interface material

TIM thermal interface material

WB wire bond

English letter symbols

B_i Piezoresistive coefficient

l direction cosine

m direction cosine

n direction cosine

R resistance, Ω

T temperature, K

t time, s

Greek letter symbols

δ_{ij} Kronecker Delta,

$\Delta\sigma$ stress change

π resistivity tensor,

ρ resistivity, kg/m^3

$\bar{\rho}$ isotropic unstressed resistivity

σ stress, MPa

θ angle

Superscripts

n n-type

p p-type

Subscripts

DA die attach

L lower arm

lid lid attach

ref reference

U upper arm

UF underfill

Chapter 1

Introduction

1.1 Area Array Components in Microprocessor Packaging

Area array microprocessor packages are at the heart of high-end workstations and servers. A typical package may consist of at least one large flip chip die attached to a high density ceramic chip carrier. Figure 1.1 illustrates the typical configuration of a server microprocessor mounted on a motherboard and topped with an air-cooled heat sink. With the need for ever increasing computing power and increased interconnect density, the first level, chip-to-substrate interconnections have transitioned to full area arrays of lead free solder bumps. Die size has also increased significantly. While older alumina ceramic substrate technology allowed better reliability performance due to the the close matching of the coefficients of thermal expansion of alumina and silicon, manufacturers are currently using “high CTE” (HiTCE) glass ceramic materials [1–7].

The thermal expansion coefficients of the HiTCE ceramics are closer to the CTE of the typical organic printed circuit board to which they are mounted, increasing second level interconnect reliability in many cases. However, matching of the thermal expansion coefficients of the second level comes at the cost of increasing the dissimilarity in the CTE values of the die and ceramic, resulting in lower reliability of the first level of interconnections. High CTE ceramics have found their place mostly due to their lower stiffness (70 - 80 GPa) and lower co-firing temperatures, which allows the use of copper conductors as opposed to lower performance tungsten conductors used with alumina ceramic substrates.

A glass-filled epoxy commonly known as underfill, found between the die and substrate, is another component of a typical microprocessor package. A metal (copper or AlSiC) lid, or heat spreader, tops the silicon die and is mechanically connected to the substrate and die by

a thermal interface material (TIM1). Figure 1.1 shows the ceramic substrate mechanically and electrically connected to a large printed circuit board (PCB) with second level solder balls, with the remaining volume under the substrate filled with a second level underfill. In this configuration, the chip and substrate assembly is referred to as a Ceramic Ball Grid Array (CBGA), due to the inclusion of an additional set of second level solder interconnects to the substrate. The chip and substrate assembly can also be used as a Land Grid Array (LGA), and be connected to the PCB with a socket and associated mechanical connections. In both cases, a heat sink is clamped to the entire assembly and bonded with a second Thermal Interface Material (TIM2).

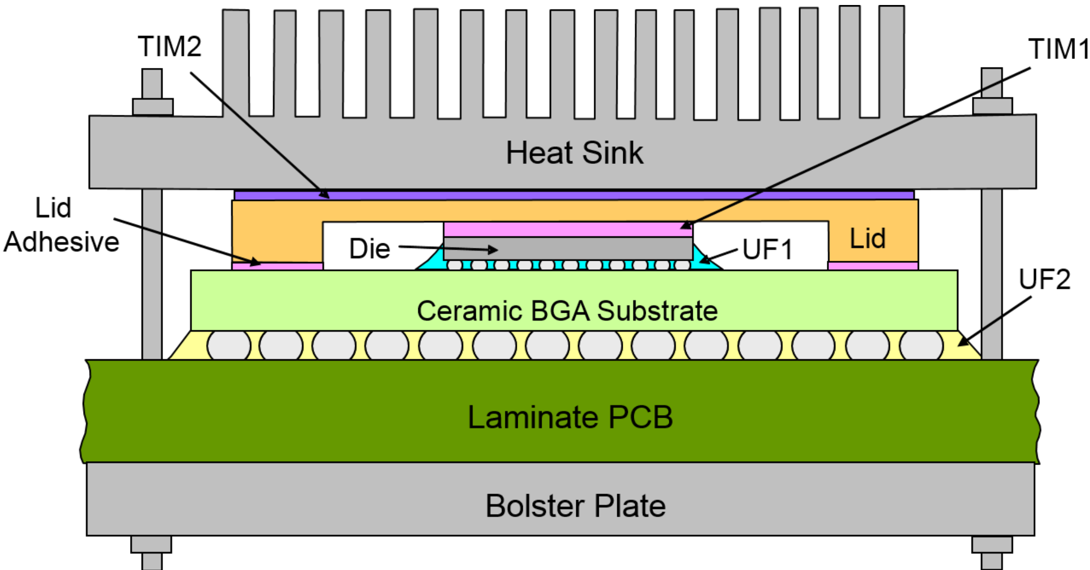


Figure 1.1: Architecture for a High Performance Flip Chip Microprocessor

This complex architecture and others under development transmit a complicated set of mechanical loads to the microprocessor chip. Along with the change to higher CTE substrates, the use of stiff lead free solders along with ever increasing die sizes have increased die stress levels. Although necessary to ensure good heat transfer, mechanical clamping of associated heat sinks adds to die stress issues. Microprocessors are also dissipating more power with each generation of new designs. The amount of power dissipation along with the cyclical nature of the power usage of microprocessors further exacerbates analysis of

package reliability. The various mechanical, thermal, and power loadings associated with a typical package affect the stresses in the die, which can degrade silicon device performance (mobility/speed) and damage critical copper/low-k dielectric chip interconnect layers.

On-chip piezoresistive stress sensors represent a unique approach for characterizing stresses in silicon die embedded within a complicated packaging architecture such as that described above. Die stress measurements in flip chip assemblies have been performed by several investigators using test chips [8–14]. Variations of the (100) silicon Sandia ATC04 test die have been used to examine device side die stresses and compare stress levels with different underfills [8–10]. In previous flip chip studies, the mechanical stresses present on the backside (top side) [11] and the device side (bottom side) [12–14] of the die at each stage of the flip chip assembly process were investigated. In these investigations, (111) silicon test chips were used that were able to measure all of the die stress components including the interfacial shear stresses. Die stress variations were observed during underfill curing, and the room temperature die stresses in the final cured assemblies have been compared for several different underfill encapsulants.

In this work, test chips using piezoresistive sensors were used to measure die stresses in microprocessor packages caused by various stages of assembly as well as mechanical, thermal, and electrical loading. Use of (111) test chips allowed measurement of the complete three-dimensional state of stress at sensor locations across the entire die. The 20 x 20 mm test chips were attached to high CTE ceramic chip carriers with a full array of 3600 lead free solder bumps. Prior to assembly, each bare test chip was manually probed to measure initial resistances of each selected sensor. The test die were then assembled by solder reflow attachment to ceramic substrates, applying and curing a first level undefill, and adding a thermal adhesive (TIM1) and heat spreader. The chosen sensor resistances were measured again after each assembly step in order to characterize stresses induced by each step. The build-up of the die stresses was found to be monotonically increasing, and the relative severity of each assembly step was judged and compared. The assemblies were

then used to characterize the stresses induced by temperature change and thermal cycling using a novel package carrier. Several assemblies were also used in the characterization of die stresses due to power dissipation in the die and initial power cycling experiments. A separate set of additional test die were measured at the bare die state and again after application of second level solder interconnects, and reflow to large laminate printed circuit boards.

Chapter 2

Literature Review

2.1 Introduction and Review of Electronic Packaging Issues

From the inception of the integrated circuit, chips have increasingly become faster, more powerful, and contained more transistors while actual feature sizes continue to shrink. These trends in IC technology have created reliability issues across all platforms, and especially in high-end computing and server applications. Each assembled chip and associated packaging contains a myriad of materials, each with, in some cases, drastic differences in mechanical and thermal properties. Some materials exhibit isotropic mechanical behavior with little or no dependence on temperature, while others are anisotropic, rate and temperature dependent. The coefficient of thermal expansion, or CTE, has been demonstrated to be one of, if not the largest contributor to package stress generation and failure. Given the relationship between mechanical stress and failure, an obvious need arises for the characterization of stress levels caused not only by manufacturing, but by the use of electronic packages.

2.1.1 Historical Packaging Issues

Dale and Oldfield [15] described die attachment, wire bonding, and encapsulation as sources of stress in electronic packaging. They found that several contributors to manufacturing induced stresses including oxidation, diffusion, metallization, and wafer processing. Lau [16] concurred with these findings and additionally cited the effects of various surface mounting processes and die bending during assembly. Lau also related stresses to wire bond damage, die passivation cracking, and package cracking. Several investigators have examined the effects of temperature on package stresses. Lesk, et al. [17], and Edwards, et al. [18] looked at metal shift and damage due to thermally induced stresses. Reference [17] also

considered the issues related to packages with large die. Inayoshi, et al. [19] also studied the effect of stress on the passivation layer of silicon die. Van Kessel, et al. [20] studied the effects of manufacturing processes, including die attachment on stresses as well as the large effect of stresses on packages with certain die surface finishes. Nishimura and co-authors [21, 22] demonstrated that while cracks in packages can be induced by thermal cycling, the cracks also have a large effect on die stress levels. Additionally, encapsulants may pose other problems in encapsulated packages.

2.1.2 High-End Microprocessor Issues

Several investigations have been performed on the thermal-mechanical reliability of the second level CBGA solder joints when using high CTE ceramic substrates. Pendse, et al. [2] demonstrated order of magnitude type improvements in the thermal cycling reliability using both thermal cycling tests and finite element simulations. Dai, et al. [3] and Pan and co-workers [4] have examined the effects on reliability of 52.5 x 52.5 mm CBGAs (2533 I/O) with various solder alloys (SnPb and SAC), ceramic substrate thicknesses, lid configurations, and lid materials (AlSiC compositions). Their results suggest that reliability is increased significantly when using the SAC solder alloy, a lid-less configuration (not practical if a heat sink is needed), and a lid material with lower SiC content. The ceramic substrate thickness had little effect on reliability due to the fact that the new ceramic materials are more compliant (lower stiffness) than traditional alumina compositions, as well as they provide a better CTE match between the ceramic substrate and PCB laminate.

Enhanced solder joint reliability has also been demonstrated for 42.5 x 42.5 mm and 45 x 45 mm CBGAs [5, 6], and for Ceramic Column Grid Arrays (CCGAs) [5, 7] when using the higher CTE ceramic substrates. Xu, et al. [23] have explored the heat transfer characteristics and air cooling limits of the packaging configuration in the previous chapter (Figure 1.1). Using finite element simulations, Tosaya et al. [6] have predicted a 2X increase in the die normal stress levels for a flip chip mounted on a high CTE ceramic carrier (relative

to the analogous configuration on an alumina carrier). In addition, the stresses at the die to underfill interface were significantly higher with the high CTE ceramic carrier, complicating underfill selection and raising concerns relative to damage of fragile Interlayer Dielectric (ILD) layers.

2.2 Stress Determination in Electronic Packaging

Integrated circuit package failures have existed since their inception, and numbers of investigators have employed diverse methods to characterize, measure, and otherwise understand stress levels in IC packages. Suhir [24, 25] drew parallels between bimetal thermostats and interfacial stresses in electronic packages. Using this understanding, an analytical approach using beam theory was developed. Tay and co-workers [26–28] modeled delamination during reflow using an analytical approach and correlated modeling results with experiments.

The complex geometries of electronic packages have historically limited the use of accurate analytical methods. Well known and often used reliability models such as Coffin-Manson equation and the Distance to Neutral Point (DNP) approach are crude, being based on simplified approaches with extensive assumptions. The limited effectiveness of these analytical models has led to increased use of experimental methods, especially when correlated with some form of simulation such as finite element analysis (FEA).

2.2.1 Experimental Methods

2.2.2 Interferometric Techniques

Moiré interferometry is a useful tool for experimental measurement of displacements of an object. Classical moiré methods capture the in-plane deformations of a body and allow for extraction of strain data in the plane. Shadow Moiré methods are invaluable for measurements of out-of-plane warpage and other out-of-plane displacement. Han and Guo [29], Bastawros and Voloshin [30], and Liu, et al. [31] have used moiré methods to measure thermally induced deformations in electronic packages. Hartsough, et al. [32] used

a combination of Twyman-Green Interferfometry and shadow moiré techniques to study warpage of non-conventional packages caused by reflow and assembly processes. Huang and co-workers [33] employed shadow moiré along with strain gages to study warpage and curvature of printed circuit boards with DIMM memory chip sockets during reflow and correlated FEM simulation results. Powell and Ume [34] developed a warpage measurement system to study packages during convective solder reflow. Verma, et al. [35] employed shadow moiré with enhanced sensitivity (SMES) along with far infrared Fizeau interferometry (FIFI) to study warpage of plastic ball grid array (PBGA) packages during thermal cycling. Wang and Hassell [36] used phase-stepping shadow moiré to study thermally induced warpage in BGA packages and substrates. Zhong, et al. [37] discussed methods of extracting high-resolution data from moiré images used in warpage measurement.

2.2.3 Semiconductor Test Chips

Silicon is a piezoresistive material which exhibits a change in resistivity upon application of a mechanical stress. This feature has led to the development of silicon stress sensing integrated circuit chips. In the 1950s, the concept of using piezoresistive semiconductors as tools to measure stress and strain was introduced by Smith [38]. Later, the temperature dependencies of the piezoresistive coefficients of silicon, as well as germanium, were studied by Tufte and Stetzer [39], as well as Suhling, et al. [40, 41]. The nonlinear nature of the piezoresistive effect was discussed by Yamada and co-workers [42], while the piezoresistive coefficients were represented graphically by Kanda [43]. A full discussion of semiconductor strain gages was given by Dally and Riley [44]. The detailed theory of silicon piezoresistive sensors was derived by Bittle, et al. [45, 46], while Kang [47] expanded and applied this theory to various wafer planes for silicon and silicon carbide.

In the use of piezoresistive silicon stress sensors, the need for calibration of the piezoresistive coefficients of the silicon chip is widely accepted. Traditionally, some form of four-point bending method is used for calibration. This method has been discussed in detail by Beaty,

et al. [48], Bittle, et al. [45, 46], Suhling, et al. [40, 41], Jaeger, et al. [49–52], and van Gestel [53]. A method of calibration employing application of a hydrostatic state of stress to a chip in a pressure vessel was devised by Kang, et al. [54]. The four-point bending and hydrostatic methods are performed on sliced silicon wafer strips and diced silicon chips, respectively. Cordes [55] and Suhling, et al. [56] have alternatively devised a calibration technique applied at the wafer level. Lwo, et al. [57–59] also discussed the design and fabrication of stress sensors, and designed and fabricated a calibration apparatus.

Piezoresistive stress sensors have been used by many researchers to study die stress levels in electronic packages. In early work, Edwards, et al. [18], Groothuis, et al. [60], and van Kessel, et al. [20] used chips fabricated from (100) silicon wafers to examine small packages. These early test chips contained two-element sensor rosettes, with the sensors oriented at 0 and 90 degrees to the wafer flat. Early work was aimed at material evaluation, reliability testing, and process control. Later, Gee, et al. [61] used four element rosettes to map stresses during thermal cycling. Van Gestel and co-workers [62] also used these same chips to study dual inline packages.

Miura, et al. [63–65] also used (100) chips to study die stresses in dual inline packages. The chips used in their study employed sensors fabricated with both n-type and p-type doping, where the n-type sensors were oriented at 0° and 90°, and the p-type sensors were oriented at ±45°. This chip was notable, as it was the first test chip able to measure out-of-plane normal stresses on the die. Zou, et al. [66–68] also used (100), four element test chips. The chips used the same sensor orientations as the Miura chips, but the doping of the sensor pairs was reversed. The Sandia ATC-04, a (100) silicon test chip, was used to study die mounted on ceramic substrates by Sweet [69]. The Sandia chip used a sensor rosette with eight resistors, including four n-type sensors at orientations of 0°, ±45°, and 90°, and four p-type sensors of the same orientations. The third generation of Sandia test chips has also been studied [70]. Bossche, et al. [71, 72] and Lo, et al. [73, 74] designed, fabricated, and calibrated stress sensing chips with similar capabilities to prior studies. Mayer [75, 76]

has also developed piezoresistive test structures, mainly to study the effects of thermosonic wire bonding.

Suhling and his co-workers [77–81] have demonstrated the advantages of stress sensors fabricated from (111) silicon wafers as opposed to (100) wafers. When optimized, rosettes on (111) silicon can measure the complete state of stress at a point. In addition, optimized (111) rosettes can measure four temperature compensated stress components, as opposed to (100) rosettes, which can measure two temperature compensated stress components. Suhling, et al. [78, 80] used these advantages to be the first to measure the complete state of stress at a point on the surface of a die with test chips designated BMW-1. This chip used an eight sensor rosette containing n-type and p-type sensors oriented at 0°, ±45°, and 90°, with respect to the wafer flat. The BMW-1 chips were mounted to organic substrates, and then used to measure stress in chip on board packages at room temperature. These studies were the first to measure out-of-plane shear stresses at the interface of the die and encapsulant. Zou, et al. [66–68] used a second iteration of the BMW chip to measure stresses in different packages. Schwizer, et al. [82, 83] described a new test chip package that uses a flip chip micro sensor, capable of measuring forces on solder balls in three directions.

Jaeger, et al. [84–88] and others [89–91] have utilized other silicon devices such as transistors and van der Pauw structures to develop stress sensor chip technology. In these studies, relationships between applied mechanical stress and transistor performance were developed. Mian [92] developed and used van der Pauw structures to characterize stress. Mayer, et al. [93] also used test chips with MOS technology.

Piezoresistive stress sensors have also been used to characterize stress levels during and after different stages of package assembly. Stresses due to die attachment and encapsulation were studied by Natarajan, et al. [94] using chips fabricated from n-doped (100) silicon wafers. Integrated piezoresistive stress sensors were also employed by Bjorneklett, et al. [95] to measure stress induced by die attachment. Ducos, et al. [96] measured stress levels during package assembly in-situ. Evans and co-workers [97] measured the resistances of sensors on

chips assembled into various ball grid array packages. Rahim [98] measured stress levels on both sides of a flip chip die during each stage of assembly. Peterson, et al. [8, 99] used test chips to study flip chip ball grid array packages. Zou and co-workers [100] also used test chips to evaluate die attachment adhesives in ceramic Pin Grid Array (PGA) packages. Palaniappan, et al. [9, 10] used test chips to study curing parameters of flip chip assemblies.

It should be noted that use of piezoresistive stress sensors requires foreknowledge of errors expected in their calibration and use. Aside from error in any data acquisition system or the physical wiring of a test setup, there are several ways inappropriate use or calibration may affect results. A discussion of optimized rosette design has been given by Suhling, et al. [78], and a complete discussion of design and calibration errors was presented by Jaeger and co-workers [52, 101, 102].

2.2.4 Numerical Methods

While experimental methods have given great insight to stress and reliability issues in electronic packaging, in many cases they are expensive and time consuming. Some methods are destructive and do not allow further testing of samples that were carefully prepared with substantial cost. In an effort to to decrease expenditures related to experimental methods, numerical methods have gained widespread popularity in industry and research. The finite element method (FEM) and finite element analysis (FEA) are powerful tools that can decrease time to market, eliminating experimental costs. Finite element analysis allows modelers to implement the wide variety of geometric, material, and environmental conditions seen by IC packages.

In early work, FEA techniques were used to study the effects of different materials and geometry on dual inline packages by Groothuis, et al. [60], and Pendse [103]. Kelly, et al. [104, 105] studied thermal stresses in plastic packages numerically. Van Gestel [62] used simulation techniques to study delamination in plastic packages. Sweet, et al. [70, 106] used a viscoplastic material model in a study of die surface stresses. Bailey, et al. [107] used

a one-eighth model to simulate the reliability of perimeter bumped flip chip on laminate assemblies.

Gektin and Bar-Cohen [108] used finite element simulations to study the effects of underfill on the reliability of flip chip assemblies. Chen, et al. [109] modeled the effects of underfill filler particles on the interfacial stresses in flip chip assemblies. Chen, et al. [110] numerically investigated die stresses in over-molded flip chip, chip scale packages (CSP). Hong and Su [111] also studied the effects of overmolding, but in plastic ball grid array (PBGA) chip scale packages using using a popular technique called slice modeling. A slice model only uses geometry of approximately one solder ball width in the linear region from the center of the die to the corner ball. This technique is popular due to small computational time and the fact that historically, the critical solder ball(s) in reliability testing is found along this diagonal.

Chen, et al. [112] used a visco-plastic model to study flip chip on flex substrate assemblies. Chung, et al. [113] modeled stresses in second level interconnects of flip chip CSP packages. Fan and coworkers [114] modeled the effects of temperature cycling on undefill delamination and cracking. Similarly, Gao, et al. [115] analyzed the effect of underfill delamination on flip chip reliability. Guo and Zhao [116] modeled die stresses and package warpage in flip chip ball grid array assemblies. Jhou [117] modeled thermally induced stresses and deformations in several geometries including copper post and copper pillar interconnects. Kpobie, et al. [118] used an FEA technique called sub-modeling to predict stresses and displacements in flip chip assemblies with a large array of fine pitch interconnects.

Ma, et al. [119] uses the Anand model for lead-free solder to study the reliability of thermally enhanced flip chip ball grid array (TEFCBGA) packages. Pang and Chong [120] used both one-eighth and slice models to study the reliability of flip chip on board assemblies. Tsai, et al. [121] and Tzeng, et al. [122] simulated the warpage and package stresses during assembly and thermal cycling of FCBGA packages. Tsai, et al. [123] also modeled the effect of underfill selection and Tzeng, et al. [124] predicted the effects of different solder bump

geometries. Ernst and coworkers [125] modeled the effects of underfill material models on the effects of underfill cure on residual package stress. Davoine, et al. [126] modeled the effects of pitch on residual stresses due to reflow for flip chip packages.

2.3 Correlation of Experimental and Numerical Methods

While models have advantages over some experimental methods in cost and time, numerical analysis is truly a prediction tool, and is only as good as the given input. Many times bad input or bad assumptions lead to incorrect finite element predictions for the mechanical system. For this reason, researchers have relied on correlation of numerical methods with experimental data. Skipor, et al. [127] used moiré interferometry to measure displacements of two different packages, then measured stresses in the packages with test chips, and compared both sets of data with finite element predictions. Ducos, et al. [96] also correlated their results with FEA data. Slattery, et al. [128] used both piezoresistive stress chips and finite element analysis to characterize stress levels in packages. Chen, et al. [129] studied the effects of underfill in two types of packages with the use of two-dimensional finite element analysis and experimental techniques. Analytical, numerical, and experimental results were also correlated in the work of Peterson, et al. [8]. Zou [66, 68, 100] related test chip stress data from PGA and chip on board packages to finite element simulations. More recently, Rahim [98] showed graphical correlation between measured die stress levels at various stages of assembly and the corresponding predictions from FEA models, and also investigated stress effects over large temperature ranges with both finite element models and piezoresistive test chips [13]. Chen [130] mapped die stress levels using CMOS stress sensors and also graphically showed agreement with finite element data.

Hong, et al. [111] correlated models of thermally induced stress with reliability data from thermal cycling. Ma, et al. [119] related numerical results of the failure mode of TEFCBGA packages to thermal cycling data and destructive failure analysis. Ouimet and coworkers [131] used acoustic microscopy, warpage measurements, and thermal performance

testing to validate models of a large dual flip chip plastic land grid array (PLGA). Shen, et al. [132] combined the use of piezoresistive stress sensors and finite element models to better understand die stresses relative to solder ball location. Son, et al. [133] combined traditional moiré, phase-shifted moiré, contact resistance measurements and finite element simulations to study fine pitch lead free flip chip on organic assemblies. Tsai and co-workers [134, 135] also correlated their finite element simulation of plastic ball grid array thermal warpage to moiré results. Guo and Zhao [116] correlated warpage and stress data in flip chip packages to finite element simulations. Fan, et al. [114] correlated models of the effects of temperature cycling on undefill delamination and cracking with course finite element models. Jhou, et al. [117] not only modeled thermally induced stresses and deformations in several geometries including copper post and copper pillar interconnects, but compared simulation with both analytical solutions and moiré data.

2.4 Heat Sink Clamping

The use of thermal heat sinks to draw heat away from the working die is commonplace in computing. It is effective method for removing heat from the die surface and improving the life performance of the overall product. The use of heat sinks does bring about several issues related to reliability and the mechanical effects on the assembly, specifically the die. Eyman and Kromann [136] investigated the effects of several types of clip on and adhesive attached heat sinks on reliability of plastic ball grid array (PBGA) componenets using several methods including thermal cycle reliability testing, drop testing, and heat sink shear testing. Zhu, et al. [137] studied the effects of the mechanical interplay between clamping force and thermal expansion during thermal cycling on the reliability of BGA packages. Lopez and co-workers [138] used Monte Carlo simulations to probabilistically determine the loading on the package for clamped CLGA assemblies.

Chen, et al. [139] measured the force acting on the die due to heat sink clamping. In one part of the study, forces acting on the package were quantified as a function of various

mounting schemes and fastener torque levels. Three-dimensional finite element models were used to predict the stress distributions in both the TIM1 layer and solder interconnects. Garner, et al. [140] and Bhatti, et al. [141] studied the effects of simulated heat sink loading on the reliability on FCBGA components using experimental reliability tests along with finite element simulations. Quinones and Babiarz [142] looked at effects of heat sink application on the reliability of chip scale packaging. Ben-Achour and Bar-Cohen [143] studied die displacement and stress under the presence of heat sink loading using finite element models as well as thermal reliability testing. Chiu, et al. [144] quantified the effects of compressive heat sink loading on board level reliability (BLR) and assembly collapse using experimental and numerical methods. Most of the literature related to heat sink clamping is focused on reliability of the interconnects on the package or thermal performance. Very few studies specifically investigated the effects of heat sink clamping on the die.

2.5 Thermal Cycling

Accelerated life testing (ALT) is a popular method of qualifying electronic components. ALT is normally performed using thermal cycling, where the test assemblies are subjected to harsh changes in temperature over a much shorter period of time than expected in field exposures of the parts. The range of temperature is also often much greater than the true application environment. The goal is to then use the ALT data to predict/estimate the reliability. This process also allows the determination of various characteristics of the packaging architecture during its life cycle, i.e. critical locations, failure modes, stress levels, etc. Subjecting a component to high stress levels not only allows for the study of failures during a life cycle, it also enables reduction of the time required to make design improvements, component choices, and material selections.

Much of the literature is related to reliability studies more than stress effects on the package. Sherry, et al. [145] thermally cycled leadless ceramic chip carriers (LCCC) on FR4 using three different thermal profiles, from -20 to 130 °C, -20 to 80 °C, and 30 to 80 °C,

and correlated finite element models to the results. Lodge and Pedder [146] cycled dielectric ceramic on silicon test chip structures for up to 2000 thermal cycles over a range of -55 to 125 °C. Suryanarayana, et al. [147] studied the effects of different encapsulants on the thermal cycling reliability of flip chip on ceramic substrate assemblies subjected to 0 to 100 °C and -55 to 125 °C testing. Various temperature profiles were used by Clementi, et al. [148] to investigate different encapsulant materials for flip chip on ceramic components, including -40 to 65 °C, 0 to 100 °C, 10 to 100 °C, -55 to 125 °C, as well as a cryogenic to room temperature cycle of -200 to 25 °C. Parts in the tests from 0 and 10 to 100 °C were cycled a minimum of 10,000 times.

Master, et al. [149] used thermal cycling tests from both 0 to 100 °C and -55 to 125 °C to quantify the reliability of ceramic column grid array (CCGA) packages as well as ceramic ball grid array (CBGA) packages. The bulk of their study looked at the CCGA packages and the effects of interconnect pitch, substrate rework, and flux type (rosin vs. no-clean) on interconnect reliability. Similar treatment was given to the AMD K6 flip chip die [150]. As part of a study on organic flip chip substrates, Petefish and co-workers [151] cycled flip chip components on organic substrates from -55 to 125 °C for a minimum of 1000 cycles. Mercado and Sarihan [152] performed a parametric reliability study to determine the effects of substrate thickness, solder composition, interconnect array design, underfill selection and solder interconnect height on reliability of CBGA components. Mercado, et al. [153, 154] later studied the effects of thermal cycling on the copper/low-k interconnects found in both PBGA and CBGA packages. Di Giacomo, et al. [155] studied the effects of cycling rate on the reliability of CBGA packages. Newman, et al. [156] tested various chip scale package (CSP) devices on the same laminate test board over the range of 0 to 100 °C.

Shinotani and co-workers [157] used thermal cycling from -55 to 125 °C to aid in material selection of substrates for system-on-package (SOP) components. Spraul, et al. [158] cycled flip chip components on low temperature cofired ceramic (LTCC) substrates from -40 to 125 °C and from -40 to 85 °C. Jen and coworkers [159] compared finite element simulations

to thermal cycling results for both flip chip plastic ball grid array (FC-PBGA) and flip chip ceramic ball grid array (FC-CBGA) components. Yan and co-workers [160] compared thermal shock results to finite element simulations for a unique double bump interconnect for flip chip assembly.

While several researchers have applied accelerate life testing techniques to flip chip packages, including many with ceramic substrates, only a few limited studies have been performed on geometries and materials that are directly related to this dissertation. Zhang, et al. [161] first studied the applicability of different lead free solder joint acceleration factor models of several geometries. A plastic ball grid array geometry and a ceramic ball grid array geometry were studied using three thermal cycles. The flip chip ceramic ball grid array investigated matches the geometry in Figure 1.1 and that found in the remainder of this work. The FC-CBGA was simulated and tested using thermal cycles of 0 to 100 °C, 25 to 85 °C, and a mini-cycle of 75 to 85 °C. Zhang [162] later carried out an experimental and numerical study of the flip chip ceramic ball grid array found in this study. He was primarily concerned with the reliability of the second level solder ball interconnects, but his work was valuable in further understanding the geometry seen later in the current study, as the basic package contained the same geometry and material set.

2.6 Power Cycling of IC Components

Thermal cycling accelerated life testing aims to gain better understanding of the mechanical behavior of electronic packages while reducing time needed to see failures representative of those seen in field use. In thermal cycling, the temperature source is external to the chip itself, which is the true heat source in working microprocessors. Power cycling of IC components aims to gain a similar understanding of the interactions seen in thermal cycling, and more importantly the actual use of the package.

In relatively early studies, Munikoti and Dhar [163, 164] used daisy chained plated through holes (PTH) to provide internal ohmic heating to evaluate the reliability of plated

through holes and interconnects on printed circuit boards. Later, Hong [165] studied the behavior of 119-ball plastic ball grid array packages under power loads of 0 to 3 Watts with a frequency of 2 cycles per hour, and showed a sawtooth wave type transient temperature response. Hong, et al. [166] also numerically and experimentally evaluated the reliability of 25 mm flip chip ceramic ball grid array packages in close proximity to each other. A power cycle of 0 to 5 Watts at 3 cycles per hour was chosen for the study, and the effects of airflow on the transient temperature response of the packages was reported. Ham and co-authors [167] worked to understand the fundamental differences between thermal cycling and power cycling by measuring deformations with moiré techniques and performing simulations for both scenarios. They found that while shear strains in the solder interconnects were similar in both cases, the normal deformations were fundamentally different, with the bending in power cycling tests found to be opposite that found in thermal cycling tests.

Syed [168] used peltier junctions attached to plastic ball grid array packages on laminate substrates to carry out power cycling experiments in order to alleviate the need for thermal test die. Using transient thermal analysis, the resulting temperature profile was correlated with finite element simulations. Towashiraporn and co-workers [169, 170] also used a peltier junction heater to provide heat dissipation, measuring the thermal response of the chip scale package with infrared thermography, and correlated their findings with finite element simulations. The work aimed to compare the effects of power cycling and thermal cycling on the same package, but admittedly the thermal profiles of the two tests were very different. Rodgers, et al. [171] also thermal and power cycled BGA packages, but instead of comparing the effects, combined them. Transient thermal response measured by both infrared thermography and on-package diodes correlated very will to predicted temperature from a transient thermal finite element model.

Mawer and co-workers [172] also thermal and power cycled components, using flip chip plastic ball grid array components on laminate substrates. In both cases, the assemblies were cycled from room temperature to 125 °C, with die temperature monitored by an integral

RTD stucture on the die. In this study the power cycled components exhibited a greater characteristic life, but it is noted that the thermal profiles of both tests did not match. Liu and Irving [173] focused on electromigration and thermal-mechanical failure in their power cycling study. Small die bumped to lead frames were subjected to one Watt of power for two minutes, followed by two minutes of no power dissipation. Transient temperature and stress profiles were also modeled for the solder ball interconnects. Similarly, Ahmed and Park [174] measured the effects of a 3 Watt, 16 second power cycle on flip chip ceramic ball grid array packages, correlating results from transient computational fluid dynamic and structural finite element simulations.

Wang, et al. [175] measured temperature effects of steady-state and transient power dissipation of 0.5 and 1 Watt with three different cycle durations. These results were compared to thermal cycling results for the same part subjected to three different thermal cycles as well as thermal and mechanical finite element simulations. Thermomechanical behavior of flip chip die on organic and ceramic substrates was studied by Park, et al. [176]. Their study employed the use of power cycling, thermal cycling, moiré interferometry, computational fluid dynamics, and a structural finite element code. Power cycling was accomplished by attached foil heaters atop packages and sectioning those in the moiré portion of the study. Pei, et al. [177] simulated FC-BGA packages comprised of both tin-lead and lead-free solders under the influence of power cycling. He modeled an on-off power cycle as well as a cycle including mini-cycles in which simulated temperatures fluctuated 15 °C over 7 minutes. Zhang [178] also included the effects of power cycling with mini-cycles in a discussion on applicable methods for reliability testing.

Chapter 3

Review of Piezoresistive Theory

3.1 General Resistance Change Equations

The term piezoresistive refers to a material that undergoes a change in electrical resistance under the application of a mechanical load. The application of a load to silicon changes its resistivity behavior from isotropic to anisotropic. The relation between the anisotropic second order resistivity tensor of silicon and the second order stress tensor can be modeled using the equation [46]

$$\rho_{ij} = \bar{\rho}\delta_{ij} + \pi_{ijkl}\sigma_{kl} \tag{3.1}$$

where π is the fourth order piezoresistivity tensor, σ is the second order stress tensor, ρ is the second order resistivity tensor, δ_{ij} is the Kronecker delta, and $\bar{\rho}$ is the original isotropic unstressed resistivity of silicon. Equation (3.1) can also be can be written for an arbitrary rotated orthogonal coordinate system as

$$\rho'_{ij} = \bar{\rho}\delta_{ij} + \pi'_{ijkl}\sigma'_{kl} \tag{3.2}$$

where π' is the fourth order piezoresistivity tensor in the rotated system, and σ' is the second order stress tensor in the rotated system. Using reduced index notation, eq. (3.2) becomes

$$\rho'_{\alpha} = \rho_{\alpha} + \pi'_{\alpha\beta}\sigma_{\beta} \qquad \alpha, \beta = 1, 2, \ldots 6 \tag{3.3}$$

At this point, the development is specialized to the filamentary silicon conductor shown in Figure 3.1. The conductor is oriented arbitrarily in an orthogonal (x_1, x_2, x_3) coordinate

system, where the unprimed axes $x_1 = [100]$, $x_2 = [010]$, and $x_3 = [001]$ are the principal crystallographic directions of the m3m silicon crystal. The normalized resistance change of the conductor can be expressed as [46]

$$\begin{aligned}\frac{\Delta R}{R} = &(\pi'_{1\alpha}\sigma'_{\alpha})\, l'^2 + (\pi'_{2\alpha}\sigma'_{\alpha})\, m'^2 + (\pi'_{3\alpha}\sigma'_{\alpha})\, n'^2 + 2\,(\pi'_{4\alpha}\sigma'_{\alpha})\, l'n' \\ &+ 2\,(\pi'_{5\alpha}\sigma'_{\alpha})\, m'n' + 2\,(\pi'_{6\alpha}\sigma'_{\alpha})\, l'm' + \left[\alpha_1 T + \alpha_2 T^2 + \ldots\right]\end{aligned} \tag{3.4}$$

where R is resistance, $\pi'_{\alpha\beta}$ are the off-axis piezoresistive coefficients, σ'_{α} are the stress stress components in the rotated primed coordinate system, α_1 and α_2 are temperature coefficients of resistance, and l', m', and n' are the direction cosines of the conductor orientation with respect to the primed system.

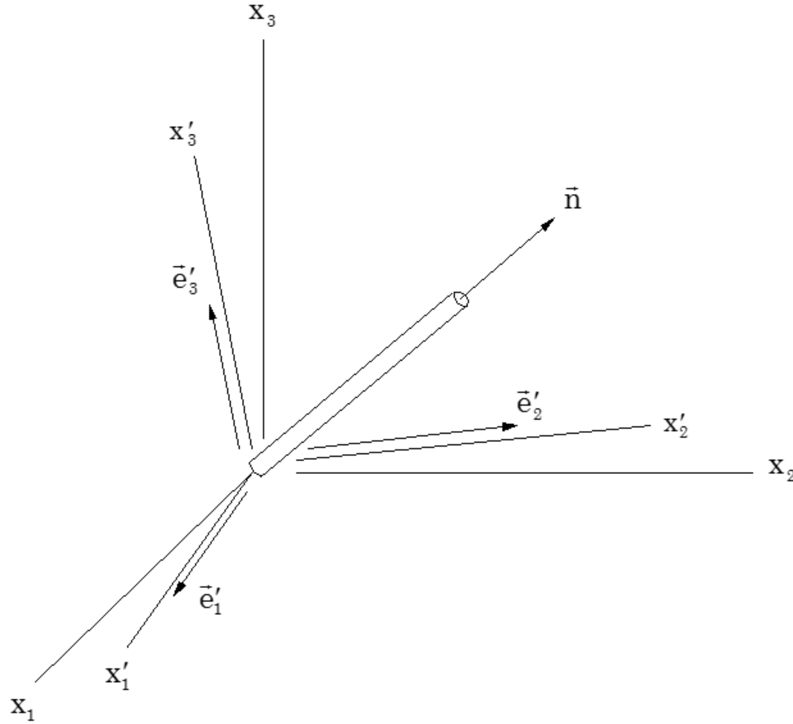


Figure 3.1: Filamentary Silicon Conductor

In this equation, T is the temperature change

$$T = T_m - T_{ref} \tag{3.5}$$

where T_m is the temperature of the silicon when the final resistance measurement is made, and T_{ref} is the reference temperature of the silicon when the initial unstressed resistance R is measured. Equation (3.4) follows the summation convention for repeated indices, and α takes on values $\alpha = 1, 2, \ldots, 6$. The stress components are given in reduced index notation:

$$\begin{aligned} \sigma'_1 = \sigma'_{11}, \quad \sigma'_2 = \sigma'_{22}, \quad \sigma'_3 = \sigma'_{33} \\ \sigma'_4 = \sigma'_{13}, \quad \sigma'_5 = \sigma'_{23}, \quad \sigma'_6 = \sigma'_{12} \end{aligned} \tag{3.6}$$

The off-axis piezoresistive coefficients $\pi'_{\alpha\beta}$ can be related to the 3 unique on-axis coefficients for silicon π_{11}, π_{22}, π_{44}, which are evaluated in the original coordinate system aligned with the principal crystallographic axes. Using tensor transformations, this relationship can be expressed as

$$\pi'_{\alpha\beta} = T_{\alpha\gamma}\pi_{\gamma\delta}T^{-1}_{\delta\beta} \tag{3.7}$$

where

$$[\pi_{ij}] = \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{bmatrix} \tag{3.8}$$

is the on-axis piezoresistive coefficient matrix for silicon, and

$$[T_{\alpha\beta}] = \begin{bmatrix} l_1^2 & m_1^2 & n_1^2 & 2l_1n_1 & 2m_1n_1 & 2l_1m_1 \\ l_2^2 & m_2^2 & n_2^2 & 2l_2n_2 & 2m_2n_2 & 2l_2m_2 \\ l_3^2 & m_3^2 & n_3^2 & 2l_3n_3 & 2m_3n_3 & 2l_3m_3 \\ l_1l_3 & m_1m_3 & n_1n_3 & l_1n_3 + l_3n_1 & m_1n_3 + m_3n_1 & l_1m_3 + l_3m_1 \\ l_2l_3 & m_2m_3 & n_2n_3 & l_2n_3 + l_3n_2 & m_2n_3 + m_3n_2 & l_2m_3 + l_3m_2 \\ l_1l_2 & m_1m_2 & n_1n_2 & l_1n_2 + l_2n_1 & m_1n_2 + m_2n_1 & l_1m_2 + l_2m_1 \end{bmatrix} \tag{3.9}$$

This transformation matrix relates the piezoresistive coefficients in the rotated coordinate system, to those in the crystallographic coordinate system. The direction cosines l_i, m_i, and n_i in eq. (3.9) are given by

$$\begin{bmatrix} l_1 & m_1 & n_1 \\ l_2 & m_2 & n_2 \\ l_3 & m_3 & n_3 \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{bmatrix} = [a_{ij}] \tag{3.10}$$

where

$$a_{ij} = cos\,(x_i', x_j) \tag{3.11}$$

The inverse of the matrix in eq. (3.9) is needed for calculation of the off-axis piezoresistive coefficients in eq. (3.7). It can be evaluated as:

$$[T_{\alpha\beta}]^{-1} = \begin{bmatrix} l_1^2 & l_2^2 & l_3^2 & 2l_1l_3 & 2l_2l_3 & 2l_1l_2 \\ m_1^2 & m_2^2 & m_3^2 & 2m_1m_3 & 2m_2m_3 & 2m_1m_2 \\ n_1^2 & n_2^2 & n_3^2 & 2n_1n_3 & 2n_2n_3 & 2n_1n_2 \\ l_1n_1 & l_2n_2 & l_3n_3 & l_1n_3 + l_3n_1 & l_2n_3 + l_3n_2 & l_1n_2 + l_2n_1 \\ m_1n_1 & m_2n_2 & m_3n_3 & m_1n_3 + m_3n_1 & m_2n_3 + m_3n_2 & m_1n_2 + m_2n_1 \\ l_1m_1 & l_2m_2 & l_3m_3 & l_1m_3 + l_3m_1 & l_2m_3 + l_3m_2 & l_1m_2 + l_2m_1 \end{bmatrix} \quad (3.12)$$

If the arbitrary primed coordinate system coincides with the crystallographic axes, the matrices in eqs. (3.9, 3.12) become the 6 x 6 identity matrix, and eq. (3.7) simplifies to

$$\pi'_{\alpha\beta} = \pi_{\alpha\beta} \quad (3.13)$$

Additionally, when the two coordinate systems are aligned, Equation (3.4) simplifies to

$$\begin{aligned} \frac{\Delta R}{R} =& \left[\pi_{11}\sigma_{11} + \pi_{12}\left(\sigma_{22} + \sigma_{33}\right)\right] l^2 + \left[\pi_{11}\sigma_{22} + \pi_{12}\left(\sigma_{11} + \sigma_{33}\right)\right] m^2 \\ &+ \left[\pi_{11}\sigma_{33} + \pi_{12}\left(\sigma_{11} + \sigma_{22}\right)\right] n^2 + 2\pi_{44}\left[\sigma_{12}lm + \sigma_{13}ln + \sigma_{23}mn\right] \\ &+ \left[\alpha_1 T + \alpha_2 T^2 + \ldots\right] \end{aligned} \quad (3.14)$$

where l, m, and n are the direction cosines of the conductor orientation with respect to the crystallographic axes. Equation (3.14) describes the normalized resistance change of an arbitrarily oriented silicon conductor as a function of all six stress components in the crystallographic coordinate system.

3.2 Piezoresistivity in the (111) Silicon Plane

A generalized schematic of a (111) silicon wafer is shown in Figure 3.2. A wafer plane is defined by the direction normal to its surface. Therefore, a (111) silicon wafer has the [111] crystallographic direction as its normal. The principal unprimed crystallographic axes mentioned previously are not found in the (111) plane. In this plane, the rotated coordinate system has been chosen so that the x'_1 direction is parallel to the wafer flat, and the x'_2 direction is perpendicular to the flat. In order to find resistance changes of a conductor in this plane using eq. (3.4), the direction cosines must be found between the rotated, primed coordinate system of the wafer plane, and the unprimed coordinate system formed by the principal crystallographic axes. The appropriate matrix of direction cosines for the (111) wafer plane can be found to be [46]

$$[a_{ij}] = \begin{bmatrix} \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} & 0 \\ \frac{1}{\sqrt{6}} & \frac{1}{\sqrt{6}} & -\frac{2}{\sqrt{6}} \\ \frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} \end{bmatrix} \tag{3.15}$$

Using these values in eqs. (3.9,3.10, 3.11), the off-axis piezoresistive coefficients found in Equation(3.7) can be calculated. These coefficients can be substituted in eq. (3.4) to produce

$$\begin{aligned} \frac{\Delta R}{R} &= \left[B_1\sigma'_{11} + B_2\sigma'_{22} + B_3\sigma'_{33} + 2\sqrt{2}\,(B_3 - B_2)\,\sigma'_{23}\right] cos^2\phi \\ &+ \left[B_2\sigma'_{11} + B_1\sigma'_{22} + B_3\sigma'_{33} - 2\sqrt{2}\,(B_3 - B_2)\,\sigma'_{23}\right] sin^2\phi \\ &+ \left[2\sqrt{2}\,(B_3 - B_2)\,\sigma'_{13} + (B_1 - B_2)\,\sigma'_{12}\right] sin2\phi \\ &+ \left[\alpha_1 T + \alpha_2 T^2 + \ldots\right] \end{aligned} \tag{3.16}$$

where ϕ is the angle between the x'_1-axis and the conductor orientation. The coefficients B_i (i = 1, 2, 3) are linearly independent constants comprised of a combination of the piezoresistive

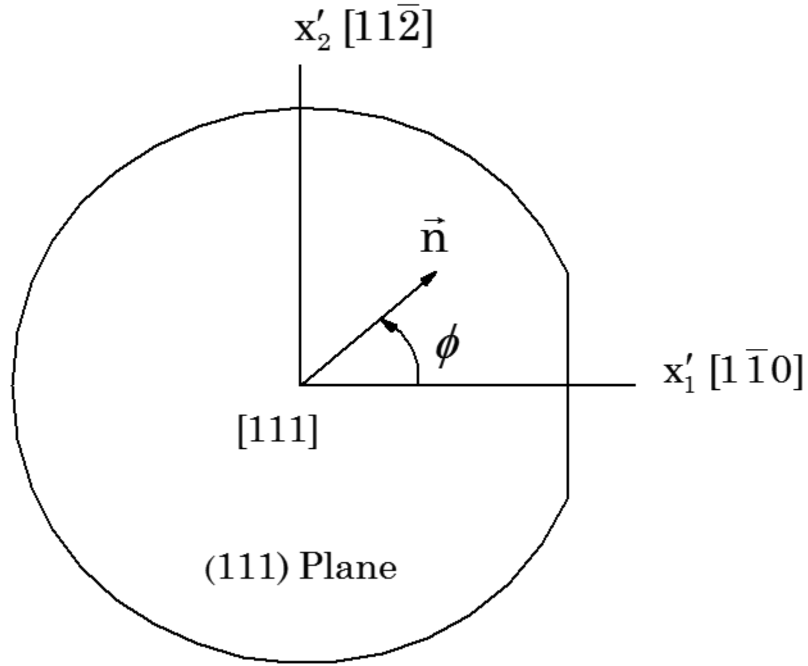


Figure 3.2: (111) Silicon Wafer

coefficients evaluated in the unprimed crystallographic coordinate system, and are expressed as

$$\begin{aligned}
B_1 &= \frac{\pi_{11} + \pi_{12} + \pi_{11}}{2} \\
B_2 &= \frac{\pi_{11} + 5\pi_{12} + \pi_{11}}{6} \\
B_3 &= \frac{\pi_{11} + 2\pi_{12} + \pi_{11}}{3}
\end{aligned} \tag{3.17}$$

Chapter 4

(111) Silicon Test Chips

4.1 Rosette and Test Chip Designs

4.1.1 Optimized Eight-Element Rosette

The eight-element (111) silicon rosette shown in Figure 4.1 has been developed at Auburn University to measure the complete state of stress on the surface of a packaged semiconductor die. The rosette is dual polarity, meaning that it uses both n-type and p-type serpentine silicon sensors. Only three unique resistance change measurements can be made for a group of sensors of one doping type and doping level combination in a single plane [45]. This fact brings about the need for two doping types present in one sensor rosette. It is also noted that only six resistors are required for measurement of the complete state of stress using (111) silicon. The sensors oriented at -45° are not necessary, but aid in making bridge measurement easier and in localizing stress measurement [79]. The complete rosette is comprised of eight elements, four of each doping type oriented at $= 0°$, $\pm 45°$, and $90°$ with respect to the x_1'-axis.

Applying eq. (3.16) to each of the sensors leads to the following equations for the normalized resistance change of each sensor as a function of the stress components:

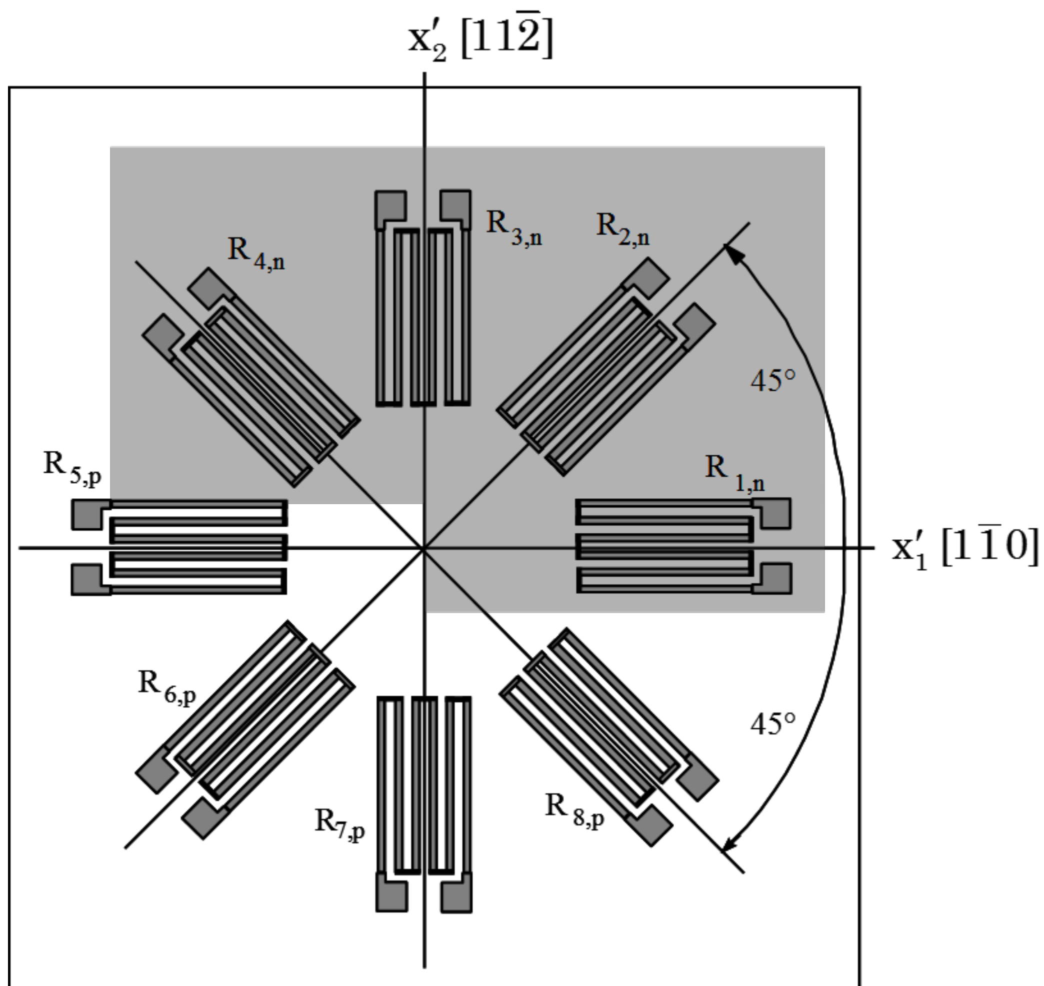


Figure 4.1: Optimized Eight-Element Rosette

$$
\begin{aligned}
\frac{\Delta R_1}{R_1} &= B_1^n \sigma'_{11} + B_2^n \sigma'_{22} + B_3^n \sigma'_{33} + 2\sqrt{2}\left(B_3^n - B_2^n\right)\sigma'_{23} \\
&\quad + \left[\alpha_1^n T + \alpha_2^n T^2 + \ldots\right] \\
\frac{\Delta R_2}{R_2} &= \left(\frac{B_1^n + B_2^n}{2}\right)\left(\sigma'_{11} + \sigma'_{22}\right) + B_3^n \sigma'_{33} + 2\sqrt{2}\left(B_3^n - B_2^n\right)\sigma'_{13} \\
&\quad + \left(B_1^n - B_2^n\right)\sigma'_{12} + \left[\alpha_1^n T + \alpha_2^n T^2 + \ldots\right] \\
\frac{\Delta R_3}{R_3} &= B_2^n \sigma'_{11} + B_1^n \sigma'_{22} + B_3^n \sigma'_{33} - 2\sqrt{2}\left(B_3^n - B_2^n\right)\sigma'_{23} \\
&\quad + \left[\alpha_1^n T + \alpha_2^n T^2 + \ldots\right] \\
\frac{\Delta R_4}{R_4} &= \left(\frac{B_1^n + B_2^n}{2}\right)\left(\sigma'_{11} + \sigma'_{22}\right) + B_3^n \sigma'_{33} - 2\sqrt{2}\left(B_3^n - B_2^n\right)\sigma'_{13} \\
&\quad - \left(B_1^n - B_2^n\right)\sigma'_{12} + \left[\alpha_1^n T + \alpha_2^n T^2 + \ldots\right] \\
\frac{\Delta R_5}{R_5} &= B_1^p \sigma'_{11} + B_2^p \sigma'_{22} + B_3^p \sigma'_{33} + 2\sqrt{2}\left(B_3^p - B_2^p\right)\sigma'_{23} \qquad (4.1) \\
&\quad + \left[\alpha_1^p T + \alpha_2^p T^2 + \ldots\right] \\
\frac{\Delta R_6}{R_6} &= \left(\frac{B_1^p + B_2^p}{2}\right)\left(\sigma'_{11} + \sigma'_{22}\right) + B_3^p \sigma'_{33} + 2\sqrt{2}\left(B_3^p - B_2^p\right)\sigma'_{13} \\
&\quad + \left(B_1^p - B_2^p\right)\sigma'_{12} + \left[\alpha_1^p T + \alpha_2^p T^2 + \ldots\right] \\
\frac{\Delta R_7}{R_7} &= B_2^p \sigma'_{11} + B_1^p \sigma'_{22} + B_3^p \sigma'_{33} - 2\sqrt{2}\left(B_3^p - B_2^p\right)\sigma'_{23} \\
&\quad + \left[\alpha_1^p T + \alpha_2^p T^2 + \ldots\right] \\
\frac{\Delta R_8}{R_8} &= \left(\frac{B_1^p + B_2^p}{2}\right)\left(\sigma'_{11} + \sigma'_{22}\right) + B_3^p \sigma'_{33} - 2\sqrt{2}\left(B_3^p - B_2^p\right)\sigma'_{13} \\
&\quad - \left(B_1^p - B_2^p\right)\sigma'_{12} + \left[\alpha_1^p T + \alpha_2^p T^2 + \ldots\right]
\end{aligned}
$$

Superscripts n and p are used on the combined piezoresistive coefficients, B_i (i =1, 2, 3), to denote n-type and p-type resistors, respectively.

For an arbitrary state of stress, inverting these equations allows the six stress components to be calculated in terms of the measured resistance and temperature changes:

$$
\begin{aligned}
\sigma'_{11} &= \frac{\left(B_3^p - B_2^p\right)\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right] - \left(B_3^n - B_2^n\right)\left[\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right]}{2\left[\left(B_2^p - B_1^p\right)B_3^n + \left(B_1^p - B_3^p\right)B_2^n + \left(B_3^p - B_2^p\right)B_1^n\right]} \\
&+ \frac{B_3^p\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^n T\right] - B_3^n\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^p T\right]}{2\left[\left(B_1^n + B_2^n\right)B_3^p - \left(B_1^p + B_2^p\right)B_3^n\right]} \\
\sigma'_{22} &= -\frac{\left(B_3^p - B_2^p\right)\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right] - \left(B_3^n - B_2^n\right)\left[\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right]}{2\left[\left(B_2^p - B_1^p\right)B_3^n + \left(B_1^p - B_3^p\right)B_2^n + \left(B_3^p - B_2^p\right)B_1^n\right]} \\
&+ \frac{B_3^p\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^n T\right] - B_3^n\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^p T\right]}{2\left[\left(B_1^n + B_2^n\right)B_3^p - \left(B_1^p + B_2^p\right)B_3^n\right]} \\
\sigma'_{33} &= \frac{-\left(B_1^p + B_2^p\right)\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^n T\right] - \left(B_1^n + B_2^n\right)\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^p T\right]}{2\left[\left(B_1^n + B_2^n\right)B_3^p - \left(B_1^p + B_2^p\right)B_3^n\right]} \qquad (4.2) \\
\sigma'_{13} &= \frac{\sqrt{2}}{8}\left[\frac{\left(B_1^p - B_2^p\right)\left[\frac{\Delta R_4}{R_4} - \frac{\Delta R_2}{R_2}\right] - \left(B_1^n - B_2^n\right)\left[\frac{\Delta R_8}{R_8} - \frac{\Delta R_6}{R_6}\right]}{\left(B_2^p - B_1^p\right)B_3^n + \left(B_1^p - B_3^p\right)B_2^n + \left(B_3^p - B_2^p\right)B_1^n}\right] \\
\sigma'_{23} &= \frac{\sqrt{2}}{8}\left[\frac{-\left(B_1^p - B_2^p\right)\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right] + \left(B_1^n - B_2^n\right)\left[\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right]}{\left(B_2^p - B_1^p\right)B_3^n + \left(B_1^p - B_3^p\right)B_2^n + \left(B_3^p - B_2^p\right)B_1^n}\right] \\
\sigma'_{12} &= \frac{-\left(B_3^p - B_2^p\right)\left[\frac{\Delta R_4}{R_4} - \frac{\Delta R_2}{R_2}\right] + \left(B_3^n - B_2^n\right)\left[\frac{\Delta R_8}{R_8} - \frac{\Delta R_6}{R_6}\right]}{2\left[\left(B_2^p - B_1^p\right)B_3^n + \left(B_1^p - B_3^p\right)B_2^n + \left(B_3^p - B_2^p\right)B_1^n\right]}
\end{aligned}
$$

In order to calculate the normal stress components σ'_{11}, σ'_{22}, and σ'_{33}, the normalized resistance changes and the temperature change T of the resistors must be measured. The piezoresistive coefficients and temperature coefficients of resistance for each doping type must also be known. Calibration of the piezoresistive coefficients and of the Temperature Coefficients of Resistance (TCR) will be discussed later in this chapter.

Upon examination of eqs. (4.2), it can be seen that the shear stresses σ'_{12}, σ'_{13}, and σ'_{23} can be evaluated from only the resistance change measurements, and that it is not necessary to know the temperature change T. Such measurements are referred to as being temperature

compensated. In addition to the three shear stresses, another temperature compensated stress quantity can be determined by subtracting the expressions for the in-plane normal stresses and in eqs. (4.2):

$$\sigma'_{11} - \sigma'_{22} = \frac{\left(B_3^p - B_2^p\right)\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right] - \left(B_3^n - B_2^n\right)\left[\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right]}{\left[\left(B_2^p - B_1^p\right)B_3^n + \left(B_1^p - B_3^p\right)B_2^n + \left(B_3^p - B_2^p\right)B_1^n\right]} \tag{4.3}$$

In all cases where temperature compensation occurs, it has been assumed that the TCRs for sensors of the same doping type are well matched.

The use of temperature compensated stress quantities has been encouraged by Jaeger, et al. [52], due to the difficulties in measuring temperature changes accurately over any extended period of time. These authors further showed that the errors in the calculated stresses could be substantial given a temperature measurement error of as little as 0.25 °C.

4.1.2 Area Array Stress Test Chip

The (111) silicon test chips utilized in this work contained piezoresistive sensor rosettes that were capable of measuring the complete state of stress at the die surface. The test chips were 20 x 20 x .625 mm in size, and contained an area array of 3600 SAC387 lead free solder bumps on a 300 micron pitch. A photograph of one of the test chips is shown in Figure 4.2. Each of the 20 x 20 mm area array stress test chips used in this work contained 16 (4 x 4 array) of identical 5 x 5 mm regions as shown in Figure 4.3.

The area array flip chip test chip wafers were obtained by redistributing an existing set of wirebond stress test chip wafers, and then subsequently bumping the topside metal layers of the redistributed wafers. The basic 5 x 5 mm wirebond stress test chip design (JSE WB200) found on the original wafers is shown in Figure 4.4. These test chips were designed specifically for wire bonding applications with 4 x 4 mil (100 x 100 μm) perimeter pads on a 5 mil (125 μm) pitch. Each WB200 test chip contains 16 optimized eight-element resistor rosettes for stress characterization, diodes for temperature measurement, a sub-surface heater across the full die area, and a fuse ID. All of the measurement functionality of the original test

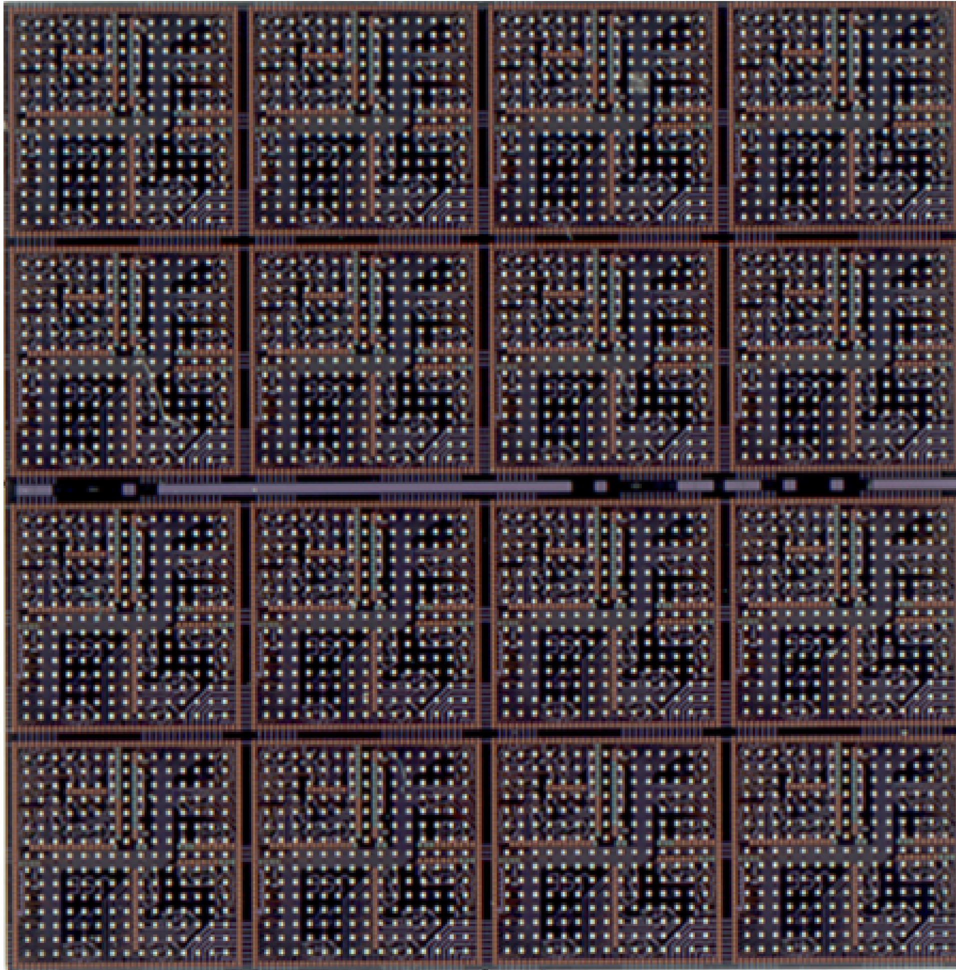


Figure 4.2: Area Array Flip Chip Stress Test Chip [20 x 20 mm, 3600 I/O]

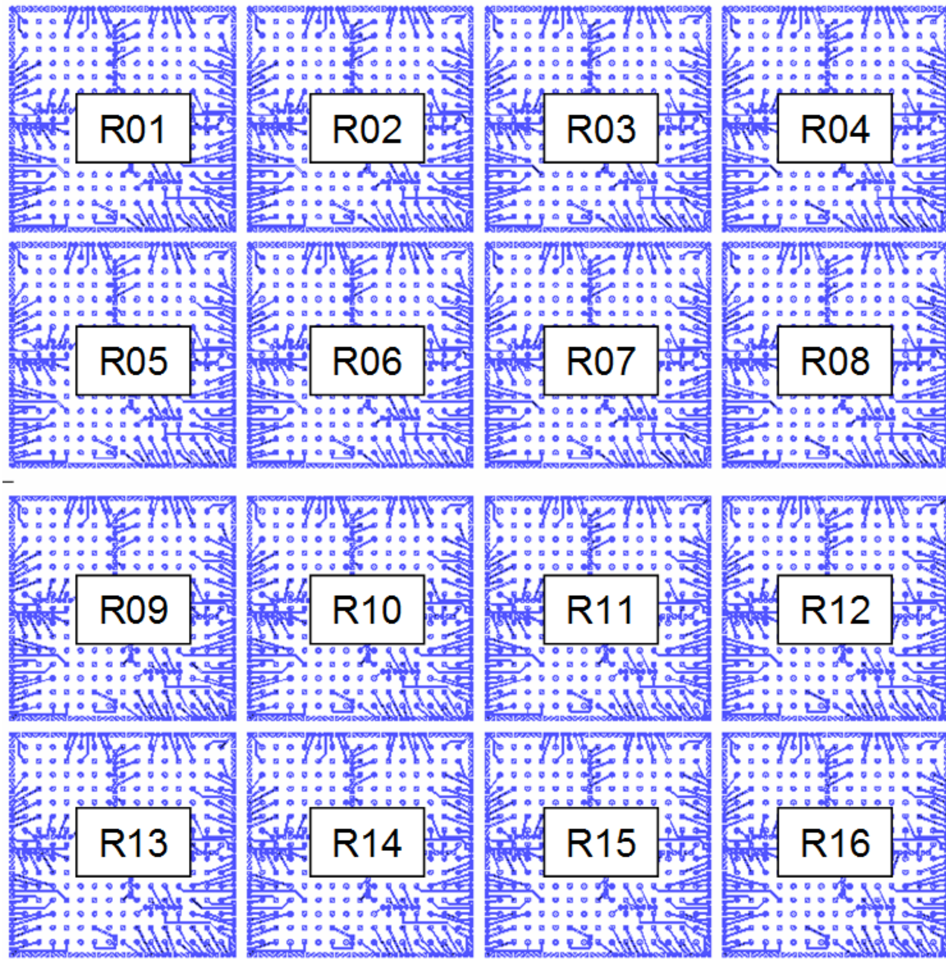


Figure 4.3: Array of Identical 5 x 5 mm Regions

chip design is routed to the perimeter pads, and the redistribution procedure transferred this to an area array flip chip bond pad configuration. The details of the redistribution routing and solder bump placement over the same 5 x 5 mm region are shown in Figure 4.4. Figure 4.6 illustrates the 20 x 20 mm test chip before redistribution, and Figure 4.7 shows the redistribution metal layer that was added as well as the solder bump pad locations.

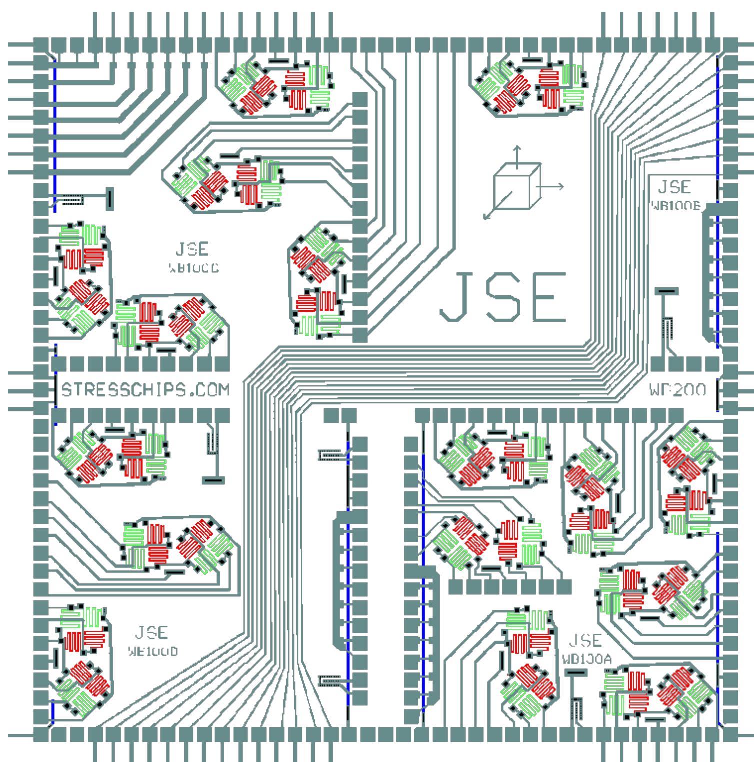


Figure 4.4: Wirebond Stress Test Chip (JSE WB200)

The eight stress sensor rosette elements are routed to the die bond pads in a manner that allows them to be configured as four two-element half-bridges in order to simplify the resistance change measurements. A fully ion-implanted bipolar process has been used in the original semiconductor device fabrication to balance the n- and p-type sheet resistances and resistor values, while maintaining high sensitivity to stress. Figure 4.8 illustrates an optical microscopy photograph of some sensor rosette sites and neighboring solder balls (black circles) on one of the final test chips. Figure 4.9 shows a close-up photograph of one of the eight-element sensor rosettes (no solder balls). It can be seen that the resistor

sensors in this work are fairly large compared to the spacing of the solder balls. Thus, averaging of the stress distributions occurs over the rosette area and the sensors in this work will not be able to resolve any stress gradients that exist between solder balls. Ueta and Miura [179, 180] have performed some initial measurements of this effect by placing 5 sensors elements between a pair of solder balls at the corner of a flip chip die.

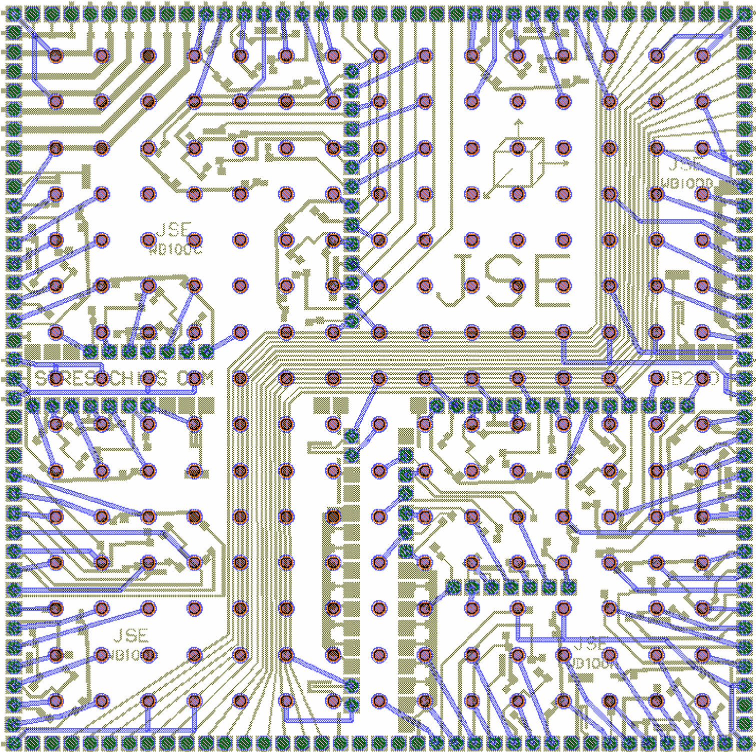


Figure 4.5: Redistribution Pattern on each 5 x 5 mm Region

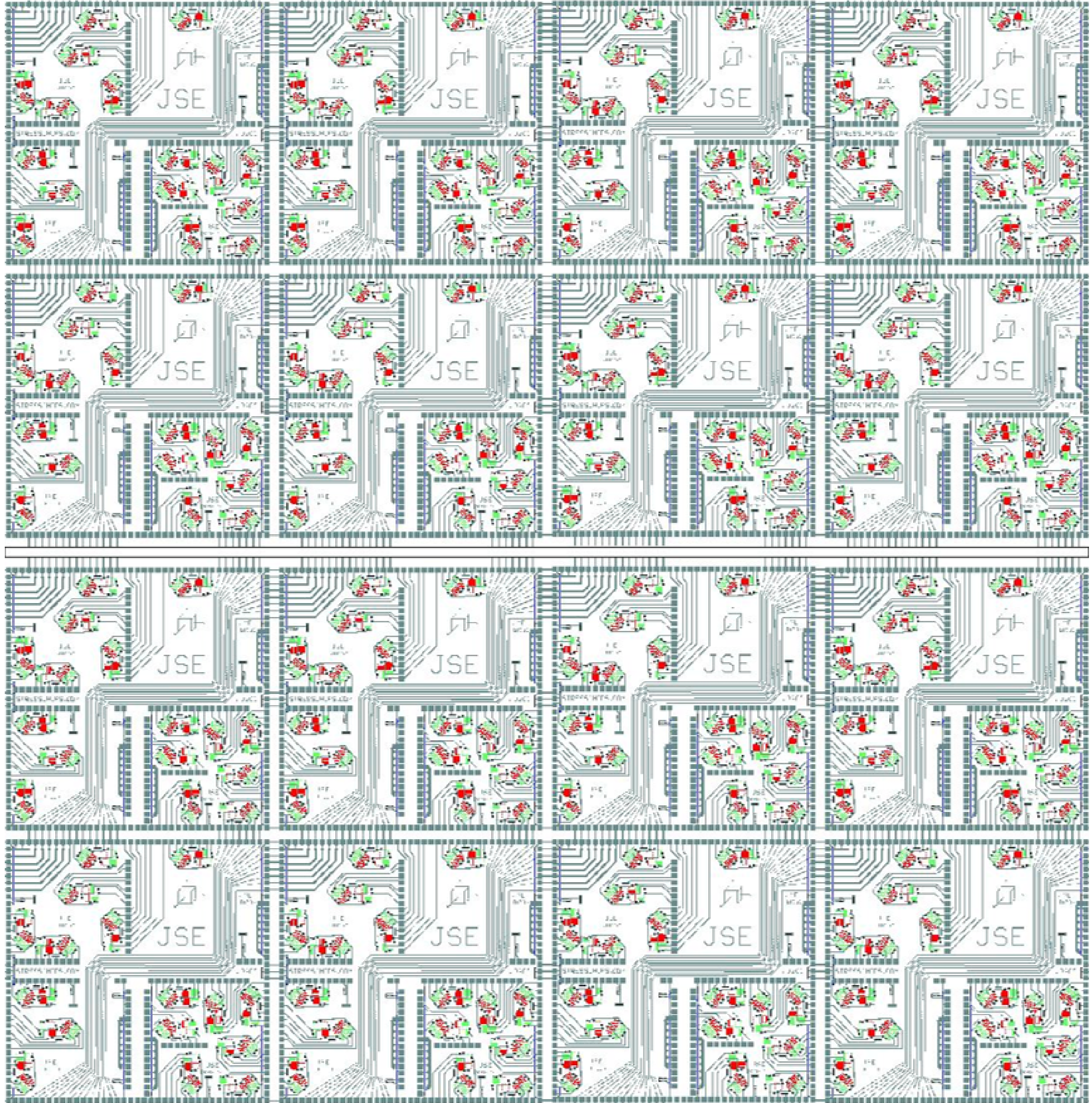


Figure 4.6: 20 x 20 mm Test Chip Before Redistribution

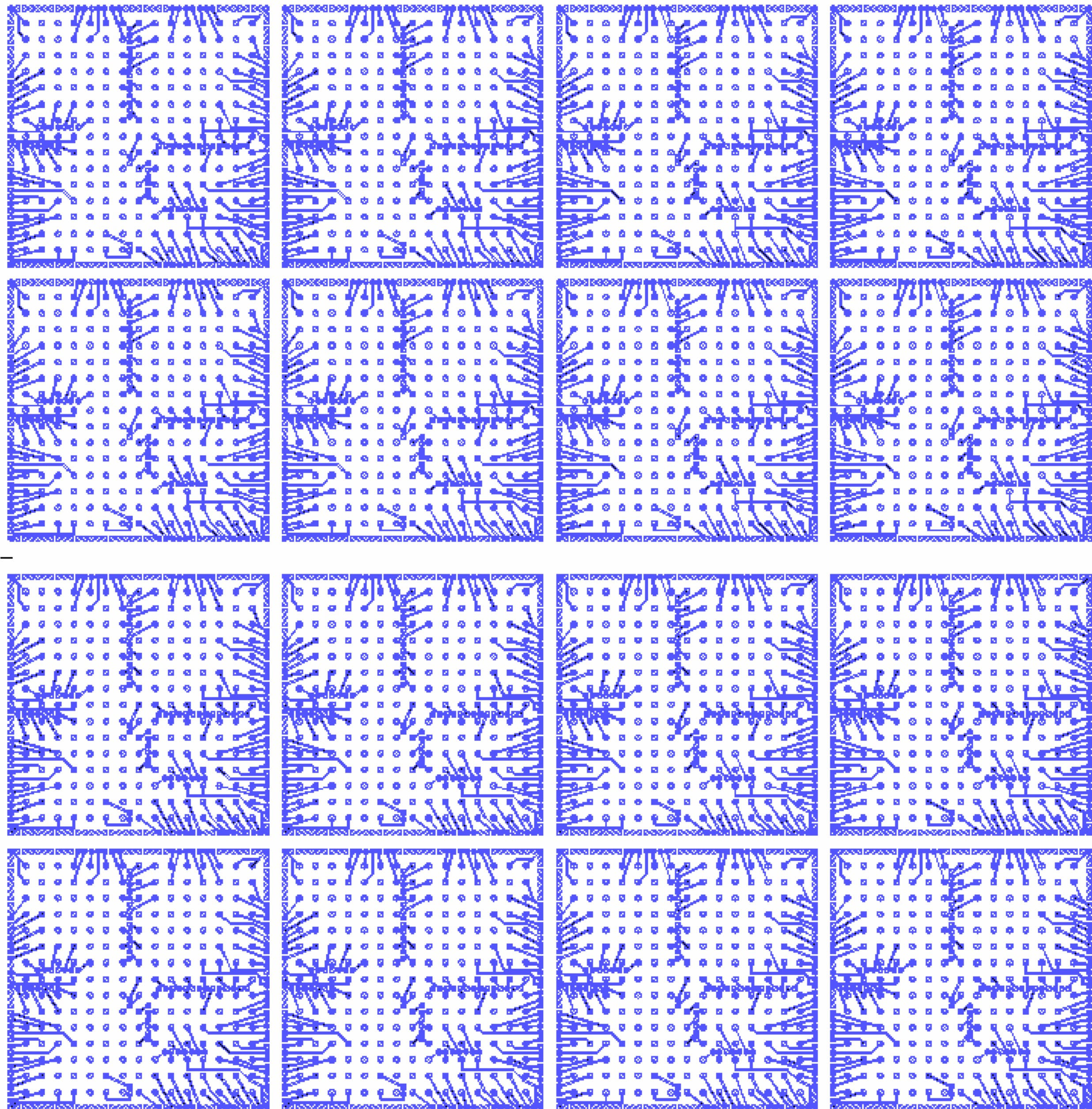


Figure 4.7: Redistribution Pattern on each 5 x 5 mm Region

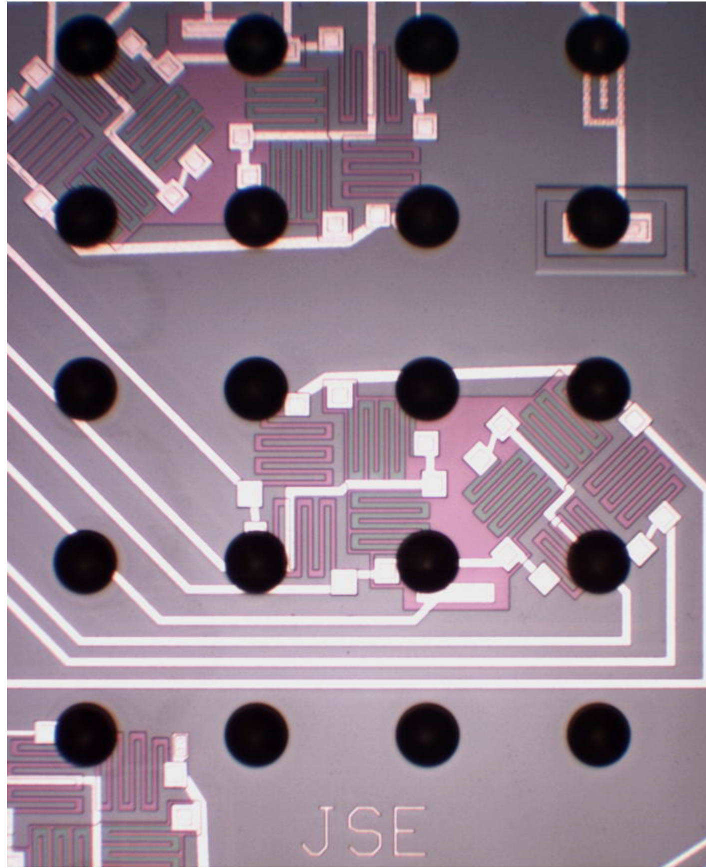


Figure 4.8: Photograph of Sensor Rosettes

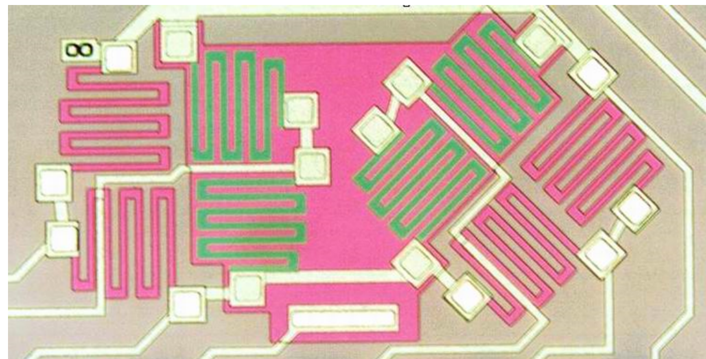


Figure 4.9: Close-Up Photograph of a Fabricated Rosette

4.2 Test Chip Calibration

4.2.1 Introduction

As noted earlier, the combined piezoresistive constants B_i (i = 1, 2, 3) must be determined by a calibration procedure before the sensors can be used for measurement. To calibrate the six parameters, three for each doping type, both uniaxial and hydrostatic pressure tests are needed.

4.2.2 Four-Point Bending Calibration

The most common configuration for loading the device surface of a silicon test chip in uniaxial tension is four-point bending as shown in Figure 4.8 [46, 48]. A silicon wafer is cut into strips to generate the silicon beams. For the geometry shown in Figure 4.8, a uniaxial tensile state of stress is applied to the top surface of the beam given by:

$$\sigma = \frac{3F\,(L-d)}{t^2 h} \tag{4.4}$$

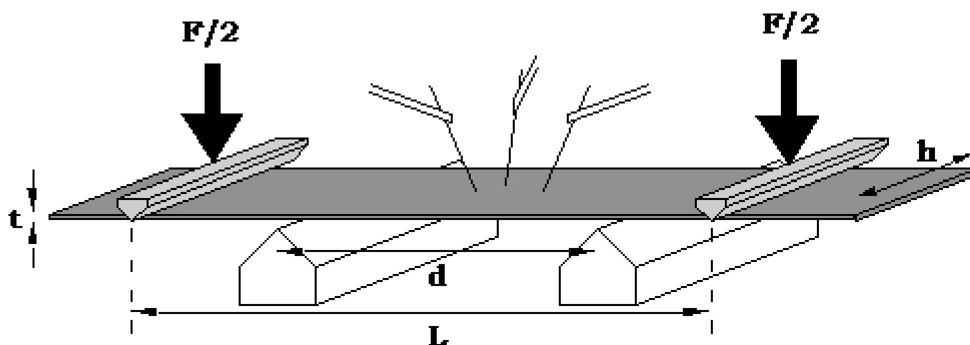


Figure 4.10: Four-Point Bending Geometry

When the wafer strips are sliced perpendicular to the wafer flat so that the length of the beam coincides exactly with the x_1' direction of the wafer, the applied stress is by definition σ_{11}'. Using eq. (4.1), application of a known stress $\sigma = \sigma_{11}'$ leads to the following resistance changes in the 0-90° oriented sensors:

$$
\begin{aligned}
\frac{\Delta R_1}{R_1} &= B_1^n \sigma + \alpha_1^n T \\
\frac{\Delta R_3}{R_3} &= B_2^n \sigma + \alpha_1^n T \\
\frac{\Delta R_5}{R_5} &= B_1^p \sigma + \alpha_1^p T \\
\frac{\Delta R_7}{R_7} &= B_2^p \sigma + \alpha_1^p T
\end{aligned}
\tag{4.5}
$$

Therefore, the combined piezoresistive constants B_1^p, B_2^p, B_1^n, B_2^n can be determined by applying uniaxial stress to wafer strip in a temperature controlled environment ($T = 0$), and measuring the resulting resistance changes of the sensor rosettes.

As part of this study, strips were sliced along the x_1'-axis from the JSE-WB wafers. The strips measured 0.2 x 6.0 inches, and were stressed in the four-point bending fixture shown in Figure 4.11. The average piezoresistive coefficients B_1^p, B_2^p, B_1^n, B_2^n are shown in Table 4.1. A complete presentation of the calibration data is contained in reference [181].

Table 4.1: Average Piezoresistive Coefficient Values and Standard Deviations (1/TPa)

B_1^p	B_2^p	B_3^p	B_1^n	B_2^n	B_3^n
368(12)	-92(7)	-452	-131(11)	91(16)	-76

4.2.3 Hydrostatic Calibration and TCR Measurement

As discussed above, the piezoresistive coefficients B_1 and B_2 were calibrated by uniaxial testing using the four-point bending method. The third combined piezoresistive coefficient, B_3, was calibrated by applying hydrostatic pressure to a silicon chip. Under the application of hydrostatic state of pressure ($\sigma_{11}' = \sigma_{22}' = \sigma_{33}' = -p$), eq. (4.1) can be used to show that the normalized resistance change on any sensor can be written in terms of piezoresistive coefficients and temperature change as:

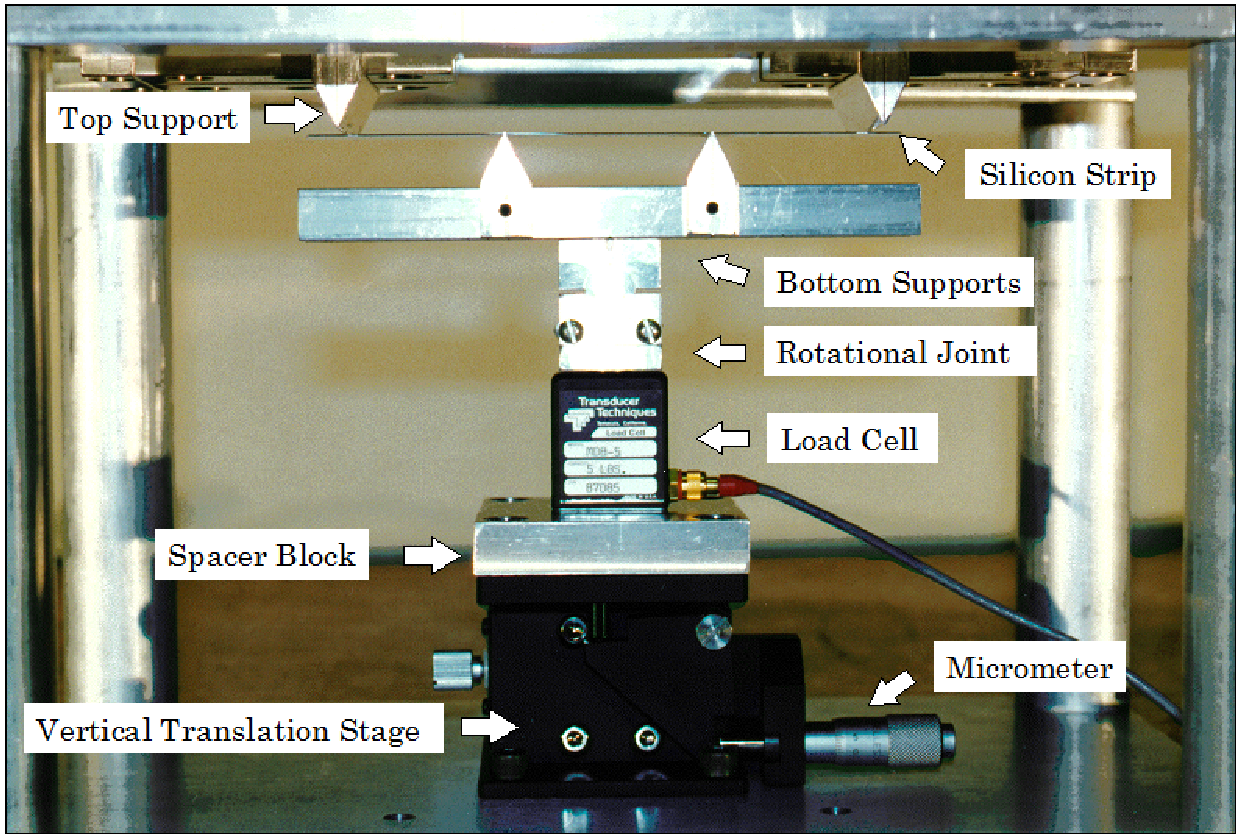


Figure 4.11: Four-Point Bending Fixture

$$\frac{\Delta R}{R} = (B_1 + B_2 + B_3)\, p + \alpha_1 T = -\left(\pi_{11} + 2\pi_{12}\right) p + \alpha_1 T = \pi_p p + \alpha_1 T \tag{4.6}$$

where π_p is the pressure coefficient defined by:

$$\pi_p = (B_1 + B_2 + B_3) = -\left(\pi_{11} + 2\pi_{12}\right) \tag{4.7}$$

and the normalized resistance change is

$$\frac{\Delta R}{R} = \frac{R\,(\sigma, T) - R\,(0,0)}{(0,0)} \tag{4.8}$$

Here, $R\,(\sigma, T)$ is the resistance measured during application of stress, and $R(0,0)$ is the resistance of the sensor in an unstressed condition. The pressure coefficient π_p can be obtained by applying hydrostatic pressure to a sensor and simultaneously measuring the resulting resistance and temperature changes.

For hydrostatic calibration, the high capacity pressure vessel shown in Figure 4.12 was employed to test several WB100 (2.5 x 2.5 mm) die. Each die was used in conjunction with a specially designed hydrostatic test Printed Circuit Board (PCB), as shown in Figure 4.13. A small dot of adhesive is placed on the PCB in a position where one corner of the WB100 chip would rest. The adhesive dot serves a dual purpose. First, it raises the chip off the PCB, allowing fluid to reach, and therefore apply pressure to every surface of the die. Second, the dot gives stability to the chip while it is wire-bonded to the PCB. After the adhesive dot is applied, the chip is set in place, and the assembly is cured, per the adhesive instructions. A bonded WB100 die on a hydrostatic PCB is shown in Figure 4.14. In this case, the glue dot is located in the lower left hand corner.

Before pressurizing the test die, TCR measurements are made. Equation (4.6) shows the dependence on temperature during hydrostatic measurements. It has previously been observed that the upper range of pressure applied in hydrostatic testing causes a temperature change of 0.8 °C [55]. Therefore, before the pressure coefficient π_p can be accurately

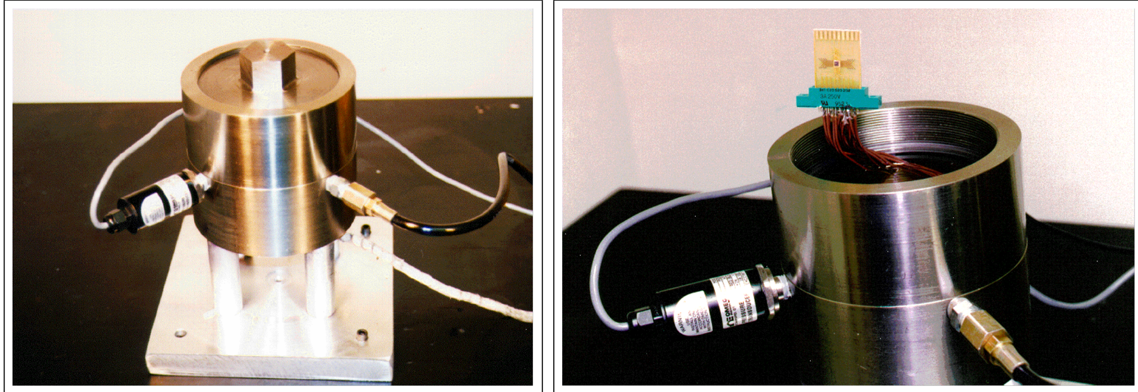


Figure 4.12: Hydrostatic Pressure Vessel

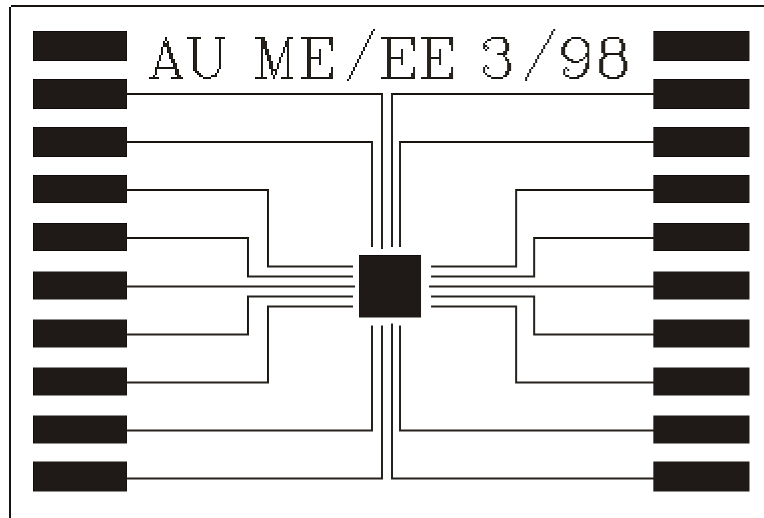


Figure 4.13: Schematic of Hydrostatic PCB

evaluated, the temperature coefficient of resistance α_1 must also be measured. TCR measurements must be made on sensors when they are stress free, so that the resistance change is solely due to temperature effects:

$$\frac{\Delta R}{R} = \alpha_1 T \tag{4.9}$$

The corner bonded chip, shown in Figure 4.14, satisfies the stress free requirement. The chips were placed in an environmental chamber and electrically connected to a data acquisition system. LabView software was used to control the chamber as well as measure temperature and resistance. Once electrically connected and in the chamber, the software lowered the temperature several degrees below room temperature, and then raised the temperature incrementally to well above room temperature while measuring resistance and temperature. Typical TCR data are shown in Figure 4.15. The slopes of the resistance change versus temperature change plots are the desired TCR = α_1 values.

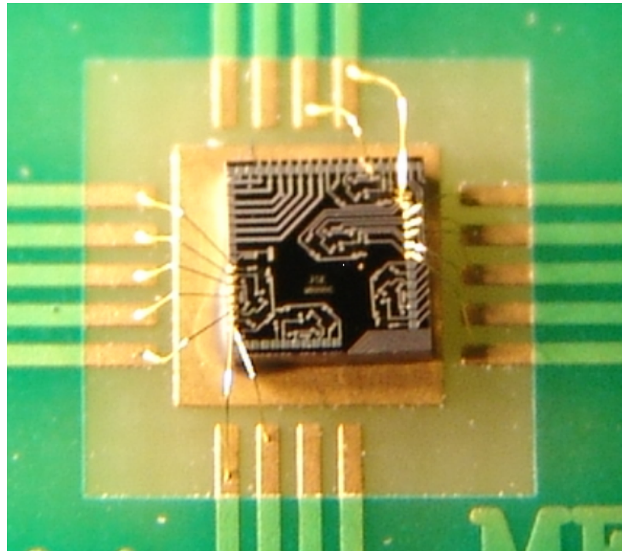
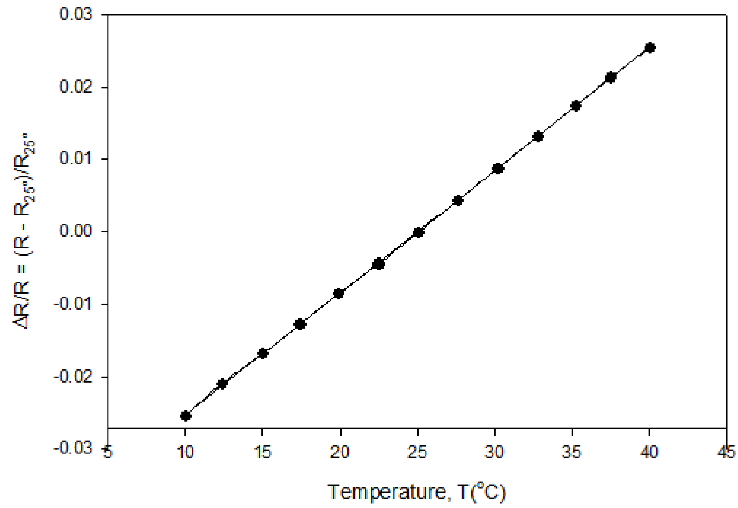


Figure 4.14: Wire-Bonded WB100 Die for TCR and Hydrostatic Tests

When TCR measurements were completed for each sensor, the packages were placed in the pressure vessel shown in Figure 4.12. This configuration was developed by Kang, et al. [47, 54]. The complete hydrostatic setup is shown in Figure 4.16. After placing



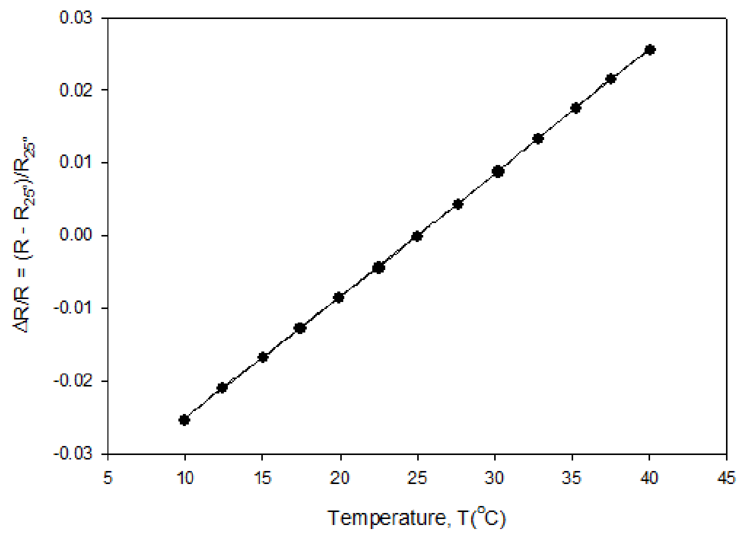


Figure 4.15: Typical TCR Data

the bonded test die in the pressure vessel, the vessel was sealed. A Teflon gasket ensured that the liquid in the vessel did not leak and pressure was retained. Pressure was then applied using a mechanical hand pump. The resistance changes of all sensors were then recorded as well as the fluid temperature using a data acquisition system and LabView software. Typical hydrostatic data are shown in Figure 4.17. The top graph shows the raw resistance change versus pressure data as well as the calculated contribution due to temperature change. The difference of these two effects is plotted in the bottom graph, and represents only the contribution of pressure on the resistance change of the sensors. The slope of the bottom graph is the desired pressure coefficient, which can be used to calculate coefficient B_3 using eq. (4.7). Average values for coefficients B_3^p and B_3^n are given in Table 4.1. Detailed hydrostatic calibration data are presented in reference [181]

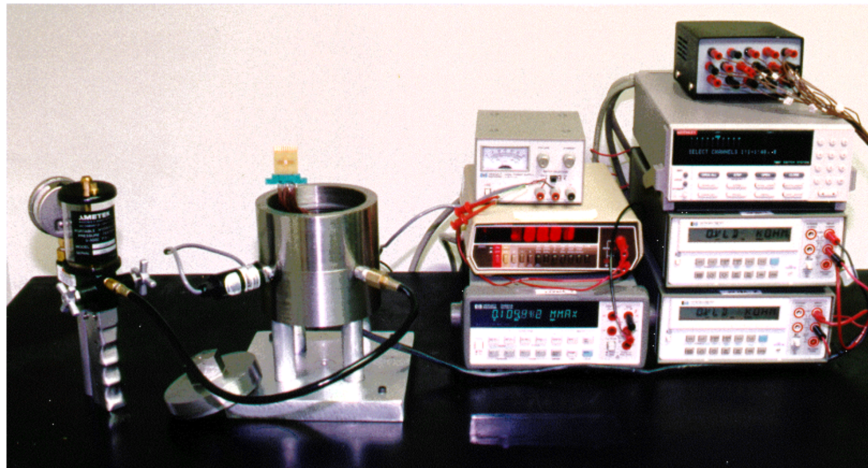


Figure 4.16: Hydrostatic Test Setup

4.3 Resistance Measurement Procedure

4.3.1 Introduction

The (111) silicon test chips used in this study were fabricated using six inch wafers and a bipolar process. The wafers were passivated using silicon nitride, and then redistributed and solder bumped. The resistances of sensors on each 20 x 20 mm test chip were characterized at

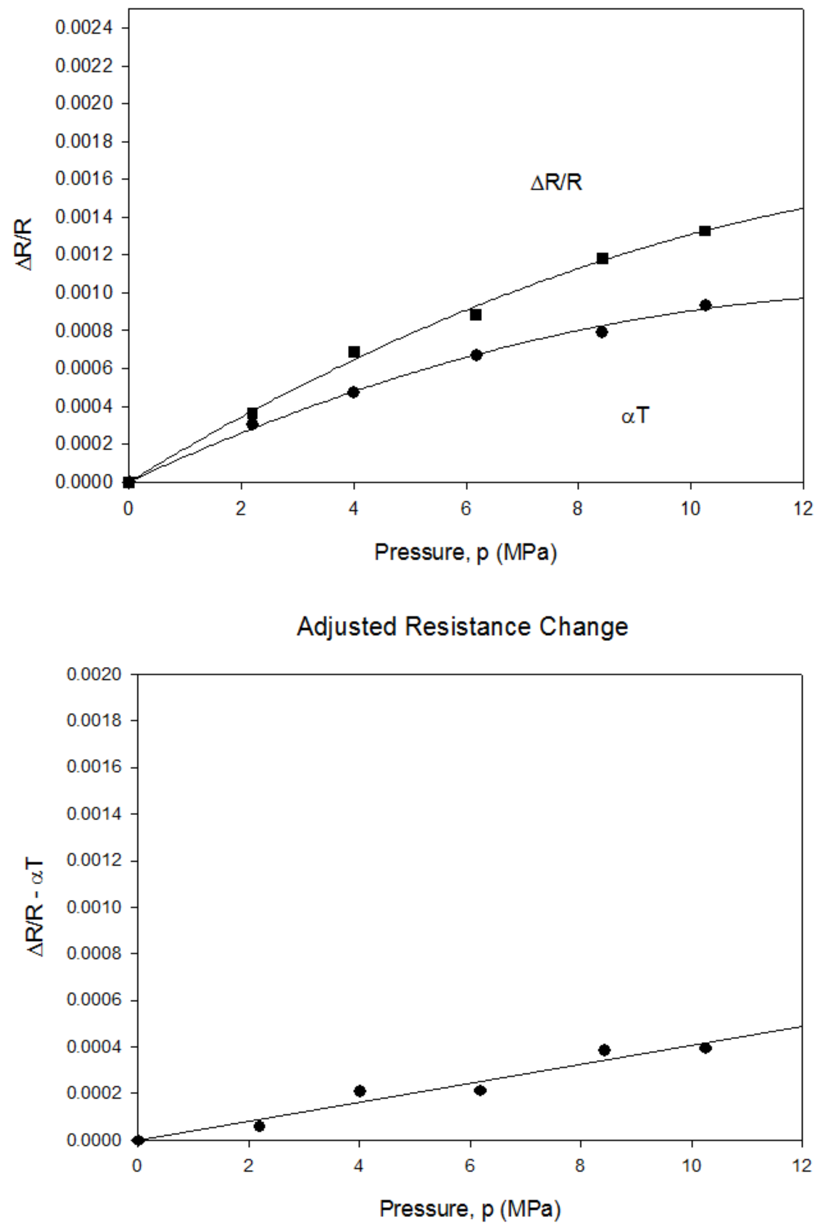


Figure 4.17: Typical Hydrostatic Test Results

several different points including as bare die, and after various packaging steps including die attachment, underfill application, and lid attachment. The hardware and software used to make resistance measurements were designed by several previous Auburn University students including Zou [66], Rahim [98, 182], and H. Abdel-Hady. The utilized methods are briefly discussed below.

4.3.2 Resistance Measurements

The Test Chip Software utilizes GPIB interface technology to control the data acquisition system used for resistance measurement of sensor rosettes. In this study, initial resistance measurements were made at the chip level by probing, and subsequent measurements were made by inserting the packaged die into a test socket as discussed in the next chapter.

4.3.3 Test Measurement Equipment

The following is a list of equipment used for test measurement, as well as a description of how each item was used.

- Computer

  A PC-based computer and a custom National Instruments LabView software program were used to control the data acquisition process. A logic chart and the program interface are shown in Figures 4.18 and 4.19, respectively.

- Keithley 7002 Switch System

  Upon prompting from the control program, the switch turns on or off multiple channels in order to measure the resistance of successive resistors. Nine scanner cards were required for measurement of all of the devices on the test chip in this work.

- HP Multimeter #1

  This multimeter measures current through a resistor.

- Power Supply

  During measurement of sensors, the power supply provides voltage to the measured resistors, and also provides bias in the circuit to prevent current leakage. For ease of resistance measurement, the voltage used is 1V. Figure 4.20 illustrates the proper biasing on n-type and p-type resistors.

- HP Multimeter #2

  This multimeter measures the exact voltage across each resistor. A side advantage of using a second multimeter is that by comparing this voltage to the bias voltage, one can check the circuit. The voltage measured by this meter is used in the calculation of resistance.

- HP Multimeter #3

  This meter measures the resistance value from a resistance thermometer, otherwise referred to as a thermistor. The thermistor is placed on the die to measure temperature changes needed for stress and TCR measurements.

- Delta Design 9010 Environmental Chamber

  As with the other equipment, the chamber is controlled through the Test Chip Software. During TCR calibration experiments, it is used to expose the chips to a range of temperatures in order to measure resistance over that range and calculate TCR. The chamber is also used to submit assembled packages to various temperature changes while measuring the sensor resistances.

- Accessories

  For TCR measurements, two edge connectors were used to connect the PCB shown in Figure 4.13 to the data acquisition system electronically. For all other measurements, a special socket attached to a test board was used to electrically connect to the packages test chips. A package clamp was developed to secure the packages and ensure proper electrical contact. This arrangement is discussed in detail in the following chapter.

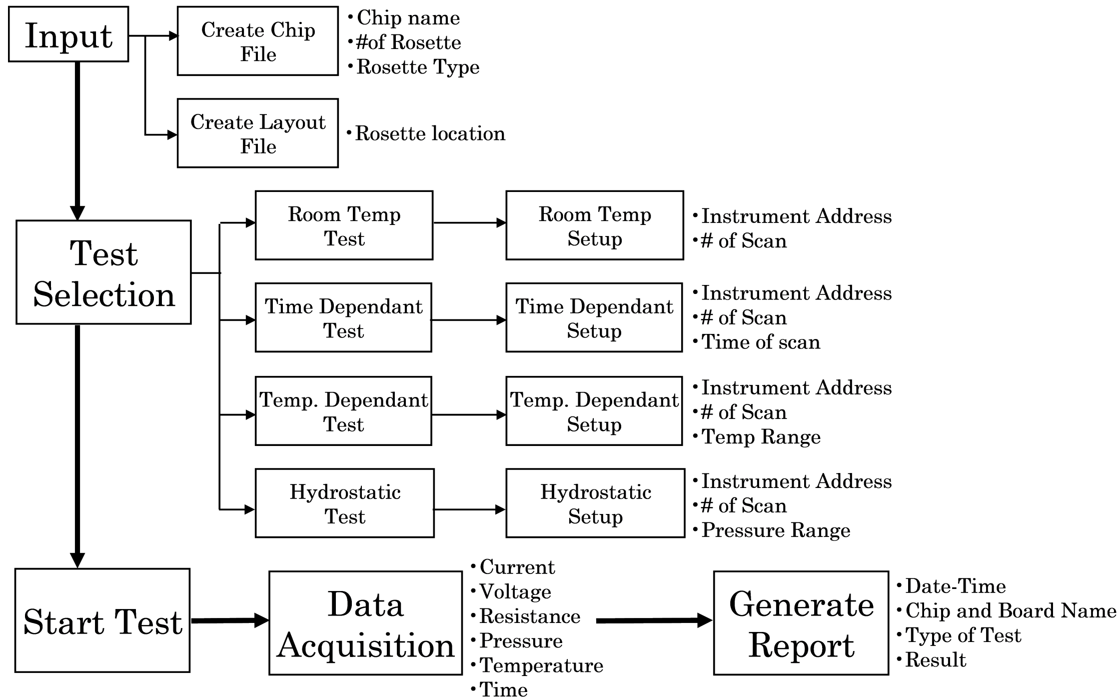


Figure 4.18: Test Chip Software Logic

As discussed earlier, each rosette has eight sensors, four of each doping type. Figure 4.21 shows the two unique wiring configurations of sensor rosettes used in the test chip. The sensors are at angles of 0°, 90°,+45°, and -45° from the x_1-direction. The resistors are denoted P1 (0°), P2 (90°), P3 (+45°), P4 (-45°), N1 (0°), N2 (90°), N3 (+45°), and N4 (-45°). Analogous sensors in the so-called Type 1 (horizontal) and Type 2 (vertical) rosettes are at different orientations. When comparing the two configurations, the orientation of a particular rosette element will switch from 0° to 90°, or from +45° to -45°.

Using the resistor orientations defined above, Figure 4.22 shows a wiring schematic for each type of rosette. The numbers 1, 2, . . . ,7 refer to the bond pad locations in the circuit. A voltage of 1 volt is applied across pads 3 and 7. In Figure 4.22, the methods utilized for measuring the resistances of sensor P1 in a Type 1 (horizontal) rosette and sensor P2 in a Type 2 (vertical) rosette are given. Referring to Figure 4.21, the multimeter (ammeter) serves as a shunt to prevent current from entering the lower sensor. Thus, the resistance of the upper sensor is simply the applied voltage of 1 V divided by the measured current.

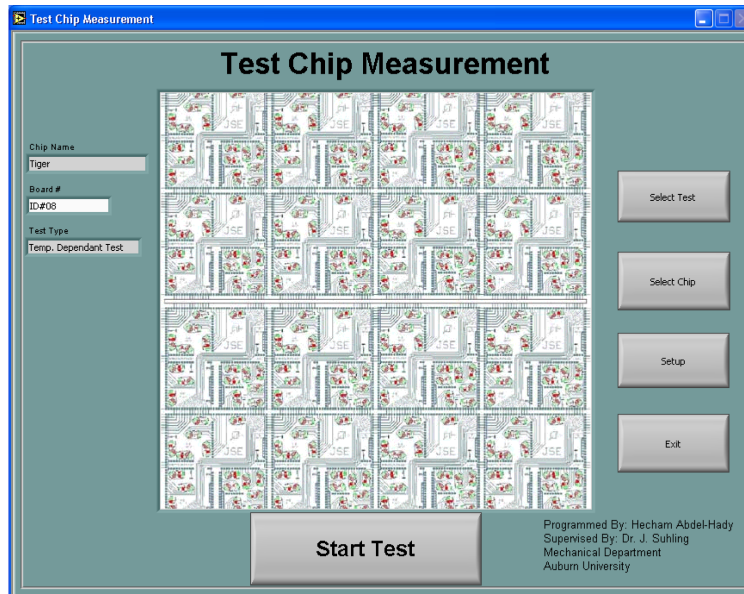


Figure 4.19: Test Chip Measurement Software Interface

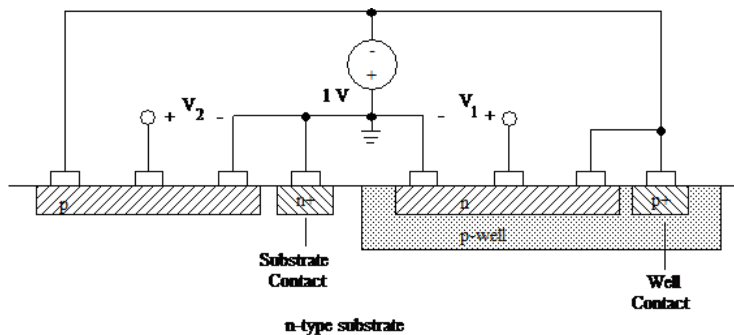
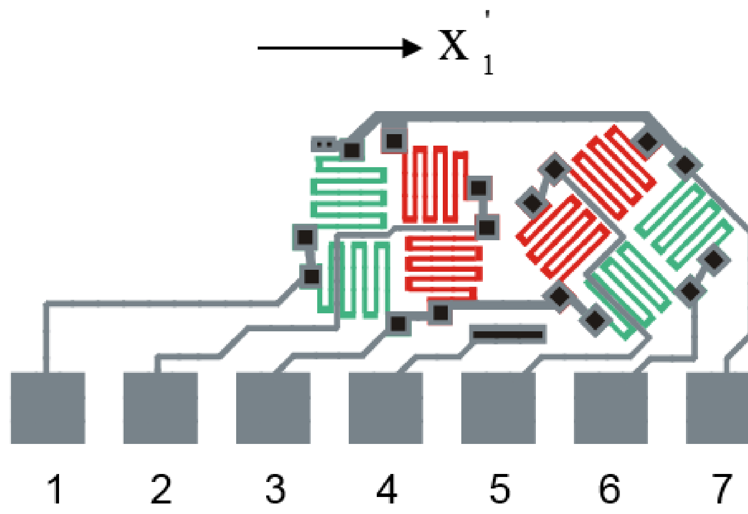
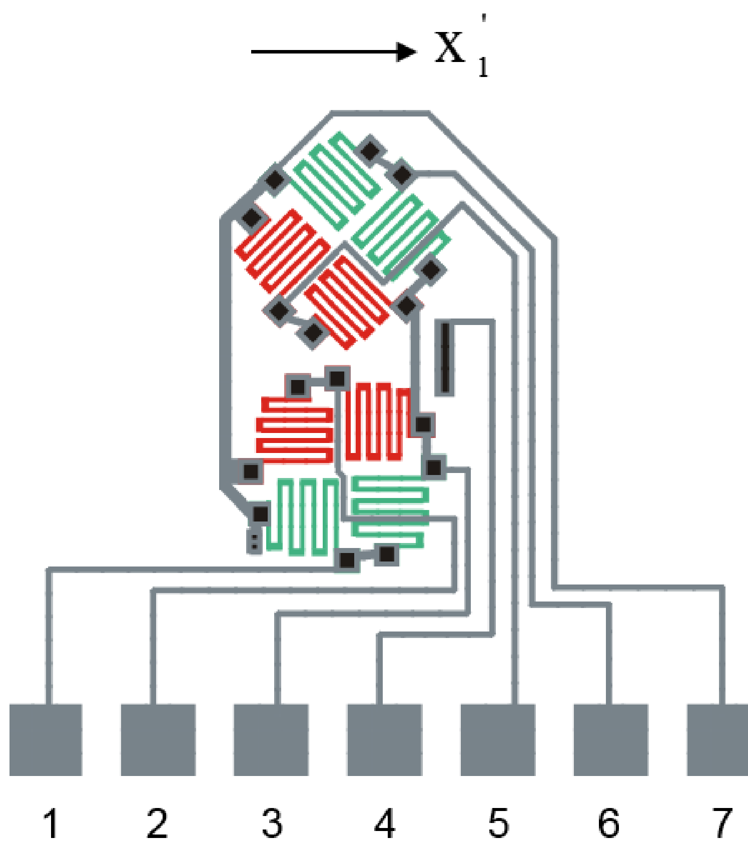


Figure 4.20: Proper Biasing of Sensors

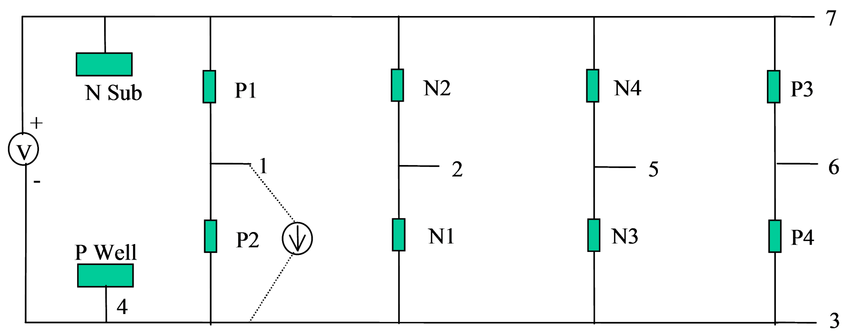


(a) Rosette Type 1

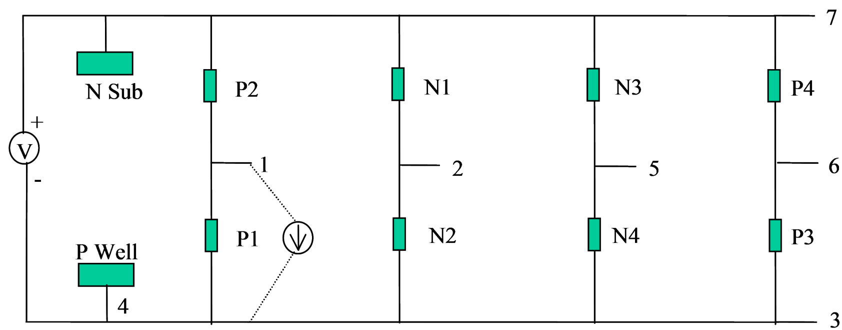


(b) Rosette Type 2

Figure 4.21: Rosette Types 1 and 2



Wiring to Evaluate Sensor P1 in a Horizontal (Type 1) Rosette



Wiring to Evaluate Sensor P2 in a Vertical (Type 2) Rosette

Figure 4.22: Typical Wiring Diagram of Sensors used in JSE-WB Test Chips

The Keithley switch system is used to sequentially access various sensors on the test chip. This system uses interchangeable cards to connect to various devices. In this work, Keithley 7011S screw terminal cards were used to connect the wires from the test board and socket to the measurement equipment. Each scanner card has four banks, and each bank can measure one sensor rosette. Table (4.2) shows the connections between bonding pads, shown in Figure 4.21, and channels of the scanner card.

Table 4.2: Bonding Pad and Scanner Card Connections

Pad Number	Channel Status	
	High	Low
7	1	
1	2	3
2	5	6
3, 4		4
5	7	8
6	9	10

As shown in Figure 4.22, the 8 sensors in a rosette are configured as the parallel connection of four two-element half bridges. In this particular work, the individual resistor changes were measured directly utilizing the techniques shown in Figures 4.23 and 4.24, and as described above and shown in Figure 4.22. For the case in Figure 4.23, an ammeter is used to force the current in upper resistor R_U to bypass lower resistor R_L and flow through the ammeter. The ammeter must force the voltage across R_L to be zero and should be implemented using a high quality digital multimeter or an electrometer (such as the Keithley 6512). The circuit in Figure 4.24 functions in a similar manner. In this case the ammeter forces current in resistor R_U to be zero, and the measured current is due to resistor R_L acting alone.

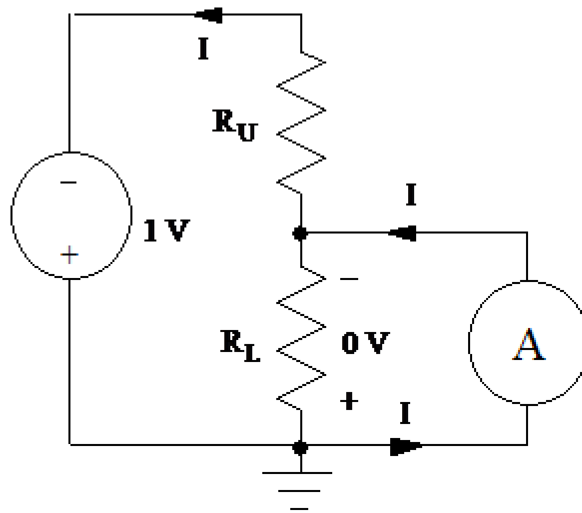


Figure 4.23: Bias for Resistance Measurements, Upper Arm of Half Bridge

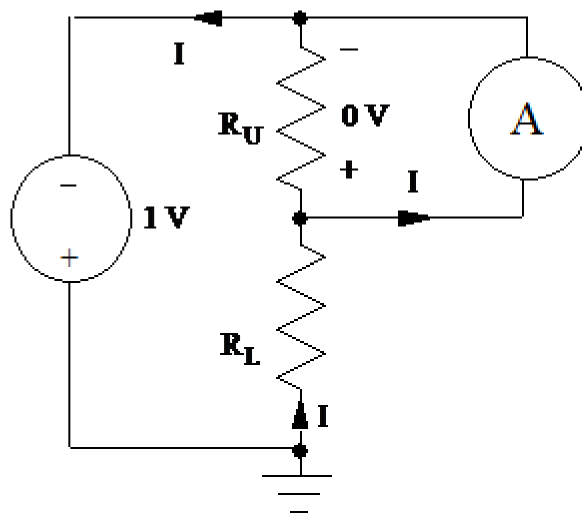


Figure 4.24: Bias for Resistance Measurements, Lower Arm of Half Bridge

Chapter 5

Die Stresses Due to Assembly

5.1 CLGA Package and Assembly Procedure

A typical microprocessor used in server and high end compute applications involves a complex set of materials, geometries, and loadings that affect the actual chip. A schematic of a typical configuration is shown in Figure 5.1. As the purpose of this study was to determine the effects of assembly and use on device side die stresses, a sequential approach was used in the measurement of the samples. First, the stresses due to each step of the assembly of the so called Ceramic Land Grid Array (CLGA) were carefully characterized. The respective assembly steps are shown in Figure 5.2, and include the attachment of the area array flip chip test die to the CLGA substrate, dispense and cure of a first level underfill, and the addition of a first level Thermal Interface Material (TIM1) and metallic lid. A total of 40 of the 20 x 20 mm flip chip stress test chips were assembled onto CLGA substrates. Schematics of cross sectional views of each assembly level are shown in Figure 5.3.

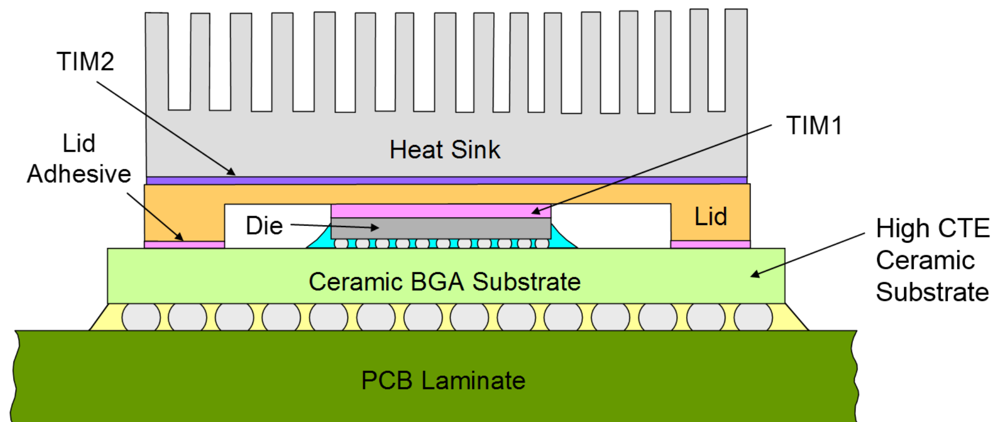


Figure 5.1: Schematic of Typical Microprocessor Architecture

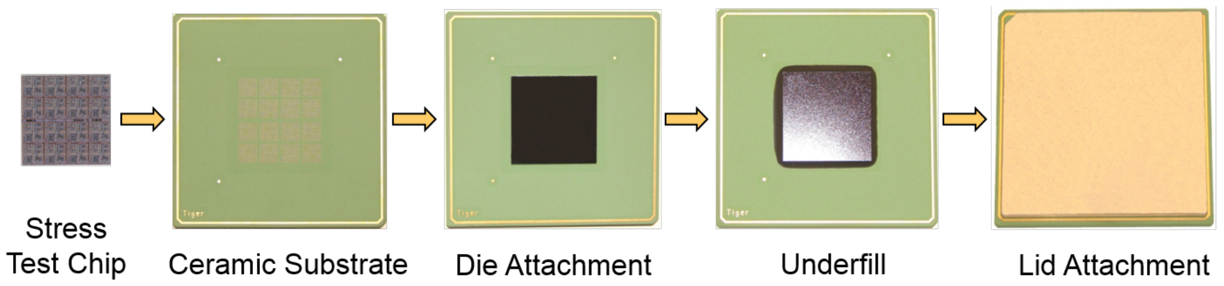


Figure 5.2: CLGA Flip Chip Test Assemblies and Packaging Process Steps

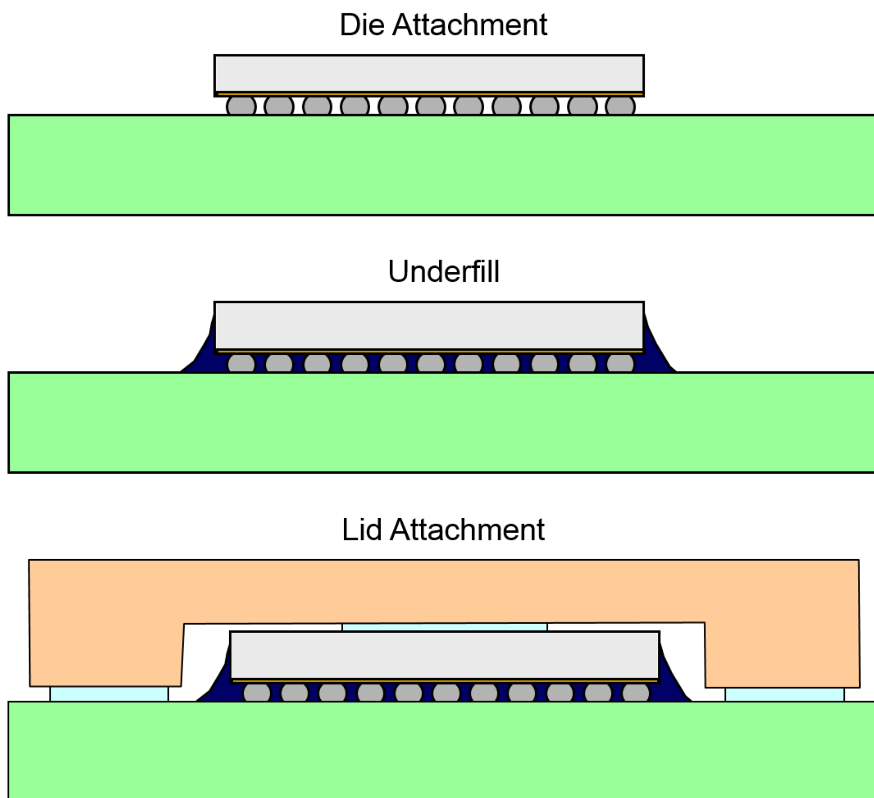


Figure 5.3: Schematics of the CLGA Package at Various Points in the Assembly Process

Each 20 x 20 mm test chip contained 256 sensor rosettes, with each rosette containing 8 piezoresistive sensor elements for a total of 2048 resistors per chip. Each flip chip die had 3600 solder bump connections with 2384 of those used to access piezoresistive sensors, diodes, heaters, and fuse identifiers (ID). In each of the 16 identical sub regions (see Figure 4.3), there were 149 active solder ball connections including 118 to access the piezoresistive sensors, 4 to access the diode temperature sensors, 18 to access the buried layer heater, and 9 to access a fuse ID. For this study, a subset of 36 rosettes was used for stress measurements. In addition, electrical access was maintained to the on-chip buried heater layer for power cycling measurements and to an eight-bit fuse style chip-ID. The ceramic substrate was designed to only route 308 of the 2384 useful chip connections from its top (where the chip is attached) to its bottom (where it is connected to a PCB). These 308 active connections included 265 pads for piezoresistive sensors, 8 pads for diodes, 26 pads for connection to the heater, and 9 pads for the fuse ID. Figure 5.4 shows the active pads on the packaged test chips including the rosette sites and solder bump locations that were interrogated after each packaging step. These sites were chosen so that measurements could be made at the die center and die corners, where several of the stress components typically have their maximum values. In addition, other sites were chosen to verify the symmetry of the observed stress distributions.

The integrity of the assembly process was evaluated after each manufacturing step. Micro-focus x-ray inspection (see Figure 5.5) was utilized on each sample after solder joint reflow to identify any mis-alignment of the die to the ceramic substrate, as well as to locate poorly formed or missing solder joints. In addition, CSAM imaging (see Figure 5.6) was utilized after underfill dispense and cure to locate voids at the die to underfill interface. With the exception of a small number of missing solder balls on a few parts, the quality of the assemblies was quite high.

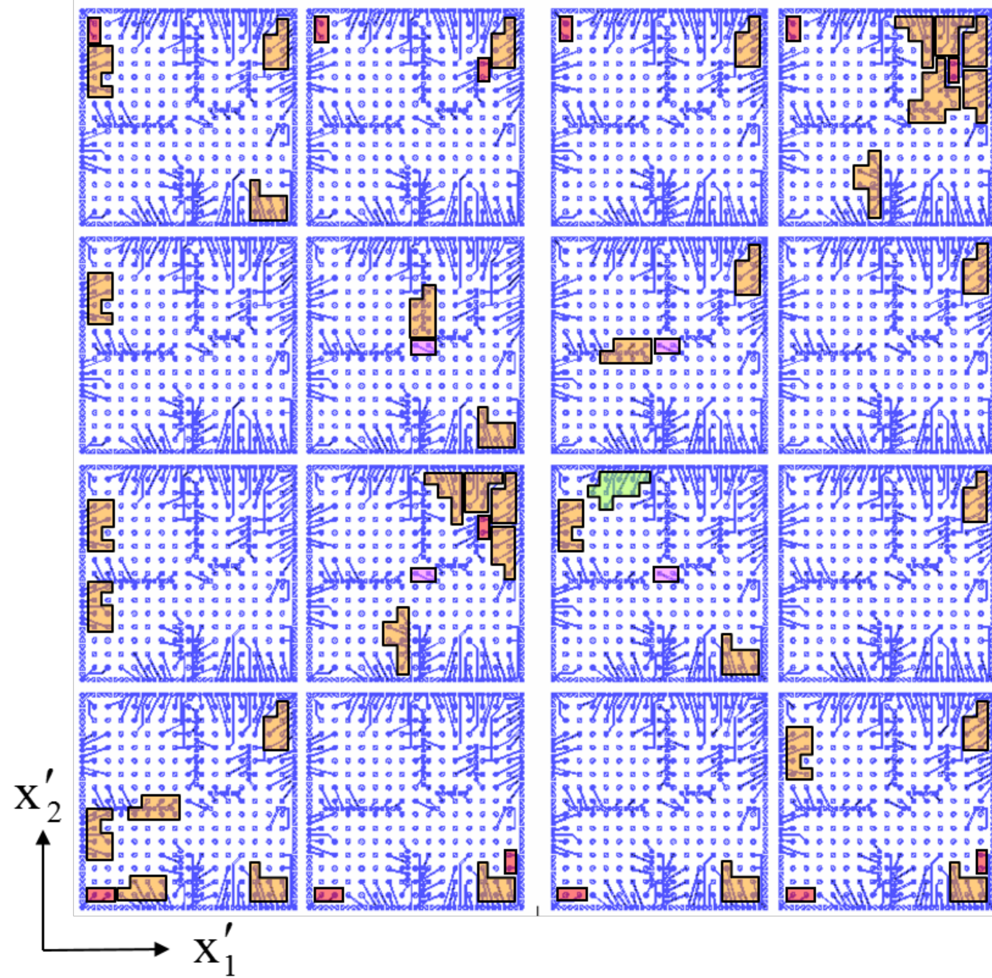


Figure 5.4: Active Pads on the Packaged Test Chips

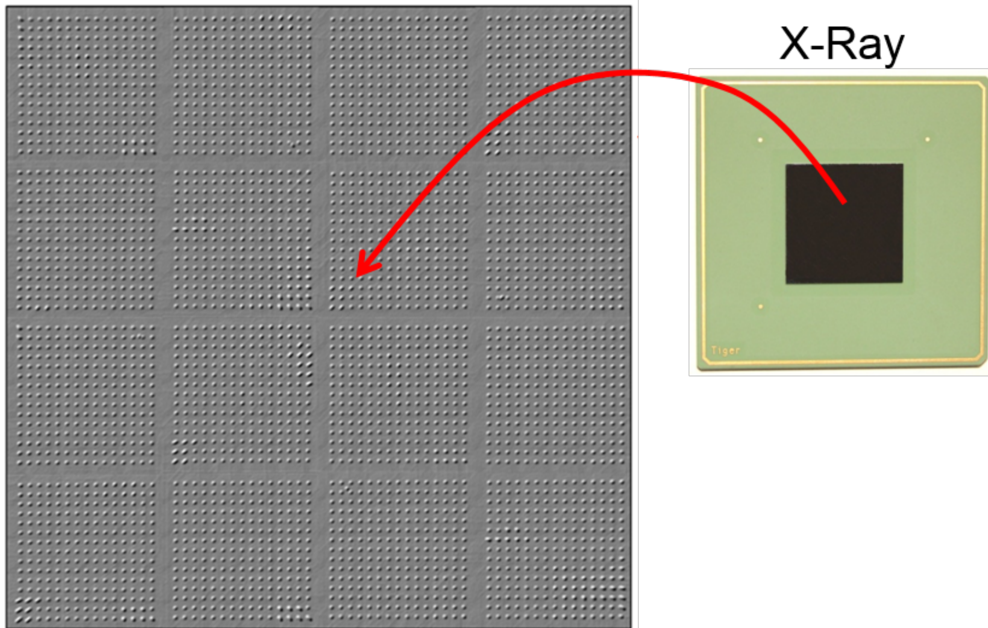


Figure 5.5: X-Ray Verification of Solder Bumps

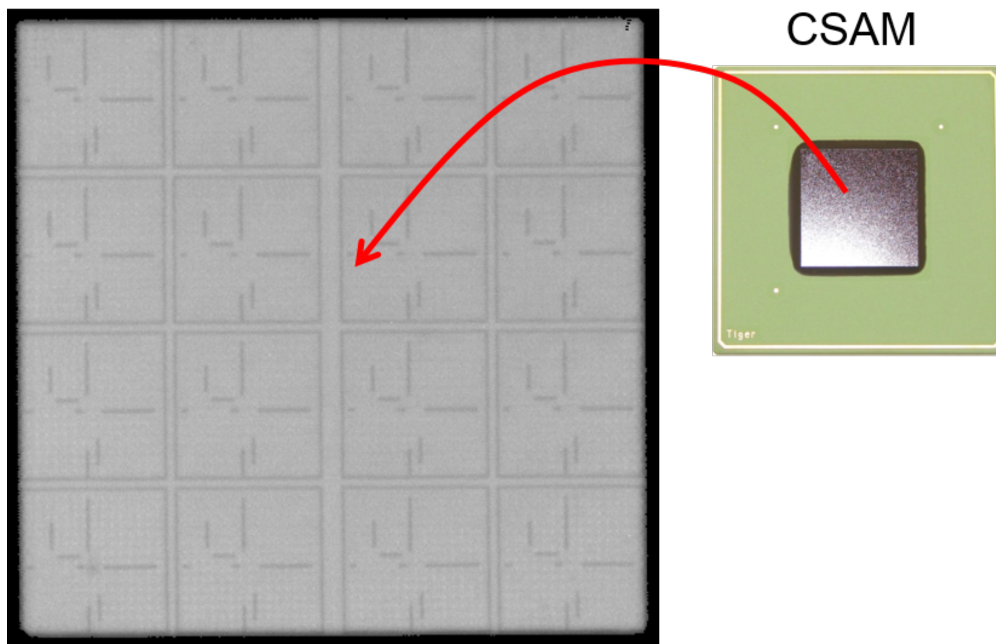


Figure 5.6: CSAM Verification of Die-Underfill Interface

5.1.1 Measurement Methodology

As mentioned earlier, calculation of die stresses for each eight element rosette requires the measurement of the initial (reference) and final (stressed) resistances of the 8 sensing elements. Typically, the preferred initial reference state is the bare chip, which is considered to be stress free. In previous studies using similar JSE stress test chips [98, 182], the initial reference state was taken to be the flip chip die reflowed to a substrate. In those studies, it was shown that the stresses induced by reflow and subsequent cooling were negligible. Thus the post-reflow die was considered to be stress free and an acceptable reference state for initial sensor resistances to be measured. It should be noted that the assemblies in that study employed a perimeter array of tin-lead solder bumps. The stiffness of the lead free solder used for first level assembly in the current study is approximately 50 percent larger than the tin-lead bumps in previous studies. In addition, the test chips in the current study were comprised of 3600 lead-free solder bumps in a full area array, as previously noted. Therefore, the solder reflow state could not be considered to be stress free, and it was necessary to characterize the bare die in the current study to establish the stress free (reference) values of the sensor resistances and to fully characterize the stresses induced in the chip by die attachment.

The sensors on each test die were initially measured at room temperature using a manual probe station as shown in Figure 5.7. Electrical access to the sensors during subsequent room temperature resistance measurements (after the various assembly steps) was obtained by inserting the ceramic Land Grid Array (LGA) substrates into a high density socket that interfaced to a test board. The LGA socket used in this work consisted of an array of metal "spring" contacts that were embedded in a flexible substrate "shell". The contacts in the socket bridged the gap between the pads on the bottom of the LGA and the pads on the PCB test board as shown in Figure 5.8. Pressure is required to hold the LGA component in the socket and insure good electrical connections. In most applications, this pressure is typically obtained by the clamping forces exerted by a heat sink and bolster plate combination as

shown earlier in Figure 1.1. This approach could not be used here because it would put direct pressure on the silicon die and change the die stress levels. Thus, several low impact clamping fixtures were developed in this work as shown in Figure 5.9 (die attachment and underfill steps) and Figure Figure 5.10 (lid attachment step). These fixtures have been demonstrated to provide good electrical connections to the CLGA bond pads, while not imparting any additional stresses to the die. A full discussion of the development of these fixtures can be found in references [181, 183]. A set of high density ribbon cables interfaced the test PCB to the PC-based data acquisition system shown in Figure 5.11 and described previously in Section 4.3.3. This system incorporated a GPIB controlled scanning system, digital multimeters, and LabView software.

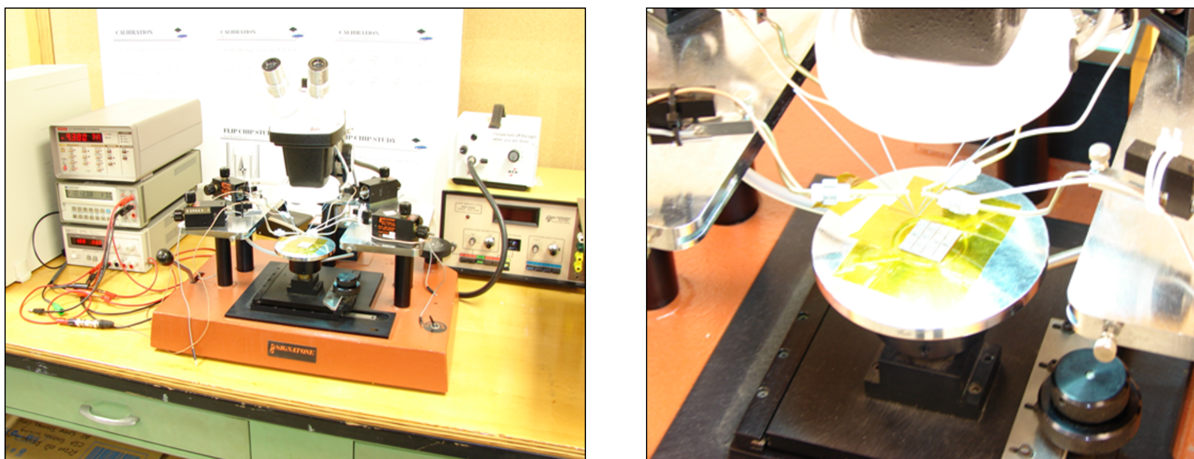


Figure 5.7: Measurement with Manual Probe Station

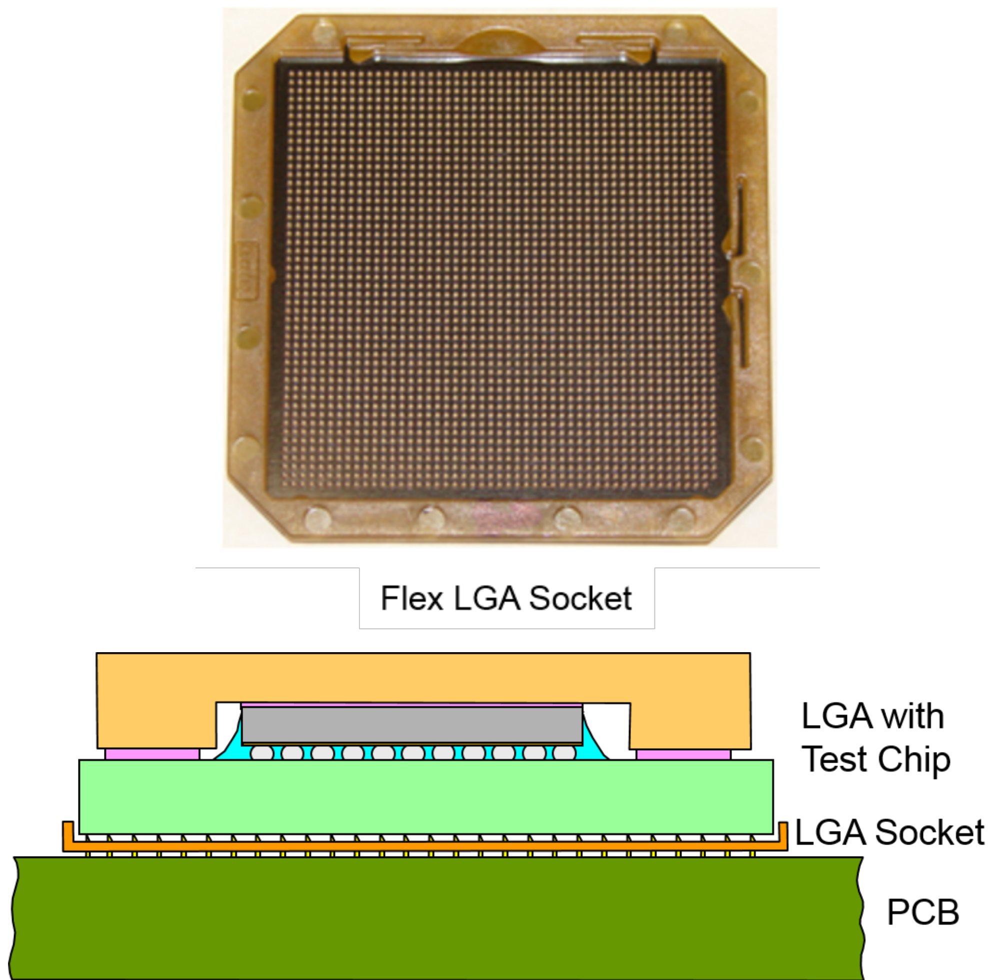
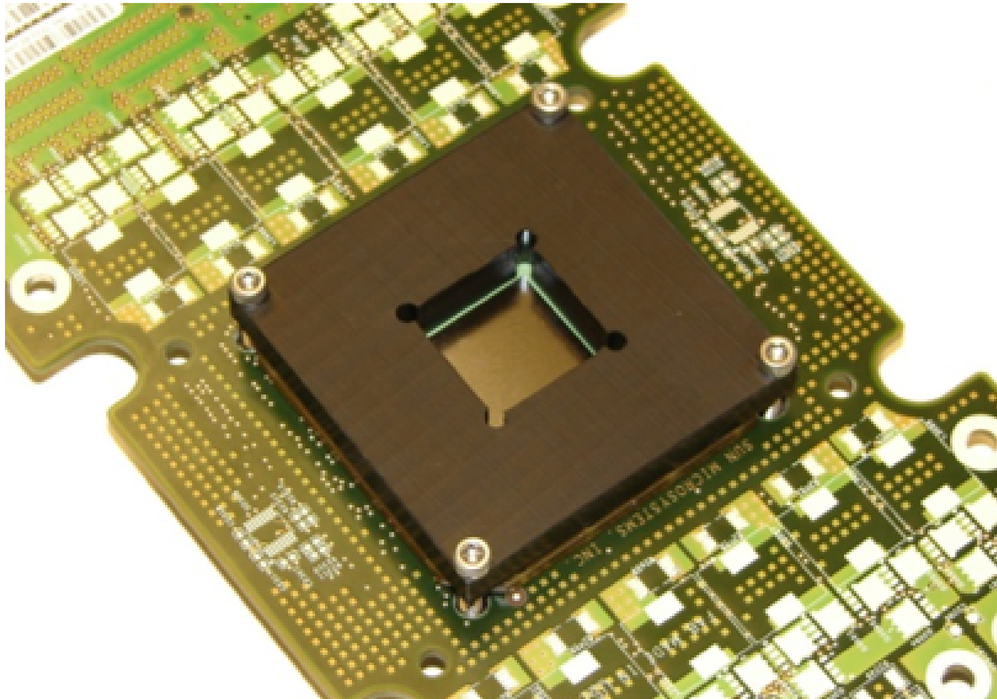


Figure 5.8: Electrical Connection via Flex LGA Socket



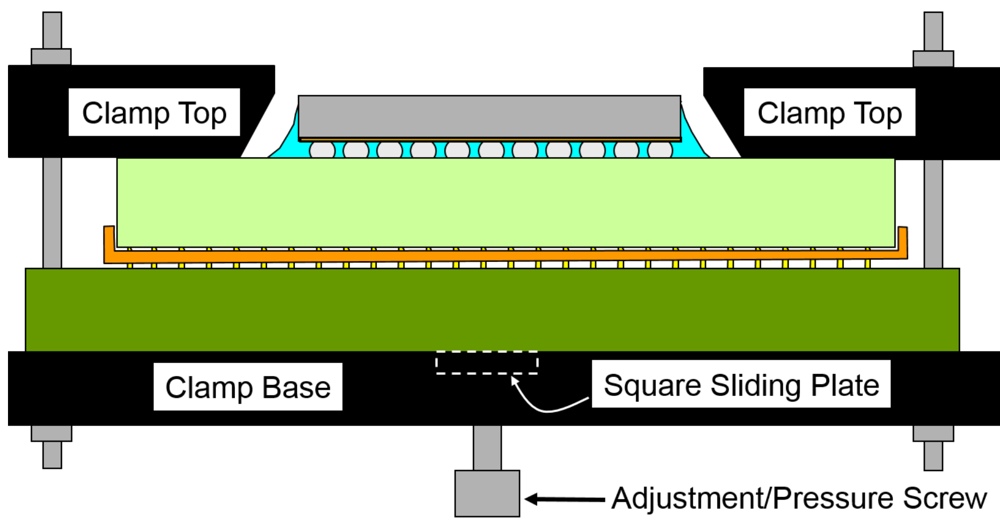
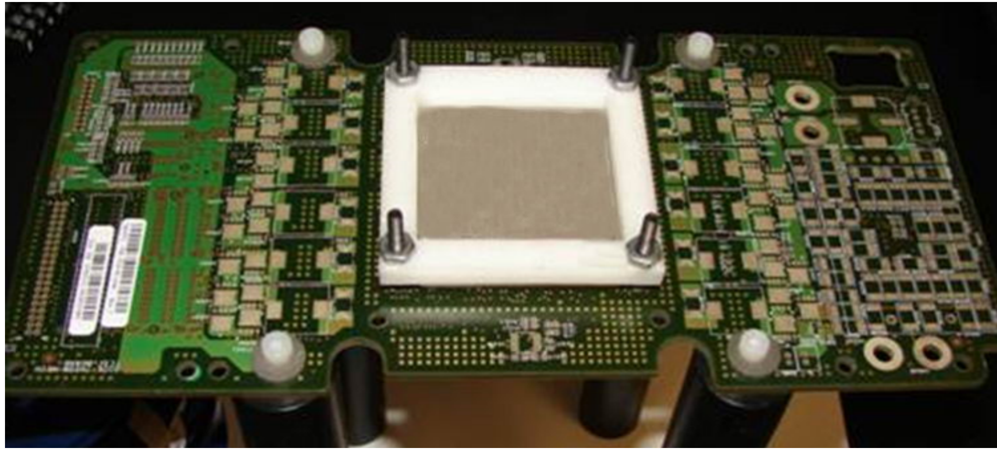


Figure 5.9: Clamping Fixture for Ceramic LGA (After Solder Reflow and Underfill Steps)



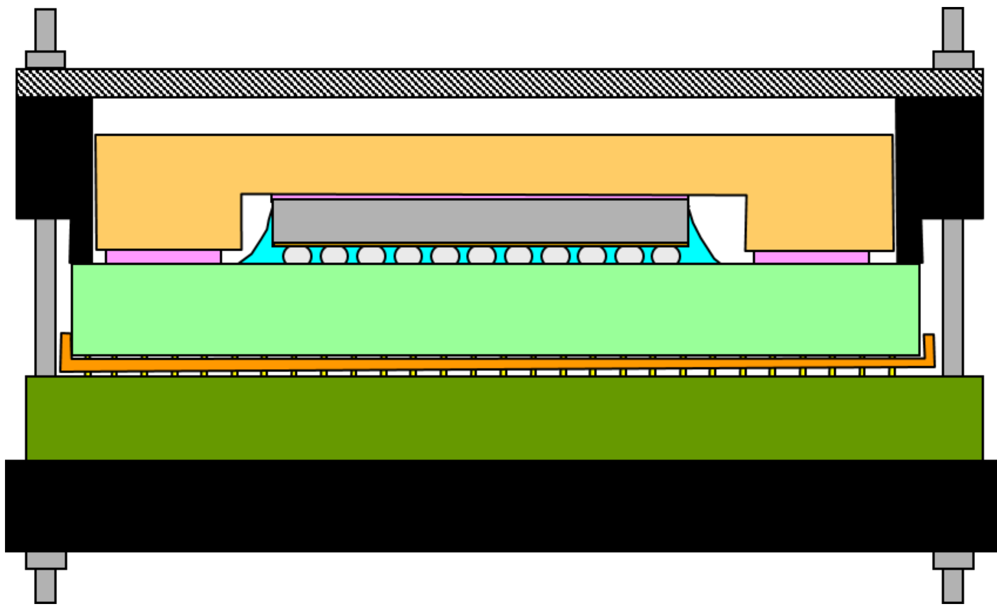


Figure 5.10: Clamping Fixture for CLGA (Lid Attachment Step)

Figure 5.11: Data Acquisition System

5.2 Experimental Stress Characterization of Packaging Induced Die Stresses

Prior to assembly, the first measurements on each test die were made using a manual probe station as shown in Figure 5.7. As mentioned, this measurement characterizes the initial or reference state of each test die. The stress state of each rosette on the test die can be extracted at any point if the initial and current resistances for each sensor, as well as the initial and final temperatures, and calibration coefficients are known. The stresses are calculated using Equations (4.2). The ΔR_i terms are defined as the initial or reference resistance of the sensor subtracted from the current resistance of the sensor. The sensor resistances measured after each stage of assembly are then considered to be the current resistances.

5.2.1 Die Stress Due to Solder Reflow

A typical package after die attachment is shown in Figure 5.12. After the flip chip die were reflow soldered to the ceramic substrates, resistances of the sensors on the test die were measured again using the data acquisition system shown in Figure 5.11 and test board and fixture in Figure 5.9. The results of the measurements agreed with historical test chip data in several ways. First, the largest in-plane normal stresses were compressive, and were observed at the center of the die. Correspondingly, the lowest values of in-plane normal stress were observed at the corners of the die. In addition, the largest values of in plane shear stress were observed at the corners of the chip. The values of the out-of-plane shear stresses were small, as seen previously, and were found to be 2-4 MPa. In comparison to earlier flip chip studies, the magnitudes of the normal stresses were 10X larger. Another noted difference to previous work [12, 66–68, 98, 100, 182] was the large value of the out-of-plane normal stress. Average values of die stress components measured at the die center and corner for 40 assemblies are shown in Figure 5.13.

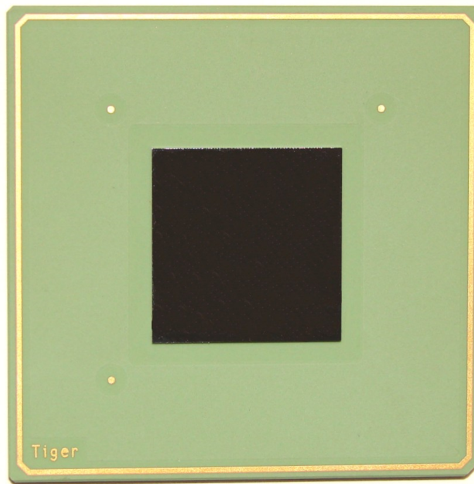
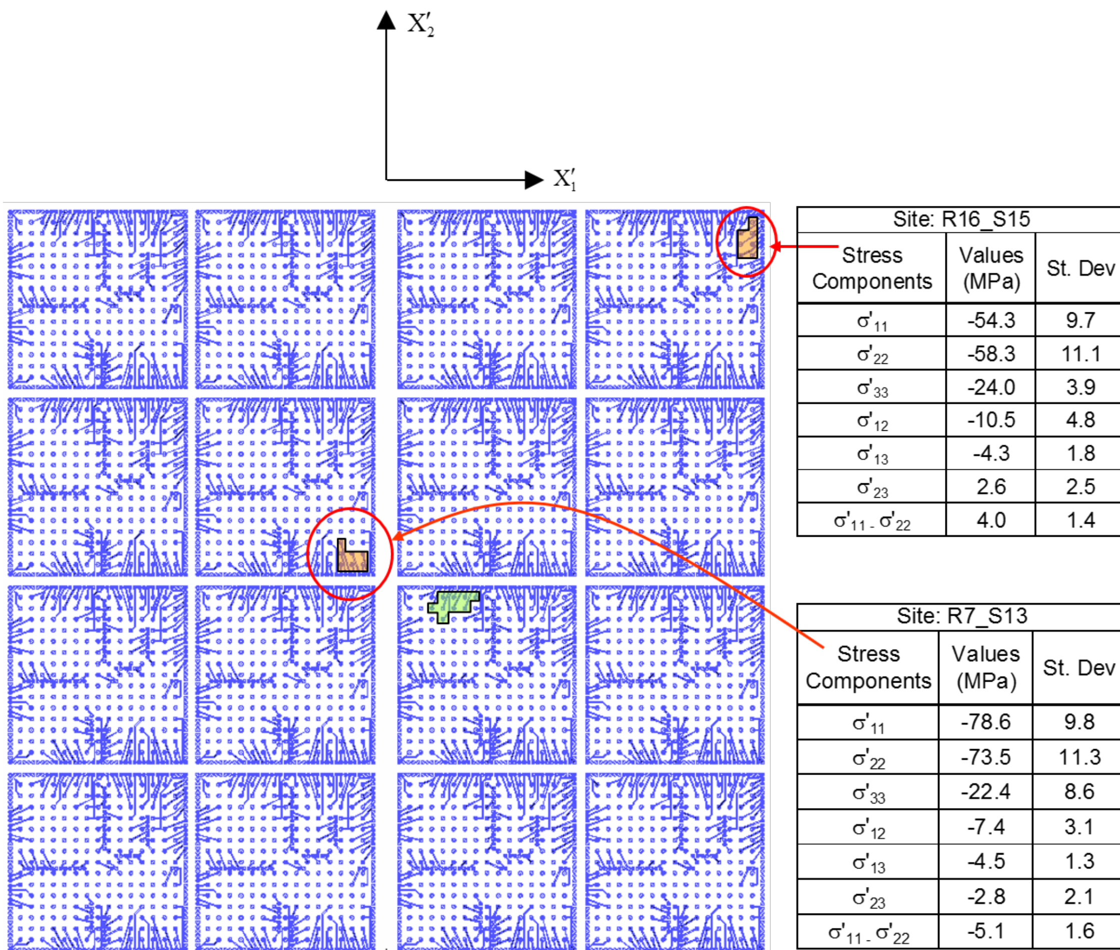


Figure 5.12: Typical Package After Die Attachment



Site: R16_S15		
Stress Components	Values (MPa)	St. Dev
σ'_{11}	-54.3	9.7
σ'_{22}	-58.3	11.1
σ'_{33}	-24.0	3.9
σ'_{12}	-10.5	4.8
σ'_{13}	-4.3	1.8
σ'_{23}	2.6	2.5
$\sigma'_{11} - \sigma'_{22}$	4.0	1.4

Site: R7_S13		
Stress Components	Values (MPa)	St. Dev
σ'_{11}	-78.6	9.8
σ'_{22}	-73.5	11.3
σ'_{33}	-22.4	8.6
σ'_{12}	-7.4	3.1
σ'_{13}	-4.5	1.3
σ'_{23}	-2.8	2.1
$\sigma'_{11} - \sigma'_{22}$	-5.1	1.6

Figure 5.13: Stresses Due to Die Attachment

5.2.2 Die Stress Due to First Level Underfill

After these measurements, the packages were underfilled with a glass filled epoxy. A typical underfilled package is shown in Figure 5.14. Results of the measurements taken on packages after underfill dispense and cure are shown in Figure 5.15. The general trends in stress values were similar to those in the die attached packages, but with dramatic increases in magnitude. The normal stress magnitudes at the center of the die more than doubled, and the in-plane shear stress at the die corners increased by 25 percent. The normal stress difference at the center of the die was statistically unchanged, while it doubled at the corner of the die. The out-of-plane shear stress values remained very low with only very small changes.

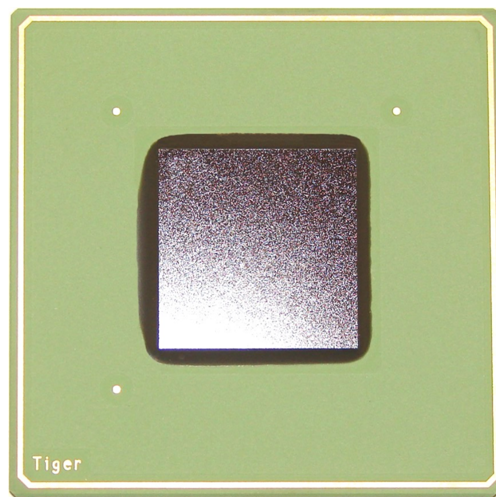
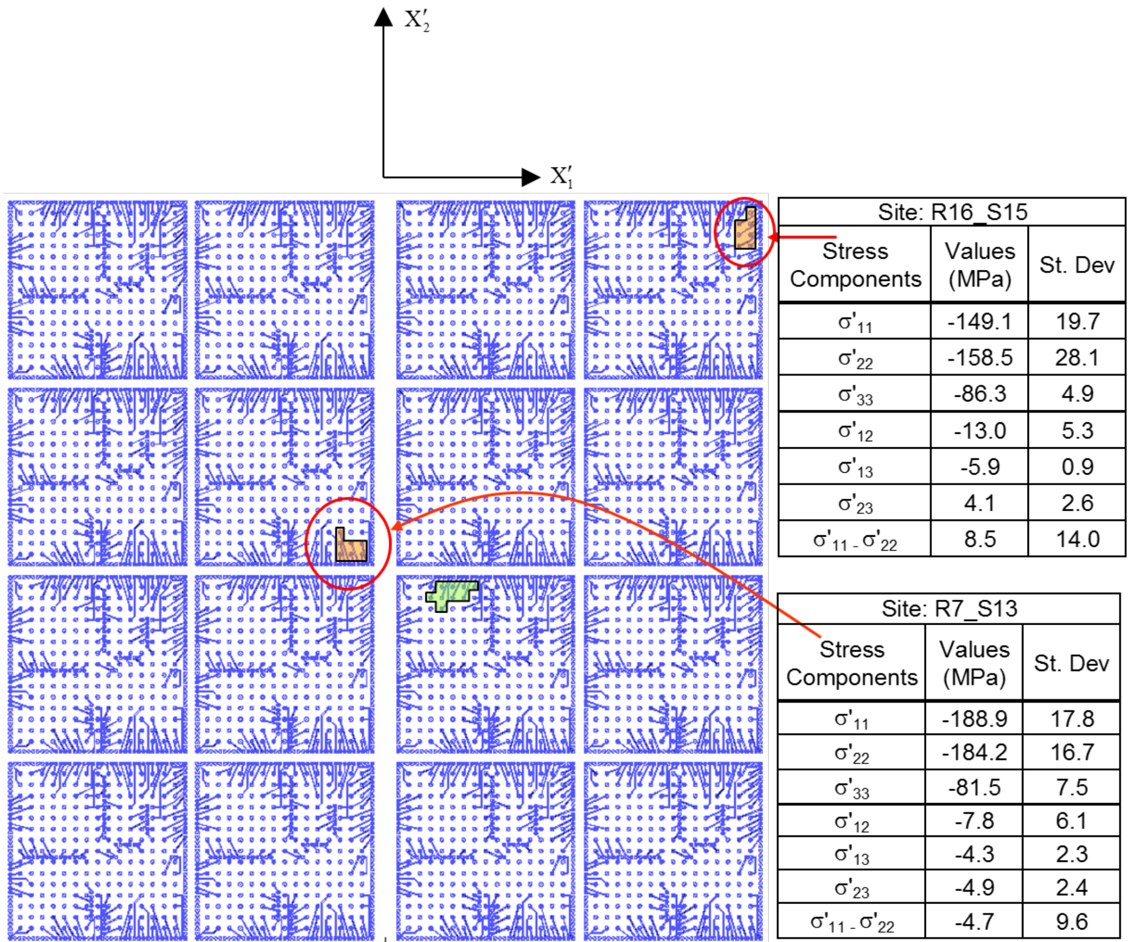


Figure 5.14: Typical Package After Underfill Dispense and Cure



Site: R16_S15		
Stress Components	Values (MPa)	St. Dev
σ'_{11}	-149.1	19.7
σ'_{22}	-158.5	28.1
σ'_{33}	-86.3	4.9
σ'_{12}	-13.0	5.3
σ'_{13}	-5.9	0.9
σ'_{23}	4.1	2.6
$\sigma'_{11} - \sigma'_{22}$	8.5	14.0

Site: R7_S13		
Stress Components	Values (MPa)	St. Dev
σ'_{11}	-188.9	17.8
σ'_{22}	-184.2	16.7
σ'_{33}	-81.5	7.5
σ'_{12}	-7.8	6.1
σ'_{13}	-4.3	2.3
σ'_{23}	-4.9	2.4
$\sigma'_{11} - \sigma'_{22}$	-4.7	9.6

Figure 5.15: Stresses After Underfill Dispense and Cure

5.2.3 Die Stress Due to Lid Attachment

The third step of assembly of the CLGA stress test chip packages saw the addition of a metalic lid, or heat spreader. An image of a typical lidded package is shown in Figure 5.16, while a schematic of the cross section of a typical lidded package is shown in Figure 5.17. Figure 5.18 shows an x-ray of the lid attachment adhesive, which also serves as the thermal interface material (TIM) for the first level of interconnection (TIM1). Figure 5.19 shows a cross section of a lidded package, specifically the thickness of the lid adhesive. Measurement results for the stresses in the lidded packages are shown in Figure 5.20.

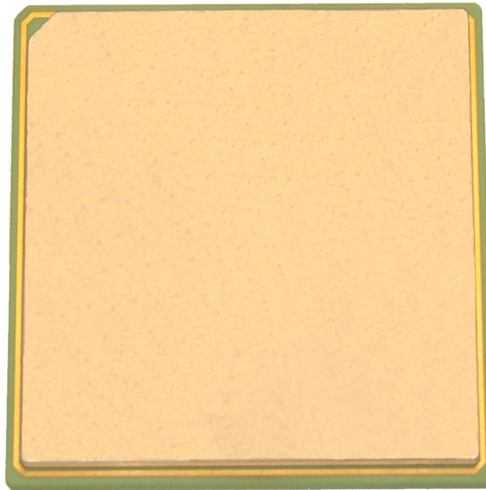


Figure 5.16: Typical Package After Lid Attachment

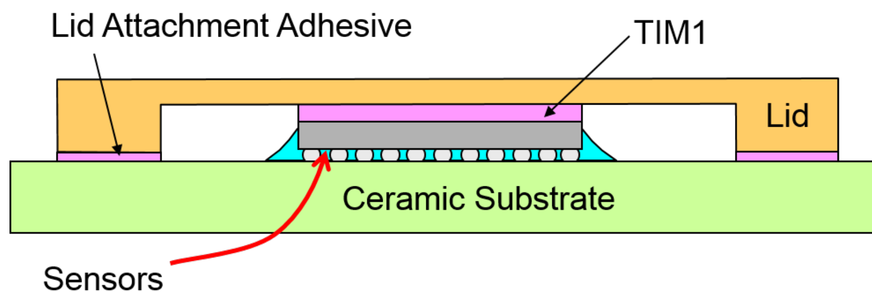


Figure 5.17: Schematic of Typical Package After Lid Attachment

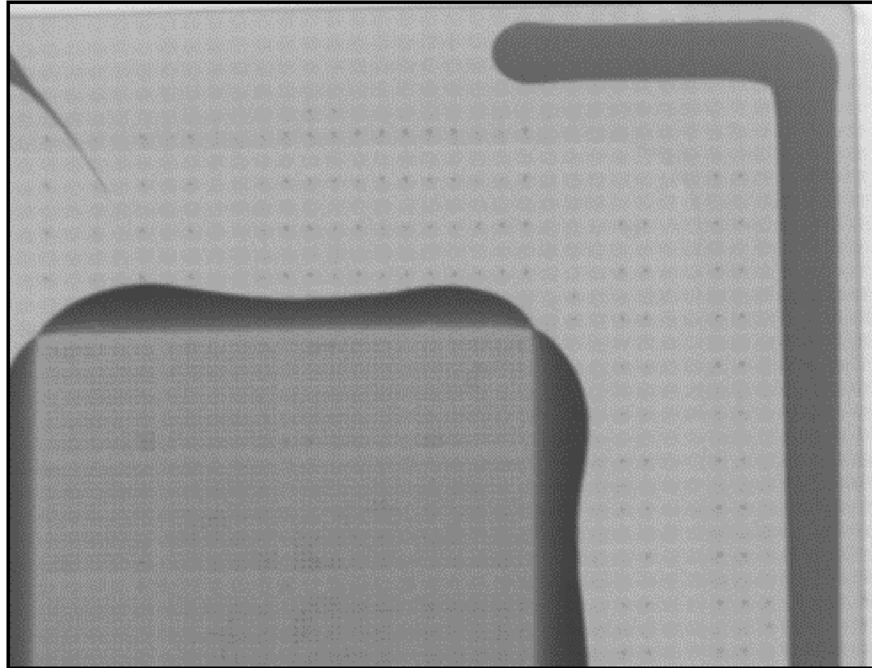


Figure 5.18: X-ray of TIM1 Layer and Lid Adhesive

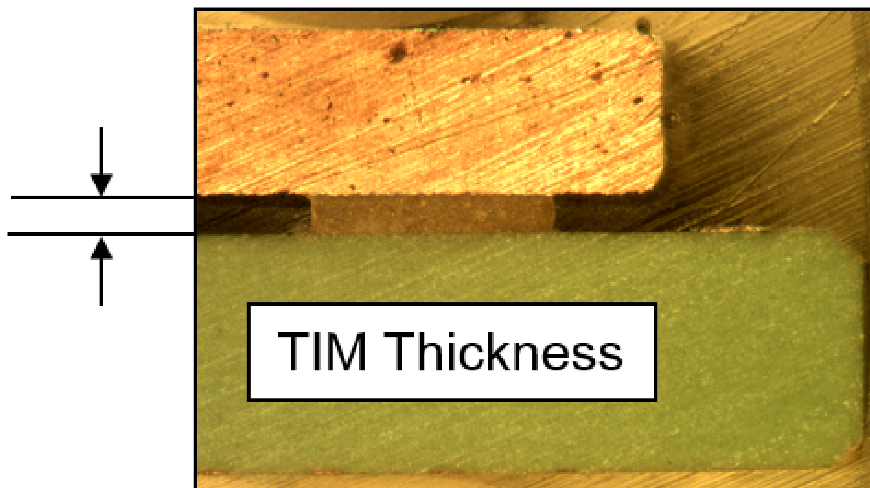
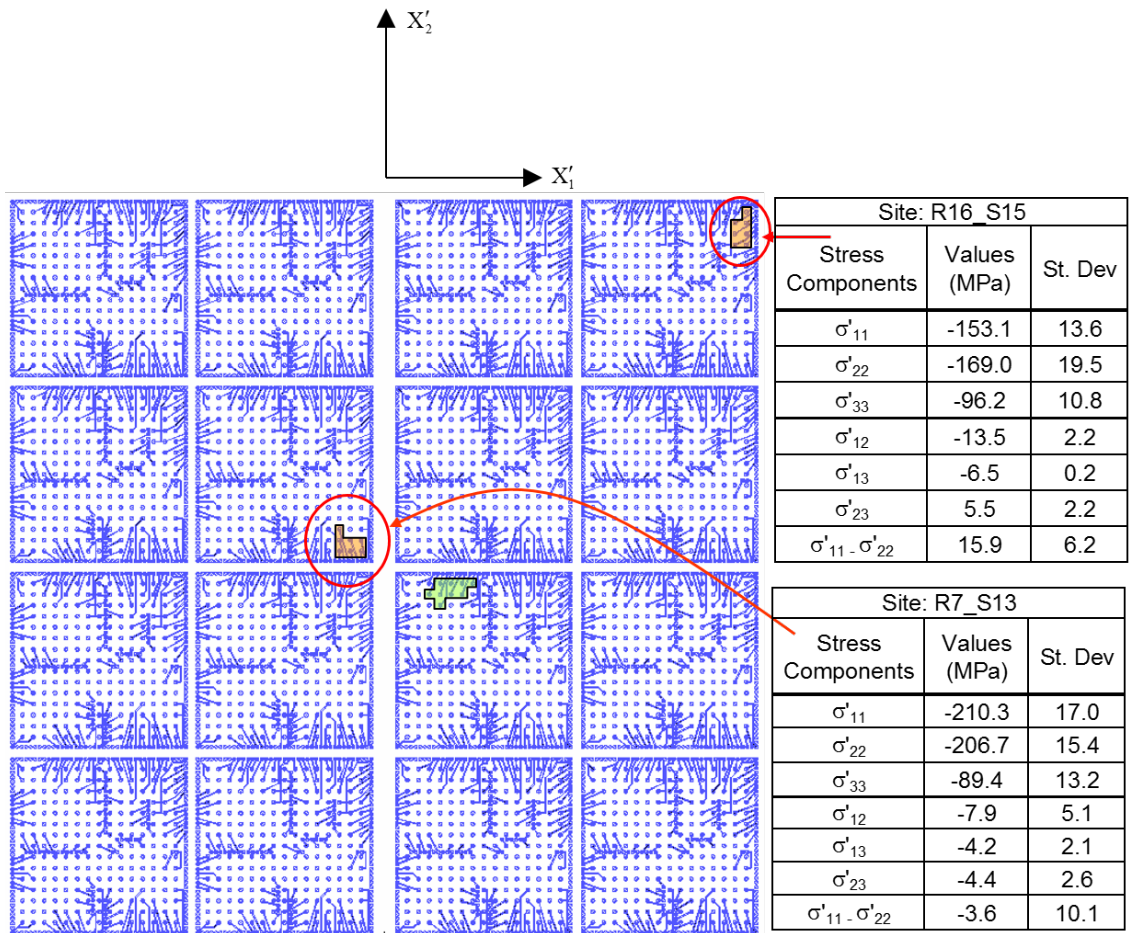


Figure 5.19: Cross Section Showing Lid Adhesive Thickness



Site: R16_S15		
Stress Components	Values (MPa)	St. Dev
σ'_{11}	-153.1	13.6
σ'_{22}	-169.0	19.5
σ'_{33}	-96.2	10.8
σ'_{12}	-13.5	2.2
σ'_{13}	-6.5	0.2
σ'_{23}	5.5	2.2
$\sigma'_{11} - \sigma'_{22}$	15.9	6.2

Site: R7_S13		
Stress Components	Values (MPa)	St. Dev
σ'_{11}	-210.3	17.0
σ'_{22}	-206.7	15.4
σ'_{33}	-89.4	13.2
σ'_{12}	-7.9	5.1
σ'_{13}	-4.2	2.1
σ'_{23}	-4.4	2.6
$\sigma'_{11} - \sigma'_{22}$	-3.6	10.1

Figure 5.20: Stresses After Lid Attachment

5.2.4 Summary of Packaging Induced Die Stresses

Analogous to many other packaging architectures, the maximum normal stresses (compressive) were found to be located at the center of the die, while the maximum shear stresses were found in the corners. Measured stress values from sensor rosettes at these two locations will be used to describe the buildup of die stress induced by each successive step of assembly. A typical outcome for the evolution of the die stresses during the assembly process is shown in Figure 5.21. In this plot, the magnitudes of the compressive horizontal normal stress at the center of the die are shown after each of the assembly operations. It is seen that the stress due to solder joint reflow is quite large (about -75 MPa). This is significantly larger than the values of 0-2 MPa observed in previous studies with small die (5 x 5 mm) attached to laminate substrates with a perimeter configuration of Sn-Pb solder bumps [12]. The larger values in the current work are most likely due to a combination of reasons including the much larger die size, use of a full area array of solder joints (instead of perimeter bumping), and the use of much stiffer lead free solder joints (instead of Sn-Pb).

After the addition of underfill, the central normal stress is seen to nearly triple to about -200 MPa. At all rosettes sites on the die, we observed that the majority of the die compressive stress is accumulated during the underfilling assembly step. Typical increases in the stress magnitude were on the order of 300% (relative to the stresses due to solder joint reflow only). The change in normal stress due to the final lid attachment packaging step was about -20 MPa, or an additional 10% increase to a total average compressive stress of -220 MPa. Such results were also observed at other rosette sites. As a general rule of thumb, approximately 2/3rds ($\approx$66%) of the final die compressive normal stresses were observed to be developed during the underfill dispense and cure, with the second largest contribution coming from the die attachment (solder reflow) assembly step, and the smallest contribution coming from lid attachment.

Figure 5.22 illustrates the evolution of all six stress components at the center of the chip with the various packaging processes. As expected, the shear stresses are quite small (mostly

< 5 MPa) near the center of the die. In addition, the results for the two in-plane normal stresses are nearly identical, verifying that the center of the die is in state of strong biaxial compression. Finally, the magnitude of the out-of-plane normal stress (also compressive) is fairly significant.

Analogous results for the evolution of all six stress components at one of the corners of the chip are shown in Figure 5.23. As expected, the shear stresses at the corner are higher than those at the center of the die (approximately 2X). The compressive normal stresses at the corner of the die are also quite large (approximately 75% of the die center values). It has been observed that the compressive normal stresses are rather uniform across the die surface, with the largest values at the center of the die, and the smallest values near the die corners and edges.

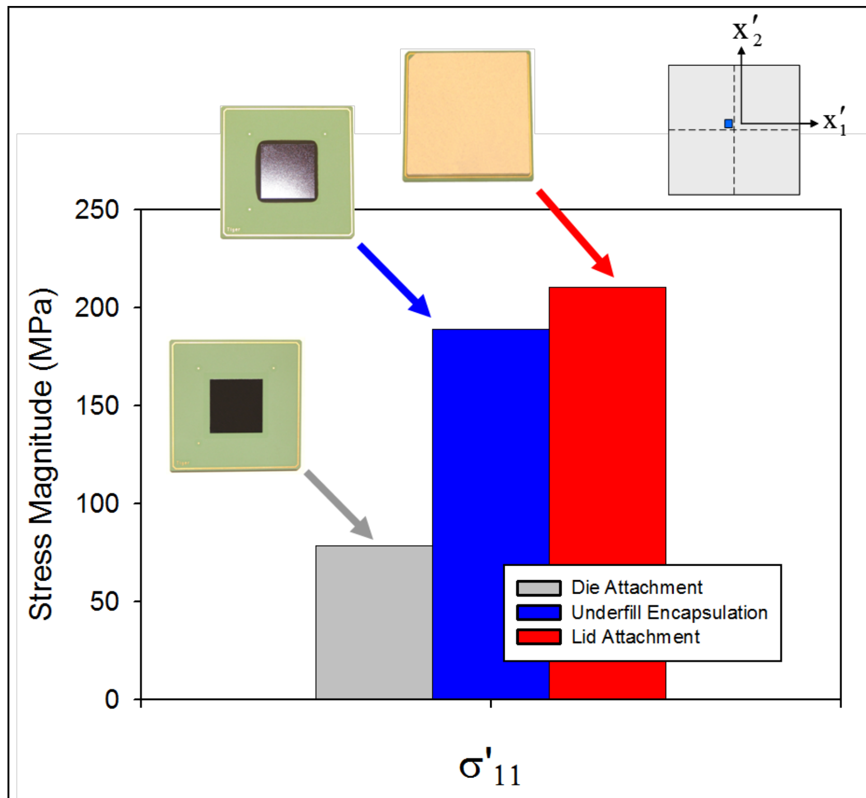


Figure 5.21: Evolution of Die Stress at the Center of the Chip (Compressive Horizontal Normal Stress)

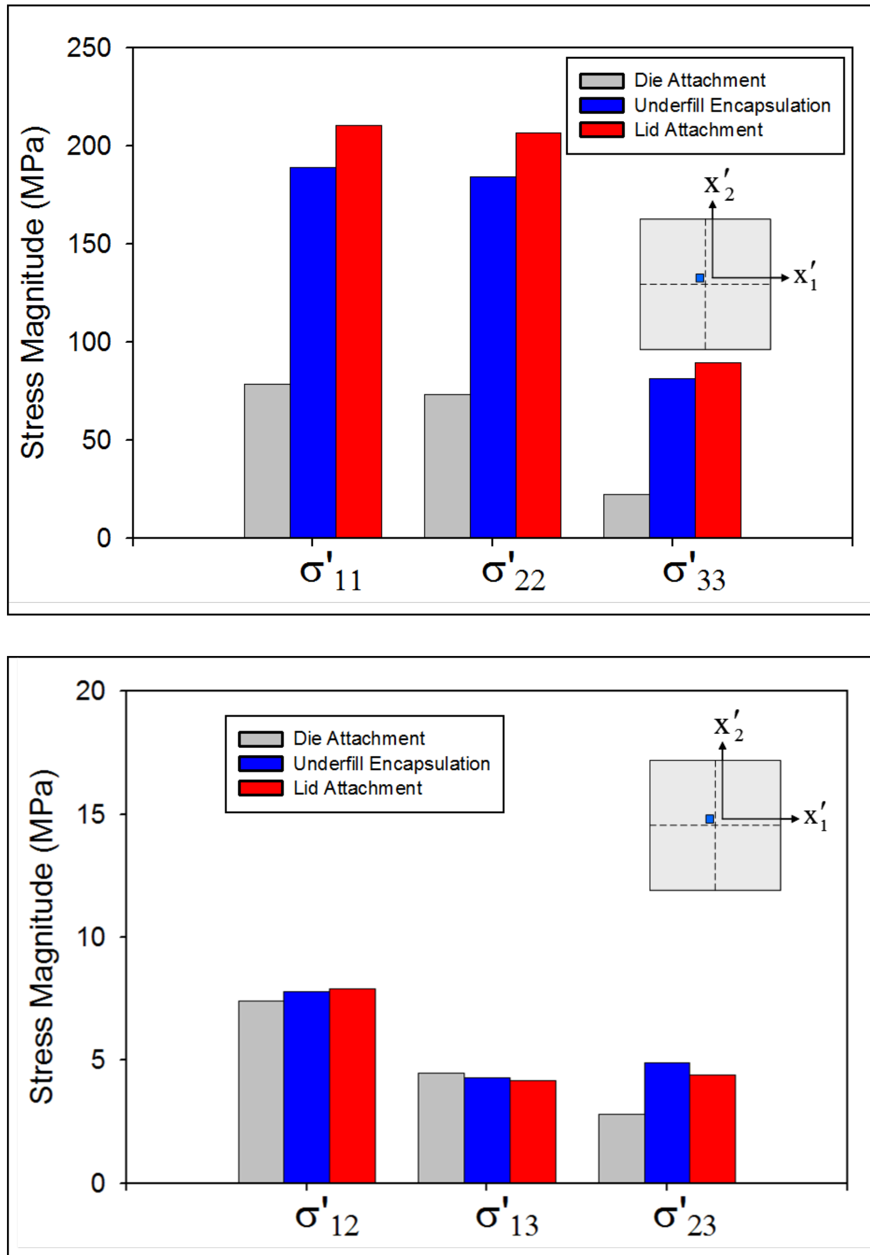
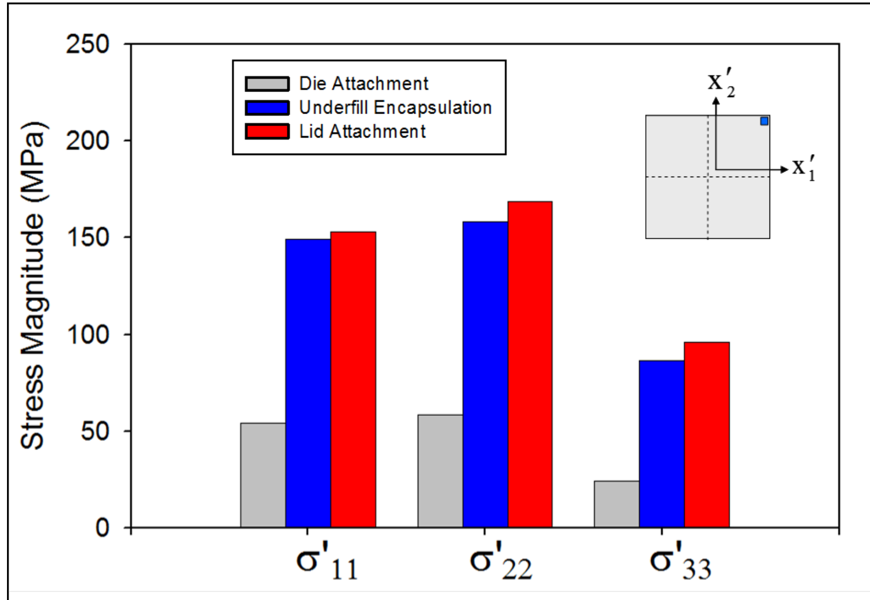


Figure 5.22: Evolution of the Six Die Stress Components at the Center of the Chip



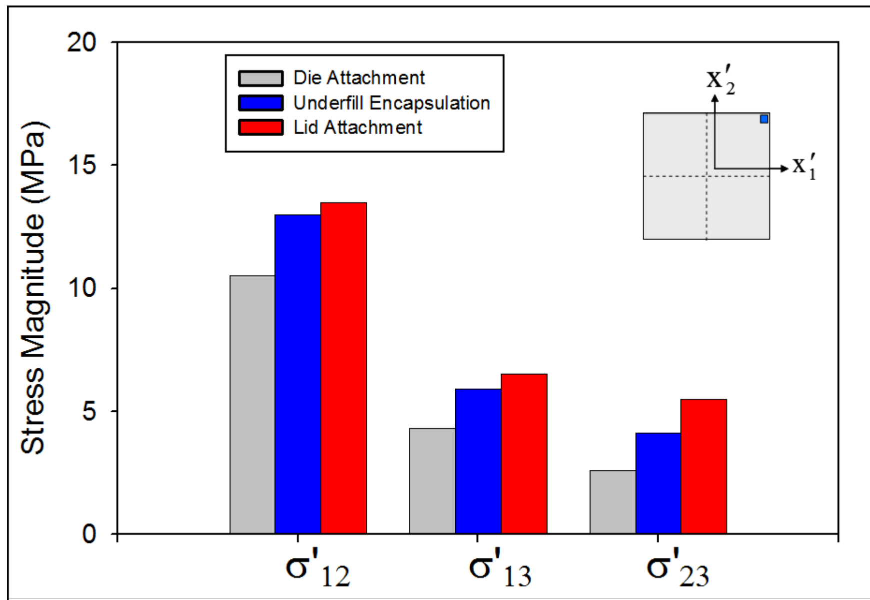


Figure 5.23: Evolution of the Six Die Stress Components at the Corner of the Chip

5.3 Numerical Evaluation of Packaging Induced Die Stresses

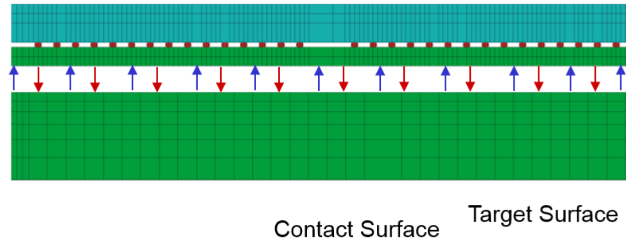
In a parallel study [183, 184], finite element analysis (FEA) was used to predict the effects of the assembly process on the die stresses found in the CLGA packages. Several iterations of multiple techniques were used to optimize the successive models, with sensitivity and convergence studies playing a key roll. To aid the accuracy of the models, mechanical testing of the materials found in the CLGA package was performed and used in the appropriate model. A brief description of the materials testing, FEA techniques, and the actual models used for each stage of assembly follows. A more detailed description of the numerical evaluation of the CLGA assemblies may be found in the work of Motalab [184].

5.3.1 Multipoint Constraints

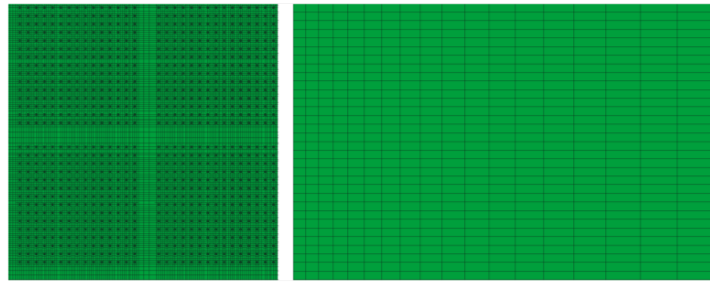
To numerically verify experimental results, a quarter model of the CLGA packages was produced for each stage of the assembly process. Using traditional methods, even a quarter model of the 3600 solder bump package proved to be very computationally intensive. The solution to this issue was the use of the Multipoint Constraint (MPC) technique. In this method, it is possible to tie together two regions with dissimilar mesh densities by generating constraint equations that connect the selected nodes of one region to the selected elements of the other region. To further streamline the model, higher order elements were used in selected regions where there were large stress gradients. Figure 5.24 shows how Multipoint Constraints were defined in different layers of the model.

5.3.2 Material Constitutive Models

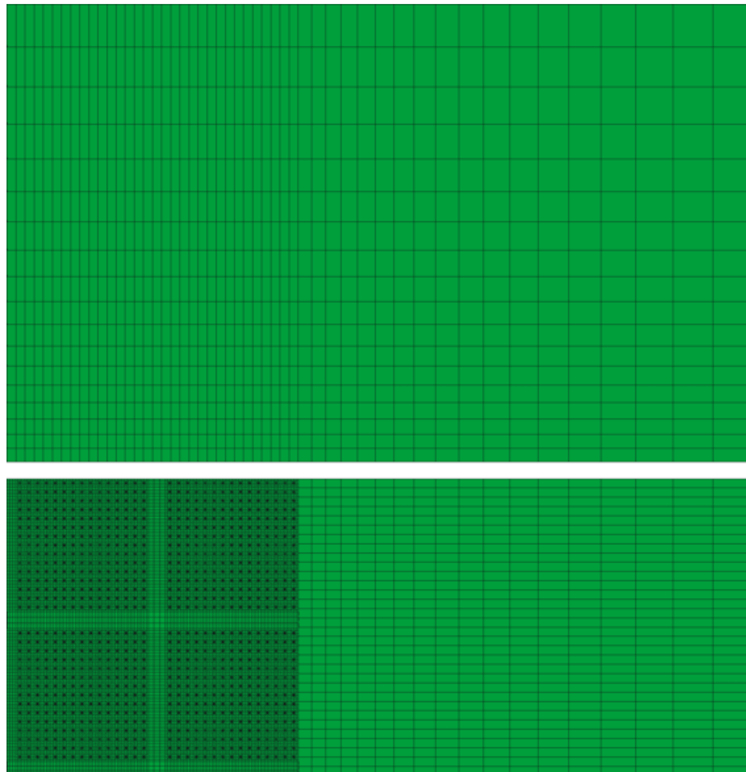
The stress-strain relations for the various materials in the microprocessor packaging geometry were characterized via mechanical testing or taken from vendor data sheets. The mechanical behaviors of the silicon chip, ceramic substrate, and AlSiC lid were all modeled as elastic with temperature dependent properties. For example, Figure 5.25 shows the tensile test results of the ceramic substrate between -40 °C and 220 °C. The flip chip underfill and



(a) Multipoint Constraint Layer 1



(b) Multipoint Constraint Layer 2



(c) Multipoint Constraint Layer 3

Figure 5.24: Multipoint Constraint Layers

TIM1 layer were both modeled as temperature-dependent elastic-plastic materials. For example, Figure 5.26 illustrates the measured stress-strain curves for the underfill encapsulant. Finally, the SAC solder used in for the flip chip bumps was modeled using the viscoplastic Anand model. The 9 material constants in the model were found using temperature and strain rate dependent stress-strain data. Table 5.1 contains a tabulation of the Anand material constants (ANSYS notation).

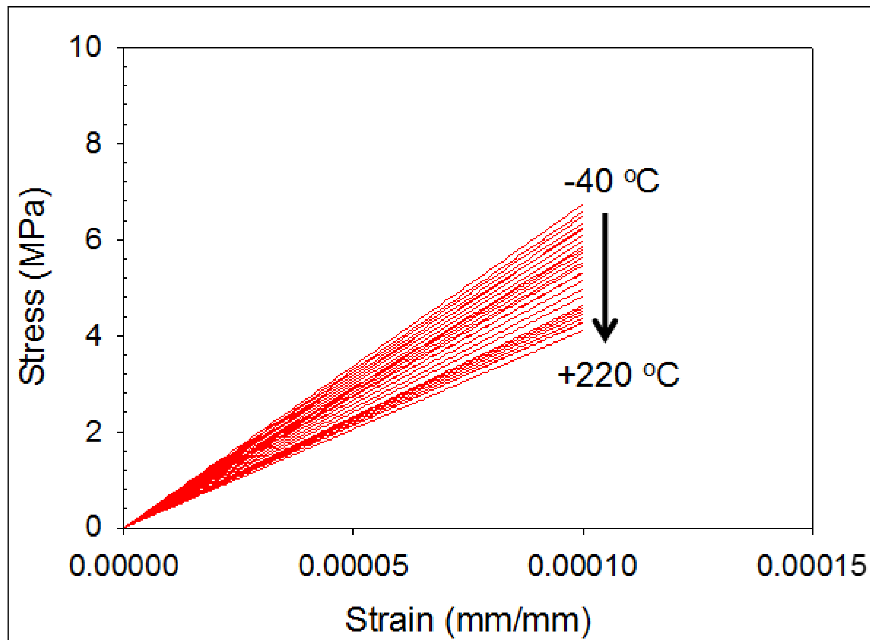


Figure 5.25: Stress Strain Behavior of HiTCE Substrate

Table 5.1: Anand Constants for Modeling of SAC Solder

Constant Number	Anand Constant	Units	Value
1	s_0	MPa	24.1
2	Q/R	1/K	9350
3	A	sec^{-1}	4000
4	ξ	Dimensionless	4.0
5	m	Dimensionless	0.2
6	h_o	MPa	25000
7	$\hat{s}$	MPa	36.0
8	n	Dimensionless	0.01
9	a	Dimensionless	1.4

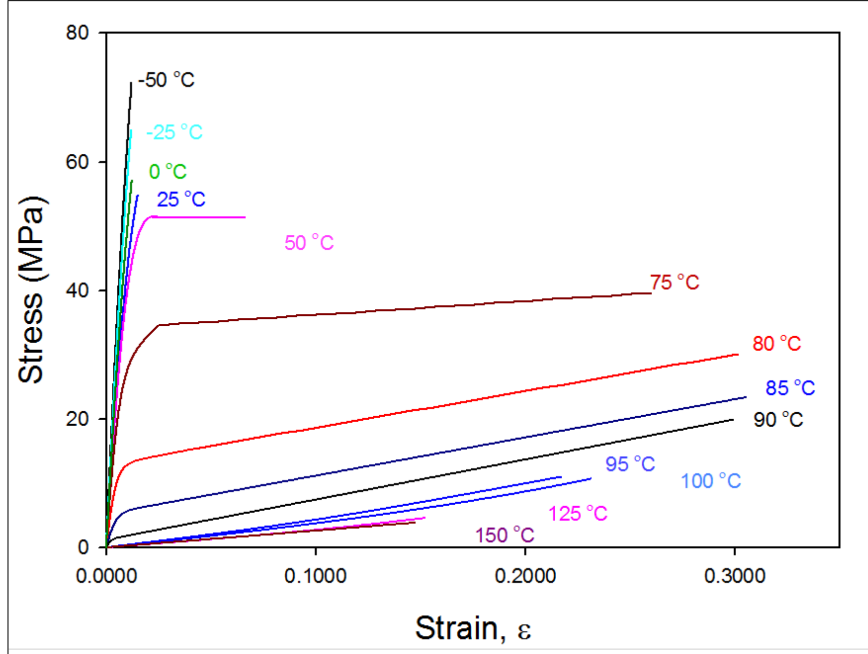


Figure 5.26: Stress Strain Behavior of First Level Underfill

5.3.3 Stress Build-up During Assembly Processes

A cross-sectional schematic of a fully assembled CLGA test specimen was shown in Figure 5.3, and photographs of actual samples after various steps in the manufacturing process were illustrated in Figure 5.2. The utilized high CTE ceramic substrates had in-plane dimensions of 51 x 51 mm, and a thickness of 2 mm.

Due to the small size and ductile nature of the flip chip solder bumps, it is a common practice to start modeling the packaging process from the underfill curing step, and to assume there are no initial stresses present after solder joint reflow. However, the experimental results shown have demonstrated that the die stresses induced by the solder reflow process are not negligible for the large die and area array lead free solder bumps in this work. Thus, it was also necessary to model the die attachment step in the assembly process.

In the packaging process, chips are reflowed to the ceramic substrates, and then subsequently underfilled and cured. Finally, a metallic lid (AlSiC) is attached to complete the ceramic LGA component. Since the stress buildup in the microprocessor die depends on the packaging history, the same sequence has been maintained in the modeling process to

correlate with the conditions of the experiments. Initial models did not follow this sequential approach and were not able to accurately predict die stress levels.

5.3.4 Solder Joint Reflow

Solder joint reflow, also referred to as die attachment, is the first step of the assembly process. Figure 5.27 shows the quarter symmetry finite element mesh used for simulating solder joint reflow, and Figure 5.28 illustrates how the layout of solder bumps in the actual package has been maintained in the modeling. The mesh, containing more than 1.2 million linear brick elements, includes the silicon die, solder balls, and ceramic substrate. Figure 5.28 also shows the horizontal and vertical streets with no solder balls that run through the center of the quarter section of the die.

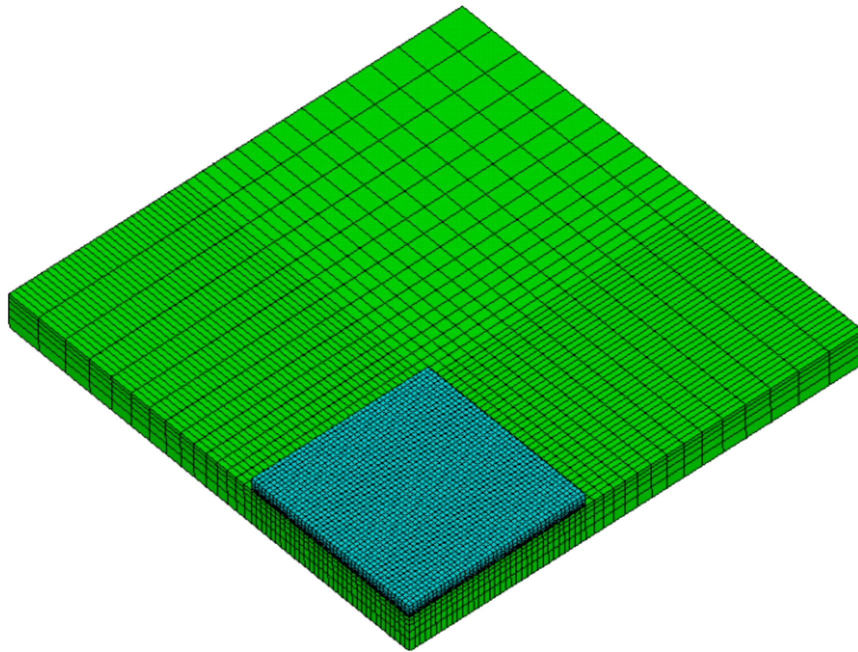


Figure 5.27: Quarter Model of Die Attachment

In the analysis, a uniform initial temperature of 217 °C was assumed across the entire structure, as it is the melting temperature of the SAC solder used on the solder bumps. In the actual assembly process, packages are cooled from the solder solidification temperature to the room temperature. To simulate the stresses due to the die attachment, a uniform

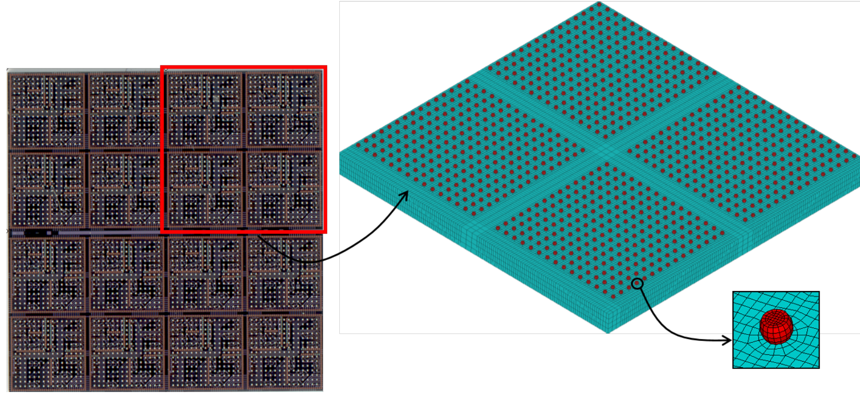


Figure 5.28: Silicon and Solder Bump Detail of Quarter Model

temperature of 25 °C was applied to all nodes of the model. Due to the geometric and material nonlinearities in the model, the total temperature load is applied in a number of load steps to insure convergence.

Figure 5.29 shows the gradual buildup of the compression in the die for the horizontal in-plane normal stress as the temperature is reduced from 217 °C to 25 °C. The maximum value of the horizontal normal stress was predicted to be -67 MPa at the center of the die. Figure 5.30 illustrates the distribution of the horizontal normal stress across the entire surface of the die. The in-plane normal stress decreases from its maximum value of -67 MPa at the die center to zero at the left and right free edge of the die. The stress distribution also reveals local stress concentrations near the solder bumps, and this phenomenon is seen across the entire die surface. Similar results were found for the vertical in-plane normal stress σ'_{22} as shown in Figure 5.31. The maximum value was also -67 MPa at the die center. Thus, there is a predicted state of biaxial compression at the center of the die. The stress distribution for σ'_{22} was similar to σ'_{11}, except rotated by 90°.

5.3.5 Underfill Curing Process

Modeling of additional packaging processes was done using a sequential approach including element birth for new materials added to the assembly. To model underfill dispense and cure, the final configuration (including the initial stress distribution) from the solder

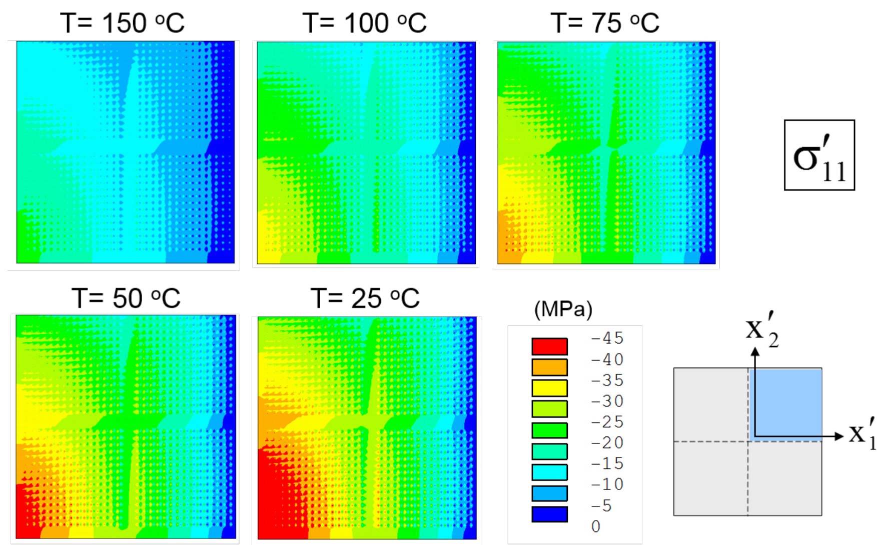


Figure 5.29: Die Stress Buildup During Cooldown After Solder Joint Reflow

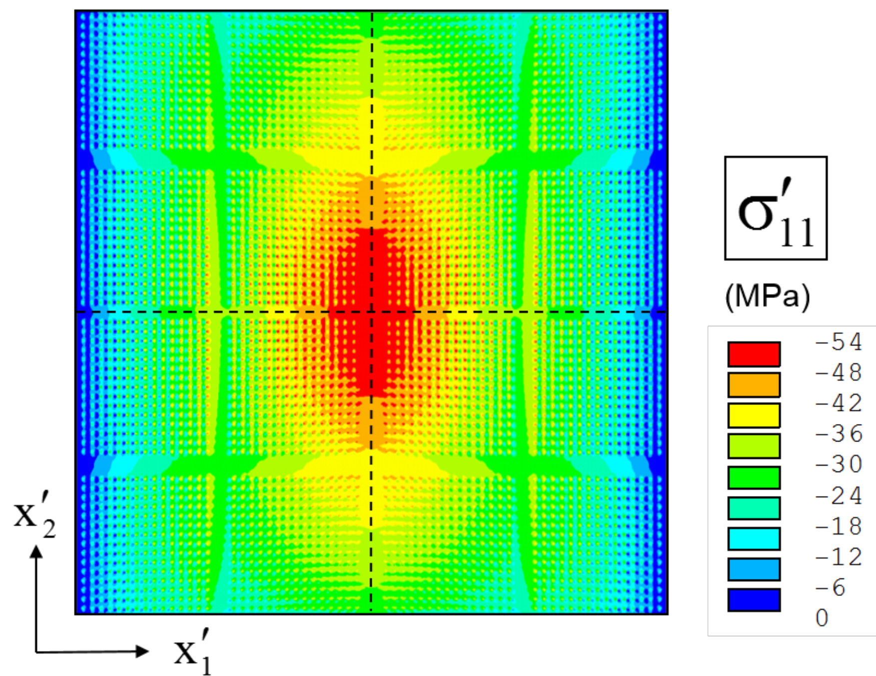


Figure 5.30: In-plane Normal Stress Distribution After Die Attachment

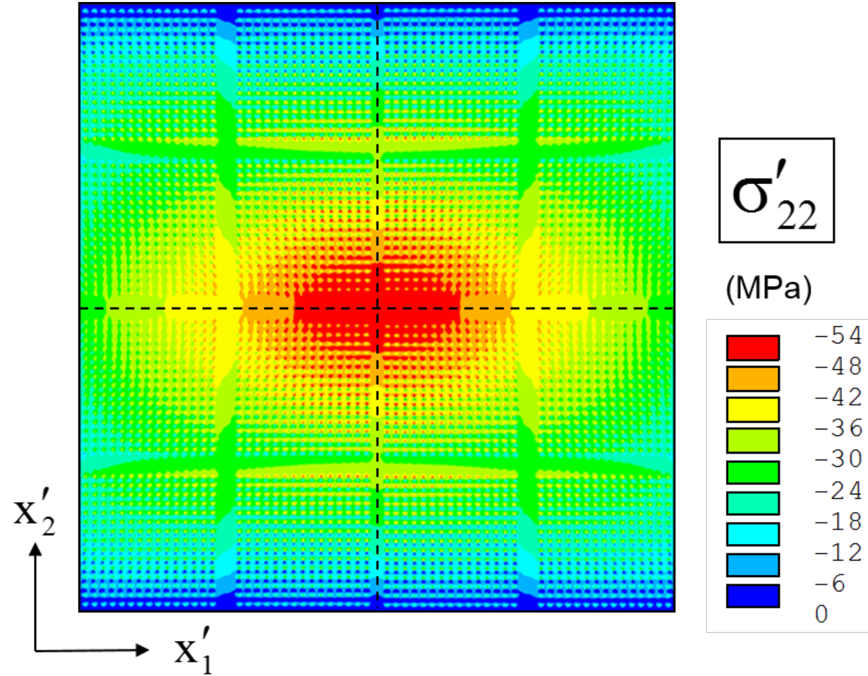
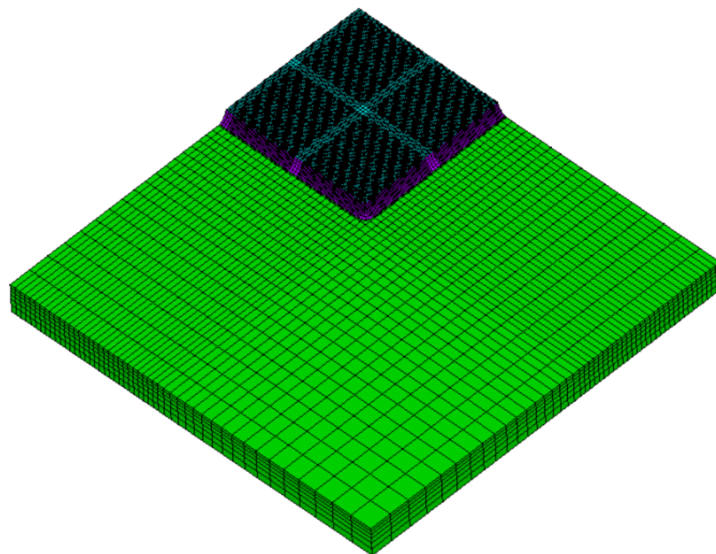


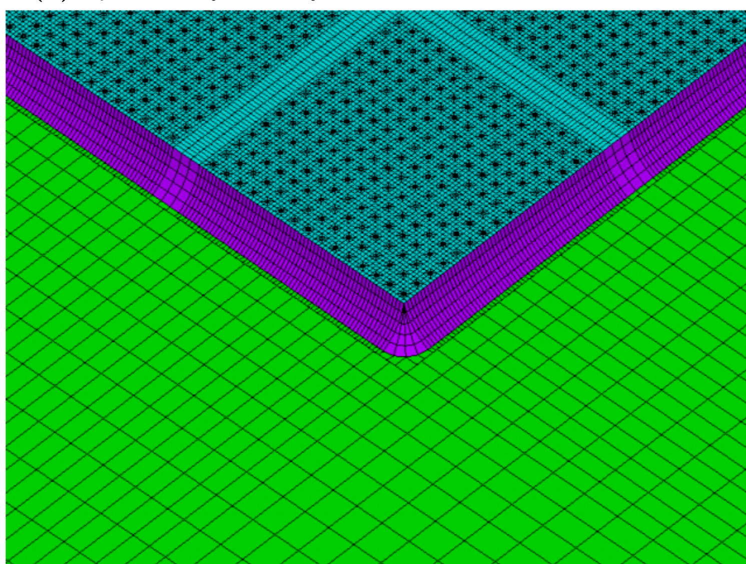
Figure 5.31: In-plane Normal Stress Distribution After Die Attachment

joint reflow model above was taken as the starting point. The quarter model simulating the underfill curing process was comprised of approximately 1.3 million linear and quadratic brick elements. A linear increase in temperature from 25 °C to 150 °C was applied at a rate of 10 °C per minute, and then the underfill material was added to the model by adding elements. The temperature was then reduced to room temperature to simulate the underfill curing process. The cooling profile was idealized based on thermocouple readings of the cooling of the underfill samples tested for Figure 5.26. The mesh for the underfill cure modeling is shown in Figure 5.32.

The predicted distribution of the in-plane horizontal normal stress σ'_{11} on die surface after the underfill curing process is shown in Figure 5.33. The maximum compressive stress value was again found to occur at the die center. Relative to the solder reflow stresses, the value at the die center was seen to nearly triple to about -190 MPa, which correlates well with the experimental results discussed earlier. The stress gradually decreases towards the edge of the die. The presence of an underfill fillet precludes the edge of the die from being a free surface. Thus, the horizontal normal stresses do not become zero at the left and right



(a) Quarter Symmetry Mesh for Underfill Cure Model



(b) Die and Underfill Fillet Detail

Figure 5.32: Quarter Symmetry Mesh for Underfill Cure Model with Detail

edges. At the corner of the die, the normal stress is -60 MPa, which is the minimum value across the die surface. It is also observed that the local stress concentrations near the solder balls were very small compared to those observed after solder joint reflow. Analogous results for σ'_{22} are shown in Figure 5.34. Again, the stress distribution for σ'_{11} was similar to σ'_{22}, except rotated by 90°.

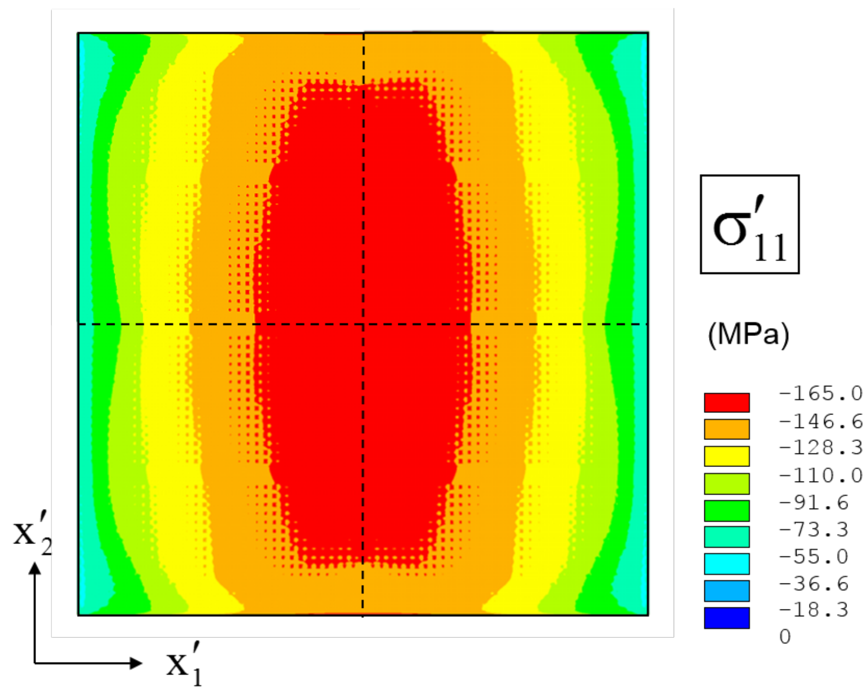


Figure 5.33: In-plane Normal Stress Distribution After Underfill Cure

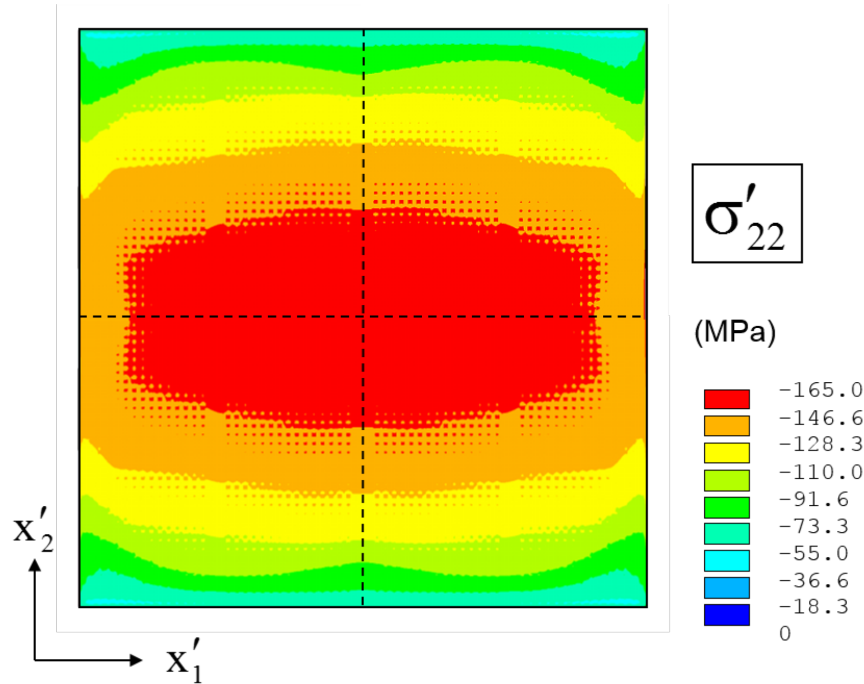
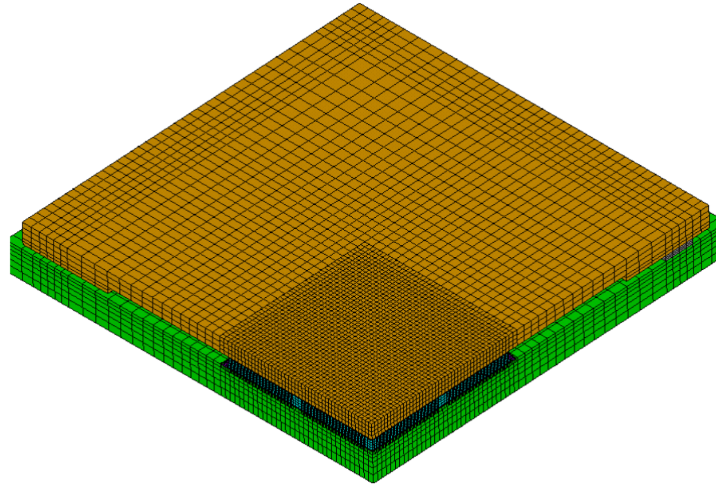


Figure 5.34: In-plane Normal Stress Distribution After Underfill Cure

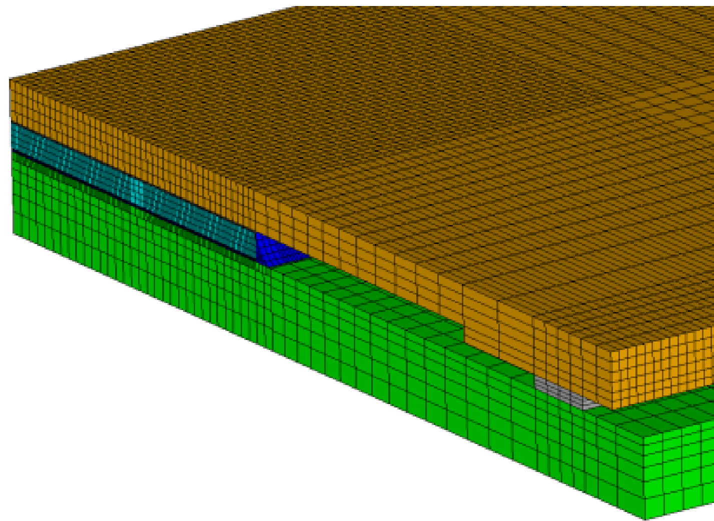
5.3.6 Lid Attachment Process

The lid attachment process is the last assembly step of the CLGA components. Continuing the sequential modeling of the manufacturing process, the final configuration (including the initial stress distribution) from the underfill dispense and cure model above was taken as the starting point. Approximately 1.35 million linear brick elements constituted the model of the lid attachment process. An increase in temperature from 25 °C to 150 °C was applied, and then the elements for the TIM1 layer and lid were added to finite element model. Finally, the temperature was reduced to room temperature to simulate the TIM1 curing process. The mesh for the lid attachment modeling is shown in Figure 5.35. In order to know the precise configuration of the TIM layer, a micro-focus x-ray system and microscopy cross-sectioning were used, as seen Figure 5.18 and Figure 5.19.

The predicted distribution of the in-plane horizontal normal stress σ'_{11} on die surface after the lid attachment and TIM1 curing process is shown in Figure 5.36. The maximum compressive stress value was again found to occur at the die center. Relative to the stresses



(a) Quarter Symmetry Mesh for Lid Attachment Model



(b) Die, Underfill Fillet, and Lid and TIM1 Detail

Figure 5.35: Quarter Symmetry Mesh for Lid Attachment Model with Detail

after underfill curing, the value at the die center was seen to increase about 10% to -205 MPa, which correlates well with the experimental results discussed earlier. Analogous results for σ'_{22} are shown in Figure 5.37. Again, the stress distribution for was similar to σ'_{11}, except rotated by 90°. The entire die surface continues to be in a state of in-plane biaxial compression.

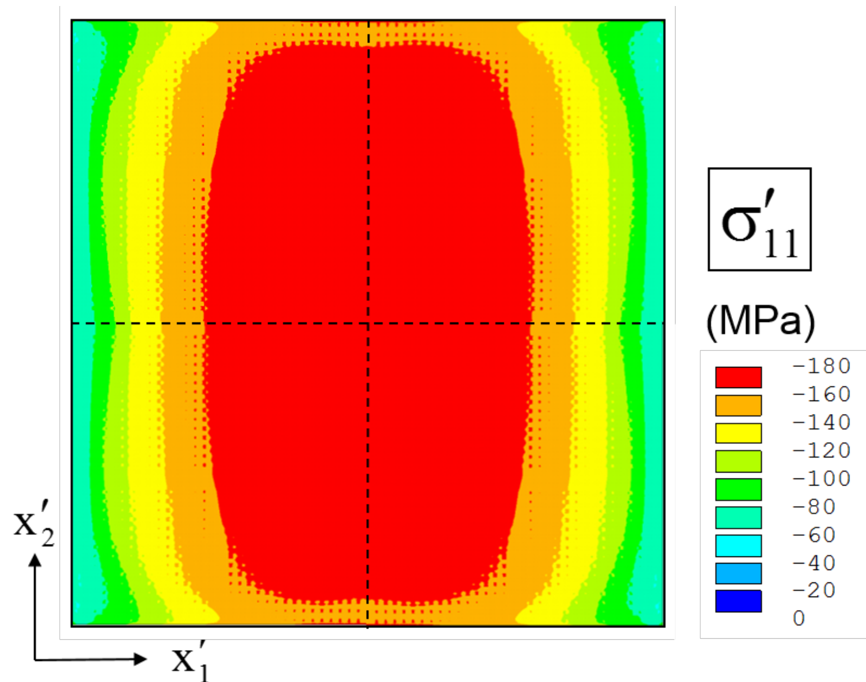


Figure 5.36: In-plane Normal Stress Distribution After Lid Attachment

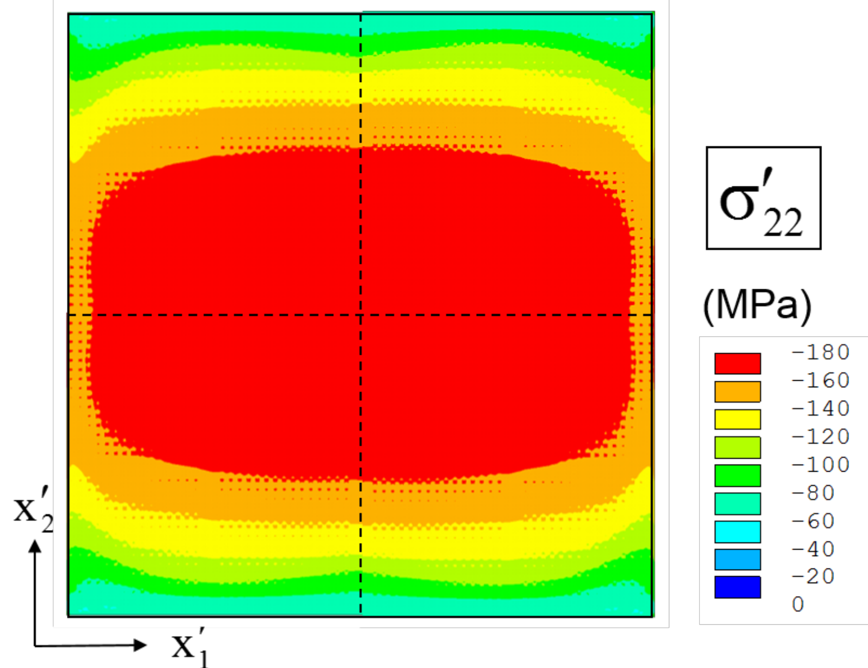


Figure 5.37: In-plane Normal Stress Distribution After Lid Attachment

5.3.7 Correlation with Experimental Measurements

Correlations of the finite element predictions and experimental stress test chip measurements for the horizontal normal stress are shown in Figures 5.38-5.40 for the solder reflow, underfill dispense and cure, and lid attachment assembly steps, respectively. The colored contours are the finite element results from Figures 5.30, 5.33, and 5.36. Small colored squares have been added at the sensor rosette locations, with the fill color of each square indicating the average experimental stress value at that rosette site. The maximum compressive stresses occur at the die center in each plot. For die attachment, the maximum compressive stress predicted by finite element model (Figure 5.38) was -67 MPa, whereas the experimental measurement was -75 MPa at the rosette site closest to the die center. After underfill curing, the maximum compressive stress predicted by finite element model (Figure 5.39) was -190 MPa, while the experimental measurement was -188 MPa at the rosette site closest to the die center. Finally, after lid attachment, the maximum compressive stress predicted by

finite element model (Figure 5.40) was -206 MPa, while the experimental measurement was -210 MPa.

Figure 5.38 shows good correlation of experimental and numerical die stress at the center of the die, but several other rosette sites do not appear to correlate well with the finite element simulation. To better understand the experimental and numerical results, several sites across the die were examined in detail. Figure 5.41 shows a micrograph of one such site. The outlined area in Figure 5.41 corresponds to the finite element mesh shown in Figure 5.42, which displays the image of the rosette site superimposed on the finite element mesh. The predicted contours for the in-plane normal stress σ'_{11} in the area of interest are shown in Figure 5.43. The finite element results indicate sharp stress gradients at each solder bump. The gradients also affect different areas of the rosette shown. While the overwhelming majority of the area shown is under approximately 50 MPa of compressive stress, areas of the sensor rosettes see as low as 25 MPa of compressive stress and as high as over 75 MPa of compressive stress. In effect, the rosette is measuring a weighted average of the stresses it is subjected to, including stress gradients across the area of the rosette. Ueta and Miura [179, 180] have confirmed the presence of stress gradients in flip chip die by placing much smaller piezoresistive test structures between flip chip bumps.

Figures 5.39-5.40 show better correlation than Figure 5.38 at most rosette sites. After underfill cure and lid attachment, the numerical predictions do not exhibit the extreme stress gradients near solder bumps, and thus better correlations were achieved.

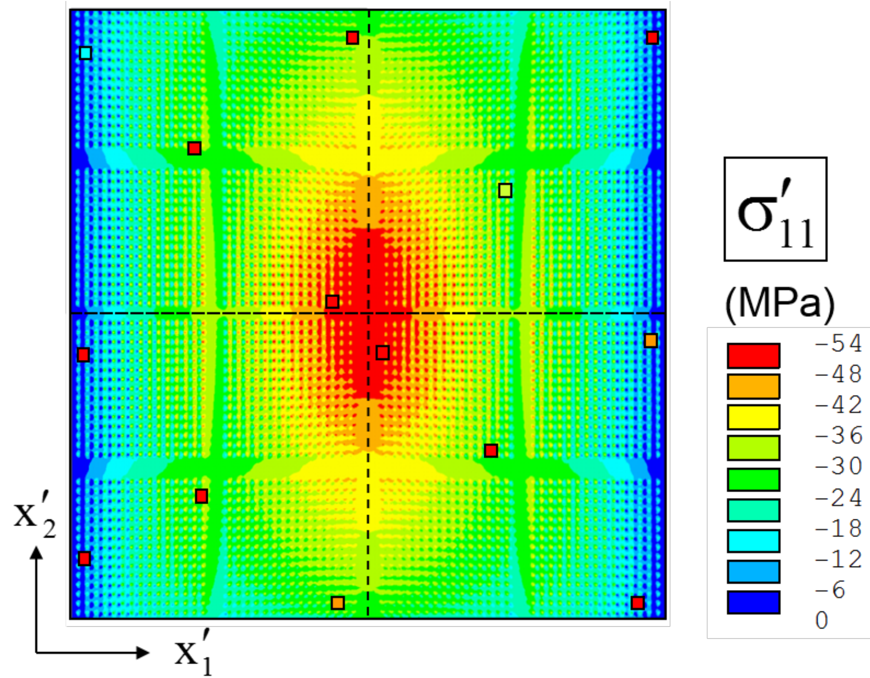


Figure 5.38: Correlation of FEA Predictions with Sensor Data (Solder Joint Reflow)

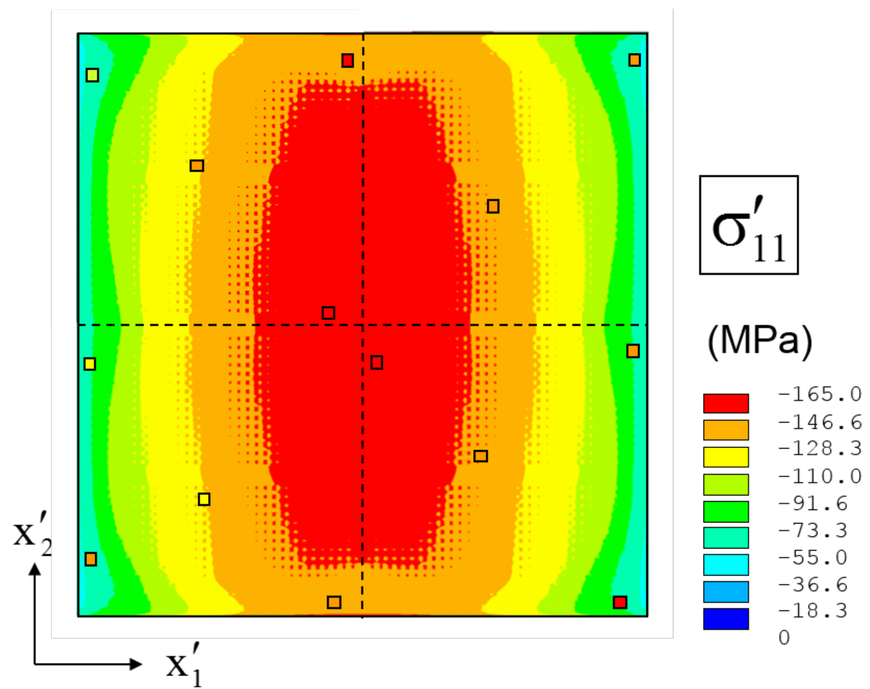


Figure 5.39: Correlation of FEA Predictions with Sensor Data (Underfill Cure)

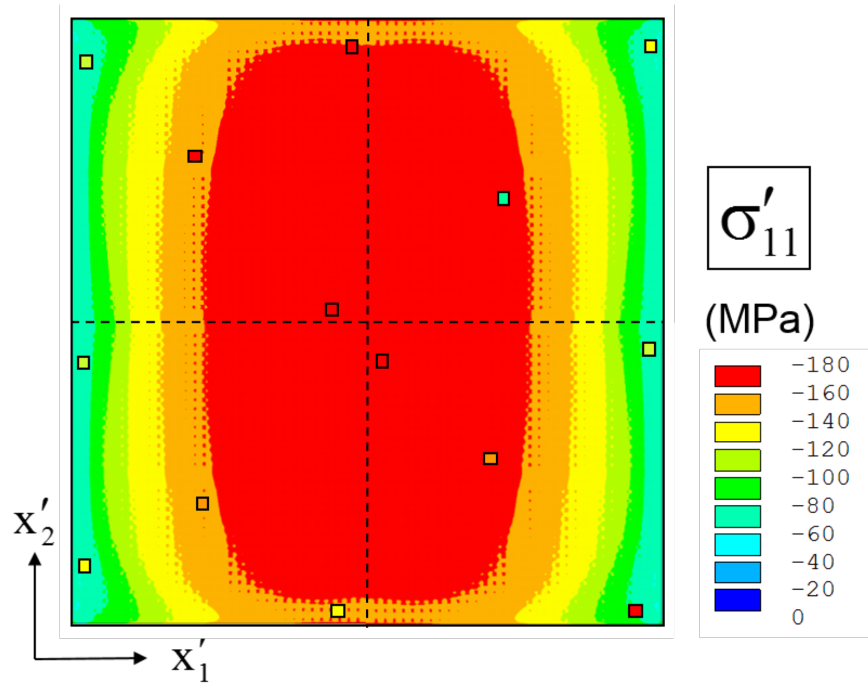


Figure 5.40: Correlation of FEA Predictions with Sensor Data (Lid Attachment)

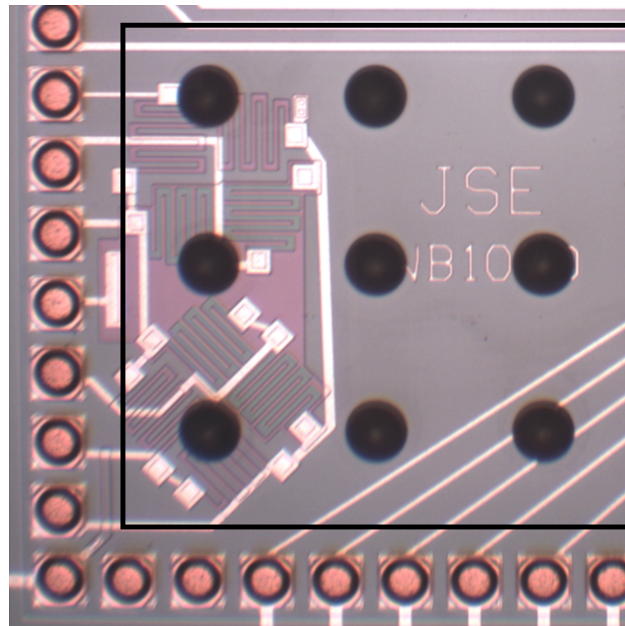


Figure 5.41: Micrograph of Rosette with Mesh Outline (Solder Joint Reflow)

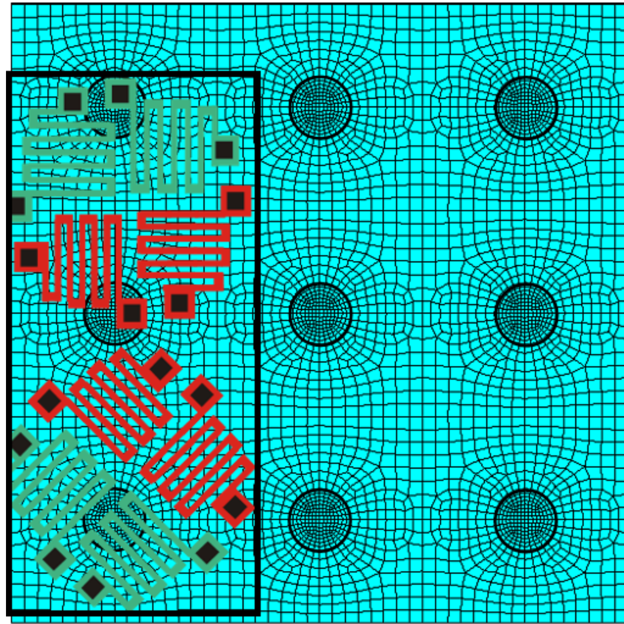


Figure 5.42: Finite Element Mesh with Rosette Superimposed (Solder Joint Reflow)

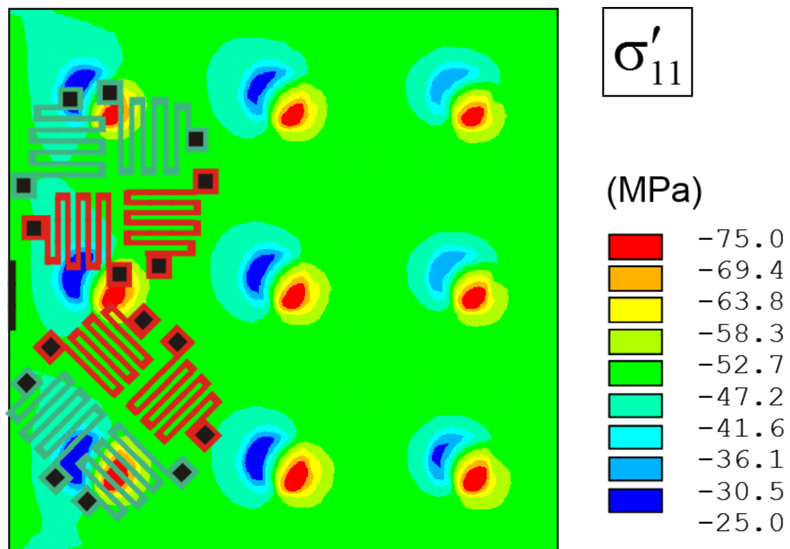


Figure 5.43: Stress Gradients near Solder Bumps (Solder Joint Reflow)

Chapter 6

Die Stresses Due to Thermal Exposures

A typical microprocessor in high-end computing and server applications will be subjected to a variety of mechanical, thermal, and electrical loadings. These loads will often be be coupled with each other. For example, increased temperature combined with materials of differing coefficients of thermal expansion will result in mechanical stresses, which in-turn may alter the device parameters of the processor. In this portion of the study, stress test chips were used to determine the effects of various temperature excursions on device side die stresses of microprocessor packages. The experimental results were again correlated with numerical simulations performed by Motalab [183, 184]. Three sets of experiments were performed. The first set of experiments aimed to gain an understanding of the effects of slow, quasi-static temperature changes on die stresses in CLGA assemblies. In a second set of experiments, discrete CLGA components were thermally cycled from low to high temperatures for thousands of cycles to understand the effects of thermal cycling on CLGA assemblies. Finally, measurements were taken in-situ during thermal cycling to understand the changing state of die stresses of a microprocessor package during thermal cycling.

6.1 Temperature Dependent Die Stresses

After first level packaging of the test chips, experiments have been performed to analyze the effects of slow (quasi-static) temperature changes on the die stresses. Several of the ceramic LGA components were subjected to controlled temperature change in a thermal chamber, and the sensor resistances were monitored in-situ. The temperature range for this set of experiments was chosen to be 0 °C to 100 °C based on the range experienced by microprocessors in use. While 0 °C represents an extreme low temperature, and likely

never actually seen in the field, 100 °C is very close to the upper range of the temperatures typically seen in large microprocessors in high-end and server applications.

In order to understand the effects of temperature on the die with only the first level of interconnection present, only the ceramic LGA assemblies were characterized. It was necessary to develop a new method to electrically access the test chip sensors at elevated temperatures. Due the thermally sensitive materials used in the flexible socket and the cables connecting to the test board, the socket and test board approach described in Chapter 5 was only effective at room temperature. To make sensor measurements in harsh environments, an innovative measurement system where the LGA components were electrically connected to a PCB using gold thermosonic wirebonds was developed (see Figure 6.1). The LGA was placed in a specially designed test board with a square hole in the center that was larger than the lid but smaller than the ceramic body, allowing for support and unconstrained in-plane expansion of the component. The temperature test board carrier is shown in Figure 6.2. Wirebonds were then made to interconnect the pads on the bottom of the component to the pads on the PCB. To enable robust wirebonding, an additional 30 μ-inches of gold was deposited on the LGA pads. If electrical access was required on pads far from the edges of the component, a wirebond stitching approach was used route the signal from the center of the package to the perimeter (see Figure 6.3). This stitching approach used dummy pads on the ceramic substrate that were not involved at routing out the 36 stress sensor rosettes.

The wirebonded LGA test assemblies were subjected to varying temperature using an environmental chamber as shown in Figure 6.4. The utilized thermal profile is shown in Figure 6.5. The samples were initially at room temperature (20 °C). They were then subsequently raised to 100 °C, followed by a temperature decrease to T = 0 °C, and finally brought back to room temperature. The temperature was changed in 10 °C increments, and the samples were allowed to equilibrate for 20 minutes at each temperature before measurements were made. Thus, the components were essentially subjected to one complete slow thermal cycle.

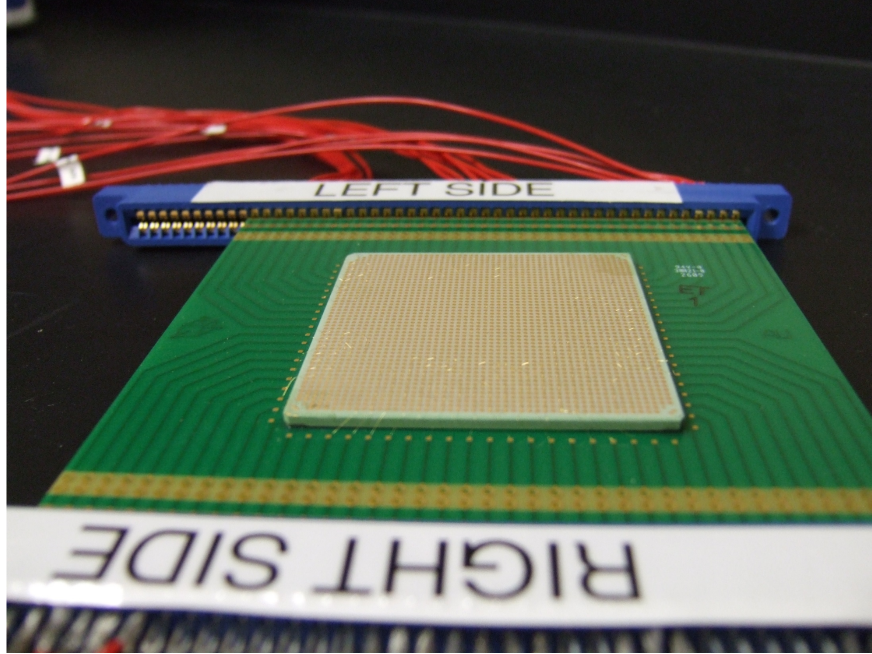


Figure 6.1: Wirebonded CLGA Test Assembly

The sensor rosettes were monitored at 6 selected sites across the die surface where the largest stresses occurred after assembly. This included the center, corners, and other points near the die edges. The results of the slow, quasi-static temperature changes showed that stress components at most locations varied linearly with temperature. For example, Figure 6.6 illustrates the measured variation of the horizontal in-plane normal stresses σ'_{11} with temperature at the center of the test die. The response is extremely linear, with the stress magnitudes being the highest at the low temperature extreme, and the lowest at the high temperature extreme. The die stresses in the LGA component should approach zero as the temperature in increased. The "stress free" temperature of chip should be near the lead free solder ball solidification temperature of approximately 221 °C. The linear trends shown in Figure 6.6 extrapolate to zero stress at approximately this temperature level. Results for σ'_{22} at the center of the die are shown in Figure 6.7. In-plane shear stress σ'_{12} at the center of the die is plotted for the same temperature range in Figure 6.8. The slope of the trend line through the data is linear with a slope near zero. This is expected, and helps validate the results as the in-plane shear should be unchanged near the intersection of two axes of

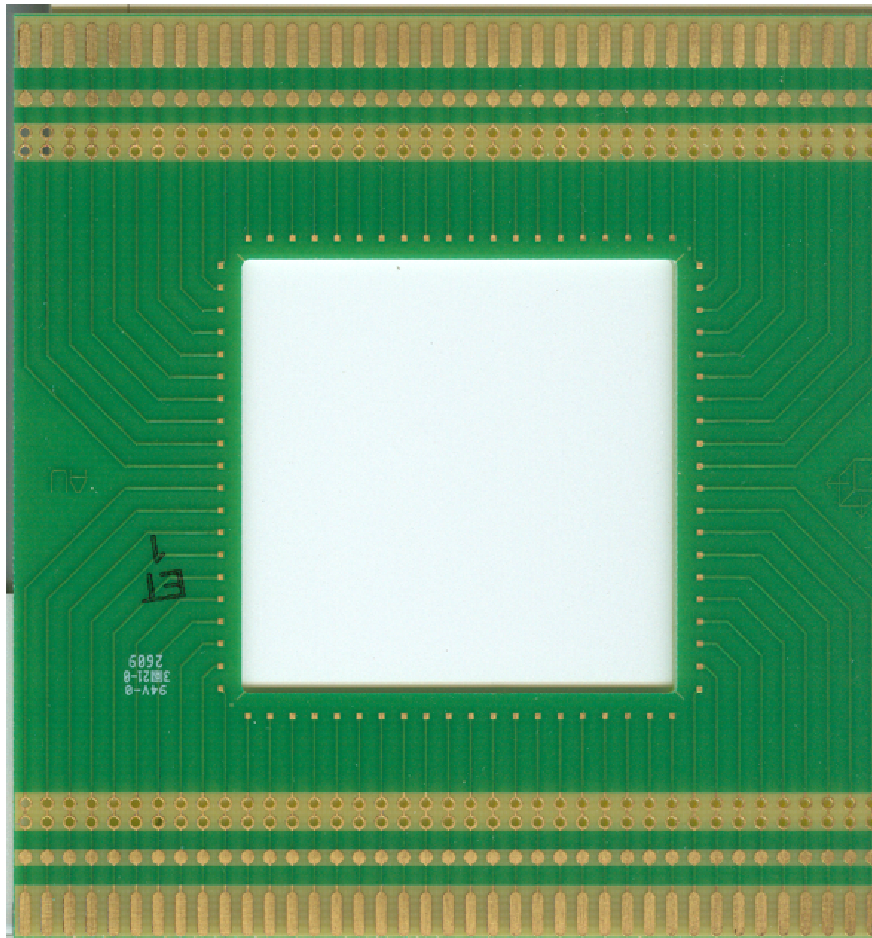


Figure 6.2: CLGA Temperature Test Board

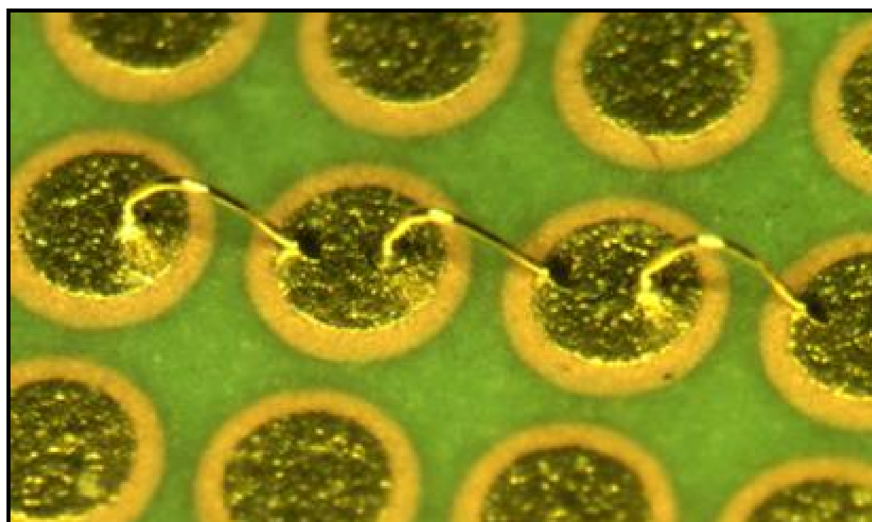


Figure 6.3: Wirebond Stitching on CLGA Lands

Figure 6.4: Thermal Chamber and DAQ

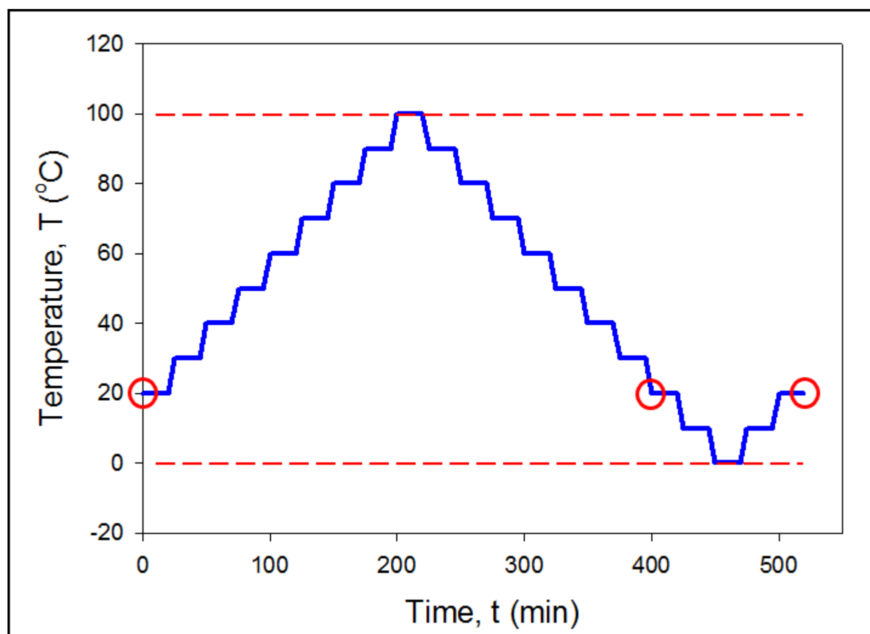


Figure 6.5: Thermal Profile for Temperature Dependent Stress Testing

symmetry. The non-zero slope is explained by the fact that the rosette in question is slightly off the die center.

Similar plots for σ'_{11}, σ'_{22}, and σ'_{12} at another rosette site near the center are shown in Figures 6.9 - 6.11. The results are very similar as this site is also very close to the center of the die. The differences in the responses of the normal stresses can be attributed to the differing locations of the two centrally located rosettes. The two sites are on opposite sides of the x'_1-axis of symmetry. The rosette with results shown in Figures 6.9 - 6.11 is also farther from the center of the die than the rosette shown in Figures 6.6 - 6.8. This explains the magnitudes of σ'_{12} in Figure 6.11. At points on the two axes of symmetry on the die, the in-plane shear stress should be identically zero. However, the offsets of the two rosettes from the symmetry axis leads to small, yet measurable changes in the in-plane shear stresses.

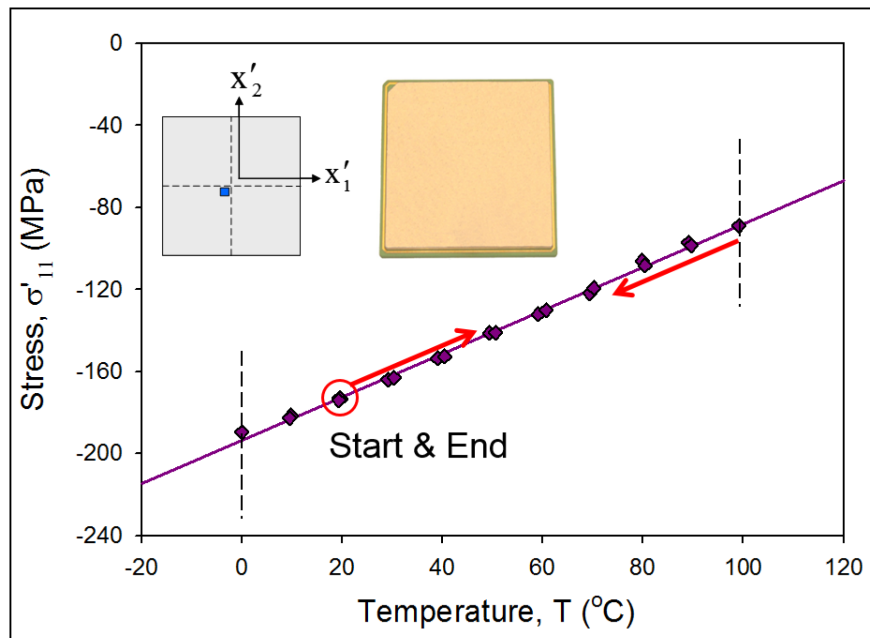


Figure 6.6: Variation of In-Plane Normal Stress with Temperature (Die Center)

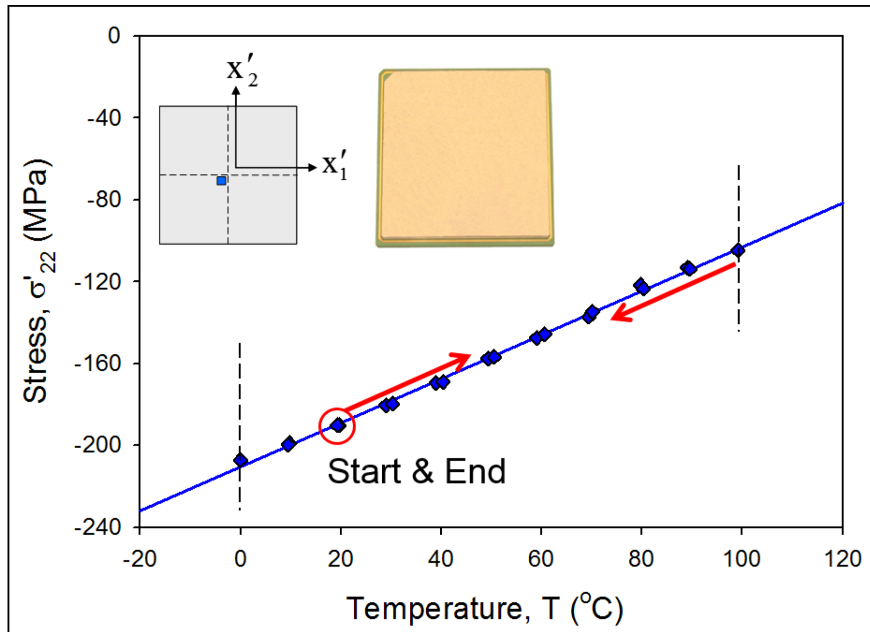


Figure 6.7: Variation of In-Plane Normal Stress with Temperature (Die Center)

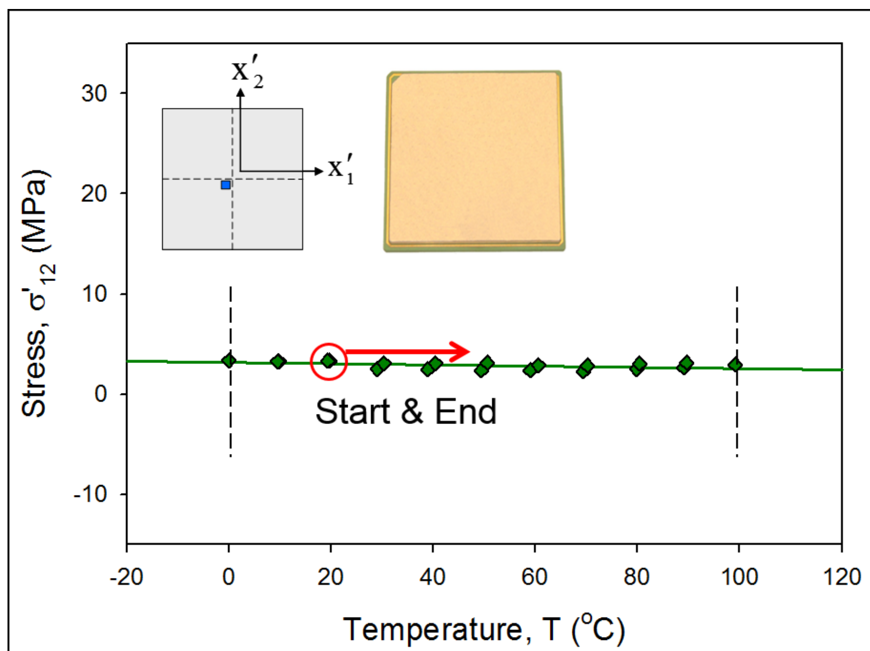


Figure 6.8: Variation of In-Plane Shear Stress with Temperature (Die Center)

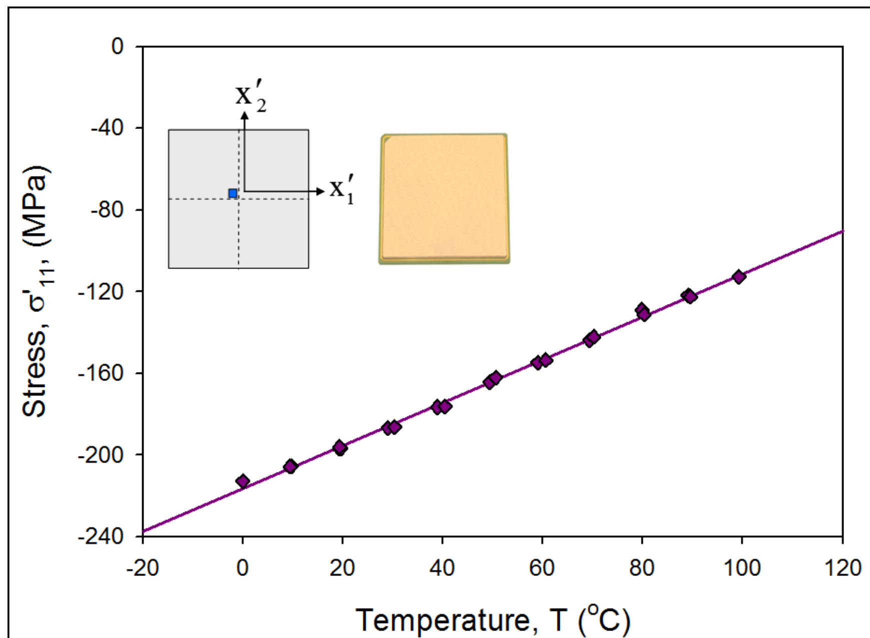


Figure 6.9: Variation of In-Plane Normal Stress with Temperature (Die Center)

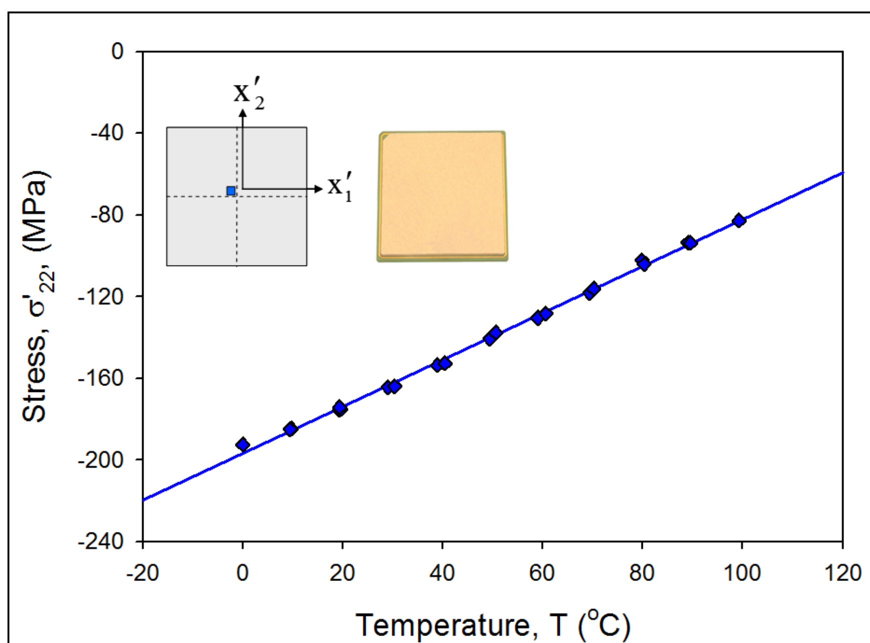


Figure 6.10: Variation of In-Plane Normal Stress with Temperature (Die Center)

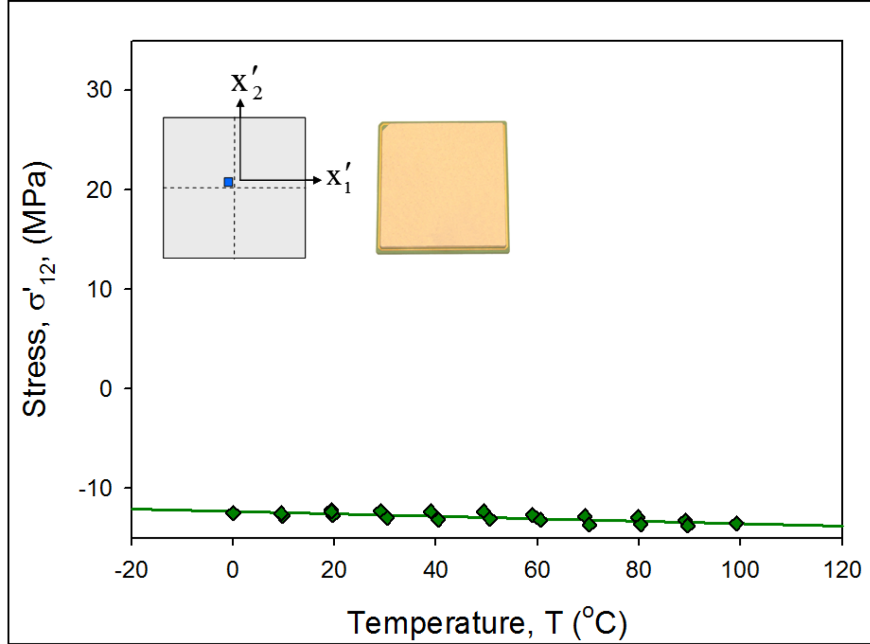


Figure 6.11: Variation of In-Plane Shear Stress with Temperature (Die Center)

Stresses extracted at the edge of the die during temperature change also showed a linear temperature dependence. In-plane normal stress σ'_{11} variations at the edge of the die near the x'_2-axis are shown in Figure 6.12. Analogous results for σ'_{22} are shown in Figure 6.13. While the slopes of the temperature responses of σ'_{11} and σ'_{22} are the same at the central rosette sites shown in Figures 6.6 - 6.7 and Figures 6.9 - 6.10, the slopes of the two in-plane normal stresses are significantly different at the center of the horizontal die edge. Variations of the shear stress σ'_{12} with temperature at the edge of the die are shown in Figure 6.14. A non-zero slope of σ'_{12} is again observed due to the off-axis location of the rosette.

The die corners were the only points on the die surface showing exception to the linear temperature dependencies. For example, Figure 6.15 illustrates the measured variation of the in-plane normal stress σ'_{11} with temperature. The responses for this stress component and others at the corner became non-linear at temperatures near the upper extreme of T = 100 °C. In addition, the responses showed hysteresis. These effects are likely due to the higher creep-plasticity occurring in the underfill and solder materials in the corner regions

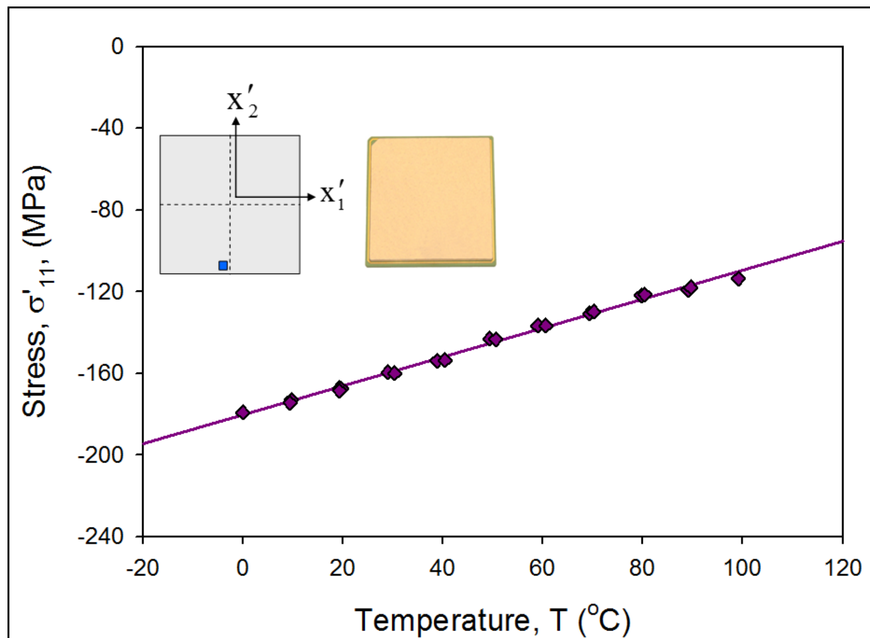


Figure 6.12: Variation of In-Plane Normal Stress with Temperature (Die Edge)

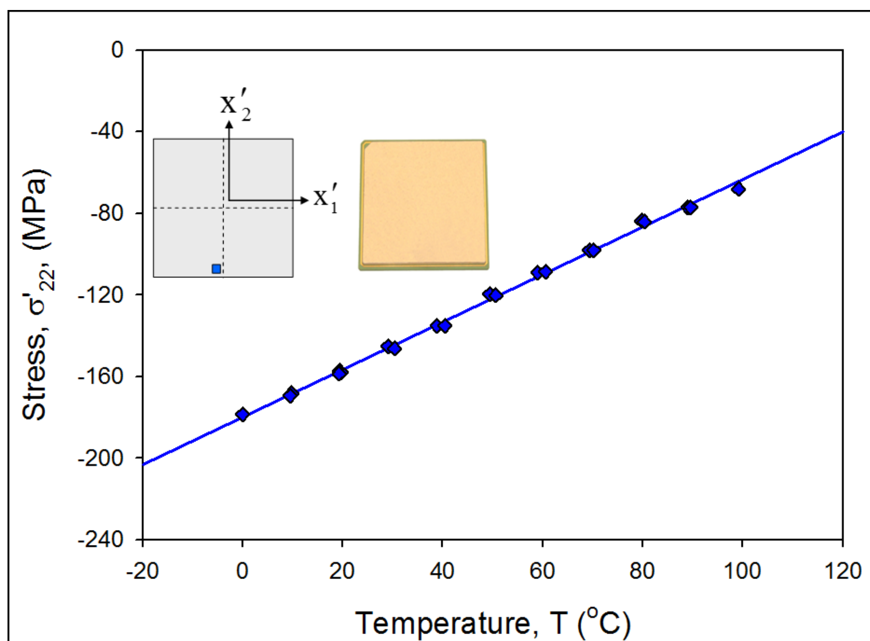


Figure 6.13: Variation of In-Plane Normal Stress with Temperature (Die Edge)

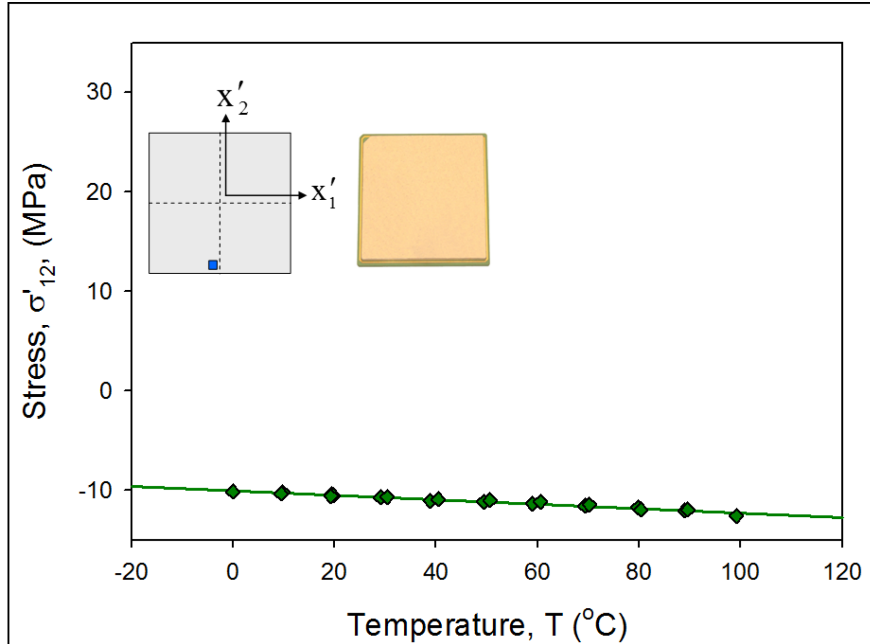


Figure 6.14: Variation of In-Plane Shear Stress with Temperature (Die Edge)

where the highest shear stresses exist, as shown by finite element results detailed later. Plots of σ'_{22}, σ'_{12}, σ'_{13}, and σ'_{23} at the corner site are shown in Figures 6.16 - 6.19.

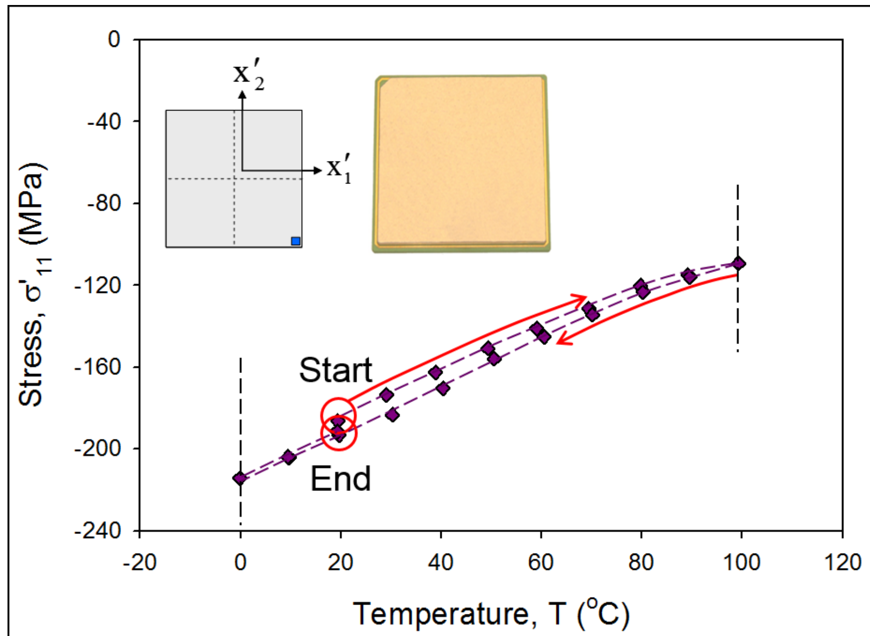


Figure 6.15: Variation of In-Plane Normal Stress with Temperature (Die Corner)

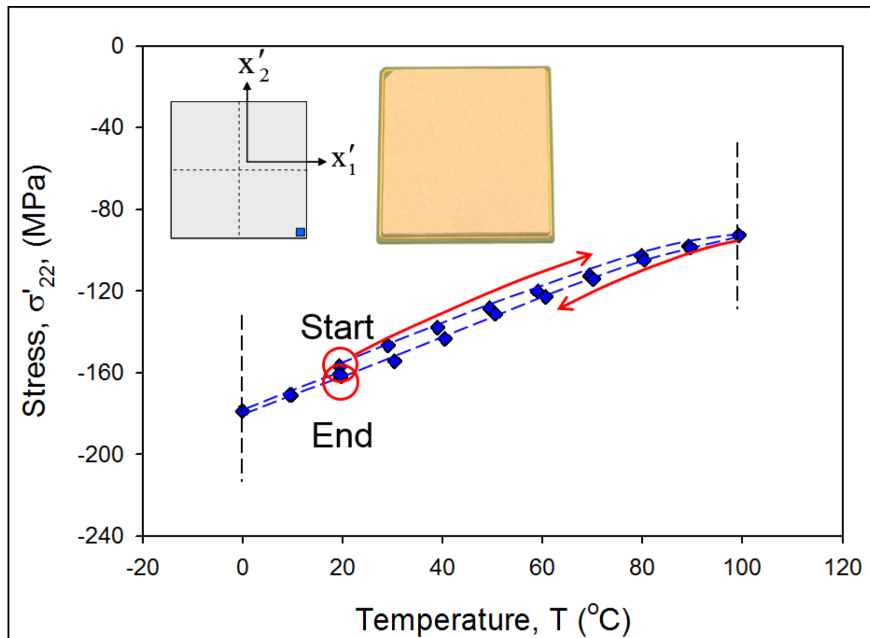


Figure 6.16: Variation of In-Plane Normal Stress with Temperature (Die Corner)

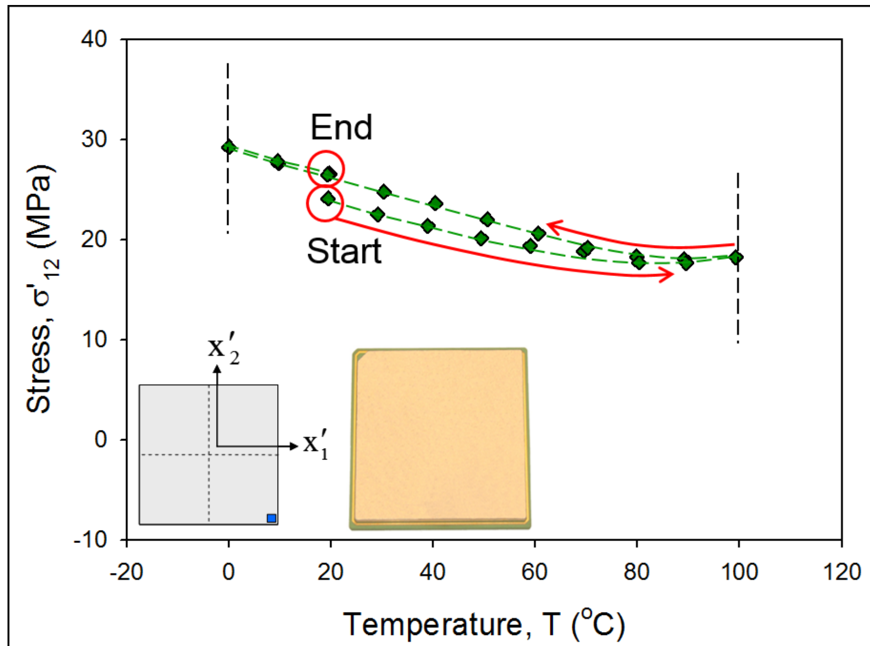


Figure 6.17: Variation of In-Plane Shear Stress with Temperature (Die Corner)

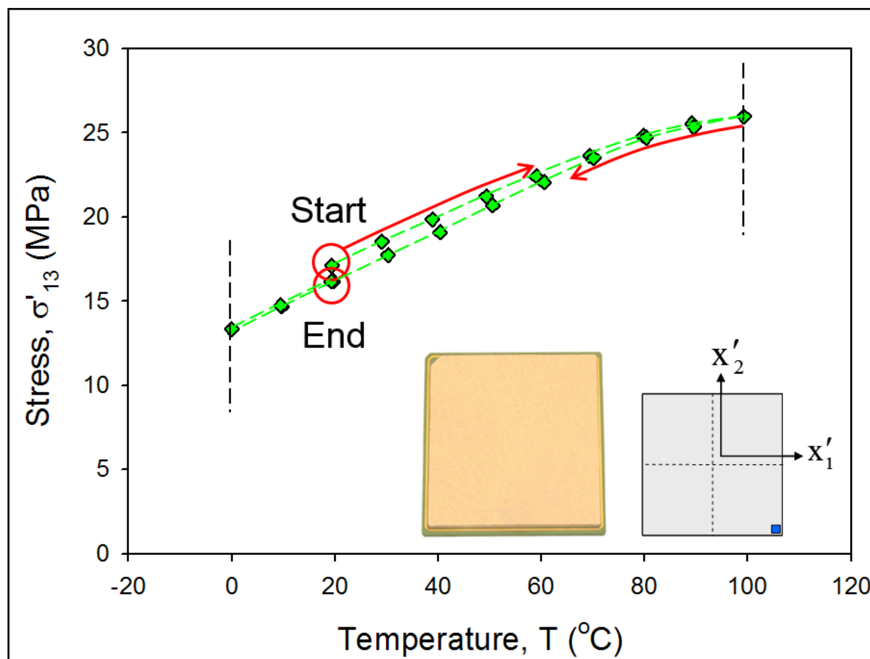


Figure 6.18: Variation of Out-of-Plane Shear Stress with Temperature (Die Corner)

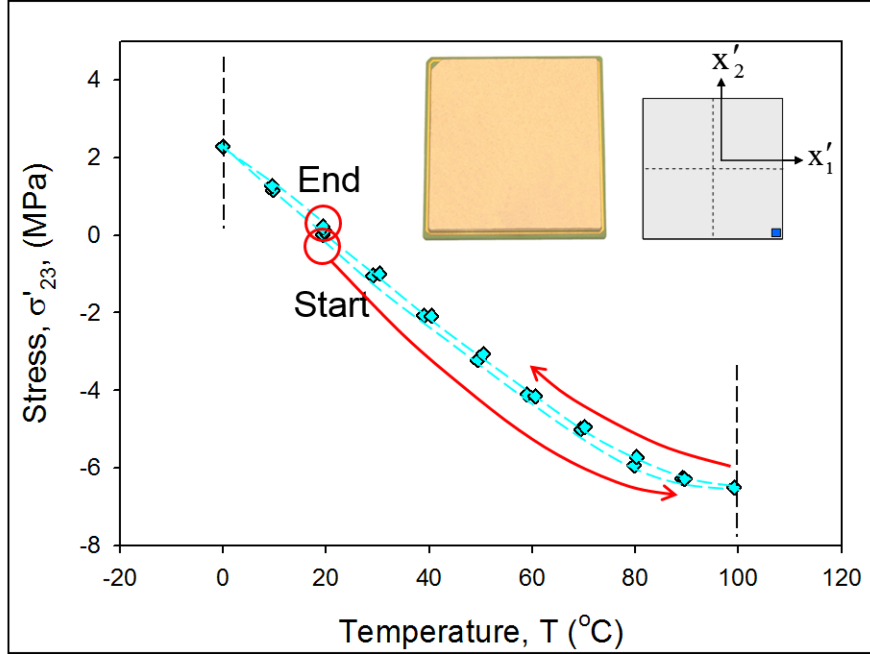


Figure 6.19: Variation of Out-of-Plane Shear Stress with Temperature (Die Corner)

6.1.1 Numerical Predictions of Temperature Dependent Die Stresses

Finite element models were developed by Motalab [184] to predict die stresses occuring in the slow, quasi-static temperature change experiments on the CLGA components. As discussed in previous chapters, the model began with the fully assembled package in the CLGA configuration, including residual stresses induced by the assembly processes. The FEA model was then subjected to the thermal profile in Figure 6.5, and the predicted stresses were extracted at the end of each 20 minute period of constant temperature. Figure 6.20 shows the predicted variation of the horizontal normal stress at the die center with temperature. The experimental values for one of the components from Figure 6.6 were included for comparison purposes. Both sets of results indicate a linear response with temperature. The magnitudes of the predicted and measured stresses are very similar, especially in the range of 20 to 60 °C. Figure 6.21 details analogous comparisons for the in-plane shear stress at the corner of the die. Both the experimental and FEA results show a non-linear response with temperature change, especially at elevated temperatures. Both results also show hysteresis in the stress response. The finite element calculations have shown that there are large inelastic deformations of

the underfill material in this region. A plot of the predicted equivalent plastic strain in the underfill of the CLGA assembly is shown in Figure 6.22. The plot shows areas of large plastic strain in the area of the underfill contacting the corner of the die.

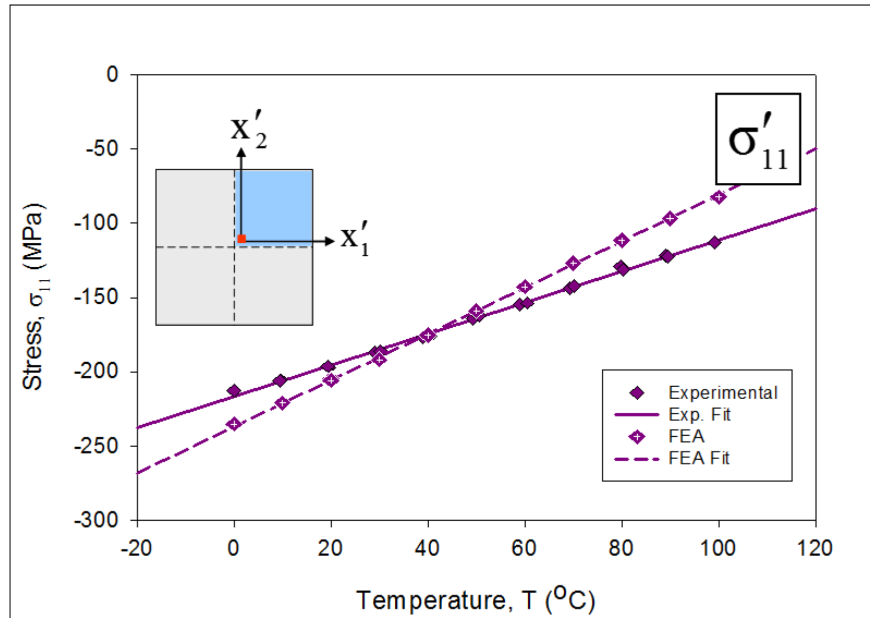


Figure 6.20: FEA Correlation of In-Plane Normal Stress with Temperature (Die Center)

It is also noted that the predicted and experimental stress values in Figures 6.20 - 6.21 are significantly different, especially at the high and low temperature extremes. This is likely due to the fact that the experimental result is from a single sample package, and that inclusion of additional sample data and averaging of the results will enhance correlation. In addition, the finite element model itself is an idealization of the geometry of the packages and cannot fully account for all manufacturing deviations among all samples. For these reasons, it may be more prudent to compare stress changes when the experimental results are for a single package (i.e. the additional stress induced by a process, condition, or loading), rather than to compare absolute stresses.

Figure 6.23 shows the predicted variations of the horizontal normal stress change at the die corner with temperature, along with the analogous experimental values from one of the

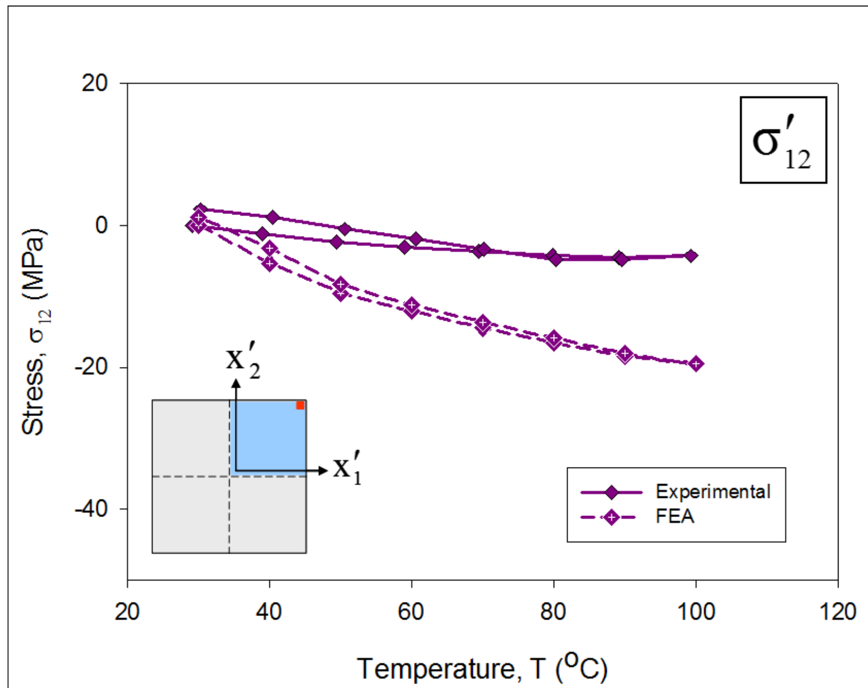


Figure 6.21: FEA Correlation of In-Plane Shear Stress with Temperature (Die Corner)

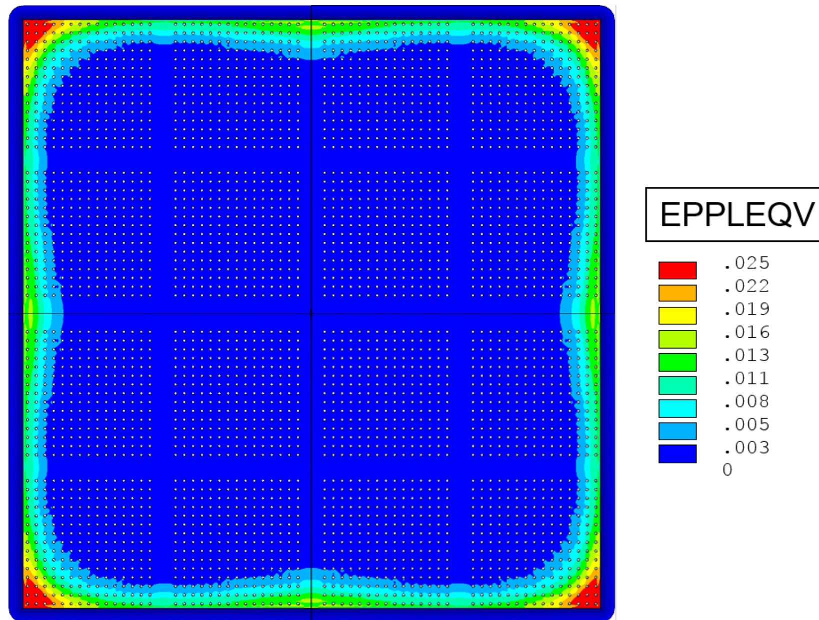


Figure 6.22: FEA Prediction of Equivalent Plastic Strain in Underfill

packages. In this case, the initial loading shows a seemingly linear response through most of the temperature range, becoming slightly non-linear at the upper region of the range. Both results also show hysteresis, again indicating inelastic behavior of the underfill material in the corner of the die with just one slow thermal cycle.

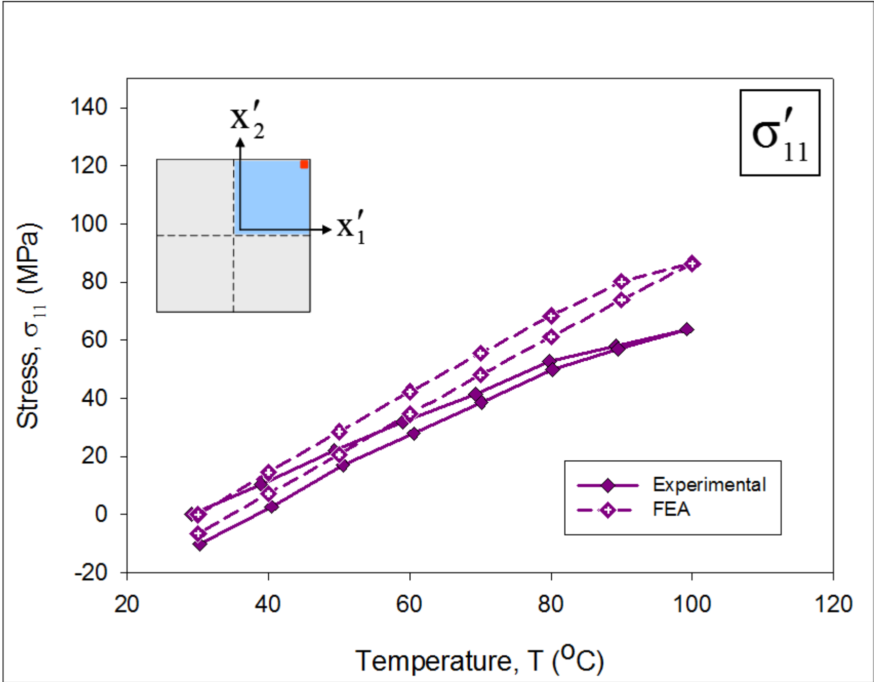


Figure 6.23: FEA Correlation of In-Plane Normal Stress with Temperature(Die Corner)

6.2 Die Stresses Due to Thermal Cycling

Accelerated Life Testing (ALT) is normally performed using thermal cycling, where the test assemblies are subjected to harsh changes in temperature over a much shorter period of time than the expected field exposure of the parts. The range of temperature is also often much greater than the true application environment. The goal is to then use the ALT data to predict/estimate the reliability. This process also allows the determination of various characteristics of the packaging architecture during its life cycle, i.e. critical locations, failure modes, stress levels, etc. Subjecting a component to high stress levels not only allows for the

study of failures during a life cycle, it also enables reduction of the time required to make design improvements, component choices, and material selections.

Several of the ceramic LGA components were also exposed to long term thermal cycling from 0 to 100 °C in the Blue M environmental chamber shown in Figure 6.24 using the 40 minute per cycle profile shown in Figure 6.25. In total, 18 CLGA assemblies were subjected to a total of 9000 thermal cycles. In this part of the thermal exposure study, the packages were not monitored in-situ, but were removed from the environmental chamber at selected levels of cycling. At each increment of cycling, the test chip sensor resistances were measured at room temperature using the PC based data acquisition system discussed previously.

Figure 6.24: Blue M ETC-16 Environmental Chamber used for Thermal Cycling

The thermal cycling tests were performed in a staged fashion with several different rounds of testing. Each stage consisted of a minimum of 50 cycles, with intervals of 100 and 500 cycles included as testing progressed. Initially the assemblies were cycled in a chamber

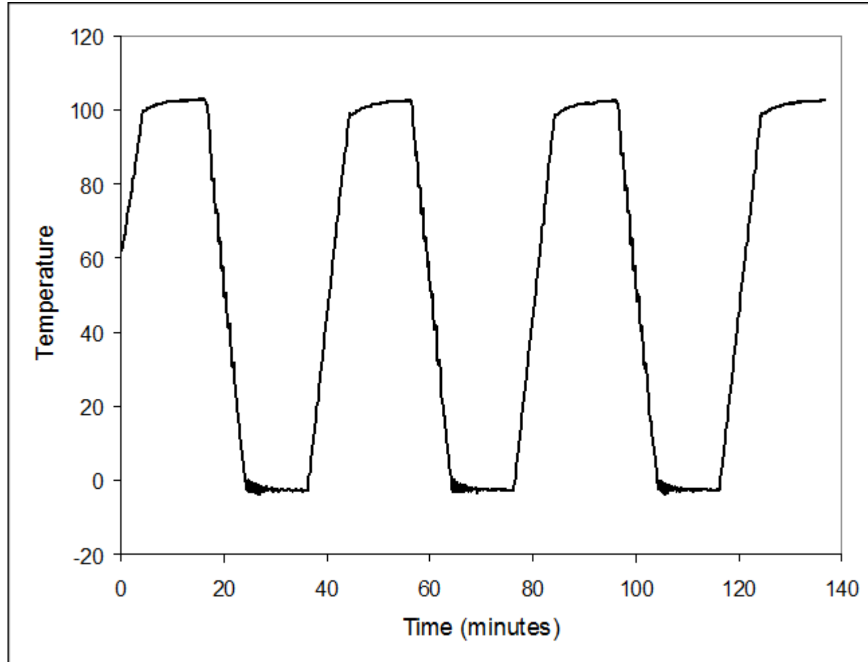


Figure 6.25: Thermal Cycling Profile (40 Minute Cycle)

for 50 cycles, then removed and measured at room temperature. Changes in the stress state of the die occur early in the cycling process, making it necessary to measure so often. After little change was seen after several increments of 50 cycles, the schedule was changed to remove the packages every 100 cycles. At 1000 cycles no significant change in die stress was observed, and the decision was made to remove the assemblies for measurement at 500 or 1000 cycle increments. Later in the process, anomalies in the data prompted the assemblies to be measured at 250 cycle increments.

In total, 36 measurement rosettes were tested at each cycling interval. Consistent with our initial (non-cycled) data, the largest values of the in-plane normal stresses were always found at the center of the die, and the highest values of the in-plane shear stress were always found at the corners of the die. The most drastic changes in the stress values with respect to cycle count were found early on, within the first 250 cycles. After the 250 cycle mark, stress values across the die "settle", and remained constant. Figure 6.26 shows the average normal stress values at the center of the die as a function of the number of thermal cycles for 18 samples. The average shear stress values at the center of the die are shown in Figure 6.27.

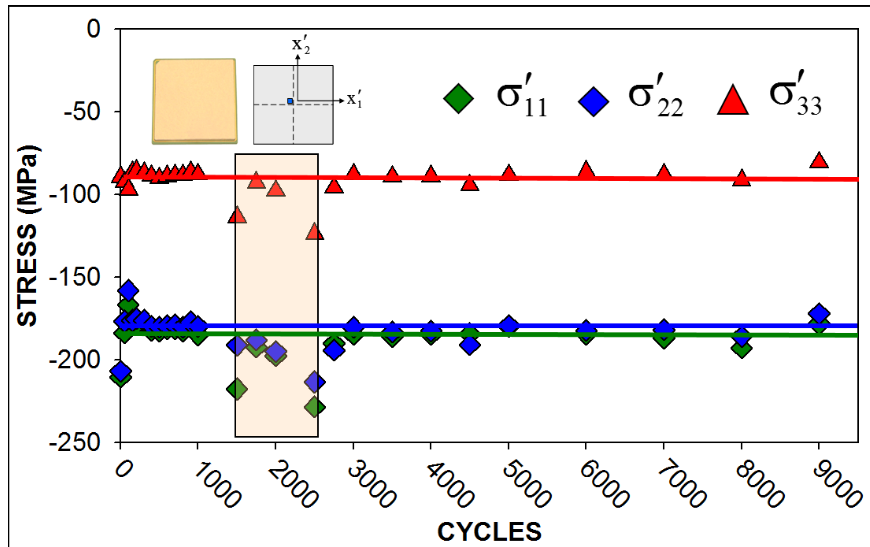


Figure 6.26: Variation of the Average Normal Stresses with Thermal Cycling (Die Center)

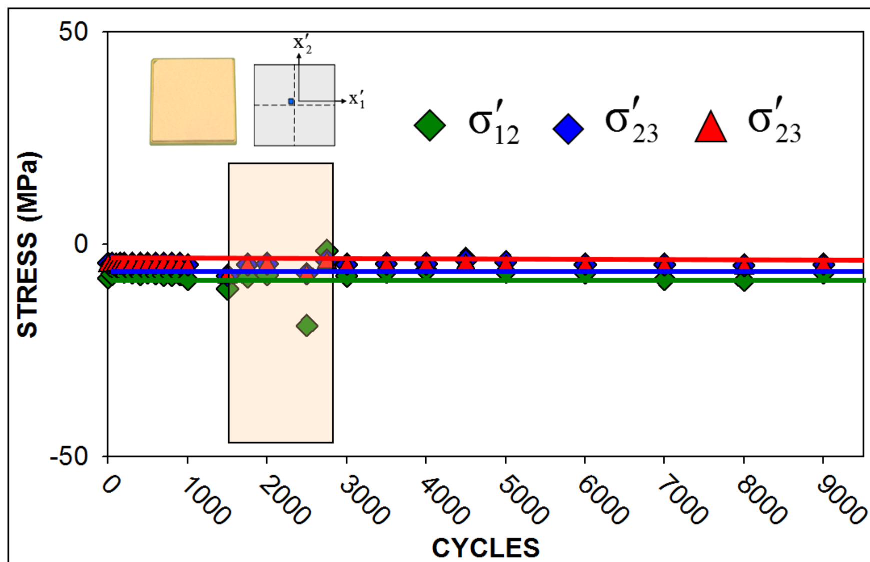
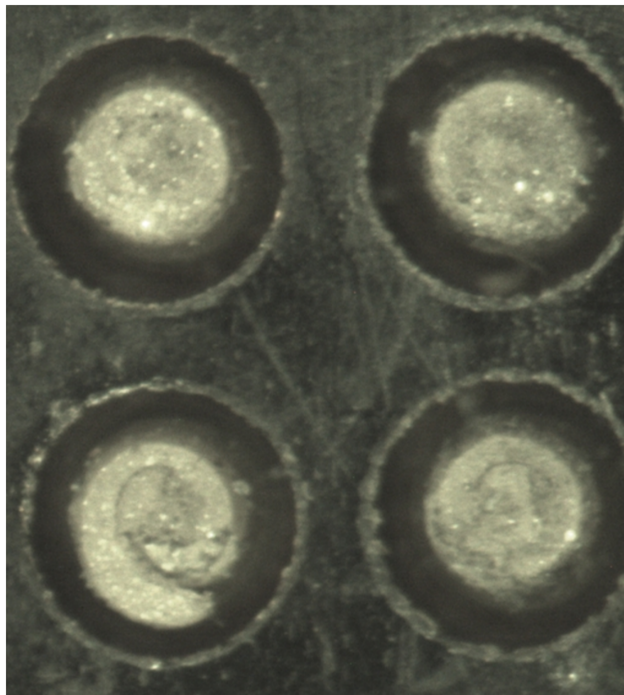


Figure 6.27: Variation of the Average Shear Stresses with Thermal Cycling (Die Center)

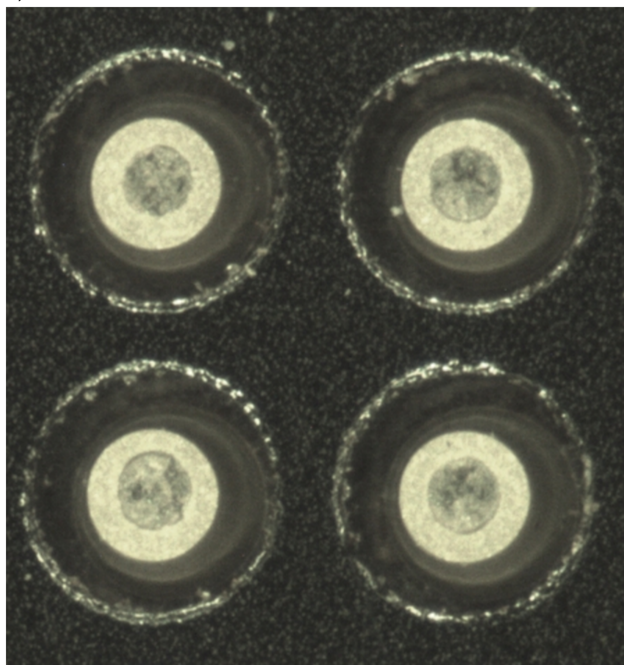
It is noted that the normal stress values shown in Figure 6.26 deviate from the trend line from approximately 1750 cycles to 2500 cycles (shaded region). From previous studies on flip chip die stresses during ALT [14, 185–187], it was expected that the die stress values would decrease in magnitude as the thermal cycling progressed. This is due to degrading solder properties and underfill delamination, among other factors. The values deviating from the trend line increased in this case, causing further investigation. The effects of clamping the packages into a test socket have been documented [181, 183]. Upon close examination of the test socket, it was found that the contact pins of the socket had degraded after approximately 750 insertions. The differences between a new socket and a socket after multiple insertions are shown in Figure 6.28. As the socket wears, it needs increased clamping pressure to make sufficient electrical contact. This increased pressure was applied unknowingly by the operator, and caused unintended additional die stress. After 2500 thermal cycles, the parts were tested with a new socket and the values were back along the trend line.

Analogous plots of the variations of the six stress components at the die corner are shown in Figure 6.29 and Figure 6.30. It is observed that the effects of the worn socket were less at the corner of the die. In all locations on the die, the stress values have been observed to remain extremely stable with thermal cycling, suggesting that the package is extremely reliable for the temperature ranges under consideration.

Of the 18 components selected for long term thermal cycling, a subset of 5 assemblies contained test die that were characterized at several rosette sites in addition to the die center and corner. These additional sites are shown in Figure 6.31. Average normal stresses for the five assemblies at all twelve sites are shown in Figures 6.32 - 6.43 . Most of the data follows the same trends as seen previously. After initial changes in the first 250 cycles, the stresses became relatively constant. Various sites were found to be affected more than others by the socket wear issue in measurements from 1750 to 2500 cycles. The data in these plots were measured averages from 5 assemblies and show slightly more variability from cycle to cycle than the data containing the averages of 18 assemblies. In Figures 6.35 and 6.42, the normal



(a) Close-up Image of Socket After ≈750 Insertions



(b) Close-up Image of Unused Socket

Figure 6.28: New and Old CLGA Socket

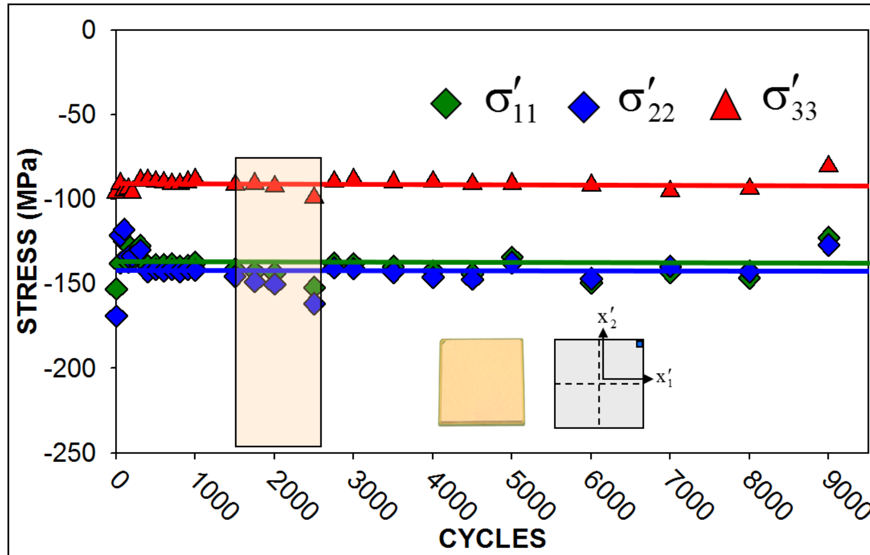


Figure 6.29: Variation of the Average Normal Stresses with Thermal Cycling (Die Corner)

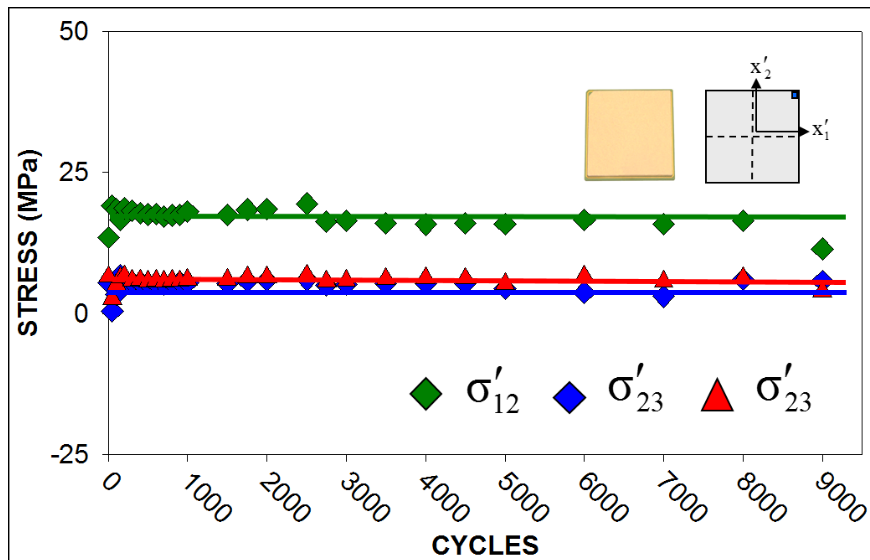


Figure 6.30: Variation of the Average Shear Stresses with Thermal Cycling (Die Corner)

stresses deviate from the trend established through the first 6000 to 7000 thermal cycles. A non-destructive physical and electrical evaluation was performed on the the three assemblies showing changes, with no outstanding reason found for the change. A destructive analysis of the assemblies was ruled out in case of future need for the samples.

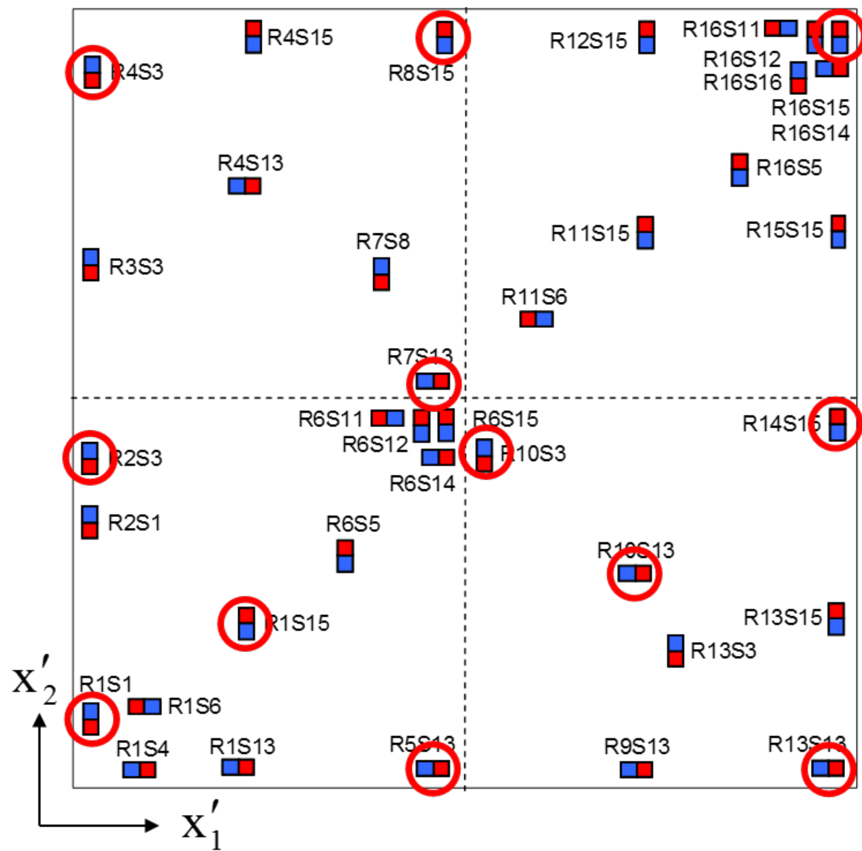


Figure 6.31: Test Chip Rosette Sites for Stress Measurement

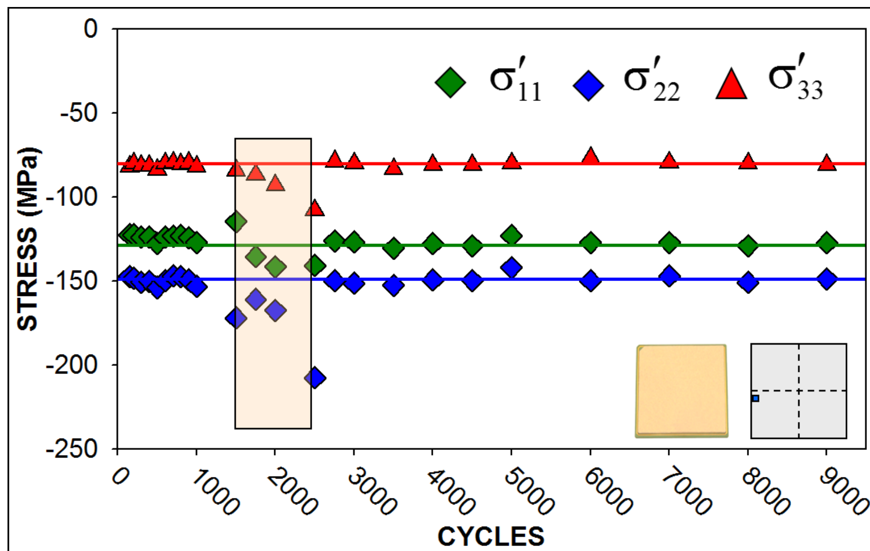


Figure 6.32: Variation of the Average Normal Stresses with Thermal Cycling

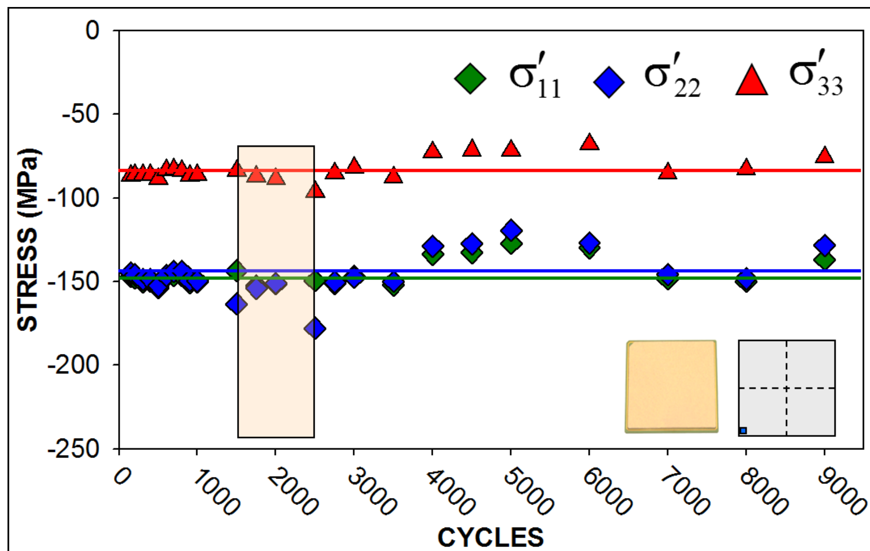


Figure 6.33: Variation of the Average Normal Stresses with Thermal Cycling

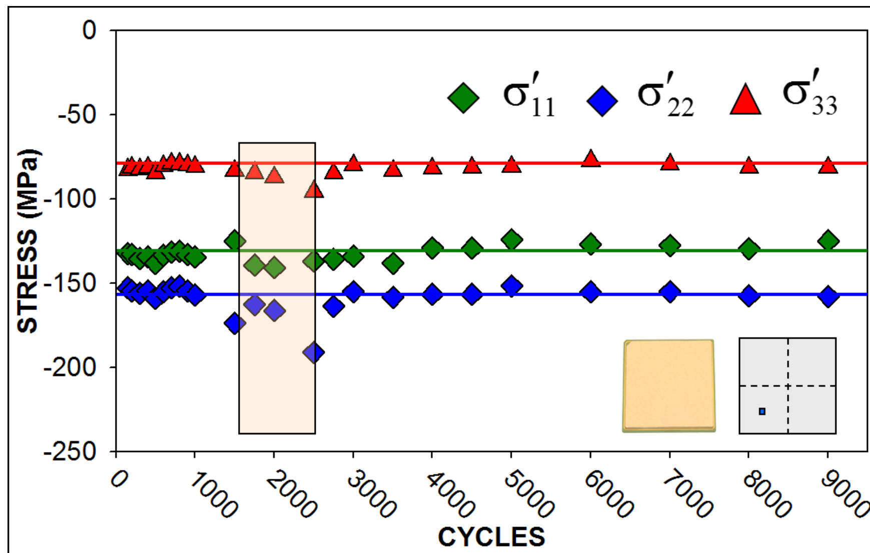


Figure 6.34: Variation of the Average Normal Stresses with Thermal Cycling

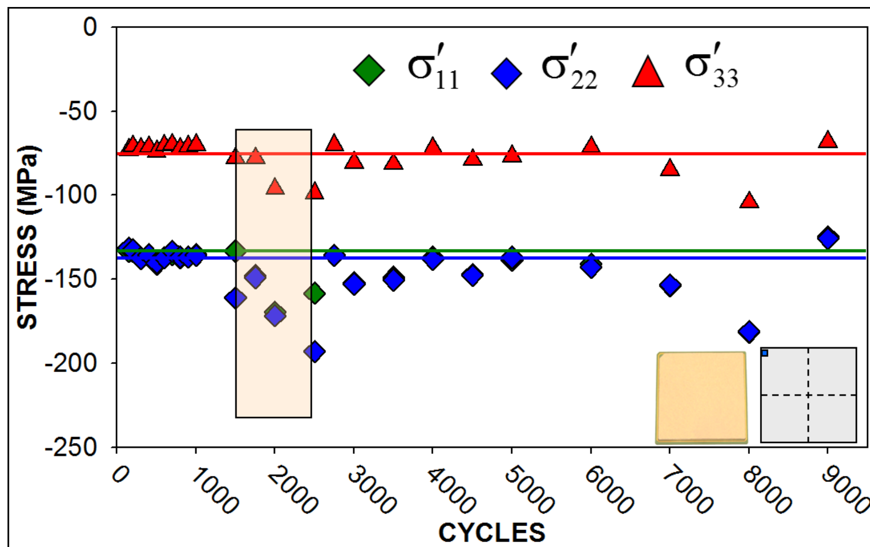


Figure 6.35: Variation of the Average Normal Stresses with Thermal Cycling

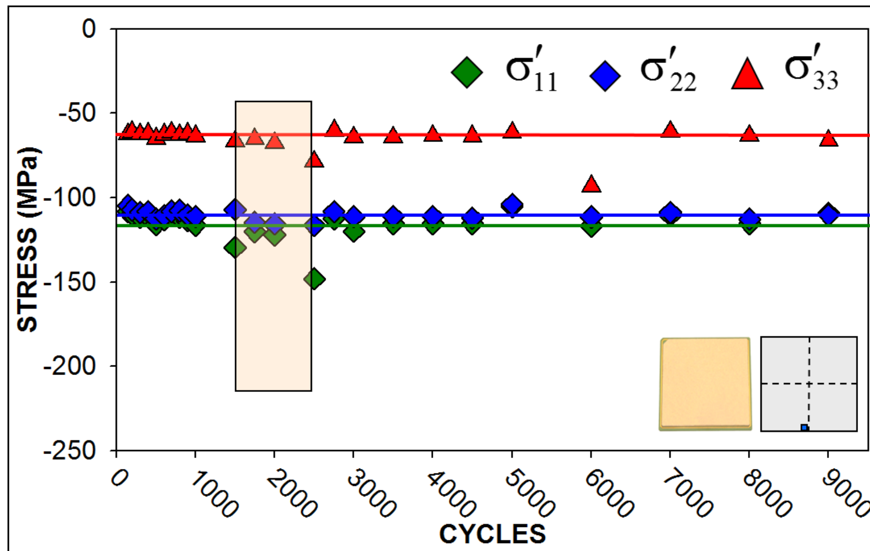


Figure 6.36: Variation of the Average Normal Stresses with Thermal Cycling

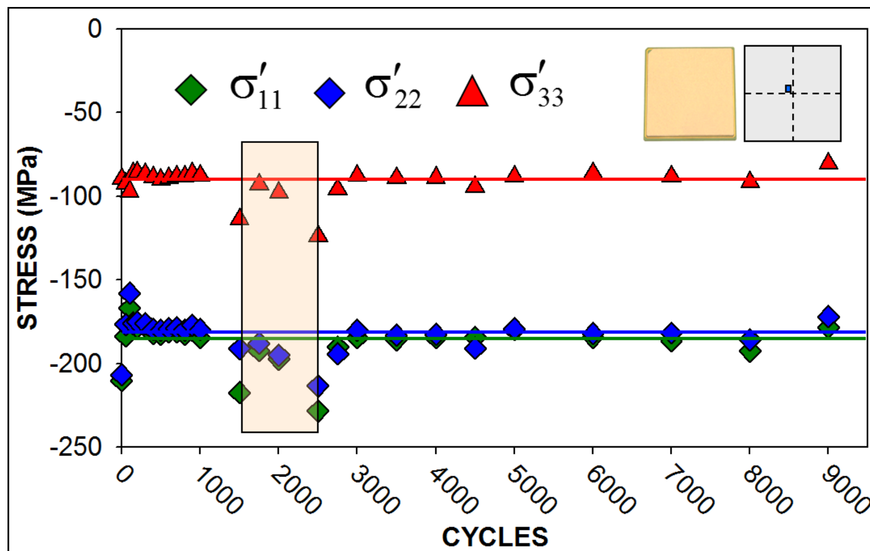


Figure 6.37: Variation of the Average Normal Stresses with Thermal Cycling

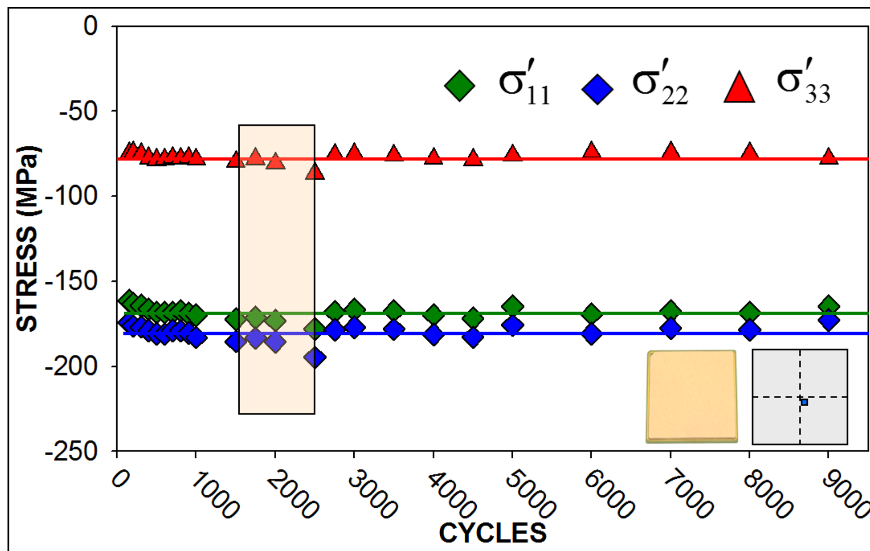


Figure 6.38: Variation of the Average Normal Stresses with Thermal Cycling

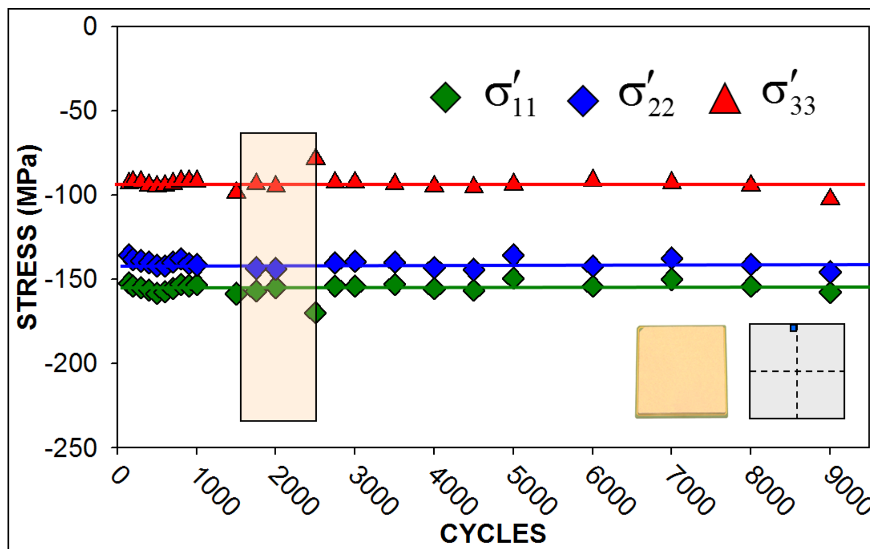


Figure 6.39: Variation of the Average Normal Stresses with Thermal Cycling

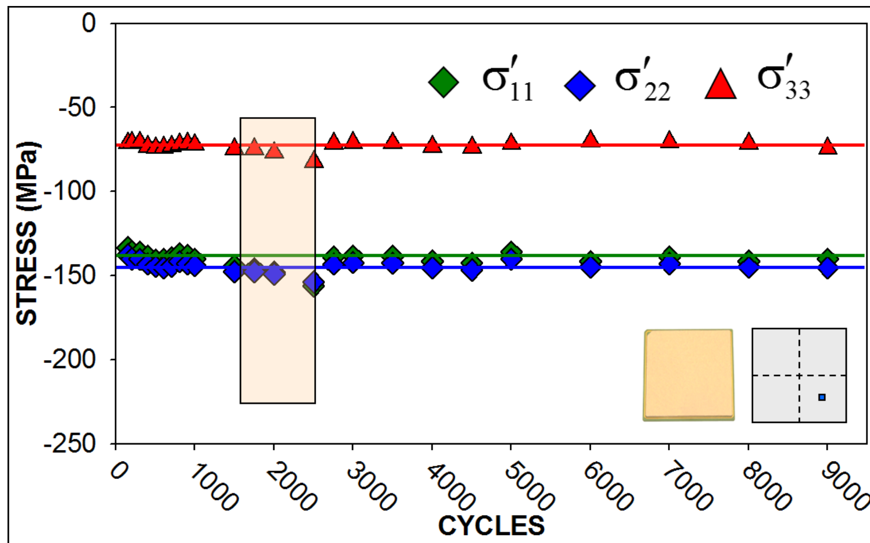


Figure 6.40: Variation of the Average Normal Stresses with Thermal Cycling

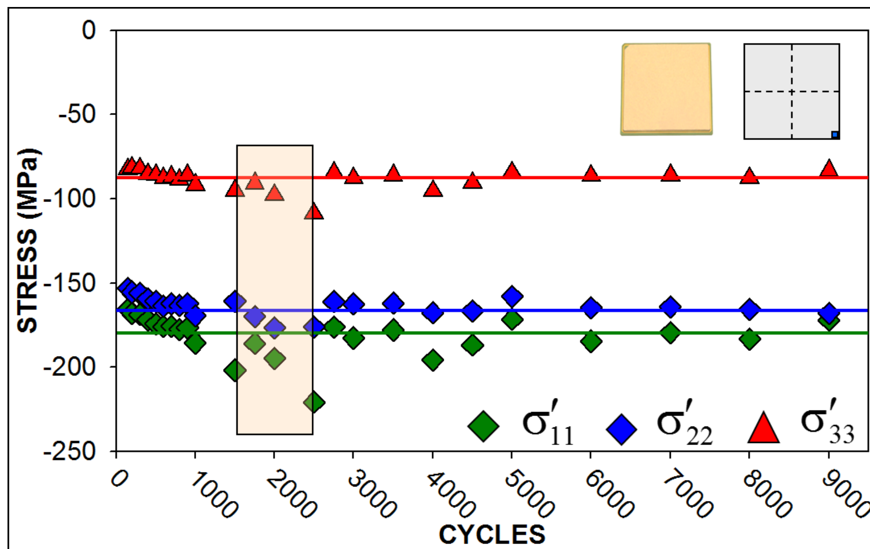


Figure 6.41: Variation of the Average Normal Stresses with Thermal Cycling

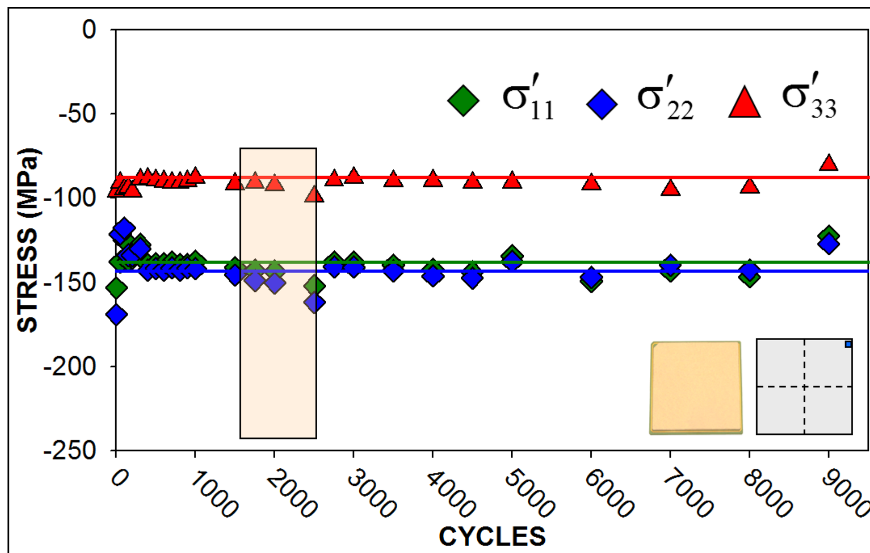


Figure 6.42: Variation of the Average Normal Stresses with Thermal Cycling

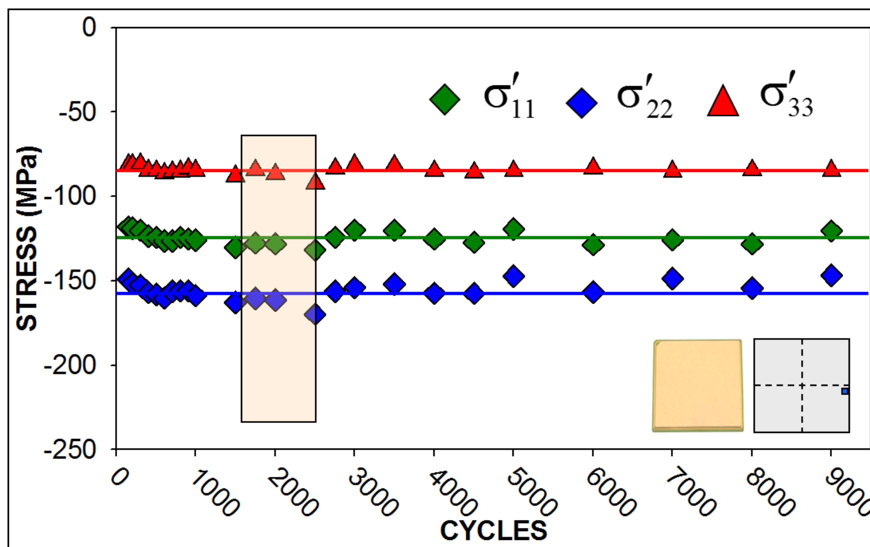


Figure 6.43: Variation of the Average Normal Stresses with Thermal Cycling

6.2.1 Numerical Prediction of Die Stresses Due to Thermal Cycling

Finite element simulations were performed by Motalab [184] to model the long term cycling experiments discussed above. The predicted maximum (0 °C) and minimum (100 °C) normal stresses during cycling are shown in Figure 6.44 and Figure 6.45, for the center and corner of the die, respectively. The analogous predicted maximum and minimum values of the in-plane shear stress (die corner) during cycling are shown in Figure 6.46. The modeling results verify what was seen in the experimental data, namely that the majority of changes in the die stresses will occur early in the cycling process. Similarly, the FEA predicted stress levels were also constant for several thousand cycles. Finally, it is noted that the experimental stress values were measured at room temperature, and thus fall between the maximum and minimum values plotted in Figures 6.44 - 6.46.

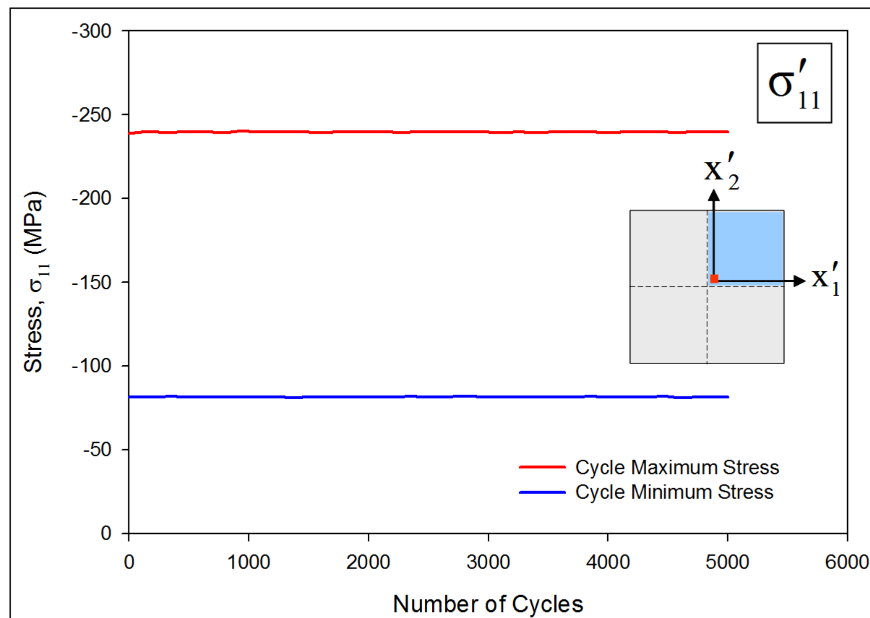


Figure 6.44: Variation of Normal Stress at the Die Center with Thermal Cycling (Finite Element)

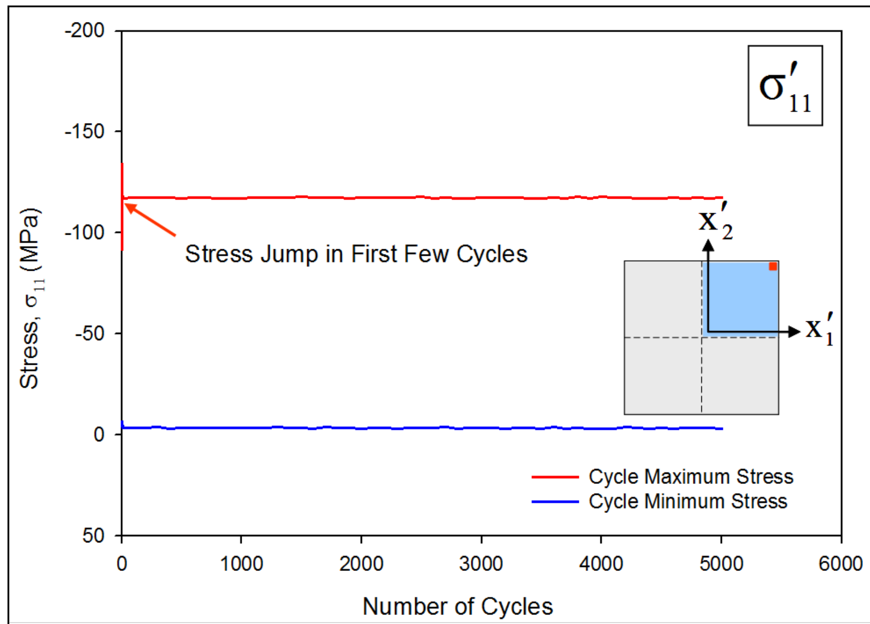


Figure 6.45: Variation of Normal Stress at the Die Corner with Thermal Cycling (Finite Element)

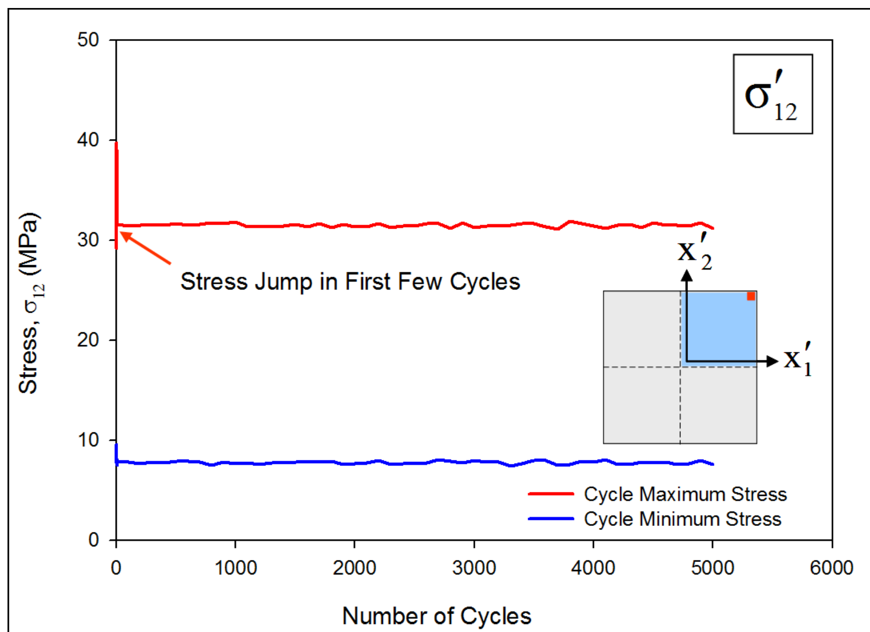


Figure 6.46: Variation of In-Plane Shear Stress at the Die Corner with Thermal Cycling (Finite Element)

6.3 In-Situ Die Stress Measurements During Thermal Cycling

With the purpose of further understanding the evolution of die stresses in the LGA during thermal cycling, die stress variations were also characterized in-situ during thermal cycling experiments. The test samples, as shown in Figure 6.1, were cycled using the twenty minute profile shown in Figure 6.25. Resistance and temperature data from the sensor rosettes were recorded continuously for several cycles, and the stresses at selected sites across the die were calculated as a function of time. The transient variations of in-plane normal stress σ'_{11} for a single rosette on the die are shown in Figure 6.47. Die stresses measured at room temperature due to thermal cycling showed stress shifts in initial cycles. The data from the in-situ experiments seemed to confirm this, as large variations in magnitude and an overall shift in the peak to peak values of stress are noted in Figure 6.47.

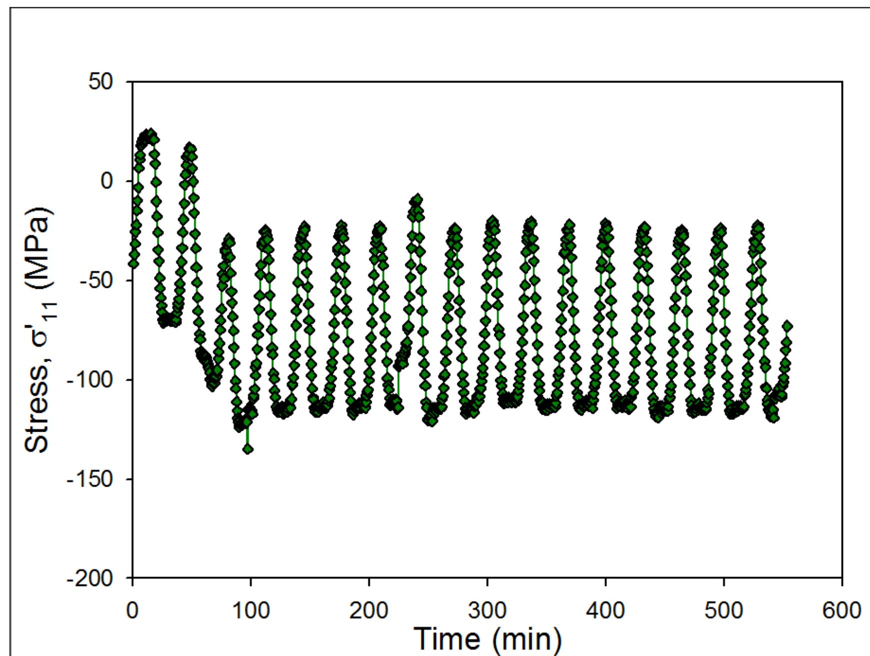


Figure 6.47: Normal Die Stress During Thermal Cycling

6.3.1 Numerical Predictions for Transient Die Stresses During Thermal Cycling

Transient finite element simulations were also performed for the thermal cycling of the CLGA components discussed above. The numerical predictions of the variations of the normal stress at the die center during the initial cycles are shown in Figure 6.48. The modeling and experimental results in Figures 6.47 and 6.48 share several trends. First, the shift or jump in the stress values during the initial cycles of the test is evident in both cases. Secondly, both results also show that the stress levels equilibrate after the first few cycles, and the values from both graphs are very similar.

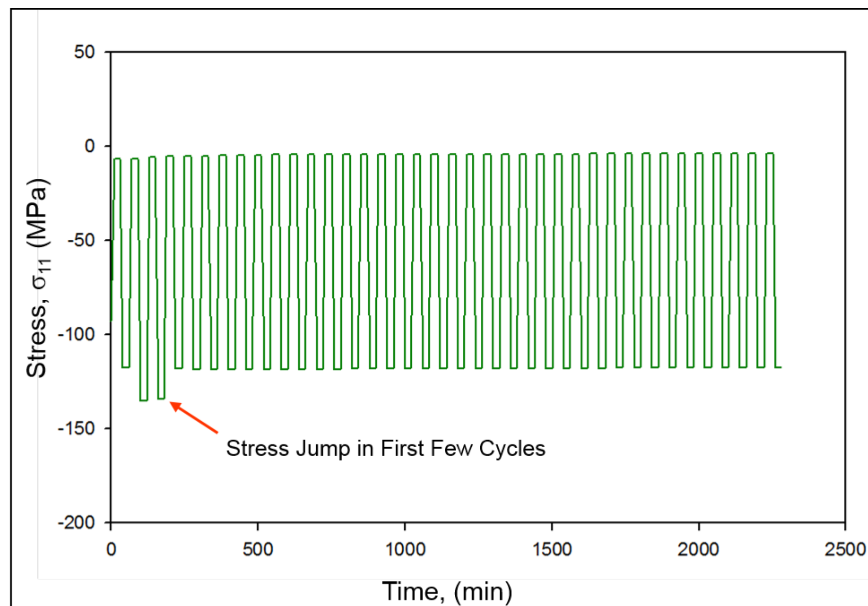


Figure 6.48: In-Plane Normal Die Stress Variation During Thermal Cycling(Finite Element)

Chapter 7

Temperature and Stress Effects Due to Power Dissipation

In the previous chapter, the effects of temperature changes on die stresses in microprocessor packages were studied. In those experiments, the temperature of the surrounding environment was changed. Elevated temperatures seen by microprocessors in actual use applications seldom come from the surrounding environment. Typically, great care is taken to regulate the ambient conditions surrounding high-end workstation computers and servers. Increased temperatures seen by the die are a byproduct of the self heating of the transistors on the die while the processor is in operation. In this chapter, die stresses and temperatures due to power dissipation have been investigated. Power dissipation was simulated using the buried layer heater on the JSE test die.

To study the effects of power dissipation on the CLGA packages seen in Figure 5.16, the test board seen in Figure 6.1 was again utilized to gain access not only to sensor rosettes, but also to power the buried layer heater on the test chips without applying mechanical loading to the CLGA packages. Several access points on the CLGA were used in order to ensure that the current carrying capability of each wirebond was not exceeded. Contacts that were routed to the heater layer on each side of the die were electrically connected together, so that two wires could be used to power the resistive buried layer. After calculation of the effective resistance of the buried layer, various voltages corresponding to pre-determined power dissipation levels were applied to the heater.

7.1 In-Situ Temperature Determination

Measuring the actual surface temperature on the die during heater excitation was preferred over simply attaching a thermocouple or RTD to a point external to the package due

to the transient nature of power cycling. One key feature of the JSE flip chip test die is the use of the test rosettes as temperature sensors. While temperature diodes are available on each chip, the calibration and use of the sensor rosettes as temperature sensors allows for use of existing instrumentation and data reduction techniques. A closer look at the piezoresistive theory in Chapter 3 shows that using the n-type resistors in each rosette is preferable as the coefficients multiplying the stresses are very small. Additionally, using a sensor in a region of lower normal stress is preferable. Using the piezoresistive theory for the test chips in this study results in two different estimates of temperature that can be averaged. Equation (7.1) and eq. (7.2) show the relationship between the n-type sensors in each rosette and temperature:

$$\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} \cong 2\alpha_1^n T \tag{7.1}$$

$$\frac{\Delta R_2}{R_2} + \frac{\Delta R_4}{R_4} \cong 2\alpha_1^n T \tag{7.2}$$

where T is the temperature change:

$$T = T_m - T_{initial} \tag{7.3}$$

These relationships are approximate as the stress multiplier terms are very small and have been neglected. If the normal stress terms are very large, or if a different doping is used, resulting in different piezoresistive coefficients, this approximation may not be acceptable. The measured temperature T_m may be calculated as the average of the two resistance equations:

$$T_m \cong \frac{1}{4\alpha_1^n}\left(\frac{\Delta R_1}{R_1} + \frac{\Delta R_2}{R_2} + \frac{\Delta R_3}{R_3} + \frac{\Delta R_4}{R_4}\right) + T_{initial} \tag{7.4}$$

Samples used in the power dissipation experiments were calibrated by exposing the assemblies to room temperature in a thermal chamber until the entire assembly was in

thermal equilibrium. The chosen rosettes were measured and the temperature was raised in ten degree increments and allowed to come to thermal equilibrium, and then the rosette was measured again. Rosette measurements were taken over a large range of temperatures, and were calibrated with a precision RTD in contact with the heat spreader assembly. An example calibration curve is shown in Figure 7.1. The coefficient of determination, or R^2 value of the fit through the data in this typical curve is 0.99987.

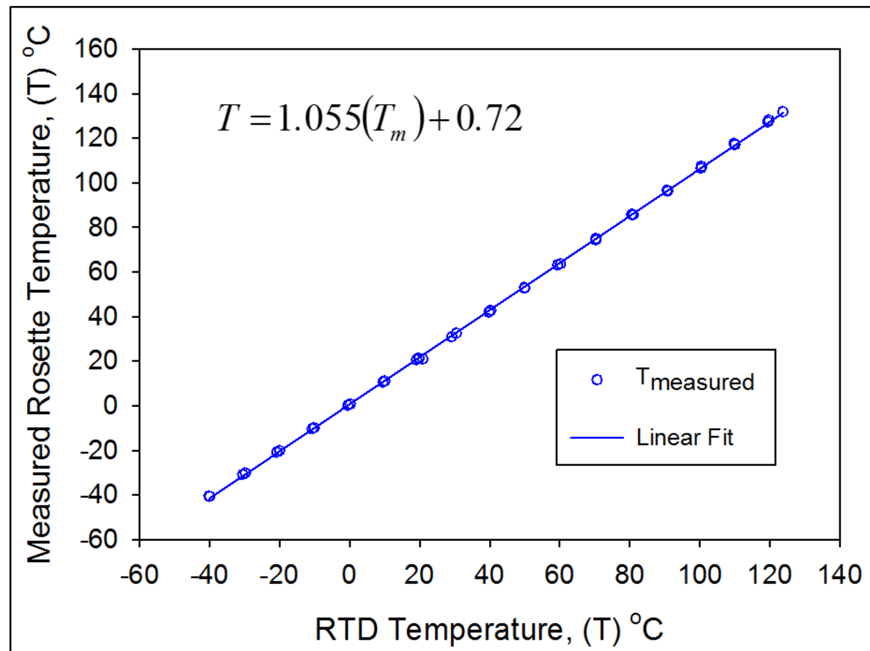


Figure 7.1: Temperature Calibration of Sensor Rosette

7.2 Temperature Change due to Power Dissipation

As discussed earlier, the tests chips in this study feature an on-chip buried heater layer that can be excited to dissipate power. The area of the buried layer is the same as the chip itself, allowing for uniform heating of the entire die. Connections on the test vehicle allow a voltage to excite the buried layer and heat the package from the inside in a manner similar to a working microprocessor. In preliminary experiments, small voltages that correlated to known power dissipation levels were injected into LGA component test vehicles configured as in Figure 6.1. In this case, the thermal boundary conditions were free convection off

all sides of the CLGA component. The on-chip sensors were able to record the device side die surface temperature during each power excitation using the technique discussed in the previous section. Figure 7.2 shows the transient die temperature variations for power levels up to 2 Watts. It is observed that steady state conditions are reached within 1000 sec for all power levels. The measured steady state die temperature at each power level is shown in Figure 7.3. The data shows a linear relationship between the power dissipated on the die and the die surface temperature.

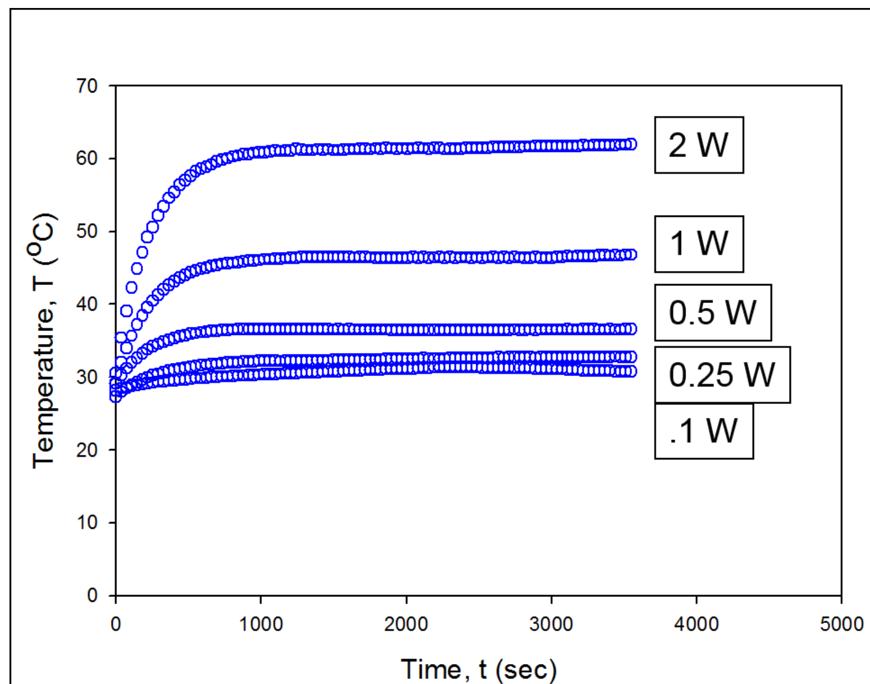


Figure 7.2: Die Surface Temperature vs. Time for On-Chip Power Dissipation

In another experiment, two watts of power was dissipated through the die heater until a steady state temperature was reached, and then the power was disconnected from the heater. The temperature on the surface of the die at the center of the die during this test is presented in Figure 7.4.

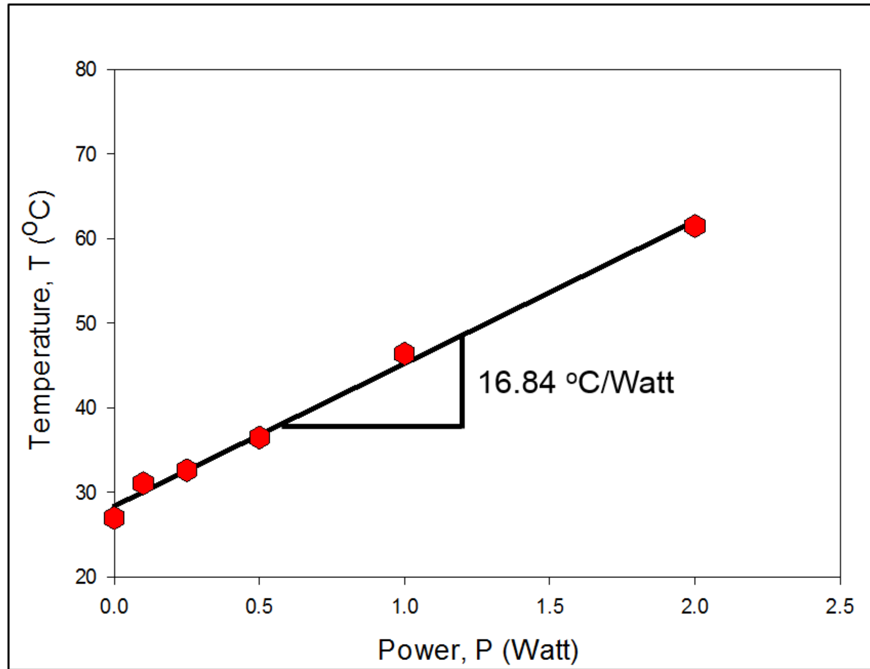


Figure 7.3: Die Surface Temperature vs. Power Dissipation

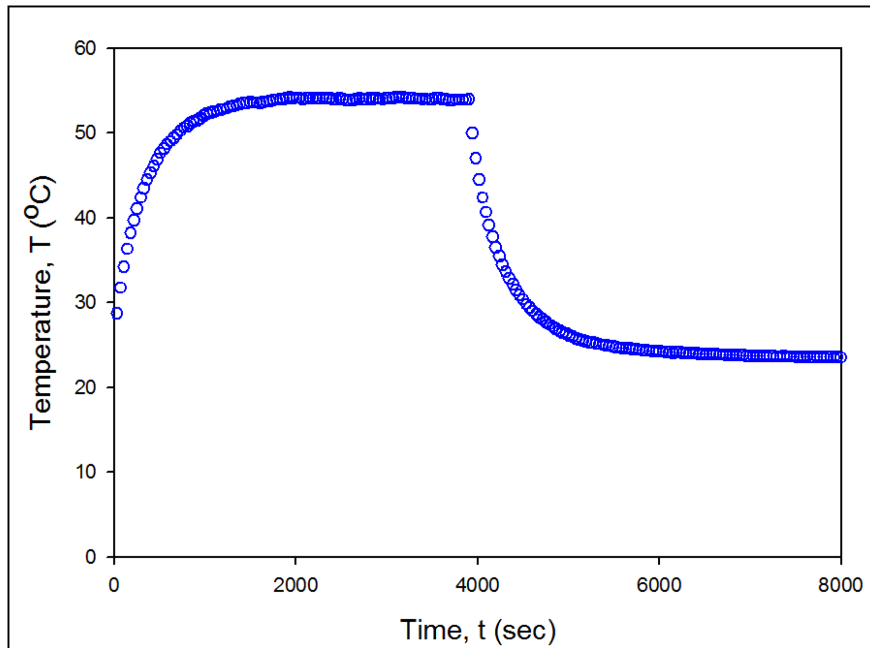


Figure 7.4: Die Surface Temperature vs. Time for On-Chip Power Dissipation

7.2.1 Numerical Predictions of Temperature Change due to Power Dissipation

Finite element modeling (transient heat transfer) was also performed by Motalab [184] to predict the on-chip temperature distributions. The LGA mesh shown in Figure 5.16 was again utilized, along with the thermal boundary conditions shown in Figure 7.5. Figure 7.6 shows the predicted transient die temperature variations for a power dissipation level of 2 Watts. The experimental data from Figure 7.2 has been included for comparison purposes. The predicted and measured steady state temperatures correlate well, while the time constant of the experimental process is slightly lower than that found using the FEA model.

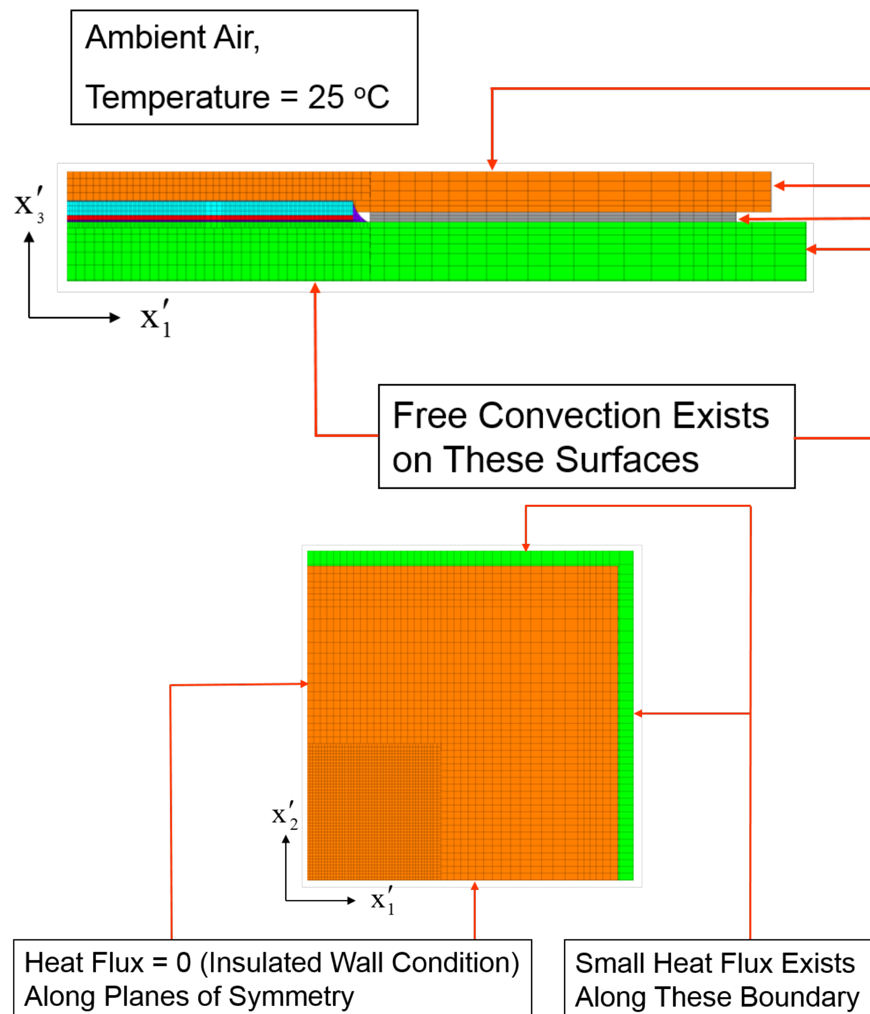


Figure 7.5: Thermal Boundary Conditions of Power Dissipation FEA Model

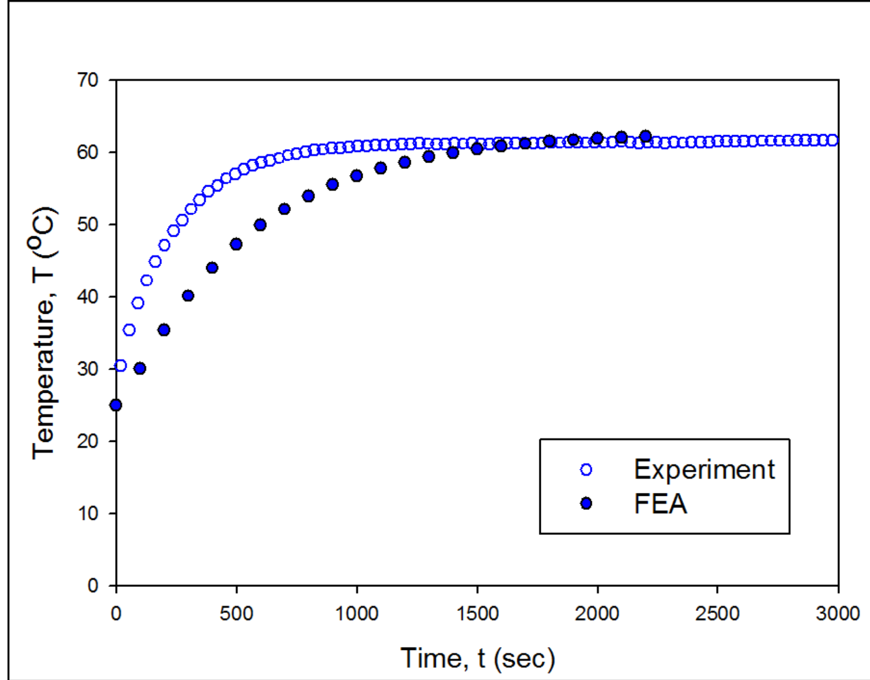


Figure 7.6: FEA and Experimental Transient Die Surface Temperatures for On-Chip Power Dissipation

7.3 Experimental and Numerical Evaluation of Power Cycling

In actual server and high-end computing applications, the processor or processors will not simply power on and operate at a constant power or temperature level. In reality, as the machine performs calculations, the power dissipated on the die will increase and decrease with use. To mimic this case, power cycling was also performed on the CLGA components by exciting the buried layer on the flip chip test die in a cyclical manner. The chosen transient power dissipation profile is shown in Figure 7.7. A square wave cycle was utilized, with a peak excitation of 2 Watts, and a cycle length of 20 minutes (10 minutes at full excitation and ten minutes of no excitation). During the power cycling, the on-chip sensors were used to record temperature data as well as resistance data for stress extraction. A plot of the measured die temperature versus time is shown in Figure 7.8, while the analogous predictions of the finite element model are shown in Figure 7.9. Good correlation is observed for the transient temperature response.

The stress change σ'_{11} due to power cycling for one rosette on the die is shown in Figure 7.10. The stress change follows the same pattern as the die temperature, as expected, and varies from 22 MPa to 40 MPa from cycle to cycle. Analagous stress change results predicted using the finite element model are shown in Figure 7.11. Similar trends are present in the numerical results with the peak stress change reaching 39 MPa, while the minimum stress calculated in each cycle is lower than the measured values.

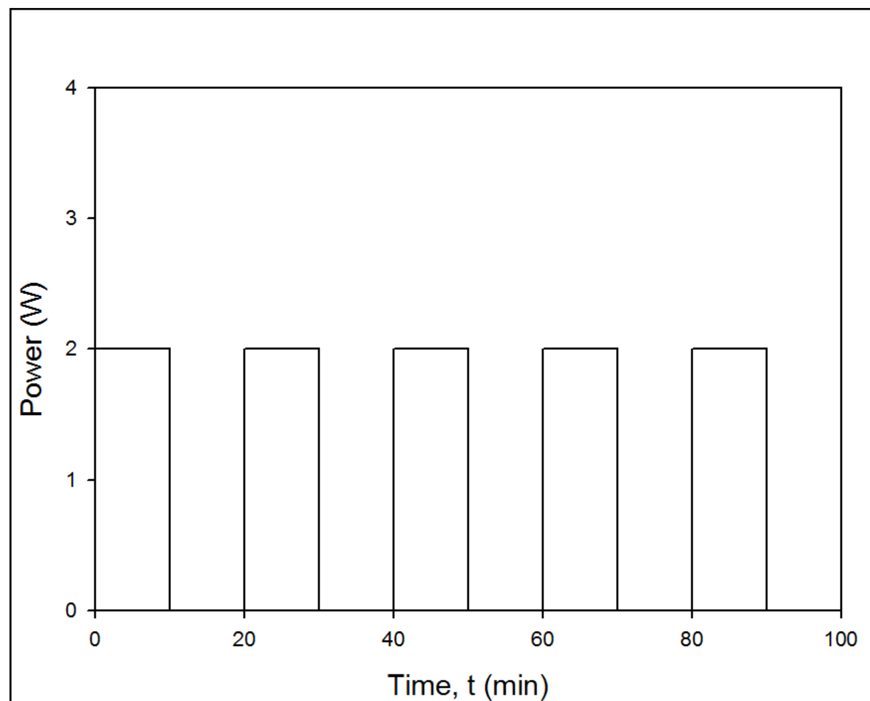


Figure 7.7: Square Wave Power Cycle

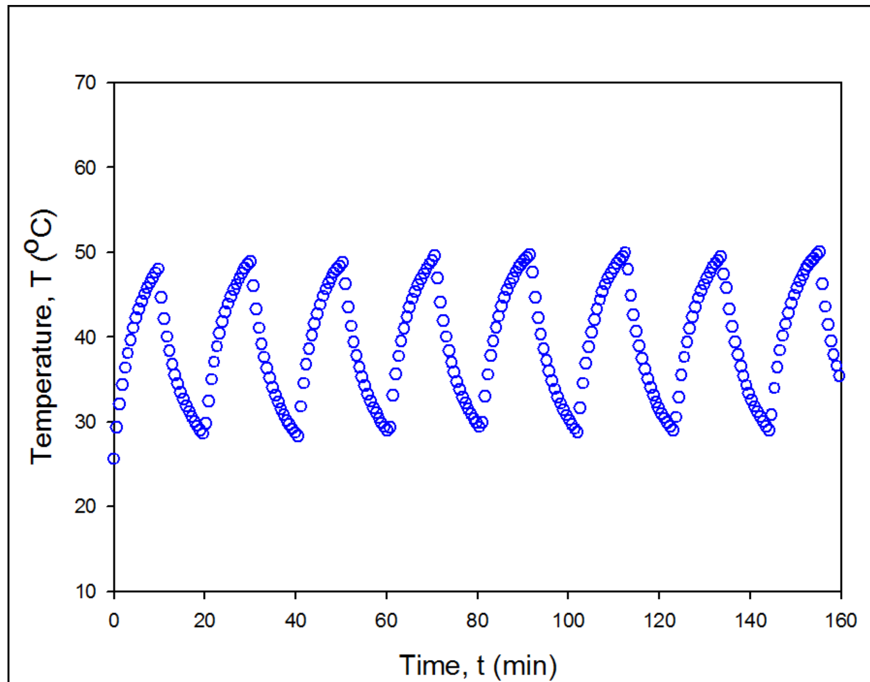


Figure 7.8: Measured Transient Die Surface Temperature Variation during Power Cycling

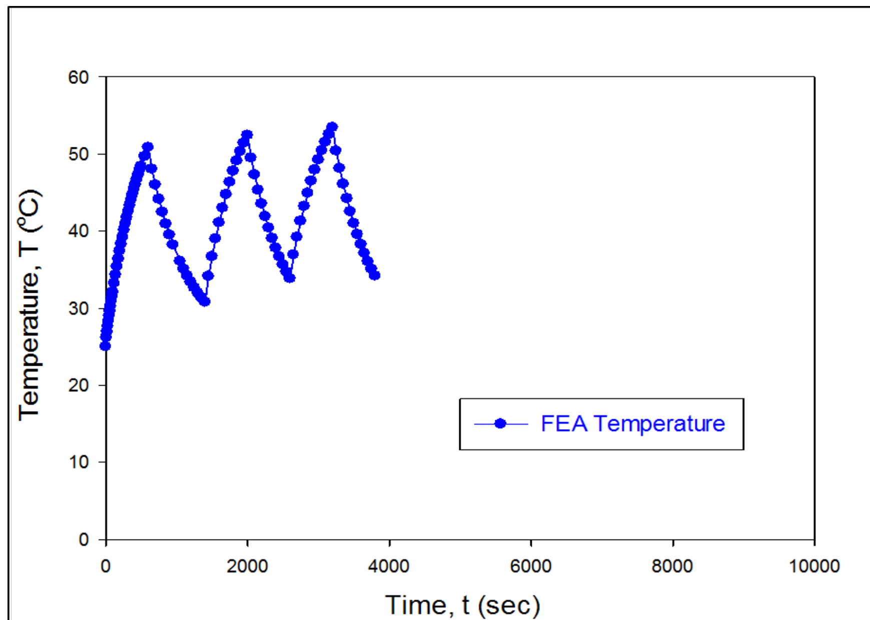


Figure 7.9: Transient Die Surface Temperature Variation during Power Cycling (FEA)

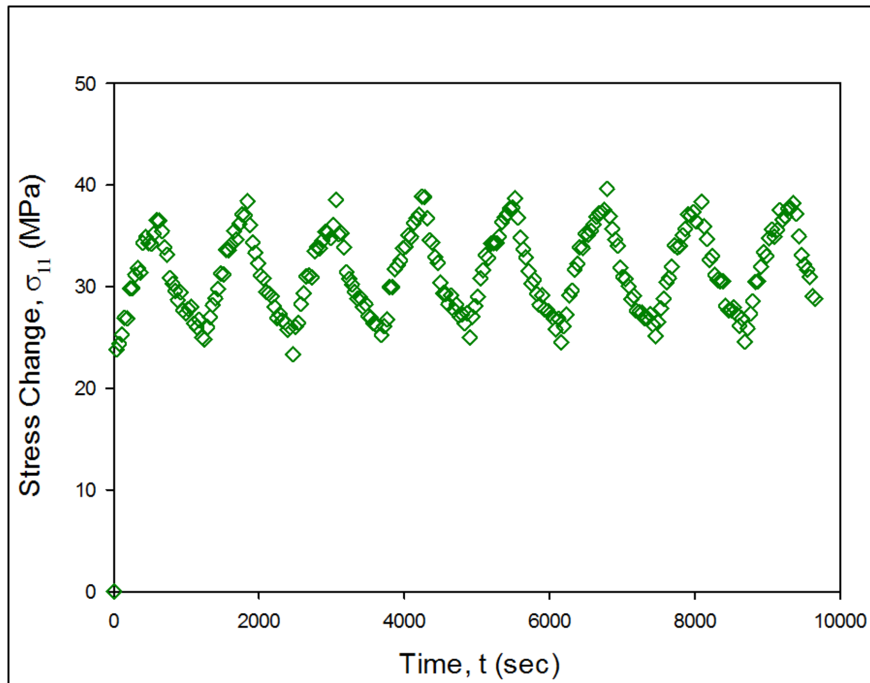


Figure 7.10: Measured Transient Die Stress Variation during Power Cycling

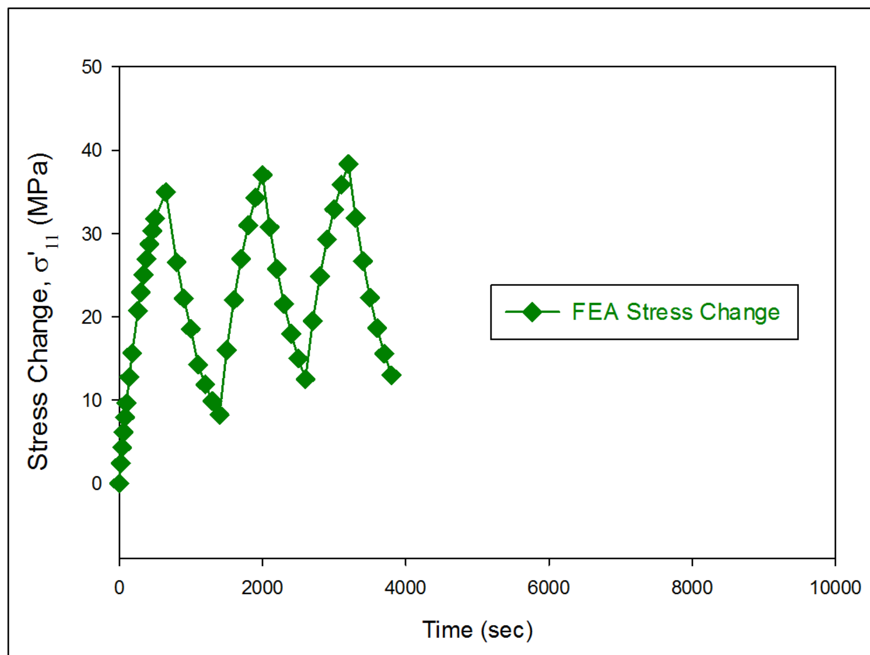


Figure 7.11: Transient Die Stress Variation during Power Cycling (FEA)

Chapter 8

Second Level Assembly of Ceramic Ball Grid Array Packages

8.1 Second Level Assembly Test Board

Microprocessor packages are typically mounted to a large printed circuit board as shown previously in Figure 1.1. Chapter 5 detailed the buildup of die stresses induced by the assembly of flip chip ceramic land grid array packages. The addition of a second level of solder ball interconnects and mounting to a large printed circuit board constituted the next step in assembly to match Figure 1.1 . The second level of interconnects are necessary to mechanically and electrically connect the CLGA assembly to the motherboard. To enable measurement of the die stresses due to addition of second level interconnects, a test board was developed for use with the CLGA components. The first step of development was to identify the geometric features of the CLGA, such as the land pattern and pitch of lands. The next step involved identification of the appropriate pads on the land grid array to access a chosen set of rosettes.

The rosettes chosen for the second level assembly study are shown in Figure 8.1. Here the regions of orange represent the access bumps on the die surface for the chosen rosettes. The red areas are the access points to the buried layer heater on the die. The green region encompasses the access points of the 8-bit fuse ID used to identify test die throughout the process. The land pattern on the CLGA substrate is shown in Figure 8.2. After careful consideration of pads needed for stress sensing rosettes, heater access points, and identification, the geometry and design of the test board routing were determined as shown in Figure 8.3. The dimensions of 250 x 130 x 3.6 mm are roughly based on test boards used by the corporate sponsor of this work. The test board included 10-layers of FR406 material and an Electroless Nickel, Immersion Gold (ENIG) finish on the copper conductors. To maintain

similarity with motherboard assemblies seen in the field, the board thickness was chosen to be 143 mils (3.62 mm). A scan of the custom fabricated board is shown in Figure 8.4

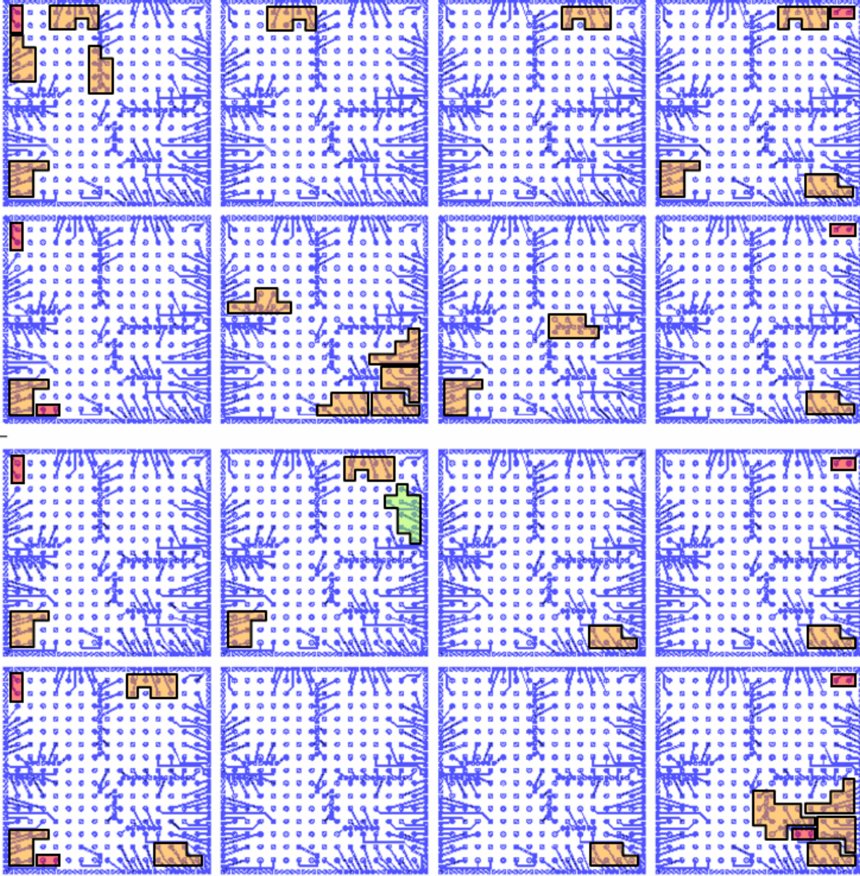


Figure 8.1: Rosettes, ID, and Buried Layer Heater Access Points for Second Level Assembly Study

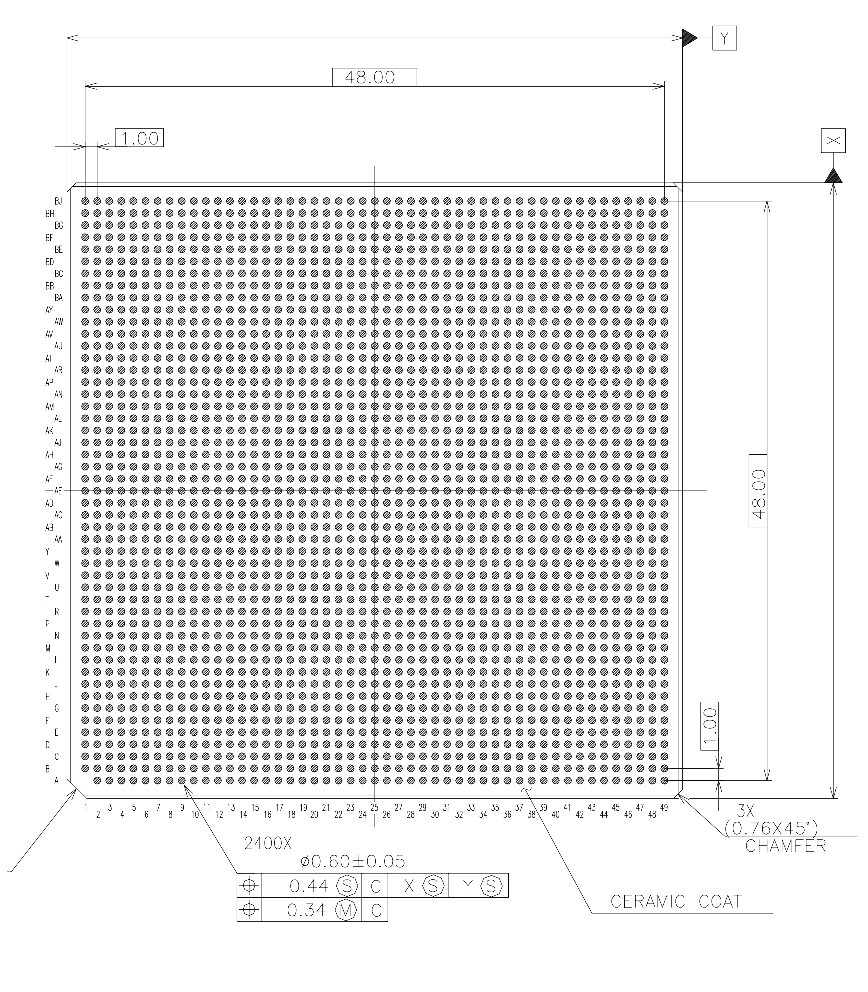


Figure 8.2: Pattern and Spacing of LGA Pads

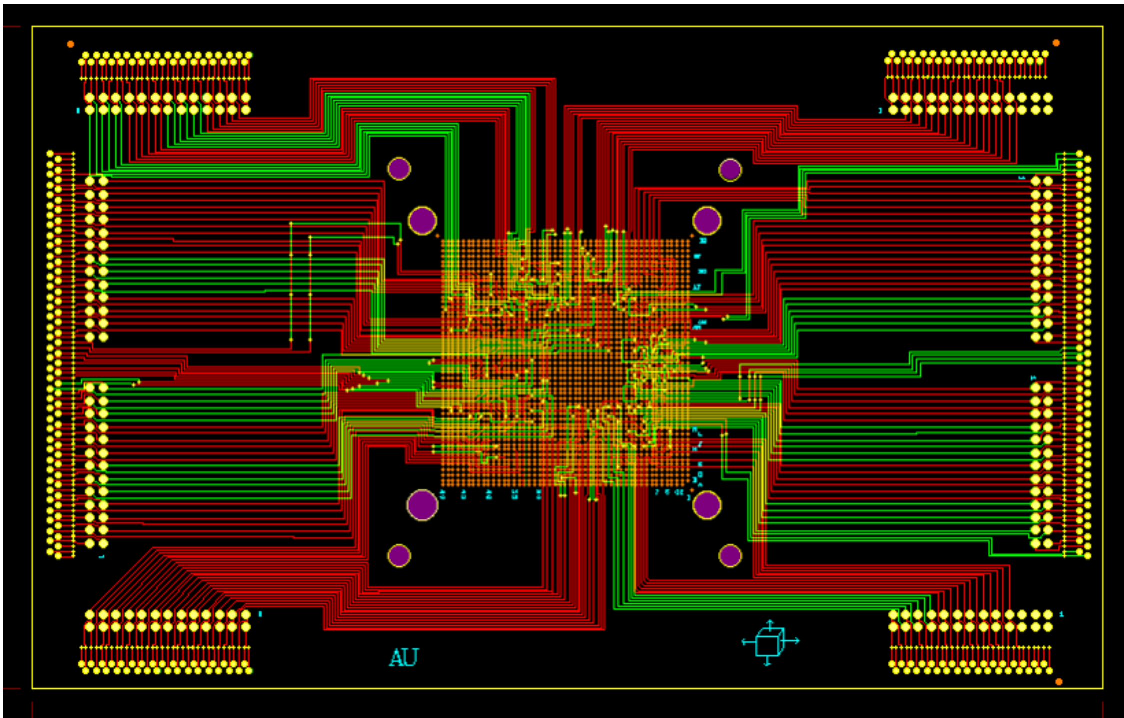


Figure 8.3: Second Level Test Board Routing Design

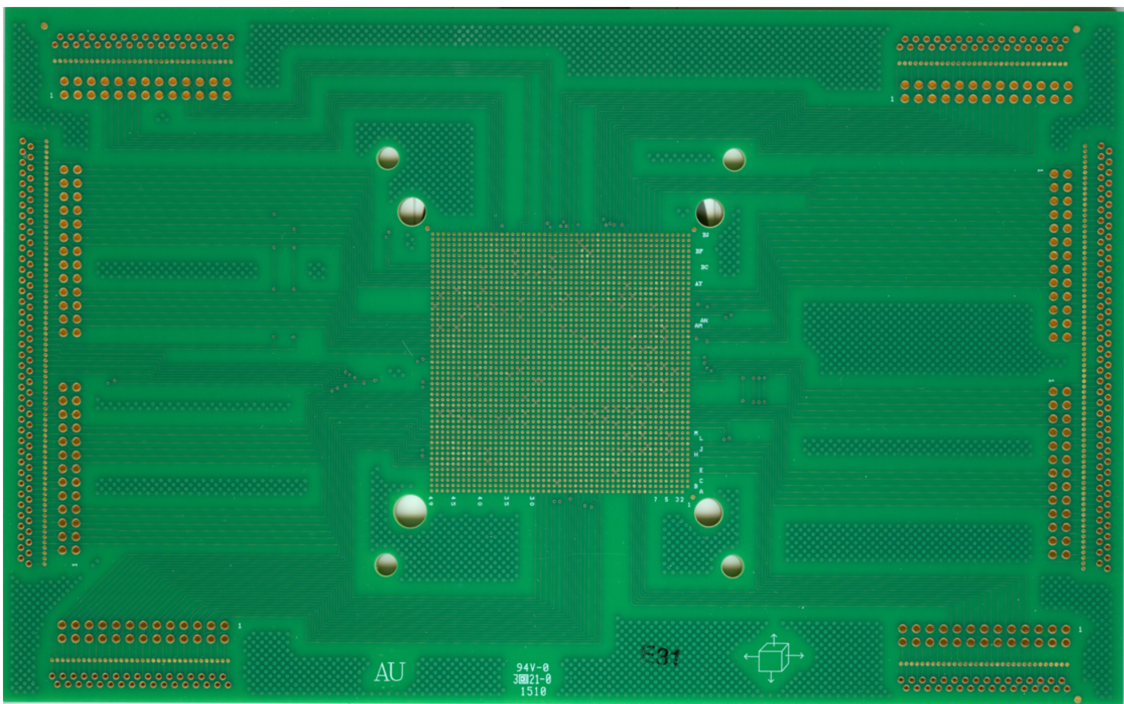


Figure 8.4: Second Level Test Board Photograph

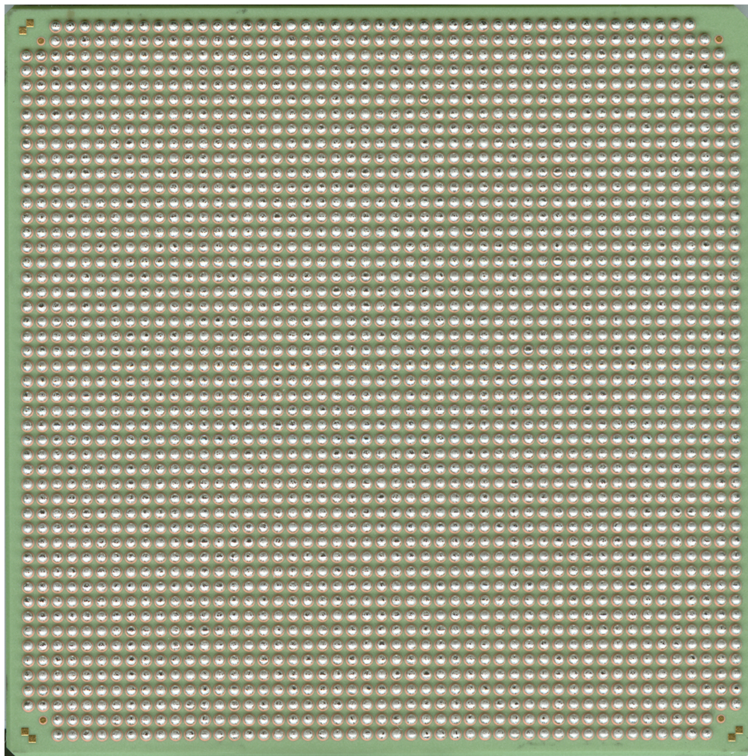
8.2 Ceramic Ball Grid Array Packages

A separate set of 18 additional area array, lead free stress test die were utilized for the second level assembly study. The initial (unstressed) sensor resistances were again measured by die probing. Instead of repeating the sequential assembly and measurement processes detailed in Chapter 5, the die were then fully assembled into ceramic land grid array packages with second level solder balls attached as shown in Figure 8.5. The sensor resistances for the assembled components were then measured again using the same test board and socket as the lidded CLGA packages shown in Figure 5.10. In the case of the CBGA package measurements, the second level solder balls made electrical contact with the test socket pins as shown in Figure 8.6. Stress measurement results calculated from the initial and final resistances are shown in Figure 8.7 for rosettes at the center of the die and two corners of the die. It is noted that the stress values in Figure 8.7 are lower than those observed in in Figure 5.20 for the previously measured CLGA assemblies. One possible reason for the discrepancy was the use of a new (different) underfill material in this round of assemblies. It is also noted that the normal stresses at the corner of the die have larger standard deviations than those at the center of the die, most notably at rosette 28 in the lower right corner of the die.

8.3 Second Level Assembly Equipment and Techniques

The second level assembly of the CBGA components to the PCB test boards took place in the Auburn University Laboratory for Electronics Assembly and Packaging (LEAP). Boards were first plasma cleaned to remove any unwanted oxides from the board plating. Prior to board assembly, a solder paste stencil was made with the aperture equal to the lands on the CLGA substrates. The stencil was used in conjunction with the MPM AP25 stencil printer shown in Figure 8.8 to screen print solder paste directly on the lands of the test board. Due to the low quantity of assemblies produced, each assembly was visually

(a) CBGA Top View



(b) CBGA Bottom View

Figure 8.5: Assembled Ceramic Ball Grid Array for Second Level Assembly Study

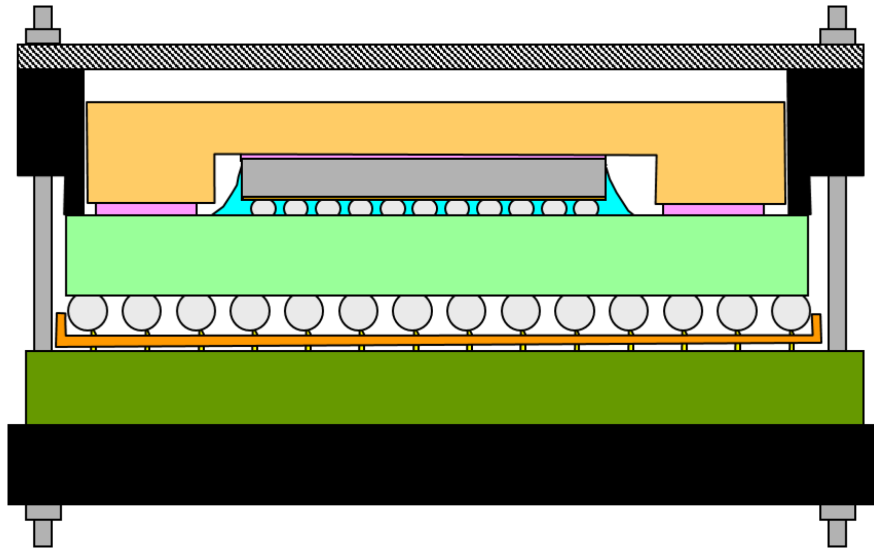
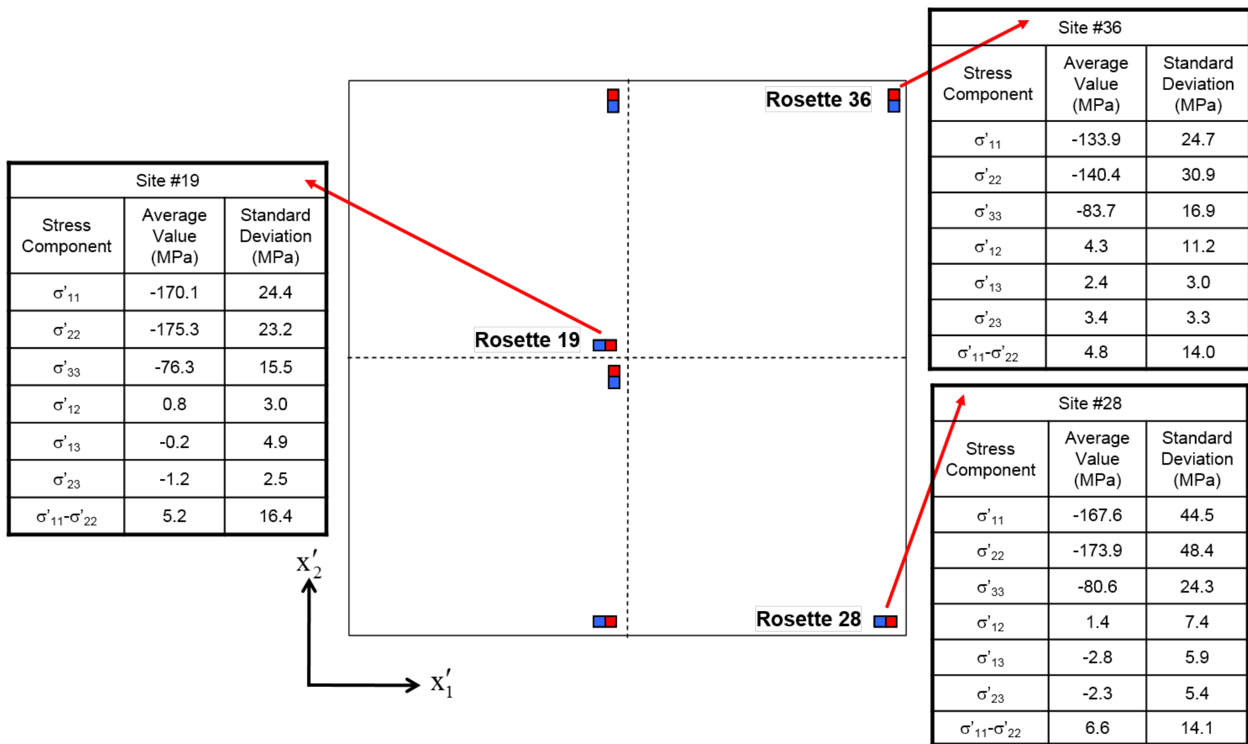


Figure 8.6: Schematic of CBGA Package Measurement



Site #19		
Stress Component	Average Value (MPa)	Standard Deviation (MPa)
σ'_{11}	-170.1	24.4
σ'_{22}	-175.3	23.2
σ'_{33}	-76.3	15.5
σ'_{12}	0.8	3.0
σ'_{13}	-0.2	4.9
σ'_{23}	-1.2	2.5
σ'_{11}-σ'_{22}	5.2	16.4

Site #36		
Stress Component	Average Value (MPa)	Standard Deviation (MPa)
σ'_{11}	-133.9	24.7
σ'_{22}	-140.4	30.9
σ'_{33}	-83.7	16.9
σ'_{12}	4.3	11.2
σ'_{13}	2.4	3.0
σ'_{23}	3.4	3.3
σ'_{11}-σ'_{22}	4.8	14.0

Site #28		
Stress Component	Average Value (MPa)	Standard Deviation (MPa)
σ'_{11}	-167.6	44.5
σ'_{22}	-173.9	48.4
σ'_{33}	-80.6	24.3
σ'_{12}	1.4	7.4
σ'_{13}	-2.8	5.9
σ'_{23}	-2.3	5.4
σ'_{11}-σ'_{22}	6.6	14.1

Figure 8.7: Stresses After CBGA Ball Attachment

inspected under a microscope to ensure the accuracy and volume of each print. Placement of the CBGA components was accomplished using the Semiconductor Equipment Corporation 4150 placement machine shown in Figure 8.9. This split optic system allows the user to view the solder printed PCB pads and the second level solder balls at the same time for alignment purposes. After alignment was verified for x, y, and θ, the packages were placed on the lands with 500 grams of force. The test board assemblies assemblies were then placed in the Heller 1800EXL reflow oven shown in Figure 8.10 to melt the second level solder interconnects.

Figure 8.8: MPM AP25 Solder Stencil Screen Printer

8.3.1 Assembly Verification

Several iterations were required to achieve a reflow profile yielding good wetting and proper ball collapse of the CBGA solder joints. A number of dummy packages containing daisy-chain test tie were used in this process. The initial iteration of the profile was derived based on two sources. The first source was a profile for a slightly thicker (192 mil) board with a similar CBGA package used by the corporate sponsor of this work, and the

Figure 8.9: Semiconductor Equipment Corporation 4150 Placement Machine

Figure 8.10: Heller 1800EXL Reflow Oven

second source was the recommended profile for the Cookson Electronics Alpha OM-340 series lead free paste used in this work. The reflow profile for the 192 mil board is shown in Figure 8.11. Using this as a starting point, a board was instrumented with several thermocouples connected to a KIC Explorer thermal profiling system as shown in Figure 8.12. The KIC Explorer is capable of recording several k-type thermocouple inputs attached to printed circuit boards being assembled while passing through the reflow oven in a protective thermal shield. Thermocouples were placed on the leading edge, trailing edge, on the assembly lid, and on two sides of the test assembly parallel to the track of the reflow oven, near of the BGA balls. Temperatures recorded from these thermocouples were compared with recommendations from Cookson Electronics for peak temperature, maximum ramp, and time above liquidus.

Parts were visually inspected after each reflow. An initial inspection of an un-wetted package is shown in Figure 8.13. It is apparent from this image that the paste (granular region below spherical volumes) was not reflowed and wetting did not occur. After making several changes in temperature in each of the 10 heating zones of the Heller oven, as well as to the track speed, satisfactory visual results were obtained. A representative image from a positive external visual inspection is shown in Figure 8.14. Once the reflow recipe was deemed repeatable and produced assemblies with acceptable wetting and collapse ratio, as determined by external inspection, a sample was cross-sectioned to determine the quality of the assembly. Typically, an x-ray inspection is performed before destructive evaluation, but the thickness of the 10 layer test board along with the geometry of the CLGA package made discernible x-ray images unobtainable with the equipment available. An image from the cross-section of a successfully assembled part is shown in Figure 8.15. With the results of this evaluation, the reflow profile was verified and used for the assembly of the test packages. A representative CBGA on laminate assembly is shown in Figure 8.16.

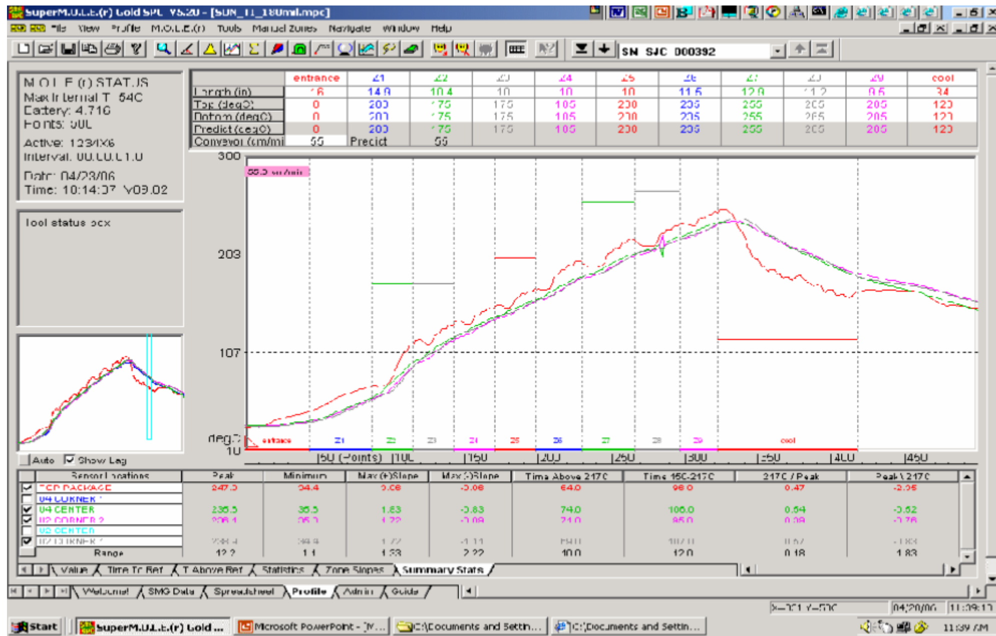


Figure 8.11: Initial Reflow Profile for Second Level Assembly

Figure 8.12: KIC Explorer Thermal Profiling System

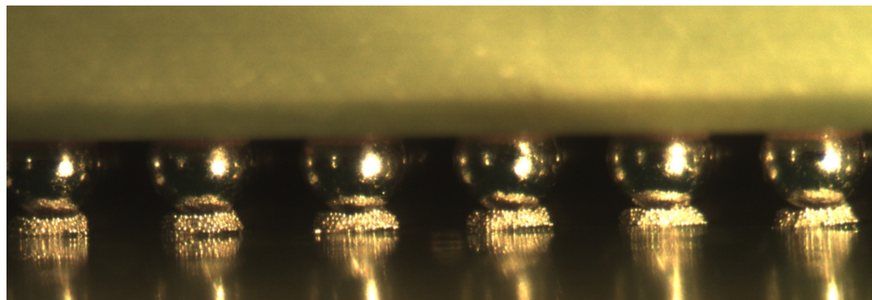


Figure 8.13: Second Level Interconnects after Bad Reflow Profile

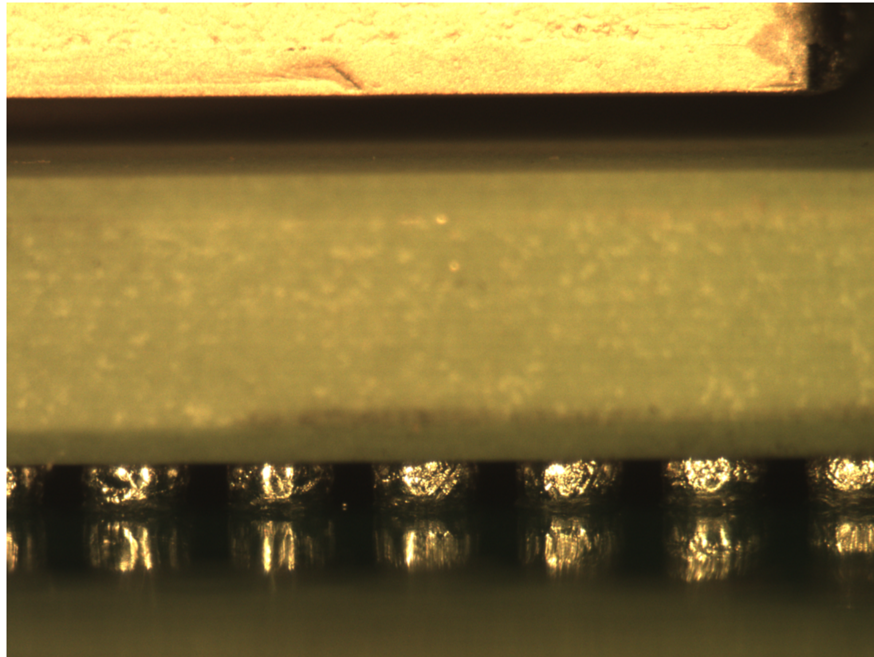


Figure 8.14: Example of Results of Good Reflow Profile

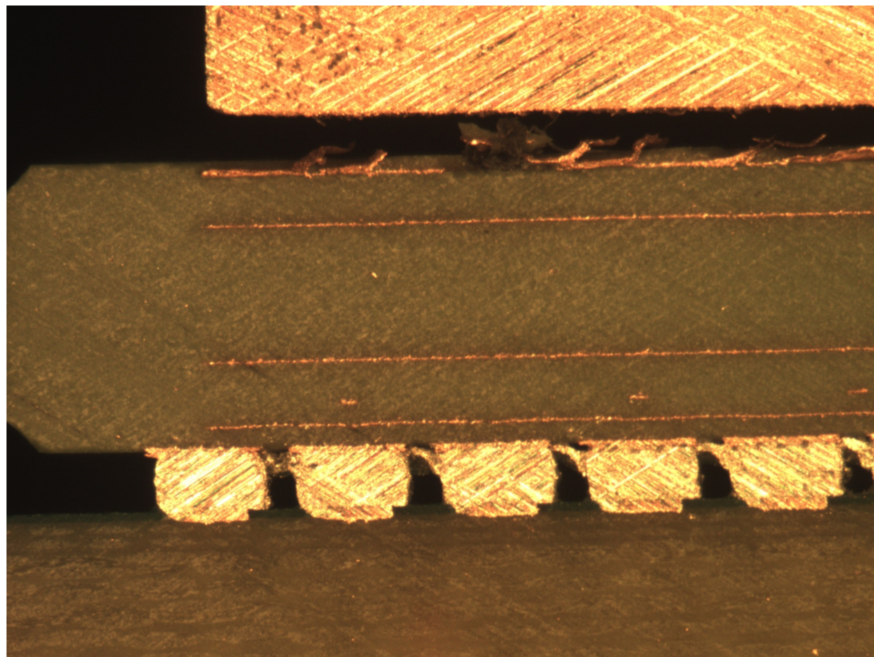


Figure 8.15: Cross Section of CBGA Second Level Assembly

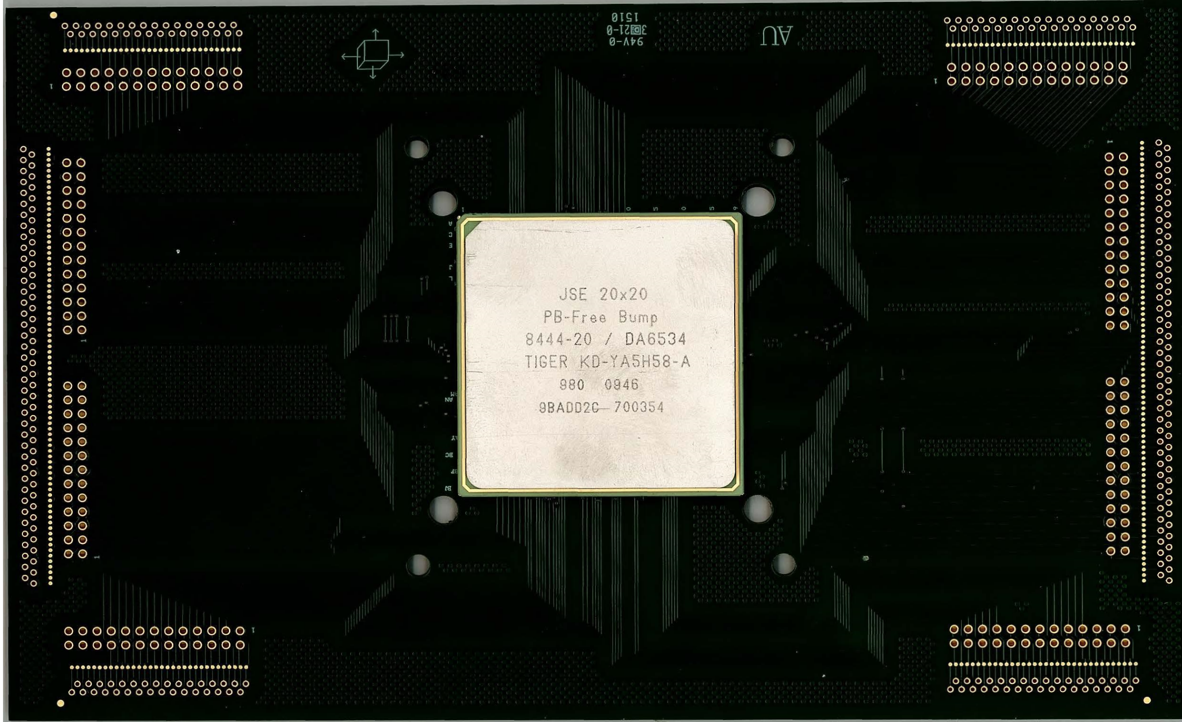


Figure 8.16: CBGA Assembled with Second Level Interconnects

8.4 Temperature Dependent Die Stresses in CBGA on Laminate Assemblies

After second level packaging of the test chips, experiments have been performed to analyze the effects of slow (quasi-static) temperature changes on the die stresses. Several of the CBGA assemblies were subjected to controlled temperature change in a thermal chamber, and the sensor resistances were monitored in-situ. The temperature range for this set of experiments was again chosen to be 0 °C to 100 °C based on the recommendation of the corporate sponsor of the study. The CBGA assemblies were subjected to varying temperature using an environmental chamber as shown in Figure 8.17. The utilized thermal profile is shown in Figure 8.18. The samples were initially at room temperature (20 °C). They were then subsequently raised to 100 °C, followed by a temperature decrease to $T = 0$ °C, and finally brought back to room temperature. The temperature was changed in 10 °C increments, and the samples were allowed to equilibrate for 20 minutes at each temperature

before sensor measurements were made. Thus, the components were essentially subjected to one complete slow thermal cycle.

Figure 8.17: Thermal Chamber and DAQ

When measuring die stresses induced by a specific loading, it is often beneficial to consider stress changes instead of absolute stresses. Using stress changes allows for a more concise understanding of the stresses caused by a particular load or temperature change alone. The measurement of stress change simply means measuring the initial or reference resistances of the sensing elements on the die in the unloaded or unheated assembly, and then measuring the sensor resistances again in the assembly during loading or thermal exposure. A more detailed discussion of stress change measurements can be found in Appendix A. The results shown below and discussed hereafter are for stress changes and not absolute stresses.

Figure 8.19 illustrates the measured variation of the in-plane normal stress change σ'_{11} with temperature at a location near the center of the die. The data measured from the initial

room temperature (20 °C) to 100 °C are plotted with red diamonds, and data measured as the temperature was slowly lowered from 100 °C to 0 °C are plotted with blue diamonds. Data measured as the temperature was slowly raised from 0 °C back to 20 °C are plotted in red diamonds containing a black cross, to delineate that section of data from other data measured with increasing temperature. All subsequent plots (Figure 8.19 - Figure 8.27) in this chapter also follow this scheme. Two measured stress changes have been plotted at each temperature from 0 °C to 100 °C with the exception of 0 °C and 100 °C (one measurement at each) and 20 °C (three measurements). Analogous results for the in-plane normal stress change σ'_{22} at the same rosette near the die center is shown in Figure 8.20. Both plots exhibit increasing response with temperature, with the stress changes being the highest (≈ 20 MPa) at the low temperature extreme, and the lowest (≈ -5 MPa) at the high temperature extreme. Figure 8.21 shows the measured die stress changes due to temperature for the in-plane shear stress σ'_{12}. As expected, the changes in σ'_{12} were very small over the applied temperature range for a site near the two axes of symmetry.

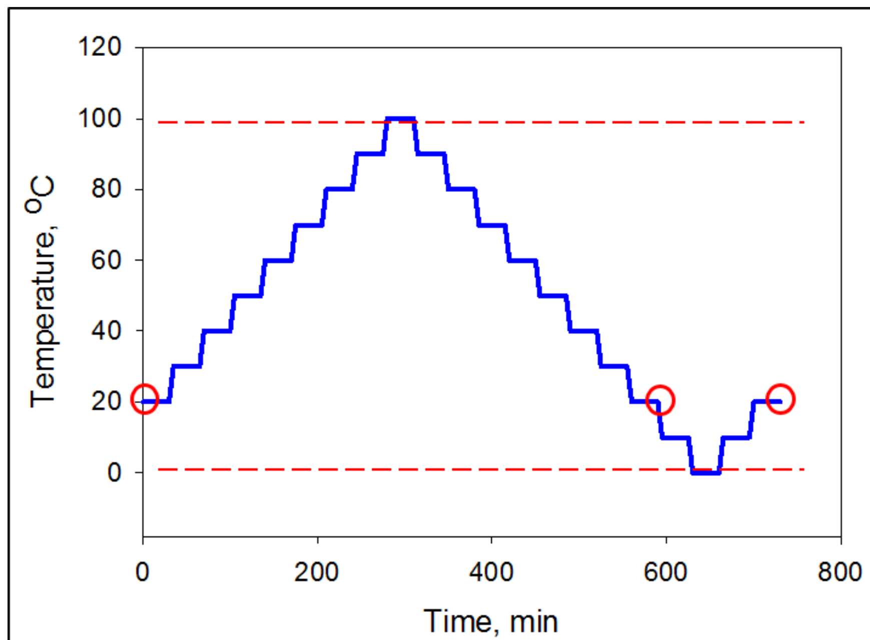


Figure 8.18: Thermal Profile for Temperature Dependent Stress Testing

Similar plots of stress changes σ'_{11}, σ'_{22}, and σ'_{12} measured at a location midway along the diagonal from the center of the die to the bottom left corner are shown in Figures 8.22 - 8.24. Die stress changes in both σ'_{11} and σ'_{22} appear linear with temperature, while the change in the in-plane shear stress σ'_{12} in Figure 8.24 is approximately linear to approximately 80 °C. Analogous measured stress changes for a rosette midway along the diagonal from the center of the die to the bottom right corner are shown in Figures 8.25 - 8.27. The measured changes in the in-plane normal stresses σ'_{11} and σ'_{22} due to slow temperature change again illustrate increasing response with temperature.

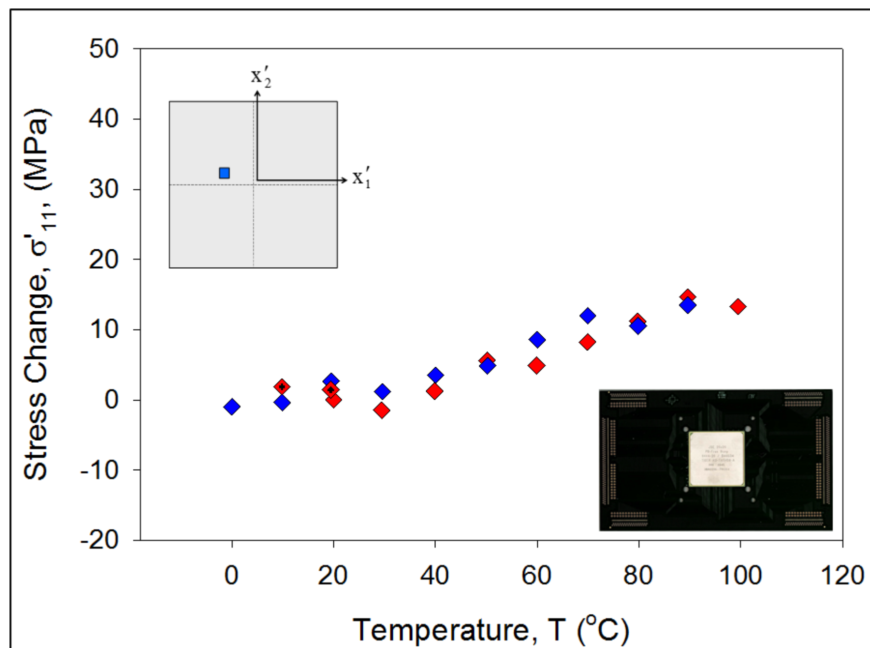


Figure 8.19: Variation of In-Plane Normal Stress with Temperature (Near Die Center)

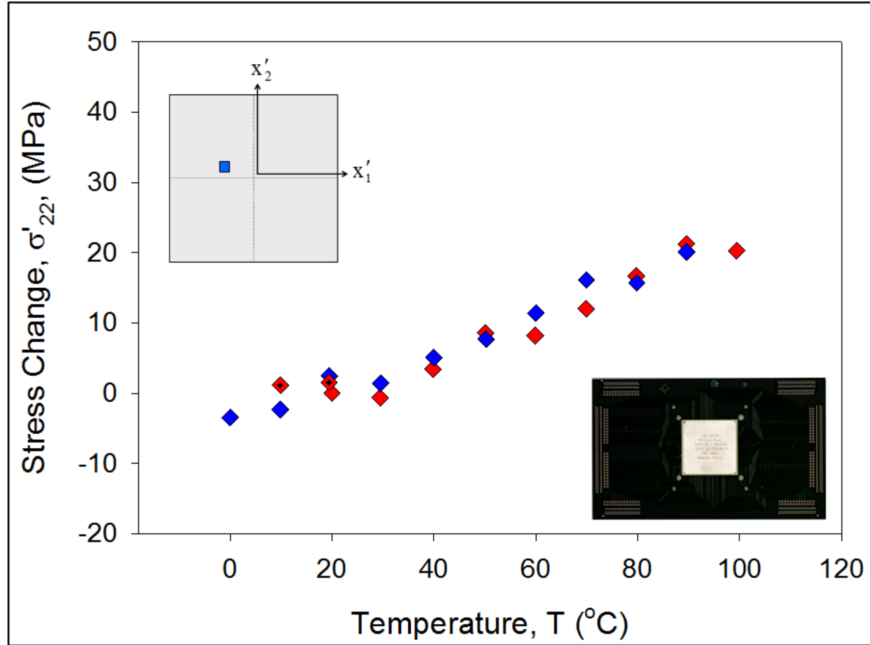


Figure 8.20: Variation of In-Plane Normal Stress with Temperature (Near Die Center)

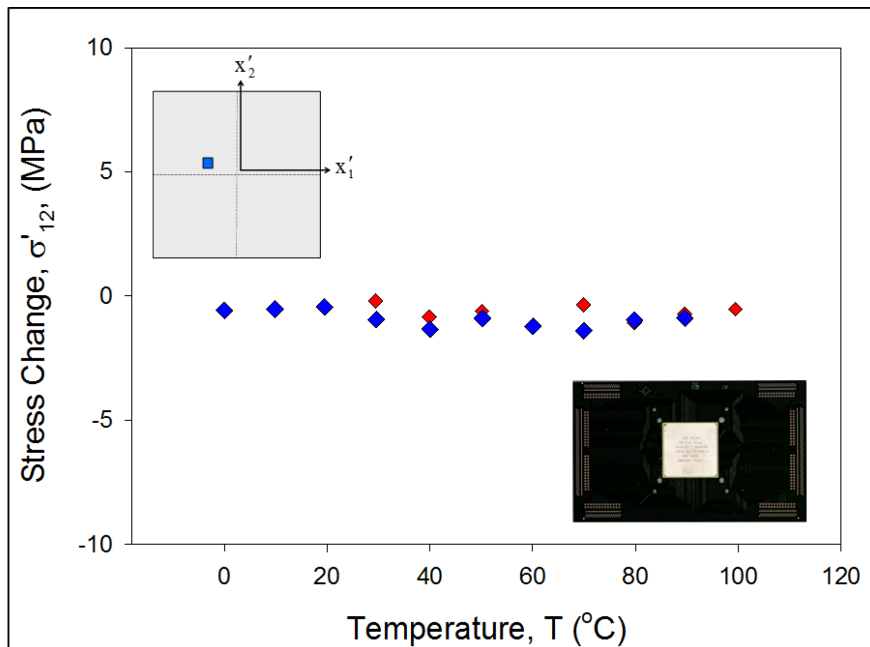


Figure 8.21: Variation of In-Plane Shear Stress with Temperature (Near Die Center)

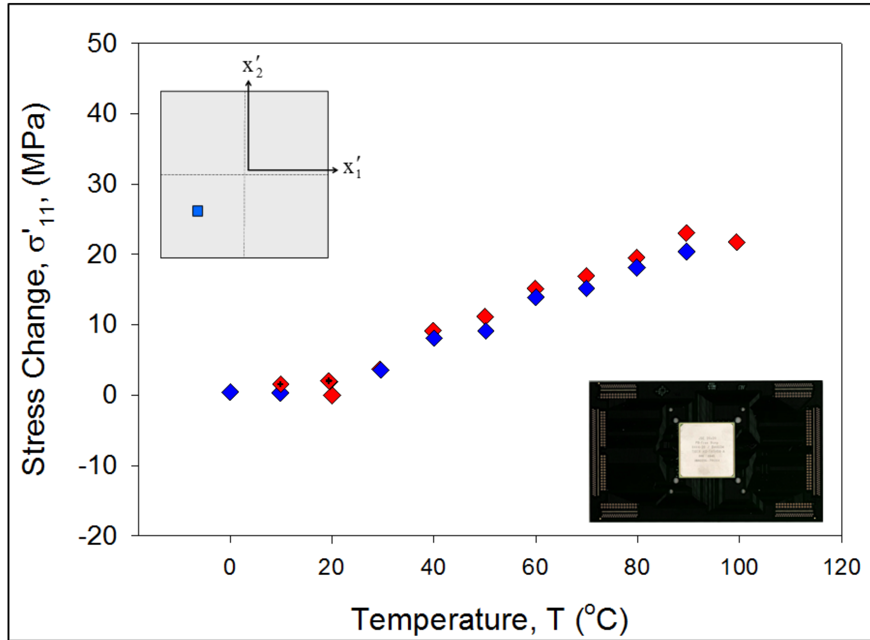


Figure 8.22: Variation of In-Plane Normal Stress with Temperature

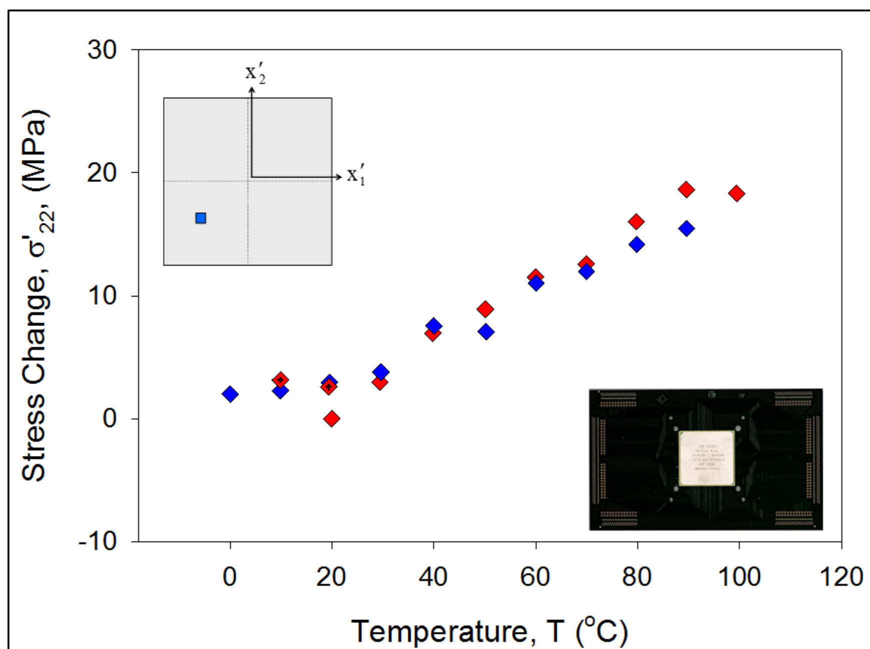


Figure 8.23: Variation of In-Plane Normal Stress with Temperature

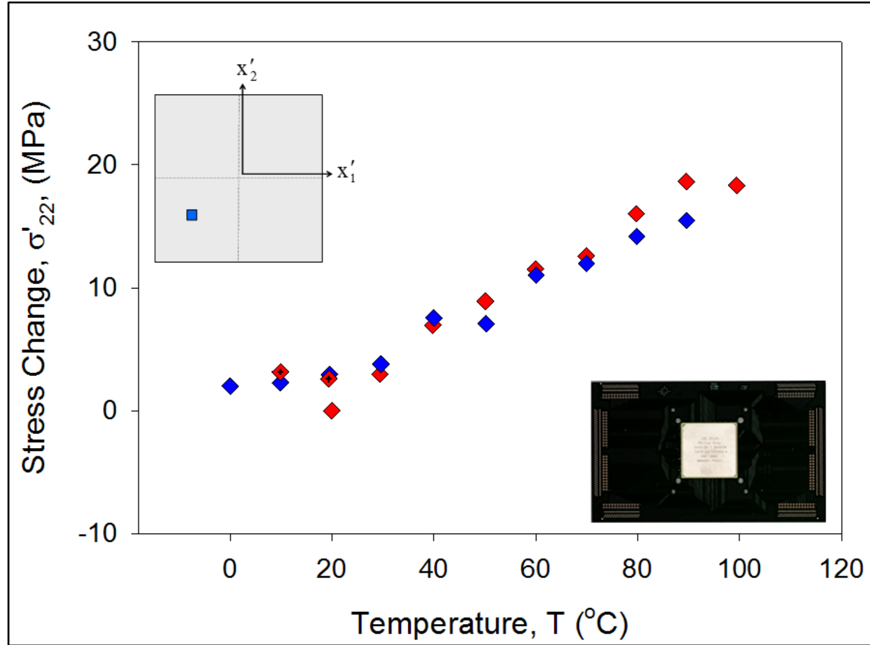


Figure 8.24: Variation of In-Plane Shear Stress with Temperature

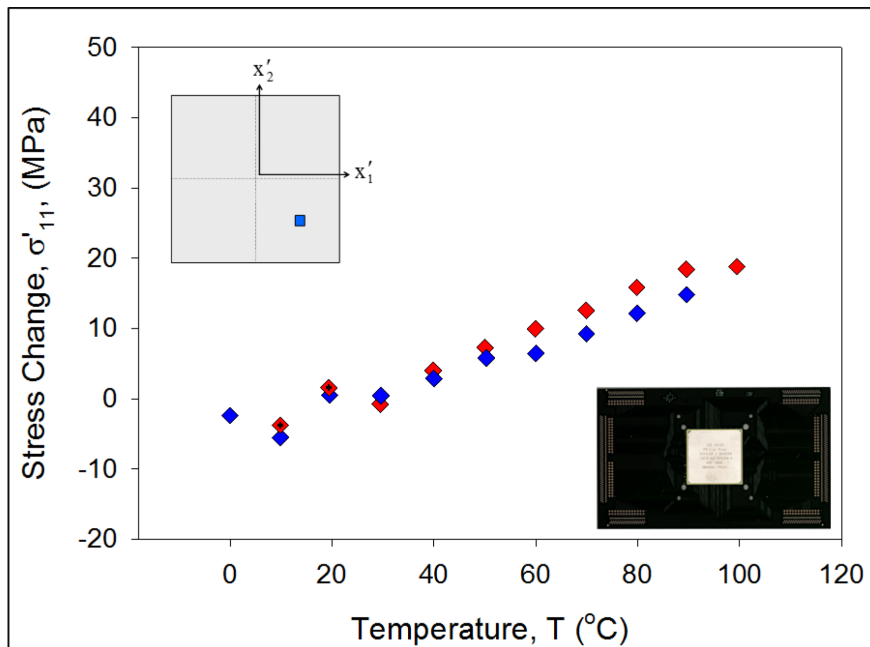


Figure 8.25: Variation of In-Plane Normal Stress with Temperature

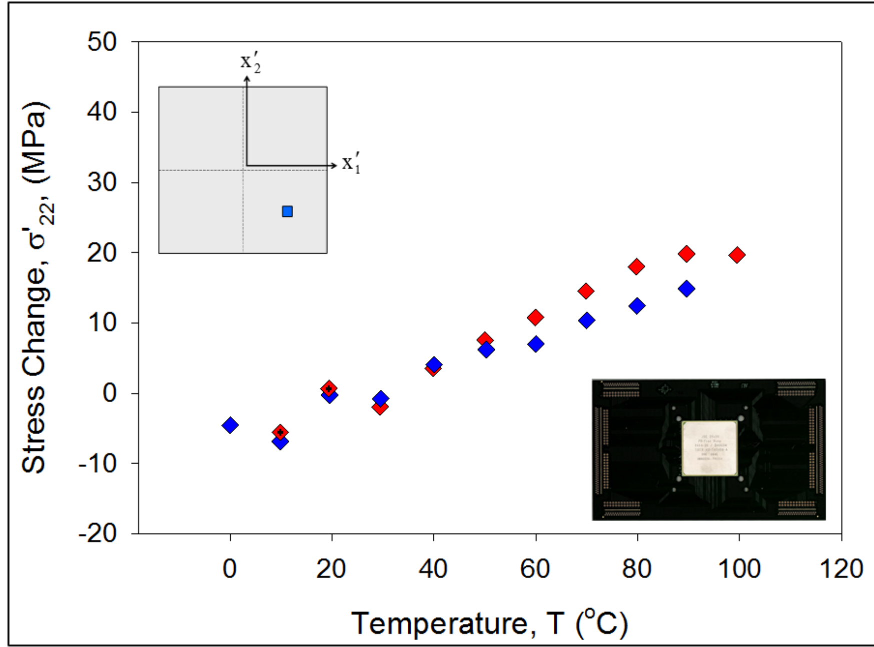


Figure 8.26: Variation of In-Plane Normal Stress with Temperature

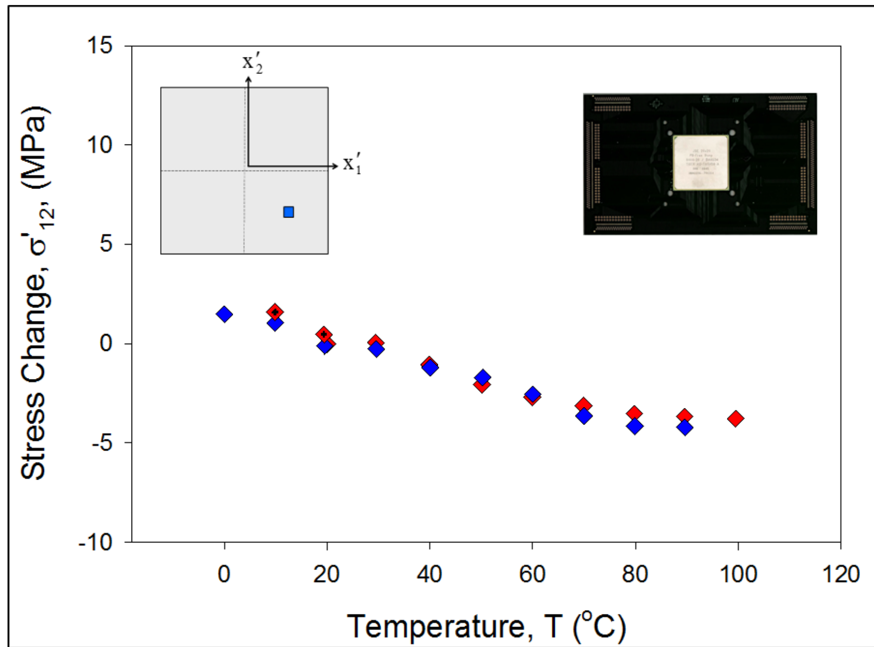


Figure 8.27: Variation of In-Plane Shear Stress with Temperature

Chapter 9

Die Stresses Due to Heat Sink Clamping

9.1 Introduction

In a typical server application, the CLGA studied in Chapter 5, would have solder balls attached to the lands of the HiTCE substrate. At this stage of assembly, the package would be referred to as a ceramic ball grid array (CBGA). The CBGA assembly would then be relowed to a large laminate printed circuit board. A second level underfill would then be applied between the HiTCE substrate and PCB, surrounding the larger BGA balls. Typical microprocessor packages in modern servers and other high performance applications produce a large amount of heat from normal use. The heat can degrade performance and may adversely affect long term reliability of both the first and second level interconnections. A typical solution is to apply a second level thermal interface material (TIM2) and mechanically attach a heat sink to the assembly as shown schematically in Figure 9.1.

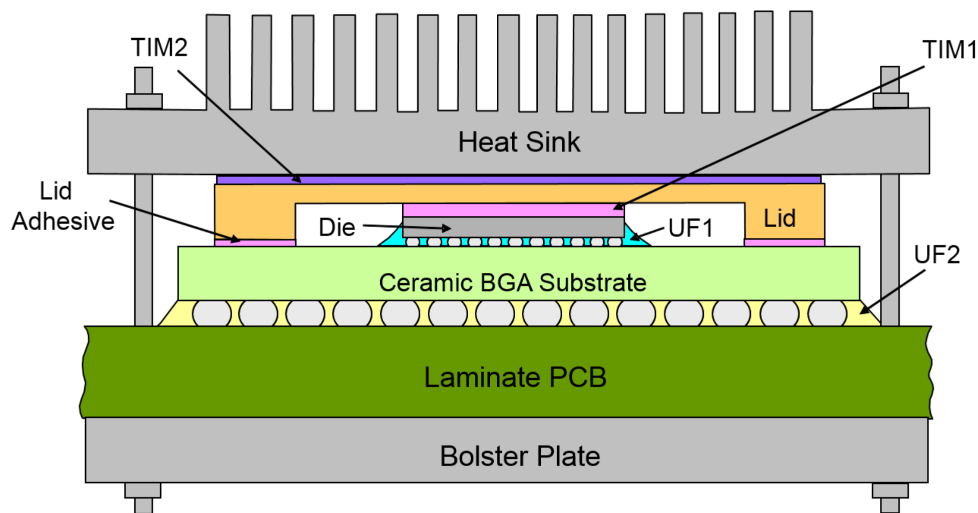


Figure 9.1: CBGA Heat Sink Clamping Geometry

The goal of the heat sink is to remove as much heat from the chip as possible. This creates an interface of two surfaces that are not perfectly flat or smooth. The second level thermal interface material serves to provide an effective path for heat as it leaves the chip. All surfaces have asperities, meaning there is not perfect contact between two mating surfaces. This increases the thermal resistance impeding the heat leaving the chip during use. The second level thermal interface material addresses the issue of asperities [188]. To address any flatness issues and to provide mechanical reinforcement, the heat sink is mechanically attached, typically bolted, to a base plate. This setup effectively squeezes the CBGA and motherboard assembly until it is approximately flat, with any excess TIM2 material evacuating the perimeter of the lid/heat spreader.

The mechanical attachment of the base plate, often referred to as a bolster plate, and the heat sink itself applies direct mechanical loading to the lid of the CBGA. The only compliant material in the force path from the heat sink to the die itself is the thin TIM1 layer. The TIM1 layer is typically only thick enough to fill in any asperities in the die and lid, so that the compliance it does provide is negligible. This means the application of the heat sink, while aiding the thermal performance, may induce large stresses to the die itself.

9.2 Experimental Characterization of Die Stresses due to Heat Sink Clamping

9.2.1 CBGA on Test Board Assemblies

In order to measure the effect of heat sink clamping on the device side die stress of the CBGA packages, several pre-assembled test boards, as shown in Figure 9.2, were subjected to controlled, simulated heat sink clamping. The pre-assembled boards contained test chips that were not available for probing at the bare die stage. Thus, for this case the reference state was taken to be the assembled test board, and the current state, or measurement state was taken to the heat sink loaded assembly. The extracted stress components using this approach were the stress changes occurring due to heat sink clamping. Numerical justification of this method for measuring stress changes was carried out by using the previously discussed data

taken from a number of CLGA assemblies, and then using various states of assembly as the reference state to evaluate stress changes. For example, the resistance values at each site on a die after die attachment in the CLGA were considered to be the reference state. The measurement state for the sensor resistances was taken to be after lid attachment. The stress differences calculated using these values were the increases (changes) in stress between die attachment and lid attachment. They were compared to the values found by using the bare die as the reference state and measuring both the die attached packages and lidded packages. Stress calculations using the differential method were found to be within one half of one percent error when compared to calculations using differences of absolute stresses with the bare die as the reference state. Details of this study can be found in Appendix A.

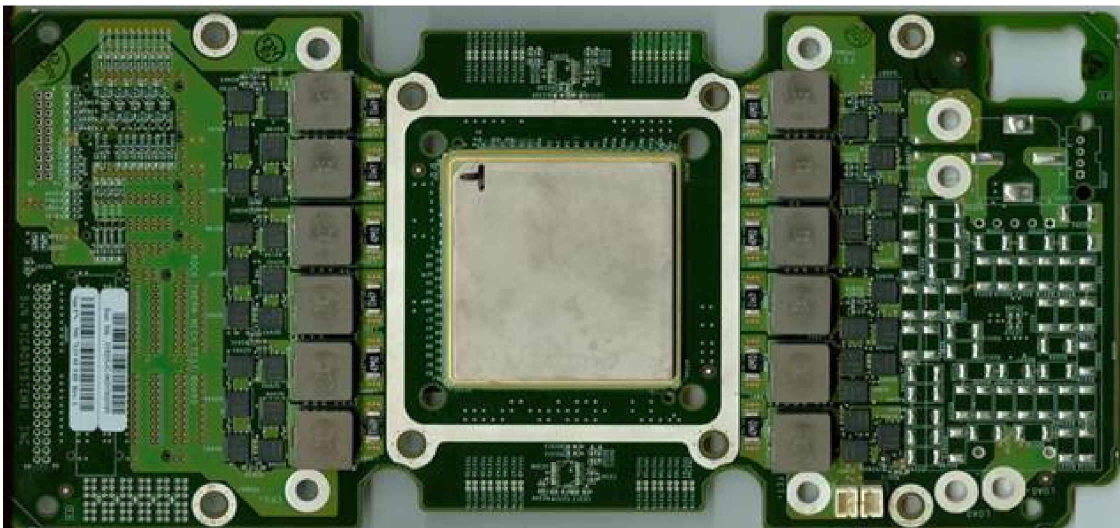


Figure 9.2: Pre-Assembled Test Board for Clamping Experiments

The pre-assembled test boards shown in Figure 9.2 were used as the reference state for the resistances used in the stress calculations. Thus, the stresses reported in this chapter are all *stress changes*, not absolute stresses. This is a careful distinction that must be made when analyzing the results.

In the field, blades containing microprocessor assemblies resembling the test board in Figure 9.2 are replaced by service technicians on location. After application of a TIM2 material, the heat sink is bolted down to the bolster plate as previously shown in Figure 9.1.

When bolting the heat sink, no measurement is taken as to the applied torque used on the fasteners and an unknown state of loading is applied to the CBGA heat spreader. A laboratory clamping fixture made by the industry partner for this study is shown in Figure 9.3. The company made this fixture to replicate the actual fastening system used in high performance servers while keeping the form factor of the assembled test boards used for this study. Instructions were given as to the field instructions for heat sink installation, which included the fasting pattern, or order in which each bolt was tightened.

Initial measurements of die stresses caused by heat sink clamping were made using the fixture shown in Figure 9.3. Sensor measurements were taken as a function of turns of each fastener, and the fasteners were tightened until the assembly was locked in place. The results for in-plane normal stress σ'_{11} at the center of the die are shown in Figure 9.4. Analogous results for σ'_{22} are shown in Figure 9.5. The results show an additional 40 to 50 MPa of compressive normal stress at the center of the die under full loading of the fixture. It is noted that the normal stresses at the center of the die increase linearly with number of turns of the applied fasteners. Stress measurements for in plane normal stress σ'_{11} at the corner of the die are shown in Figure 9.6. Analogous results for σ'_{22} are shown in Figure 9.7. While the normal stresses seen in the corner of the die increase monotonically, they are not as linear with the number of turns as the in-plane stresses seen in the center of the die. The in-plane normal stresses in the corner increase until the final turn of the fasteners and remain constant from turn 8 to 9. Between turns 8 and 9, the fasteners in the clamp bottomed out, and mechanical locking prevented further stress increase.

While the above results were valuable, they did not allow correlation with the actual forces applied to the die. To measure the forces being applied to the heat spreader as opposed to simply correlating die stress to fastener position, a thin resistive force sensor was implemented as shown in Figure 9.8. An image of the force sensor in the test fixture is shown in Figure 9.9. To visualize the placement of the sensor in use, the setup with the thin force sensor is shown schematically in Figure 9.10. Prior to testing, each reusable force

Figure 9.3: Clamping Fixture Provided by Test Sponsor

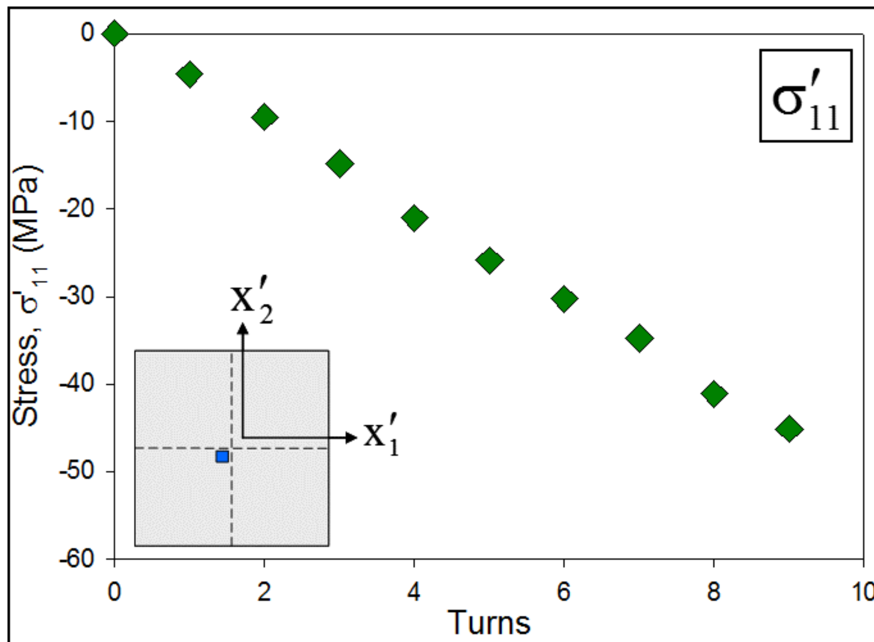


Figure 9.4: In-plane Normal Stress Due to Clamping (Die Center)

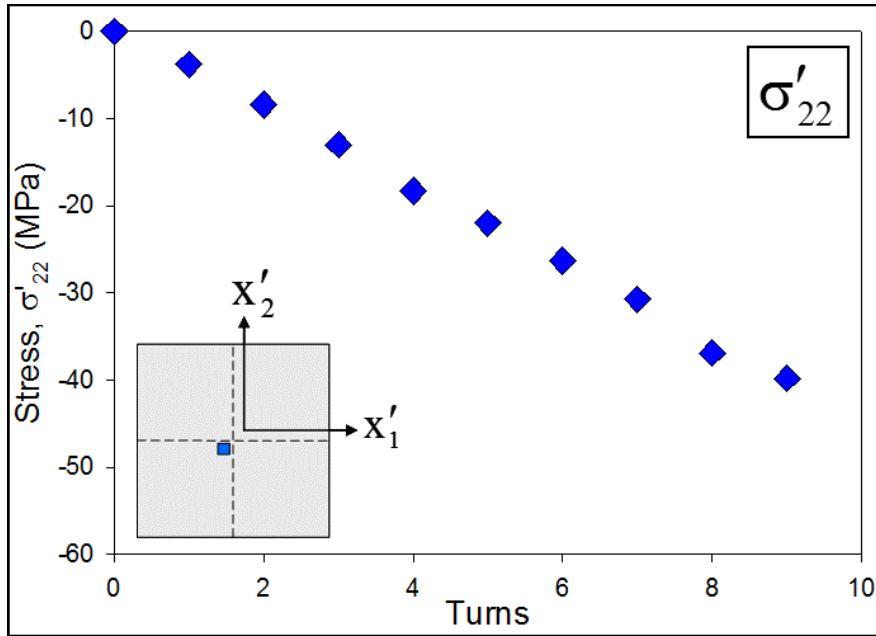


Figure 9.5: In-plane Normal Stress Due to Clamping (Die Center)

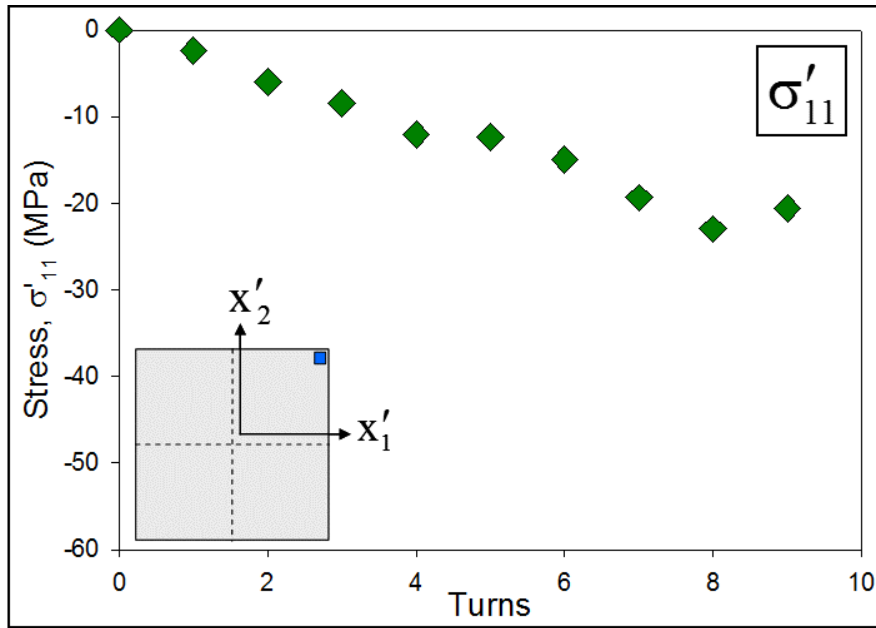


Figure 9.6: In-plane Normal Stress Due to Clamping (Die Corner)

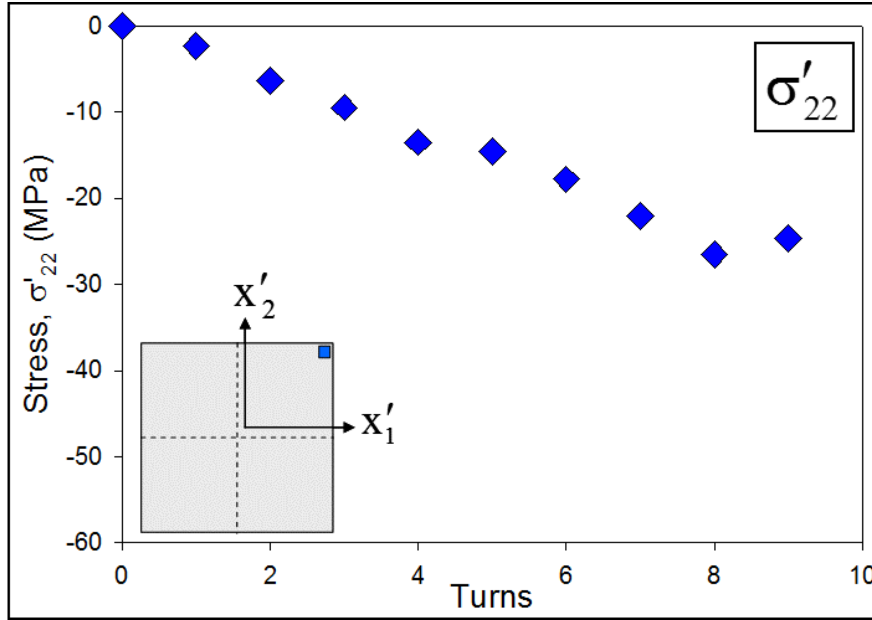


Figure 9.7: In-plane Normal Stress Due to Clamping (Die Corner)

sensor required calibration as shown in Figure 9.11. The results for in-plane normal stress σ'_{11} at the center of the die are shown in Figure 9.12 . Analogous results for σ'_{22} are shown in Figure 9.13. The results compare favorably with earlier data and again show an additional 40 to 50 MPa of compressive normal stress at the center of the die under full loading of the fixture (55 lbs or $\approx$ 250 N). As in the previous experiments, the normal stresses at the center of the die increased linearly with the number of turns of the applied fasteners. Stress measurements for in-plane normal stress σ'_{11} at the corner of the die are shown in Figure 9.14. Analogous results for σ'_{22} are shown in Figure 9.15. The corner data measured along with the force sensor show slightly more linear results, with any no apparent saturation occuring in the stress measurements.

While the experimental setup seen in Figure 9.3 was able to produce valuable data, there were issues with the measurements. First, there was undesirable variablity of force application, and the force level could not be easily related to the turns of the fasteners. While keeping the protocol for order of tightening, the fixture operator must decide how much of the total force desired is being applied by each fastener. This led to re-tightening and individual adjustment of fasteners. This method could be repeatable with the same

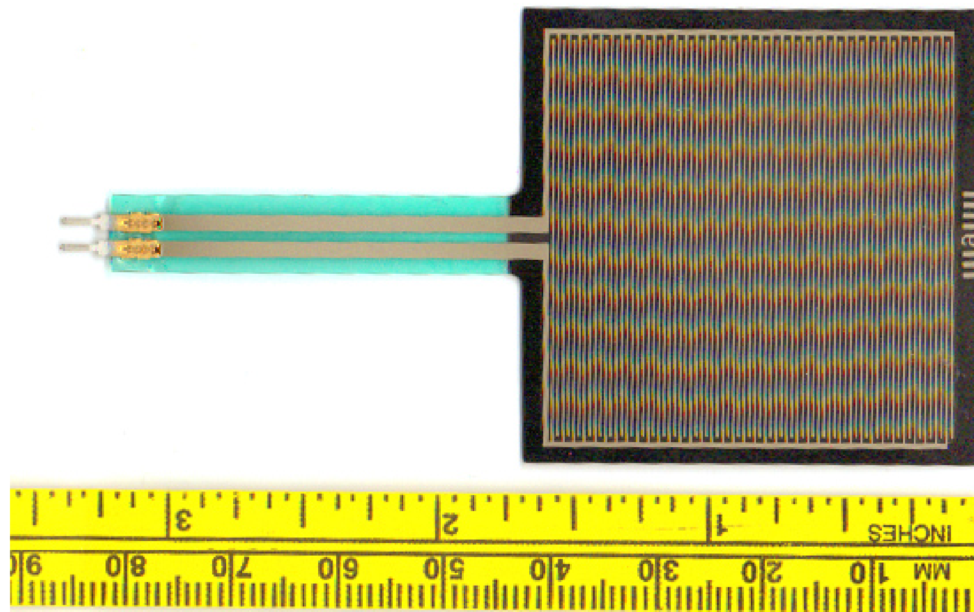


Figure 9.8: Thin Resistive Force Sensor

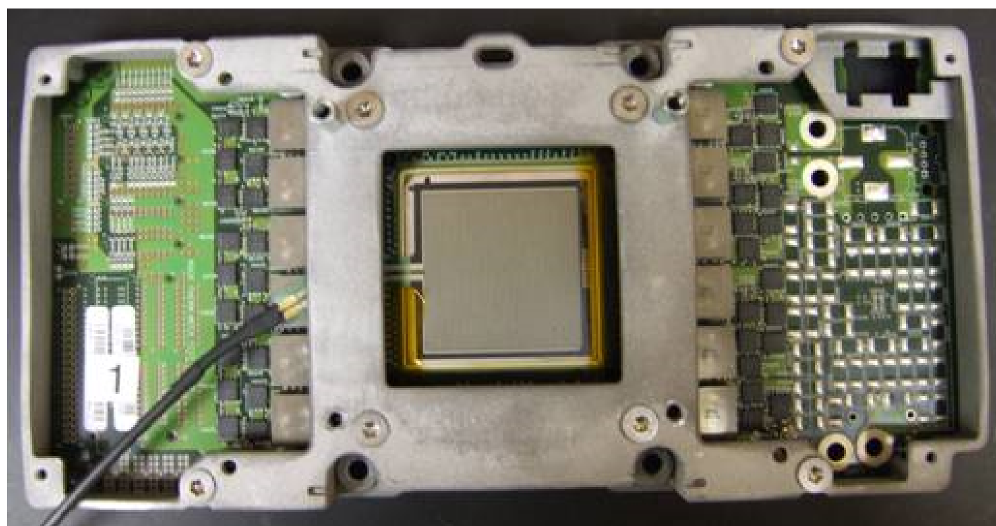


Figure 9.9: Thin Resistive Force Sensor in Clamping Fixture

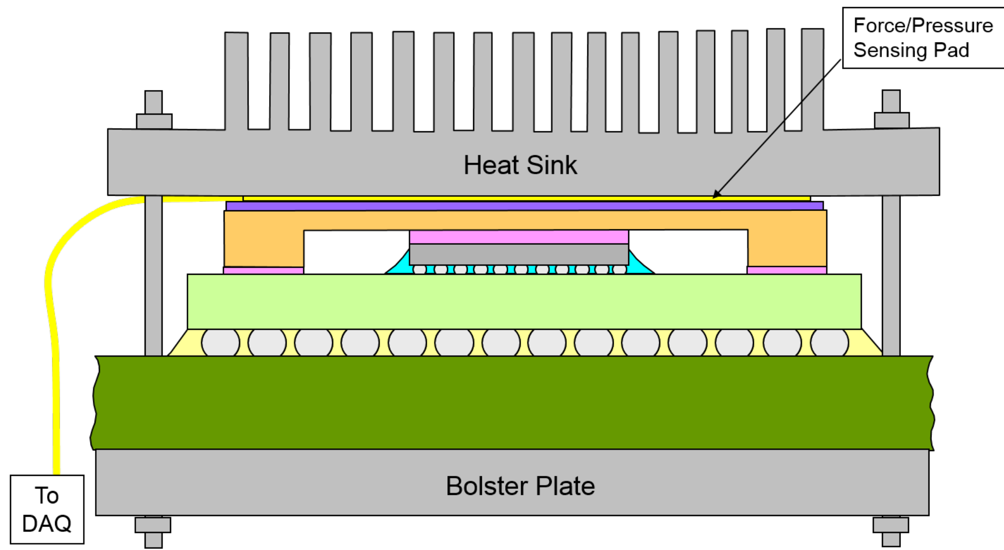


Figure 9.10: Schematic of Resistive Force Sensor in Clamping Fixture

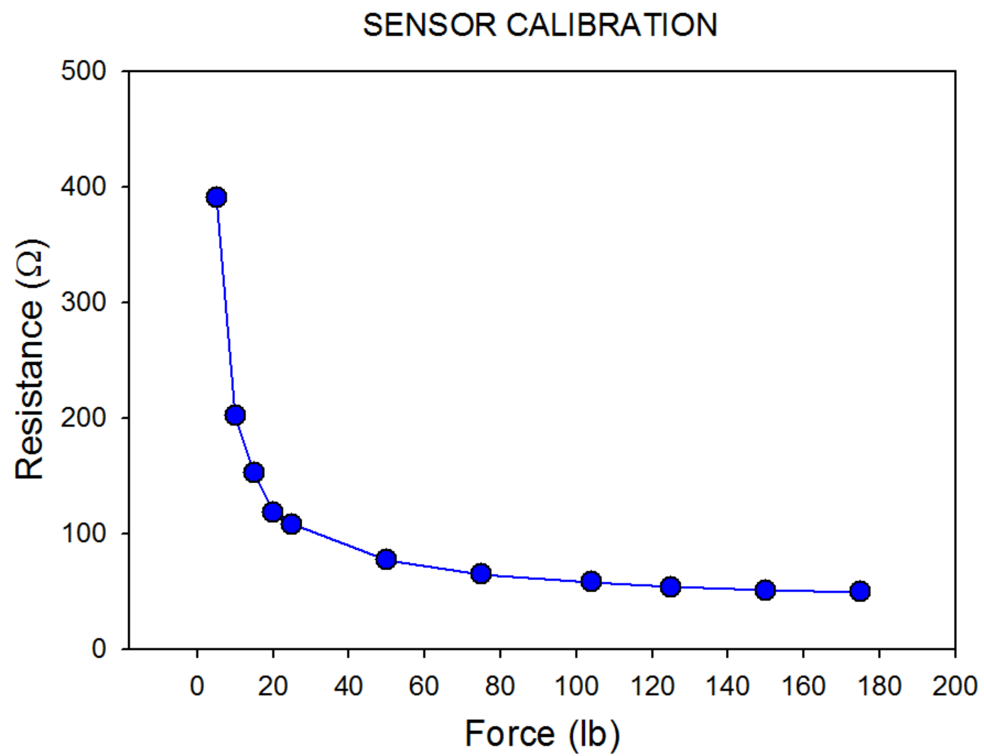


Figure 9.11: Resistive Force Sensor Calibration

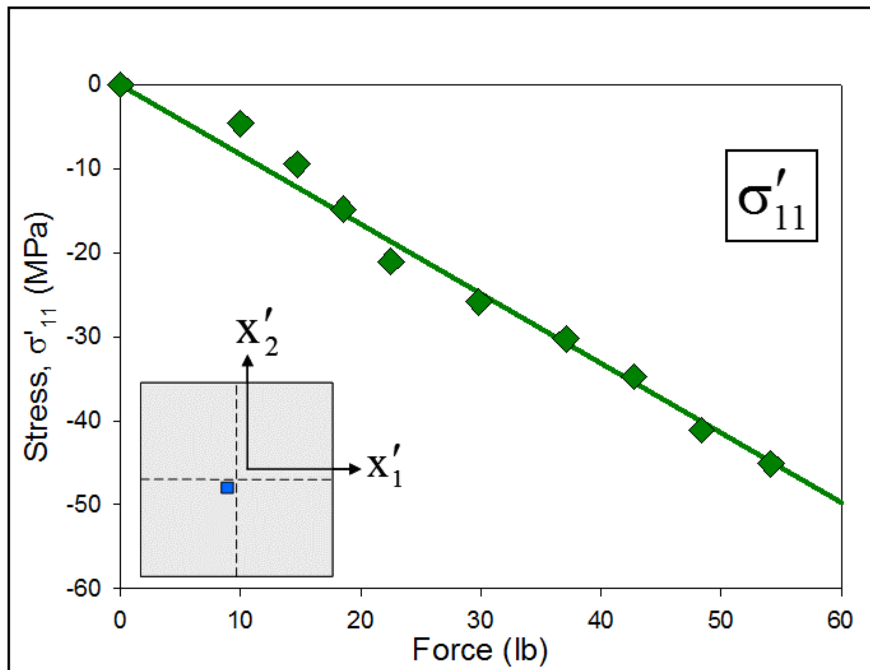


Figure 9.12: In-Plane Normal Stress Due to Clamping (Die Center)

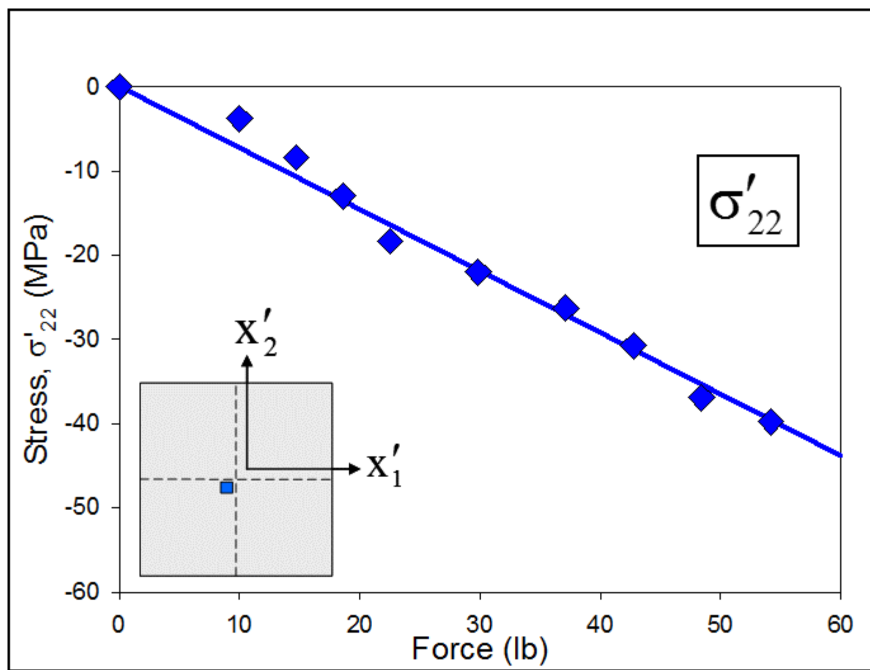


Figure 9.13: In-Plane Normal Stress Due to Clamping (Die Center)

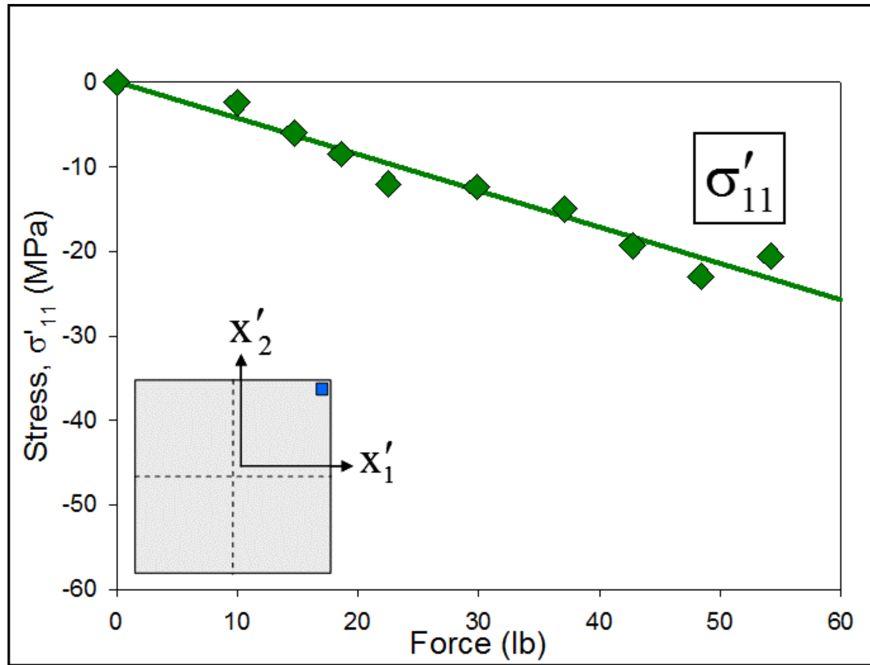


Figure 9.14: In-Plane Normal Stress Due to Clamping (Die Corner)

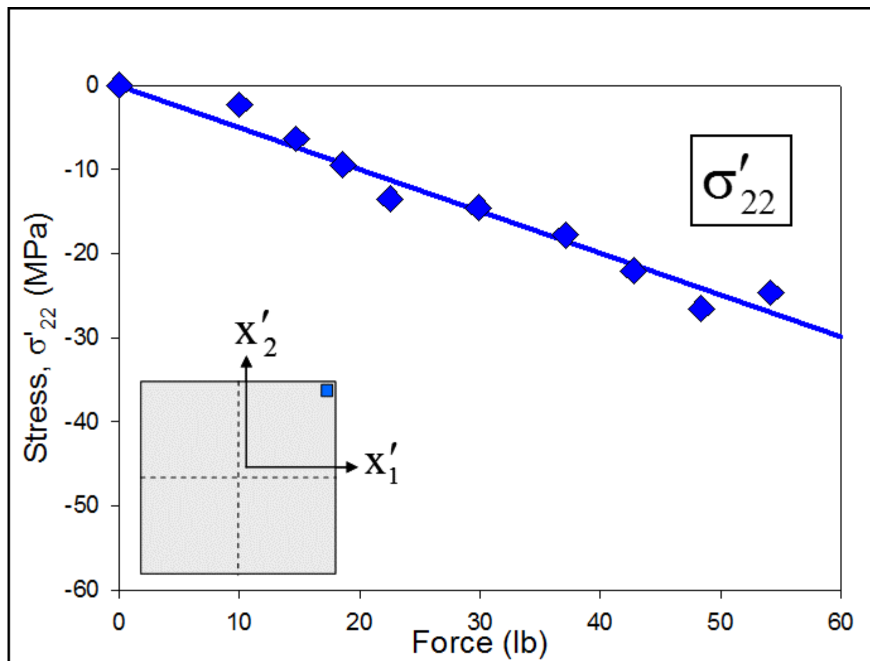


Figure 9.15: In-Plane Normal Stress Due to Clamping (Die Corner)

operator, but will vary from operator to operator. Second, the placement of the resistive force sensor was dependent on the visual alignment of the operator. Alignment was performed by ensuring the distance from each edge of the sensor pad to the edge of the lid was equal on all sides. This could lead to variability from sample to sample, if the sensors were not carefully placed with calipers or other measurement devices. Third, the size of the resistive sensor was slightly smaller than the heat spreader on the CBGA assemblies. While undetectable in Figure 9.8, there was a small lip surrounding the sensor element. Since the element was smaller than the heat spreader, a shim was required to obtain direct force application to the sensor and subsequently the CBGA. The use of the shim carried with it the same issues of visual alignment seen with the force sensor itself. The most critical issue with using a shim was that it must fit within the lip of the sensor, meaning the load was not applied to the entire heat spreader unlike an actual heat sink. All of these issues led to the development of a new clamping fixture as described below.

These issues in the measurement of the CBGA test board assemblies were addressed in steps, with the most critical issue being the uneven application of force to the heat spreader during testing. The clamping fixture shown in Figure 9.16 addressed the issue of uneven force application. This test clamp is comprised of a thick base and bulkhead, to which a power screw was attached. To maintain planarity of the simulated heat sink, two low friction guide pins located the simulated heat sink (SHS). Within the SHS, a ball bearing and keeper were used to ensure a purely axial load, so that no torque could be applied from the power screw. This fixture also employed four nylon locating pins to positively locate each assembly in the test fixture.

The resistive force sensor was also used in conjunction with the developed clamping fixture. The same issues were present due to its size relative to the heat spreader, and the need for a shim. A second iteration of the clamping fixture was then developed to address those issues. As shown in Figure 9.17, a second piece of aluminum was added to the previous simulated heat sink along with a second set of low friction glides and a button load

cell. The button load cell was centered on the simulated heat sink. The top surface of the load cell was radiused to ensure that forces applied through it were applied through a single point. The load cell was wired to a project box, with appropriate binding posts connected to an Omega Engineering DP25B-S panel meter programmed with the appropriate sensitivity and excitation for the load cell. The new test clamping fixture and readout are shown in Figure 9.17.

Figure 9.16: Simulated Heat Sink Clamping Fixture (First Edition)

The final version of the developed test fixture was able to repeatably apply a known load, position the board accurately, and apply the load repeatably to the entire area of the heat spreader. Using this fixture, several tests were performed on 5 CBGA test board assemblies. The measured variations of the in-plane normal stresses with the applied clamping load for a single assembly are shown in Figure 9.18 and Figure 9.19. Figure 9.20 shows the variation of the average in-plane normal stress σ'_{11} at the center of the die with the applied load for all 5 assemblies. The error bars at the data points represent the standard deviations of the measurements for the 5 assemblies. Figure 9.19 shows analogous results for the average

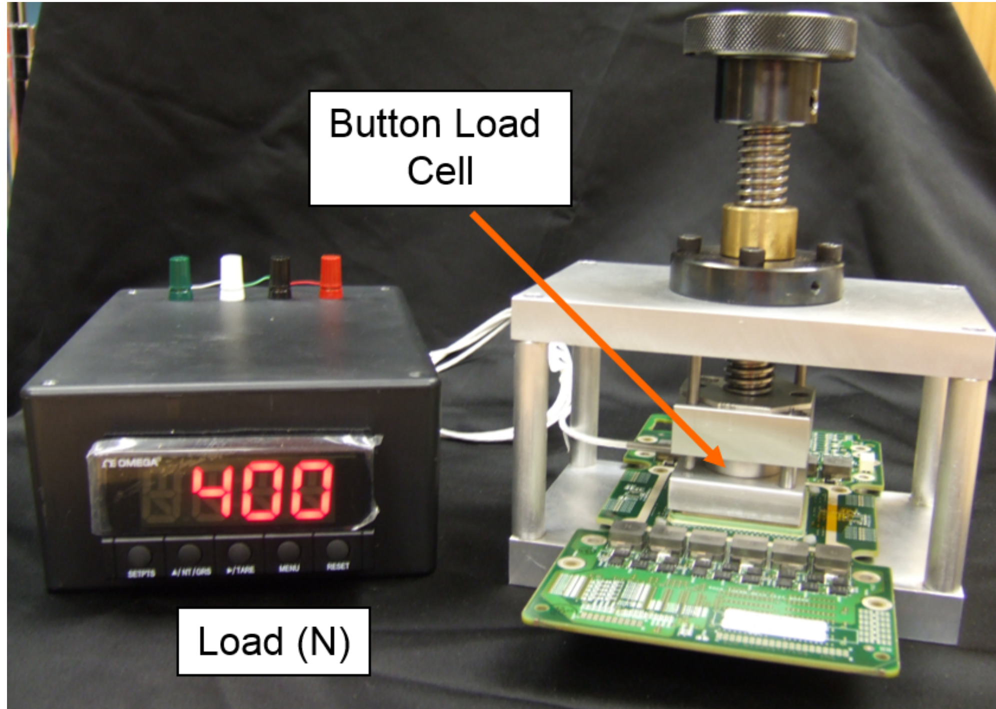


Figure 9.17: Second Iteration Clamping Fixture with Instrumentation

in-plane normal stress σ'_{22} at the center of the die. Figure 9.22 and Figure 9.23 show the analogous variations of in-plane normal stresses σ'_{11} and σ'_{22} with clamping force for a sensor site at the corner of the test die.

9.2.2 CLGA in Socket Assemblies

In addition to the CBGA clamping study discussed above, a small sample of CLGA assemblies (Figure 5.16) were clamped using the test board and socket discussed previously in Chapter 5. These measurements were performed with the test fixture shown in Figure 9.9 and the resistive force sensor in Figure 9.8. Schematically, the CLGA and socket assembly with heat sink is shown in Figure 9.24. The measured in-plane normal stress σ'_{11} at the center of the die as a function of applied load is plotted in Figure 9.25. The sensor site resistances were only measurable at higher levels of force. For lower load levels, the force was not sufficient to allow the compliant socket to make electrical contact with the CLGA pads near the center of the land grid array.

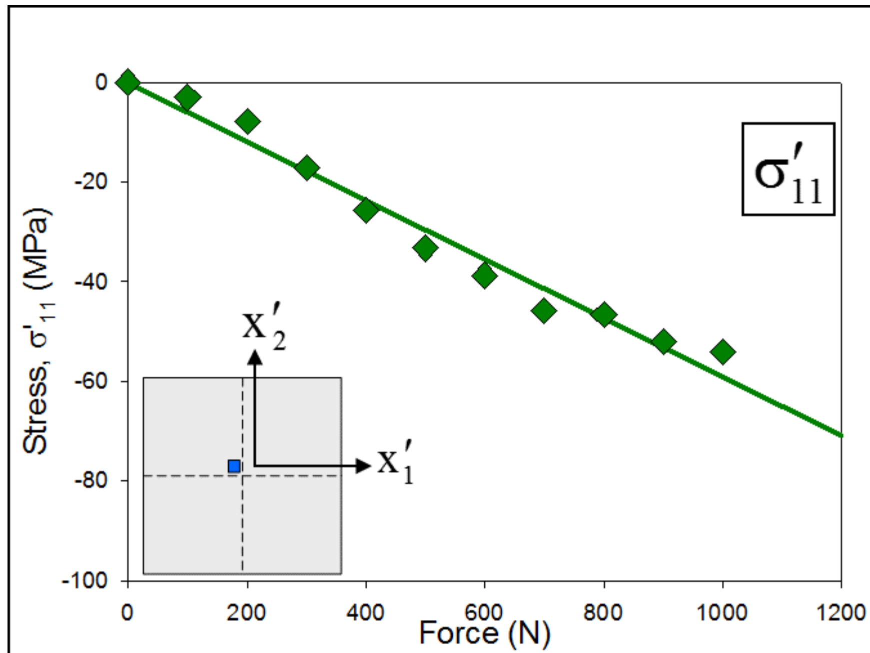


Figure 9.18: In-Plane Normal Stress Due to Clamping (Die Center, Single Sample)

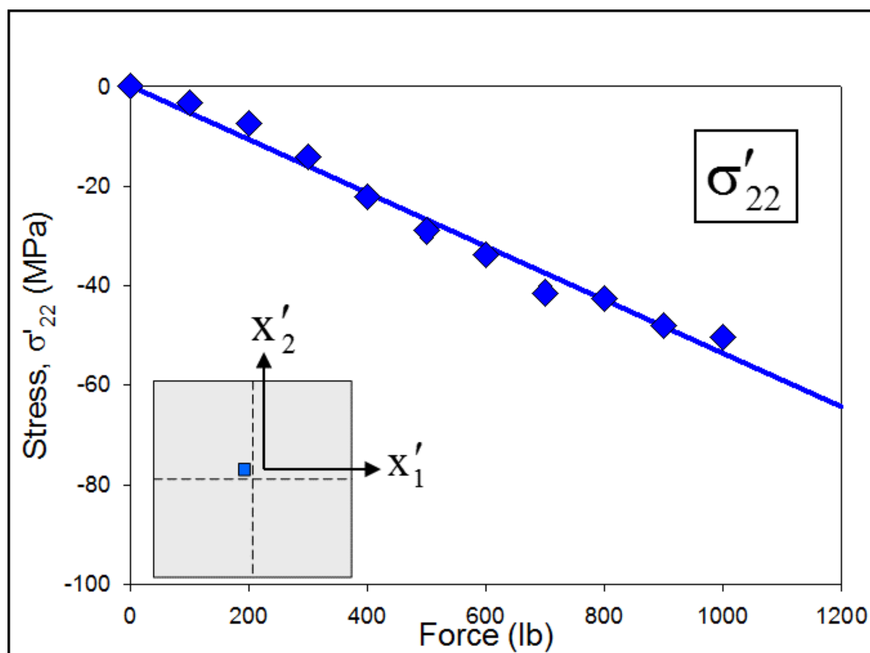


Figure 9.19: In-Plane Normal Stress Due to Clamping (Die Center, Single Sample)

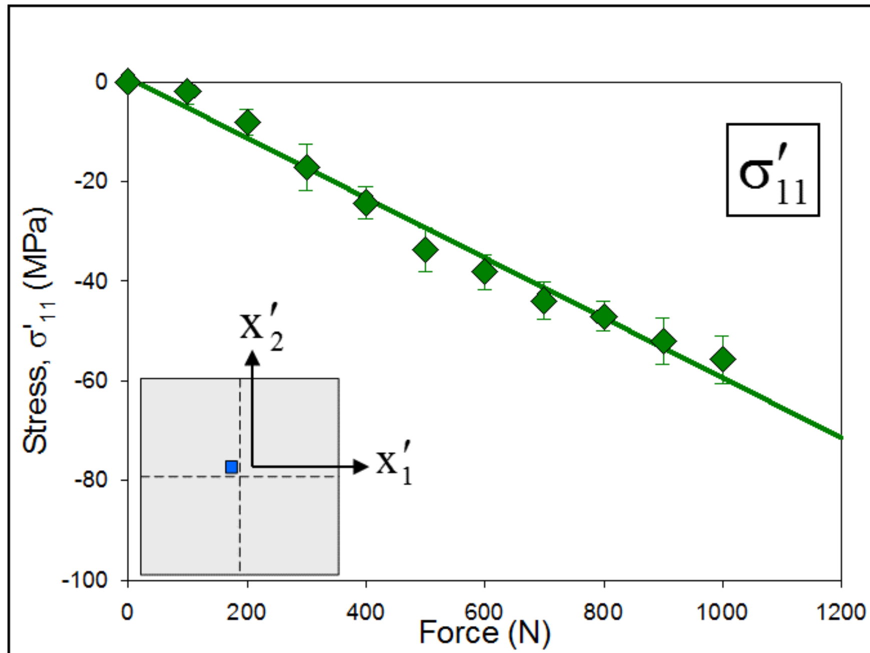


Figure 9.20: Average In-Plane Normal Stress Due to Clamping (Die Center)

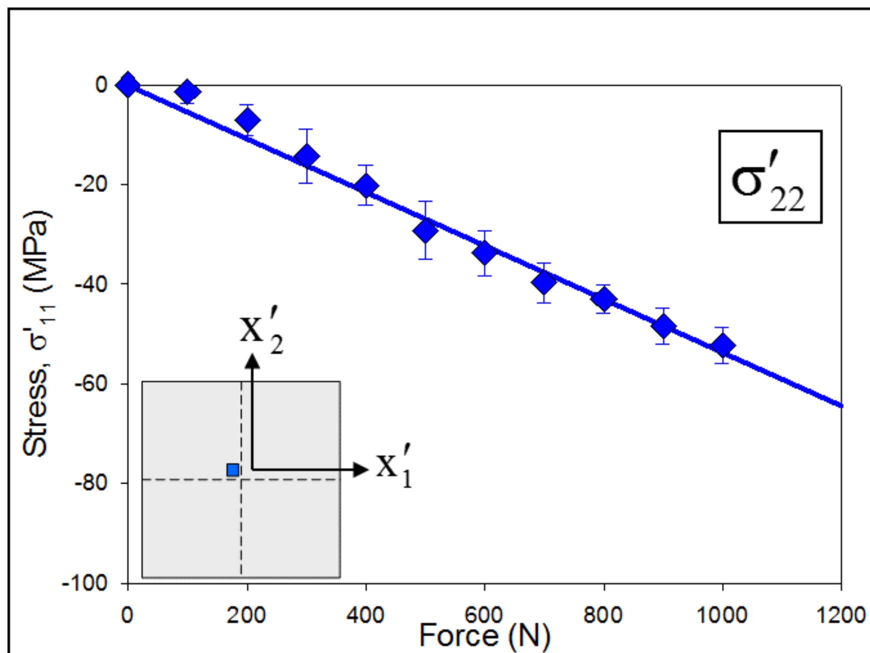


Figure 9.21: Average In-Plane Normal Stress Due to Clamping (Die Center)

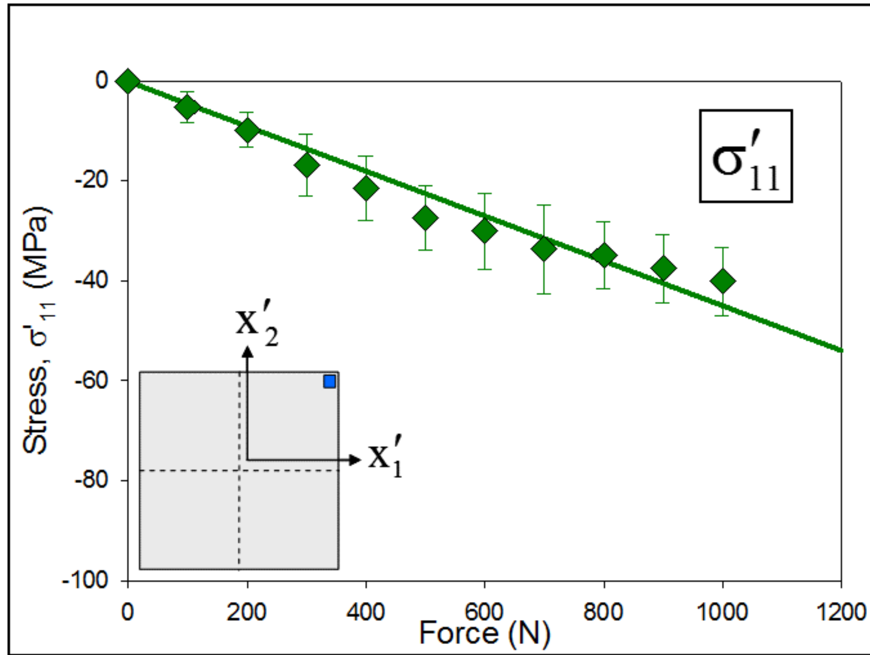


Figure 9.22: Average In-Plane Normal Stress Due to Clamping (Die Corner)

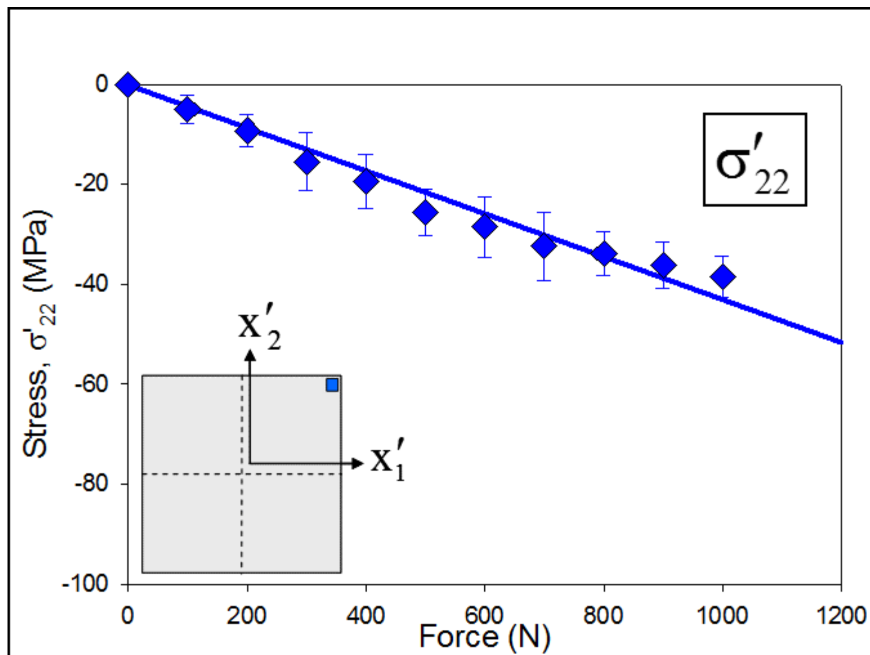


Figure 9.23: Average In-Plane Normal Stress Due to Clamping (Die Corner)

In earlier measurements in Chapter 5 made for each of the assembly steps of the CLGA assemblies, it was necessary to add an adjustment screw to the back plate of the test setup to bring the test board, CLGA, and socket in electrical contact with each other. This was due to the curvature of the test board and to a smaller degree, the CLGA substrate. The compliance of the socket, combined with the curvature of the assemblies leads to a need for more than minimal loading for proper electrical contact.

The stress in Figure 9.25 increases linearly with load. However, it is also noted that the data appear to be noisy relative to the analogous CBGA results in Figure 9.20. Similar results for σ'_{22} are plotted in Figure 9.26 for the die center rosette. In-plane normal stress variations with load at the corner rosette site are shown in Figure 9.27 and Figure 9.28. At this site, measurements could be made at all load levels, as good electrical contact was present at the corner LGA pads. Similar to CBGA tests, the results show a fairly linear response with increasing loads. Again, the data exhibit slightly more noise than found in the CBGA tests.

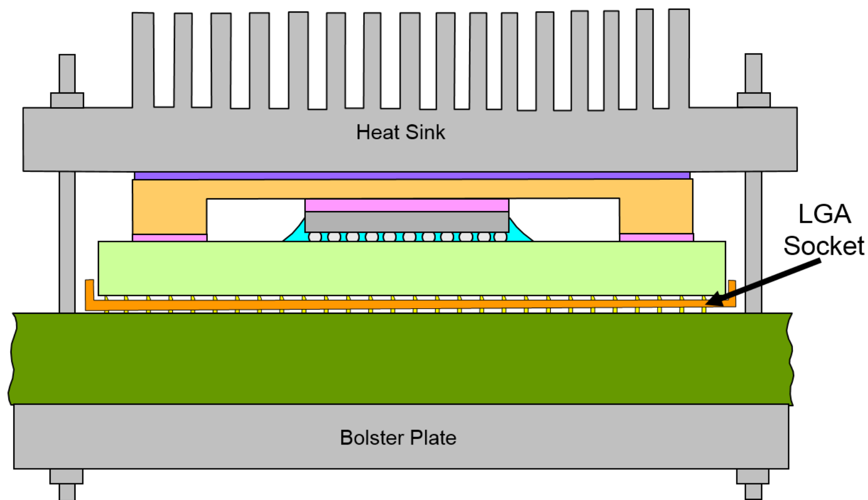


Figure 9.24: Schematic of CLGA Clamping Fixture

9.2.3 Comparison of CBGA and CLGA Clamping Response

To compare the results for CBGA on test board and CLGA in test socket assemblies in simulated clamping tests, the data from Figures 9.12-9.15 and Figures 9.25-9.28 were

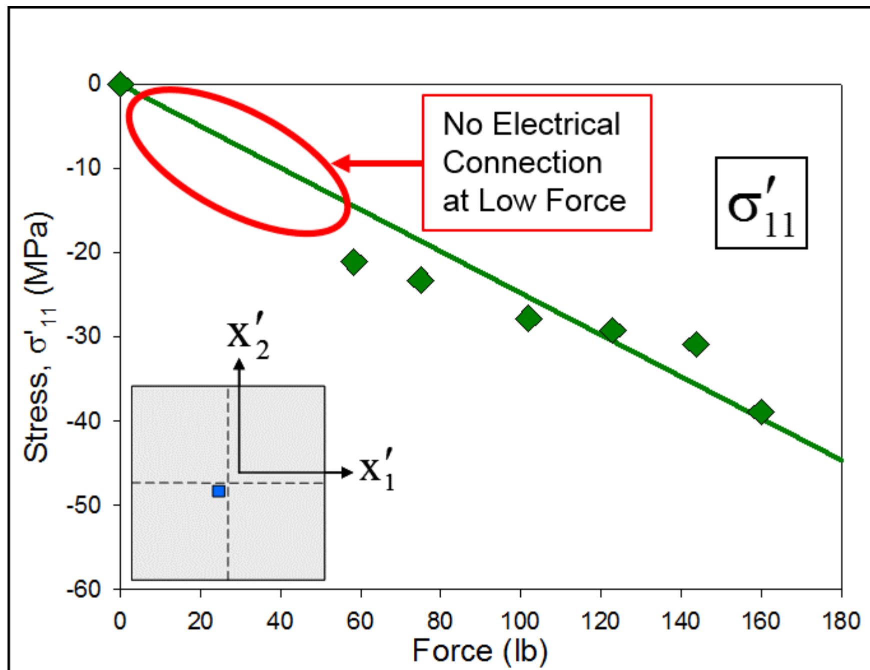


Figure 9.25: Average In-Plane Normal Stress Due to CLGA Clamping (Die Center)

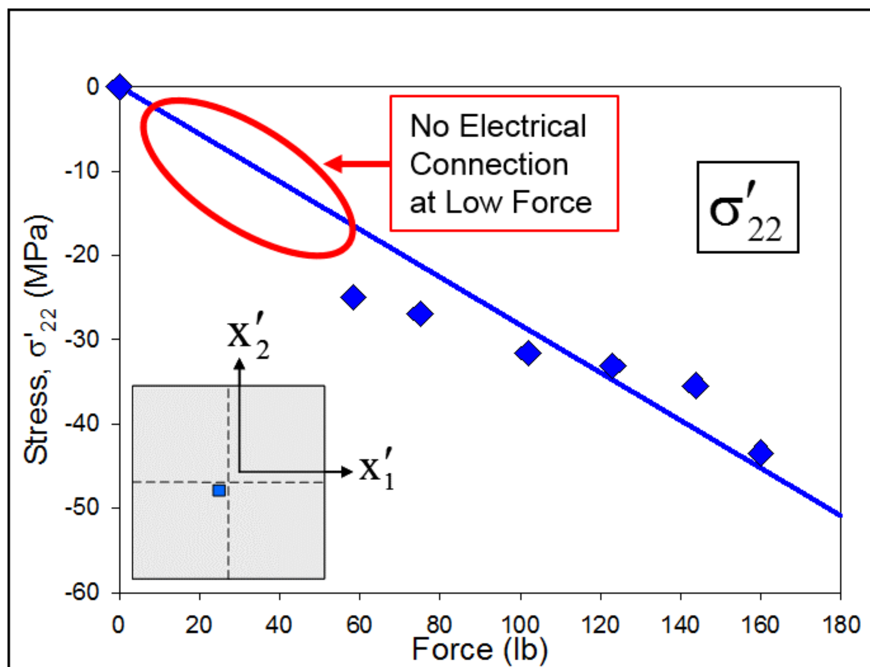


Figure 9.26: Average In-Plane Normal Stress Due to CLGA Clamping (Die Center)

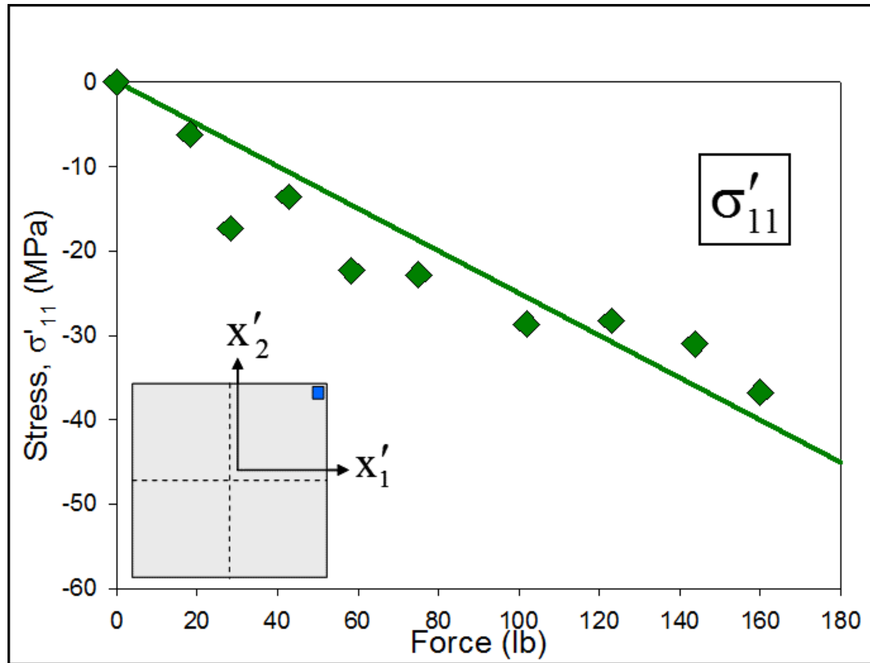


Figure 9.27: Average In-Plane Normal Stress Due to CLGA Clamping (Die Corner)

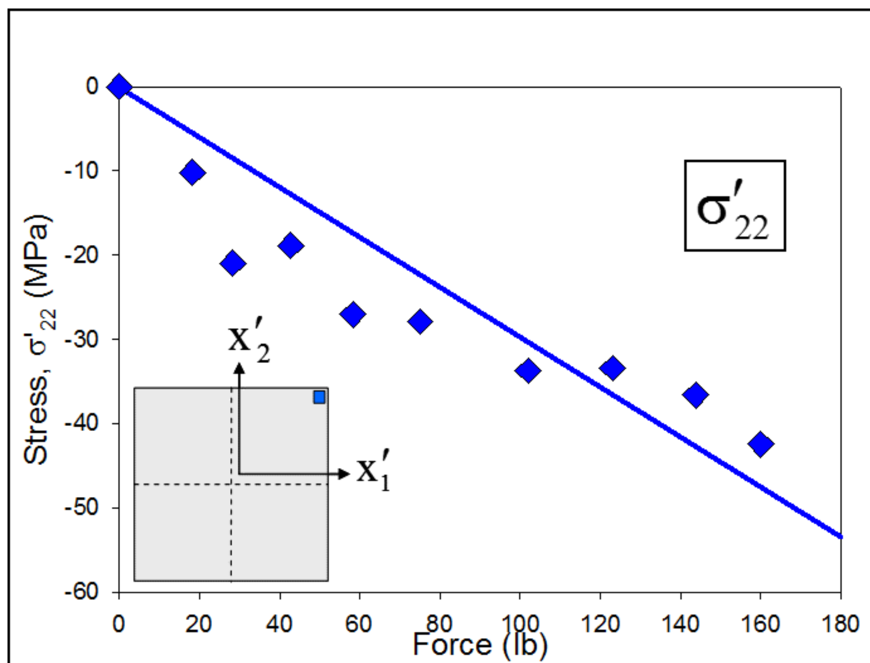


Figure 9.28: Average In-Plane Normal Stress Due to CLGA Clamping (Die Corner)

combined on new plots. All of these results involved the same clamping fixture (Figure 9.2) and resistive force sensor (Figure 9.8). As in all clamping data shown in this chapter, the stress values are stress changes from a reference state and not the absolute stresses. For the CLGA assemblies, the reference state was measured by manually probing the lands on the HiTCE LGA substrate. The reference state for the CBGA on board assemblies was measured before any clamping load was applied by the fixture. As the measurement conditions are the same for both assemblies, the results of both tests may be compared. Figure 9.29 shows measured data for in-plane normal stress σ'_{11} at the center of the die as a function of heat sink clamping force for both LGA and BGA architectures. Linear fits for each data set are also plotted where each fit has been forced through the origin at the known reference (zero stress) point of the stress change plot. The fit through the measured BGA data appears to represent the data well, while the fit forced through the origin of the measured LGA data is not the best fit to the data. The slope of the stress-force trend line of the measured CBGA data is approximately 3.5 times greater than the analogous slope of the trend line of the measured CLGA data, and the difference is greater if the fit through the LGA data is not forced through the origin. As expected, the results are similar for σ'_{22} at the same location, as shown in Figure 9.30. The difference in the trend line slopes for the σ'_{22} data is slightly less than for the σ'_{11} data. This could be due to the slightly off center location of the sensor rosette. If the rosette was perfectly centered on the die, both stresses would be equal due to symmetry.

Figure 9.31 shows measured data for σ'_{11} at the corner of the die for both types of assembly. These results at the corner show that the response the CLGA package is statistically equivalent to the response of the CBGA package. The response of σ'_{22} at the corner of the die to heat sink loading exhibits the same trends, as shown in Figure 9.32.

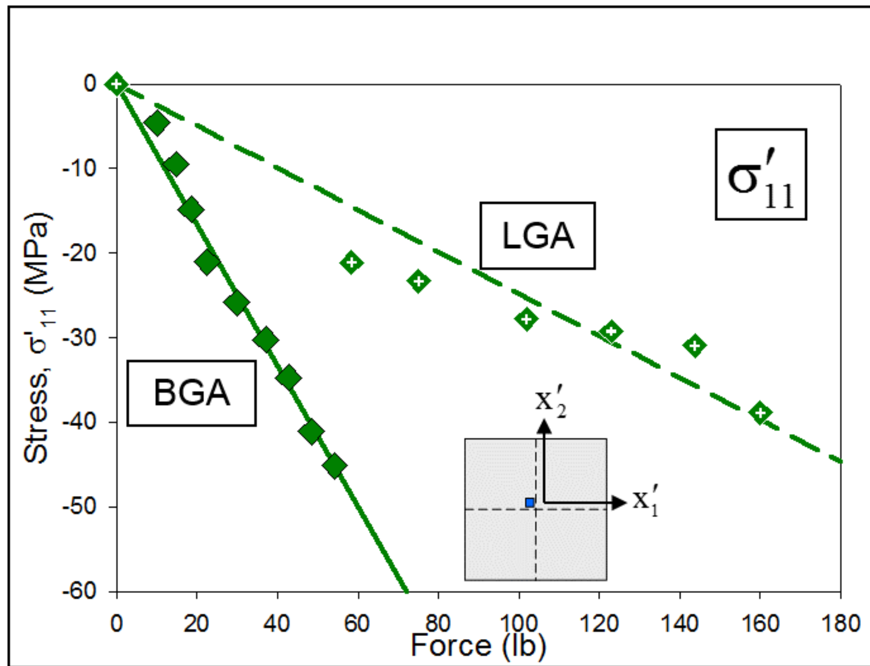


Figure 9.29: Comparison of In-Plane Normal Stress at Die Center (CBGA vs. CLGA)

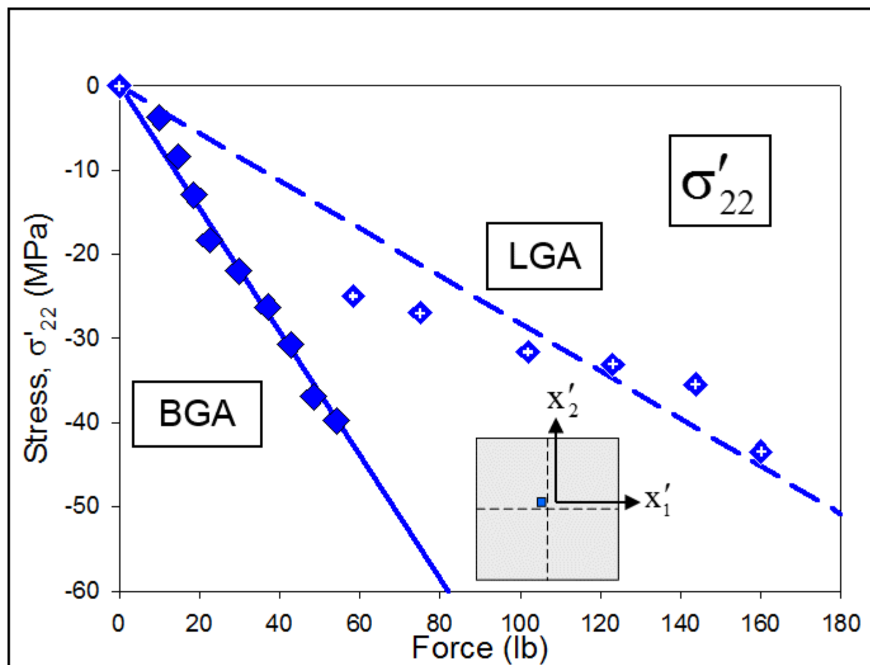


Figure 9.30: Comparison of In-Plane Normal Stress at Die Center (CBGA vs. CLGA)

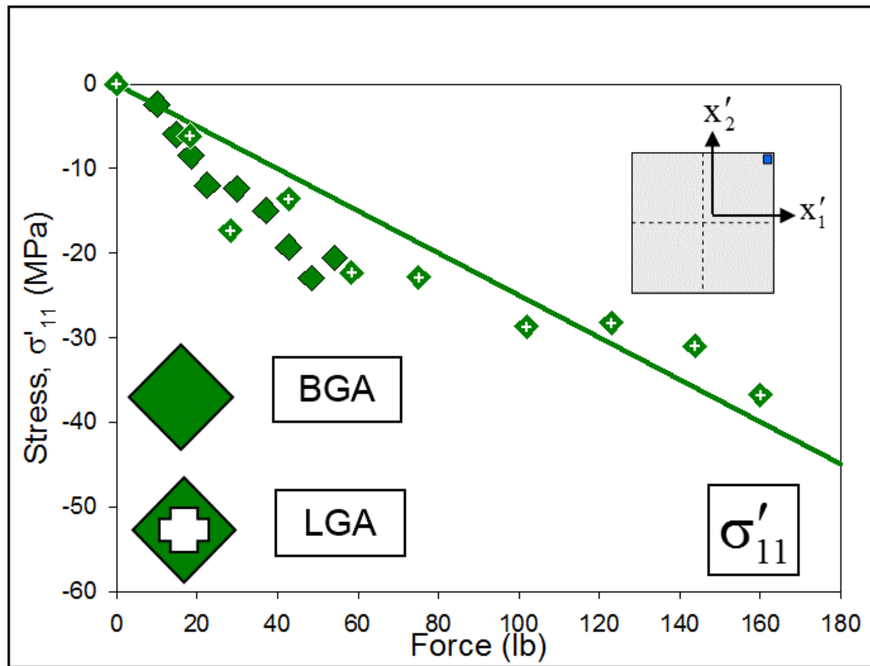


Figure 9.31: Comparison of In-Plane Normal Stress at Die Corner (CBGA vs. CLGA)

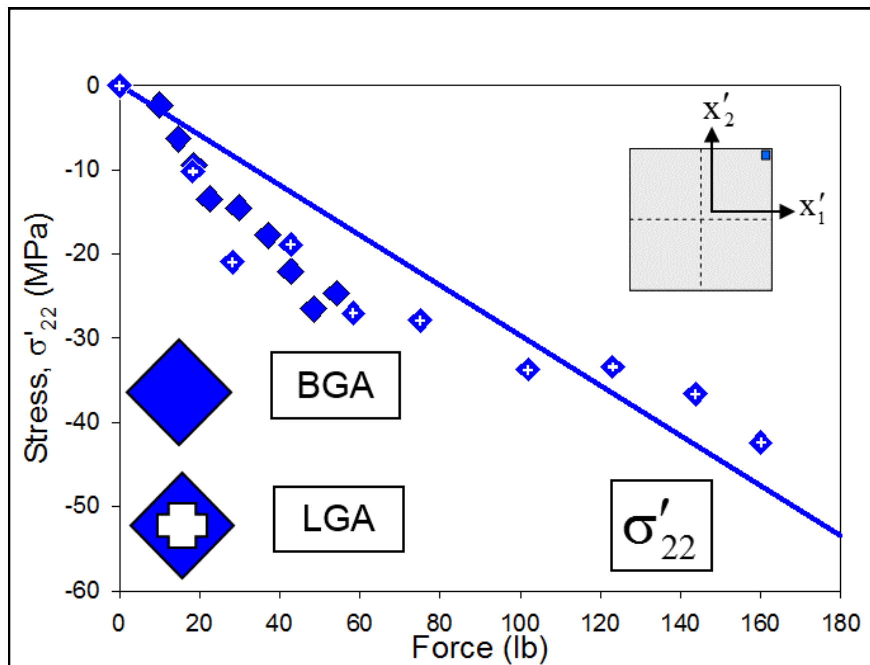


Figure 9.32: Comparison of In-Plane Normal Stress at Die Corner (CBGA vs. CLGA)

9.3 Numerical Simulation of CBGA Die Stresses due to Heat Sink Clamping

To further study the effects of heat sink clamping, finite element analysis was also used to predict the stresses induced by the heat sink clamping forces [183, 184]. The starting point for the CBGA clamping model was the CLGA model for lid attachment shown in Figure 5.35. This model retained the stress history of the previous assembly steps. An increase in temperature was first applied to the model, from 25 °C to 220 °C, to replicate second level solder reflow. CBGA solder balls were then added to the model at the reflow temperature, and then the model was cooled to mimic the reflow profile of the actual assembly. Similarly, the model was next reheated, and the second level underfill material was added. The utilized mesh for the CBGA soldered to the test PCB is shown in Figure 9.33. To closely model the experiments performed using the test fixture in Figure 9.17, the actual distribution of force seen by the heat spreader is critical. Due to the complex geometry, material set, and assembly procedure, most of the materials in the assembly were no longer flat, but exhibited curvature. This is especially true of the heat spreader (lid). To obtain the pressure profile acting on the lid, a thin Mylar-based pressure sensitive film was placed between the lid and the simulated heat sink. When pressure was applied, tiny microcapsules in the film ruptured, changing the color of the film and leaving a topographical image of the pressure distribution between the two surfaces. Figure 9.34 shows the pressure distributions for 200 N, 400 N, 600 N, 800 N, and 1000 N loads applied to the heat spreader.

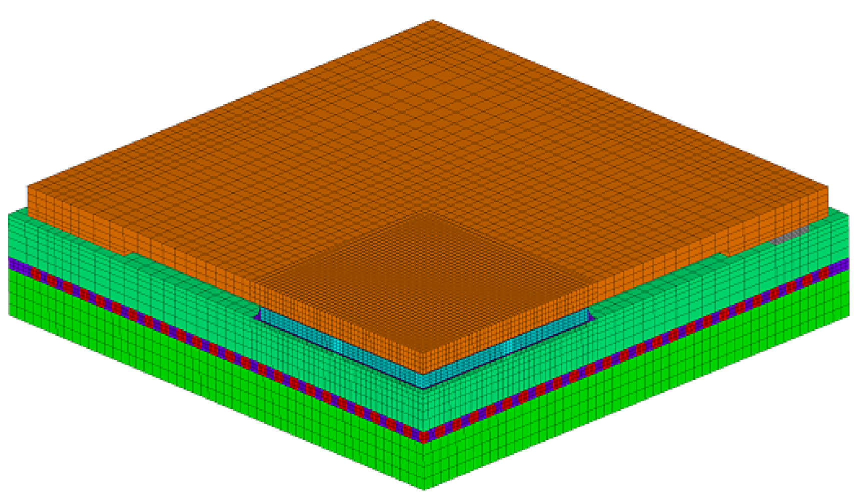
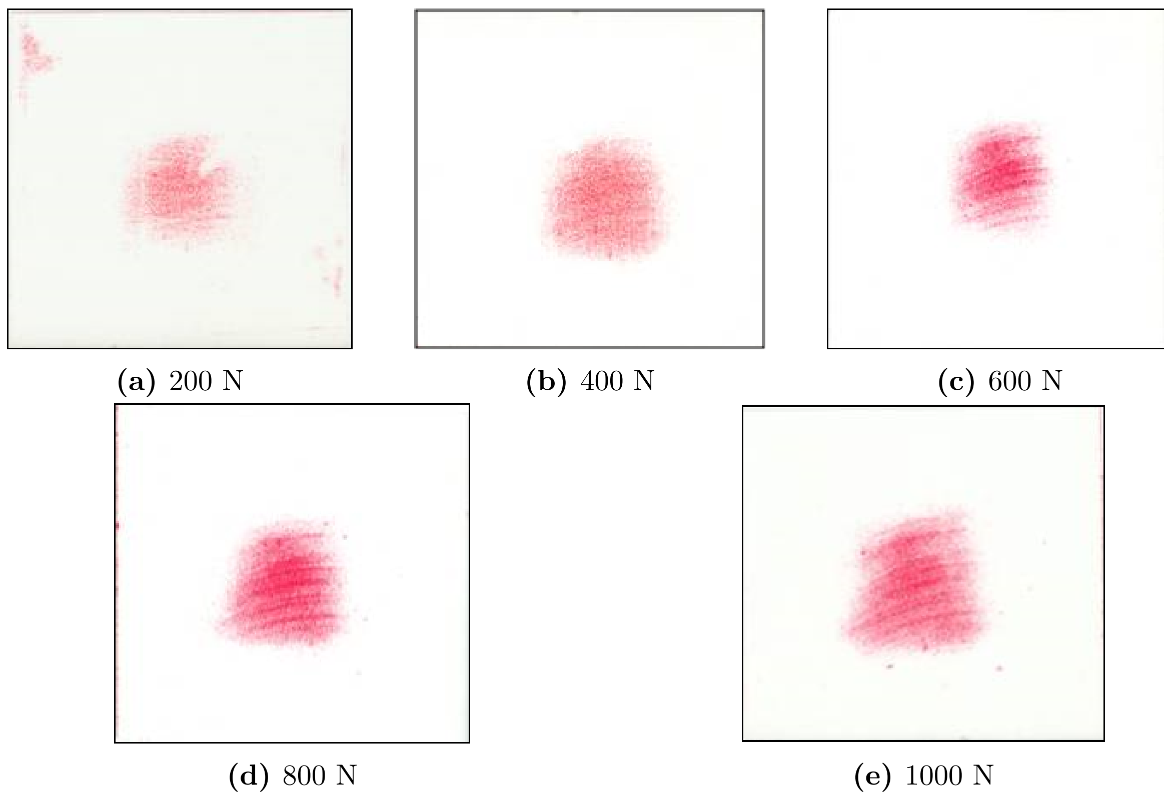


Figure 9.33: Quarter Model of CBGA and Second Level Solder Balls with Underfill



(a) 200 N

(b) 400 N

(c) 600 N

(d) 800 N

(e) 1000 N

Figure 9.34: Pressure Map of Applied Load on Heat Spreader

The pressure maps indicated the largest pressure was at the center of the lid and that the pressure decreased dramatically to very low values at the edges. The pressure maps also indicate the non-symmetric nature of the warpage in the heat spreader. The film was also sensitive enough to detect tooling marks in the simulated heat sink. An idealized pressure distribution was generated for each loading used in testing, and an example is shown in Figure 9.35. A schematic of the idealized loading and the boundary conditions for the clamping FEA model are indicated in Figure 9.36. The materials in the simulations were modeled as elastic except for the solder (Anand viscoplastic model) and underfill (elastic-plastic). More than 1.4 million brick elements made up the final quarter model of the CBGA. A comparison of the experimental measurements (data in Figure 9.20) and finite element predictions for the stress changes at the die center are shown in Figure 9.37. Fairly good agreement was obtained. Both experimental and finite element results are fairly linear, but become nonlinear with higher loads.

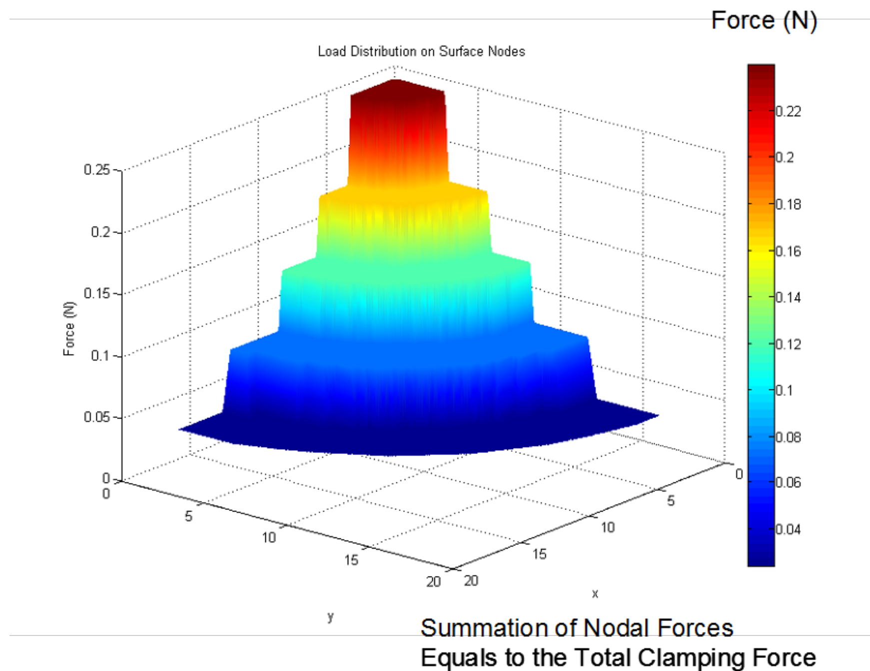


Figure 9.35: Nonuniform Pressure Used in Simulation of Clamping Measurements

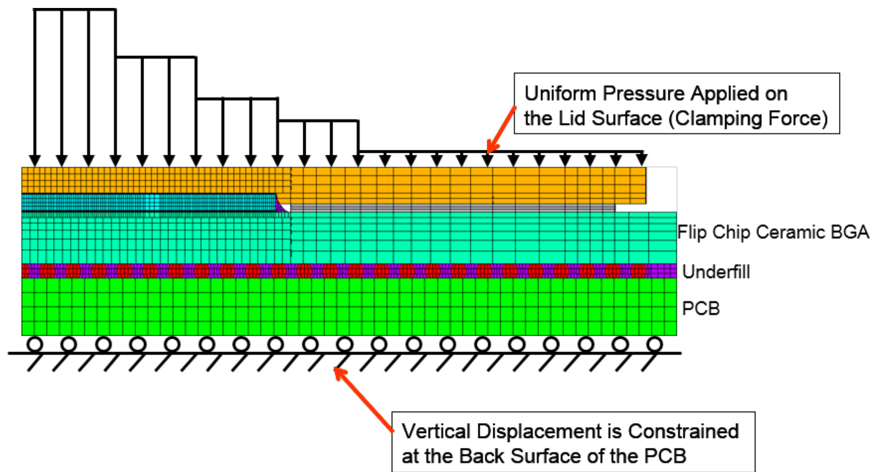


Figure 9.36: Loading and Boundary Conditions for Clamping Finite Element Model

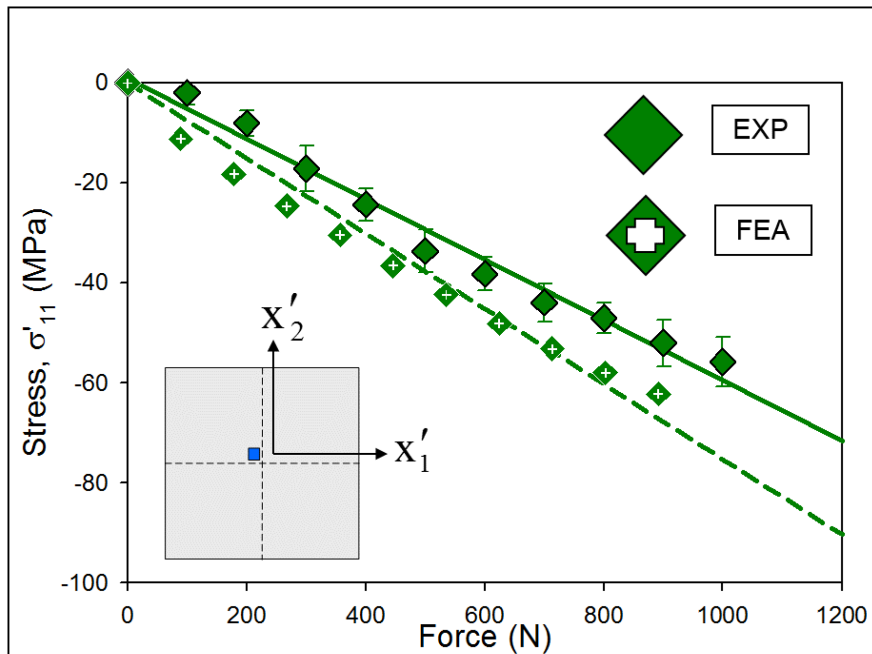


Figure 9.37: Experimental and FEA Results for In-plane Normal Stress σ'_{11} (Die Center)

Chapter 10

Summary and Conclusions

10.1 Summary

In this study, (111) silicon piezoresistive test chips using stress sensor rosettes have been utilized to characterize the device side die stresses in flip chip ceramic ball grid array microprocessor packages during assembly and use. The applied 20 x 20 mm test chips consisted of a full area array of 3600 lead free solder bumps, and were attached to 52 x 52 mm HiCTE ceramic chip carriers. After die attachment, a glass filled epoxy known commonly as underfill was dispense to flow under the die and around the first level solder interconnects. The underfill was cured at high temperatures, and later a first level thermal interface material (TIM1) was applied to the die that also acted as a lid attachment adhesive. To complete the assembly, a second level of larger solder ball interconnects were added and used to mechanically and electrically connect the ceramic substrate to a large 10-layer organic laminate printed circuit board. The resistances of sensor rosettes on the test chips were characterized in their bare state and measured again at room temperature after each successive assembly step.

The assembly consisting of test die, ceramic substrate, underfill, TIM1, and lid, for ease of discussion was considered to be a ceramic land grid array (CLGA), in part due to the use of the lands on the bottom of the ceramic substrate. These lands were used to electrically connect the test chips to a measurement system with the use of a special printed circuit board and CLGA socket. The complete stress state of 40 CLGA packages was characterized after three assembly steps at 36 rosette locations across the die using the computer based data acquisition system. Stress results from non-linear three-dimensional finite element simulations were correlated to the measured stress data after each assembly step. In CLGA

form, stress rosettes were able to measure die stresses as packages were subjected to slow temperature changes, thermal cycling, power dissipation, and power cycling. After the addition of a second level of lead free solder balls to the CLGA componenents, the assembly was then reflowed to a specially designed printed circuit board. The stress effects of second level assembly were also measured. CBGA assemblies were subjected to the same single temperature cycle loading as the CLGA packages, as well as to simulated heat sink clamping.

The experimental observations validated concerns about larger die size when bumped in a full area array. Previous work on perimeter flip chip components showed that even when the die size doubled from 5 x 5 mm to 10 x 10 mm, the stresses induced by solder reflow were negligible. However, results from this study show clearly that large area array flip chips are subjected to large compressive in-plane normal stresses after solder reflow. It was observed that the majority of the die compressive stress is accumulated during the underfilling assembly step. Typical increases in the stress magnitude were on the order of 300% (relative to the stresses due to solder joint reflow only). As a general "rule of thumb", approximately two thirds (≈66%) of the final die stress magnitudes were observed to be developed during the underfill dispense and cure, with the second largest contribution coming from the die attachment (solder reflow), and the smallest contribution coming from lid attachment.

A novel package carrier was developed to allow testing of CLGA packages without inducing additional mechanical stress on the die. Using the carrier and a carefully planned wire-bond stitching technique, the CLGA packages were subjected to slow, quasi-static changes in temperature over a range of 0 to 100 °C in a thermal chamber. Resistances selected sensor rosettes were measured as a function of temperature, and stress values were extracted from the measurements. The CLGA finite element model was also subjected to the same thermal range, and was able to predict stresses over the entire test range. Results from the finite element simulations were compared to results from measured sensors.

It was observed that the stress components at most locations on the chip varied linearly with the temperature. However, at the die corners the responses for all stress components became non-linear for temperatures near the upper extreme of T = 100 °C. In addition, the stress variations showed hysteresis. These effects are due to inelastic deformations occurring in the underfill material in the corner regions where the highest shear stresses exist. Good correlation was found with finite element simulations in all cases.

A subset of 18 CLGA packages were also subjected to long term thermal cycling from 0 to 100 °C using a 40 minute cycle. Packages were removed from the thermal cycling chamber at regular intervals, with stress sensor measurements made at room temperature. In total 9000 thermal cyclines were recorded. An anomaly in stress data was caused by wear in the socket used to measure the assemblies at room temperature. The worn socket was replaced and the results of measurements made with a new socket were confirmed by manual probing of the packages. Using the stress free package carrier discussed above, CLGA packages were measured *in-situ* during thermal cycling. Die stresses were able to be correlated with temperature changes affecting the assembly. Good correlation was also found between the measured thermal cycling data and a finite element simulation of extended thermal cycling.

It was noted that during the initial thermal cycles, that the stress jumped from initial measurements, but settled to a near constant trend by 250 cycles. Other than stresses measured using a worn test socket, rosettes across the die showed little fluctuation due to thermal cycling when measured at room temperature. A small subset of the 18 samples showed variation in the last two measurement periods, but non-destructive methods were unable to determine the cause of the variation. Data taken on thermally cycled parts in-situ show cycle to cycle variations in die stress that correlate to the affecting temperature. In-situ measurements also recorded shifts in stress values during early cycles.

Using the developed package carrier used in the quasi-static and thermal cycling experiments, rosettes of test die in selected CLGA packages were calibrated as temperature sensors. This allowed for a more direct measurement of die surface temperature than employing lid

mounted thermocouples or infrared thermography. The buried layer heater in the test die was used to dissipate various power levels in the CLGA packages. Sensor rosettes were measured during power dissipation and transient temperature measurements were taken for several power levels. Finally, the buried layer heater was used to introduce a two Watt power cycle in the CLGA packages. Transient measurements were again recorded using the sensor rosettes.

Power levels from one-tenth to two Watts were dissipated in CLGA packages, with peak die temperatures reaching approximately 60 to 70 °C. On-die steady state temperature shows a linear correlation with power dissipation. A 2-Watt on-off power cycle was used to study the transient behavior of the packages. Die temperature measurements exhibited a sawtooth-like behavior, with stress values coinciding with temperatures.

Additionally, a process was developed to assemble the CLGA packages to a large 10-layer laminate printed circuit board. After addition of second level solder ball interconnects the assemblies were considered ceramic ball grid array (CBGA) packages. Assembly processes were discussed including solder paste printing, package alignment and attachment, and final reflow. Assembled CBGA packages were visually inspected and cross-sectioned to determine the quality of assembly. Rosette measurements were taken after second level assembly. Assembled CBGA packages were also subject to quasi-static thermal exposure.

Finally, several CBGA assemblied were constructed with the addition of a second level underfill. These assemblies were used to measure the die stress response to heat sink clamping. In field use, clamping of heat sinks are necessary to ensure good thermal performance. However, the forces applied to the lid of typical microprocessor components transmits directly to the die and may affect performance. Several measurement techniques were used to quantify the force applied to CBGA components including bolt torque, a resistive force sensor, and a button load cell. Pressure sensitive film was used to determine the distribution of force on the lid of the assemblies. The finite element model used earlier in the study was

extended to simulate the effects of heat sink clamping, and stress results were correlated to test chip measurements.

Loads ranging from 200 to 1000N were applied using a special simulated heat sink clamping fixture. Normal die stress values at the center of the die were found to be affected most by clamping, showing a linear response throughout the range of loads. Finite element simulations were in close agreement over the entire range of loads. Measurements were also taken on CLGA assemblies with a socket forming interconnects with a test board and compared to CBGA tests. It was found that while less stress acts on the die at a given force, more force is needed to make sufficient electrical connection to a test board.

10.2 Conclusions

- Device side die stresses in large area array flip chip die with lead free solder balls are much larger than stresses previously seen in smaller flip chip packages. Thus, chip and package engineers must take these higher loads into consideration when designing flip chip microprocessor packages.

- Strong gradients exist at each solder ball in the device side stress distributions in lead free flip chip packaging after solder reflow. Thus, on-chip sensors must be extremely small to fully resolve stress distributions between and near solder balls.

- The underfill cure cycle creates the largest changes in stress during the assembly. Thus, the choice of underfill and cure profile are very important to designers of flip chip packaging.

- Good correlations between finite element predictions and experimental data were obtained when the model input data included well characterized material behavior, and when the experimental data were averaged over several samples to smooth out manufacturing variations. Correlations are more qualitative when simulation results are compared to data from a single assembly.

- Die stresses in HiTCE ceramic packaging due to long term thermal cycling were extremely stable from cycle to cycle. Thus, HiTCE ceramic microprocessor packages are resistant to environmental exposures.

- Stress changes during thermal cycling exhibited hysteresis near corners of the die due to plasticity of the underfill encapsulant. Thus, the the die corners are likely locations for failures due to underfill delamination and solder joint cracking.

- Maximum values of die compressive stress changes due to heat sink clamping were found to be approximately 25% of the total stress due to component assembly. Thus, the die stresses produced by heat sink clamping cannot be neglected and must be considered in the design of microprocessor packages.

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Appendices

Appendix A

Calculation of Die Stresses using Alternative Stress-Free Reference States

This study, along with previous test chip studies have detailed absolute die stresses after packaging steps and when subjected to environmental conditions such as thermal cycling. Absolute stress results are useful as they allow direct comparison to material failure criteria among other positive attributes. However, considering bare die as a reference, stress free, state for future stress measurements requires probing at the bare die state which is time consuming, labor intensive, and may delay critical testing.

Consider the following equation for in plane normal stress using the previously described (111) silicon test chips.

$$\sigma'_{11} = \frac{(B_3^p - B_2^p)\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right] - (B_3^n - B_2^n)\left[\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right]}{2\left[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n\right]} + \frac{B_3^p\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^n T\right] - B_3^n\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^p T\right]}{2\left[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n\right]} \tag{A.1}$$

The $\frac{\Delta R_1}{R_1}$ term found here may be considered as:

$$\frac{\Delta R_1}{R_1} = \frac{R_{\text{current state}} - R_{\text{initial state}}}{R_{\text{initial state}}} \tag{A.2}$$

where R is the resistance of a sensor in the rosette.

The assembly stresses of the CLGA packages used in this study will by used as an example. Figure (A.1) shows measured normal stresses due to assembly at the center of the die.

As noted earlier, stress values increased with each step of package assembly. To determine the stress change, or additional stress, added by the underfill cure process, the stress

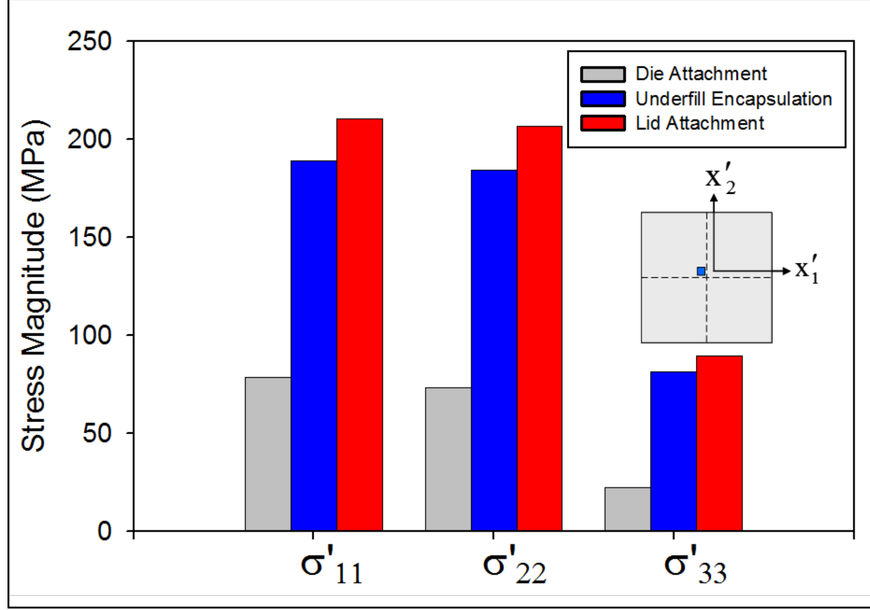

Figure A.1: Normal Stresses Due to Assembly at Die Center

value measured for the packages with die attachment only are subtracted from the values measured of packages at the underfilled stage. Representing this mathematically,

$$\Delta\sigma_{UF} = \sigma_{UF} - \sigma_{DA} \tag{A.3}$$

where subscript UF is representative of packages in the underfilled stage, and subscript DA is representative of packages in the die attached stage. Table (A.1) shows calculations of the stress change due to underfill at the center of the die by the method of subtraction for one CLGA package.

Table A.1: Stress Change Due to Underfill (Subtraction Method)

Stress Component	σ_{UF}	σ_{DA}	$\Delta\sigma_{UF}$
σ'_{11}	-187.7	-84.9	-102.8
σ'_{22}	-168.0	-60.6	-107.4
σ'_{33}	-106.8	-34.3	-72.6

An alternative method to stress change calculation is to consider an intermediate state as the reference, stress-free state. In this example, the intermediate state considered to be

stress-free is the die attached package stage. Rosette resistances at the die attached stage of assembly are considered as the initial state and resistances of die sensors at the underfilled stage of assembly are considered the current state. Using the alternative reference state calculation method, the normal stresses for the same package at the same rosette location are shown in Table (A.2).

Table A.2: Stress Change Due to Underfill (Alternate Reference Method)

Stress Component	$\Delta\sigma_{UF}$
σ'_{11}	-102.4
σ'_{22}	-107.0
σ'_{33}	-72.3

Similar calculations can also be performed for the stress change due to lid attachment. In the subtraction method, the stress at the lid attach stage of assembly is subtracted from the stress values at the lid attached stage of assembly. Results of the subtraction method to determine stress change due to lid attachment are shown in Table (A.3). Table (A.4) shows the results of stress calculations using the sensor rosette resistances at the underfilled stage of assembly as the initial state and rosette resistances at the lid attachment stage of assembly as the current state.

Table A.3: Stress Change Due to Lid Attachment (Subtraction Method)

Stress Component	σ_{Lid}	σ_{UF}	$\Delta\sigma_{Lid}$
σ'_{11}	-206.4	-187.7	-18.7
σ'_{22}	-186.4	-168.0	-18.4
σ'_{33}	-106.6	-106.8	0.2

A final pair of stress change calculations can be made from measured CLGA packages. The stress change due to both underfill cure and lid attachment can also be calculated using both methods discussed here. Table (A.5) shows the normal stresses at the center of the die due to underfill dispense and lid attachment for a single package calculated using the

Table A.4: Stress Change Due to Lid Attachment (Alternate Reference Method)

Stress Component	$\Delta\sigma_{Lid}$
σ'_{11}	-18.3
σ'_{22}	-18.1
σ'_{33}	-0.6

subtraction method. Table (A.6) shows the normal stresses at the center of the die due to underfill dispense and lid attachment for a single package calculated using the alternate reference method.

Table A.5: Stress Change Due to Underfill Cure & Lid Attachment (Subtraction Method)

Stress Component	σ_{Lid}	σ_{DA}	$\Delta\sigma_{UF+Lid}$
σ'_{11}	-206.4	-84.9	-121.5
σ'_{22}	-186.4	-60.6	-125.8
σ'_{33}	-106.6	-34.3	-72.3

Table A.6: Stress Change Due to Underfill Cure & Lid Attachment (Alternate Reference Method)

Stress Component	$\Delta\sigma_{UF+Lid}$
σ'_{11}	-120.8
σ'_{22}	-125.1
σ'_{33}	-71.8

A method to calculate stress changes has been demonstrated and validated with the method of superposition. The alternative reference method allows calculation of die stress changes without knowing the initial resistances of bare die. It is noted that the calculations only relate stress changes and should not be used as an indicator of absolute stress values. It is valuable for making comparisons between stresses induced by successive assembly steps or between any two states of loading that may affect die stress.