AN ACCURATE CMOS FOUR-QUADRANT ANALOG MULTIPLIER

Except where reference is made to the work of others, the work described in this thesis is my own or was done in collaboration with my advisory committee. This thesis does not include proprietary or classified information.

_____

Ramraj Gottiparthy

Certificate of Approval:

_____	_____
Richard C. Jaeger Distinguished University Professor Electrical and Computer Engineering	Bogdan M. Wilamowski, Chair Professor Electrical and Computer Engineering
_____	_____
Fa Foster Dai Associate Professor Electrical and Computer Engineering	Stephen L. McFarland Dean Graduate School

AN ACCURATE CMOS FOUR-QUADRANT ANALOG MULTIPLIER

Ramraj Gottiparthy

A Thesis

Submitted to

the Graduate Faculty of

Auburn University

in Partial Fulfillment of the

Requirements for the

Degree of

Master of Science

Auburn, Alabama
May 11, 2006

AN ACCURATE CMOS FOUR-QUADRANT ANALOG MULTIPLIER

Ramraj Gottiparthy

_____
Signature of Author

_____
Date of Graduation

VITA

Ramraj Gottiparthy, son of Rajaiah G, and Bharathi G, was born on May 29, 1981 in Hanamkonda, India. After finishing high school from Nalanda Jr. College in 1998, he attended National Institute of Technology Warangal, India where he received his Bachelor of Technology (Electrical and Electronics) degree in 2002. He entered graduate school at Auburn University in Fall of 2003 as a graduate research assistant, and later went on to accept a fellowship through Auburn University.

THESIS ABSTRACT

AN ACCURATE CMOS FOUR-QUADRANT ANALOG MULTIPLIER

Ramraj Gottiparthy

Master of Science, May 11, 2006
(B. Tech., National Institute of Technology Warangal, 2002)

63 Typed Pages

Directed by Bogdan M Wilamowski

Analog multipliers are used in communication circuits, neural networks as well as frequency doublers, RMS circuits and phase detectors. High linearity is the prime issue for multipliers in conventional applications like modulation circuits. Power consumption is the criteria in case of massive parallel processing based neural networks. This thesis details the design process of four-quadrant multiplier designed using AMIS C5F CMOS process which could able to address the challenges mentioned above. Initially, different multiplier architectures are reviewed. A MOS resistor based multiplier and divider circuits are designed and simulated. Eliminating the limitations of this configuration, final four-quadrant multiplier is designed. In addition to these, input signal range, bandwidth, mismatching of transistors and active area of the chip are also optimized.

The final design of multiplier has ±2.2V input range, 73MHz bandwidth, 0.242mW power consumption with 10μA bias current and -63db total harmonic distortion at 100 KHz 1Vp-p input signal. Special layout techniques like interdigitation and common centriod methods are used to reduce mismatches between transistors and effects of process variations are minimized.

ACKNOWLEDGEMENTS

My deepest respect and appreciation goes to my advisor, Dr. Bogdan M. Wilamowski for his guidance, support and encouragement provided in my journey towards the Master's Degree in Engineering. I will forever be grateful for his endless advice, incredible patience, generosity and friendship. I am also grateful to my committee members Dr.Richard C. Jaeger and Dr. Fa Foster Dai for their guidance and support. I take the opportunity to thank Mr. Charles Ellis for his support and help.

I would like to thank my father and mother, my sister Sandhya Rani and my brother Rajkumar for their enduring love, immense moral support and encouragement throughout my life.

Style manual of journal used Graduate School: Guide to preparation and submission of theses and dissertations

Computer software used Microsoft Office XP

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1 INTRODUCTION

1.1 Motivation

Out surrounding world is analog in nature. Digital systems require analog to digital conversion at the front of the system and digital to analog conversion at its end. Analog computation and signal processing makes it simpler and faster [1]. Analog signal processing represents the signals as physical quantities like e.g. charge, current, voltage or frequency. These signals are continuous in value and continuous in time. Analog signal processing is most effective when precision is not the major criteria and when massive parallel collective processing of large number of signals that are continuous in time and amplitude is required [2]. Multiplication and division of analog signals are difficult operations in analog signal processing.

Analog multipliers and dividers are used in communication circuits as well as in neural networks and fuzzy logic applications. Phase detector, adaptive filter, function generators, frequency doubling and amplitude modulation are some applications of analog multipliers in communications industry. Voltage gain amplifier, signal squarer, RMS signal estimator and weight-input multiplication in neural networks are some application in signal processing. Phase detector is an essential element in phase locked loops. PLLs are widely used in frequency synthesizers, demodulators, clock generation circuits, clock recovery circuits and spread spectrum PLLs. Analog multipliers as part of automatic gain control circuits used in AM radio receivers and radar systems.

Communication systems, low power portable applications and low power massive signal processing circuits like neural and fuzzy logic circuits have lot of demand in this century. Low power and high performance hardware implementation of these circuits is a challenging task. In addition to these, the cost of circuits must be lowered as well. All these challenges of analog multiplier and divider circuits are addressed in this thesis.

1.2 Architecture of Phase locked loop and neural network

Phased locked loop is a universal building block used in both analog and digital applications. The basic structure of Phase locked loop is shown in the Figure 1.1. Phase detector finds the phase difference between input and output signals of the controlled oscillator and locks the PLL on zero phase difference. Analog multiplier is most widely used as phase detector in PLLs with sine wave inputs and sine wave outputs [3]. Multiplier with two inputs having a phase difference of ϕ (inputs $v_x \sin \omega t$ and $v_y \sin(\omega t + \phi)$) gives output v_{out}.

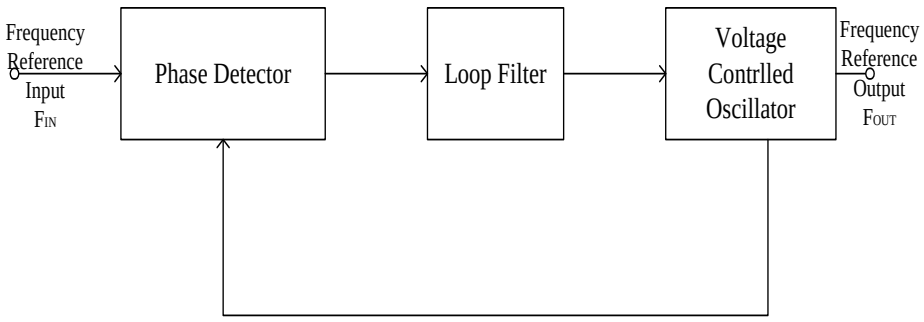


Figure 1.1 Block diagram of phased locked loop

$$v_{out} = v_x v_y / 2\{cos\phi - cos(2\omega t + \phi)\} \qquad [1.1]$$

The output of multiplier has DC term and double frequency term. Either by filtering the output or taking average of the output gives phase detection or phase error of the input signals.

Analog VLSI implementation of artificial neural networks represents one of approaches to enhance the computational capabilities in real-time information processing. Character recognition, retrieval of data/image from fragments, pattern recognition and speech synthesis are some applications of artificial neural networks [4]. These neural networks consist of massive parallel layers of neurons interconnected with synapses as shown in Figure 1.2. The main function of the synapse cell is to achieve linear multiplication of input and a weight. These synaptic connections are implemented using Analog multipliers. Applications like multi layer feed forward networks require large number of interconnected neurons and synaptic connections (multipliers). Therefore careful design of multiplier is crucial in achieving compact silicon area, minimizing power consumption and improving input range.

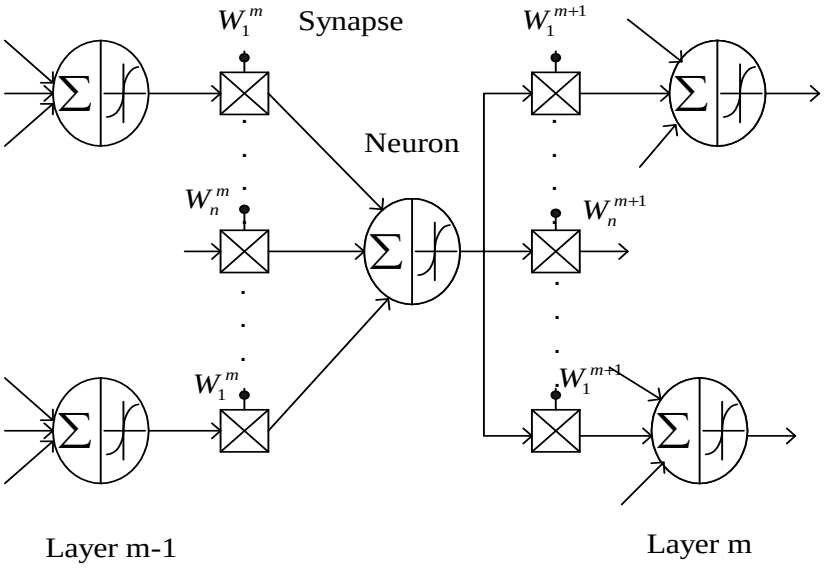


Figure 1.2 Architecture of Neural Network [5]

1.3 Research Goal

Our goal is to design CMOS analog multiplier and dividers with profound application to frequency doublers, phase locked loops, neural and fuzzy networks. Most of CMOS implementation of analog neural networks uses sub-threshold characteristics of MOS operation. Sub-threshold region of operation gives very limited range of operation (-100mV<VIN<100mV) [5]. Since this design implements MOS multiplier operation in saturation region of MOS, operating range (-2V<VIN<2V) of multiplier is extended. This thesis pays special attention in improving design characteristics like input range, linearity and power consumption of multiplier and divider circuits.

In addition to wide input range the most important characteristic of multiplier/divider design is linearity. The linearity of the multiplier/divider is estimated in terms of either percentage of distortion in DC transfer characteristics or Total harmonic distortion (THD) of multiplier/divider. A THD of less than 2% in the region of operation is sufficient for many analog VLSI signal and information processing applications [6]. The innovative design of differential multiplier is source degeneration by means of MOS controllable resistor in differential pair. This design can achieve THD of 1% for 1V@1MHz input signal.

Low supply voltage is directly translated to lower power consumption in digital circuits. Similar conclusions cannot necessarily be drawn for analog circuits. Therefore low power analog design raises its own challenges. Low supply voltages, low bias currents, low effective threshold voltages of MOS transistors are some methods to reduce power consumption in multiplier and divider architectures. Low bias currents and less number transistors in this design leads to reduced power consumption compared to bias

currents in other multiplier architectures (Ib = 600μA) [7]. The multiplier and divider circuits' layout is done in AMIS C5F 0.5μm CMOS technology. The design, analysis and simulation results are provided in this thesis.

1.4 Thesis outline

This thesis is organized such that first it provides an insight into different multiplier, divider and MOS resistor architectures and then discusses specifics of different design methods, simulation results and layout considerations. Chapter 2 presents background of multiplier/divider circuits with the help of different multiplier architectures. The principle of operation of these multipliers is based on MOS operating region. Different MOS resistor and divider circuits are also presented in this chapter.

Chapter 3 concentrates on MOS resistor implementation. This building block is used to design MOS multiplier and divider circuit. Frequency responses as well as Total harmonic distortion of this MOS resistor based multiplier circuit simulation results are presented.

Chapter 4 will discuss design method to improve the characteristics of four quadrant multiplier. In this chapter the proposed differential multiplier architecture design is analyzed by means of small signal analysis. Chapter 4 also presents simulation results of four quadrant multiplier illustrating its characteristics and its applications.

Chapter 5 is mainly presenting analog layout methods used in multiplier, current subtraction circuit and load resistor. Finally, conclusions about my research work are presented in Chapter 6.

CHAPTER 2 BACKGROUND

2.1 Introduction

Analog circuits are designed to implement some of mathematical operations. Addition, subtraction, integration and differentiation are some of the simple operations compared to multiplication and division of analog signals. If both the inputs of multiplier/divider can be either positive or negative, then it is called as four-quadrant multiplier/divider circuit. The inputs and outputs can be either voltage or current.

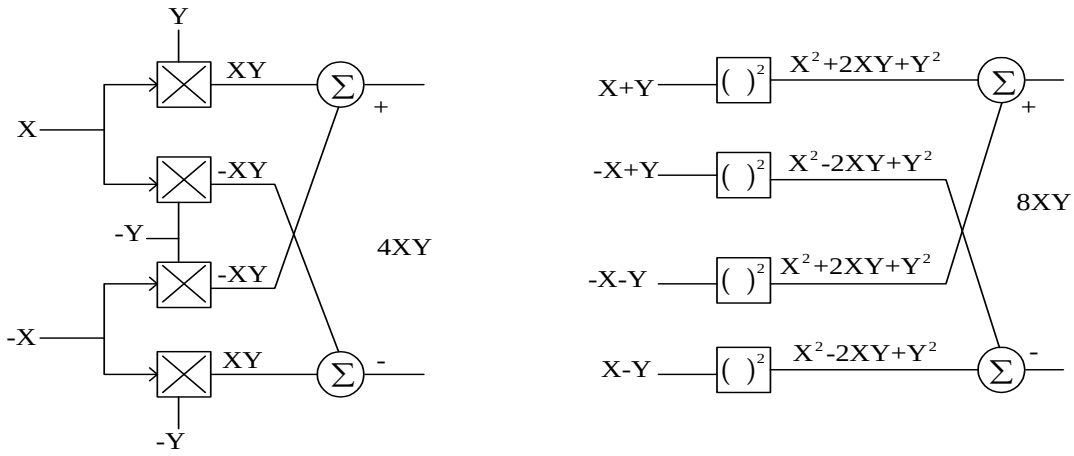


Figure 2.1 Nonlinearity cancellations in four quadrant multiplier (a) using four single quadrant multipliers (b) using square devices

The ideal output of multiplier/divider is related to its inputs by

$$V_{out} = K.V_x.V_y \qquad [2.1]$$

$$V_{out} = K.(V_x / V_y) \qquad [2.2]$$

K is the multiplier/divider gain and V_x,V_y are voltage inputs of multiplier/divider circuits. In reality, the nonlinear characteristics of transistors results in offsets and nonlinearities. Non ideal output of multiplier can be written as [8]

$$V_{out} = K(V_x + V_{osx})(V_y + V_{osy}) + V_{osout} + V_x^n + V_y^m \qquad [2.3]$$

$V_{osx}, V_{osy}, V_{osout}$ are the offset voltages and V_x^m, V_y^n represent nonlinearities in the multiplier [9]. These nonlinearities in four-quadrant multipliers are cancelled by using four single quadrant multipliers or four squared devices as shown in the Figure 2.1.

Barrie Gilbert designed one of successful four-quadrant multiplier in 1968 using the characteristics of bipolar transistor [10]. From Gilbert BJT multiplier to recently designed MOS transconductors based multipliers different topologies of multipliers are proposed. Multipliers are classified based on its MOS region of operation [11]. One type is analog multiplier circuit based on square-law characteristics of MOS transistor and the other type is based on linear characteristics of MOS transistor. Most of these transconductance multipliers are further categorized based on type of non linearity cancellation methods used in each multiplier. In transconductance multipliers, non linearities are cancelled either by single quadrant multipliers or squared devices as shown in Figure 2.1. In addition to these methods, current mode operation of multipliers is introduced.

Low voltage, low power, wide input range and linearity are the basic criteria in designing multipliers. CMOS multipliers are most widely used compared to BJT multipliers because CMOS multiplier gives low power and low voltage capabilities than BJT based multiplier. CMOS designs give low fabrication cost because of much widely used cmos digital technology.

2.2 Multiplier Classification

2.2.1 BJT Gilbert multiplier

Gilbert multiplier using emitter-coupled differential pairs is shown in the Figure 2.2. The dc transfer characteristics of emitter-coupled pair exhibit tangential hyperbolic nature. This characteristic of emitter-coupled pair is used for implementation of Gilbert multiplier. The collector currents of emitter-coupled pairs Q3, Q4 and Q5, Q6 are given as

$$I_{c3} = \frac{I_{c1}}{1+\exp\left(-\frac{V_1}{V_T}\right)} \quad [2.4]$$

$$I_{c4} = \frac{I_{c1}}{1+\exp\left(\frac{V_1}{V_T}\right)} \quad [2.5]$$

$$I_{c5} = \frac{I_{c2}}{1+\exp\left(\frac{V_1}{V_T}\right)} \quad [2.6]$$

$$I_{c6} = \frac{I_{c2}}{1+\exp\left(-\frac{V_1}{V_T}\right)} \quad [2.7]$$

The collector currents of bottom emitter-coupled pair Q1, Q2 are given as

$$I_{c1} = \frac{I_{EE}}{1+\exp\left(-\frac{V_2}{V_T}\right)} \quad [2.8]$$

$$I_{c2} = \frac{I_{EE}}{1+\exp\left(\frac{V_1}{V_T}\right)} \quad [2.9]$$

The differential output current is given as

$$I_{out} = I_{c3-5} - I_{c4-6} \qquad [2.10]$$

The differential output current is product of e hyperbolic tangent of the two input voltages.

$$I_{out} = I_{EE}\left[\tanh(V_1 / 2V_t)\right]\left[\tanh(V_2 / 2V_t)\right] \qquad [2.11]$$

For small values of x (x<<1) $\tanh x \approx x$, therefore equation (2.11) reduces to

$$I_{out} = \frac{I_{EE}}{4V_T^2} * V_1 * V_2 \qquad V_1, V_2 << V_T \qquad [2.12]$$

Where V_T is thermal voltage with a value of 26mV at 300^o K.

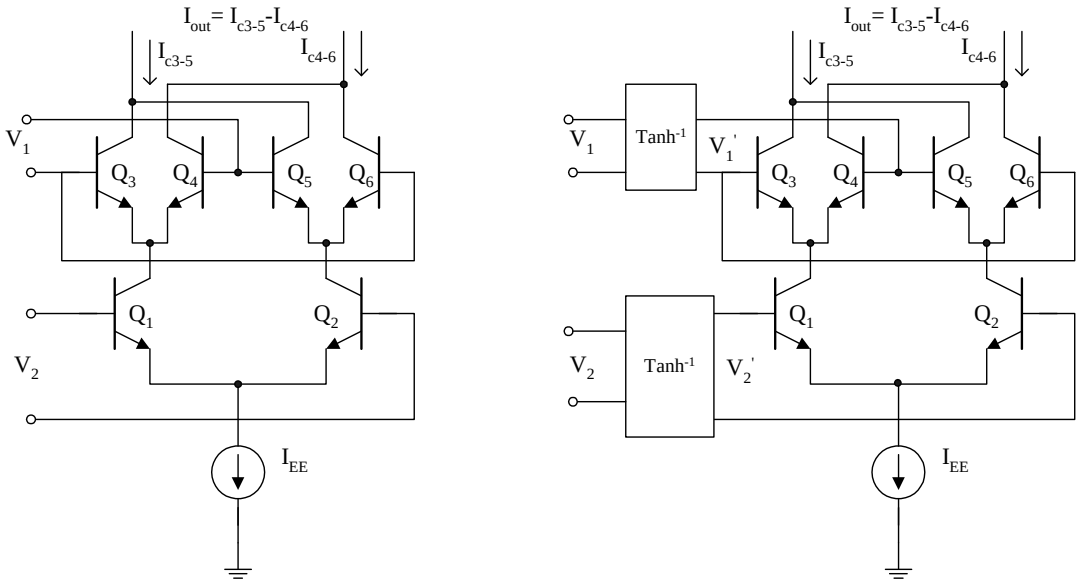


Figure 2.2 (a) BJT Gilbert multiplier (b) Gilbert multiplier with predistortion circuit [12]

Multiplication of input signals is obtained by keeping the magnitude of input voltages (V_1 and V_2) small relative to V_t (Thermal voltage). This multiplier limits the input signal range to few tens of mill volts. In order to extend range of one of the input signals more

than V_t, emitter degeneration is used in lower emitter-coupled pair. But this method cannot be used for cross coupled BJT pairs. As shown in Figure 2.2 (b) an inverse hyperbolic tangent transfer characteristic circuit compensates nonlinearity in the BJT multiplier. This inverse hyperbolic tangent pre-distortion circuit before input voltages eliminates restriction on input voltage ranges. Input voltages are still limited by voltage-current conversion capability of pre-distortion circuits.

2.2.2 MOS multiplier operating in voltage saturation region

A simple multiplier configuration using four cross connected MOS transistors is shown in the Figure 2.3. All the four transistors M1-M4 operate in triode region.

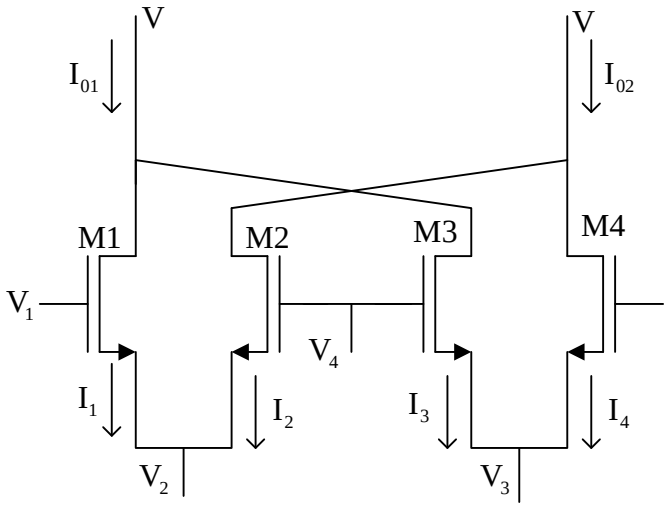


Figure 2.3 MOS multiplier with transistors M1-M4 operating in triode region

For a NMOS transistor operating in triode region, the drain current (I) is

$$I = K[V_{GS} - V_T - V_{DS}/2]V_{DS} \qquad [2.13]$$

Where K is NMOS transconductance parameter

$$I_1 = K[V_1 - V_2 - V_T - (V - V_2)/2](V - V_2) \qquad [2.14]$$

$$I_2 = K[V_4 - V_2 - V_T - (V - V_2)](V - V_2) \qquad [2.15]$$

$$I_3 = K[V_4 - V_3 - V_T - (V - V_3)/2](V - V_3) \quad [2.16]$$

$$I_4 = K[V_1 - V_3 - V_T - (V - V_3)/2](V - V_3) \quad [2.17]$$

Output current I_0 of multiplier is given by

$$I_0 = I_{01} - I_{02} = (I_1 + I_3) - (I_2 + I_4) \quad [2.18]$$

$$I_0 = K[(V_1 - V_4)(V_2 - V_3)] \quad [2.19]$$

These triode region multipliers are insensitive to the distributed effects in the channel, and that the four-transistor circuit itself possesses inherent compensation to such effects [13]. Because of better nonlinearity cancellation methods in this fully differential configuration, linearity and power supply rejection ratio (PSRR) are improved. But the inherent limitation of these multipliers is that all the drain voltages of MOS transistors must be same, to achieve nonlinearity cancellation. An operational amplifier in the output can keep the drain voltages constant.

2.2.3 MOS multiplier operating in current saturation region

The topology shown in Fig. 2.3 can also be used as if all the transistors work in current saturation region. The operating current (I) of a saturated NMOS transistor is given as

$$I = \frac{K}{2}[V_{GS} - V_T]^2 \quad [2.20]$$

The drain currents of transistorsM1-M4 are

$$I_1 = \frac{K}{2}[V_1 - V_2 - V_T]^2 \quad [2.21]$$

$$I_2 = \frac{K}{2}[V_4 - V_2 - V_T]^2 \quad [2.22]$$

$$I_3 = \frac{K}{2}[V_4 - V_3 - V_T]^2 \quad [2.24]$$

$$I_4 = \frac{K}{2}[V_1 - V_3 - V_T]^2 \quad [2.24]$$

Output current I_0 of multiplier is given by

$$I_0 = I_{01} - I_{02} = (I_1 + I_3) - (I_2 + I_4) \quad [2.25]$$

$$I_0 = K[(V_1 - V_4)(V_2 - V_3)] \quad [2.26]$$

It is important to note that, the drain current of MOS transistor operating in saturation region is not controlled by drain voltage. Therefore drain voltages needn't be equal for this multiplier configuration. Note that the above analysis neglects both channel length modulation (λ) and mobility reduction (θ). Moreover multipliers operating in saturation region have much higher frequency response than multiplier operating in triode region [14]. Number of practical multiplier topologies is more in case of saturation region multipliers [11].

2.2.4 MOS multiplier working in weak inversion region

Battery powered portable applications like Neuromorphic VLSI chips require low power analog signal processing. MOS multiplier working in sub threshold region has the advantage that the current levels are typically orders of magnitude lower than devices biased above threshold. This allows low power (1μW) dissipation [15]. Input signal linear range (±2V) can be extended by source degeneration, gate degeneration and bump linearization. In these multipliers transconductance is directly proportional to the drain

current. Because of highly nonlinear exponential characteristics in sub threshold region, THD is more than acceptable value (3% THD). The extremely low values of bias currents ($I_{bias} = 80nA$) limit the bandwidth (-3dB bandwidth of 10 KHz) of the multiplier. These multipliers are not suitable for high frequency applications [15]. The current mode implementation of multiplier/divider with sub-threshold region operated MOS transistors improves accuracy [16].

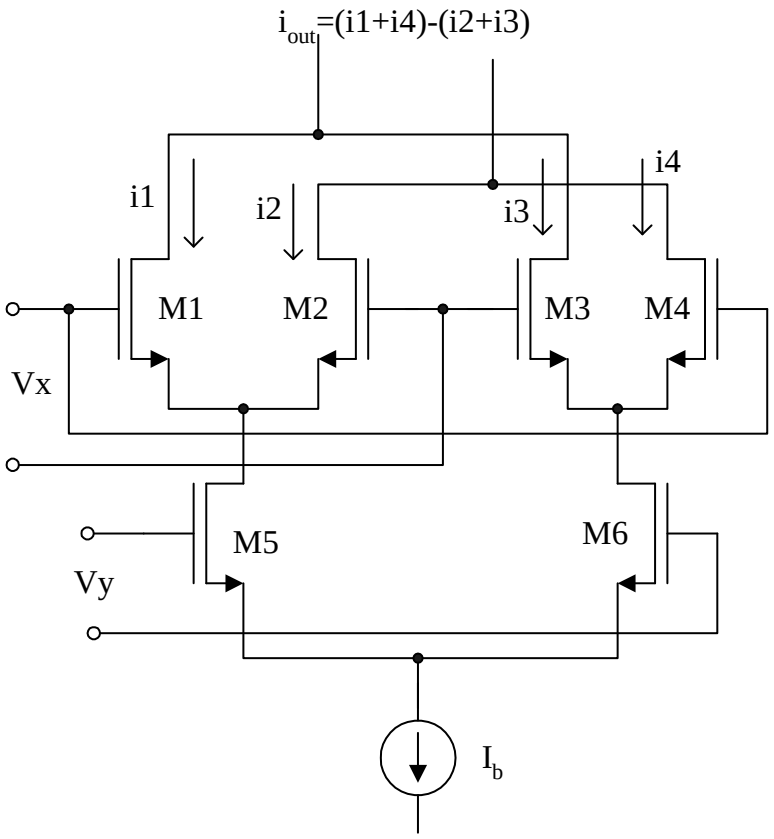


Figure 2.4 MOS version of Gilbert multiplier working in weak inversion region

As shown in Figure 2.4, the exponential characteristics of MOS transistor are used to implement MOS version of Gilbert multiplier. Further power consumption is reduced by using four transistors instead of six transistors in usual stacked differential pair configuration [17].

2.2.5 MOS multiplier based on translinear principle

A translinear circuit should have inputs and outputs in the form of currents and no voltages other than the junction voltages are involved [18]. Initial translinear (TL) circuits used exponential current-voltage characteristics of bipolar transistors. MOS translinear (MTL) circuits are designed using exponential I-V characteristics in sub-threshold region. But dynamic range and speed of operation of such circuits are limited due to MOS transistors operating in weak inversion. The widely used MTL circuits are based on linear relationship between transconductance and voltage [19]. Compared to BTL circuits MTL circuits have less current range, bounded at low end by weak inversion and at high end by mobility reduction. But MTL circuits have better matching properties and zero gate leakage current. In MTL circuits all transistors operate in saturation region and generalized TL equation for loop connected MOS transistors is given by (2.27).

$$\sum_{cw}\sqrt{\frac{I_d}{W/L}} = \sum_{ccw}\sqrt{\frac{I_d}{W/L}} \qquad [2.27]$$

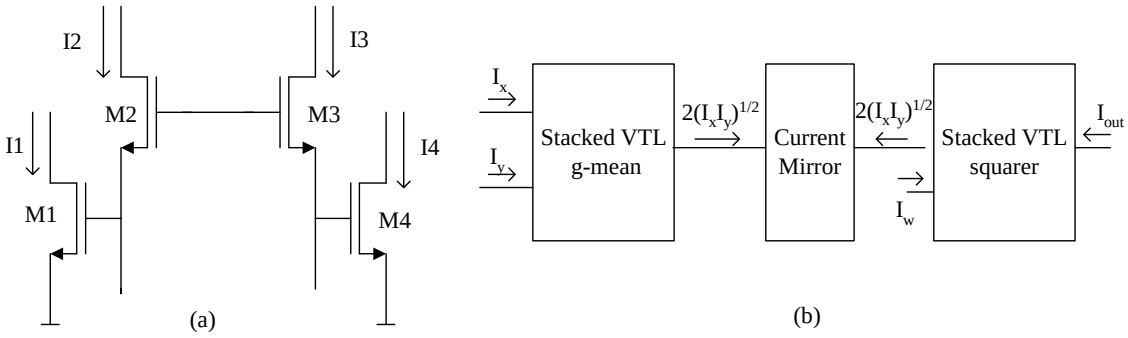


Figure 2.5 Voltage-translinear loop based (a) stacked topology (b) multiplier [20]

Many Multiplier/Dividers ([21], [20], [22]) are designed based on TL principle of MOS transistors. Figure 2.5 shows multiplier Voltage-translinear principle based multiplier

block diagram and its blocks. The stacked VTL circuit gives geometric mean of input currents. Assuming identical transistors, W/L ratios of all transistors becomes same and equation (2.27) reduces to

$$\sqrt{I_1} + \sqrt{I_2} = \sqrt{I_3} + \sqrt{I_4} \qquad [2.28]$$

Squaring on both sides gives

$$I_1 + I_2 + 2\sqrt{I_1 I_2} = I_3 + I_4 + 2\sqrt{I_3 I_4} \qquad [2.29]$$

By forcing currents I3 and I4 equal to

$$I_3 = I_4 = \frac{I_1 + I_2 + 2I_z}{4} \qquad [2.30]$$

I_z is copy of output current. Using equations (2.28), (2.29) and (2.30) I_z obtained as

$$I_z = \sqrt{I_1 I_2} \qquad [2.31]$$

Geometric mean and squarer circuits are obtained from stacked topology by enforcing the conditions in equations (2.32) and (2.33).

$$I_1 = I_x \quad I_2 = I_y \quad I_3 = I_4 = I_x + I_y + I_z \qquad [2.32]$$

$$4(W1/L1) = 4(W2/L2) = (W3/L3) = (W4/L4) \qquad [2.33]$$

$$I_z = 2\sqrt{I_x I_y} \qquad [2.34]$$

$$I_{out} = I_z^2 / I_w \qquad [2.35]$$

As shown in Fig.2.5 (b) first VTL circuit gives geometric mean of input currents as given by equation (2.34). This combined with squarer circuit and one more current input I_w implements multiplier/divider functionality as given by

$$I_{out} = I_x I_y / I_w \qquad [2.36]$$

TL based multipliers have high precision, wide current dynamic range (0.024% increase in slope of THD with input current) and insensitive to temperature and processing (less than 0.35% change in THD for -50C to 100C temperature change) [21]. The voltage translinear principle based stacked and up-down topologies of multipliers [20] have small area (0.32mm^2 for stacked topology and 0.24mm^2 for up-down topology), low power consumption, less complexity and low nonlinearity error (THD 1% and 1.5%). As shown in Figure 2.6, an improved configuration of multiplier [22] with reduced supply voltages and less THD is designed.

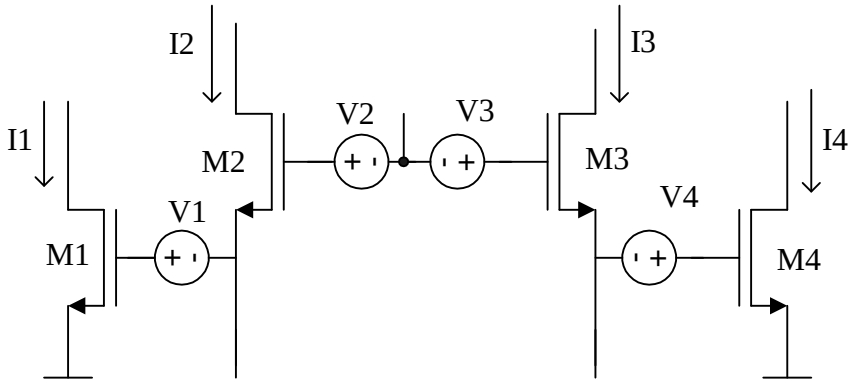


Figure 2.6 Voltage translinear loop with floating voltage sources

With same (W/L) ratios for all transistors, the TL loop equation (2.27) modifies as follows:

$$\sqrt{I_1}+\sqrt{I_2}-\sqrt{\frac{K}{2}}\left(V_1+V_2\right)=\sqrt{I_3}+\sqrt{I_4}-\sqrt{\frac{K}{2}}\left(V_3+V_4\right) \qquad [2.37]$$

where K is transconductance parameter. $V_1+V_2= V_3+V_4$ condition has to be satisfied to get stacked VTL loop equations. This modified configuration also extends its dynamic range of the signals. But these multiplier configurations are single quadrant and have less frequency response at higher values of current gain.

2.2.6 MOS Resistors

MOS implementation of resistors has many applications in analog signal processing. Tunable MOS resistors are used in active RC filters, controlled oscillators, variable gain amplifiers, current or voltage dividers and in variable resistive network synthesis [23]. Voltage controlled resistors or current controlled resistors are implemented by MOSFETs operating in linear, saturation region or sub-threshold region. Dependence of MOS resistance on threshold voltage limits tuning capability and injects substrate noise into the signal path and design becomes sensitive to process variations [24]. MOS resistors operating in linear region [25] have limited frequency response because of distributed channel capacitance in the triode region. Degree of nonlinearity is more pronounced especially for MOS control voltages close to threshold voltage. This prohibits application of MOS resistor to large signal applications [26].

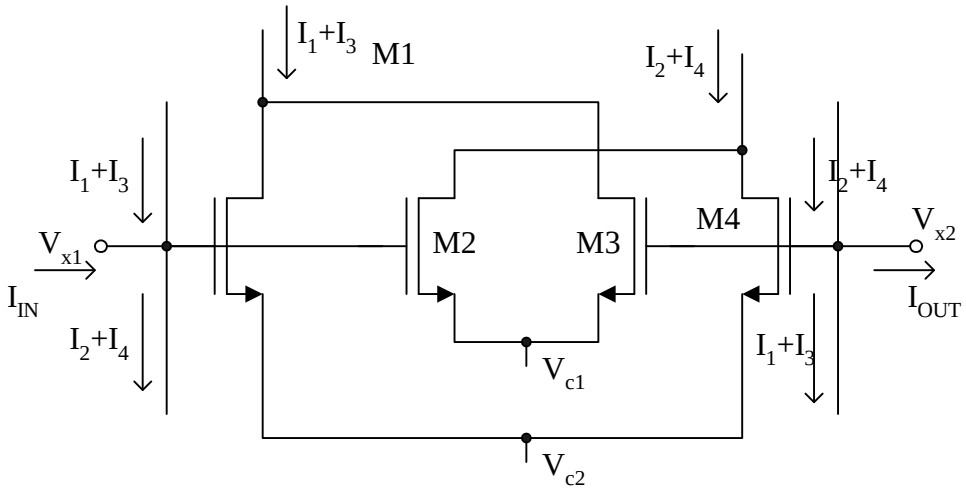


Figure 2.7 Floating MOS resistor circuit.

MOS resistors using saturated transistors have wide resistance values (3.3KΩ to 67KΩ) [27] as well as positive and negative resistance values (50KΩ to ∞ and -50kΩ to -∞) [28]. Figure 2.7 shows floating MOS resistor circuit with positive and negative

resistance values. The output resistance of this configuration with equal input and output currents is given as

$$R = \frac{1}{2K(V_{c2} - V_{c1})} \qquad [2.38]$$

Where K is transconductance parameter and V_{c1}, V_{c2} are control voltages. Saturated MOS resistors have high frequency of response and many times resistors in active RC filters are replaced with MOS resistors [29]. Resistive networks are used for smoothing signals and filtering of noise. In resistive networks, number of resistors used is large. The important characteristics of MOS resistors are small area, less power consumption at the expense of precision. MOS transistors working in weak inversion are used in low precision resistive networks [24].

2.2.7 MOS Divider Circuits

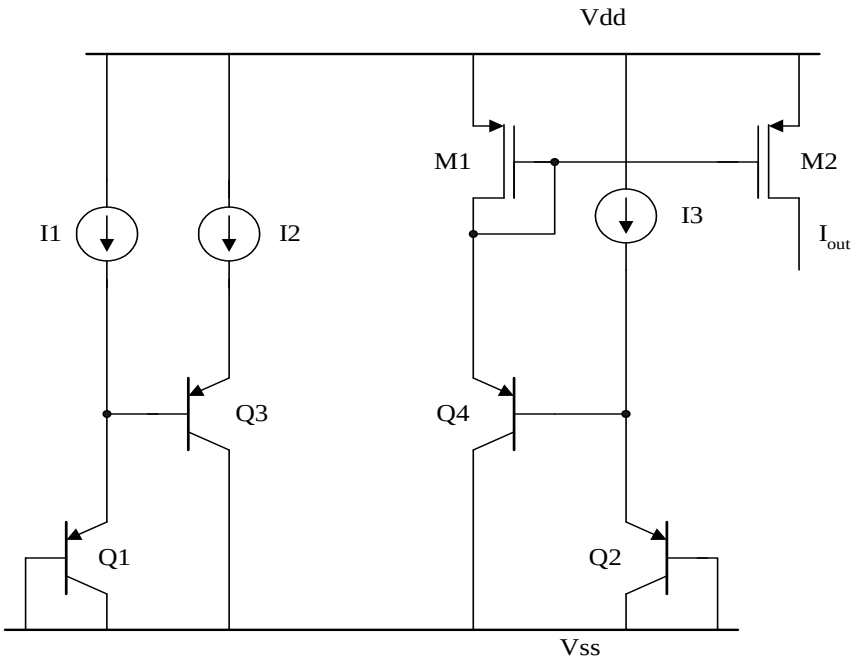


Figure 2.8 BJT Translinear divider configuration

Analog dividers do mathematical operation of division of two signals (voltage or current). An ideal divider with positive input signals is shown in Figure 2.9. In BJT technology, Gilbert translinear principle can be used to implement both multiplier and divider circuits [30] as shown in Figure 2.8. The exponential relationship between emitter current and base to emitter voltage is used in this type of dividers. Neglecting the effect of base currents, the output current Iout is expressed as

$$I_{out} = \frac{I_{E1} * I_{E3}}{I_{E2}} \qquad [2.39]$$

MOS dividers design is more complex compared to MOS multiplier design. A simplest form of divider is implemented by using MOS multiplier in the feedback path of an op amp based inverting amplifier [24]. Voltage variable resistance of MOS transistor is widely used to implement dividers ([31], [32]). The current dividers implemented in this configuration have less linearity error (THD < 1%), high frequency of

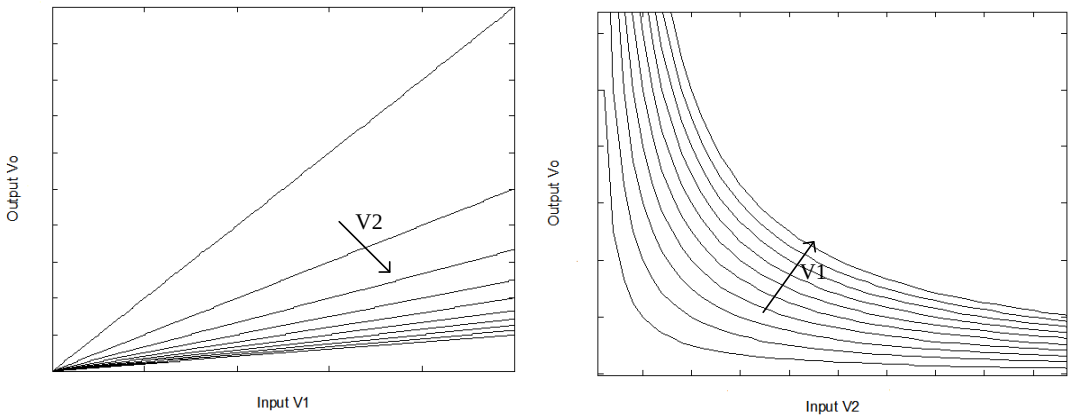


Figure 2.9 Ideal voltage divider characteristics Vo=V1/V2

response and low power consumption (less than 0.22mW) [31]. Sampled data quotient circuit realizations of dividers [33] have low frequency response and high power consumption and area. But recently proposed current mode A/D-D/A based divider has

low power consumption (318μW), less area (0.077mm^2) but at the expense of linearity error (±2.47%) and offset error of 1.82% of full scale current [34]. In divider design, trade-off exists between area, power consumption and accuracy. Therefore each divider design is specific to area of application.

CHAPTER 3 DESIGN AND SIMULATION OF MOS RESISTOR/DIVIDER

3.1 Introduction

In this chapter, current controlled grounded MOS resistor is explained. Later in this chapter, using this MOS resistor for signal divider is also presented. In the end, implementation of four quadrant differential input multiplier using this MOS resistor is also presented. The qualitative analysis will be supported by Cadence Analog Artist simulation results based on AMIS C5F 0.5μm process.

3.2 MOS resistor/divider design

The small signal output resistance of MOS transistor is inversely proportional to the bias current.

$$r_o = \frac{1}{\lambda I_d} \qquad [3.1]$$

where λ is channel length modulation parameter and I_d is drain current. For channel lengths more than 5T (T is minimum feature size for given technology) and for given gate to source voltage (V_{GS}) change in small signal output resistance is small. MOS resistor is designed based on this principle. The idea is shown in Figure 3.1, where all transistors are working in current saturation mode. In this MOS resistor M0, M3, M4-M5 and M7-M8 form current mirror pairs. M6 and M9 are output stage transistors of MOS resistor. Small signal equivalent circuit of MOS resistor is shown in Figure 3.2.The

output resistance seen through the terminal B into the grounded resistor (Input A grounded) is equal to R_{out}.

$$R_{out} = v_x / i_x$$
$$= r_{06} // r_{09} \qquad [3.2]$$

r_o is small signal output resistance of M6/M9 transistors. This MOS resistor is voltage follower between points A and C. It has high input impedance at the input node (A) and comparatively low output impedance at node B. This is special case of MOS resistor, at one end of input (A) it gives high resistance where as at other end the resistance is controlled by current.

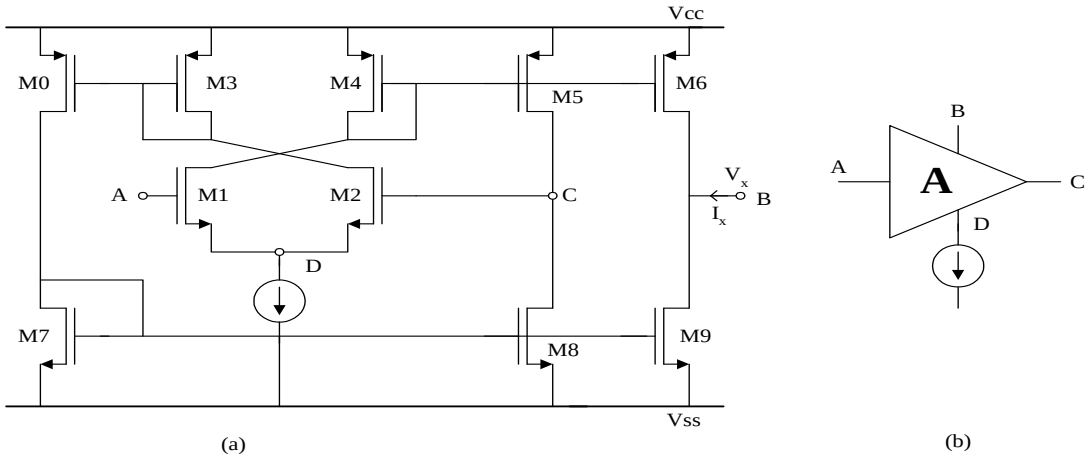


Figure 3.1 (a) Current controlled MOS resistor synthesis (b) block diagram representation

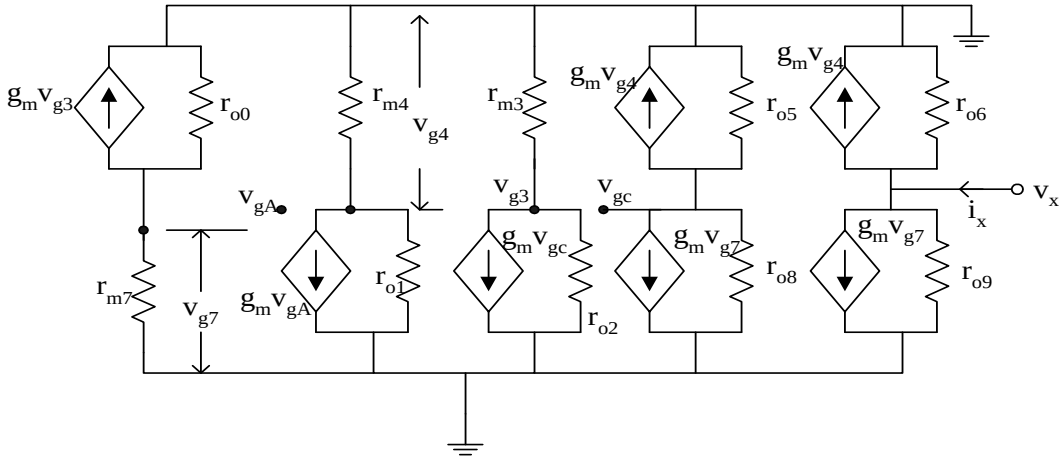


Figure 3.2 Small signal equivalent circuit of MOS resistor

3.3 Four quadrant multiplier using MOS resistor

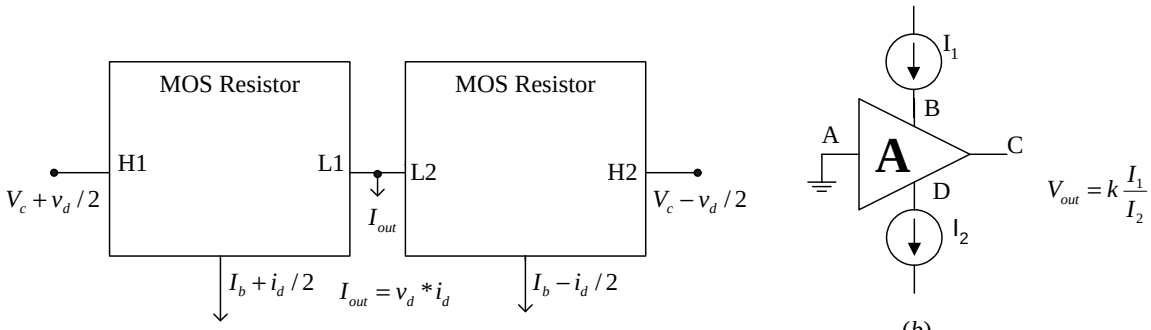


Figure 3.3 (a) Four-quadrant multiplier using MOS resistors (b) Signal divider

Four-quadrant multiplier is implemented using two MOS resistors as shown in Figure 3.3 (a). H1, H2 are high impedance nodes and L1, L2 are low impedance nodes of MOS resistor. With differential input voltage applied at one end of MOS resistor, output current is given by

$$\Delta i_{out} = \frac{\Delta v_d}{R} \qquad [3.3]$$

Where R is simulated value of MOS resistor. Since R is controlled by differential current input, output current is given by

$$\Delta i_{out} = K \Delta v_d * \Delta i_d \qquad [3.4]$$

Signal divider function implementation using MOS resistor is shown in Figure 3.3 (b). Input current i_1 is applied at input B and output voltage gives divider function given by

$$v_{out} = i_1 * R \qquad [3.5]$$

$$v_{out} = K\frac{i_1}{i_2} \qquad [3.6]$$

Since the controlling current i_2 has to be positive, this divider works only first-quadrant.

3.4 Simulations

To find the performance of MOS resistor, simulations are performed using Spectre simulator utilizing transistor parameters of 0.5μm AMIS C5F CMOS process supplied by MOSIS. The results of simulation are shown in Figure 3.4 and Figure 3.5. The size of NMOS transistors is (W/L)=20/0.6μm and PMOS transistors (W/L)=60/0.6μm. With these dimensions, the simulated values of resistance are 16.4KΩ to 35.2KΩ with control current ranging from 50μA to 500μA. As can been seen, the proposed MOS resistor can work in two quadrants. This MOS resistor has acceptable linearity and it has limited dynamic range of operation with input voltages restricted between ±1V.

This MOS resistor is used to implement differential input four quadrant multiplier as shown in Figure 3.3. Each differential input is set by two balanced signals defines as the following,

$$V_1 = V_c + v_d / 2 \qquad V_2 = V_c - v_d / 2 \qquad [3.7]$$

$$I_1 = I_b + i_d / 2 \qquad I_2 = I_b - i_d / 2 \qquad [3.8]$$

Where V_c and I_b are common mode input voltage and bias current, and v_d and i_d are differential inputs. The simulated transfer characteristics of multiplier are shown in Figure 3.6. The common-mode voltage is set to 0.6V and a bias current of 100μA is chosen. The higher value to bias current is chosen to improve bandwidth. As shown in Figure 3.7, the MOS resistor based multiplier has 3-dB bandwidth of 110MHz. The maximum average power of 1.25mW is dissipated at the full input swings. This multiplier has limited input signal range of ±1V and ±10μA. Total harmonic distortion

(THD) gives the percentage of total harmonic content of a signal with respect to fundamental frequency.

$$THD_{\%} = 100\% * \frac{\sqrt{\sum_{2}^{\infty} V_n^2}}{V_1} \qquad [3.9]$$

where $V_1, V_2 ... V_n$ are harmonic components in the signal [35]. The THD is obtained by keeping one input at a constant DC value while changing the signal at the other input. The worst case THD simulated is 3% for 10 KHz input voltage with 1Vp-p amplitude, while other input is kept at 5μA.

The same MOS resistor can be used as single quadrant current signal divider as shown in Figure 3.3. The output characteristics of divider function ($V_o=I_1/I_2$) with two signal currents as parameters are shown in Figure 3.8 and Figure 3.9. Input current I_1 has signal range of 0 to 10μA and input current I_2 has signal range of 10μA to 500μA. Input current signal range cannot be extended to lower values, because of high nonlinearities at current less than 10μA. Figure 3.9 shows simulated waveforms of divider at the output where numerator is held constant (I_1=5μA) and I_2 is a 5 KHz triangular waveform varying between 10μA and 100μA. The output voltage in inversely proportional to the input current ($V_o=5/I_2$) as observed in Figure 3.10.

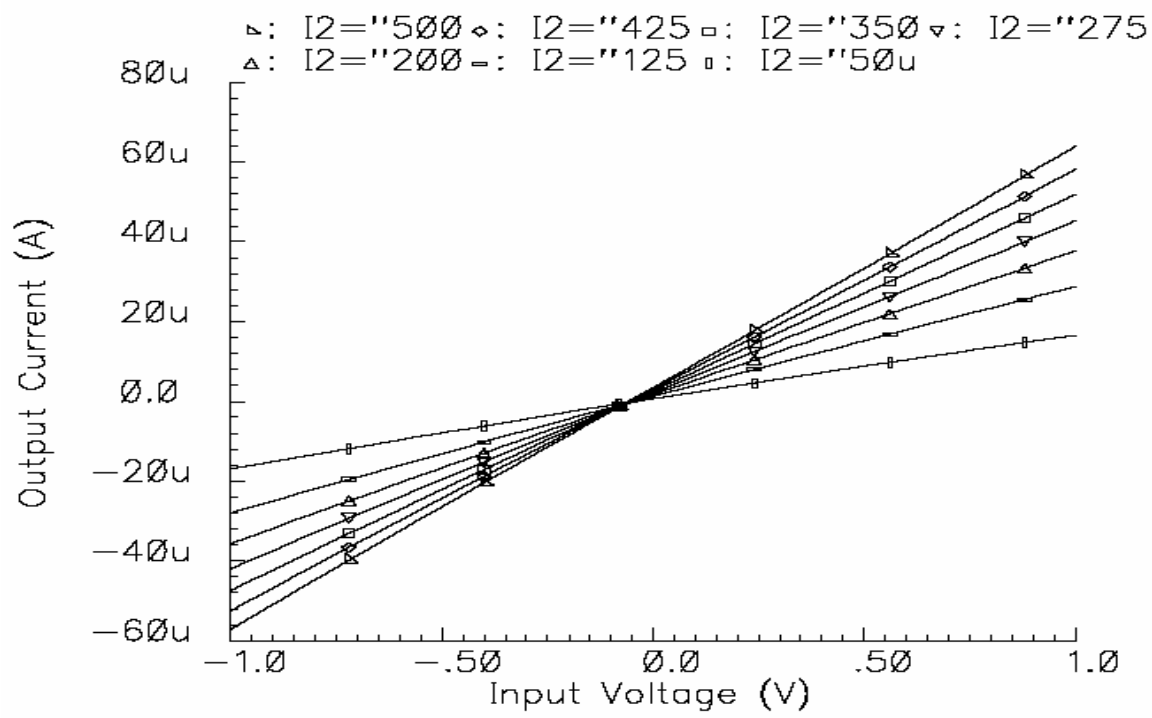


Figure 3.4 Transfer characteristics of MOS resistor

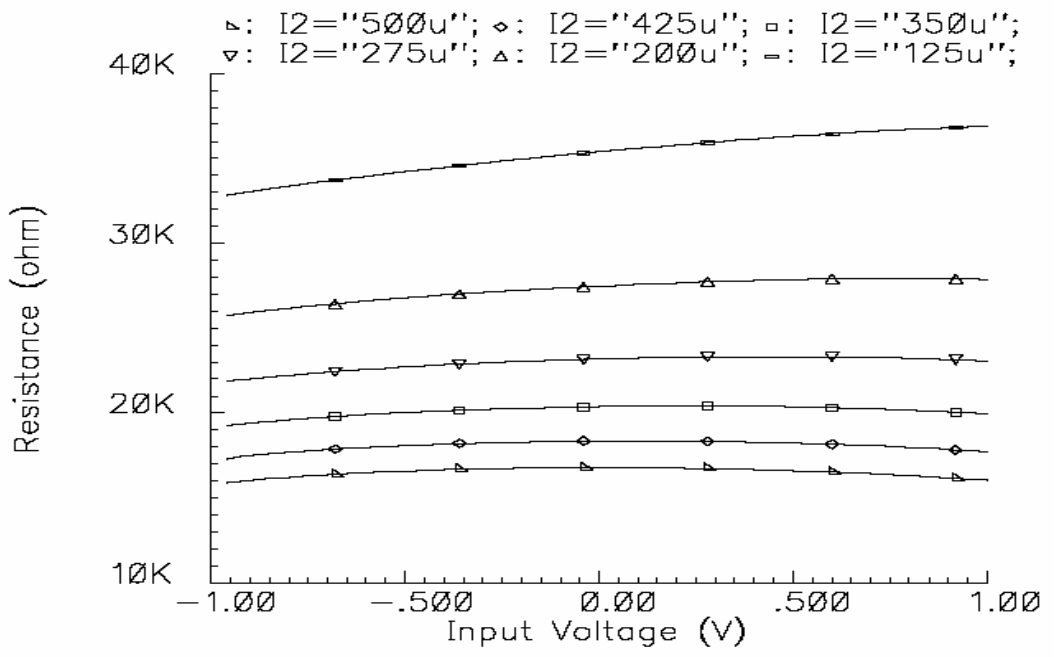


Figure 3.5 Synthesized resistance of MOS resistor

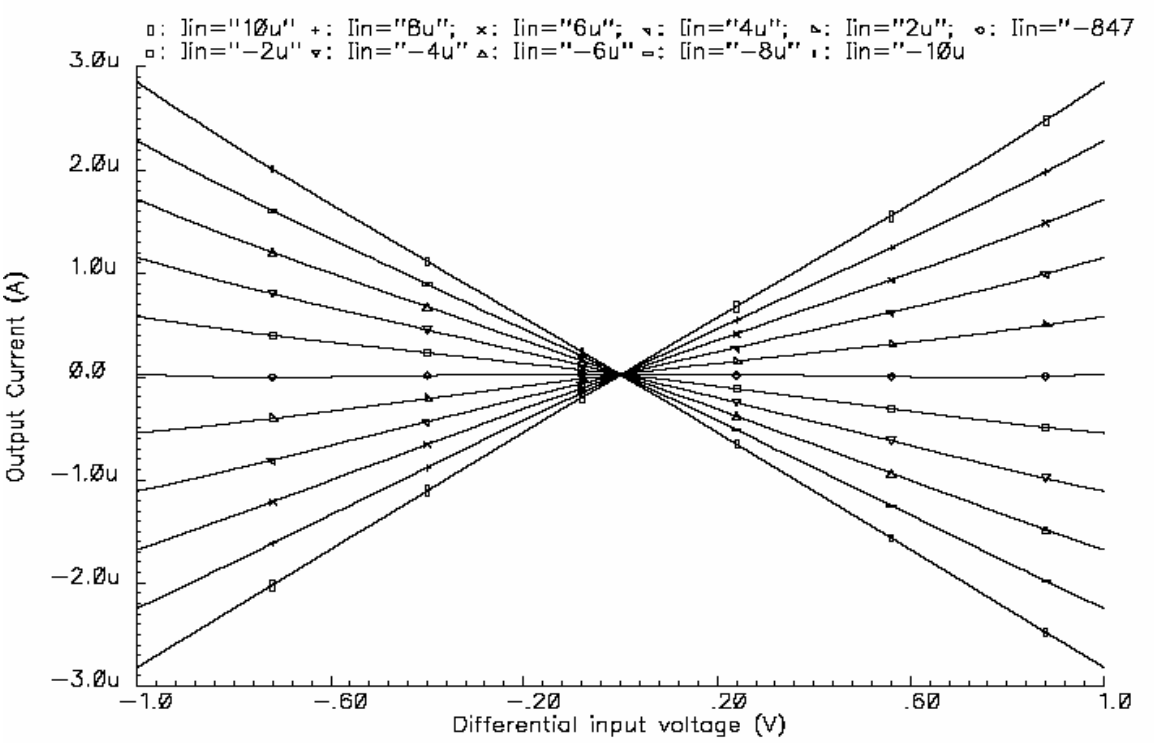


Figure 3.6 Transfer characteristics of MOS resistor based four-quadrant multiplier

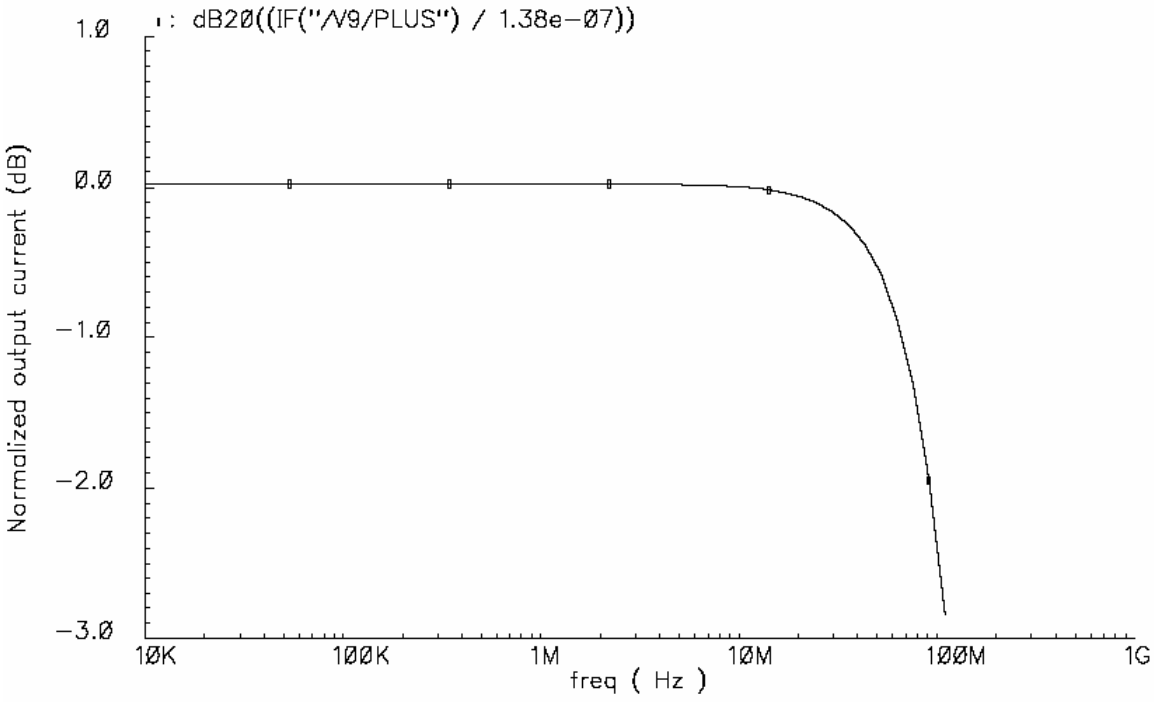


Figure 3.7 Normalized frequency response of four quadrant multiplier

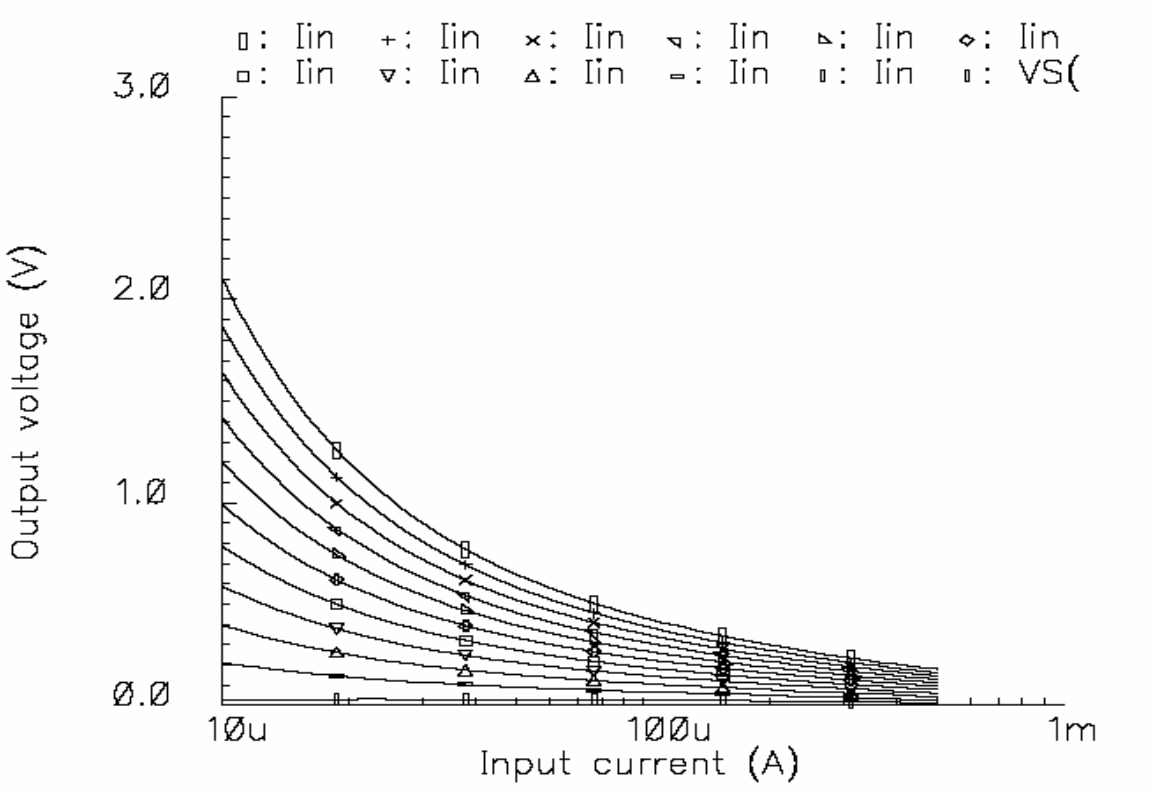


Figure 3.8 Output voltage (V_o) of divider with input current (I_1) as parameter ($Vo=I_1/I_2$)

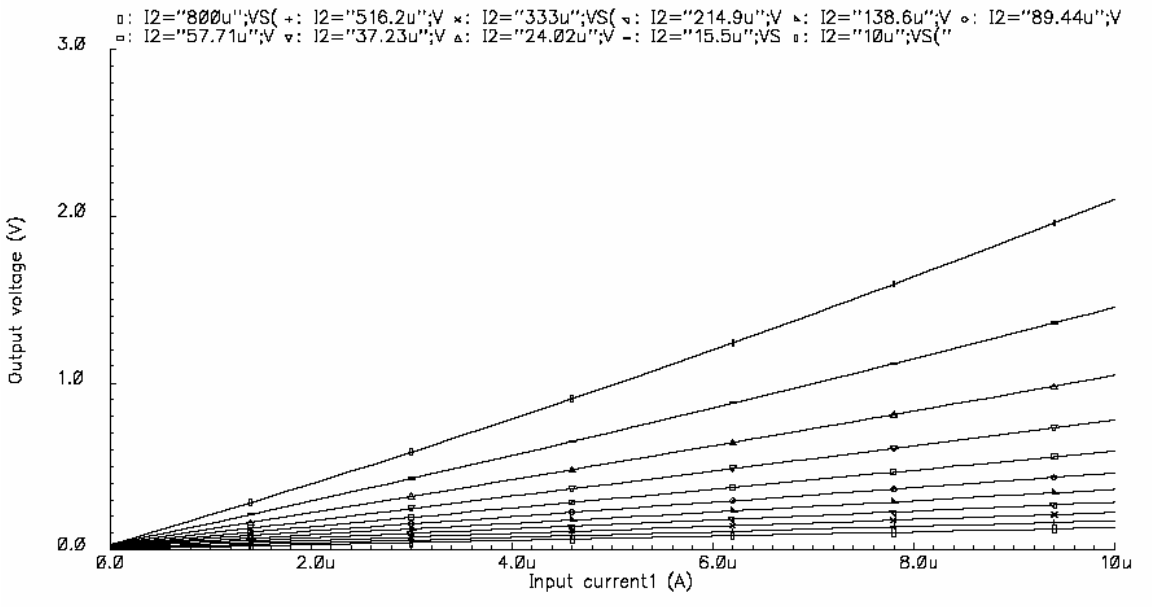


Figure 3.9 Output voltage (V_o) of divider with Input current (I_2) as parameter ($V_o=I_1/I_2$)

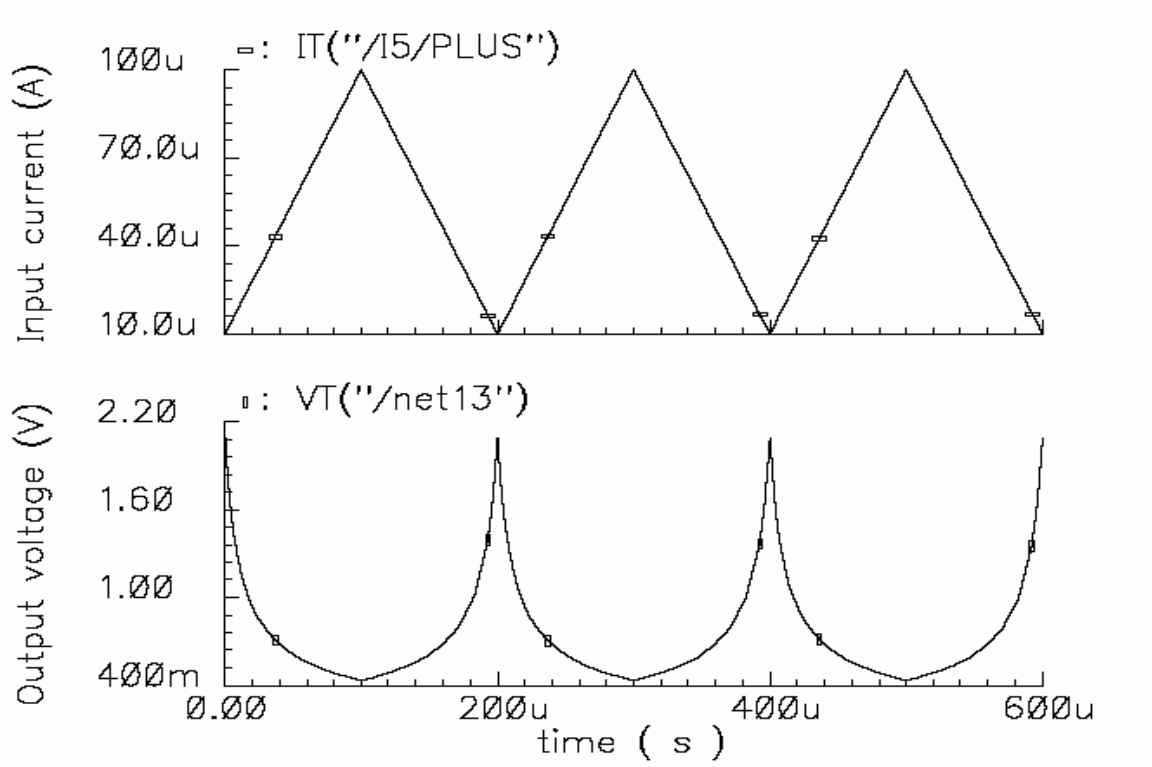


Figure 3.10 Simulated transient response of MOS divider

3.5 Summary of Simulation Results

Table 3.1 Summary of simulation results of MOS resistor, multiplier and divider

Parameters	Values
$\left(\frac{W}{L}\right)_n, \left(\frac{W}{L}\right)_p$	20μm/0.6μm, 60μm/0.6μm
Power consumption	1.25mW
Multiplier voltage and current range	±1V ±10μA
Divider current ranges	0-10μA , 10μA-500μA

Some of MOS resistor, MOS resistor based multiplier and divider parameters are listed in Table 3.1. As this configuration of multiplier is more complex, consumes more power and has poor linearity, a better configuration of multiplier is designed and explained in the next chapter.

CHAPTER 4 DESIGN AND SIMULATION OF MULTIPLIER

4.1 Introduction

In this chapter a new approach to designing a differential input multiplier configuration is presented. This multiplier works in all four quadrants; i.e., both the inputs can be positive or negative. The approach here is unique in that we attempt to use source connected resistance of MOS differential pair for multiplier implementation. This method improves the output resistance as well as linearity of the output. This voltage and current input differential multiplier has many applications in neural networks because neural networks use weights as voltage inputs and synapse signals as current inputs. This multiplier assumes no mismatching in the circuit. At sub-micron level the second order effects of MOSFETs like channel length modulation cannot be neglected because of small channel lengths. The inherent advantage of this multiplier is that it accurately models MOS voltage-current characteristics by taking channel length modulation effects into consideration. The output resistance of MOS transistor is proportional to the channel length modulation parameter (λ) and MOS bias current. This principle is used in multiplier implementation. The differential configuration also cancels out inherent noise present in the inputs and thus improves common mode rejection ration of this differential configuration.

4.2 Differential multiplier design

4.2.1 Principle of operation

As shown in Figure 4.1 the core of differential multiplier consists of two cross coupled N-type differential pairs. Each differential pair (M1, M2, M5, M6 and M3, M4, M7, M8) uses pair of composite transistors. Each composite transistor has N-type MOS transistor connected to the source of differential input transistor. The drain voltages of differential pair are maintained at equal value by current subtractor of next stage. All the MOS transistors (M1-M8) operate in current saturation region. Common mode voltage (V_c) and differential input (V_x) are applied to each differential pair.

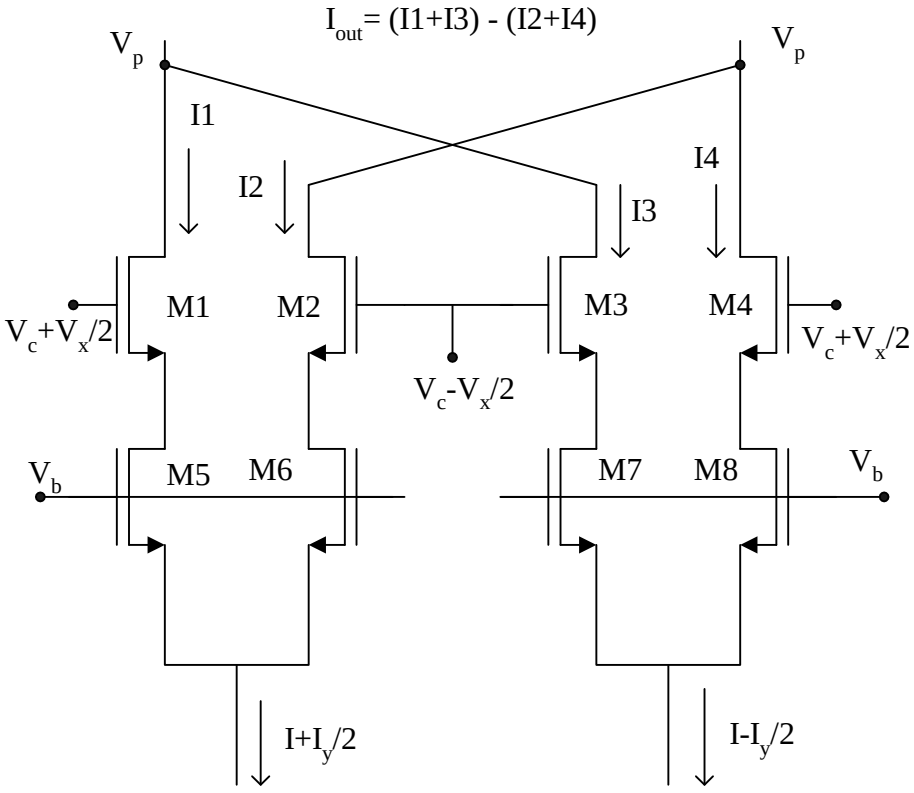


Figure 4.1 Simplified schematic of four quadrant differential multiplier

All the source connected transistors (M5-M8) are biased by fixed voltage (Vb). Gate source voltages of M5, M6 and M7, M8 transistors are same.

$$V_{GS5} = V_{GS6} \qquad V_{GS7} = V_{GS8} \tag{4.1}$$

The change in drain current of these transistors is controlled by channel length modulation parameter (λ). The drain current of current saturated MOS transistor is given by (4.2) including channel length modulation. V_t is threshold voltage and K' is transconductance parameter of MOS transistor.

$$I_d = \frac{K'W}{2L}(V_{GS} - V_t)^2(1 + \lambda V_{DS}) \tag{4.2}$$

$$\frac{\Delta I_d}{\Delta V_{DS}} = \frac{K'W}{2L}(V_{GS} - V_t)^2 \lambda = \lambda I_d = g_o \tag{4.3}$$

I_d in equation (4.3) is drain current without channel length modulation and g_o is output conductance of MOS transistor. Therefore transistors M5-M8 are modeled as resistors with the resistance value given by r_o. The small signal model of the schematic is shown in Figure 4.2. This variable r_o gives more control on transfer characteristics of multiplier. The small signal drain current of source degenerated MOS transistor with source resistance of R_s is given by equation (4.4). r_m is transresistance of MOS transistor.

$$i_d = \frac{v_{in}}{r_m + R_s} \tag{4.4}$$

$$i_d = v_{in} / R_s \qquad R_s >> r_m \tag{4.5}$$

Since output resistance of MOS transistor is more than transresistance, output current is controlled by output resistance of source connected transistors (r_{o5}-r_{o8}). Using equation (4.5), the small signal currents are given by

$$i_1 = (v_c + \Delta v_x / 2) / r_{o5} \tag{4.6}$$

$$i_2 = (v_c - \Delta v_x / 2) / r_{o6} \tag{4.7}$$

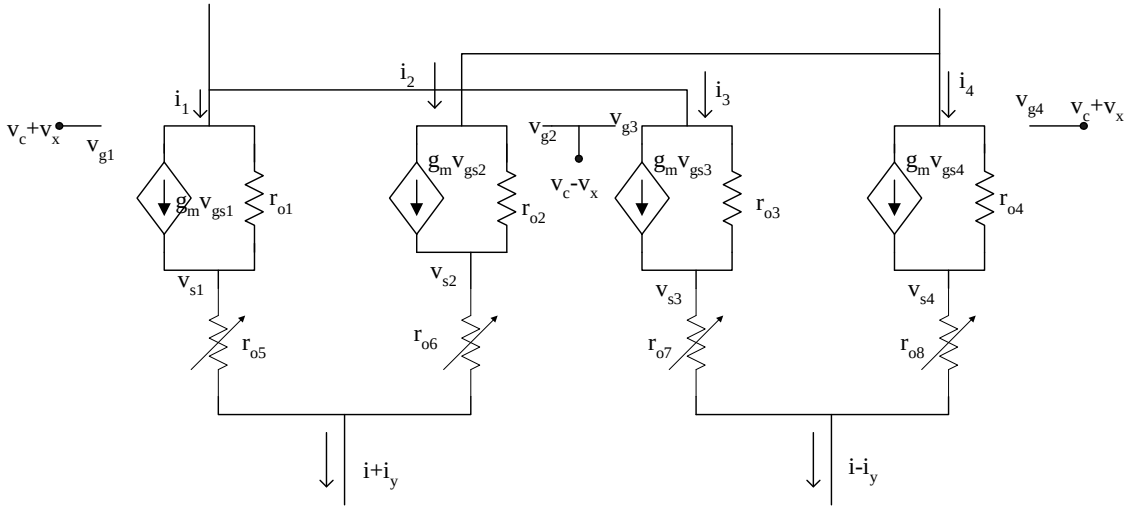


Figure 4.2 small signal schematic of differential multiplier

$$i_3 = (v_c - \Delta v_x / 2) / r_{o6} \qquad [4.8]$$

$$i_4 = (v_c + \Delta v_x / 2) / r_{o8} \qquad [4.9]$$

Using equations (4.6)-(4.9) output current i_o is given by

$$i_o = (i_1 + i_3) - (i_2 + i_4) \qquad [4.10]$$

$$i_o = (v_c + \Delta v_x / 2) / r_{o5} + (v_c - \Delta v_x / 2) / r_{o7} - (vc - \Delta v_x / 2) / r_{o6} - (vc + \Delta v_x / 2) / r_{o8} \qquad [4.11]$$

Assuming matching of transistors M5, M6, M7 and M8 and equation (4.3)

$$\begin{aligned} i_o = \lambda\{&(v_c + \Delta v_x / 2)(i + \Delta i_y / 2) + (v_c - \Delta v_x / 2)(i - \Delta i_y / 2) \\ &- (vc - \Delta v_x / 2)(i + \Delta i_y / 2) - (vc + \Delta v_x / 2)(i - \Delta i_y / 2)\} \end{aligned} \qquad [4.12]$$

$$i_o = K \Delta v_x \Delta i_y \qquad [4.13]$$

K is a constant whose value is equal to λ. Thus for any given input voltage and input current, the output voltage is proportional to the product of differential input voltage and differential input current. Output current is obtained by subtracting output currents of differential pairs. This current subtractor is explained in the next section.

4.2.2 Design of current subtraction circuit

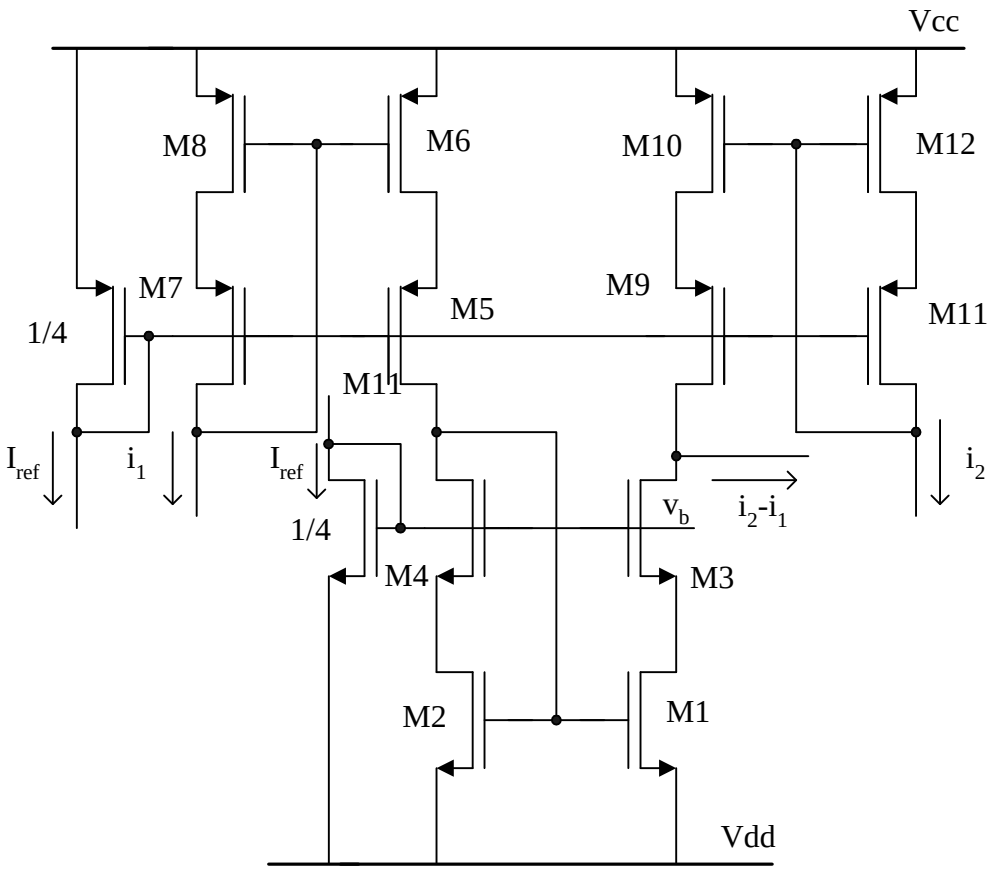


Figure 4.3 CMOS current subtraction circuit

Although, a simple current mirror can be used for current subtraction, the drain voltages of input transistors need to be kept at same value. The simple current mirror drain voltages differ by threshold voltage. So a special subtraction circuit is designed with high output resistance current mirrors. Figure 4.3 shows current subtraction circuit, which uses three identical current mirrors i.e. M1-M4, M5-M8 and M9-M11. These are high swing and high output resistance current mirrors. All these transistors have same W/L ratio and no mismatching is assumed for threshold voltages and transconductance parameters of PMOS and NMOS transistors. In this current mode implementation of

subtractor, the input current i_1 is mirrored by M5-M8 and current i_2 is mirrored by M9-M12. By principle of KCL at the output node of M1-M4 current mirror pair, i_1-i_2 is obtained. Current gain is excellent because of same V_{ds} for lower pair of transistors in each mirror. To reduce channel length modulation effect, length of channels is kept high. This current subtraction circuit is connected to output of differential multiplier. The important characteristic of multiplier is to obtain large input signal ranges. Stacking less number of transistors between the power supply lines allows larger signal swings. In addition to the threshold voltages of input transistors, the current mirrors in current subtraction circuits prevents the input voltage swings from reaching the supply rails. The minimum input voltage (V_t+Δ) required for current mirrors decides the input swing of differential multiplier.

$$\Delta = \sqrt{\frac{2I}{K'(W/L)}} \qquad [4.14]$$

I is input current and V_t is threshold voltage of transistor. In order to improve the input signal range, Δ is kept small by using lower values of bias currents. The smaller supply currents also guarantee lower power dissipation.

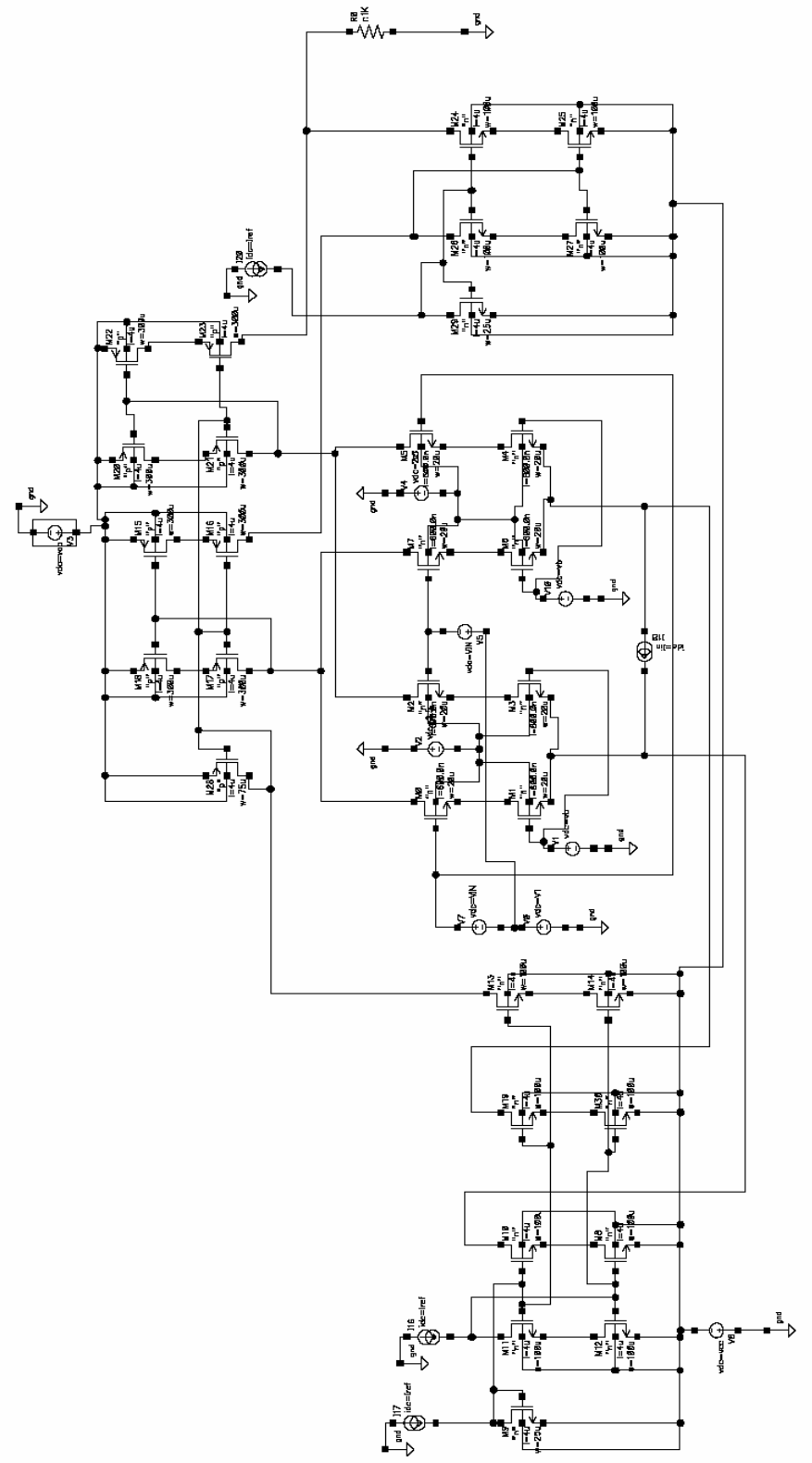


Figure 4.4 Complete schematic diagram of four quadrant multiplier

4.3 Simulations

The simulations of this differential multiplier were done using SPECTRE circuit simulator, in Cadence Analog Artist with AMIS C5F 0.5μm technology parameters. The simulated CMOS multiplier schematic is shown in Figure 4.4. Important parameters of NMOS and PMOS like transconductance parameter (K') and channel length modulation parameter (λ) are extracted from device characteristics [36]. The extracted parameters are listed in the Table 4.1. Mismatches are avoided between NMOS and PMOS transistors by proper selection of W/L ratios as shown in table 4.1. A higher value of bias current gives better bandwidth to multiplier but at the expense of power consumption. Therefore an optimum value of bias current (10μA) is chosen to give good bandwidth as well as low power consumption.

Table 4.1 Parameter summary of CMOS four quadrant multiplier

Parameters	Values
K'_n, K'_p (extracted parameter)	$72.96\mu A/V^2$, $6.41\mu A/V^2$
λ (extracted parameter)	$0.0217V^{-1}$
Bias current I_B	10μA
Loading resistor R_L	1kΩ
$(W/L)_0$-$(W/L)_3$	20μm/0.6μm
$(W/L)_4$-$(W/L)_7$	20μm/1.8μm
$(W/L)_8$, $(W/L)_{28}$	25μm/2.4μm
$(W/L)_{23}$, $(W/L)_{15}$-$(W/L)_{22}$	75μm/2.4μm,
$(W/L)_9$-$(W/L)_{14}$, $(W/L)_{24}$-$(W/L)_{27}$	100μm/2.4μm

Fig. 4.5 illustrates the simulated DC transfer characteristics of multiplier obtained for input voltage ranging from -2.2V to 2.2V in 7 steps and input current swept form -10μA to 10μA. These transfer characteristics are simulated with 1KΩ load resistor. Figure 4.6 shows variation of Total Harmonic Distortion (THD) with input signal amplitude. THD simulations performed with 1V @ 100 KHz sine wave input. THD is as low as -20dB (0.1%) for full range of input current. The variation in THD is from 0.07% to 0.1% for full swing of input current. These characteristics show superior performance in terms of linearity. The output frequency response is shown in fig. 4.7. It shows that the output 3-dB bandwidth is 73MHz with 1KΩ resistive loading. With change in bias current the highest bandwidth that was obtained for multiplier is 192MHz for bias current of 100μA.

Fig. 4.8 and Fig. 4.9 show the applications of multiplier as amplitude modulator and phase detector. Fig. 4.8 illustrates an amplitude modulator with 100 KHz carrier sinusoid (upper waveform), 5 KHz triangular periodic modulating signal (lower waveform) inputs to the multiplier and AC modulated output (middle waveform). Two input sinusoid signals ($V_1 \sin(2\pi 10Kt)$ and $I_1 \sin(2\pi 10Kt + \phi)$) with phase difference are applied to the multiplier and the average output current (DC component) is plotted against phase as shown in Fig.4.9. The average output current is proportional to the cosine of phase difference ($\cos\phi$) between input signals. As shown in Fig. 4.2 MOS transistors connected at source terminals of input transistors acts as variable resistors with resistance controlled by bias current. This provides programmable multiplier cell. The worst case power consumption for multiplier is estimated to be 0.242mW.

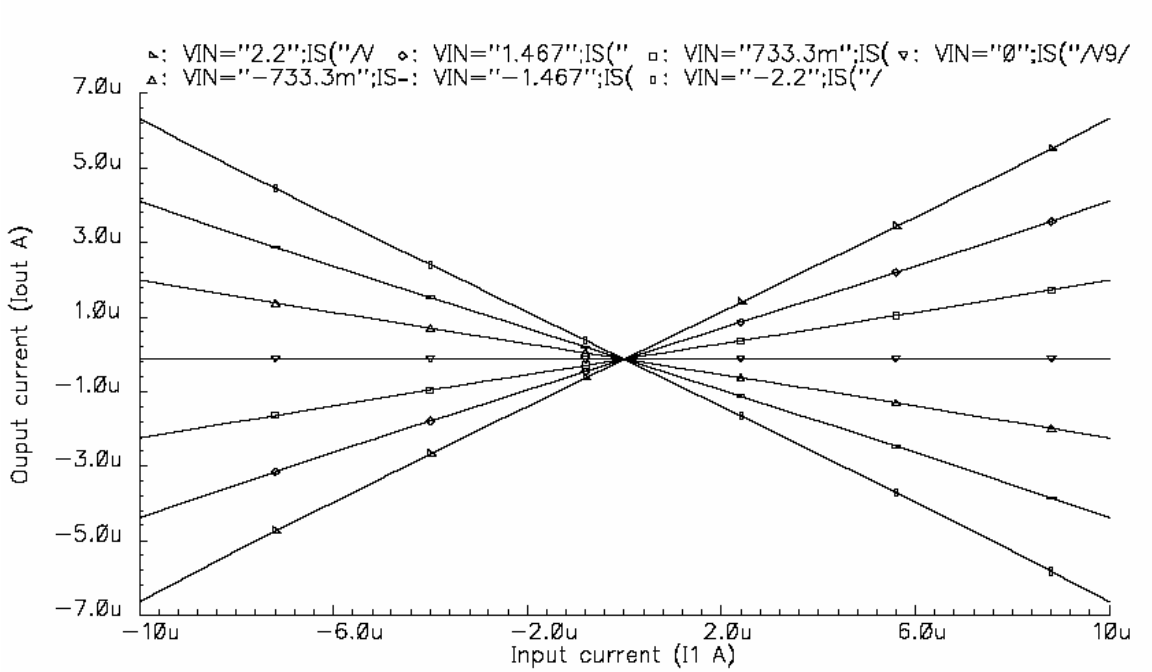


Figure 4.5 Simulated transfer characteristics of CMOS multiplier

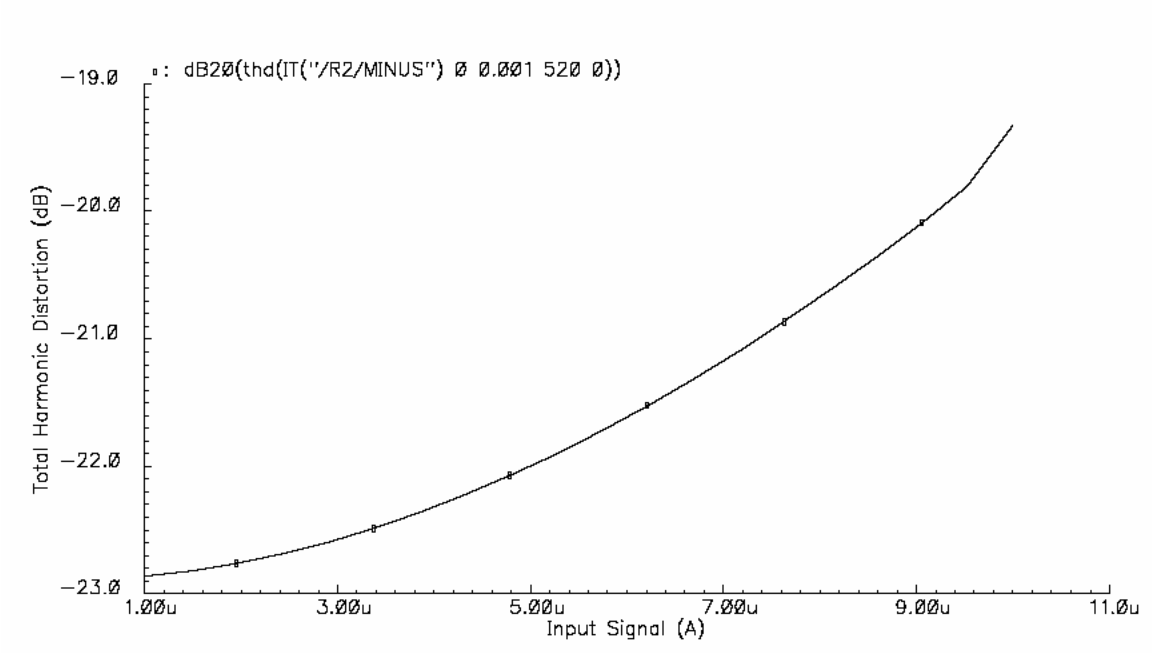


Figure 4.6 Total harmonic distortion of CMOS multiplier as a function of input current

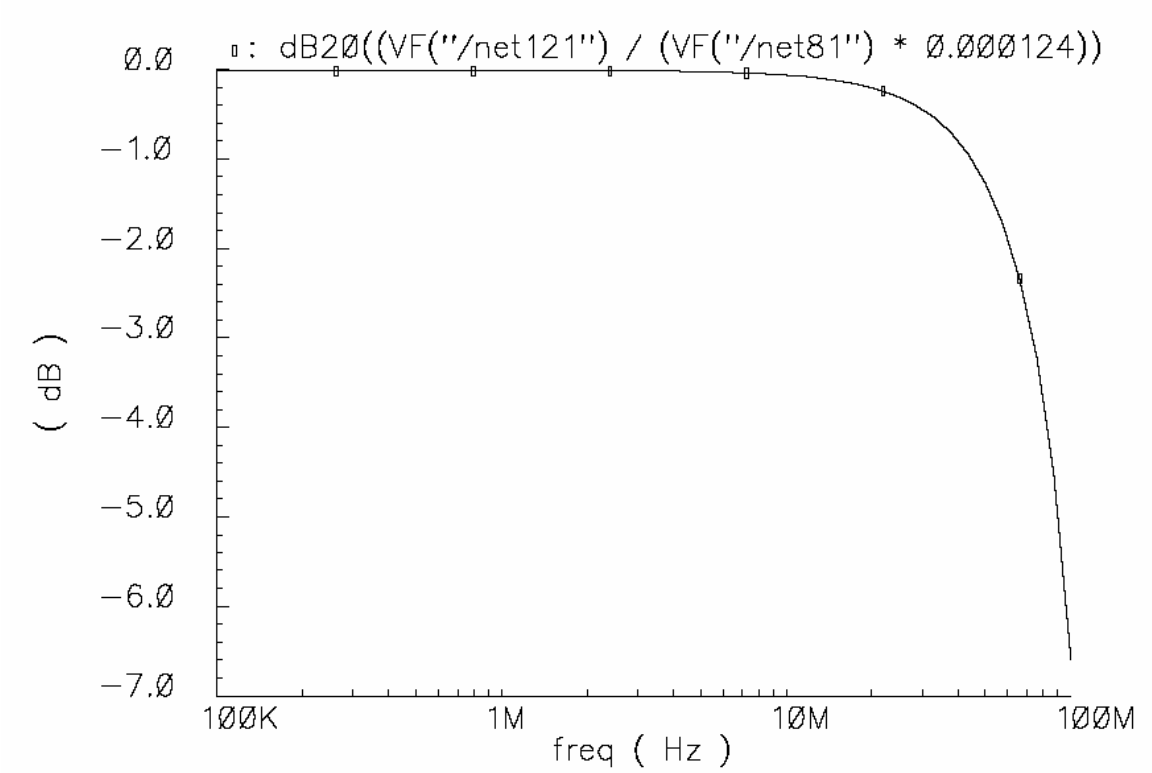


Figure 4.7 Normalized frequency response of CMOS four quadrant multiplier

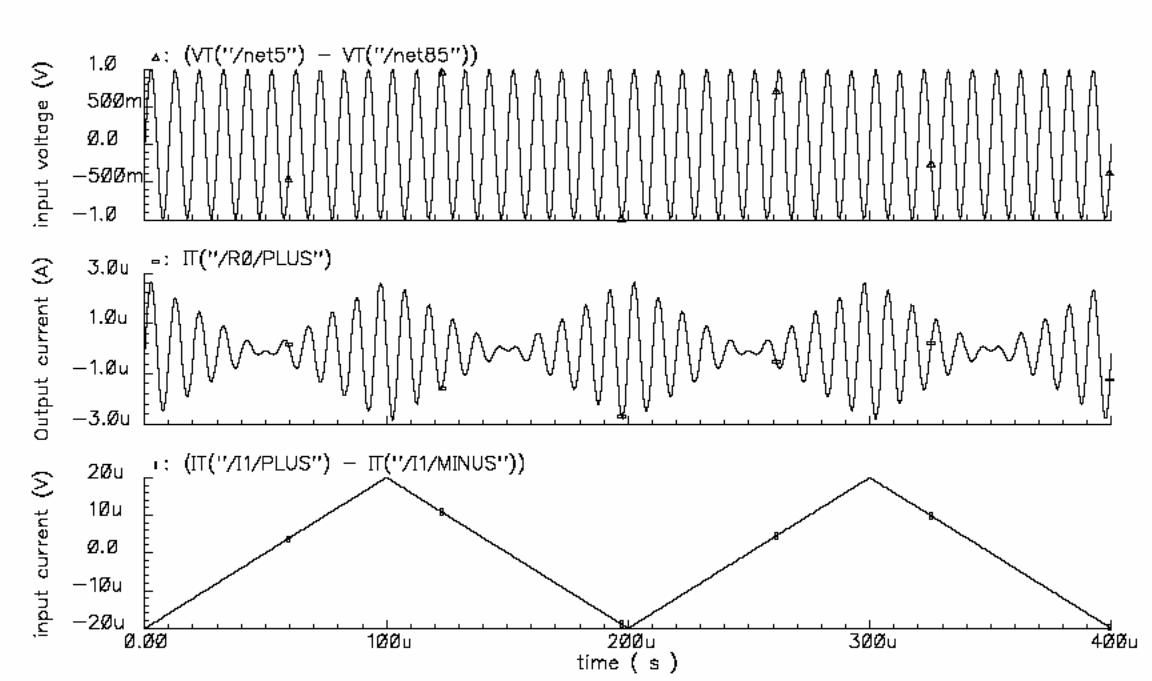


Figure 4.8 Modulated output waveform of multiplier with sine and triangular wave inputs

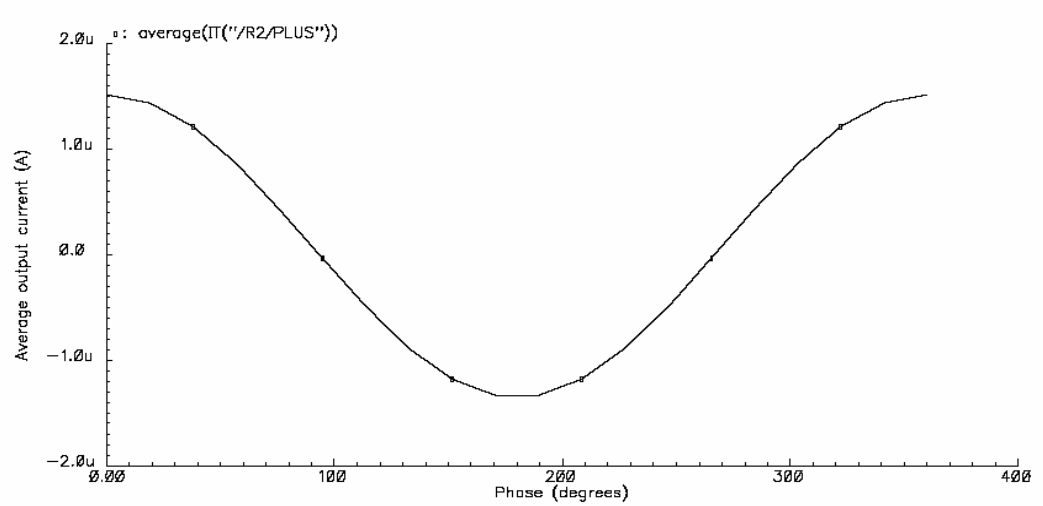


Figure 4.9 Average output current of multiplier as a function of phase difference of inputs

4.4 Summary of Simulation Results

Table 4.2 Summary of simulation results of Multiplier

Multiplier Characteristics	Values
Input voltage	±2.2V
Input current range	±10μA
THD @ 100KHz	0.07%
Input BW	73MHz
Bias current	10μA
Power consumption	0.242mW

Some crucial parameters that affect the performance of multiplier are provided in Table 4.2. For same supply voltage, some of parameters like power consumption, linearity and bandwidth are much better in this design compared to current-mode multiplier[37].

CHAPTER 5 LAYOUT OF MULTIPLIER

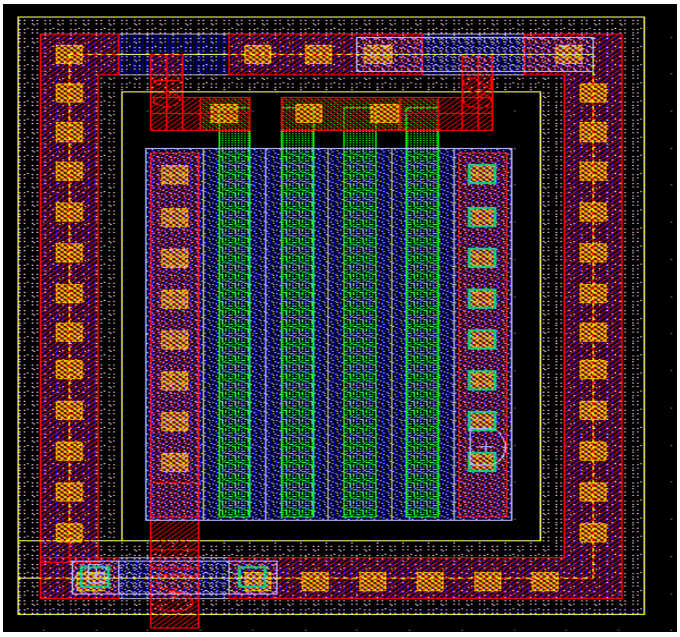
5.1 Introduction

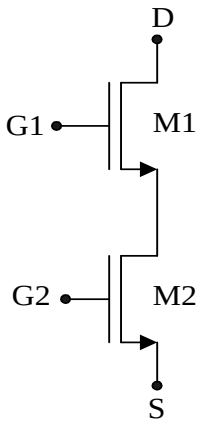
The successfully simulated four-quadrant multiplier layout is made in this chapter. Some special layout techniques used in four-quadrant multiplier layout are presented in this chapter. The techniques are very important in analog circuit design in order to avoid mismatching problems in the multiplier. Some tradeoffs are made to optimize the effects. In the end, post-layout simulation results are presented using multiplier circuit extracted from layout. Layout of the multiplier is done using Cadence Virtuoso layout editor using AMIS C5F technology libraries. Assura is used for design rule check (DRC) and layout versus schematic (LVS) checking. The area is occupied by the large current mirrors of subtraction circuit with higher values of (W/L) ratios.

5.2 Layout considerations

A customized transistor layout [38] is used for cascode input transistors as shown in Figure 5.1. In this configuration channel length of M2 transistor is three times longer than channel length of M1. This gives higher output resistance to M2 transistor and satisfies the condition (4.5). In this customized layout the source of M1 transistor and drain of M2 transistor are shared. Since this layout eliminates the need of metal contact between source and drain and reduces diffusion area, the effective capacitance also reduces. Further, this configuration reduces any mismatches between the two transistors.

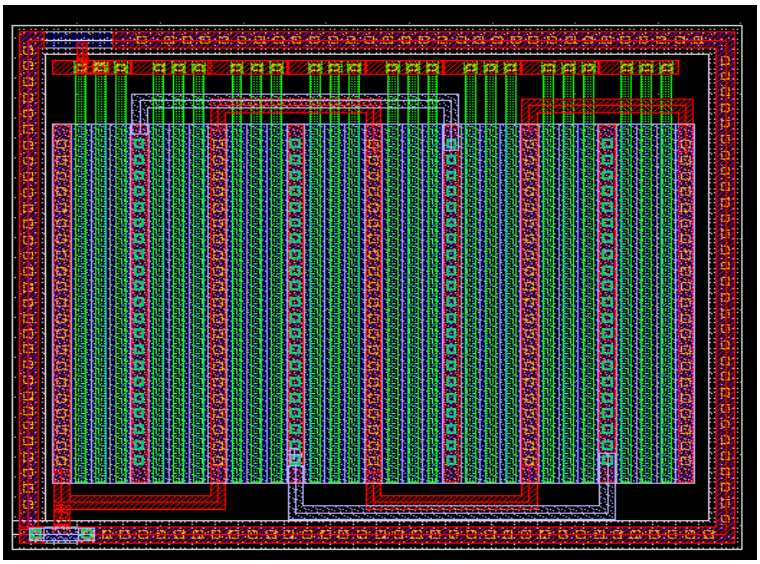
Figure 5.2 shows layout of current mirror MOS transistors. To reduce current mismatches between input and output, very high width (W=100μm) transistors are used.

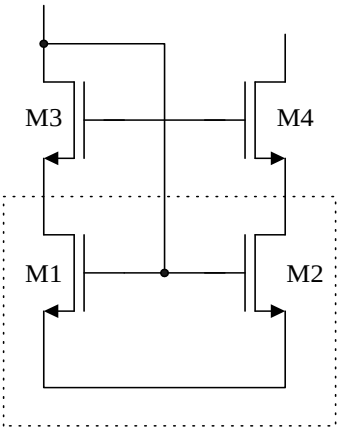




(a) (b)

Figure 5.1 (a) Two MOS transistor layout with L1=2λ and L2=6 λ (b) equivalent circuit





(a) (b)

Figure 5.2 (a) Current mirror transistors layout with L=2λ (M1 and M2) (b) equivalent circuit

Long channel transistors are made by using series of 3 short channel devise with gates shorted. Process gradient-induced mismatches are minimized by reducing the distance between centriods of matched devices [39]. This interdigitated MOS transistors configuration gives common centriod to the two transistors M1 and M2. Figure 5.3 also shows common centriod based 1kΩ high resistance poly based resistor. HIRES mask layer is used for resistor layout. This layer blocks poly2 doping, giving very high resistance [40]. Figure 5.4 shows final four quadrant multiplier layout.

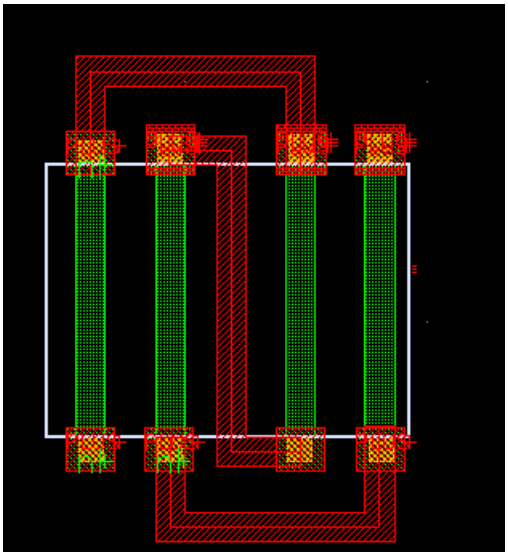


Figure 5.3 1kΩ high resistance poly based resistor layout

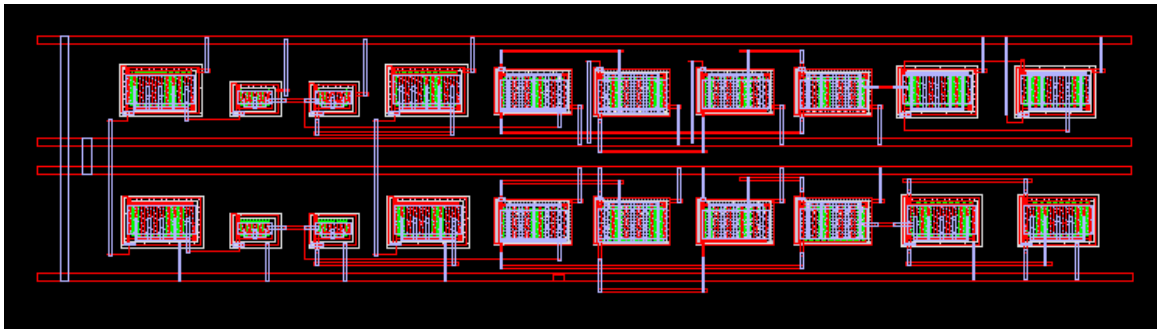


Figure 5.4 Four quadrant multiplier layout

CHAPTER 6 CONCLUSION

In this work, a MOS resistor is designed and simulated. This work attempted to design four-quadrant multiplier and divider using this MOS resistor. The limited input range, low linearity and higher power dissipation of these multipliers are analyzed by means of simulation results. A better approach for differential input four-quadrant multiplier is designed and verified by means simulations to provide better results. This multiplier as phase detector can detect phase difference between input signals over 360 degree range is illustrated by simulation. The design is able achieve ±2.2V input range with 0.07% THD @ 100 KHz with 1V p-p input signal. For bias current of 10μA, the power consumption was 0.242mW. The design layout was done using AMIS C5F 0.5μm technology using Cadence Virtuoso environment.

The layout of final design is verified by means of Assura (Verification tool) without any design kit. The design is cleared with respect to Design Rule Check (DRC) and Layout Versus Schematic (LVS) check. Because of setup problems with extraction tool, a post layout extraction and post layout simulations were not performed. Because of lack of post layout simulation results, the chip was not sent for fabrication. A second way of avoiding Assura and using NCSU design kit with MOSIS test run parameters is also underway. However, the design process was valuable and much was learned about multipliers and dividers. While the results obtained in simulations are not verified, the process of designing the chip from start to finish was valuable.

BIBLIOGRAPHY

[1] Bogdan M. Wilamowski, "VLSI Analog Multiplier/divider Circuit," *International Symposium on Industrial Electronics*, July, 7-10, 1998, Pretoria, South Africa, pp. 493-496.

[2] Eric A. Vittoz, "Analog VLSI signal processing: Why, where and how?", *International Journal on Analog Integrated Circuits and Signal Processing,* Vol. 6, No. 1, July 1994, pp. 27-44.

[3] Thomas H. Lee, *The Design of CMOS Radio Frequency Integrated Circuits,* Cambridge University Press, United Kingdom, 1998.

[4] M. Ismail, T. Fiez, *Analog VLSI Signal and Information Processing,* McGraw-Hill, Inc., United States, 1994.

[5] Dominique Coue and George Wilson, "A four quadrant sub-threshold mode multiplier for analog neural-network applications", *IEEE Transactions on Neural Networks,* Vol. 7, No. 5, September 1996, pp. 1212-1219.

[6] K. T. Lau, S.T. Lee, V.K.S. Ong, "Four-quadrant analog CMOS multiplier cell for VLSI signal and information processing", *IEE Proceedings on Circuits, Devices and Systems,* Vol. 145, No. 2, April, 1998, pp. 132-134.

[7] J. Ramirez-Angulo, S. Thoutam, A. Lopez-Martin and R.G. Carvajal, "Low-voltage CMOS Analog Four-quadrant multiplier based on flipped voltage followers", *International Symposium on Circuits and Systems,* 2004, Vol. 1, pp. 681-684.

[8] S. Soclof, *Applications of Analog Integrated Circuits,* Prentice Hall, 1985.

[9] R. Jacob Baker, Harry W. Li and David E. Boyce, *CMOS Circuit Design, Layout and Simulation,* Prentice Hall, 1998.

[10] B. Gilbert, "A precise four-quadrant multiplier with sub nanosecond response," *IEEE Journal of Solid State Circuits,* Vol. 3, No. 4, December 1968, pp. 365-373.

[11] Gunhee Han and Edgar Sanchez Sinencio, "CMOS transconductance amplifiers: A Tutorial", *IEEE Transactions on Circuits and Systems-II,* Vol. 45, No. 12, December 1998, pp. 1550-1563.

[12] Paul R. Gray, Paul J. Hurst, Stephen H. Lewis and Robert G. Meyer, *Analysis and Design of Analog Integrated Circuits,* John Wiley & Sons Inc., 2001.

[13] M. Ismail and D.Rubin, "Improved circuits for the realization of MOSFET-capacitor filters", *Proceedings of IEEE International Symposium on Circuits and Systems,* San Jose, May 1986, pp. 1186-1189.

[14] S. Szczepanski and S. Koziel, "1.2V Low-power four-quadrant CMOS transconductance multiplier operating in saturation region", *International Symposium on Circuits and Systems,* Vol. 1, 2004, pp. 1016-1019.

[15] A. Pesavento and C. Koch, "A wide linear range four quadrant multiplier in sub-threshold CMOS", *Proceedings of IEEE International Symposium on Circuits and Systems,* Vol. 2, July 1999, pp. 240-243.

[16] Bogdan M. Wilamowski, "VLSI analog multiplier/divider circuit", *IEEE International Symposium on Industrial Electronics,* Vol. 2, July 1998, pp. 493-496.

[17] Dominique Coue and George Wilson, "A four quadrant sub-threshold mode multiplier for analog neural network applications", *IEEE Transactions on Neural Networks,* Vol. 7, No. 5, September 1996, pp. 1212-1219.

[18] C. Toumazou, F.J. Lidgey, D.G. Haigh, *Analog IC design: The Current-Mode Approach,* IEE circuits and systems series 2, 1998.

[19] E. Seevinck and R.J. Wiegerrink, "Generalized translinear circuit principle", *IEEE Journal on Solid-State Circuits,* Vol. 26, No. 8, August 1991, pp. 1098-1102.

[20] Antonio J. Lopez-Martin and Alfonso Carlosena, "Current-mode multiplier/divider circuits based on MOS translinear principle", *Journal on Analog Integrated Circuits and Signal Processing,* 2001, Vol. 28, No. 3, pp. 265-278.

[21] Weixin Gai and Hongyi Chen, "A current-mode analog multiplier based on translinear principle", *4th International Conference on Solid-State and Integrated Circuit Technology,* October 1995, pp. 196-198.

[22] Carlos A. De La Cruz-Blas, Antonio Lopez-Martin and Alfonso Carlosena, "1.5-V MOS translinear loops with improved dynamic range and their applications to current-mode signal processing", *IEEE Transactions on Circuits and Systems-II,* Vol. 50, No. 12, December 2003, pp. 918-927.

[23] Niksa Tadic and Desa Gobovic, "A voltage-controlled resistor in CMOS technology using bisection of the voltage range", *IEEE Transactions on Instrumentation and Measurement,* December 2001, Vol. 50, No. 6, pp. 1704-1710.

[24] Mohammed Ismail, Terri Fiez, *Analog VLSI Signal and information processing*, McGraw-Hill Inc., 1994.

[25] M. Banu and Y. Tisvidis, "Floating voltage controlled resistors in CMOS technology", *Electronic Letters*, 1982, Vol. 18, pp. 678-679.

[26] K.M. Al-Ruwaihi, "A floating voltage-controlled linear resistor and its application to active RC filters", *International Journal on Electronics*, 1997, Vol. 82, No. 5, pp. 483-498.

[27] G. Moon, M.E. Zaghloul and R.W. Newcomb, "An Enhancement-mode MOS voltage-controlled linear resistor with large dynamic range", *IEEE Transactions on Circuits on Systems*, October 1990, Vol. 37, No. 10, pp. 1284-1288.

[28] S. Tantry, T. Oura, T. Yoneyama and H. Asai, "A low voltage floating resistor having positive and negative resistance values", *Asia-Pacific Conference on Circuits and Systems*, 2002, Vol. 1, pp. 347-350.

[29] H. O. Elwan, S. A. Mahmoud and A.M. Soliman, "CMOS voltage controlled floating resistor", *International Journal on Electronics*, 1996, Vol. 81, No. 5, pp. 571-576.

[30] C. Y. Wu and C.H. Chen, "A new analog multiplier-divider with compact structure for cmos neural network applications", *IEEE Asia-Pacific Conference on ASIC*, August, 1999.

[31] W. Liu, S. I. Liu and S. K. Wei, " CMOS current-mode divider and its applications", *IEEE Transactions on Circuits and Systems-II*, March 2005, Vol. 52, No. 3, pp. 145-148.

[32] D. Gosh and D. Patranabis, " A simple analog divider having independent control of sensitivity and design conditions", *IEEE Transactions on Instrumentation and Measurements*, June 1990, Vol. 39, No. 3, pp. 522-526.

[33] Th. Laopoulos and C.A. Karybakas, "A simple analog division scheme", *IEEE Transactions on Instrumentation and Measurements*, August 1991,Vol. 40, pp. 779-782.

[34] I. Baturone,S. Sanchez-Solano and J.L. Huertas, "A CMOS current-mode multiplier/divider circuit", *Proceedings of International Symposium on Circuits and Systems*, June 1998, Vol.1, pp. 520-523.

[35] Richard C. Jaeger and Travil N. Blalock, *Microelectronic circuit design*, McGraw-Hill publishers,2003.

[36] Phillip E. Allen, Douglas R. Holdberg, Allen, *CMOS Analog Circuit design*, Kluwer Academic Publishers, 2002.

[37] Tanno K., Ishizuka O. and Tang Z. “Four-quadrant CMOS current-mode multiplier Independent of device parameters”, *IEEE Transactions on Circuits and Systems II,* May 2000, Vol. 47, No. 5, pp. 473-477.

[38] J.J. Tang, *A 2.4GHz CMOS four port mixer and analog multiplier,* Thesis at Hong Kong university of science and technology, August, 1998.

[39] Alan Hasting, *Art of analog layout,* Prentice Hall publishers, 2002.

[40] C5X 0.5μm AMIS technology design rules.