The Effects of Mechanical Stress on Semiconductor Devices

by

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Abstract

Mechanical strains and stresses are developed during the fabrication, assembly and packaging of the integrated circuit (IC) chips. Sources include processes such as shallow trench isolation, wafer backgrinding and dicing, TSV formation, die attachment, and first level packaging (e.g. encapsulation). These stresses and strains cause parametric shifts in the electronic components which change their electrical performance, and can result in devices operating out of specification.

The influence of mechanical stress on devices that operate using conduction of majority carriers is often modeled using piezoresistive theory. Extensive investigation has been done on mechanical stress effects on resistors fabricated on integrated circuit chips. In addition, test chips using resistor sensors have been successful in measuring die stresses for various packaging architectures. Stress effects on diodes, field effect transistors (FETs), van der Pauw structures, and CMOS sensor arrays have also been well characterized. The influences of mechanical stress/strain on bipolar junction transistors (BJT) are more complicated than those for other devices. This is because bipolar transistors feature conduction in both n-type and p-type regions, as well as conduction of minority carriers.

In prior studies, the influence of stress on BJT behavior has been described using the so-called piezojunction effect, which includes variations in the minority carrier mobility and the intrinsic carrier concentration. Whereas the piezoresistive effect

describes the variation of the resistivity components of the majority carriers with applied mechanical stress, the piezojunction effect governs the dependence of the minority carrier conduction on stress.

In BJTs, both bandgap and the attendant mobility variations influence various parameters including saturation current I_S, collector current I_C, base current I_B, and DC current gain β. Analog circuits containing bipolar transistors are also affected by stress, including precision voltage references, op-amps, A/D and D/A converters, etc. Experimental data for resistors and resistive channels of CMOS devices have demonstrated that their changes in their electrical characteristics can be explained by linear piezoresistive theory that includes only first order terms. However, most data for bipolar transistors in the literature illustrate non-linear variations of saturation current, collector current, and base current with applied uniaxial stress.

In this dissertation, mechanical stress related phenomena for several electronic devices including resistors, field effect transistors, and bipolar transistors have been explored. In the first portion of this work, measurement and other errors have been investigated for multi-element resistor sensor rosettes on (111) silicon. Resistors are widely used in the semiconductor industry as silicon stress sensors. They are fabricated on the surface of test chips and then used to extract stresses over the die surface. To make such measurements, the user must measure the changes in the resistances of the sensors, the piezoresistance coefficient values, and the temperature. These experimental measurements inherently contain certain uncertainties in their values. In this work, an error analysis was performed, which included uncertainties in measurements and calibration constants. This sensitivity analysis included direct calculations of the

sensitivities of the extracted stresses to uncertainties in the calibrated piezoresistive coefficients, measured sensor resistances, and the measured temperature.

In the second portion of this work, calibration of field effect transistor (FET) stress sensors was investigated. Stress effects on FETs can be modeled using piezorsistive theory similar to resistors. In this dissertation, the dependence of the piezoresistive coefficients on the drain current operating point of the FET device has been explored. Both the PMOS and NMOS devices demonstrated strong drain current dependencies. The piezoresistance coefficients were also expressed as a function of carrier mobility in the channel region.

In the third and final portion of this work, stress effects on bipolar junction transistors have been investigated. The primary goal of this research topic was to understand and model the impact of mechanical stress on bipolar transistors and precision analog circuits. Although piezojunction coefficients have previously been proposed in the literature to describe the variation of transistor saturation currents under stress, there has not been a comprehensive modeling effort for use in circuit simulation. In this dissertation, a basic charge-control model for the transistor has been proposed that adequately captures the macroscopic impact of stresses on the BJT device characteristics. In addition, the developed approach has been used to model the influence of stress on analog circuits employing these devices. This work has provided an understanding of the dominant effects of stress on the basic BJT model parameters.

To support the proposed models, the response of BJTs to the controlled application of mechanical stress has been characterized experimentally. Test structures have been utilized to characterize the stress sensitivity of vertical bipolar devices

fabricated on both (100) and (111) silicon wafers. Uniaxial normal stresses were applied using a four-point-bending fixture, and changes in the electrical performance of the BJTs were observed. The experimental data acted as a benchmark in the development of the theoretical model, and the developed stress equations for the BJT have been shown to have excellent correlations with the experimental results. Based upon the current gain and saturation current data, a methodology has been developed for properly separating the contributions of intrinsic carrier concentration and minority carrier mobility on the overall stress induced variations of the collector current and current gain of the BJT. In the future, the developed formulations can be applied to theoretically optimize transistor design, placement, orientation, and processing to minimize the impact of fabrication and packaging induced die stresses.

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CHAPTER 1

INTRODUCTION

1.1 Advancement of the Semiconductor Industry

The semiconductor industry at present is utilizing ultra-large-scale integrated circuit (IC) technology and system-in-package technology to achieve smaller feature sizes, higher transistor performance, more speed, and reductions in cost. We are living in the world of high performance computers, tablets, high speed communication through cellular phones, wireless application modules, GPS, PDAs, hand-held devices, and image capturing devices. These are all possible due to tremendous technological developments in the semiconductor industry such as the invention of integrated circuits and scaling of semiconductor devices. The scaling down of transistors follows the famous empirical observation by Gordon Moore, co-founder of Intel Corporation, which states that number of transistors on a chip doubles approximately every two years (Fig. 1.1) with improved performance from the previous technology node and reduced cost per transistor [1]. This observation known as “Moore’s Law”, acts as a guidance for the semiconductor industry to set goals for the development and engineering of the next technology node. With each improvement, silicon technology downscaling results in more transistors on a single chip and an increase in computational capability.

For last 40 years, down scaling of the minimum feature size from 10 μm to 10 nm has been the predominant factor for increasing device density and lowering the cost

of the integrated circuit chips. However, below 90 nm technology, planer transistor technology has reached its practical downsizing limits [2]. To maintain Moore's law trajectories of performance improvement and to meet International Technology Roadmap for Semiconductors (ITRS) targets, the semiconductor industry has adopted several new innovative technologies and new materials such as strained silicon, multigate devices, strained SiGe technology, as well as introducing high-K dielectric materials, metal gates and so on. These new technologies and materials pose new challenges and complexity for critical dimensions, mobility, variability, leakage, and reliability, greatly increasing the capital cost and risk.

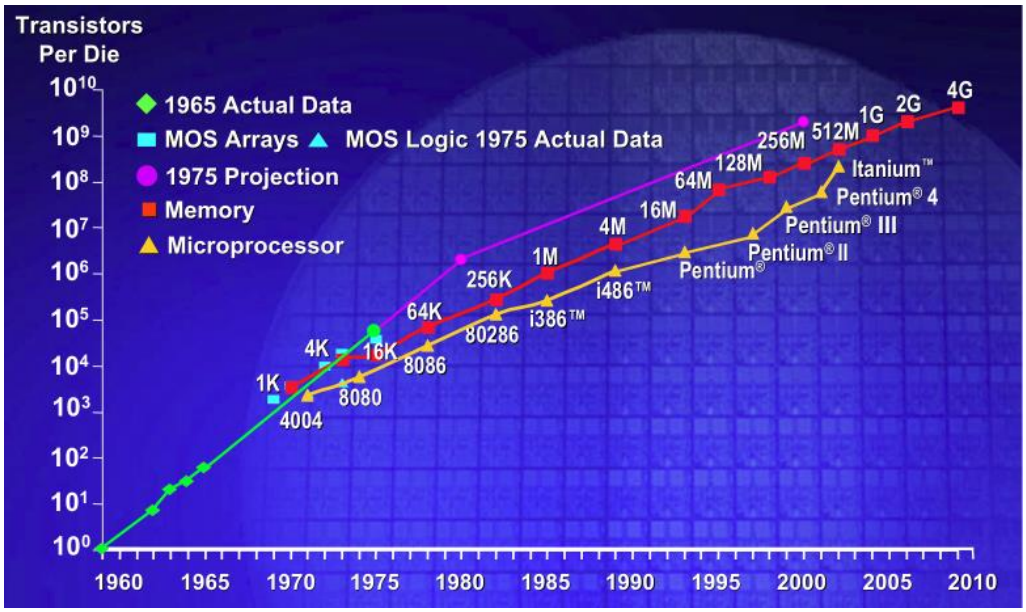


Figure 1.1 Moore's Law for Memory Chips and Microprocessors
(http://www.cmg.org)

1.2 Mechanical Stress in Semiconductor

Silicon integrated circuits are complex structures that consist of complicated assemblies of various materials that are deposited, implanted, and grown at different

temperatures upto 1200˚ C. IC fabrication involves various processes such as silicon crystal growth, photolithography, etching, thermal oxidation, deposition, and implantation, etc. After fabrication, packaging of the ICs is performed using a wide range of materials that provide structural reliability, electrical connection of the die to the PCB, paths for heat dissipation, physical protection of the circuit, and environmental isolation from mechanical and chemical hazards.

Mechanical strains and stresses are developed during Ic fabrication and packaging steps. These stresses are often due to thermal expansion coefficient mismatches between the wide variety of materials used in packaging. Other sources of stress generation include intrinsic stresses in the deposited films, thermal oxidation of silicon, and implantation of materials that have different lattice constants from that of silicon. Large localized stresses can also occur in the silicon active area near the edges of the deposited thin films, near embedded structures such as trenches, and in regions of material growth such as local oxidation. Mechanical stress generating sources include processes such as shallow trench isolation, wafer back grinding, dicing, TSV formation, die attachment, and first level packaging (e.g. encapsulation) (Fig. 1.2). The demand for smaller geometric circuits and increased circuit density make the stress distributions in silicon die more complicated due to the complexity of device patterns. Sources of mechanical stress in integrated circuit chip are reviewed in the references [3-5].

1.2.1 Fabrication Induced Thermal Stress

Materials expand when heated and contract when cooled down. During fabrication and also during packaging, interaction of the different materials that constitute the assembly, cause thermal stress to develop due to high temperature processing steps

and also temperature cycling during operation. Such thermal stresses develop due to thermal expansion coefficient mismatches of the various utilized materials. Table 1.1 shows a list of thermal expansion coefficients of the materials typically used in silicon fabrication and packaging.

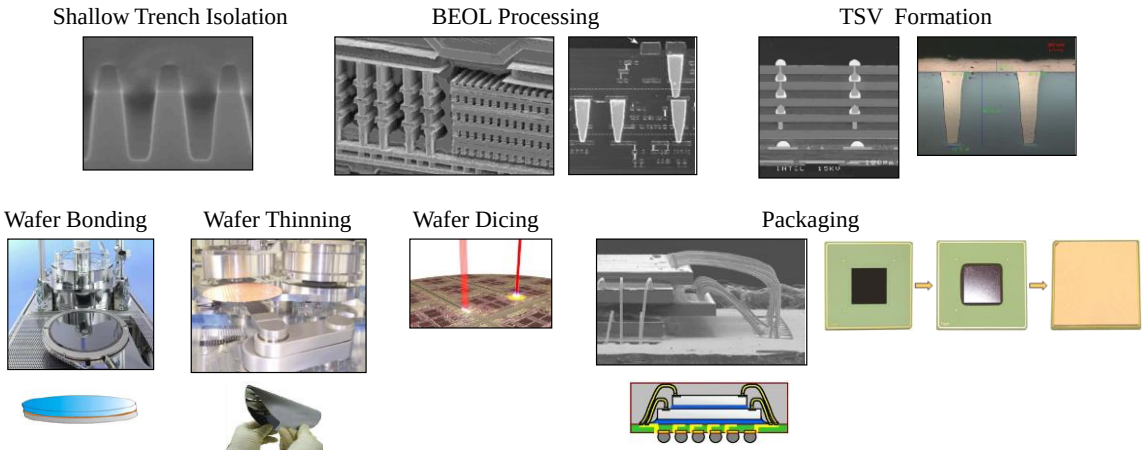


Figure 1.2 Various Sources of Mechanical Stress Generation in an IC

Table 1.1 Thermal Expansion Coefficients of Some Materials Used in the Semiconductor Industry

Material	Thermal Expansion Coefficient, $(10^{-6})1/C$
Silicon	2.6
Silicon Oxide, SiO_2	1
Silicon Nitride, Si_3N_4	3
Polysilicon	3.05
Aluminum	24
Copper	17
Pb-Sn Solder	24
Polyamide	40-50
Silica filled Epoxy	14-24
Ag-filled Epoxy	32

Localized stresses can be caused by embedded structures such as shallow trench isolations (STI) and through silicon vias (TSV). In order to achieve higher packing density and improve electrical performance, the electronic devices on the chip are made smaller and packed closer together. Such scaling requires that the devices are electrically isolated from each other so that they don't interfere with each other during operation. STIs are used in ICs to provide electrical isolation between adjacent semiconductor devices.

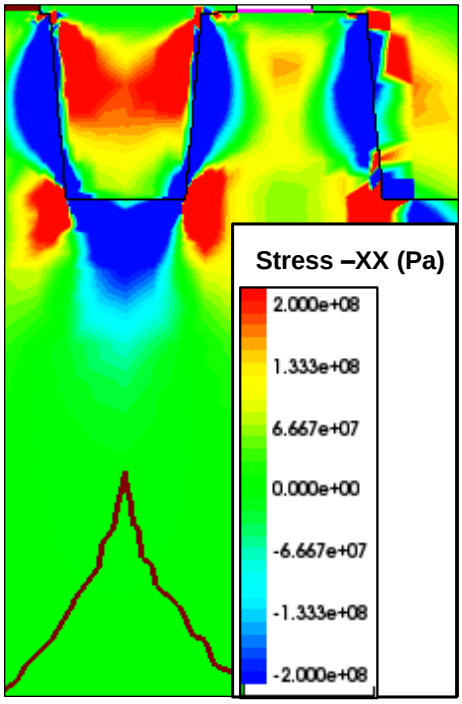


Figure 1.3 Stress Distribution Near a Shallow Trench Isolation

The process steps to form STIs usually consist of trench formation using photolithography and etching, depositing silicon dioxide in the trenches, and finally planarization of the surfaces using chemical mechanical polishing techniques. The deposition of the dielectric material in the trench is usually performed at high temperatures typically around 700-800˚ C [3]. At the deposition temperature, both the

silicon and oxide are stress free. As the assembly is cooled down to room temperature, the oxide contracts less than silicon due to the differences in the coefficients of thermal expansion (CTE). This can result in high stresses on the order of several hundred of MPa between the isolation edge of the silicon and oxide (Fig. 1.3) [6]. The stress magnitudes drop as the distance from the isolation edge increases [6]. The mechanical stresses generated from STIs have been observed to increase with downsizing of the devices.

Another such embedded feature that poses similar problem is the through silicon via (TSV). The use of three-dimensional integrated circuit chips (stacking of chips) is the recent trend in semiconductor industry to accommodate more functionally in smaller space, improve power efficiency, and enhance performance [7]. TSVs have been introduced in three-dimensional integration of chips to address the issue of increased number of I/O from the chip. With the wirebonding or solder ball interconnects rapidly reaching their practical density limits with the scaling of devices and increased device density, TSV technology with interconnects embedded in the chip itself, have emerged as a potential solution.

The fabrication steps for TSV usually are as follows: (i) etching silicon to form a cylindrical through hole via, (ii) deposition of a seed layer on the side walls (iii) filling the via with a conducting material such as copper. However, the differences in the thermal expansion coefficients of the silicon and copper can cause significant stresses to develop as shown in Fig. 1.4. These thermal stresses can cause the delaminations of the copper, as well as degradations of the electrical performance of the transistors placed near the TSV due to changes in mobility [8, 9].

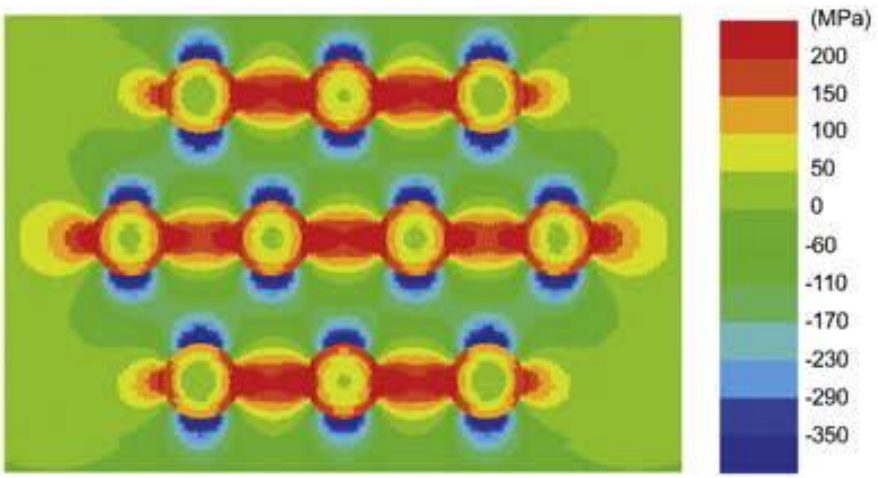


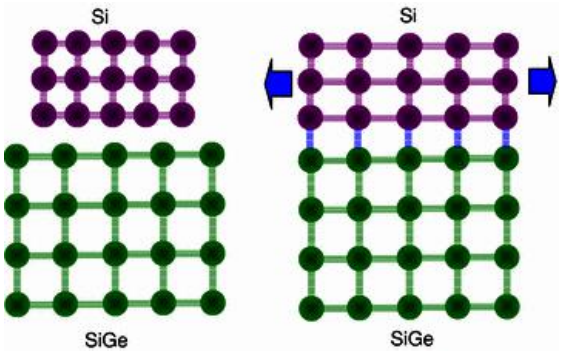
Figure 1.4 Finite Element Simulation of the Horizontal Normal Stress Distribution Near TSVs (Top View). [8]

1.2.2 Stress Due to Lattice Mismatch

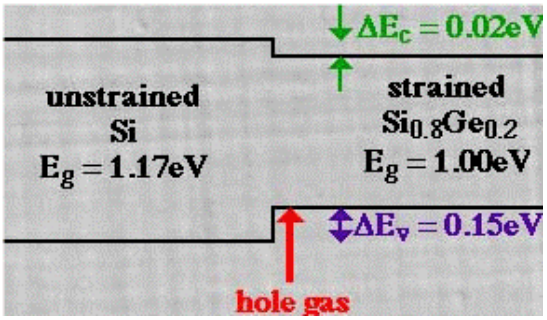
With the scaling of silicon based devices approaching its downsizing limits, researchers are actively looking for alternative methodologies to improve the performance of the electronic devices. One such method widely used in recent times is strain engineering or bandgap engineering, which mainly consists of adding other materials to the silicon lattice to form silicon germanium (SiGe) or silicon carbide (SiC) [10].

Adding germanium or carbon to the silicon substrate causes the band gap to change. As shown in Fig. 1.5, there is a mismatch of the lattice constant of these materials (silicon and germanium lattice constants are 1.17 and 1.22 Å, respectively). The germanium lattice is 4.2% larger than that of silicon, and the diamond lattice is 45% smaller than silicon. Therefore, a thin film of silicon epitaxially grown on top of SiGe or SiC becomes strained due to the lattice mismatch [3]. This strain that is intentionally induced in the silicon lattice enhances the performance of the transistors by improving the mobility of the carriers. Such strain engineering is the latest trend that has been

adopted in state-of-the-art transistor technology to keep pace with Moore's law, along with other technological advancements.



(a)



(b)

Figure 1.5 (a) Strain Induced due to the Lattice Mismatch Between Silicon and Silicon-Germanium
(b) Difference in Bandgap between Silicon and Silicon-Germanium [11].

1.2.3 Intrinsic Stress

Various semiconductor fabrication parameters such as thin film growth rate, thin film thickness, temperature processing profiles, etc. can cause intrinsic stresses to develop in silicon [5]. Deposition and growth of films cause unintentional stress to develop. For example, localized large stress can be developed when a film is deposited on a nonplaner surface [12]. Also, a substantial amount of stress can be developed during the thermal oxidation of silicon, and this stress can cause discontinuities at the silicon-oxide interface. One reason this stress develops is that the volume of the oxide that is grown is 2.2 times more than that of the silicon. As a result, compressive stress builds up in the

oxide [3]. During fabrication processes such as oxidation of trench sidewalls or the selective oxidation of silicon nitride layers, stresses develop due to the volume expansion associated with oxide formation. Stresses also develop when oxidation is done on a nonplanar silicon surface. Convex or concave corners cause the oxidation layer to be strained, resulting in a buildup of stress in the oxide. Oxidation induced stresses are a common concern due to the pervasive use of thermal oxidations in silicon device fabrication.

Intrinsic stress development in films during silicon fabrication is often intentionally implemented in current technology nodes to improve the performance of the devices. One such example is strained Contact-Etch-Stop-Layer (sCESL) technology as shown in Fig. 1.6. Improvement of the performance of the transistors is accomplished by utilizing the internal stresses developed in the silicon during silicon nitride passivation processing.

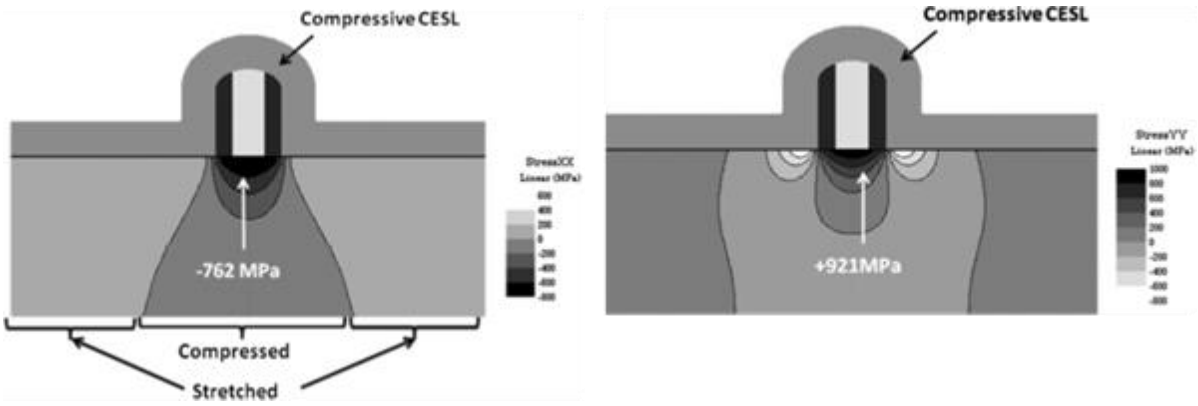


Figure 1.6 Stress Distribution due to Compressive CESL in a PMOS (left), Stress Distribution due to Compressive CESL in a NMOS (right) [3]

1.2.4 Electronic Packaging Induced Stress

After semiconductor fabrication, packaging of the chip is performed. Packaging is a field which involves many disciplines, as shown in the Table 1.2 [13], and involves

complex engineering to establish links between the circuits on the chip and the system. An electronic package is a composite assembly with different materials and geometrical configurations, where one or more silicon chips are placed in an enclosure. The choice of packaging for a particular product is driven by the demands for higher performance, increased density of devices on the chip, increased reliability and cost reduction.

Table 1.2 Packaging Disciplines [13]

Discipline	Problems addressed
Chemical Engineering	Chemical Process Systems
Electrical Engineering	Electronics and Electrical Design
Industrial Engineering	Cost and Production Analysis
Mechanical Engineering	Stress Analysis, Mechanical Design Tools
Materials Engineering	Materials Selection, Metallization Process, Wirebonding/ Solder Interconnects
Physics	Electrical, Thermal and Mechanical Characteristics
Thermal Engineering	Heat Transfer

Fig. 1.7 shows the evolution of packaging technologies over the last few decades, which involves the use of various packaging architectures. This packaging road map for Texas Instruments is typical of those used by other companies. Packaging can be categorized in different ways; such as ceramic and plastic molded chip carriers. They can also be classified in terms of their interconnection configuration, such as Quad Flat Pack (QFP), Pin Grid Array (PGA), Ball Grid array (BGA) and Flip Chip (FC).

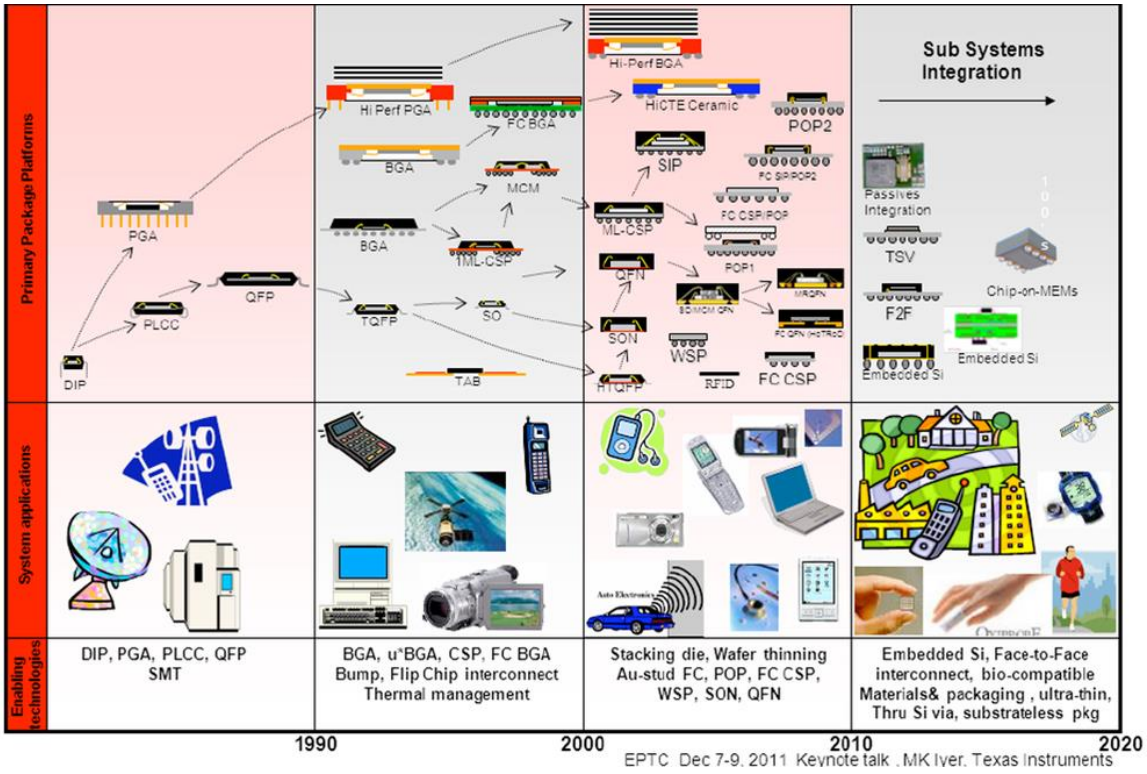


Figure 1.7 TI Packaging Technology Trends
(http://www.monolithic3d.com/blog/archives/04-2012)

Fig. 1.8 illustrates a typical packaging hierarchy. One or more chips packaged in protective chip carriers comprise the first level of packaging. The chip carriers usually contain protective encapsulation materials such as ceramic or plastic as well as a leadframe or substrate to provide a path for electrical connection to the outside system. Wirebonding, solder interconnections, or tape automated bonding are technologies used to electrically connect the chip to the leadframe or the substrate. The Printed Circuit Board (PCB) containing the mounted chip carriers is referred to as the second level of packaging. The chip carriers are connected to the PCB using either Plated Through Hole (PTH) or the Surface Mount Technology (SMT). The third level packaging is the mother board, where several printed circuit boards are connected together [14].

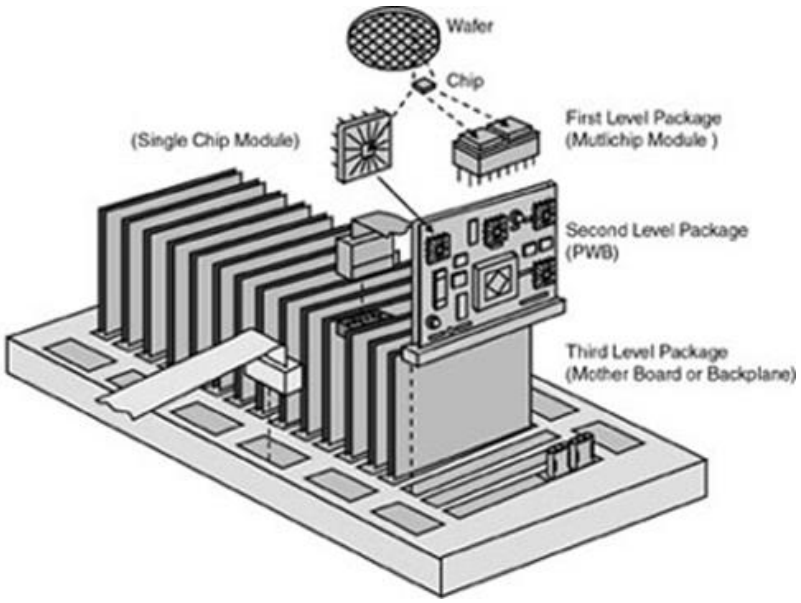


Figure 1.8 Packaging Hierarchy
(http://www.ewh.ieee.org/soc/cpmt/press/pressimage.html)

Electronic packages consist of different materials having different geometries with different mechanical properties. Elevated temperature processing of these materials such as die attachment to the leadfame or substrate, plastic encapsulation, wirebonding, and solder reflow causes thermal stresses to develop because of the mismatches in the coefficients of thermal expansion of the different materials in the package. The heat dissipated by high power devices can also cause thermal stresses to develop. For example, Fig. 1.9 shows a typical CBGA packaging architecture for a high performance microprocessor that consists of various materials in a complex geometrical configuration. As indicated, the thermal expansion coefficients are widely different for the various materials.

When systems are turned off, the packages cool down and the materials comprising the package contract at different rates. Repetitive cooling and heating results

in thermal cycling, which causes fatigue loading of the package. Mechanical loadings can also be caused by human interactions, such as shock/drop events and loads transferred to the package from the contact with the printed circuit board. All the above mentioned loadings cause complex biaxial (two-dimensional) or triaxial (three-dimensional) stresses to develop in the package. Excessive stresses can affect the reliability of electronic modules.

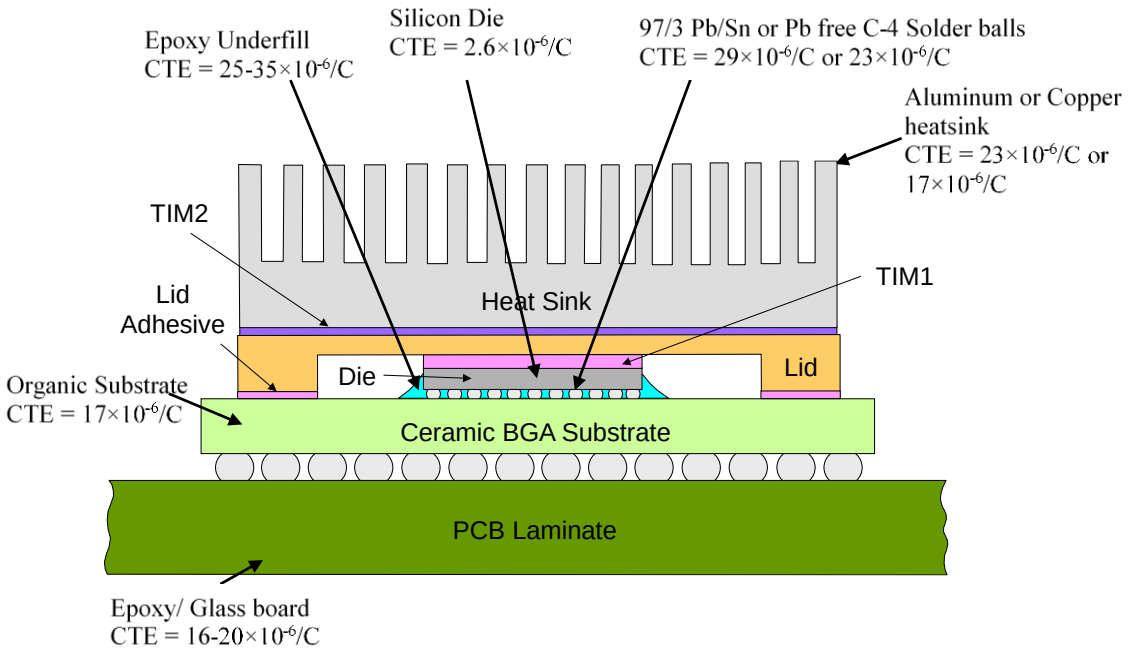


Figure 1.9 Typical CBGA Packaging Architecture

1.3 Impact of Mechanical Stress in Electronics

The possible stress generating processes in the fabrication and packaging of a silicon chip have been discussed above. The impact of these stresses on the performance of electronic devices will now be discussed. Mechanical stress is considered both desirable and undesirable in semiconductor industry. Before the year 2000, stress was

always considered to be undesirable in the processing and fabrication of the die, because it was one of the reasons for defects, delamination, and performance degradation. As a consequence, stresses were avoided at any cost [6, 15-17]. However, during the last decade, stress has been intentionally introduced in selective regions of the devices to enhance the circuit performance [18-21], although stress induced failures are still considered unwanted.

Undesirable stresses are an unavoidable product of the fabrication or packaging of semiconductor integrated circuits. When the stress in the silicon exceeds the material strength, defects such as dislocations or slip patterns can occur in the silicon crystal [3]. During oxidation and ion implantation steps, nucleation of dislocations occur [12]. Dislocations can grow and move to other parts of a device boundary with further accumulation of stress at later stages of fabrication and packaging that adversely affects the circuit performance of the chip.

For area array packaging architectures, thermal cycling imposes the greatest reliability challenge. As shown in Fig. 1.9, different components in packaging often have different thermal expansion coefficients, different elastic moduli, and the components are of different geometrical shapes. Thermal stresses that are developed due to these differences in material properties can cause delaminations to occur at the component interfaces due to repeated thermal cycling loadings. In addition, fatigue and creep under stress can occur over a period of time, which can cause performance of the electronic system to degrade. Fig. 1.10 shows typical failure sites and failure modes for a typical flip chip package that occur as a consequence of mechanical stresses during thermal cycling.

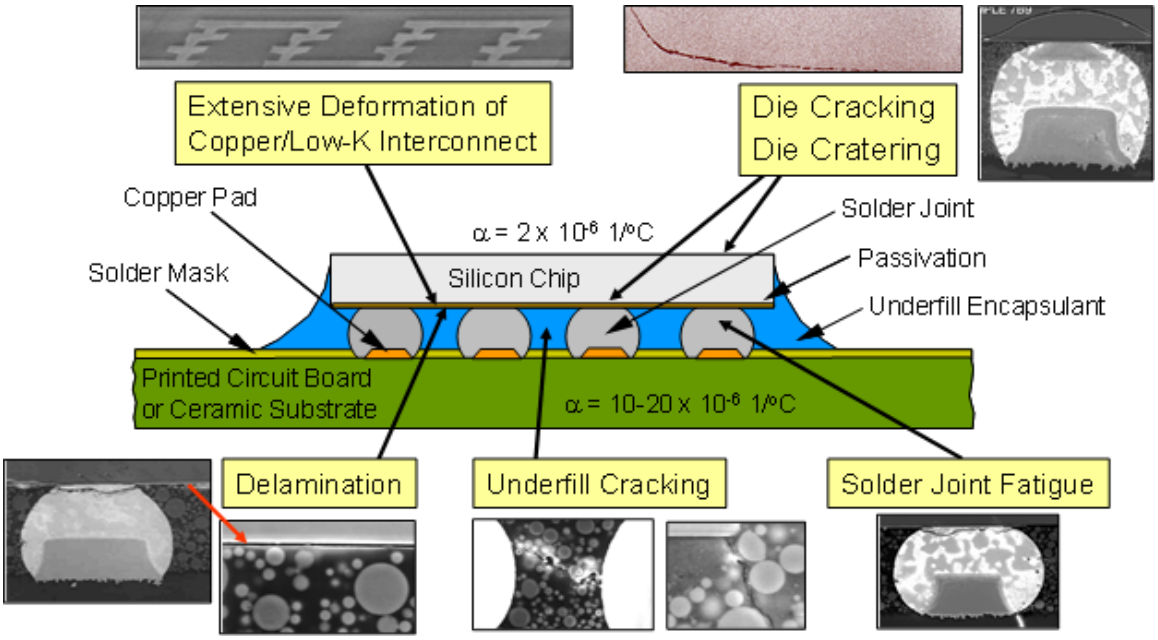


Figure 1.10 Flip Chip Packages Potential Fail Locations

Other than structural failure of the packages, thermal stress can also adversely affect the performance of the devices on the chip. When stress is applied to a semiconductor material, the electrical resistivity of the material changes, and such an effect is called piezoresistance. In semiconductor materials such as silicon, stress alters the positions of the conduction and valence bands, changing the band structure and band gap. These effects change the carrier mobility of the device that results in change in electrical resistivity of the material. Such changes in bandgap and carrier mobility cause parametric shifts in the electronic devices and can cause device performance to degrade.

Although the semiconductor industry has considered stress as unwanted for 40+ years, the industry has now used stress effects to improve device performance by changing carrier mobility and to boost the performance of the transistors on a silicon chip. With the scaling of transistors reaching their practical minimum size limit due to the

leakage current at small gate lengths, the industry has been exploiting new technological solutions to keep pace with Moore's law beginning at the 90 nm technology node. To continue with projected improvements in performance without changing the transistor size, the semiconductor industry has opted to apply stress/strain into selected regions of the device. Examples include the channel and source/drain in Metal-Oxide-Semiconductor (MOS) transistors and in the base region of bipolar transistors. This intentional inclusion of stress into silicon lattice, known as strain engineering or bandgap engineering, is being widely implemented in nearly all submicron technology nodes. Strained silicon technology is based on changing of the band structure of silicon due to the presence of stress along appropriate crystallographic directions, and has been shown to result in remarkable performance gain [22].

The beneficial effect of stress on the electron and hole mobilites has been known since the 1950's [23]. However, the industry did not start researching implementations of this phenomena until the 1980's [24, 25]. As mentioned above, improvements are often obtained through straining the lattice of silicon by overgrowing silicon epitaxially above a relaxed silicon-germanium ($Si_{1-x}Ge_x$) structure to significantly increase electron mobility [11, 26]. Epitaxial growth of silicon on SiGe substrate causes the silicon to assume the larger lattice constant of SiGe, and thus causes the silicon to be stressed biaxially over the whole wafer. This technique of biaxially stressed silicon cannot be used for both n-type (NMOS) and p-type (PMOS) transistors, since NMOS needs to be stretched while PMOS should be compressed for performance enhancement. Thus, the biaxial stress/strain technique is only beneficial for n-type transistors. Several alternative uniaxial stress techniques have been developed for local stress generation. These

techniques include nitride contact etch stop liner [19], embedded SiGe growth in the source and drain contacts [27], and even from shallow trench isolation [28] for high volume manufacturing. Another method of stress generation to enhance performance is to use tensile or compressive layers grown on top of a transistor depending upon whether the transistor is of n-type or p-type. This method is called Dual Stress Liner (DSL), and involves tensile layers of silicon-nitride grown on n-type transistors, and compressive layers placed on top of p-type transistors. Using this method, the drain current can be increased by up to 20% in p-type and 11% in n-type transistors [29, 30]. Some of these local stress generating techniques are used simultaneously. For example, a stressed nitride cap can be used along with embedded SiGe in the source and drain regions to achieve even greater performance improvement [30, 31].

1.4 Objectives of this Research

The motivation of this work is to investigate issues related to mechanical stress in semiconductor devices. The semiconductor devices investigated in this research are resistors, field-effect transistors (FETs), and bipolar junction transistors (BJTs). This dissertation also addresses the impact of mechanical stress on precision analog devices and circuits. Three topics will be covered in this dissertation as outlined below:

1. Perform an error analysis for piezoresistive stress sensors used in flip chip packaging.
    - The objective of this work was to understand how errors made in the measurements influence the stress extractions made subsequently with multi element sensor rosettes on (111) silicon.

- A sensitivity analysis has been performed where direct calculations of the sensitivities of the extracted stresses to uncertainties in the piezoresistive coefficients and the measured temperature have been made.

2. Determination of the operating point dependence of the piezoresisitve coefficients of CMOS Stress sensors on (100) silicon.
   - The drain current dependence of the piezoresistive coefficients of NMOS and PMOS field-effect transistors has been charaterized.
3. Develop a fundamental understanding required for characterization, modeling, and mitigation of the impacts of mechanical stress on the performance of precision analog devices (bipolar transistors).
   - Measure and quantify the effects of stress on precision analog devices and circuits.
   - Develop a theoretical model based on the experimentally obtained to predict the stress induced changes in the electrical characteristics of bipolar transistors.

1.5 Organization of the Dissertation

This dissertation focuses on issues related to changes in electrical characteristics of resistors, field effect transistors (FETs), and bipolar junction transistors (BJTs) caused by presence of mechanical stress. The presentaton is organized into the following chapters:

Chapter 1: The introduction chapter discusses the sources of mechanical stress in integrated circuits (ICs). The sources include various processes during

fabrication and packaging of the IC. The impact of mechanical stress on ICs is also discussed.

Chapter 2: A literature review on piezoresistivity, the piezojunction effect, and the application of piezoresistive effect to sensors are presented

Chapter 3: Multi-element resistor stress sensor rosettes on (111) silicon are discussed and the effects of uncertainties in the measured values of the piezoresistive coefficients, sensor resistances, and the temperature on the measurement results have been explored. Direct calculations of the sensitivities of the extracted stresses to uncertainties in these parameters are presented.

Chapter 4: The capability of metal oxide semiconductor field-effect transistors (MOSFET) to be used as stress sensors is discussed, and the dependence of the piezoresistance coefficients on the drain current of the FET device is investigated.

Chapter 5: Experimental methods for characterizing the effects of mechanical stress on bipolar transistor device characteristics are discussed and experimental results are presented.

Chapter 6: A theoretical model to predict the stress induced changes in bipolar junction transistor characteristics is developed, and then correlated with the experimental results discussed on the Chapter 5.

Chapter 7: The effects of stress on selected integrated analog bipolar circuits are explored and discussed.

Chapter 8: Summary and conclusions of the dissertation are presented

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

To achieve lower chip production cost, the semiconductor industry is working towards incorporating more transistors per chip by downsizing the transistors and improving performance of the transistors hence enhancing computational capability. As the scaling down of the dimensions of the devices on chip continue, the stress patterns in the chip are becoming more complex. Moreover packaging of the chip further exacerbates the stress condition in the chip which may cause parametric shifts in device performance, interconnect failure and damage yo the die and package. Therefore, stress evolution during fabrication and packaging is a major reliability issue and great emphasis is given in semiconductor industry on the studies of the effect of stress on the electronic devices.

The stress effect on electronic devices such as resistors, field-effect transistors (FETs) and bipolar junction transistors (BJTs) are referred to as piezoresistive or piezojunction effects. Piezoresistance is a material property which causes electrical resistance of the material to change due to the application of mechanical stress. Stress/strain alters the symmetry of the semiconductor crystal and modulates the conduction mechanism in semiconductors which results in variation in resistivity of the material. The mechanical stress can be uniaxial tensile or compressive stress, hydrostatic

pressure, shear stress or a combination of these stresses. Depending on the semiconductor material and crystallographic axis along which the stress is applied, there can be an increase or decrease of the resistivity of the material. The piezoresistive effect is very well understood since extensive research has been conducted in this area. The change in the current of the p-n junction or the bipolar transistor due to the mechanical stress is referred to as the piezojunction effect. Based on piezoresistive and piezojunction property of silicon, micro-electro-mechanical-system (MEMS) sensors are designed and widely used as strain gauges, accelerometers, cantilever force sensors, pressure sensors etc. [32-36]. These sensors have the properties of high sensitivity, good linearity, small size, mechanical sturdiness, the benefits of mass production due to microelectronic fabrication techniques, and the ease of incorporation in standard IC technology [37].

2.2 Piezoresistive Effect

Widely used semiconductor materials silicon and germanium have a single cubic crystal structure and these materials are extensively used as piezoresistors. Smith in 1954 first studied the piezoresistive behavior of germanium and silicon material [23]. He conducted his measurements on lightly doped silicon and germanium samples and measured large piezoresistive coefficients for these semiconductor materials compared to metallic conductors. Smith's coefficient values still serve as a reference to the upper bound of these coefficients since as doping increases the value of piezoresistive coefficients decreases. Smith measured first order piezoresistive coefficients for cubic materials, which are reduced to three nonzero coefficients (π_{11}: longitudinal, π_{12}: transverse and π_{44}: shear) for silicon because of silicon's diamond crystal structure. The first utilization of the piezoresistive properties of germanium and silicon materials as

sensors to measure force, displacement and torque was done by Mason and Thurston in 1957 [38]. In their work they used bonded semiconductors as strain gauges to a test sample, cut along different crystallographic directions to maximize the longitudinal piezoresistive effect. In 1961, Pfann and Thurston talked about advantages of utilization of transverse and shear piezoresistive effects along with the longitudinal effect [39]. In their paper they discussed utilization of semiconductor strain gauges along different crystallographic directions on either (100) or (111) surface to measure resistance change of the gauges in terms of principal stresses, independent of the orientation of the gauge. They also proposed incorporating diffused piezoresistive materials instead of bonded strain gauges with a semiconductor force, torque or displacement sensing element. Kerr and Milnes further investigated piezoresistive characteristics of the semiconductor materials of a diffused layer on the semiconductor materials surface [40]. Tufte et al., in 1962 at Honeywell Research, were first to develop an integrated device using a piezoresistive pressure sensing diaphragm formed by impurity diffusion which had advantages over the bonded strain gauge diaphragm since the latter suffers from hysteresis and creep problems [41]. In a paper published in 1964, Tufte and Stelzer discussed experimental investigation of the effect of heavy doping and temperature on n-type silicon [42]. The change in hole mobility due to piezoresistive effects on a silicon p-type inversion layer was first studied by Colman et al [43].

The piezoresistive property of semiconductor has the disadvantages of nonlinearity and temperature sensitivity. Investigation of nonlinearity is important for the design of high precision sensors, since this nonlinearity must be avoided by selecting a particular crystallographic direction or using some compensating circuits. The

nonlinearity exhibits a temperature dependence. Several researchers addressed the nonlinearity of the semiconductor piezoresistance effect [33, 40, 44, 45], but they did not address the issue quantitatively. Yamada et al. discussed the detailed measurement of nonlinearity of p-type silicon diffused layers [46]. They proved that the third-order stress terms gives good estimation for the piezoresistance effect and also showed that the nonlinearity in the transverse mode is greater than the longitudinal nonlinearity. The nonlinear piezoresistance of both n-type and p-type diffused layer were studied for different stress and current directions by Matsuda and his coworkers [47, 48]. To incorporate nonlinearity in the piezoresistance effect, Lenkkeri included nine nonzero second-order piezoresistance coefficients for silicon along with the three first-order coefficients determined by Smith [49].

A graphical representation of anisotropy of the piezoresistance effect of silicon is represented by Kanda [50]. In his paper he plotted the longitudinal and transverse piezoresistance coefficients at room temperature as a function of the crystal direction for the (100), (110) and (211) surfaces. In another paper, Kanda showed graphical representations of the shear piezoresistance coefficients as a function of the crystal direction for the (100) plane [51].

2.3 Sensors Based on Piezoresistive Effect

Piezoresistive sensors are widely used for the characterization of complex stresses developed in electronic package during operation of the electronic module. These sensors are mainly resistor sensors which are implanted or diffused in the surface of the die in suitable locations on the surface. These sensors are not mounted like traditional strain gauges, rather they are fabricated in the surface of the die, hence an integral part of the

die. They can measure stresses nonintrusively even when the die is encapsulated. By placing these sensors strategically over the surface of a test chip, full area array mapping of the stresses over the die surface is possible. Piezoresistive sensors act as a guide towards selection of manufacturing processes and materials, new package design, prevention of package failures and improving reliability of electronic packages. The capability of sensing stress in plastic encapsulated packages was first exploited by Texas instruments in early 1980s [52-54]. Two-element sensor rosettes with 0-90 orientations, capable of measuring in-plane normal stress at a particular point on the die surface on (100) silicon were used by few early researchers such as Spencer et al. [54], Edwards et al. [52, 53] and Beaty et al. [55]. Four-element sensor rosettes with 0-±45˚-90˚ configuration of either n- or p-type, that can measure all three in-plane stress components were studied by Natarajan et al. [56] on (100) silicon and Gee et al. [57, 58] on (111) silicon. Miura et al. introduced a sensor rosette capable of measuring three in-plane stresses and one out-of-plane normal stress utilizing a four-element dual polarity rosette with 0-90˚ n-type and ±45˚ p-type resistors [59-61, 67]. These sensors were used to characterize thermally induced and packaging induced die stresses in DIPs.

Numerous papers on the application of the piezoresistive sensors to characterize die stress was published by various researchers. Usell and Smiley in 1981 talked about using test chips containing resistors sensors to quantify the strain induced due to the molding process and change in temperature of plastic encapsulated Dual-Inline-Packages (DIPs) [62]. Edwards et al. [52, 53], Spencer et al. [54] and Schroen et al. [63] performed studies on plastic encapsulated packages to investigate the effect of fabrication process variation, material variables and thermal cycling on the reliability of these packages. Test

chips on (111) silicon containing four-element sensor rosettes with 0-±45˚-90˚ orientations capable of measuring in plane stresses were used by Gee at el. [57, 58], Nguyen et al. [64] and van Gestel [65] to map the distribution of stress across the surface of die that were encapsulated in DIP packages. In these studies the researchers investigated the location of the maximum normal stress and shear stress on the die surface due to over molding of the DIP packages and thermal cycling. The effect of package materials, assembly techniques and geometrical parameters on the stress evolution were also explored. Lundström et al. explored the stress evolution of plastic leaded chip carrier (PLCC) packages using stress sensors on (111) silicon [66].

Sweet et al. from Sandia national laboratories worked on several series of ATC (ATC04, ATC06) test chips consisting of four n-type and four p-type resistors in each cell at an orientations of 0-±45˚-90˚ with respect to a die edge [68-76]. Using these test chips the researchers were able to extract three linear combination of the six unique stress components. They measured the stresses in plastic encapsulated DIPs, QFNs and flip chips [68, 70, 73, 74] and investigated the correlation of the stress evolution with the stress induced damage in packaged integrated circuits [72].

The Suhling and Jaeger group from Auburn University have extensively investigated the stress effects on resistors embedded on integrated chips and were successful in characterizing die stresses for various packaging architectures [77-89]. This group discovered the optimized sensor rosette on the (111) silicon which is capable of measuring complete three-dimensional state of stress at any point on the surface of the die as discussed by Bittle et al., Suhling et al. and Cordes et al [77, 78, 85]. To characterize six stress components, both n-type and p-type eight element dual polarity

sensing elements in 0-±45˚-90˚ configuration are used since the piezoresistive coefficients of n-type and p-type sensors are different [77, 78, 82]. They also presented the general resistance change expression for resistors embedded in (111) silicon and showed that four stress components can be measured in a temperature compensated manner using this sensor rosette. Temperature compensated measurements should be made whenever possible since there are large errors associated with the nontemperature compensated stress terms if the exact temperature change is not known [79, 81]. Kang worked out the piezoresistivity theory on various silicon wafer planes and also on silicon carbide [89]. Thermally induced stress was measured by Suhling et al. by calibrating the sensors over a wide temperature range [83]. A paper published by Jaeger et al. in 1993, demonstrated the first use of off-axis rosette capable of measuring temperature compensated results for both π_{44} and $(\pi_{11}-\pi_{12})$ [80]. Jaeger at al. discussed about the sources of errors associated with the measurement of stresses using piezoresistive sensors and discussed the methods to minimize the errors [79, 81]. Suhling et al. were first to use a test chip to characterize the complete state of stress in plastic encapsulated die attached to an FR-4 substrate [84]. To accurately measure the stresses developed in electronic packages using test chips containing piezoresistive sensors, accurate determination of the piezoresistive coefficients is necessary. Calibration of these coefficients is done using four point bending, wafer level and hydrostatic methods [86, 90, 91]. Zou et al. published papers on the stress characterization of PLCC, Chip on Board (COB), Quad Flat Pack (QFP) and Pin Grid Array (PGA) packages using (100) and (111) silicon test chips containing arrays of optimized piezoresistive stress sensor rosettes developed by this group [92-96]. Finite element analysis was also performed to correlate the simulation

results with the experimental stress observations showing reasonable agreement. A comprehensive review on piezoresistive theory and its application was published by Suhling and Jaeger in 2001 [88]. Mian et al. from the same group investigated analytically and experimentally a new piezoresistive stress sensor utilizing the van der Pauw structure (VDP), and showed that this sensor has three times more stress sensitivity than conventional resistor sensors [97, 98]. Rahim et al. used (111) test chips containing the eight-element sensor rosettes to measure the die stresses on backside and device side of the flip chip on laminate assemblies during various steps of assembly process and also during thermal cycling [87, 99-103]. In these studies, the die stress evolution due to the curing of the underfill was investigated for different underfill materials, and the residual stresses present in the final cured assemblies were compared which aided the material selection. These studies showed that in-plane shear stress provides an excellent indicator of the initiation and growth of delamination between the underfill and die surface during thermal cycling. The authors have also performed measurements of die stresses at extremely low temperatures down to -180˚ C [99, 100]. Finite element analysis of flip chip on laminate assemblies were presented in these papers and good agreement was found with the obtained stress measurement data with the predictions of nonlinear finite element models. Cho, Jaeger and Suhling [104] reported characterization of temperature dependence of the piezoresistance coefficient for n-type and p-type silicon from -150˚C to +125˚C using stress sensing chips. Roberts et al. utilized test chips to characterize die surface stresses in flip-chip and Plastic Ball Grid Array (PBGA) packaging during thermal cycling [105]. In more recent studies, Roberts et al. performed an extensive study of die stresses in large flip-chip microprocessor die attached to a high CTE ceramic

substrate through lead free solder bumps [105-115]. In research performed on CBGA packages, die stresses were measured after every packaging step (solder reflow, underfill dispense and cure, and lid attachment), and the stresses were found to be increasing monotonically. Die stresses were also measured during in-situ thermal cycling and power cycling tests. A detailed sequential finite element analysis was performed to obtain stress generation after each packaging stage and also during thermal cycling and power cycling that incorporated thermal histories of the package, nonlinear temperature and time dependent material properties and creation of elements. The simulation model showed excellent correlation with the experimental data. In another study, Jaeger et al. and Hussain et al. discussed the errors that arise in the stress extraction for a die on a flip chip assembly due to the inherent uncertainty in the values of the piezoresistive coefficients as well as measurement errors associated with measurement of rosette resistor values and temperature [116-118]. A finite element simulation was performed to have an estimate of the stresses that may occur on the die of a flip chip package and using the sensitivity expressions derived by the authors, the sensitivities of extracted stress to resistor measurement error, temperature measurement error and uncertainty in piezoresistive coefficients values have been presented and discussed in these papers. Monte Carlo simulations were utilized to estimate the expected errors in stress measurements of a silicon die mounted in a typical flip chip package. The results indicated that the sensitivities are stress dependent and vary widely over the die surface and it was shown that the temperature compensated stress terms generally tend to have low sensitivity to measurement uncertainty.

The device characteristics of both analog and digital circuits consisting of MOS transistors change due to the fabrication and process induced stress [119-124]. So extensive studies have been performed by various researchers to understand stress effect son FETs [43, 123-128]. In an FET, the channel consist of a resistive region when the transistor is biased in either linear or saturation region in strong inversion. With proper biasing, mechanically applied stress changes the mobility of the carriers in the inversion layer and makes FETs potential stress sensors. The advantage of the FET stress sensors over the conventional resistor sensors is that these sensors occupy very small chip area and as a result can be used to measure localized stress. Due to the light doping of the channel region, the sensitivity of the FET sensors is much higher than the traditional resistor sensors and also they can be operated in wide temperature range. In their paper, Jaeger at el. characterized the stress induced changes in device parameters of the FETs due to the piezoresistive channel region and commented on layout techniques to minimize piezoresistive response of resistors and FETs in CMOS circuits [123]. In another work, Jaeger at el. discussed relationships between CMOS circuit output and temperature compensated stress components on the (100) silicon and suggested layout techniques for optimized FET based piezoresistive sensor [129, 130]. A paper published by in 1999 Bradley at el. talked about measuring package induced die stress for using test chips containing 49 orthogonal CMOS FET sensor rosettes as stress sensors [131]. Bradley et al. showed in a later paper that the stress sensitivity of the FET channel does not depend on the channel length and showed that parasitic resistance is the reason for the observed reduction in piezoresistive coefficients of short-channel devices [132]. Chen et al., reported implementation of 512 CMOS current mirror type stress sensors in a test

chip to map stress distribution over the chip surface with high resolutions and compared the experimentally obtained data with that of finite element simulations for several packaging test cases, yielding good correlation [133, 134]. In a recent work performed by Hussain et al., it has been demonstrated that the piezoresistive coefficients of PMOS and NMOS devices vary significantly with choice of operating point and are strongly correlated with the underlying value of channel mobility [135]. The stress sensitivity of the PMOS devices was demonstrated to be linearly dependent on both operating current and mobility, whereas the NMOS sensitivity increased more rapidly as the current was reduced and exhibited a quadratic relation to electron mobility.

2.4 Piezojunction Effect

As mentioned in the beginning of this chapter, the mechanical stress effect on silicon p-n junction is termed the piezojunction effect, defined as the saturation current change of the p-n junction or bipolar junction transistor (BJT) due to the application of mechanical stress. The stress effect in p-n junctions and BJTs is different from resistors and field-effect transistors since the conduction in the later devices are due to the conduction of majority carriers where as in diodes and BJTs the conduction is due to minority carriers. The piezojunction effect is similar to the piezoresistive effect in semiconductors. In 1951, Hall, Bardeen and Pearson first talked about piezojunction effect in p-n junctions due to hydrostatic pressure [136]. Their experimental data showed a decrease in junction current, and they attributed the observed data to the stress induced change in energy gap. In 1962, Rindner from Raytheon Research investigated the effect of high anisotropic stress on the resistance of p-n junctions caused by a diamond stylus applied at the junction and found the change in resistance to be several orders of

magnitude larger than what Hall, Bardeen and Pearson obtained [137-139]. Rindner attributed the increase in current to that of an increased generation-recombination rate under stress along with the change in bandgap effect, and his experimental data also demonstrated the effect of stress in the junction has strong temperature dependence. Rindner discussed a further experimental study in 1965 of the effect of uniaxial stress on silicon and germanium p-n junctions. His experimental results supported the bandgap model proposed by Wortman et al. [140]. After Rindner, several researchers reported studies related to stress effect on p-n junctions [141] [156]-[161]. Imai et al. performed experimental observation of uniaxial stress effect on germanium p-n junctions [141-145]. Bulthuis applied local pressure and uniaxial stress at silicon and germanium p-n junctions [142, 143]. Mattson et al. applied incremental stress to p-n junctions [144]. Jayaraman et al. reported the effect of hydrostatic pressure on p-n junctions of Si and GaAs [145]. All these researchers concluded from their experimental data that the change in currents in the p-n junction under uniaxial, homogenous or localized stresses can be attributed to changes in the energy band structure due to stress, an increase in generation-recombination centers, and changes in the lifetime of the carriers. They all used styli for stress generation at the p-n junction which resulted in generation of large non uniform stress. Monteith and Wortman performed their experiments on stress effect on p-n junctions with the use of cantilever beams and as a result they were able to exert small stresses at the junction and were able to apply both tensile and compressive stress [146]. To explain their experimental data they used the deformation potential model and their data indicated that change in bandgap played a role in the change in current due to mechanical stress.

The theory behind the piezojunction effect was addressed by Hall, Bardeen and Pearson where they considered the changes in bandgap due to the applied isotropic stress [136]. Wortman et al. in 1964 refined the theory for high hydrostatic and uniaxial stresses since very high stress in the GPa range was applied in all the experiments performed on the p-n junction at that time [140]. The analytical model provided by Wortman at el. considered the change in generation-recombination current to be caused by changes in energy band structure and changes in generation-recombination centers. They calculated the minority carrier concentration change assuming stress independent effective masses for heavy and light holes. In a later analyses, Matukura and Miura considered changes in minority carrier mobility along with the change in carrier concentration [147]. But his assumption of mobility varying linearly with stress in case of large stress was not valid since linear relationship in case of large stress is not effective. Kanda further modified the theory provided by Wortman et al. by taking into account the changes in effective masses of heavy and light holes due to stress in the calculation of the minority carrier concentration [148]. He considered higher order stress dependence of the mobility of the minority carriers. In a later study, Kanda took into account the effect of a spin-orbit-split-off band on the valence band structure calculations [149]. He developed a basic framework for stress dependence of current gain and found out that stress dependence of current gain is a function of stress dependence of emitter efficiency and base transport factor.

Until the early 1970s all the experiments on the stress effect oin p-n junctions or bipolar transistors were based on applying large stress (in the GPa range) through a stylus on the surface of the individual diode or BJT. By then, the semiconductor industry had

moved into the era of large-scale integration. With large-scale integration, the packing of the devices continued to grow and the device sizes started to become smaller. Process and fabrication induced stress became important and a better understanding of the stress effect was needed. With the advent of micro fabrication of the ICs, better controlled stress generation techniques became accessible since diodes and BJTs can be incorporated in wafer strips which can be stressed in a controlled manner. Stresses applied can be either tensile or compressive and a stress magnitude of about few hundred MPa can be applied before failure of the ICs in wafer strip form.

The effect of fabrication and package induced stresses in bipolar ICs under moderate level of stress (~200-250 MPa) have been studied in detail by Fruett et al. and Creemer et al. Fruett focused his study on experimental quantification of stress induced changes in precision BJT devices and circuits such as bandgap references and temperature sensors and talked about reducing the inaccuracies and instabilities in these circuits caused by mechanical stress [4, 150-153]. He also provided detailed analysis on designing a stress sensor utilizing the piezojunction effect which can be an alternative to classical piezoresistive based sensors. Voltage reference circuits consisting of BJTs usually utilize the temperature sensitivity of the base-emitter voltage. But, the base-emitter voltage is also stress dependent, so Fruett suggested to be cautious while designing these circuits to eliminate the stress induced effects as much as possible. Fruett recommended a few solutions to get rid of the undesirable stress effects in circuits such as optimal placement of the bipolar devices on the surface of the wafer where the piezojunction effect is minimum. Other suggestions were the optimal design of the circuit so that the stress effect is minimized, such as using the bipolar devices in pairs [150-152]

as well as particular packaging architectures that will introduce particular stress pattern [151]. He reported characterization of piezojunction effect in vertical npn and pnp devices on (100) silicon and showed that this effect is nonlinear unlike piezoresistive effect which is quite linear in the stress range considered [153].

Creemer, a researcher from the same research group of Delft University worked on the analytical model of the piezojunction effect to quantify the changes in BJT characteristics due to the fabrication and package induced stresses [154-159]. The model provided by Kanda was well suited for modeling the stress effects on individually fabricated devices while applying stresses through styli, which introduced stress as high as 1 GPa. That model does not necessarily provide a good base, since the fabrication or package induced stress is much lower than that produced by styli. Also, the stress may be compressive as well as tensile, and both the devices and stresses can be at any orientation on the wafer surface. Creemer reported a new model based on the stress level that is typical in the fabrication or package induced stress domain [154, 155, 158]. He performed experiments on the npn and pnp transistors to characterize stress induced changes in saturation current of these devices for various orientation of the current and the stress with respect to the crystal axes. Then he proposed a theoretical model based on piezojunction coefficients which has the same expression as the piezoresistance model [158]. He showed from his experimental results and also from theoretical work that piezojunction effect is non-linear and the change in saturation current is larger when the stress is compressive. He also reported that the npn transistors are more sensitive to stress induced changes than the pnp transistors and that mobility change of carriers are senstitive to the current direction through the base, whereas the change in intrinsic carrier

concentration is insensitive to the direction of current. From his findings he recommended ways either to amplify or minimize this piezojunction effect depending upon whether the BJT is a stress sensor or used in stress insensitive circuits [156].

2.5 Sensors Based on Piezojunction Effect

Sensors based on piezojunction effect of the p-n junction or bipolar transistors have been discussed by several researchers [34, 160-166]. These diodes or BJT sensors has several advantages over conventional piezoresistors such as low power consumption, smaller size, higher sensitivity. The low power requirement is an important requirement for biomedical applications because of the constraints in the power supply for these biomedical devices. Sikorski was of the first researchers to utilize the piezojunction effect of a bipolar transistor as a microphone [160]. He was using a styli at the emitter base junction of npn and pnp transistors to apply stress and reported various geometric and electrical factors to improve the sensitivity of these sensors. In the same year, Legat et al. used the cantilever beam approach to apply stress in the junction of a stress transducer instead of using a styli [161]. Several other researchers reported several other piezojunction sensors where a stress generating styli or needle was used to generate large stresses at the junction [34, 162-166]. But these sensors were subjected to damage due to high stress that was generated with the styli or needle and also the proper alignment of the styli was also an concern, hence manufacturing this type of sensors were difficult. However the advent of micromachining facilitated the new sensor designs such as pressure sensors and uniaxial accelerometers, which helped eliminate critical assembly steps that were required for previous sensor designs [34].

2.6 Effect of Stress on Semiconductor Band Structure

The energy band structure of semiconductor material changes due to the application of mechanical stress or strain. Silicon and germanium, widely used semiconductor materials in the industry, have diamond cubic crystal structure. The periodicity of the crystal structure shifts when a crystal is mechanically stressed since the distances between atoms are altered. This stress causes the relative position of the conduction band and valence band to change as well as warping of the energy band surfaces. The altered band structure causes the charge transport parameters to change. As a result of these modified transport parameters, the electrical characteristics of the resistors, diodes and transistors shift exhibit piezoresistive or piezojunction effects in semiconductors. The semiconductor device physics behind the piezoresistive effect and piezojunction effect have been a great interest among researchers for many decades now. The first physics based study on the stress effect in single crystal semiconductors was done by Bardeen and Shockley [167]. In 1950, the Nobel Prize winners for transistor invention, Bardeen and Shockley, talked about the mobility change of the carriers in semiconductors due to shifts in conduction band edge which were caused by distortion of crystal lattice as a result of mechanical stress. They first coined the term “deformation potentials” to explain change in the bandgap due to dilation in semiconductors. Their simplified model was based on a model that considered one valley for conduction band and did not take into account the degeneracy of the energy bands.

Herring and Vogt in 1955, considered a many valley non degenerate energy bands to develop deformation potential theory to model the changes in energy bands due to strain to replace the previously developed theory for single non degenerate model for the

conduction band [168]. They explained the piezoresistance effect in terms of the shifts of energy valleys of the energy band in energy-wave vector space and repopulation of carriers between the energy valleys of the conduction band.

The model for stress induced changes in the conduction band, proposed by Herring and Vogt, is good enough to explain the piezoresistance phenomenon of n-type silicon and germanium, where the majority carriers are electrons.

For holes, the stress induced changes are more complicated since the relative shifts of the valence band edges cannot be adequately explained by the deformation potential model as the valence bands are degenerate at the k = 0 point and exhibit strong band warping. First theoretical work on the stress induced shift of the valence band was attempted by Adams et al. [169]. Later, a detailed study was performed by Kleiner and Roth [170] and finally a comprehensive and widely accepted work on the stress induced changes in valence band was done by Bir and Pikus [171, 172]. Bir and Pikus used perturbation theory method to determine the band structure around certain positions in E-k space. This k.p method, formulated by Luttinger and Kohn [173], determines the effective masses and dispersion relations for the energy bands at a particular point in the first Brillouin zone by applying group theory of semiconductor crystals. Along with implementing the k.p theory to obtain the effect of stress on valence band structure, this method also yields analytical equations of the extremities of band structure. Bir and Pikus introduced a strain Hamiltonian along with the k.p Hamiltonian to account for the relative shifts between the bands and also for the modification of band shapes due to stress. This Hamiltonian was used to obtain valence band effective masses and deformation potentials in stressed silicon.

A series of papers was published on cyclotron resonance experiments to obtain improved understanding of the band structure of semiconductors, to obtain the effective masses of the carriers, and also the deformation potentials [174-180]. If an external static magnetic field is applied to a semiconductor crystal, the carriers of the semiconductor accelerate in spiral motion about the static magnetic field at an angular frequency that is inversely proportional to the effective mass of the carriers. The cyclotron resonance experiment is an effective way to ascertain the shapes of the semiconductor band edges, since curvature of the band surfaces are determined by the effective mass of the carriers. Dresselhaus et al. and Lax et al. were the first researchers to initiate successful cyclotron resonance experiments that reported the shapes of the conduction band from the effective mass of the electrons [174, 180]. The conduction band shape was well explained by cyclotron resonance experiment performed by these investigators, but the degeneracy of the valence band and the complex shape of the warped energy surfaces due to the coupling of the degenerate heavy hole and light hole bands made it difficult to define the shape of valence band. In an attempt to have a better understanding of the valence band shape of semiconductors, Hensel et al. and Hasewaga carried out cyclotron resonance experiment on holes by straining the semiconductor crystal by applying large uniaxial stresses [175-179]. As a result of the uniaxial stress, the degeneracy of the valence band, which causes the complex warping of the band, was removed as the symmetry of the crystal was destroyed. Hensel et al. and Hasewaga reported that the compressive stress along (001) direction causes the light hole mass to become larger, whereas heavy hole mass does not change much with strain. Their work also showed that for compressive stress along (110) and (111) direction, the light hole band become the top valence band as

it shifted up, and the heavy hole band shifted down. They discussed the stress induced splitting of the bands as a function of strain, warping of the bands, changes in effective mass due to stress and changes in the density of states of the carriers that effects the band occupation of the carriers. However, they did not address the issue of strain induced changes in carrier mobilities.

There were other experimental methods adopted by researchers to obtain semiconductor deformation potentials such as photoluminescence [181, 182] and piezoelectroreflectance [183]. Fischetti [184-186] reported theoretical work on determining the deformation potentials using pseudopotential calculations which were later on found to be consistent with experimental observations made by Lim et al. [187].

Theoretical estimation of the piezoresistive coefficients for both n-type and p-type semiconductor was attempted using the deformation potential model by several researchers [47, 48, 148, 168, 188-193]. The theoretical work by Herring and Vogt [168] based on the energy transfer mechanism was successful in obtaining the piezoresisitive coefficients of n-type semiconductors that revealed good correlation with the experimentally obtained data. Theoretical aspects of piezoresistive coefficients were studied extensively by Kanda [47, 48, 148, 188-193]. He showed that explanation of the piezoresistance effect in n-type silicon, required changes in effective mass of the electrons to be considered along with the electron-transfer mechanism explained by Herring and Vogt. Kanda was able to obtain the non-zero shear piezoresistive coefficient considering the change in effective mass with stress that was otherwise found to be zero in previous analyses. Theoretical expressions for second order piezoresistive coefficients were provided by Matsuda et al [47]. The theory proposed by Bir and Pikus adequately

explained the linear piezoresistivity in p-type semiconductors [171]. A model proposed by Suzuki et al. for p-type silicon considering decoupling of the degenerate valence bands due to the stress showed somewhat good agreement with the experimental data [193]. Using the model by Suzuki, Toriyama et al. analyzed the piezoresistance of p type silicon using hole transfer and hole effective mass change due to stress [194].

2.7 Summary

In this chapter, a literature review on the mechanical stress effect on semiconductor materials are presented. The periodicity of the semiconductor crystal is altered due to the mechanical stress which causes changes in currents or voltages at the terminals of the electronic devices, which is described as the piezoresistive effect or piezojunction effect. Piezoresistive and piezojunction effects cause the electrical characteristics of the electronic devices such as resistors, field effect transistors (FET), bipolar junction transistors (BJT) to alter. A detailed literature review on sensors based on piezoresistive effect and piezojunction effect was also discussed in this chapter. Finally an overview of the literary work on the electronic band structure changes in semiconductor materials due to stress was presented.

CHAPTER 3

ERROR ANALYSIS FOR PIEZORESISTIVE STRESS SENSORS USED IN FLIP CHIP PACKAGING

3.1 Introduction

Multi-element resistor rosettes on silicon IC chips have been widely used by many researchers to obtain die stress measurements in different electronic packaging and in other applications [52-61, 64, 69]. Due to the piezoresistive effect, the electrical resistivity of silicon changes when stress is applied [23, 38-43]. Silicon is a suitable material for the piezoresistive stress sensor fabrication because of the fully established integrated circuit technology. In place of an actual die, a test die containing the piezoresistive stress sensors on the surface of the die, is placed in the electronic package in order to determine the die stress. These sensors are integral part of the die, i.e.; they are fabricated in the die using microelectronic fabrication technology. The resistor sensors have serpentine form to adjust the resistance of these sensors, and the sensitivity of these sensors depends on the orientation of the sensors on the wafer and also the silicon crystallographic orientation. Resistor sensors in rosette form on the (111) surface respond to all six components of the stress state and therefore can measure the complete three-dimensional state of stress at points on the surface of a die by using properly designed rosettes [82, 84, 88], whereas the sensor rosettes on (100) silicon surface can measure only four different stress quantities. The formulation to extract stresses from the resistance change of the resistor sensors is discussed in the following section.

Past studies of many sources of error have led to rosette optimization and demonstrated that temperature-compensated stress extraction should be used whenever possible. In this work, we extend the error analysis to include the inherent uncertainty in the measured values of the sensor resistances, piezoresistive coefficients and the temperature at time of the measurement. The stresses in an under-filled flip chip package are calculated using finite element simulation and utilized to evaluate the stress dependent sensitivities across the die surface. Sensitivity analysis has been performed where direct calculations of the sensitivities of the extracted stresses to uncertainties in the piezoresistive coefficients, sensor resistances and the measured temperature are presented. Monte Carlo simulation results confirm that temperature compensated rosette configurations should be utilized whenever possible.

3.2 Piezoresistive Theory for Silicon

The theory that describes the relation between resistor sensor response and applied stress is fully developed [82, 84, 88] and explained in Appendix A. Although silicon wafers can be obtained with a number surface orientations, the (100) and (111) surfaces represent the commonly utilized orientations in the semiconductor industry, and the discussion that follows is restricted to these two cases.

3.2.1 (100) Silicon

In the current microelectronics industry, the vast majority of silicon devices are fabricated using (100) silicon wafers as depicted in Fig. 3.1. The surface of the wafer is an (001) plane, and the [100] direction is normal to the wafer surface. The unprimed coordinate system represents the crystallographic axes for the wafer, whereas the primed coordinate system is rotated 45˚ from the principal crystallographic axes. The primed

axes x'_1 and x'_2 are parallel and perpendicular to the primary flat of the wafer and aligned with the edges of normal semiconductor chips.

Angle ϕ represents the angle between the x'_1 - axis and the resistor orientation. When only the first order temperature coefficient is retained, the normalized resistance change is given in Eq. (3.1) below in which R(0,0) is the unstressed resistance at reference temperature T_{REF} and $\Delta T = T - T_{REF}$.

$$\begin{aligned}\frac{\Delta R}{R} &= \frac{R(\sigma,\Delta T)-R(0,0)}{R(0,0)} \\ &= \left[\left(\frac{\pi_{11}+\pi_{12}+\pi_{44}}{2}\right)\sigma'_{11}+\left(\frac{\pi_{11}+\pi_{12}-\pi_{44}}{2}\right)\sigma'_{22}\right]\cos^2\varphi + \\ &\quad \left[\left(\frac{\pi_{11}+\pi_{12}-\pi_{44}}{2}\right)\sigma'_{11}+\left(\frac{\pi_{11}+\pi_{12}+\pi_{44}}{2}\right)\sigma'_{22}\right]\sin^2\varphi \\ &\quad + \pi_{12}\sigma'_{33}+(\pi_{11}-\pi_{12})\sigma'_{12}\sin 2\varphi+\alpha_1\Delta T\end{aligned} \tag{3.1}$$

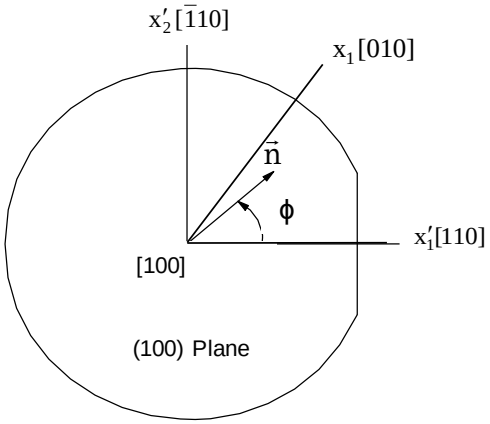


Figure 3.1 (100) Silicon Wafer

Eq. (3.1) indicates that the out-of-plane shear stresses σ'_{13} and σ'_{23} do not influence the resistances of stress sensors fabricated on (100) wafers. This means that a sensor rosette on (100) silicon can at best measure four of the six unique components of the stress state at a point on the surface of the silicon. Three unique piezoresistive coefficients for

silicon ($\pi_{11}, \pi_{12}, \pi_{44}$) appear in Eq. (3.1), and these parameters must be measured before stress component values can be extracted from resistance change measurements. Typical room temperature values for the piezoresistive coefficients in lightly doped silicon appear in Table 3.1 [23]. As doping increases, the piezoresistive response decreases, and the coefficients can be substantially smaller than the Table 3.1 values for heavily doped resistors. However, the tabulated values do provide important comparative information as well as upper bounds on the magnitudes of the coefficients. Coefficient π_{44} is the largest coefficient for p-type material whereas the values of π_{11} and π_{12} are very small. For n-type material, π_{44} is small, but the other two individual coefficients are relatively large. In Eq. (3.1), parameters π_{11} and π_{12} always appear together in sum and difference terms, and we define the sum and difference of these coefficients as $\pi_S = \pi_{11} + \pi_{12}$ and $\pi_D = \pi_{11} - \pi_{12}$, respectively. Note from Table 3.1 that π_D has a very large value in n-type material.

Table 3.1 Piezoresistive Coefficients for Ligthly Doped Silicon [23]

Silicon Piezoresistive Coefficients		
π Coefficient	n-type Si ($\times 10^{-12}$ Pa^{-1})	p-type Si ($\times 10^{-12}$ Pa^{-1})
π_{11}	-1022	+66
π_{12}	+534	-11
π_{44}	-136	+1381
$\pi_S = \pi_{11}+\pi_{12}$	-488	+55
$\pi_D = \pi_{11}-\pi_{12}$	-1556	+77
B_1	-312	718
B_2	297	-228
B_3	61	-448

3.2.2 (111) Silicon

The second common silicon crystal orientation used in semiconductor fabrication is (111) material, and a general (111) silicon wafer is shown in Fig. 3.2. The surface of the wafer is a (111) plane, and the [111] direction is normal to the wafer plane. The principal crystallographic axes x_1 = [100], x_2 = [010], and x_3 = [001] no longer lie in the wafer plane and are not shown. As mentioned previously, it is convenient to work in an off-axis primed wafer coordinate system where the x'_1 and x'_2 axes are parallel and perpendicular to the primary wafer flat, corresponding to the edges of fabricated IC dice.

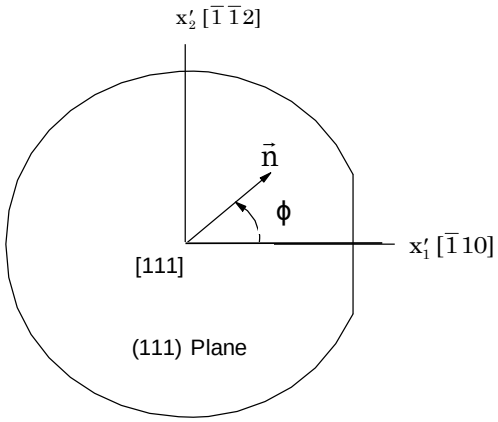


Figure 3.2 (111) Silicon Wafer

The resistance change of an arbitrarily oriented in-plane resistor on the (111) surface can be expressed in terms of the stress components resolved in this natural wafer coordinate system as described below:

$$\begin{aligned}\frac{\Delta R}{R} &= \frac{R(\sigma,\Delta T)-R(0,0)}{R(0,0)} \\ &= \left[B_1\sigma'_{11}+B_2\sigma'_{22}+B_3\sigma'_{33}+2\sqrt{2}(B_2-B_3)\sigma'_{23} \right]\cos^2\phi \\ &+ \left[B_2\sigma'_{11}+B_1\sigma'_{22}+B_3\sigma'_{33}-2\sqrt{2}(B_2-B_3)\sigma'_{23} \right]\sin^2\phi \\ &+ \left[2\sqrt{2}(B_2-B_3)\sigma'_{13}+(B_1-B_2)\sigma'_{12} \right]\sin 2\phi+\alpha_1\Delta T\end{aligned} \tag{3.2}$$

where the B coefficients are

$$B_1 = \frac{\pi_{11} + \pi_{12} + \pi_{44}}{2} \qquad B_2 = \frac{\pi_{11} + 5\pi_{12} - \pi_{44}}{6} \quad B_3 = \frac{\pi_{11} + 2\pi_{12} - \pi_{44}}{3}$$

and ϕ is the angle between the x'_1-axis and the resistor orientation.

The B coefficients represent a set of linearly independent temperature dependent combined parameters that are convenient for characterization of piezoresistance on the (111) surface. These parameters must be measured before stress component values can be extracted from resistance change measurements.

Typical values of the "B" coefficients for lightly doped material also appear in Table 3.1. In n-type material, B_1 and B_2 are the largest coefficients whereas B_3 is quite small. One thing to be noted is that B_1 and B_2 are approximately equal in magnitude and opposite in sign. For p-type material, B_1 and B_3 have the largest magnitudes, although all three coefficients have useful values.

It is very important to note that the general resistance change expression in Eq. (3.2) is dependent on all six of the stress components that describe the state of stress at a point in the silicon material. Therefore, the potential exists for developing a sensor rosette that can measure the complete three-dimensional state of stress at points on the surface of a die by using properly designed (111) silicon sensors.

3.3 Rosette Designs

From Eq. (3.1), the resistance change of an in-plane sensor fabricated on (100) silicon is observed to depend on four stress components (σ'_{11}, σ'_{22}, σ'_{33}, σ'_{12}) and the orientation of the sensor element. Likewise, from Eq. (3.2), the resistance change of an in-plane sensor fabricated on (111) silicon is found to depend upon all six stress

components and the orientation of the sensor. Because of this, it is natural to assume that the potential exists to design a four-element rosette on (100) silicon capable of measuring four stress components, and a six-element rosette on (111) silicon capable of measuring all six stress components. However, it can also be proved theoretically that, when considering all possible resistor orientations at a point, there are only three unique (linearly independent) responses on any given silicon plane for a given silicon impurity type.

The full potential of multi-element sensor rosettes to measure up to six stress components can be achieved by using dual-polarity sensing elements fabricated with both n-type and p-type silicon. Since the piezoresistive coefficients of the n-type and p-type resistors are different, there can be up to six unique sensor responses in dual-polarity rosettes.

Besides the ability to measure two additional stress components, theoretical analysis has established that properly designed sensor rosettes on the (111) silicon wafer plane have other advantages relative to sensors fabricated using standard (100) silicon [88]. In particular, optimized sensors on (111) silicon are capable of measuring four temperature compensated combined stress components, while those on (100) silicon can only be used to measure two temperature compensated quantities.

In this discussion, "temperature compensated" refers to the ability to extract the stress components directly from the resistance change measurements without the need to know the temperature change ΔT. This is particularly important attribute, given the large errors that can be introduced into non-temperature compensated stress sensor data when the temperature change is not precisely known.

Furthermore, computer-aided symbolic analysis was used to consider all possible silicon wafer orientations, and it established that the (111) plane in fact offers the opportunity to measure the highest number (four) of stress components in a temperature compensated manner of any possible silicon wafer plane[77, 78, 85, 89]. The four stress components that can be measured in a temperature compensated manner are the three shear stress components and the difference of the in plane normal stress components.

3.3.1 Optimized 4-Element Rosette on (100) Silicon

A four-element dual-polarity sensor rosette on (100) is shown in Fig. 3.3. The rosette contains a 0-90^o p-type resistor pair and a $\pm$45^o n-type resistor pair. This choice of sensor orientations minimizes thermally induced errors as well as those due to resistor misalignment relative to the true crystallographic axes, and permits accurate temperature compensated measurement of the values of the in-plane normal stress difference (σ'_{11} - σ'_{22}) and the in-plane shear stress σ'_{12} as outlined below.

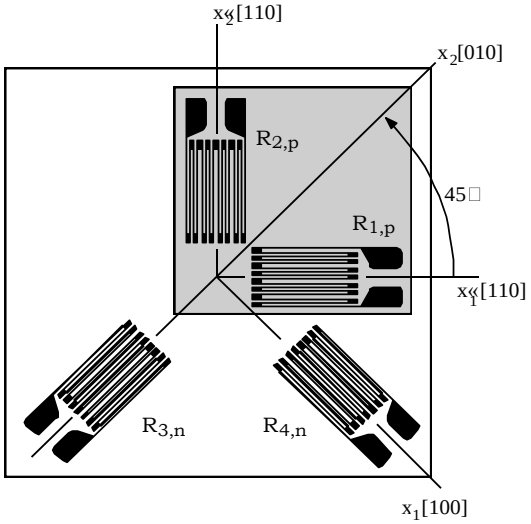


Figure 3.3 A Four-Element Rosette for (100) Silicon

Application of eq. (3.1) to the four resistor orientations gives the following relations between the resistance changes and the stresses at the rosette site:

$$\begin{aligned}
\frac{\Delta R_1}{R_1} &= \frac{\left(\pi_S^p + \pi_{44}^p\right)}{2}\sigma_{11}^{'} + \frac{\left(\pi_S^p - \pi_{44}^p\right)}{2}\sigma_{22}^{'} + \pi_{12}^p\sigma_{33}^{'} + \alpha_1^p\Delta T \\
\frac{\Delta R_2}{R_2} &= \frac{\left(\pi_S^p - \pi_{44}^p\right)}{2}\sigma_{11}^{'} + \frac{\left(\pi_S^p + \pi_{44}^p\right)}{2}\sigma_{22}^{'} + \pi_{12}^p\sigma_{33}^{'} + \alpha_1^p\Delta T \\
\frac{\Delta R_3}{R_3} &= \frac{\pi_S^n}{2}\left(\sigma_{11}^{'} + \sigma_{22}^{'}\right) + \pi_D^n\sigma_{12}^{'} + \pi_{12}^n\sigma_{33}^{'} + \alpha_1^n\Delta T \\
\frac{\Delta R_4}{R_4} &= \frac{\pi_S^n}{2}\left(\sigma_{11}^{'} + \sigma_{22}^{'}\right) - \pi_D^n\sigma_{12}^{'} + \pi_{12}^n\sigma_{33}^{'} + \alpha_1^n\Delta T
\end{aligned} \tag{3.3}$$

Six independent piezoresistive coefficients now appear, and superscripts n and p are used to denote the piezoresistive coefficients of the n-type and p-type resistors, respectively. The expressions in Eq. (3.3) can be inverted to yield Eqs. (3.4) for the four stress components (σ'_{11}, σ'_{22}, σ'_{33}, σ'_{12}) in terms of the resistance changes of the sensing elements, the six piezoresistive coefficients, and the temperature change ΔT.

$$\sigma'_{11} = \frac{\pi_{12}^p\left[\frac{\Delta R_3}{R_3} + \frac{\Delta R_4}{R_4} - 2\alpha_1^n T\right] - \pi_{12}^n\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_2}{R_2} - 2\alpha_1^p T\right]}{2(\pi_{11}^n\pi_{12}^p - \pi_{11}^p\pi_{12}^n)} + \frac{1}{2\pi_{44}^p}\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_2}{R_2}\right]$$

$$\sigma'_{22} = \frac{\pi_{12}^p\left[\frac{\Delta R_3}{R_3} + \frac{\Delta R_4}{R_4} - 2\alpha_1^n T\right] - \pi_{12}^n\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_2}{R_2} - 2\alpha_1^p T\right]}{2(\pi_{11}^n\pi_{12}^p - \pi_{11}^p\pi_{12}^n)} - \frac{1}{2\pi_{44}^p}\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_2}{R_2}\right] \tag{3.4}$$

$$\sigma'_{33} = \frac{\pi_S^n\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_2}{R_2} - 2\alpha_1^p T\right] - \pi_S^p\left[\frac{\Delta R_3}{R_3} + \frac{\Delta R_4}{R_4} - 2\alpha_1^n T\right]}{2(\pi_{11}^n\pi_{12}^p - \pi_{11}^p\pi_{12}^n)}$$

$$\sigma'_{12} = \frac{1}{2\pi_D^n}\left[\frac{\Delta R_3}{R_3} - \frac{\Delta R_4}{R_4}\right] \qquad \sigma_{11}^{'} - \sigma_{22}^{'} = \frac{1}{\pi_{44}^p}\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_2}{R_2}\right]$$

Direct combination of the expressions in eq. (3.4) also yields to two temperature compensated (independent of ΔT) resistance-stress expressions.

The piezoresistive coefficients needed to solve for the stress components can be measured using a combination of uniaxial and/or hydrostatic pressure calibration testing [87-88]. The original choice of n- and p-type material for the four resistors in Fig. 3.3 is based upon the values of π_{44}^{p} and π_{D}^{n} in Table 3.1.

3.3.2 Optimized 8-Element Rosette on (111) Silicon

The eight-element dual-polarity rosette on (111) silicon illustrated in Fig. 3.4 contains p-type and n-type sensor sets, each with resistor elements making angles of $\phi = 0$, ± 45, and 90 degrees with respect to the horizontal x'_1-axis. This sensor has been developed for measurement of the complete state of stress at points on the surface of a packaged semiconductor die. It has beenoptimized to measure four stress components in a temperature compensated manner, and the "B" coefficients can be measured using a combination of uniaxial and hydrostatic testing.

A six-element rosette (without the -45^{o} resistors) can also be used to extract the complete stress state. However, including the two extra resistors allows for more convenient bridge measurements of the resistance changes and better stress measurement localization as only $0/90^{o}$ or $+45^{o}/-45^{o}$ resistor pairs appear in any given expression.

Repeated application of Eq. (3.2) to each of the piezoresistive sensing elements leads to the expressions in Eq. (3.5) for the stress-induced resistance changes. Superscripts n and p are used on the combined piezoresistive coefficients to denote n-type and p-type resistors, respectively. For an arbitrary state of stress, these expressions can be inverted to solve for the six stress components in terms of the measured resistance changes, and the results appear in Eq. (3.6).

$$
\begin{aligned}
\frac{\Delta R_1}{R_1} &= B_1^n \sigma'_{11} + B_2^n \sigma'_{22} + B_3^n \sigma'_{33} + 2\sqrt{2}(B_2^n - B_3^n)\sigma'_{23} + \alpha_1^n \Delta T \\
\frac{\Delta R_2}{R_2} &= \left(\frac{B_1^n + B_2^n}{2}\right)(\sigma'_{11} + \sigma'_{22}) + B_3^n \sigma'_{33} + 2\sqrt{2}(B_2^n - B_3^n)\sigma'_{13} + (B_1^n - B_2^n)\sigma'_{12} + \alpha_1^n \Delta T \\
\frac{\Delta R_3}{R_3} &= B_2^n \sigma'_{11} + B_1^n \sigma'_{22} + B_3^n \sigma'_{33} - 2\sqrt{2}(B_2^n - B_3^n)\sigma'_{23} + \alpha_1^n \Delta T \\
\frac{\Delta R_4}{R_4} &= \left(\frac{B_1^n + B_2^n}{2}\right)(\sigma'_{11} + \sigma'_{22}) + B_3^n \sigma'_{33} - 2\sqrt{2}(B_2^n - B_3^n)\sigma'_{13} - (B_1^n - B_2^n)\sigma'_{12} + \alpha_1^n \Delta T \\
\frac{\Delta R_5}{R_5} &= B_1^p \sigma_{11} + B_2^p \sigma'_{22} + B_3^p \sigma'_{33} + 2\sqrt{2}(B_2^p - B_3^p)\sigma'_{23} + \alpha_1^p \Delta T \\
\frac{\Delta R_6}{R_6} &= \left(\frac{B_1^p + B_2^p}{2}\right)(\sigma'_{11} + \sigma'_{22}) + B_3^p \sigma'_{33} + 2\sqrt{2}(B_2^p - B_3^p)\sigma'_{13} + (B_1^p - B_2^p)\sigma'_{12} + \alpha_1^p \Delta T \\
\frac{\Delta R_7}{R_7} &= B_2^p \sigma'_{11} + B_1^p \sigma'_{22} + B_3^p \sigma'_{33} - 2\sqrt{2}(B_2^p - B_3^p)\sigma'_{23} + \alpha_1^p \Delta T \\
\frac{\Delta R_8}{R_8} &= \left(\frac{B_1^p + B_2^p}{2}\right)(\sigma'_{11} + \sigma'_{22}) + B_3^p \sigma'_{33} - 2\sqrt{2}(B_2^p - B_3^p)\sigma'_{13} - (B_1^p - B_2^p)\sigma'_{12} + \alpha_1^p \Delta T
\end{aligned}
\tag{3.5}
$$

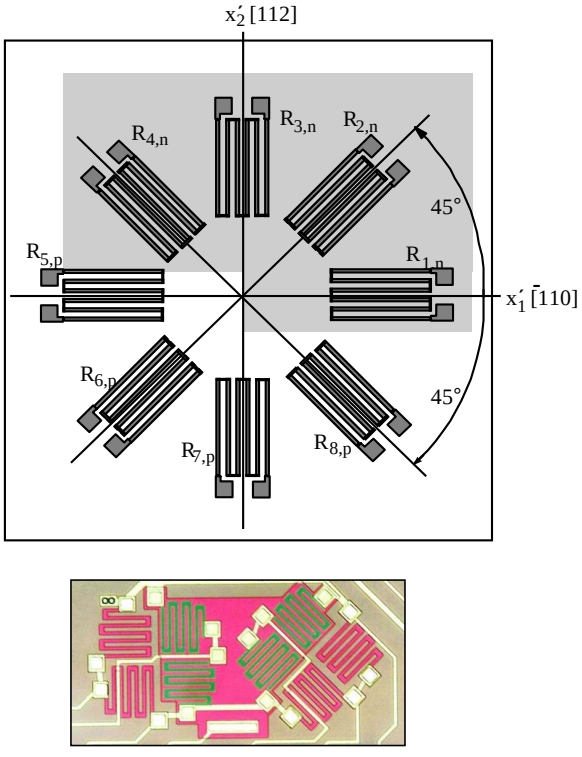


Figure 3.4 Top: A Sensor Rosette for (111) Silicon.
Bottom: Microphotograph of the Sensor Rosette

$$\sigma'_{11} = \frac{(B_3^p - B_2^p)\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right] - (B_3^n - B_2^n)\left[\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right]}{2[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]} + \frac{B_3^p\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^n \Delta T\right] - B_3^n\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^p \Delta T\right]}{2[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]}$$

$$\sigma'_{22} = -\frac{(B_3^p - B_2^p)\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right] - (B_3^n - B_2^n)\left[\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right]}{2[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]} + \frac{B_3^p\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^n \Delta T\right] - B_3^n\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^p \Delta T\right]}{2[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]}$$

$$\sigma'_{33} = \frac{-(B_1^p + B_2^p)\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^n \Delta T\right] + (B_1^n + B_2^n)\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^p \Delta T\right]}{2[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]}$$

$$\sigma'_{13} = \frac{\sqrt{2}}{8}\left[\frac{(B_2^p - B_1^p)\left[\frac{\Delta R_4}{R_4} - \frac{\Delta R_2}{R_2}\right] - (B_2^n - B_1^n)\left[\frac{\Delta R_8}{R_8} - \frac{\Delta R_6}{R_6}\right]}{(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n}\right] \qquad (3.6)$$

$$\sigma'_{23} = \frac{\sqrt{2}}{8}\left[\frac{-(B_2^p - B_1^p)\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right] + (B_2^n - B_1^n)\left[\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right]}{(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n}\right]$$

$$\sigma'_{12} = \frac{-(B_3^p - B_2^p)\left[\frac{\Delta R_4}{R_4} - \frac{\Delta R_2}{R_2}\right] + (B_3^n - B_2^n)\left[\frac{\Delta R_8}{R_8} - \frac{\Delta R_6}{R_6}\right]}{2[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}$$

$$\sigma'_{11} - \sigma'_{22} = \frac{(B_3^p - B_2^p)\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right] - (B_3^n - B_2^n)\left[\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right]}{[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}$$

In Eq. (3.5) and (3.6), only the first order temperature terms have been retained. From the expressions in Eq. (3.6), it is clear that the extraction of the three shear stresses (σ'_{13}, σ'_{23}, and σ'_{12}) from the measured resistance changes is independent of T. Evaluation of the three normal stress components requires measurement of the normalized resistance changes of the sensors and the temperature change ΔT experienced by the sensing elements. The temperature coefficients of resistance must also be known for each doping type. Besides the three shear stresses, an additional temperature compensated quantity can be obtained by subtracting the expressions for the normal stresses σ'_{11} and σ'_{22}.

3.4 Stress Extraction using Piezoresistive Theory

A typical expression of the relation between resistor sensor response and applied stress is shown in eq. (3.7).

$$\sigma'_{11} = \frac{\pi_{12}^{p}\left[\frac{\Delta R_3}{R_3} + \frac{\Delta R_4}{R_4} - 2\alpha_1^{n}\Delta T\right] - \pi_{12}^{n}\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_2}{R_2} - 2\alpha_1^{p}\Delta T\right]}{2(\pi_{11}^{n}\pi_{12}^{p} - \pi_{11}^{p}\pi_{12}^{n})} + \frac{1}{2\pi_{44}^{p}}\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_2}{R_2}\right] \quad (3.7)$$

for (100) Silicon

$$\sigma'_{33} = \frac{-(B_1^{p} + B_2^{p})\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^{n}\Delta T\right] + (B_1^{n} + B_2^{n})\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^{p}\Delta T\right]}{2[(B_1^{n} + B_2^{n})B_3^{p} - (B_1^{p} + B_2^{p})B_3^{n}]}$$

for (111) Silicon

These mathematical expressions in Eq. (3.8) indicate that to extract stress using the piezoresistive stress sensors either on (100) or (111) silicon, the piezoresistive coefficients ‘π’ for (100) and ‘B’ for (111) silicon, temperature change ‘ΔT’ and the change in resistance value of the resistors ‘$\Delta R/R$’ need to be measured. To obtain the piezoresistive coefficients, a calibration procedure is performed before stress component values can be extracted. The calibration of the piezoresistive coefficient values are done using methods such as four-point bending, cantilever bending, and hydrostatic pressure.

3.5 Sensitivity Analysis

In order to extract die stresses using piezoresistive sensor rosette, resistance changes of the sensing elements, piezoresistive coefficients and temperature are required to be measured as can be seen from Eqs. (3.5) and (3.7). The resistance change of the sensing elements are obtained from the deviation of the resistance values of the sensors from their

initial values. The piezoresistive coefficient values are measured using methods including four-point bending, cantilever bending, and hydrostatic pressure. Each of the measurement techniques inherently introduces experimental error. Errors in the experiment or the uncertainty in the experiments can be due to the methodology, operational condition, and environmental effect or due to the problematic measurement unit. Other sources of uncertainty include the precise surface orientation, location of the actual crystallographic axes, and precision of mask alignment during semiconductor fabrication[79].

Experimental uncertainty inherently introduces errors in the measured values of the resistance changes and temperature. The calibration process of the piezoresistive coefficients results in uncertainties of 10% or more in the values of the piezoresistive coefficients used to calculate the stresses from measured resistor changes. These uncertainties can potentially lead to significant errors in the extracted stress values. So it is important to express the measured calibration coefficients, temperatures and resistance change values by including the associated uncertainties in the measurements. These uncertainties of the extracted stress data due to the uncertainties in the input parameters can be evaluated by data analysis technique, predominantly statistical technique.

The uncertainties in the extracted outcome of an experiment because of the uncertainties or errors in the input parameters can be addressed using sensitivity analysis. The sensitivity analysis is an effective way to estimate the uncertainties of an extracted or derived quantity by accounting for the different uncertainties in the experimentally measured input parameters to obtain the response.

To explore how the uncertainties in the input parameters affect the response, we use the classic definition of sensitivity of a given quantity to parametric changes. If an

algebraic equation exists to define the correlation between the output response and the input variables, then the sensitivity of an intended response can be calculated from the first order partial derivative of the response to the given input variables. For example, the sensitivity of stress component σ'_{ij} to changes in a given parameter P is given by

$$S_P^{\sigma'_{ij}} = \frac{P}{\sigma'_{ij}} \frac{\partial \sigma'_{ij}}{\partial P} = \left(\frac{\partial \sigma'_{ij}}{\sigma'_{ij}} \right) \Bigg/ \left(\frac{\partial P}{P} \right) \tag{3.8}$$

$S_P^{\sigma'_{ij}}$ is a unit-less quantity that represents the ratio of the fractional change in stress that results from a fractional change in the specified parameter. The quotient (P/σ'_{ij}) is introduced to remove the effect of units by normalizing the parameters. The sensitivity of an output to its input value demonstrate how significant is the input variability. The larger the sensitivity value, the more significant is the input value. Values of S equal to one or less are regarded as good, whereas those much greater than one are problematic.

3.5.1 Resistance Measurement Errors

A typical resistor sensitivity expression for (111) silicon (1 of a total of 63) resulting from the evaluation of Eq. (3.8) using the results in equations in Eq. (3.6) appears in Eq. (3.9).

$$S_{\frac{\Delta R_1}{R_1}}^{\sigma'_{33}} = \frac{-(B_1^p + B_2^p)}{2[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]} \times \left[B_1^n \frac{\sigma'_{11}}{\sigma'_{33}} + B_2^n \frac{\sigma'_{22}}{\sigma'_{33}} + B_3^n + 2\sqrt{2}(B_2^n - B_3^n) \frac{\sigma'_{23}}{\sigma'_{33}} \right] \tag{3.9}$$

As an example, this expression indicates the problem of having a small stress σ'_{33} in the denominator of the expression that will cause the sensitivity to be high.

Therefore, it is difficult to measure a small stress such as σ'_{33} in the presence of large normal stresses. However, one must be careful with the sensitivities. A zero value of stress leads to an infinite sensitivity, and it is also useful to study the individual derivatives of stress with respect to the resistor values that are needed to evaluate Eq. (3.9). For example, the derivative of σ'_{33} with respect to R_1 is

$$\frac{\partial \sigma'_{33}}{\partial \dfrac{\Delta R_1}{R_1}} = \frac{-(B_1^p + B_2^p)}{2[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}$$

$$\text{and} \qquad \frac{\partial \sigma'_{33}}{\partial R_1} = \frac{1}{R_1(0,0)} \frac{\partial \sigma'_{33}}{\partial \dfrac{\Delta R_1}{R_1}} \tag{3.10}$$

The complete set of expressions for the derivatives appears in Table B.1 of Appendix B. Note that these expressions are convenient since they are independent of stress, which is not the case for the derivatives related to the piezoresistive coefficients.

3.5.2 Temperature Measurement Errors

In a similar manner, the sensitivity of stress to temperature is evaluated as

$$S_T^{\sigma_{ij}} = \frac{T}{\sigma_{ij}} \frac{\partial \sigma_{ij}}{\partial T} \tag{3.11}$$

A sample of the derivative needed above is

$$\frac{\partial \sigma'_{11}}{\partial T} = \frac{\alpha_1^p B_3^n - \alpha_1^n B_3^p}{(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n} \tag{3.12}$$

The derivatives for the three temperature dependent stresses appear in Table B.2 of Appendix B.

3.5.3 Piezoresistive Coefficient Uncertainty

The sensitivity of stress σ to changes in values of the π or B coefficients is expressed using (3.8) as

$$S_{B_k}^{\sigma_{ij}} = \frac{B_k}{\sigma_{ij}} \frac{\partial \sigma_{ij}}{\partial B_k} = \left(\frac{\partial \sigma_{ij}}{\sigma_{ij}} \right) \Big/ \left(\frac{\partial B_k}{B_k} \right) \tag{3.13}$$

A sample of the derivative needed above is

$$\begin{aligned} S_{B_1^p}^{\sigma'_{11}} = & \frac{-B_1^p (B_2^n - B_3^n)}{2[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]} (1 - \frac{\sigma'_{22}}{\sigma'_{11}}) \\ & + \frac{B_1^p B_3^n}{2[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]} (1 + \frac{\sigma'_{22}}{\sigma'_{11}}) \end{aligned} \tag{3.14}$$

The complexity of the interaction between stress and B coefficient variation is apparent in (3.14) and is hard to interpret, so the sensitivities have been investigated through numerical evaluation in the following sections. The complete set of stress sensitivities to piezoresistive coefficients appear in Appendix C.

In the following part of this chapter the uncertainties of the piezoresistive coefficients are discussed and then the discussion is extended to error analysis in order to include the sensitivities of the extracted stresses to errors in the measurement of the sensor resistances and temperature. Monte-Carlo simulation results yield estimates for errors due to uncertainty in sensor element measurements.

Sensitivity results are generated across the surface of a flip-chip die based upon finite-element simulation for a generic flip chip package configuration. The results are presented in two- and three-dimensional graphical form and demonstrate that the sensitivities are stress dependent and again vary widely from very small to very large over the die surface.

3.6 Finite Element Modeling

The finite element modeling of a flip chip package is performed in order to obtain the die stress distribution of a typical flip chip assembly. The die stress data from the finite element simulation was further used to calculate the sensitivity of the the piezoresistive coefficients to the extracted stress values. A drawing of the basic flip chip package to be modeled here appears in Fig. 3.5.

The simplified finite element model includes a 51 mm x 51 mm ceramic substrate, the 20 mm x 20 mm sensor die, and the under fill including its fillet. ANSYS® was used to obtain the stress distribution over the surface of the die resulting from cooling the die from its assumed stress-free state at 150°C to the room temperature of 25°C. The model assumed anisotropic and elastic properties for silicon, elastic properties for the ceramic, and temperature dependent elastic-plastic behavior for the under-fill material.

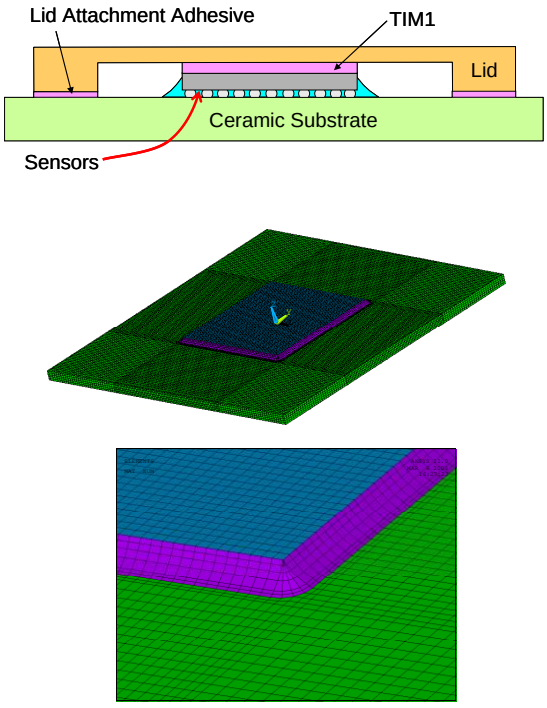


Figure 3.5 Flip-Chip Package and the Finite-Element Model

The resulting stress distributions appear in Figs. 3.6-3.8. For clarity in viewing the results of both the stress distributions and the stress sensitivity results, the data from the FEM simulations have been transferred to MATLAB for graphical presentation in both 2D contour plots and 3D surface plots. The finite element stress predictions can be combined with the analytical sensitivity formulas to generate plots of the sensitivities over the die surface.

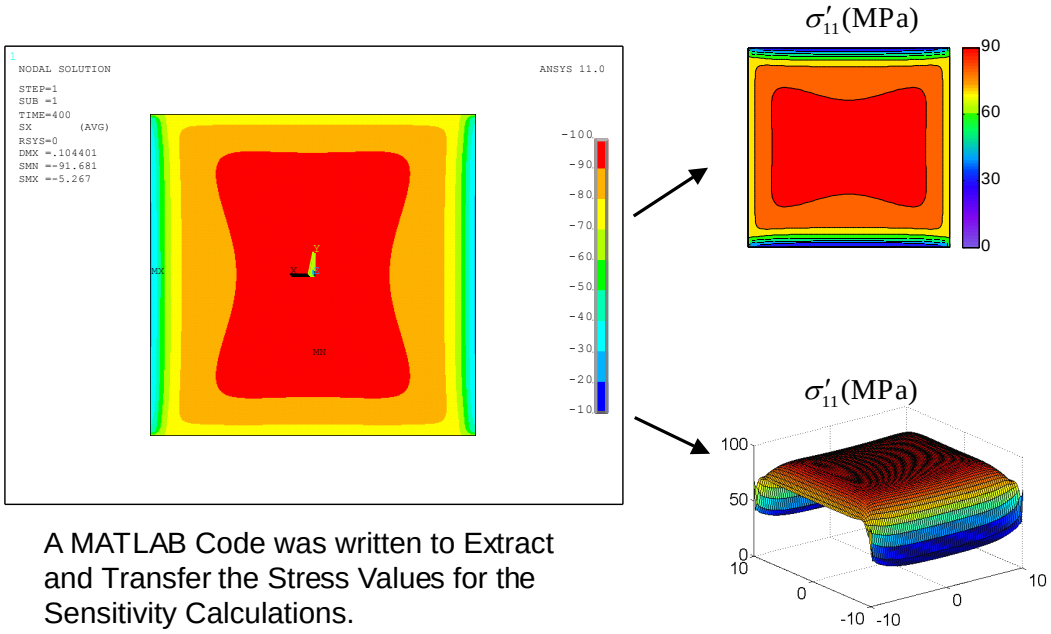


Figure 3.6 Simulation Results for σ'_{11}.

. Table 3.2 presents measured values of the piezoresistive coefficients utilized in the sensitivity calculations, and sample results are presented in Figs. 3.9-3.12.

Table 3.2 Typical Coefficient Data (^{o}C, 1/TPa, ppm/^{o}C)

T	B_1^n	B_2^n	B_3^n	B_1^p	B_2^p	B_3^p	α_1^p	α_1^n
300	-230	207	55	507	-145	-399	1800	2800

3.7 Discussion of Results

In Fig. 3.7, we observe that the in-plane normal stresses, σ'_{11} and σ'_{22}, are large in the center of the die, and tail off toward the edges of the die. The stress normal to the surface, σ'_{33}, is low over most of the die, but becomes large at the four corners since the die is being warped yielding high out-of-plane stress at the corners. In Fig. 3.8, one observes concentrations of all three shear stresses in the vicinity of the corners. Thus there are large variations of all the individual stresses across the die surface, which will lead to significant variations of the stress sensitivities as well.

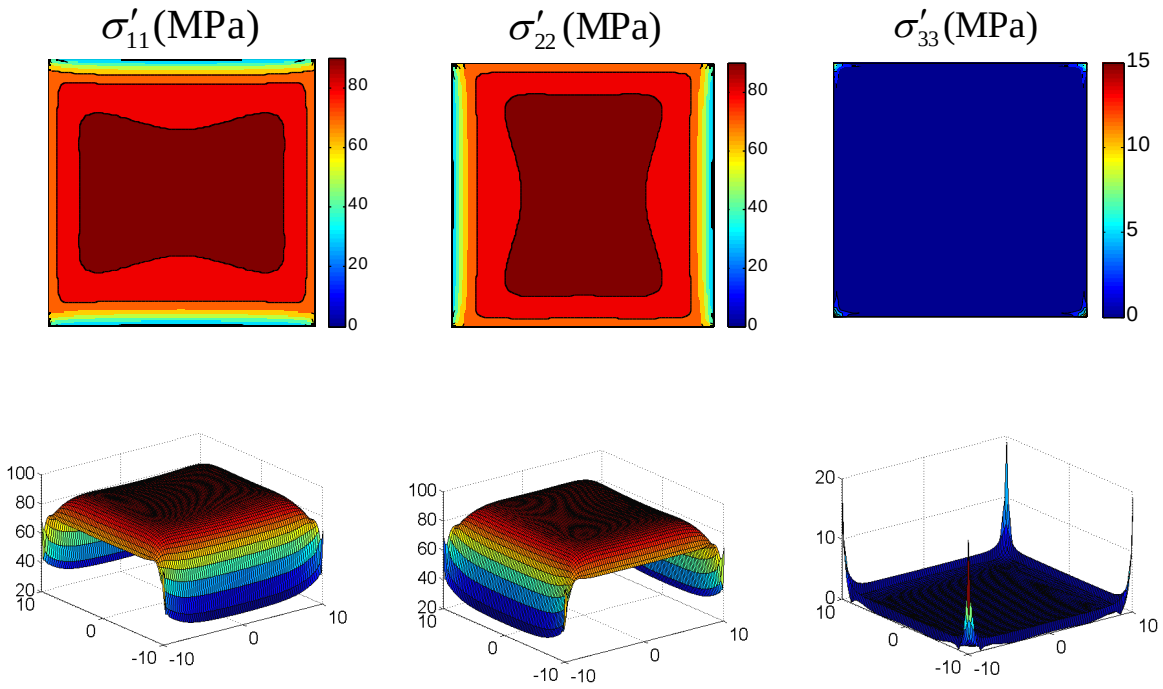


Figure 3.7 Simulated Normal Stress Fields on the Die Surface

3.7.1 Review of Piezoresistive Coefficient Sensitivities

Graphs of selected plots of the stress sensitivities appear in Figs. 3.9 - 3.12. High sensitivity suggests regions where errors will most likely occur during measurements. A sensitivity of 10 indicates that a 10% error in a coefficient leads to a 100% error in the

stress estimate, so small sensitivities are most desirable. Sensitivities of less than 2 or so are acceptable, whereas those above 5 are becoming problematic.

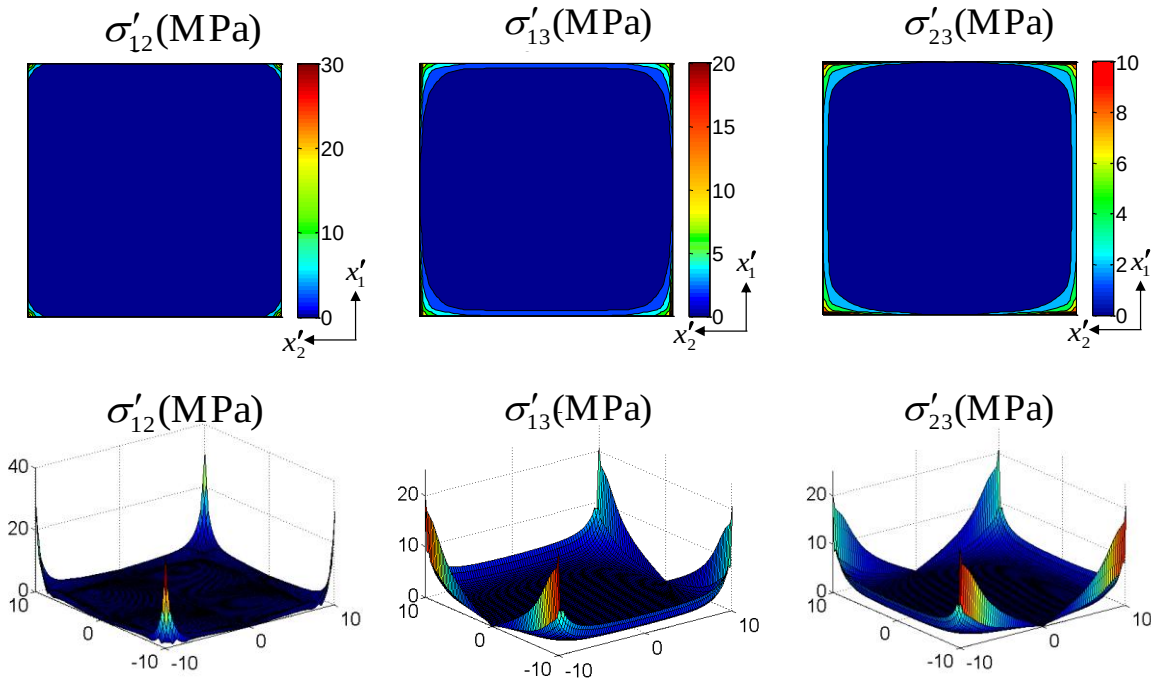


Figure 3.8 Shear Stress Fields Across the Die

In Fig. 3.9, we find sensitivities of σ'_{11} to B_1^n and B_2^n ranging from 5 to 15 that should raise a flag. A similar result occurs in Fig. 3.10 for σ'_{22}. We must expect relatively wide data spreads and error bars for in-plane normal stress measurements. From Fig. 3.9(c), we see a small sensitivity to the B_3^n coefficient across the whole die. This is encouraging because measurement of the small B_3^n is quite difficult and has many sources of possible error.

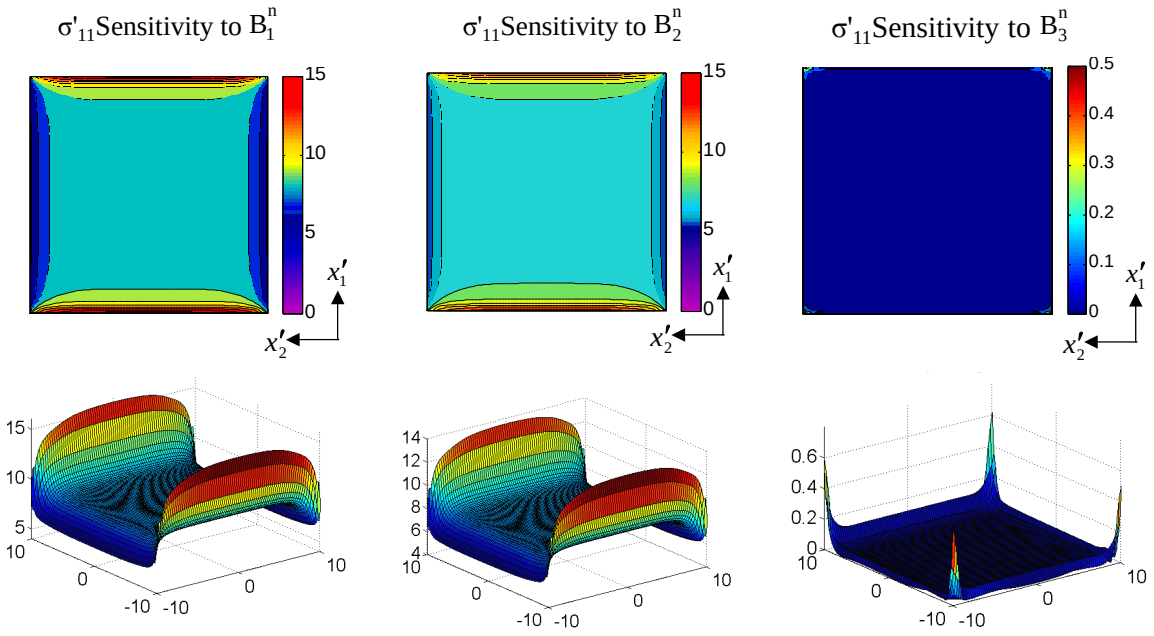


Figure 3.9 Sample Sensitivities of the In-Plane Normal Stress σ'_{11} to Errors in Various B Parameters

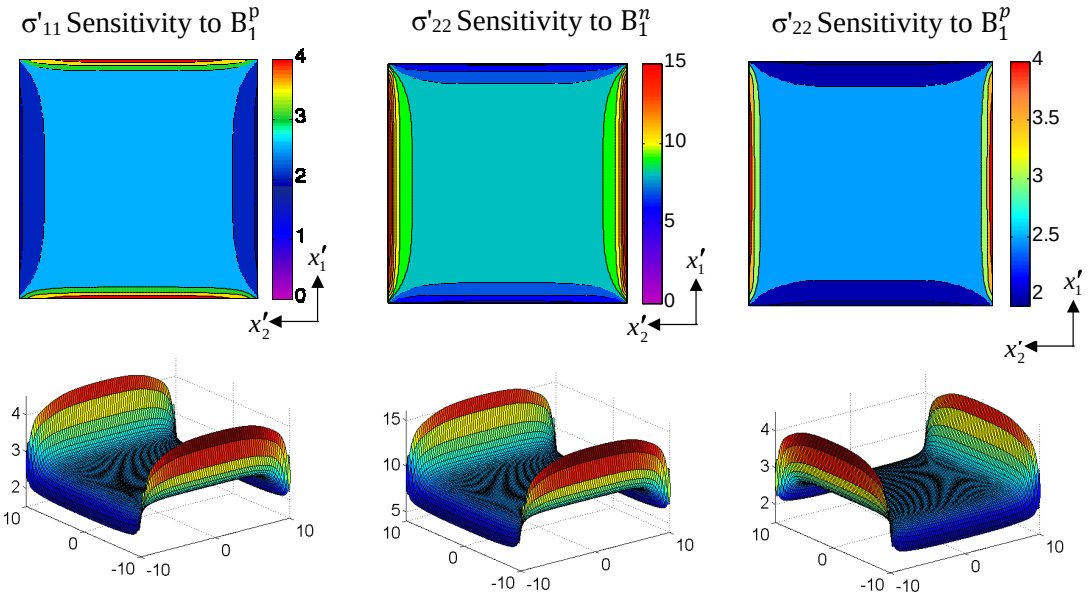


Figure 3.10 Sample Sensitivities of the In-Plane Normal Stresses σ'_{11} and σ'_{22} to Errors in B Parameters.

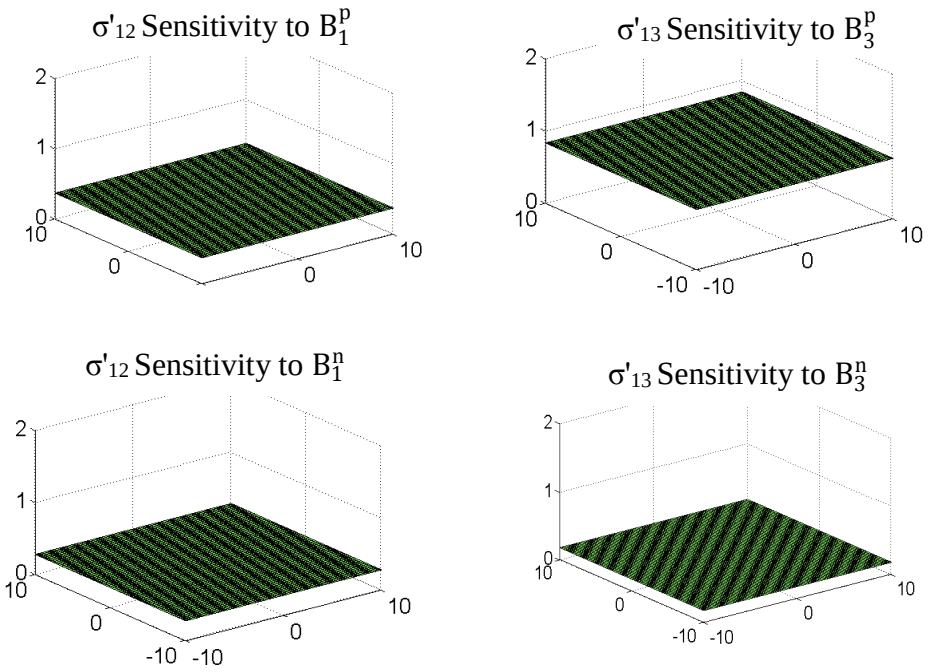


Figure 3.11 Sensitivity of Shear Stresses (Temperature Compensated) to Errors in Various B Parameters.

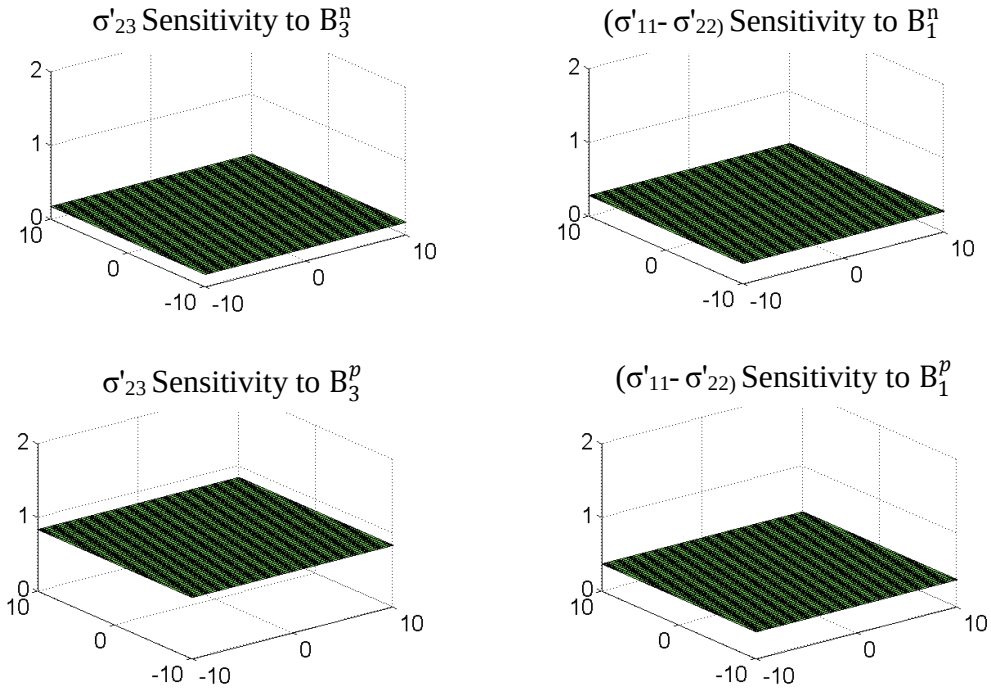


Figure 3.12 Sensitivity of Shear Stresses (Temperature Compensated) to Errors in Various B Parameters.

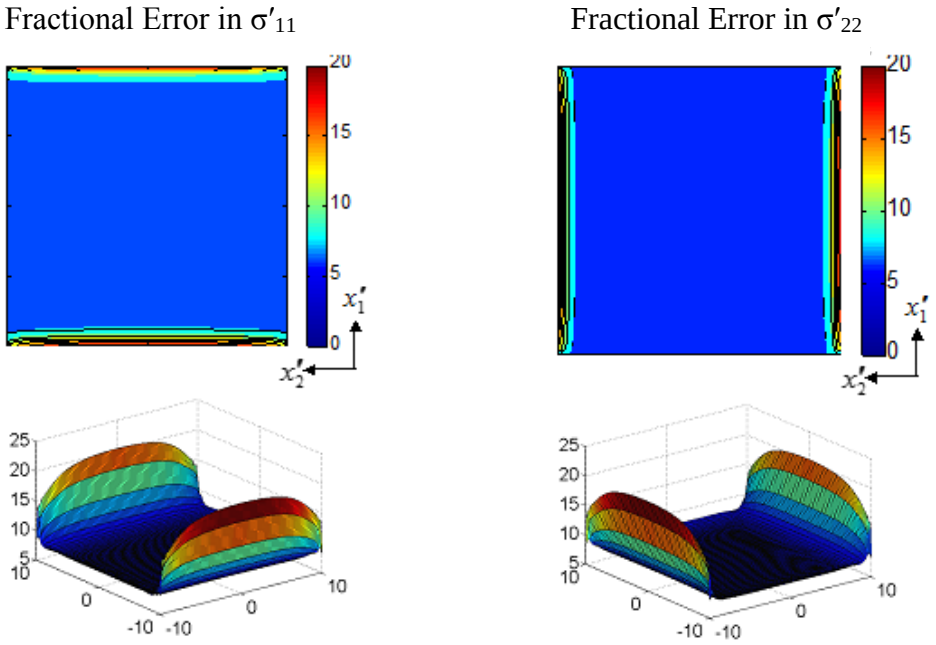


Figure 3.13 Fractional Errors for In-Plane Normal Stresses to a 5˚K Temperature Error at 300 K Showing High Sensitivity Across the Die.

The sensitivities in the first and third parts of Figure 3.10 are mostly between 2 and 4 and are relatively low, whereas those in the second part are relatively large. Figure 3.11 and 3.12 presents samples of the sensitivities to piezoresistive coefficient variation for the temperature compensated stresses that can be measured using the (111) rosettes. Here we observe very low sensitivities across the whole die for each case.

Figure 3.13 shows the high sensitivity of the in-plane normal stresses to temperature measurement errors, another indicator of the importance of strict control of temperature and other errors that may mimic temperature errors [79, 81].

Table 3.3 presents complete sets of calculations of the sensitivities at two points on the surface of the die, one at the die center (3.3-A) and one at the center of the edge of the die (3.3-B).. For the cases highlighted in italics (and green) in Table 3.3 A and 3.3 B,

the sensitivities are small, whereas those in bold (and yellow) range from not good to terrible.

Table 3.3 Stress Sensitivities with respect to Errors in the "B" Coefficients and Temperature								
Table 3.3 A- Magnitudes Near Die Center								
		B_1^n	B_2^n	B_3^n	B_1^p	B_2^p	B_3^p	T
σ'_{11}		**8.54**	**7.70**	*0.00*	2.60	*0.74*	*0.00*	**373**
σ'_{22}		**8.54**	**7.70**	*0.00*	2.60	*0.74*	*0.00*	**373**
σ'_{33}		**253000**	**228000**	1.86	**35400**	**10100**	*0.85*	**10^7**
σ'_{12}		*0.28*	*0.34*	*0.02*	*0.37*	*0.14*	*0.10*	*0*
σ'_{23}		**4.47**	**3.38**	*0.17*	**6.61**	1.59	*0.83*	*0*
σ'_{13}		2.06	2.49	*0.17*	**3.04**	1.17	*0.83*	*0*
$\sigma'_{11}- \sigma'_{22}$		*0.28*	*0.21*	*0.01*	*0.37*	*0.09*	*0.05*	*0*
$\sigma'_{11}+ \sigma'_{22}$		**8.55**	**7.69**	*0.00*	2.60	*0.74*	*0.00*	**373**
Table 3.3 B - Magnitudes Near Center of Die Edge								
σ'_{11}		**5.85**	**4.91**	*0.00*	1.91	*0.47*	0.00	**469**
σ'_{22}		**15.5**	**13.9**	*0.04*	**4.36**	1.29	0.09	**1210**
σ'_{33}		**1920**	**1730**	*1.86*	**269**	**76.8**	0.86	**145000**
σ'_{12}		*0.28*	**5.39**	*1.37*	*0.37*	*2.26*	**5.93**	*0*
σ'_{23}		1.52	2.01	*0.17*	2.25	*0.94*	*0.83*	*0*
σ'_{13}		*0.03*	*0.67*	*0.17*	*0.05*	*0.32*	*0.83*	*0*
$\sigma'_{11}- \sigma'_{22}$		*0.28*	*0.37*	*0.03*	*0.37*	*0.15*	*0.14*	*0*
$\sigma'_{11}+ \sigma'_{22}$		**8.55**	**7.70**	*0.01*	2.60	*0.74*	*0.01*	**676**

. A couple of observations can be made from Table 3.3 A. For example, the sensitivities of σ'_{11} and σ'_{22} to B_1^n is 8.54 which indicates that a 10% error in B_1^n can lead to 85% error in the calculated values of σ'_{11} and σ'_{22}. The high sensitivities to temperature in the individual normal stresses are also evident. A very high sensitivities were noted for σ'_{33}, which is very small at the middle of the die. Therefore, the sensitivity data indicates that the measurement of $\sigma'_{33}$is very difficult. The sensitivities of the temperature

compensated stresses to the piezoresistive coefficients in general show lower sensitivities. A number of the sensitivities are large even in the case of the temperature compensated shear stresses especially for σ'_{23} and σ'_{13}.

A second case that is representative of the stress in the middle of one side of the die appears in Table 3.3 B. Here, only a 1% error in B_1^n or B_1^p may lead to significant errors in σ'_{22} and σ'_{33}. The high sensitivities to B_1^n or B_1^p arise because, for typical values, they nearly cancel each other in the denominator of the sensitivity expression. These high sensitivities are a further argument for making temperature compensated measurements whenever possible. Tables 3.3 A and 3.3 B both indicate there will be difficulty in obtaining accurate values for σ'_{33}.

Coefficients B_3^n or B_3^p are the most difficult to measure accurately, requiring the use of hydrostatic pressure or some other technique. Fortunately, the sensitivities to errors in these coefficients are all relatively small. Note that the very high sensitivities to temperature have been discussed in references [79, 81]. One must be careful when using sensitivities as we can observe from those for σ'_{33}. Sensitivity S can become large when a stress is small since σ'_{33} is used as a normalization factor. The results further indicate the difficulty of measuring small stresses in region in which other stresses are large. This problem can also be inferred from the resistance change equations.

Since all the B parameters will be in error, the sum of the magnitudes of a given row is also significant. Using the chain rule,

$$\frac{\Delta\sigma'_{ij}}{\sigma'_{ij}} = \frac{1}{\sigma'_{ij}}\left[\sum_k \frac{\partial\sigma'_{ij}}{\partial B_k}\Delta B_k\right] = \sum_k S_{B_k}^{\sigma'_{ij}}\frac{\Delta B_k}{B_k} \qquad (3.15)$$

Table 3.4 presents the results of a worst - case evaluation of Eq. (3.15) by summing the magnitudes of the results assuming a 5% error in each coefficient and a 1-K temperature error at T = 300 K. Here we see that significant percentage errors can occur in extraction of all the stresses due to parameter uncertainty. The best case is that the temperature compensated in-plane terms, (σ'_{11}- σ'_{22}) and σ'_{12}.

Table 3.4 Fractional Error - Worst Case Total

Stress	Die Center	Die Edge
σ'_{11}	2.2	2.2
σ'_{22}	2.2	5.8
σ'_{33}	61400	682
σ'_{12}	0.1	0.8
σ'_{23}	0.9	0.4
σ'_{13}	0.05	0.1
σ'_{11}- σ'_{22}	0.1	0.1
σ'_{11}+ σ'_{22}	2.2	3.2
$\Delta B/B = 0.05$ and $\Delta T/T = 1/300$		

3.7.2 Sensitivities to Temperature Measurement Errors

The values for the derivatives of the normal stresses (σ'_{11}, σ'_{22}, σ'_{33}) with respect to temperature appear in Table 3.5. The values are on the order of 100 MPa/^{o}C! Thus, a 0.1 degree error in measuring temperature will make a 10 MPa error in the stress extraction. The other stresses are temperature compensated and have zero derivatives.

3.7.3 Sensitivities to Resistor Measurement Errors

Values for the derivatives of stress with respect to resistor values expressed in MPa/% appear in Table 3.6 based upon the data in Table 3.1. The values for the

temperature dependent stress extractions are high, whereas those for the temperature-compensated calculations are low. For example, a 1% measurement error in R_1 causes a 180 MPa error in the extracted value of σ'_{11}. These derivatives are used in the Monte Carlo analysis in the next section.

Table 3.5 Derivatives with Respect to Temperature

	T	Value (MPa/^{o}C)
σ'_{11}	$\frac{-\alpha_1^n B_3^p + \alpha_1^p B_3^n}{D_2}$	-113
σ'_{22}	$\frac{-\alpha_1^n B_3^p + \alpha_1^p B_3^n}{D_2}$	-113
σ'_{33}	$\frac{\alpha_1^n\left(B_1^p + B_2^p\right) - \alpha_1^p\left(B_1^n + B_2^n\right)}{D_2}$	-93.7
σ'_{13}	0	0
σ'_{23}	0	0
σ'_{12}	0	0
$\sigma'_{11} - \sigma'_{22}$	0	0

Table 3.6 Derivatives of Stress with Respect to Errors in Measured Resistor Values $\frac{\partial \sigma'_{ij}}{\partial \Delta R_k / R_k}$ (MPa/%)

		R_1	R_2	R_3	R_4	R_5	R_6	R_7	R_8
σ'_{11}		**180**	0	**192**	0	**29.2**	0	**22.0**	0
σ'_{22}		**192**	0	**180**	0	**22.0**	0	**29.2**	0
σ'_{33}		**-8.61**	0	**-8.61**	0	**10.7**	0	**10.7**	0
σ'_{12}		0	5.49	0	-5.49	0	3.68	0	-3.68
σ'_{23}		5.49	0	5.49	0	3.68	0	-3.68	0
σ'_{13}		0	-6.04	0	6.04	0	3.62	0	-3.62
σ'_{11}- σ'_{22}		-12.1	0	12.1	0	7.23	0	-7.23	0
σ'_{11}+ σ'_{22}		372	0	372	0	51.2	0	51.2	0

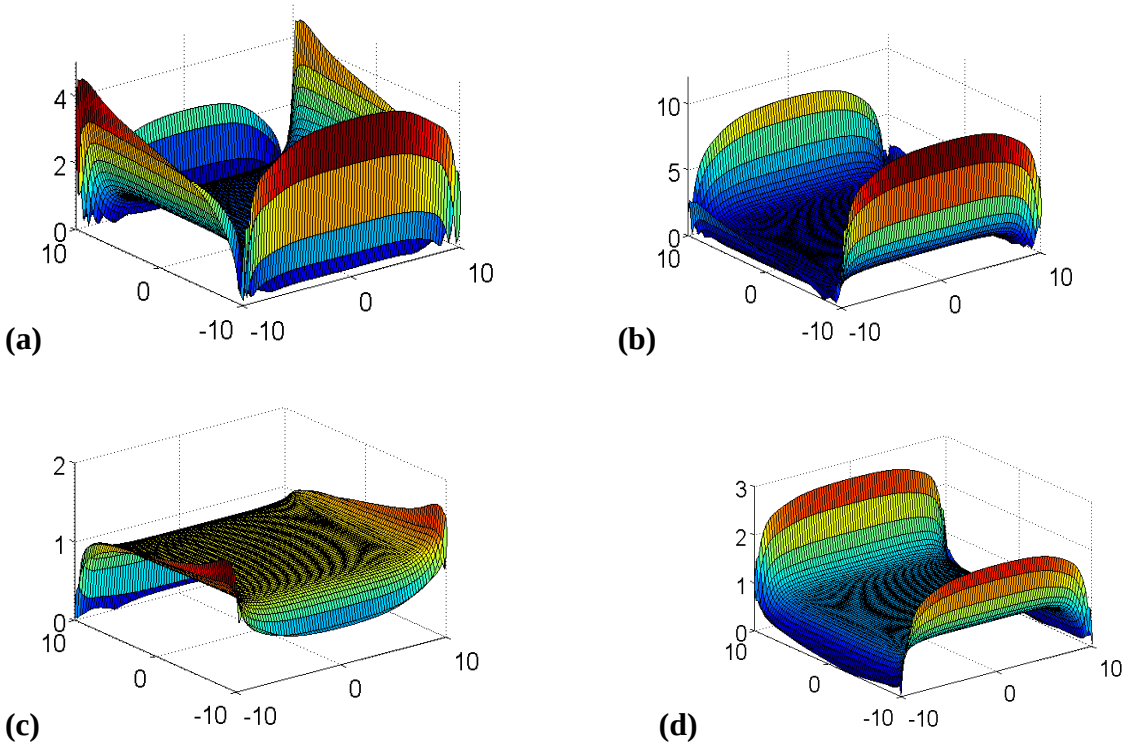


Figure 3.14 Sample Sensitivities of σ'_{11} with respect to Errors in
(a) $\Delta R_1/R_1$ (b) $\Delta R_3/R_3$ (c) $\Delta R_5/R_5$ (d) $\Delta R_7/R_7$

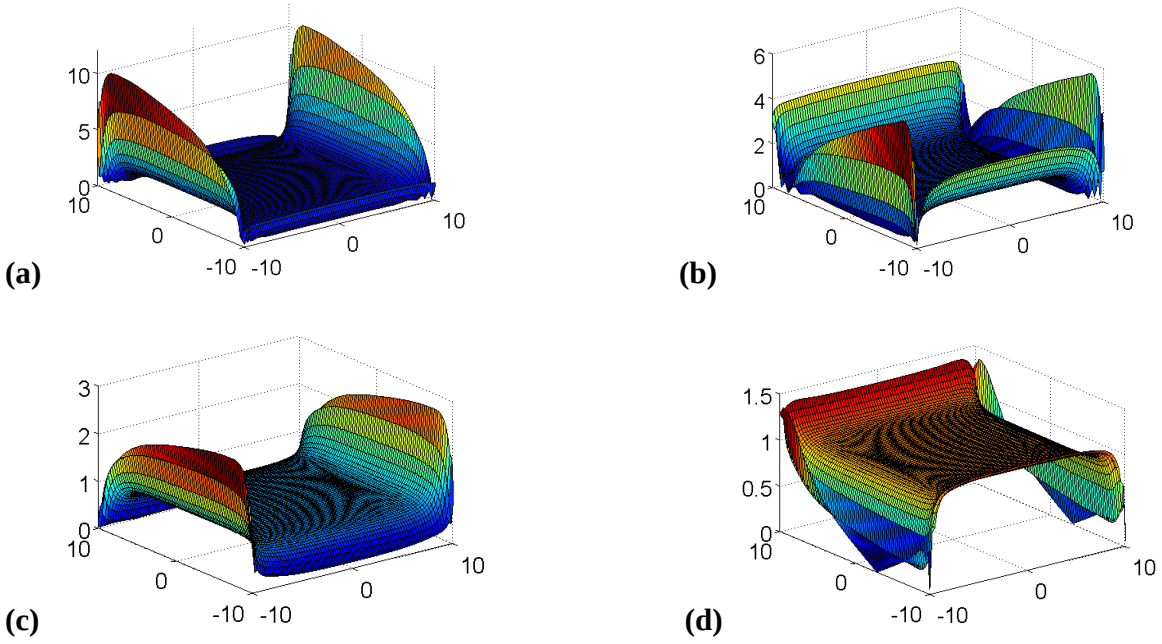


Figure 3.15 Sample Sensitivities of σ'_{22} with respect to Errors in
(a) $\Delta R_1/R_1$ (b) $\Delta R_3/R_3$ (c) $\Delta R_5/R_5$ (d) $\Delta R_7/R_7$

Examples of the sensitivities to resistor measurement error are plotted in Figs. 3.14-3.15 using expressions similar to Eq. (3.10) and the simulated stress distributions. These results are similar to those for the piezoresistive coefficients and exhibit wide variation across the wafer and from stress to stress. The sensitivity of σ'_{11} with respect to R_3 is a problem along the edges where σ'_{11} is small. Similarly, the sensitivity of σ'_{22} with respect to R_1 is a problem along the edges where σ'_{22} is small.

3.7.4 Monte Carlo Analysis

Monte Carlo analysis is an experimental probabilistic method for determining the sensitivity of a system by considering the variables that effect that system within statistical limits of those variables. In an experiment, some of the parameters that determine the data of the experiment can contain uncertainties in their values and their values can be distributed within their maximum and minimum limit. In such case it is highly unlikely for all the parameters of an experiment to reach their maximum uncertainty limit at the same time and vice versa. The analysis based on all randomly varying parameters attaining the extremes at the same time is referred to as worst- case analysis technique and this technique often results in conservative analysis of the experimental result and that may prove to be expensive due to the overestimation of the parameters of the experiment. Another way of dealing with experiments with randomly distributed parameters is a statistical method referred to as Monte Carlo analysis which is quite complex but yield in a satisfactory result. During dealing with uncertainties of the parameters in data estimation, random values of the parameters are used in the analysis within their uncertainty space instead of a single calculation that is performed in straight

forward methods. Such analysis yields closer approximation of the measurement data that are probabilistic in nature.

The way the analysis works is that it uses random values of each of the parameters of an experiment which is selected from the possible distributions of parameters to statistically predict the behavior of the experiment. Multiple cases of such prediction of the experiment are generated by random selection of its parameters and a probabilistic nature of the experiment is established from the analysis of several test cases. Usually a computer program is generated to carry on the Monte Carlo simulation capable of generating random numbers for the parameters. The flowchart of the Monte Carlo analysis is shown in Fig 3.16.

For calculation of overall uncertainty, the errors associated with all the variables of an experiment are needed to be specified. An error is usually expressed by a probability distribution function or by its mean value and its standard deviation. We can obtain additional insight into the expected errors caused by imprecise resistor measurement by using Monte Carlo analysis to estimate the errors in stress extraction caused by various levels of uncertainty in the measured values of the resistances. Using the chain rule,

$$\Delta\sigma'_{ij} = \sum_{1}^{8} \frac{\partial\sigma'_{ij}}{\partial R_i}\Delta R_i = \sum_{1}^{8} \frac{\partial\sigma'_{ij}}{\partial \dfrac{\Delta R_i}{R_i}} \frac{\Delta R_i}{R_i(0,0)} \tag{3.16}$$

For the Monte Carlo simulation, the factional errors in the resistor values are chosen randomly assuming uniformly distributed values. In our experiments, we have observed maximum deviations of approximately 0.05% in the resistor measurements

with 6 digit multi-meters, and these have been used in the uniform random value generation. The results appear in Table 3.7 for a small 100-case simulation.

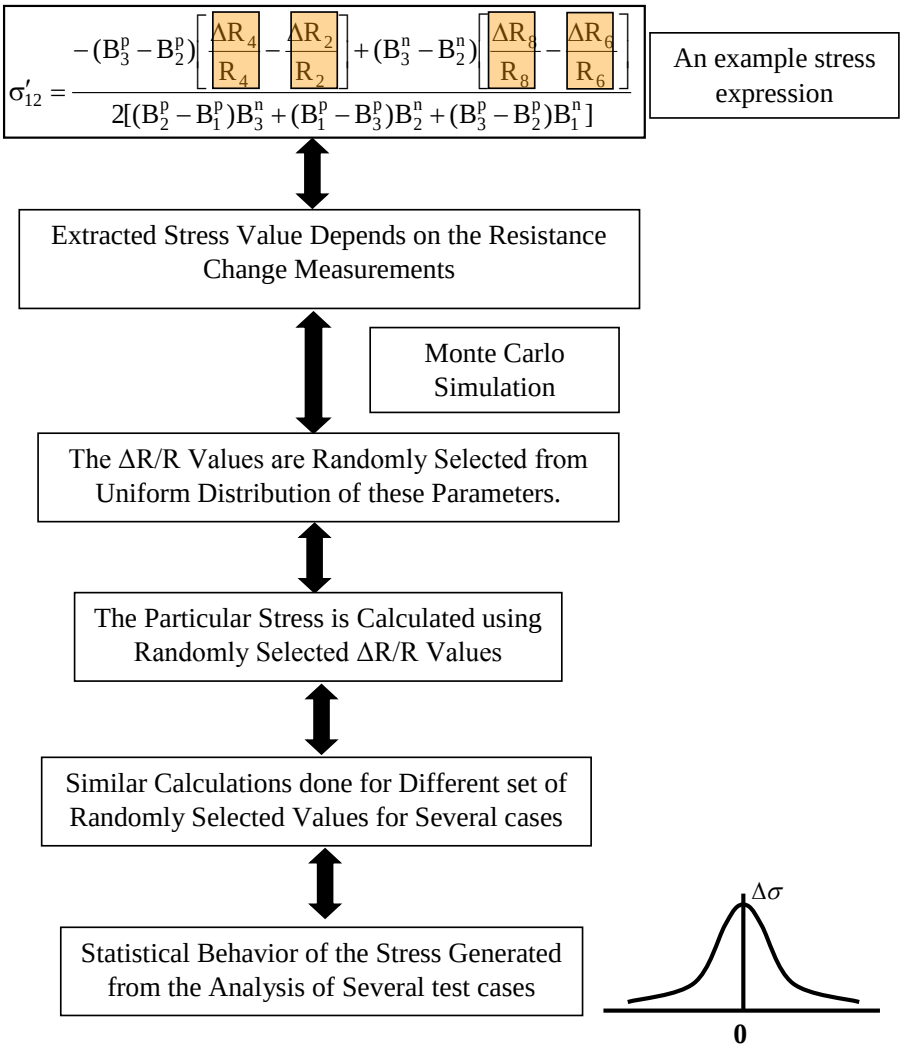


Figure 3.16 Monte Carlo Process Steps

The averages are small as they should be since the random resistor values have zero mean. The standard deviations for the temperature compensated stresses are a fraction of 1 MPa with maximum and minimum values a factor of two larger. The non-

temperature compensated stress have much higher sensitivities, and these result in larger errors in σ'_{11} and σ'_{22}. However, since these two in-plane stresses are often relatively large (100 MPa and greater), the errors are still not severe. Based upon these results, it appears that errors due to resistor measurement errors are entirely manageable.

Table 3.7 Monte Carlo Results 100 Cases (MPa)

	σ'_{11}- σ'_{22}	σ'_{12}	σ'_{23}	σ'_{13}	σ'_{11}	σ'_{22}	σ'_{33}
Average	0.0025	0.0068	0.029	0.014	0.53	0.035	0.035
St. Dev.	0.60	0.30	0.28	0.28	7.8	7.9	0.54
Minimum	-1.3	-0.69	-0.62	-0.50	-17	-16	-1.4
Maximum	1.2	0.74	0.68	0.67	17	16	1.4

3.8 Summary and Discussion

Multi-element resistor rosettes on silicon are widely utilized to measure integrated circuit die stress in electronic packages and other applications. Previous analyses of many sources of error have led to rosette optimization and the realization that temperature compensated stress extraction should be used whenever possible. This chapter has discussed the errors that occur in stress extraction due to the inherent uncertainty in knowledge of the values of the piezoresistive coefficients as well as measurement errors associated with measurement of rosette resistor values and temperature for stresses corresponding to a die in a flip chip package.

Expressions for the sensitivity of extracted stress to resistor measurement, temperature measurement and piezoresistance coefficient measurement errors have been presented and discussed. Monte Carlo simulations have been utilized to estimate the expected errors in stress measurements of a silicon die mounted in a typical flip chip package due to the resistance measurement error. The results presented here show the

sensitivities to be stress dependent and to vary widely over the die surface and that the temperature compensated stress terms generally tend to have low sensitivity to measurement uncertainty, although this is not true for every case. Therefore, further studies must be directed towards optimizing the multi-element sensor rosette (111) silicon to have lower sensitivities to the piezoresistance coefficient, temperature and resistance change value uncertainties.

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CHAPTER 4

CURRENT DEPENDENCE OF THE PIEZORESISTIVE COEFFICIENTS OF MOSFETS ON (100) SILICON

4.1 Introduction

Piezoresistive stress sensors are widely used to monitor mechanical stresses developed on the chip and to package during its operation. These sensors offer non-intrusive and real time measurement of stresses, and they can be fabricated on the chip using the prevailing microelectronic fabrication technology. Because of the advantage of measuring stress on a chip in packaged condition, it has been successfully utilized to monitor chip and package health and reliability over period of time. Implanted or diffused resistor sensors are most prevalent stress sensors which are fabricated at suitable locations on the surface of the die. These sensors are not mounted like traditional strain gauges rather they are fabricated on the surface of the die, hence an integral part of the die. The problems associated with resistor sensors are that they occupy large area in the chip in order to have reasonable resistor values. As a result, they cannot provide localized stress value and can only provide an average stress distribution over the area of the sensor. These sensors are often highly doped which causes low sensitivity of these devices.

Metal-oxide-semiconductor (MOS) transistors on (100) silicon are excellent stress sensors because of their advantages of smaller size, high sensitivity due to lighter doping, operable in wide temperature range over the traditional resistor sensors. The resistive

channel of the MOS transistor can be utilized as piezoresistive element. They can be used as sensor arrays that can provide high-resolution mapping of stress across the surface of specially designed test die [88, 130, 195]. Optimized piezoresistive FET (PiFET) rosettes on (100) silicon make use of the two largest piezoresistive coefficients (pi-coefficients), Π_{44}^{p} of PMOS devices and Π_{D}^{n} of NMOS devices, to measure the in-plane normal stress difference $(\sigma'_{11} - \sigma'_{22})$ and the in-plane shear stress σ'_{12} on the surface of the silicon wafer, thereby providing highly localized stress measurements with high sensitivity[129]. However, the MOS pi-coefficients of the sensor rosettes have typically been evaluated at only one operating point without any real data to guide the choice of operating conditions.

This chapter presents new results for the operating point dependence of the piezoresistive coefficients of PMOS and NMOS devices. Uniaxial stress is utilized to calibrate both the normal stress difference and shear stress sensors, and the piezoresistive coefficient values are characterized as a function of drain current thereby providing the information necessary to make appropriate operating point choices for the design of CMOS stress sensors. From a more fundamental point of view, it is shown that the magnitude of the Π_{44}^{p} exhibits a direct correlation with the PMOS channel mobility, whereas Π_{D}^{n} exhibits a nonlinear relation to NMOS channel mobility.

4.2 Metal Oxide Semiconductor Transistors

This section contains an overview of a metal oxide semiconductor field effect transistor (MOSFET). It is the most widely used device in IC circuits. Fig. 4.1 shows a schematic structure of two types of MOSFETs; NMOS and PMOS. As the figure indicates, this transistor consists of diffused or implanted regions of source and drain, an

SiO_2 insulator, a channel region and a gate. The source and the drain as the names indicate are the sources of the electrons/holes and provides a drain for those carriers respectively. The gate is insulated from the silicon substrate by a high quality insulator usually SiO_2. The surface potential of the silicon is determined by the gate voltage and by applying proper gate voltage, an inversion layer can be created in the region between source and drain with an electric field through the gate oxide that determines the conduction through the transistor. Based on operation of these transistors at zero gate-source voltage, they can be classified as either depletion-mode or enhancement-mode transistors. In depletion-mode device, at zero gate voltage the device is in the ON state and in enhancement-mode device the transistor is OFF at zero gate voltage. Depletion-mode devices contain an conductive channel region which can be depleted through an application of a gate voltage. Enhancement-mode devices do not contain a built in channel, rather conduction of carriers occur by developing a channel region by applying an appropriate gate voltage. Most silicon transistors are enhancement-mode transistors.

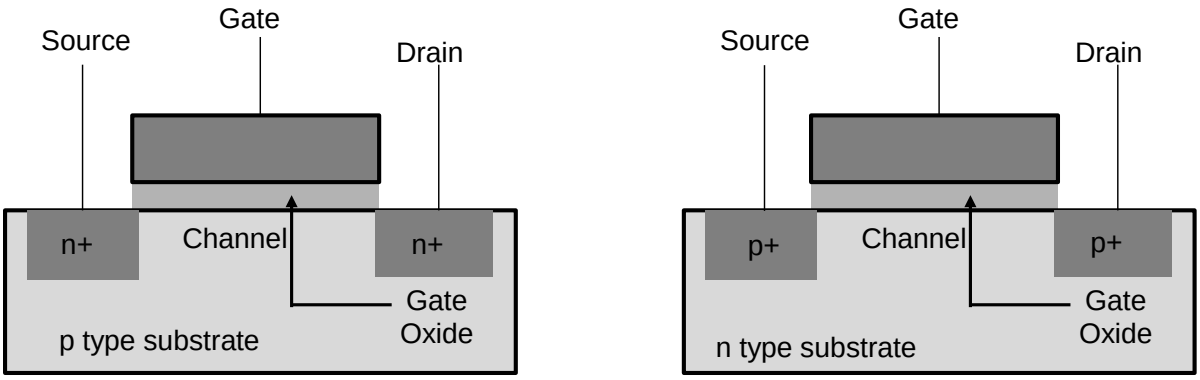


Figure 4.1 Schematic Diagram of an NMOS (left) and PMOS (right) Transistors

The threshold voltage, V_T of a transistor corresponds to the minimum gate-source voltage V_{GS} that is required to generate conduction of carriers from the source to drain

terminals. For an enhancement mode FET, depending upon the voltages at the terminals, there are three different operational regions, cutoff, linear and saturation regions. These three different operation mode are discussed in the following:

Cutoff Region:

The cutoff region occurs when the gate-source voltage V_{GS} is less than the threshold voltage $V_{T.}$ In this operation mode only a small leakage current flows through the device and the transistor is basically considered to be turned off.

Linear Region:

The linear region of the transistor is entered when the gate-source voltage is above threshold voltage (V_{GS}> V_T) but still below the value required for saturation, that is (V_{GS} -V_T)>V_{DS}, where V_{DS} is drain–source voltage. In this region the transistor is turned on and a charge rich inversion layer is formed between the source and drain terminals that allows conduction of current between the source and drain. If the drain to source voltage is increased by a small amount, the conducting current will increase linearly. In linear region the transistor acts as a variable resistor which is modulated by the gate voltage. The drain current in the linear region is expressed as:

$$I_{DN} = K_n\left(V_{GS} - V_{TN} - \frac{V_{DS}}{2}\right)V_{DS} \quad \text{for NMOS}$$
$$\text{and } I_{DP} = K_p\left(V_{GS} - V_{TP} - \frac{V_{SD}}{2}\right)V_{SD} \quad \text{for PMOS} \tag{4.1}$$

where K_n and K_p are the transconduction parameters defined as

$$K = \mu_n \frac{\varepsilon_{ox}}{T_{ox}} \frac{W}{L} \tag{4.2}$$

where V_{TN} and V_{TP} are the NMOS and PMOS threshold voltages of the transistor, μ_n and μ_p are the electron mobility and hole mobility respectively, T_{ox} is the oxide thickness,ε_{ox} is the dielectric constant of the oxide layer and W and L are the width and length of the channel, respectively.

Saturation (Pinch Off) Region.

The transistor operates in the saturation region when the drain voltage exceeds the saturation voltage that is $V_{DS} \geq (V_{GS} - V_T)$. The increase of drain voltage causes the depletion region from the surrounding to make the channel near the drain to narrow down and that will cause reduction of charge carrier density. As the drain current increases, the channel will be totally "pinched off" from the drain region indicating lack of channel region near the drain. However, the current through the device will still continue to conduct even with the pinch off because the high electric field between the drain and the channel causes charges to be swept through the depletion region into the drain. In the saturation region, the DC drain current has a weak dependence on drain voltage and is modulated predominantly by the gate-source voltage. The expression for drain current in the saturation region can be expressed as:

$$I_{DN} = \frac{K_n}{2}\left(V_{GS} - V_{TN}\right)^2 (1 + \lambda_n V_{DS}) \quad \text{for NMOS}$$
$$\text{and } I_{DP} = \frac{K_p}{2}\left(V_{GS} - V_{TP}\right)^2 (1 + \lambda_p V_{SD}) \quad \text{for PMOS} \tag{4.3}$$

where λ_n and λ_p are the channel length modulation parameters that model the current dependence on the drain voltage.

4.3 Piezoresistive MOS Sensors

The theory of piezoresistance effect in MOSFETs that describes the relation between transistor response and applied stress is explained in Appendix A. The conduction of the carriers through the channel determined by the resistive region of the channel when the transistor is operated in strong inversion in either linear or saturation region. The normalized change in drain current due to stress for a MOSFET on (100) silicon in strong inversion can be written [134] as

$$\begin{aligned}\frac{\Delta I_D}{I_D} = &\left[\frac{\Pi_S + \Pi_{44}}{2}\sigma'_{11} + \frac{\Pi_S - \Pi_{44}}{2}\sigma'_{22}\right]\cos^2\phi \\ &-\left[\frac{\Pi_S - \Pi_{44}}{2}\sigma'_{11} + \frac{\Pi_S + \Pi_{44}}{2}\sigma'_{22}\right]\sin^2\phi \\ &-\Pi_{12}\sigma'_{33} - \Pi_D\sigma'_{12}\sin 2\phi + f(T)\end{aligned} \tag{4.4}$$

Conceptual layouts of the optimized PMOS and NMOS stress sensor rosettes [130, 134] appear in Fig. 4.2 where the (0-90°) PMOS transistor pair measures the difference in the in-plane normal stresses (σ'_{11}-σ'_{22}), and the (±45°) NMOS pair measures in-plane shear stress s¢. The stresses are resolved along the x'_1andx'_2axes defined for the (001) silicon wafer in Fig. 4.3.

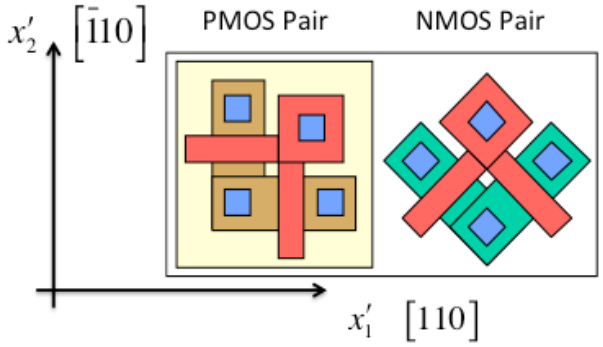


Figure 4.2 Conceptual Layouts of 0/90° PMOS and ±45° NMOS Stress Sensors on (100) Silicon

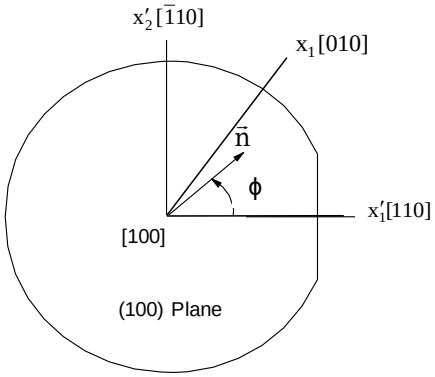


Figure 4.3 (001) Silicon Wafer Coordinates

The stated angles indicate the channel orientation relative to the [110] wafer axis. Stresses and pi-coefficients are both determined from fractional changes in the pairs of drain currents for the circuits in Fig. 4.4, assuming saturation region operation:

$$\begin{aligned} \frac{\Delta I_{90}}{I_{90}} - \frac{\Delta I_0}{I_0} &= \Pi_{44}^{p}\left(\sigma'_{11} - \sigma'_{22}\right) \quad \text{for PMOS} \\ \frac{\Delta I_{45}}{I_{45}} - \frac{\Delta I_{-45}}{I_{-45}} &= 2\Pi_{D}^{n}\sigma'_{12} = 6\Pi_{S}^{n}\sigma'_{12} \ \text{ for NMOS} \end{aligned} \tag{4.5}$$

These circuits provide differential measurements, so transistor temperature dependencies cancel out in these expressions. As mentioned in the introduction, the PMOS and NMOS transistor pairs in the "optimized" FET rosettes are chosen totake advantage of the largest piezoresistive coefficients based upon the classic values for bulk silicon in Table 4.1.

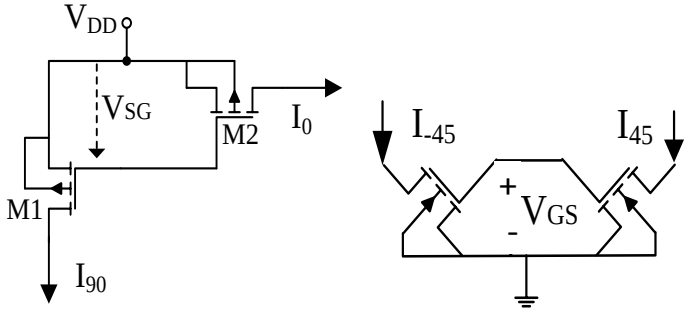


Figure 4.4 PMOS (left) & NMOS (right) Sensor Circuits

Table 4.1 Classic Piezoresistive Coefficients for Lightly-Doped Silicon from C. S. Smith [23]		
Coefficient	n-type Si (1/TPa)	p-type Si (1/TPa)
π_{11}	-1020	+66
π_{12}	+534	-11
π_{44}	-136	+1380
$\pi_S = \pi_{11} + \pi_{22}$	-488	+55
$\pi_D = \pi_{11} - \pi_{22}$	-1560	+77

It can be observed from (4.5) that Π_{44}^{p} is easily determined by applying a controlled uniaxial stress σ'_{11} in a four-point-bending fixture, for example. However, shear stress σ'_{12} is more difficult to apply to the transistors in a controlled manner. Fortunately the ±45° NMOS devices also respond to in-plane uniaxial stress σ'_{11}, for example,

$$\frac{\Delta I_{45}}{I_{45}} = \frac{\Delta I_{-45}}{I_{-45}} = \frac{\Pi_S^n}{2}\sigma'_{11} + \alpha_n \Delta T \tag{4.6}$$

in which α_n is the temperature coefficient of the NMOS device. The required pi-coefficient can be estimated from $\Pi_D^n = 3\Pi_S^n$ based upon well-known theoretical results for electrons in silicon ($\pi_{11} = -2\pi_{12}$) [50]. With this assumption, the necessary pi-coefficients can be obtained without the need for additional off-axis devices [80], assuming that temperature change ΔT is controlled during the measurement.

4.4 Experimental Method

For this work, sensors were fabricated in a standard 180 nm CMOS foundry process. The calibration results for pi-coefficients were obtained from wafer strips containing sensors bonded to a flexible circuit that connects to a semiconductor

parameter analyzer through an interface box as shown in Fig. 4.5. The detail of the measurement system is discussed in Chapter 5.

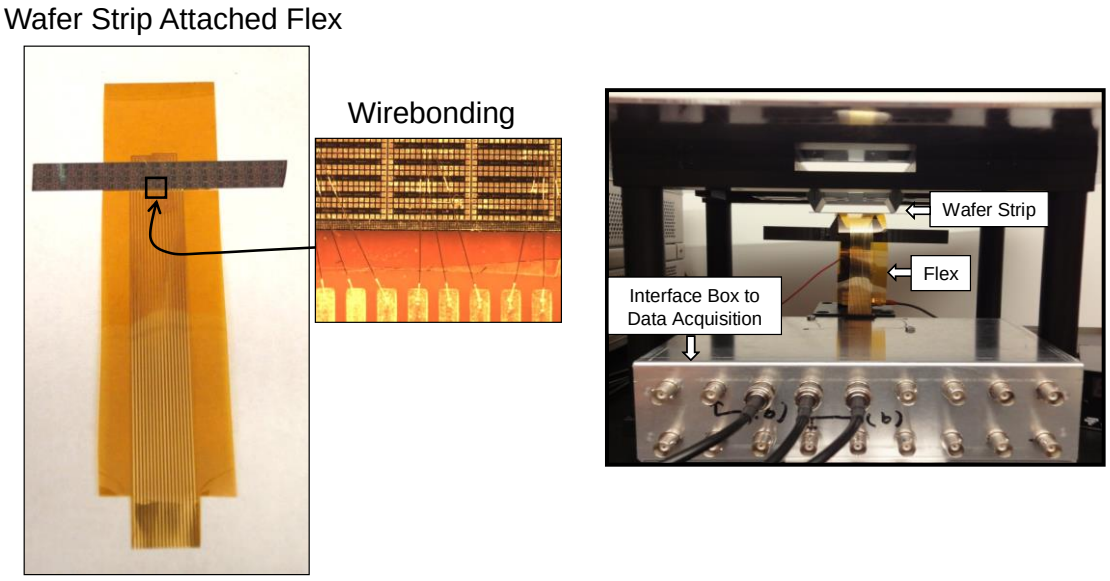


Figure 4.5 Flexible Circuit Used to Interface to Wafer Strip

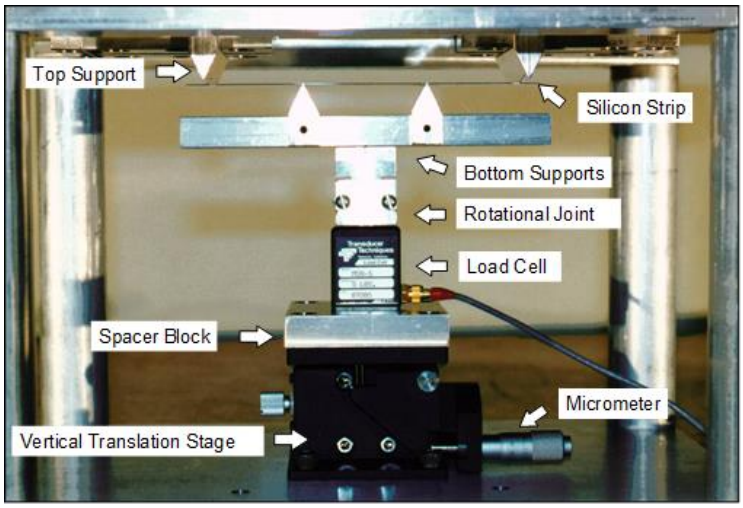


Figure 4.6 Four Point Bending Fixture

A four-point-bending fixture is used to apply uniaxial stress σ'_{11} along the x'_1 direction which is along the [110] crystal direction. The four point bending fixture that was used to apply uniaxial stress is shown in Fig. 4.6. Each transistor pair in Fig. 4.4 is biased in saturation with equal drain voltages (1.25 V), and the gate-source voltage is

swept over a range corresponding to strong inversion. A separate sweep is performed at each tensile stress from 0 to 75 MPa in 5 MPa increments. The stress responses have been verified to be the same for tensile and compressive stress that can be measured by turning the strip over in the fixture.

4.5 Experimental Results

Typical responses of the individual drain currents to stress at a fixed bias voltage appear in Fig. 4.7 in which the slopes of the two PMOS curves are $\left(\Pi_S^p + \Pi_{44}^p\right)/2$ and $\left(\Pi_S^p - \Pi_{44}^p\right)/2$ and that for the NMOS device is $\Pi_S^n/2$, corresponding to drain current of 490 µA for PMOS pair and 960 µA for NMOS pair.

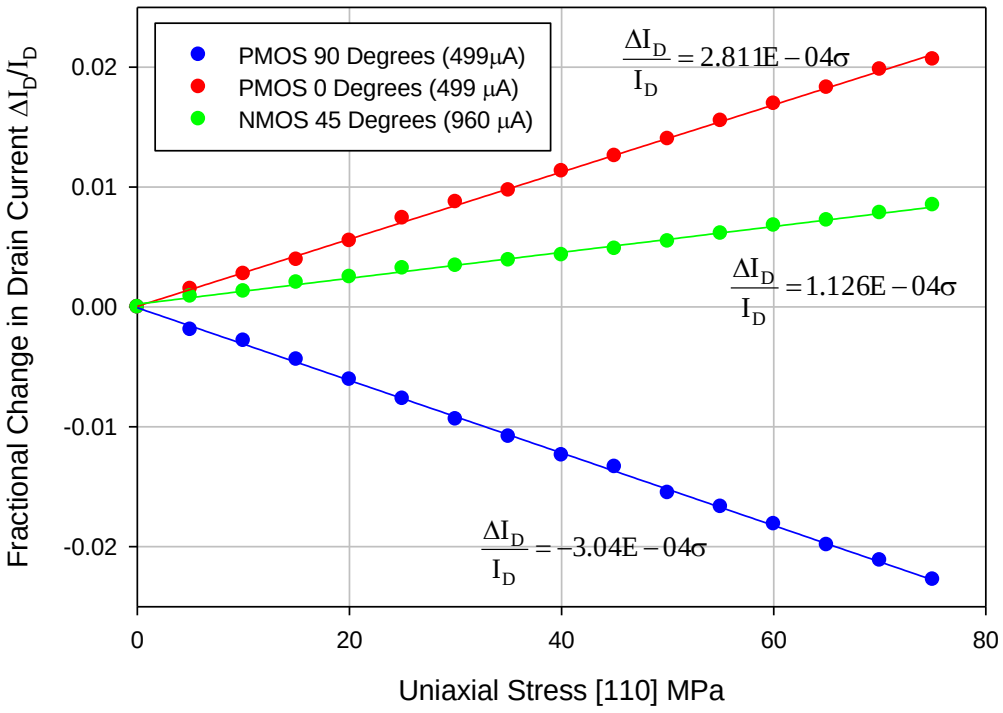


Figure 4.7 Typical Responses of the PMOS and NMOS Transistors

The slopes of the characteristics were calculated from the normalized drain current variations using least standard square methods:

$$\left(\Pi_S^p + \Pi_{44}^p\right)\Big/2 = +281/\text{TPa},$$

$$\left(\Pi_S^p - \Pi_{44}^p\right)\Big/2 = -304/\text{TPa},$$

$$\text{and } \Pi_S^n/2 = +113/\text{TPa}.$$

Theil-Sen estimation [196, 197], that is insensitive to "outliers," was also used but did not materially change the results. The sensor theory is based upon strong inversion operation, so the threshold voltages for the two sets of devices (V_{TN} = 0.44 V and V_{TP} = -0.37 V) were extracted from the linear region of the turn-on characteristics. The data here correspond to gate-source voltages ranging from 0 to 0.75 V.

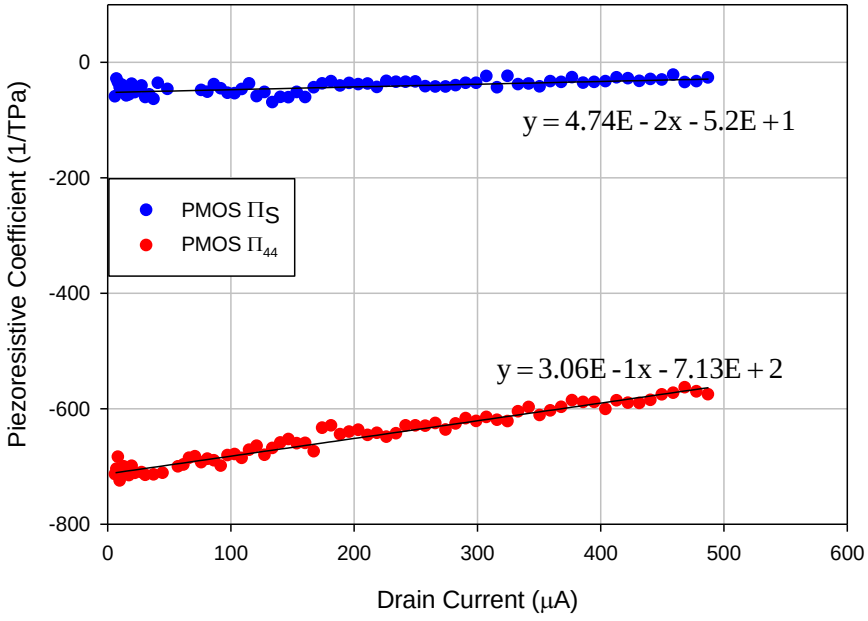


Figure 4.8 Extracted Values of Π_{44}^p and Π_S^p vs. PMOS Drain Current (Threshold Voltage -0.48 V at 5 μA of Drain Current)

4.5.1 PMOS Calibration Results

Addition and subtraction of the slopes of the PMOS responses yield values for pi-coefficients Π_{44}^{p} and Π_{S}^{p} as given in Fig. 4.8 for drain currents ranging from approximately 5 μA to 500 μA. Π_{44}^{p} and Π_{S}^{p} both exhibit a linear variation over the measured current range as described by

$$\Pi_{44}^{p} = -713 + 0.306\,I_D \quad \text{and}$$
$$\Pi_{S}^{p} = -52.0 + 0.0474\,I_D \qquad (4.7)$$

The magnitudes of both coefficients increase with decreasing collector current, as might be expected from the increasing channel mobility obtained at reduced gate fields. Although not actually needed for sensor use, Π_{S}^{p} is included here since it is obtained automatically from the extraction. The extracted values are reasonable based upon the doping levels in the channels. Note that the signs are opposite those in Table I since $I_D \propto \mu$ whereas $R \propto 1/\mu$. It should also be noted that Π_{44} characterization is a differential measurement, hence temperature and threshold variations cancel. However, Π_S extraction is a "common-mode" measurement, and threshold voltage, temperature and temperature coefficient variations can impact the results. The problems became very clear in attempts to extract the pi-coefficients in subthreshold where the FET temperature coefficients become very large. Extraction at lower currents is a topic for future work.

4.5.2 NMOS Calibration Results

Fig. 4.9 presents the results of extraction of $\Pi_D^n = 3\Pi_S^n$ for currents ranging from approximately 100 μA to 850 μA corresponding to a range of gate-source voltages from

0.65 to 1.15 V. Here we observe a stronger increase in the pi-coefficient values with the decrease in operating current that is well described by

$$\Pi_D^n = 3\Pi_S^n = 1211 - 1.349\,I_D + 8.242x10^{-4}\,I_D^2 \tag{4.8}$$

The current sweep is performed at one stress point, the stress is increased or decreased, and the next current sweep is performed. Measurement of the 16 stress points takes time, and as mentioned earlier, it is important that temperature be maintained constant during the NMOS calibration measurements. MOSFET temperature coefficient (TC) changes rapidly above and below the zero TC point as displayed in the graph of measured NMOS and PMOS TCs for currents from approximately 50 µA to 700 µA in Fig. 4.10. Rewriting Eq. (4.6),

$$\frac{\Delta I_{45}}{I_{45}} = \frac{\Delta I_{-45}}{I_{-45}} = \frac{\Pi_S^n}{2}\left(\sigma'_{11} + \frac{2\alpha_n}{\Pi_S^n}\Delta T\right) \tag{4.9}$$

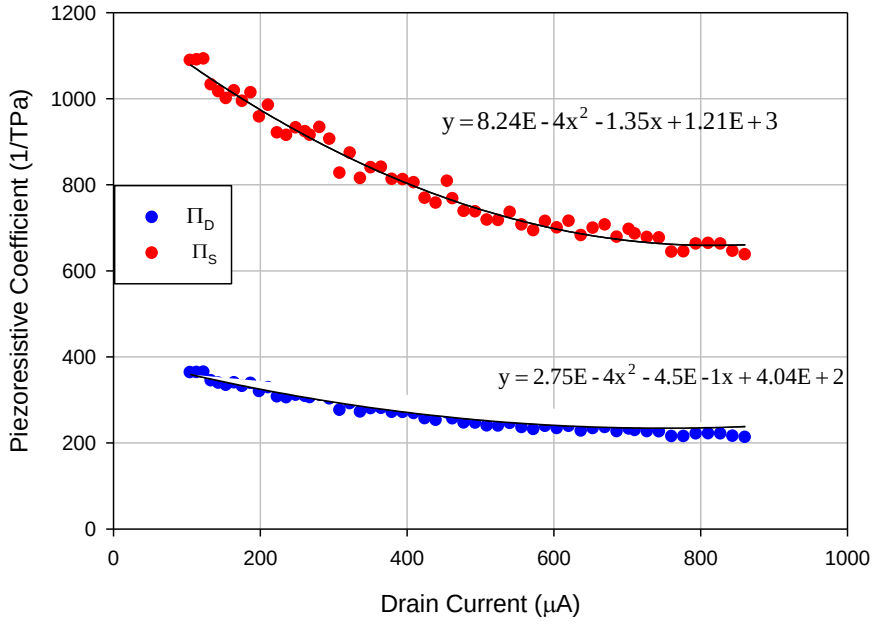


Figure 4.9 Extracted Π_S^n and Π_D^n vs. NMOS Drain Current
(Threshold Voltage 0.48 V at 3.5 µA of Drain Current)

For $|\alpha_n|$ = 2000 ppm/°C, the equivalent stress error is $2\alpha_n \left/ \Pi_S^n \cong 10\,\text{MPa} \right/ {}^{\circ}\text{C}$. Temperature was carefully monitored during the calibration measurements and fluctuations were maintained below ±0.1 °C corresponding to an equivalent stress error of ±1 MPa. Thus the results in Fig. 4.9 are presented only for TCs below 2000 ppm/°C.

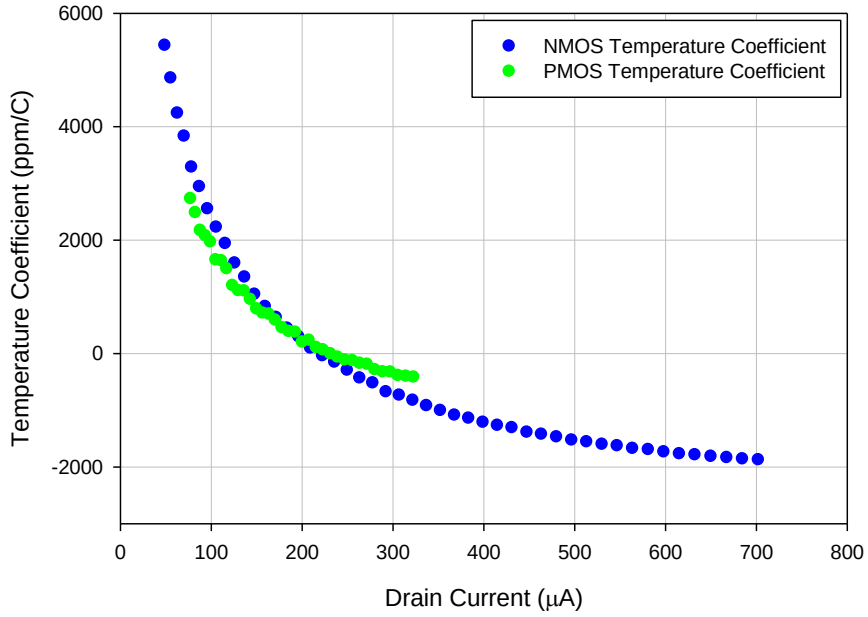


Figure 4.10 Measured NMOS and PMOS TCs vs. Drain Current

4.6 Correlation with Mobility

As noted, both Figs. 4.8 and 4.9 indicate that higher stress sensitivity is obtained by operating at low current levels. One expects the bulk silicon piezoresistive coefficient to be directly correlated with the underlying value of mobility itself [188]. Because of the scattering mechanisms involved, it is not clear whether to expect a similar relation between FET channel mobility and the PiFET sensitivities.

The relationship between the PiFET coefficients and mobility has been explored using the universal mobility expressions from Chen et al. [198]. The expression used for calculating electron and hole mobilities are presented in Eq. 4.10 and 4.11. The T_{ox} for PMOS transistor is 235 nm and for NMOS is 250 nm.

$$\mu_p = \frac{185}{1+\frac{1}{0.45}\left(\frac{V_{SG}-1.5V_{TP}}{7.5T_{OX}}\right)} \tag{4.10}$$

$$\mu_n = \frac{540}{1+\left(\frac{V_{GS}+V_{TN}}{5.4T_{OX}}\right)} \tag{4.11}$$

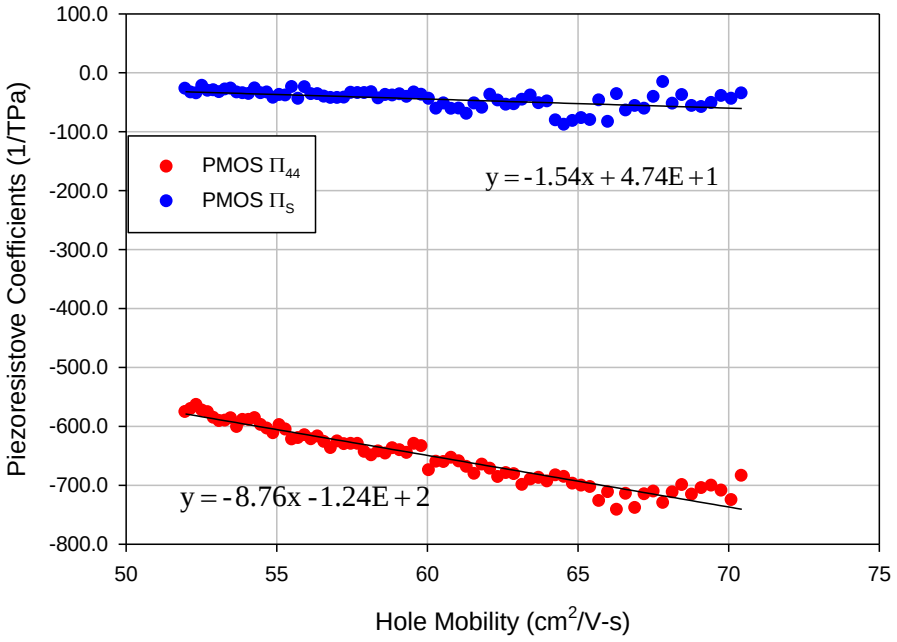


Figure 4.11 Π_{44}^{p} and Π_{S}^{p} vs. Hole Mobility in the PMOS Channel

Fig. 4.11 recasts the pi-coefficient data from Fig. 4.8 in terms of calculated hole mobility in the PMOS channel. For these strong inversion results, both PMOS

coefficients are directly proportional to mobility although the total variation in Π_S^p remains small.

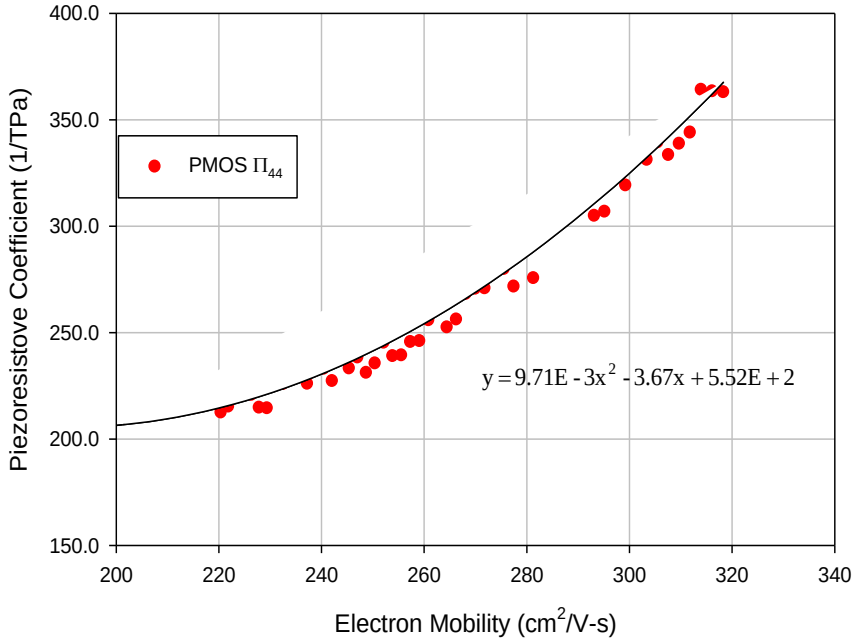


Figure 4.12 Π_S^n vs. Electron Mobility in the NMOS Channel

Fig. 4.12 presents a similar plot for the relationship between Π_S^n andthe electron mobilityin the NMOS channel. Here we again see a stronger dependence between the pi-coefficient and the electron mobility that is well described by a quadratic relationship over the range of measured data.

4.7 Summary and Discussion

This work has demonstrated that the piezoresistive coefficients of PMOS and NMOS devices vary significantly with choice of operating point and are strongly correlated with the underlying value of channel mobility. The stress sensitivity of the

PMOS devices was demonstrated to be linearly dependent on both operating current and mobility, whereas the NMOS sensitivity increased more rapidly as the current was reduced and exhibited a quadratic relation to electron mobility. Thus low current operation (i.e. low gate fields) achieves highest sensitivity, but it is important to note that the results presented here are valid only for strong inversion operation. The results for the variation of PMOS and NMOS piezoresistive coefficientsversus operating current can be used for both stress sensor design and analysis purposes, and are also useful in analysis of stress sensor pairs that have large initial mismatches and hence differing values for the pi-coefficients.

CHAPTER 5

CHARACTERIZATION OF THE IMPACTS OF MECHANICAL STRESS ON THE PERFORMACE OF BIPOLAR JUNCTION TRANSISTORS

5.1 Introduction

In this chapter, the response of bipolar junction transistors (BJT) to the controlled application of mechanical stress has been explored. Mechanical strains and stresses are developed during the fabrication, assembly and packaging of the integrated circuit (IC) chips. Due to these stresses and strains, it has been observed by many researchers that changes can occur in the electrical performance of both analog and digital devices. Mechanical stresses and strains can cause parametric shifts in the electronic components which change their electrical performance.Stress-induced device parametric shifts affect the performance of analog circuits that depend upon precise matching of bipolar and/or MOS devices, and can cause them to operate out of specifications. In this present work, the stress dependence of the electrical behavior of bipolar transistors has been investigated. Test structures have been utilized to characterize the stress sensitivity of vertical bipolar devices fabricated mostly on (100) silicon wafers and few on (111) silicon. In the experiments, uniaxial normal stresses were applied to silicon wafer strips using a four-point-bending fixture.

General strain effects in semiconductors can also be modeled using deformation potential theory as detailed in the monograph by Bir and Pikus [171]. This theory is

based on strain-induced changes in the energy bandgap, which results in alterations of the carrier concentrations and distribution of the carriers in the conduction and valance band valleys as well as the electron and hole mobilities. The bandgap in a crystalline semiconductor is the gap between the conduction band and valence band. The deformation potential theory states that the strain modifies the periodicity of the crystalline material and causes the conduction and valence band edges to shift from their positions, and deforms the band edge curvatures. This causes the carriers that fill up these bands to be rearranged in energy-momentum space, which changes the effective masses and as a result the mobilities of the carriers change. Detailed expressions for the shifts in conduction band and valance band potentials with strain, and the deformation of the shapes of these bands due to strain have been given in ref. [171].

Stress effects on devices that operate using conduction of majority carriers are often modeled using the piezoresistive effect smith [23, 69, 77, 88] Our research group and others have actively applied the phenomenological constitutive equations of piezoresistivity theory to study various electronic devices such as resistors [77-79, 81-85, 88], field effect transistors [90, 129-134], and van der Pauw structures [97]. Once the response of these devices to stress is well understood, they may be used as sensors to characterize silicon die stress in various packaged semiconductor chips [87, 92-96, 99-103, 105-118, 135].

The mechanical stress-induced phenomena in bipolar transistors have been referred to and modeled using the piezojunction effect [4, 136-146, 148, 150-159]. The effects of mechanical stress/strain on analog such as bipolar junction transistors in an integrated circuit chip have been explored to a lesser extent then MOS devices. However,

a number of recent investigations have been conducted by Creemer, Fruett, and co-workers [4, 150-159].

The bipolar transistor is distinct from other electronic devices because the electrical conduction involves the minority carriers, whereas in resistors and field-effect transistors the conduction is due to the majority carrier. The piezojunction effect occurs due to the changes in carrier mobility and the intrinsic carrier concentration which include both the conduction and the valence band carriers. The piezoresistive effect describes the variation of the resistivity components of the majority carriers with applied mechanical stress, whereas the piezojunction effect describes the stress dependence of the minority carrier conduction with stress. Creemer et al. [154-159] characterized effects of uniaxial normal stress on the saturation current of bipolar transistors, and obtained the piezojunction coefficients to correlate their experimental measurements with theory.

In bipolar junction transistors (BJTs), both bandgap and the attendant mobility variations affect various parameters including saturation current and DC current gain. Fig. 5.1 shows the effect of uniaxial stress on the normalized change in current gain of a bipolar transistor. The plot shows a 5% change in current gain for an applied stress of 100 MPa. Circuits containing bipolar transistors that are affected by stress include precision voltage references, op-amps, A/D and D/A converters, balanced mixers, VCOs and PLLs, etc. Experimental data for resistors and resistive channels of CMOS devices have demonstrated that their change in electrical characteristics can be explained by a linear piezoresistive effect that includes only first order stress effects. However, most data for bipolar transistors in the literature illustrate non-linear (quadratic) variations of saturation current and current gain with applied uniaxial stress (e.g. see Fig 5.1). In addition, the

nonlinear dependence on uniaxial stress has been observed to be different for tension and compression.

In this chapter, the response of bipolar junction transistors (BJT) to the controlled application of mechanical stress is discussed. Our overall objective is to develop a fundamental understanding of the influence of stress on precision analog devices/circuits. Test structures have been utilized to characterize the stress sensitivity of vertical bipolar devices fabricated on (100) and (111) silicon wafers. Uniaxial normal stresses were applied using a four-point-bending fixture to observe the changes in the electrical performance of the BJTs due to the stress. Utilizing the experimentally obtained data, the objective is to provide a theoretical model to explain the stress induced changes in the characteristics of BJTs.

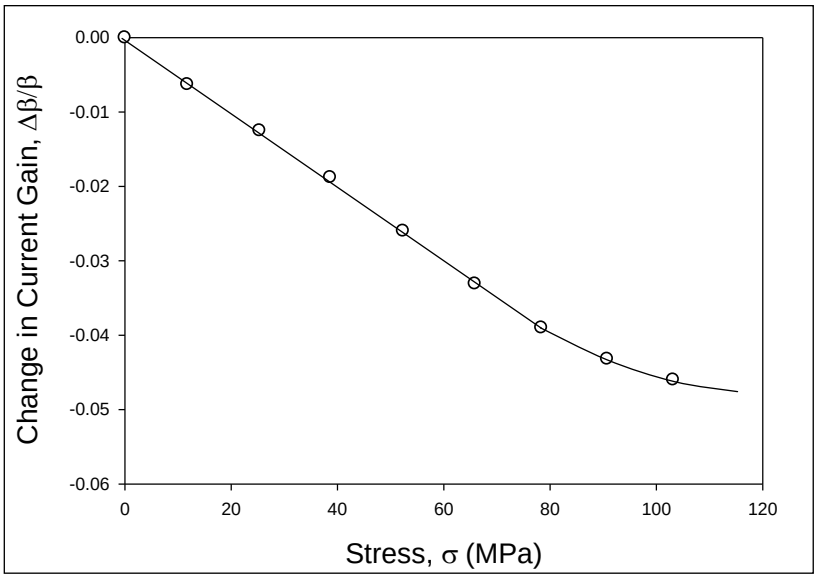


Figure 5.1 Normalized Change in Current Gain vs. Uniaxial Stress for a Vertical Bipolar Transistor

5.2 Bipolar Transistors

Bipolar transistors are electronic devices where electrical current conduction involves minority carriers. This vertical bipolar device is comprised of emitter, base and collector regions as shown in Fig. 5.2. The base region in the middle is narrow compared to the other two regions. Also, the doping in the base is always different from both the emitter and collector region. For example, if the base is p-type silicon, then the emitter and collector are n-type doped silicon. Depending on the doping type of the regions, bipolar devices can be either npn or pnp transistors. The emitter region is usually highly doped compared to the base and collector. For this transistor to operate in the forward-active region, the emitter-base junction is forward biased and the collector-base junction is reversed biased. With these conditions, electrons are injected from the emitter into the base region. The injected carriers diffuse and drift through the base into the collector, with very little recombination of the holes and electrons in the base since the base is usually very thin. Due to the forward bias across the emitter-base junction, there is also a small flow of holes in the opposite direction from the base into the emitter forming the majority of the base current. Thus, the current from collector-to-emitter for this mode of biasing is due to the electron transport across the base.

In a vertical bipolar transistor, the current flows perpendicular to the surface as shown in Fig. 5.2 where as in lateral transistors the current flows parallel to the surface as the name indicates. Vertical npn bipolar junction transistors are most widely used devices in semiconductor industry and they are optimized for high current gain and cut-off frequency, low values of Early effect and the emitter current crowding effect [150]. Because of the use of the substrate of a vertical pnp transistor as the collector region of

the transistor, these particular vertical pnp transistors are sometimes referred to as substrate pnp devices. Although not possessing a high current gain comparable to the vertical npn transistor, the vertical pnp bipolar transistors are frequently used as reference devices in analog circuits.

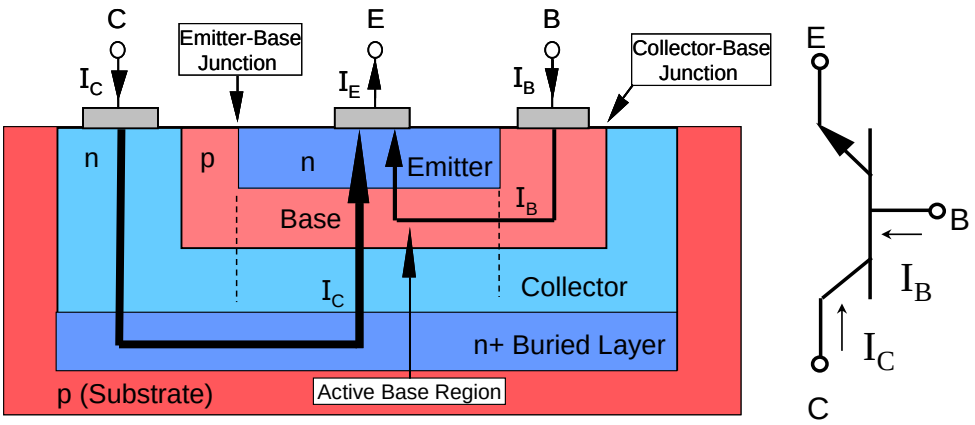


Figure 5.2 Simplified Schematic a Vertical npn Bipolar Transistor

For an ideal bipolar transistor, the collector and base currents I_C and I_B are related to the base-emitter voltage V_{BE} in forward bias using the exponential relation:

$$I_C = \beta I_B = I_S\left[\exp\left(\frac{qV_{BE}}{kT}\right)-1\right]\left(1+\frac{V_{CE}}{V_A}\right) \tag{5.1}$$

$$\beta = \frac{I_C}{I_B} \tag{5.2}$$

where β is the forward common-emitter DC current gain, I_S is the saturation current, q is the charge, k is the Boltzmann constant, and T is the absolute temperature. The DC current gain is an important performance parameter of a bipolar transistor and is the ratio of the collector current to the base current as shown in Eq. (5.2).

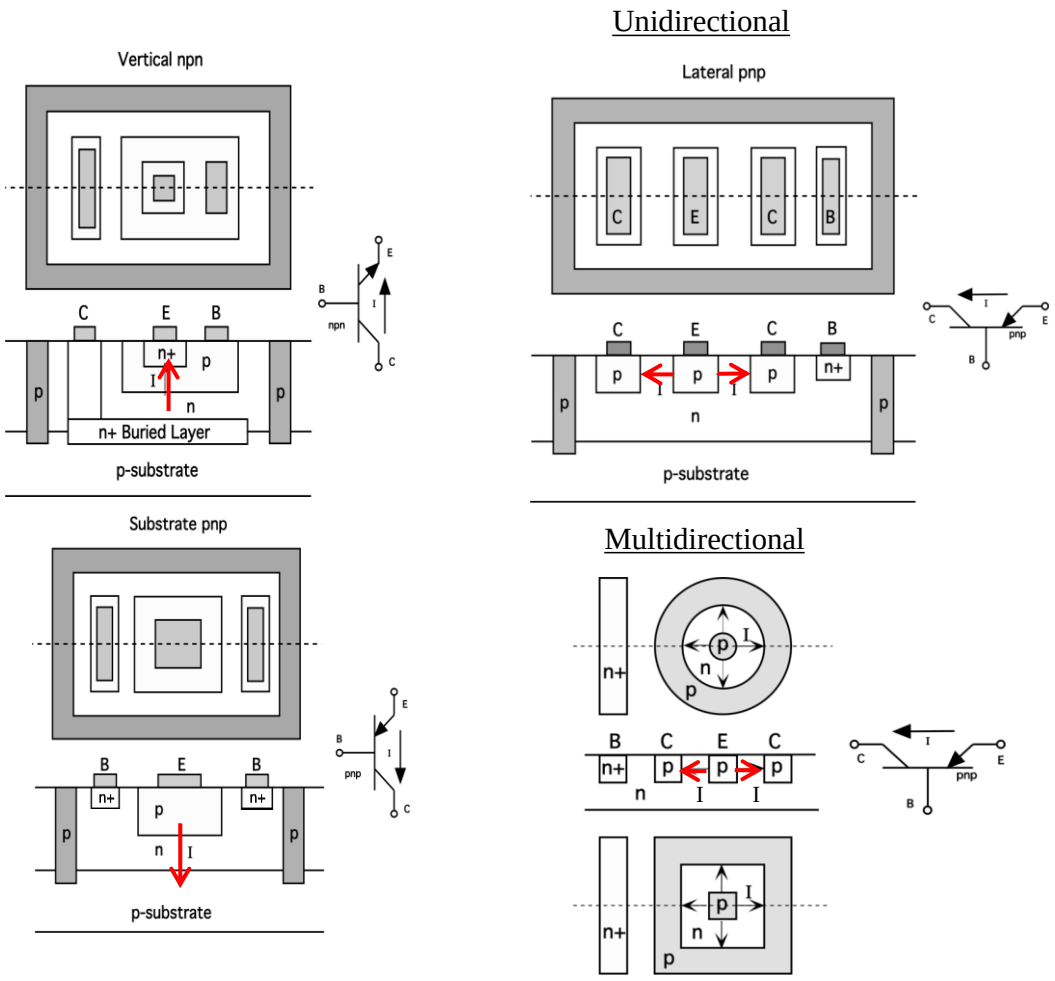


Figure 5.3 Vertical and Lateral Bipolar Transistors

The saturation current I_S of a bipolar transistor can be expressed using the following proportionality relationship:

$$I_S \propto \mu n_i^2 \quad \text{and} \quad n_i^2 \propto N_C N_V \exp\left(-\frac{E_G}{kT}\right) \tag{5.3}$$

where μ is the mobility, and n_i is the intrinsic carrier concentration. The intrinsic carrier concentration is related to the densities of states in the conduction and valance bands,

$N_C$and N_V, and is exponentially dependent upon the energy bandgap E_G. N_C and N_V are dependent upon the effective masses of the carriers and hence the energy band curvature.

Typical characteristic plots for an npn bipolar transistor are shown in Figs 5.4-5.6. Figure 5.4 contains the output characteristic plot for the transistor showing collector current I_C versus collector-emitter voltage V_{CE}. In this particular example, V_{CE} was swept from 0 to 1.0 V, and I_B was stepped from 2 μA to 10 μA, in steps of 2 μA. Fig. 5.5 illustrates the so-called Gummel plot for the transistor, which consists of a semi-log plot of the transistor currents collector current I_C and base current I_B versus the base emitter voltage V_{BE}. Such Gummel plots are obtained by sweeping V_{BE}, while keeping collector emitter voltage V_{CE} constant. The plot shows the typical region of operation where the current gain is approximately constant in value.

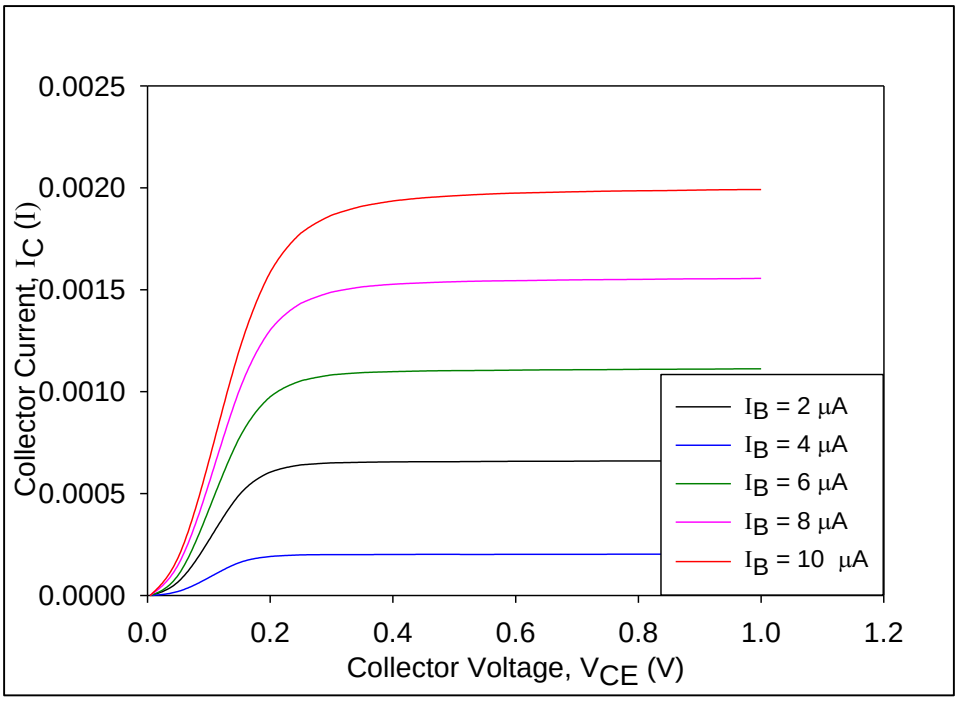


Figure 5.4 Output Characteristic Plot for a Bipolar Transistor

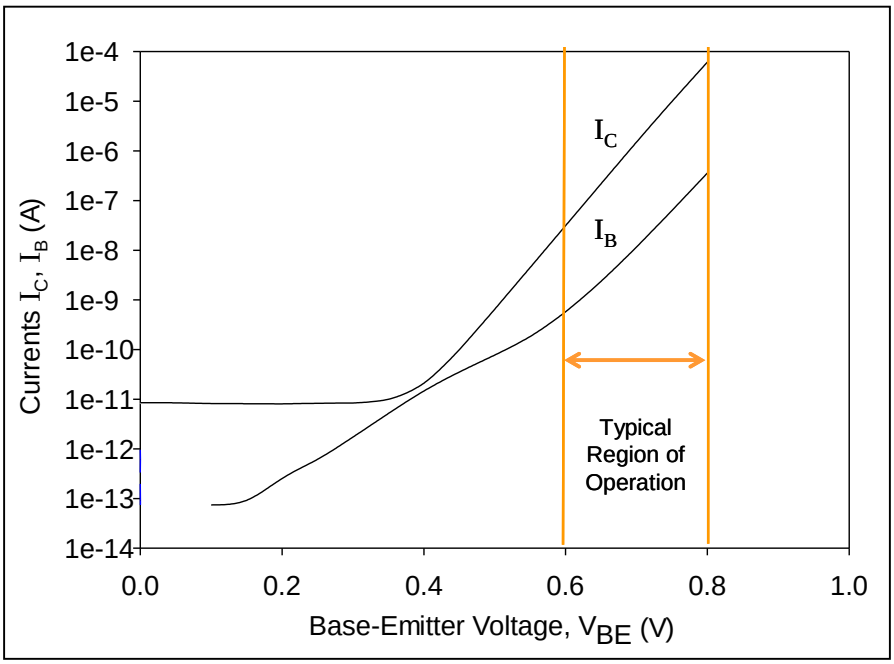


Figure 5.5 Gummel Plot for an npn Bipolar Transistor

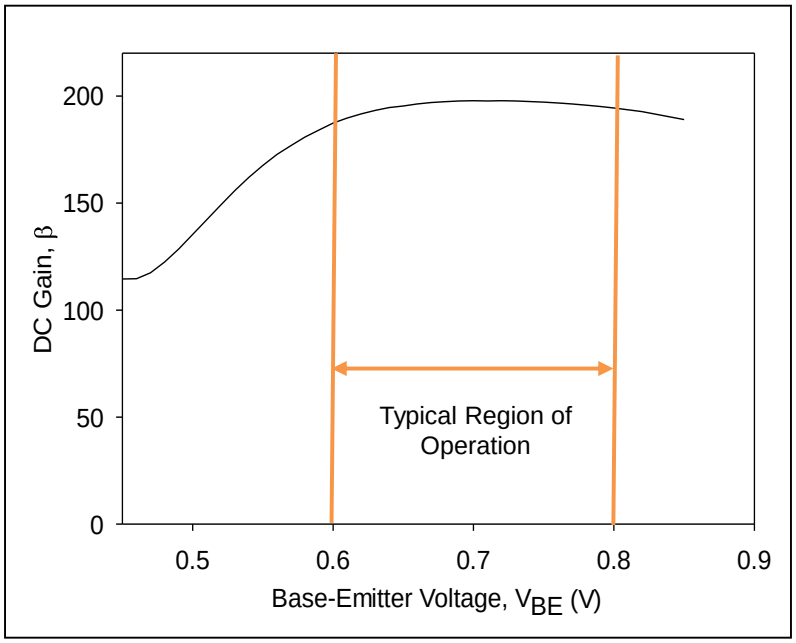


Figure 5.6 DC Current Gain vs. Base-Emitter Voltage for High Performance npn Bipolar Transistor

Using the collector and base currents extracted from Fig. 5.5, a typical plot of the bipolar transistor DC current gain β versus the base-emitter voltage V_{BE} can be generated as shown in Figure 5.6. From this graph, it can be seen that the current gain is fairly constant with a value of nearly 200 for npn transistor in the typical region of operation for $0.6 < V_{BE} < 0.8$ V.

5.3 Experimental Procedure

The objective of this research work is to investigate the influence of uniaxial stress on bipolar transistors. The npn and pnp transistors on (100) silicon that are tested in this work, are fabricated using a 0.5 μm BiCMOS process with trench isolation and 3 metal layers as shown in Fig. 5.7. A total of 15 different transistor designs were available and representative examples are shown in Fig 5.8. Fig. 5.9 shows a BWM chip on a (111) silicon wafer strip which consists of a van der Pauw (VDP) structure from past research [97]. We operated the van der Pauw structure as an npn transistor. The n type van der Pauw structure is on a p type well and the substrate of the wafer is n type. Therefore using the n type VDP as the emitter, p well as the base and the substrate as a collector, we were able to operate this device as avertical npn transistor on (111) silicon wafer strip.In the normal-mode, current gain has been measured to be 36 and in the inverted mode the current gain is 0.5. Controlled application of uniaxial normal stress to silicon strips is performed using a four point bending fixture as shown in Figs 5.10 and 5.11.

5.3.1 Mechanical Stress Generation

The silicon wafer strips with the test structures were cut from the processed (100) silicon wafer along the $[\bar{1}10]$ direction as shown in Fig. 5.7. The four point bending

was utilized to apply well-controlled uniaxial normal stress to the silicon wafer strip which contains the integrated BJT devices. Bending was applied to the strips by placing them between the top and bottom supports of the fixture with the transistor structures facing up as shown in Figure 5.10. Using a micrometer controlled actuator, load was applied by raising the inner bottom supports of the strip while maintaining the outer top supports fixed in position in a four point bending fixture.

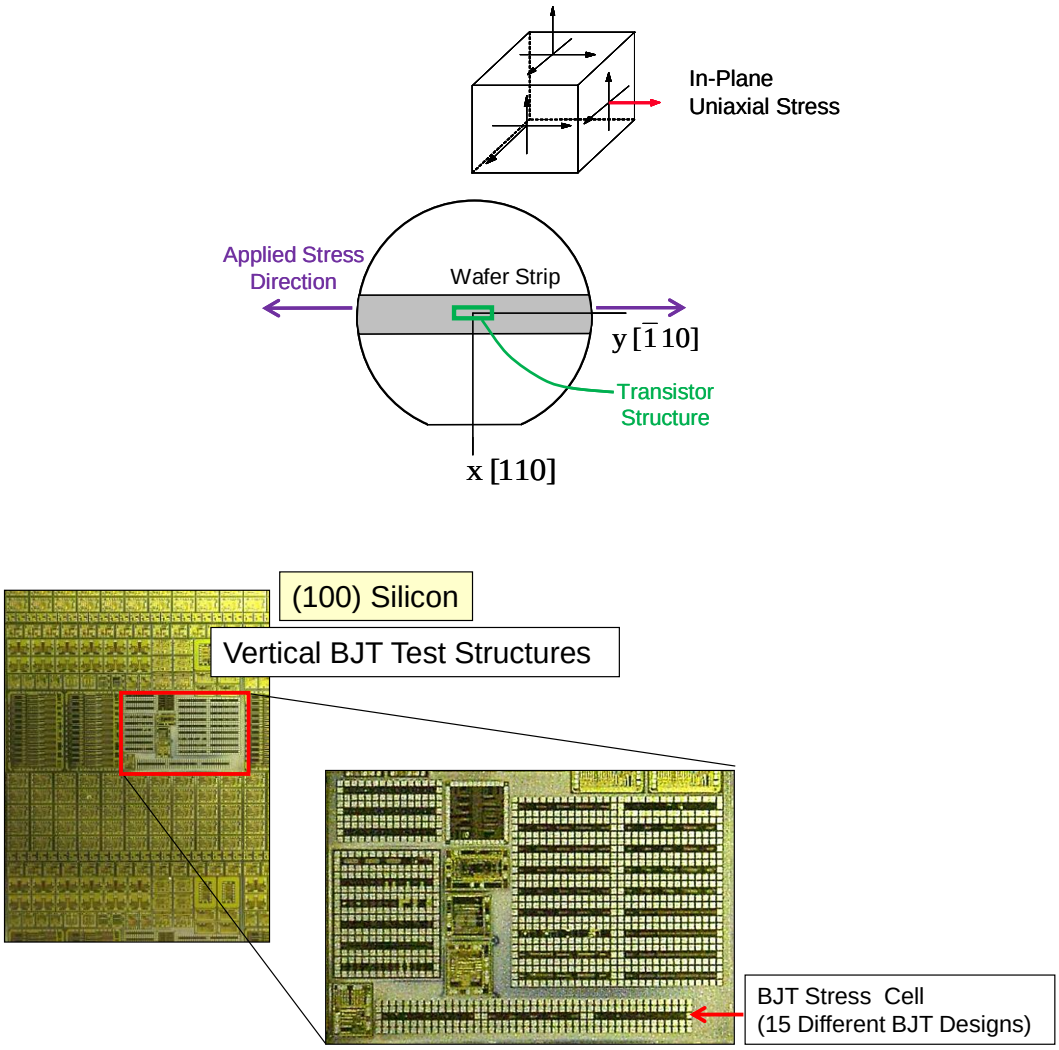


Figure 5.7 Bipolar Transistor Wafer Strip on (100) Silicon

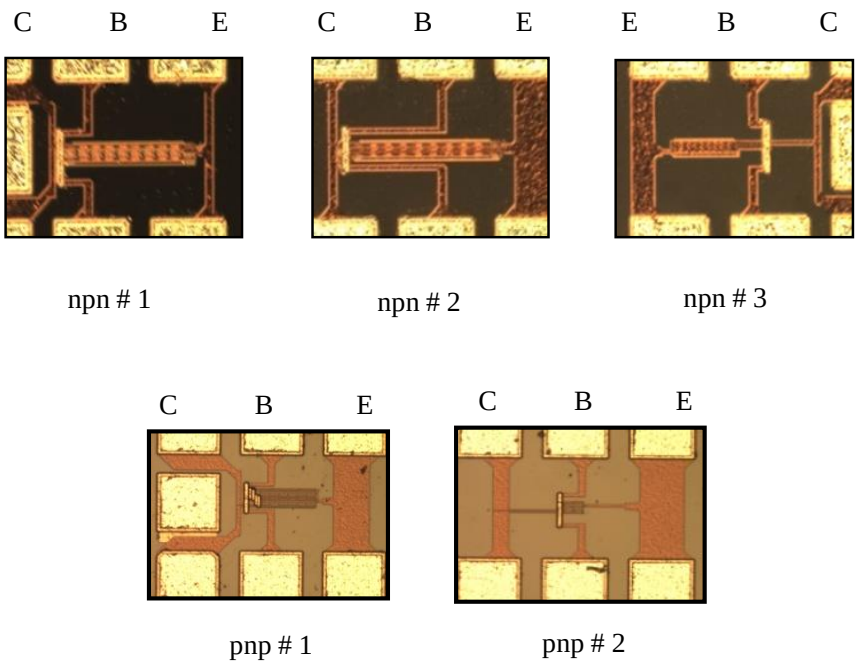


Figure 5.8 Bipolar Transistor Test Structures on (100) Silicon

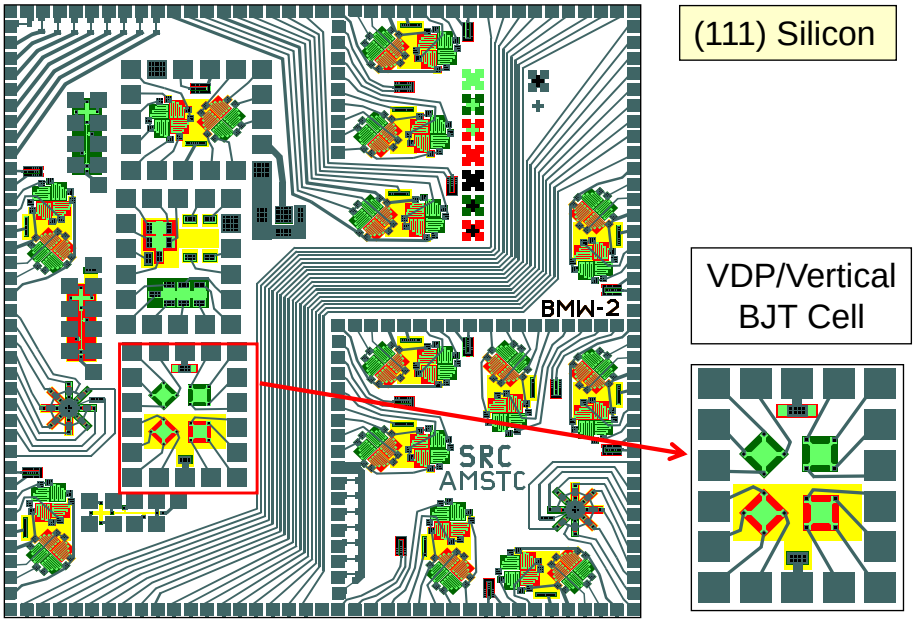


Figure 5.9 Bipolar Transistor Test Structures on (111) Silicon

The uniaxial stress that devices on the upper surface of the wafer strip experienced are given by the following equation:

$$\sigma = \frac{3F(L-d)}{2t^2h} \qquad (5.4)$$

where F is the load applied by raising the micrometer, L is distance between upper outer supports, d the distance between the bottom inner supports, t the thickness of the wafer strip and h the width of the strip.

The four point bending approach produced a known constant tensile stress between the inner supports since the surface of the strip is a free surface so other normal and shear stresses are zero at the surface. The stress in the transistor that was applied through the supports was known uniquely from the load cell reading. Again since the supports were at some distance from the devices that were tested so the devices were insensitive to the stresses generated by the supports of the four point bending fixture. Using the four point bending fixture, uniaxial stress is applied within the range of -150 MPa to +150 MPa. Both compressive and tensile stress by changing the direction of the defection were possible to apply.

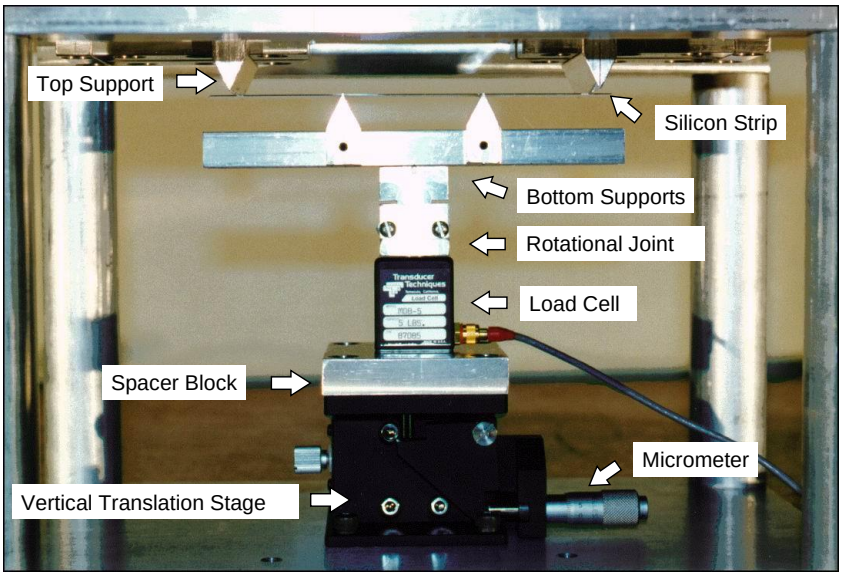


Figure 5.10 Four Point Bending Test Fixture

At first, manual probing was done as shown in Fig 5.11 to obtain the electrical characteristics of the npn bipolar transistors, and stress-induced changes in the characteristics were measured. Keithley 4200-SCS or HP 4146B semiconductor parameter analyzers were used to record the data.

Because of the exponential dependence of the currents in the BJT on temperature and voltage, and the required high sensitivity of BJT measurements, we have found that using manual probing to the flexed silicon strips yields unsatisfactory results (noisy data) as shown in Fig5.12.

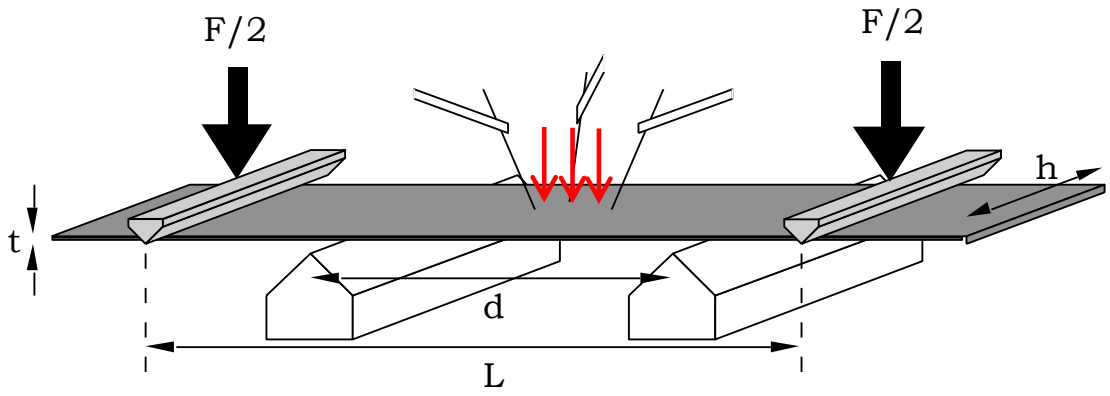


Figure 5.11 Four Point Bending of Wafer Strip

To make good contact with the probing pads of the transistors, probe forces in excess of 30 g were typically required. Even with great care to use consistent probe forces, the probing effect was observed to influence the measured stress effects, and changes in the slopes in the plots in Fig 5.12 occurred due to the probing force induced errors. Thus, reduced accuracy was caused by the effects of the extra stresses induced by the probes and the inability to control these errors. The probing process was also very

slow due to the necessity to reseat the probes after each applied stress level, and small temperature variations between the measurements further exacerbated the inaccuracies of the characterization procedure.

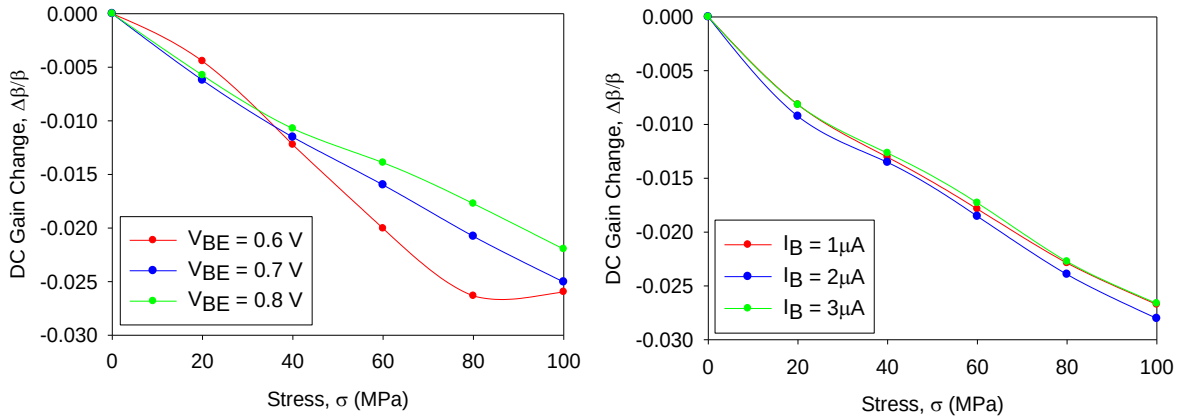


Figure 5.12 Noisy Data due to Probing Force Errors

Since high accuracy measurements were needed to characterize stress effects on the bipolar transistor currents and DC gain measurements, the traditional probing approach was considered unacceptable. Therefore, a new flex circuit approach as shown in Fig. 5.13 has been developed to replace manual probing. The wafer strip was bonded to the flexible polyimide material at a single point at the center of the strip and gold wirebonds were used to electrically connect the appropriate bond pads on the wafer strip to the gold plated copper traces on the flex. The flex had 18 bonding pads through which six transistors either npn or pnp (3 terminals for each transistor) were able to be connected to the flex. The gold wirebonds were used to electrically connect the devices on the strip to the flex since it had the advantage of being flexible and also it did not produce additional stress. The gold wirebonds also posed several problems such as we had to be careful during loading and unloading the sample in the four point bending fixture to avoid breakage of the wirebonds. Moreover the adjacent flexible wirebonds at

times were touching each other, sometimes getting tangled with each other, resulting in causing short circuits. As a result we were not able to get measurement data from all the devices connected through a flexible circuit. The far end of the flexible circuit was configured to mate with a zero insertion force connector attached to an interface board within an interface box as shown in Fig. 5. 14.

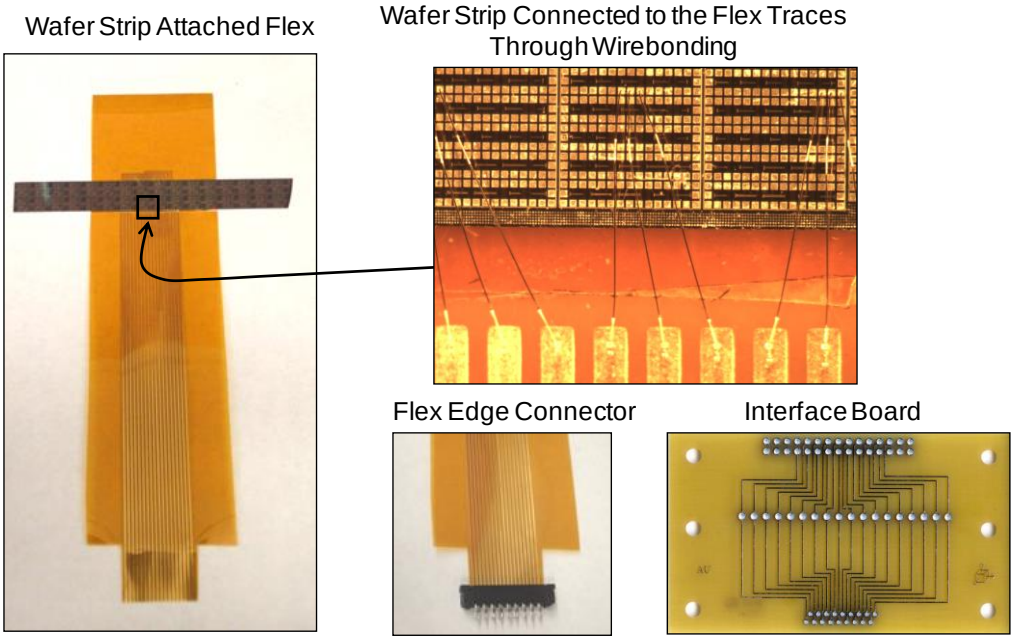


Figure 5.13 Flexible Circuit Used to Interface to Wafer Strip

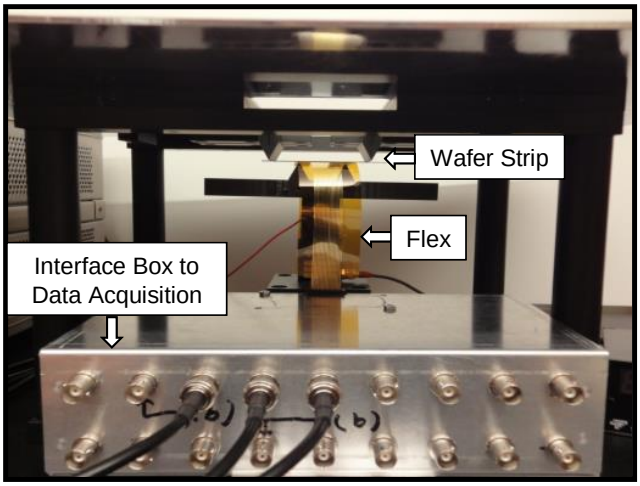


Figure 5.14 Flexible Circuit and Interface Box

Cables from the interface box to the semiconductor parameter analyzer were used to complete the data acquisition system. The new flex circuit approach had the advantages of adding minimal stiffness to the wafer strip, eliminating the need for probes, and significantly reducing the time needed to make measurements.

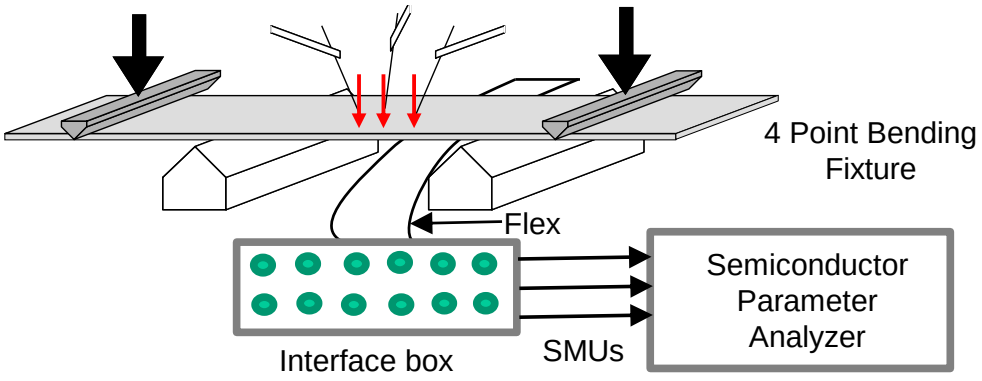


Figure 5.15 Schematic Diagram of the Test Structure

5.3.2 Electrical Measurements

To characterize the variations of characteristics of the npn and pnp BJT devices due to applied stress, electrical measurements were made. The current-voltage characteristics of these devices were obtained using the data acquisition system. The data acquisition system consisted of interface box, Keithley 4200-SCS or HP 4146B semiconductor parameter analyzers and the source measurement units (SMUs). Source measurement units were used to force a voltage/current and sense the corresponding current/voltage. The electrical characteristics of the BJTs were measured by biasing the devices in the forward-active region. The schematic diagram of the measurement setup is shown in Fig. 5. 15.

Four point bending experiments using the flex circuit interconnection scheme discussed above were performed on silicon strips containing vertical npn and pnp bipolar transistors. The forward biasing arrangement that was initially implemented in the electrical measurements of the npn and pnp BJT devices are shown in Fig. 5.16. For both npn and pnp cases the base emitter voltage $V_{BE}$was swept while keeping the collector emitter voltage V_{CE}constant and in that way the Gummel plot was obtained for collector current I_C and base current I_B over a current domain of several decades. The similar method to generate Gummel plots were generated for a range of both compressive and tensile stress. From these Gummel plots at various stress levels, the region were the exponential relationship of the collector current I_C and base current I_B as a function of the base-emitter voltage V_{BE} were valid, was identified and furthermore the DC gain plots which are the ratio of I_C and I_B were obtained. The benefit of biasing by sweeping V_{BE} is that both the current I_C and I_B can be obtained through this method.

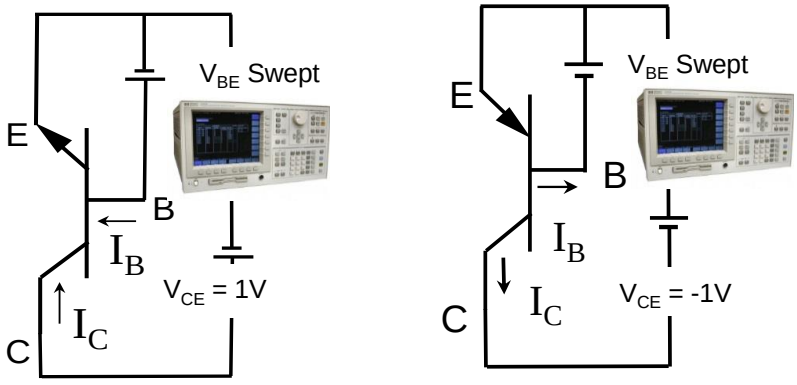


Figure 5.16 The Forward Biasing of the npn (Right) and pnp (Left) Transistor

5.4 Experimental Results

Several different electrical measurement techniques were employed to obtain the stress induced changes in the electrical charaterictis of the npn and pnp bipolar devices. These measuerement techniques are described in the following sections.

5.4.1 Base-Emitter Voltage V_{BE} Sweep Method

Example results for the effects of uniaxial stress on the electrical behavior of the npn transistors using the V_{BE} sweep method on (100) silicon are shown in Figures 5.17-5.19. Fig. 5.17 shows the changes in the current voltage (I-V) characteristic curves of a bipolar transistor under uniaxial in-plane tensile stress along the transistor axis. A magnified view of the curves is also shown so that the monotonic decrease in the collector currentunder stress is apparent. Figs. 5.18 and 5.19 show the corresponding stress effects on the gummel plot and DC current gain response of the same device. In these measurements, the stress level was changed from 0 to 100 MPa with increments of 5 MPa. The observed variations in these plots are uniform and consistent with each other, with both the collector current and DC current gain becoming smaller with increasing stress and base current increasing with the increasing stress.

For a particular base-emitter voltage, the measured variation of the current gain with stress can be extracted from the curves in Fig. 5.19. This has been done at the point of maximum current gain (V_{BE} = 0.72 V), and Fig. 5.20 illustrates the resulting plot of the normalized change in current gain $\Delta\beta/\beta$ vs. the applied uniaxial stress σ for (100) silicon. The response is quite linear, with a slope of -429 (1/TPa). Similar results were found for other vertical npn bipolar devices as shown in Fig. 5.21. The graphs in this figure are for several different types of vertical npn transistors from different wafer strips, and the

plotted data in each graph were for the fixed base emitter voltage where the maximum gain occurred.

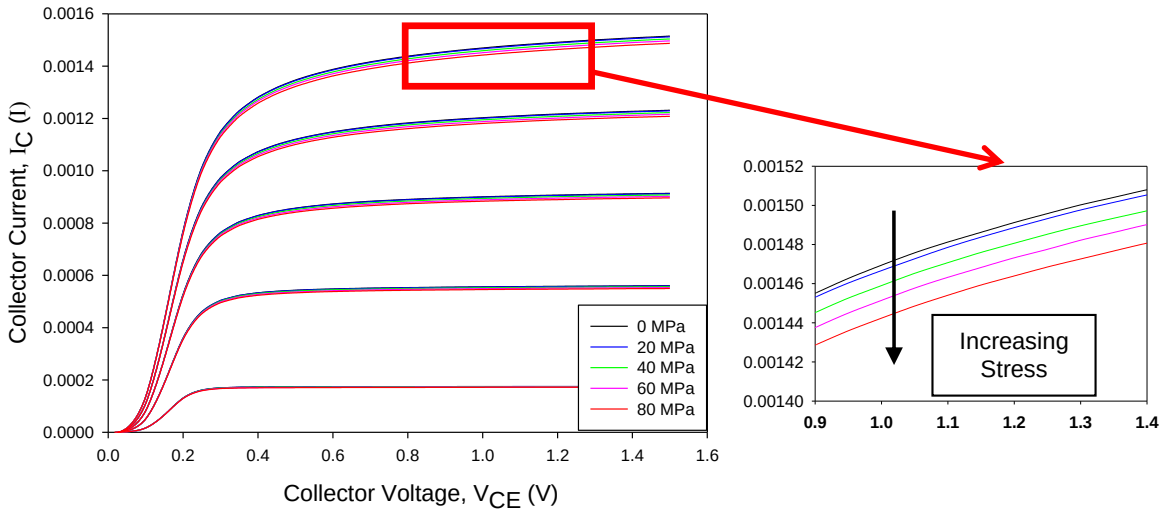


Figure 5.17 Changes in npn Bipolar Transistor Characteristics Due to Stress

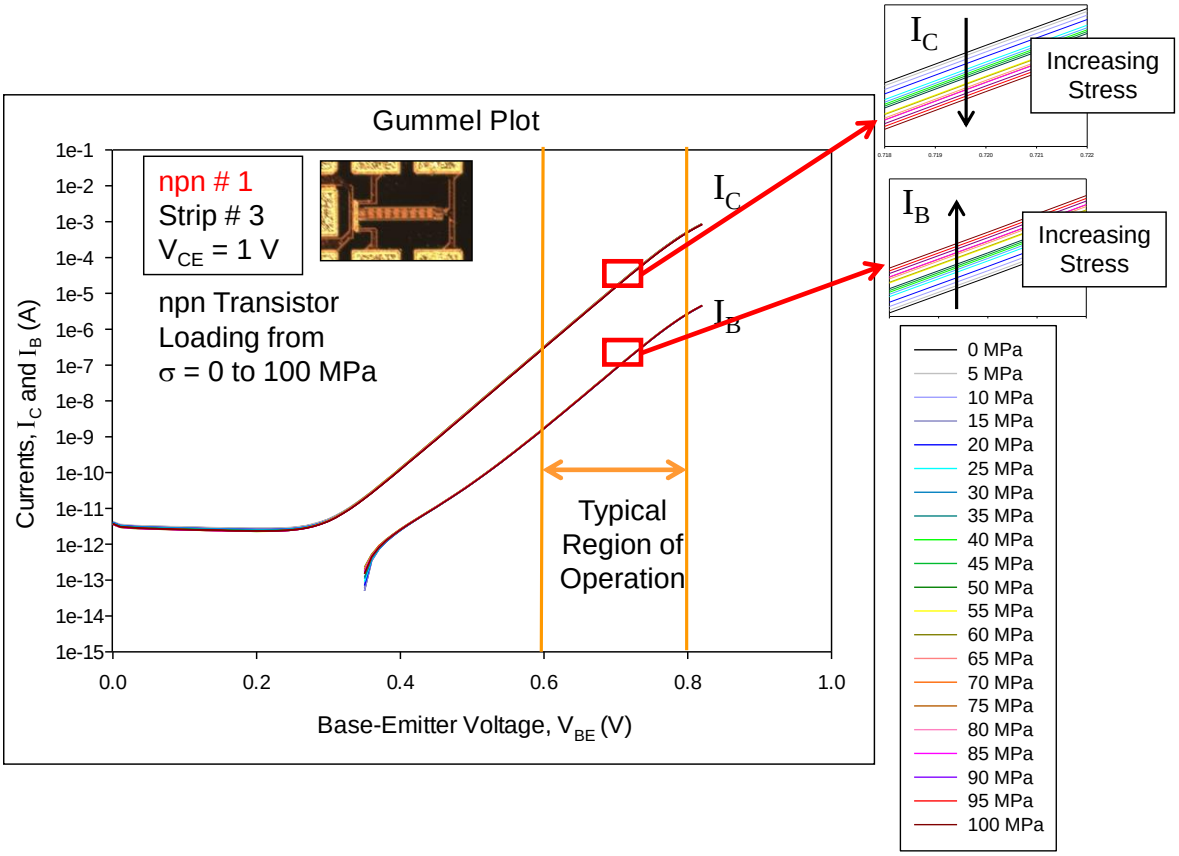


Figure 5.18 Change in Gummel Plots with Stress npn Bipolar Transistor

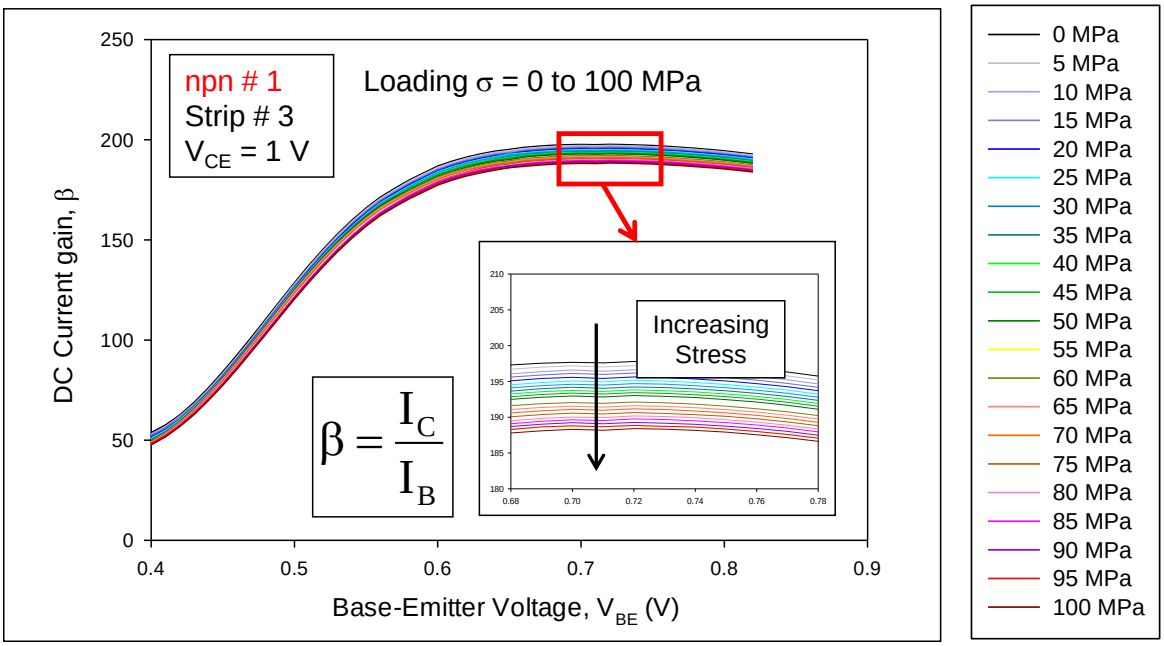


Figure 5.19 Change in Current Gain vs. Base-Emitter Voltage Response with Stress for npn Bipolar Transistor

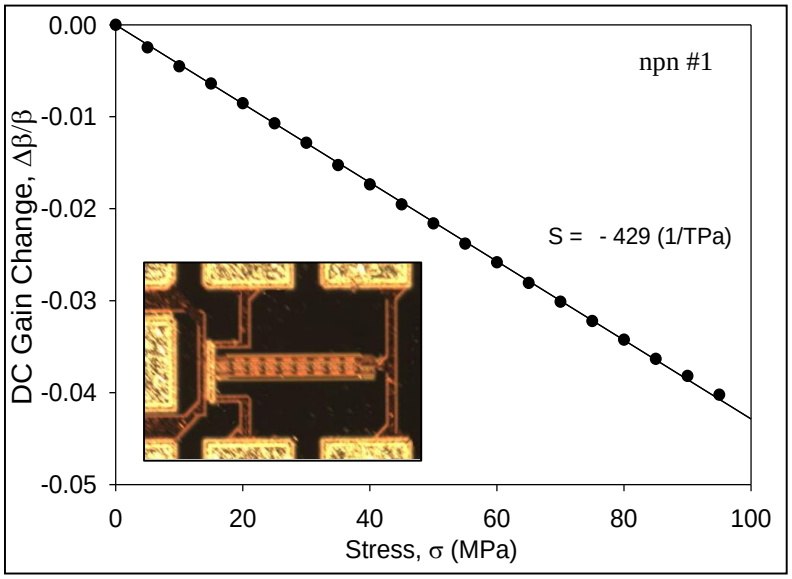


Figure 5.20 Normalized Change in Current Gain vs. Stress npn Bipolar Transistor

The first two plots in Fig. 5.21 are the $\Delta\beta/\beta$ vs. σ response for the same npn transistor on (100) silicon for loading and unloading case. During loading the device is stressed from 0 to 100 MPa and during unloading the stress on the device was brought down in a controlled manner from 100 to 0 MPa and corresponding change in characteristics were recorded. It is evident from both the plots that the slope values for both the loading and unloading case is almost the same, so there is no hysteresis in measurement data while unloading the sample after it being loaded. Values of the extracted slope S of the $\Delta\beta/\beta$ vs. σ response from all of the measured devices are tabulated in Table 1. It is observed that the slopes vary over a limited range of $-420 \leq S \leq -500$ (1/TPa). The data in the Table 1 are for vertical npn transistors having several different emitter areas and from different wafer strips, and the current gain values are for the base-emitter voltage corresponding to maximum gain.

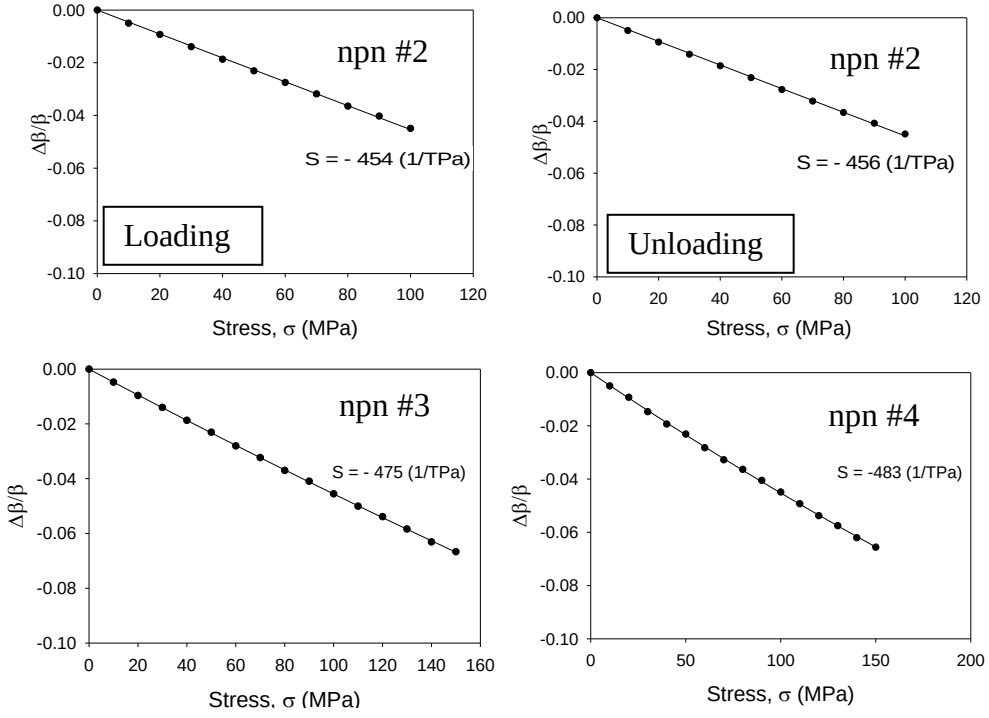


Figure 5.21 Normalized Change in Current Gain with Stress for Several npn Bipolar Transistor

Fig. 5.22 shows the Δβ/β vs. σ response on npn transistor on (100) silicon for various V_{BE} point. As mentioned earlier, the Δβ/β vs. σ response plots were obtained corresponding to maximum gain point. In Fig. 5.22, the Δβ/β vs. σ plots for other V_{BE} points are shown to compare between various operating points. From the plot it is clear that all the plots have same trend and the slope values vary within the expected limit of $-420 \leq S \leq -500$ (1/TPa). Therefore we conveniently used the maximum gain point for our data extraction.

Table 5.1 Δβ/β vs σ Slope Values for Different npn Bipolar Transistor	
Transistor	Slope, S (1/TPa)Δβ/β vs σ
npn # I	-429
npn # II	-454
npn # III	-475
npn # IV	-483
npn # V	-489
npn # VI	-452
npn # VII	-448
npn # VIII	-466
npn # IX	-455
npn # X	-449

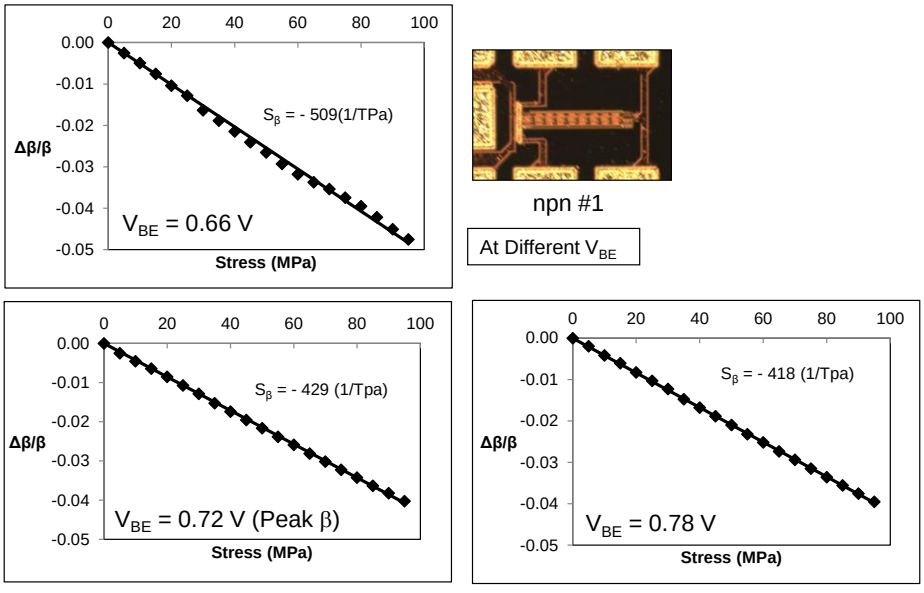


Figure 5.22 Normalized Change in Current Gain vs. Stress for npn Transistor at various V_{BE}.

Similar plots for pnp transistors on (100) silicon for the V_{BE} sweep method are shown in Figs. 5.23-5.25. Fig. 5.23 is the gummel plot for pnp transistor for stress levels varying from 0 to 100 MPa. In case of pnp transistors both the collector current I_C and base current I_B show decreasing trend whereas for the npn, collector current I_C was decreasing and base current I_B was increasing.

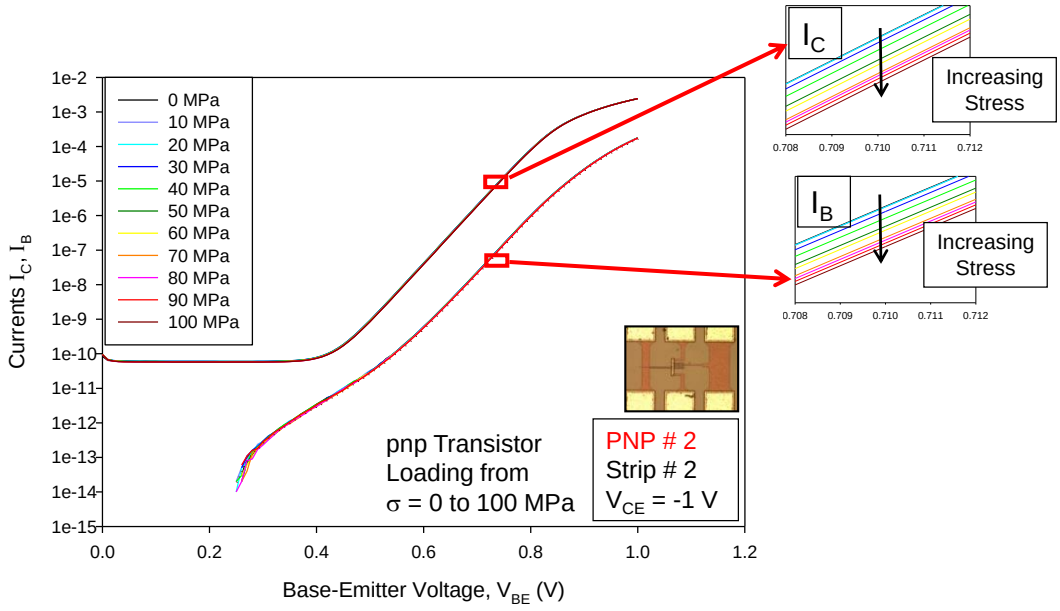


Figure 5.23 Change in Gummel Plots with Stress pnp Bipolar Transistor

Fig. 5.24 is the DC gain plot for pnp transistor with respect to the base emitter voltage V_{BE} and the plot shows that the current gain is increasing with stress which is opposite for that of npn transistor in which the DC gain was increasing with the stress. The change in current gain with stress for a particular V_{BE}can be extracted from the curves in Fig. 5.24. Fig. 5.25 shows plot of the normalized change in current gain $\Delta\beta/\beta$ vs. the applied uniaxial stress σ at maximum current gain (V_{BE} = - 0.6 V) point. One thing to be noticed is, although the $\Delta\beta/\beta$ vs σ plot for npn BJT has a decreasing trend and the plot is quite linear, the pnp $\Delta\beta/\beta$ vs σ plot exhibits nonlinear behavior. Comparison of

the slope values of the Δβ/β vs σ plots for npn and pnp BJTs, the plots for npn transistors are more sensitive to stress compared to the pnp which demonstrates very small change in the current gain with stress.

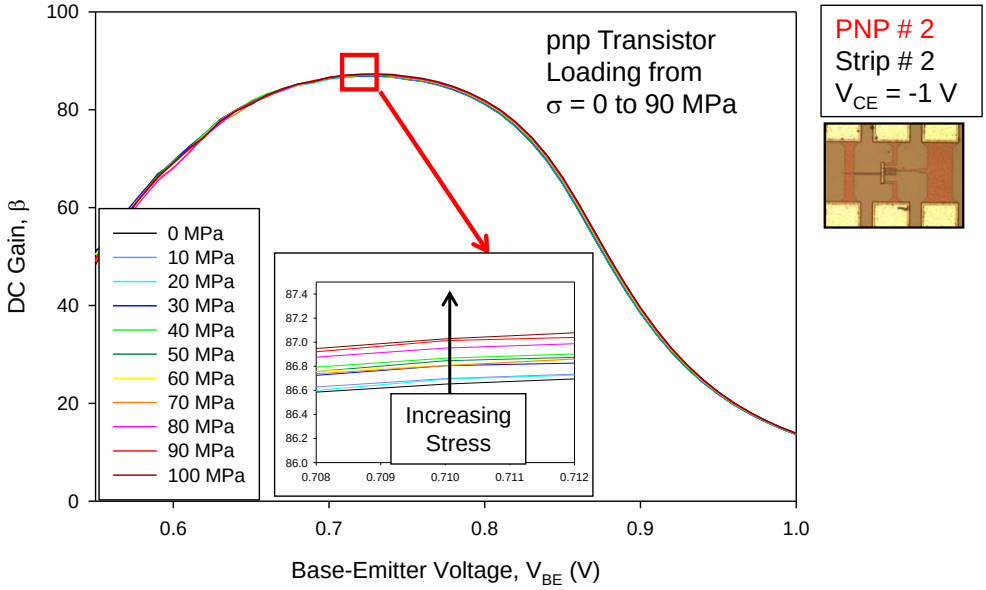


Figure 5.24 Change in Current Gain vs. Base-Emitter Voltage Response with Stress for pnp Bipolar Transistor

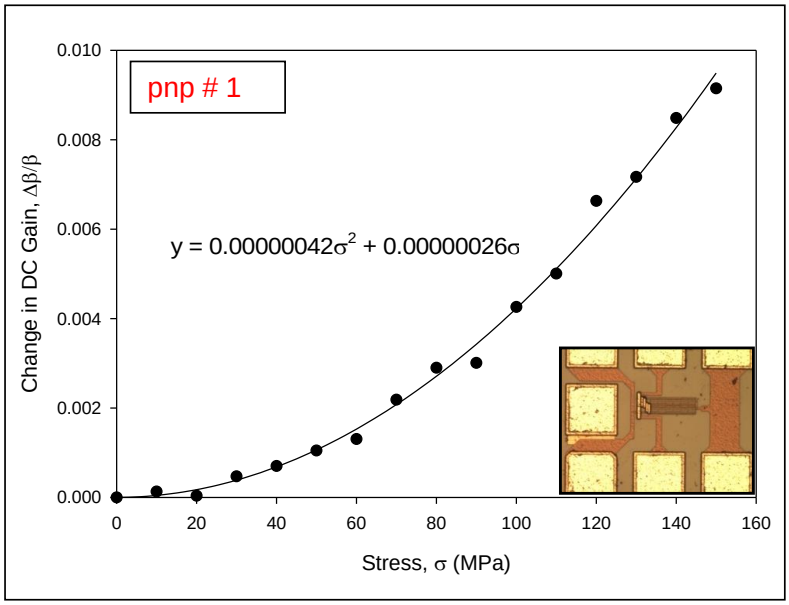


Figure 5.25 Change in Current Gain vs. Base-Emitter Voltage Response with Stress for pnp Bipolar Transistor

5.4.2 Fixed Base-Emitter Voltage V_{BE} Method

Plots in Fig. 5.26 show the variations of the normalized changes in collector and base currents with applied uniaxial tensile stress along with the normalized change in current gain $\Delta\beta/\beta$ for vertical npn transistors on (100) silicon. Although the corresponding $\Delta\beta/\beta$ vs σ plots for these same transistors show very linear changes with stress, the individual current plots illustrate some noise in the data. This noise is caused by small temperature variations due to self-heating of the devices or change in room temperature during the experiments.

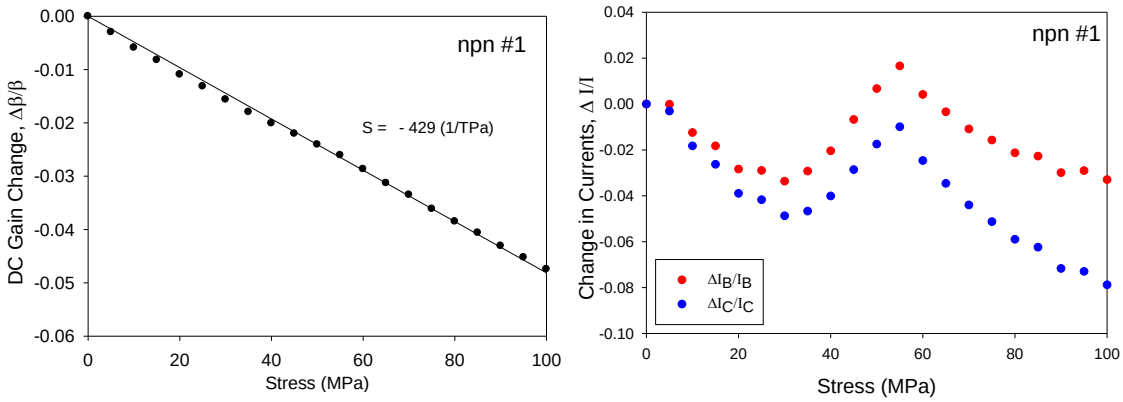


Figure 5.26 Changes in the Current Gain with Applied Uniaxial Stress (Left)
Changes in the Currents with Applied Uniaxial Stress (Right)

Attempts at extracting currents I_C and I_B from the curves such in Fig. 5.19 is compromised by self-heating of the transistors.On the other hand, the fluctuations in the collector and base currents are highly correlated and essentially cancel out in the graph of current gain versus stress as discussed below.

By taking the differentials of the expressions for I_C and I_B in Eq. (5.1), considering most of the base current I_B is due to the back injection into the emitter, it can be established that:

$$\frac{\Delta I_C}{I_C} = \frac{\Delta \mu_{nB}}{\mu_{nB}} + \frac{\Delta n_{iB}^2(\sigma)}{n_{iB}^2} + \frac{q\Delta V_{BE}}{V_T} + \left(1.6 + \frac{E_{GB}}{kT} - \frac{qV_{BE}}{kT}\right)\frac{\Delta T}{T} \qquad (5.5)$$

$$\frac{\Delta I_B}{I_B} \cong \frac{\Delta \mu_{pE}}{\mu_{pE}} + \frac{\Delta n_{iE}^2(\sigma)}{n_{iE}^2} + \frac{q\Delta V_{BE}}{kT} + \left(1.8 + \frac{E_{GE}}{kT} - \frac{qV_{BE}}{kT}\right)\frac{\Delta T}{T} \qquad (5.6)$$

For $E_{GE} \cong E_{GB}$= 1.12 eV and V_{BE} = 0.75 V, the terms corresponding to the ΔT/T expressions in Eq. (5.5) and (5.6) are approximately16 ΔT/T!Thus, both the normalized collector and normalized base currents have very high and similar temperature dependence. Because of the high temperature dependence, small temperature changes that occur between applied load levels in a uniaxial stress experiment will cause the current data points to jump up and down in sync as demonstrated in Figure 5.26, leading to the appearance of noise in the responses. By subtracting Eqs. (5.5-5.6) or differentiating Eq. (5.2), it can be shown that the normalized DC current gain is related to the normalized collector and base currents using:

$$\begin{aligned} \frac{\Delta\beta}{\beta} &= \frac{\Delta I_C}{I_C} - \frac{\Delta I_B}{I_B} \\ \frac{\Delta\beta}{\beta} &= \cong \left[\frac{\Delta \mu_{nB}}{\mu_{nB}} - \frac{\Delta \mu_{pE}}{\mu_{pE}}\right] + \left(\frac{\Delta n_{iB}^2(\sigma)}{n_{iB}^2} - \frac{\Delta n_{iE}^2(\sigma)}{n_{iE}^2}\right) + \left(\frac{E_{GB} - E_{GE}}{kT} - 0.2\right)\frac{\Delta T}{T} \end{aligned} \qquad (5.7)$$

Hence, the temperature terms almost cancel leaving the 0.2ΔT/T term, and bandgap narrowing E_G is typically smaller than kT, so current gain is far less dependent upon temperature than collector current or base current. So the normalized change in the DC current gain can be considered to be a quasi-temperature compensated parameter. This leads to the stable (temperature insensitive) response shown in Figs 5.20 and 5.21.

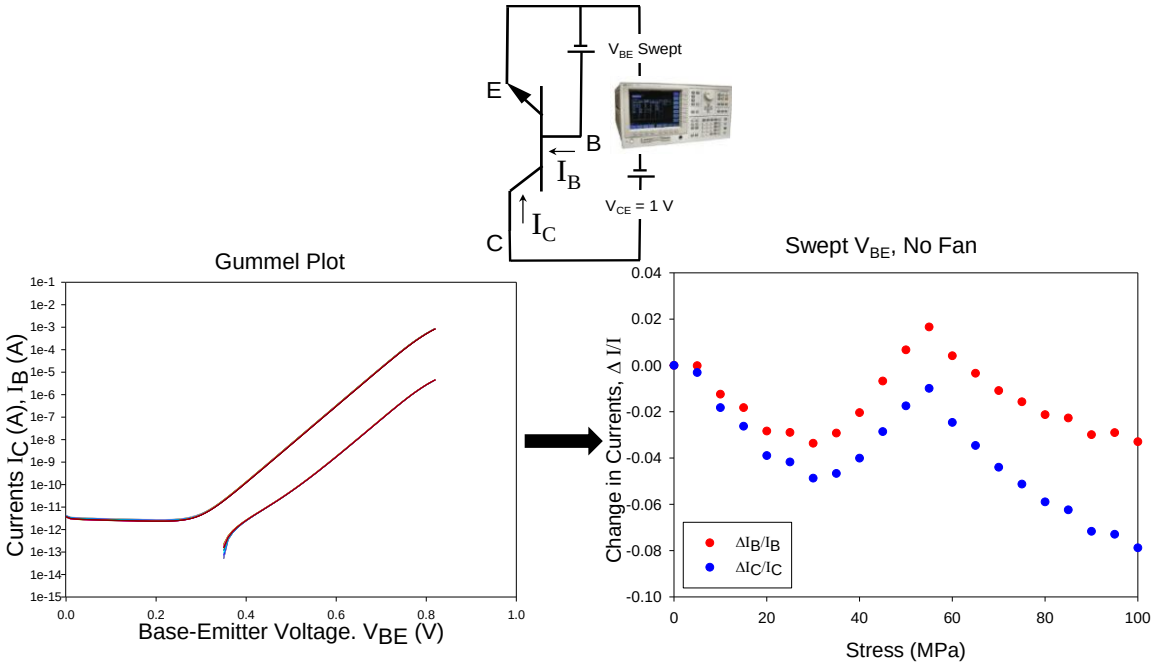


Figure 5.27 Gummel Plot for an npn Transistor (Left)
Changes in the Currents of the Same Transistor with Stress (Right)

Various attempts were made to minimize the effect of temperature on the base and collectorcurrents. The most desirable way to minimize thermal errors is to use compensation involving similar devices where one is stressed and compared to an unstressed device [150, 157]. Unfortunately, we were unable to do implement this approach with our samples. Therefore we attempted other methods. Initially we were generating the entire Gummel plots for every stress level and then obtaining the collector and base currents for a particular base-emitter voltage to extract the currents and the current gain as shown in Fig 5.27. This was causing the device to heat up and the room temperature was also changing slightly during the measurements. So in an effort to minimize the temperature effect, our first attempt was to use a fan to maintain a more constant temperature throughout the measurement, and as can be seen from the second

plot of Fig. 5.28, significant improvement in the collector and base current data was attained. Then to minimize the self-heating of the device, we reduced the measurement time by measuring the currents only at the fixed base-emitter voltage V_{BE} corresponding to the maximum gain point which yielded further improvements in results as can be seen from the third plot of Fig. 5.28.

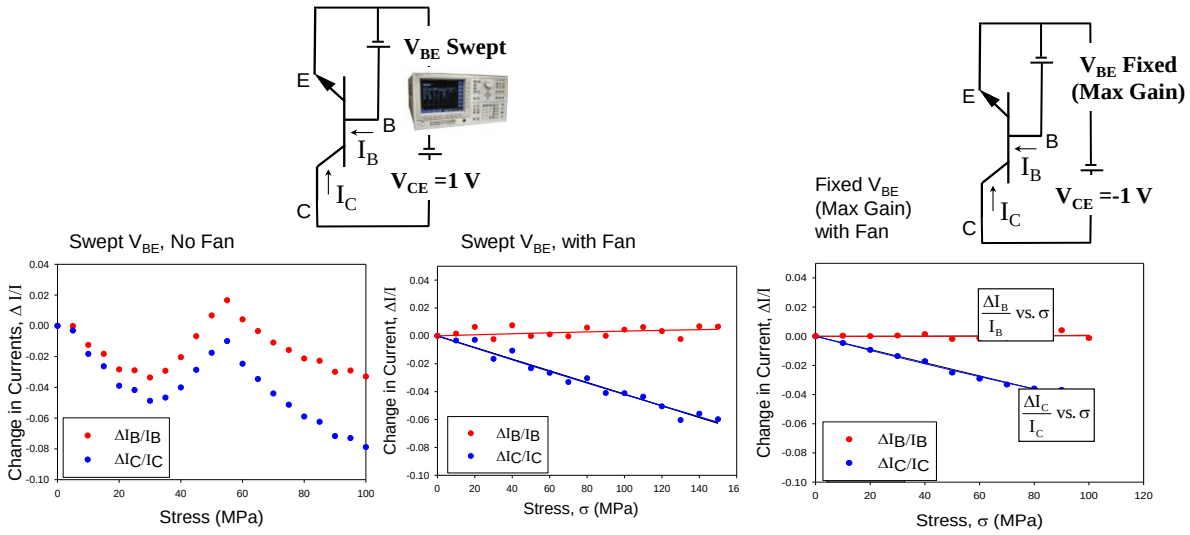


Figure 5.28 Attempts Made to Improve Change in the npn Currents on (100) Silicon

Therefore utilization of a fan across the setup and also obtaining the currents and the current gain data corresponding to fixed V_{BE} point proved to be a better method in attaining these plots. Fig. 5.29 shows normalized change in collector current and base current using the fixed V_{BE} method for both npn and pnp transistors on (100) silicon. These plots are obtained by averaging values from 10 different experiments. The collector current change for both type of transistors are comparable whereas the change in base current for npn transistor is almost negligible.

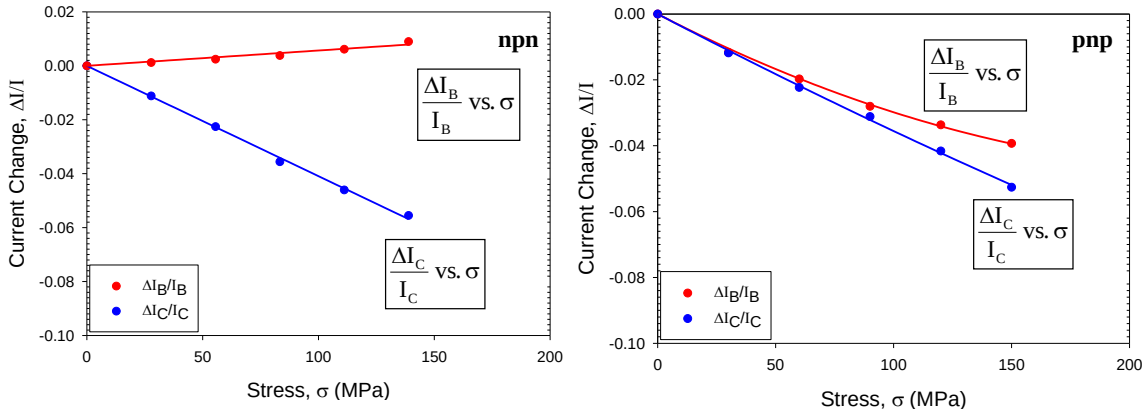


Figure 5.29 Normalized Change in the npn and pnp Currents on (100) Silicon

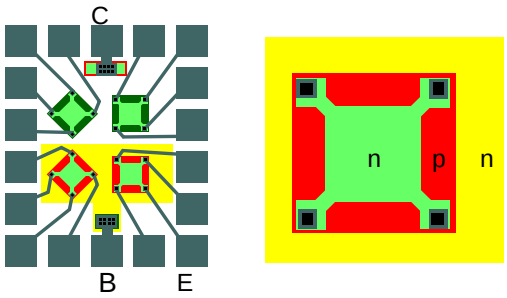


Figure 5.30 Van der Pauw Structure

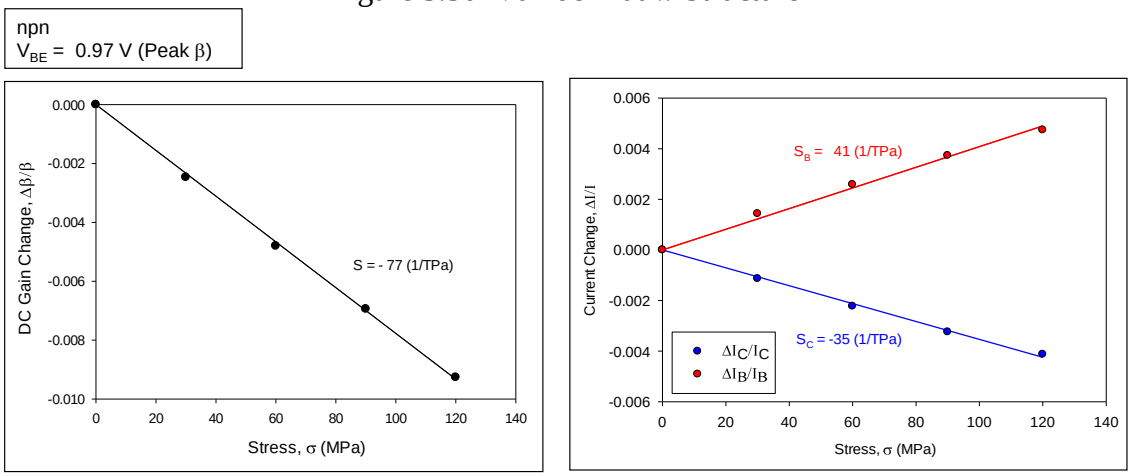
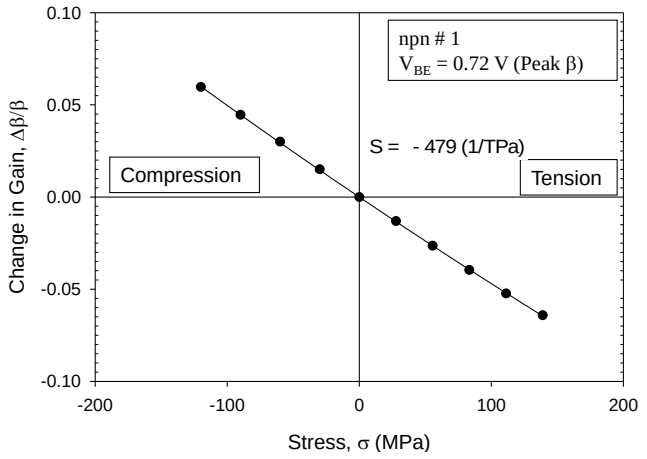
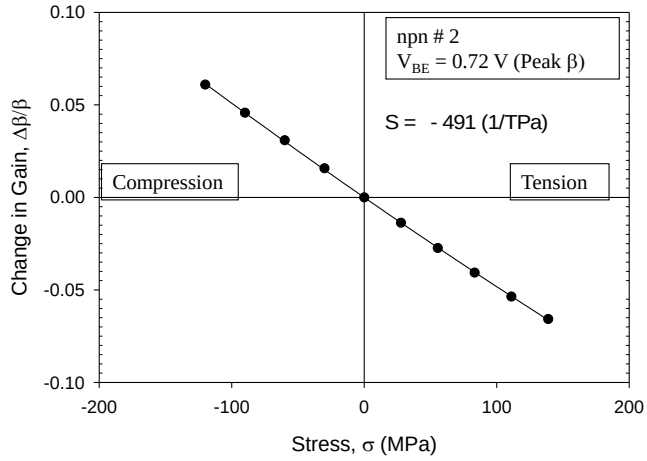


Figure 5.31 Change in Current Gain and Currents of an npn Transistor on (111) Silicon

Fig. 5.31 illustrates the normalized change in current gain and collector current and base current of an npn transistor on (111) silicon. Since we wanted to characterize the response of an npn transistor on (111) silicon, although we did not have an actual npn transistor on (111) silicon, we tried to operate a van der Pauw structure that we had on a BMW strip as an npn transitor. As mentioned at the beginning of this chapter, that operating n type VDP as the emitter, p well as the base and the substrate as a collector, this VDP structure functioned as an npn transistor with a very wide base (~3μm) as shown in Fig. 5.30. As a result, the current gain of this transistor was quite low, in the normal-mode was around 35 whereas the npn transistor on (100) silicon has a current gain of 200. The plots shown in Fig. 5.31 are an average of five different experiments to get rid of temperature related errors.

So far all the plots that have been shown contained the stress response of BJT due to the tensile stress. Measurements were also done to observe the effect of compressive stress on the vertical npn or pnp transistors on (100) silicon by turning the strip over in the bending fixture or changing the positions of the inner and outer supports of the four point bending fixture. Both the responses for three vertical npn transistors are plotted in the graph shown in Fig. 5.32 obtained by fixed V_{BE} method, and it can be seen that the trendofβ remains linear. The slope value of ~450/TPa is consistent among the npn transistors. All these plots contain data that are an average of 10 different experiments. One can observe a small curvature in the current gain plot that may arise from a second order piezoresistive response, thermal errors, and/or small changes in bandgap narrowing.





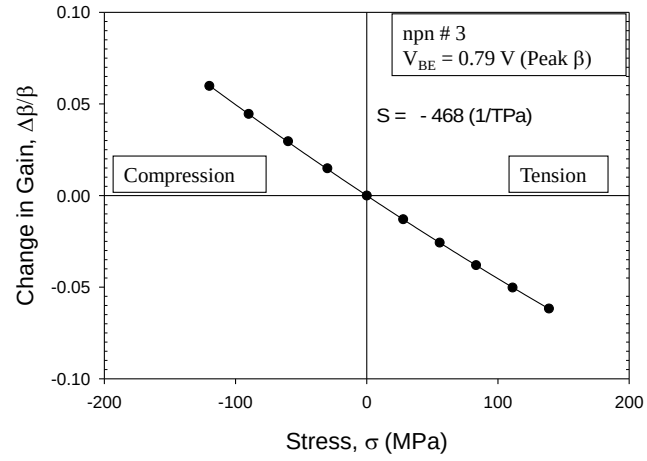
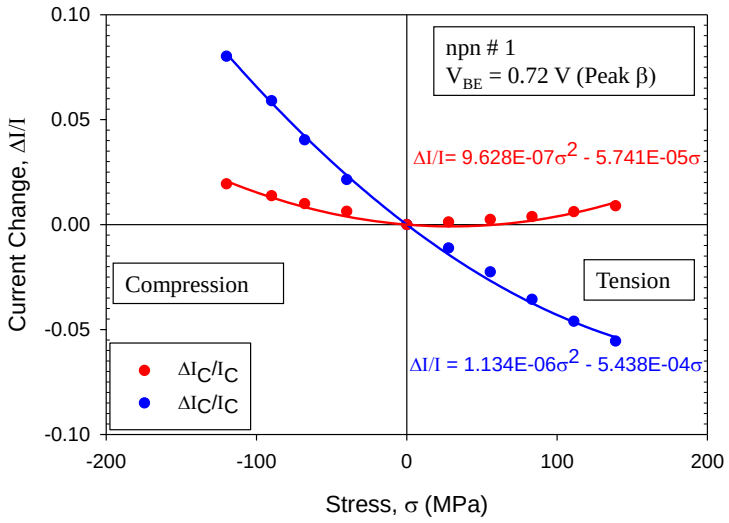
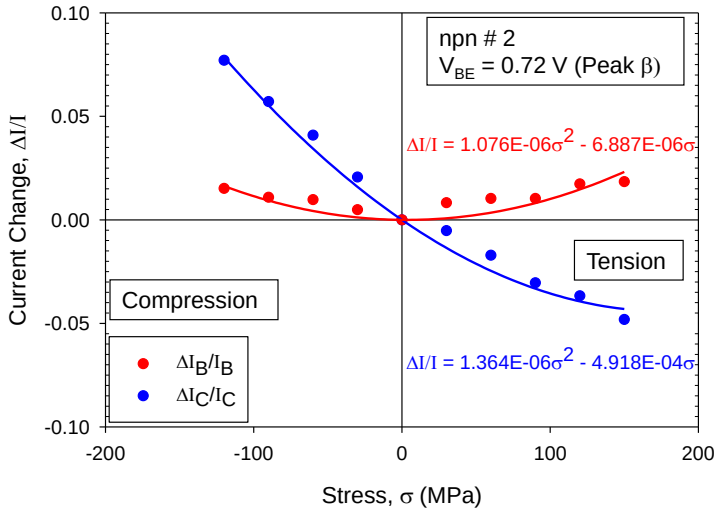


Figure 5.32 Change in Current Gain of an npn Transistor on (100) Silicon





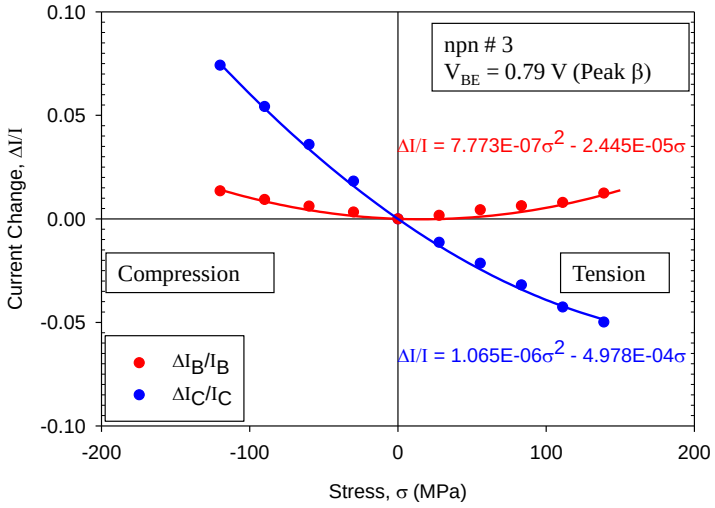
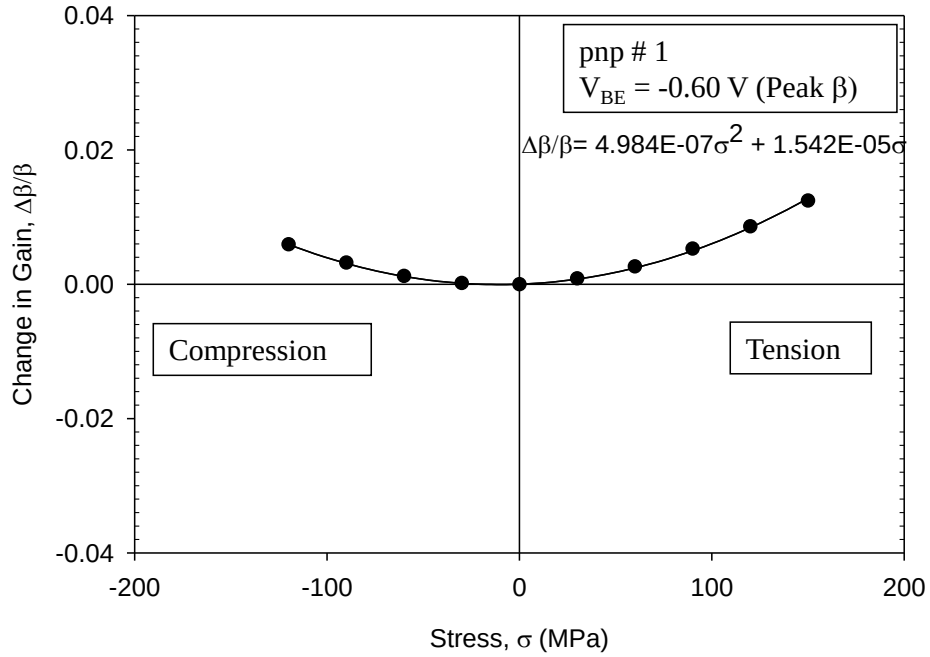


Figure 5.33 Change in Currents of an npn Transistor on (100) Silicon



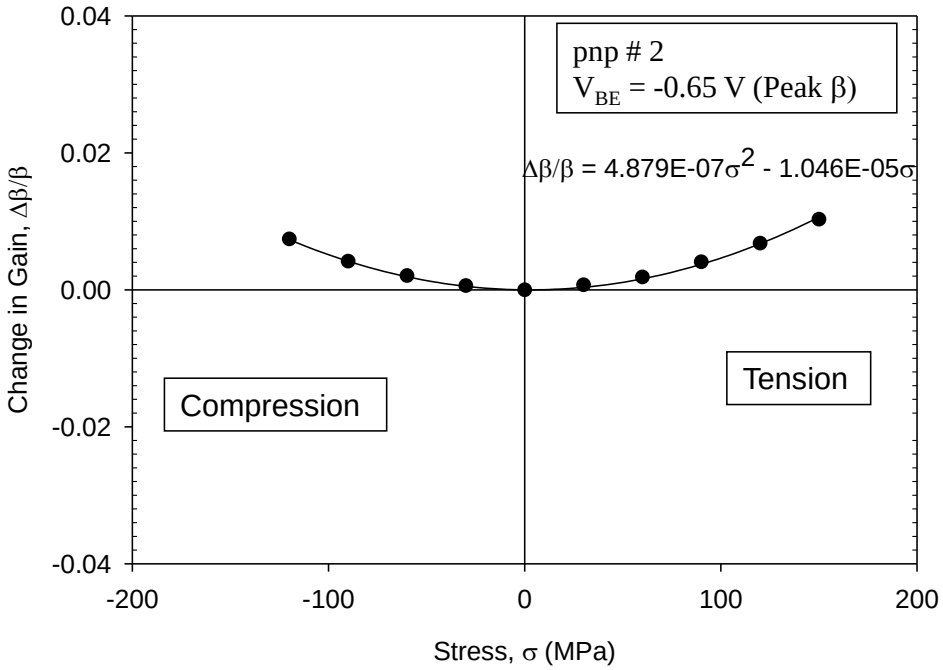
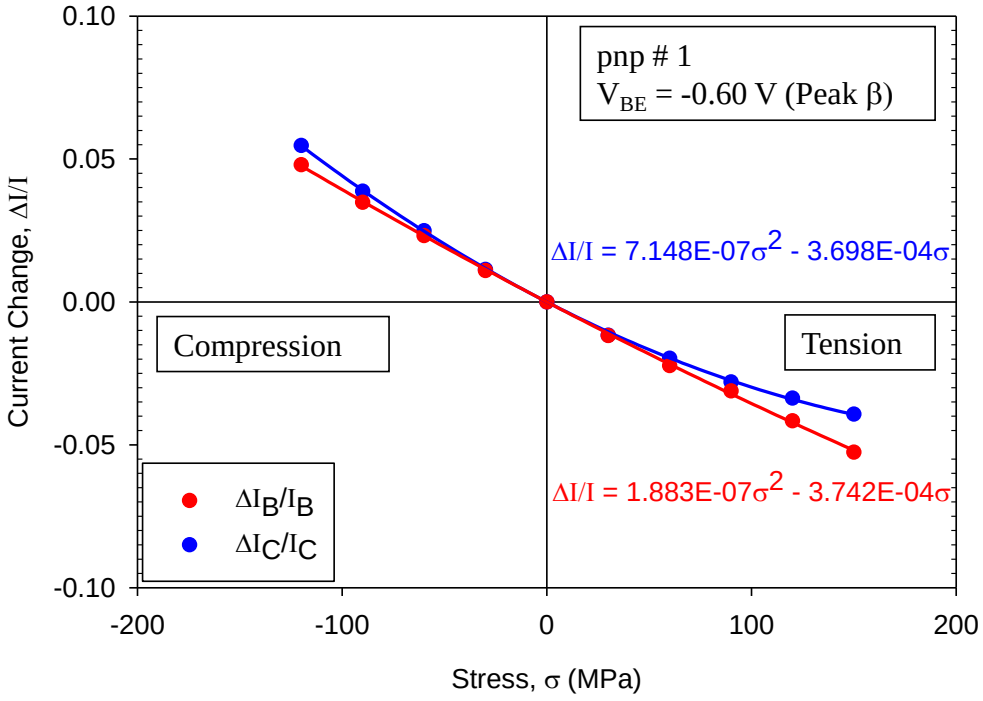


Figure 5.34 Change in Current Gain of an pnp Transistor on (100) Silicon



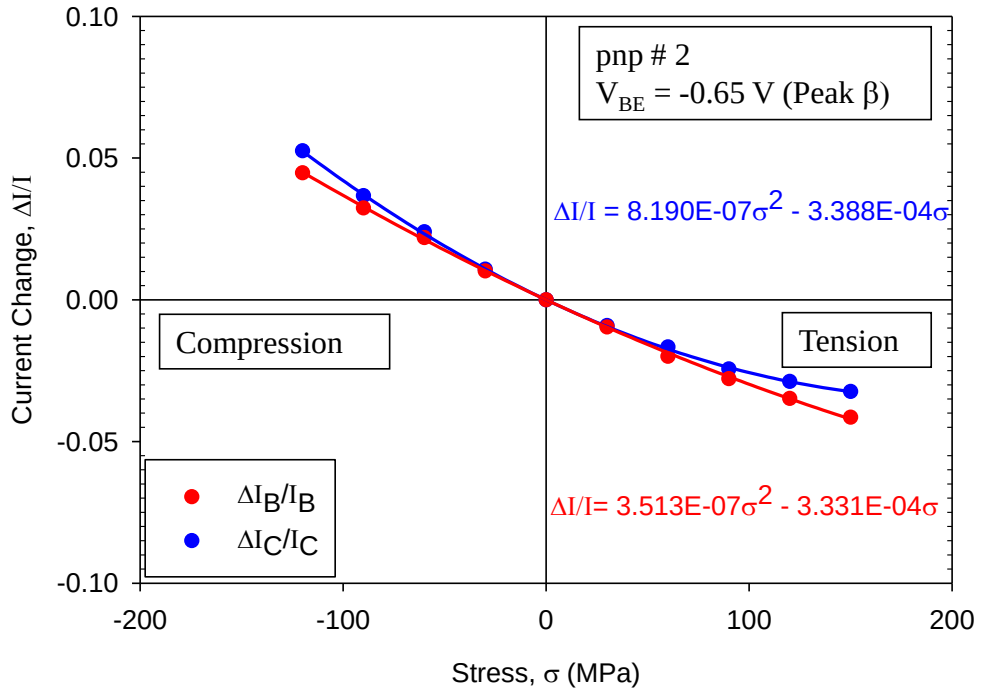


Figure 5.35 Change in Currents of an pnp Transistor on (100) Silicon

The normalized I_C and I_B changes for vertical npn transistors on (100) silicon are plotted for both tensile and compressive stress in Fig. 5.33. The plots are again an average of 10 different experiments and further reduce the impact of temperature fluctuations during the measurements. Though the $\Delta\beta/\beta$ vs σ plots show a linear trend, the corresponding $\Delta I/I$ vs σ plots show non linearity because of the presence of the intrinsic carrier change $\Delta n_i^2 / n_i^2$ terms in their expression given in Eq. (5.5) and (5.6). The variation $\Delta n_i^2 / n_i^2$ with stress is quadratic in nature as will be discussed in the next chapter hence the $\Delta I/I$ has nonlinearityin their response with stress.

The responses of the vertical pnp transistors on (100) silicon for both tensile and compressive stress are illustrated on Figs. 5.34 and 5.35. From the comparison of the responses of npn and pnp transitors on (100) silicon it is evident that although the $\Delta\beta/\beta$ vs σ plots for npn transistor shows a linear trend, the pnp transistors show nonlinearity in their response and the change in current gain with stress in case on pnp transistor is very small which is approximately ~25 times more for npn transistors.

5.4.3 Emitter Current I_E Sweep Method

In this section, a new method of measurement, the emitter current I_E sweep method is discussed. From Eq. (5.1) we can see that the collector and base currents have exponential dependence on base-emitter voltage and hence temperature. Figure 5.36 depicts the temperature response of the base emitter voltage and indicates that the base emitter voltage has a strong well-known temperature dependence that is around -2 mV/^{o}C.

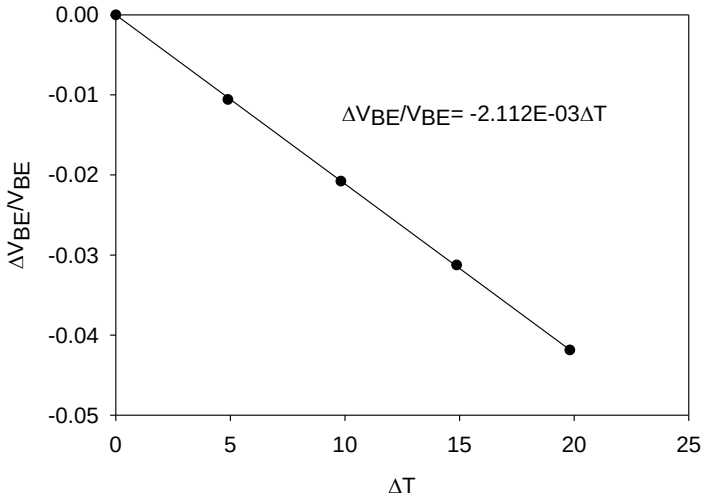


Figure 5.36 Temperature Dependence of Voltage V_{BE}

Although during measurements using the fixed V_{BE} method, V_{BE} was kept constant but temperature change due to change in room temperature or the self-heating of the device was causing I_C to drift. Unfortunately, accurate extraction of model parameters I_S and β from measurement of collector current I_C and base current I_B is easily compromised by the large temperature sensitivity of the BJT due to the exponential dependencies on temperature.For example, if one measures I_C and I_B with constant base-emitter voltage, one must contend with large temperature sensitivities, for example a 1˚ K change at room temperature yields a 15% change in I_S.

To help overcome the inaccuracies due to the change in temperature that is encountered in the fixed base-emitter voltage V_{BE} method, we employed an approach based upon fixed emitter current $I_E$biasing that still provides two degrees of freedom necessary to independently measure current gain and saturation currentwith manageable temperature sensitivity. Examples of the new measurement technique to characterize variations of β and I_S are presented for vertical npn transistors under tensile and compressive stresses ranging between -120 MPa and 150 MPa. The proposed

measurement technique forces a current from the emitter while keeping base and collector terminals grounded as shown in Fig. 5.37. This measurement technique has only two degrees of freedom (I_B and V_{BE}), so we can obtain $\Delta\beta/\beta$ and $\Delta I_S/I_S$ data from this measurement.

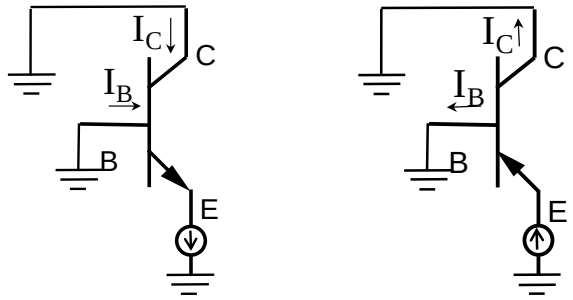


Figure 5.37 The Emitter Current I_E Biasing of the npn (Right) and pnp (Left) Transistor

Forcing current through the emitter causes I_C to be nearly fixed, so the change in I_B determines the change in $\Delta\beta/\beta$:

$$\frac{\Delta\beta}{\beta} = \frac{\Delta I_C}{I_C} - \frac{\Delta I_B}{I_B} \cong 0 - \frac{\Delta I_B}{I_B} \tag{5.8}$$

Current gain is shown to be a quasi-temperaturecompensated quantity relative to either the individual collector or base currents, with the residual temperature coefficient limited by the bandgap difference between the base and emitter regions of the transistor as discussed in the previous section.With this method, the base-emitter voltage is allowed to change and by carefully recording the temperature data at each measurement point, the temperature related change in V_{BE} can be compensated. We can also correct for small I_C variations as β changes by measuring, or calculating, $\Delta I_C/I_C$.

If there is no change in I_C, we can obtain normalized change in I_S using the following equation:

$$\frac{\Delta I_S}{I_S} = -\frac{\Delta V_{BE}}{V_T} - \left(1.6 + \frac{E_{GB}}{kT} - \frac{V_{BE}}{V_T}\right)\frac{\Delta T}{T} \tag{5.9}$$

Through careful measurement of temperature in a controlled oven, we can correct for any temperature errors in Eq. (5.9) which effectively becomes:

$$\frac{\Delta I_S}{I_S} = -\frac{\Delta V_{BE}}{V_T} \tag{5.10}$$

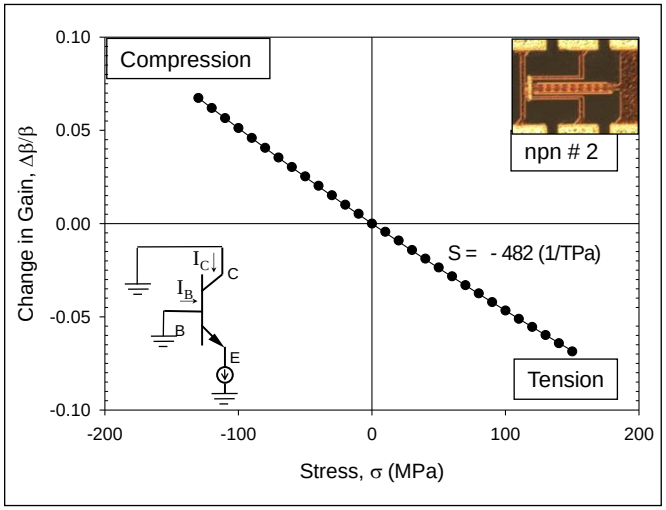


Figure 5.38 Change in Current Gain of an npn Transistor on (100) Silicon using I_E Sweep Method

By carefully monitoring any temperature change during measurements using a thermistor we were able to correct for the variation in base emitter voltage V_{BE} for any error due to thermal drift. Examples of the emitter current biasing method to characterize variations of saturation current I_S and current gain β under stress are presented in Figs. 5.38 and 5.39 for an npn transistor under tensile and compressive stresses ranging between -120 MPa and 150 MPa. Figure 5.40 provides a comparison between a fixed base emitter voltage V_{BE} measurement and constant emitter current biasing. Both methods yield almost identical results for $\Delta\beta/\beta$ of approximately -490 (1/TPa). Figure 5.41 shows the normalized change in saturation current I_S for pnp transistors. The

advantage of this method is we can obtain the variation of saturation current I_S with applied stress which were not possible with the previous methods.

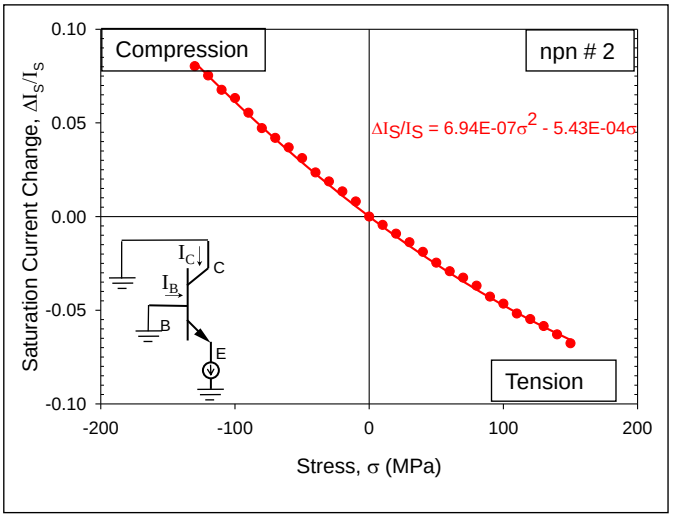
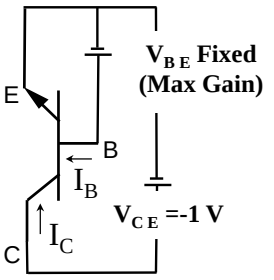
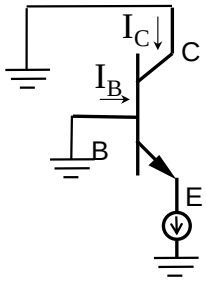
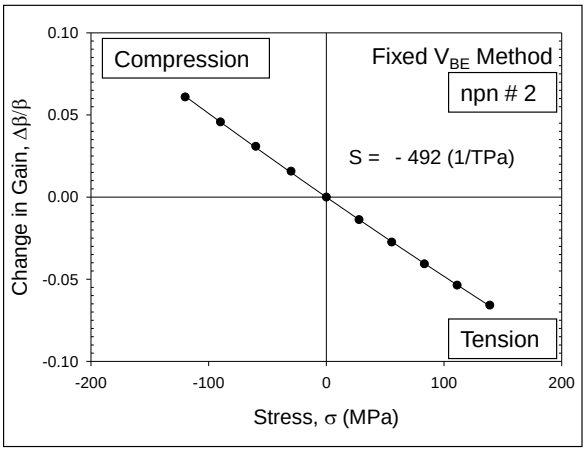


Figure 5.39 Change in Saturation Current I_S of an npn Transistor on (100) Silicon using I_E Sweep Method







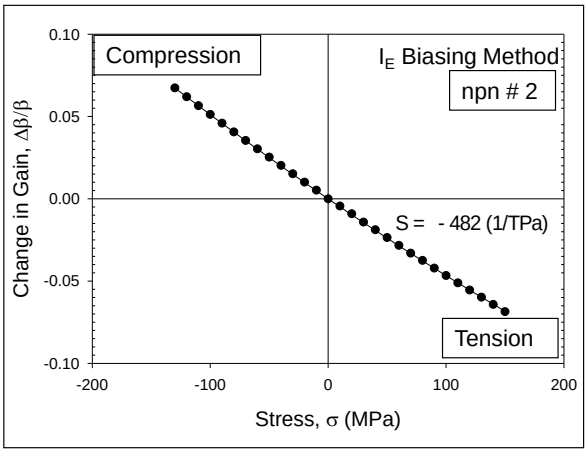


Figure 5.40 Comparison Between Fixed V_{BE} and Emitter Current I_E Biasing Method

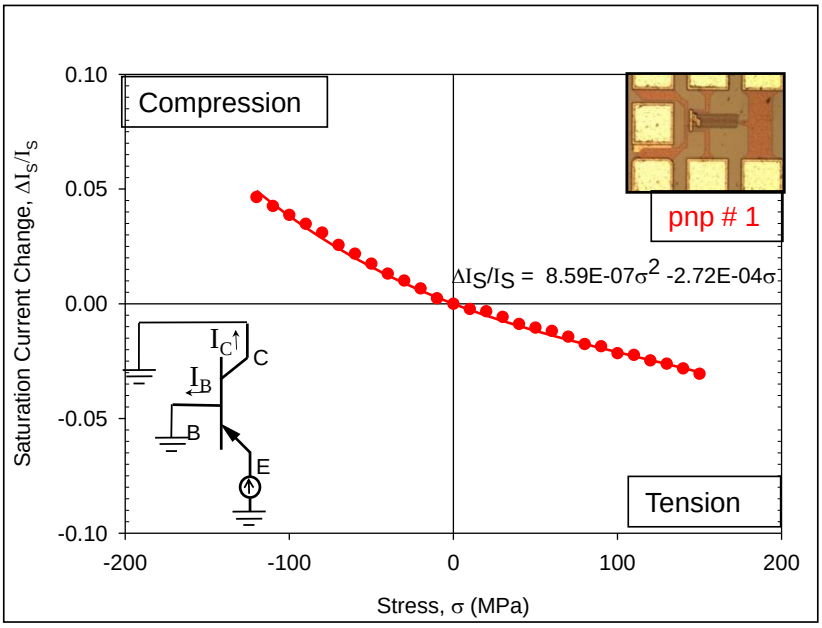


Figure 5.41 Change in Saturation Current I_S of an pnp Transistor on (100) Silicon using I_E Sweep Method

5.5 Summary and Conclusions

In this chapter, we have characterized the response of bipolar junction transistors (BJT) due to the application of mechanical stress. Test structures have been utilized to characterize the stress sensitivity of vertical npn and pnp bipolar devices fabricated on (100) and (111) silicon wafers. Uniaxial normal stresses were applied to silicon wafer strips using a four-point-bending fixture to observe the stress-induced changes in the electrical performance of the BJTs. The collector current and DC current gain were both found to decrease with stress, while the base current was found to increase with stress for npn transistors on (100) and (111) silicon. For pnp transistors the collector current and base current were both found to decrease with stress, while the current gain was found to increase with stress.The slope of the normalized current gain vs. stress response for both

npn and pnp transistors was found to be fairly constant for a variety of bipolar transistor designs. For an npn transistor, the variation of current gain with stress demonstrates a linear trend, but the corresponding collector current and base current shows nonlinearity because of the presence of $\Delta n_i^2 / n_i^2$ term present in the current expressions. For pnp transistors the current gain variation shows a nonlinear trend, but one thing to be noticed is that the response of a pnp transistor is very small compared to the npn transistor and from a practical point of view, we can neglect the curvature terms in the plot.

Different methods of electrical measurements such as base emitter voltage V_{BE} sweep method, fixed V_{BE}method, emitter current I_E sweep method was discussed and the corresponding advantages and the disadvantages of these methods were addressed. It has been shown that accurate measurements can be done using non temperature-compensated techniques with careful attention to the experimental measurements. We have developed a new non-temperature compensated approach based upon fixed emitter current biasing that still provides two degrees of freedom necessary to independently measure current gain and saturation current, but with manageable temperature sensitivity.

All these experimentally obtained results using various measurement methods guided us towards the development of theoretical formulations to accurately calculate the electrical characteristics of these bipolar devices when subjected to fabrication and packaging induced stress. This will help the circuit designers to include stress induced changes in their designs hence helping them to correctly predict the response of the bipolar devices in a circuit in a particular stress condition.

CHAPTER 6

THEORETICAL MODELING OF MECHANICAL STRESS EFFECT ON THE PERFORMACE OF PRECISION ANALOG DEVICES

6.1 Introduction

It is well known that mechanical strains and stresses developed during the fabrication, wafer level and BEOL processing, and subsequent packaging of precision analog devices cause parametric shifts in their electrical performance. The stress/strain destroys the crystal symmetry of the silicon lattice that causes shift in the energy bandgap which results in changes in electron and hole carrier concentrations and their mobilities. The changes in the carrier concentration and their mobilities are manifested through modulation of currents or voltages at the terminals of these devices as discussed in the previous chapter. In MOS devices, mobility variations primarily affect transistor transconductance parameters which are related to the mobilities of the carriers whereas bandgap changes affect threshold voltages. In bipolar junction transistors (BJTs), both bandgap and the attendant minority carrier mobility variations affect various parameters including saturation current, base-emitter voltage, and current gain. Additionally, long-term strain/stress can lead to crystal lattice damage (defects and dislocations), creating additional generation-recombination centers and leading to changes in minority carrier lifetimes and interface charge that affect behavior of both MOS and bipolar transistors.

Stress affects the reliability and performance of stress sensitive circuits adversely. Stress-induced device parametric shifts will affect the performance of analog circuits that

depend upon precise matching of bipolar and/or MOS devices, and can cause them to operate out of specifications. Stresses can be induced by fabrication and assembly processes such as shallow trench isolation, wafer backgrinding and dicing, TSV formation, die attachment, and first level packaging (e.g. encapsulation). The resulting stresses alter the relative characteristics of the transistors and the parametric shifts ultimately reduce overall circuitmanufacturing yield and increase manufacturing cost. The analog devices are usually more affected by stresses, therefore the circuits containing these analog devices demonstrates more stress sensitivity. Circuits that are affected include phase-locked loops (PLLs), digital analog converters (DACs), analog-digital converters (ADCs), precision voltage references, op-amps, regulators, filters etc. which have applications in electronics field such as cellular phones, wireless application modules, PDAs, hand held devices and image capturing devices.MEMS transducer structures and interface circuits can also be adversely influenced.

One thing to acknowledge is that the determination of stress sensitive circuits are highly dependent on the technology used in the fabrication of these circuits and also the end user requirement. As an example, in an application where high performance is required, small modulation of the electrical output of the circuit is more likely to be a serious design problem compared to a low performance requirement. That is why the older generation circuits with larger device sizes and low performance, were not affected as strongly by stress related issues. With the trend of device size scaling down by the semiconductor industry, the stress related problems are more important since fabrication and package induced stresses are problematic in small feature size devices. Moreover the

tendency of the industry towards high performance circuits make the circuits more susceptible to stress.

In the previous chapter, endeavors have been made to characterize experimentally the variations in current gain β, collector current I_C, base current I_B and saturation current I_S of npn and pnp bipolar transistors with the application of uniaxial stress. Using these experimentally obtained data we attempt to develop a theoretical model that fits the experimental data. In literature there are a few detailed investigations by Creemer et al. to develop a theoretical model to characterize the stress effects on analog devices [154-159]. Their proposed model was based on determining piezojunction coefficients by fitting their theoretical model (similar to that for the piezoresistance effect) to the experimentally obtained data. Although characterization of the piezojunction coefficients that describe the variation of transistor saturation currents under stress has been explored, there has not been a comprehensive modeling effort for use in circuit simulation. Here we discuss a basic charge-control model for the transistor that adequately captures the macroscopic impact of stresses on the BJT device characteristics and demonstrates its use in exploring the behavior of analog circuits employing these devices. This leads to an understanding of the dominant effects of stress on the basic BJT model parameters and elucidates the roles of mobility and intrinsic carrier concentration.

The performance of a circuit in any mechanical stress environment should be well known by a circuit designer so that during designing the circuit he/she can design the circuits to minimize stress related variations. Therefore, the objective of this chapter is to develop theoretical formulations for stress induced variations in the electrical characteristics of the analog devices so that these formulations can be applied to

theoretically optimize transistor design, placement, orientation, and processing to minimize the impact of fabrication and packaging induced die stresses.

6.2 Bipolar Junction Transistor Modeling

To develop a more fundamental understanding of the variation of the electrical performance of bipolar transistors under mechanical stress, a theory has been developed to model uniaxial stress-induced changes in the current gain of vertical bipolar junction transistors on (100) and (111) silicon. The developed expressions are based on the standard one-dimensional theory for a uniformly doped bipolar junction transistor as shown in Fig. 6.1. For the bipolar transistor depicted in Fig. 6.1, the collector and base currents, I_C and I_B, are related to the base-emitter and base-collector voltages V_{BE} and V_{CE} in the forward-active region using a basic transport model,

$$I_C = \beta I_B = I_S\left[\exp\left(\frac{qV_{BE}}{kT}\right)-1\right]\left(1+\frac{V_{CE}}{V_A}\right) \quad \text{and} \quad \beta = \frac{I_C}{I_B} \tag{6.1}$$

where β represents the current gain, V_A is the Early voltage, k is the Boltzmann constant, and T is absolute temperature.

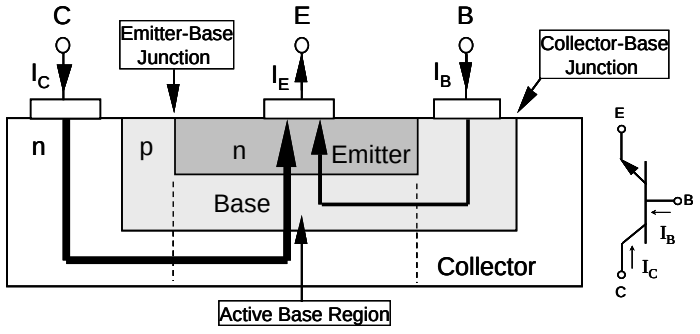


Figure 6.1 Simplified Cross-Section of a Vertical npn Bipolar Transistor

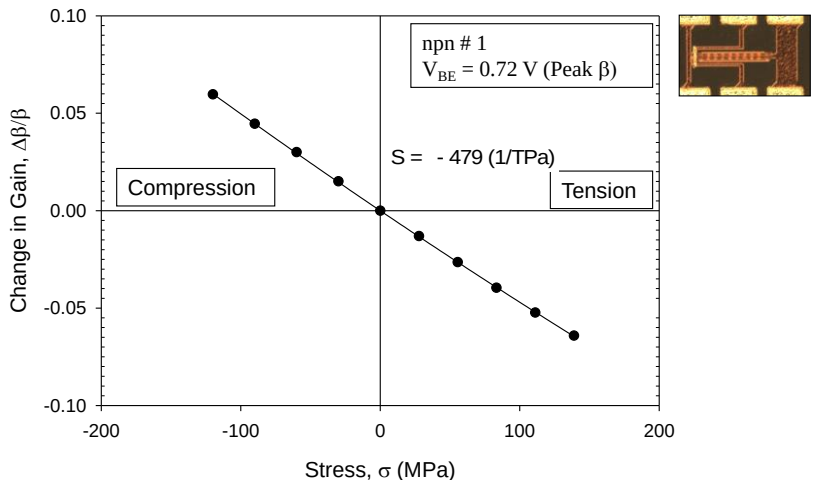


Figure 6.2 Change in Current Gain vs. Stress for a Sub-Micron npn Bipolar Transistor

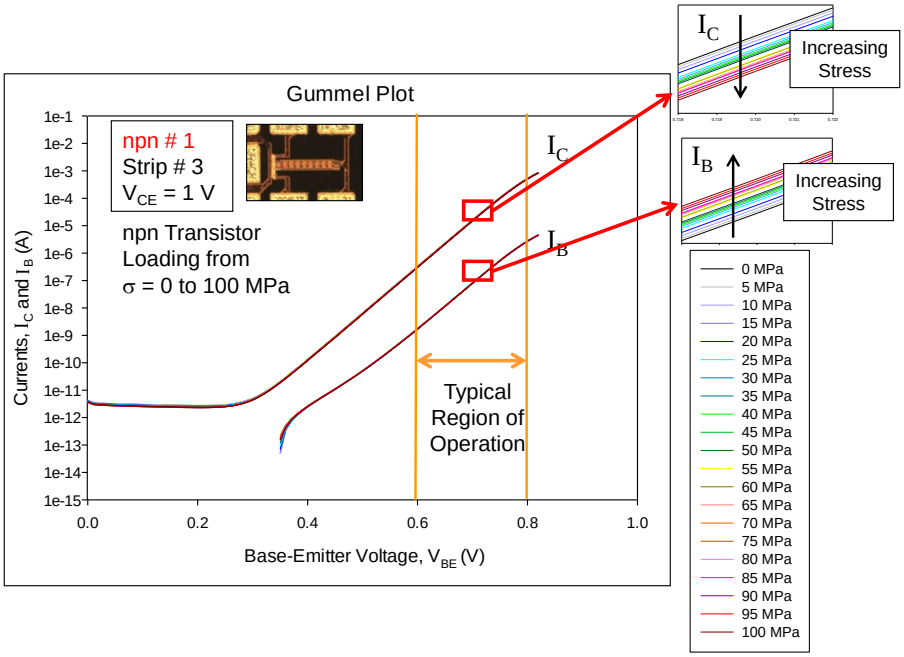


Figure 6.3 Stress Response of Gummel Plot for a npn Transistor

In bipolar transistors used in analog circuits (e.g., see Fig. 6.1), mechanical stresses/strains induce bandgap changes that affect both the mobility and carrier concentrations of the devices. Stress induced changes in I_S,β, and V_A lead to changes in

the I-V characteristics of the transistor (parametric shifts), and ultimately affect the performance of analog circuits that depend upon precise matching of devices, causing them to operate out of specifications. Fractional changes in collector current and current gain based upon Eq. (6.1) at a given operating point are

$$\frac{\Delta I_C}{I_C} = \frac{\Delta I_S}{I_S} - \left(\frac{V_{CE}}{V_A + V_{CE}}\right)\frac{\Delta V_A}{V_A} \quad \text{and} \quad \frac{\Delta\beta}{\beta} = \frac{\Delta I_C}{I_C} - \frac{\Delta I_B}{I_B} \tag{6.2}$$

As examples, Figs. 6.2-6.5 illustrate data we have measured for variations of the parameters of various vertical npn transistors subjected to moderate levels of uniaxial stress. Fig.6.2 presents a typical change in npn current gain as a function of tensile stress giving a 4.3% change for a 100 MPa tensile stress, corresponding to an effective piezoresistive coefficient of -430/TPa. Fig.6.3 shows the changes in the Gummel plot for the same BJT, and Fig. 6.4 presents further measurements of current gain versus tensile stress over a wide range of bias conditions.

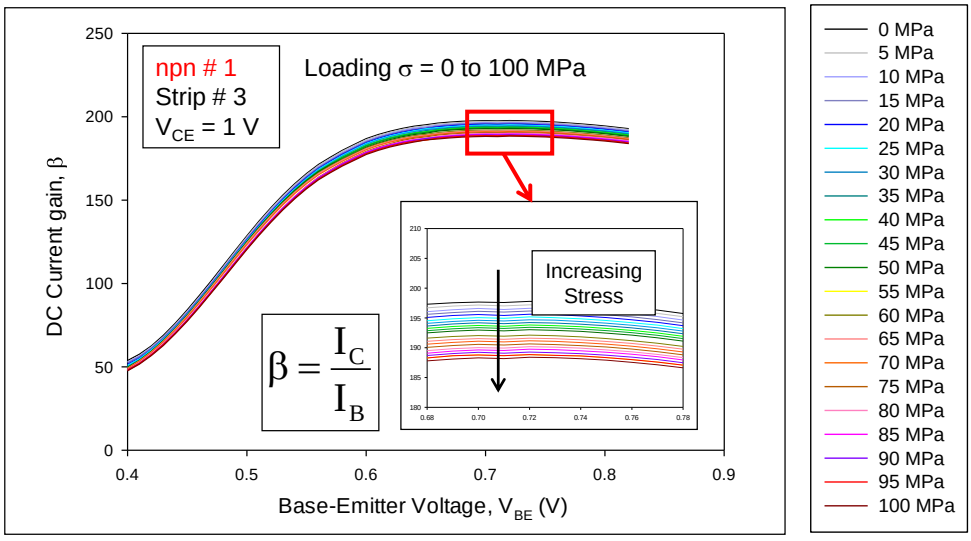


Figure 6.4 Current Gain vs. Base-Emitter Voltage and Stress for a npn Transistor

Fig.6.5 presents measured data for the stress dependence of Early Voltage. For the case in which V_{CE} is typically much less than V_A as in low voltage submicron scale devices, Eq. (6.2) indicates that we can neglect the impact of Early voltage changes on collector current since $V_{CE} << V_A$. Thus we focus here upon variations in I_S and β and neglect changes in V_A in the subsequent discussions.

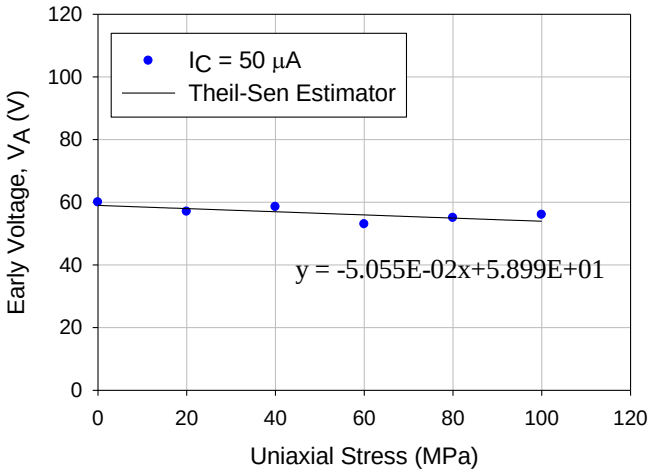


Figure 6.5 Measured Early Voltage for an npn Transistor

Stress effects in p-n junction diodes and bipolar transistors, such as those depicted above, have been reported by many investigators over the past 40 years [4, 136-146, 148, 150-159]. Such stress-induced phenomena in bipolar transistors have been collectively referred to as the piezojunction effect in which the mechanical stresses/strains induce bandgap changes that affect both the mobility and carrier concentrations of the device. These effects cause variations in the saturation current I_S of bipolar transistors: $I_S \propto \mu n_i^2$ where μ represents the minority carrier mobility, and n_i is the intrinsic carrier concentration.

$$I_S \propto \mu n_i^2 \quad \text{where} \quad n_i^2 \propto N_C N_V \exp\left(-\frac{E_G}{kT}\right) \tag{6.3}$$

The intrinsic carrier concentration is related to the densities of states in the conduction and valance bands, N_C and N_V respectively, and exponentially dependent upon the bandgap energy E_G. N_C and N_V are dependent upon the effective masses of the carriers and hence the energy band curvature.

Experimental data for resistors and resistive channels of CMOS devices have demonstrated that only the first order stress effects must be retained in the mobility terms in Eq. (6.3) [124, 130, 199]. However, most data for bipolar transistors in the literature illustrate non-linear (quadratic) variations of saturation current with applied uniaxial stress [154-159]. In addition, the nonlinear dependence of the electrical characteristics on uniaxial stress has been observed to be different for tension and compression and depends upon the direction of the applied stress.

In this work, we separate the mobility and intrinsic carrier concentration terms as in Eq. (6.4):

$$\frac{\Delta I_S}{I_S} = \frac{\Delta \mu}{\mu} + \frac{\Delta n_i^2}{n_i^2} \tag{6.4}$$

This approach provides new insight into the coupling of stress with the device physics of the bipolar transistor. For example, the slope of the linear portion of the $\Delta\beta/\beta$ curve in Fig. 6.2 is approximately $-430/\mathrm{TPa}$. Over an extended period of time, our research group has measured many npn transistors ranging from relatively large and deep double-diffused structures from our university laboratory to state-of-the-art sub-micron devices from our industrial contacts. The slope is amazingly consistent, typically falling in the range between 400 and 500/TPa. We believe there must be a relatively simple and

fundamental explanation for this behavior. The theory developed in this chapter explains these observations.

6.3 Piezoresistive Theory

Piezoresistance causes modulation of the electrical resistance of the material due to the application of mechanical stress. In the past our group extensively investigated the stress effects on resistors embedded on integrated chips. The relationship between resistor sensor response and applied stress is fully developed [82, 84, 88] and explained in Appendix A. The resistance of a conductor can be expressed in terms of resistivity ρ and conductively σ as

$$R = \rho\frac{L}{A} = \frac{1}{\sigma}\frac{L}{A} \quad \text{where} \quad \sigma = q\left(u_n n + u_p p\right) \tag{6.5}$$

where L is the length of the resistor and A is its cross-sectional area. Piezoresistance is caused by changes in the majority carrier mobility terms in Eq. (6.5) and the stress dependencies are expressed differently on different silicon surfaces. Two surfaces of primary interest here are depicted in Fig. 6.6. (100) silicon is now the most widely utilized material for IC fabrication, whereas (111) silicon has been historically utilized for bipolar transistor fabrication but is in more limited use today. In the following sections, discussions on the basic piezoresistive formulations used on those surfaces are presented.

6.3.1 (100) Silicon

The surface of the wafer is an (001) plane, and the [100] direction is normal to the wafer surface. The primed coordinate system are along [110] and $[\bar{1}10]$ directions which

are parallel and perpendicular to the primary flat of the wafer respectively. The crystallographic axes for the wafer are along the unprimed axes whereas the primed coordinate system is rotated 45° from the principal crystallographic axes. Eq. (6.6) represents the standard theory for piezoresistive behavior of conductors in (100) silicon in which the stresses in the resistance change equation are expressed as values in the principal (crystallographic) coordinate system in Fig. 6(a) as presented in Appendix A [77, 88].

$$\begin{aligned}\frac{\Delta R}{R} &= \left[\pi_{11}\sigma_{11} + \pi_{12}\left(\sigma_{22} + \sigma_{22}\right)\right] l^2 + \left[\pi_{11}\sigma_{22} + \pi_{12}\left(\sigma_{11} + \sigma_{33}\right)\right] m^2 \\ &+ \left[\pi_{11}\sigma_{33} + \pi_{12}\left(\sigma_{11} + \sigma_{22}\right)\right] n^2 \\ &+ 2\pi_{44}\left[\sigma_{12}\, l m + \sigma_{13}\, l n + \sigma_{23} m n\right] + \left[\alpha_1 T + \alpha_2 T^2 + \cdots\right]\end{aligned} \tag{6.6}$$

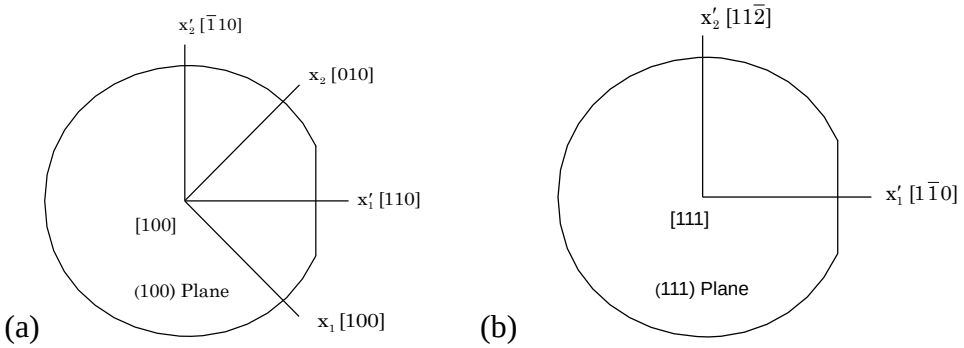


Figure 6.6 Principal and Primed Coordinate System for
(a) (100) silicon and (b) (111) Silicon
Note that the crystallographic axes are not in the plane of the (111) wafer.

Parameters π_{11}, π_{12}, and π_{44} are the three basic piezoresistive coefficients of silicon, and l, m, and n are the direction cosines describing the orientation of the conductor with respect to the [100] axis. The values of piezoresistive coefficients π_{11}, π_{12}, and π_{44} are different for n- and p-type silicon.

6.3.2 (111) Silicon

The surface of the wafer is a (111) plane, and the [111] direction is normal to the wafer plane. For (111) silicon, the crystallographic axes are not in the plane of the wafer, so the changes in resistance are cast in terms of the primed coordinate system in Fig. 6.6(b). As mentioned previously, the resistance change of an arbitrarily oriented in-plane resistor on the (111) surface can be expressed in terms of the stress components resolved in this natural wafer coordinate system as described below:

$$\begin{aligned}\frac{\Delta R}{R} &= \left[B_1\sigma'_{11} + B_2\sigma'_{22} + B_3\sigma'_{33} + 2\sqrt{2}\left(B_2 - B_3\right)\sigma'_{23} \right]\cos^2\phi \\ &+ \left[B_2\sigma'_{11} + B_1\sigma'_{22} + B_3\sigma'_{33} + 2\sqrt{2}\left(B_2 - B_3\right)\sigma'_{23} \right]\sin^2\phi \\ &+ \left[2\sqrt{2}\left(B_2 - B_3\right)\sigma'_{13} + \left(B_1 - B_2\right)\sigma'_{12} \right]\sin 2\phi + \left[\alpha_1 T + \alpha_2 T^2 + ... \right]\end{aligned} \tag{6.6}$$

where

$$B_1 = \frac{1}{2}(\pi_{11} + \pi_{12} + \pi_{44}) \quad B_2 = \frac{1}{6}(\pi_{11} + 5\pi_{12} - \pi_{44}) \quad B_3 = \frac{1}{3}(\pi_{11} + 2\pi_{12} - \pi_{44})$$

in which the "B" coefficients are convenient recurring combinations of the three basic piezoresistive coefficients. In this case, the direction cosines are calculated relative to the $[\bar{1}10]$axis.

6.4 Transistor Theory

We have found that the classic one-dimensional transistor model in Fig. 6.7 well characterizes the basic behavior of a bipolar transistor and yields the desired insights into the various stress dependencies. Fig. 6.7 includes the important currents in an npn device including collector current I_C and the two dominant components of base current: I_{BE} representing back injection into the emitter, and I_{BR} representing recombination in the base. As noted in Eq. (6.1), we are most interested in modeling collector current and

current gain, or equivalently collector current and base current, and to a lesser extent the Early voltage.Note that the “horizontal” currents are all actually directed normal to the wafer surface as in the transistor in Fig. 6.1.

The electrical conduction through the bipolar transistor is due to the minority carriers. In case of a vertical npn transistor, electrons from the n-type emitter are injected in the p-type base and diffuse to collector forming the collector current. Holes from base get injected into the n-type emitter and form the base current. Some of the holes ended up in combining with the electrons in the base forming the recombination current. Both electrons and holes are minority carriers for both base and emitter respectively. The diffusion current density is expressed by Eq. 6.8, where q is the charge, Dn and Dp are the diffusion coefficient and dn/dx and dp/dx are the carrier gradients.

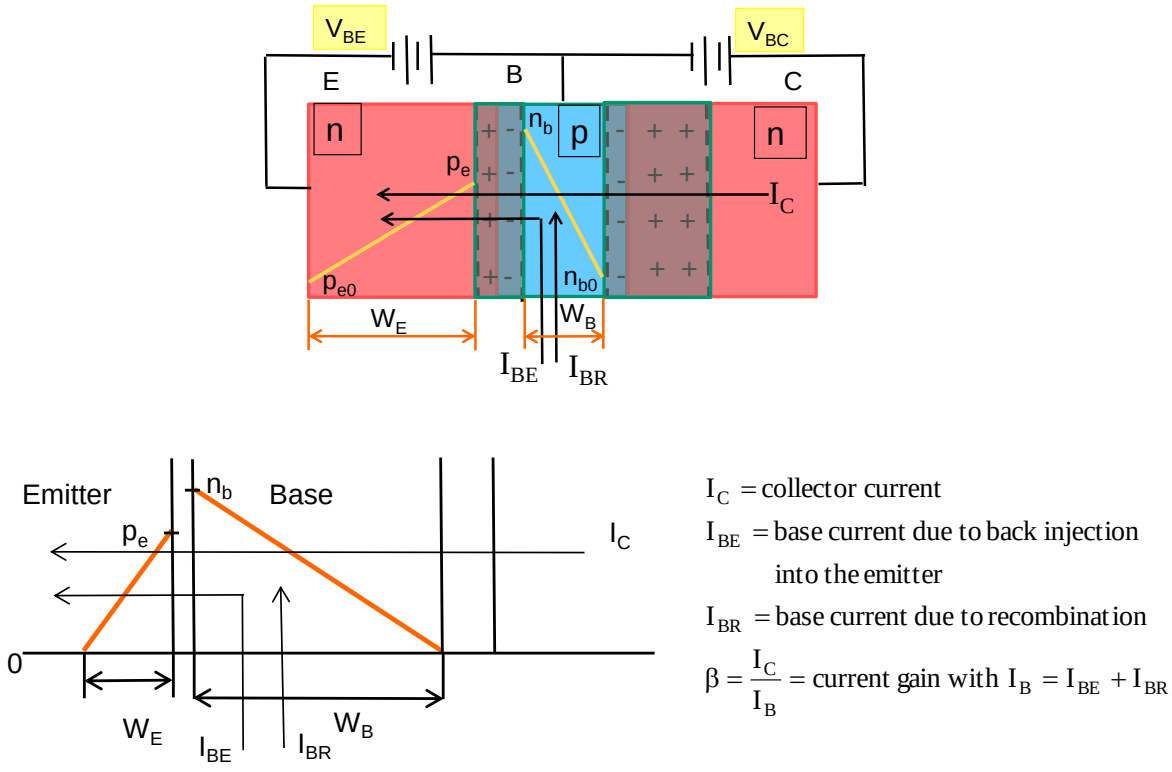


Figure 6.7 One Dimensional npn Transistor

$$\begin{aligned} &p-\text{side Base}, J_n = qD_n \frac{dn}{dx}; \\ &n-\text{side Emitter}, J_p = qD_p \frac{dp}{dx} \end{aligned} \tag{6.8}$$

For this diffusion process of electrons or holes to occur the diffusion current density J_n or J_p should be constant which means the minority carrier concentration gradient dn/dx or dp/dx must be constant or minority carrier distribution n or p must be linear. Therefore in Fig. 6.7 the minority carrier distribution is shown as a linear distribution, which is high at the injection point and gets low at the other boundary due to diffusion.

6.4.1 npn Transistors on (100) Silicon

Using the classical bipolar transistor theory, the collector and base currents for the npn transistor are expressed in the equations that follow in which G_B and G_E represent the Gummel numbers in the base and emitter.

Collector Current

$$I_C \propto \frac{qA_B}{G_B}\overline{D}_{nB}n_i^2 = V_T\frac{qA_B}{G_B}\bar{\mu}_{nB}n_i^2 \quad \text{with} \quad G_B = \int_{\text{Base}} p(x)dx \cong \int_{\text{Base}} N_A(x)dx \tag{6.9}$$

Base Current due to Back Injection

$$I_{BE} \propto qA_E\frac{\overline{D_{pE}}}{G_E}n_{iE}^2 = \frac{qA_EV_T}{G_E}\bar{\mu}_{pE}n_{iE}^2 \text{ and } G_E = \int_{\text{Emitter}} n(x)dx \cong \int_{\text{Emitter}} N_D(x)dx \tag{6.10}$$

Base Current due to Recombination

$$I_{BR} = qA_B\int_{\text{Base}}\frac{n-n_{B0}}{\tau_{nB}} \propto \frac{n_{iB}^2}{\tau_{nB}} \tag{6.11}$$

The normalized changes in the collector and base currents in Eq. (6.12) are found from Eqs. (6.9- 6.11).

$$\begin{aligned}
\frac{\Delta I_C}{I_C} &= \frac{\Delta \mu_{nB}}{\mu_{nB}} + \frac{\Delta n_{iB}^2}{n_{iB}^2} + \frac{\Delta V_{BE}}{V_T} + f_1(T) \\
&= -\pi_{12}^{nB}\left(\sigma_{11} + \sigma_{22}\right) - \pi_{11}^{nB}\sigma_{33} + \frac{\Delta n_{iB}^2}{n_{iB}^2} + \frac{\Delta V_{BE}}{V_T} + f_1(T) \\
\frac{\Delta I_{BE}}{I_{BE}} &= \frac{\Delta \mu_{pE}}{\mu_{pE}} + \frac{\Delta n_{iE}^2}{n_{iE}^2} + \frac{\Delta V_{BE}}{V_T} + f_2(T) \\
&= -\pi_{12}^{pE}\left(\sigma_{11} + \sigma_{22}\right) - \pi_{11}^{pE}\sigma_{33} + \frac{\Delta n_{iE}^2}{n_{iE}^2} + \frac{\Delta V_{BE}}{V_T} + f_2(T) \\
\frac{\Delta I_{BR}}{I_{BR}} &= \frac{\Delta n_{iB}^2}{n_{iB}^2} - \frac{\Delta \tau_{nB}}{\tau_{nB}} + f_3(T) \\
&\cong \frac{\Delta n_{iB}^2}{n_{iB}^2} + f_3(T)
\end{aligned} \tag{6.12}$$

The $f_1(T)$, $f_2(T)$ and $f_3(T)$ are the temperature terms associated with the expressions of the transistor currents which will be discussed later in this chapter. The coupling of stresses σ_{11} and σ_{22} on the chip surface into the vertical transistor currents are characterized by π_{12}, whereas the coupling of normal stress σ_{33} is characterized by π_{11}. The values of n_{iE} and n_{iB} may in fact differ due to bandgap narrowing in the emitter, and it is possible that the fractional changes in intrinsic carrier concentrations in the base and emitter under stress are not identical. This work actually indicates that they do appear to be slightly different due to the effects of heavy doping. Thus the deformation potentials may be different in the base and emitter.

6.4.2 pnp Transistors on (100) Silicon

The collector and base current expressions for the pnp transistors are similar to those of the npn transistors with appropriate changes in the piezoresistive coefficients for holes and electrons.

Collector Current

$$I_C \propto V_T \frac{qA_B}{G_B} \bar{\mu}_{pB} n_i^2$$

$$\frac{\Delta I_C}{I_C} = \frac{\Delta \mu_{pB}}{\mu_{pB}} + \frac{\Delta n_{iB}^2}{n_{iB}^2} + \frac{\Delta V_{BE}}{V_T} + f_5(T) \qquad (6.13)$$

$$= -\pi_{12}^{pB}\left(\sigma_{11} + \sigma_{22}\right) - \pi_{11}^{pB}\sigma_{33} + \frac{\Delta n_{iB}^2}{n_{iB}^2} + \frac{\Delta V_{BE}}{V_T} + f_5(T)$$

Base Current due to Back Injection

$$I_{BE} \propto \frac{qA_E V_T}{G_E} \bar{\mu}_{nE} n_{iE}^2$$

$$\frac{\Delta I_{BE}}{I_{BE}} = \frac{\Delta \mu_{nE}}{\mu_{nE}} + \frac{\Delta n_{iE}^2}{n_{iE}^2} + \frac{\Delta V_{BE}}{V_T} + f_6(T) \qquad (6.14)$$

$$= -\pi_{12}^{nE}\left(\sigma_{11} + \sigma_{22}\right) - \pi_{11}^{nE}\sigma_{33} + \frac{\Delta n_{iE}^2}{n_{iE}^2} + \frac{\Delta V_{BE}}{V_T} + f_6(T)$$

Base current due to recombination

$$I_{BR} = qA_B \int_{Base} \frac{p - p_{B0}}{\tau_{nB}} \propto \frac{n_{iB}^2}{\tau_{nB}}$$

$$\frac{\Delta I_{BR}}{I_{BR}} = \frac{\Delta n_{iB}^2}{n_{iB}^2} - \frac{\Delta \tau_{nB}}{\tau_{nB}} + f_7(T) \qquad (6.15)$$

$$\cong \frac{\Delta n_{iB}^2}{n_{iB}^2} + f_7(T)$$

6.4.3 Current Gain

The overall current gains for both npn and pnp transistors can now be written as

$$\beta = \frac{I_C}{I_{BE} + I_{BR}} \qquad (6.16)$$

and

$$\frac{\Delta\beta}{\beta}=\frac{\Delta I_C}{I_C}-\frac{\Delta I_B}{I_B}=\frac{\Delta I_C}{I_C}-\frac{\delta\Delta I_{BE}}{I_{BE}}-(1-\delta)\frac{\Delta I_{BR}}{I_{BR}} \qquad (6.17)$$

where $\delta=\dfrac{I_{BE}}{I_{BR}+I_{BE}}\le 1$

Parameter δ represents the fraction of current gain that is determined by back injection into the emitter. δ = 1 corresponds to 100% back injectionand δ = 0 corresponds to 100% recombination.

The behavior of the base current $I_B$with collector-base voltage V_{BC} changes can be used to determine δ.Base current has two parts, back injection into the emitter I_{BE} and recombination current I_{BR}. To understand the base current transport mode, the experimental method applied was to modulate base width W_B by increasing the reverse collector-base voltage V_{CB} while keeping either $I_B$or V_{BE}constant as can be seen from Fig. 6.8. Therefore increase of the reverse bias increases the depletion region in the base collector junction, that causes the base width to shrink, and as a result the minority carrier concentration gradient changes slope. Since I_C is proportional to minority carrier concentration gradient, the shift in carrier concentration gradient causes collector current to increase as can be seen from Eq. (6.8).This effect is known as the Early effect and is characterized by Early voltage V_A discussed earlier.

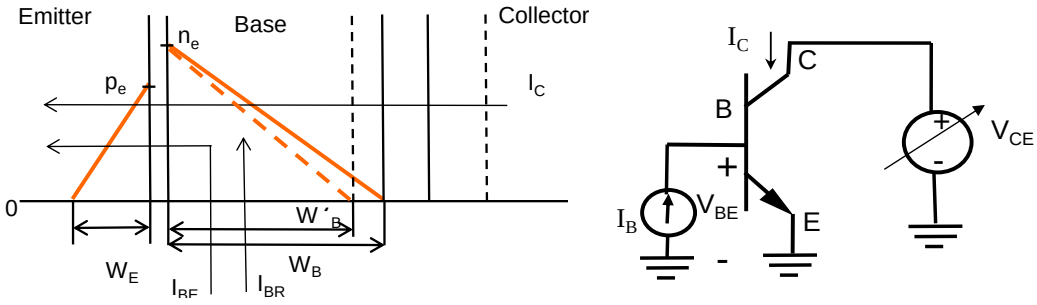


Figure 6.8 (Left) Demonstration of Early Effect in an 1D npn Transistor (Right), The Biasing Used for Early Effect

At the same time, if the base width decreases there will be less recombination and if the transistor is transport limited or the base current mainly comprises of recombination current I_{BR} then the change in base current $I_B$will be significant. Therefore, I_{BR} should show a dependence upon V_{CB} since the recombination current is proportional to the total minority carrier concentration in the base, whereas base current I_{BE}, injected back into the emitter, should be independent of V_{CB}.

Figure 6.9 presents the normalized variations of npn and pnp currents and/or voltages versus collector-base voltage. With constant I_B in Fig. 6.9(a), the npn base-emitter voltage dependence upon collector voltage is very small, yielding $\delta \approx 1$. For the pnp transistor in Fig. 6.9(b), the results show approximately a 6:1 difference in the slopes of the changes of the collector and base currents yielding $\delta \sim 6/7$. Therefore, in our experiments the base current in the npn transistors on (100) silicon is mainly due to the back injection of the holes and in case of pnp transistors it is due to the combination of both back injection and some recombination, with the back injection current still dominating.

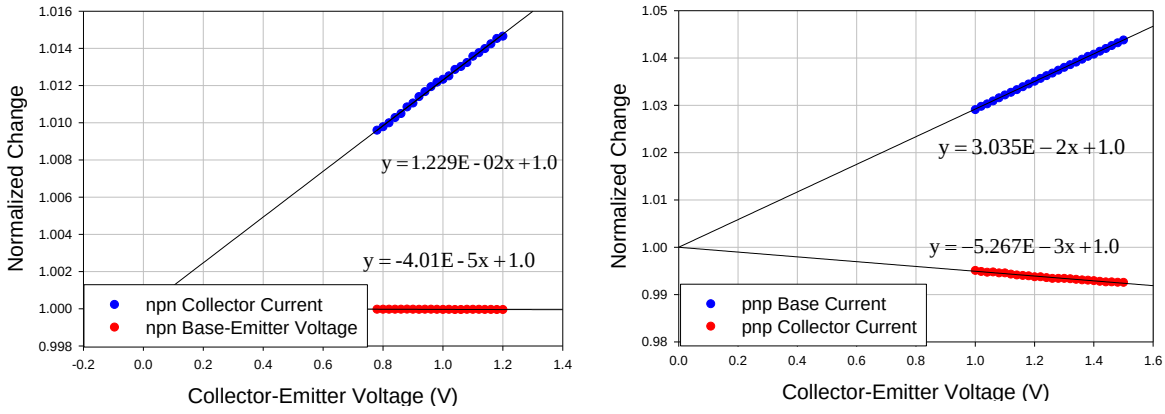


Figure 6.9 Measured npn I_C and V_{BE} versus V_{CE}(Left)
Measured pnp I_C and I_B versus V_{CE} (Right)

6.4.4 Overall npn and pnp Stress Dependencies

The stress dependencies resulting from the theory above for the npn and pnp transistors on (100) silicon are consolidated in Table 6.1, and similar results appear in Table 6.2 for transistors on the (111) surface in which the appropriate "B" coefficients have been substituted in the expressions.

Table 6.1 Vertical Transistor Stress Dependencies for (100) Silicon

Parameter	npn	pnp
$\frac{\Delta I_C}{I_C}$ and $\frac{\Delta I_S}{I_S}$ **	$-\pi_{12}^{nB}(\sigma_{11}+\sigma_{22})-\pi_{11}^{nB}\sigma_{33}+\frac{\Delta n_{iB}^2}{n_{iB}^2}+\frac{\Delta V_{BE}}{V_T}+f_1(T)$	$-\pi_{12}^{pB}(\sigma_{11}+\sigma_{22})-\pi_{11}^{pB}\sigma_{33}+\frac{\Delta n_{iB}^2}{n_{iB}^2}\frac{\Delta V_{BE}}{V_T}+f_5(T)$
$\frac{\Delta I_{BE}}{I_{BE}}$	$-\pi_{12}^{pE}(\sigma_{11}+\sigma_{22})-\pi_{11}^{pE}\sigma_{33}+\frac{\Delta n_{iE}^2}{n_{iE}^2}+\frac{\Delta V_{BE}}{V_T}+f_2(T)$	$-\pi_{12}^{nE}(\sigma_{11}+\sigma_{22})-\pi_{11}^{nE}\sigma_{33}+\frac{\Delta n_{iE}^2}{n_{iE}^2}+\frac{\Delta V_{BE}}{V_T}+f_6(T)$
$\frac{\Delta I_{BR}}{I_{BR}}$	$\frac{\Delta n_{iB}^2(\sigma)}{n_{iB}^2}+f_3(T)$	$\frac{\Delta n_{iB}^2(\sigma)}{n_{iB}^2}+f_7(T)$
$\frac{\Delta\beta}{\beta}$	$-\left(\pi_{12}^{nB}-\delta\pi_{12}^{pE}\right)(\sigma_{11}+\sigma_{22})-\left(\pi_{11}^{nB}-\delta\pi_{11}^{pE}\right)\sigma_{33}+\delta\left(\frac{\Delta n_{iB}^2(\sigma)}{n_{iB}^2}-\frac{\Delta n_{iE}^2(\sigma)}{n_{iE}^2}\right)+f_4(T)$	$-\left(\pi_{12}^{pB}-\delta\pi_{12}^{nE}\right)(\sigma_{11}+\sigma_{22})-\left(\pi_{11}^{pB}-\delta\pi_{11}^{nE}\right)\sigma_{33}+\delta\left(\frac{\Delta n_{iB}^2(\sigma)}{n_{iB}^2}-\frac{\Delta n_{iE}^2(\sigma)}{n_{iE}^2}\right)+f_8(T)$
Notes	$\frac{\Delta V_A}{V_A}\cong 0 \quad A_E=A_B \quad \mu_n\propto T^{-2.4} \quad \mu_p\propto T^{-2.2}$ $\Delta\beta/\beta=\frac{\Delta I_S}{I_S}-\delta\frac{\Delta I_{BE}}{I_{BE}}-(1-\delta)\frac{\Delta I_{BR}}{I_{BR}} \quad \delta=\frac{I_{BE}}{I_{BE}+I_{BR}}$ $I_C\cong I_S\exp\left(\frac{V_{BE}}{V_T}\right) \quad \frac{\Delta I_S}{I_S}=\frac{\Delta I_C}{I_C}-\frac{\Delta V_{BE}(\sigma)}{V_T}+\frac{V_{BE}}{V_T}\frac{\Delta T}{T}$ ** The expression for $\Delta I_S/I_S$ is the same as $\Delta I_C/I_C$ with the $\Delta V_{BE}/V_T$ term removed.	

Table 6.2 Vertical Transistor Stress Dependencies for (111) Silicon

Parameter	npn	pnp
$\frac{\Delta I_C}{I_C}$ and $\frac{\Delta I_S}{I_S}^{**}$	$-B_3^{nB}\left(\sigma_{11}^{'}+\sigma_{22}^{'}\right)-\left(B_1^{nB}+B_2^{nB}-B_3^{nB}\right)\sigma_{33}^{'}$ $+\frac{\Delta n_{iB}^2}{n_{iB}^2}+\frac{\Delta V_{BE}}{V_T}+f_1(T)$	$-B_3^{pB}\left(\sigma_{11}^{'}+\sigma_{22}^{'}\right)-\left(B_1^{pB}+B_2^{pB}-B_3^{pB}\right)\sigma_{33}^{'}$ $+\frac{\Delta n_{iB}^2}{n_{ib}^2}+\frac{\Delta V_{BE}}{V_T}+f_5(T)$
$\frac{\Delta I_{BE}}{I_{BE}}$	$-B_3^{pE}\left(\sigma_{11}^{'}+\sigma_{22}^{'}\right)-\left(B_1^{pE}+B_2^{pE}-B_3^{pE}\right)\sigma_{33}^{'}$ $+\frac{\Delta n_{iE}^2}{n_{iE}^2}+\frac{\Delta V_{BE}}{V_T}+f_2(T)$	$-B_3^{nE}\left(\sigma_{11}^{'}+\sigma_{22}^{'}\right)-\left(B_1^{nE}+B_2^{nE}-B_3^{nE}\right)\sigma_{33}^{'}$ $+\frac{\Delta n_{iE}^2}{n_{iE}^2}+\frac{\Delta V_{BE}}{V_T}+f_6(T)$
$\frac{\Delta I_{BR}}{I_{BR}}$	$\frac{\Delta n_{iB}^2(\sigma)}{n_{iB}^2}+f_3(T)$	$\frac{\Delta n_{iB}^2(\sigma)}{n_{iB}^2}+f_7(T)$
$\frac{\Delta\beta}{\beta}$	$-\left(B_3^{nB}-\delta B_3^{pE}\right)\left(\sigma_{11}^{'}+\sigma_{22}^{'}\right)$ $-\left[\left(B_1^{nB}+B_2^{nB}-B_3^{nB}\right)-\delta\left(B_1^{pE}+B_2^{pE}-B_3^{pE}\right)\right]\sigma_{33}^{'}$ $+\delta\left(\frac{\Delta n_{iB}^2}{n_{iB}^2}-\frac{\Delta n_{iE}^2}{n_{iE}^2}\right)+f_4(T)$	$-\left(B_3^{pB}-\delta B_3^{nE}\right)\left(\sigma_{11}^{'}+\sigma_{22}^{'}\right)$ $-\left[\left(B_1^{pB}+B_2^{pB}-B_3^{pB}\right)-\delta\left(B_1^{nE}+B_2^{nE}-B_3^{nE}\right)\right]\sigma_{33}^{'}$ $+\delta\left(\frac{\Delta n_{iB}^2}{n_{iB}^2}-\frac{\Delta n_{iE}^2}{n_{iE}^2}\right)+f_8(T)$
Notes	$\frac{\Delta V_A}{V_A}\cong 0 \quad A_E=A_B \quad \mu_n\propto T^{-2.4} \quad \mu_p\propto T^{-2.2}$ $\Delta\beta/\beta=\frac{\Delta I_S}{I_S}-\delta\frac{\Delta I_{BE}}{I_{BE}}-(1-\delta)\frac{\Delta I_{BR}}{I_{BR}} \quad \delta=\frac{I_{BE}}{I_{BE}+I_{BR}}$ $I_C\cong I_S\exp\left(\frac{V_{BE}}{V_T}\right) \quad \frac{\Delta I_S}{I_S}=\frac{\Delta I_C}{I_C}-\frac{\Delta V_{BE}(\sigma)}{V_T}+\frac{V_{BE}}{V_T}\frac{\Delta T}{T}$ **The expression for $\Delta I_S/I_S$ is the same as $\Delta I_C/I_C$ with the $\Delta V_{BE}/V_T$ term removed.	

6.4.5 Temperature Dependencies

Because of the exponential dependences in Eq. (6.1) as well as in expressions of the intrinsic carrier concentrations in Eq. (6.3), temperature must be carefully controlled during experiments. The temperature coefficients of the currents and current gain have

been summarized in Table 6.3. Current gain has a much lower (30X) temperature dependence than either the collector or base currents, and thus β is much easier to measure accurately.

Table 6.3 Vertical Transistor Theory Temperature Dependencies

Parameter	npn	pnp
$\frac{\Delta I_C}{I_C}$	$f_1(T)=\left(1.6+\frac{E_{GB}}{kT}-\frac{V_{BE}}{V_T}\right)\frac{\Delta T}{T} \quad \left(\cong 18\frac{\Delta T}{T}\right)$	$f_5(T)=\left(1.8+\frac{E_{GB}}{kT}-\frac{V_{BE}}{V_T}\right)\frac{\Delta T}{T}$
$\frac{\Delta I_{BE}}{I_{BE}}$	$f_2(T)=\left(1.8+\frac{E_{GE}}{kT}-\frac{V_{BE}}{V_T}\right)\frac{\Delta T}{T} \quad \left(\cong 18\frac{\Delta T}{T}\right)$	$f_6(T)=\left(1.6+\frac{E_{GE}}{kT}-\frac{V_{BE}}{V_T}\right)\frac{\Delta T}{T}$
$\frac{\Delta I_{BR}}{I_{BR}}$	$f_3(T)=\left(3+\frac{E_{GB}}{kT}-\frac{V_{BE}}{V_T}\right)\frac{\Delta T}{T} \quad \left(\cong 19\frac{\Delta T}{T}\right)$	$f_7(T)=\left(3+\frac{E_{GB}}{kT}-\frac{V_{BE}}{V_T}\right)\frac{\Delta T}{T}$
$\frac{\Delta\beta}{\beta}$	$f_4(T)=\left(-1.4+1.2\delta+\delta\frac{E_{GBE}}{kT}\right)\frac{\Delta T}{T} \quad \left(\cong 0.6\frac{\Delta T}{T}\right)$	$f_8(T)=\left(-1.2+1.4\delta+\delta\frac{E_{GBE}}{kT}\right)\frac{\Delta T}{T}$
Notes	$\frac{\Delta V_A}{V_A}\cong 0 \quad A_E=A_B \quad \mu_n \propto T^{-2.4} \quad \mu_p \propto T^{-2.2}$ $\Delta\beta/\beta=\frac{\Delta I_S}{I_S}-\delta\frac{\Delta I_{BE}}{I_{BE}}-(1-\delta)\frac{\Delta I_{BR}}{I_{BR}} \quad \delta=\frac{I_{BE}}{I_{BE}+I_{BR}}$ $I_C\cong I_S\exp\left(\frac{V_{BE}}{V_T}\right) \quad \frac{\Delta I_S}{I_S}=\frac{\Delta I_C}{I_C}-\frac{\Delta V_{BE}(\sigma)}{V_T}+\frac{V_{BE}}{V_T}\frac{\Delta T}{T}$	

6.4.6 Simplifications and Numerical Estimates

In order to understand and predict the expected transistor behavior from the results in Tables 6.1 and 6.2, we need values for the piezoresistive coefficients for the

minority carriers and for the normalized changes in intrinsic carrier concentration versus applied stress.

6.5 Intrinsic Carrier Concentration (n_i)

At thermodynamic equilibrium, the product of the concentration of conduction band electrons n and the concentration of the valence band holes p is equal to the square of intrinsic carrier concentration ($pn = n_i^2$).. The intrinsic carrier concentration (n_i) is a constant for a semiconductor material. As can be seen from Eq. (6.3), $n_i$has an exponential dependence on bandgap and temperature of the material. The thermal excitation will cause more electrons to get free from the valence band into the conduction band causing the intrinsic carrier concentration to increase, the larger the bandgap, the less thermally excited carriers will be able to get into conduction band from valence band. The intrinsic carrier concentration is a function of densities of states in the conduction and valance bands, N_C and N_V respectively. N_C and N_V are dependent upon the effective masses of the carriers and hence the energy band curvature.

The intrinsic carrier concentration is significant in bipolar junction transistors since electrical conduction in the BJTs happens due to the minority carriers, and the intrinsic carrier concentration is used to determine the minority carrier concentrations as can be seen from the from Eq. (6.18)

$$n_b = \frac{n_i^2}{N_A} e^{\left(\frac{qV_{BE}}{kT}\right)} \qquad p_e = \frac{n_i^2}{N_D} e^{\left(\frac{qV_{BE}}{kT}\right)} \tag{6.18}$$

in which n_b is electron concentration in the base and p_e is the hole concentration in the emitter. In Eq (6.18) N_A is the doping in the p-type base and N_D is the doping in n-type

emitter of an npn transistor. $n_b$and p_e are both minority carriers in base and emitter respectively.

Mechanical stress causes a shift in the conduction band and valence band edges of the semiconductor and also in the density of states due to the redistribution of the carriers which result in changes in intrinsic carrier concentration with stress. Creemer et al [154-159] have calculated $\Delta n_i^2 / n_i^2$ for uniaxial and shear stresses along different crystal directions. They used $k\hat{p}$ method based upon solid-state physics incorporating full stress/strain relationship with deformation potentials from the theory of Bir and Pikus[171]. Fig. 6.10 represents our quadratic fits to their data with the coefficients listed in Table 6.4.

6.6 Minority Carrier Piezoresistive Coefficients

The expressions in Tables 6.1 and 6.2 involve piezoresistive coefficient data for minority carrier mobilities, whereas the bulk of the available literature data piezoresistive coefficient data is for majority carriers. This issue is addressed in Fig. 6.11 which compares the majority and minority carrier mobilities from recent research results [200, 201]. As shown in the boxes in the Fig. 6.11, the emitter doping concentration is in the range of the $10^{21}/cm^3$ and the base doping is in the range of 10^{17} to 10^{18} $/cm^3$. For typical base and emitter doping levels, we observe that the pairs of majority and minority electron and hole mobilities are very similar to each other. Since piezoresistive coefficeints are proportional to mobilities of the carriers, so we assume here that the piezoresistive properties of minority carriers are the same as those of majority carriers for equivalent doping levels.

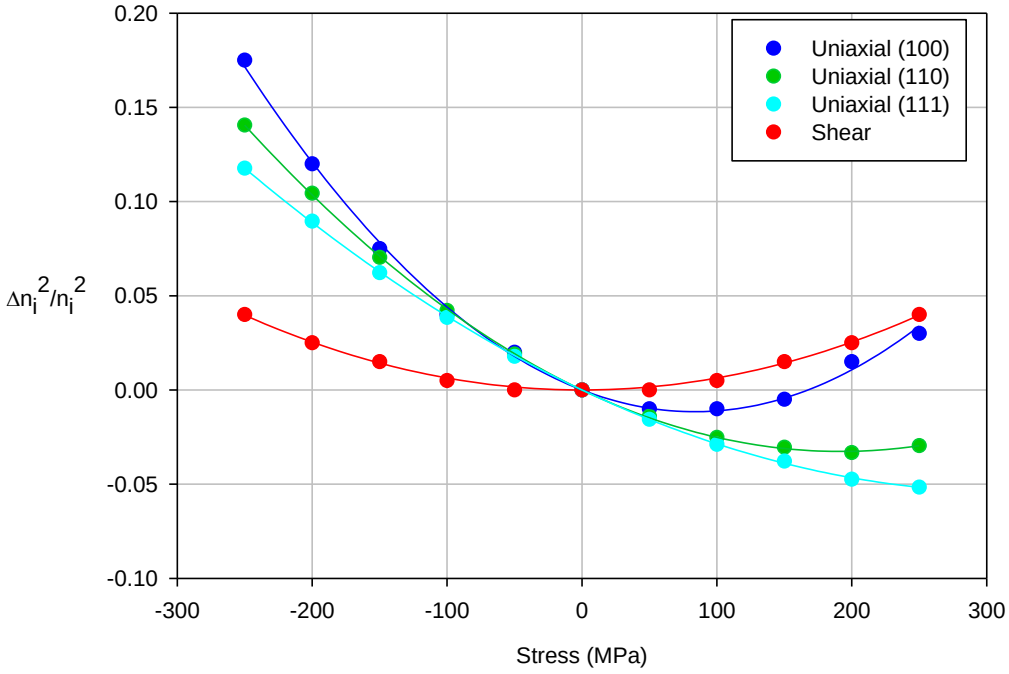


Figure 6.10 Calculations done by Creemer, et al. using kp̂ method
Employing Bir and Pikus Deformation Potential Theory

Table 6.4 Quadratic Fits to Theoretical Plots of Creemer [171]	
Stress Orientation	$\Delta n_i^2 / n_i^2$
[100]	$1.644\text{x}10^{-6}\sigma^2 - 2.755\text{x}10^{-4}\sigma$
[110]	$8.873\text{x}10^{-7}\sigma^2 - 3.403\text{x}10^{-4}\sigma$
[111]	$5.285\text{x}10^{-7}\sigma^2 - 3.387\text{x}10^{-4}\sigma$
Shear	$6.353\text{x}10^{-7}\sigma^2$

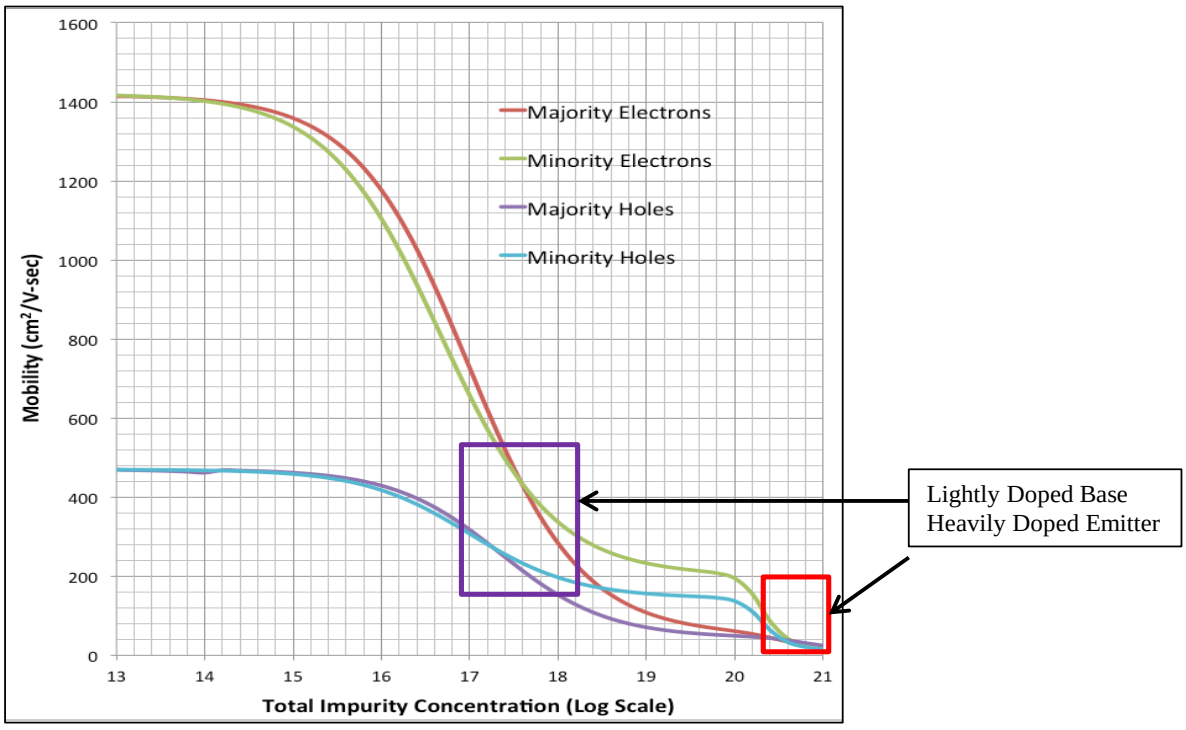


Figure 6.11 Comparison of Majority and Minority Carrier Mobilities versus Impurity Concentration

6.6.1 Piezoresistive Coefficient Simplifications

Table 6.6-A presents our best estimates of the complete set of piezoresistive coefficients for use with npn and pnp bipolar junction transistors on (100) and (111) silicon. These are based upon the original results of Smith [23], the work of Kanda[149], and Cho[104].Table 6.6-B presents coefficient simplifications to help understand the results and predict stress dependent behavior. First-order solid-state theory predicts electrons to have a significant response to normal stress components and no response to shear stress. In contrast, holes are predicted to have negligible response to normal

stresses and a large response to shear stresses. In addition, theory indicates that $\pi_{11} = -2\pi_{12}$ for electrons. The classical results of Smith [23] for lightly doped coefficients support these theoretical results in which π_{11} and π_{22} are large for electrons, whereas π_{44} is by far the largest coefficient for holes (Table 6.5). The other coefficients are much smaller. It is also well known from the literature that the coefficients are significantly reduced with moderate to heavy doping, and we can get estimates from the data of Cho [104] regarding the magnitudes of the piezoresistive coefficients.

Table 6.5 Piezoresistive Coefficients in Lightly-Doped Silicon [41]

Coefficient	n-type Si ($\times 10^{-12}$ Pa^{-1})	p-type Si ($\times 10^{-12}$ Pa^{-1})
π_{11}	-1020	+66
π_{12}	+534	-11
π_{44}	-136	+1380
$\pi_S = \pi_{11} + \pi_{12}$	-488	+55
$\pi_D = \pi_{11} - \pi_{12}$	-1560	+77
B_1	-311	+718
B_2	+298	-228
B_3	+61	-442
$B_1 - B_2$	-609	+946
$B_1 = \frac{\pi_{11} + \pi_{12} + \pi_{44}}{2}$ $B_2 = \frac{\pi_{11} + 5\pi_{12} - \pi_{44}}{6}$ $B_3 = \frac{\pi_{11} + 2\pi_{12} - \pi_{44}}{3}$		

The simplified coefficients in Table 6.6 result from application of the above results for the basic dependence of holes and electrons due to stress:

1. Electrons have negligible response to shear stress. Thus $\pi_{44} \cong 0$ in n-type silicon.

2. Holes only respond to shear stress. Thus π_{11} and $\pi_{12} \cong 0$ in p-type silicon.

The numerical results from Table 6.6 are incorporated in Table 6.7 for BJTs on (100) silicon and in Table 6.8 for (111) material.

Table 6.6 Piezoresistive Coefficient Estimates for Silicon Bipolar Transistors

$N_{Bavg} = 10^{18}/cm^3$ $N_{Eavg} = 1 \times 10^{21}/cm^3$

	npn Transistors		pnp transistors	
Coefficient	π^{nB} (x 10^{-12} Pa^{-1})	π^{pE} (x 10^{-12} Pa^{-1})	π^{nE} (x 10^{-12} Pa^{-1})	π^{pB} (x 10^{-12} Pa^{-1})
π_{11}	-600	20	-100	30
π_{12}	+300	-10	+50	-15
π_{44}	-70	+200	-10	+750
$\pi_S = \pi_{11} + \pi_{12}$	-300	+10	-50	+30
$\pi_D = \pi_{11} - \pi_{12}$	-900	+10	-150	+30
B_1	-260	+105	-30	+390
B_2	+235	-30	+25	-120
B_3	+25	-65	-5	-240
$B_1 + B_2 - B_3$	-50	+140	-10	+500

$$B_1 = \frac{\pi_{11} + \pi_{12} + \pi_{44}}{2} \qquad B_2 = \frac{\pi_{11} + 5\pi_{12} - \pi_{44}}{6} \qquad B_3 = \frac{\pi_{11} + 2\pi_{12} - \pi_{44}}{3}$$

Table 6.7 Simplified Piezoresistive Coefficient Estimates for Silicon Bipolar Transistors

$N_{Bavg} = 10^{18}/cm^3$ $N_{Eavg} = 10^{21}/cm^3$

	npn Transistors		pnp transistors	
Coefficient	π^{nB} (x 10^{-12} Pa^{-1})	π^{pE} (x 10^{-12} Pa^{-1})	π^{nE} (x 10^{-12} Pa^{-1})	π^{pB} (x 10^{-12} Pa^{-1})
π_{11}	-600	0	-200	0
π_{12}	+300	0	+100	0
π_{44}	0	+200	0	+750
$\pi_S = \pi_{11} + \pi_{12}$	-300	0	-50	0
$\pi_D = \pi_{11} - \pi_{12}$	-900	0	-150	0
B_1	-150	+100	-25	+375
B_2	+150	-35	+25	-125
B_3	0	-65	0	-250
$B_1 + B_2 - B_3$	0	+130	0	+500

Electrons have negligible response to shear stress. Thus $\pi_{44} \cong 0$ in n-type silicon.

Holes only respond to shear stress. Thus π_{11} and $\pi_{12} \cong 0$ in p-type silicon.

6.6.2 Theoretical Model for Uniaxial Stress

It is much easier to understand what to expect based upon the simplified results in Table 6.7. Equivalent arguments correspond to Table 6.8.

Table 6.8 Simplified Stress Dependencies – (100) silicon

Uniaxial Stress $(\sigma_{11}+\sigma_{22})=\sigma$ .Vertical Transistors

Constant V_{BE} – See Table 6.3 for Temperature Dependencies

Parameter	npn	Pnp
$\frac{\Delta I_C}{I_C}$	$-\frac{300}{TPa}\sigma+\frac{\Delta n_{iB}^2(\sigma)}{n_{iB}^2}$	$\frac{\Delta n_{iB}^2(\sigma)}{n_{iB}^2}$
$\frac{\Delta I_{BE}}{I_{BE}}$	$\frac{\Delta n_{iE}^2(\sigma)}{n_{iE}^2}$	$-\frac{100}{TPa}\sigma'_{11}+\frac{\Delta n_{iE}^2(\sigma)}{n_{iE}^2}$
$\frac{\Delta I_{BR}}{I_{BR}}$	$\frac{\Delta n_{iB}^2(\sigma)}{n_{iB}^2}$	$\frac{\Delta n_{iB}^2}{n_{iB}^2}$
$\frac{\Delta\beta}{\beta}$	$-\frac{300}{TPa}\sigma+\delta\left(\frac{\Delta n_{iB}^2(\sigma)}{n_{iB}^2}-\frac{\Delta n_{iE}^2(\sigma)}{n_{iE}^2}\right)$	$+\frac{100}{TPa}\sigma+\delta\left[\left(\frac{\Delta n_{iB}^2(\sigma)}{n_{iB}^2}-\frac{\Delta n_{iE}^2(\sigma)}{n_{iE}^2}\right)\right]$
Notes	$\frac{\Delta\beta_\gamma}{\beta_\gamma}=\frac{\Delta I_C}{I_C}-\frac{\Delta I_{BE}}{I_{BE}}-\frac{\Delta I_{BR}}{I_{BR}}$ $\quad \delta=\frac{I_{BE}}{I_{BE}+I_{BR}}\le 1$ Measured values of δ for our transistors: npn $\delta\cong 1$; pnp $\delta\cong 6/7$	

6.6.2.1 pnp Transistors

- Collector current variation in the pnp transistor is dominated by to variations in intrinsic carrier concentration in the lightly doped base. Thus it provides a direct test of the $\Delta n_i^2/n_i^2$ results of Creemer et al. [154-159].

- pnp base current characterization is completed by adding a weak pieozresistive term (100σ/ TPa) to the intrinsic carrier concentration variation.
- Note that the expressions for n_{iE} and n_{iB} variations will both be present in the total base current expression and may not be equal. Current gain would be expected to have a linear response if the two intrinsic carrier concentration terms were to cancel out. However our work shows that they do not cancel.

Table 6.9 Simplified Stress Dependencies – (111) Silicon
$(\sigma'_{11}+\sigma'_{22})=\sigma$ - Vertical Transistors - Silicon
Constant V_{BE} – See Table 6.3 for Temperature Dependencies

Parameter	npn	pnp
$\frac{\Delta I_C}{I_C}$	$+\frac{\Delta n_{iB}^2(\sigma)}{n_{iB}^2}$	$+\frac{250}{TPa}\sigma'_{11}+\frac{\Delta n_{iB}^2(\sigma)}{n_{iB}^2}$
$\frac{\Delta I_{BE}}{I_{BE}}$	$\frac{65}{TPa}\sigma+\frac{\Delta n_{iE}^2(\sigma)}{n_{iE}^2}$	$\frac{\Delta n_{iE}^2(\sigma)}{n_{iE}^2}$
$\frac{\Delta I_{BR}}{I_{BR}}$	$\frac{\Delta n_{iB}^2}{n_{iB}^2}$	$\frac{\Delta n_{iB}^2}{n_{iB}^2}$
$\frac{\Delta\beta}{\beta}$	$\delta\left[-\frac{65}{TPa}\sigma+\left(\frac{\Delta n_{iB}^2}{n_{iB}^2}-\frac{\Delta n_{iE}^2}{n_{iE}^2}\right)\right]$	$+\frac{250}{TPa}\sigma+\delta\left(\frac{\Delta n_{iB}^2}{n_{iB}^2}-\frac{\Delta n_{iE}^2}{n_{iE}^2}\right)$
Notes	$\frac{\Delta\beta}{\beta}=\frac{\Delta I_C}{I_C}-\frac{\Delta I_{BE}}{I_{BE}}-\frac{\Delta I_{BR}}{I_{BR}}\qquad \delta=\frac{I_{BR}}{I_{BE}+I_{BR}}\le 1$	

6.6.2.2 npn Transistors

- Collector current variation in the npn transistor is similar to base current in the pnp, with a substantial linear mobility term added to variations in intrinsic carrier concentration in the lightly doped base.

- npn base current is almost entirely due to back injection into the emitter and provides direct look at intrinsic carrier concentration variations in the heavily doped emitter.
- Current gain would be expected to have a linear response from mobility variations if the two intrinsic carrier concentration terms cancel out. Again, our work indicates they often do not cancel. See discussion concerning Fig. 6.12 in next section.

Similar simplification results appear in Table 6.8 for (111) silicon.

6.7 Correlation of Theory with Experimental Results

6.7.1 (100) Silicon

Our test transistors come from a complementary bipolar technology with npn and pnp transistor test devices in close proximity to each other, so we expect the intrinsic carrier changes in emitter and base to be similar both both npn and pnp transistor. Therefore, our work provides a unique chance to explore the differences between the stress behavior of the intrinsic carrier concentrations in the base and emitter.

pnp Transistors:

According to Table 6.7, the collector current of the pnp transistor will directly mirror the changes of intrinsic carrier concentration in the base. In Fig. 6.12, the comparison between the theory and the experimental data of the pnp collector current is presented. The solid line represent fits of the numerical results in Fig. 6.10 and Table 6.6 to the data. As evident from the plot, the pnp collector current data is almost an exact fit to numerical values in Table 6.4 verifying the calculations of Creemer et al. [170-175].

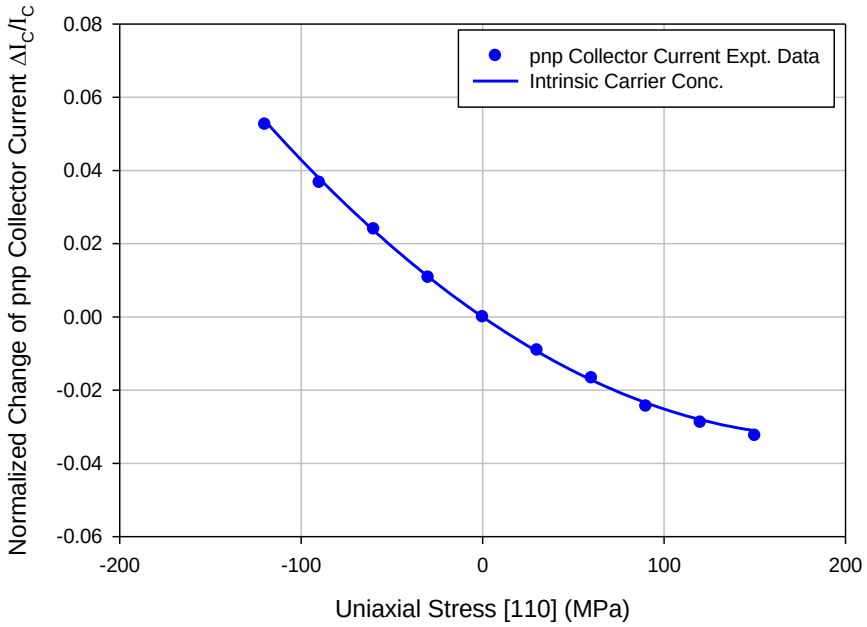


Figure 6.12 Comparison of pnp Collector Current with Theory

As mentioned earlier in this chapter that base current in pnp transistor has combination of both the back injection current and the recombination current and indicated a $\delta \approx 6/7$. The base current expression for pnp transistor is shown in Eq. 6.19.

$$\frac{\Delta I_{B_{pnp}}}{I_{B_{pnp}}} = -\delta \pi_{12}^{nE} \sigma + \frac{\Delta n_{iB}^2}{n_{iB}^2} + \delta \left(\frac{\Delta n_{iE}^2}{n_{iE}^2} - \frac{\Delta n_{iB}^2}{n_{iB}^2} \right) \tag{6.19}$$

Fig. 6.13 shows the correlation between the pnp base current experimental data and that of theory. The theoretical fit shown in the plot is achieved with a 100/TPa piezoresistive coefficient and assuming intrinsic carrier concentration change in both emitter and base to be equal. The base current fit with theory shows a good correlation with some discrepancies at the extremities. This discrepancies can be due to the fact that the intrinsic carrier changes with stress in base and emitter are not same. This is because there may be some bandgap narrowing due to the heavy doping in the emitter.

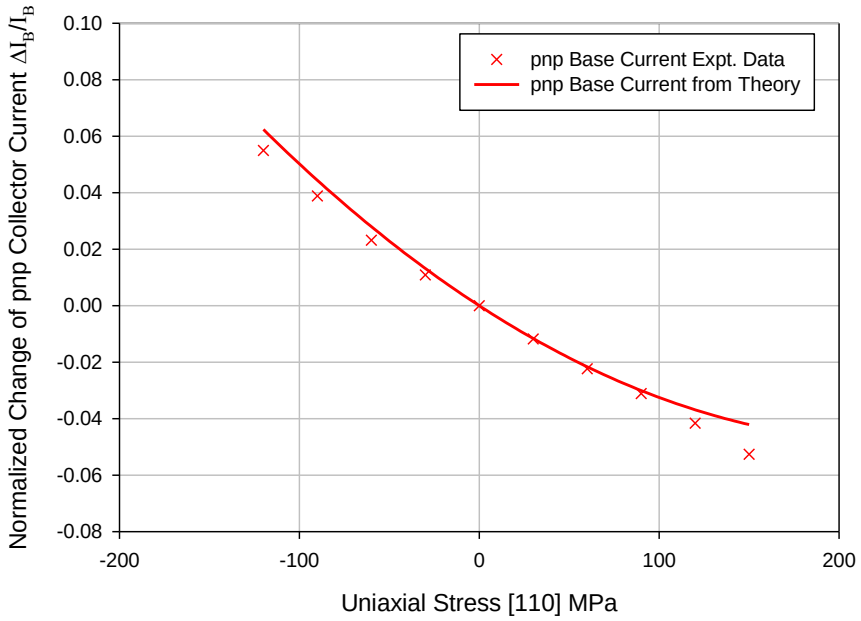


Figure 6.13 Comparison of pnp Base Current with Theory

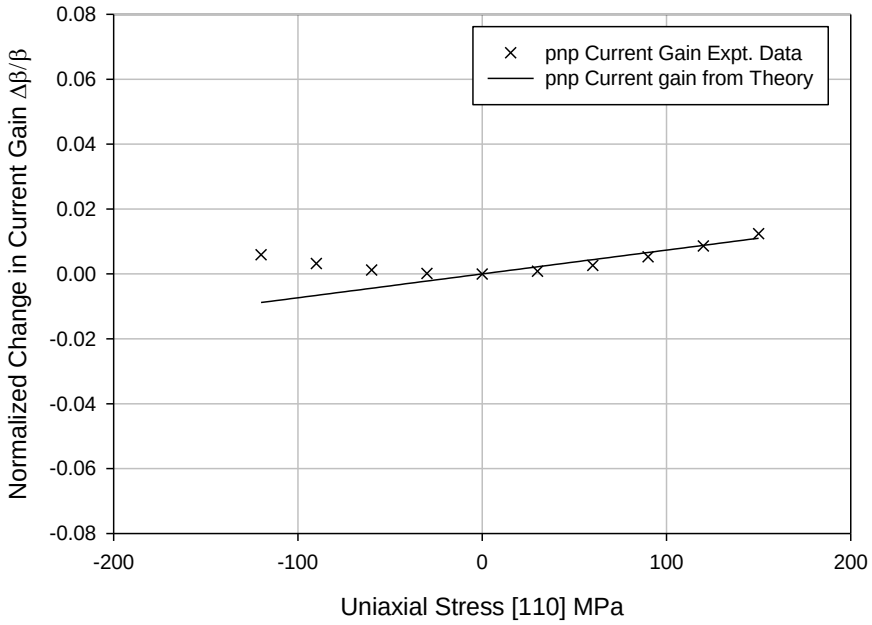


Figure 6.14 Comparison of pnp Current Gain with Theory

In Fig. 6.14 the comparison between the theoretical and experimental results of the pnp current gain is presented. The plot shows that the experimental current gain plot

is almost a pure quadratic plot. The theoretical fit is again without considering the changes in intrinsic carrier concentration due to bandgap narrowing. If both the intrinsic carrier changes were same the plot would have showed a linear trend as can be seen from the theoretical fit. As mentioned earlier the reason for this divergence may be due to the bandgap narrowing under stress.

npn Transistors:

In case of npn, measurements results of δ in Fig. 6.9(a) indicate that the base current of the npn is all due to back injection into the emitter so that the npn base current will provide a view of the changes of intrinsic carrier concentration in the emitter, but may exhibit differences due to heavy doping effects in the emitter.

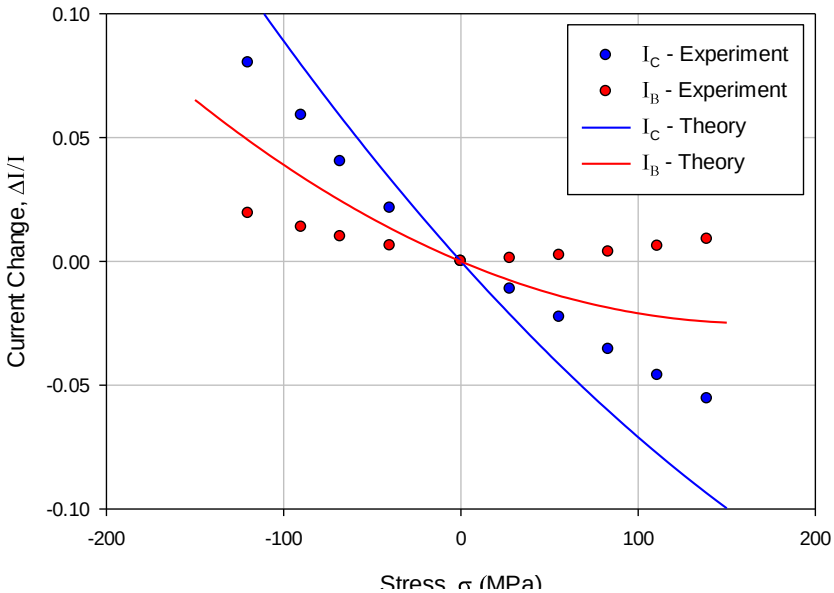


Figure 6.15 Comparison of npn Currents with Theory

Fig. 6.15 compares our experimental data with theoretical results for npn collector and base current. The solid line in Fig. 6.15 corresponds to the combination of the theoretical results in Fig. 6.10 and Table 6.6, and the data points are the experimentally

obtained values. As the theory predicts, the npn transistor base current should match with the changes of intrinsic carrier concentration as in Fig. 6.10, and adding a linear piezoresistive term to the base current change should give the change in collector current. But Fig. 6.15 shows that the experimental data and the theoretical predictions are not quite matching. However for the base current of the npn, the same numerical results of the change in intrinsic carrier concentration with stress provide an excellent fit to the data, when the curve is shifted to account for a built-in stress in the emitter of 150 MPa. The procedure to obtain the built-in stress is discussed in the following,

The change in intrinsic carrier concentration from Creemer can be expressed as:

$$\left.\frac{\Delta I_B}{I_B}\right|_{Theory} = \frac{\Delta n_{iE}^2}{n_{iE}^2} = A\sigma^2 + B\sigma \tag{6.20}$$

This change in intrinsic carrier concentration in Eq. (6.20) should match with the change in base current in npn transistor in absence of any built-in stress in the emitter. However, presence on any built-n stress will cause the change in intrinsic carrier concentration in Eq. (6.20) to shift by

$$\left.\frac{\Delta I_B}{I_B}\right|_{Theory} = A(\sigma^2 - \sigma_S^2) + B(\sigma - \sigma_S) \tag{6.21}$$

where σ_S is the built-in stress. Now to find out the required shift of the theoretical plot to match with the experimental data, least square method was applied. The required shift minimizes the least square error between the data points and theory as shown in Eq. 6.22.

$$\sum_{i=1}^{n}\left[\left(A(\sigma_i{}^2 - \sigma_S^2) + B(\sigma_i - \sigma_S)\right) - \left.\frac{\Delta I_B}{I_B}\right|_i\right]^2 \tag{6.22}$$

Minimizing Eq. (6.22) yields the value of the required shift σ_S of the theoretical intrinsic carrier change that needs to be incorporated to match with the experimental data.

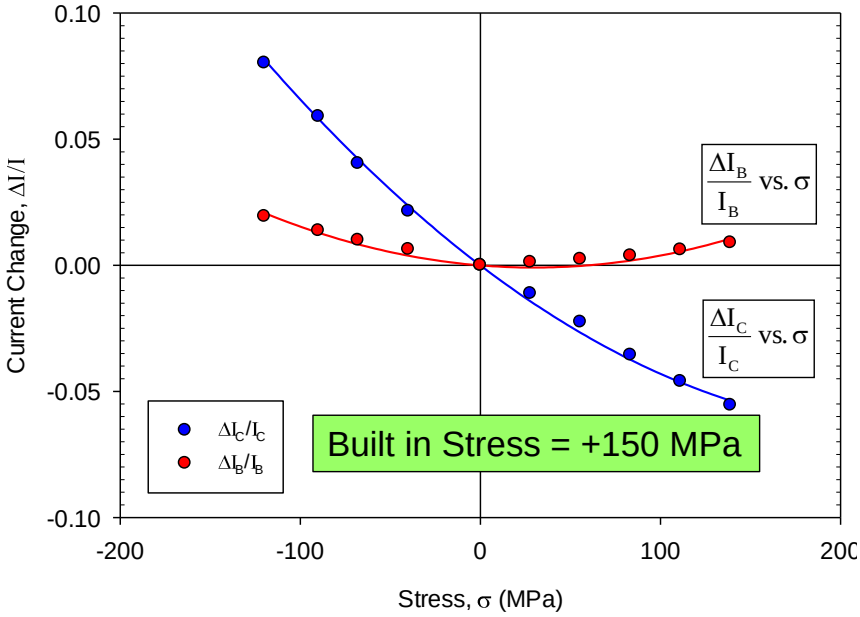


Figure 6.16 Comparison of npn Currents with Theory

A Matlab code was written to find out the required shift in the theoretical plot to match the experimental data provides the built-in stress to be 150 MPa. The correlation of the theory and experimental results with the built-in stress is presented in Fig. 6.16. The red solid line is the theoretical change in intrinsic carrier concentration with the built-in stress shift, whereas the blue line utilizes the same data as the pnp collector current along with an added piezoresistive term of 200/TPa. Both collector current and base current experimental data show excellent agreement with the theoretically obtained plots. The fit of the curve is highly sensitive to the value of the shift, and we believe this measurements represent an excellent method for quantifying built-in stress due to a combination of heavy doping effects and fabrication processes such as in the shallow trench isolation, polysilicon emitter processes, etc.

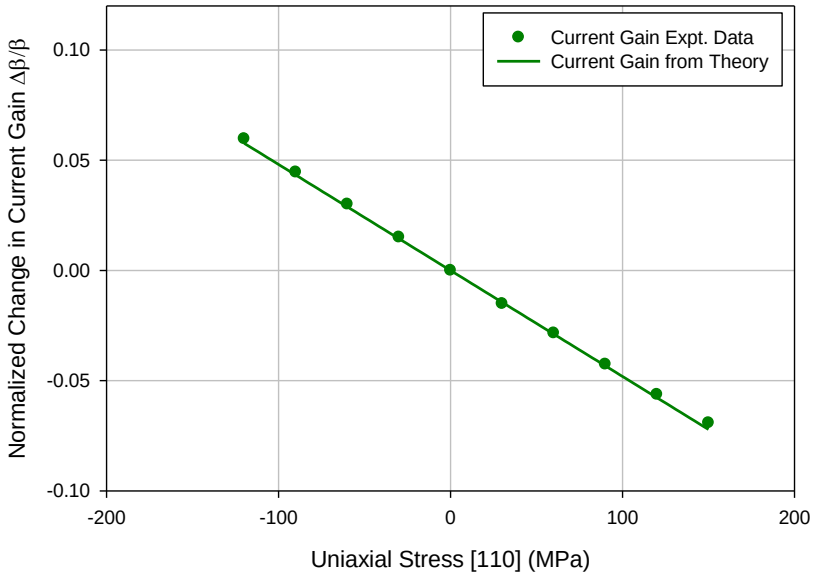


Figure 6.17 Comparison of npn Current Gain with Theory

Fig. 6.17 compares theory and experiment for the current gain of the npn transistor. The experimentally obtained current gain variation is quite linear with a small curvature. For theoretical evaluation of the current gain, the base current variation is subtracted from the collector current variations obtained from theoretical fits. This subtraction yields a strictly linear curve since both the collector current and base current variation is quadratic in nature. The yielding of a linear plot from the subtraction of the quadratic plots can be explained as shown in the following. The simplified numerical expressions for base current variation with the built-in stress and collector current can be expressed as

$$\frac{\Delta I_C}{I_C} = \frac{\Delta n_{iB}^2}{n_{iB}^2} = C_2\sigma^2 + C_1\sigma$$
$$\frac{\Delta I_B}{I_B} = \frac{\Delta n_{iE}^2}{n_{iE}^2} = C_2\left(\sigma - \sigma_S\right)^2 + C_1\left(\sigma - \sigma_S\right) \qquad (6.23)$$
$$\frac{\Delta\beta}{\beta} = \frac{\Delta I_C}{I_C} - \frac{\Delta I_B}{I_B} = \frac{\Delta n_{iB}^2}{n_{iB}^2} - \frac{\Delta n_{iE}^2}{n_{iE}^2} = 2C_2\sigma_S\sigma - \left(C_2\sigma_S^2 - C_1\sigma_S\right)$$

where σ_S is the built-in stress. Therefore from Eq. 6.23, it is evident that subtracting two equal quadratic terms will yield a straight line. As a result the variation of npn current gain is found out to show a linear trend. Any curvature in the current gain plot corresponds to a slight difference in the quadratics due to heavy doping.

6.6.3 (111) Silicon

We have limited access to devices on the (111) surface. However, we have been able to operate one of our van der Pauw structures as a vertical npn transistor.

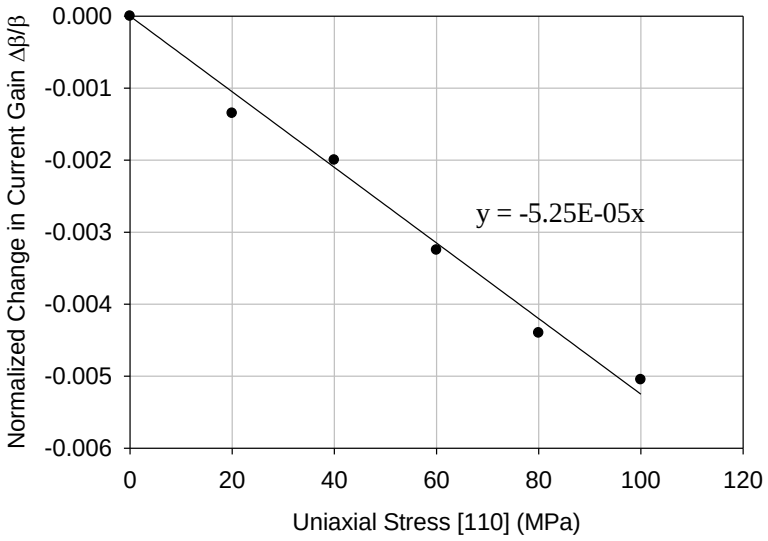


Figure 6.18 (111) Transistors Under Uniaxial Stress: npn Normal-Mode Current Gain. Straight Line Represents Least Square Fit to the Data.

The current gain fits the theory for the npn device on (111) silicon. The structure utilized has similar sheet resistances for the base and emitter diffusions and hence the intrinsic carrier concentration terms should cancel out leaving only the mobility term equal to the slope in Fig. 6.18 (-53/TPa). δ has not been determined for this device but is expected to be < 1.

(111) npn current gain theory: $\delta\left[-\frac{65}{TPa}\sigma+\left(\frac{\Delta n_{iB}^2}{n_{iB}^2}-\frac{\Delta n_{iE}^2}{n_{iE}^2}\right)\right]$ (6.25)

6.6.4 Systematic Approach to Parameter Extraction

The list below represents an extraction process that can be used to fit the theory to the data.

npn

1. Use validated theoretical result for $\frac{\Delta n_{iB}^2}{n_{iB}^2}$

2. Determine value of π_{12}^{nB} needed to fit collector current data.

3. Determine "built-in" stress necessary to fit $\frac{\Delta\beta}{\beta}$ and hence $\frac{\Delta I_B}{I_B}$

pnp

1. Use validated theoretical result for $\frac{\Delta n_{iB}^2}{n_{iB}^2}$

2. Determine value of π_{12}^{pB} and "built-in" stress needed to fit current gain and base current data.

6.7 Conclusions

We have demonstrated that classic one-dimensional bipolar junction transistor adequately models the stress dependent behavior of BJTs and provided a systematic approach to extraction of the necessary stress dependent parameters in the model for npn and pnp transistors. Collector current and base current variations are dominated by

intrinsic carrier concentration variations, whereas current gain tends to be nearly linear with a small quadratic term. It has been shown that Early voltage variations can be neglected.

Theoretical results for variations of intrinsic carrier concentration under stress provide excellent fits to data related to base transport, whereas those for heavily doped emitters require the assumption of a built-in stress. In fact, measurements versus applied uniaxial stress appear to provide a highly sensitive means of measuring the built-in stress in the emitter since the moderately doped base regions show no indication of built-in stress. Stress measurements also indicate an apparent change in the deformation potentials in heavily doped silicon.

CHAPTER 7

MECHANICAL STRESS EFFECTS ON BIPOLAR ANALOG CIRCUITS

7.1 Introduction

In this chapter, the impact of mechanical stress on several bipolar basic analog IC building blocks is demonstrated and discussed. In previous chapters, the focus was on how the device parameters of bipolar transistors change due to mechanical stress and the development of theoretical formulation by incorporating the stress induced changes in device characteristics based on the experimentally obtained data. The understanding of the stress induced device parameter modulations of individual npn and pnp transistors can be utilized to predict the changes in the circuit output containing these transistors.

This chapter deals with the experimental investigation of the impact of stress on few basic bipolar analog circuits such as PTAT (Proportional-to-Absolute-Temperature) voltage generators, offset voltage of differential pairs and current mirrors. Stress response of these circuits are presented in this chapter and furthermore correlation of the stress dependent transistor models with the measurements of these circuits are established.

7.2 Stress Induced Changes in Circuit Output

The basic building block of bipolar ICs usually consist of resistors, standard npn and pnp transistors, substrate pnp's and diodes (diode connected transistors). The performance of the circuits is affected due to the stress induced parametric shifts of the

circuit elements due to the piezo effects experienced by these elements.

In this section, experimental study of the changes in some basic bipolar analog circuit outputs are reported due to application of mechanical stress. These basic circuits were constructed by connecting adjacent npn or pnp transistors situated on the (100) silicon wafer strips as shown in Fig. 7.1. A total of 15 different npn and pnp transistors with various transistor area sizes were present in the (100) wafer strip. Uniaxial normal stress was then applied along the $[\bar{1}10]$ direction to the silicon strips cut from the processed wafers containing the bipolar circuits using a four point bending loading fixture as shown in Fig. 7.2. The same method was used to apply the uniaxial stress on the circuits as that was used for individual npn and pnp transistors on wafer strips as explained in Chapter 5. In the following subsections the stress induced changes PTAT voltage generators, differential pair offset voltages and the mirror ratio of current mirrors are explored and discussed.

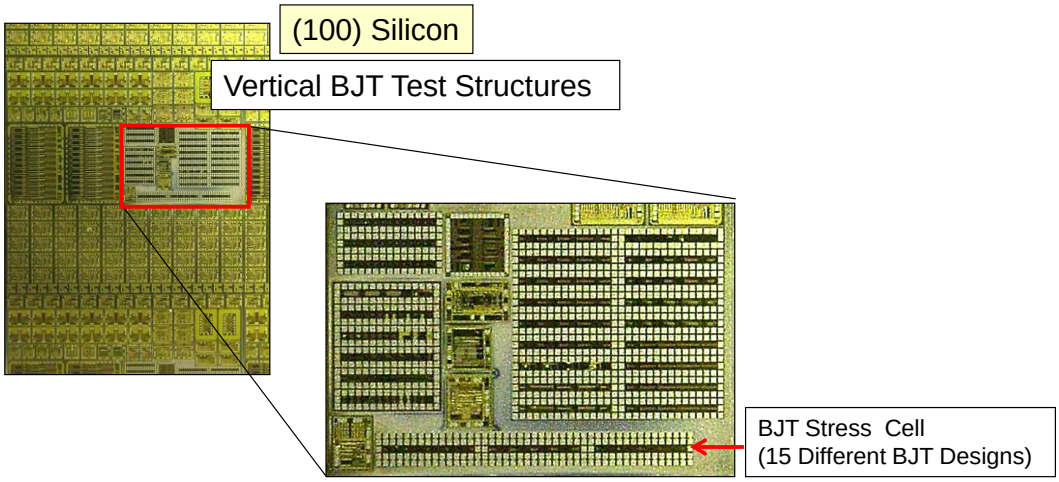


Figure 7.1 Bipolar Transistor Wafer Strip on (100) Silicon

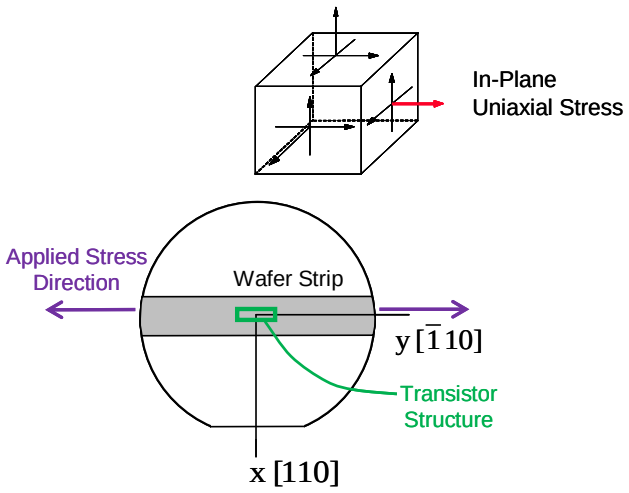


Figure 7.2 Application of Uniaxial Stress to Bipolar Circuits

7.2.1 Stress Response of the Offset Voltage of Differential Pairs

One of the most common and important circuits in bipolar ICs is an npn or pnp differential pair. Fig. 7.3 shows a simple npn differential pair. Q_1 and Q_2 are two npn transistors with the best matching of V_{BE} where the collectors of both the devices are connected together so that the collector-emitter voltages are equal. The base of Q_1 is connected to a voltage supply whereas the base of the Q_2 is grounded. The emitters of $Q_1$and Q_2 share a commonconnection through which current is pulled out of the circuit as shown in Fig. 7.3.

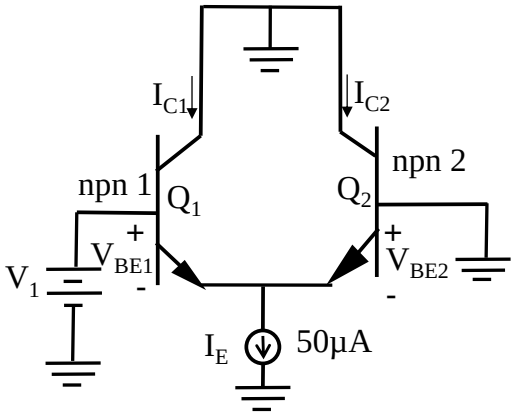


Figure 7.3 npn Differential Pair

Considering the npn differential pair,also referred to as emitter-coupled pair, as shown in Fig. 7.3, from Kirchhoff's voltage law for the input loop, it can be written:

$$V_1 - V_{BE1} + V_{BE2} = 0 \qquad (7.1)$$

For the bipolar transistor, the collector current $I_C$is related to the base-emitter voltage V_{BE} in forward bias region as shown in Eq. (7.2).

$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right) \qquad (7.2)$$

where I_S saturation current and V_T is the thermal voltage. Therefore for both npn transistors it can be written as,

$$I_{C1} = I_{S1} \exp\left(\frac{V_{BE1}}{V_T}\right) \qquad (7.3)$$

and

$$I_{C2} = I_{S2} \exp\left(\frac{V_{BE2}}{V_T}\right) \qquad (7.4)$$

Offset voltage is defined as the voltage required to set I_{C2}= I_{C1} in the circuit in Fig 7.3. Setting I_{C1} = I_{C2} yields:

$$\frac{I_{S1}}{I_{S2}} = \exp\left(\frac{V_{BE2} - V_{BE1}}{V_T}\right)$$

which becomes (7.5)

$$V_{OS} = V_T \ln \frac{I_{S1}}{I_{S2}}$$

where V_{OS} = V_{BE1}-V_{BE2}, which is the offset voltage between two transistors.

Application of uniaxial stress will cause the saturation currents of the transistors to change which can be incorporated in Eq. 7.5 as shown in Eq. 7.6, where I_{S1}° and I_{S2}° represent the unstressed values of the saturation currents.

$$V_{OS} = V_T \ln \frac{I_{S1}^{\circ}\left(1+\pi\sigma+\frac{\Delta n_{iB}^2(\sigma)}{n_{iB}^2}\right)}{I_{S2}^{\circ}\left(1+\pi\sigma+\frac{\Delta n_{iB}^2(\sigma)}{n_{iB}^2}\right)} \tag{7.6}$$

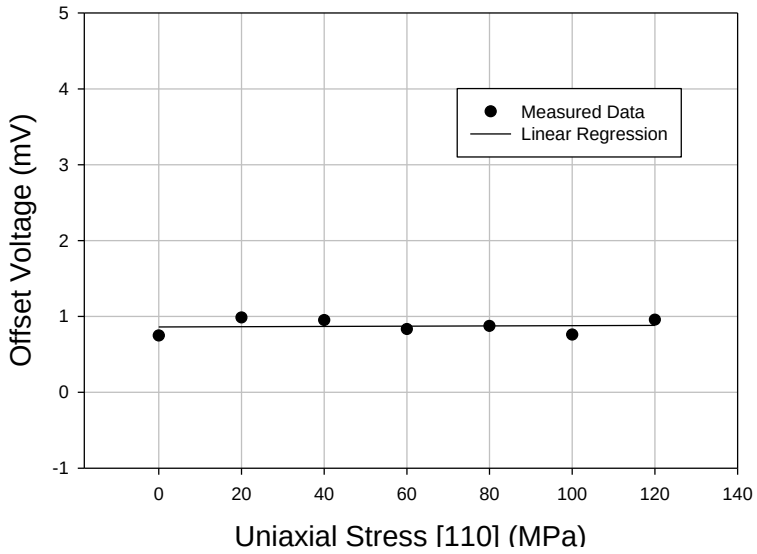


Figure 7.4 Offset Voltage vs. Stress Plot of an npn Differential Pair

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Experimental data obtained from the application of uniaxial stress on the npn differential pair yields the result shown in Fig. 7.4. The experimental data was obtained by biasing the differential pair with a current of 50 µA. The offset voltage is found by sweeping voltage V_1 to find value required to set $I_{C2}= I_{C1}$.. The plot shows that there is no variation of the offset voltage of the differential pair due to stress. This result can be explained through the theoretical equation stated in Eq. 7.6. If stress applied to this circuit is maintained as a common-mode effect, V_{OS} will be independent of stress. Since the

stress was applied along $[\bar{1}10]$ direction and current flow through both the transistors in the circuit are perpendicular to the direction of stress, the saturation currents in both the transistor should be affected by stress in similar way, hence no significant change in the offset voltage of the circuit should occur.

7.2.2 Stress Response of PTAT Circuit

In this section, the uniaxial stress effect on a PTAT circuit is discussed. Fig. 7.4 shows a typical configuration of a PTAT circuit. The two transistors in a PTAT circuits are operated at different current densities, which effectively produces a voltage difference between two transistors (an offset voltage). The difference in voltage is proportional to absolute temperature (PTAT) and depends on the emitter area ratio and the collector currents of the devices

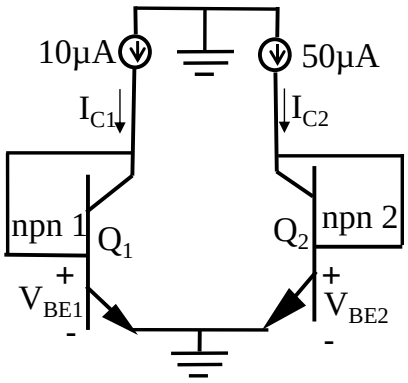

Figure 7.5 PTAT Circuit

The expression for PTAT voltage can be written following the same procedure explained in previous section. Similar expression can be written for PTAT circuit as in Eq. 7.5 for perfectly matched npn transistors,

$$V_{PTAT} = V_{BE1} - V_{BE1} = V_T \ln \frac{I_{C2}}{I_{C1}} \frac{I_{S1}}{I_{S2}} \tag{7.7}$$

Introduction of stress induced changes in Eq. 7.7, we can write

$$V_{PTAT} = V_T \ln \frac{I_{C2}}{I_{C1}} \frac{I_{S1}^{\circ}\left(1+\pi\sigma+\frac{\Delta n_{iB}^2(\sigma)}{n_{iB}^2}\right)}{I_{S2}^{\circ}\left(1+\pi\sigma+\frac{\Delta n_{iB}^2(\sigma)}{n_{iB}^2}\right)} \tag{7.8}$$

Since the stress state is the same in both transistors, the change in saturation current for the transistors should be same, as in the npn differential pair. Therefore for For $I_1 = 5I_2$ with $I_{S1}^{\circ} = I_{S2}^{\circ}$ and $\sigma_1 \approx \sigma_2, V_{PTAT} = V_T \ln(5) = 0.0259V(1.609) = 41.7$ mV .The theoretical evaluation shows that the PTAT output voltage should not change with stress and if the collector current ratio between both the transistors is 1:5 then V_{PTAT} should be 41.7 mV.

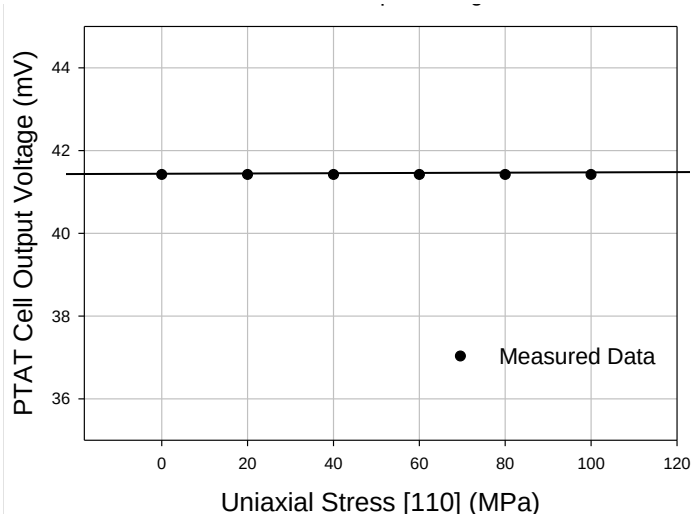

Figure 7.6 PTAT Output Voltage vs. Uniaxial Stress

To obtain a correlation between theory and experiments, we have performed experimental measurements on a PTAT circuit as shown in Fig. 7.4 by applying uniaxial stress. Transistor Q_1 was supplied with a collector current of 10 µA current whereas Q_2 was supplied with a current of 50 µA. The resultant plot is shown in Fig. 7.5. The

experimental data shows that PTAT output voltage is around 41.5 mV and that the PTAT voltage does not change with stress which agrees with what theory has predicted.

7.2.3 Stress Response of Current Mirror

The current mirror is another important building block of bipolar integrated circuits that we have investigated in this chapter. A current mirror is a current source that provides fixed bias current and/or active loads to other analog circuits. The devices in the ideal current mirror should be identical so the output current of the circuit (I_O) replicates the collector current (I_{C1}) of Q_1.

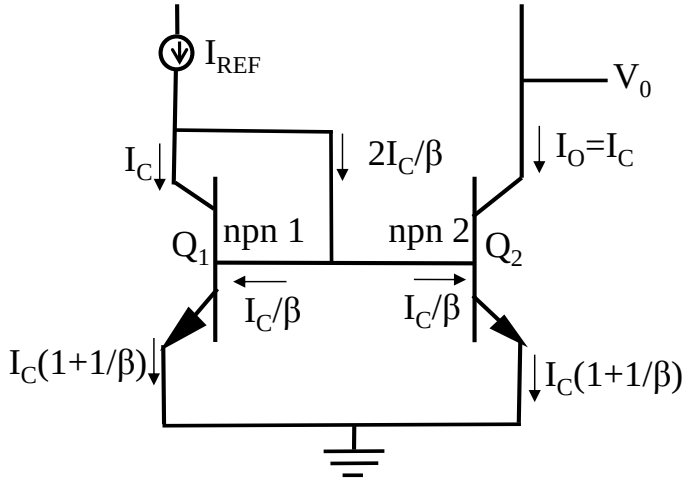

Figure 7.7 Current Mirror Circuit

The basic bipolar current mirror\ shown in Fig. 7.5 consists of two npn identical transistors Q_1 and Q_2 whose bases are connected and the base and collector of Q_1 transistor is joined to provide a negative feedback. If the two transistors Q_1 and $Q_2$are properly matched, then mirror circuit output current I_O will be same as the collector current of Q_1.

Applying Kirchhoff's current law at node Q_1,

$$I_{REF} = I_C + 2I_B = I_C\left(1+\frac{2}{\beta}\right) \tag{7.9}$$

where β is the current gain of the transistors in which both Q_1 and Q_2 are matched perfectly. If the emitter area of both the transistors are not same, i.e.; $I_{S1}^{\circ} = mI_{S2}^{\circ}$ then Eq. 7.9 can be written as:

$$I_{REF} = I_C\frac{\left(1+\frac{(m+1)}{\beta}\right)}{m} \tag{7.10}$$

In a current mirror, the output current follows the collector current of Q_1 transistor, i.e.; $I_C = I_O$, hence,

$$\frac{I_O}{I_{REF}} = \frac{m}{\left(1+\frac{(m+1)}{\beta}\right)} \tag{7.11}$$

Due to mechanical stress, there will be changes in the output current of the current mirror circuit due to the changes in current gain of the device as evident from Eq. 7.11. Incorporating the stress induced changes in the current gain in Eq. 7.11, the change in output current of the current mirror circuit due to stress can be written as,

$$\frac{\Delta I_O}{I_O} = \frac{\Delta\beta}{\beta_0} - \frac{\Delta\beta}{\beta_0+(m+1)} \tag{7.12}$$

where β_0 is the stress free current gain. Substituting $\frac{\Delta\beta}{\beta} = \pi\sigma + \left(\frac{\Delta n_{iB}^2(\sigma)}{n_{iB}^2} - \frac{\Delta n_{iE}^2(\sigma)}{n_{iE}^2}\right)$, m = 3 and using appropriate values for the piezoresistance coefficient π and the intrinsic carrier concentration, n_i in Eq. 7.12, Fig 7.6 can be obtained. From the plot it is evident that for a 30 μA of output current in stress free case, an application of 100 MPa stress will

cause the output current of the circuit to change approximately 23 nA. This change in output current will affect the performance of the current mirror circuit that is usually used in analog IC to provide a fixed bias current or load to other circuits. Note that changes in the saturation currents cancel out just as in the previous two circuits, as long as the stress is the same in both transistors.

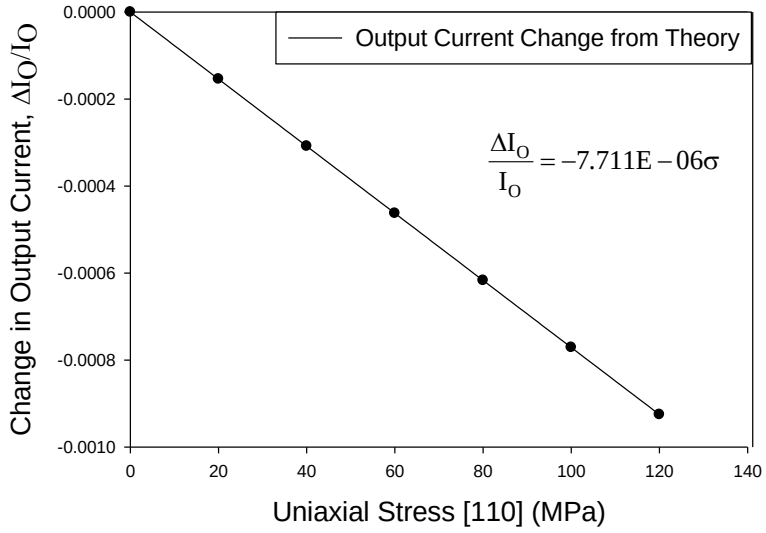

Figure 7.8 Output Current Change Vs. Stress of Current Mirror Circuit (Theory)

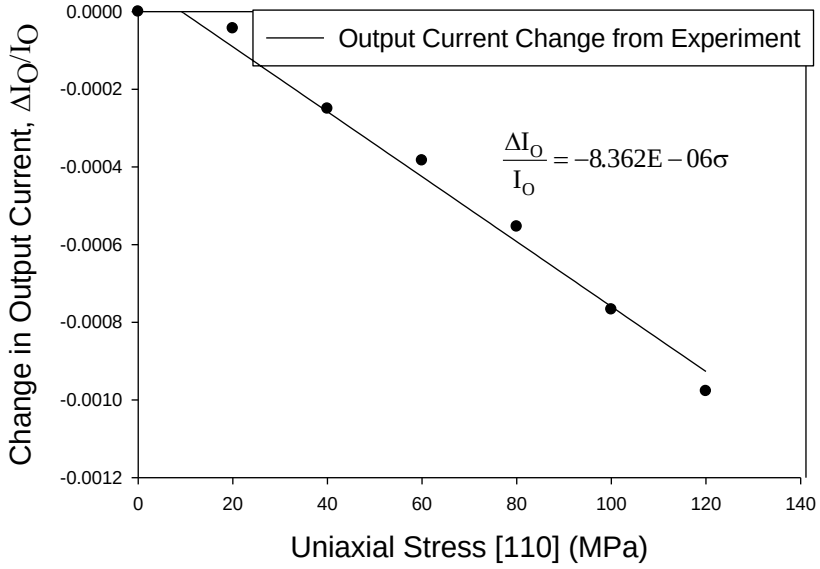

Figure 7.9 Output Current Change vs. Stress of Current Mirror Circuit (Experiment)

For experimental investigation of the uniaxial stress effect on an npn current mirror circuit, the circuit configuration shown in Fig. 7.5 was assembled in a wafer strip and an uniaxial stress of 0 to 120 MPa was applied. The emitter area ratio m between two npn transistors in the circuit was 3 and the input current I_{REF} was set to 10 µA, which resulted in an output current of approximately 30 µA. The plot of the experimentally obtained data is shown in Fig. 7.7. The theoretically result in Fig. 7.8 shows excellent agreement with the experimentally obtained data presented in Fig. 7.9.

7.3 Conclusion

In this chapter, the impact of uniaxial stress on several basic analog circuits are investigated. The stress dependent transistor models are correlated with the experimentally obtained stress response of the circuits to demonstrate the impact of stress on basic analog IC building blocks.Measurements agree well with the theoretical model for PTAT voltage generators, the offset voltage of differential pairs and the mirror ratio of current mirrors. Therefore, the theoretical model can be effectively implemented to obtain the impact of stress on bipolar analog circuits.

CHAPTER 8

CONCLUSIONS

In this thesis, the effect of mechanical stresses in several electronic devices have been explored and discussed. The stress sensor aspect of some devices such as resistors and field effect transistors, are discussed and research related to that topic is addressed. For bipolar junction transistor the stress induced changes in the electrical characteristics are characterized experimentally and a related theoretical work has also been discussed in this thesis to address the stress related shifts in bipolar transistors.

In Chapter 1, an overview of the sources of mechanical stress generation due to the fabrication, processing and packaging of the integrated circuit chips are discussed in detail. The thermal expansion coefficient mismatch and the mechanical property mismatch between the materials used in IC processing are the causes of stress generation. Stress can also be generated due to the intrinsic stress on the deposited film, thermal oxidation of silicon and, lattice mismatch between different implanting material in silicon etc. The scaling down of the devices and increase in circuit density are causing more complicated stress patterns in IC chips. The impact of stress on silicon chip is also presented in Chapter 1.

The stresses and strain in the integrated circuit chips cause parametric shifts in the electrical performance of the electrical devices in the circuit and affects their output

performance. The reason behind these parametric shifts are attributed to the piezoressistance and piezojunction effects of semiconductor devices. Silicon being a cubic crystal, the stress and strain causes the crystal symmetry of the silicon to alter and that causes the electrical characteristics such as the resistivity or the saturation current of the devices to change. The piezoresistance effect causes alterations of the resistivity of the resistors and field effect transistors and this effect is due to the changes in majority carrier mobility. This effect is extensively studied by various researchers and the physics behind the changes in mobility of the carriers due to the changes in the band structure of the silicon is very well understood. The piezojunction effect is attributed to the variations in saturation current of p-n junctions and bipolar transistors and the variation in minority carrier mobility and the changes in the intrinsic carrier concentration causes this effect since this devices operate due to the conduction of minority carriers. There are few researchers who studied this effect in details. The literature review on piezoresistive effect and piezojunction effect is discussed in Chapter 2.

Chapter 3 focuses on the piezoresistive effect of multi element resistor stress sensor rosettes capable of measuring die stresses in packaged electronic modules. The piezoresistive theory for resistor sensors are fully developed and a review of that theory is presented in Appendix A. The piezoresistive theory for various rosette design in various silicon wafer surface is also discussed in Chapter 3. To extract stress distribution on a silicon die, the change in resistance values of the resistor elements, piezoresistance coefficients and the change in temperatures are needed to be known. For stress characterization, the parameters required are obtained from experimental data. There can be uncertainties in acquiring these parameters due to the errors made during the

experiments and due to these uncertainties in measured values there can be significant errors in the extracted stress values. To determine the effect of these uncertainties in the extracted stress values, a sensitivity of the stresses to these parameters are explored. For that reason, the stress distribution over the die of a flip chip package is obtained from finite element analysis and using those stresses the sensitivity analysis is performed. The results show that the sensitivities are stress dependent and that temperature compensated measurements should be performed because they are associated with low sensitivities.

Chapter 4 deals with the piezoresitive effect on field effect transistors (FETs) and the operation of this device as a potential stress sensor. The smaller geometrical size of the device and also its lighter doing of the resistive channel makes it advantageous over the resistor sensors. In this chapter the dependence of the piezoresistive coefficients on the operating point of the device is discussed. The calibration of the piezoresistance coefficients are performed by applying uniaxial stress. The piezoresistance coefficients are expressed as a function of drain current to demonstrate its dependence to operating point. Piezoresistance coefficients corresponding to the PMOS devices exhibit linear dependence on the drain current whereas for NMOS devices shows a nonlinear trend. The piezoresistance coefficients are also expressed as a function of carrier mobility in the channel region. At low currents high sensitivity can be obtained but at subthreshold region the FET temperature coefficients become very large. As a future work on this topic, an extraction of the piezoresistance coefficients in the subthreshold region will be attempted.

In Chapter 5 and 6 the piezojunction effect on bipolar junction transistors (BJTs) are explored. The objective of this work is to characterize the effect of mechanical stress

on these devices and then develop a theoretical model based on the experimental data to obtain an understanding of the influence of stress on precision analog devices/circuits. To experimentally characterize, both npn and pnp bipolar transistors fabricated on (100) and (111) silicon wafers were utilized. Uniaxial stress was applied on the wafer strips containing these devices to obtain changes in device parameters due to uniaxial stress. In Chapter 5, the mechanical setup used for the experiments is discussed. Different electrical measurement techniques that were used to the electrically characterize these devices are also presented and advantages and limitations of each measurement techniques are discussed as well. The experimentally obtained changes in the current gain, collector and base current due to the application of uniaxial stress are shown in Chapter 5.

In Chapter 6, a theoretical model is developed to predict the stress induced changes in the electrical parameters of a bipolar junction transistor. The experimental data that is presented in Chapter 5 acted as a guide to develop this model. Our theory is based on basic charge-control model for the transistor and using that charge control model we obtained expressions for changes current gain, collector current and base current due to mechanical stress. The expressions for stress induced changes in electrical parameters indicated that the variations are due to change in minority carrier mobility and also the change in intrinsic carrier concentration of the device. These expressions helped us towards developing an understanding of the dominant effects of stress on the basic BJT model parameters. The validity of the model was verified by correlating it with the experimentally obtained data. The modeling steps to have a good correlation is presented step by step in this chapter. The correlations show few inconsistencies which can be attributed due to the bandgap narrowing due to heavy doping in the emitter and also due

to variation in bandgap due variation to stress. The overall comparison yielded a good correlation. The developed formulations can be applied to theoretically optimize transistor design, placement, orientation and processing to both maximize and minimize the impact of induced die stresses to utilize these devices either as stress sensors or to incorporate them in stress insensitive precision analog circuits respectively.

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APPENDIX A

PIEZORESISTANCE IN RESISTORS AND FIELD EFFECT TRANSISTORS

A.1 Introduction

In this chapter, the piezoresistivity theory is discussed that govern resistor and field effect transistor sensors. The piezoresistivity theory is derived to correlate the effect with the stress induced changes in the resistance of the resistors and the changes in drain current in case of field effect transistors. The theory describes the relation between resistor or FET sensor response and applied stress.

A.2 Piezoresistive Theory for Silicon

Piezoresistance is a phenomena which modulates the electrical resistance of the material by mechanical stress acted on the material. The conduction mechanism on the semiconductor material is altered due to the stress and that is the origin of the piezoresistance effect. In this chapter, the piezoresistance theory of optimized resistor sensor on (100) and (111) silicon is presented and based on that the piezoresistance theory of metal–oxide–semiconductor (MOS) devices on the (100) silicon is discussed.

The stress induced change in resistance is a function of resistivity and geometrical changes. The electrical resistance of a material can be expressed as [A2]:

$$R = \frac{\rho L}{A} \tag{A.1}$$

In (A.1) ρ is the resistivity, L is the length and A is the average cross-sectional area. The normalized change is resistance of a material due to small fractional changes in stress can be defined by

$$\frac{\Delta R}{R} = \frac{\Delta \rho}{\rho} + \frac{\Delta L}{L} - \frac{\Delta A}{A} \cong \frac{\Delta \rho}{\rho} \tag{A.2}$$

For resistors made of metal the change in geometrical dimensions in L and A are main reason for the change in resistance of the material with stress whereas for semiconductor resistors, the resistivity change is the dominant effect for the stress induced changes with only a very small percent change is attributed to the change in dimensions. The strain induced change in dimensions is negligible compared to the resistivity change of the semiconductor material based on the fact that the resistance change due to stress is large and also semiconductor materials have high elastic modulus.

The conductivity of a semiconductor material is a function of the carrier concentrations, n and p, and carrier mobilities μ_n and μ_p.

$$\sigma = q\left(n\mu_n + p\mu_p\right) \tag{A.3}$$

where q is the electric charge. For silicon those are doped either n type or p type, the majority carriers are either electrons or holes. For example, for n type silicon the majority carrier is electron and the concentration of electron is much higher that the concentration of holes which is the minority carrier. So for n type silicon the minority carrier can be neglected and the conductivity equation can be written as

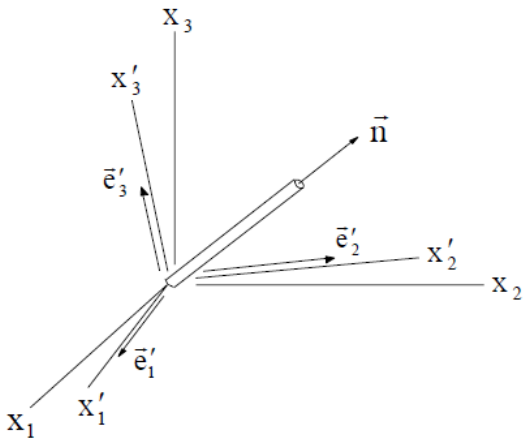
$$\sigma = q\, n\, \mu_n \tag{A.4}$$

Now the resistivity of the material is inversely proportional to the conductivity, hence based on Eq. (A.4) the normalized change in resistivity of the resistivity of the material can be expressed as

$$\frac{\Delta\rho}{\rho} = -\frac{\Delta\sigma}{\sigma} = -\frac{\Delta\mu}{\mu} \tag{A.5}$$

Therefore the stress induced change in resistance of a semiconductor material can be written in terms of the change in the mobility of the carrier.

$$\frac{\Delta R}{R} = -\frac{\Delta\mu}{\mu} \tag{A.6}$$



FigureA.1 Arbitrarily Oriented Silicon Filamentary Conductor

A.3 Piezoresistive Theory for Resistors

Silicon being an anisotropic material, the piezoresistance in silicon is also anisotropic and depends on the wafer surface in which the resistor it is fabricated and also the resistor direction on the surface.

A filamentary conductor as shown in Fig: A.1 is oriented arbitrarily with reference to the unprimed axes x_1 = [100], x_2 = [010] and x_3 = [001] that represents the

principal crystallographic directions of the cubic silicon crystal. The primed coordinate system is at arbitrary angle with the unprimed coordinate system. For this filament in Fig. A.1, the normalized change in resistance can be expressed in terms of the primed components using [A1] [A2]:

$$\begin{aligned}\frac{\Delta R}{R} &= (\pi'_{1\alpha}\sigma'_{\alpha})l'^{2} + (\pi'_{2\alpha}\sigma'_{\alpha})m'^{2} + (\pi'_{3\alpha}\sigma'_{\alpha})n'^{2} \\ &+ 2(\pi'_{4\alpha}\sigma'_{\alpha})l'n' + 2(\pi'_{5\alpha}\sigma'_{\alpha})m'n' + 2(\pi'_{6\alpha}\sigma'_{\alpha})l'm' \\ &+ [\alpha_1\Delta T + \alpha_2(\Delta T)^2 + \ldots]\end{aligned} \qquad \text{(A.7)}$$

where l', m' and n' are the direction cosines of the conductor orientation with respect to the primed axes x'_1, x'_2 and x'_3. $\pi'_{\alpha\beta}$ (α,β = 1,2,….6) are thetemperature dependent piezoresistance components along the off-axes, α_1 and α_2 are the temperature coefficients of resistance and ΔT is the difference between the reference and measurement temperature. If the principal coorodinate system [100], [010] and [001] is considered as the reference axes, the cubic symmetry reduces the total number of unique piezoresistance components from thirty six to three π_{11}, $\pi_{12}$and π_{44}using the transformation

$$\pi'_{\alpha\beta} = T_{\alpha\gamma}\pi_{\lambda\delta}T_{\delta\beta} \qquad \text{(A.8)}$$

where

$$[\pi_{ij}] = \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{bmatrix} \qquad \text{(A.9)}$$

and the transformation matrix has the form

$$[T_{\alpha\beta}]=\begin{bmatrix} l_1^2 & m_1^2 & n_1^2 & 2l_1n_1 & 2m_1n_1 & 2l_1m_1 \\ l_2^2 & m_2^2 & n_2^2 & 2l_2n_2 & 2m_2n_2 & 2l_2m_2 \\ l_3^2 & m_3^2 & n_3^2 & 2l_3n_3 & 2m_3n_3 & 2l_3m_3 \\ l_1l_3 & m_1m_3 & n_1n_3 & l_1n_3+l_3n_1 & m_1n_3+m_3n_1 & l_1m_3+l_3m_1 \\ l_2l_3 & m_2m_3 & n_2n_3 & l_2n_3+l_3n_2 & m_2n_3+m_3n_2 & l_2m_3+l_3m_2 \\ l_1l_2 & m_1m_2 & n_1n_2 & l_1n_2+l_2n_1 & m_1n_2+m_2n_1 & l_1m_2+l_2m_1 \end{bmatrix} \quad \text{(A.10)}$$

where l, m, n are the direction cosines of the primed coordinate system with respect to the unprimed coordinate system and are given by

$$[a_{ij}]=\begin{bmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{bmatrix}=\begin{bmatrix} l_1 & m_1 & n_1 \\ l_2 & m_2 & n_2 \\ l_3 & m_3 & n_3 \end{bmatrix} \quad \text{(A.11)}$$

The transformation matrix is reduced to 6 × 6 identity matrix when the unprimed axes coincides with the primed axes. Thus Eq. (A.7) then becomes

$$\begin{aligned} \frac{\Delta R}{R} &= [\pi_{11}\sigma_{11}+\pi_{12}(\sigma_{22}+\sigma_{33})]l^2+[\pi_{11}\sigma_{22}+\pi_{12}(\sigma_{11}+\sigma_{33})]m^2 \\ &+[\pi_{11}\sigma_{33}+\pi_{12}(\sigma_{11}+\sigma_{22})]n^2+2\pi_{44}[\sigma_{12}lm+\sigma_{13}nl+\sigma_{23}mn \\ &+[\alpha_1\Delta T+\alpha_2(\Delta T)^2+\ldots] \end{aligned} \quad \text{(A.12)}$$

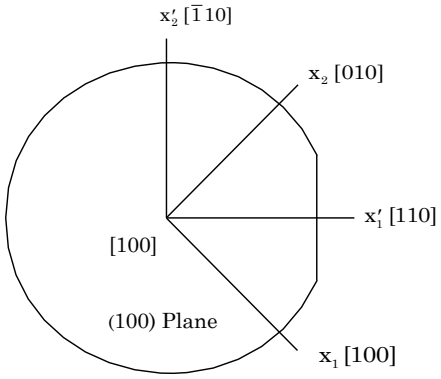
Thus stress induced resistance change in an arbitrarily oriented silicon resistor is a function of all six stress components, three unique piezoresistive coefficients and temperature difference. By fabricating the resistor sensors in certain silicon wafer planes that allows to take the advantage of the property of that wafer plane and as a result certain stress components can be extracted from the resistance change measurements due to stress.

A.4 Piezoresistance Equations for Silicon Wafer Planes

For an arbitrarily oriented resistor, Eq. (A.7) can be used to determine the change in resistance for any wafer plane. In the current microelectronics industry, the commonly

used silicon wafer plane is (100) as depicted in Fig. A.2. We will discuss the resistance change equations of resistors on (100) as well as on (111) wafer planes since the later provides the advantage of extracting all six stress components by using optimized sensor rosettes on that wafer surface [A1] [A2].

(100) Silicon



FigureA.2 (100) Silicon Wafer

Fig. A.2 shows the orientation of the principal (unprimed) and primed coordinate system on (100) silicon wafer. Since it is a (100) silicon wafer so the direction perpendicular to the surface is [001] direction. The [110] and [$\bar{1}$10] directions are the unprimed axes which are at an angle 45° with the principal crystallographic axes and are along and perpendicular to the primary flat of the wafer respectively.

In Fig. A.2, the direction cosines between the primed and the unprimed axes can be obtained from Eq. (A.11)

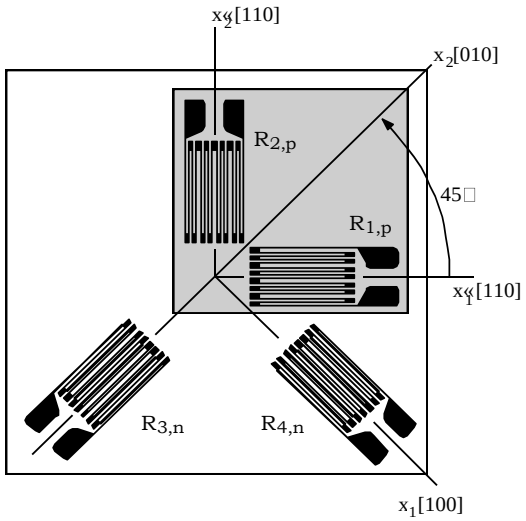
$$[a_{ij}]=\begin{bmatrix} l_1 & m_1 & n_1 \\ l_2 & m_2 & n_2 \\ l_3 & m_3 & n_3 \end{bmatrix}=\begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & 0 \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & 0 \\ 0 & 0 & 1 \end{bmatrix} \qquad \text{(A.13)}$$

Using theses direction cosines, the off-axis piezoresistive coefficients are calculated using Eq. (A.8) and substituting that to Eq. (A.7) gives

$$\begin{aligned}\frac{\Delta R}{R} &= \frac{R(\sigma,\Delta T)-R(0,0)}{R(0,0)} \\ &= \left[\left(\frac{\pi_{11}+\pi_{12}+\pi_{44}}{2}\right)\sigma'_{11}+\left(\frac{\pi_{11}+\pi_{12}-\pi_{44}}{2}\right)\sigma'_{22}\right]\cos^2\phi + \\ &\quad \left[\left(\frac{\pi_{11}+\pi_{12}-\pi_{44}}{2}\right)\sigma'_{11}+\left(\frac{\pi_{11}+\pi_{12}+\pi_{44}}{2}\right)\sigma'_{22}\right]\sin^2\phi \\ &\quad + \pi_{12}\sigma'_{33}+(\pi_{11}-\pi_{12})\sigma'_{12}\sin 2\phi+\alpha_1\Delta T\end{aligned} \qquad \text{(A.14)}$$

where $l' = \cos\varphi$, $m' = \sin\varphi$ and $n' = 0$ and angle ϕ represents the angle between the x'_1 - axis and the resistor orientation. From Eq. (A.14) it is evident that, due to the absence of σ'_{13} and σ'_{23}in the equation, a sensor rosette on (100) silicon can be used to measure four of the six unique components of the stress state at a point on the surface of the silicon.

A four-element dual-polarity sensor rosette on (100) is shown in Fig. A.3 that is optimized for reducing thermal errors in measurements. The rosette contains a 0-90° p-type resistor pair and a ±45° n-type resistor pair.



FigureA.3 A Four-Element Rosette for (100) Silicon

Application of Eq. (A.14) to the four resistor orientations gives the following relations between the resistance changes and the stresses at the rosette site, where $\pi_S = (\pi_{11} + \pi_{12})$and $\pi_D = (\pi_{11} - \pi_{12})$ has been introduced for expressing the equations for notational convenience,

$$\begin{aligned}
\frac{\Delta R_1}{R_1} &= \frac{\left(\pi_S^p + \pi_{44}^p\right)}{2}\sigma_{11}^{'} + \frac{\left(\pi_S^p - \pi_{44}^p\right)}{2}\sigma_{22}^{'} + \pi_{12}^p\sigma_{33}^{'} + \alpha_1^p\Delta T \\
\frac{\Delta R_2}{R_2} &= \frac{\left(\pi_S^p - \pi_{44}^p\right)}{2}\sigma_{11}^{'} + \frac{\left(\pi_S^p + \pi_{44}^p\right)}{2}\sigma_{22}^{'} + \pi_{12}^p\sigma_{33}^{'} + \alpha_1^p\Delta T \\
\frac{\Delta R_3}{R_3} &= \frac{\pi_S^n}{2}\left(\sigma_{11}^{'} + \sigma_{22}^{'}\right) + \pi_D^n\sigma_{12}^{'} + \pi_{12}^n\sigma_{33}^{'} + \alpha_1^n\Delta T \\
\frac{\Delta R_4}{R_4} &= \frac{\pi_S^n}{2}\left(\sigma_{11}^{'} + \sigma_{22}^{'}\right) - \pi_D^n\sigma_{12}^{'} + \pi_{12}^n\sigma_{33}^{'} + \alpha_1^n\Delta T
\end{aligned} \tag{A.15}$$

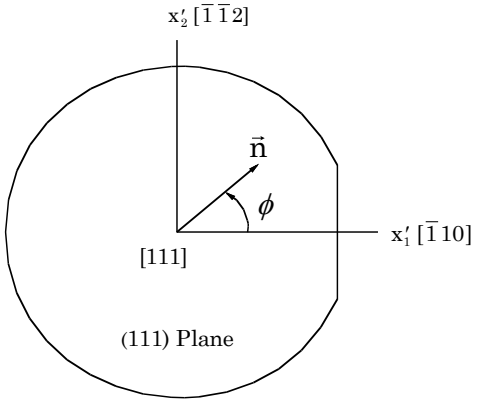
(111) Silicon

The second common silicon crystal orientation used in semiconductor fabrication is (111) material, and a general (111) silicon wafer is shown in Fig. A.4. The direction [111] is at a perpendicular direction on the (111) silicon surface. The principal crystallographic axes x_1 = [100], x_2 = [010], and x_3 = [001] does not lie on this (111) wafer surface. In Fig. A.4, the direction cosines between the primed and the crystallographic direction can be obtained from Eq. (11) similar to that for shown for (100) silicon.

$$[a_{ij}] = \begin{bmatrix} l_1 & m_1 & n_1 \\ l_2 & m_2 & n_2 \\ l_3 & m_3 & n_3 \end{bmatrix} = \begin{bmatrix} \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} & 0 \\ \frac{1}{\sqrt{6}} & \frac{1}{\sqrt{6}} & -\frac{2}{\sqrt{6}} \\ \frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} \end{bmatrix} \tag{A.16}$$

The resistance change of an arbitrarily oriented in-plane resistor on the (111) surface can be expressed in terms of the stress components resolved in this natural wafer coordinate system as described below :

$$\begin{aligned}\frac{\Delta R}{R} &= \left[B_1\sigma'_{11} + B_2\sigma'_{22} + B_3\sigma'_{33} + 2\sqrt{2}(B_2 - B_3)\sigma'_{23}\right]\cos^2\phi \\ &+ \left[B_2\sigma'_{11} + B_1\sigma'_{22} + B_3\sigma'_{33} - 2\sqrt{2}(B_2 - B_3)\sigma'_{23}\right]\sin^2\phi \\ &+ \left[2\sqrt{2}(B_2 - B_3)\sigma'_{13} + (B_1 - B_2)\sigma'_{12}\right]\sin 2\phi + \alpha_1\Delta T\end{aligned} \qquad \text{(A.17)}$$



FigureA.4 (111) Silicon Wafer

whereϕ is again the angle between the x'$_1$-axis and the resistor orientation. The B coefficients

$$B_1 = \frac{\pi_{11} + \pi_{12} + \pi_{44}}{2} \qquad B_2 = \frac{\pi_{11} + 5\pi_{12} - \pi_{44}}{6} \quad B_3 = \frac{\pi_{11} + 2\pi_{12} - \pi_{44}}{3} \qquad \text{(A.18)}$$

represent a set of linearly independent temperature dependent combined parameters that are convenient for characterization of piezoresistance on the (111) surface. From Eq. (A.17) it is evident that, a sensor rosette on (111) silicon can be used to measure all six unique components of the stress state at a point on the surface of the silicon die due to the presence of all 6 stress components in the equation.

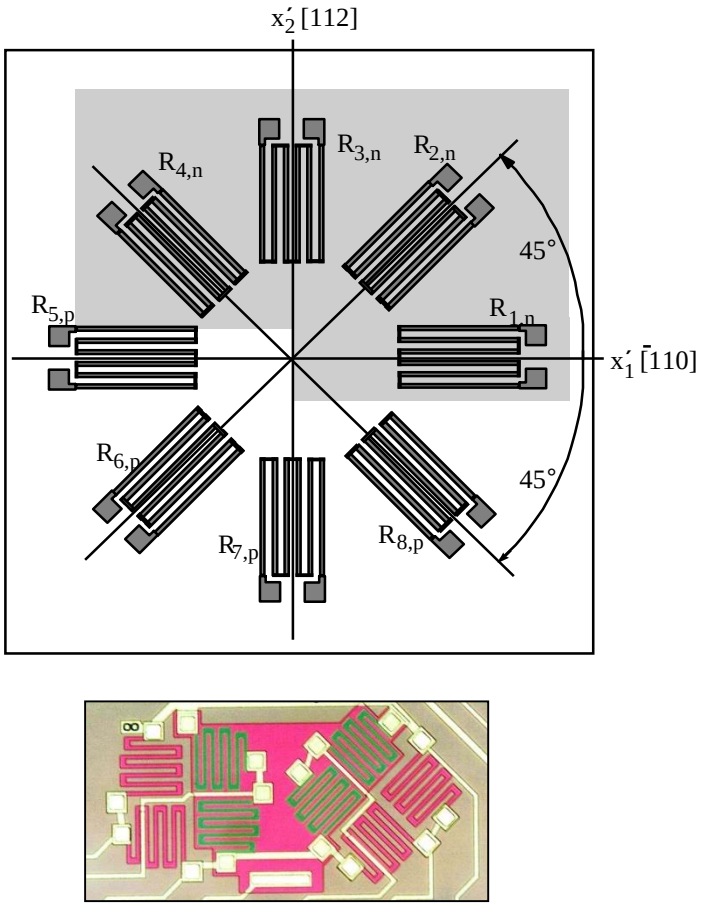


Figure A.5 Top: An Eight-Element Rosette for (1110) Silicon. Bottom: Microphotograph of an Eight-Element Complete Stress State Sensor on (111) Silicon

The eight-element dual-polarity rosette on (111) silicon illustrated in Fig. 5 contains p-type and n-type sensor sets, each with resistor elements making angles of ϕ = 0, ±45, and 90 degrees with respect to the horizontal x'1-axis. This sensor has been developed for measurement of the complete state of stress at points on the surface of a packaged semiconductor die. It has been optimized to measure four stress components in a temperature compensated manner, and the "B" coefficients can be measured using a combination of uniaxial and hydrostatic testing

Repeated application of Eq. (A.17) to each of the piezoresistive sensing elements leads to the expressions in Eq. (A.19) for the stress-induced resistance changes.

Superscripts n and p are used on the combined piezoresistive coefficients to denote n-type and p-type resistors, respectively.

$$
\begin{aligned}
\frac{\Delta R_1}{R_1} &= B_1^n \sigma'_{11} + B_2^n \sigma'_{22} + B_3^n \sigma'_{33} + 2\sqrt{2}(B_2^n - B_3^n)\sigma'_{23} + \alpha_1^n \Delta T \\
\frac{\Delta R_2}{R_2} &= \left(\frac{B_1^n + B_2^n}{2}\right)(\sigma'_{11} + \sigma'_{22}) + B_3^n \sigma'_{33} + 2\sqrt{2}(B_2^n - B_3^n)\sigma'_{13} + (B_1^n - B_2^n)\sigma'_{12} + \alpha_1^n \Delta T \\
\frac{\Delta R_3}{R_3} &= B_2^n \sigma'_{11} + B_1^n \sigma'_{22} + B_3^n \sigma'_{33} - 2\sqrt{2}(B_2^n - B_3^n)\sigma'_{23} + \alpha_1^n \Delta T \\
\frac{\Delta R_4}{R_4} &= \left(\frac{B_1^n + B_2^n}{2}\right)(\sigma'_{11} + \sigma'_{22}) + B_3^n \sigma'_{33} - 2\sqrt{2}(B_2^n - B_3^n)\sigma'_{13} - (B_1^n - B_2^n)\sigma'_{12} + \alpha_1^n \Delta T \\
\frac{\Delta R_5}{R_5} &= B_1^p \sigma_{11} + B_2^p \sigma'_{22} + B_3^p \sigma'_{33} + 2\sqrt{2}(B_2^p - B_3^p)\sigma'_{23} + \alpha_1^p \Delta T \\
\frac{\Delta R_6}{R_6} &= \left(\frac{B_1^p + B_2^p}{2}\right)(\sigma'_{11} + \sigma'_{22}) + B_3^p \sigma'_{33} + 2\sqrt{2}(B_2^p - B_3^p)\sigma'_{13} + (B_1^p - B_2^p)\sigma'_{12} + \alpha_1^p \Delta T \\
\frac{\Delta R_7}{R_7} &= B_2^p \sigma'_{11} + B_1^p \sigma'_{22} + B_3^p \sigma'_{33} - 2\sqrt{2}(B_2^p - B_3^p)\sigma'_{23} + \alpha_1^p \Delta T \\
\frac{\Delta R_8}{R_8} &= \left(\frac{B_1^p + B_2^p}{2}\right)(\sigma'_{11} + \sigma'_{22}) + B_3^p \sigma'_{33} - 2\sqrt{2}(B_2^p - B_3^p)\sigma'_{13} - (B_1^p - B_2^p)\sigma'_{12} + \alpha_1^p \Delta T
\end{aligned}
\tag{A.19}
$$

A.5 Piezoresistive Theory for Field Effect Transistors (FETs)

Fig. A.6 shows a schematic of a field effect transistor where S is the source, D is the drain and G is the gate of the transistor. It has been observed that the current in the field effect transistor is controlled by the resistive channel region when the transistor is functioned in strong inversion in either the linear or saturation regions of operation. Therefore, the application of stress can change the resistance of the channel region in strong inversion, hence can demonstrate the piezoresistive behavior similar to that of a resistor along the channel region [A3][A4][A5]. As a result of the change in resistance of

the channel region, the drain current changes. Since the channel region is lightly doped so the lightly doped values of the piezoresistive coefficients can be used for FET's.

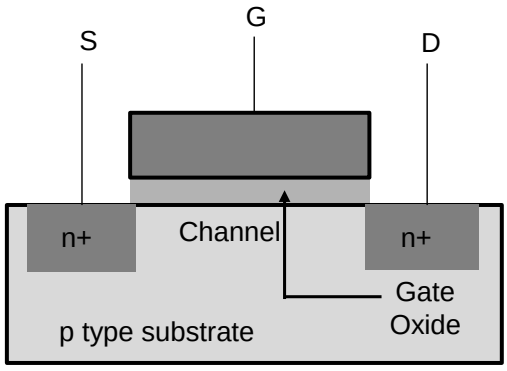


Figure A.6: Cross-section of a Field Effect Transistor

The drain-source current expression for NMOS and PMOS transistors in the saturation region is shown in the following.

$$I_{DN} = \frac{K_n}{2}\left(V_{GS} - V_{TN}\right)^2 (1 + \lambda_n V_{DS}) \tag{A.20}$$

$$I_{DP} = \frac{K_p}{2}\left(V_{GS} + V_{TP}\right)^2 (1 + \lambda_p V_{SD}) \tag{A.21}$$

where K_n and K_p are the transconduction parameters that is defined as

$$K_n = \mu_n C''_{ox} \frac{W}{L} = \mu_n \frac{\varepsilon_{ox}}{T_{ox}} \frac{W}{L} \tag{A.22}$$

$$K_p = \mu_p C''_{ox} \frac{W}{L} = \mu_n \frac{\varepsilon_{ox}}{T_{ox}} \frac{W}{L} \tag{A.23}$$

where V_{TN} and V_{TP} are the NMOS and PMOS threshold voltages of the transistor, V_{GS} is the gate to source voltage, V_{DS} is the drain to source voltage, C''_{ox} is the gate oxide capacitance per unit area, μ_n and μ_p are the electron mobility and hole mobility respectively, T_{ox} is the oxide thickness, λ_n and λ_p are the channel length modulation

parameters,$\varepsilon_{ox}$is the dielectric constant of the oxide layer and W and L are the width and length of the channel, respectively. It is obvious from the above equation is that the stress induced change in drain current of the transistor can be caused by modulation of the mobility, threshold voltage or change in device dimensions.

It has been discussed by Bradley that the strain-induced device geometry changes in silicon can be neglected since the modulation of channel-length and width W and L, are generally small compared to the stress induced changes in carrier mobility which is an order or two larger in magnitude than the dimensional changes [A4]. Therefore the modulation in drain current in NMOS in the saturation region can be written as disregarding the dimensional change terms

$$\frac{\Delta I_D}{I_D} \cong \frac{\Delta K_n}{K_n} - 2\frac{\Delta V_{TN}}{V_{TN}}\left(\frac{V_{TN}}{V_{GS}-V_{TN}}\right) + \frac{\Delta \lambda_n}{\lambda_n}\left(\frac{\lambda_n V_{DS}}{1+\lambda_n V_{DS}}\right) \qquad \text{(A.24)}$$

Similar expression can be written for PMOS. The stress induced changes in threshold voltage demonstrate that this quantity is independent of stress . Therefore the variation in drain current can be conveniently expressed by neglecting the second term and only considering the stress induced mobility variation term alone.

The CMOS optimized sensor consists of pairs of NMOS and PMOS transistors with orthogonal channel orientations as shown in Fig. A.7. The resistive channels of PMOS transistor pair is oriented along 0˚ and 90˚ and for NMOS along ± 45˚. For an arbitrary stress state, the drain current through a MOSFET by neglecting the effect of threshold voltage variation can be written as

$$I_D + \Delta I_D = I_D\left(1+\frac{\Delta I_D}{I_D}\right) = I_D\left(1+\frac{\Delta \mu}{\mu}\right) \qquad \text{(A.25)}$$

where

$$\frac{\Delta\mu}{\mu} = -\frac{\Delta R}{R} \tag{A.26}$$

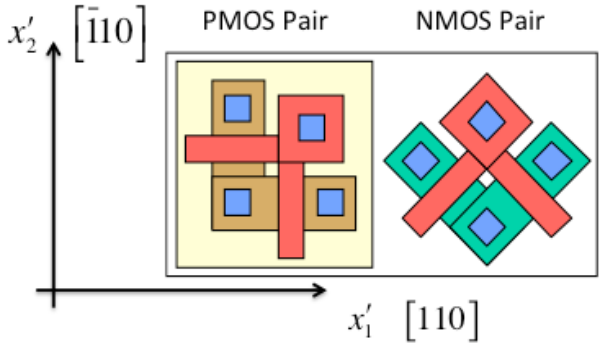


Figure A.7 CMOS Sensor Rosette in (100) Silicon

The stress induced variation in mobility depend on the orientation of wafer surface and the current direction through the channel of the MOS device. The normalized change in drain current due to stress for a MOSFET on (100) silicon in strong inversion can be written [5] as

$$\begin{aligned}\frac{\Delta I_D}{I_D} = &\left[\frac{\Pi_S + \Pi_{44}}{2}\sigma'_{11} + \frac{\Pi_S - \Pi_{44}}{2}\sigma'_{22}\right]\cos^2\phi \\ &-\left[\frac{\Pi_S - \Pi_{44}}{2}\sigma'_{11} + \frac{\Pi_S + \Pi_{44}}{2}\sigma'_{22}\right]\sin^2\phi \\ &-\Pi_{12}\sigma'_{33} - \Pi_D\sigma'_{12}\sin 2\phi + f(T)\end{aligned} \tag{A.27}$$

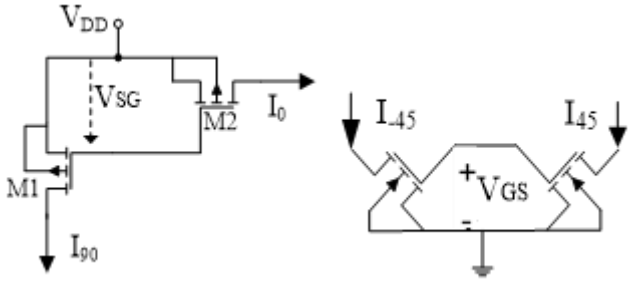


Fig. A.8: PMOS (Left) & NMOS (Right) Sensor Circuits

Considering direct analogy to the resistor case shown in Fig A.3 and using the equations for the optimized resistor sensor rosette on (100) silicon given in Eq. (A.15), the equations for the resistive channel of MOS transistors oriented at 0˚, 90˚ and ± 45˚ shown in Fig. A.7 can be given by

$$
\begin{aligned}
I_D\big|_{0^\circ} &= I_{D0}\left[1-\frac{\Pi_S}{2}\left(\sigma'_{11}+\sigma'_{22}\right)-\frac{\Pi_{44}}{2}\left(\sigma'_{11}-\sigma'_{22}\right)-\Pi_{12}\sigma'_{33}+f_p(T)\right]\\
I_D\big|_{90^\circ} &= I_{D0}\left[1-\frac{\Pi_S}{2}\left(\sigma'_{11}+\sigma'_{22}\right)+\frac{\Pi_{44}}{2}\left(\sigma'_{11}-\sigma'_{22}\right)-\Pi_{12}\sigma'_{33}+f_p(T)\right]\\
I_D\big|_{45^\circ} &= I_{D0}\left[1-\frac{\Pi_S}{2}\left(\sigma'_{11}+\sigma'_{22}\right)-\Pi_{12}\sigma'_{33}-\Pi_D\sigma'_{12}+f_n(T)\right]\\
I_D\big|_{-45^\circ} &= I_{D0}\left[1-\frac{\Pi_S}{2}\left(\sigma'_{11}+\sigma'_{22}\right)-\Pi_{12}\sigma'_{33}+\Pi_D\sigma'_{12}+f_n(T)\right]
\end{aligned}
\tag{A.28}
$$

In which the unstressed drain currents for both PMOS and NMOs devices are

$$
\begin{aligned}
I_{D0}\big|_n &= \frac{K_{n0}}{2}\left(V_{GS}-V_{TN}\right)^2\left(1+\lambda_n V_{DS}\right)\\
&= \frac{\mu_{n0}C''_{ox}}{2}\frac{W}{L}\left(V_{GS}-V_{TN}\right)^2\left(1+\lambda_n V_{DS}\right)\\
I_{D0}\big|_p &= \frac{K_{p0}}{2}\left(V_{GS}+V_{TP}\right)^2\left(1+\lambda_p V_{DS}\right)\\
&= \frac{\mu_{p0}C''_{ox}}{2}\frac{W}{L}\left(V_{GS}+V_{TP}\right)^2\left(1+\lambda_p V_{DS}\right)
\end{aligned}
\tag{A.29}
$$

The Π's are the effective piezoresistive coefficients for the majority carrier mobility in the channel of the MOS transistor and they are adopted for FETs as compared to lowercase π values for resistors. The value of Π_{44}^{p} is quite large compared to the value of Π_{44}^{n} which is very small. Therefore the 0˚- 90˚ PMOS pair will demonstrate high sensitivity to in plane normal stress difference. On the contrary, the value of Π_{D}^{n} is quite large

compared to the value of Π_D^p , therefore the ± 45° NMOS pair should be highly sensitive to in-plane shear stress.

The MOSFET sensor for normal stress difference (PMOS) and for in-plane shear stress (NMOS) are shown in Fig. A.8. One of the main considerations during the utilization of piezoresistive stress sensors are the temperature compensation of the measured stress terms since the temperature causes significant change in the measurements. On the (100) surface, there are two basic temperature compensated rosette configurations. If the normalized drain current variation for the orthogonal pair of devices are subtracted from each other, which results in temperature compensated expressions and only the effect of stress on the drain current remain.

$$\begin{aligned} &\frac{\Delta I_{D90}}{I_{D90}} - \frac{\Delta I_{D_0}}{I_{D_0}} = \Pi_{44}^p \left(\sigma'_{11} - \sigma'_{22}\right) \\ &\frac{\Delta I_{D-45}}{I_{D-45}} - \frac{\Delta I_{D45}}{I_{D45}} = 2\left(\Pi_{11}^n - \Pi_{12}^n\right)\sigma'_{12} = 2\Pi_D^n \sigma'_{12} \end{aligned} \tag{A.30}$$

Due to the high values Π_{44}^p and Π_D^n , the orthogonal pair of PMOS devices is elected for in-plane normal stress sensors and the orthogonal pair of NMOS devices is taken as the in plane shear stress sensor.

A.6 Reference

[A1] Suhling, J. C. and Jaeger R.C. Silicon Piezoresistive Stress Sensors and Their Application in electronic Packaging. IEEE Sensors Journal.pp. 14-30, 2001..

[A2] Bittle, D. A., Suhling, J. C., Beaty, R. E., Jaeger, R. C., and Johnson, R.W. . Piezoresistive stress sensors for structural analysis of electronic packages,. Journal of Electronic Packaging. 113(3): p. 203–215, 1991.

[A3] R. Ramani, "Piezoresistive Behaviour of MOSFET and FET-based Stress Sensor Circuits," PhD Dissertation, Auburn University, 1996.

[A4] A. Bradley, “Piezoresistive Behavior of MOSFETS and MOS Circuits”’ PhD Dissertation, Auburn University, 1999.

[A5] A. T. Bradley, R. C. Jaeger, J. C. Suhling, and K. J. O’Connor, “Stress sensitivity of short-channel MOSFETs on (100) silicon,” IEEE Transaction Electron Devices, vol. 48, no. 9, pp. 2009–2015, Sep. 2001.

APPENDIX B

Table B.1 Derivatives of Stress with respect to Resistor Values

$$D_1 = \left(B_2^p - B_1^p\right)B_3^n + \left(B_1^p - B_3^p\right)B_2^n + \left(B_3^p - B_2^p\right)B_1^n \qquad D_2 = \left(B_1^n + B_2^n\right)B_3^p - \left(B_1^p + B_2^p\right)B_3^n$$

	$\Delta R_1/R_1$	$\Delta R_2/R_2$	$\Delta R_3/R_3$	$\Delta R_4/R_4$	$\Delta R_5/R_5$	$\Delta R_6/R_6$	$\Delta R_7/R_7$	$\Delta R_8/R_8$
σ'_{11}	$+\frac{B_3^p - B_2^p}{2D_1} + \frac{B_3^p}{2D_2}$	0	$-\frac{B_3^p - B_2^p}{2D_1} + \frac{B_3^p}{2D_2}$	0	$-\frac{B_3^n - B_2^n}{2D_1} - \frac{B_3^n}{2D_2}$	0	$+\frac{B_3^n - B_2^n}{2D_1} - \frac{B_3^n}{2D_2}$	0
σ'_{22}	$-\frac{B_3^p - B_2^p}{2D_1} + \frac{B_3^p}{2D_2}$	0	$+\frac{B_3^p - B_2^p}{2D_1} + \frac{B_3^p}{2D_2}$	0	$+\frac{B_3^n - B_2^n}{2D_1} - \frac{B_3^n}{2D_2}$	0	$-\frac{B_3^n - B_2^n}{2D_1} - \frac{B_3^n}{2D_2}$	0
σ'_{33}	$-\frac{B_1^p + B_2^p}{2D_2}$	0	$-\frac{B_1^p + B_2^p}{2D_2}$	0	$\frac{B_1^n + B_2^n}{2D_2}$	0	$\frac{B_1^n + B_2^n}{2D_2}$	0
σ'_{13}	0	$-\frac{\sqrt{2}}{8}\frac{B_2^p - B_1^p}{D_1}$	0	$+\frac{\sqrt{2}}{8}\frac{B_2^p - B_1^p}{D_1}$	0	$+\frac{\sqrt{2}}{8}\frac{B_2^n - B_1^n}{D_1}$	0	$-\frac{\sqrt{2}}{8}\frac{B_2^n - B_1^n}{D_1}$
σ'_{23}	$-\frac{\sqrt{2}}{8}\frac{B_2^p - B_1^p}{D_1}$	0	$+\frac{\sqrt{2}}{8}\frac{B_2^p - B_1^p}{D_1}$	0	$+\frac{\sqrt{2}}{8}\frac{B_2^n - B_1^n}{D_1}$	0	$-\frac{\sqrt{2}}{8}\frac{B_2^n - B_1^n}{D_1}$	0
σ'_{12}	0	$+\frac{B_3^p - B_2^p}{2D_1}$	0	$-\frac{B_3^p - B_2^p}{2D_1}$	0	$-\frac{B_3^n - B_2^n}{2D_1}$	0	$+\frac{B_3^n - B_2^n}{2D_1}$
$\sigma'_{11} - \sigma'_{22}$	$+\frac{B_3^p - B_2^p}{D_1}$		$-\frac{B_3^p - B_2^p}{D_1}$		$-\frac{B_3^n - B_2^n}{D_1}$		$+\frac{B_3^n - B_2^n}{D_1}$	

Table B.2 Derivatives of Stress with respect to Temperature		
	T	Value (MPa/^{o}C)
σ'_{11}	$\frac{-\alpha_1^n B_3^p + \alpha_1^p B_3^n}{D_2}$	–113
σ'_{22}	$\frac{-\alpha_1^n B_3^p + \alpha_1^p B_3^n}{D_2}$	–113
σ'_{33}	$\frac{\alpha_1^n \left(B_1^p + B_2^p\right) - \alpha_1^p \left(B_1^n + B_2^n\right)}{D_2}$	–93.7
σ'_{13}	0	0
σ'_{23}	0	0
σ'_{12}	0	0
$\sigma'_{11} - \sigma'_{22}$	0	0

APPENDIX C

Sensitivities for (111) Silicon

Sensitivities for (111) Silicon
σ'_{11}
$S^{\sigma'_{11}}_{B_1^p} = \frac{-B_1^p(B_2^n - B_3^n)}{2[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}(1 - \frac{\sigma'_{22}}{\sigma'_{11}}) + \frac{B_1^p B_3^n}{2[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]}(1 + \frac{\sigma'_{22}}{\sigma'_{11}})$
$S^{\sigma'_{11}}_{B_1^n} = \frac{-B_1^n(B_3^p - B_2^p)}{2[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}(1 - \frac{\sigma'_{22}}{\sigma'_{11}}) - \frac{B_1^n B_3^p}{2[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]}(1 + \frac{\sigma'_{22}}{\sigma'_{11}})$
$S^{\sigma'_{11}}_{B_2^p} = \frac{B_2^p(B_2^n - B_3^n)}{2[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}(1 - \frac{\sigma'_{22}}{\sigma'_{11}}) + \frac{2\sqrt{2}B_2^p(B_2^n - B_3^n)}{[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}(\frac{\sigma'_{23}}{\sigma'_{11}}) + \frac{B_2^p B_3^n}{2[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]}(1 + \frac{\sigma'_{22}}{\sigma'_{11}})$
$S^{\sigma'_{11}}_{B_2^n} = \frac{B_2^n(B_3^p - B_2^p)}{2[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}(1 - \frac{\sigma'_{22}}{\sigma'_{11}}) - \frac{2\sqrt{2}B_2^n(B_2^p - B_3^p)}{[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}(\frac{\sigma'_{23}}{\sigma'_{11}}) - \frac{B_2^n B_3^p}{2[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]}(1 + \frac{\sigma'_{22}}{\sigma'_{11}})$
$S^{\sigma'_{11}}_{B_3^p} = \frac{-2\sqrt{2}B_3^p(B_2^n - B_3^n)}{[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}(\frac{\sigma'_{23}}{\sigma'_{11}}) + \frac{B_3^p B_3^n}{[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]}(\frac{\sigma'_{33}}{\sigma'_{11}})$

$$S^{\sigma'_{11}}_{B_3^n} = \frac{2\sqrt{2}B_3^n(B_2^p - B_3^p)}{[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}\left(\frac{\sigma'_{23}}{\sigma'_{11}}\right)$$
$$- \frac{B_3^n B_3^p}{[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]}\left(\frac{\sigma'_{33}}{\sigma'_{11}}\right)$$

σ'_{22}

$$S^{\sigma'_{22}}_{B_1^p} = \frac{-B_1^p(B_2^n - B_3^n)}{2[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}\left(1 - \frac{\sigma'_{11}}{\sigma'_{22}}\right)$$
$$+ \frac{B_1^p B_3^n}{2[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]}\left(1 + \frac{\sigma'_{11}}{\sigma'_{22}}\right)$$

$$S^{\sigma'_{22}}_{B_1^n} = \frac{-B_1^n(B_3^p - B_2^p)}{2[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}\left(1 - \frac{\sigma'_{11}}{\sigma'_{22}}\right) - \frac{B_1^n B_3^p}{2[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]}\left(1 + \frac{\sigma'_{11}}{\sigma'_{22}}\right)$$

$$S^{\sigma'_{22}}_{B_2^p} = \frac{B_2^p(B_2^n - B_3^n)}{2[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}\left(1 - \frac{\sigma'_{11}}{\sigma'_{22}}\right)$$
$$- \frac{2\sqrt{2}B_2^p(B_2^n - B_3^n)}{[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}\left(\frac{\sigma'_{23}}{\sigma'_{22}}\right) + \frac{B_2^p B_3^n}{2[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]}\left(1 + \frac{\sigma'_{11}}{\sigma'_{22}}\right)$$

$$S^{\sigma'_{22}}_{B_2^n} = \frac{B_2^n(B_3^p - B_2^p)}{2[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}\left(1 - \frac{\sigma'_{11}}{\sigma'_{22}}\right)$$
$$+ \frac{2\sqrt{2}B_2^n(B_2^p - B_3^p)}{[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}\left(\frac{\sigma'_{23}}{\sigma'_{22}}\right) - \frac{B_2^n B_3^p}{2[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]}\left(1 + \frac{\sigma'_{11}}{\sigma'_{22}}\right)$$

$$S^{\sigma'_{22}}_{B_3^p} = \frac{2\sqrt{2}B_3^p(B_2^n - B_3^n)}{[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}\left(\frac{\sigma'_{23}}{\sigma'_{22}}\right)$$
$$+ \frac{B_3^p B_3^n}{[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]}\left(\frac{\sigma'_{33}}{\sigma'_{22}}\right)$$

$$S^{\sigma'_{22}}_{B_3^n} = \frac{-2\sqrt{2}B_3^n(B_2^p - B_3^p)}{[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}\left(\frac{\sigma'_{23}}{\sigma'_{22}}\right)$$
$$- \frac{B_3^n B_3^p}{[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]}\left(\frac{\sigma'_{33}}{\sigma'_{22}}\right)$$

σ'_{33}

$$S^{\sigma'_{33}}_{B_1^p} = \frac{-B_1^p(B_1^n + B_2^n)}{2[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]}\left(\frac{\sigma'_{11} + \sigma'_{22}}{\sigma'_{33}}\right) = -0.23\left(\frac{\sigma'_{11} + \sigma'_{22}}{\sigma'_{33}}\right)$$

$$S^{\sigma'_{33}}_{B_1^n} = \frac{B_1^n(B_1^p + B_2^p)}{2[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]}\left(\frac{\sigma'_{11} + \sigma'_{22}}{\sigma'_{33}}\right) = 3.30\left(\frac{\sigma'_{11} + \sigma'_{22}}{\sigma'_{33}}\right)$$

$$S^{\sigma'_{33}}_{B_2^p} = \frac{-B_2^p(B_1^n + B_2^n)}{2[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]}\left(\frac{\sigma'_{11} + \sigma'_{22}}{\sigma'_{33}}\right) = 0.074\left(\frac{\sigma'_{11} + \sigma'_{22}}{\sigma'_{33}}\right)$$

$$S^{\sigma'_{33}}_{B_2^n} = \frac{B_2^n(B_1^p + B_2^p)}{2[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]}\left(\frac{\sigma'_{11} + \sigma'_{22}}{\sigma'_{33}}\right) = -3.14\left(\frac{\sigma'_{11} + \sigma'_{22}}{\sigma'_{33}}\right)$$

$$S^{\sigma'_{33}}_{B_3^p} = \frac{-2B_3^p}{2[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]}(B_1^n + B_2^n) = 0.29$$

$$S^{\sigma'_{33}}_{B_3^n} = \frac{2B_3^n}{2[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]}(B_1^p + B_2^p) = -1.29$$

σ'_{13}

$$S^{\sigma'_{13}}_{B_1^p} = \frac{-\sqrt{2}B_1^p(B_1^n - B_2^n)}{4[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}\left(\frac{\sigma'_{12}}{\sigma'_{13}}\right)$$

$$S^{\sigma'_{13}}_{B_1^n} = \frac{\sqrt{2}(B_1^p - B_2^p)B_1^n}{4[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}\left(\frac{\sigma'_{12}}{\sigma'_{13}}\right)$$

$$S^{\sigma'_{13}}_{B_2^p} = \frac{\sqrt{2}B_2^p(B_1^n - B_2^n)\left(2\sqrt{2} + \frac{\sigma'_{12}}{\sigma'_{13}}\right)}{4[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}$$

$$S^{\sigma'_{13}}_{B_2^n} = \frac{\sqrt{2}B_2^n(B_2^p - B_1^p)\left(2\sqrt{2} + \frac{\sigma'_{12}}{\sigma'_{13}}\right)}{4[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}$$

$$S^{\sigma'_{13}}_{B_3^p} = \frac{-B_3^p(B_1^n - B_2^n)}{[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}$$

$$S^{\sigma'_{13}}_{B_3^n} = \frac{B_3^n(B_1^p - B_2^p)}{[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}$$

σ'_{23}

$$S^{\sigma'_{23}}_{B_1^p} = \frac{-\sqrt{2}B_1^p(B_1^n - B_2^n)}{8[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}\left(\frac{\sigma'_{11} - \sigma'_{22}}{\sigma'_{23}}\right)$$

$$S^{\sigma'_{23}}_{B_1^n} = \frac{\sqrt{2}B_1^n(B_1^p - B_2^p)}{8[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}\left(\frac{\sigma'_{11} - \sigma'_{22}}{\sigma'_{23}}\right)$$

$$S^{\sigma'_{23}}_{B_2^p} = \frac{\sqrt{2}B_2^p(B_1^n - B_2^n)}{8[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}\left(4\sqrt{2} + \frac{\sigma'_{11} - \sigma'_{22}}{\sigma'_{23}}\right)$$

$$S^{\sigma'_{23}}_{B^n_2} = \frac{\sqrt{2}B^n_2(B^p_2 - B^p_1)}{8[(B^p_2 - B^p_1)B^n_3 + (B^p_1 - B^p_3)B^n_2 + (B^p_3 - B^p_2)B^n_1]}(4\sqrt{2} + \frac{\sigma'_{11} - \sigma'_{22}}{\sigma'_{23}})$$

$$S^{\sigma'_{23}}_{B^p_3} = \frac{-B^p_3(B^n_1 - B^n_2)}{[(B^p_2 - B^p_1)B^n_3 + (B^p_1 - B^p_3)B^n_2 + (B^p_3 - B^p_2)B^n_1]}$$

$$S^{\sigma'_{23}}_{B^n_3} = \frac{B^n_3(B^p_1 - B^p_2)}{[(B^p_2 - B^p_1)B^n_3 + (B^p_1 - B^p_3)B^n_2 + (B^p_3 - B^p_2)B^n_1]}$$

σ'_{12}

$$S^{\sigma'_{12}}_{B^p_1} = \frac{(B^n_3 - B^n_2)B^p_1}{[(B^p_2 - B^p_1)B^n_3 + (B^p_1 - B^p_3)B^n_2 + (B^p_3 - B^p_2)B^n_1]}$$

$$S^{\sigma'_{12}}_{B^n_1} = \frac{(B^p_2 - B^p_3)B^n_1}{[(B^p_2 - B^p_1)B^n_3 + (B^p_1 - B^p_3)B^n_2 + (B^p_3 - B^p_2)B^n_1]}$$

$$S^{\sigma'_{12}}_{B^p_2} = \frac{(B^n_2 - B^n_3)B^p_2}{[(B^p_2 - B^p_1)B^n_3 + (B^p_1 - B^p_3)B^n_2 + (B^p_3 - B^p_2)B^n_1]}(1 + 2\sqrt{2}\frac{\sigma'_{13}}{\sigma'_{12}})$$

$$S^{\sigma'_{12}}_{B^n_2} = \frac{(B^p_3 - B^p_2)B^n_2}{[(B^p_2 - B^p_1)B^n_3 + (B^p_1 - B^p_3)B^n_2 + (B^p_3 - B^p_2)B^n_1]}(1 + 2\sqrt{2}\frac{\sigma'_{13}}{\sigma'_{12}})$$

$$S^{\sigma'_{12}}_{B^p_3} = \frac{-2\sqrt{2}(B^n_2 - B^n_3)B^p_3}{[(B^p_2 - B^p_1)B^n_3 + (B^p_1 - B^p_3)B^n_2 + (B^p_3 - B^p_2)B^n_1]}(\frac{\sigma'_{13}}{\sigma'_{12}})$$

$$S^{\sigma'_{12}}_{B^n_3} = \frac{2\sqrt{2}(B^p_2 - B^p_3)B^n_3}{[(B^p_2 - B^p_1)B^n_3 + (B^p_1 - B^p_3)B^n_2 + (B^p_3 - B^p_2)B^n_1]}(\frac{\sigma'_{13}}{\sigma'_{12}})$$

σ'_{11}- σ'_{22}

$$S^{\sigma'_{11}-\sigma'_{22}}_{B^p_1} = \frac{-B^p_1(B^n_2 - B^n_3)}{[(B^p_2 - B^p_1)B^n_3 + (B^p_1 - B^p_3)B^n_2 + (B^p_3 - B^p_2)B^n_1]}$$

$$S^{\sigma'_{11}-\sigma'_{22}}_{B^n_1} = \frac{-B^n_1(B^p_3 - B^p_2)}{[(B^p_2 - B^p_1)B^n_3 + (B^p_1 - B^p_3)B^n_2 + (B^p_3 - B^p_2)B^n_1]}$$

$$S^{\sigma'_{11}-\sigma'_{22}}_{B^p_2} = \frac{B^p_2(B^n_2 - B^n_3)}{[(B^p_2 - B^p_1)B^n_3 + (B^p_1 - B^p_3)B^n_2 + (B^p_3 - B^p_2)B^n_1]}$$
$$+ \frac{4\sqrt{2}B^p_2(B^n_2 - B^n_3)}{[(B^p_2 - B^p_1)B^n_3 + (B^p_1 - B^p_3)B^n_2 + (B^p_3 - B^p_2)B^n_1]}(\frac{\sigma'_{23}}{\sigma'_{11} - \sigma'_{22}})$$

$S^{\sigma'_{11}-\sigma'_{22}}_{B^n_2} = \frac{B^n_2(B^p_3 - B^p_2)}{[(B^p_2 - B^p_1)B^n_3 + (B^p_1 - B^p_3)B^n_2 + (B^p_3 - B^p_2)B^n_1]}$ $- \frac{4\sqrt{2}B^n_2(B^p_2 - B^p_3)}{[(B^p_2 - B^p_1)B^n_3 + (B^p_1 - B^p_3)B^n_2 + (B^p_3 - B^p_2)B^n_1]}(\frac{\sigma'_{23}}{\sigma'_{11} - \sigma'_{22}})$
$S^{\sigma'_{11}-\sigma'_{22}}_{B^p_3} = \frac{-4\sqrt{2}B^p_3(B^n_2 - B^n_3)}{[(B^p_2 - B^p_1)B^n_3 + (B^p_1 - B^p_3)B^n_2 + (B^p_3 - B^p_2)B^n_1]}(\frac{\sigma'_{23}}{\sigma'_{11} - \sigma'_{22}})$
$S^{\sigma'_{11}-\sigma'_{22}}_{B^n_3} = \frac{4\sqrt{2}B^n_3(B^p_2 - B^p_3)}{[(B^p_2 - B^p_1)B^n_3 + (B^p_1 - B^p_3)B^n_2 + (B^p_3 - B^p_2)B^n_1]}(\frac{\sigma'_{23}}{\sigma'_{11} - \sigma'_{22}})$
$\sigma'_{11} + \sigma'_{22}$
$S^{\sigma'_{11}+\sigma'_{22}}_{B^p_1} = \frac{B^p_1 B^n_3}{[(B^n_1 + B^n_2)B^p_3 - (B^p_1 + B^p_2)B^n_3]}$
$S^{\sigma'_{11}+\sigma'_{22}}_{B^n_1} = \frac{-B^n_1 B^p_3}{[(B^n_1 + B^n_2)B^p_3 - (B^p_1 + B^p_2)B^n_3]}$
$S^{\sigma'_{11}+\sigma'_{22}}_{B^p_2} = \frac{B^p_2 B^n_3}{[(B^n_1 + B^n_2)B^p_3 - (B^p_1 + B^p_2)B^n_3]}$
$S^{\sigma'_{11}+\sigma'_{22}}_{B^n_2} = -\frac{B^n_2 B^p_3}{[(B^n_1 + B^n_2)B^p_3 - (B^p_1 + B^p_2)B^n_3]}$
$S^{\sigma'_{11}+\sigma'_{22}}_{B^p_3} = \frac{2B^p_3 B^n_3}{[(B^n_1 + B^n_2)B^p_3 - (B^p_1 + B^p_2)B^n_3]}(\frac{\sigma'_{33}}{\sigma'_{11} + \sigma'_{22}})$
$S^{\sigma'_{11}+\sigma'_{22}}_{B^n_3} = -\frac{2B^n_3 B^p_3}{[(B^n_1 + B^n_2)B^p_3 - (B^p_1 + B^p_2)B^n_3]}(\frac{\sigma'_{33}}{\sigma'_{11} + \sigma'_{22}})$