

**Optimization of High Power Gallium Nitride Based Point of Load Converters for
Data Center Power Supply Chains**

by

Luke L. Jenkins

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Approved by

Robert N. Dean, Chair, Associate Professor of Electrical and Computer Engineering
Mark Halpin, Alabama Power Company Distinguished Professor of Electrical and Computer
Engineering

Michael Hamilton, Assistant Professor of Electrical and Computer Engineering

ABSTRACT

Wide-bandgap semiconductors are enabling higher efficiency, greater power density, smaller size, and higher switching frequency than traditional Si semiconductors. This work shows the development of an over 96% efficient 12-to-1 V GaN-based point of load (POL) converter capable of 150 A operation. The multiphase POL converter demonstrates superior performance to commercial and other published POL converters. Layout and control algorithms help to produce a reliable product that is in a pre-production state. Development begins with optimizing a single phase POL converter and expanding to multiphase to meet load requirements and improve output signal integrity. Major concerns include reliability, efficiency, transient performance, and power density. These concerns are currently preventing industry adoption of wide-bandgap systems. In this work, efficiency is remarkably high, reliability studies have been performed and are ongoing, transient analysis is competitive with modern POL converters, and the current system has a competitive power density of approximately 270 W/in³. The POL converter is part of a wide-bandgap power supply chain designed for data center applications and is tested along with a three-phase front end rectifier and intermediate bus converter to show the potential of modern semiconductors in power conversion applications. This work results in reduced energy consumption, higher output power, smaller size, and will ease reliability concerns of future wide-bandgap power electronics.

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LIST OF ABBREVIATIONS

2DEG	Two-Dimensional Electron Gas
BCM	Bulk Converter Module
BPR	Bulk Power Regulator
CCM	Continuous Conduction Mode
CPES	Center for Power Electronics Research
CSP	Chip-Scale Package
DCCA	Distributed Converter and Control Assembly
DCM	Discontinuous Mode
DRAM	Dynamic Random Access Memory
D-Mode	Depletion-Mode
eGaN	Enhancement-Mode Gallium Nitride
E-Mode	Enhancement-Mode
EPC	Efficient Power Conversion Corporation
ESD	Electrostatic Discharge
f_{eff}	Effective Frequency
FER	Front-End Rectifier
FET	Field Effect Transistor
FLOPS	Floating-Point Operations Per Second

GaAs	Gallium Arsenide
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
HP	Hewlett-Packard
HPC	High Performance Computing
HVDC	High Voltage Direct Current
IBA	Intermediate Bus Architecture
IBC	Intermediate Bus Converter
IBM	International Business Machine
IC	Integrated Circuit
IR	International Rectifier
L_{Loop}	High Frequency Power Loop Inductance
L_S	Common Source Inductance
MOSFET	Metal Oxide Field Effect Transistor
PA	Power Amplifier
PCB	Printed Circuit Board
PDU	Power Distribution Unit
PFC	Power Factor Correction
POL	Point of Load
PPM	Parts Per Million
PRM	Pre Regulator Module
PSU	Power Supply Unit
$R_{DS(ON)}$	Drain-to-Source On-Resistance

RF	Radio Frequency
SCR	Silicon Controlled Rectifier
Si	Silicon
SiC	Silicon Carbide
SMPS	Switch-Mode Power Supply
SR	Synchronous Rectifier
UPS	Uninterrupted Power Supply
VTM	Voltage Transformation Module
WBG	Wide-Bandgap

CHAPTER 1

INTRODUCTION

1.1 Statement of Purpose

The purpose of this research is to make significant improvements to state-of-the-art low-voltage point of load (POL) converters. In order of priority, the POL converter should demonstrate substantial improvements in efficiency (>5% improvement) beyond the best commercial products, demonstrate reliable operation, match or beat transient performance of commercial POL converters, and exhibit high power density. The design is tailored to data center and server power supplies but is applicable to many other areas. This progression will yield energy savings, reduced maintenance, higher server availability, reduced volume, and lower line loss since a smaller POL can be located closer to the load.

1.2 Motivation

Data center energy costs are on the rise due to an immense escalation in cloud computing and digital information storage [1]. To illustrate, a 1 MW high availability data center will consume approximately \$20 million of electricity in its lifetime [2]. In the U.S. alone, the annual power cost to operate data centers was \$4.5 billion in 2007 [3], it has increased every year since 1980 [4], and it is projected to increase more rapidly in the future due to greater cloud computing dependence [5]. Traditionally, computer system design has been focused on increasing performance [6]. Today, the energy cost of high performance servers has become large enough that, from a business standpoint, it is worth investing in more expensive hardware to reap savings in operating cost [7]. The same mindset is becoming evident in other applications like transportation, HiRel, and consumer electronics and has led to recent growth in higher efficiency wide-bandgap (WBG)

power semiconductor development [8]. With the development of new materials for power semiconductors, the power electronics market is primed for technological advancements that will lead to more efficient and power dense switch-mode power supplies (SMPS).

1.3 Data Center Power Supply Chain

Typical data centers exhibit less than 50% energy efficiency because over half of the power is consumed by power conversion, distribution, battery backups, and cooling [9]. The power supply chain is especially inefficient due to overdesign to reach near 100% availability. Most high-end systems claim N+1 redundancy, no single-points of failure, hot swappable sub-assemblies, and large uninterruptible power supplies (UPSs) to achieve as high as 99.998% availability [10]. For reliability concerns, data is often stored in multiple locations to ensure it is not lost due to failure. Additionally, it is very desirable that the system may receive maintenance without bringing the rack offline. This improves availability in the event of component or sub-assembly failure. The additional components used to achieve high reliability systems also consume energy, which presents a direct trade-off between efficiency and reliability. In most industrial systems, reliability is of the highest concern since the customer immediately notices a system failure. Poor efficiency adds significant cost over the system's life but is not as tangible as system failure; however, as cloud computing and digital storage increase rapidly, the market is beginning to realize the value in an efficient system and how it may reduce cost over the system's life.

The conventional power supply architecture (see Fig. 1.1) connects a 480 V three-phase (3 ϕ) AC bus to the power distribution unit (PDU), which contains the UPS and is external to the server rack. An AC/DC rectifier and DC/AC inverter are necessary to incorporate the UPS into the PDU. A 120 V AC bus leaves the PDU and connects to the rack. The power supply unit (PSU) is

located at the bottom of the rack and creates a 12 V DC bus that is distributed to each blade. Each blade contains several POLs located near the electronic loads (i.e. DRAM, processors, auxiliary power, etc.). Typical modern processor loads operate between 0.9 and 1.2 V. This architecture contains unnecessary conversion stages and significant line loss—particularly at the 12 V DC distribution.

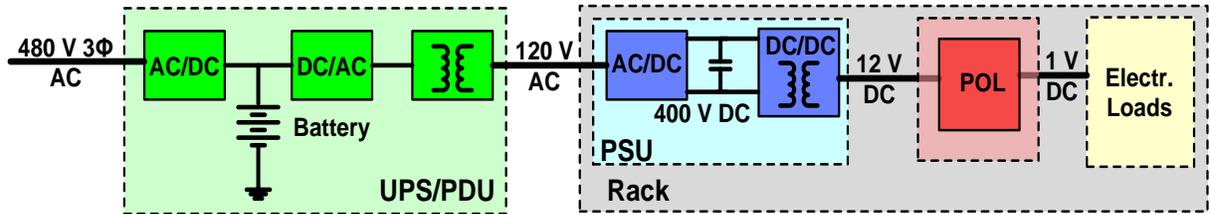


Fig. 1.1: Conventional power supply architecture.

In pursuit of higher power supply efficiency, it is purposed that WBG power semiconductors can lead to smaller size and allow the entire architecture to be located on the rack. To reduce distribution losses, a 400 V distribution bus is purposed. High voltage distribution offers many benefits but also requires additional safety precautions; however, a safe 400 V distribution is certainly attainable. A few high-end products have already begun developing high voltage distribution, such as IBM’s Power 775/775+ and System Z196, which distribute 350 V DC to each blade/drawer within the rack. Unnecessary power conversion stages can be eliminated by implementing the UPS on the 400 V DC bus, and distribution losses can be reduced as a result of a high voltage DC (HVDC) bus connecting to each blade. This proposed architecture can improve system efficiency to as high as 73% (see Fig. 1.2 and Fig. 1.3) [9][11]. With fewer power conversion stages, there exist fewer points of failure and reduced size. Additionally, WBG materials have increased power density by 50-80% in general, allowing power converters to be

located closer to the load to reduce line loss. Wide-bandgap semiconductors are the enabling technology that support higher voltage step down ratios in a smaller package.

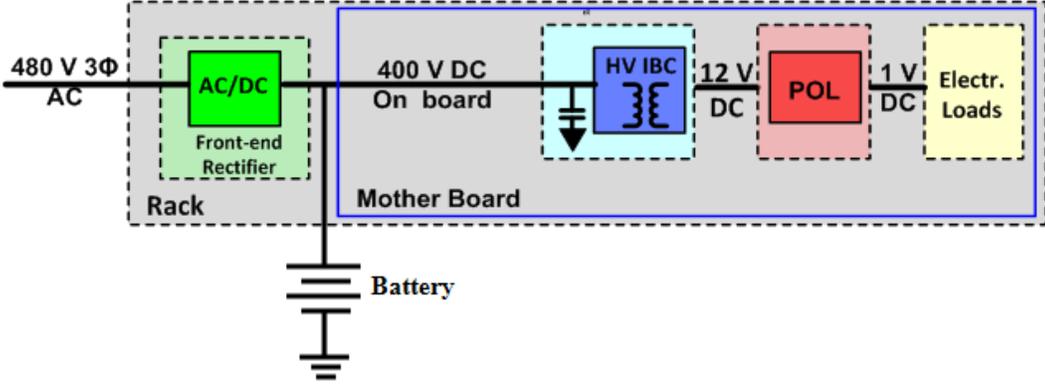


Fig. 1.2: WBG HVDC Distribution Architecture.

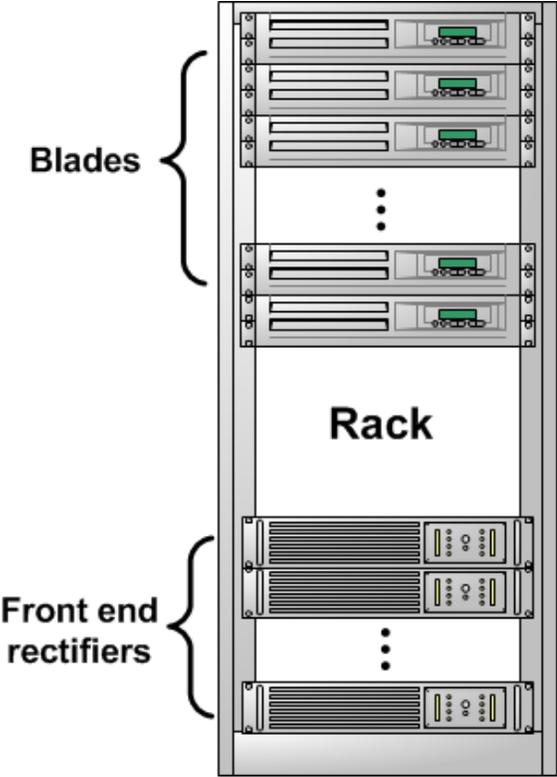


Fig. 1.3: Purposed architecture places all power conversion systems within the rack. IBC and POL are located on the motherboard, which is within each blade.

1.4 Enterprise Commercial Servers

The current server market is divided among many competitors—the three dominate competitors being International Business Machine (IBM), Hewlett-Packard (HP), and Dell. IBM and HP offer the most technologically advanced servers. In 2012, these three server powerhouses combined for \$38,062,000,000 in revenue, 74.2% of the world’s market share. Several other competitors such as Oracle, Fujitsu, Hitachi, Cisco, Lenovo, Intel, Acer, Cray, and others compete for the remaining 25.8% of the world server market [12][13]. Fig. 1.4 reveals the world’s server market share in more detail.

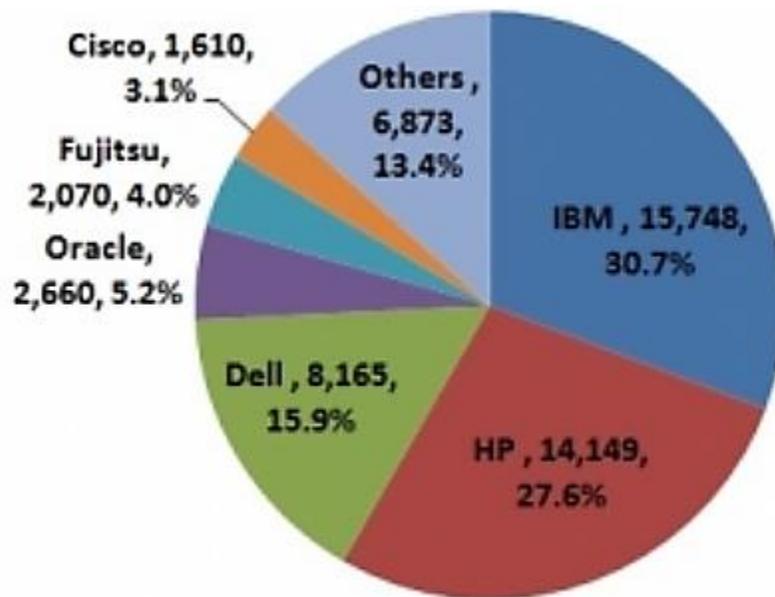


Fig. 1.4: Worldwide sever revenue in 2012
(Revenue in Millions of US dollars) [12].

1.4.1 HP Server Overview

The power architecture of HP servers is not particularly advanced. HP’s primary advantage is the use of Intel’s Xeon processors that offer up to 18 internal cores, the use of DDR 4 HP 2.433 GHz Smart Memory, high I/O throughput, and a new generation of processor power

management that reduces power consumption and increases processor efficiency by 36% compared to earlier Intel processors. With the pinnacle in high performance Intel processors most commonly operating on the LINEX platform, HP is a serious competitor in the server industry [14].

1.4.2 IBM Server Overview

IBM offers many server solutions from the System X and System Z, which are largely commercial products, to the Power Systems that are Enterprise grade and research level frames. The Power 775 server from IBM, for example, is a “massive scale-out high performance computing (HPC) server that provides unparalleled capacity that’s been optimized for running large, highly parallel computationally-intensive workloads and algorithms” [10]. The Power Systems utilize IBM’s POWER8 processors that feature 4 GHz operating frequency, 12 cores per processor with 8 hardware threads per core for 96 threads of parallel execution, are built on 22 nm technology, and can operate on the UNIX, LINEX, or AIX platforms. IBM’s processors are impressive but still second to Intel.

Where the Power 775 server shines is its unmatched power capability and power density, unmatched parallel computational ability, and unmatched compute power per rack. The Power 775 is water-cooled, capable of 360 kW of power conversion (four times that of most competitors), and can be equipped with 3,072 cores in a single frame. Therefore, a Power 775 server equipped with POWER8 processors could operate at up to 4.3 petaflops, which is 4.3×10^{15} floating-point calculations per second (flops). This compute power per rack is enabled by advanced power conversion systems, which is easily the most advanced power conversion hardware available in a commercial product.

1.4.3 IBM Power Conversion and Packaging

The IBM Power 775 offers a 350 V DC distribution and a three-stage power conversion system with sub-assemblies, all of which are located on the rack. The first system is the bulk power regulator (BPR), which is the equivalent of a FER on some systems. The BPR converter works with either of the following inputs: 380-520 V DC or 200-480 V 3 ϕ AC (no neutral). The output of the BPR is the 350 V distributed bus. Each BPR operates up to 90 kW, and there are up to four BPRs per rack. The BPR contains three sub-assemblies summarized in Fig. 1.5 and Fig. 1.6. The rectifier converts three-phase AC power to three phases of a rectified sinusoid by means of a three phase silicon controlled rectifier (SCR) bridge. The BPR utilizes a buck-boost power factor correction (PFC) circuit. Buck-boost PFCs are preferred to boost PFCs because they allow a wider input voltage range. The PFC circuit operates in boost mode when the rectified waveform is below 410 V and operates in buck mode when the rectified waveform is above 410 V. The 410 V DC is converted to 350 V DC through an isolated DC-DC converter. This final stage within the BPR provides voltage regulation and DC isolation for safety.

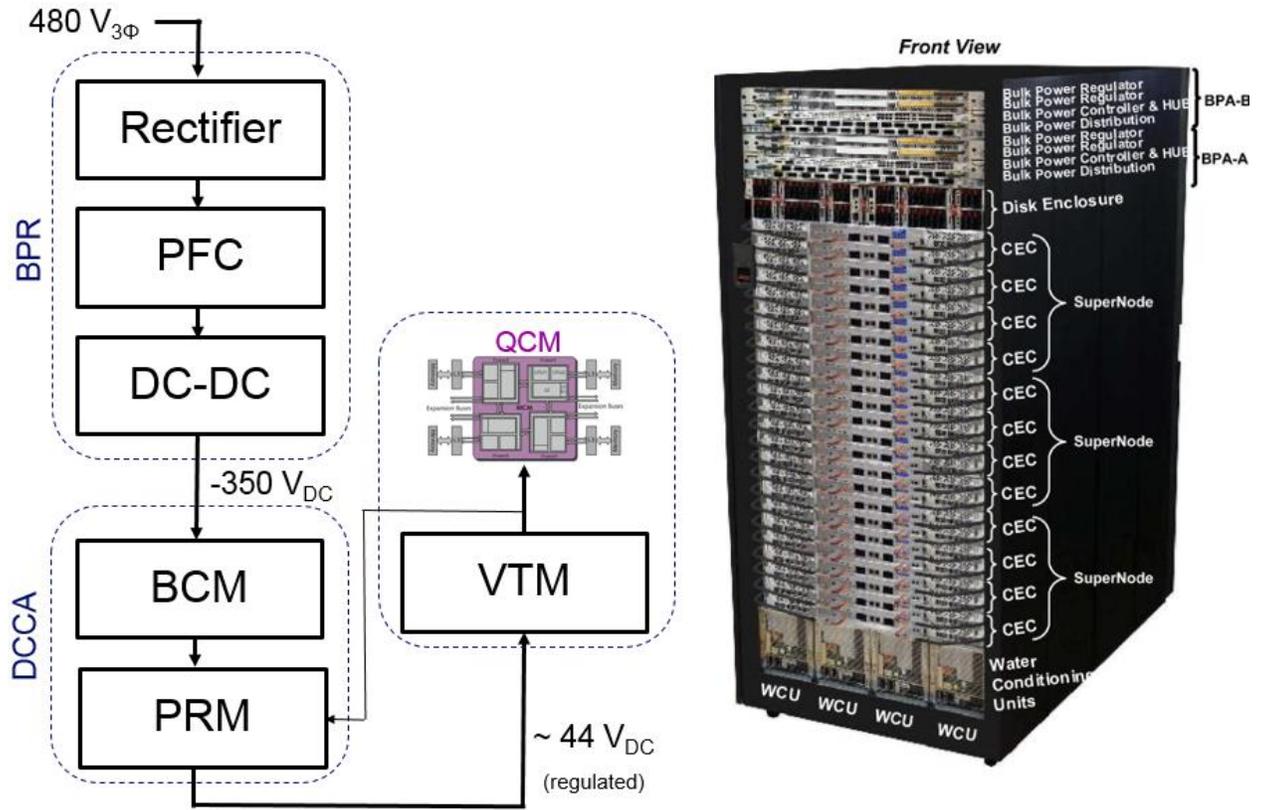


Fig. 1.5: IBM Power 775 power conversion architecture.

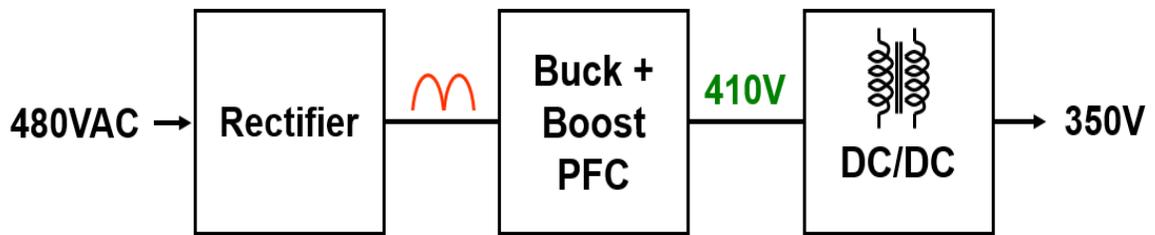


Fig. 1.6: BPR sub-assembly overview (rectifier + PFC + DC-DC) [15].

After the BPR, a system called the distributed converter and control assembly (DCCA), which is similar to the IBC from section 1.3, converts 350 V DC to a regulated voltage around 44 V DC that proceeds to the POL located next to the processor. Each DCCA has 61 regulated voltages on the output that combine for 17,500 W. The DCCA utilizes Vicor VI chip sets. The

Vicor bulk converter module (BCM) and pre-regulator module (PRM) are located on the DCCA, and the voltage transformation module (VTM), an unregulated form of a POL, is located on the motherboard near the load. This power conversion architecture has enabled vast increases in power density over previous designs, it is the most advanced server from a power aspect on the commercial market but is only available in large orders to select customers, and it has influenced the purposed wide-bandgap topology in this work [15].

1.5 Point of Load Overview

Data center power supply chains usually have three or more power conversion stages (e.g. a FER, IBC, and POL); many systems have additional stages to create a DC voltage large enough for batter backups. Of these power conversion stages, FERs demonstrate typical efficiencies of 88-92%; IBCs will demonstrate similar efficiencies of 90-92%, and the POL is often much less efficient—usually between 80 and 85% with an exceptional few above 85% in ideal operating conditions. The POL sustains the greatest percentage loss due to high conduction loss and the lowest output power per POL module. Efficiency is calculated by

$$\%Eff = \frac{P_{OUT}}{P_{IN}} = \frac{P_{IN} - P_{LOSS}}{P_{IN}}, \quad (1.1)$$

where

$$P_{LOSS} = P_{CONDUCTION} + P_{SWITCHING} + P_{GATE\ DRIVE} + P_{MAGNETIC} + P_{ESR} \dots \quad (1.2)$$

The POL converter operates at the lowest input power, P_{IN} , of the conversion stages, and the power loss is particularly high due primarily to conduction loss, switching loss, and magnetic loss. Therefore, the large negative term in the numerator and comparatively small denominator force the POL converter efficiency to be lower than the other conversion stages, at least in modern commercial systems [7][9].

Typical efficiencies of commercial state-of-the-art low-voltage POLs are approximately 80% to 88% at most [16]-[19]. However, some of these POL converters have unregulated outputs and will incur additional loss to regulate their outputs. Some research publications in WBG POL converters have documented high eighty to low ninety percent efficiencies [20]-[22]. However, enhancement-mode (E-mode) Gallium Nitride (GaN) FETs are a young technology and are not yet available with on-resistances as low as some mature Silicon (Si) MOSFETs. Thus, many GaN-based power supplies are limited by high on-resistance, while Si-based systems are limited by slow switching speeds [23]. Neither system is ideal and is thus limited in efficiency. High on-resistance in the commercially available GaN FETs makes it difficult to design a POL converter to operate at high operating currents (over 100 A). The increased energy cost of POL converters can be detrimental to large scale operations, such as data centers. POL converters are usually located very close to the load to reduce conduction loss between the POL and the load, and losses near the load generate additional heat that requires additional cooling efforts [24]. It is estimated that for every 1 W of loss at the POL, an additional 1 W is dissipated by the previous conversion stages to get that power to the POL, and there is an additional 1 W required to remove the additional heat from the system [8]. Therefore, every 1 W saved in POL efficiency improvements results in up to 3 W of power savings, and the POL yields high economical return. In other applications, such as portable electronics and telecommunications systems, poor POL efficiency can drastically reduce battery life, and battery life has become one of the greatest short-comings of today's technology [25]. WBG electronics enable smaller size that can eliminate the power brick used to charge a computer, reduce cell phone size and weight, and much more. Thus, POL efficiency and size are vital in a variety of applications. The application in this work is simply directed towards data centers, HPC, and similar applications that consume large quantities of power.

1.6 Common Point of Load Topologies

The two most common topologies applied to low-voltage POL converters are the LLC resonant converter and the synchronous buck converter (represented in Fig. 1.7, Fig. 1.8 and compared in Table 1.1). The major advantage to employing an LLC resonant converter is achieving fast transient performance. The synchronous buck converter offers a fully regulated output, superior efficiency, and good performance over a large load range.

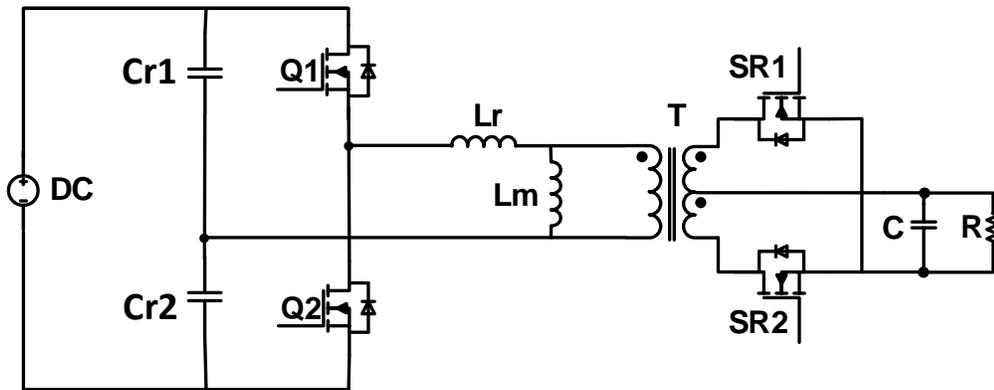


Fig. 1.7: LLC resonant converter topology.

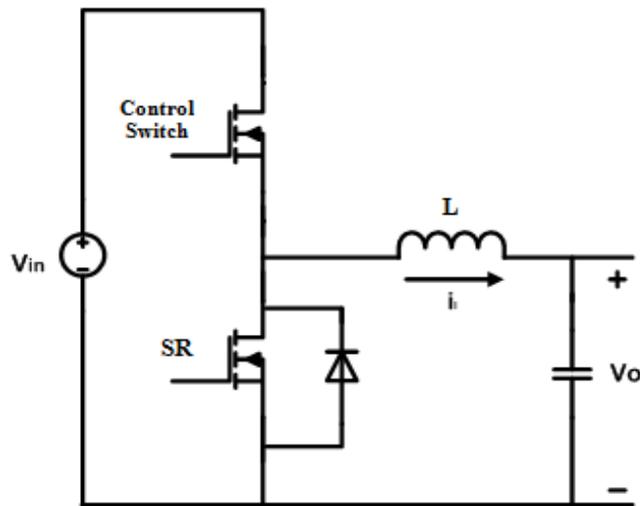


Fig. 1.8: Synchronous buck converter topology.

Table 1.1: LLC resonant and synchronous buck converter comparison.

	DC Isolation	Efficiency	Performance Over Load Range	Well Regulated Output
LLC Resonant	✓	✓	✗	✗
Synchronous Buck	✗	✓	✓	✓

In the synchronous buck converter, the smaller the ratio V_{OUT}/V_{IN} , the smaller the duty cycle and more free-wheeling current that circulates through the synchronous rectifier (SR) (see Fig. 1.8) [26], and large currents in the SR lead to significant conduction loss. With the application of E-mode GaN (eGaN) high electron mobility transistors (HEMTs), a term interchangeable with heterostructure field effect transistor (HFET), fast switching and reasonably low $R_{DS(ON)}$ reduces transistor loss compared to Si MOSFETs, according to [20][27]-[29]. However, due to limitations in $R_{DS(ON)}$, parallel GaN FETs are often required in the SR of the synchronous buck converter to achieve desirable high load efficiency. Adding parallel FETs increases gate charge, which slows the switching speed of the device(s). For this application, the control switch does not conduct current for as long as the SR; thus, a single eGaN FET is acceptable in the control switch and results in fast switching with only minor sacrifice in conduction loss. Overall, the synchronous buck converter offers many favorable characteristics, and a multiphase buck converter can achieve higher load requirements while reducing output ripple. If efficiency is high in design priority, the synchronous buck converter is a popular choice among power supply designers.

1.7 State-of-the-Art Commercial POL Converters

State-of-the-art commercial off the shelf (COTS) POL converters are primarily Si-based and 12-to-1 V DC-DC conversion efficiencies typically range from 80-88%, some of which are

unregulated converters and require additional regulators to maintain proper output voltage. The following are some of the best commercial POL competitors and their performance at 12-to-1 V power conversion:

- Vicor (86%, 100 A)
- Intersil (86%, 18 A)
- International Rectifier (88%, 15 A)
- Picor (88%, 8 A)
- Enpirion (85%, 2 A)

Some of these POLs are unregulated, and efficiency decreases by adding voltage regulation. By comparison, Si-based POL converters are limited by slow switching, which limits operating frequency, limits efficiency, and requires significant space to accommodate larger Si transistors and large passives. Of the COTS POL converters, the Vicor product is the only one that operates at high enough load currents to supply high performance processors, which often demand 100 to 200 A at 0.9 to 1.2 V. Vicor is the fundamental building block for the impressive IBM powertrain presented in Section 1.4.3.

WBG devices, such as GaN and Silicon Carbide (SiC), offer superior characteristics to Si. GaN devices are well suited for low-voltage applications and are recently (since 2009) available as E-mode power field effect transistors. E-mode transistors are preferred to depletion-mode (D-mode) transistors because they are normally off devices and the drive circuit can be simplified as a result. Fast switching and small size enables higher efficiency and greater power density. The objective of this research is to push the boundaries of WBG power devices to greatly improve power conversion efficiency while providing reliable products with superior output characteristics, fast transient response, and high power density.

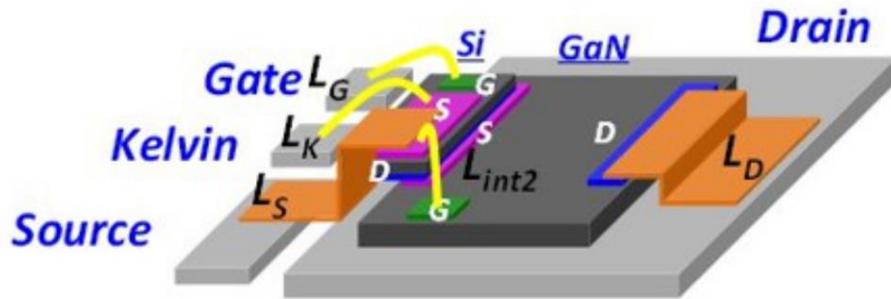


Fig. 1.10: Cascode GaN transistor die attach [31].

When true eGaN FETs were introduced in 2009 by Efficient Power Conversion Corporation (EPC), many organizations began to research and experiment with the fast-switching eGaN FETs and how they could be implemented in power electronic applications. Since the best commercial POL converters operating from 12-to-1 V have conversion efficiencies of 80-88%, simply breaking the 90% efficiency barrier has been considered a very reputable accomplishment, which only a few have achieved [30]. Although many authors have attempted this task, most do not reach 90% efficiency, see [20][30]-[37].

When implementing eGaN FETs, the ability to switch rapidly allows improvements in efficiency or reduction in size. A research group from Virginia Technological University's Center for Power Electronics Systems (CPES), in conjunction with EPC application engineers, have developed and published several non-isolated POL converters that reach low 90% efficiencies while making improvements in POL size and power density. The CPES group is leading the way in high power density, low-voltage POL converters. Three generations of the POL converters are presented in Fig. 1.11, and their efficiency analysis is shown in Fig. 1.12 & 1.13.

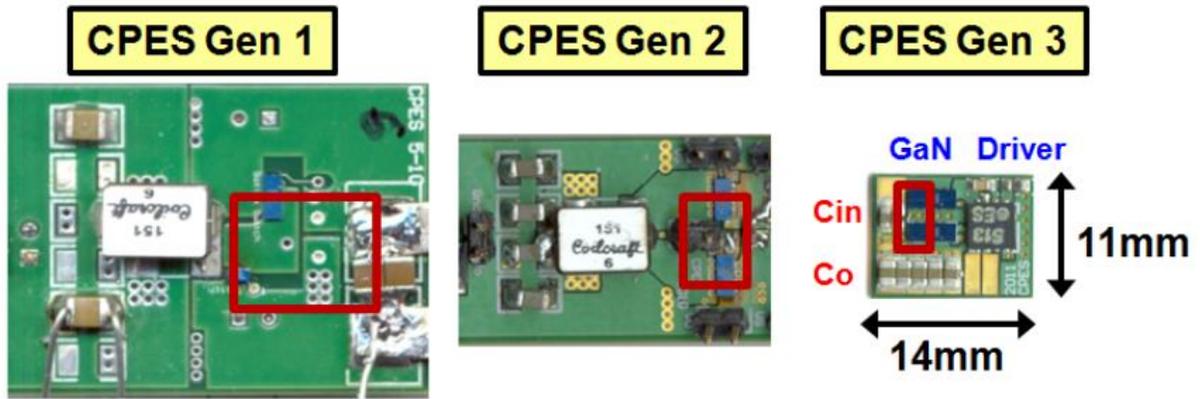


Fig. 1.11: Three generations of CPES synchronous buck converters [22].

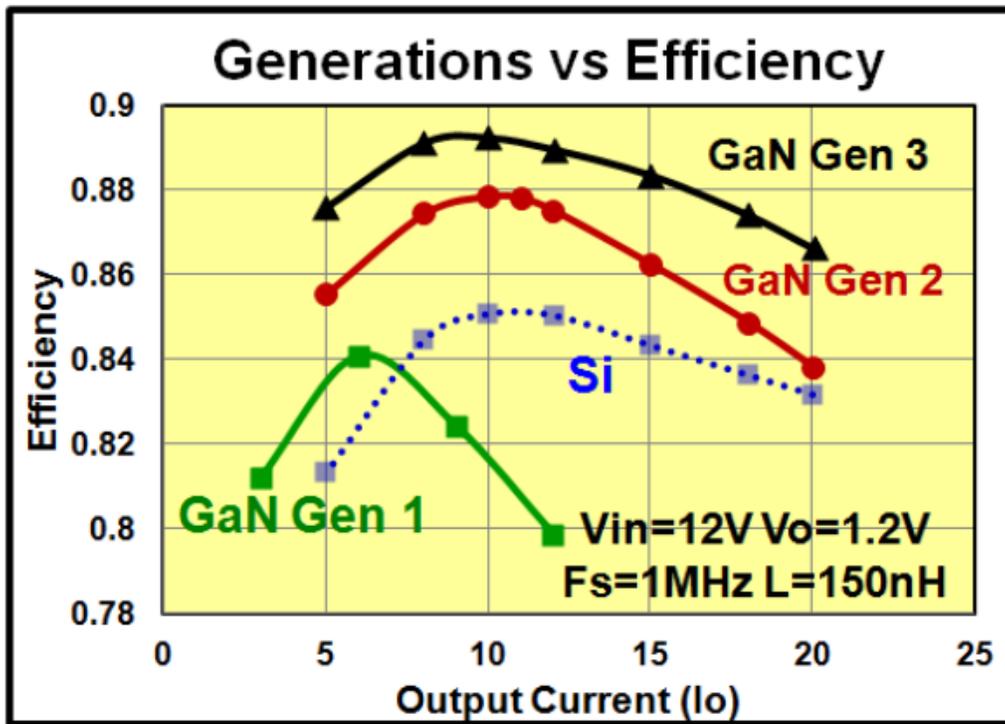


Fig. 1.12: Efficiency of CPES' GaN and Si POL prototypes [22].

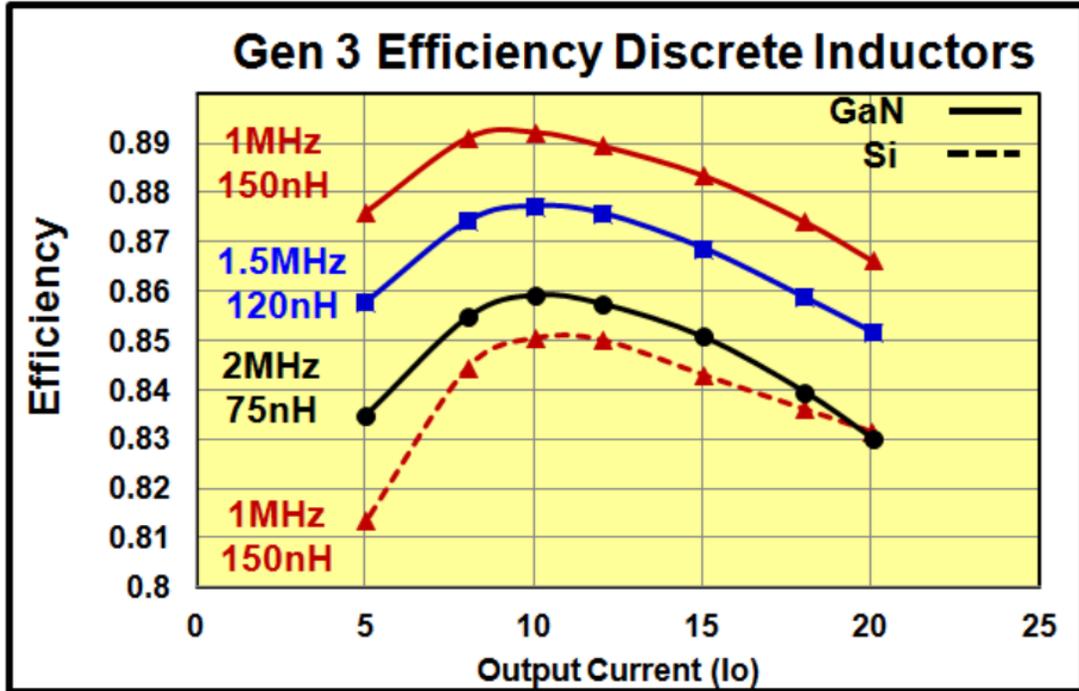


Fig. 1.13: Efficiency of CPES' GaN and Si POL prototypes at multiple frequencies [22].

These prototypes may be capable of over 90% efficiency if switching frequency was reduced and larger magnetic components were applied to the design; however, this design still does not achieve remarkably high output current. Many modern loads require at or above 100 A. Few authors are working on GaN-based POL converters with the highest priority placed on efficiency and most authors are unsuccessful in achieving significantly higher than 90% efficiency. Therefore, this work is unique as the final prototypes operate in excess of 100 A and well above 90% efficiency.

CHAPTER 2

BUCK (STEP-DOWN) CONVERTERS

2.1 Overview

The buck or step-down converter is one of the most fundamental SMPS. In ideal operation, it has only two basic states: when the control switch is on and when the control switch is off. To understand the buck converter, consider the schematic and output waveform presented in Fig. 2.1. When the control switch is closed, the input voltage is connected to the output directly. When the control switch is open, the output voltage returns to zero (ground). By alternating states, the average output voltage at the output, V_{AVG} , can be adjusted as a ratio of the two states. For this reason, in continuous-conduction mode (CCM), the duty cycle, D , and output voltage, V_{OUT} , can be defined as

$$D = \frac{\tau_{ON}}{T} \quad (2.1)$$

$$V_{OUT} = D \cdot V_{IN} , \quad (2.2)$$

where τ_{ON} is the time interval that the control switch is on and T is the period. A low-pass filter is then applied to the output to average the output voltage and provide a near DC output. The allowable ripple governs the filter design.

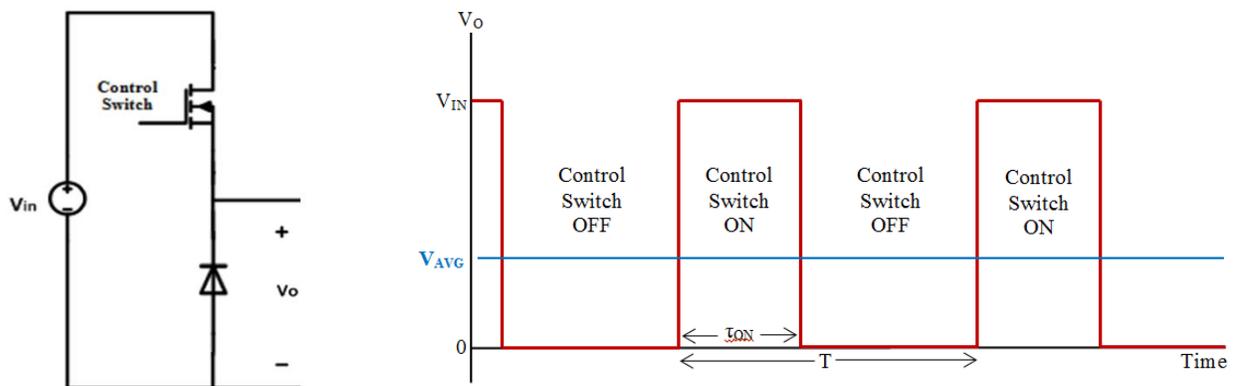


Fig. 2.1: Simplified buck converter without filter (left) and output voltage waveform (right).

Applying a low-pass filter and inserting a load results in the generic buck converter topology (see Fig. 2.2). During the first of two states (control switch on), current flows in the direction indicated in Fig. 2.3, and the input supplies current to the load and charges the inductor. During the second state (control switch off), the input is removed from the circuit, and the inductor maintains current at the output to supply the load (Fig. 2.4). During this second state, current circulates through the diode and is referred to as freewheeling current.

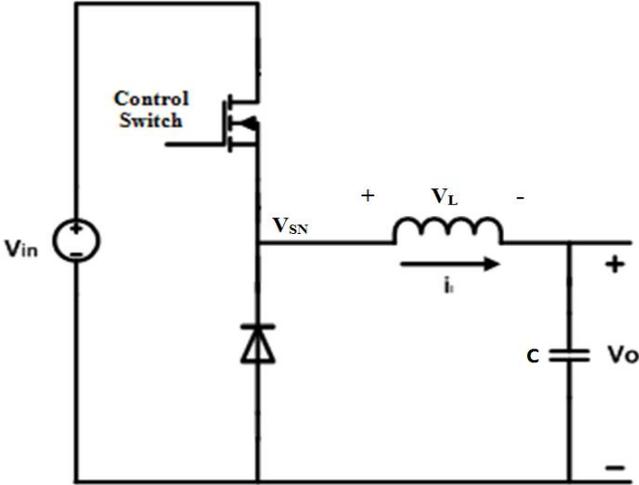


Fig. 2.2: Buck converter topology.

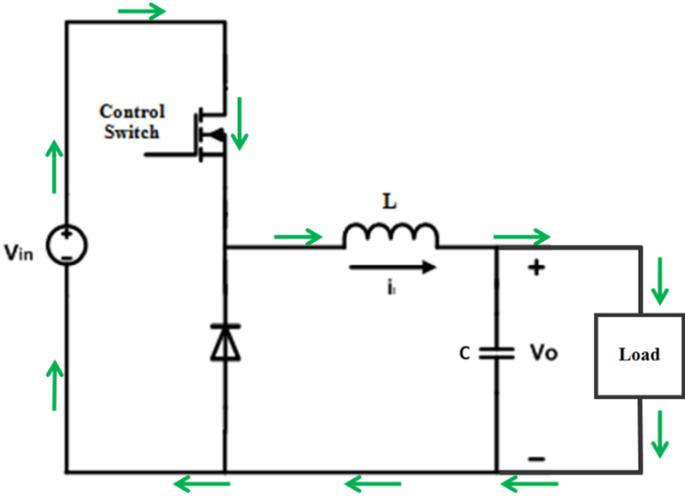


Fig. 2.3: Buck converter with control switch on.

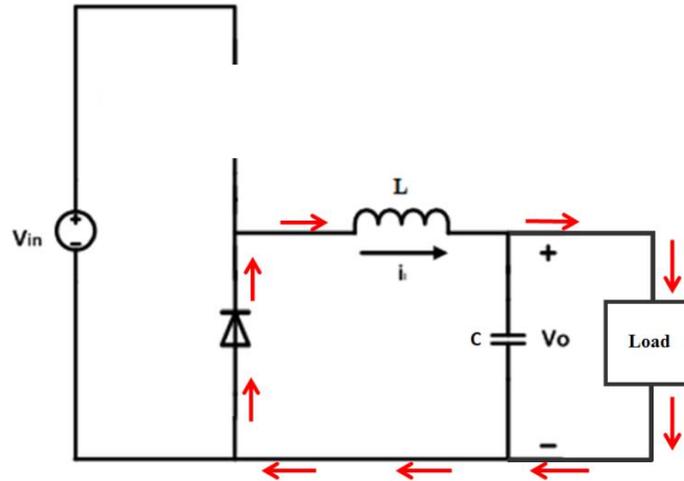


Fig. 2.4: Buck converter with control switch off.

The switch-node voltage is defined as the voltage between the control switch and diode. The instantaneous switch-node voltage (V_{SN}), inductor current (i_L), inductor voltage (V_L), and input current (i_{IN}) are depicted in Fig. 2.5. When the control switch is on, the switch-node voltage is at the input voltage minus the forward voltage drop of the control switch. At this point, the input is charging the inductor, which creates a positive voltage across the inductor (V_L orientation shown in Fig. 2.2), and the input current is equal to the inductor current. During the next state, when the control switch is off, the switch-node voltage is slightly below ground, due to the forward bias voltage drop of the diode. The inductor has a negative voltage and thus the inductor current is decreasing. At this time, the input is not providing any power to the network. These two states continue to repeat as indicated in Fig. 2.5.

Based on the switching frequency, design of the low-pass filter, and load current, there are three basic operating states of the buck, or step-down, converter: continuous-conduction mode (CCM), discontinuous-conduction mode (DCM), and critical-conduction mode. CCM occurs when the inductor current is always positive, such as the case in Fig. 2.5. In DCM, the inductor

current becomes zero for a finite length of time, and critical-conduction operation refers to the boundary between CCM and DCM, where the inductor current reaches zero but does not remain at zero for any finite length of time. In other words, inductor current, i_L , immediately begins to increase again once reaching zero. Each operating state is governed by a different set of equations. Therefore, the design process changes based on the operating state.

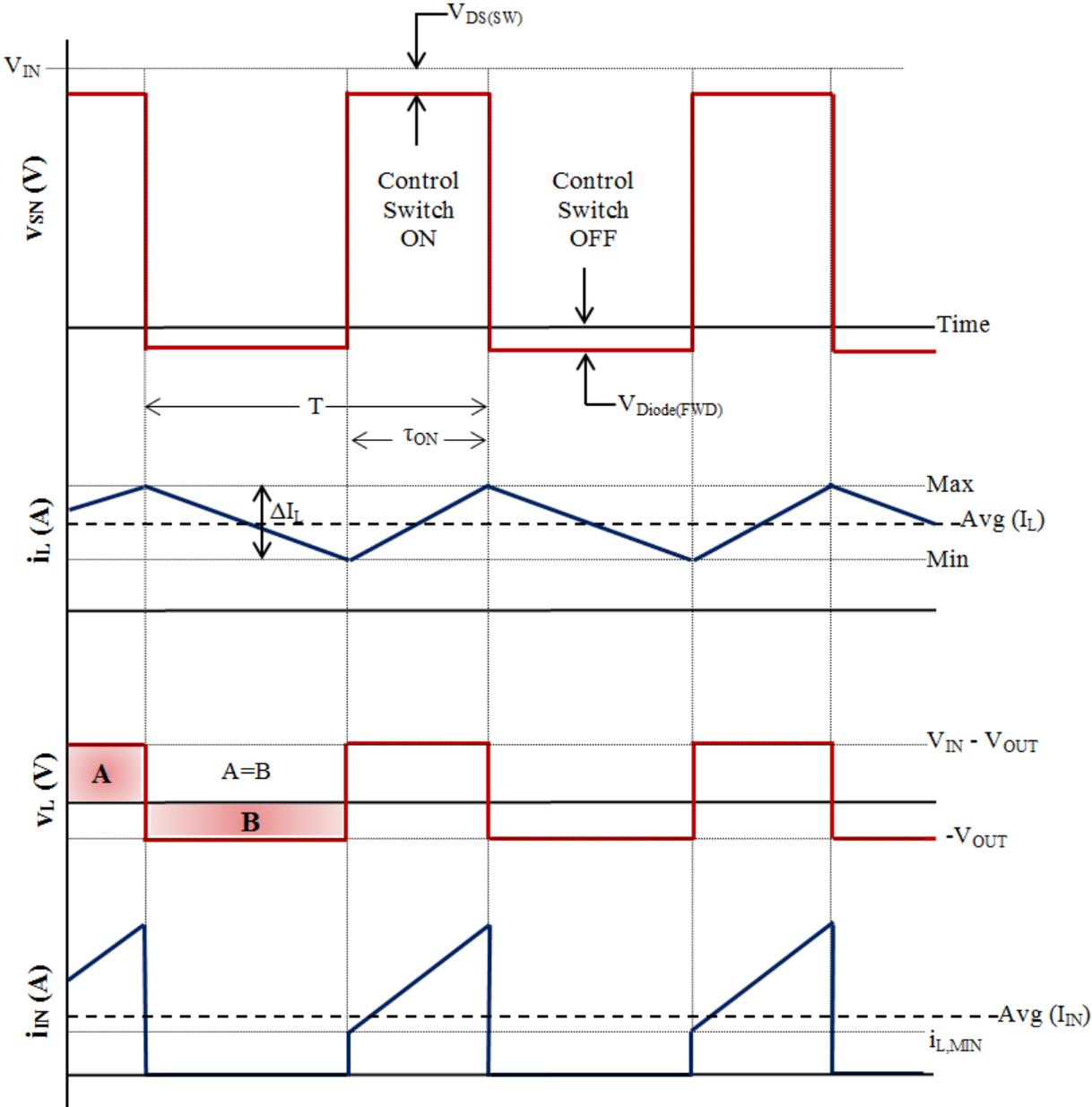


Fig. 2.5: Buck converter steady-state analysis in CCM.

2.2 Continuous-Conduction Mode

CCM is the most common operating state for battery chargers and DC power supplies where a DC voltage with minimal ripple is desired. As defined previously, the duty ratio or duty cycle is the ratio of control switch on-time (τ_{ON}) and the switching period (T), which defines the ratio of input voltage to output voltage in CCM for a lossless system as

$$D = \frac{\tau_{ON}}{T} = \frac{V_O}{V_{IN}} . \quad (2.3)$$

In a lossless or ideal case, power is conserved and the duty ratio can also be defined as a ratio of the input and output current as seen in Eq. 2.6.

$$P_{IN} = P_{OUT} \quad (2.4)$$

$$V_{IN} \cdot I_{IN} = V_{OUT} \cdot I_{OUT} \quad (2.5)$$

Therefore,

$$D = \frac{V_{OUT}}{V_{IN}} = \frac{I_{IN}}{I_{OUT}} . \quad (2.6)$$

To design a system in CCM with an allowable current ripple (ΔI_L), the inductance and switching frequency must be designed properly based on the input voltage and duty cycle. Given that

$$f = 1/T , \quad (2.7)$$

the following relationship can be established:

$$L = \frac{D V_{IN} (1-D)}{f \cdot \Delta I_L} , \quad (2.8)$$

indicating that as frequency is increased, inductance can be decreased without increasing ΔI_L . ΔI_L is a design constraint based on the tolerance of the load to handle non-ideal DC current. By rearranging (2.8), the output current ripple can be determined for a system in steady-state as

$$\Delta I_L = \frac{V_{OUT} (1-D)}{L \cdot f} . \quad (2.9)$$

Additionally, capacitance is also used to filter the output and therefore depends on frequency, inductance, and allowable output voltage ripple. Large output capacitance is imperative to keeping low output voltage ripple during steady-state operation and preventing large voltage spikes and drops during transient response. In steady-state, output capacitance is determined by

$$C = \frac{D V_{IN} (1-D)}{8f \cdot L \cdot \Delta V_{OUT}} \quad (2.10)$$

Increasing output capacitance will reduce the voltage drop or spike during an increase or decrease in load. However, higher output capacitance also increases the amount of time for the output to recover to its desired voltage after a load transient. Thus, output capacitance, C , is not solely determined by steady-state operation but also by transient performance.

System design before simulation and operation provides a starting point; however, many of these equations are idealized and neglect losses. Losses are seen as voltage drops across components in the circuit and appear as voltage drops at the output as well. For this reason, in a practical system, the duty cycle must be increased to compensate for output voltage drop; thus,

$$D > \frac{V_O}{V_{IN}} \quad (2.11)$$

for practical systems.

2.3 Discontinuous-Conduction Mode

DCM is common in applications such as DC motor speed control, where V_{IN} remains relatively constant and V_{OUT} is adjusted to influence motor speed. However, it is not imperative to maintain output current, so the inductor current, i_L , is allowed to remain at zero for a period of time. Since i_L is not continuously flowing, this state is called discontinuous-conduction mode. As seen in Fig. 2.6, there is a period of discontinuation in the inductor current during DCM.

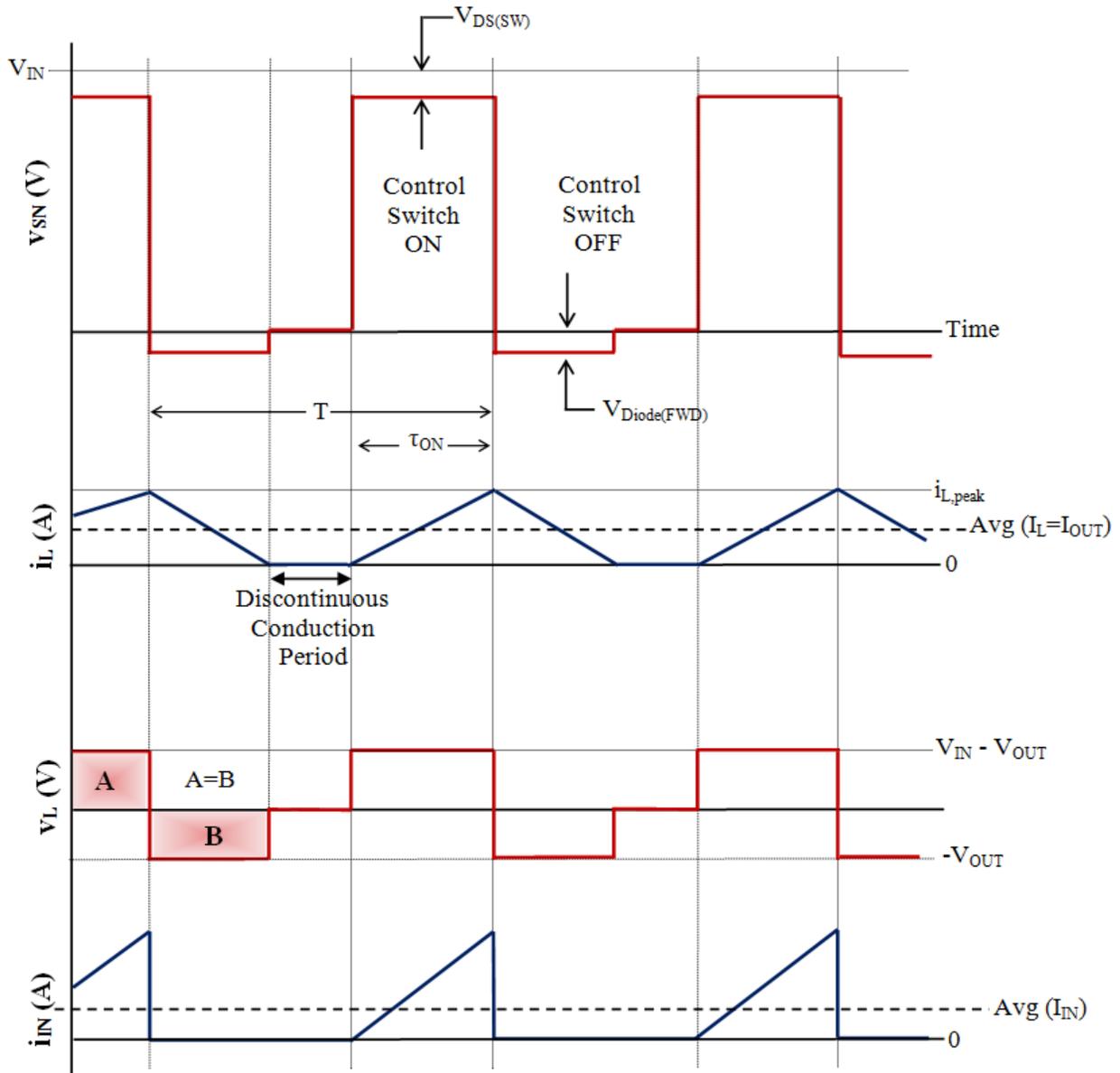


Fig. 2.6: Buck converter steady-state analysis in DCM.

The governing equations in DCM are different from CCM and are often written in terms of a variable K , defined as

$$K = \frac{2L \cdot f}{R}, \quad (2.12)$$

where R is the resistive load and assumed to be purely resistive. In DCM, the duty cycle is not the ratio of the output voltage over the input voltage. Rather, duty cycle is defined as

$$D = \sqrt{\frac{4K}{\left(2\frac{V_{IN}}{V_{OUT}}-1\right)^2-1}}, \quad (2.13)$$

and the voltage gain is defined as

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{2}{\left(1 + \sqrt{1 + \frac{4K}{D^2}}\right)} \quad (2.14)$$

or can be written as

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{1}{\left(1 + \frac{2I_L^2 \cdot L \cdot f}{V_{IN} \cdot D}\right)}. \quad (2.15)$$

Because increased inductance reduces the inductor current rate of change, $\frac{di_L}{dt}$, since

$$V_L = L \cdot \frac{di_L}{dt}, \quad (2.16)$$

V_L is unchanged, and increased frequency reduces the time that the inductor current is able to rise or fall, the maximum inductor current ($I_{L,max}$) is inversely proportional to inductance and frequency. The maximum inductor current, which is approximately the maximum output current, can be determined by

$$I_{L,max} = \frac{(V_{IN}-V_{OUT})D}{L \cdot f}. \quad (2.18)$$

Most buck converters are designed to operate in CCM or DCM but not often are they designed to switch between operating modes. Both modes have particular applications, and due to the discontinuity in inductor current, the governing equations are different.

2.4 Critical-Conduction Mode

Critical-conduction mode is the boundary between CCM and DCM, where the inductor current reaches zero but immediately begins to increase again. This operation is defined by the

same basic equations as CCM. As seen in Fig. 2.7, the voltage and current waveforms look very similar to that of Fig. 2.5. However,

$$i_{L,min} = i_{OUT,min} = i_{IN,min} = 0, \quad (2.19)$$

$$\begin{aligned} \Delta I_L &= i_{L,max} - i_{L,min} \\ &= i_{L,max} - 0 \\ &= i_{L,max}, \end{aligned} \quad (2.20)$$

and the average inductor current equals half the maximum inductor current,

$$I_L = \frac{1}{2} i_{L,max}. \quad (2.21)$$

It can be helpful to determine other characteristics of critical-conduction mode, such as critical inductance (L_{crit}), load resistance (R_{crit}), power (P_{crit}), inductor current ($I_{L,crit}$), and the variable K_{crit} . They are defined by the following equations and derived from general CCM equations while setting the average inductor current to half the maximum inductor current.

$$L_{crit} = \frac{R(1-D)}{2f} = \frac{V_{OUT}(1-D)}{2f \cdot I_{L,crit}} \quad (2.22)$$

$$R_{crit} = \frac{2L \cdot f}{(1-D)} \quad (2.23)$$

$$P_{crit} = \frac{V_{OUT}^2}{R_{crit}} = \frac{V_{OUT}^2(1-D)}{2L \cdot f} \quad (2.24)$$

and

$$I_{L,crit} = \frac{V_{OUT}(1-D)}{2L \cdot f}. \quad (2.25)$$

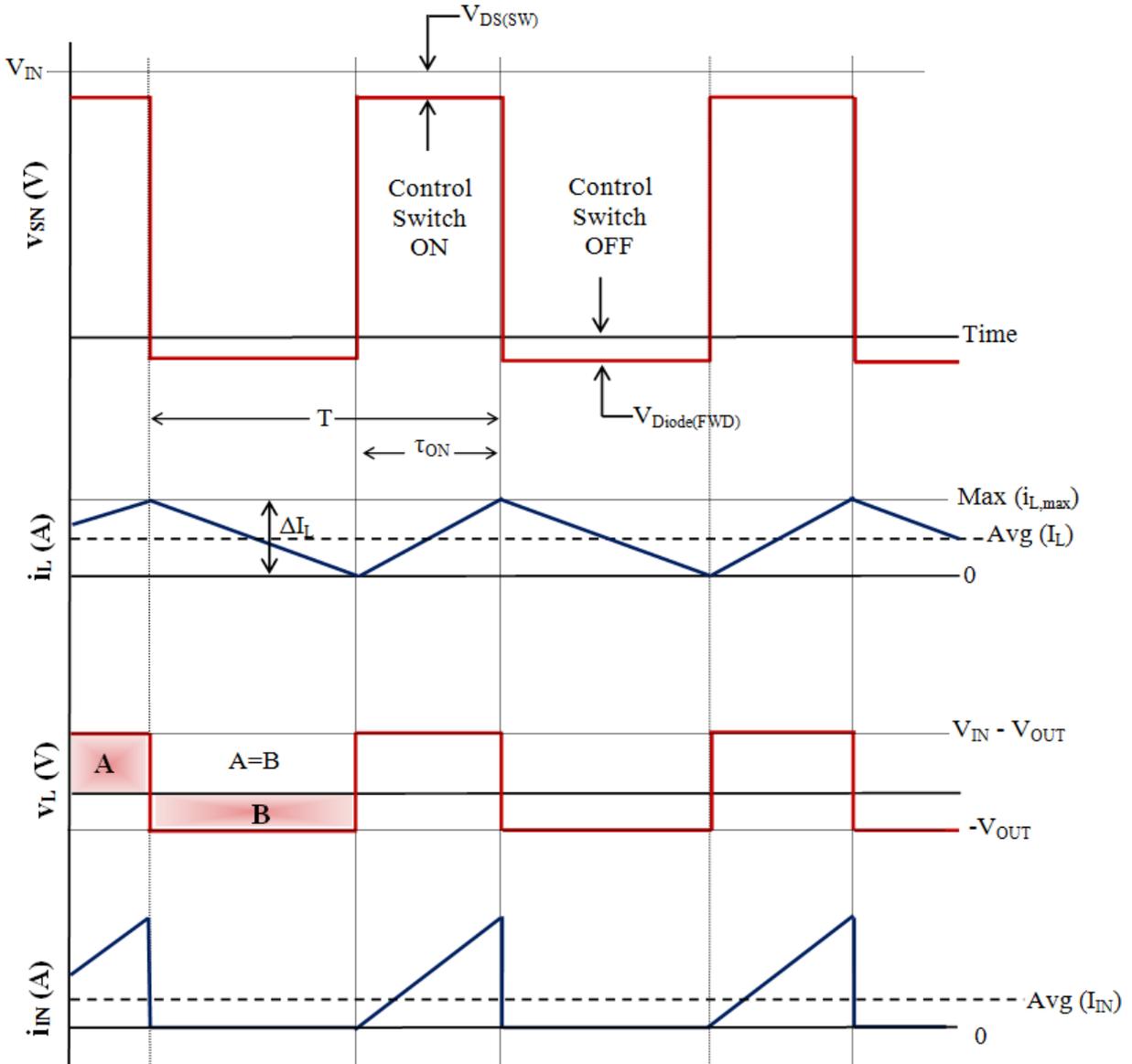


Fig. 2.7: Buck converter steady-state analysis in critical-conduction mode.

Most often, operation in critical-conduction mode is not the intent nor is it a practical system design. However, it is helpful to analyze the critical operating point to ensure the design stays in the desired operating state, CCM or DCM. For example, if $L > L_{crit}$, $R < R_{crit}$, $P > P_{crit}$, and $I_L > I_{L,crit}$, then the system will operate in CCM. If any one of these statements is true, the rest will also be true. Therefore, if any of the statements are false, the system will operate in critical-

conduction mode or DCM. This analysis of the boundary condition is useful for determining the mode of the buck converter operation.

2.5 Synchronous Buck Converters

The concept of synchronous buck converters is simply to replace the diode in the buck converter with a low drain-to-source on-resistance ($R_{DS(ON)}$) transistor, typically a MOSFET with body diode. The benefit to synchronous buck conversion is lower conduction loss due to the free-wheeling current. The transistor that replaces the diode will have a near constant $R_{DS(ON)}$, while the diode has a near constant voltage drop. For example, most Schottky diodes have approximately 0.5 V forward voltage drop. The two states of the synchronous buck converter are nearly identical to the asynchronous buck converter, and power flow during the two dominate states are shown in Fig. 2.8.

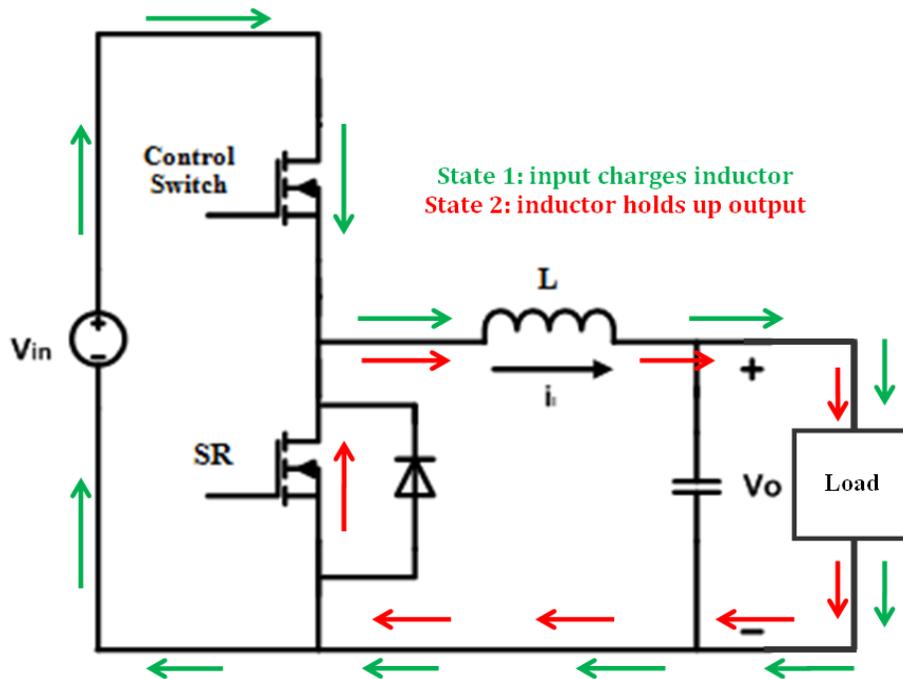


Fig. 2.8: Synchronous buck converter.

The synchronous buck converter results in some additional losses, such as transistor conduction loss, switching loss, and gate drive loss—calculated by the following, respectively:

$$P_{C,SR} = I_{OUT}^2 \cdot R_{DS(ON)} \cdot (1 - D) , \quad (2.26)$$

$$P_{SW} = \frac{1}{2} V_{IN} \cdot I_{OUT} \cdot (t_R + t_F) \cdot f , \quad (2.27)$$

where

$$t_R \approx t_F \approx \frac{Q_G}{I_G} + \frac{L_{LUMP} \cdot I_G}{V_{GS} - V_{TH}} , \quad (2.28)$$

and

$$P_G = Q_G \cdot V_{GS} \cdot f \cdot \left(\frac{R_{G_{sink}}}{R_{G_{sink}} + R_G + R_{GI}} + \frac{R_{G_{source}}}{R_{G_{source}} + R_G + R_{GI}} \right) . \quad (2.29)$$

The body diode, which is parallel to the MOSFET, still has reverse recovery losses and is necessary to avoid large voltage spikes across the inductor during switch dead-time. Dead-time is required to avoid shoot-through current from input to ground, which occurs if both FETs are on simultaneously, and properly controlling dead-time adds complexity to the system controller. It is ideal to minimize dead-time, since the diode must conduct during dead-time, which leads to losses governed by

$$P_D = V_F \cdot I_F \cdot \frac{t_D}{T} , \quad (2.30)$$

where V_F is the diode forward voltage drop (~ 0.5 V), I_F is the diode forward current, which is equal to the freewheeling current, t_D is the amount of time that the diode conducts each period, and T is the period.

Synchronous conversion is more common for low-voltage applications, as there is much more potential for efficiency improvements. Even with all the additional transistor losses, the sum of these losses are less than that of an asynchronous converter, whose diode forward voltage loss is defined by

$$P_D = V_F \cdot I_F \cdot (1 - D) . \quad (2.31)$$

This loss term can be catastrophic to a low-voltage POL converter. For example, consider a 24-to-1 V POL converter operating at 10 A load current. The resulting duty cycle is approximately

$$\begin{aligned} D &\approx \frac{V_{OUT}}{V_{IN}} \cdot C_L & (2.32) \\ &\approx \frac{1V}{24V} \cdot (1.1) \\ &= 0.0458 , \end{aligned}$$

where C_L is a loss coefficient. Power loss due to diode forward voltage drop is then

$$\begin{aligned} P_D &= V_F \cdot I_F \cdot (1 - D) \\ &= (0.5 V)(10 A)(1 - 0.0458) \\ &= 4.77 W . \end{aligned}$$

Considering that the total output power of this system is

$$\begin{aligned} P_{OUT} &= I_{OUT} \cdot V_{OUT} & (2.33) \\ &= (10 A)(1 V) \\ &= 10 W , \end{aligned}$$

The diode forward voltage loss alone accounts for nearly one third of the input power and limits the maximum efficiency as follows:

$$\begin{aligned} \%Eff &< \frac{P_{OUT}}{P_{OUT} + P_D} \times 100 & (2.34) \\ &< \frac{10 W}{(10 W + 4.77 W)} \times 100 \\ &< 67.7\% . \end{aligned}$$

This example demonstrates the importance of synchronous rectification, particularly at low voltages. Even with several additional loss terms from introducing an additional transistor to the

system, the efficiency improvements from the synchronous buck converter are well worth the added complexity to the design and control.

3.1 FET Selection

Until recently, power semiconductors were usually produced in TO, power-PAK, and D-PAK style packaging due to die size, thermal dissipation requirements, and the vertical flow of current through the devices. The introduction of GaN to power semiconductors has allowed manufactures to produce devices with approximately 9% the footprint of similar rated D-PAK Si MOSFETs. In addition, GaN semiconductors have much better theoretical limits of specific on-resistance to breakdown voltage, when compared to Si and SiC. The IR GaN is a cascode device from International Rectifier (IR) and the GaN HFET is an E-mode GaN FET from EPC; they are compared to device theoretical limits in Fig. 3.1. As of now, GaN devices offer very good performance at much less cost than SiC, very small footprints, no reverse recovery losses of a body diode, very low $R_{DS(ON)}$, and very fast turn-on and turn-off times due to Q_G in single-digit nC range. In the current market, GaN is generally the preferred WBG material at lower voltages (≤ 600 V), and SiC is the preferred WBG material at higher voltages (≥ 600 V). Since Si transistors originated in the 1950s, they have continued to improve in performance; however, since the start of the 21st century, Si transistor improvement has drastically slowed as Si approaches its theoretical limits. GaN transistors already outperform Si and are expected to make vast improvements over the next decade (see Fig. 3.2). GaN devices are very appealing in the design of high performance power electronics; unfortunately, this decrease in package size has made prototyping significantly more challenging. Traditional manual solder iron assembly is not sufficient for these devices. Difficulties include board design, device handling, alignment, solder reflow, flux residue removal, and post-assembly inspection. The EPC2014 and EPC2015 devices both have a 4mm pitch and

are 1.85 mm² and 6.70 mm², respectively. In many situations, the decreased pitch and small size of these devices mandate the use of automated assembly equipment, such as a pick & place, to ensure quality and repeatable assembly. However, this may not be feasible for initial prototyping, due to cost and time constraints. For more detail, a manual assembly process for these chip scale devices, applied specifically to the EPC2014 and EPC2015 is presented in Chapter 9. This process decreases the cost and turn time for prototype assembly when utilizing these types of chip scale packaged power semiconductors, making design prototyping a more rapid process.

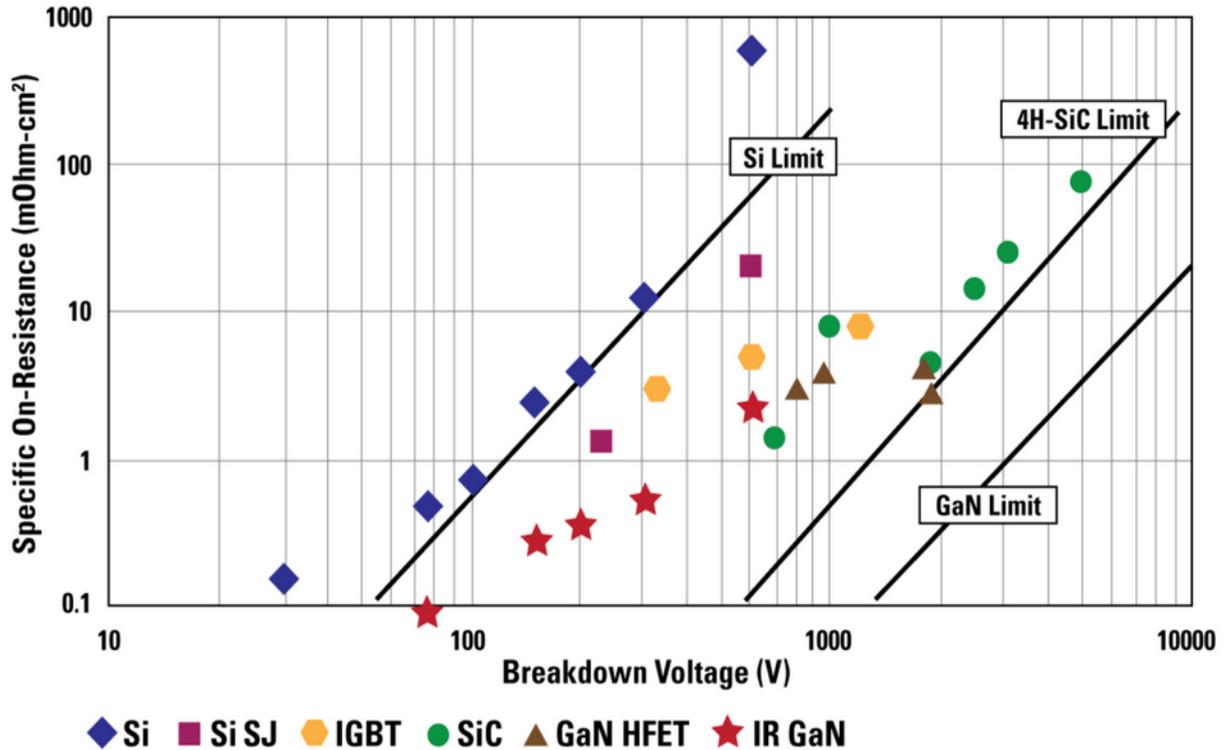


Fig. 3.1: Comparison of maximum theoretical on-resistance to breakdown voltage for Si, SiC, and GaN [32].

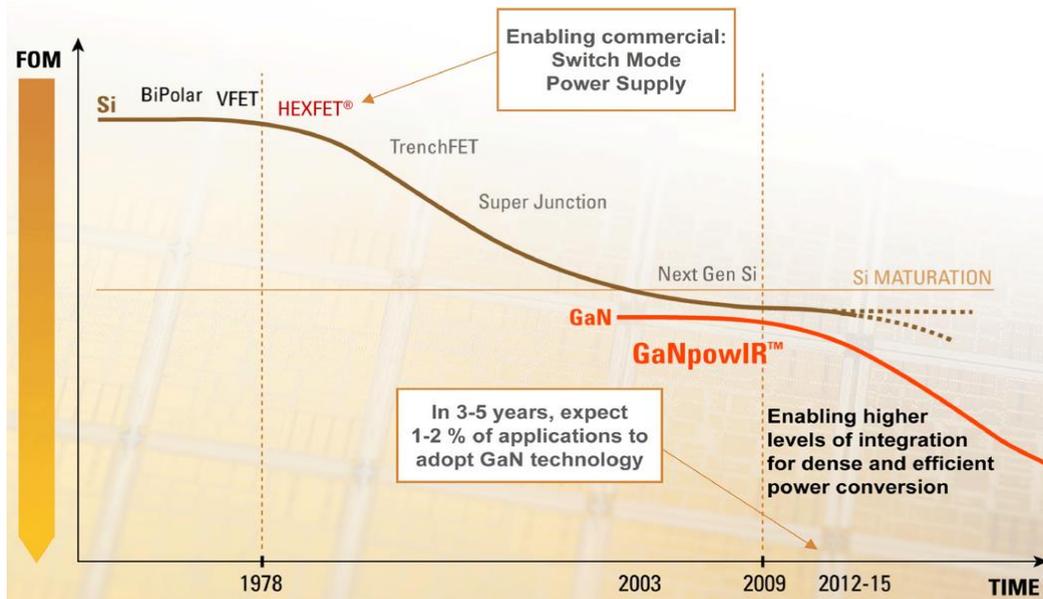


Fig. 3.2: Performance improvements with GaN as Si reaches maturation [33].

The EPC2015 was selected as the preferred GaN FET for the 12-to-1 V non-isolated POL converter, regardless of prototyping difficulties. These GaN FETs have significantly lower Q_G and C_{OSS} than other Si alternatives, thus resulting in faster switching and reduced switching loss; however, the $4\text{ m}\Omega$, 40 V_{DS} GaN FET has nearly four times the on-resistance of the best Si MOSFET alternative ($1.1\text{ m}\Omega$, 25 V_{DS} Infineon BSC010NE2LS). Both on-resistances were measured at $V_{GS} = 4.5\text{ V}$. With an approximate duty cycle of 9%, the higher on-resistance is not detrimental in the control switch. However, the SR is conducting for approximately 91% of the period in 12-to-1 V operation, and conduction losses are much greater. Studying parallel GaN FET performance helped determine how many GaN FETs should be in parallel to appropriately reduce equivalent $R_{DS(ON)}$ to balance conduction and switching losses for maximum efficiency over a large operating range [21]. For example, a single EPC2015 has $4\text{ m}\Omega$ $R_{DS(ON)}$ and 10.5 nC . If two EPC2015s are paralleled in the SR, they yield an equivalent on-resistance of $2\text{ m}\Omega$ and an equivalent gate charge of 21 nC . Thus, adding parallel devices will decrease on-resistance and

increase switching loss since the switching time is increased. Properly balancing these variables is key to optimizing design performance.

3.2 Parallel GaN HEMT Performance Analysis

The impact of parallel GaN HEMTs on efficiency of a non-isolated POL converter is investigated to analyze how additional parasitics and uneven current sharing impact the design. In this work, HEMT and HFET can both be used to describe the GaN devices and are thus interchangeable terms. Simulations alone do not adequately represent realistic performance using GaN HEMTs because parasitic inductances are on the same order of magnitude as the device inductance, and inductance increases switching time and loss; thus, this experiment was necessary to determine the impact of parallel GaN HEMTs.

The test results indicate how many parallel GaN HEMTs should be used to achieve maximum efficiency based on load conditions. Loss calculations and simulations provided initial direction, and ten POL converters were tested while only varying the number of parallel GaN HEMTs in the control switch and SR. The designs tested are summarized in Table 3.1. Each design was tested between 2.5 and 30 A output. Depending on application load and frequency, the optimal combination of GaN HEMTs can be derived from this data. Experimental results indicate that I_{OUT} above 19.5 A, two EPC2015 switches and four EPC2015 synchronous rectifiers (referred to as 2x2015/4x2015) minimizes loss. Below 19.5 A, a 1x2015/2x2015 HEMT combination minimizes loss. Results presented here should expedite the design process for future engineers seeking greater power supply efficiency with GaN transistors, and it provides novel test data over a large load spectrum, variety of frequencies, and ten combinations of GaN HEMTs in a 12-to-1 V non-isolated POL converter.

Table 3.1: Summary of POL converter designs to investigate parallel GaN HEMTs.

Converter Reference #	Parallel in switch	Parallel in SR
1	1 x 2014	1 x 2015
2		2 x 2015
3	1 x 2015	1 x 2015
4		2 x 2015
5		3 x 2015
6		4 x 2015
7	2 x 2015	1 x 2015
8		2 x 2015
9		3 x 2015
10		4 x 2015

3.2.1 Analysis

Gate charge times on-resistance ($Q_G \times R_{DS(ON)}$) is a figure of merit (FOM) that can be used to measure the overall performance of a FET or HEMT. With everything else constant, lowering $R_{DS(ON)}$ linearly reduces conduction loss, and lowering Q_G increases switching speed thus reducing switching loss. Therefore, operating load and frequency govern the optimal design. By placing HEMTs in parallel, the effective $R_{DS(ON)}$ is divided but Q_G is added; therefore, a trade-off between switching and conduction losses is presented. Calculating the conduction loss for the switch and SR is straightforward using Eq. 3.1 and 3.2, respectively.

$$P_{C,SW} = I_{out}^2 \cdot R_{DS(ON)} \cdot D \quad (3.1)$$

$$P_{C,SR} = I_{out}^2 \cdot R_{DS(ON)} \cdot (1 - D) \quad (3.2)$$

Calculating switching loss is more complex and must include gate charge loss (Eq. 3.3) and drain-to-source power loss (Eq. 3.4), where t_R and t_F are approximated by Eq. 3.5. Complete MOSFET loss models in [20][38][39] can be applied to GaN HEMTs with minor manipulation.

$$P_G = Q_G \cdot V_{GS} \cdot f \cdot \left(\frac{R_{G_{sink}}}{R_{G_{sink}} + R_G + R_{GI}} + \frac{R_{G_{source}}}{R_{G_{source}} + R_G + R_{GI}} \right). \quad (3.3)$$

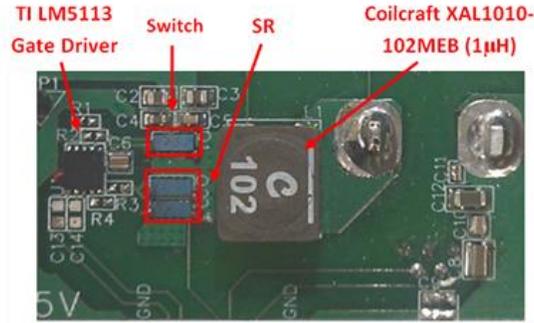
$$P_{SW} = \frac{1}{2} V_{IN} \cdot I_{OUT} \cdot (t_R + t_F) \cdot f, \quad (3.4)$$

$$t_R \approx t_F \approx \frac{Q_G}{I_G} + \frac{L_{LUMP} \cdot I_G}{V_{GS} - V_{TH}}, \quad (3.5)$$

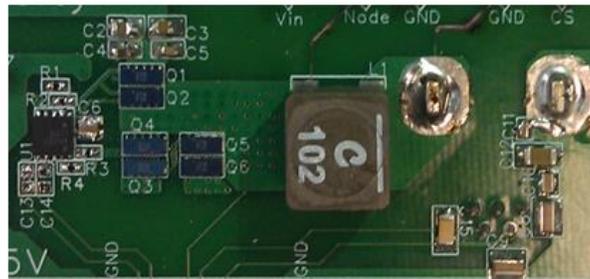
A summary of effective on-resistance, $R_{DS(ON),eff}$, and effective gate charge, $Q_{G,eff}$, is given in Table 3.2, and converters 4 and 10 from Table 3.1 are shown in Fig. 3.3. The GaN HEMTs were assembled using the manual assembly process presented by Henning et. al. [40].

Table 3.2: Effective on-resistance and gate charge of parallel HEMTs.

HEMTs	$R_{DS(ON),eff}$ (m Ω)	$Q_{g,eff}$ (nC)
2014	16	2.5
2015	4	10.5
2x2015	2	21
3x2015	1.33	31.5
4x2015	1	42



(a) Converter 4 (1x2015/2x2015)



(b) Converter 10 (2x2015/4x2015)

Fig. 3.3: Example POL converter prototypes.

3.2.2 Performance & Experimental Results

Converters 1 and 2, referring to Table 3.1, use the EPC2014 as the control switch. Both designs performed poorly overall, particularly at high load (see Fig. 3.4 – 3.5). In addition, reliable performance was not evident above 20 A, due to the I_D limitations of the EPC2014. The POL converters were air cooled with a 250 cfm high velocity fan during testing, but the current limit on GaN FETs is primarily due to thermal limitations.

Converter 2 adds an additional EPC2015 to the SR, and a drastic improvement is evident by its performance. This indicates that conduction losses are a significant source of loss in converter 1 which is often the case for low-voltage, high current applications.

Fig. 3.6 – 3.8 show converters 3, 4, and 10, respectively. Converter 3 (1x2015/1x2015), like converter 1 (1x2014/1x2015) has only one EPC2015 in the SR and is thus dominated by conduction losses. Performance suffers particularly at high load. Converter 4 (1x2015/2x2015) adds an additional parallel EPC2015 in the SR, which makes a significant improvement in performance. 92% peak efficiency is attained at 11 A. For loads below 15 A, this design results in significant improvement upon commercially available Si-based POL converters.

Converters 5 – 9 did not outperform converter 4. Converter 10 (2x2015/4x2015) does not reach peak efficiencies as high as converter 4; however, its efficiency does not decrease as rapidly with increasing load, a result of low conduction loss. Thus, converter 10 is the most efficient design at loads above 19.5 A.

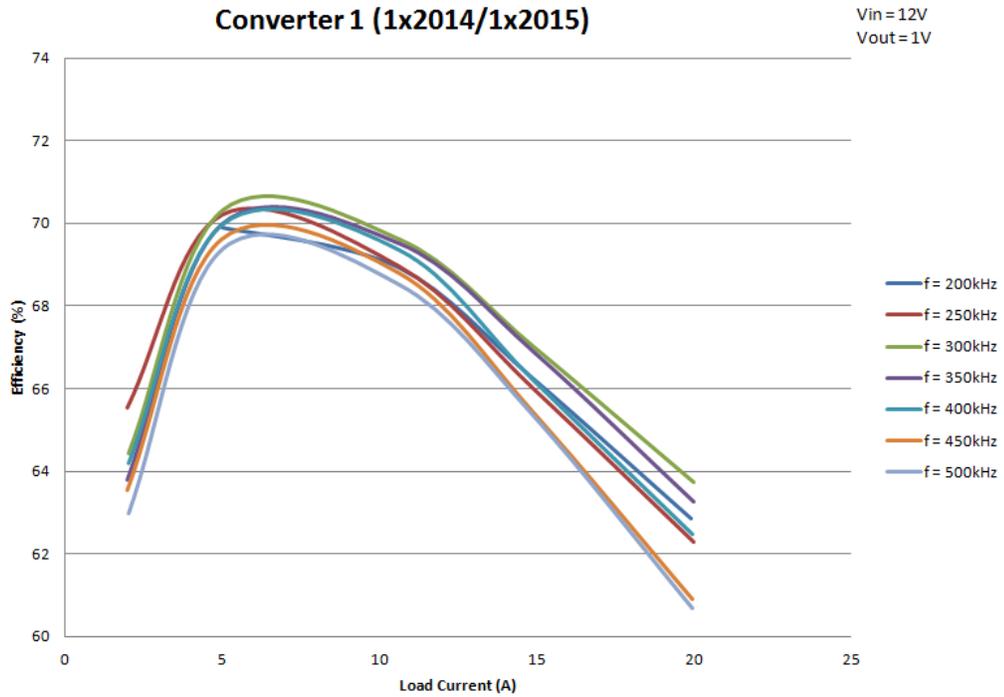


Fig. 3.4: Efficiency vs. load – converter 1 (referenced to Table 3.1).

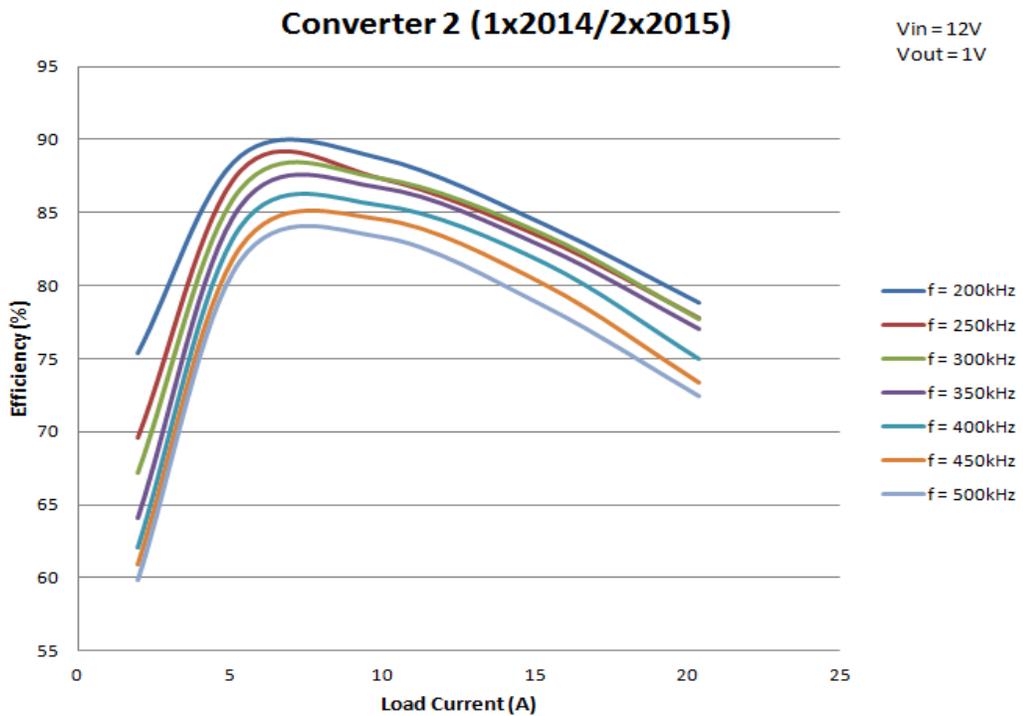


Fig. 3.5: Efficiency vs. load – converter 2 (referenced to Table 3.1).

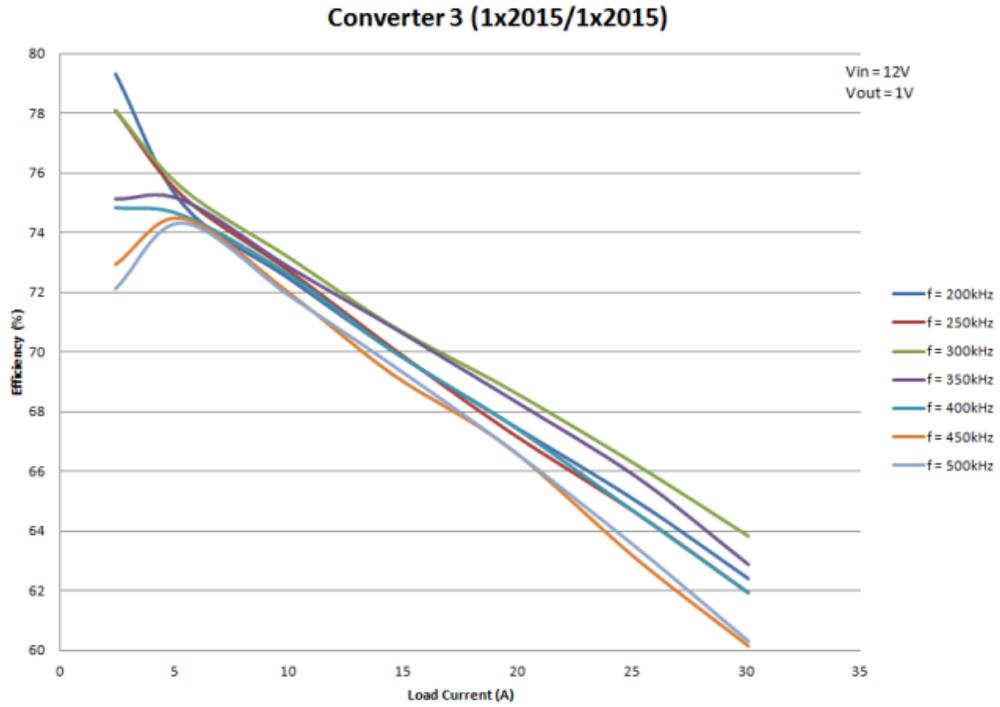


Fig. 3.6: Efficiency vs. load – converter 3 (referenced to Table 3.1).

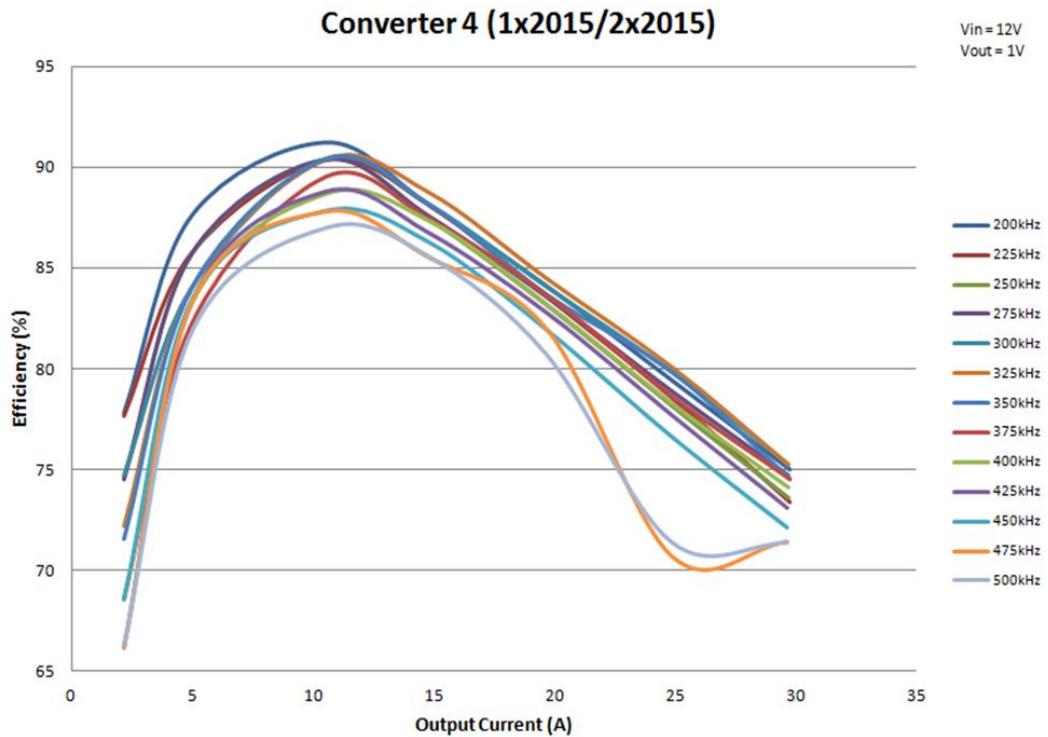


Fig. 3.7: Efficiency vs. load – converter 4 (referenced to Table 3.1).

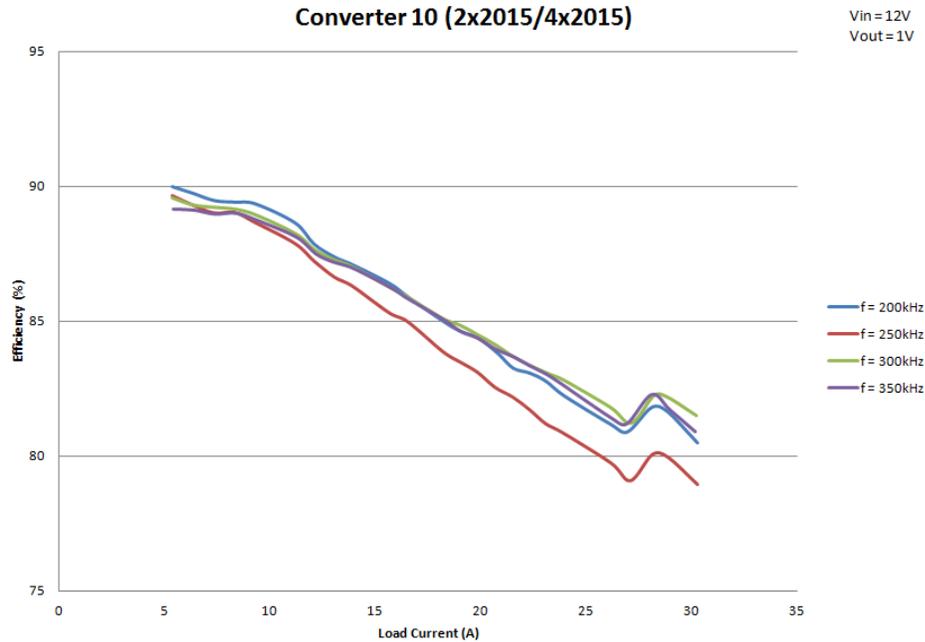


Fig. 3.8: Efficiency vs. load – converter 10 (referenced to Table 3.1).

3.2.3 Summary

GaN power semiconductors are facilitating higher power density, higher frequency, and higher efficiency DC-DC converters. The GaN HEMT market is still limited in product, so some compromise in on-resistance may be necessary. Nevertheless, this can be overcome by paralleling multiple HEMTs, which is a trade-off between switching speed and on-resistance. This paper discusses how that trade-off applies to a 12-to-1 V POL converter. Because the SR conducts the output current for approximately 91% of the period, or one minus the duty ratio, reducing $R_{DS(ON)}$ in the SR is especially important. For this reason, drastic efficiency improvements are realized when implementing a second GaN HEMT in the SR. Results of the 12-to-1 V POL converter indicate that below 19.5 A, one EPC2015 switch and two EPC2015s in the SR is the best design and maximizes efficiency. Above 19.5 A, two EPC2015s in the switch and four EPC2015s in the SR maximizes efficiency. These conclusions can be drawn by analyzing Fig. 3.9, which compares efficiency performance of the best POL converters tested in this section. The design layout and

supporting components are shown and result in a 92% efficiency 12-to-1 V POL converter employing WBG GaN power semiconductors.

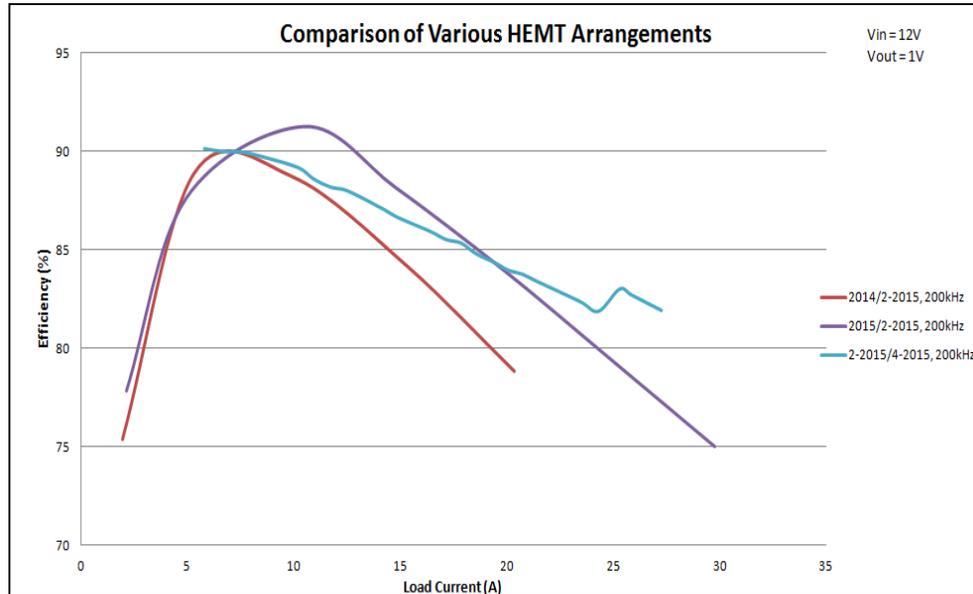


Fig. 3.9: Efficiency vs. load of best performing FET combinations.

3.3 Dead-Time Management

Dead-time management is an important step in designing any synchronous converter where two transistors alternate states to direct current. Recall in Chapter 2 that the asynchronous converter is very easily controlled with a single switch. Once the synchronous system was introduced in Section 2.5, the system controller had to become more complex to operate two alternating switches. Fig. 3.10 shows the two synchronous buck converter states that alternate at a desired duty ratio, D , to reduce the voltage from input to output. The body diode parallel to the SR is necessary in Si-based converters to avoid large inductor voltage spikes if the current was stopped each period while the switches changed states. It is ideal in this system to minimize dead-time since the current flowing through the diode creates more power loss than current flowing through the SR.

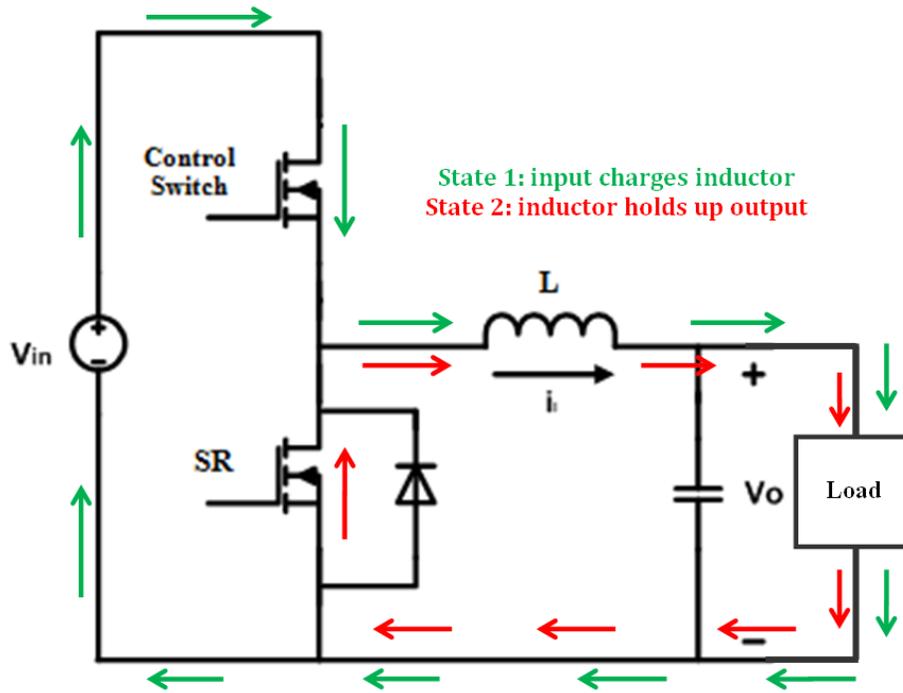


Fig. 3.10: Synchronous buck converter.

In synchronous conversion employing eGaN HEMTs, the body diode is optional, since the GaN HEMT will conduct with applied $V_{SD} \geq 2$ V. Thus, the eGaN HEMT has a built-in body diode effect; however, while the eGaN HEMT conducts due to applied V_{SD} , the forward voltage drop across the HEMT is approximately 2 V. If a Schottky body diode was placed in parallel to the SR, the forward voltage drop of the body diode would only be approximately 0.5 V, reducing the conduction losses during dead-time by 75%. The reverse conduction for a MOSFET body diode and an eGaN HEMT are compared in Fig. 3.11. The penalty, however, is that the body diode also requires energy to turn-off, which is called reverse recovery loss E_{RR} . A finite amount of E_{RR} is lost every time the diode is forced to conduct. This occurs twice every period and the E_{RR} is dependent on the diode characteristics. Hence, minimizing or eliminating E_{RR} loss is beneficial to the system. Since the use of a body diode is optional when using eGaN HEMTs, the two systems

(with and without a body diode) must be studied separately. Each design presents advantages and disadvantages.

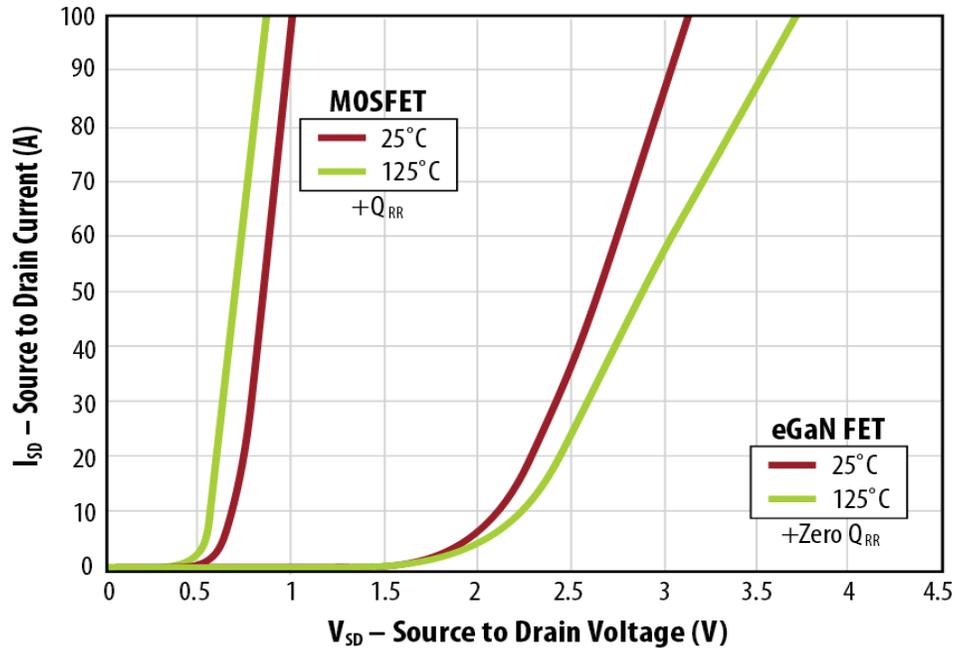


Fig. 3.11: Reverse conduction of MOSFET with body diode and eGaN HEMT [41].

3.3.1 Dead-Time with Body Diode

A distinction must be made between the terms dead-time and effective dead-time. Dead-time is referred to as the time between controller gating signals. Therefore, in a system with zero dead-time, the controller will turn one switch off at the same time that it turns the other switch on. Still, this zero dead-time condition will have effective dead-time since the transistors start and stop conducting at a non-zero gate-to-source threshold voltage (V_{TH}). A system with zero effective dead-time will slightly overlap the control signals so that the V_{GS} of the two switches intersect at V_{TH} . An example of zero effective dead-time and a zero dead-time switching in a half-bridge is presented in Fig. 3.12. Although dead-time is easy to establish, effective dead-time is a function of variations in device threshold, gate resistance, gate driver variation, operating voltage, operating temperature, and gate capacitance. Therefore, a particular amount of controller gate overlap will

not produce consistent effective dead-time among multiple systems, devices, and operating conditions.

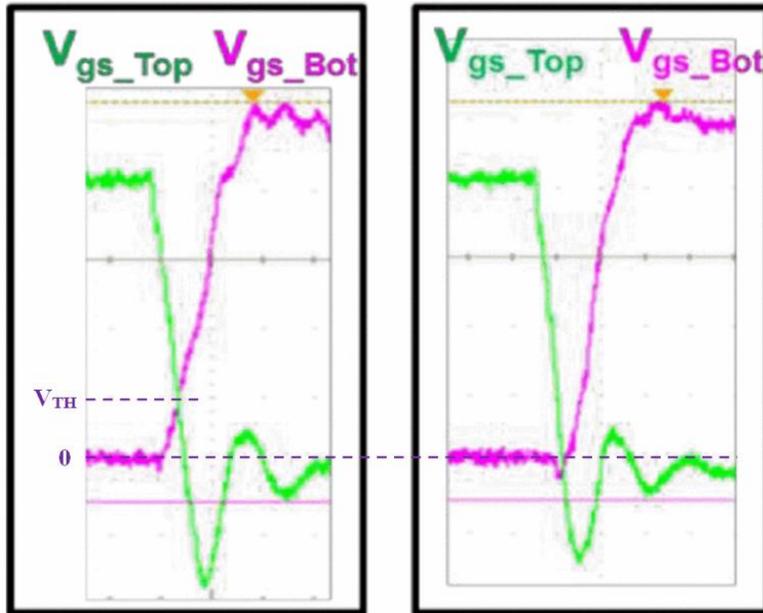


Fig. 3.12: V_{GS} vs. time of a zero effective dead-time system (left) and a zero dead-time system (right) [42].

The more conservative approach is to use an external body diode in parallel with the eGaN SR. Especially for early prototypes, the body diode is very useful because the controller does not have to be fine-tuned, and the system does not pay as much of a penalty for additional dead-time. Once the system design is more mature, it is optional to remove the body diode. At this time, it is much more important to reach near zero effective dead-time.

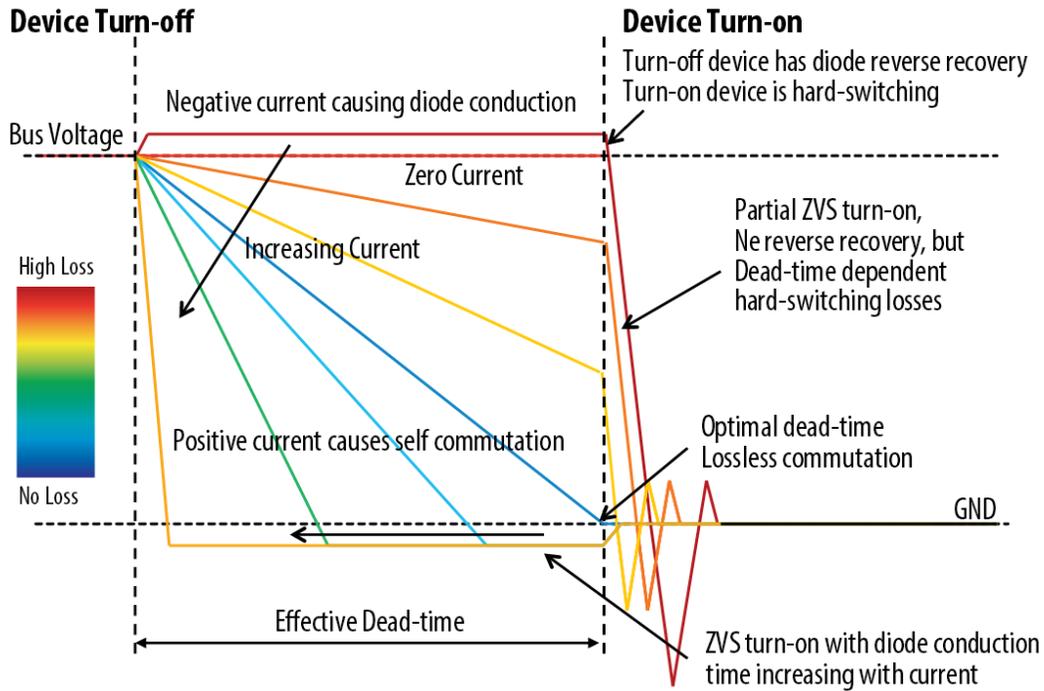
Consider the dead-time interval before SR turn-on. The drain terminal of the SR is externally commutated by positive current flowing into the drain. This current is dependent upon the rate of turn-off of the control switch, which is also load dependent. If the inductor has sufficient energy to completely commutate the voltage, lossless zero voltage switching (ZVS) turn-on can be achieved by the SR; however, if the effective dead-time is increased further, the diode will be forced to conduct. As soon as the diode conducts, it incurs diode conduction losses proportional to

the remaining effective dead-time and reverse recovery losses, which can be calculated using Eq. 3.6 and Eq. 3.7 [41].

$$E_{D,Cond} = I_L \cdot V_F \cdot \Delta t \quad (3.6)$$

$$E_{RR} = Q_{RR} \cdot V_{SN} \quad (3.7)$$

where I_L is the inductor current, V_F is the forward voltage drop of the diode, Δt is the diode conduction time, Q_{RR} is the reverse recovery charge of the diode, and V_{SN} (sometimes referred to as V_{BUS}) is the switch-node voltage and is the node between the two transistors. Consider Fig. 3.13, which represents the SR drain-to-source voltage (V_{DS}) commutation waveforms plotted against time for various load conditions. The lines with larger negative slopes represent the converter operating at higher loads. The converter in this work is designed to operate between the green and blue lines in Fig. 3.13, resulting in only brief diode conduction.



Blue = lossless ZVS with zero diode conduction (ideal SR turn-on)
Yellow = rapid turn-on due to high load = lossless ZVS + diode conduction
Orange = slow turn-on due to light load = lossy hard switching + no diode conduction

Fig. 3.13: SR V_{DS} commutation for varying load conditions [43].

Clearly, dead-time is a complicated matter as the effective dead-time changes based on so many variables, including load condition. The benefit of implementing a body diode, although not necessary, reduces the penalty for forward voltage conduction of the diode during effective dead-time. In the application of the 12-to-1 V synchronous buck converter presented in this work, the operating load is between 0 and 30 A. This large load range means the effective dead-time will change significantly depending on load. With this consideration, a very small 2 A Schottky diode (Vishay MSS2P3-M3/89A) is placed in parallel with the SR. This diode has a maximum reverse DC voltage ($V_{R,Max}$) of 30 V, a forward voltage drop (V_F) of 0.6 V, approximately 65 pF reverse recovery charge (Q_{RR}) that results in low reverse recovery loss, and only a 2 A average current rating. See Fig. 3.14 for the layout implementation of the Schottky diode. Note that the converter may require the diode to conduct up to 30 A for a short time, yet only a 2 A diode is necessary which helps reduce size and reverse recovery loss. If effective dead-time is managed well, an even lower current diode may be acceptable. A similar but lower current diode would significantly reduce Q_{RR} to reduce reverse recovery loss but increase V_F which will increase diode conduction losses. This is a trade-off that may be desirable if the control loop is well-defined to manage effective dead-time sufficiently.

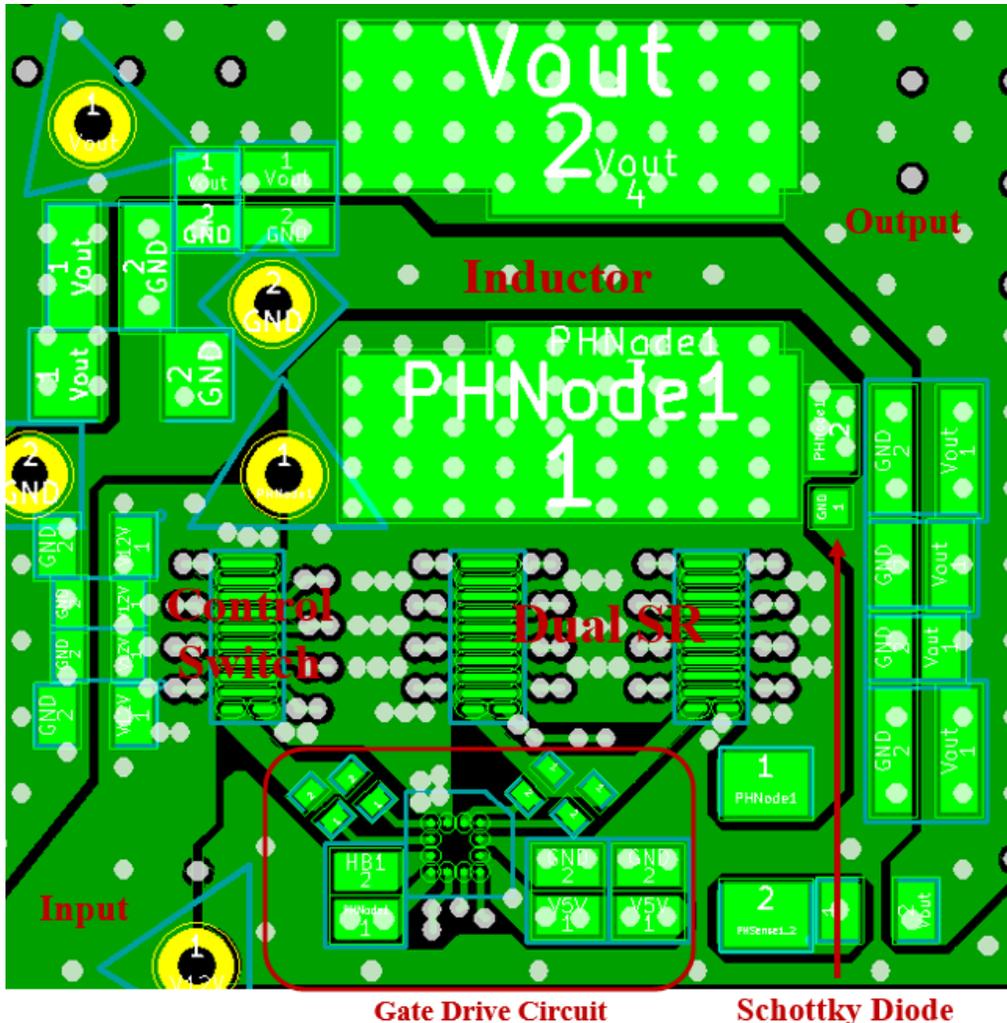


Fig. 3.14: eGaN synchronous buck converter layout with Schottky diode.

3.3.2 Dead-Time without Body Diode

Third party studies show some improvement in conversion efficiency when removing the Schottky diode from the synchronous buck converter. As mentioned previously, this is only beneficial with very low effective dead-time and the effective dead-time must be a function of load current, which complicates the control algorithm. Fig. 3.15 shows the experimental efficiency results from a 1 MHz, 12-to-1.2 V synchronous buck converter employing EPC2015 40 V eGaN FETs; the figure compares GaN and Si systems with and without a Schottky diode, and it compares effective dead-times from 0 to 10 ns. Note that when the third party figure refers to dead-time, this

is effective dead-time as it is defined in this work, and the effective dead-time is equivalent for both switching states.

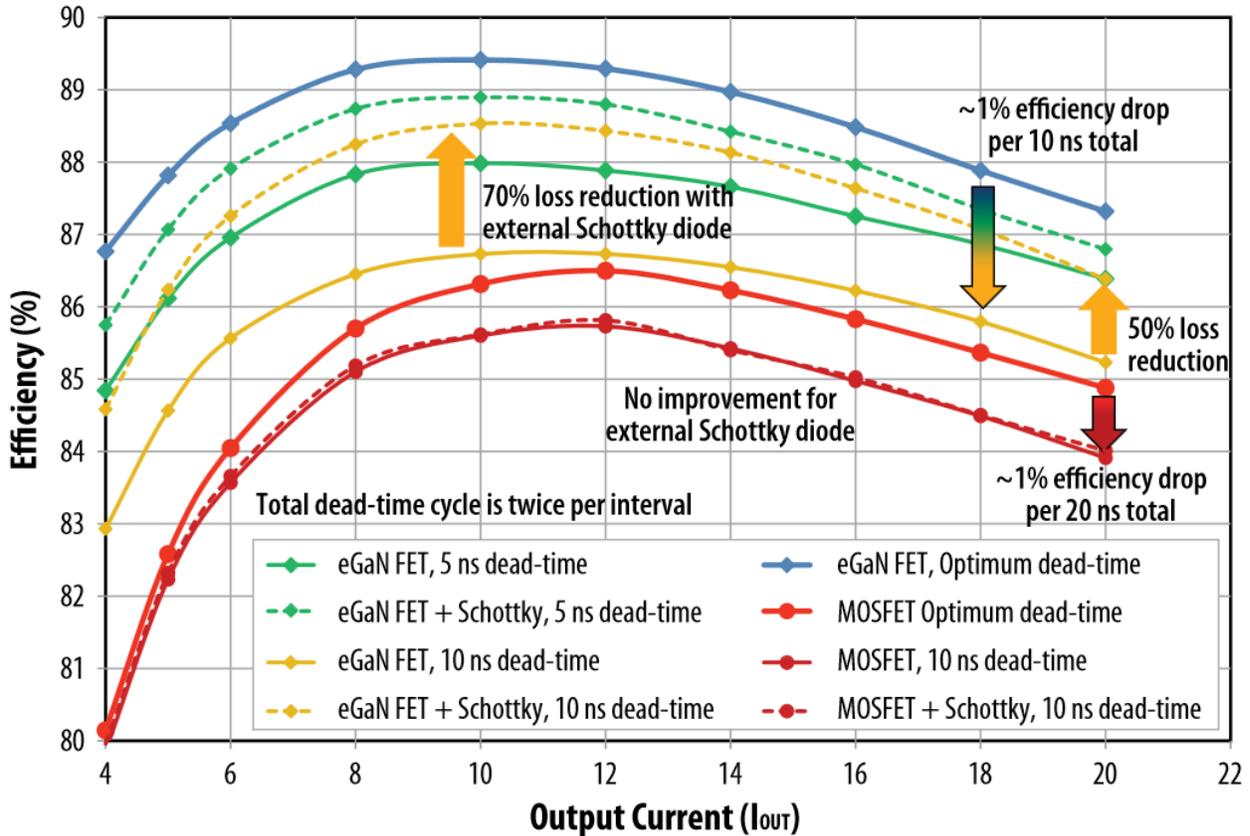


Fig. 3.15: Efficiency of a 1 MHz, 12-to-1.2 V synchronous buck converter with different effective dead-times [43].

Regarding Fig. 3.15, the eGaN efficiency is greater than the Si efficiency due primarily to decreased switching time, while all else remains constant. This is evident by the shapes of the efficiency curves. With 5 ns and 10 ns effective dead-times, the eGaN designs experience significant loss reduction with a Schottky diode. The optimum dead-time, or zero effective dead-time, results in the lowest converter loss. At this operating point, the eGaN FET has no need for a Schottky diode. If the effective dead-time becomes slightly positive, the body diode effect of the

eGaN FET with $V_{SD} \geq 2$ V will conduct with a somewhat large forward voltage drop of 2 V. Therefore, deviation from the effective dead-time comes with a large efficiency penalty.

Although finely tuned systems can operate with near zero effective dead-time, it is unlikely that real products would be capable of doing so while operating reliably. If effective dead-time becomes negative, even slightly, it results in shoot-through current where current travels with nearly zero resistance from input to ground. Very brief shoot-through current causes an immediate drop in efficiency. Longer shoot-through current will damage one or both of the switching devices in the half bridge, blow inrush fuses, or damage other aspects of the circuit. Ultimately, shoot-through current leads to reliability issues and system failure. For this reason, the work presented here retains the Schottky body diode and controls the system to avoid shoot-through at very light loads. Then, at higher loads, when switching occurs more rapidly, the body diode conducts for a longer period of time and incurs some additional loss as a result. This system operates on a constant dead-time control system. A variable dead-time control system may be an option to further improve the system and is thus mentioned in the future work section of this document.

3.4 Impact of Layout Parasitics on GaN-Based Designs

Layout parasitics play an important role in switching quality and speed. In traditional Si-based designs, layout parasitics, particularly parasitic inductance, was only a small fraction of the package inductance of a transistor. Therefore, layout had only minor effect on circuit performance. With GaN bare die packages, parasitics in the semiconductor packaging are drastically reduced, and the layout parasitic inductance is a larger percentage of the inductance that prevents current from changing rapidly. Therefore, small improvements in layout for GaN-based designs results in major efficiency improvement, less voltage ringing, and more reliable FET operation.

There are several critical parasitic inductances that must be minimized for reliable and efficient GaN FET operation: the gate inductance (L_G), common source inductance (L_S), and high frequency inductance loop (L_{Loop}). Although these inductances are experimentally analyzed in a synchronous buck converter, the layout principles can be applied to any GaN-based topology.

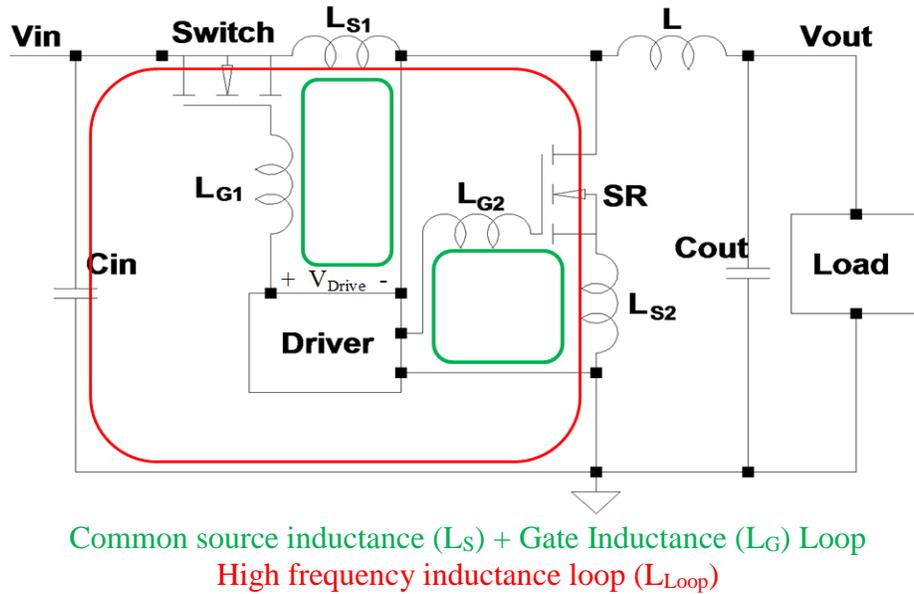


Fig. 3.16: Synchronous buck converter with parasitic inductances.

Large common source inductance creates a voltage drop across L_S during FET turn-on (see Fig. 3.16). This voltage drop subtracts from the drive voltage and slows the rate at which current enters the gate [22]. Gate inductance, L_G , behaves in a similar fashion. A voltage drop across L_G during turn-on reduces the effective drive voltage and limits current to the gate. The gate current is determined by

$$I_G = \frac{V_{Drive} - V_{GS} - V_{LS} - V_{LG}}{R_G}, \quad (3.8)$$

which is equivalent to

$$I_G = \frac{V_{Drive} - V_{GS} - L_S \left(\frac{di_D}{dt} \right) - L_G \left(\frac{di_G}{dt} \right)}{R_G}, \quad (3.9)$$

where V_{Drive} is the gate drive voltage, V_{GS} is the FET gate-to-source voltage, and V_{LS} and V_{LG} are the voltage drops across the common source and gate inductances, respectively. During turn-off, L_{S} and L_{G} inhibit fast switching in the same manner as turn-on but with opposite signs applied to voltages and currents. Reducing L_{S} and L_{G} is particularly important to efficient and reliable switching, as slow switching speeds and increased voltage ringing on the gate are indications of large L_{S} and L_{G} and will apply more stress to the switching transistor.

The high frequency inductance loop, L_{Loop} , is the sum of the parasitic inductances from the input capacitors, through the switch, SR, ground, and back to the input capacitors. L_{Loop} significantly impacts switching speed and switch-node voltage spike. The switch-node is connected to the source of the control switch and the drain of the SR. During turn-on, L_{Loop} lowers the effective voltage across the device—decreasing switching loss. However, during turn-off, L_{Loop} raises the effective voltage across the device—increasing switching loss [41]. The exact trade-off between turn-on and turn-off losses is presented in [22]. However, the net effect is that switching loss becomes greater as L_{Loop} is increased, so it is beneficial to reduce L_{Loop} to promote lower overall switching loss.

It has been established that L_{S} , L_{G} , and L_{Loop} increase switching loss and induce voltage ringing. Yet, the majority of this inductance can be mitigated by employing efficient layout technique [44].

3.5 Experimental Analysis of Layout Parasitics

Although nearly forty different layouts were compared experimentally to determine the optimum layout for this design, three layout approaches to a synchronous buck converter are compared here to explain the concepts gained from this experimental analysis. Incremental improvements are realized as layout is improved to reduce parasitic inductance loops. Three designs are presented in Fig. 3.17. The merits used to compare layouts are switching speed, voltage ringing, and 12-to-1 V DC-DC conversion efficiency.

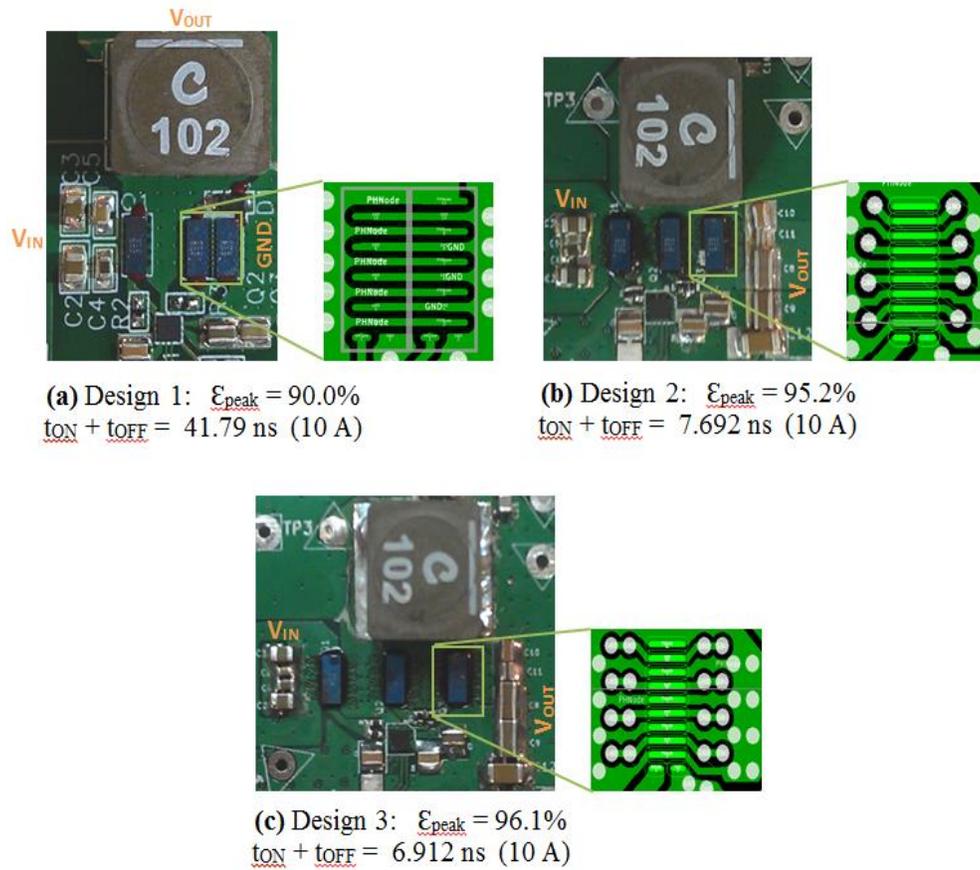


Fig. 3.17: Synchronous buck converter layout comparison.

3.5.1 Design 1: Single-Sided Termination

Design 1 is a single-sided termination design inspired by the low-cost recommendation by EPC [20]. It is a single-sided termination design because current can only enter and exit the source and drain pads of the device in one direction. The two parallel EPC2015s in the SR are placed close and share long source and drain pads. Although this design is functional and physically small, a single-sided termination adds too much common source inductance to be optimal. This layout is represented in Fig. 3.17(a).

3.5.2 Design 2: Double-Sided Termination

A double-sided design has the immediate benefit of letting current enter and exit from both sides of each drain and source pad. The resulting layout reduces parasitic inductance by creating two parallel current paths. Design 2 places the EPC in the middle of the switch-node copper (Cu) plane. The drain pads are connected directly to the Cu plane on layer 1, while the source pads are connected to other ground layers by a single 0.25/0.50 mm via (0.25 mm hole and 0.5 mm pad) on each side of every source pad. This layout is represented in Fig. 3.17(b).

3.5.3 Design 3: Double-Sided Termination (Two Vias)

Design 3 improves upon design 2 by adding an additional 0.25/0.50 mm via on each side of every source pads. This adds more parallel vias to further reduce parasitic inductance compared to design 2. The layout for design 3 is represented in Fig. 3.17(c).

3.5.4 Gate Path Optimization

Rather than running gate and source traces side-by-side on layer 1, as done in design 1, designs 2 and 3 have a wide gate trace on layer 1 with the source return to the driver on layer 2, directly below the gate trace. Interacting magnetic fields reduce inductance on the gate similar to two semi-infinite sheets of current with opposing direction. As the distance between the two conductors becomes smaller, the inductance also becomes smaller. Thus, it is ideal to have a very small isolation layer between the gate line (on layer 1) and the source return to the driver (on layer 2). Rather than the printed circuit board (PCB) manufacturer's default 0.356 mm thick isolation layer, a 0.127 mm isolation layer was selected at no additional cost to reduce gate inductance. A reduction in isolation layer between gate send and return paths is recommended for reduced L_G . This gate layout is presented in Fig. 3.18, where layer 1 (top Cu) is shown in green and layer 2 (first inner layer) is shown in red.

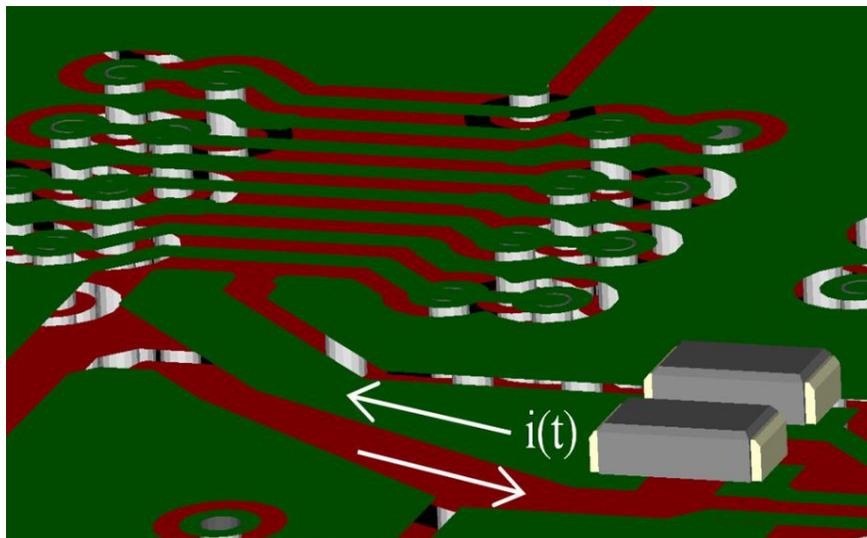


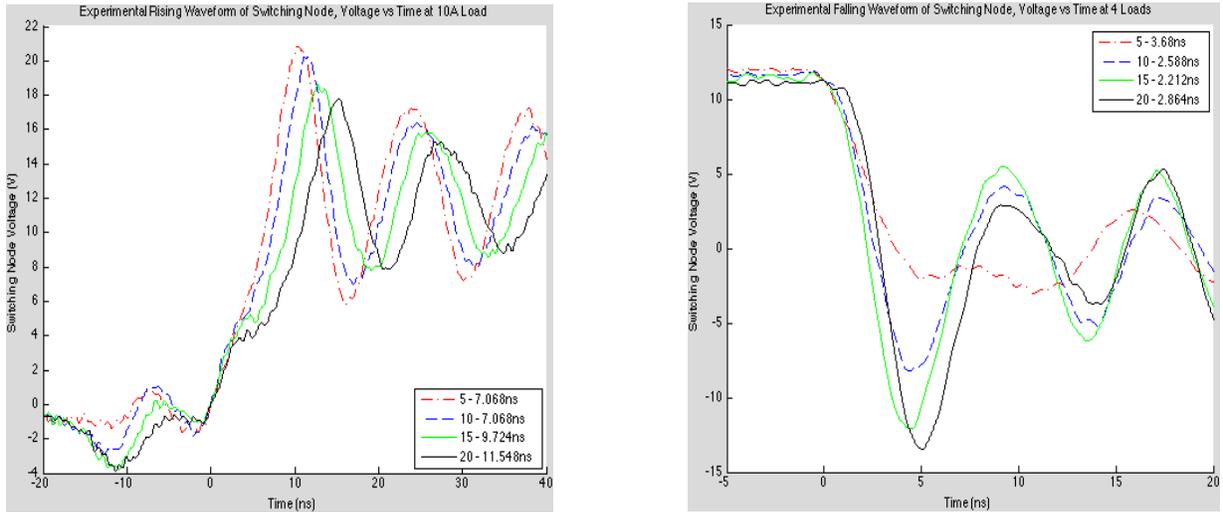
Fig. 3.18: Optimized gate layout for reduced gate inductance L_G .

3.5.5 Impact of Parasitics on Switching Speed and Voltage Ringing

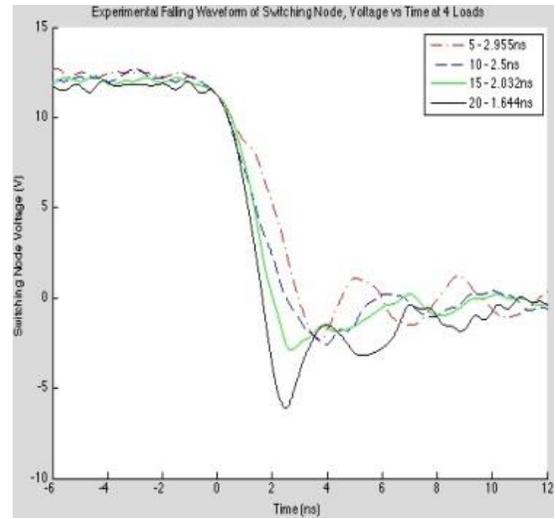
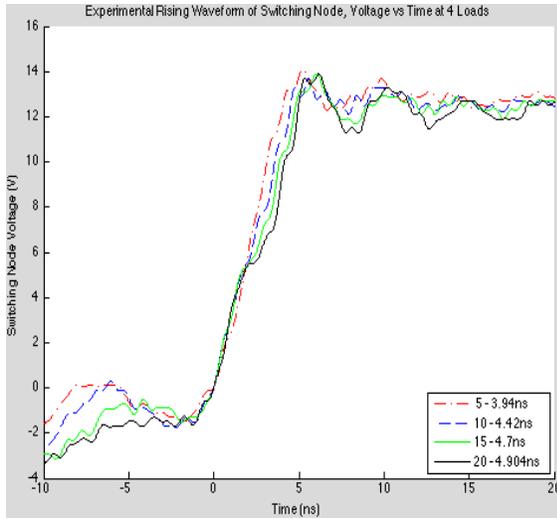
The switching performance was examined by viewing the switch-node voltage overshoot and switching time. Significant improvements are gained from design 1 to 3. This is solely as a result of reduced parasitic inductance. See Fig. 3.19 for switching comparisons. By reducing overvoltage, the FET drain-source breakdown voltage limit is not threatened, which leads to longer device life. By switching faster, the FETs dissipate less heat, leading to improved efficiency and cooler, more reliable operation. Tables 3.3 and 3.4 present turn-on time (t_{ON}), turn-off time (t_{OFF}) and voltage spike of all three designs. Since switching power loss (P_{SW}) is determined by

$$P_{SW} = \frac{1}{2} V_{IN} \times I_{OUT} \times (t_{ON} + t_{OFF}) \times f, \quad (3.10)$$

switching power is directly proportional to total FET switching time ($t_{ON} + t_{OFF}$). It is clear from Table 3.5, that design 3 exhibits the lowest switching loss, as it switches an average of 45% faster than design 1 and 18% faster than design 2.



(a) Design 1 switch-node voltage at turn-on (left) and turn-off (right)



(b) Design 3 switch-node voltage at turn-on (left) and turn-off (right)

Fig. 3.19: Experimental switching waveforms of 12-to-1 V synchronous buck converter at incremental load currents.

Table 3.3: Turn-on time and overshoot

Turn-On	Design 1	Design 2	Design 3
Time (ns): 5A	7.068	4.55	3.94
Peak (V): 5A	20.84	15.21	14.08
Time (ns): 10A	8.23	5.008	4.42
Peak (V): 10A	20.24	14.22	13.7
Time (ns): 15A	9.724	5.836	4.7
Peak (V): 15A	18.6	14.01	13.86
Time (ns): 20A	11.548	5.744	4.904
Peak (V): 20A	17.77	14.08	13.9

Table 3.4: Turn-off time and overshoot

Turn-Off	Design 1	Design 2	Design 3
Time (ns): 5A	4.892	4.888	2.945
Peak (V): 5A	-3.014	-2.02	-2.44
Time (ns): 10A	2.588	2.684	2.492
Peak (V): 10A	-8.2	-2.87	-2.85
Time (ns): 15A	2.212	2.2	2.028
Peak (V): 15A	-12.07	-3.02	-3.41
Time (ns): 20A	2.864	2.12	1.64
Peak (V): 20A	-13.49	-4.04	-6.07

Table 3.5: Total switching time ($t_{ON} + t_{OFF}$) comparison

Total Switching Time (ns)	Design 1	Design 2	Design 3
at 5A load current	11.96	9.438	6.885
10A	10.818	7.692	6.912
15A	11.936	8.036	6.728
20A	14.412	7.864	6.544

3.5.6 The impact of Parasitics on Conversion Efficiency

In order to analyze the role of layout on converter efficiency, efficiency of all three layouts is studied during 12-to-1 V operation from 3 to 25 A load, resulting in an average of 5% efficiency improvement between design 1 and design 3. Greater efficiency improvements are realized at light loads because switching loss is a greater percentage of total converter loss. Improving layout only has significant effect on switching loss. Other loss terms remain relatively constant. Experimental efficiency data is presented in Fig. 3.20.

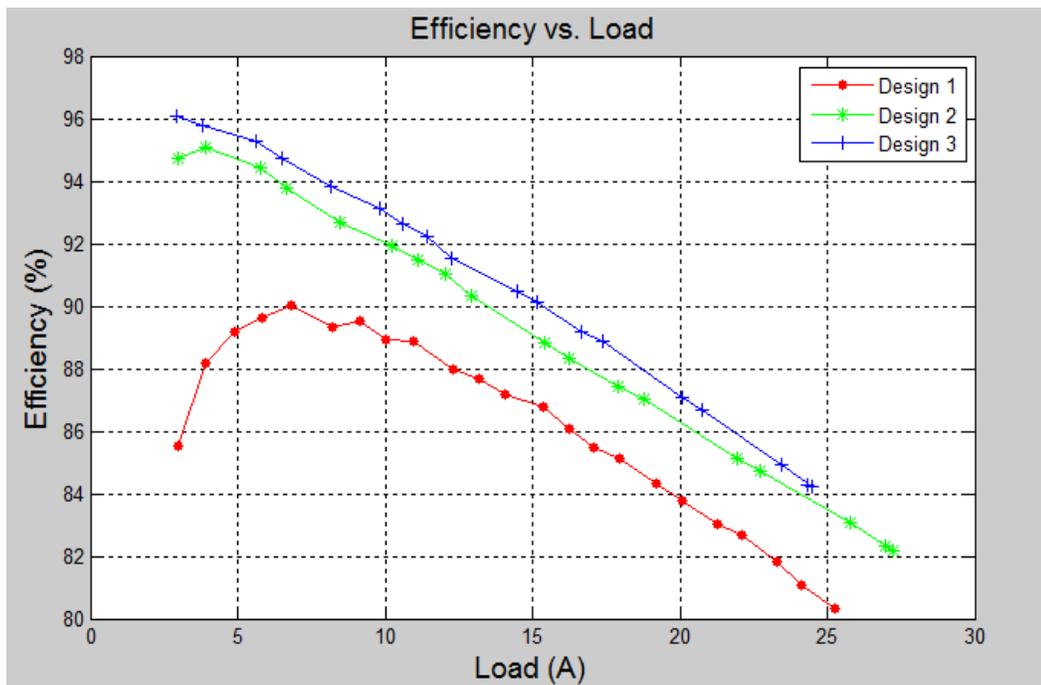


Fig. 3.20: Efficiency vs. load ($V_{IN} = 12$ V, $V_{OUT} = 1$ V, and $f = 180$ kHz).

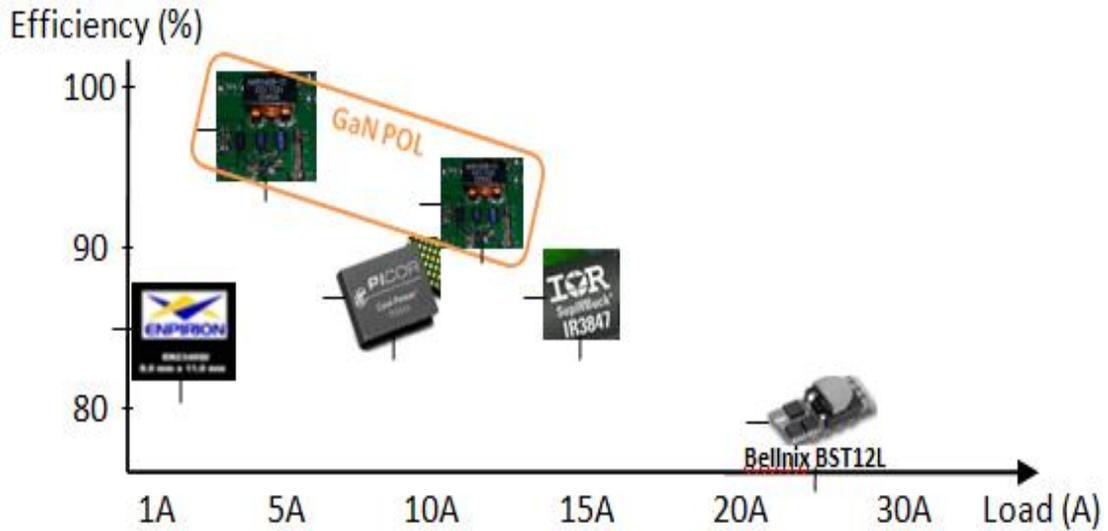


Fig. 3.21: GaN POL experimental efficiency vs. commercial state-of-the-art POL converters operating at $V_{IN} = 12\text{ V}$ and $V_{OUT} = 1\text{ V}$.

With peak efficiency over 96%, this single phase GaN-based POL converter outperforms commercial state-of-the-art DC-DC converters and rivals or beats WBG converter designs found in published work. Many power supply designers are employing GaN primarily to increase power density. The novelty in this work is that GaN is exploited to push the boundaries of conversion efficiency. This is done by first finding the optimal trade-off between conduction and switching loss to determine how many GaN FETs to place in parallel. Next, layout parasitics are minimized through novel techniques that were developed through rapid device prototyping. Once the design is optimized, there is a direct trade-off between size and efficiency. In order to make the POL converter smaller, switching frequency must be increased to reduce the size of the magnetic components. By reducing the size of the inductor, winding and magnetic loss are often increased. Additionally, switching losses are directly proportional to switching frequency and thus linearly increases transistor switching loss. However, if efficiency has precedence over power density, the switching frequency can remain lower, similar to that of Si-based systems, and the reduction in switching loss reduces system loss to raise system efficiency. That is the goal in the design

presented here. The prototype still has very high power density as the transistor size is reduced simply by using smaller eGaN FETs, yet it is also remarkably efficient.

CHAPTER 4

GAN VS. GAN/SI HYBRID POINT OF LOAD CONVERTERS

4.1 Design

Enhancement-mode GaN (eGaN) FETs are a young technology and not yet available with on-resistance as low as some mature Si MOSFETs. Thus, many GaN-based power supplies are limited by high on-resistance, while Si-based systems are limited by slow switching speeds [23]. Neither system is ideal and is thus limited in efficiency. With the application of eGaN HEMTs, fast switching and reasonably low $R_{DS(ON)}$ reduces transistor losses compared to Si MOSFETs [20][27]-[29]. However, there are still some applications better suited for low $R_{DS(ON)}$ Si MOSFETs. For example, in the 12-to-1 V synchronous buck converter presented here, the eGaN FET is a prime candidate for the control switch, but due to the large free-wheeling current, some lower $R_{DS(ON)}$ Si MOSFETs are superior to eGaN FETs for the SR application. This leads to the notion that perhaps the best low-voltage non-isolated POL converter employs a combination of eGaN and Si technology [45][46]. This chapter explores combining eGaN and Si transistors to improve the overall POL design.

When selecting the proper transistors, it is important to be able to compare electrical characteristics of each and understand how they impact performance. $R_{DS(ON)}$ linearly impacts the conduction loss in a FET. Similarly, gate charge, Q_g , is a large factor in determining switching time and thus switching loss [20]. A commonly referred to FOM has been presented in a previous chapter and will be used extensively here. The FOM is calculated by

$$FOM = Q_G \cdot R_{DS(ON)}. \quad (4.1)$$

Many of the best transistors on the market have similar FOMs but increase Q_G and reduce $R_{DS(ON)}$ or vice versa. This is a design trade-off that can be selected in the transistor design. With this in

mind, it should be noted that the control switch will not conduct for very long and thus is optimized by selecting a fast switching device with low Q_G . Alternatively, the SR conducts most of the time, so the SR should have very low $R_{DS(ON)}$.

With several transistors experimentally compared, the EPC2015 reduces overall losses in the control switch. The EPC2015 has $R_{DS(ON)} = 4 \text{ m}\Omega$ and $Q_G = 10.5 \text{ nC}$. Since the equivalent on-resistance of the SR must be further reduced, two different POLs were designed and are shown in Fig. 4.1 & 4.2). The GaN design in Fig. 4.1 uses four parallel EPC2015s to achieve an equivalent on-resistance $R_{DS(ON),Eq} = 1 \text{ m}\Omega$, and a total gate charge $Q_{G,Eq} = 42 \text{ nC}$. The GaN/Si hybrid design in Fig. 4.2 replaces four EPC2015s with a single $1.1 \text{ m}\Omega$, 32 nC Si MOSFET, resulting in a slightly improved FOM, lower overall gate charge, and less required board space.



Fig. 4.1: GaN POL converter (1.25 in^2 per phase)



Fig. 4.2: GaN/Si Hybrid POL converter (0.74 in^2 per phase)

The synchronous buck converter is an easy topology to parallel. Thus, the system can be designed and analyzed with a single phase, and expansion to multiphase designs is relatively simple. The POL designs from Fig. 4.1 and Fig. 4.2 are identical with the exception of the SR and slight layout modifications to accommodate the change in SR. The Texas Instruments' LM5113 gate driver

operates at 4.5 V, and the Infineon BSC010NE2LS replaces four EPC2015s in the GaN/Si design, which leads to a 40% decrease in size. Calculations and simulations of both designs indicate very similar performance. They were constructed and tested with two interleaved phases, which essentially doubles the output current, and the performance results of both designs are quite similar.

4.2 Experimental Comparison

Both designs are tested with two parallel phases (a two phase POL) from 6 to 40 A load, 120 – 500 kHz switching frequency, and with 1.5 μ H and 2.0 μ H Coilcraft SER1410 inductors. Test data is presented in Fig. 4.3 – 4.5. Results indicate that the GaN design has greater switching loss, as its efficiency drops quicker with increasing frequency. Efficiency vs. load indicates that the GaN design has slightly less conduction loss. Thus, low current operation is more efficient with the GaN/Si design, while high current operation is slightly more efficient with the GaN design at low switching frequencies; but above 400 kHz, the GaN/Si design performs better regardless of load due to reduced switching loss. With overall better performance and 40% smaller footprint, the GaN/Si hybrid design appears to offer many advantages for high current POL applications, at least until GaN technology matures to accommodate lower $R_{DS(ON)}$ applications. Expansion to more than two phases with this GaN/Si design will be addressed later in Chapter 7.

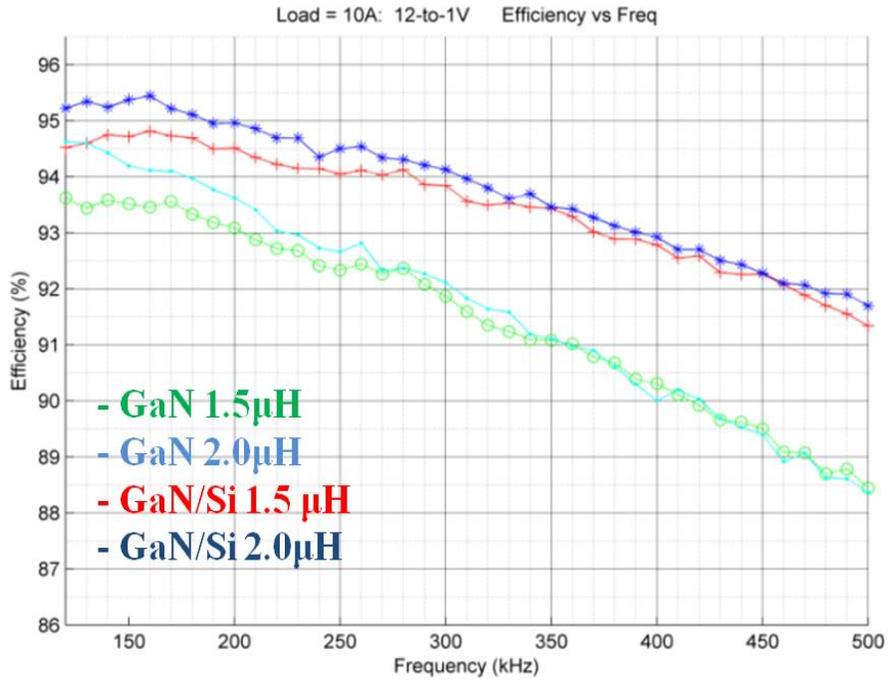


Fig. 4.3: Efficiency vs. frequency, $I_{OUT} = 10$ A.

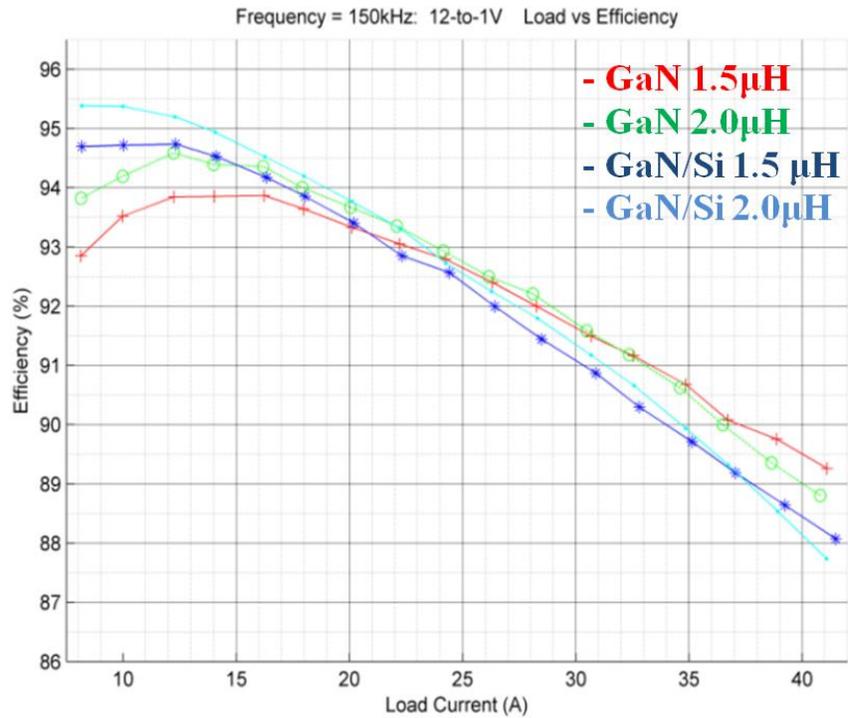


Fig. 4.4: Efficiency vs. load, $f_S = 150$ kHz and $f_{eff} = 300$ kHz.

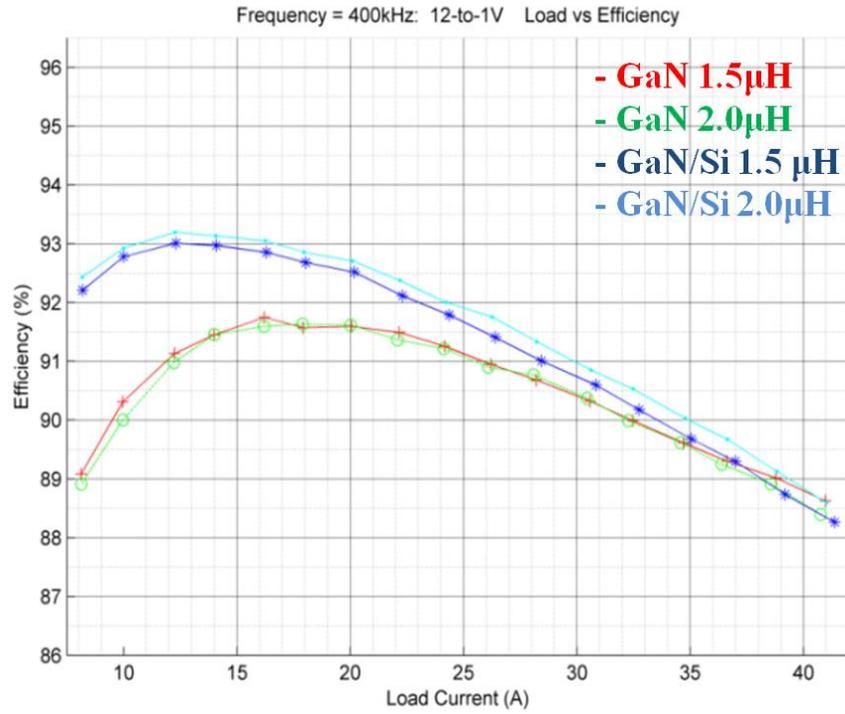


Fig. 4.5: Efficiency vs. load, $f_s = 400$ kHz and $f_{eff} = 800$ kHz.

CHAPTER 5

EXPERIMENTAL ANALYSIS OF COMMERCIAL INDUCTORS

The two largest contributors to loss in synchronous buck converters are the power semiconductors and the magnetic components. Since several previous sections have addressed how to reduce losses in the power semiconductors, this section compares many of the best commercially available inductors suitable for this design to determine which inductors yield the lowest overall loss. Inductor loss is subdivided into two forms of loss: winding loss and magnetic or core loss. Naturally, there will be particular inductors suitable for high load, low load, high frequency, and low frequency operation. This chapter will address the best magnetic components for each application and suggest a good compromise for the best overall performance incorporated into the POL converter.

The testing in this section takes place on the single phase eGaN synchronous buck converter (design 2 from Section 3.5.2), and the converter is shown in Fig. 5.1. After testing more than fifty commercial inductors between 0.05 and 3 μH from several vendors such as Coilcraft, Würth Electronics, EPCOS, and others, the six best performing inductors for this 12-to-1 V POL application are:

- Coilcraft SER1408-102 (1 μH)
- Coilcraft SER1590-102 (1 μH)
- Coilcraft XAL1010-102 (1 μH)
- Coilcraft SER1590-152 (1.5 μH)
- Coilcraft SER1410-152 (1.5 μH)
- Coilcraft SER1410-202 (2.0 μH)

The experimental testing results are shown in Fig. 5.2 – 5.5. Additional information on these commercial inductors can be found in [47]-[49]. In general, the higher inductance improves efficiency at light loads because AC core loss is reduced. However, at higher load currents, lower inductance improves efficiency because there is often less DC resistance (DCR) in lower value inductors.

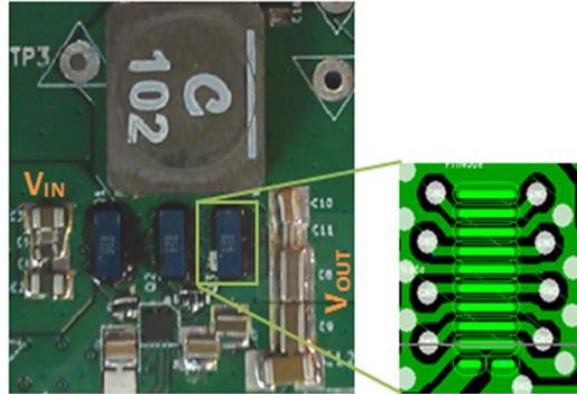


Fig. 5.1: Synchronous buck converter platform for characterizing inductors.

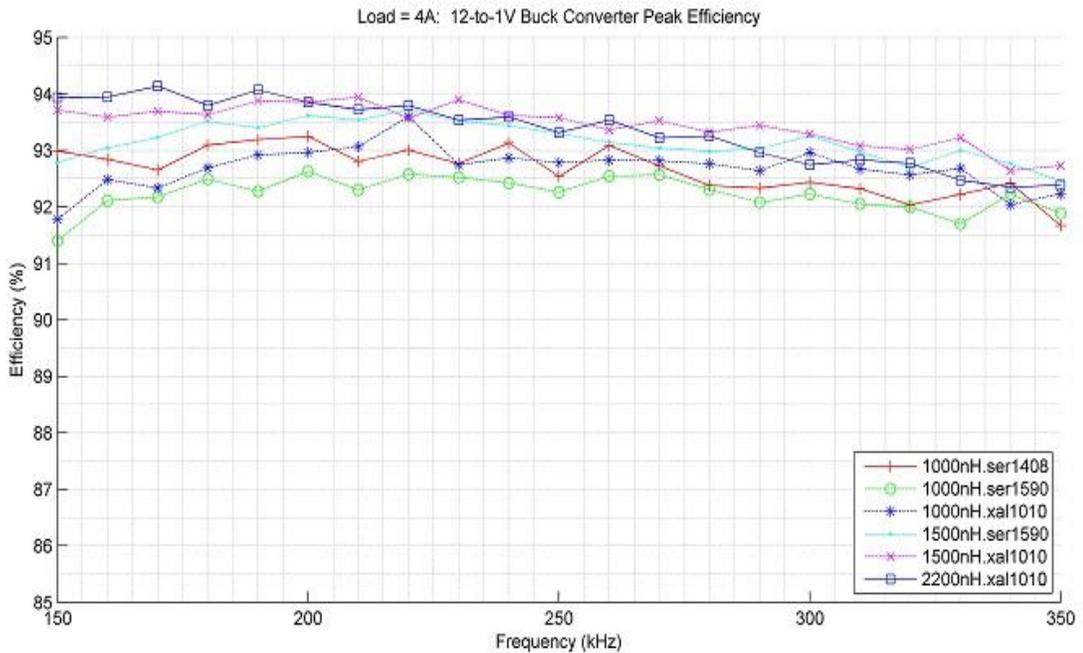


Fig. 5.2: Efficiency vs. frequency at 4 A load with various inductors.

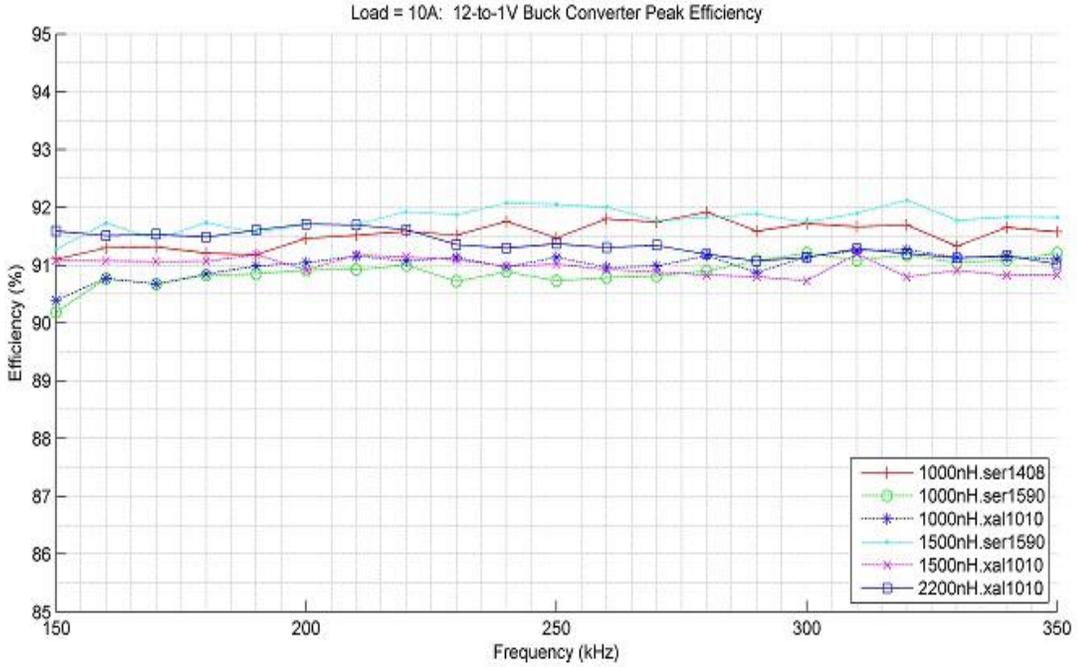


Fig. 5.3: Efficiency vs. frequency at 10 A load with various inductors.

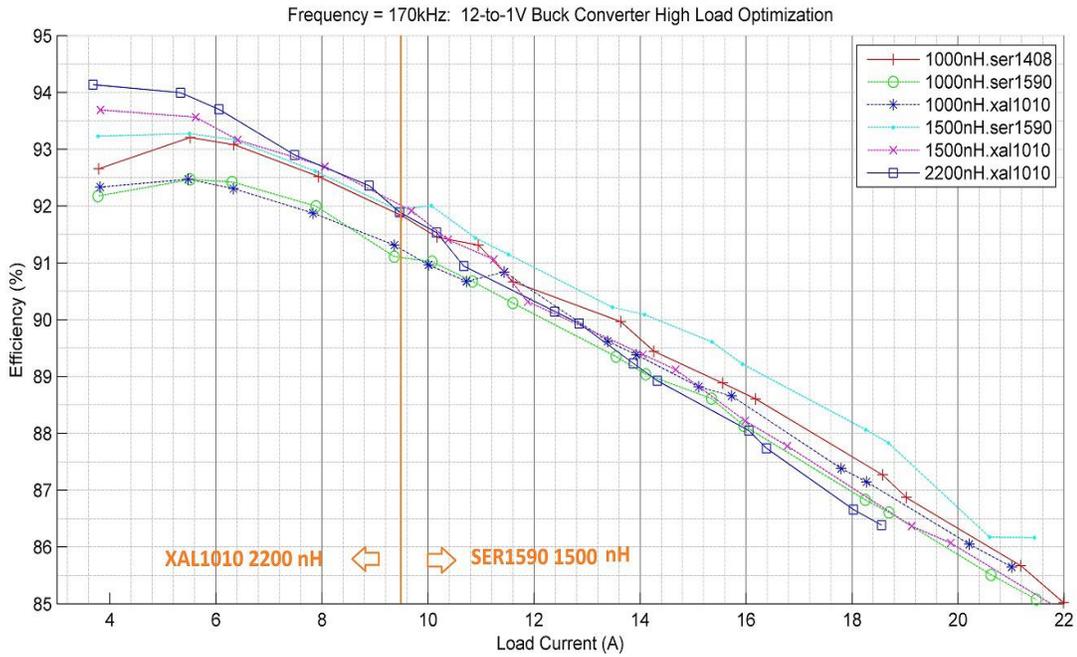


Fig. 5.4: Efficiency vs. load at 170 kHz with various inductors. Below 9 A, the XAL1010 2200 nH is the most efficient. Above 9 A, the SER1590 1500 nH inductor is most efficient.

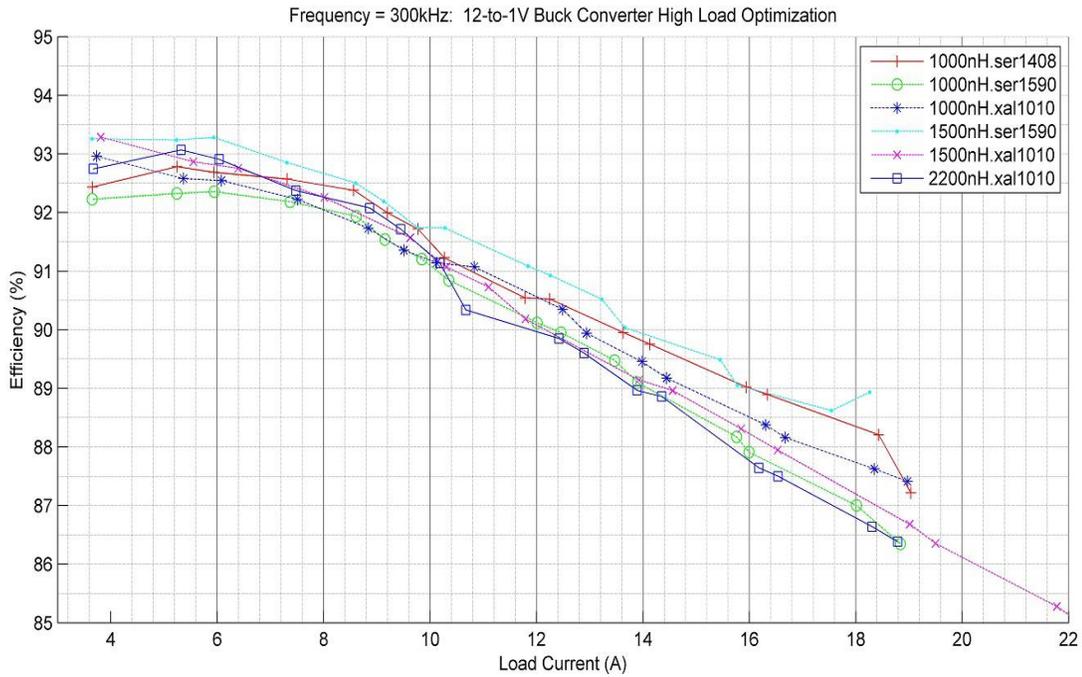


Fig. 5.5: Efficiency vs. load at 300 kHz with various inductors. The SER1590 1500 nH inductor is one of the top performers at higher frequencies.

Experimental data indicates that best converter efficiencies are realized around 170-200 kHz. With that in mind, below 9 A load current, the 2.2 μH inductor is ideal. Above 9 A, the 1.5 μH Coilcraft SER1590-152 performs best. All considered inductors are similar in physical size, so load conditions determine the best inductor for peak efficiency.

CHAPTER 6

PLANAR INDUCTOR DESIGN AND COMPARISON

6.1 Overview

In this chapter, the design and implementation of planar inductors in low-voltage GaN-based applications are investigated, and design techniques conducive to inexpensive, simple implementations are utilized. The advantages and limitations of planar inductor technology, as it relates to filter inductors, are presented. Design considerations such as core material, core geometry, number of turns, gap size, fringing fields, and winding construction are addressed, and several planar inductors are evaluated in a 12-to-1 V GaN-based synchronous buck converter. Experimental results are used to determine the feasibility and advantages of replacing commercially packaged components, such as those addressed in chapter 5, with planar inductors. The primary focus is to reduce inductor core loss, winding loss, size, and raise saturation current by employing well-designed planar inductors to modern, wide-bandgap power converters.

With the high power density demands of power supplies, switched-mode power supplies (SMPS) have experienced an increase in switching frequencies to facilitate smaller packaging and stringent load conditions [29][53][54]. The magnetics are often responsible for the majority of system losses, especially in high current and high frequency applications[55]. A decrease in the size of magnetic components is a natural consequence of increasing the switching frequency[56]. However, additional losses are introduced in the inductor as a result of skin and proximity effects from higher frequency AC current. Conventional round-wire inductors are particularly sensitive to such losses. Planar magnetic technology provides the framework for developing inductors more favorable for operation at high frequencies [57]. Planar magnetics offer numerous advantages over

traditional wire wound components, including reduced AC winding loss, great thermal characteristics, and repeatability with narrow tolerance.

The primary drawback of planar magnetic technology is the difficulty in achieving an acceptable DCR. Thick copper traces and parallel PCB layers can mitigate this drawback, but will increase the cost of the PCB. Consequently, the gains made with respect to the AC resistance can be negated by the DC losses at high load currents. For this reason, PCBs with more layers can make a significant improvement in DCR by adding additional conduction paths and should be strongly considered in the cost-to-performance analysis of any planar magnetic design [57].

6.2 Planar Magnetic Design

Inductor losses can generally be subdivided into two categories: core loss and winding loss. Core loss involves hysteresis loss and eddy current formation within the core material. Winding loss is often spoken of in terms of AC and DC losses. DC losses are proportional to the DCR of the windings and the square of the DC current. AC losses occur as a result of the skin and proximity effects. For many low-voltage SMPS applications, winding loss makes up the majority of the total inductor loss since output currents are often high [58][59].

Several core materials are available and have a variety of trade-offs. Four of the core materials and core geometries examined in this work are presented in Fig. 6.1 and Fig. 6.2, respectively. The rounded center posts of the ER18 and ER23 (Fig. 6.2) facilitate superior winding design and are used extensively in this work.

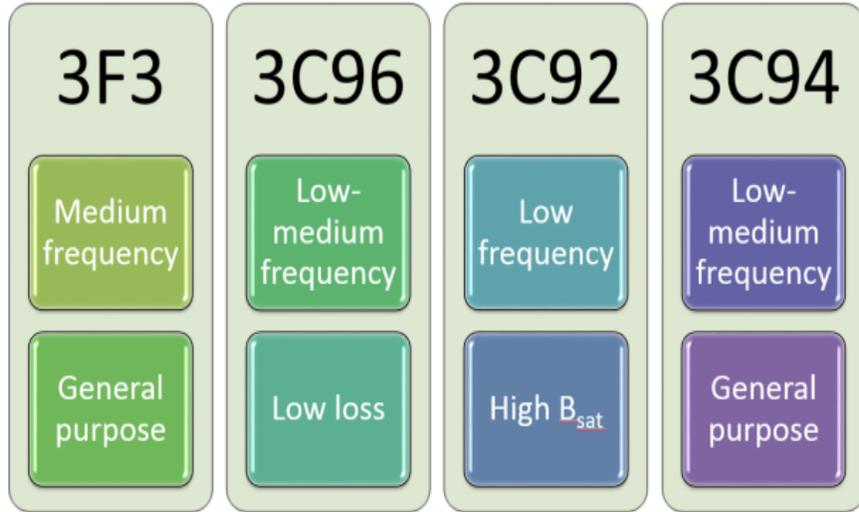


Fig. 6.1: Core materials (Ferroxcube).

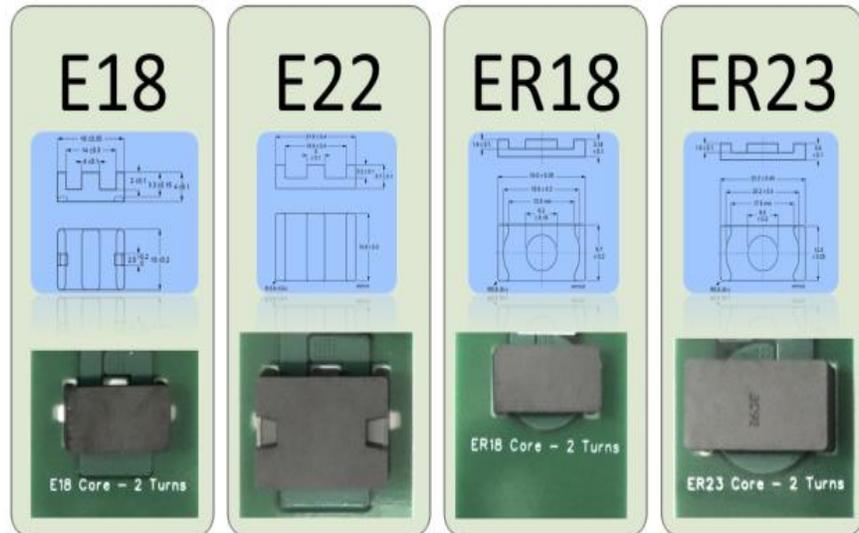


Fig. 6.2: Core geometries (Ferroxcube).

When considering inductor winding design, a one-turn inductor will result in lower inductance; however, a one-turn inductor has the advantage of lower DCR, since the length of the winding is shorter and all PCB layers become parallel conduction paths. However, if higher inductance is desirable and a multi-turn planar inductor is necessary, the ideal interleaved winding construction that promotes proper current sharing is depicted in Fig. 6.3. This interleaving technique alternates first turn and second turn layers and is discussed extensively in [54][55]. This

technique was also verified through 3-D finite element analysis (FEA) before physical implementation.

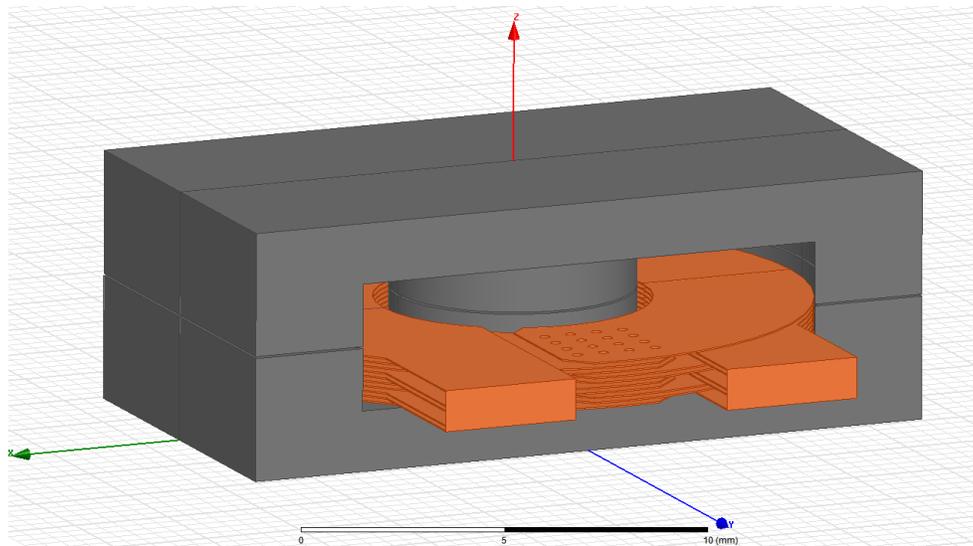


Fig. 6.3: 3-D inductor winding structure with ER18 core and 10 PCB layers.

Gapping is often required to maintain a predictable inductance and to increase saturation current. The size and location of the gap can substantially change the performance of the inductor by determining effective permeability and inductance, which impacts current ripple. These two parameters oppose one another, and an iterative process should be used to determine proper gap size [55][56]. Designing an inductor that yields maximum allowable ripple forms a suitable starting point within the design trade space. Subsequently, the inductance can be increased by reducing gap size until the saturation current is reached at maximum load, thus providing the designer with an experimental operating range. In this work, inductors with center post gaps and distributed gaps are evaluated. The air gap ($\mu_r = 1$) raises the reluctance of the path to increase energy storage; however, the air-gap also exhibits magnetic fringing effects that induce eddy currents in nearby windings. Fringing fields induce additional AC winding loss and crowd the current near the air gap, where magnetic fields are the highest. The result is uneven current sharing that leads to increased conduction loss. Proper layout technique can mitigate the effect of fringing

fields by spacing inductor windings to avoid the highest concentration of fringing fields (see Fig. 6.4(a)). The optimal space from the air gap is when the eddy currents and AC resistance are low without sacrificing winding size that significantly increases DCR (see Fig. 6.4(b)).

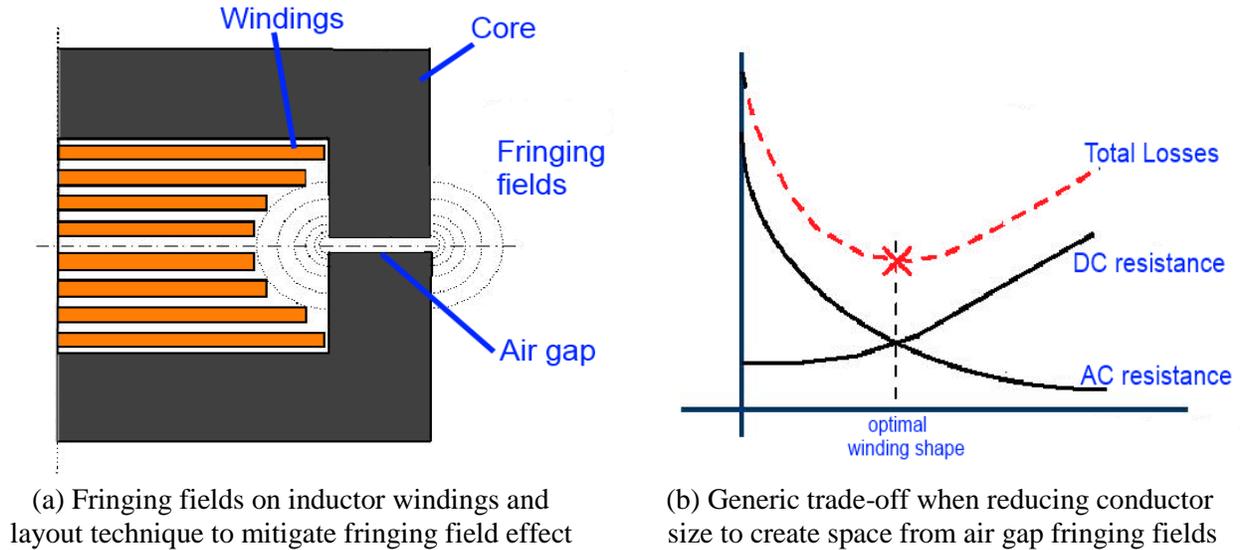
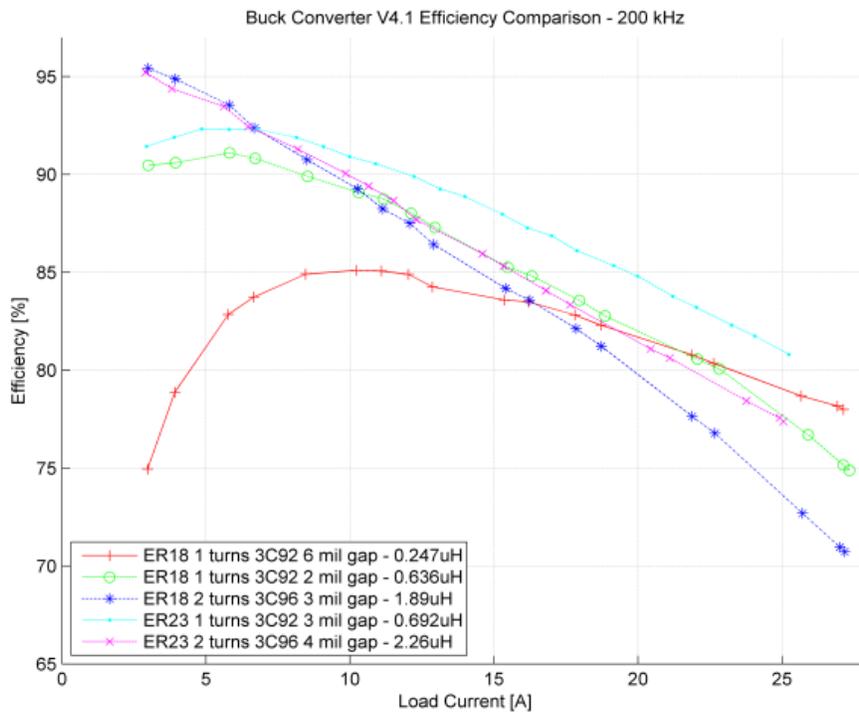


Fig. 6.4: Spacing inductor windings to reduce eddy currents induced by fringing fields.

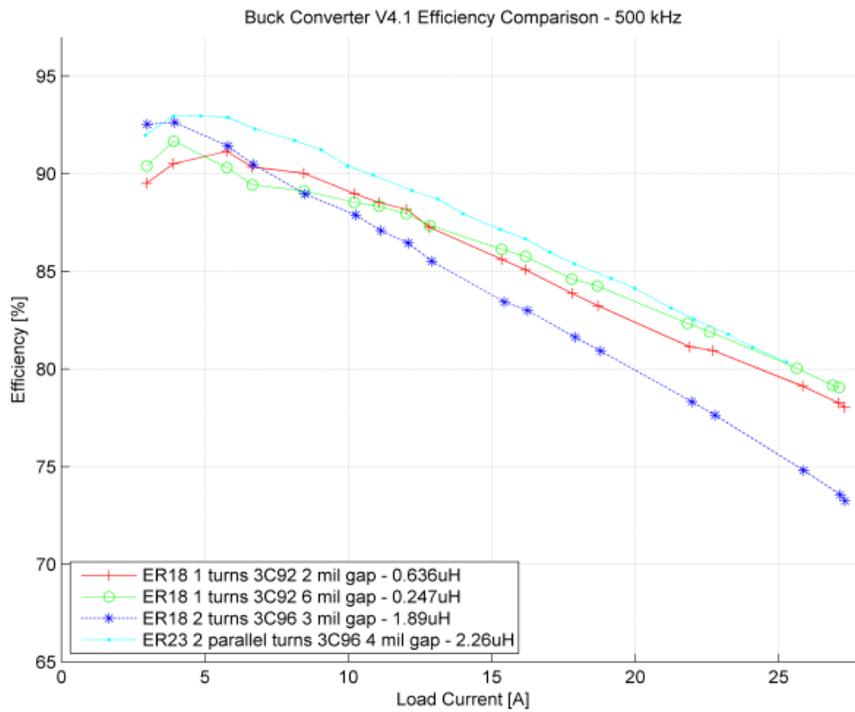
6.3 Preliminary Experimental Comparison

First, broad preliminary experimentation with planar inductors is explored. The results of the preliminary data will guide a more focused planar inductor design. In the preliminary experimental comparison, many combinations of core material, core geometry, gap size, gap type, and number of turns were compared by mounting a planar inductor encompassing the windings and planar core to the POL converter. This enabled easy planar inductor comparison without redesign of the entire POL converter. Testing took place on a 12-to-1 V GaN-based synchronous buck converter; efficiency results are shown in Fig. 6.5. There are significant trade-offs depending on operating conditions. For example, a two-turn inductor demonstrated better low current efficiency than a single-turn inductor due to higher inductance and reduced AC loss, whereas a single-turn inductor increased high load efficiency by decreasing DCR. This trade-off between

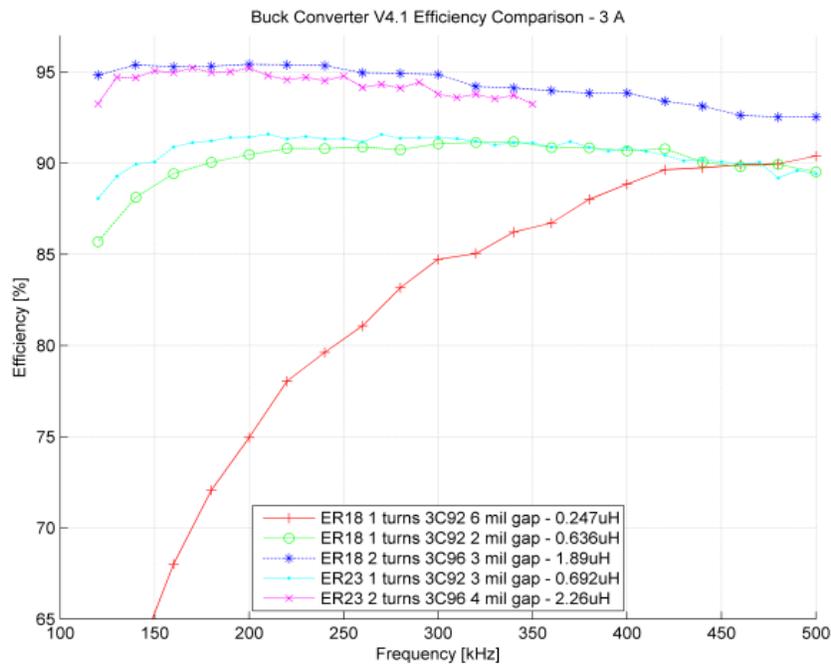
inductance and DCR is particularly evident in Fig. 6.5(a) and Fig. 6.5(d). The ER23 core geometry outperformed the E18, E22, and ER18 cores with its rounded center post and slightly larger size. At 200 kHz, a 3 mil gap appeared ideal. At 500 kHz, a 4-6 mil gap performed best, particularly at higher load currents where the larger gap prevented core saturation. A larger gap is acceptable because the decreased inductance that resulted from a larger gap did not result in additional output ripple, as long as the frequency was increased accordingly. For the widest load and frequency conditions, a two-turn inductor delivered the best overall performance. Thus, preliminary experimental results indicated that the 2.26 μH ER23 two-turn inductor with a 4 mil distributed gap optimized performance in this design. However, in later designs, space constraints disqualified the use of this core due to its larger size, and the ER18 core geometry was employed instead while other parameters remained the same.



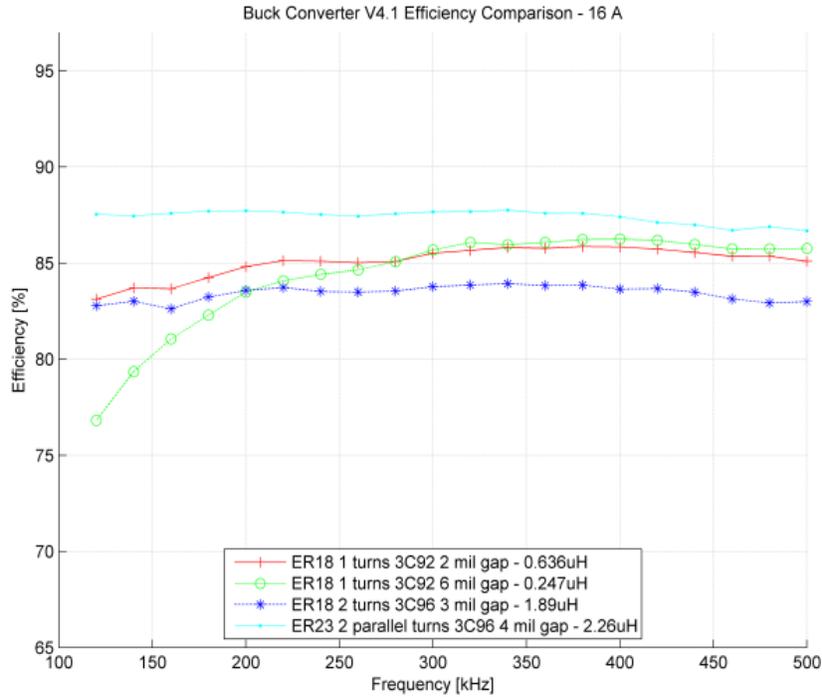
(a) Efficiency vs. load current – 200 kHz



(b) Efficiency vs. load current – 500 kHz



(c) Efficiency vs. frequency – 3 A



(d) Efficiency vs. frequency – 16 A

Fig. 6.5: Preliminary experimental analysis of planar inductors in a 12-to-1 V synchronous buck converter.

6.4 Final Experimental Comparison

The broad experimental comparison and FEA simulations narrowed the field to enable a final planar inductor prototype, which was optimized for this application. In the final design prototype, shown in Fig. 6.6, the smaller ER18 core was utilized to meet space constraints, even though the ER23 showed improvements in performance. This design uses a two-turn winding, 3C96 core material, and a 4 mil distributed gap. The result is a compact 1.59 μH planar inductor that has been optimized for this 12-to-1 V DC-DC application. Efficiency results are presented in Fig. 6.7 and efficiency was particularly high for a low-voltage converter of this nature. Typical commercial converters of comparable specifications operate well below 90% efficiency, even under the best operating conditions.

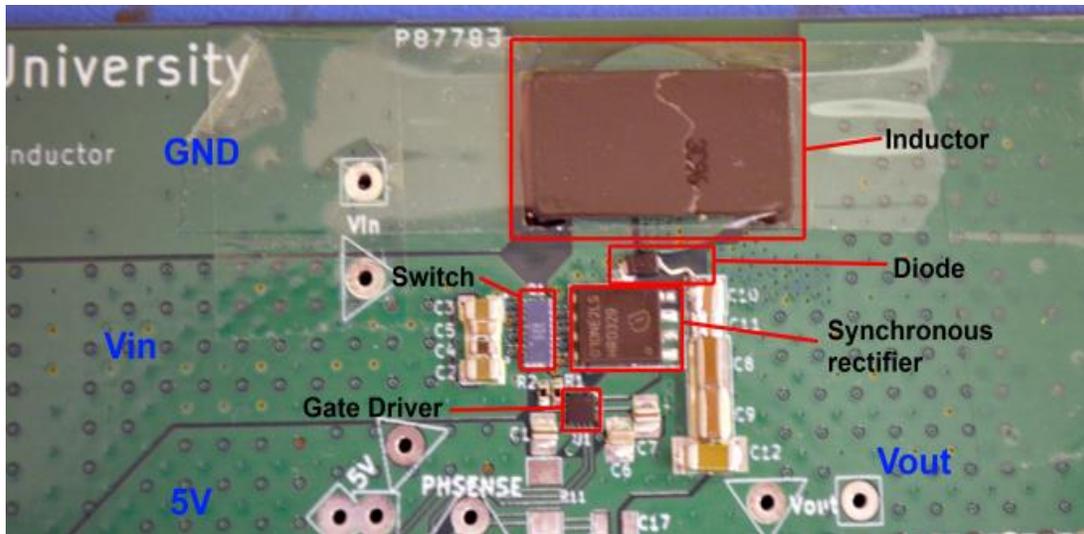


Fig. 6.6: Synchronous buck converter with planar inductor.

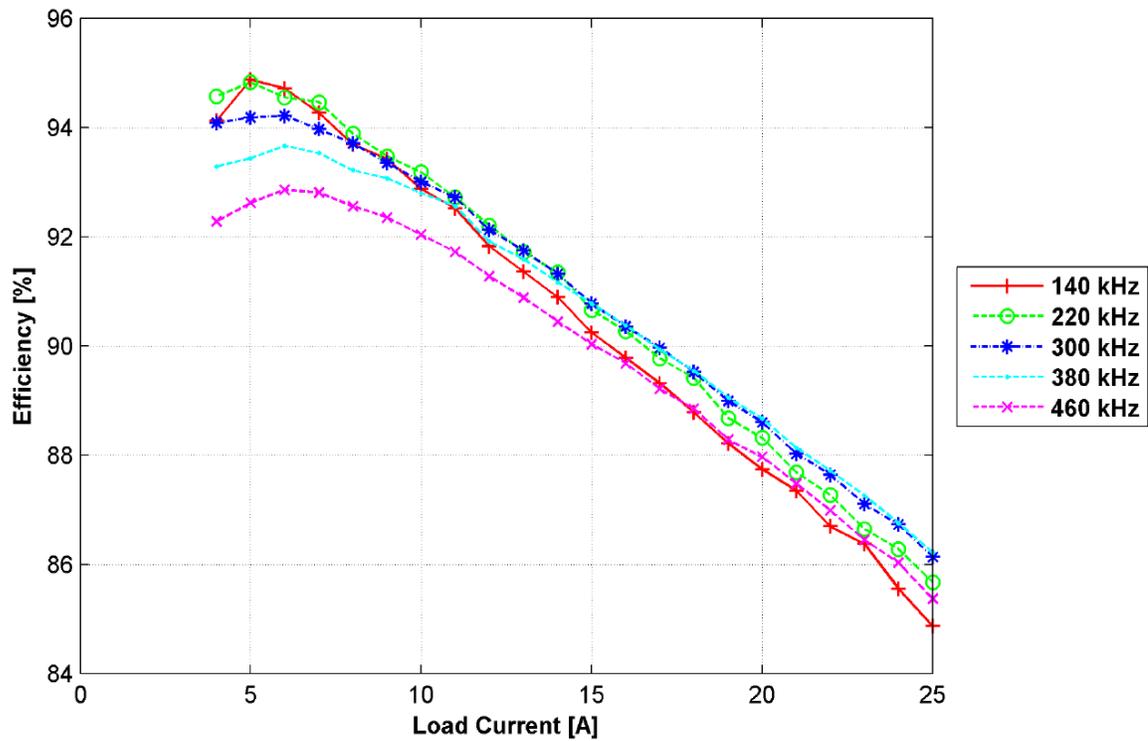
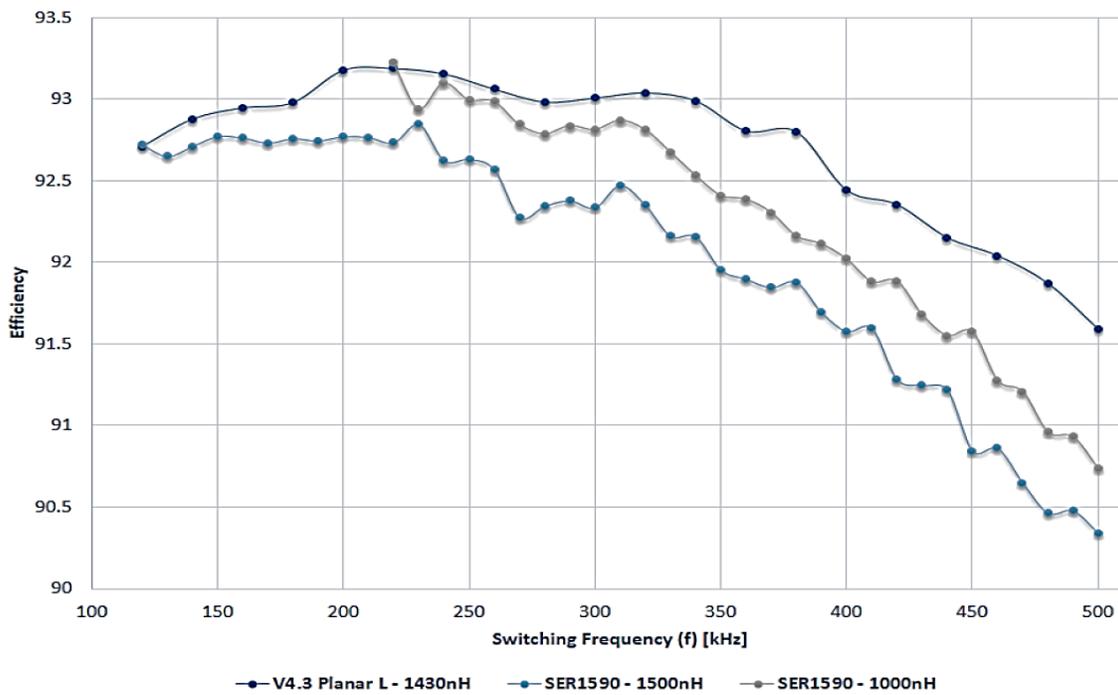


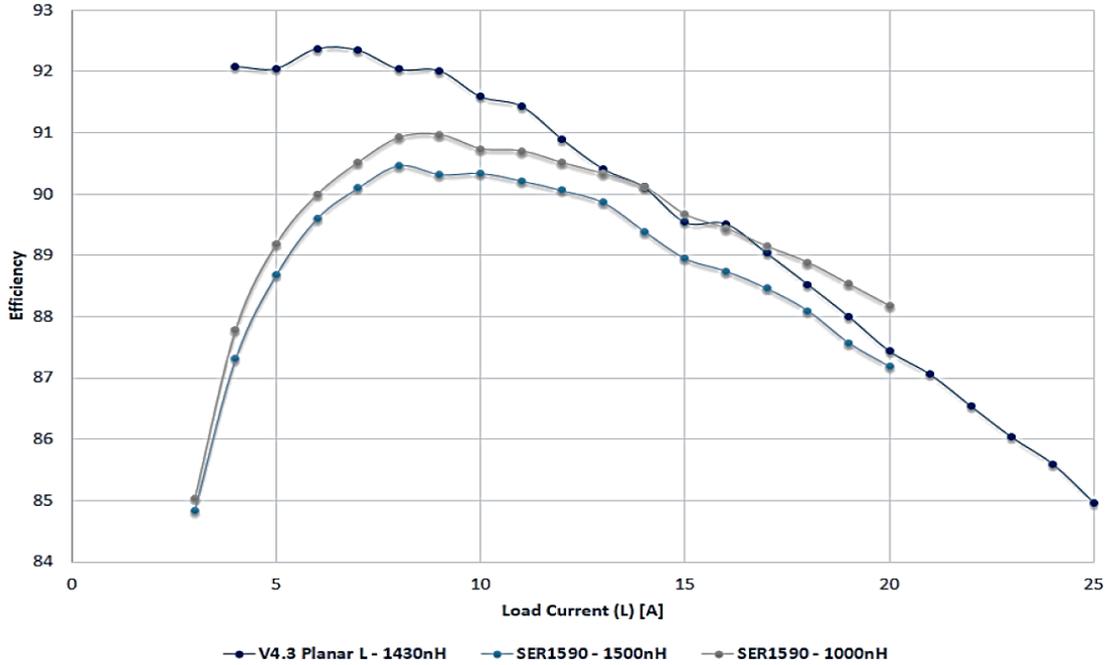
Fig. 6.7: Efficiency vs. load (ER18 / 2 turns / 3C96 / 4 mil gap / 1.59 μ H).

To validate this design and compare to commercial inductors, Fig. 6.8 compares the efficiency of this planar inductor to two Coilcraft inductors with similar footprint, saturation

current, and inductance. Fig. 6.8(a) indicates that the planar inductor shows lower AC losses, as the efficiency drops less with increasing frequency compared to the commercial alternatives. Next, Fig. 6.8(b) shows significant improvement in efficiency at light loads, which is a result of low AC losses; however, efficiency decreased more rapidly with an increase in load compared to the commercial alternatives. This is a result of slightly higher DCR in the planar inductor but is an acceptable trade-off considering the overall performance advantage achieved with the planar design. Additionally, DCR may be further reduced by adding more PCB layers, which result in more parallel conduction paths. The advantages of this inductor are even more evident when increasing frequency, making this planar inductor design ideal for modern WBG power conversion that often operates at or above 1 MHz.



(a) Efficiency vs. frequency – 10 A



(b) Efficiency vs. load current – 500 kHz

Fig. 6.8: Performance comparison of planar inductor and commercial inductors.

6.5 Conclusions

Planar inductors have been experimentally developed and integrated into a 12-to-1 V synchronous buck converter. Major parameters governing planar inductor design were described in a simplistic manor to facilitate a similar design process, regardless of the application. Major design parameters include: core material, core geometry, air gap size, and winding construction. These parameters have been investigated in a broad experimental comparison which allowed trade-offs to be established for this particular design. Next, an optimized 1.59 μH planar inductor was compared to similar commercial inductors to demonstrate the improvement in AC losses and overall performance with planar technology. With a reduction in AC loss and high saturation current, this planar inductor design is ideal for high frequency wide-bandgap power conversion applications.

CHAPTER 7

MULTIPHASE POINT OF LOAD DESIGN

7.1 Theory

Multiphase synchronous buck converters offer many appealing features and are simple to implement by connecting common V_{IN} and V_{OUT} and sharing common output capacitance. When I^2R losses begin to dominate the system, strategically dividing the output current among the phases can drastically reduce conduction loss. By spacing each phase by $\Delta\theta$, where

$$\Delta\theta = \frac{360^\circ}{\text{number of phases}}, \quad (7.1)$$

output current and voltage ripple is minimized because inductor currents add at the output. Fig. 7.1 shows efficiency of a one, two, and three phase POL converters operating at 170 kHz per phase, which results in effective frequencies (f_{eff}) of 170 kHz, 340 kHz, 510 kHz, respectively. Adding POL phases results in nearly identical performance with reduced output ripple, and performing phase shedding allows optimum efficiency to be maintained over a wide load range [60]. As the effective frequency is increased by increasing the number of phases, the output ripple is reduced. Fig. 7.2 simulates the reduction in output voltage ripple when adding POL phases and the trend continues as more phases are added.

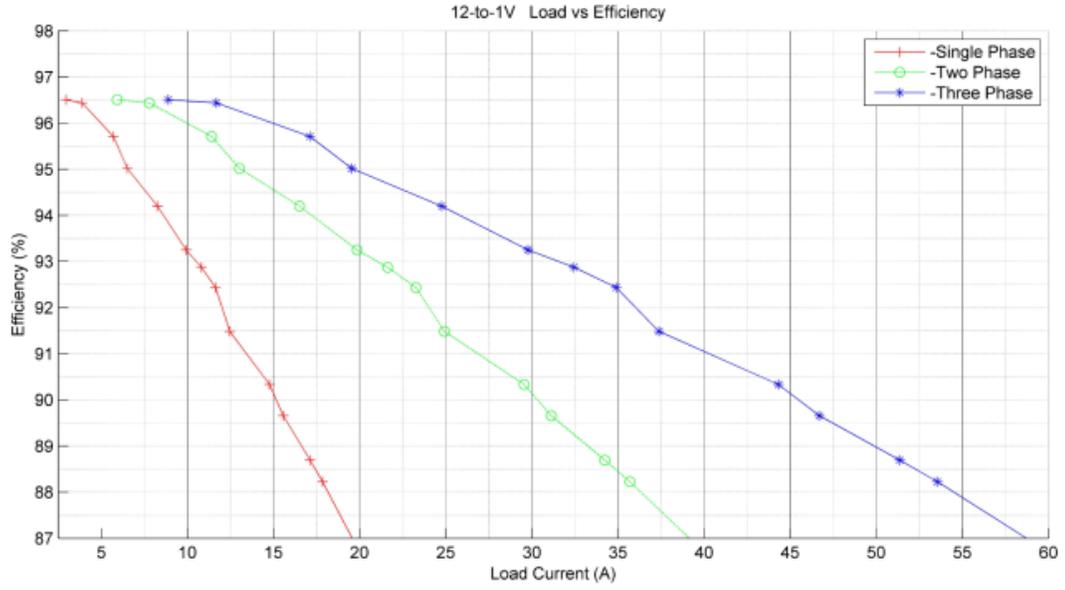
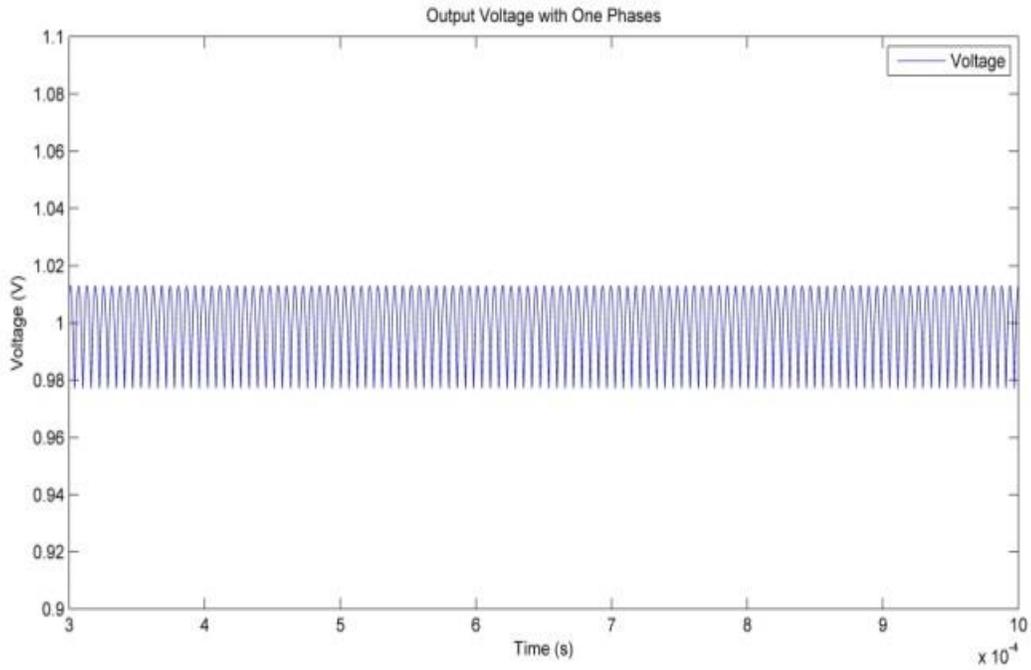
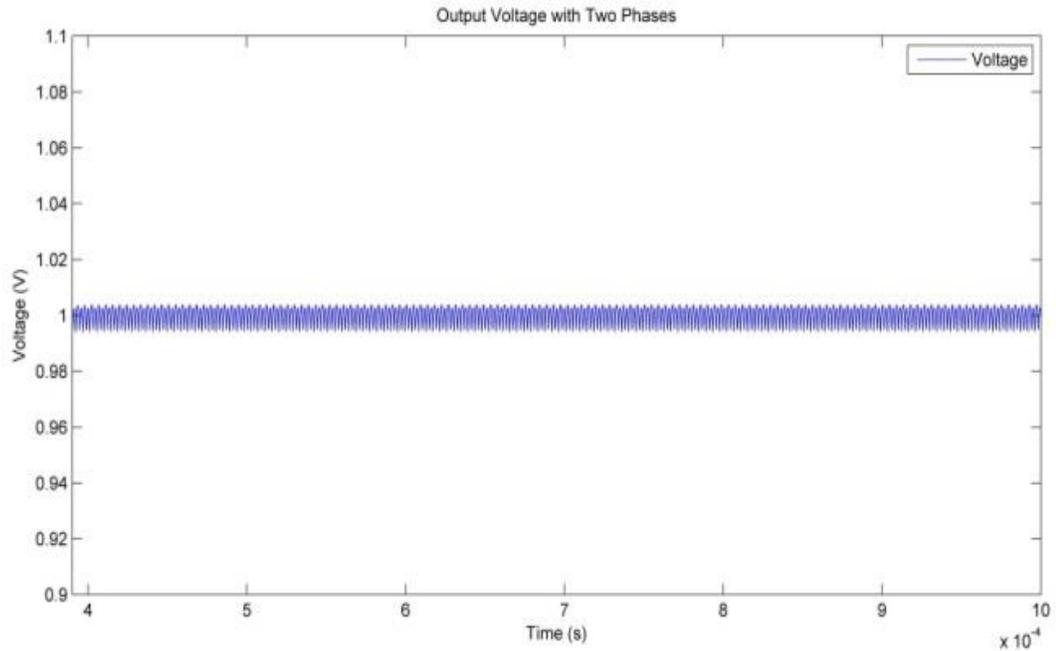


Fig. 7.1: Efficiency vs. Load for One, Two, and Three Phase POL Converters ($f = 170$ kHz per phase).



a) One phase POL output ripple (simulated)



b) Two phase POL output ripple (simulated)

Fig. 7.2: Output voltage ripple comparison.

7.1.1 Advantages of multiphase POLs

There are many significant advantages to multiphase POL converters. A multiphase POL converter:

- Distributes current to reduce conduction loss
- Increases output power
- Reduces steady-state output ripple
- Raises output frequency to reduce transient response delay (time from load change until the next phase turns on)
- Reduces the current demand through semiconductors at partial load
- Can perform phase shedding to maintain high efficiency over a very large load range

7.1.2 Disadvantages of multiphase POLs

Likewise, there are several sacrifices that must be made. Multiphase POL converters may result in:

- Increased size
- More complex control algorithms
- Circulating currents between phases
- Concerns of uneven current sharing (easily manageable by reading phase current and adjusting the duty ratio, D)

7.2 Version 3 Testing Platform

The Version 3 testing platform in Fig. 7.3 enables experimentation with multiphase POL converters. It has been designed to test between one and five phases. The TI DSP controller is capable of controlling all five phases. Each phase can be plugged into one of the 100-pin headers located on the right side of the mother board. All POL designs are constructed on this platform, tested as a single phase POL, and then tested with one to five phases if preliminary single phase data looks promising. This platform has separate inputs for 5 V (controller), 5 V (driver), and input voltage so that each loss can be measured and recorded separately. Part of the test set-up also includes a static/dynamic load board that was specifically designed to meet the current and power demand of this POL converter. This load board has been improved over multiple iterations and is presented in Fig. 7.4 and Fig. 7.5.

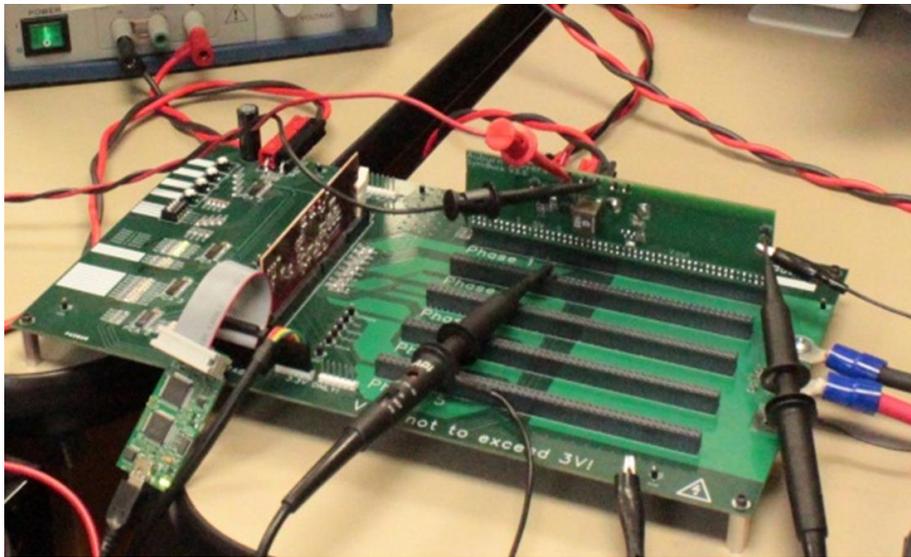


Fig. 7.3: Version 3 POL testing platform capable of testing 1-5 phase converters.

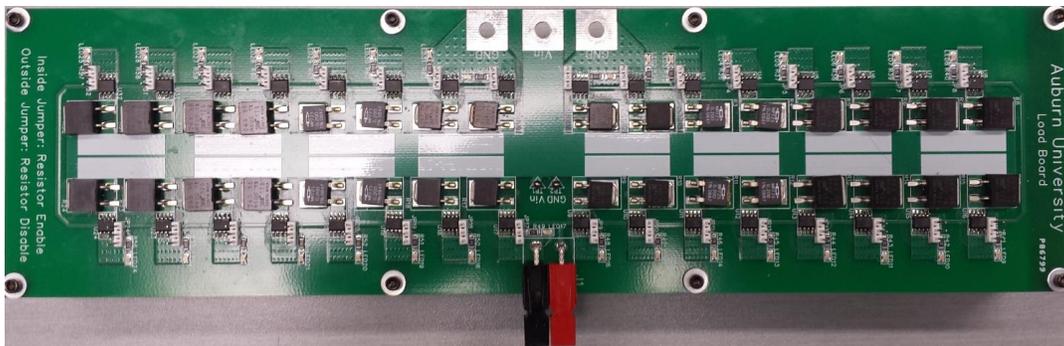


Fig. 7.4: Dynamic load board revision 1.

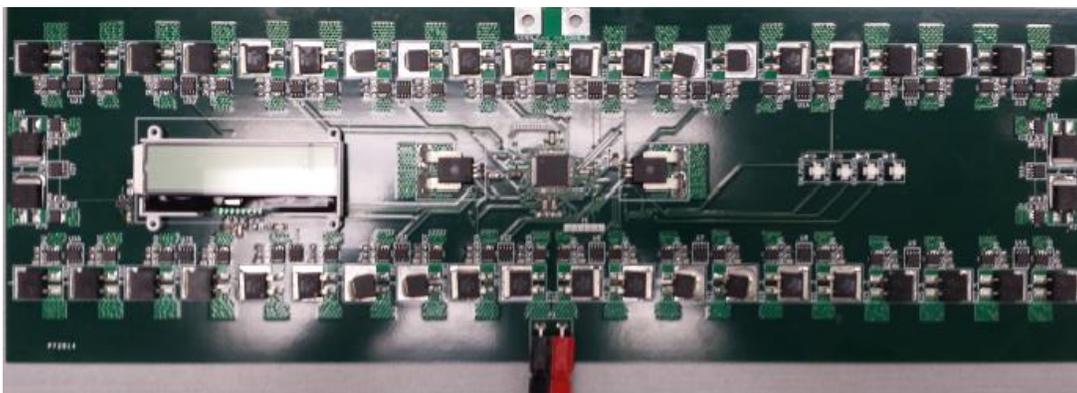


Fig. 7.5: Dynamic load board revision 2.

7.2.1 Five Phase GaN/Si Hybrid Design

This section presents experimental results of an optimized five phase GaN/Si hybrid synchronous buck converter designed to improve converter efficiency while meeting increasing load demands typical in HPC. This section presents an expansion of the GaN/Si hybrid design presented in Chapter 4, as the previous work is now implemented in five interleaved phases. Interleaved is a term used to identify that the control switches from each phase are turned on at evenly spaced times within the period.

It has been established that the best eGaN FETs have very low gate charge, switch much faster than Si, and reduce size, and eGaN FETs are not yet available with extremely low $R_{DS(ON)}$, like comparable Si MOSFETs. For this reason, eGaN-based systems are susceptible to poor efficiency at high loads. To mitigate this consequence, the appropriate combination of GaN and Si is utilized in a 125 W, five phase, 12-to-1 V POL converter that achieves over 95% efficiency.

Similar to the work in Chapter 4, the FOM defined as gate charge multiplied by on-resistance is used to compare transistors. The comparison of the eGaN FET and Si MOSFET used in this work is presented in Table 7.1. Comparing the two devices reveals that the eGaN FET will switch faster; however, the Si MOSFET will reduce conduction loss. This section and the following section compare a GaN-based POL, a Si POL, and a GaN/Si hybrid POL. All three designs are implemented as five interleaved phases to increase output power capability, increase effective frequency, reduce steady-state output ripple, and improve transient response.

Table 7.1: GaN and Si transistor comparison with $V_{GS} \approx 4.5$ V.

Manufacturer	Part Number	Material	V_{DS} (V)	I_D (V)	$R_{DS(ON)}$ (m Ω)	Q_G (nC)	FOM (m Ω x nC)
EPC	EPC2015	GaN	40	33	4	10.5	42
Infineon	BSC010NE2LS	Si	25	100	1.1	27	29.7



Fig. 7.6: One of five GaN/Si hybrid POL converter stages in five phase converter.

Each GaN POL phase is identical to design 3 from Section 3.5 (Fig. 3.17). Each GaN/Si hybrid POL phase is identical to that presented in Chapter 4 and is represented again in Fig. 7.6. Each Si POL is simply the Infineon BSC010NE2LS MOSFET used as the control switch and the SR, and all other design aspects remain unchanged.

The POL converters uses the TI LM5113 gate driver, which has been designed specifically to drive eGaN FETs in a half bridge configuration. The driver has an internal 2.1 m Ω pull-up gate resistance to reduce gate overvoltage, and it uses a bootstrap technique to internally clamp the gate at 5.2 V, which prevents the eGaN FETs from exceeding their gate-to-source voltage limit ($V_{GS,MAX}$) of 6 V [61]. The Si SR is about 150% the size of the eGaN FET but is still quite small compared to similar Si devices. The Si device is also driven with the LM5113 at $V_{GS} = 4.5$ V. Since Si MOSFETs are capable of being driven with a wide range of gate voltages, there is a direct trade-off between V_{GS} , $R_{DS(ON)}$, and Q_G for the Si device. This design drives the Si MOSFET with

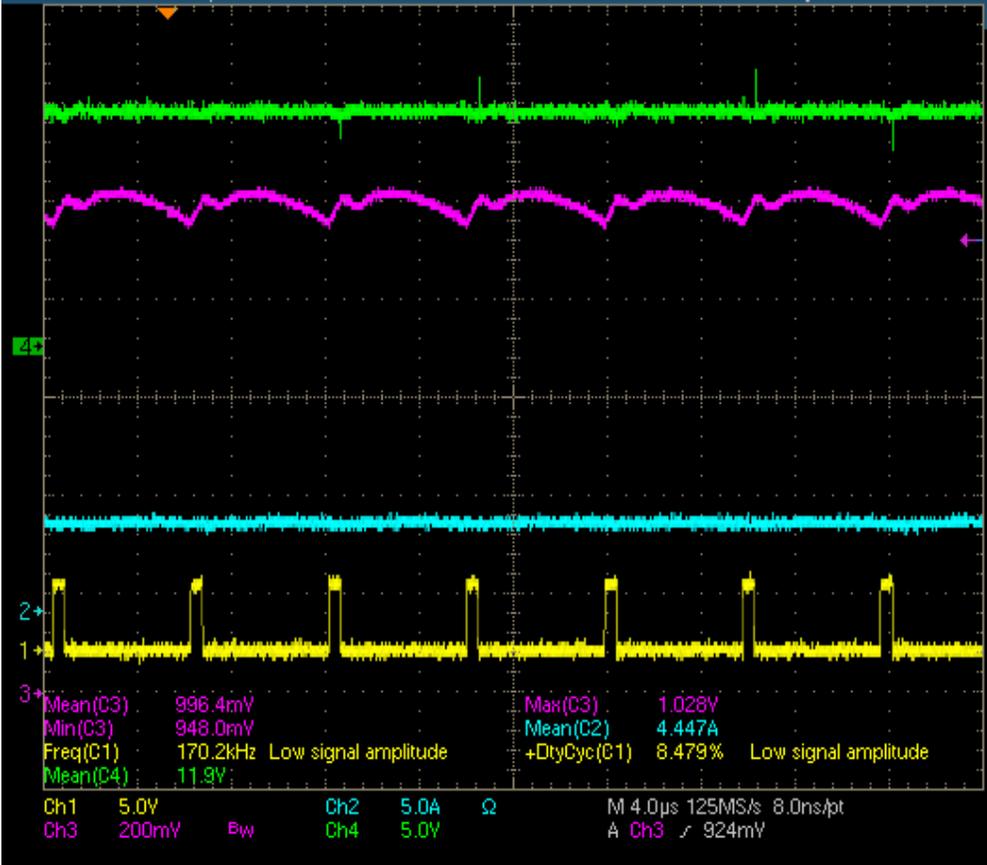
a low gate voltage that results in slightly higher $R_{DS(ON)}$ and lower Q_G . External gate resistors are $0\ \Omega$ resistors because additional gate resistance was not necessary to reduce gate current to prevent overvoltage of the gate. Referring to Fig. 7.6, C2 – C5 are input capacitors, and C9 – C12 are output capacitors. The inductor footprint was designed to accommodate several COTS inductors such as this $2\ \mu\text{H}$, $0.9\ \text{m}\Omega$ Coilcraft SER1410-202 inductor, which was the largest inductance value and was generally the most efficient inductor tested in this design.

Expansion from a single to multiple phases is simple as long as the controller is designed efficiently, the controller is fast enough to manage all active phases, and proper spacing of the PWM signals for interleaving applications can be managed. Each phase has a gate driver but is driven by the same controller; the phases can be synchronous or interleaving. Synchronous phases turn on and off at the same time, while interleaving phases are staggered evenly throughout the period. Interleaving phases have many advantages such as raising the effective output frequency by

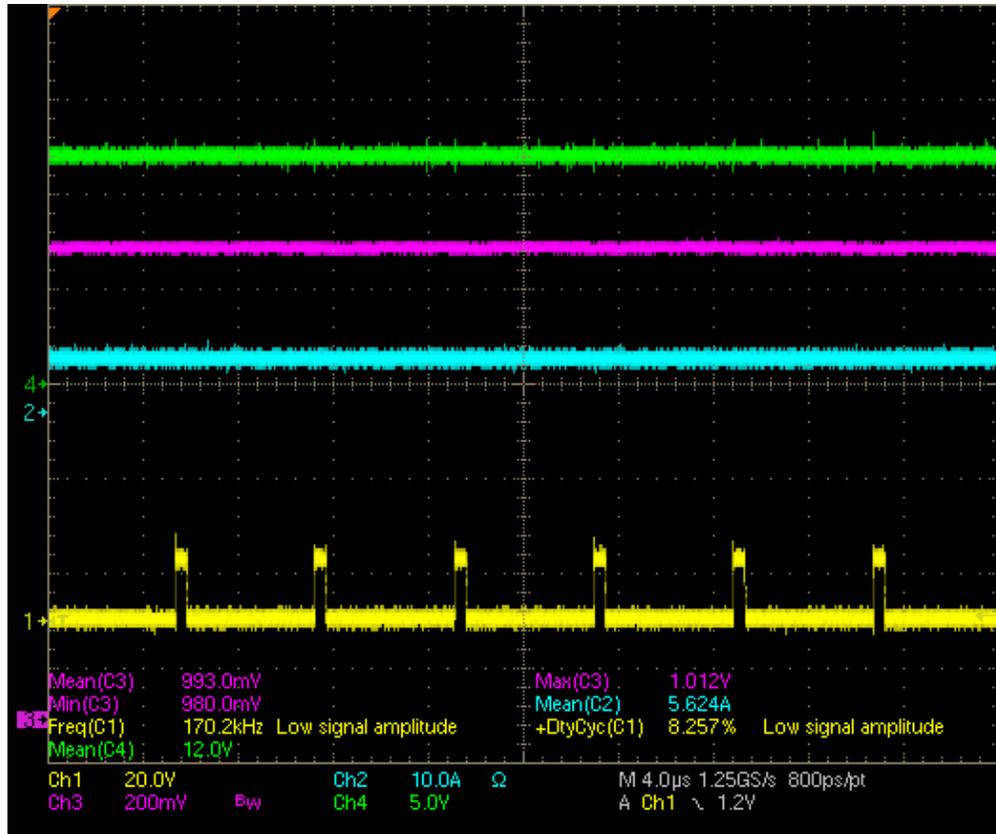
$$f_{eff} = f_s \cdot N, \quad (7.1)$$

where f_{eff} is the effective frequency or frequency of the POL converter output; f_s is the switching frequency of each phase, and N is the number of phases in an interleaved arrangement. Thus, five phases switching at 200 kHz results in a 1 MHz multiphase converter. The higher output frequency significantly reduces output voltage ripple, which can reduce the number and size of the passives required to meet design specifications and thus may reduce size. Additionally, multiphase POL converters respond better to transient loads because the higher effective frequency means that at least one phase is never far from turning on; this does however require a controller with enough bandwidth to sense the change in load and increase the duty cycle to accommodate the change. Fig. 7.7 compares the steady-state 5 A output voltage and current waveforms of a single phase and

an interleaved five phase POL converter. The five phase POL has a much cleaner output waveform. Notice the five phase POL converter has significantly less output voltage ripple. There are many other great advantages of multiphase POL converters such as distributing current to minimize I^2R loss, produces a cleaner output signal, has higher load capability, and can perform phase shedding. Phase shedding promotes high efficiency by dropping phases to operate the remaining phases at the load that yields peak efficiency, similar to the concept of cylinder deactivation in modern vehicle engines.



(a) Single phase POL converter, 5 A output.



(b) Interleaved five phase POL converter, 5 A output.

Fig. 7.7: Comparison of output voltage waveforms (purple) between a single phase POL converter and interleaved five-phase POL converter.

7.2.2 Five phase GaN vs. Si vs. GaN/Si

The GaN/Si hybrid POL converter significantly improves efficiency beyond similar Si-based designs, and it improves high load efficiency beyond the ability of GaN-based designs. Fig. 7.8 compares experimental efficiency of a Si-based, a GaN-based, and a GaN/Si hybrid POL converter. These three converters are all interleaved five phase synchronous buck converters capable of more than 125 A load current. All three converters utilize the same controller, inductors, capacitors, and gate drivers. The only changes between them are the SRs. The SR of the GaN-based POL converter is two EPC2015s in parallel to yield an effective on-resistance $R_{DS(ON),EFF} =$

2 mΩ, which is still twice that of the Si SR. Additionally the two parallel GaN FETs in the SR have an effective gate charge $Q_{G,EFF} = 21$ nC.

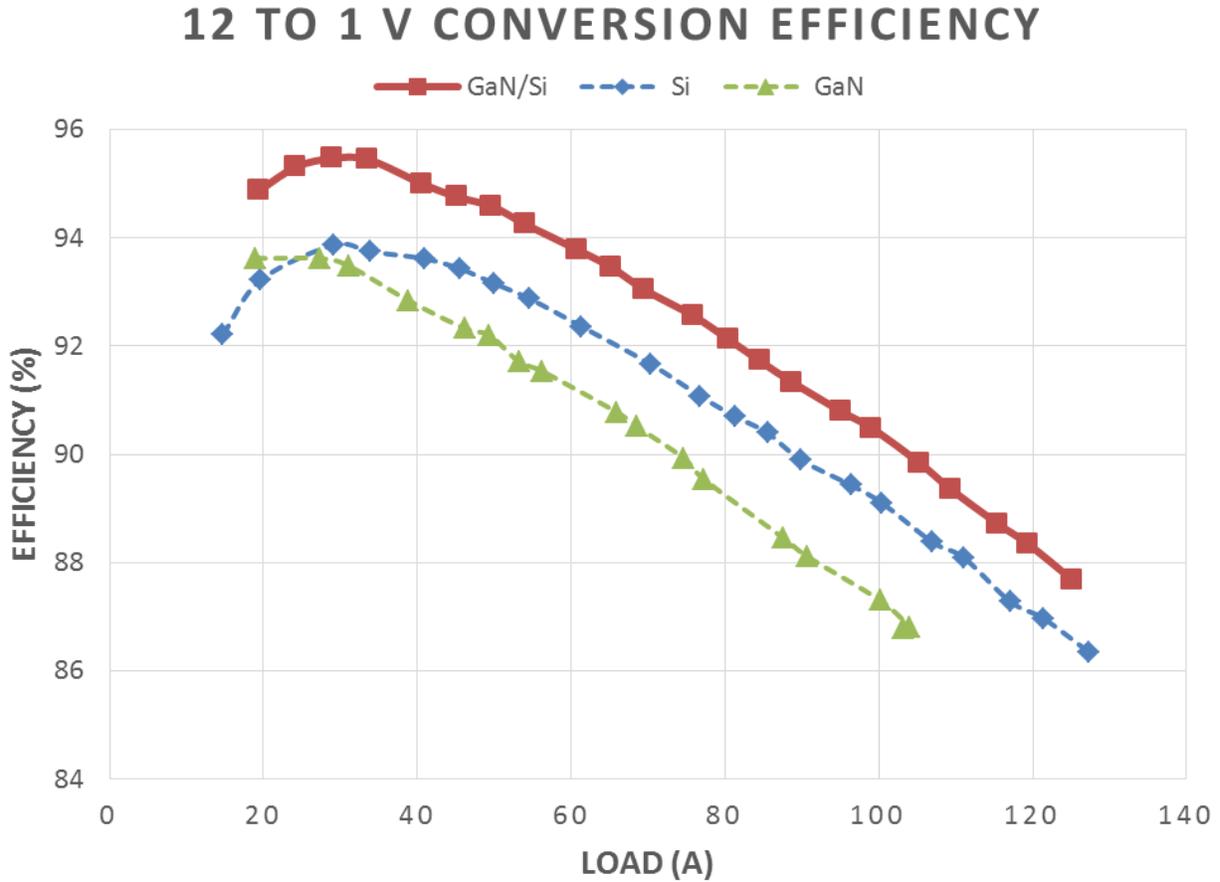


Fig. 7.8: Efficiency comparison of a Si-based, a GaN-based, and a GaN/Si hybrid POL converter (each an interleaved five phase synchronous buck converter topology)

7.2.3 Thermal Analysis of GaN/Si Hybrid POL

Each GaN/Si hybrid POL phase is approximately 0.74 in² and can be nearly half this size with the inductor mounted on the backside of the PCB. Fig. 7.9 includes thermal images of the GaN/Si hybrid POL converter at 25 and 100 A without any forced cooling. The thermal images are upside-down relative to Fig. 7.6. In both designs, “A” represents the GaN control switch and “B” denotes the Si SR. Both the control switch and SR are similar in temperature, even though the

SR conducts for nine times as long as the control switch; with that said, the SR also has a larger surface area to dissipate heat.

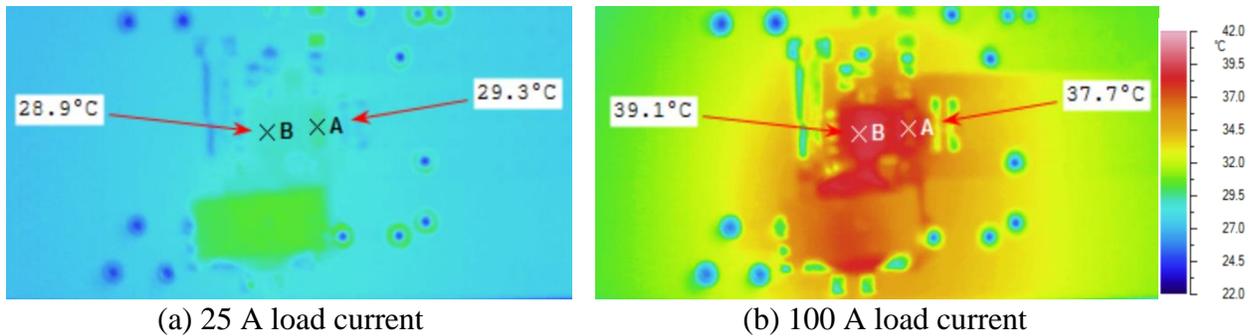


Fig. 7.9. Thermal images of one GaN/Si POL converter phase.
No forced cooling and $T_{\text{ambient}} = 23.3 \text{ }^{\circ}\text{C}$.

GaN certainly has some remarkable characteristics – particularly switching around three times faster than Si. There is certainly a bright future for GaN semiconductors, and they will continue to improve. Nevertheless, there are still some applications best suited for Si, and perhaps some applications that are best when utilizing GaN and Si. Experimental results show that the GaN POL converter is dominated by conduction loss at high loads, whereas the Si POL converter is dominated by switching loss at light loads. However, the GaN/Si hybrid approach yields improved efficiency over a large load range and offers exceptional power density. Since the EPC GaN FET still proved to be the best applicant for the control switch, the conclusion is that, with the current semiconductor market, a combination of GaN and Si can produce better high load results than either technology can independently. The expectation is that eventually, as GaN transistors mature, GaN power semiconductors will surpass Si with very low $R_{\text{DS(ON)}}$ and low Q_{G} ; however, at this time, the GaN/Si hybrid POL converter approach improves high load performance in the 12-to-1 V POL application.

7.3 POL Version 5 Design

Although the GaN/Si design from Section 7.2 optimizes conversion efficiency at very high load currents, a GaN design has some operating ranges (i.e. light load and high frequency) where it is unmatched and is thus pursued further to improve upon previous GaN designs. POL Version 5 was designed to be a more power dense prototype than Version 3. All phases are on the same PCB and located closer together to reduce output conduction loss, which can be large when operating above 100 A.

Version 5 is a 10 layer PCB. Every other layer (inner 1, 3, 5, 7, and bottom Cu) are all ground layers. Version 3 prototypes were only 6 layer PCBs. Several layers are nearly duplicated, and ten layers are used to reduce Cu losses to the output terminals, as the output is capable of reaching as much as 150 A. The COTS TI DSP controller card is located near the bottom of Fig. 7.10, and several additional communication ICs, accompanying passives, and headers are located below the controller. Directly above the controller are resistor dividers for the current sense lines from each phase. Slightly above the middle of the PCB, five identical GaN synchronous buck converters are located side-by-side. Input and output terminals are all located at the top of the board, and two 5 V terminals are used to measure power consumption by the DSP controller and communication integrated circuits (ICs) separately from the gate drivers.

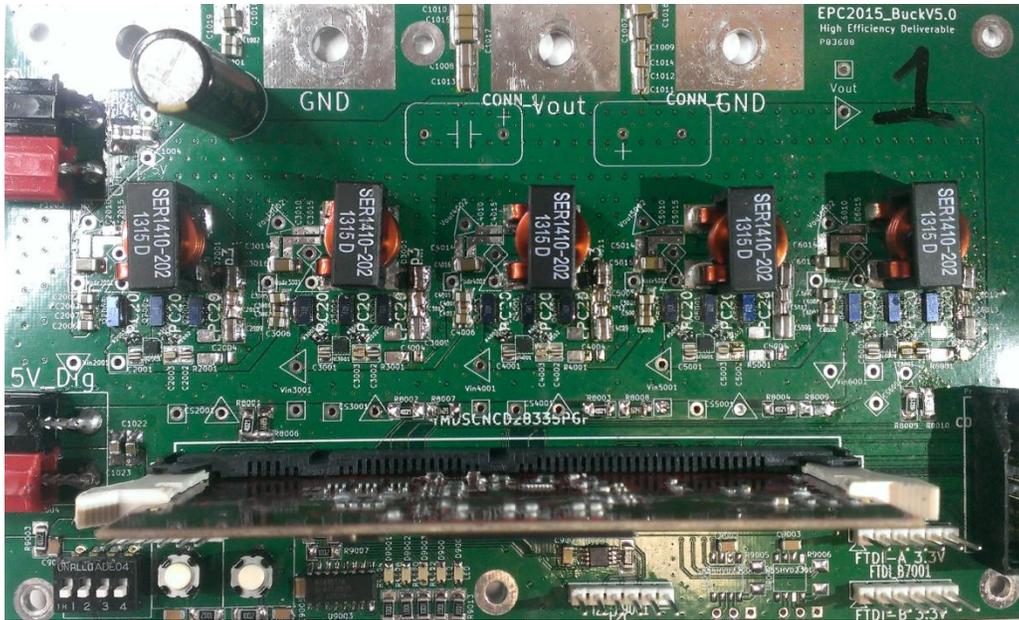


Fig. 7.10: POL Version 5 prototype.

7.3.1 POL Version 5 Efficiency

Compared to the best commercial and published POL converters at similar operating conditions, Version 5 achieves significantly improved efficiency (5-12% improvement). Maximum efficiency is realized at 25 A at over 96%. Efficiency vs. load is presented for several frequencies in Fig. 7.11 – Fig. 7.14. As frequency increases, efficiency decreases slightly. The advantage, however, to increasing frequency is the ability to reduce the size of the passives and improve transient analysis. This is a trade-off to be tailored to a specific design. The effect of frequency on efficiency is presented in Fig. 7.15.

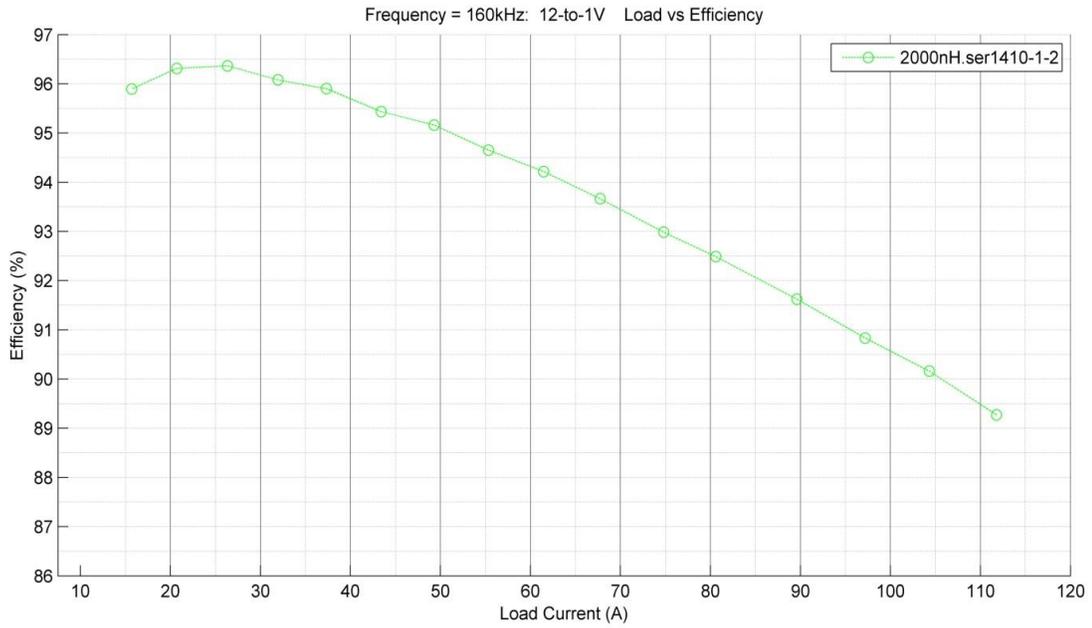


Fig. 7.11: Efficiency vs. load ($f = 160 \text{ kHz}$, $f_{\text{eff}} = 800 \text{ kHz}$).

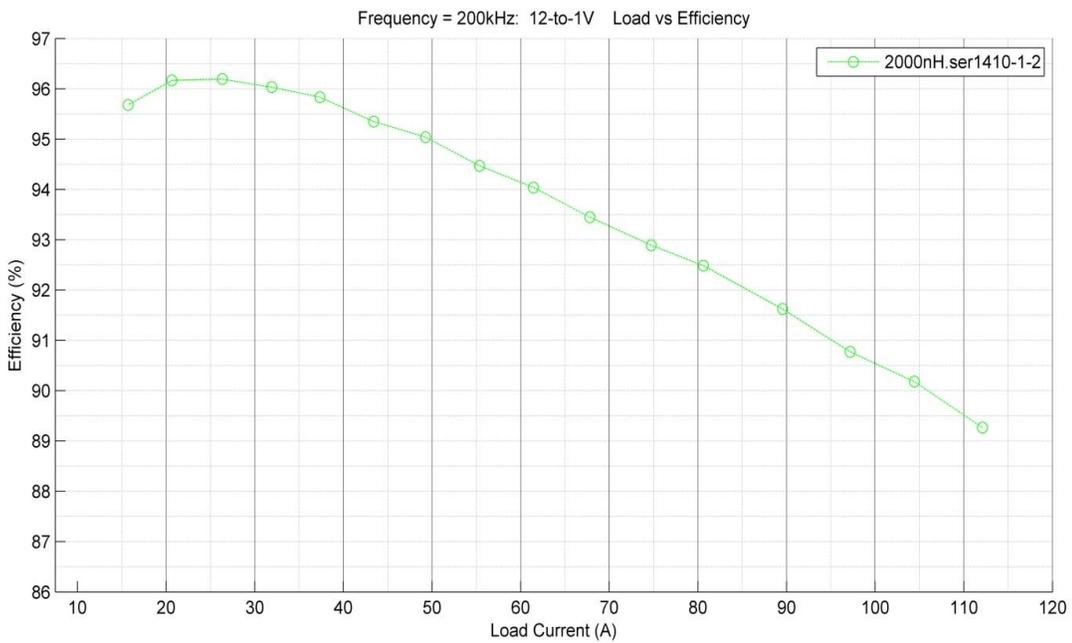


Fig. 7.12: Efficiency vs. load ($f = 200 \text{ kHz}$, $f_{\text{eff}} = 1 \text{ MHz}$).

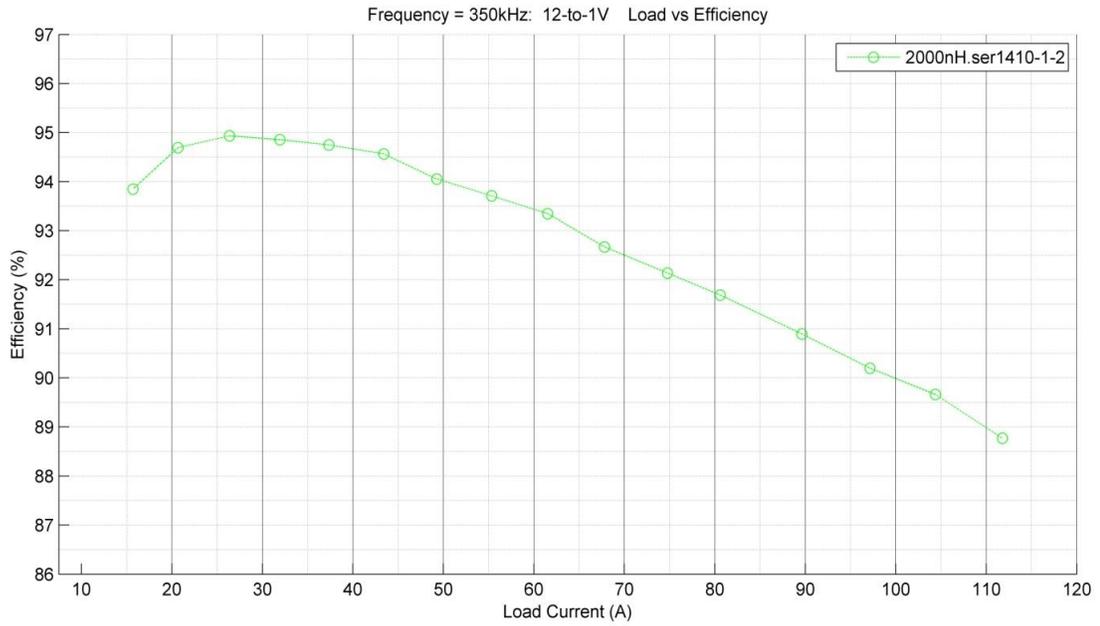


Fig. 7.13: Efficiency vs. load ($f = 350 \text{ kHz}$, $f_{\text{eff}} = 1.75 \text{ MHz}$).

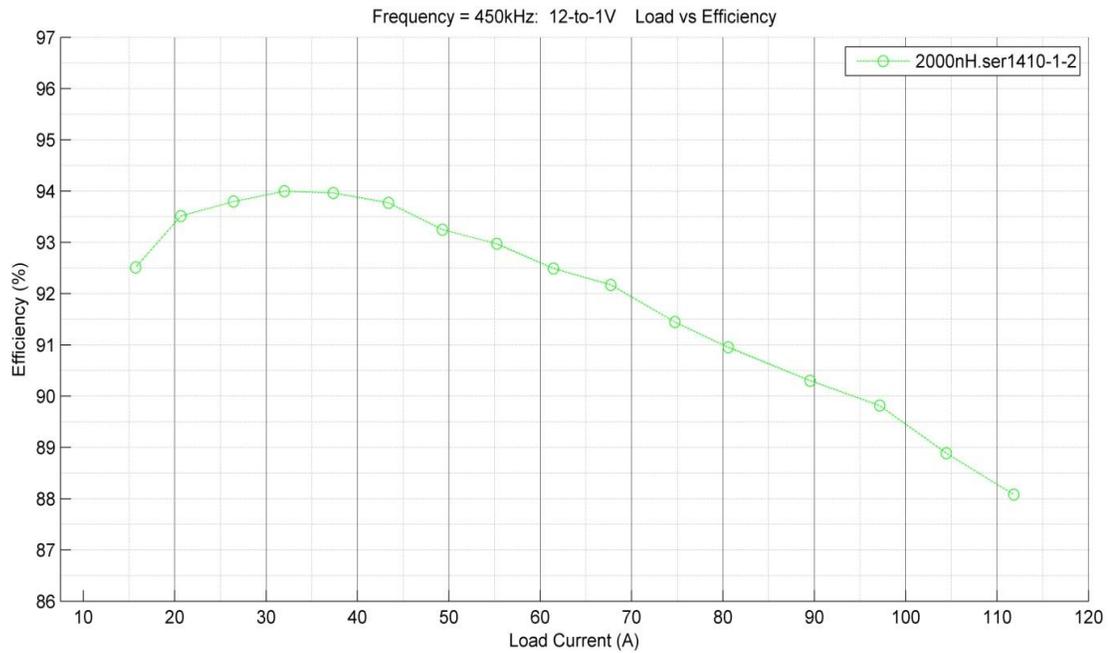


Fig. 7.14: Efficiency vs. load ($f = 450 \text{ kHz}$, $f_{\text{eff}} = 2.25 \text{ MHz}$).

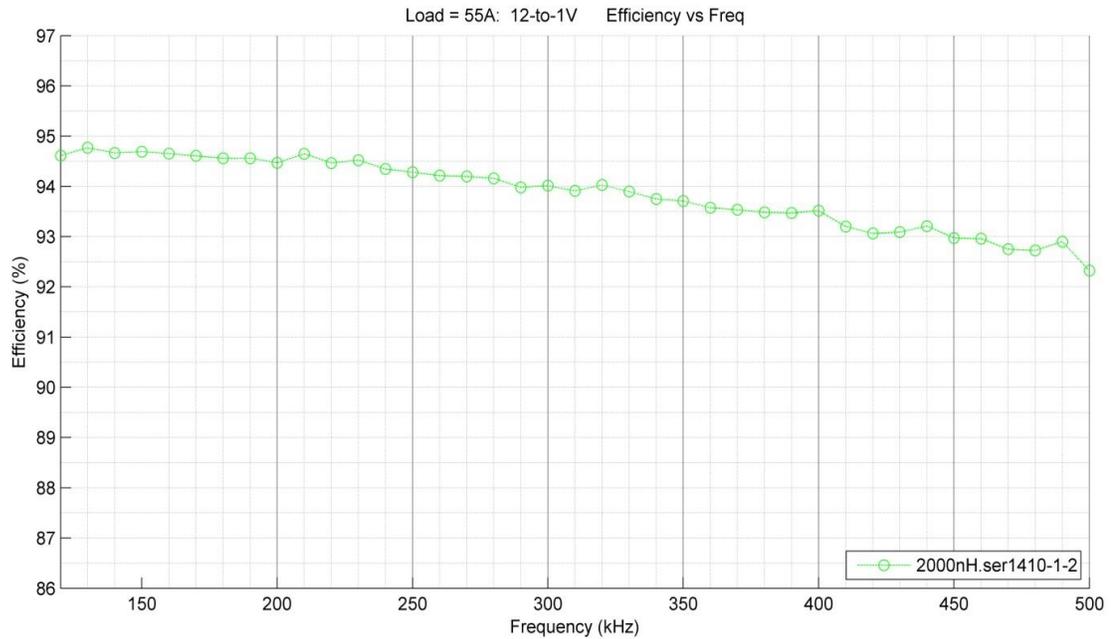


Fig. 7.15: Efficiency vs. frequency at 55 A.

It is very practical to operate this POL converter at lower frequency, since the effective frequency is multiplied by the number of phases. That means transient response should be improved with an increase in phases, the inductance can be decreased without increased output ripple, and size of each phase can be reduced. To ensure reasonable current sharing and verify that devices operate well beneath their thermal limits, thermal images were taken at 20 and 50 A load in Fig. 7.16 and Fig. 7.17, respectively.

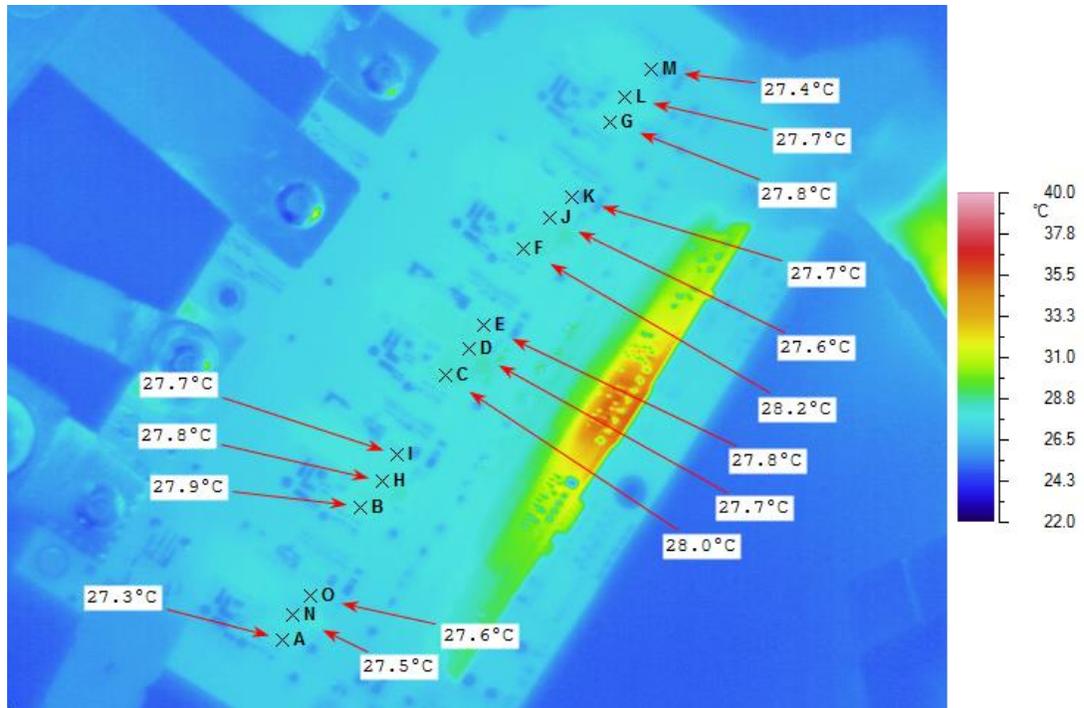


Fig. 7.16: Thermal image of Version 5 operating at 20 A load ($T_{MAX} = 28.2\text{ }^{\circ}\text{C}$).

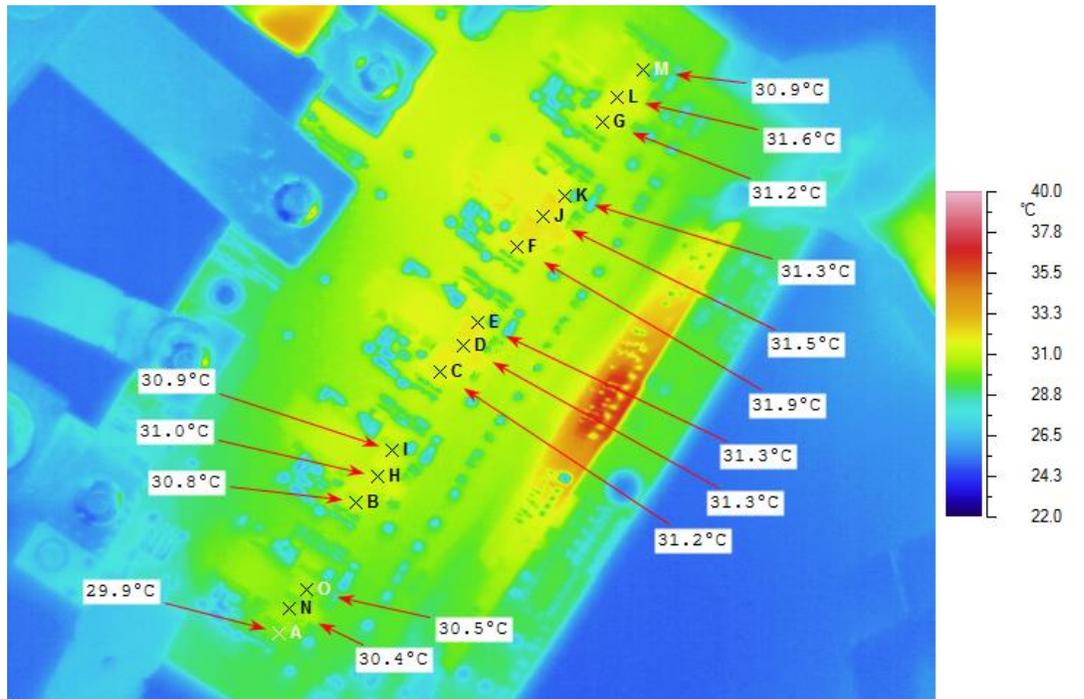


Fig. 7.17: Thermal image of Version 5 operating at 50 A load ($T_{MAX} = 31.9\text{ }^{\circ}\text{C}$).

The GaN POL Version 5 converter is currently in a pre-production state. The topology, layout, and components have been optimized for a wide range of input and output voltages ($V_{IN} = 2 - 24 \text{ V}$ and $V_{OUT} = 0.5 - 5 \text{ V}$), and only slight design modification would be needed for voltages outside of this range. The five phase POL can operate from 0 – 150 W with ideal performance (>90% efficiency) between 15 and 105 W. Higher power requirements could be met by adding additional phases. With this design, unwanted components and test points would be removed, and size would decrease for a commercial product, resulting in a power density of approximately 270 W/in^3 . Ideally, the controller would be implemented in an ASIC to reduce size drastically and to reduce the power consumption of the digital controller. The final performance of the five-phase GaN/Si hybrid POL converter is compared to several commercial and research prototype POL converters in Fig. 7.18. From this figure, it is evident that this design operates at much higher load and much better efficiency than alternative POL converters.

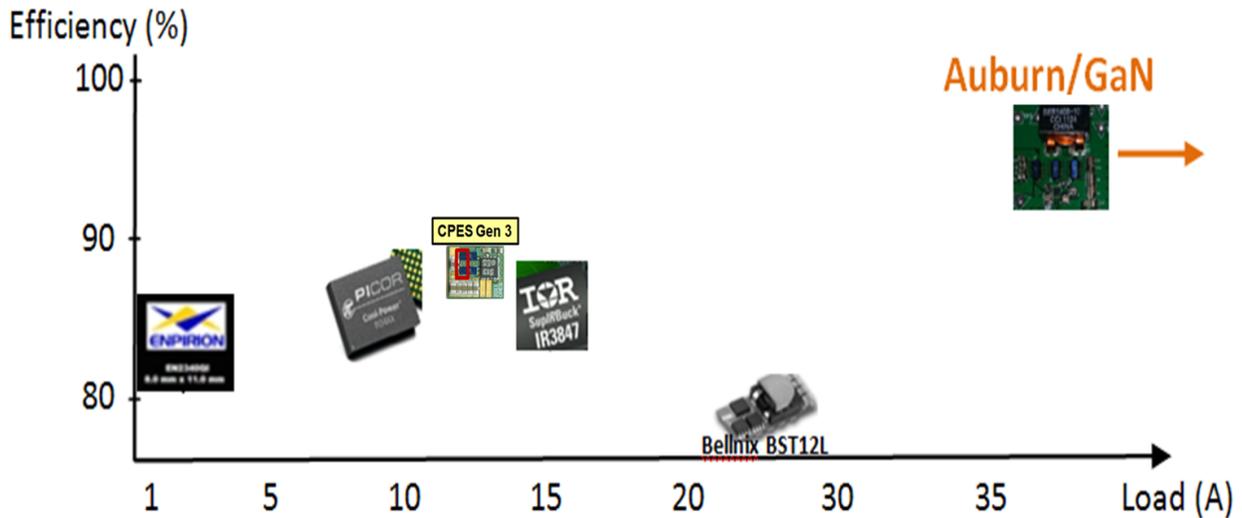


Fig. 7.18: Auburn GaN POL prototype compared to state-of-the-art commercial 12-to-1 V POLs and best WBG prototypes.

CHAPTER 8

WBG DATA CENTER POWER SUPPLY CHAIN

It has been established that energy consumption of most commercial data centers is high and power conversion efficiency is low because more than half of the power is consumed during power conversion, distribution, and cooling. This chapter discusses the design of three WBG power conversion stages that rectifies and converts 480 V three-phase (3ϕ) AC to ~ 1 V DC. This system architecture is presented in Fig. 8.1, and this system approach employs WBG power devices, including SiC and GaN FETs and diodes, which helps to increase converter efficiency and power density. Scaled down prototypes of all power conversion stages in the data center power supply chain have been designed, built, and tested. The advantages of utilizing WBG power devices are illustrated through simulations and then verified by experimental results. This chapter provides a system level view of the WBG architecture and analyzes each stage individually.

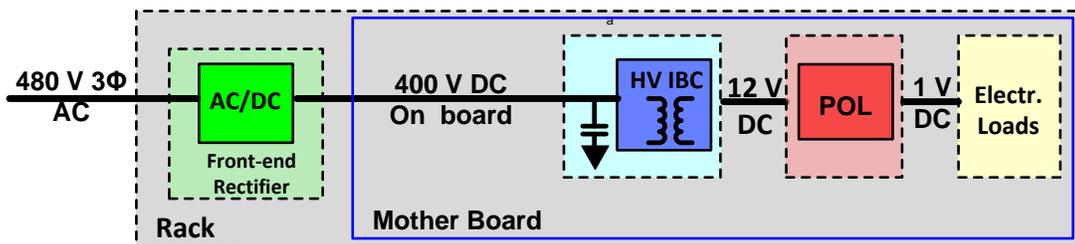


Fig. 8.1: Three stage WBG power conversion architecture.

Compared to a full-scale system, the prototype power ratings have been scaled down for demonstration purpose. The front end rectifier was selected to be 7.5 kW. Three front end rectifiers are located in parallel to power a 19 kW load with a 2+1 redundancy structure. The power rating of each blade (or drawer) is 1600 W, which is divided into four quadrants. Each quadrant is rated at 400 W which is met by three 300 W IBCs and four 150 W POLs. The additional IBC and POL power capacity provides N+1 redundancy for each conversion stage.

Overall system efficiency of 89.6 % has been reached at full load with WBG devices in all three power stages calculated as the product of each power stage's individual efficiency. This is 3% higher than the highest Si efficiency based on theoretical maximum calculations. A 3% increase in the world's data center supply chains would result in a savings of 3.6 TWh per year [62].

$$\begin{aligned} 3.6 \text{ TWh} &= 3.6 \times 10^{12} \text{ Wh} \\ &= 3,600,000,000,000 \text{ Wh} \end{aligned} \quad (8.1)$$

That is enough energy to power 332,000,000 average households in the US for a year. In the following three sections, each of the three power stages will be introduced in detail.

8.1 Intermediate Bus Voltage

The system architecture in Fig. 8.1 is a starting point but is still flexible. For instance, the input voltage to the front end rectifier can be 480 V 3 ϕ AC, which is common in the US, or it can be a range of HVDC. The 400 V DC bus was chosen to distribute through the cabinet because 400 V is an ideal output for front end rectifier efficiency, it reduces current to reduce transmission loss within the rack, and 400 V can be implemented without overly complicated safety protocol. Since the load determines the output of the POL, there is only one intermediate voltage that can be tuned for best system performance: the intermediate bus voltage. The intermediate bus voltage is defined as the output of the IBC and the input to the POL, and an investigation has been performed to determine the optimum DC voltage for this bus.

The IBC is an LLC resonant converter which is DC isolated; however, the output voltage is unregulated (Fig. 8.2). Therefore, the intermediate bus voltage is unregulated but the turns of the transformer in the IBC determines the approximate intermediate bus voltage. The intermediate

bus voltage will usually drop as load increases due to additional loss in the IBC. The synchronous buck converter is a non-isolated, highly regulated topology (Fig. 8.3). Therefore, it can compensate for large shifts in intermediate bus voltage. These two stages work harmoniously to compensate for each other's shortcomings. The IBC provides DC isolation for the POL and the POL regulates the output for the IBC. Working together, these two stages form what will be referred to as the intermediate bus architecture (IBA). The IBA is presented in Fig. 8.4. The input and output to the IBA is predetermined; however, the intermediate bus voltage (V_{int}) may still be determined by the system designer.

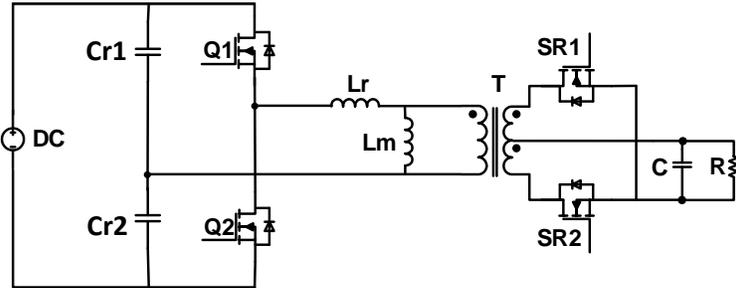


Fig. 8.2: Topology of LLC converter.

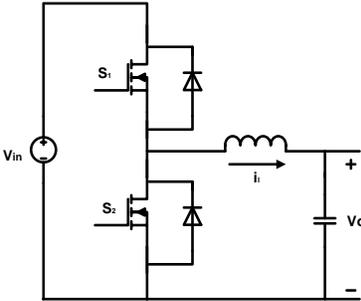


Fig. 8.3: Topology of buck converter.



Fig. 8.4: Intermediate bus voltage optimization [63].

The goal is to determine maximum efficiency of the IBA without sacrificing reliability, steady-state output signal, and output transient performance. Table 8.1 – 8.3 list the specifications, devices selection and transformer design of the LLC and buck converters with different intermediate bus voltages. All of these factors must be considered in order to calculate

losses for both systems. Efficiency for the IBC and POL were calculated and plotted against output power (Fig. 8.5 and Fig. 8.6). By combining this data, Fig. 8.7 represents the IBA losses at various intermediate bus voltages ranging from 4 V to 24 V.

Table 8.1: Specifications and device selection of LLC converter at different bus voltages [63].

Parameter		Value
Input Voltage		400 V
Output Voltage		4...24 V
Power Rating		300 W
Switching Frequency		1 MHz
Primary side MOSFET		Transphorm 600 V
SR	4-8 V	Infineon 25 V
	10-12 V	EPC 40 V
	24 V	EPC 100 V

Table 8.2: Transformer design with different bus voltages [63].

Output Voltage	Copper Thickness	Core Type	Turns ratio
24, 12, 10, 8V	Primary: 2 oz	E22/6/16 PLT22/16/2.5	8, 16, 20, 24
6, 4 V	Secondary: 2 oz	2 *E18/4/10 PLT18/10/2	32, 48

Table 8.3: Specifications and device selection of buck converter at different bus voltages [63].

Parameter		Value
Input Voltage		4...24 V
Output Voltage		1 V
Power Rating		30 W
Switching Frequency		200 kHz
Inductor		1 μ H CoilCraft XAL1010
MOSFET	4 V	Greatwall 7 V
	6-12 V	Infineon 25 V
	24 V	EPC 40 V

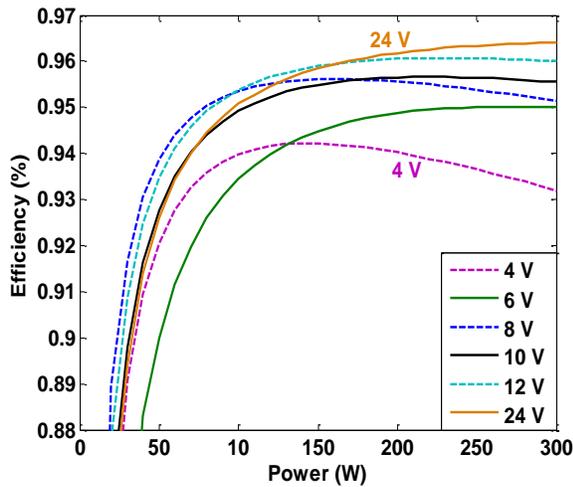


Fig. 8.5: LLC efficiency at different bus voltage [63].

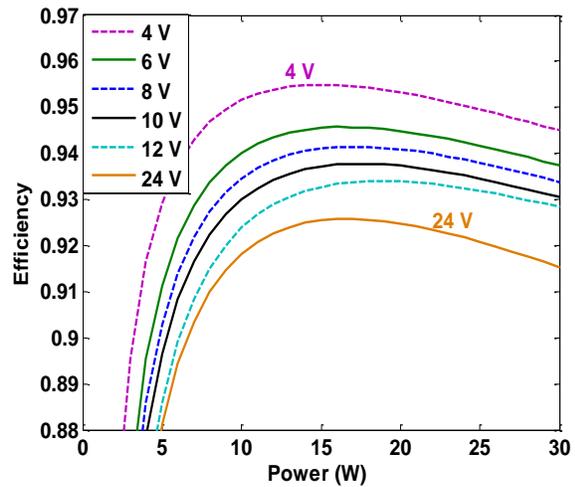


Fig. 8.6: Buck efficiency at different bus voltage [63].

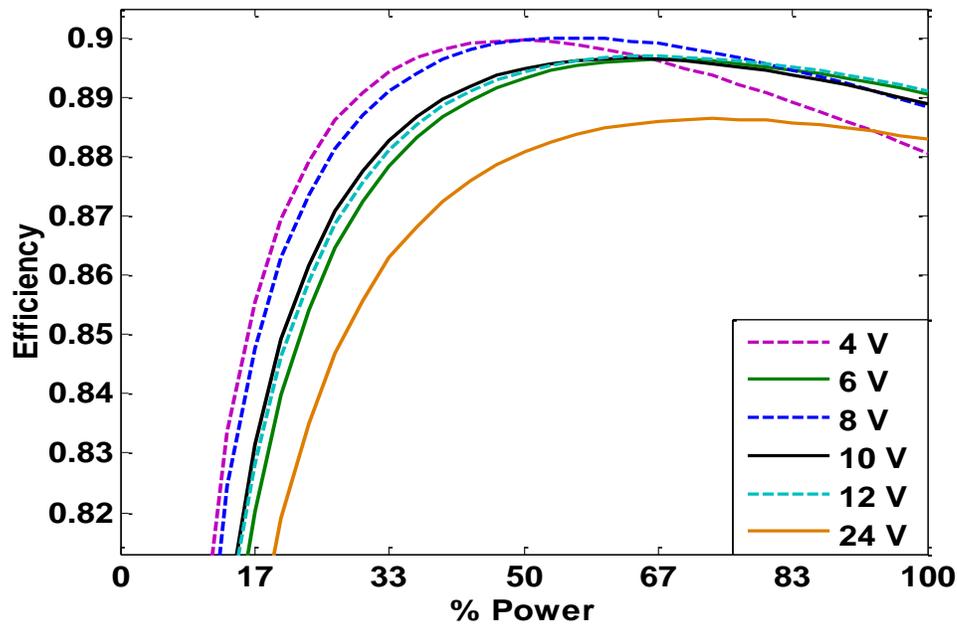


Fig. 8.7: IBA system efficiency at different bus voltage [63].

As calculations will generally indicate, the efficiency of each system will decrease as the ratio V_{IN}/V_{OUT} increases. The synchronous rectification on the secondary side of the LLC resonant converter will inherit additional conduction loss if the intermediate bus voltage is decreased. Meanwhile, the synchronous buck converter reduces conduction loss in the SR due to freewheeling

current under the same conditions. Additionally, the synchronous buck converter is limited in conversion ratio as ratios greater than 24-to-1 reduce the duty ratio to a very inefficient and small value. Thus, intermediate bus voltages above 24 V were not explored. In the end, a 12 V intermediate bus was selected based on calculated results. Interestingly, 12 V has been the input to POLs in similar systems for many years.

8.2 Front End Rectifier

The front end rectifier (FER) is the first stage in the power supply chain. The specifications for the WBG prototype are listed in Table 8.4 and the topology used to implement this stage is presented in Fig. 8.8. Two major designs have been implemented. The first design uses Si IGBTs with 1200 V Si diodes. The second design uses SiC MOSFETs with 1200 V SiC Schottky barrier diodes. Both designs have been tested and compared to determine the advantages of a WBG FER. Major parameters of interest include system loss, volume, and weight. These parameters are compared in Fig. 8.9.

Table 8.4: FER specifications.

Power rating	7.5 kW
Input voltage	3 phase 480 V _{ac}
Input range	± 10%
Input current	9 A
Output voltage	400 V _{dc}
Output current	18.75 A
Input power factor	> 0.99
Current total harmonic distortion	< 5%
Operating temperature	50 °C
EMC standard	EN55022 Class B

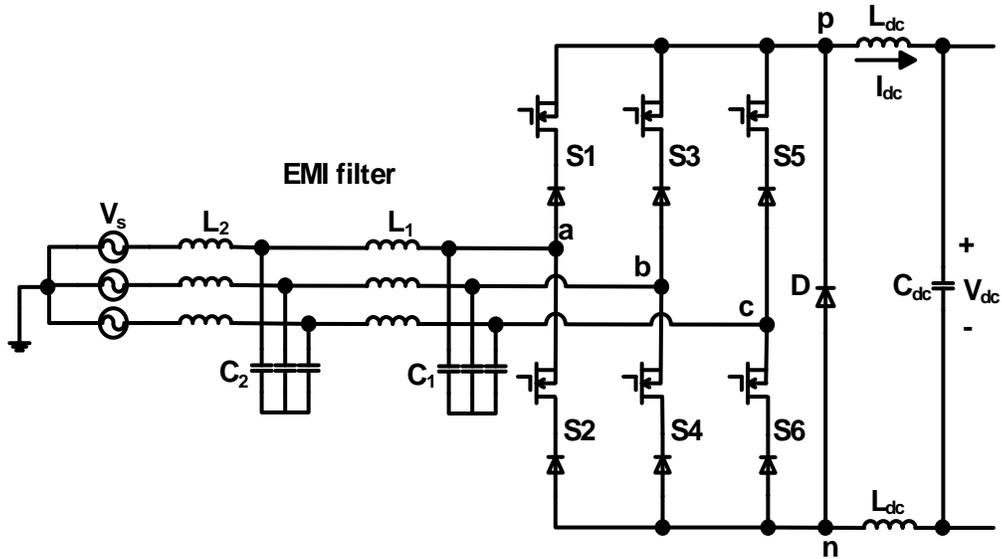


Fig. 8.8: Three phase buck rectifier topology.

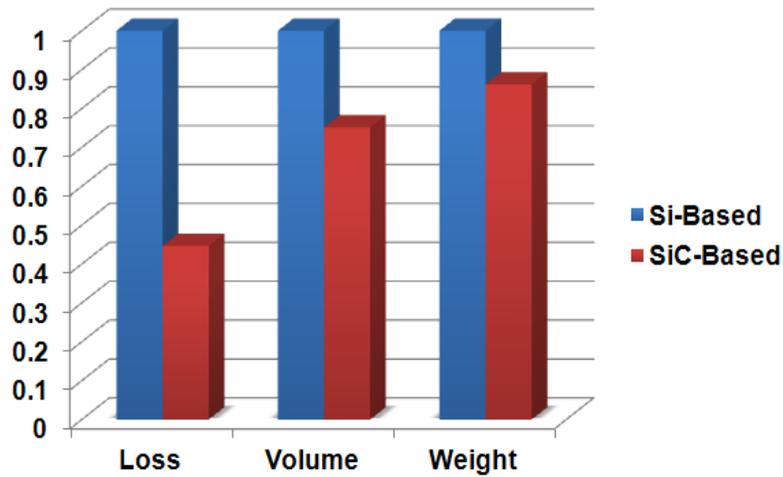


Fig. 8.9: Loss, volume, and weight compared in Si and SiC FERs [64].

The Si FER operates at 20 kHz; however, the faster switching speeds of SiC allow the SiC design to switch at 28 kHz. The increase in switching frequency allows the system to reduce the size of the magnetic components, which results in the majority of the volume and weight reduction. Even with 40% higher switching frequency, the SiC FER reduces converter loss by a combination of lower switching and conduction loss. The prototype and input/output waveforms are presented

in Fig. 8.10 and Fig. 8.11, respectively. Waveforms were captured at full load with 480 V 3 ϕ AC line-to-line input, input power factor of 0.9996, input current total harmonic distortion (THD) of 2.9%, and an output of 400 V DC [64]. Each transistor and diode in the FER topology can be a single device or multiple parallel devices. Since efficiency is of the utmost importance, several variations of parallel SiC MOSFETs and diodes were tested to obtain the best efficiency from this subsystem. See Fig. 8.12 for efficiency analysis. For best full load performance, four MOSFETs and two diodes yield best results but not much improved from the addition of the last MOSFET.



Fig. 8.10: Three phase SiC FER prototype [9].

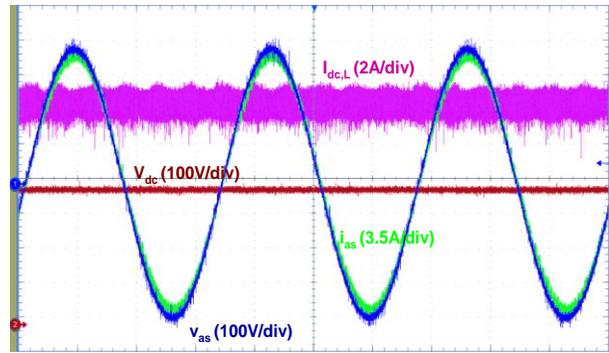


Fig. 8.11: Three phase SiC FER inputs and outputs (V_{IN} , I_{IN} , V_{OUT} , I_{OUT}) [9].

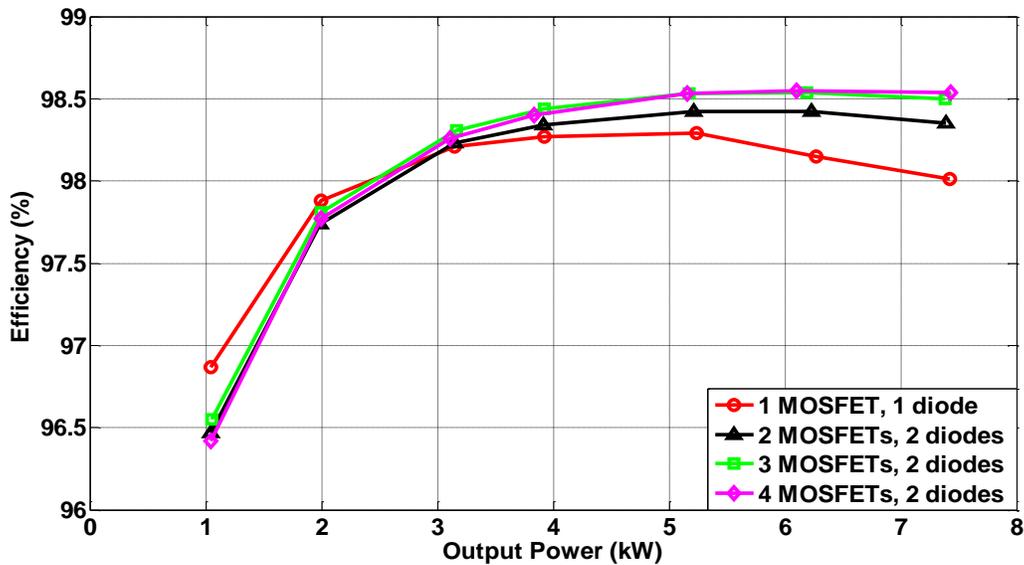


Fig. 8.12: Efficiency analysis of three phase FER with different parallel SiC MOSFET and diode combinations [9].

8.3 Intermediate Bus Converter

The IBC is located on the motherboard very close to the POL and to the processor, DRAM, or other electronic load. Therefore, size and efficiency are very important. Output waveform is not as important in the IBC, as the POL acts as a buffer between the IBC and load. The LLC resonant topology with a half-bridge primary and half-bridge synchronous secondary with a center tap transformer is shown in Fig. 8.13, and the specifications for the WBG IBC prototype are given in Table 8.5. The LLC resonant topology enables lossless zero voltage switching (ZVS) of the primary side throughout the entire load range and zero current switching (ZCS) of the secondary side at the resonance frequency.

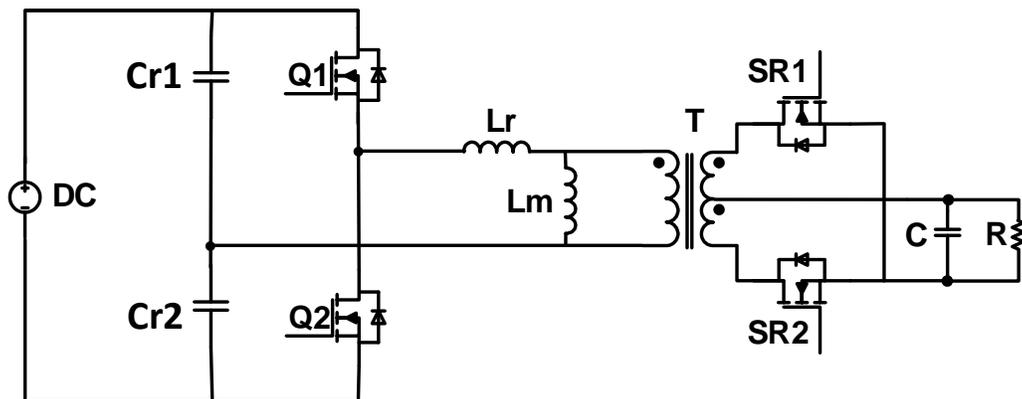


Fig. 8.13: IBC topology (dual half-bridge LLC resonant converter).

Table 8.5: IBC specifications.

Power rating	300 W
Input voltage	400 V _{DC} (±1%)
Output voltage	11.5 V - 13.5V (12 V nominal)
Switching frequency	1 MHz
Hold up time	20 ms

Two LLC resonant converters were build and tested to compare the best Si and WBG components. The Si design uses Infineon CoolMOS for the primary and Infineon OptiMOS for the secondary synchronous rectification. The GaN design uses 600 V Transphorm cascode GaN HEMTs for the primary and 40 V EPC eGaN HEMTs for the secondary synchronous rectification. The current in the primary side devices is negatively related to the output capacitance. Thus, low output capacitance is desired to reduce transformer winding loss. Table 8.6 compares output capacitance of the Si and GaN devices. The GaN devices have up to 50% lower output capacitance, which should reduce transformer winding loss.

Table 8.6: Output charge comparison between Si and GaN primary and secondary devices.

400 V-12 V LLC Resonant Converter	Output charge of each primary side device (nC)	Output charge of each SR device (nC)	Winding charge (nC)
Si	105	31.2	52
GaN	52	18.6	52

The calculated loss of the Si and GaN IBCs at full load (330 W) is compared in Fig. 8.14. The GaN design reduces overall loss by 12%. The efficiency improvement due to GaN transistors is limited as the transformer is the dominant source of loss in the LLC resonant topology. However, a closer look reveals that the primary side device loss is reduced by 38% and the secondary side device loss is reduced by 26% compared to the Si alternative. The GaN IBC prototype is also presented in Fig. 8.15. The prototype has an externally mounted planar transformer on a 12 layer PCB with a turns ratio of 16:1. Each PCB layer is 2 oz. Cu and the transformer windings are

interleaved. The transformer core is a MnZn-Ferrite N49 core material in the ER23/5/13 core geometry.

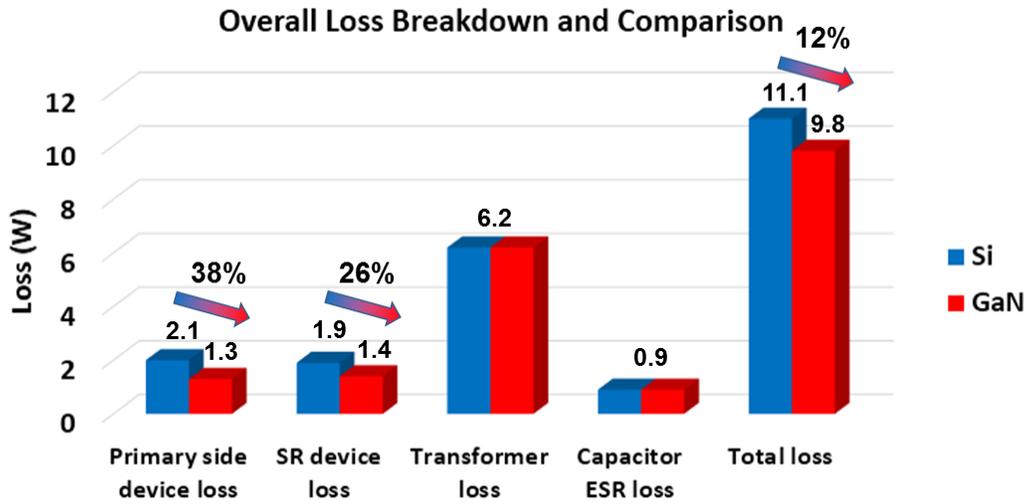


Fig. 8.14: IBC Si and GaN loss comparison [9].

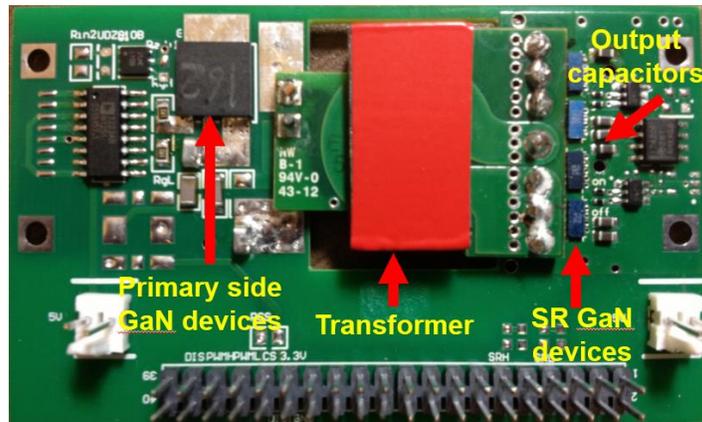


Fig. 8.15: GaN IBC prototype [9].

Si and GaN IBC input/output waveforms are very similar and shown in Fig. 8.16; the noticeable difference in switching figures is the faster, cleaner switching from the GaN IBC, particularly at turn-on. Efficiencies of the two designs are compared in Fig. 8.17. Again, efficiency is not drastically improved since the transformer dominates the loss of this design.

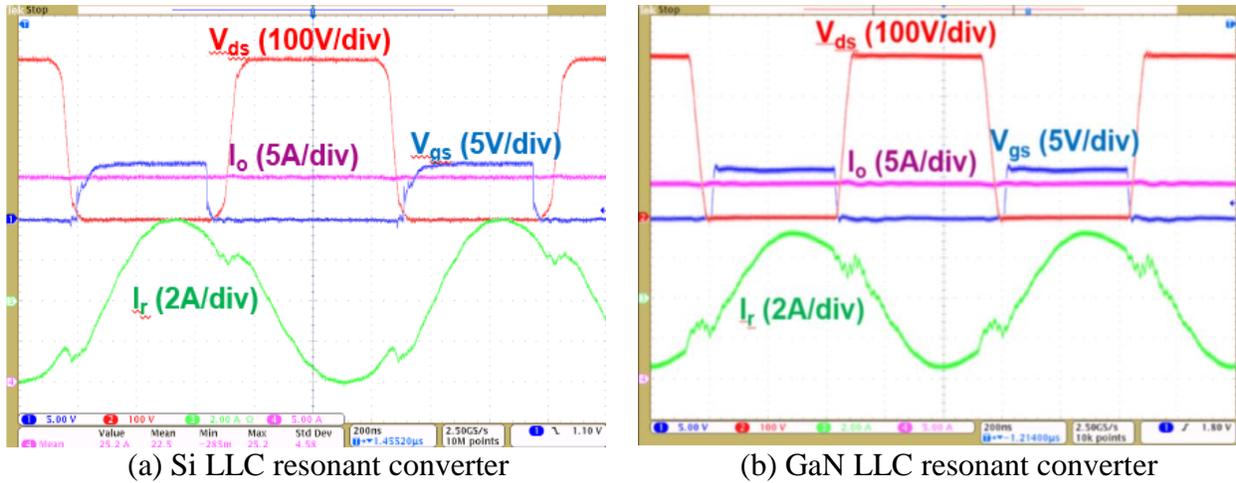


Fig. 8.16: Analysis of LLC resonant converter switching and output [9].

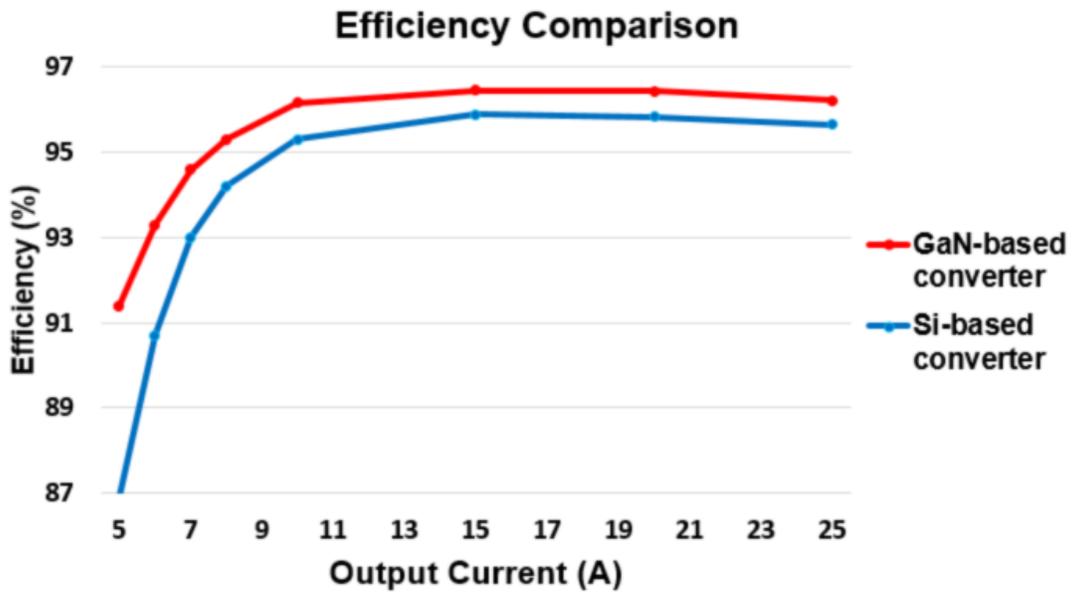


Fig. 8.17: Efficiency of GaN and Si LLC resonant converter ($V_{IN} = 400\text{ V}$, $V_{OUT} \approx 12\text{ V}$) [9].

8.4 Point of Load Converter

The POL converter in this architecture has been discussed thoroughly in Section 7.3 of this text. It is a five-phase eGaN-based synchronous buck converter that is rated at 150 W. With the N+1 redundancy of this architecture, each POL operates at only 100 W under maximum load

conditions. However, in the event that a POL becomes inoperable, the remaining three POLs each operate at 133 W. Thus, the POL stage in each quadrant of the motherboard is 3+1 redundant. In the event of a POL failure, the system can flag the failure, but the remaining POLs meet the power requirements until maintenance can be completed. The efficiency of the 850 kHz effective frequency five-phase POL converter is presented in Fig. 8.18. Under normal operating conditions, less than 100 A, the POL efficiency is greater than 90%. At partial load and with implementation of phase shedding, the POL can operate above 95% efficiency for a very large operating range.

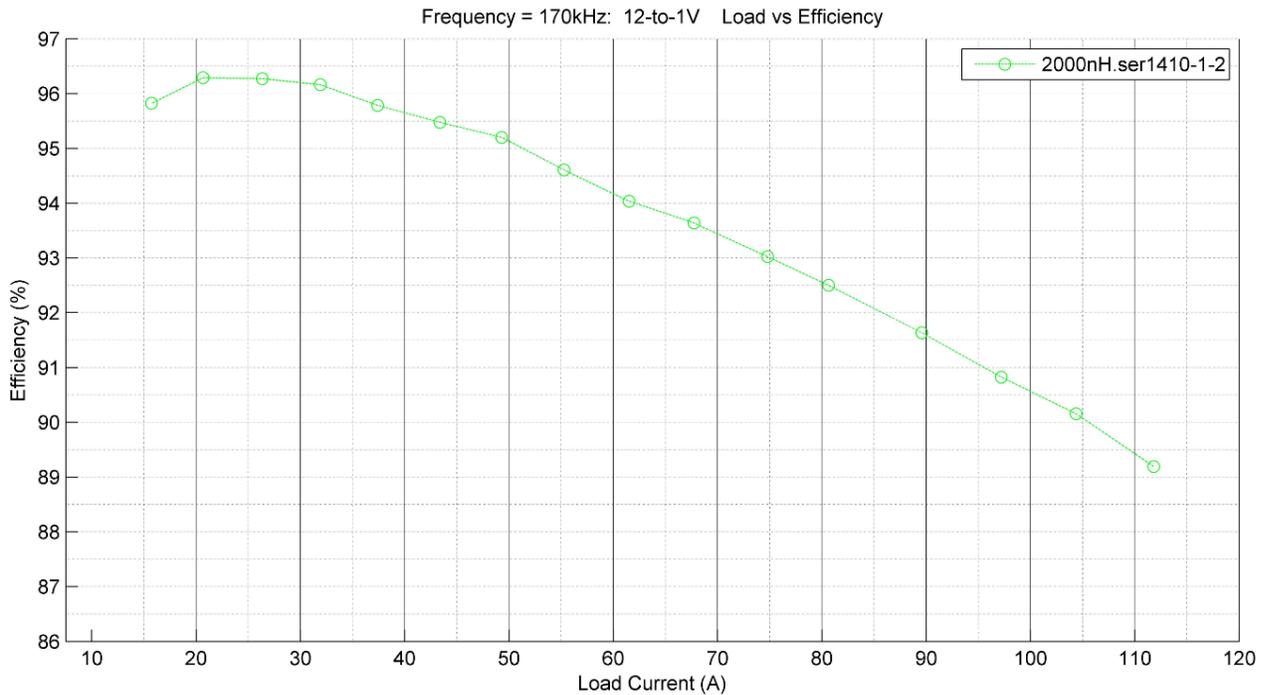


Fig. 8.18: Experimental efficiency of five-phase POL converter ($V_{IN} = 12\text{ V}$, $V_{OUT} = 1\text{ V}$, $f_s = 170\text{ kHz}$, and $f_{eff} = 850\text{ kHz}$).

CHAPTER 9

RELIABILITY

Si is a mature technology that has been applied to power systems for decades. Naturally, much effort has been spent to verify and improve reliability of Si components. The Si devices used in automotive applications means those devices have failure rates below ten PPM, meaning less than ten parts per million fail. One of the biggest reservations that industry users have with WBG materials, such as GaN and SiC, is that long-term reliability is still a mystery. Needless to say, most companies are not willing to risk their reputation for moderate performance gains. Therefore, rather than identifying the best performing (hero) prototype and claiming astounding performance that cannot be consistently repeated, this work averages performance results to develop realistic expectation for these systems. Additionally, reliability studies have been completed to ensure prolonged use is attainable with modern WBG semiconductors.

9.1 Dynamic $R_{DS(ON)}$

Before GaN HEMTs can be analyzed, a phenomena called dynamic $R_{DS(ON)}$, which is inherent to lateral eGaN devices, must be explained. According to EPC's published text on eGaN FETs, dynamic $R_{DS(ON)}$ is an event where the on-resistance of a GaN HEMT is increased after being subjected to a drain bias [20]. In fact, the magnitude of the increase in $R_{DS(ON)}$ is dependent upon the drain-side gate edge electric field, under which electrons accelerate and some remained trapped in the epitaxial layer, which is commonly referred to as the EPI surface. The greater the applied drain voltage, the greater the increase in $R_{DS(ON)}$ after biasing [20]. Eventually, $R_{DS(ON)}$ should return to the initial resistance value, and high temperatures decrease the relaxation time by

removing trapped electrons quicker. Relaxation (a return to original $R_{DS(ON)}$) occurs because the once trapped electrons become free from the EPI layer. Hence, dynamic $R_{DS(ON)}$ is not evidence of the part degrading; rather, it is an interesting phenomenon explained by the physics of the GaN HEMT. EPC reports that during the reliability testing of the first generation eGaN devices, they observed an average of 10% increase in $R_{DS(ON)}$ throughout many devices. The EPI layer is the thin AlGaN layer above the GaN layer, where the two dimensional electron gas (2DEG) is formed. It is necessary to understand dynamic $R_{DS(ON)}$ to recognize that an increase in on-resistance is not necessarily a permanent degradation of the transistor but may be a temporary condition.

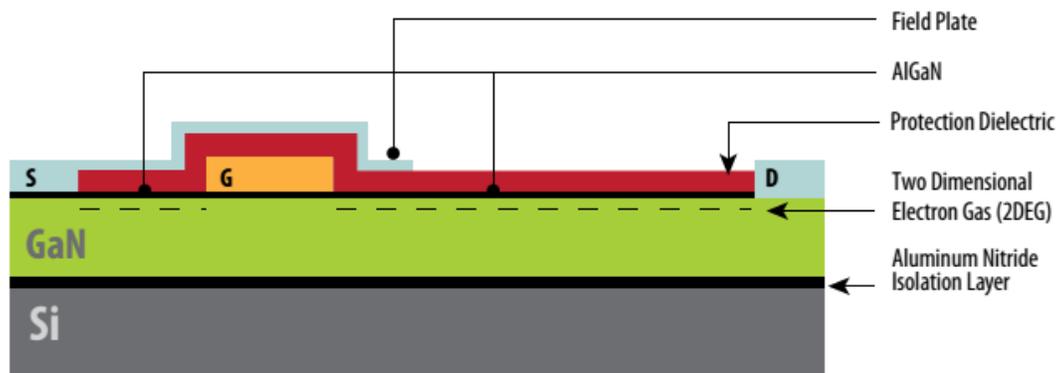


Fig. 9.1: EPC GaN FET cross-section [20].

9.2 1,000 Hour Testing

A 1,000 hour, 125 °C reliability test was performed on the three types of EPC eGaN HEMTs considered for this work. The HEMTs were constantly monitored using a digital multimeter and switch matrix, and no device failures were observed during testing. The tests completed are summarized in Table 9.1. Four different tests were completed on each of three different eGaN HEMTs. The rated drain-to-source voltage of the EPC2001, EPC2014 and EPC2015 is 100 V, 40 V and 40 V, respectively. The 40 V devices were tested for use in the POL, and the 100 V device was tested for use in an early prototype of the IBC.

Each eGaN HEMT was mounted on a break-out board (seen in Fig. 9.2) to allow I-V characterization before and after reliability testing. All HEMTs were mounted on carrier boards and placed on ESD mats in the oven (see Fig. 9.3), and the carrier boards contained a series resistor to detect inrush current by means of a voltage spike across the resistor in the event of a failure.

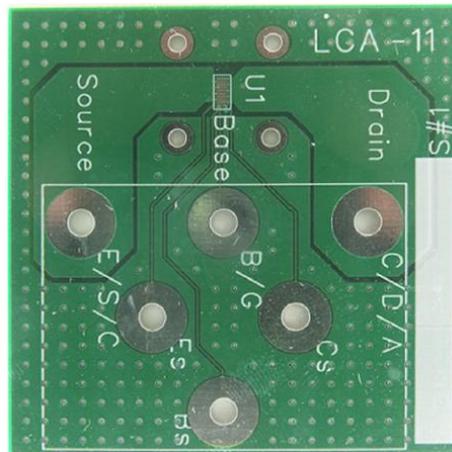


Fig. 9.2: GaN HEMT break-out board.

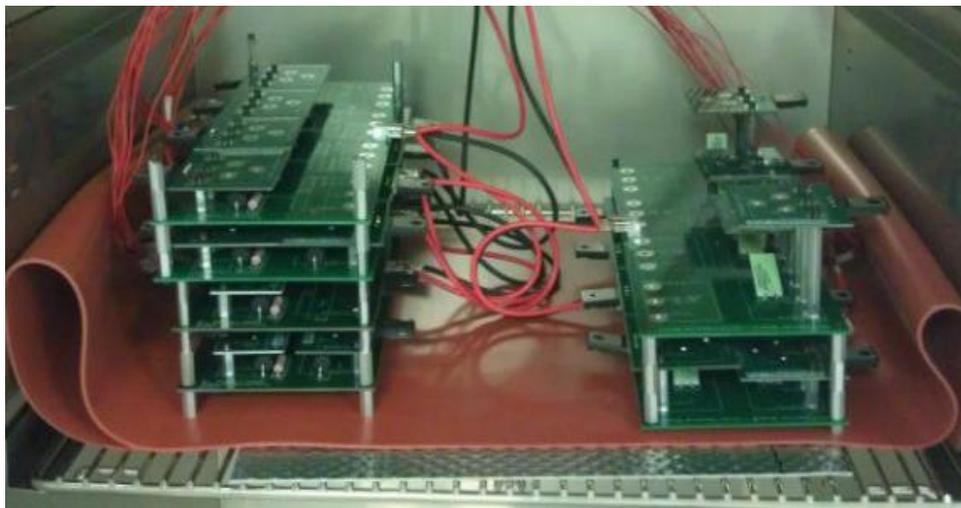


Fig. 9.3: Populated carrier and breakout boards inside oven.



Fig. 9.4: 1,000 hour test set-up with oven (left), switch matrix and multimeter (right), and computer to monitor the test (center).

Table 9.1: Summary of 1,000 hour reliability tests

Part	Test 1	Test 2	Test 3	Test 4
EPC 2001	$V_{DS} = 130V$ $V_{GS} = \text{Short}$	$V_{DS} = 100V$ $V_{GS} = \text{Short}$	$V_{DS} = 60V$ $V_{GS} = \text{Short}$	$V_{DS} = \text{Short}$ $V_{GS} = 5V$
EPC 2014	$V_{DS} = 40V$ $V_{GS} = \text{Short}$	$V_{DS} = 48V$ $V_{GS} = \text{Short}$	$V_{DS} = 52V$ $V_{GS} = \text{Short}$	$V_{DS} = \text{Short}$ $V_{GS} = 5V$
EPC 2015	$V_{DS} = 40V$ $V_{GS} = \text{Short}$	$V_{DS} = 48V$ $V_{GS} = \text{Short}$	$V_{DS} = 52V$ $V_{GS} = \text{Short}$	$V_{DS} = \text{Short}$ $V_{GS} = 5V$

All devices appeared functional until re-characterization, when some of the EPC2014s failed in the I-V curve tracer (Tektronix 371A). It is believed that most of the devices failed due to the applied $V_{GS} = 6V$ during re-characterization. When a device failed during re-

characterization, it almost always took place when 6 V was applied to the gate and the device was conducting current. Also, the maximum current rating is based on the devices ability to dissipate heat. Hence, reaching its maximum current rating after increased on-resistance due to an applied drain bias may have played a role in damaging the EPC2014s. The EPC2001s and the EPC2015s all passed during re-characterization, so this testing only raised concerns about the EPC2014, which are no longer being used in design.

Simply being able to re-characterize a device means that the transistor does not demonstrate a drain-to-source or gate-to-source short. Not until later analysis of post reliability on-resistance were some EPC2001s and EPC2015s considered failures because their on-resistance increased enough to cause significantly higher conduction loss. It was the EPC2014s that proved not to be as rugged as needed for this project. For this reason, the EPC2014s were no longer considered a viable option for the WBG POL design; using the EPC2014s was never a serious consideration for the synchronous rectifier because of its higher on-resistance; however, it was considered for the control switch. Due to its lack of size, the EPC2014 simply cannot dissipate enough heat to withstand extreme conditions and high load currents. The saving on size of the EPC2014 over the EPC2015 and the slight decrease in gate charge do not outweigh the disadvantages of higher on-resistance and less dependability. Hence, the EPC2015 became the GaN transistor of choice for the continued work on the 12-to-1 V POL converter.

Table 9.2 breaks down the observed pass/fail rates for each device and from each of the four tests completed on each transistor. A “pass” simply means that the device is still operational and thus can be re-characterized without an undesired short or open-circuit. Notice that 100% of the EPC2015s, the GaN HEMTs used in the final POL, passed reliability testing. After completion of testing, pre and post-test on-resistance of all devices are compared in Fig. 9.5 – 9.7.

Table 9.2: Pass/fail results of 1,000 hour reliability testing

Part/Test	Total Devices Tested	# Passing Devices	# Devices Failed Shorted	Pass Ratio
EPC2001/Test 1	10	10	0	100%
EPC2001/Test 2	10	10	0	100%
EPC2001/Test 3	10	10	0	100%
EPC2001/Test 4	10	10	0	100%
EPC2014/Test 1	10	9	1	90%
EPC2014/Test 2	10	9	1	90%
EPC2014/Test 3	10	7	3	70%
EPC2014/Test 4	10	9	1	90%
EPC2015/Test 1	10	10	0	100%
EPC2015/Test 2	10	10	0	100%
EPC2015/Test 3	10	10	0	100%
EPC2015/Test 4	10	10	0	100%

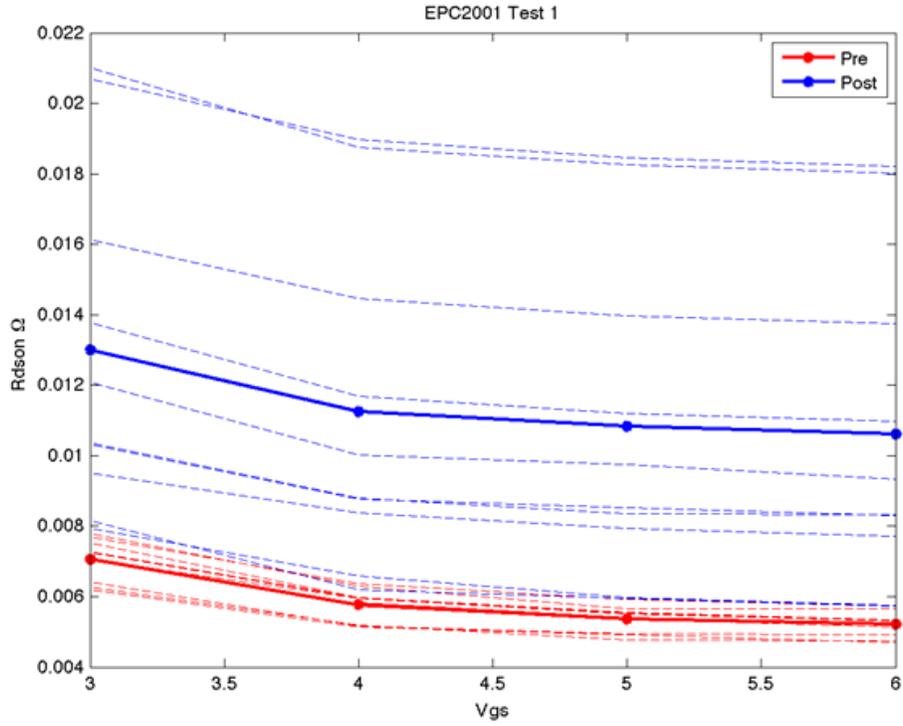


Fig. 9.5: EPC2001 $R_{DS(on)}$ comparison over 1,000 hour testing.

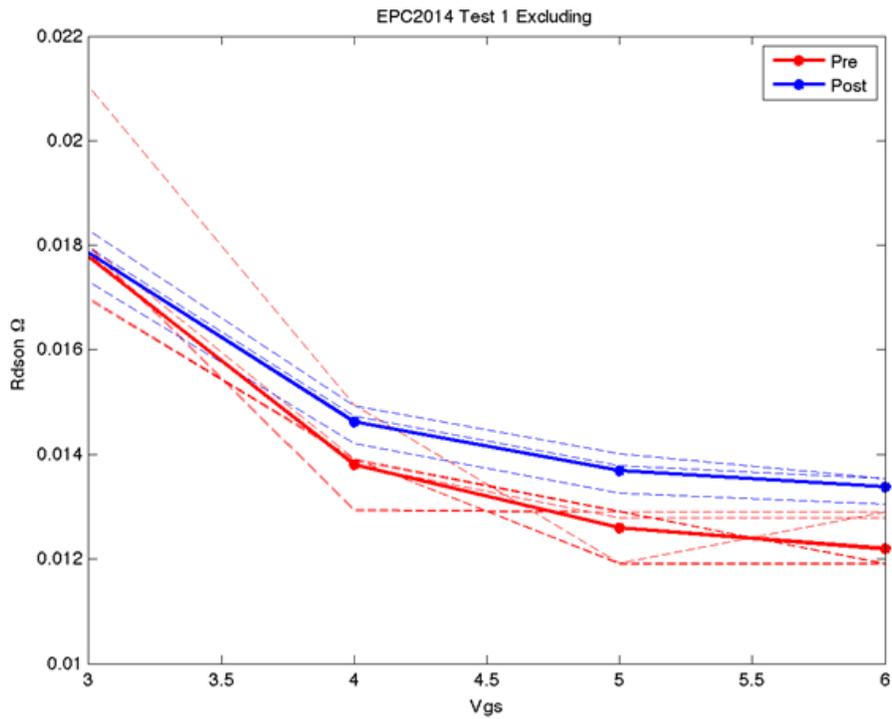


Fig. 9.6: EPC2014 $R_{DS(on)}$ comparison over 1,000 hour testing.

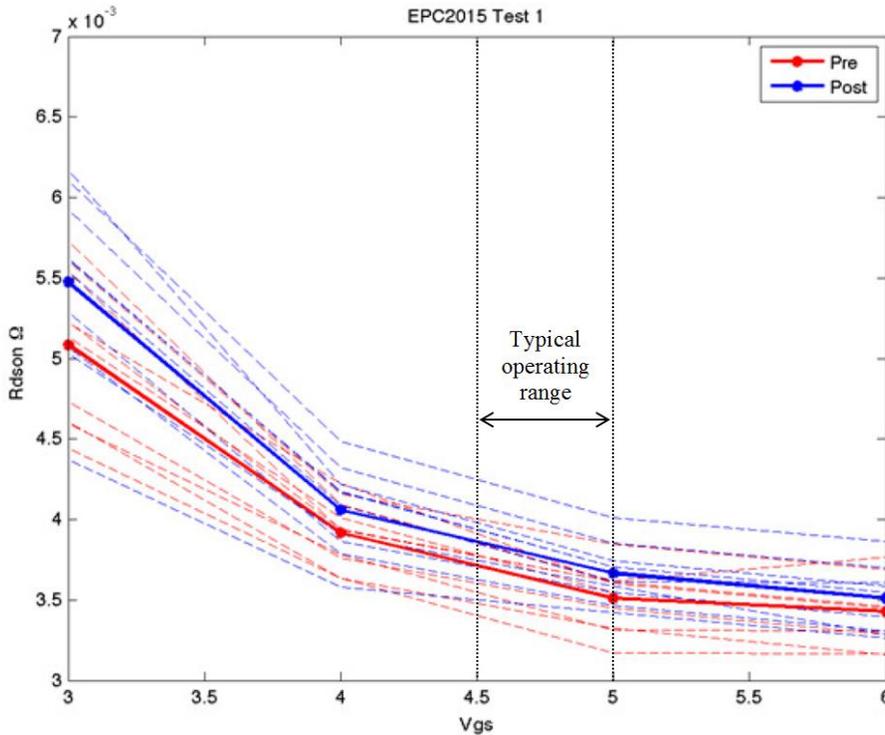


Fig. 9.7: EPC2015 $R_{DS(ON)}$ comparison over 1,000 hour testing.

9.3 20 Month In-Circuit GaN Reliability Testing

This work analyzes the $R_{DS(ON)}$ of enhancement-mode GaN FETs to draw conclusions about eGaN FET reliability while operating in a low-voltage POL converter. The purpose of this study is to observe component degradation as a result of normal power conversion operation over a 20 month (~14,500 hours) period. Throughout the twenty month study, the eGaN FETs have been routinely re-characterized to detect any increase in on-resistance or failures due to normal operating conditions. Results indicate that on-resistance increased initially due to a phenomenon known as dynamic $R_{DS(ON)}$, which is a phenomena inherent to GaN FETs and is a result of trapped electrons in the epitaxial later. Other than observation of dynamic $R_{DS(ON)}$, no significant device degradation or failure has been observed. Reliability studies of GaN devices are necessary to promote industry adoption of wide bandgap semiconductors. Reliability results presented in this

work indicate zero device failures and only minor performance changes over twenty months of practical 8-to-1 V point-of-load converter operation, and these results may encourage industry adoption of wide bandgap semiconductors such as these eGaN FETs.

The second generation 40 V, 33 A lateral eGaN FET from EPC (EPC2015) is studied in this work. An EPC2015 is used as the switch and SR in an 8-to-1 V non-isolated POL converter (Q1 and Q2 in Fig. 9.9). The EPC2015s are mounted on small breakout PCBs that enable intermittent characterization throughout the test period (see Fig. 9.10). The eGaN FETs are then connected to a motherboard that contains the controller, passives, gate drivers, and adjustable load suitable for the desired in-circuit test (see Fig. 9.11). Each converter operates at these approximate specifications: $V_{IN} = 8\text{ V}$, $V_{OUT} = 1\text{ V}$, $I_{OUT} = 10\text{ A}$, $V_{GS} = 4.5\text{ V}$, and a duty cycle $D = 0.14$.

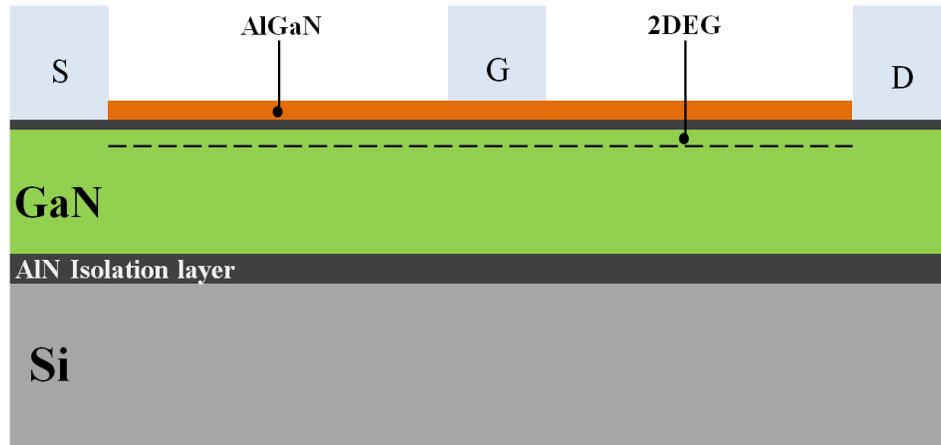


Fig. 9.8: Typical GaN on Si Heterostructure Field Effect Transistor (HFET) structure.

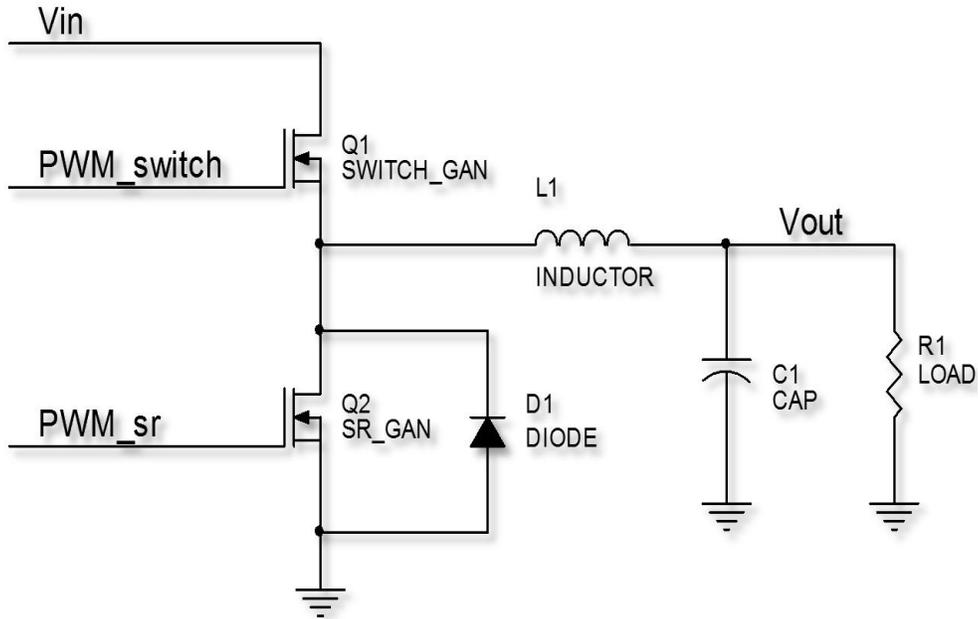


Fig. 9.9: Synchronous buck converter topology.

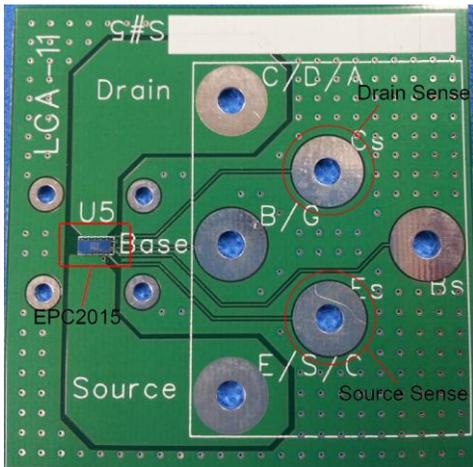


Fig. 9.10: Breakout PCB for GaN FET characterization.

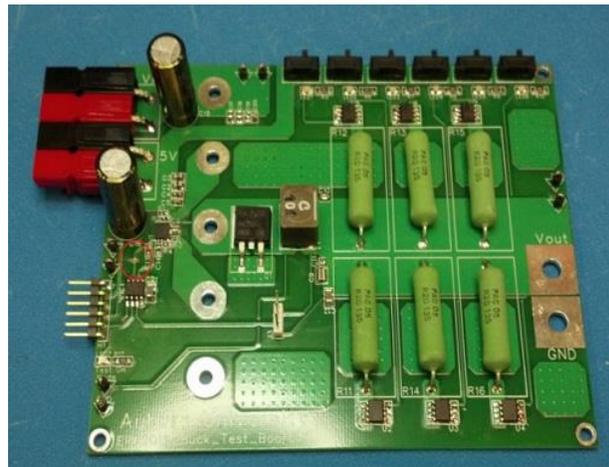


Fig. 9.11: Motherboard containing controller, passives, gate drivers, and adjustable load.

9.3.1 Test Set-Up

The GaN FETs were placed in-circuit and in a test chamber. Early in the testing period, they were removed and re-characterized every week to examine changes in $R_{DS(ON)}$. After the first month, the time between re-characterizations was prolonged to every two weeks. As the test

proceeded, the GaN FETs were re-characterized less frequently, and the change in drain-to-source on-resistance $\Delta R_{DS(ON)}$ appeared to stabilize. Each characterization only required the eGaN FETs to be removed from the circuit for less than one hour, and they were immediately replaced afterwards. Characterization took place on a Tektronix 371a curve tracer accompanied by software to automate the re-characterization process to remove the element of human error.

9.3.2 Results

The EPC2015s begin to turn on with an applied $V_{GS} \geq 3$ V. Therefore, $R_{DS(ON)}$ is studied for gate voltages between 3 and 5 V. Operating eGaN FETs with $V_{GS} > 5$ V is dangerous because gate-to-source voltage spikes above 6 V are likely to cause device damage. Fig. 9.12 illustrates the relationship between the average on-resistance of the test group at gate voltages of 3, 4, and 5 V before and after the completing twenty months of operation. Although significant changes are evident at $V_{GS} = 3$ V, only a 10.8% change in $R_{DS(ON)}$ occurs at $V_{GS} = 5$ V. This is similar to the anticipated 10% increase in on-resistance from dynamic $R_{DS(ON)}$ and is thus a satisfactory result. To elaborate on these results, Fig. 9.13 – Fig. 9.15 shows how $R_{DS(ON)}$ changes with operating time for each individual GaN FET, as well as the average of all the GaN FETs evaluated.

With $V_{GS} = 5$ V and maximum drain current, the manufacturer claims the nominal on-resistance is 3.2 m Ω and the maximum on-resistance is 4 m Ω . This reliability study concludes that the average on-resistance is slightly higher at around 4.1 m Ω , and the increase in on-resistance begins to stabilize and become more constant within the testing period.

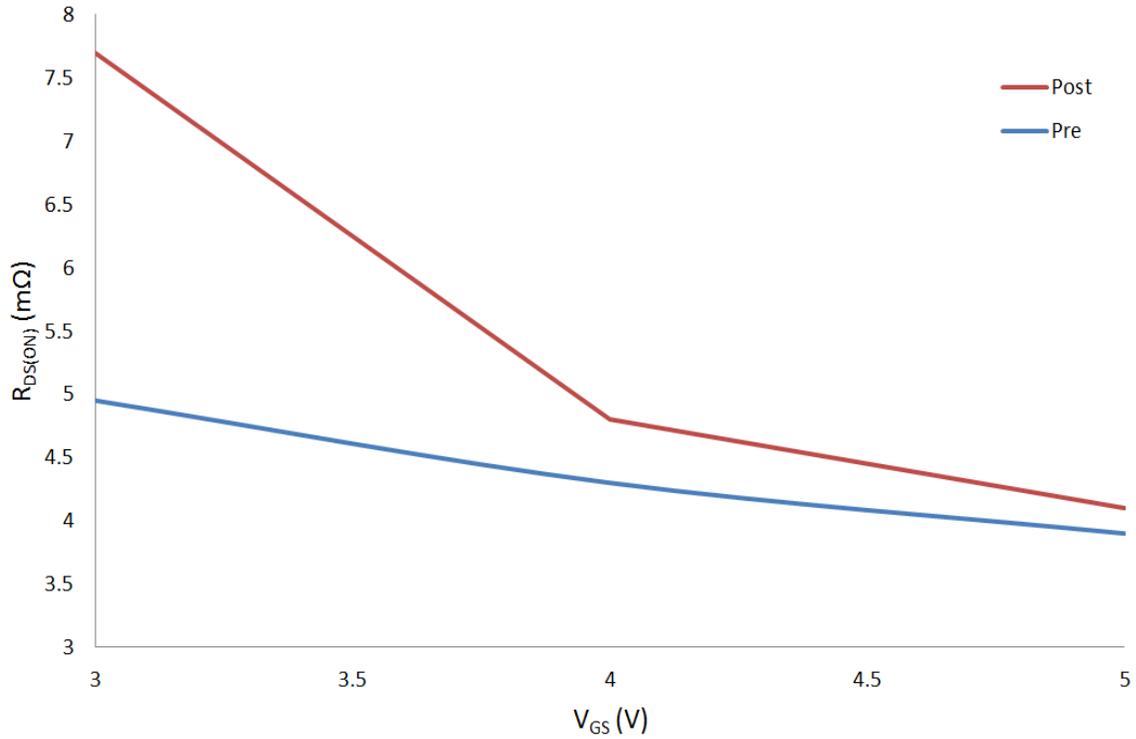


Fig. 9.12: $R_{DS(ON)}$ vs. V_{GS} before and after 12,000 hour testing.

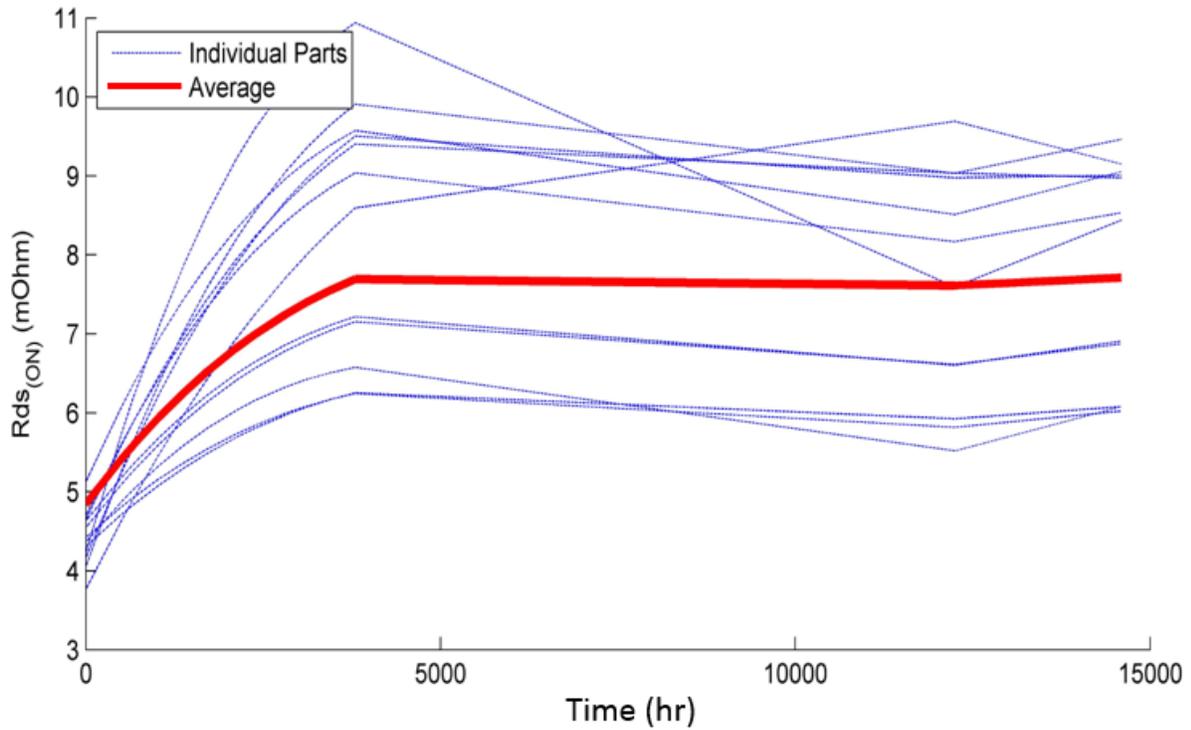


Fig. 9.13: Change in $R_{DS(ON)}$ with operating time, $V_{GS} = 3$ V.

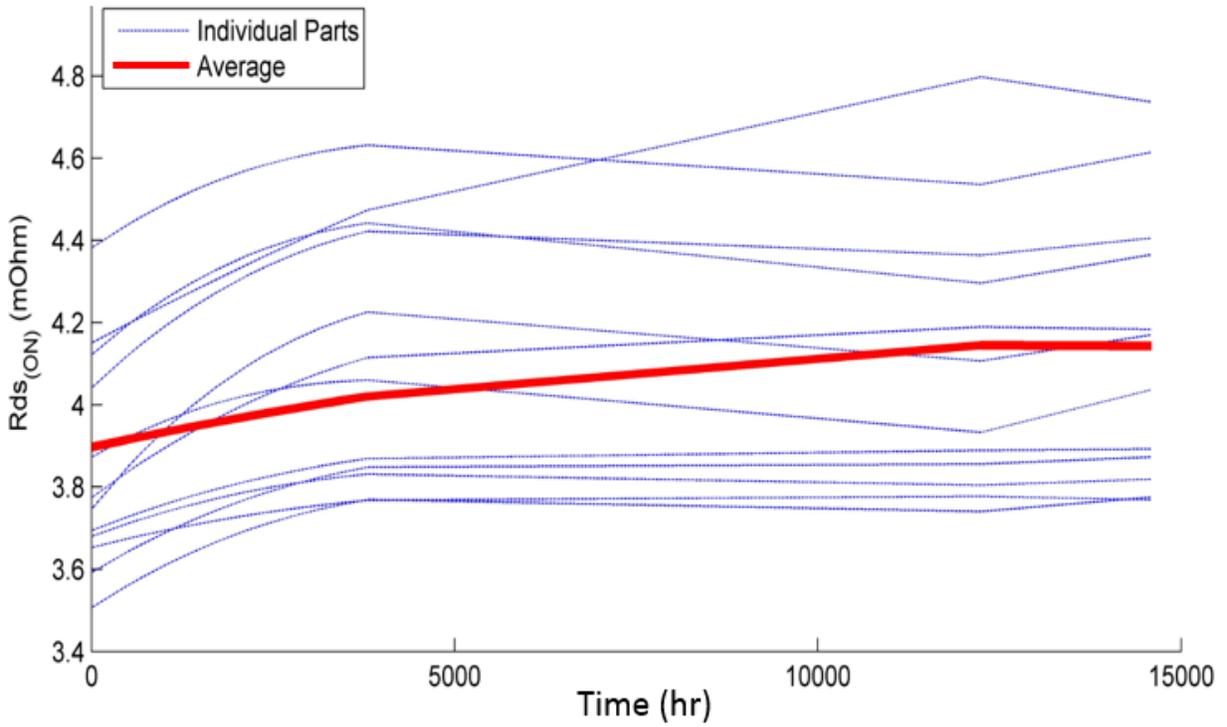


Fig. 9.14: Change in $R_{DS(ON)}$ with operating time, $V_{GS} = 5\text{ V}$.

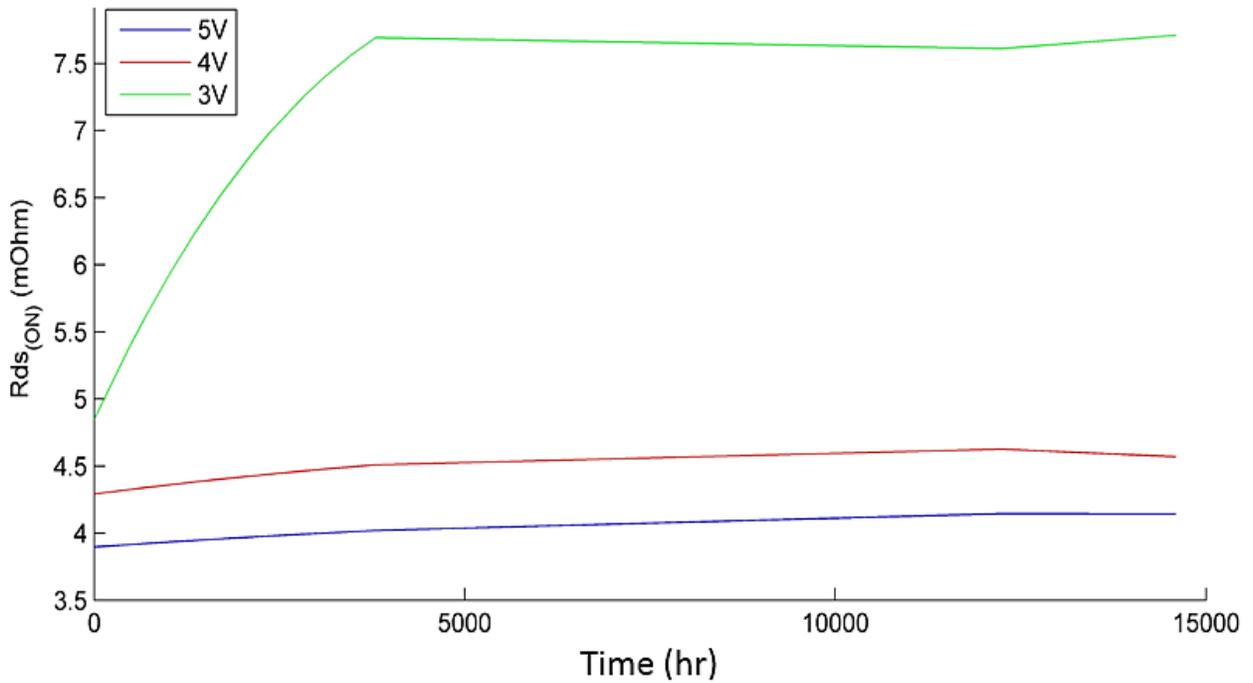


Fig. 9.15: Average change in $R_{DS(ON)}$ with operating time for $V_{GS} = 3\text{ V}$, 4 V , and 5 V .

Power supply designers may be interested to understand the statistical changes in the eGaN FETs in order to incorporate device tolerances and parameter changes in the design specification, to understand the change in performance with time, or to adjust cooling needs. For this reason, Table 9.3 shows the minimum, maximum, average, and standard deviation in on-resistance at the beginning and end of the twenty month test period. The normalized distribution of on-resistance is presented in Fig. 9. A histogram and normalized distribution of change in on-resistance ($\Delta R_{DS(ON)}$) provides an expectation of how each individual device may change with operating time (see Fig. 10). Lastly, and perhaps most importantly, zero device failures occurred during the twenty months of operation in this 8-to-1 V POL converter, perhaps a testament to the durability of the eGaN semiconductors.

Table 9.3: $R_{DS(ON)}$ before and after twenty month test period.

	$R_{DS(ON)}$ - Pre (m Ω)	$R_{DS(ON)}$ - Post (m Ω)	Increase (%)
Minimum	3.3	3.8	15.2
Maximum	4.1	4.8	17
Average (μ)	3.7	4.1	10.8
Standard Deviation (δ)	0.247	0.322	30.4

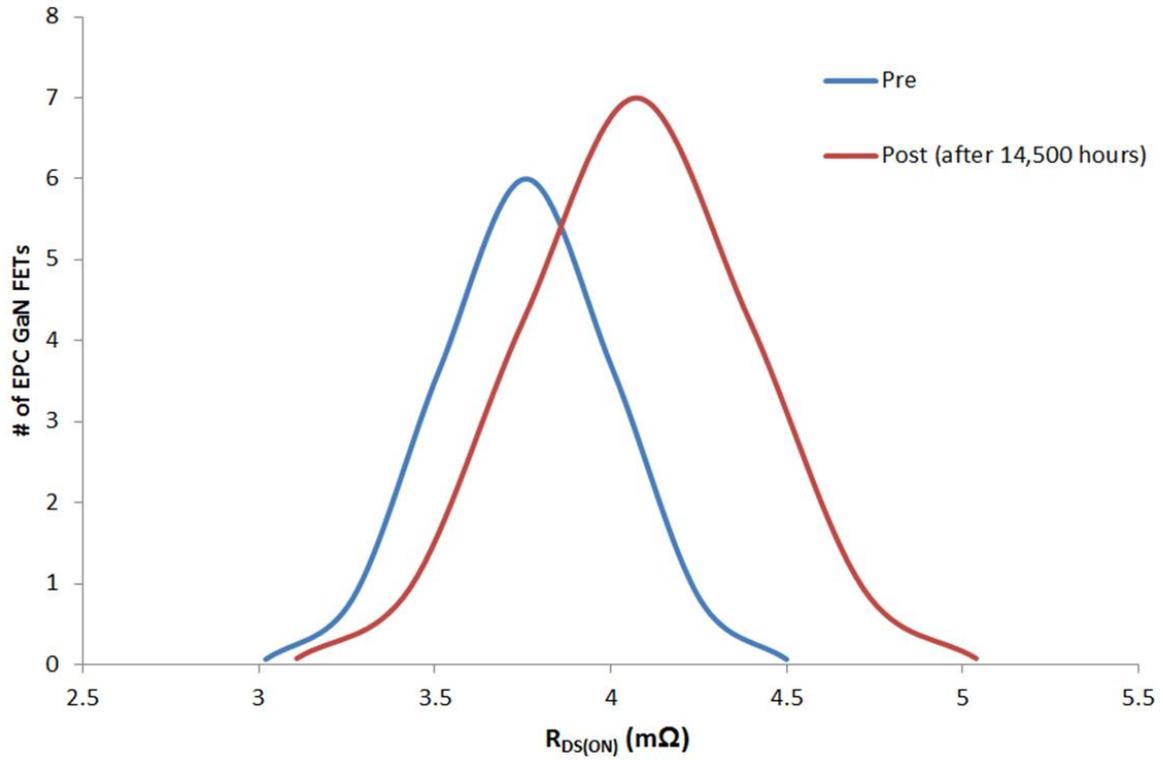


Fig. 9.16: Normalized distribution of $R_{DS(ON)}$ pre and post test, $V_{GS} = 5$ V.

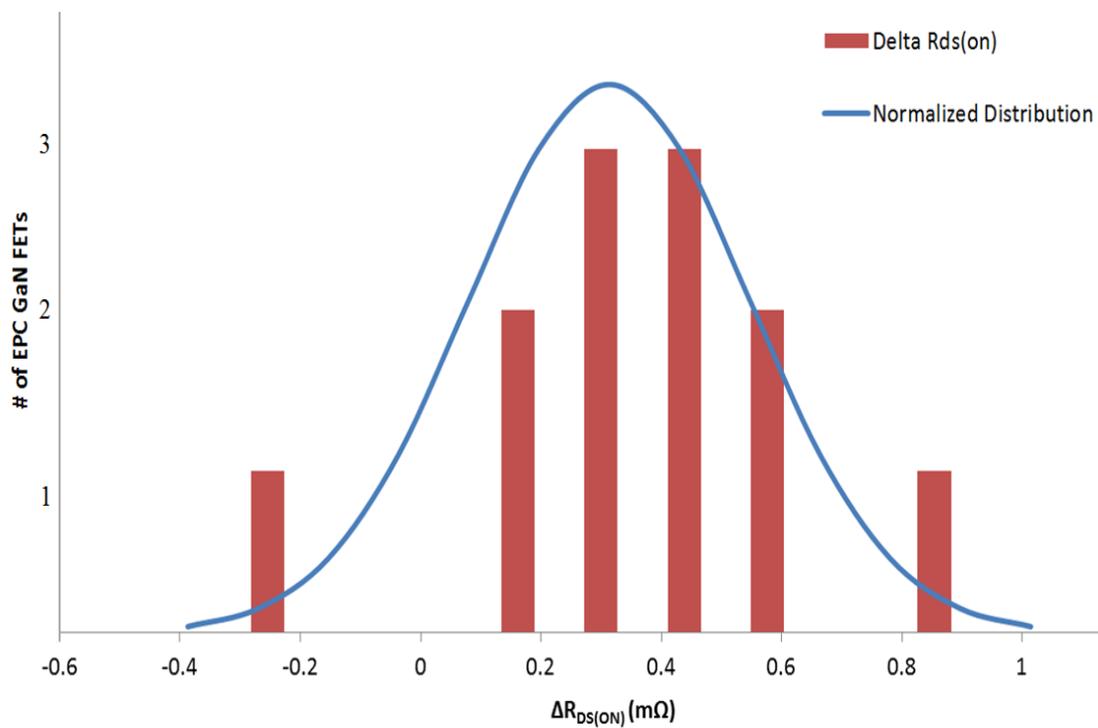


Fig. 9.17: Normalized distribution of $\Delta R_{DS(ON)}$, $V_{GS} = 5$ V.

9.3.3 Conclusion

With WBG manufacturing quality, component tolerances, and reliability still relatively unknown, lateral eGaN FETs are operated in a switch-mode power supply for a twenty month (over 600 days or 14,500 hours) reliability study to determine a device failure rate and to examine any change in device performance over the test period. An average of 10.8% increase in on-resistance was observed and the increase in on-resistance begins to stabilize within the test period. This increase in on-resistance is most likely a result of dynamic $R_{DS(ON)}$ and should be expected in eGaN devices. Statistical analysis will assist power supply designers and give a realistic expectation of how these eGaN devices age. This reliability investigation is one of the longest in-circuit performance evaluations of modern, low-voltage GaN power semiconductors, and these results may encourage industry adoption of WBG materials in the future.

CHAPTER 10

RELIABLE ASSEMBLY PROCESS FOR GAN FETS

As transistors rapidly move to smaller packages, reliable prototyping becomes increasingly difficult. Ideally, high accuracy placement machines are preferred for device placement but are not practical for low-volume production. Here, a novel manual assembly process is applied to the 400 μm pitch EPC GaN FETs that has resulted in near 100% yield and exceptional reliability. The process requires a soldering iron and a reflow oven. An X-Ray image is preferred to verify alignment, but a successful alternate method is also presented. This assembly process, which can be applied to other flip chip and chip-scale packaging, will save time and resources in the development of new products employing WBG power devices like EPC GaN FETs, and it has delivered significantly greater yield than alternative published methods. Without an assembly process that provides a solid solder joint in low-volume production and reduces dendrite issues, the reliability testing and circuit performance of modern semiconductors would yield inaccurate results.

The small packages of EPC GaN FETs, shown in Fig. 10.1, provide exceptional power density but are difficult to assemble [29][40]. With the increased use of GaN FETs, small volume production and prototyping have become significantly more difficult—making an efficient, low-cost, and high yield manual assembly process a valuable asset [40].

EPC's recommended technique for manual assembly of GaN FETs, as stated in [20] and [67], requires a hot air gun, is prone to misalignment, can be difficult to execute properly, and requires repeated heating of the PCB for designs employing several FETs. Henning et al presents an assembly technique using a reflow oven and X-ray image for alignment in [40]. This technique

improved yield beyond EPC’s recommendations; however, the use of water-soluble tacky flux, even when cleaned, led to early solder corrosion and dendrite growth—resulting in premature failure. Additionally, neither publication presents an appropriate underfill for EPC GaN FETs. An iterative process has been used to find a quick, reliable, high-yield assembly technique for these wide-bandgap power semiconductors and similar chip-scale packages (CSPs), including appropriate underfills.



Fig. 10.1: EPC2015 (bottom) and EPC2014 (top).

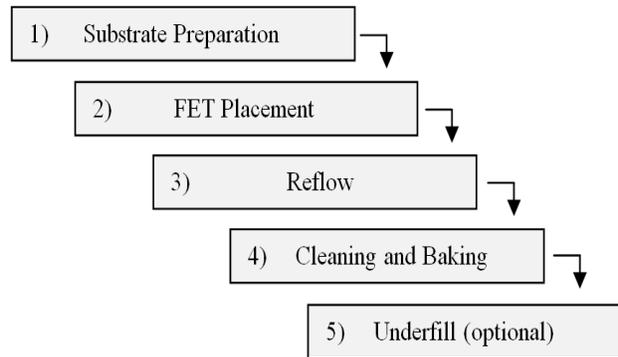


Fig. 10.2: Five step assembly process.

10.1 Assembly process

The assembly process is summarized in Fig. 10.2, and necessary materials are listed in Table 10.1. This process should begin with following electrostatic discharge (ESD) protocol; at a minimum, this should include wearing a grounded ESD wrist strap, ESD gloves, and working on anti-static mats.

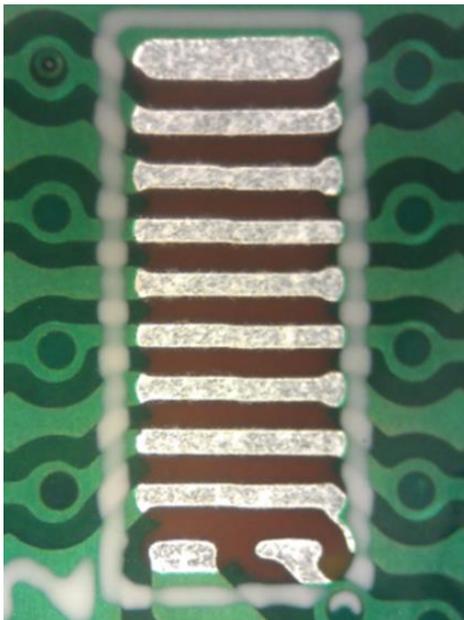
A. Substrate Preparation

- 1) Clean the PCB with a lint-free cloth to remove dirt, dust, and debris.
- 2) Position a hotplate under a microscope with adequate lighting, and set the hotplate to 150 - 160°C.
- 3) Place a fine tip on a soldering iron set to approximately 370°C.

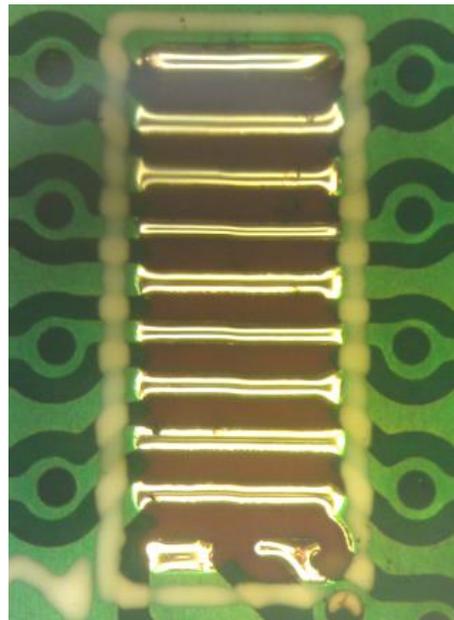
- 4) Position the PCB on the hotplate and under the microscope, and liberally apply no clean tacky flux to the pad(s) of interest. An EPC2015 pad covered in tacky flux is presented in Fig. 10.3(a).
- 5) Put a very small amount of no clean solder on the tip of the solder iron and run the solder iron over the pad(s) of interest. This is referred to as “bumping the pads”. After bumping the pads of an EPC2015, they should look smooth, rounded, and slightly raised—similar to Fig. 10.3(b). Step 4) and 5) should take less than fifteen seconds when executed properly. Note: one smooth stroke over each pad should leave adequate solder on the pad. If necessary, clean the solder tip and, with no additional solder, run it back over the pads to smooth out the solder. Based on the surface tension of the solder, with adequate tacky flux, the right temperature, and solder that has not been on the tip long enough to significantly oxidize, each pad should take as much solder as it needs and no more.
- 6) Remove the PCB from the hotplate, allow it to cool to room temperature and clean any remaining tacky flux in ethanol using a soft bristle brush. Then, allow the PCB to dry. Troubleshooting: if the solder clumps or balls up on or between pads, the solder has oxidized, not enough tacky flux was used, or the board is not warm enough. If this occurs, apply more tacky flux, remove the oxidized solder, clean the soldering tip, and begin with new solder that has not oxidized.

Table 10.1: Equipment and materials list for manual LGA assembly.

Equipment/material	Application group
ESD wrist strap, ESD gloves, anti-static mats	ALL
Hotplate	Substrate Preparation
Microscope (recommended)	Substrate Preparation
Soldering iron	Substrate Preparation
No clean rosin core solder	Substrate Preparation
No clean tacky flux	Substrate Preparation, FET Placement
Ethanol and soft bristle brush (e.g. toothbrush)	Substrate Preparation, Cleaning and Baking
Anti-static tweezers	FET Placement
X-ray machine (recommended)	FET Placement
Reflow oven	Reflow
Oven (capable of 150°C)	Cleaning and Baking, Underfill
Underfill (Ablestik Ablefill UF8830 recommended)	Underfill



(a) Without solder bumps



(b) with solder bumps

Fig. 10.3: EPC2015 PCB pads before and after bumping with solder.

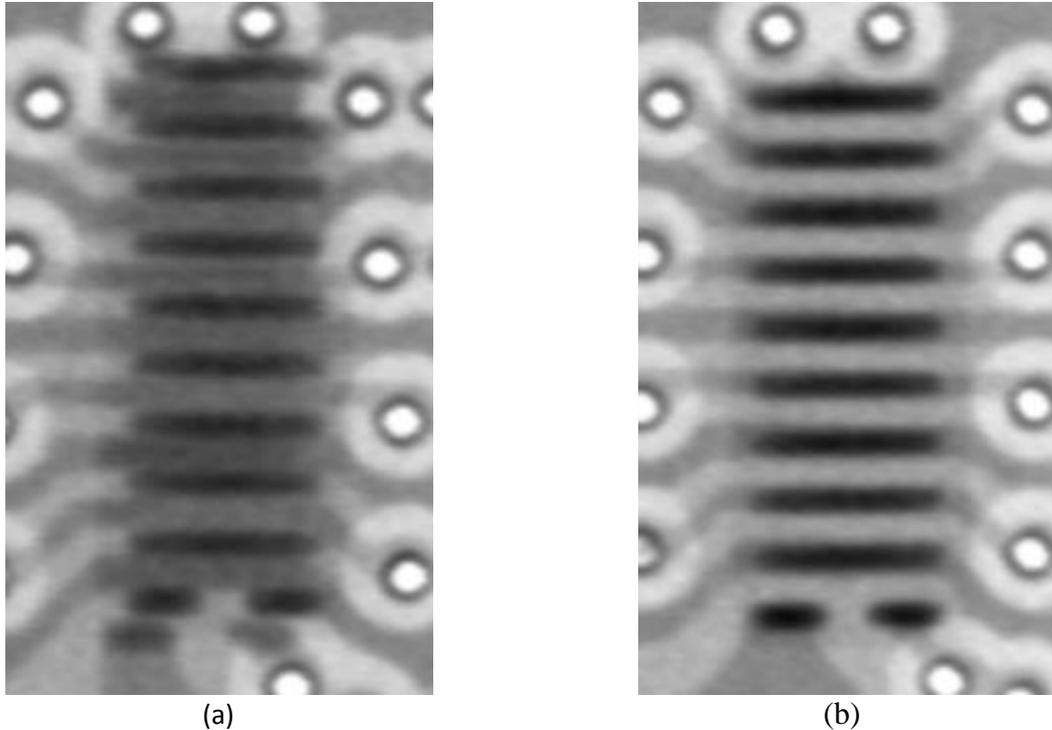


Fig. 10.4: X-ray images of (a) improperly and (b) properly aligned EPC2015.

B. FET Placement

- 1) With the EPC pads bumped and cleaned, pick up the EPC with tweezers and determine the proper orientation.
- 2) Dip the EPC in no clean tacky flux.
- 3) Roughly place the EPC on its pads. Use the silkscreen to place the part as accurately as possible.
- 4) Place the PCB in an X-ray machine and move the EPC until its lands overlap the pads on the PCB. Fig. 10.4 shows X-ray images of improperly and properly aligned EPC2015s, respectively. The EPC in Fig. 10.4(a) is shifted high and to the right of its pads. If an X-ray machine is available to verify alignment, proceed to step C-1.

4b) If an X-ray machine is not available, an alternate method is presented. If the silkscreen is designed properly, it can significantly aid proper alignment. Fig. 10.5 shows a recommended silkscreen design.

5b) When sliding the EPC along its longer direction, it is obvious when the EPC sits lower—when the lands of the part sit between the raised solder bumps of the circuit board; see Fig. 10.6(a).

Move the EPC along its longer direction until the EPC sits higher because the lands of the part are on the bumped pads of the PCB, see Fig. 9.15(b), and the part appears centered within the silkscreen. The LGA package has fair self-aligning properties, so the placement should be close, but it does not have to be perfect.

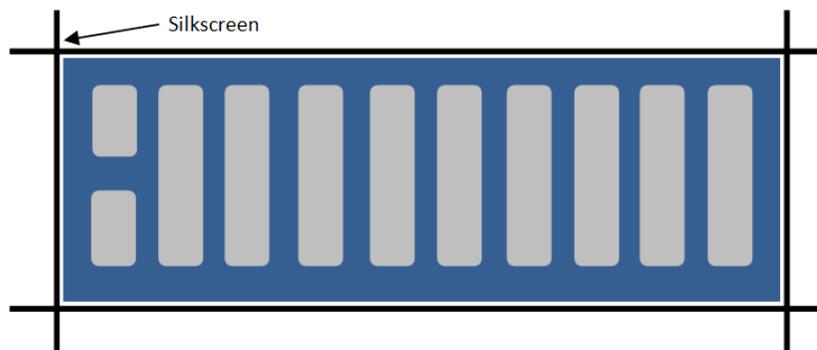


Fig. 10.5: Recommended silkscreen to align EPC without an X-ray machine.

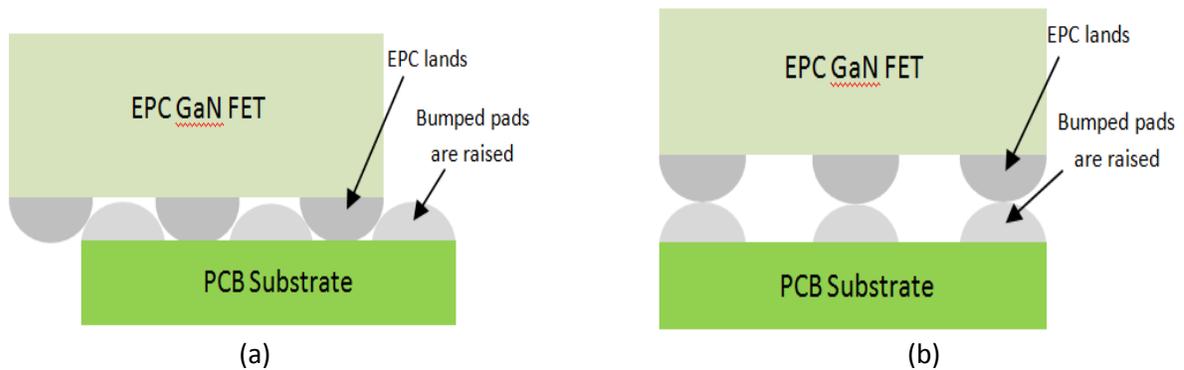


Fig. 10.6: Side view of (a) improperly and (b) properly aligned EPC2015s.

C. Reflow

- 1) Set the reflow oven temperature profile according to the recommendations for the solder being used.
- 2) Once the EPCs are properly aligned, place the circuit board in the reflow oven.
- 3) When reflow is finished, remove the PCB from the reflow oven and allow it to cool.
- 4) If an X-ray machine is available, check to ensure solder did not bridge between pads and the part did not shift.

D. Cleaning and Baking

It is imperative that the remaining flux is thoroughly cleaned and the boards are baked to cure any remaining flux between the lands of the EPC. Follow these steps to prevent premature failure due to dendrite growth:

- 1) Submerge the PCB in ethanol, and gently scrub with a small, soft bristle brush (e.g. a toothbrush). Using a sonic cleaner is preferred to remove flux from between the lands of the part. Be sure to remove as much flux as possible while cleaning and allow the PCB to dry.
- 2) To ensure remaining flux is cured, bake the PCB in an oven at 150°C for 30 minutes or at 125°C for 60 minutes.

Now that the flux has been cleaned and baked, it is now safe to apply a voltage to the EPC with minimal risk of dendrite growth. For many users, the part is now ready for testing and application. If, however, underfill is desired, complete the following steps in *E. Underfill*.

E. Underfill

Underfill can make drastic improvements in the reliability of flip chips, like the EPC GaN FETs. Underfill is highly recommended for parts that will see continued use. The underfill adds

mechanical strength between the device and the substrate and seals out contaminants [68]. Additionally, underfill may provide some additional protection from dendrite growth. The following instructions guide the reader through the steps to underfilling the EPC GaN FETs with the underfill specified in Table 10.1, Ablestik Ablefill UF8830. UF8830 has a viscosity of $12,000 \text{ mPa} \cdot \text{s}$ at 25°C and a cure time of 2 hours at 150°C .

- 1) The underfill is best applied to a warm substrate, so this step works well directly following step *D-2*. Remove a PCB that has reached 150°C substrate temperature from the oven and immediately (before the substrate cools) apply a small fillet of room temperature underfill to one of the longer sides of the EPC. A hotplate may be useful while applying underfill to keep the substrate warm.
- 2) Place the underfilled EPC back in the oven for the time and at the temperature recommended by the underfill manufacturer.
- 3) Remove PCB and allow it to cool. The device is ready for testing.

Capillary effects should pull the underfill under and around all sides of the EPC within a few seconds, as long as enough underfill was supplied to the fillet. Ideally a viscosity of $8,000 - 12,000 \text{ mPa} \cdot \text{s}$ will ensure that the underfill flows between the lands of the EPC. A successfully underfilled EPC2015 is presented in Fig. 10.7, and the red line denotes where the fillet of underfill was applied.

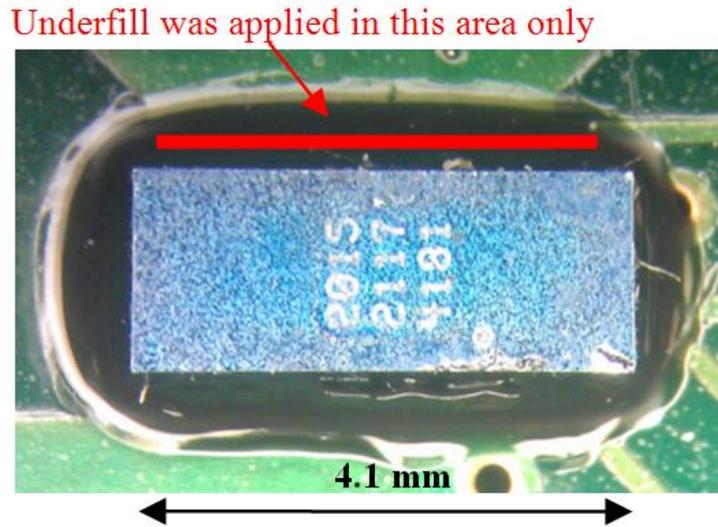


Fig. 10.7: Completely assembled and underfilled EPC2015.

10.2 Results & Layout Considerations

Over a two year period, well over a thousand EPCs have been manually assembled with various techniques; insufficient yield and early failures plagued the use of these WBG power semiconductors. With the assembly process presented here, near 100% yield and great success in power supply and reliability testing has been observed. The process is quick, easy, will save time in low-volume production, and near 100% yield is attainable by following the details of this process.

Be sure to use EPC's recommended layout and keep soldermask clearances small enough that it does not expose excess copper areas near the FET. If the FET is placed within a copper area, use a copper area cutout around the FET to ensure pads on the same net as the copper area do not become larger than desired due to user specified or manufacturer minimum soldermask clearance. If FET pads are larger than EPC's recommended footprint, bridging is more likely, and some solder may need to be removed from the substrate pads during the process of bumping the pads (section A-5).

10.3 Summary

This manual assembly process begins with following specific ESD precautions and cleaning the substrate. The substrate pads must be bumped with solder. The silkscreen can aid approximate part placement. With the pads of the PCB raised with additional solder, placing the part without an X-ray image becomes easier. When the part is properly placed on the pads, it is also slightly raised because the EPC lands sit atop the raised substrate pads, and when the part shifts down to a lower point, it is misaligned (see Fig. 10.6). The difference between proper and improper placement can now be felt when moving the device. However, an X-ray image allows for better placement verification and is recommended. Once the part has been aligned, it is ready for the reflow oven, inspection, cleaning in ethanol, baking to cure any remaining flux, and underfill to improve reliability and further prevent dendrite growth—a problem that can be tricky to avoid with EPCs. A completely assembled and underfilled EPC2015 is shown in Fig. 10.7. This manual assembly process is quick, easy, and ideal for low-volume production and prototyping.

CHAPTER 11

CONCLUSIONS

In Chapter 1, it was stated that this research should make significant improvements to state-of-the-art low-voltage POL converters. In order of priority, the POL converter should demonstrate substantial improvements in efficiency ($> 5\%$ beyond the best commercial products), demonstrate reliable operation, match or beat transient performance of commercial POL converters, and exhibit high power density. This design is tailored to data center and server power supplies but is applicable to many other areas. These POL advancements will yield energy savings, reduce maintenance, improve server availability, reduce volume, and lower line loss since a smaller POL can be located closer to the load. With the development of new materials for power semiconductors, the power electronics market is primed for technological advancements that will lead to more efficient and power dense switch-mode power supplies. This work explores the potential of WBG devices to meet today's power conversion demands.

The design process began by selecting the best power semiconductors for the application and determining how many semiconductors should be in parallel to reduce overall conduction and switching loss. Next, a single-phase POL converter was optimized by developing new layout techniques to minimize layout parasitics for faster device switching, testing a wide variety of commercial inductors, developing planar inductors ideal for high frequency and high power density designs, and properly managing effective dead-time for safe and efficient operation. The best GaN-based POL prototypes were compared to very similar Si prototypes. Eventually, a combination of GaN and Si produced a product that improved high load efficiency.

Once the single-phase GaN and GaN/Si hybrid POL converters were optimized, they were implemented in a five-phase POL converter, which resulted in up to 150 W operation, up to 96% peak efficiency, reduced steady-state output ripple, and very good transient response. The multiphase POL converters discussed in Chapter 7 far outperform the best commercial and research level POL converters on the merits of efficiency and power capacity, while merits such as power density and dynamic response are also very good compared to commercial POLs.

Finally, the 150 W, 12-to-1 V GaN-based POL converter is implemented into a three-stage WBG power supply chain design to improve data center power conversion from 480 V 3 ϕ to as low as 0.9 V DC. System optimization helped determine the best intermediate bus architecture (IBA) and intermediate bus voltage for the system. Each of the three power conversion stages were analyzed to see the improvement from similar Si prototypes, and implementation of this WBG architecture provides DC isolation at the IBC, strict voltage regulation at the load, significantly improved efficiency, and a compact lightweight design. This effort was a culmination of a three year effort, and all conversion stages we brought to a pre-production level. With additional work, these prototypes could be commercially packaged and significantly reduced in size. Overall, this was a very successful effort that exceeded customer deliverables and propelled the ability of what these power conversion systems could do when this work began.

Other additional work included reliability studies of WBG devices. Some of the reliability studies, like the twenty month in-circuit operation, are the longest running reliability test of eGaN FETs. A novel assembly technique was also created to simply and reliably assemble GaN FETs in low-volume for rapid prototyping purposes.

CHAPTER 12

FUTURE WORK

As with most research efforts, there is often remaining work that could be explored. Regarding the GaN-based POL converters, there are several areas that could be explored in the future. These areas are discussed in the following sections.

12.1 Improvements in Semiconductors

Since the field of WBG semiconductors is growing extremely rapidly, new devices are becoming available constantly. For example, EPC has already released several new devices including a 30 V, 1.3 m Ω , 20 nC gate charge device that improves the FOM of the EPC2015 discussed in Chapter 3 and reduces the need for parallel GaN FETs in the SR. Also, this device would likely perform better than the Si MOSFET used in Chapter 4. This work could be very simple and would only entail slight PCB modifications to accommodate the new transistors. 30 V eGaN FETs were not available until very recently; otherwise, they would have been included in this work.

Further advancements should and eventually will be made using the eGaN technology. EPC claims to be working on a half-bridge and gate driver that is packaged together. This would eliminate some of the layout complexity, improve switching performance, and may reduce the footprint slightly. Perhaps a switch and two parallel dies for the SR could be packaged as one device. This would also help eliminate the conduction loss in the SR. These half-bridge devices

will soon be available. EPC states that the only delay is the low yield associated with these complex devices. In the future, this would be an interesting area to revisit.

12.2 Thermal Management Analysis

Currently, the design is limited in its power capability by the amount of heat that it can dissipate. The control switch will fail consistently when the current exceeds 35 A per phase; therefore, the design is de-rated to 30 A per phase, where it will operate consistently for a long period of time. It would be interesting to attach cold plates to the GaN FETs and the driver to dissipate some of that heat and determine if higher current or more efficient operation is possible. Some minor and crude experimentation was done with heat sinks at one point in time, but no noticeable difference was observed.

12.3 Intermediate Bus Voltage

In Section 8.1, the concept of an intermediate bus architecture (IBA) was introduced, which included the intermediate bus converter (IBC) and point of load (POL) converter. Since the intermediate bus voltage is not seen by the front end rectifier (FER) or the load, it is flexible and subject to change. Section 8.1 uses mathematical models to determine the ideal intermediate bus voltage. This could be done experimentally to analyze the IBA at intermediate bus voltages of 5, 8, 12, 18, and 24 V. Some important parameters to observe at these different intermediate bus voltages should include IBA efficiency, output ripple, transient response, component stress, and additional line loss between IBC and POL converter.

12.4 Transient Analysis

This work observed the output transient performance of the POL to ensure that it was comparable to some commercial systems. As a result, the amount of output capacitance was increased to hold up the output voltage. Since the output voltage was acceptable during transients, it was not investigated further. It may be interesting to study the effects of switching frequency on output transients, and the controller could have been further improved to handle load transients better, especially when operating at light load with several phases turned off and then a large load increase occurs. Controller modification could handle this better by turning on all phases for a short time to uphold the output voltage, then returning to an interleaved control state once the load has stabilized. This work becomes difficult quickly because it requires the controller to bounce between two highly nonlinear states very quickly while still remaining stable.

12.5 Other Areas of Interest

There are several other areas of interest that were not explored for the sake of time and/or budget. Several of these may still be explored in the near future using current hardware at relatively no additional cost. These areas include:

- Injecting noise on the input of the POL and measuring additional noise on the output.
- Analyze the POLs ability to regulate an unpredictable, unregulated input and determine minimum and maximum input voltage ratings as a result.

- Combining different phases on the POL Version 3 platform, one to reach peak efficiency at very light loads and others to operate at high load. This could improve efficiency over a very large load range.

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