Characterization of Thermally Induced Stress in IC Packages using Piezoresistive Sensors

by

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Abstract

This thesis presents the characterization of thermally induced stress in IC packages using CMOS sensor circuits. In various applications, the IC packages are exposed to extreme environments. The knowledge of the thermally induced stress in the packages aids the prediction of degradation/failure of the device and calibration of the devices for such environments. Change in resistance is caused by the mismatch in coefficients of thermal resistance for different materials. These circuits are highly sensitive to stress and provide well localized stress measurements than the traditional resistor rosettes and also provide direct current outputs. The sensors are oriented in such a way that the effects of certain stress components are isolated. These sensors are also temperature compensated so that only the effect of stress components is counted. The experiments in this work are conducted in the temperature range of -180°C to 80°C.

Piezoresistive coefficients for p material that can be used for obtaining the normal stress components are extracted by using a four point bending fixture. The die is attached to the beam and a force is applied using the bending fixture at different temperatures. The stress components obtained from the simulations along with output from the PMOS sensor cells are used to extract the piezoresistive coefficients. The range of coefficient values are also confirmed by using a number of samples.

Thermally induced shear stress components in the packages are obtained by using NMOS sensor cells. The packages are cycled through the temperature range and at each temperature, the current from the sensor cells are measured. The current readings along with the piezoresistive coefficients for the n material is used to extract the shear stress component in the package. Finite element analysis using temperature dependent material properties was also done for the comparison of the results.

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α_m	Coefficient of thermal expansion of the material
$\Delta\mu$	Change in mobility of the carriers
$\Delta\mu$	Change in mobility of the carriers
$\Delta\rho$	Change in the resistivity of the conductor material
$\Delta\sigma$	Change in conductivity of the material
ΔI_D	Change in drain current
ΔK	Change in conduction factor
Δl	Change in the length of the conductor
ΔR	Change in the resistance
ΔT	Change in temperature
Δt	Change in the thickness of the conductor
ΔV_T	Change in threshold voltage
Δw	Change in the width of the conductor
μ_n	Electron mobility
μ_p	Hole mobility
$\overline{\tau}$	Average scattering time of the carrier
ϕ	Angle at which the resistor is oriented to [110]

π_{mn} Piezoresistive coefficients

ρ Resistivity of the conductor material

ρ_o Initial resistivity of the conductor material

σ Conductivity of the material

σ'_{mn} Stress components

C'_{ox} Capacitance of the gate per unit area

$CMOS$ Complementary Metal Oxide Semiconductor

CTR Coefficient of Thermal Resistance

I_D Drain current in NMOS transistor in saturation

IC Integrated Circuit

K Conduction factor

L Length of the channel

l Length of the conductor

l_o Initial length of the conductor

m^* Effective mass of the carrier

$MOSFET$ Metal Oxide Semiconductor Field Effect Transistor

n Electron density

$NMOS$ n-channel MOSFET

$NMOS$ p-channel MOSFET

p Hole density

q	Charge of an electron
R	Resistance of the conductor
R_0	Resistor that is oriented at 0° to [110]
R_o	Initial resistance
R_{-45}	Resistor that is oriented at -45° to [110]
R_{45}	Resistor that is oriented at 45° to [110]
R_{90}	Resistor that is oriented at 90° to [110]
t	Thickness of the conductor
t_o	Initial thickness of the conductor
V_G	Gate voltage
V_T	Threshold voltage
VDP	van der Pauw
W	Width of the channel
w	Width of the conductor
w_o	Initial width of the conductor

Chapter 1

INTRODUCTION

Mechanical stress in IC(integrated circuit) packages are responsible for the performance degradation or even failure of the device. The devices that are used in applications with large temperature variations are prone to this type of failure. When exposed to temperatures, resistance of different materials expand at different rates depending upon their corresponding coefficient of thermal resistance. Since various materials are used in ICs, there are mismatches in the expansion of materials and this unequal expansion leads to the stress in IC packages. Sensors that measure the stress use the piezoresistive property by which the electrical resistivity of a material changes with the application of external stress. Piezoresistive sensors [1–6] are used widely in the packages as they are more sensitive to the stress than the metallic sensor structures [7–9]. Silicon, which is widely used in the manufacture of electronics shows high sensitivity to the piezoresistive effect, that makes it easy to integrate stress sensors to the electronic ICs. Therefore, silicon is used to fabricate different structures/devices that are used in the characterization of the stress in the IC packages [10].

Previously, various resistor rosettes, van der Pauw(VDP) structures [11], MOSFETs(Metal Oxide Semiconductor Field Effect Transistor) [12] that gave the voltage or current readings were used to characterize the stress. The current/voltage readings under applied stress are measured from these devices and the stress is extracted from the measurements. In this work, a CMOS(complementary metal oxide semiconductor) circuit designed by Chen et al. [13] is used to characterize the stress at different temperatures [14–16]. For a better understanding of the work, the circuit is briefly explained in the thesis. The circuit has 16X16 arrays of NMOS(n-channel MOSFET) and PMOS(p-channel MOSFET) sensors with a biasing circuit, subtraction circuit, counter and a multiplexer circuit. The current mismatch in

the sensors under different temperatures in a temperature cycle are obtained by comparing the currents in the sensors using a subtraction circuit. The current mismatches from the output pins are used to extract the stress at different temperatures. This thesis proceeds as follows. Chapter 2 discusses the various piezoresistive sensors and their working principles. Theory behind this work is also explained in the chapter. Chapter 3 gives a brief explanation of the different circuits used in the work. Chapter 4 and Chapter 5 takes the reader through detailed experimental procedures followed in the work along with the simulations and the results of the work. Chapter 5 also outlines certain issues that were encountered during the experiment and also suggests some improvements.

Chapter 2

PIEZORESISTIVE SENSOR

This chapter gives a brief description about the theory of piezoresistivity, equations involved and how this effect in MOSFETS can be utilized in extracting the thermally induced stress in IC packages.

2.1 Piezoresistivity

Piezoresistivity is the property by which the resistance of a material is altered by applying mechanical stress. This property can be used to analyze the thermally induced stress in the IC packages. A resistance change is induced in the package due to the mismatches in the CTR(Coefficient of Thermal Resistance) when subjected to temperature variations. The resistance of a rectangular conductor is given by,

$$R = \rho \frac{l}{wt} \tag{2.1}$$

where ρ is the resistivity of the conductor material, l, w, t are length, width and thickness of the conductor respectively. When stress is applied, the conductor is deformed. In the piezoresistive material, the resistivity [17] is also changed. So, the normalized change in resistance is given by:

$$\frac{\Delta R}{R_o} = \frac{\Delta l}{l_o} - \frac{\Delta w}{w_o} - \frac{\Delta t}{t_o} + \frac{\Delta \rho}{\rho_o} \tag{2.2}$$

In piezoresistive materials, the change in resistance due to the change is resistivity is considerably larger than that due to the change in dimensions. So the resistance change can be expressed by:

$$\frac{\Delta R}{R_o} \cong \frac{\Delta \rho}{\rho_o} \tag{2.3}$$

The conductivity of a material depends both on majority and minority carriers which is governed by the equation,

$$\sigma = qn\mu_n + qp\mu_p \tag{2.4}$$

where q is the charge of an electron, n is the electron density, p is the hole density, μ_n and μ_p are electron mobility and hole mobility respectively. In the case of a doped semiconductor, concentration of majority carriers is comparatively higher than that of minority carriers. So, the conductivity by the minority carriers can be neglected. For an NMOS, the conductivity is given by:

$$\sigma \cong qn\mu_n \tag{2.5}$$

Since change in conductivity, mobility and resistivity can be related by the equation,

$$\frac{\Delta\rho}{\rho} = -\frac{\Delta\sigma}{\sigma} = -\frac{\Delta\mu}{\mu} \tag{2.6}$$

eq.(2.3) becomes

$$\frac{\Delta R}{R} \cong -\frac{\Delta\mu}{\mu} \tag{2.7}$$

When a conductor material is subjected to stress, the mobility of the carriers change as their effective mass is altered. The mobility(μ) of a carrier is inversely proportional to its effective mass as given by the equation,

$$\mu = \frac{q}{m^*}\overline{\tau} \tag{2.8}$$

where q is the charge of an electron, m^* is the effective mass of the carrier and $\overline{\tau}$ is the average scattering time.

In the case of n type silicon, when the stress is applied, the carriers get redistributed among energy valleys in different directions [18]. The electrons in different energy valleys have different effective mass. So, the redistribution of the carriers under stress causes a

change in the overall mobility of the conducting electrons [19–22]. In the case of p type

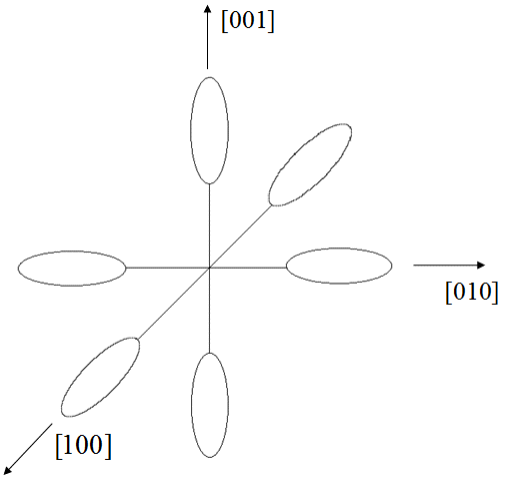


Figure 2.1: Energy valleys in Si with different effective masses.

silicon, the energy bands with different effective masses are aligned in same direction when no stress is applied. But, under a stressed condition, the bands are aligned separate. This causes the redistribution of holes that results in change in effective mass and therefore leads to the change in overall mobility of the holes.

2.2 Piezoresistive Sensors

Piezoresistive sensors are based on the principle of piezoresistivity according to which there is a change in the resistance of the material when a mechanical stress is applied. Mainly, different types of resistor sensors are used as piezoresistive sensors. Since the resistance can be related to the current, MOSFET devices are also used as piezoresistive sensors.

2.2.1 Resistor sensor

Fig.(2.2) shows the principal and primed coordinate system for silicon. The general expression for the normalized change in resistance of resistor that is oriented at an angle ϕ

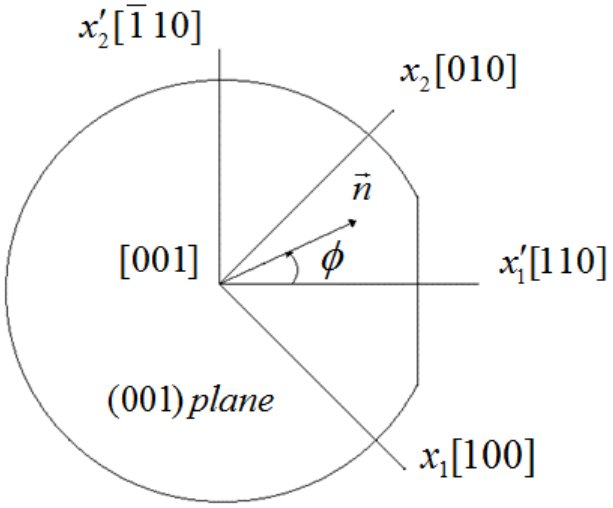


Figure 2.2: Principal and primed coordinate system for (100) Si.

with respect to [110] axis on a (001) plane is given by,

$$\begin{aligned}\frac{\Delta R}{R} = &[(\frac{\pi_{11}+\pi_{12}+\pi_{44}}{2})\sigma'_{11} + (\frac{\pi_{11}+\pi_{12}-\pi_{44}}{2})\sigma'_{22}]\cos^2\phi \\ &+[(\frac{\pi_{11}+\pi_{12}-\pi_{44}}{2})\sigma'_{11} + (\frac{\pi_{11}+\pi_{12}+\pi_{44}}{2})\sigma'_{22}]\sin^2\phi \\ &+\pi_{12}\sigma'_{33} + (\pi_{11}-\pi_{12})\sigma'_{12}\sin 2\phi \\ &+[\alpha_1\Delta T + \alpha_2(\Delta T)^2 + ...]\end{aligned} \tag{2.9}$$

where π_{11}, π_{12}, π_{44} are the three unique on axis piezoresistive coefficients, σ s are the stress coefficients, α_1, α_2 are the coefficients of thermal expansion, ΔT is the change in temperature and ϕ is the angle at which the resistor is oriented to [110]. If the resistor orientation is chosen carefully($\phi = 0^o, 90^o, 45^o, -45^o$), the equation for normalized resistance can be simplified as

$$\frac{\Delta R_0}{R_0} = (\frac{\pi_{11}+\pi_{12}+\pi_{44}}{2})\sigma'_{11} + (\frac{\pi_{11}+\pi_{12}-\pi_{44}}{2})\sigma'_{22} + \alpha_1\Delta T + \alpha_2(\Delta T)^2 + ... \tag{2.10}$$

$$\frac{\Delta R_{90}}{R_{90}} = (\frac{\pi_{11}+\pi_{12}-\pi_{44}}{2})\sigma'_{11} + (\frac{\pi_{11}+\pi_{12}+\pi_{44}}{2})\sigma'_{22} + \alpha_1\Delta T + \alpha_2(\Delta T)^2 + ... \tag{2.11}$$

$$\frac{\Delta R_{45}}{R_{45}} = (\frac{\pi_{11}+\pi_{12}}{2})(\sigma'_{11}+\sigma'_{22}) + (\pi_{11}-\pi_{12})\sigma'_{12} + \alpha_1\Delta T + \alpha_2(\Delta T)^2 + ... \quad (2.12)$$

$$\frac{\Delta R_{-45}}{R_{-45}} = (\frac{\pi_{11}+\pi_{12}}{2})(\sigma'_{11}+\sigma'_{22}) - (\pi_{11}-\pi_{12})\sigma'_{12} + \alpha_1\Delta T + \alpha_2(\Delta T)^2 + ... \quad (2.13)$$

2.2.2 van der Pauw sensor

The van der Pauw(VDP) method, which is used to find the sheet resistance of a material, is also used to measure the stress [11,23]. Since the VDP structures are comparatively smaller in size than the usual resistor rosettes, more localized stress measurements are possible. In the case of silicon, the sheet resistance is highly sensitive to stress. In order to reduce the measurement errors, the VDP structures are to be fabricated with high sheet resistance and the contact effects should be minimized.

2.2.3 MOSFET sensor

As the stress measurements are dependent on the resistance of the channel region, which is very small, more localized measurements are possible. When biased in saturation, the drain current of a MOSFET is based on the resistance of the channel region. So, the MOSFET can be regarded as a resistor that is controlled by the gate voltage.

2.3 Piezoresistive MOSFET

Silicon is widely used to fabricate the MOSFET structures. The n channel (NMOS) enhancement MOSFET is fabricated using p-well CMOS process. In a p type material, n type diffusion is done, which serves as the drain and source terminal. The drain and source terminals are determined by their relative potentials. The gate terminal is insulated from the silicon by a thin high quality insulator. The potential on the gate terminal controls the

flow of electrons through the channel between the source and the drain terminal. In the case of nmos, the source is the terminal that is at low potential and it supplies the electrons. The body(p-well) is connected to the lowest potential. Generally, the body and the source of the MOSFET are tied together.

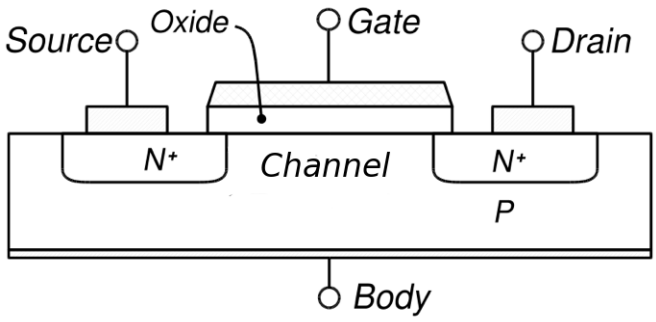


Figure 2.3: N-type MOSFET structure.

In the absence of the channel, the source and drain terminals are isolated by a p region. The MOSFET is said to be 'TURNED OFF'. The gate voltage at which the channel is formed is known as the threshold voltage. When the gate potential is lower than the threshold voltage, there is no current flow ideally. But there might be a small current flow due to the sub-threshold leakage. When the gate voltage is greater than the threshold voltage, a channel is formed and the current flows from drain to source. The drain current is dependent on both the gate to source voltage and drain to source voltage. The MOSFET is said to be 'TURNED ON'. The output characteristics of an NMOS is shown in Fig.(2.4).

Mismatches in the characteristics of MOSFET is used for stress characterization in the study. Mismatches can be expressed as variation in the physical properties among the identical devices. Mismatches can be of two types, namely global and local. Global variations are the random variations in the identical devices at different sites on the wafer or on devices fabricated in different batches. These are caused mainly because of non uniform defect density distribution, uneven doping and different process parameters between different wafers. Local variations are the random variations among adjacent devices on the same

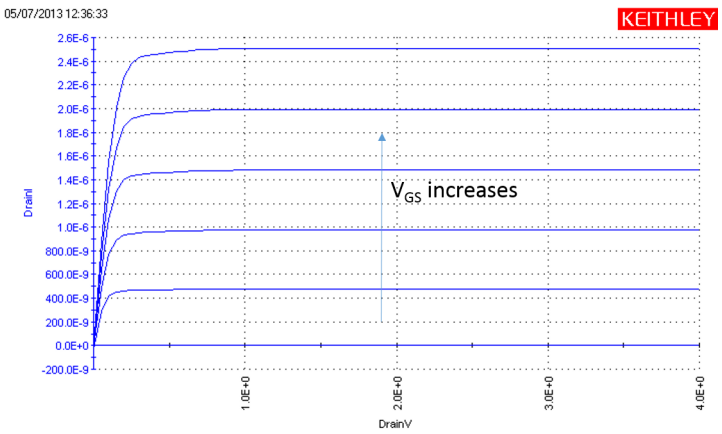


Figure 2.4: Output characteristics of NMOS when V_{GS} increased from 3V to 5V in steps of 0.5V.

wafer. In the study, the local variations are considered. Physical sources for mismatch include edge effects, mobility effects and oxide effects [24]. Some mismatches are caused due to either jagged edge of the photoresist or due to random nature of etching process. The oxide variations may be caused due to the granularity of the polysilicon, surface defects of the silicon crystal, etc. The uncertainty in oxide thickness and permittivity can cause random errors in MOS capacitor. Effective mobility of the charge carriers are also effected by the impurities as well as lattice scattering and piezoresistive effect. In the case of thermally induced stress characterization, the stress sensors are designed to detect only the carrier mobility mismatch due to the mechanical stress induced by the temperature variations. Therefore, all the other mismatches are to be kept as small as possible.

The drain current in NMOS transistor biased in saturation is given by,

$$I_D = \frac{K}{2}(V_G - V_T)^2 \tag{2.14}$$

where K, the conduction factor is defined as

$$K = \frac{W\mu_n C'_{ox}}{L} \tag{2.15}$$

and μ_n is the mobility of electrons, C'_{ox} is the capacitance of the gate per unit area, W and L are the width and length of the channel respectively, V_G is the gate voltage and V_T is the threshold voltage. The normalized drain current can be expressed as

$$\frac{\Delta I_D}{I_D} = \frac{\Delta K}{K} - 2\frac{\Delta V_T}{V_G - V_T} \tag{2.16}$$

From the equation, it can be seen that when the transistor is biased at high overdrive voltage($V_G - V_T$), the normalized current is dependent only on the conduction factor mismatch ΔK. The other factor in the equation can be neglected as it is very small. The mismatch in the conduction factor is caused mainly due to the mismatch in the carrier mobility [13]. So, the eq.(2.16) can be simplified as

$$\frac{\Delta I_D}{I_D} \cong \frac{\Delta \mu}{\mu} \tag{2.17}$$

From eq.(2.7,2.9, 2.17), the equation for normalized drain current can be given as

$$\begin{aligned} \frac{\Delta I}{I} = &-[(\frac{\pi_{11}+\pi_{12}+\pi_{44}}{2})\sigma'_{11} + (\frac{\pi_{11}+\pi_{12}-\pi_{44}}{2})\sigma'_{22}]\cos^2\phi \\ &-[(\frac{\pi_{11}+\pi_{12}-\pi_{44}}{2})\sigma'_{11} + (\frac{\pi_{11}+\pi_{12}+\pi_{44}}{2})\sigma'_{22}]\sin^2\phi \\ &-\pi_{12}\sigma'_{33} - (\pi_{11}-\pi_{12})\sigma'_{12}\sin 2\phi \\ &-[\alpha_1\Delta T + \alpha_2(\Delta T)^2 + ...] \end{aligned} \tag{2.18}$$

For extraction of inplane stress components, the MOSFET channels are oriented in certain angles [13] so that the out-of-plane stress components can be avoided from the eq.(2.18). Table.(2.1) gives the values for piezoresistive coefficients extracted using both N-type and P-type silicon [17]. It can be seen in both the cases that, each one of them is noticeably sensitive to a single coefficient. N-type silicon is most sensitive to coefficient $\pi_D(\pi_{11} - \pi_{12})$ whereas P-type coefficient is sensitive to coefficient π_{44}. While selecting the orientation of

Piezoresistive Coefficient	**N-type Silicon(TPa^{-1})**	**P-type Silicon(TPa^{-1})**
π_{11}	-1022	66
π_{12}	534	-11
π_{44}	-136	1381
$\pi_S = \pi_{11} + \pi_{12}$	-488	55
$\pi_D = \pi_{11} - \pi_{12}$	-1556	77

Table 2.1: Typical Piezoresistive Coefficient For Lightly Doped Silicon$(TPa)^{-1}$.

the sensor rosettes, it should be taken care that only the corresponding coefficients remain in the eq.(2.18).

2.3.1 Shear stress extraction

When two MOSFET elements are oriented at 45^o and -45^o, eq.(2.18) gets simplified as

$$\frac{\Delta I_{45}}{I_{45}} = -(\frac{\pi^n_{11} + \pi^n_{12}}{2})(\sigma'_{11} + \sigma'_{22}) - (\pi^n_{11} - \pi^n_{12})\sigma'_{12} - \alpha^n_1 \Delta T - \alpha^n_2 (\Delta T)^2 \tag{2.19}$$

$$\frac{\Delta I_{-45}}{I_{-45}} = -(\frac{\pi^n_{11} + \pi^n_{12}}{2})(\sigma'_{11} + \sigma'_{22}) + (\pi^n_{11} - \pi^n_{12})\sigma'_{12} - \alpha^n_1 \Delta T - \alpha^n_2 (\Delta T)^2 \tag{2.20}$$

The two element rosettes for shear stress extraction are shown in the Fig.(2.5).

Finding the difference of the equations, eq.(2.19) and eq.(2.20) gives,

$$(\frac{\Delta I_{45}}{I_{45}} - \frac{\Delta I_{-45}}{I_{-45}}) = -2(\pi^n_{11} - \pi^n_{12})\sigma'_{12} \tag{2.21}$$

It can be observed that the direct effects of temperature are also canceled out. Only the thermally induced mechanical stress component σ'_{12} remains in the equation.

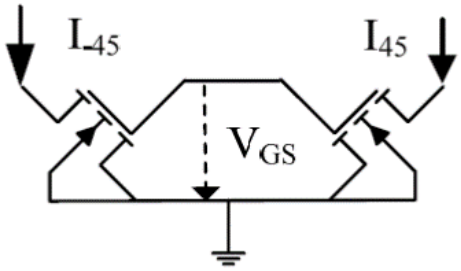


Figure 2.5: Two element MOSFET rosette for shear stress [13].

2.3.2 Normal stress extraction

When two MOSFET elements are oriented at 0^o and 90^o, eq.(2.18) gets simplified as

$$\frac{\Delta I_0}{I_0} = -(\frac{\pi_{11}^p + \pi_{12}^p + \pi_{44}^p}{2})\sigma'_{11} - (\frac{\pi_{11}^p + \pi_{12}^p - \pi_{44}^p}{2})\sigma'_{22} - \alpha_1^p \Delta T - \alpha_2^p (\Delta T)^2 \tag{2.22}$$

$$\frac{\Delta I_{90}}{I_{90}} = -(\frac{\pi_{11}^p + \pi_{12}^p - \pi_{44}^p}{2})\sigma'_{11} - (\frac{\pi_{11}^p + \pi_{12}^p + \pi_{44}^p}{2})\sigma'_{22} - \alpha_1^p \Delta T - \alpha_2^p (\Delta T)^2 \tag{2.23}$$

The two element rosettes for normal stress extraction are shown in the Fig.(2.6).

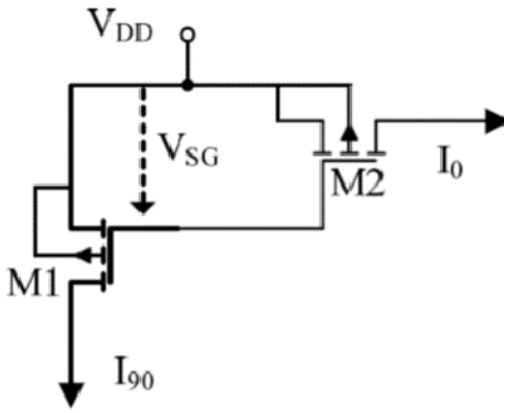


Figure 2.6: Two element MOSFET rosette for normal stress [13].

Finding the difference of the equations, eq.(2.22) and eq.(2.23) gives,

$$(\frac{\Delta I_{90}}{I_{90}} - \frac{\Delta I_0}{I_0}) = \pi_{44}^p(\sigma'_{11} - \sigma'_{22}) \tag{2.24}$$

Also in this case, it can be observed that direct temperature effects are canceled out.

Chapter 3

CIRCUIT DESIGN AND CHIP LAYOUT

The circuit used in the work was designed by Chen et al [13]. Different sections of the circuit are described here for better understanding of the work. As discussed earlier, a sensor cell with N type MOSFETs oriented at 45° and -45° are used for extracting the shear stress component and P type MOSFETs oriented at 0° and 90° are used for extracting the normal stress component. The operation of a sensor cell is based on the current mirror circuit.

3.1 Current Mirror Circuit

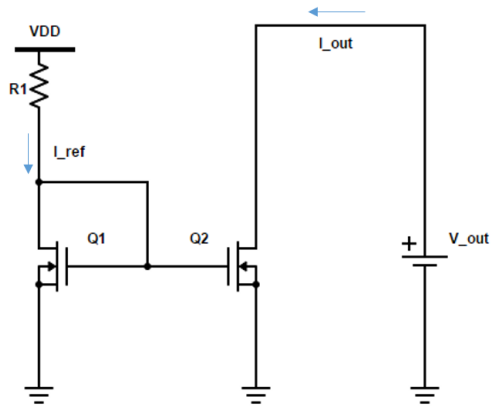


Figure 3.1: Current mirror cell

Fig.(3.1) shows a current mirror circuit. A current mirror circuit copies current from one active device to another. In a MOSFET, the drain current I_D is a function of gate voltage(V_G) and drain to gate voltage(V_{DG}). In the case of transistor Q1, $I_D = I_{-ref}$. Since $V_{DG} = 0$ for Q1, I_{-ref} determines V_G for Q1. The same voltage is applied to the gate of transistor Q2. If Q2 is biased at zero drain to gate voltage, then the drain current of Q2(I_{-out}) becomes equal to drain current of Q1(I_{-ref}).

3.2 PMOS sensor cell

The schematic of the PMOS sensor cell used in the work is shown in the Fig.(3.2). MOSFETs Ms1 and Ms3 are oriented at 90° and Ms2 and Ms4 are oriented at 0° with respect to x_1' axis in [110] direction."D1" and "D2" in the layout indicates the terminal for the drain curents, I_{out1} and I_{out2}. In this case, the equation for extracting stress component becomes,

$$(\frac{\Delta I_{out1}}{I_{out1}} - \frac{\Delta I_{out2}}{I_{our2}}) = \pi_{44}^{p}(\sigma_{11}' - \sigma_{22}') \tag{3.1}$$

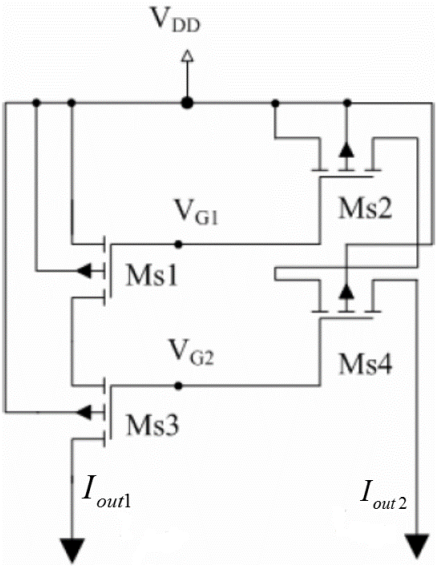


Figure 3.2: PMOS sensor cell schematic [13].

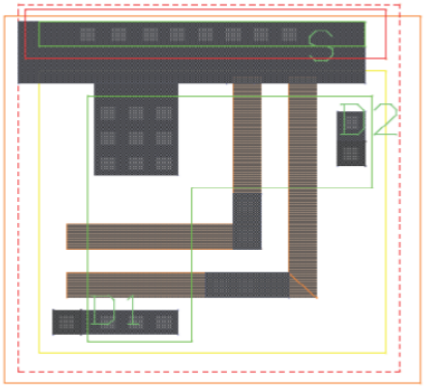


Figure 3.3: PMOS sensor cell layout [13].

3.3 NMOS sensor cell

The schematic of the NMOS sensor cell used in the work is shown in the Fig.(3.4). MOSFETs Ms1 and Ms3 are oriented at -45° and Ms2 and Ms4 are oriented at 45° with

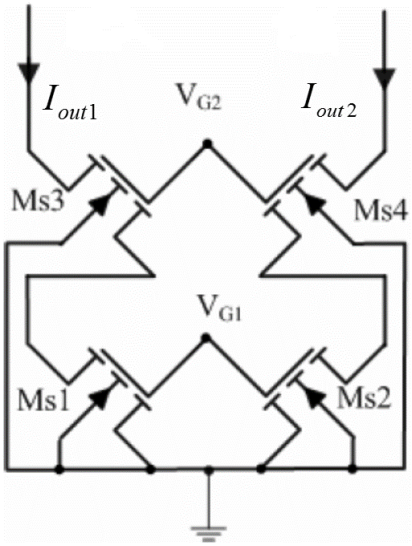


Figure 3.4: NMOS sensor cell schematic [13].

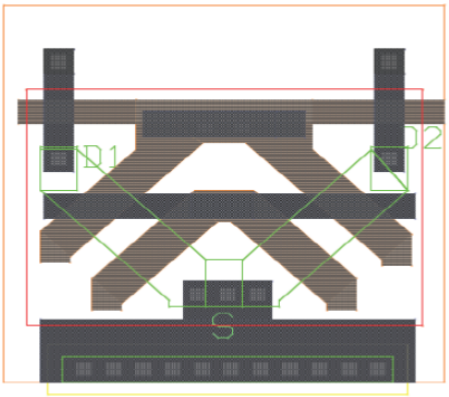


Figure 3.5: NMOS sensor cell layout [13].

respect to x_1' axis in [110] direction.The symbols "D1" and "D2" in the layout indicates the terminal for the drain curents, I_{out1} and I_{out2}. In this case, the equation for extracting stress component becomes,

$$(\frac{\Delta I_{out1}}{I_{out1}} - \frac{\Delta I_{out2}}{I_{out2}}) = -2(\pi_{11}^n - \pi_{12}^n)\sigma_{12}' \tag{3.2}$$

3.4 Subtraction circuit

The subtraction circuit was used so that the difference of the two drain currents can be obtained directly. The schematic of the subtraction circuit is given in the Fig.(3.6). The circuit consists of a cascode current mirror with four transistors placed close to each other in the same orientation so that the mismatch is minimized. When the two currents I_1 and I_2 is

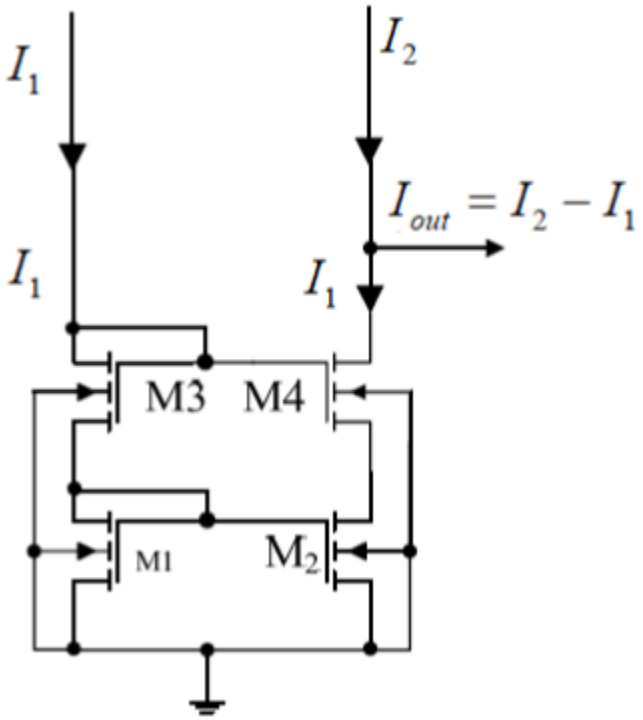


Figure 3.6: Subtraction circuit schematic [13].

injected, I_1 is copied and same amount of current is drained from the output node(from I_2). Since the voltage at the output node remains constant, the output current I_1 is the difference of the two currents, I_1 and I_2.

3.5 Biasing circuit

In both PMOS and NMOS array, the biasing circuit is shared by single row. The biasing circuit used in the circuit is described below.

3.5.1 PMOS sensor cell circuitry

Fig.(3.7) shows the PMOS sensor cell with biasing, subtraction and output circuitry. The sensor cell is marked by the shaded region and consists of transistors Ms1, Ms2, Ms3, Ms4. The sensor cell is repeated 256 times(16X16) to form the complete sensor array.The sensor cell is biased using the biasing circuit consisting of transistors Mb1 and Mb2. The subtraction circuit is formed by the transistors M1, M2, M3 and M4 that provides the current difference I_{diff} and the output current I_{out} is mirrored by transistors Mo1 and Mo2.

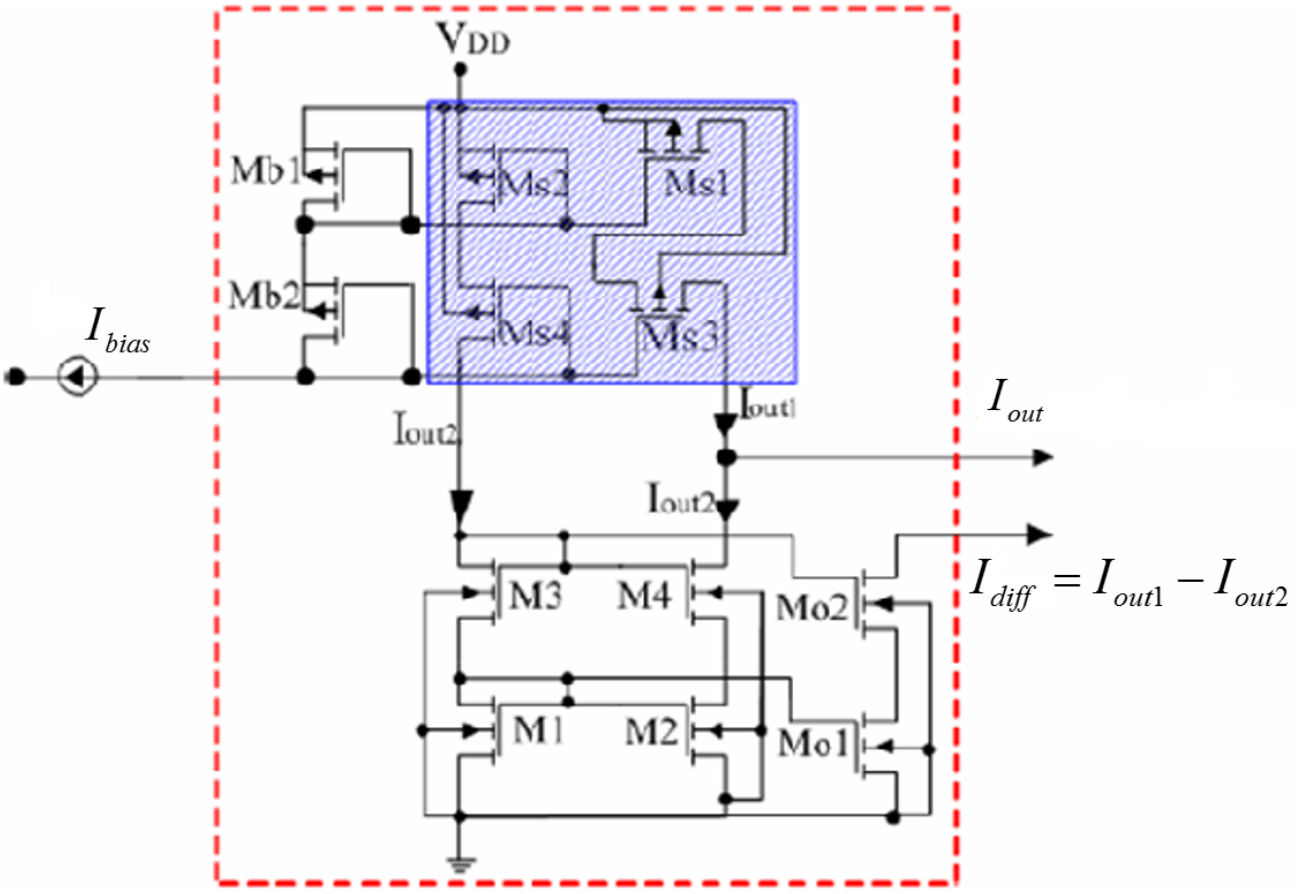


Figure 3.7: PMOS sensor cell with bias, subtraction and output circuitry [13].

3.5.2 NMOS sensor cell circuitry

Fig.(3.8) shows the NMOS sensor cell with the biasing, subtraction and output circuitry. Different sections of the circuitry are marked and labeled similar to the ones in PMOS sensor. The NMOS sensor cells are also repeated 256 times(16X16). In the case of both the sensors, the bias circuit is shared by a row of sensors and the subtraction circuit is shared by the whole array. As in PMOS, the subtraction circuit, which consists of transistors M1, M2, M3 and M4, provides the current difference I_{diff} and the output current is mirrored by the transistors Mo1 and Mo2.

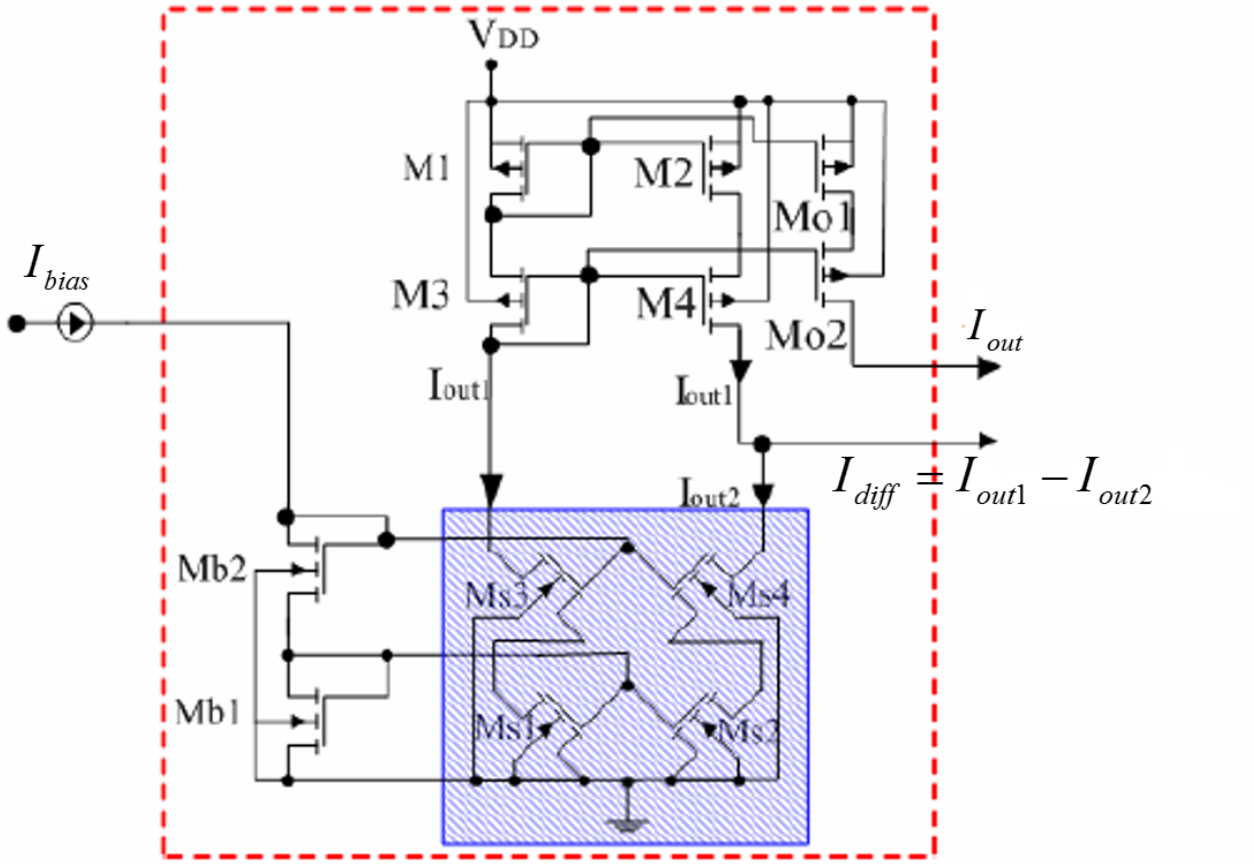


Figure 3.8: NMOS sensor cell with bias, subtraction and output circuitry [13].

3.6 Multiplexer and counter

The multiplexer used in the work is designed with the pass transistor logic in which the control signal is applied to the gate of the transistor for its operation. Multiplexers are used to selectively bias a row of sensors and to select a column as an output. A 5 bit column select multiplexer and a 4 bit row select multiplexer is used in the design.

A counter was also used in the circuit in order to generate the signal for scanning the sensors in the array so as to save the output pins. A ripple counter designed with master-slave toggle flip-flops were used. Transmission gates were used to construct the flip-flops and the flip-flops are controlled by a complimentary clock signal. The output signal is buffered before it is sent to drive the multiplexers. When the reset signal RST is released, all outputs are set to '1'.

3.7 System Schematic

The system schematic used for NMOS array is shown in the Fig.(3.9). The biasing circuit and the subtraction circuit is shown in the dashed-line boxes. For the entire circuit, a single power supply, single biasing current and one clock signal are needed. Two outputs are measured.

The entire row in the array share a single biasing circuit and the whole array share a single subtraction circuit. The column selectors are implemented in 5 bit 32 to 1 configuration and the row selectors are implemented in 4 bit 16 to 1 configuration. Since the arrays are in the form of 16X16 sensor cells, 4-bit column select multiplexer is sufficient for each array. The fifth bit of the column selector can be used as an array selector.

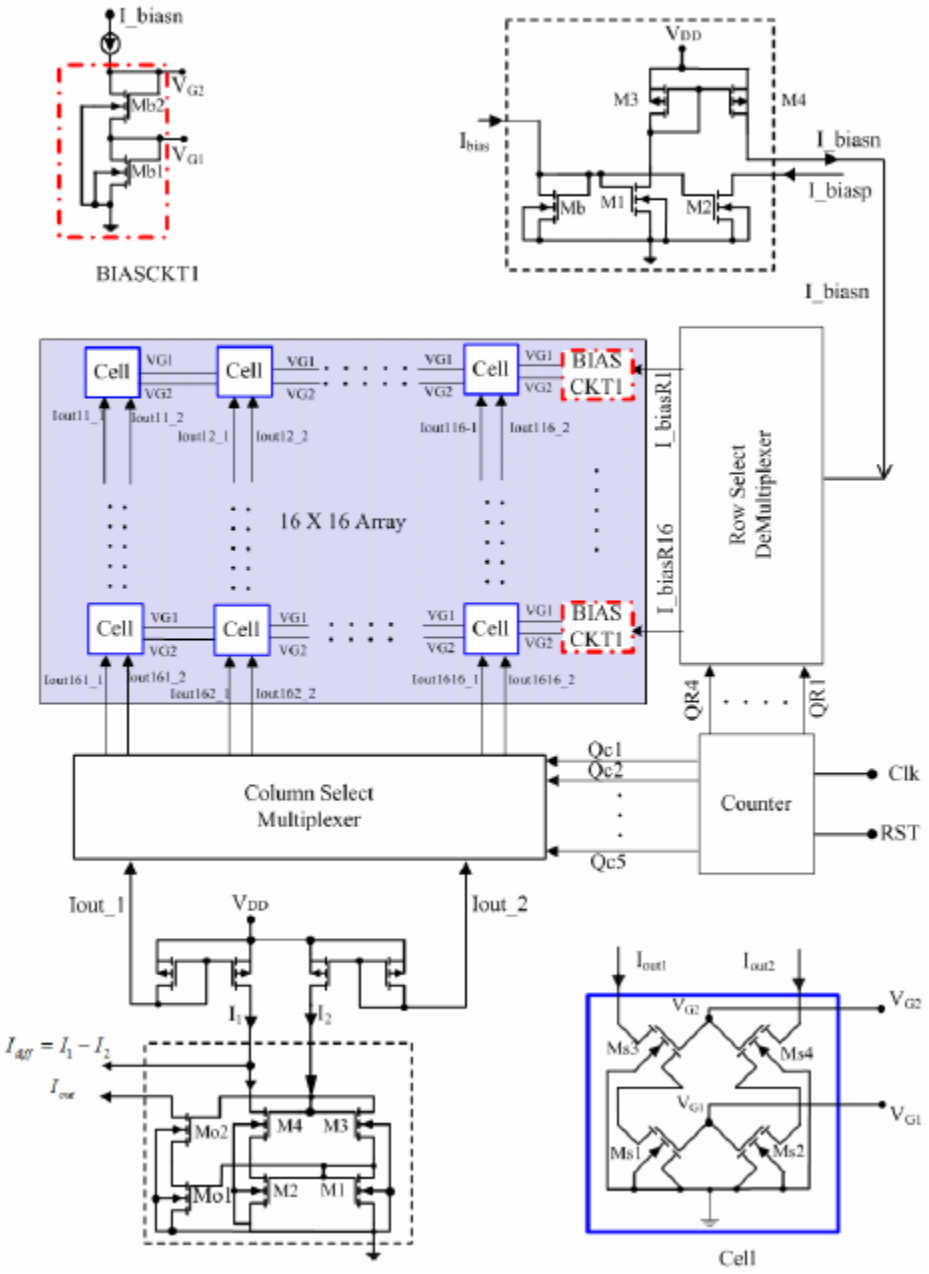


Figure 3.9: System schematic for NMOS sensor array [13].

3.8 Chip Layout

Fig.(3.10) shows the layout of the chip used for the stress characterization. The function that each part does is as indicated in the figure. The design uses 9-bit counter to scan all the sensors in NMOS and PMOS array. With the subtraction circuit, multiplexer and counter circuits, the current difference(I_{diff}) and the current(I_{out}) outputs can be obtained from the two pins.

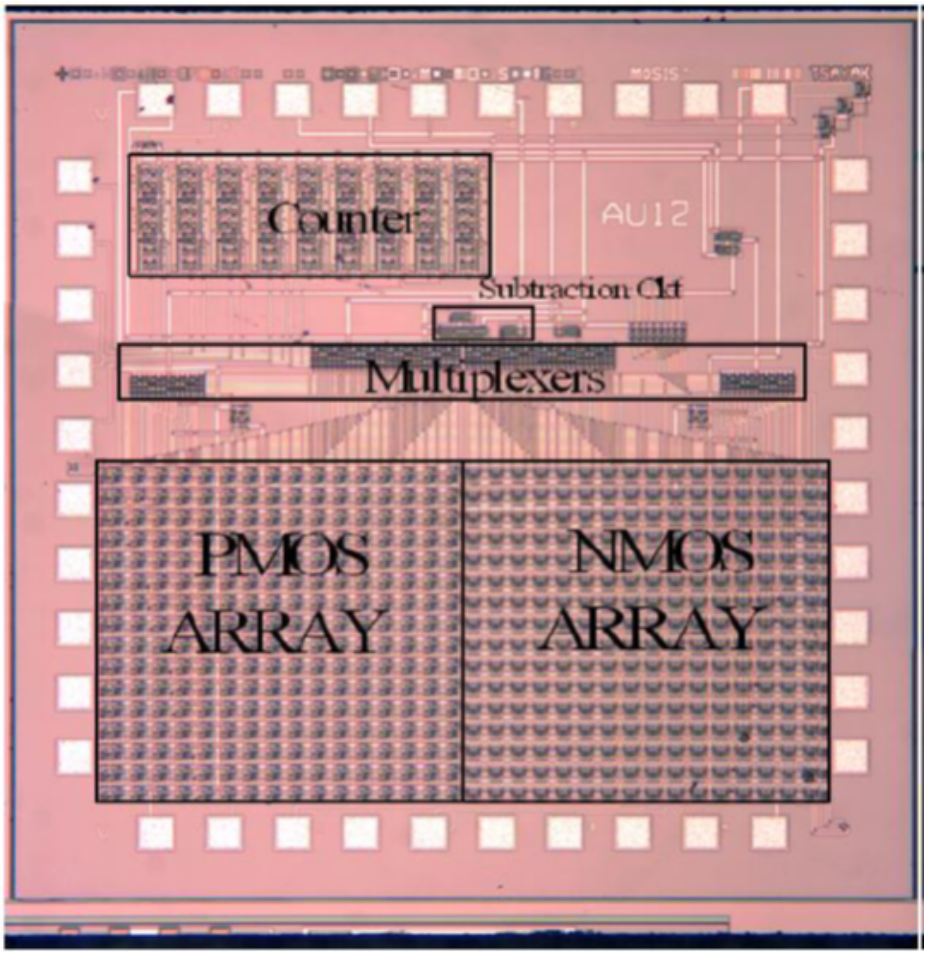


Figure 3.10: Chip Layout [13].

Chapter 4

PIEZORESISTIVE COEFFICIENT EXTRACTION

The piezoresistive coefficient [25] of p-type silicon π_{44}^{p} at temperatures ranging from -180^{o}C to 80^{o}C was extracted from the samples using the chip-on-beam technology.

4.1 Experimental setup and procedure

A Delta oven with a built-in four-point-bending fixture (4PB) as shown in Fig.(4.1), a PCB beam on which the chip is mounted, a voltage and a current source, a wave generator and NI LABVIEW interfaced Agilent digital multimeter was used for the coefficient extraction. Once the current difference readings are obtained from the measurements, eq.(3.1) was used for the coefficient extraction. The stress component, $(\sigma'_{11} - \sigma'_{22})$ for the chip on beam at different temperatures were simulated in ANSYS by giving the different properties of materials to the software. On each sample, the first sensor cell on PMOS array was used for the extraction. A minimum voltage of 6V is applied for the proper operation of the chip and the output nodes were biased at a voltage(1.5V) twice higher than the overdrive voltages in order to make sure that the stress sensitive transistor is working in the saturation region. A biasing current of 5μA is also applied. The counter is reset so that the first sensor in the PMOS array is selected. The desired temperature is set in the oven and a force of 12.74N was applied on the beam with the help of 4PB fixture and load cell. A stabilization time of 15 minutes is allowed at each temperature. After the outputs at a temperature are taken, the load is released and the oven is set to the next temperature and the procedure is repeated. Initially, the outputs at room temperature is taken and then the oven is cooled down to -180^{o}C and the current measurements are taken. Then the temperature is brought up gradually and the output measurements are taken at regular intervals.

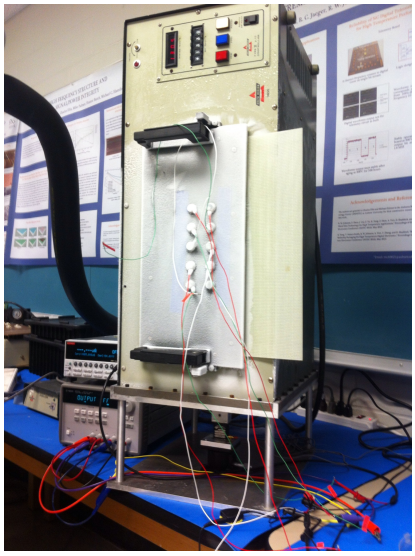


Figure 4.1: Delta oven with a built-in 4PB fixture.

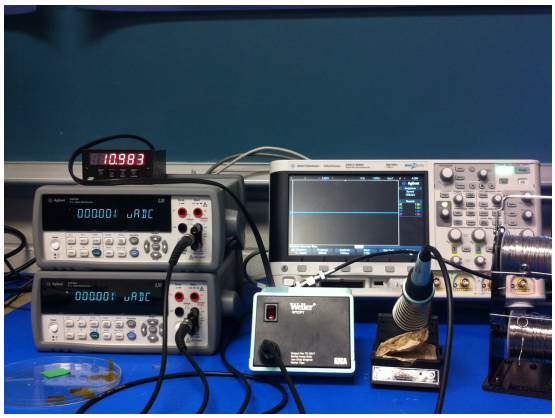


Figure 4.2: Multimeters and waveform generator.

4.2 Finite Element Simulation

ANSYS workbench has been used for mechanical simulations to extract normal stress data under mechanical and thermal load at different temperatures. The model is shown in Fig.(4.3). The beam is made of PCB material and the silicon chip is attached to the beam using ME525. For the simulations, properties of different materials at different temperatures such as Young's modulus, Poisson's ratio, bulk modulus, shear modulus were obtained from various references at a wide range of temperatures and were extrapolated when required to the temperature range of the measurement data. Table(4.2) shows the material properties

for PCB(printed circuit board). Table(4.3) and Table(4.4) has the properties for ME525 [26] and silicon respectively. The coefficient of thermal expansion for the materials is tabulated in Table(4.1). A load of 12.74 N was applied and was simulated at each temperature in the temperature cycle. As shown in the Fig.(4.4), points B and C is fixed and the load is applied at points A and D.

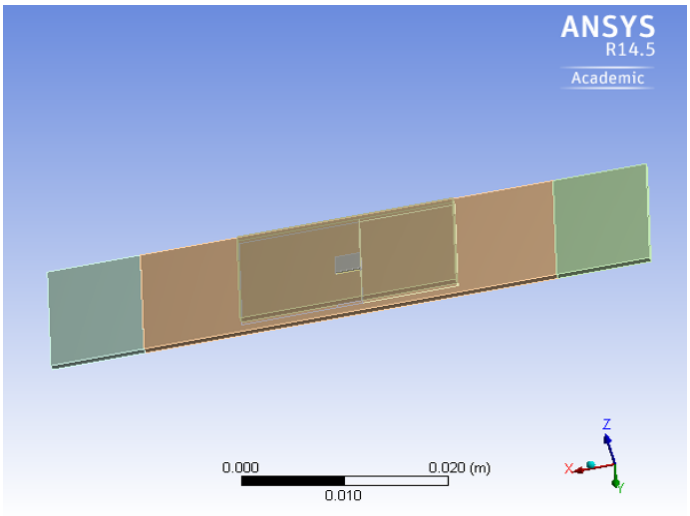


Figure 4.3: Model used for simulation.

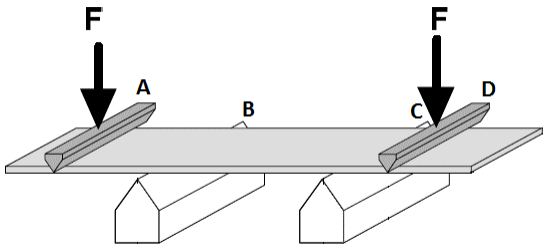


Figure 4.4: Four point bending fixture [13].

Fig.(4.5) to Fig.(4.8) shows the normal stress on the die surface at different temperatures from the simulation results. Since the sensor cell used in the work is located in center of the chip towards the left side, the stress values at that location is considered for extraction of the coefficients. From the simulation, it is quite clear that the stress effect induced by the change in temperature at the desired position decreases as the temperature is increased.

Temp(C)	**Material**	**Coefficient of Thermal Expansion(K^{-1})**
25	Silicon	2.6E-06
25	ME525	6.8304E+10
25	PCB	1.3E-05

Table 4.1: Coefficient of thermal expansion for different materials at 25^0C.

Temp	**Young's Modulus(MPa)**	**Poisson's Ratio**	**Bulk Modulus(Pa)**	**Shear Modulus(Pa)**
25	1.72E+05	0.21	9.8851E+10	7.1074E+10

Table 4.2: Material properties for PCB at 25^0C.

Temp	**Young's Modulus(MPa)**	**Poisson's Ratio**	**Bulk Modulus(Pa)**	**Shear Modulus(Pa)**
25	10430	0.3	8.6917E+09	4.0115E+09
50	9850	0.3	8.2083E+09	3.7885E+09
75	8750	0.3	7.2917E09	3.3654E+09

Table 4.3: Material properties for ME525 at different temperatures.

Temp	**Young's Modulus(MPa)**	**Poisson's Ratio**	**Bulk Modulus(Pa)**	**Shear Modulus(Pa)**
-151	1.729E+05	0.262	1.2108E+11	6.8502E+10
-133.4	1.724E+05	0.262	1.2073E+11	6.8304E+10
-113.4	1.72E+05	0.262	1.2045E+11	6.8146E+10
-93.2	1.715E+05	0.262	1.201E+11	6.7948E+10
-71.4	1.71E+05	0.262	1.1975E+11	6.775E+10
-48.2	1.706E+05	0.262	1.1947E+11	6.7591E+10
-23.6	1.7E+05	0.262	1.1905E+11	6.7353E+10
0.6	1.697E+05	0.262	1.1884E+11	6.7235E+10
25.1	1.69E+05	0.262	1.1835E+11	6.6957E+10
49.9	1.684E+05	0.262	1.1793E+11	6.6719E+10
75.1	1.679E+05	0.262	1.1758E+11	6.6521E+10
100.6	1.673E+05	0.262	1.1716E+11	6.6284E+10
125.9	1.668E+05	0.262	1.1681E+11	6.6086E+10
151.5	1.662E+05	0.262	1.1639E+11	6.5848E+10

Table 4.4: Material properties for Silicon at different temperatures.

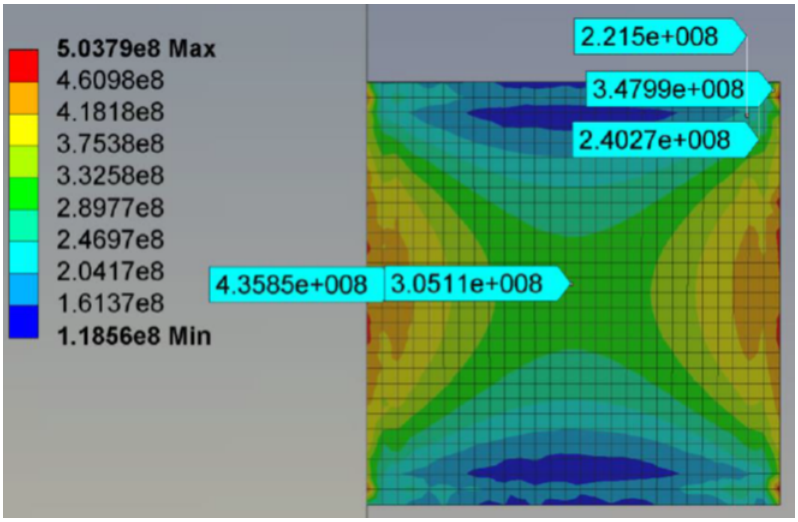


Figure 4.5: Normal stress on die at -180°C.

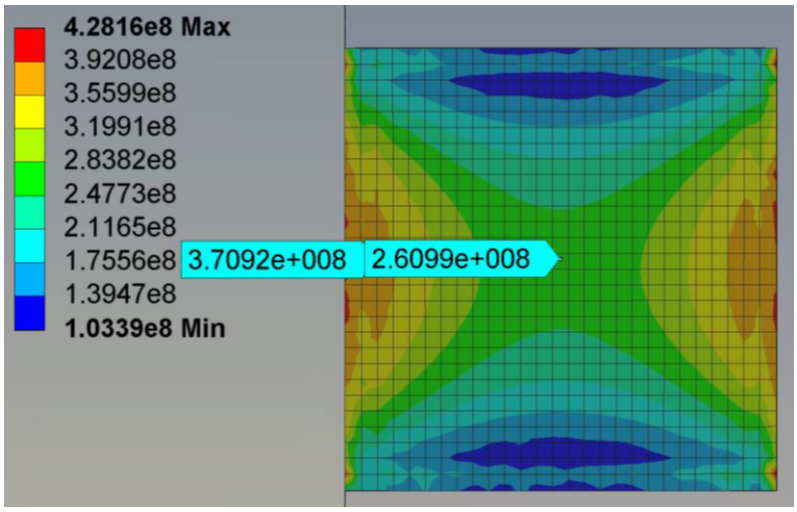


Figure 4.6: Normal stress on die at -140°C.

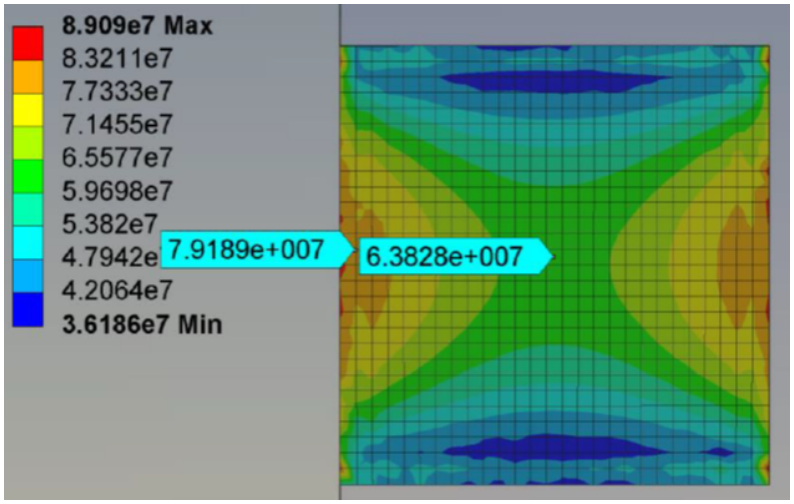


Figure 4.7: Normal stress on die at 40°C.

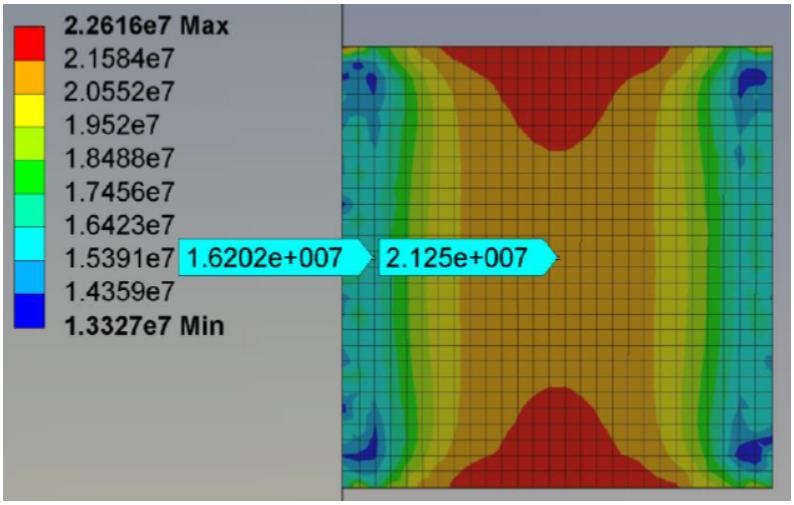


Figure 4.8: Normal stress on die at 80°C.

4.3 Coefficient Extraction

Once the currents and current differences from the sensor cell is obtained, the current differences are normalized to the currents at the corresponding temperature. Then the difference between the normalized current at each temperature and the normalized current at the reference temperature(80°C) is found. This value makes up the left hand side of the eq.(3.1) which is used to extract the coefficients. The normal stress values at each temperature is obtained from the finite element simulations as shown in Fig.(4.9). Then the slope of variation of normal stress with temperature is found, which is then multiplied with the change in temperature with respect to reference temperature(80°C). This values is the stress component($\sigma'_{11} - \sigma'_{22}$) of eq.(3.1). The values are then substituted in the equation and the π^p_{44} coefficients are extracted. The coefficients obtained from different samples are shown in Fig.(4.10) to Fig.(4.14). The average coefficient value with values from individual samples are plotted in Fig.(4.15).

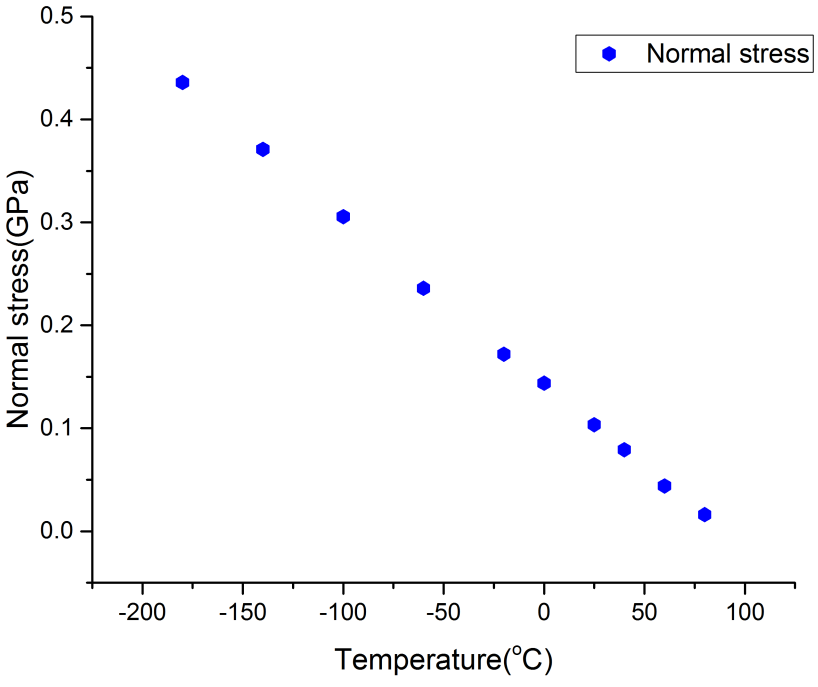


Figure 4.9: Normal stress values obtained from simulations.

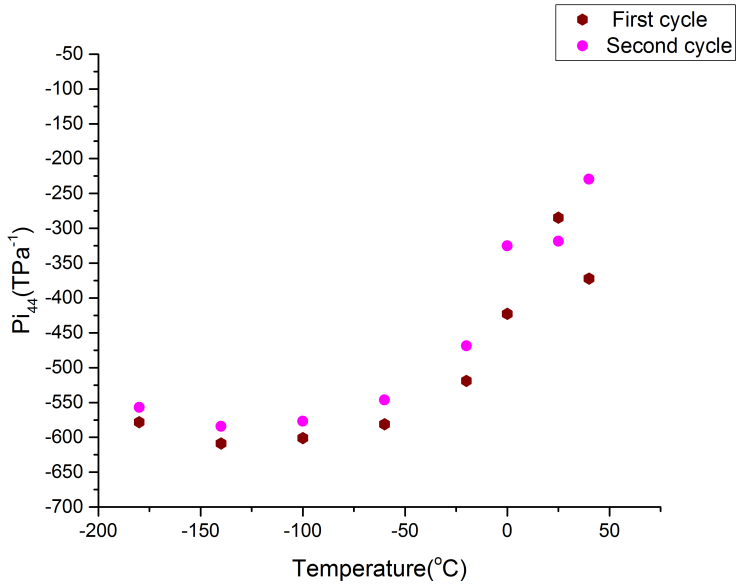


Figure 4.10: π_{44}^{p} extracted from sample 2.

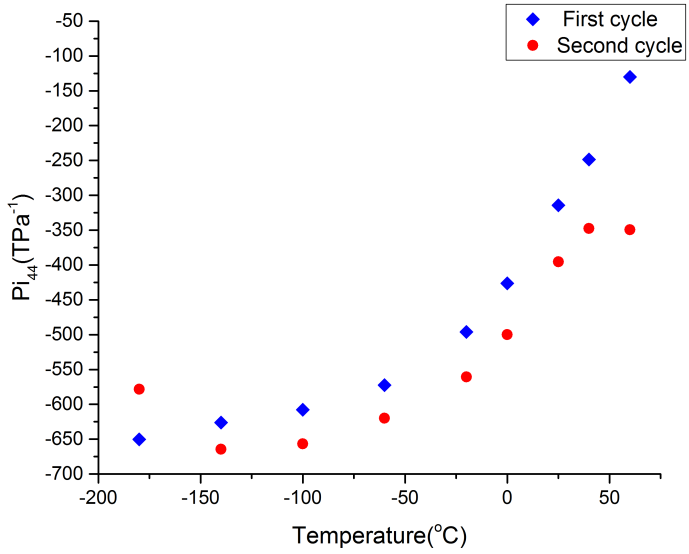


Figure 4.11: π_{44}^{p} extracted from sample 4.

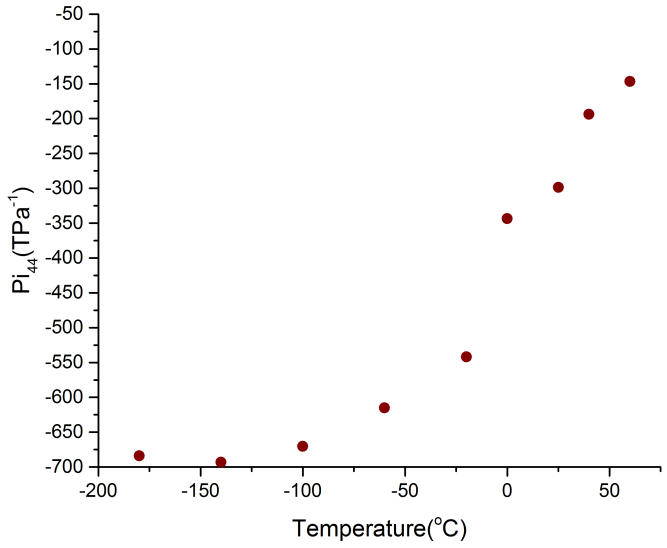


Figure 4.12: π_{44}^{p} extracted from sample 6.

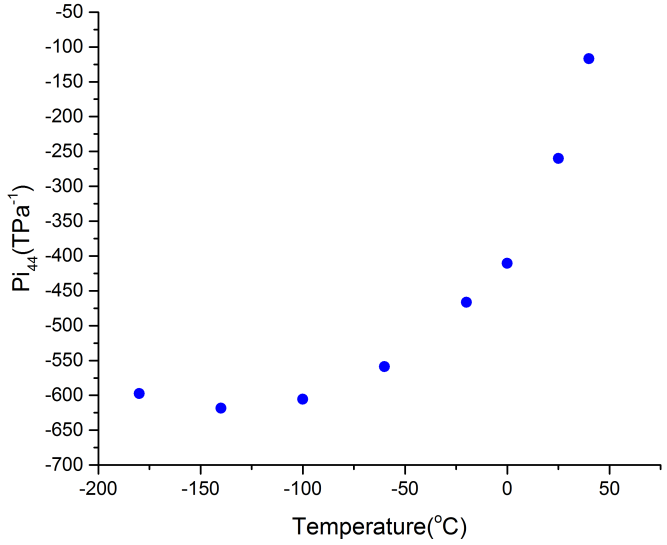


Figure 4.13: π_{44}^{p} extracted from sample 7.

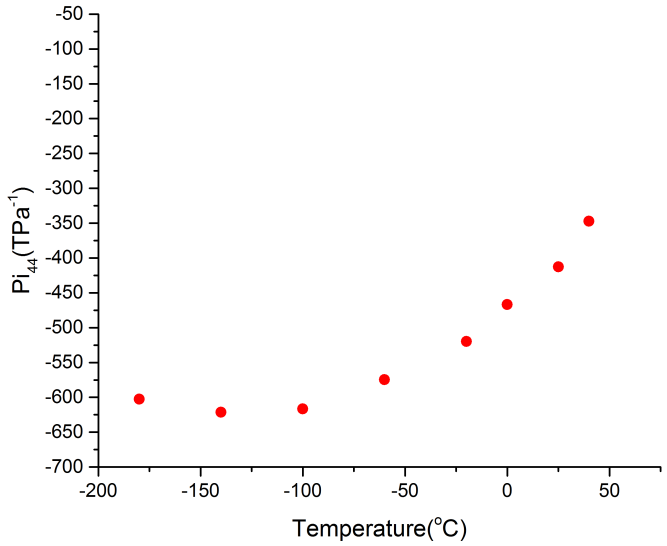
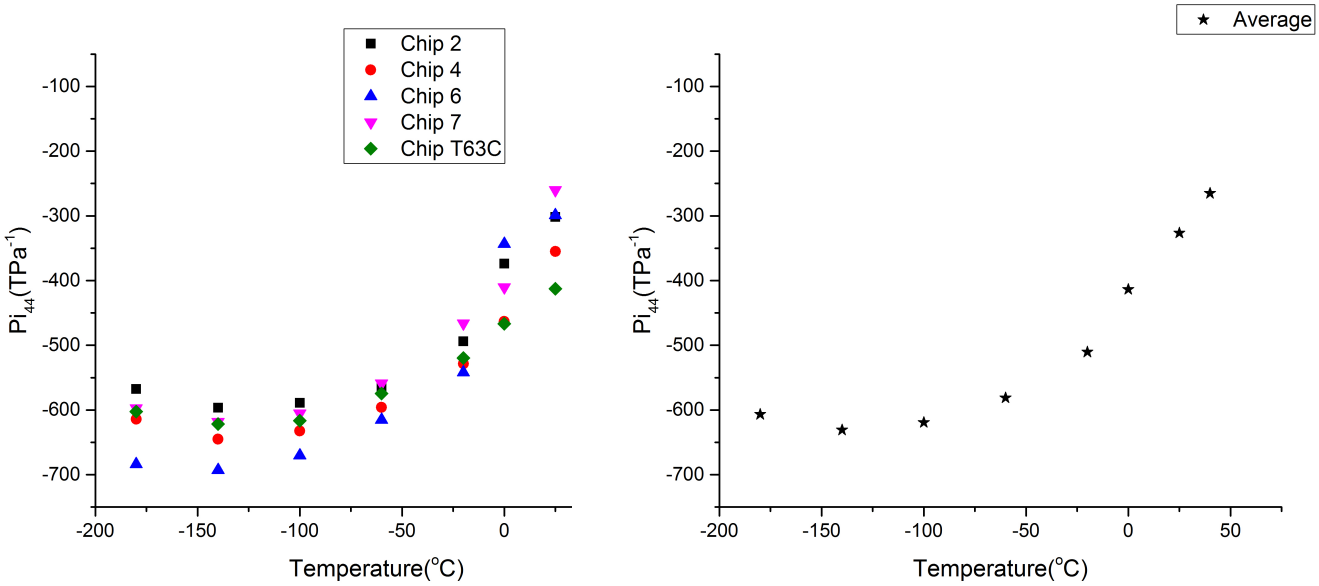


Figure 4.14: π_{44}^{p} extracted from sample T63C.



(a) Values from all samples.

(b) Average of all samples.

Figure 4.15: π_{44}^{p} extracted from all samples

The average π_{44}^{p} values from different samples are tabulated in Table.(4.5). The coefficients were extracted from seven samples. But, the values obtained from two samples were not close to the values of the other five samples. So, the values from those two samples were not considered. The coefficient values from other samples fell in a close range [27].

Temperature(°C)	π_{44}^{p}**(TPa^{-1})**
-180	-610
-140	-630
-100	-620
-60	-580
-20	-510
0	-410
25	-330
40	-270

Table 4.5: Average π_{44}^{p} values from the samples.

Chapter 5

STRESS EXTRACTION

The stress induced in the package was extracted from the sensor cells in the corner of the die. NMOS sensor cell was used for the extraction. The n coefficients($\pi_D^n = \pi_{11} - \pi_{12}$) used for the extraction was extracted in the work by C-H. Cho et al. [28].

5.1 Experimental Setup and Procedure

A Delta oven, which is cooled with liquid nitrogen, a voltage source, Keithley 4200SCS were used for the experiment. Once the currents from the two MOSFETS in a sensor cell is obtained, the coefficients at corresponding temperature and the eq.(3.2) was used to extract the stress components. First the Delta oven with the sample is set to the desired

Figure 5.1: Experimental Setup.

temperature. Once the temperature is attained, a stabilization time of 15 minutes is allowed at each temperature. 6V is applied to the chip by using a voltage source. Then using Keithley 4200SCS, a biasing current of 5μA is forced and the output currents from both the MOSFETS are measured. Once the current readings from the two MOSFETS in a sensor

cell are obtained, the difference between drain current of one MOSFET in the sensor cell and the average of the two drain currents is found. This value is then normalized with the average of two drain currents. The same procedure is repeated for the next drain current of the next MOSFET in the same sensor cell. From this value, the offset value at room temperature is removed. For example, consider the two MOSFETS oriented at 45° and -45°:

$$(\frac{\Delta I_{out1}}{I_{out1}} - \frac{\Delta I_{out2}}{I_{out2}}) = \frac{I_{45} - I_{avg}}{I_{avg}} \tag{5.1}$$

where I_{avg} is the average of drain currents from two MOSFETS from one sensor cell. This value at each temperature along with the coefficients at the corresponding temperature is plugged into the eq.(3.2) and the stress components are obtained.

The Fig.(5.2) shows the chip layout designed by Chen et al. [13] where the magnified section shows the sensor cells at the corner of the chip that was used to extract the stress. In the figure, cell #1 is the one at the corner, cell #2 is the one in the middle and the cell #3 is the one closest to the center of the die.

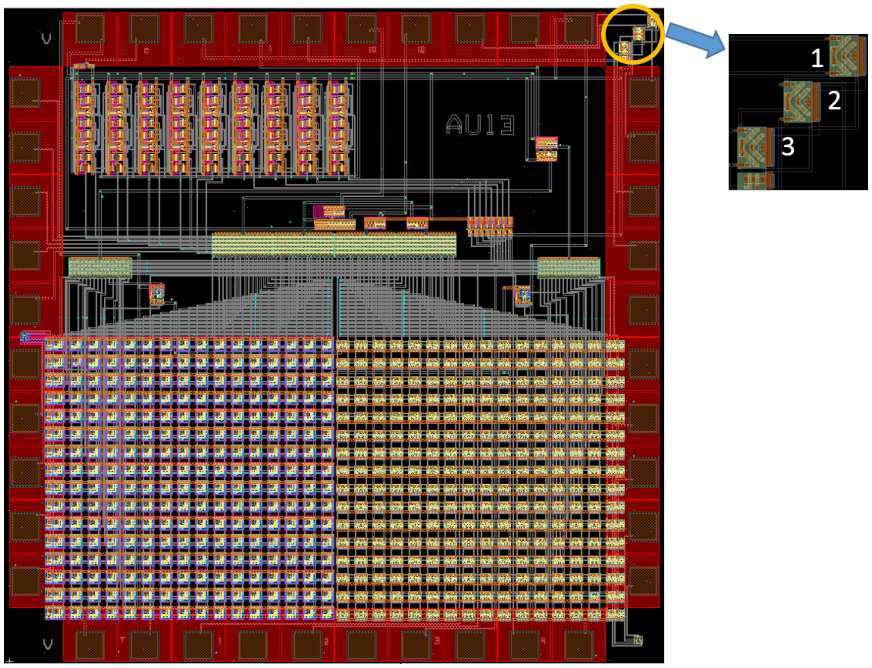


Figure 5.2: Chip layout with NMOS sensor cells at the top right corner of a 4mm^2 die with zoomed in view of the sensor cells [13].

5.2 Stress from Simulation

Thermally induced stress in the package was modeled and simulated using ANSYS workbench by providing the available temperature dependent properties of different materials in the package. The model used for simulation is shown in Fig.(5.3). The package is assumed to be ceramic and the silicon chip is assumed to be attached to the package using ME525 underfill. The temperature dependent properties for the underfill for simulations were obtained from Rahim et al [29]. The simulated stress values at different temperatures at desired locations were used to compare with the stress relation obtained from the measured data.The simulation results for shear stress at 25°C are shown in the Fig.(5.4) and the three sensor cells are located at the top right corner of the die as indicated in the figure. The shear stress component σ'_{12} obtained from the finite element analysis for cell #1 is plotted in the Fig.(5.5) and can be described by:

$$\sigma'_{12} = 0.0025 * T - 0.075MPa \tag{5.2}$$

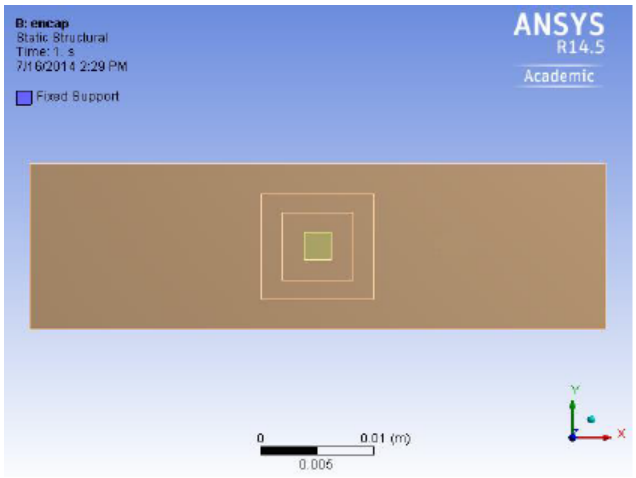


Figure 5.3: The package model used in ANSYS for simulation.

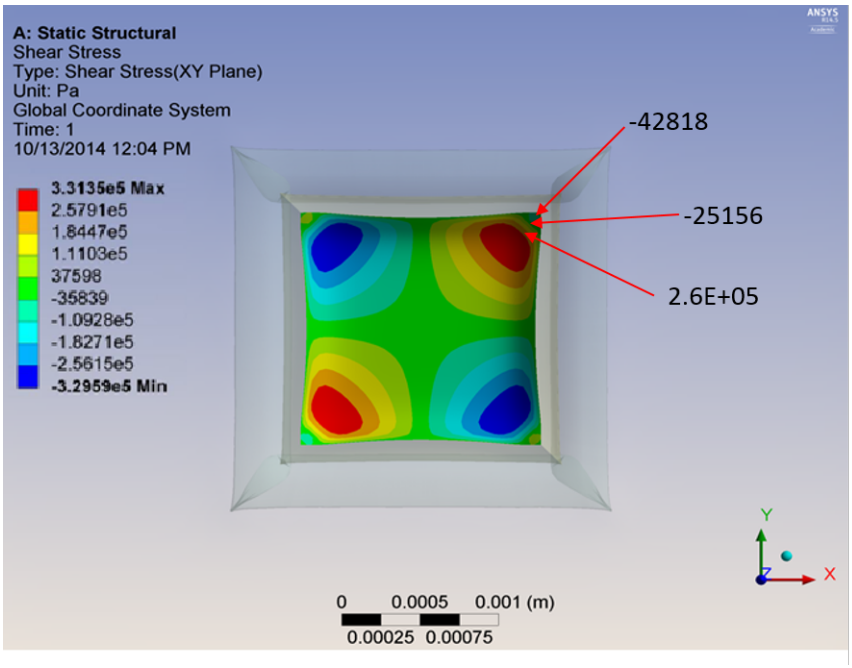


Figure 5.4: Simulation showing shear stress component at positions of sensor cells at 25°C.

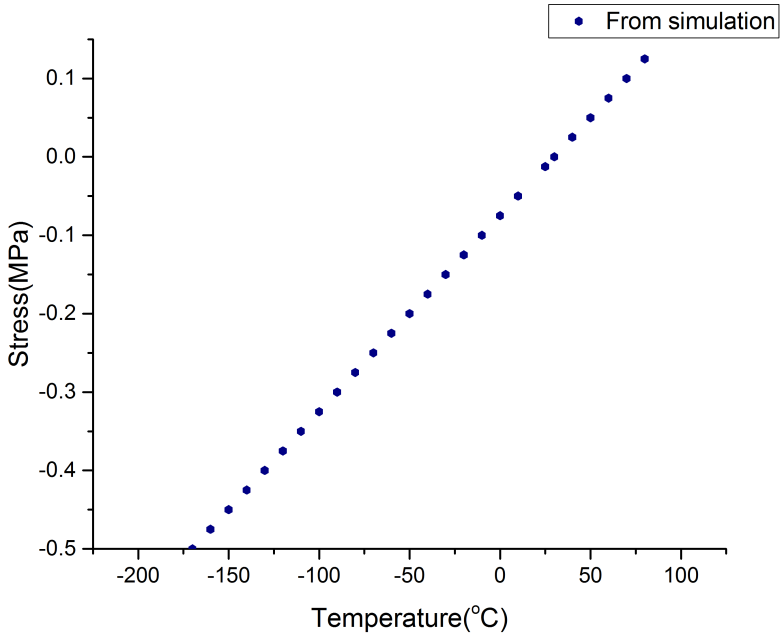


Figure 5.5: Shear stress from simulation for cell #1.

5.3 Stress from Measurements

Fig.(5.6) shows the plot of average cell current obtained from the measurements at different temperatures. Averaging the two output currents cancels the effect of stress, and provides the proper normalization current as a function of temperature. Rotation of the transistors modifies the W/L ratio of the transistors. Hence the current output is 2.5μ A when 5μ A is injected into the current mirror. Fig.(5.7, 5.8, 5.9) present the normalized output current, as functions of temperature, from the sensors that are proportional to the shear stress at the sensor locations and correspond to the cell #1, cell #2 and cell #3 respectively. The magnitude of the normalized current difference is close in all the three cells. It can be seen that the sign of the stress changed with the temperature. In both cells, the normalized current difference curves flatten out towards higher temperatures. This may be due to softening of the die attachment layer, which can reduce the stress.

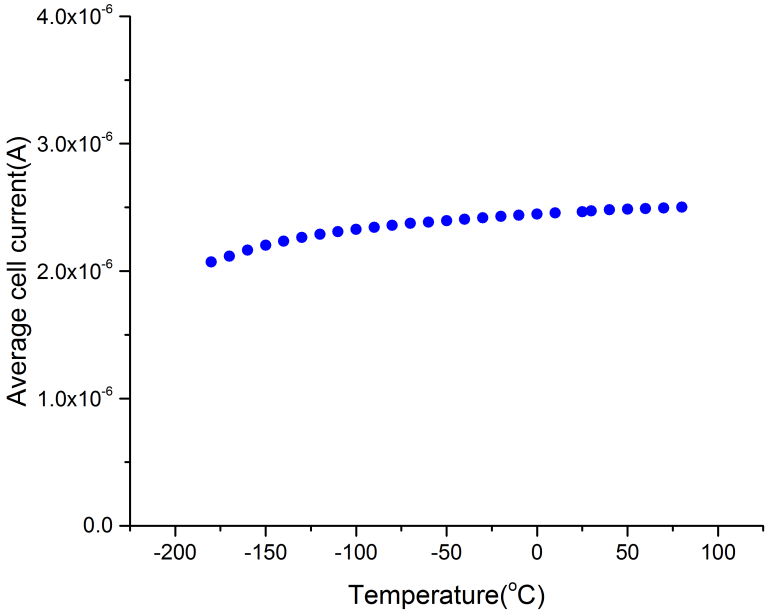


Figure 5.6: Average cell current vs. temperature.

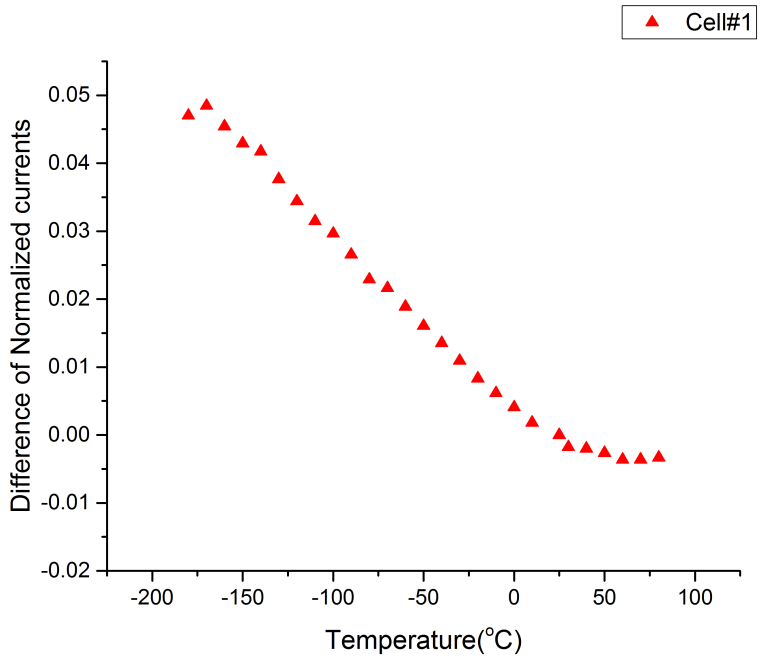


Figure 5.7: Plot of normalized output current vs. temperature for sensor cell #1.

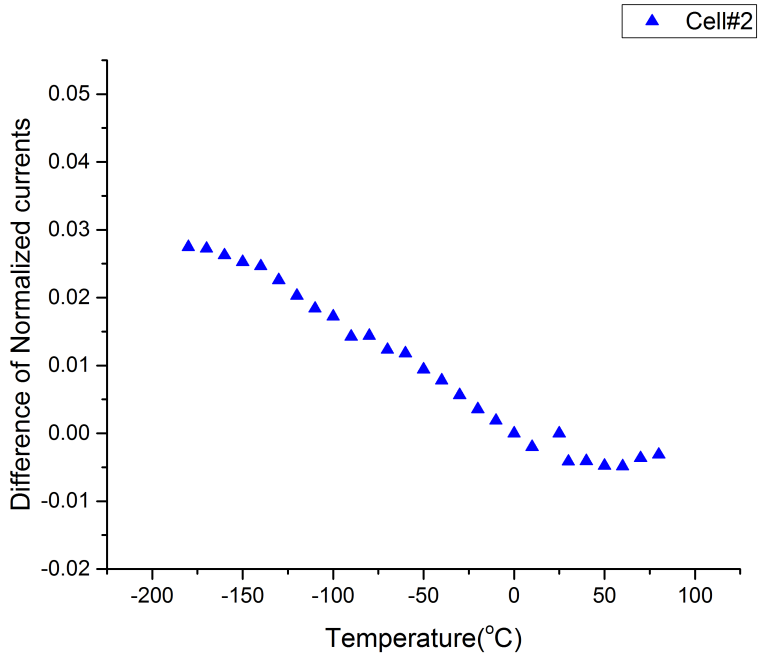


Figure 5.8: Plot of normalized output current vs. temperature for sensor cell #2.

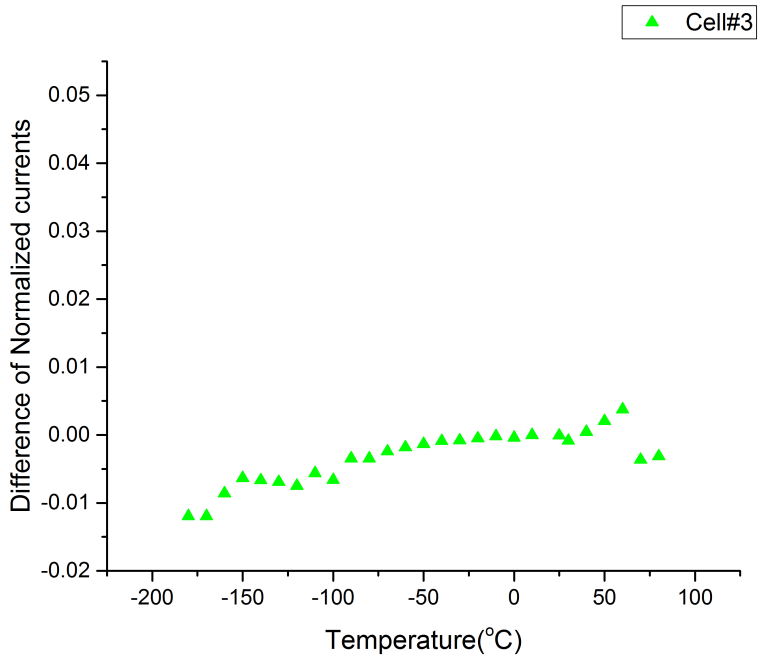


Figure 5.9: Plot of normalized output current vs. temperature for sensor cell #3.

The data obtained from the measurements are used in combination with the piezoresistive coefficients of Chen et al. [30] at room temperature and the trend at other temperatures from C-H. Cho et al. [28] to extract the stress:

$$2\pi_D^n = 1120(1 - 3.1 * 10^{-03}(T - 300)) \tag{5.3}$$

$$\sigma'_{12} = \frac{I_{D,diff}}{-2\pi_D^n} \tag{5.4}$$

where $I_{D,diff}$ is the difference of normalized currents at each temperature for each of the measured data. The piezoresistive coefficients used for extraction at each temperature is plotted in the Fig.(5.10). The variation of σ'_{12} with the temperature is shown in Fig.(5.11) for the sensor cell #1.

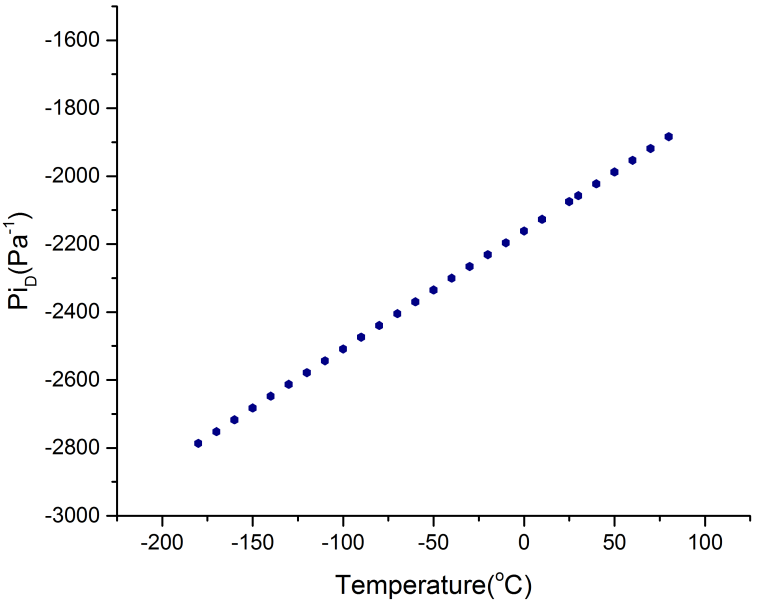


Figure 5.10: Coefficients used for stress extraction.

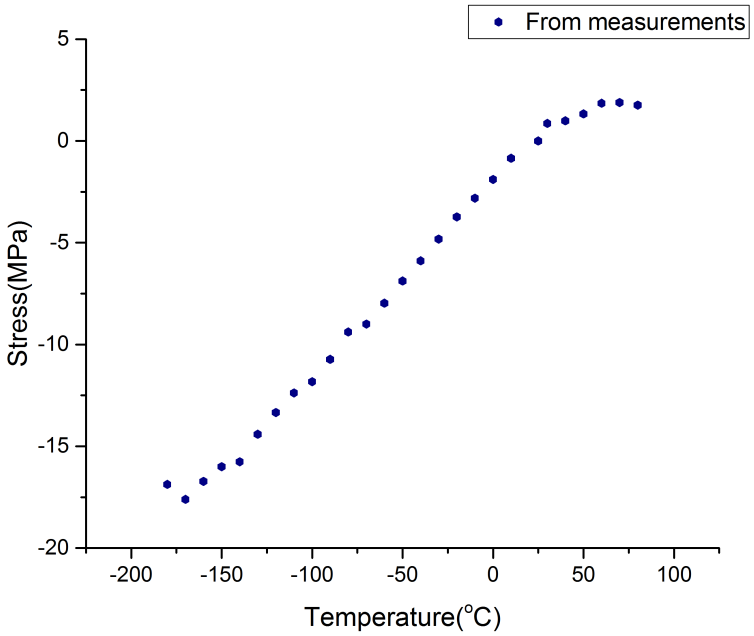


Figure 5.11: Shear stress variation for sensor cell #1.

Even though there was a similar trend in the shear stress variation in the case of simulation and measurements, there was a discrepancy in the stress component values. This might be due to the non-availability of material properties at all the temperatures for the simulation. With improved modeling, the discrepancy can be reduced. Both the cases showed a similar change in sign for the stress of inner sensors compared to the outer sensors. The shear stress in the package increased with decrease in temperature. The stress curve was linear for most part of the temperature cycle and it got flattened out at high temperatures. This might be due to the softening of the die attachment layer. Thus, from the stress variation plot shown in Fig.(5.11), it was clear that the shear stress in the package was dependent on the temperature.

Chapter 6

CONCLUSION

The piezoresistive coefficients for p material were extracted using the PMOS sensor cell. A number of samples were used for obtaining the coefficients. All the samples showed a similar trend of coefficient variation with respect to the temperature. The inconsistency in the coefficient values, which have been reported earlier [12], can be attributed to a number of factors such as basic measurement uncertainty or to the fact of transistors not being biased far enough into strong inversion to saturate the coefficient values. Some other factors can be quantization within the quasi two dimensional channel charge sheet. Thermally induced shear stress components were extracted using the NMOS sensor cells. The dependency of shear stress in packages on temperature was clear from the results obtained. A discrepancy was found between the stress values obtained from measurements and simulations, which could be attributed to the non-availability of material properties at all temperatures and to the unknown history of the processes/conditions in the past, to which the samples were subjected to.

There were issues with the working of counters at low temperatures that prevented reliable measurements from the pmos and nmos sensor arrays. This might be due to the increase in threshold voltages with decrease in temperature for the cascaded mosfets used in pass transistor logic for building the counter. Attempts were made with increased supply voltage upto 9V. But there was no improvement. More accurate and reliable results could be obtained with improved design. A better picture of the thermally induced stress over the whole die area could be obtained with a counter design that is reliable at low temperatures.

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