Advanced RC Phase Delay Capacitive Sensor Interface Circuits for MEMS

by

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Abstract

Many types of sensors in MEMS technology convert a measurand to a proportional change in capacitance. One of the techniques of measuring capacitance is utilizing the phase delay of an RC network with a resistor and the sensor capacitor. Specifically, the state of an input square wave signal is delayed by the RC network and gives a pulse width modulated signal according to the phase delay at the output, which is proportional to the capacitance, if the resistance is fixed. However, the response of this method becomes severely nonlinear if the phase delay is bigger than approximately $45°$. Two improved implementations are presented to avoid the nonlinearity caused by the capacitor being not fully charged and discharged each cycle. The first one uses a PMOSFET switch to charge the unknown capacitor and an NMOSFET to discharge it during each measurement cycle. The second one uses an analog switch to switch the resistance to be significantly lower when the capacitor needs to be fully charged or discharged in each cycle. Both methods were simulated and proved effective. Prototype circuits were also implemented and tested with an $8-128\text{pF}$ variable capacitor, and linear responses were measured. These techniques produced a linear response over different and large capacitance ranges, and can possess fast response times.

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1. INTRODUCTION

There are lot of sensors in Microelectromechanical Systems (MEMS) technology that convert different kinds of measurand to proportional changes in capacitance, with the help of certain interface circuits. In such sensors, the capacitance of the sensing capacitors varies due to the changes of measurands, such as from the spatial distance or overlapping area of the electrodes, the permittivity of the dielectric material between the electrodes, etc. In this thesis, the focus is the design of interface electronics, and a multi-plate angular displacement capacitor is used, in which the variation of overlapping area of the electrodes is simulated.

There are also plenty of electronic techniques to interface and measure the capacitance of the capacitive sensors. One of these techniques is utilizing the phase delay of an RC network with a fixed resistor and a changing capacitor which is the sensing part. Specifically, the state of an input square wave signal is fed into the circuit and delayed by the RC network and gives a pulse width modulated (PWM) signal according to the phase delay at the output, which is proportional to the capacitance, as the resistance is set. When the phase delay becomes bigger than approximately $45°$, however, the response becomes seriously nonlinear, which limits the performance of the capacitive sensor.

To solve this problem, two improved implementations are presented to avoid the nonlinearity caused by the capacitor being not fully charged and discharged each cycle. The first one uses a PMOSFET switch to charge the unknown capacitor and an NMOSFET to discharge it during each measurement cycle. The original idea for the second one was to replace the resistor with a digital potentiometer to switch the resistance to be significantly lower when the capacitor needs to be charged or discharged in each cycle. In the experiment, however, a commercial digital potentiometer with a response frequency high enough for small capacitance measurement could not be found. Therefore, keeping the same idea of lowering resistance in charging and discharging periods, the design is changed to its equivalent circuit with an analog switch to switch between two resistance levels. Both methods were simulated and proved effective. Prototype circuits were also implemented and tested with a small variable capacitor with the range of $8-128\text{pF}$, and linear responses were tested. The output PWM is then filtered by a low pass filter to be converted to a DC current which makes it easy to read and process.

2. LITERATURE REVIEW FOR CAPACITIVE SENSORS AND THEIR INTERFACE CIRCUITS

2.1 Capacitive sensors

2.1.1 Overview

Capacitive sensors are useful in a lot of different sensing and measuring problems. They are found a big variety in applications, such as gyroscopes [1], accelerometers [2], pressure sensing [3], humidity sensing [4], flow sensing [5], light switches [6], and proximity detection [7], etc. They can be small as size as integrated into a PCB [8] or, in MEMS technology, a microchip [9]. A good example is a smart phone which usually contains a gyroscope, an accelerometer, a capacitive touchscreen [10], and even the microphone uses capacitive sensing.

Capacitive sensors have the following advantages [11]:

- Large range of measurement. The ratio of effective variety $\Delta C/C$ can be as big as 100%.
- High sensitivity. The amount of relative change can be as small as 10^{-7}. Some paper reached a high sensitivity of 0.61fF/nm [12].
- Short time of dynamic response. The mass of motion part is small and the

eigenfrequency is high.

- Simple structure, good adaptability. Since the materials for electrodes are metal and the dielectric materials between the electrodes are inorganic, such as air, glass, quartz etc., capacitive sensors adapt well in environments like high/low temperature, strange magnetic or radiation.

2.1.2 A Capacitor

A capacitor is an electric component that is composed of two conductive electrodes separated by an insulator, which can be a nonconductive substance calls dielectric, such as air, oil, fuel, mica etc., or vacuum [13]. Charge or electrical energy is stored on the electrodes which are usually parallel conducting plates. For such a capacitor, the capacitance is used to describe the relationship between the charge and the difference in voltage between the plates:

$$C = \frac{Q}{V} \tag{2.1}$$

where,

C is the capacitance in Farads (F),

Q is the magnitude of charge on each plate in Coulombs (C),

V is the voltage applied across the plates in Volts (V).

The capacitance is determined not only by the geometrical design of the electrodes, which can be parallel plates, disks, spheres, cylinders, or concentric cylinders, cylinders and planes, strips and planes etc.,[14] but also by the dielectric material between them. For

instance, the capacitance of a capacitor made of n equally parallel plates can be calculated using the following equation:

$$C \approx \frac{\varepsilon_0 \varepsilon_r S(n-1)}{d} \tag{2.2}$$

where,

C is the capacitance in Farads (F),

ε_0 is the dielectric constant for vacuum, which is 8.854×10^{-12} pF/m,

ε_r is the relative dielectric constant, which is 1 for a vacuum,

S is the overlapping area in square meters (m^2),

n is the number of parallel plates,

d is the distance between them in meters (m).

Note that Equation 2.2 ignores fringing effects.

According to Equation 2.2, the capacitance changes when any phenomenon causes a variation of S, d, or ε_r. Capacitive sensors are such devices that are based on this relationship and considered to sense the change of one or more of those parameters, either in the geometry or in the dielectric material. For instance, a capacitor with increased surface area for the conducting plates are able to store more charge and thus has an increased capacitance value.

When a voltage is applied across the two electrodes of the capacitor, the plates start to charge and store electrical energy, until the voltage across the capacitor matches with the source. Positive charges are stored on the plate connected to the positive terminal of the source and negative charges are stored on the one connected to the negative terminal. The

charged capacitor can hold the charge if the source is disconnected until other components consume it or leakage happens because no dielectric is a perfect nsulator. The charge accumulation process when a voltage is applied is illustrated in Figure 2.1. [15]

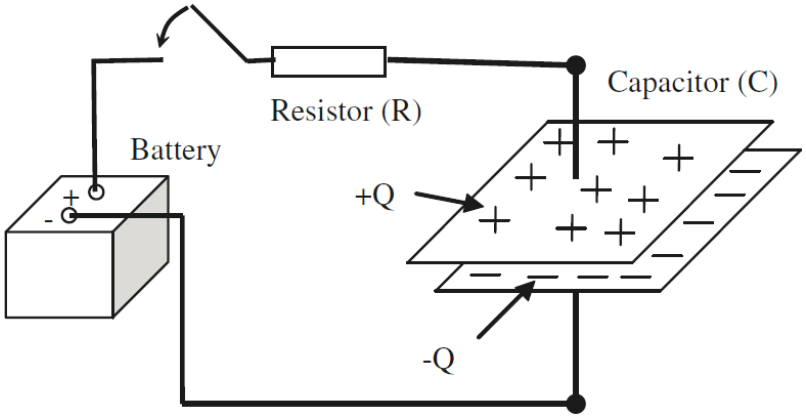

Figure 2.1 A capacitor used in a circuit begins to store charge when switch closes.

The time required to charge a capacitor fully is determined by a time constant of τ_0 defined as in Equation 2.3, where R is the resistor connected in series with the capacitor C. τ_0 describes the time for the capacitor to be charged to 63% of its total capacitance.[15] The value of τ_0 is measured in seconds.

$$\tau_0 = RC \tag{2.3}$$

2.1.3 Spacing Variation

Spacing variation is widely used in motion detecting capacitive sensors whose capacitance depends on the spacing of the plates. A 10% spacing change leads to about a 10% change in capacitance [16], thus this kind of capacitive sensor is very sensitive when the separation distance between the plates is much smaller than the dimension of the

overlapping area of the electrodes.

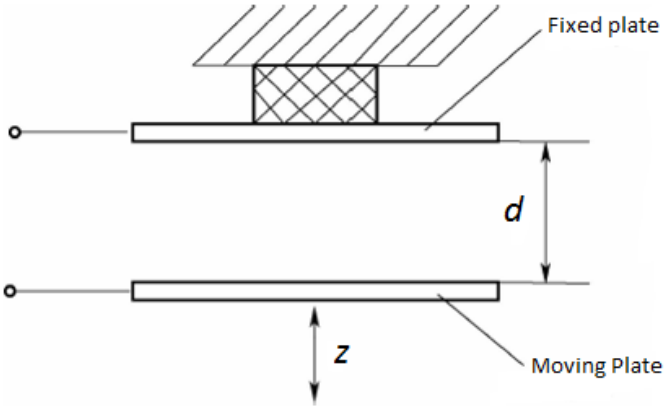

Figure 2.2 A spacing varying capacitor.

Figure 2.2 shows an example of a spacing varying capacitor, in which one of the two plates is fixed and the other moves along the direction vertical to the parallel plates. With the area of plates S and the dielectric material unchanged, the capacitance varies only along with the variation of the spatial distance d. In Figure 2.2, the moving plate is connected to the sensing object. When we want to measure the capacitor directly, as we can see in Equation 2.2, the nonlinear relationship between capacitance C and spacing d appears to be a problem. This can be solved by measuring the impedance of the capacitor instead of the capacitance, since $Z_C = 1/j\omega C$ (Figure 2.3 [16]).

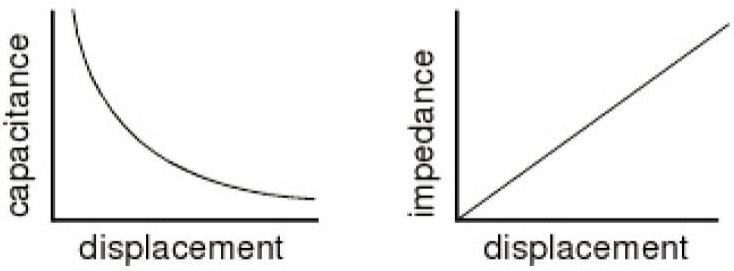

Figure 2.3 Illustration of spacing variation of plates.

Yet in the measurement of a very small displacement, the relationship between capacitance and displacement can be considered as linear. Assuming the initial distance is d_0, thus the initial capacitance is $C_0 = \varepsilon S/d_0$. When the moving plate has a displacement of Δz along Z-axis, the capacitance becomes

$$C_x = \frac{\varepsilon S}{d_0 - \Delta z} = \frac{\varepsilon S/d_0}{1 - \frac{\Delta z}{d_0}} = C_0 \frac{1 + \frac{\Delta z}{d_0}}{1 - \frac{\Delta z^2}{{d_0}^2}} \tag{2.4}$$

When $\Delta z \ll d_0$ (usually, $\Delta z/d_0 = 0.02 \sim 0.1$ in engineering for small displacement measurement), Equation (2.4) yields to

$$C_x \approx C_0 \left(1 + \frac{\Delta z}{d_0}\right) \tag{2.5}$$

which gives an approximate linear relationship between capacitance and displacement.

For such a geometry of two parallel plates with the same sizes, there is an undesired sensitivity.

2.1.4 Area Variation

Transverse motion of one or two of the plates causes area variation and results in changed capacitance. Different from spacing varying capacitive sensors, this kind of variation offers a linearly related capacitance and variation of area and a long range of motion measurement.

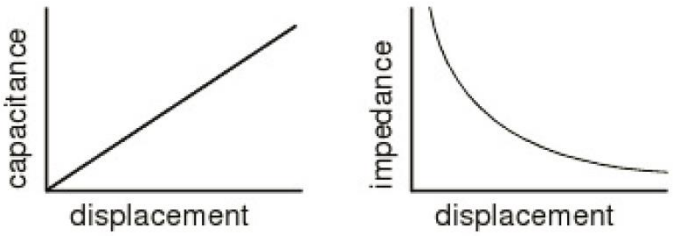

Figure 2.4 Illustration of area variation of plates.

There are usually two types of area varying capacitor: line displacement and angular displacement. Figure 2.5 depicts a typical area varying capacitor with line displacement. One of the two plates is fixed and the other moves along the direction parallel to the plates. The distance between the parallel plates d is fixed and so is the dielectric material. The overlapping area S varies linearly with the transverse displacement Δx, since the other side b does not change. According to Equation (2.2), the capacitance thus varies linearly along with the displacement Δx, as it is concluded in Figure 2.4 [16].

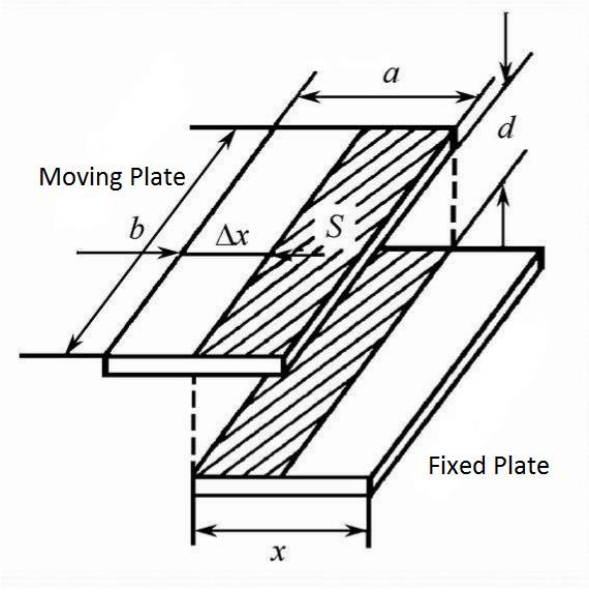

Figure 2.5 An area varying capacitor with line displacement.

The other type of area varying capacitor is with angular displacement. Figure 2.6

shows such pie-shaped sectors of capacitor plates. When the moving plate 1 has an angular displacement of θ, the overlapping area experience a change which causes a change of capacitance. The relationship is expressed as below:

$$C = \frac{\varepsilon_0 \varepsilon_r S}{d}\left(\frac{\pi - \theta}{\pi}\right) = C_0 - C_0\frac{\theta}{\pi} \tag{2.6}$$

where C_0 is the initial capacitance before the displacement occurs.

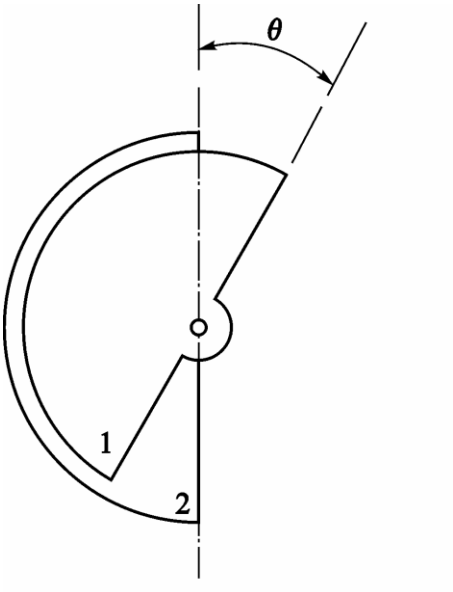

Figure 2.6 An area varying capacitor with angular displacement.

Figure 2.7 gives more examples of area varying capacitive sensors.

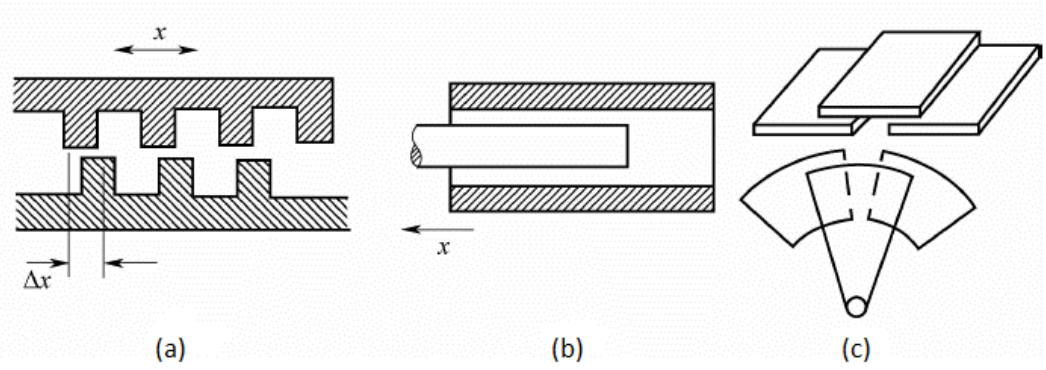

Figure 2.7 (a) Tooth profile plates; (b) Concentric cylinders; (c) Differential area variation capacitors.

As a comparison, for a spacing varying capacitive sensor, since the increase of the

displacement not only leads to nonlinearity, but it also causes vanishing signal level thus lowering sensing accuracy. Considering about this limited range of displacement, whose maximum is just a small fraction of the diameter of the plates, area variation is preferred. And in this thesis, the capacitor used in later application is a multi-plate area varying capacitor with angular displacement.

2.1.5 Dielectric Material Variation

Capacitive sensors can not only sense the motion of electrodes directly, they are also able to sense the dielectric property between the electrodes or, in many applications, the motion of the dielectric material between the electrodes.

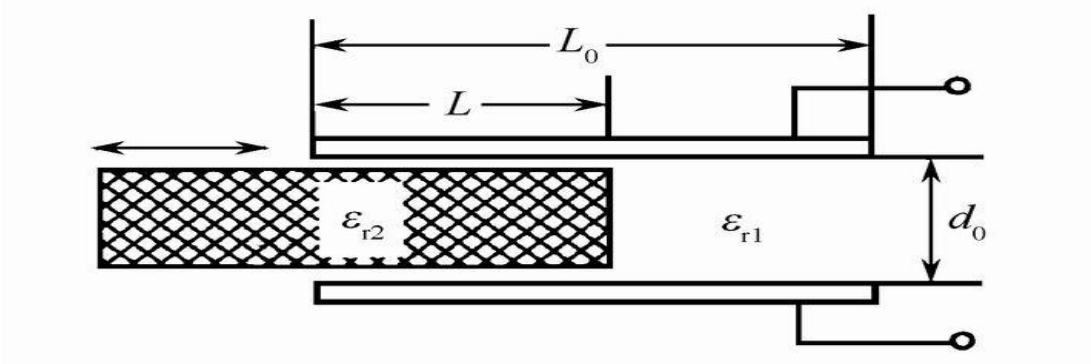

Figure 2.8 A dielectric material varying capacitive sensor.

In Figure 2.8, we have a capacitor with two fixed electrode plates. The relative dielectric constant ε_{r1} of the gas between the plates is different from the relative dielectric constant ε_{r2} of the object moving parallel to the plates. Dividing the capacitor into two parts: the one without the dielectric object and the one with it, the capacitance of these two parts C_1 and C_2 are different according to Equation (2.2). Assuming the spatial distance and the dimension of the plates are constant, and the dimension of the dielectric object is

b_0, we have

$$C = C_1 + C_2 = \varepsilon_0 b_0 \frac{\varepsilon_{r1}(L_0 - L) + \varepsilon_{r2} L}{d_0} \tag{2.7}$$

When $L = 0$, the initial capacitance is $C_0 = \frac{\varepsilon_0 \varepsilon_{r1} L_0 b_0}{d_0}$. Therefore, when the dielectric object moves into the plates the depth of L, the relative variation of the capacitance is

$$\frac{\Delta C}{C_0} = \frac{C - C_0}{C_0} = \frac{(\varepsilon_{r2} - \varepsilon_{r1})L}{\varepsilon_{r1} L_0} \tag{2.8}$$

which is constant, i.e. the relationship of capacitance variation and dielectric displacement is linear.

The case analyzed above is based on an ideal geometric profile of the dielectric object. If the object is not perfectly flat, such sensors can be used to measure the thickness variation of the object (Figure 2.9 (a)). Since the capacitance varies as long as there is a change in the overall dielectric properties of a local material, this kind of sensor has more applications such as measurement of liquid level (Figure 2.9 (c)), temperature or moisture (Figure 2.9 (d)) etc.

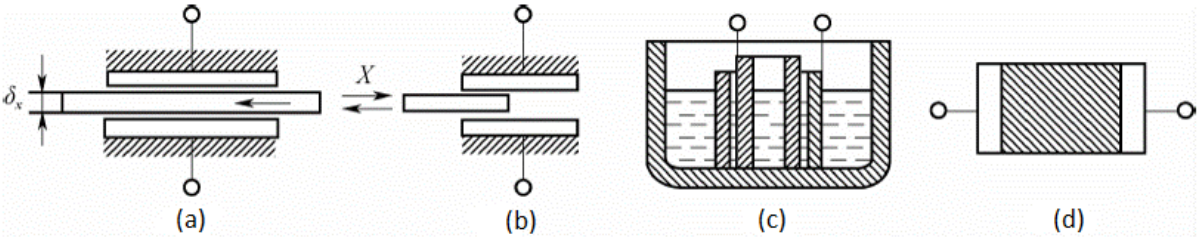

Figure 2.9 Typical application of dielectric material varying capacitive sensors:
(a) Measurement of thickness; (b) Measurement of displacement;
(c) Measurement of liquid level; (d) Measurement of temperature/moisture.

2.1.6 Capacitive Fringing Field Sensors

As mentioned before, Equation 2.2, on which all of the three kinds of capacitive

sensors are based, ignores fringing effects. Another kind of capacitive sensor can also be realized, however, if a measurand can interact with the fringing field of the electrodes. Figure 2.10 shows one of such sensors in MEMS and printed circuit board (PCB) technology [16]. In this design, there are n parallel electrodes of area a with a fixed separation distance of d. These finger or comb like digits are in a dielectric material of a relative permittivity of ε_r. Note that every other electrode is connected electrically.

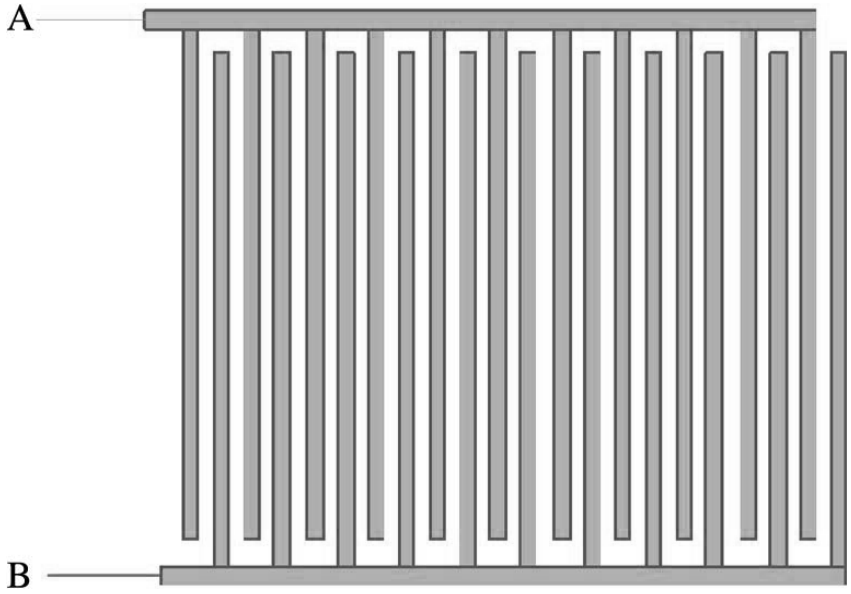

Figure 2.10 Two interdigitated capacitor electrodes.

When the magnitude of the overlapping area of the electrodes is much bigger than the distance between the electrodes, fringing effects can be negligible to some degree. In this design, however, since the perimeter around the electrodes is much bigger than the perimeter around the overlapping area, the fringing effects become greater and cannot be neglected (Figure 2.11). The equation for the capacitance is [16]:

$$C \approx \frac{(n-1)\varepsilon_0\varepsilon_r a\gamma}{d} \tag{2.9}$$

where γ is the fringing scale factor.

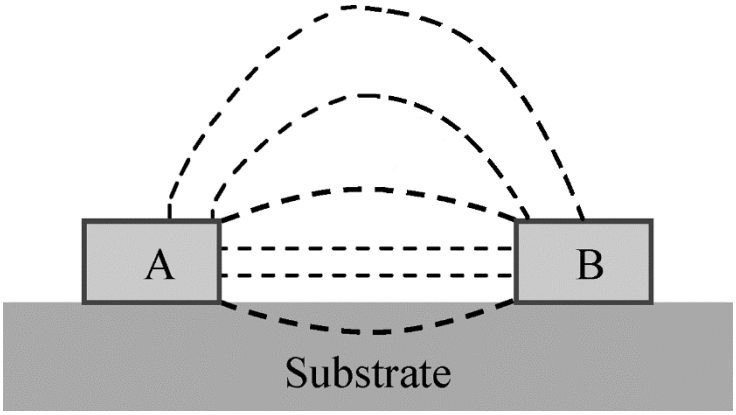

Figure 2.11 A representative drawing of the fringing fields of two neighboring electrodes.

Since the fringing field is projected to the sensing material without changing the configuration of electrodes, this type of capacitive fringing fields sensor has the advantage of allowing the capacitor electrodes to be isolated from the sensing environment physically. Capacitive fringing sensors find the wide applications in sensing moisture [16], capacitive touch switches [17], proximity sensors [18], biomedical sensors [19], etc.

More sensing configurations and applications can be realized with flexible printed circuit board (FPCB) technology, which is also mature and commercially available, instead of fixed fringing field sensors mentioned above [20]. FPCB is similar to rigid PCB technology and the main difference between them is that the substrate of FPCB is a thin and flexible material. This enables capacitive fringing field sensors to adapt into more environments of application such as the sensors or sensor array that can be directly and conformally mounted onto nonplanar surfaces such as a PVC pipe [20].

2.2 Interface circuits for capacitive sensors

The capacitive sensing parts mentioned above are able to convert measurand variables

to capacitance through the change of the electrodes' spatial distance, overlapping area or the dielectric property of the material between, while interface circuits convert the changing capacitance to output signals. As capacitance is usually measured indirectly and there are many techniques designed to interface to the capacitive sensors.

2.2.1 Direct DC Circuits

The simplest technique is called direct DC circuit [21]. As we can see in Figure 2.11, a DC voltage is applied on a simple RC network and, simply by charging the sensor capacitor C_s and connecting it to a very high impedance amplifier, the change in the capacitance can be measured as the difference in the DC voltage. From Equation 2.1 we have the relationship of $Q = CV$. Thus when the charge is nearly constant, the voltage across C_s varies as the reciprocal of the capacitance. To avoid low frequency losses, the time constant of $\tau = R_0 C_s$ given in Equation 2.3 where, in this case, R_0 is the input resistance of the amplifier must be bigger than the period of measurement. When C_s varies at a frequency bigger than $1/\tau$, we have the output

$$E_o = \frac{Q}{C_s} = \frac{C_0 V}{C_s} \tag{2.10}$$

where Q is the charge on the sensor capacitor C_s and C_0 is the capacitance of C_s when there is no displacement.

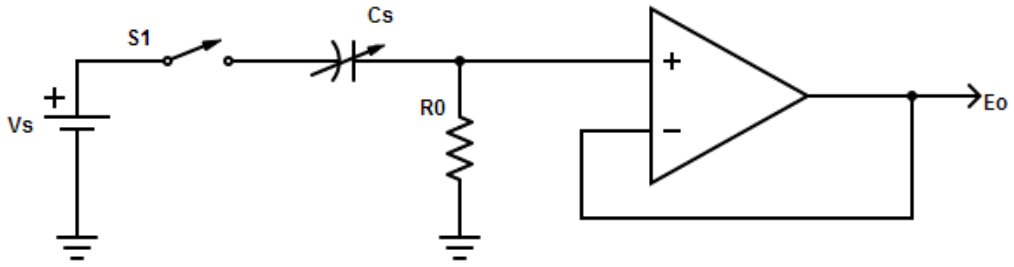

Figure 2.12 Direct DC capacitance circuit.

This circuit is simple in structure and small in size, but it may be easily affected by stray capacitance and leakage, and it is sensitive to noise from the shunt resistor. Thus it is not suitable for capacitive sensors with very small electrodes. The nonlinearity of the response limits its application as well.

2.2.2 Bridge Circuits

Figure 2.13 shows a standard Wheatstone bridge circuit [22]. This kind of circuit is used to measure the unknown resistance R_4 by balancing the two legs of the bridge. When the bridge is balanced, i.e. $R_1/R_2 = R_3/R_4$, and the output V_o equals zero. If the unknown resistance R_4 varies, even with a small disturbance, the balance is disrupted and there is a voltage at the output. The large amplifier gain is used to amplify the small differences in the legs. This bridge circuit has the advantage that two identical pairs of resistors can be used in both legs so that thermal drifts will not affect the balance.

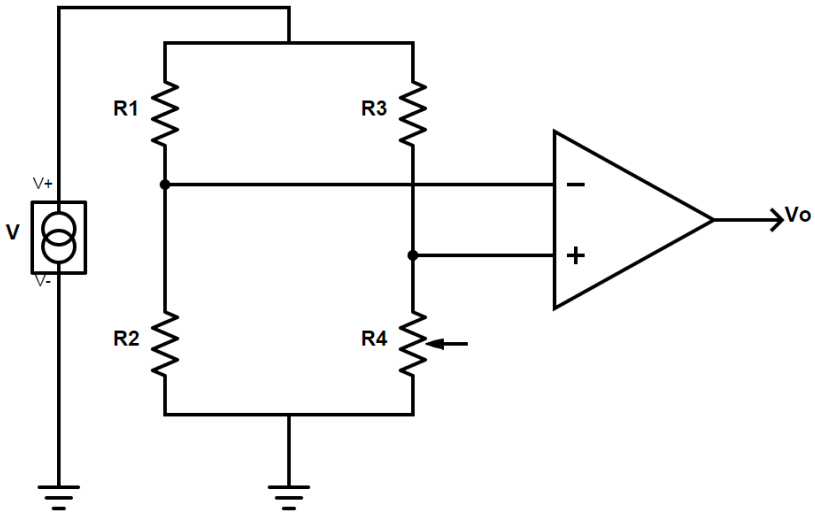

Figure 2.13 Resistor bridge.

This idea can be applied in several kinds of capacitor bridge circuits. A typical one shown in Figure 2.13 has capacitors replacing the resistors, and a balanced drive instead of the differential amplifier [21]. For this circuit, we have the following equation:

$$V_o = -V\frac{C_1 - C_2}{C_f} \tag{2.11}$$

For this equation to be accurate, the gain of the amplifier should be large. The stray capacitance at the input of the amplifier should be minimized because, even though it does not affect V_o, it cuts down the amplifier's available gain when the frequency is high. Also, C_1 and C_2 should be identical in construction so that the bridge's balance can be stable.

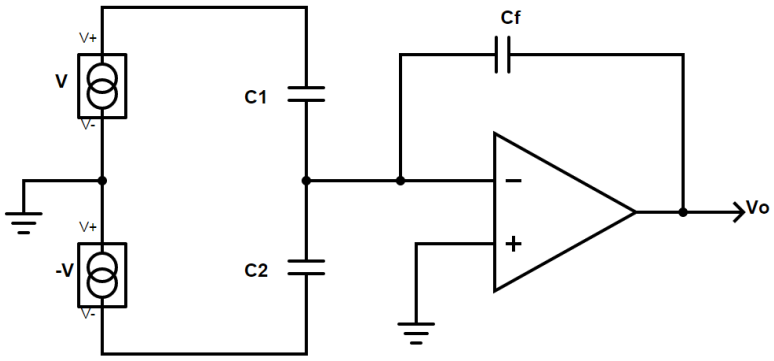

Figure 2.14 Capacitor bridge.

This kind of capacitor bridge is generally preferred because it is essential for sensitive circuits amplifying small varieties of the sensor capacitance and it is much easier to make a ratio of similar components to be stable than that of different components. For circuits which have low amplifier gain and large linear range, this kind of bridge can be designed to not be sensitive to many parameters of the circuit. [23]

2.2.3 Oscillator Circuits

As we mentioned previously, the direct DC circuit is not able to deal with very slow variations of the capacitance without an amplifier with a very high input impedance. Other disturbances like thermocouple voltages, slow variation of parameters, cable noise, power frequency crosstalk, etc. are admitted as well. Circuits with high frequency excitation are thus preferred. For instance, if we use the sensor capacitor as the tuning element in an oscillator, the unknown capacitance can be calculated by measuring the change of oscillation as the result of capacitance variation.

Such a design is often based on a relaxation oscillator [24], no matter whether the sensed capacitance forms a portion of an RC circuit or a LC one. For an RC oscillator, the frequency is proportional to $1/RC$, while it is proportional to $1/\sqrt{LC}$ with a LC oscillator which is more difficult to linearize. The technique works basically by charging the unknown sensor capacitance with a known current. Taking an RC oscillator as an example, the capacitance can be calculated by measuring the charging time needed to reach the threshold voltage of the relaxation oscillator, or the frequency of the oscillator which is

also proportional to the time constant τ_0 as in Equation 2.3. [25]

A typical and simple RC oscillator used in capacitive sensing is a CMOS ring oscillator circuit which can produce square waves and greatly reduced sideband noise [26-27]. A ring oscillator is a closed loop circuit with odd number of identical inverters or NOT gates connected head to tail in a chain. Figure 2.14 illustrates a 3-inverter ring oscillator with an RC network. As the output of the last inverter feeds back to the input of the first one, according to the logic function of inverters and the odd number, it is easy to see that the stage of each node of the circuit is very unstable and a small disturbance above a certain threshold voltage will drive an oscillation. Taking the case of Figure 2.14 as an example, assuming C_s is much bigger than the capacitance of the inverter, each inverter is fast and the trip voltage is half of the driven voltage V_{dd}, the system changes states when $V_0 = V_{dd}/2$, thus the output frequency f_o is modulated by the time constant of the external RC network. f_o can be derived to yield

$$f_o \approx \frac{0.455}{RC_s} \tag{2.12}$$

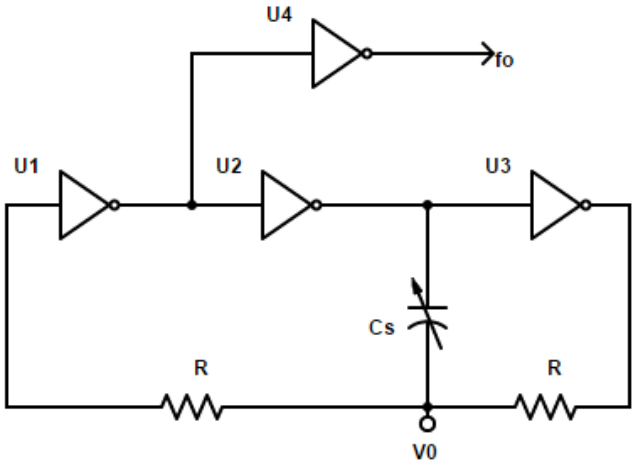

Figure 2.15 A 3-stage ring oscillator consisting identical inverters and a RC network.

As we can see from Equation (2.12), the relationship between output frequency and input capacitance is inverse. To interface the output frequency converted from capacitance by this relaxation oscillator, frequency-locked loops (FLL) can be used [28]. The logic level square wave of the oscillator's output is fed into an all-digital FLL which frequency locks to the input signal and produces a digital output of N. This word N is inversely proportional to f_o, thus linearly proportional to the sensor capacitance C_s, which greatly simplifies the capacitance measurement.

2.2.4 Other Interface Circuit Techniques

There are many other interface circuit techniques developed for capacitive sensing, such as charge amplifier [29], AC voltage division [30], transimpedance amplifier circuits [31], relative phase delay using the delay from the capacitive sensor through a RC stage [32] and its improvement with a wider linear range [33], etc.

Since the relative phase delay resulting from the time constant of an RC network plays a key role in the advanced full linear range phase delay interface circuit designs of this thesis, more theoretical details and discussions will be given in the next chapter.

3. THEORY BASIS AND DISCUSSION

As summarized in the last chapter, one of the interface circuit techniques for capacitive sensing is relative phase delay using the delay from the capacitive sensor through an RC stage. This technique has a great advantage of being immune to the surrounding noise because it only detects the shifts in phase [34].

3.1 Analysis of RC circuit phase delay

Figure 3.1 is a schematic diagram of an RC network circuit which is usually used as a one pole low pass filter. Its transfer function [32] is

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{1/_{sC}}{R + 1/_{sC}} = \frac{1/_{RC}}{s + 1/_{RC}} \tag{3.1}$$

where,

$V_{in}(s)$ is the Laplace transform of the input voltage,

$V_{out}(s)$ is the Laplace transform of the output voltage,

s is the Laplace transform complex frequency variable,

R is the resistance,

C is the capacitance.

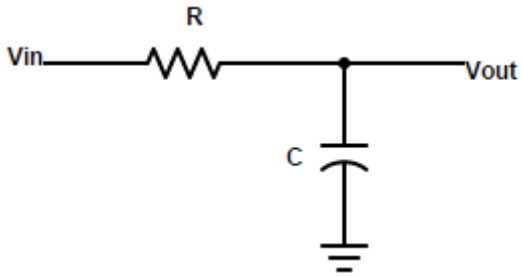

Figure 3.1 A simple RC network circuit.

From Equation (3.1), we can derive

$$V_{out}(s) = \frac{V_{in}}{s}\left(\frac{1/RC}{s + 1/RC}\right) = \frac{V_{in}}{s} - \frac{V_{in}}{s + 1/RC} \tag{3.2}$$

Thus

$$V_{out}(t) = V_{in}(t)\left(1 - e^{-t/\tau}\right) \tag{3.3}$$

where,

$V_{in}(t)$ is the input voltage,

$V_{out}(t)$ is the output voltage,

t is time,

τ is the time constant defined in Equation (2.3) that $\tau = RC$.

Assuming the capacitor is initially discharged, when the output voltage $V_{out}(t)$ reaches half of the input voltage of $V_{in}(t)$, Equation (3.3) can yield to

$$t_{0.5} = -\tau \ln\left(\frac{1}{2}\right) = 0.693\tau = 0.693RC \tag{3.4}$$

where,

$t_{0.5}$ is the time for $V_{out}(t)$ to reach half of $V_{in}(t)$,

τ is the time constant,

R is the resistance,

C is the capacitance.

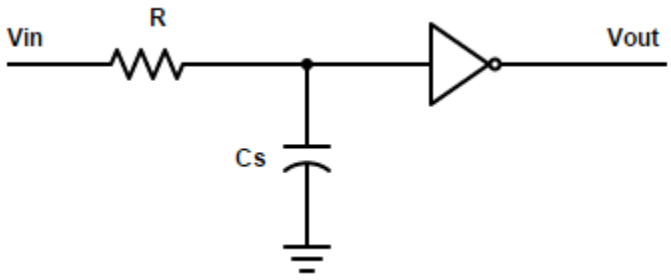

Figure 3.2 A RC network circuit attached to a CMOS inverter.

We can see from Equation (3.4) that $t_{0.5}$ is proportional to C if the value of R is fixed. Consider about the circuit shown in Figure 3.2 where C is replaced with a capacitive sensor of C_s and the former output pin is attached to the input of a Complementary Metal-Oxide-Semiconductor (CMOS) inverter (or NOT logic gate). Ideally, the inverter's trip voltage (the input voltage needed to trigger a change in output state) approximately equals to one half of its driven voltage V_{dd}. When additional protecting circuits are neglected, a CMOS inverter can be depicted in Figure 3.3 where the input A is connected to the gates of a p-channel MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) and an n-channel MOSFET, thus the input resistance of the inverter is much larger than R. Since the typical input capacitance is in pF (21pF for the 74HC04 invertor) which is comparable to the typical capacitance in small capacitance sensing application, C is now the summation of two parallel capacitances C_s and C_g:

$$C = C_s + C_g \tag{3.5}$$

where,

C is the total capacitance,

C_s is the sensor capacitance to be measured,

C_g is the gate capacitance of the MOSFETs in the inverter.

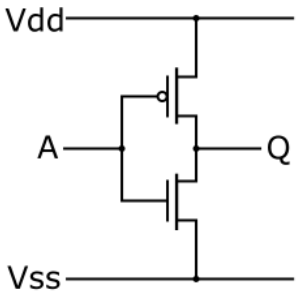

Figure 3.3 A CMOS inverter.

If the input voltage $V_{in}(t)$ is a step function from 0 to V_{dd}, $t_{0.5}$ in Equation (3.4) is the time delay that the inverter in Figure 3.2 experiences to switch states compared with the same inverter but without the RC network circuit between its input and $V_{in}(t)$. Notice that, in practice, $V_{out}(t)$ may not be perfectly square compared with the case without the RC network, yet adding one or more inverter stages can solve it if this problem is significant.

To detect the delay caused by the RC network electronically, we can use a circuit shown in Figure 3.4. In this circuit, the input voltage V_{in} is divided into two parallel legs, both of which contain the same number of inverter stages. In Figure 3.4, each leg contains two inverters, which will make the logic state of both output voltages, V_{o1} and V_{o2}, the same with V_{in} after inputting from 0 to V_{dd}. The difference is that there is an RC network between inverter U1 and U2, because of which V_{o1} will experience a delay τ_d, equal to $t_{0.5}$, relative to the state change in V_{o2}. This relative delay of τ_d is proportional to the total capacitance C. Therefore a change in value of the capacitance C can be converted

to the change of τ_d thus a measurement of C can be realized.

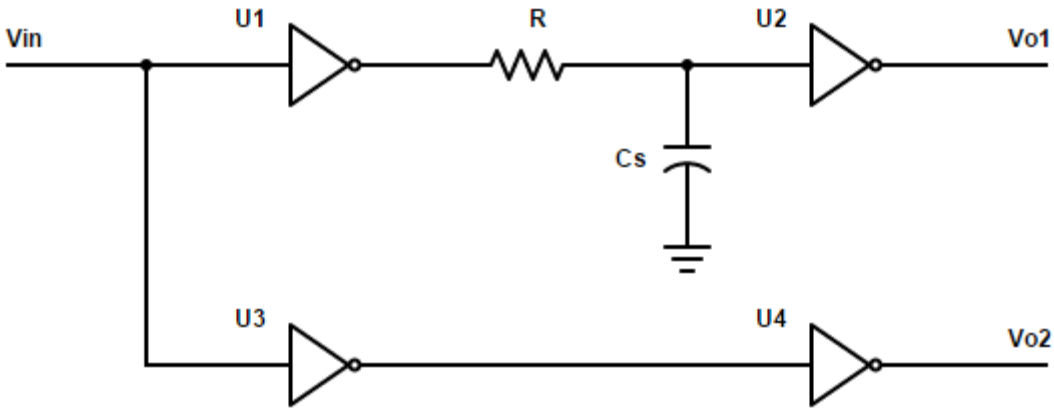

Figure 3.4 A conventional phase delay circuit with RC network.

However, in most sensor applications, single time of measurement is not practical. In order to have a continuous dynamic sensing of the capacitance and make it easier to do further processing, we apply a square wave signal in the input, instead of a step function, with frequency of f, period of T, duty cycle of 50%, high voltage value of V_{dd} and low value of 0. If $T \gg \tau_d$, C can be fully charged to V_{dd} or fully discharged to 0V before the inverter U1 changes logic state in each cycle. Thus $t_{0.5}$ in Equation (3.4) is still able to describe the relative delay between the output voltages V_{o1} and V_{o2}, and their difference in phase is proportional to C linearly.

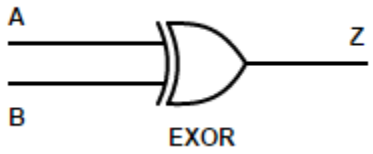

Figure 3.5 An Exclusive OR Gate.

An Exclusive OR (EXOR, Figure 3.5) logic gate [35] can be used to detect and measure the relative phase difference between V_{o1} and V_{o2} as both output values are the output of identical inverters and thus consist of logical "0's" and "1's". An EXOR gate,

whose truth table is shown in Table 3.1, produces a high output or state "1" at Z if only one of the inputs A and B is a high or "1" state. If the two inputs are at the same logic state, both high/1 or both low/0, the output of the EXOR gate is a low or "0" state. In other words, in this application, when the phase difference between V_{o1} and V_{o2} is $180°$, the output is high/1, while when the phase difference is $0°$, the output is low/0.

Table 3.1 Truth table of an EXOR gate

Input		Output
A	B	Z
0	0	0
0	1	1
1	0	1
1	1	0

When two identical trains of square waves of 50% duty cycle at the same frequency are input to the EXOR gate with a certain relative phase difference bigger than $0°$ and smaller than $180°$, the output of the EXOR gate is a Pulse Width Modulated (PWM) signal at a frequency twice that of the input square wave signal, whose duty cycle is linearly proportional to the relative phase difference at the inputs. If the relative phase difference increases from $180°$ to $360°$, the duty cycle of the output PWM signal decreases linearly from 100% back to 0%. Thus the EXOR gate can only be used within a range of $180°$ phase difference, either from $0°$ to $180°$ or from $180°$ to $360°$. In addition, because of phase jitter, the EXOR gate works better if the range of phase difference avoids being too

close to $0°$ or $180°$ or $360°$.

As we mentioned before, the condition for the relative phase difference to be linearly proportional to C is that $T \gg \tau_d$, under which C can be nearly charged to V_{dd} or nearly discharged to 0V before the inverter U1 changes logic state in each cycle. The phase difference, however, would be extremely small due to this limited condition. According to the former research in [32], if the permissible nonlinearity is limited to 2.6%, the usable range of phase delay resulting from the RC network circuit is from $0°$ to $45°$, which is a small portion of the potential maximum range of $180°$ that is available from the EXOR gate detector. This thesis is thus interested in making use of the "wasted" approximately $3/4$ of the potential range to expand the linearity of capacitance sensing.

3.2 Converting PWM to DC Voltage

Since it is easier to measure a DC voltage than the pulse width of a PWM signal, the output PWM signal from the EXOR gate can be simply filtered by a passive low pass filter and converted to a DC output whose voltage level is proportional to the duty cycle of the PWM signal thus proportional to the sensed capacitance. Specifically, the low pass filter works like applying a fast Fourier transform and attenuate the AC components which has a fundamental frequency twice that of the input square wave signal, but pass the DC component whose frequency is considered to be zero and value to be proportional to the PWM duty cycle.

Passive low pass filters can be realized very simply with resistors and capacitors,

which is exactly like the RC network in Figure 3.1. Yet adding more stages of this RC network head-to-tail in series with certain different resistance and capacitance values resulting in a certain order of the filter (1st order if it is single stage) can realize different cutting-off frequencies and ripples. The concept can be applied to more advanced filters in faster response, however, since we are only interested in the function of converting PWM to DC voltage, we will use a simple 1st order low pass filter with small ripples to do the job.

3.3 Resistance and gate capacitance of MOSFETs

As we saw in Equation (3.5), the gate capacitance of the CMOS inverter needs to be considered as well since it is parallel to the sensor capacitor and is also changed or discharged in each cycle, which influences the relative phase difference detected. Therefore, when new interface circuits are being designed to improve the linear range of measurement, the gate capacitance of MOSFETs should be carefully considered, and also the MOS resistance which could be a considerable addition to the resistance R.

3.3.1 Basis of MOSFETs

Firstly consider the structure of MOSFETs. Figure 3.6 depicts the structure of an n-channel MOSFET usually called an NMOS transistor or NMOSFET, and a p-channel MOSFET usually called a PMOS transistor or PMOSFET.

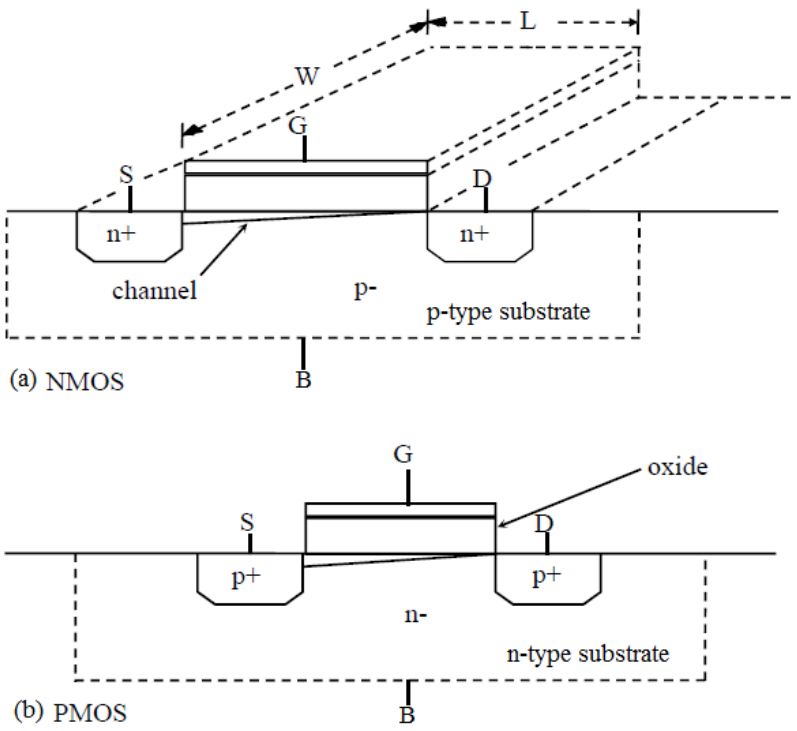

Figure 3.6 (a) NMOS transistor structure (planar view); (b) PMOS transistor structure (cross section).

Consider the NMOSFET as an example, the top electrode is called the gate (G) of the MOSFET, and the two heavily doped n-type (n^+) regions are called the source (S) and the drain (D). The source and drain are formed in the p-type substrate aligned with the edge of the gate. A thin layer of silicon dioxide is grown over the substrate material and a conductive gate material (usually metal or polycrystalline silicon) covers the oxide between the source and drain as a plate. Applying a positive voltage on the gate, as the voltage increases, electrons are attracted to the surface. At a particular voltage level called the threshold voltage, the electron density on the surface exceeds the hole density and the surface inverts from the original p-type polarity to an n-type inversion layer, directly under the gate plate electrode. The inversion layer is extremely shallow and exist as a charge sheet below the gate and between the source and drain. [36] Therefore, in operation,

the gate-source voltage (V_{GS}) modifies the conductivity of the layer under the gate, allowing the gate voltage to control the current flowing from drain to source. This control of the gate can be used to provide gain in analog circuits and switching function in digital circuits.

The reason for current flowing from drain to source in the NMOSFET is that the source is the source of electrons, which means the source operates at a lower voltage than the drain and the current flows in a direction opposite to the electrons in the channel. In the PMOSFET, however, the source is the source of holes, thus the source operates at a higher voltage than the drain and the current flows in a direction from source to drain. This also requires the voltage applied on the gate of a PMOSFET to be negative relative to the source for the transistor to be in the forward active mode.

3.3.2 Output Resistance of MOSFET Used as a Switch

There are various passive components that are available in MOSFET technologies. Resistors include diffused resistors, poly-silicon resistors, well resistors etc. The overall drain-source on-resistance of a power MOSFET (Figure 3.7 [37]), for example, is made up of the contribution of several components:

$$R_{DS_{on}} = R_{source} + R_{CH} + R_A + R_J + R_D + R_{SUB} \tag{3.6}$$

where,

R_{source} is the source diffusion resistance,

R_{CH} is channel resistance,

R_A is accumulation resistance,

R_J is the parasitic JFET component resistance of the region between two body regions,

R_D is drift region resistance,

R_{SUB} is substrate resistance.

Looking back at the Equation (3.4), the sensitivity of the phase delay to the capacitance would be higher if the value of the resistance R is dominant compared with the capacitance C. This observation inspires us to choose a reasonably high R for the RC network. As for the application in small capacitance measurement, the capacitance C is expected to be in pico Farads (pF). To realize a high frequency response of the system, several kilo Hertz (kHz) for instance, a reasonable resistance R should be in hundreds of kilo Ohms (kΩ) after trading off. As for typical drain-source on-resistance of a commercial MOSFET, it is several Ohms (FDC6320C by Fairchild for example [38]) or even less than 0.1 Ohm (Si4500BDY by Vishay Siliconix for example [39]), which can be neglected when compared with R.

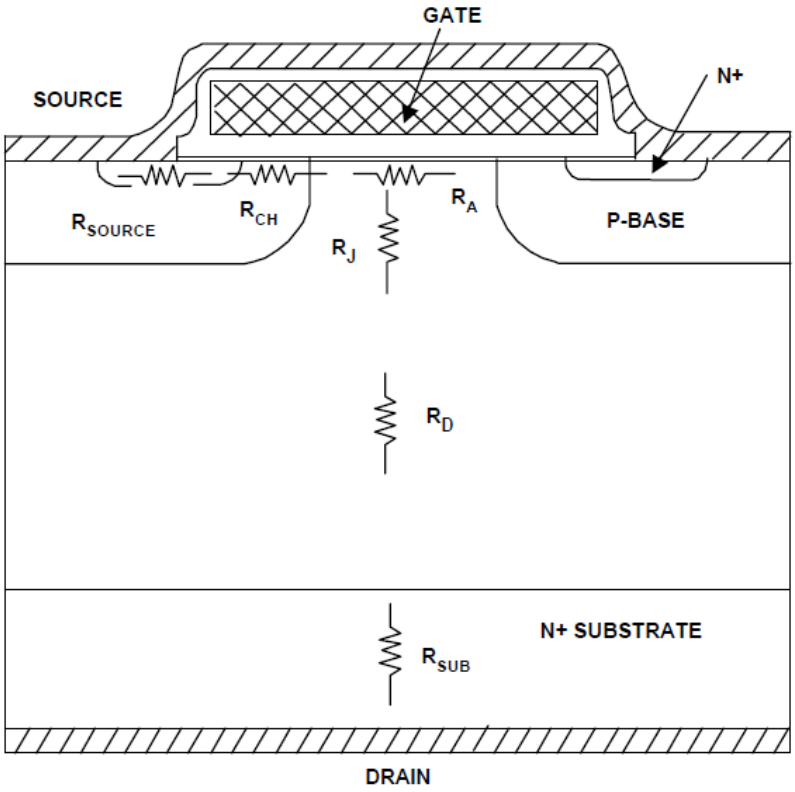

Figure 3.7 Contribution of different parts of a power MOSFET to the on-resistance.

3.3.3 Output Capacitance of MOSFET Used as a Switch

When used as a switch, the basic function of the MOSFET is to control the drain current by the gate voltage. Figure 3.8 [37] shows an equivalent circuit model often used to analyze switching performance of MOSFETs. In this model, R_G is the distributed resistance of the gate, L_D and L_S are drain and source lead inductances which are about tens of nano Henrys (nH). MOSFET data sheets often give values of input capacitance C_{iss}, output capacitance C_{oss} and reverse transfer capacitance C_{rss} for circuit designers to use as starting points to determine components values. Manufacturers use these values because they can be measured directly on the MOSFET. They are defined as:

$$C_{iss} = C_{GD} + C_{GS} \tag{3.7}$$

$$C_{oss} = C_{GD} + C_{DS} \tag{3.8}$$

$$C_{iss} = C_{GD} \tag{3.9}$$

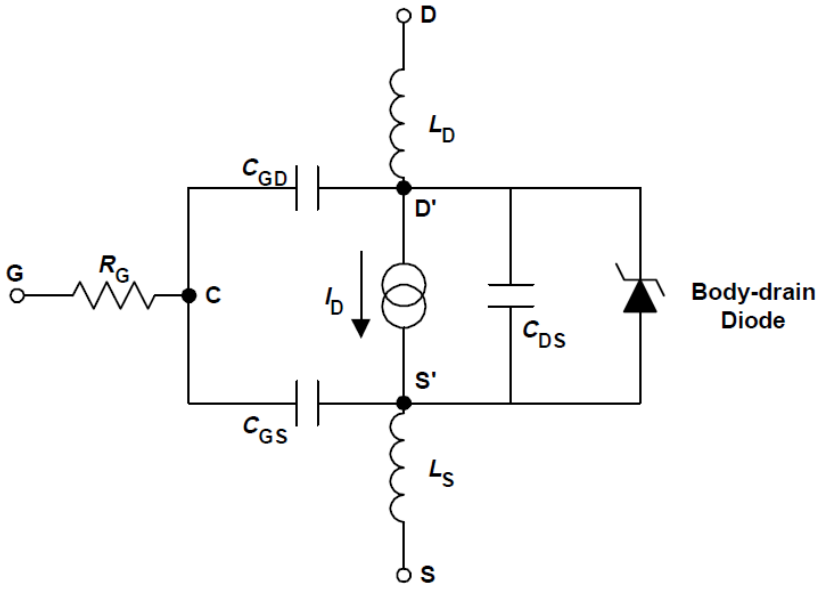

Figure 3.8 Equivalent circuit showing components that have the greatest effect on switching.

where,

C_{GD} is gate-to-drain capacitance,

C_{GS} is gate-to-source capacitance,

C_{DS} is drain-to-source capacitance.

These capacitors must be charged or discharged when the MOSFET is switching. Typical values of output capacitances for commercial MOSFETs are, Si4500BDY by Vishay Siliconix as an example [39], 400 pF for n-channel and 200 pF for p-channel at $V_{GS} = 5\text{V}$ (same as the V_{dd} of the CMOS invertor). To have as accurate as possible results for the application of small capacitance measurement that is usually below 100 pF, these values are too large to be parallel to the sensor capacitor. Therefore, utilizing commercial

MOSFETs with smaller output capacitances is obliged. The dual NMOS/PMOS FDC6320C by Fairchild Semiconductor [38] turns out to be a better choice: C_{oss} is 8 pF for n-channel and 9 pF for p-channel at $V_{GS} = 5\text{V}$. This model of MOSFET is used in the MOSFET interface circuit in this thesis.

It is interesting to notice that smaller on-resistance (less than 0.1 Ohms for the Si4500BDY) usually means larger gate capacitance (hundreds of pF for the Si4500BDY), while on the other hand, larger on-resistance (several Ohms for the FDC6320C) usually means smaller gate capacitance (several pF for the FDC6320C). This is due to the structures of fabrication and quite understandable because, generally speaking, the resistance decreases when the physical distance between the two gate electrodes is smaller but the capacitance increases. In this application, it is easy to make a choice of selection based on the gate capacitance since the system is much more sensitive to the capacitance than to the resistance and the differences among on-resistances are relatively smaller.

4. MOSFET CIRCUIT

4.1 Circuit design

As previously discussed, using the technique of charging and discharging the capacitor of an RC network, an unknown sensor capacitance can be measured by a RC network phase delaying a square wave fed into the network buffered by CMOS inverters and then compared with a reference square wave identical to the input by an EXOR gate phase detector to generate a PWM signal whose duty cycle is linearly proportional to the sensed capacitance. Then this PWM signal is low pass filtered and converted to a DC voltage whose level is proportional to the PWM duty cycle and thus to the sensed capacitance.

Although the process is clear, the linear relationship between the duty cycle and the capacitance has a very small range limited by C not being fully charged and discharged each cycle. To illustrate this, consider the schematic of a traditional RC phase delay interface circuit in Figure 4.1. In this interface circuit, the RC network consists of a resistor $R = 150\text{k}\Omega$, a sensor capacitor $C_s = 10\text{pF}$ and a board capacitance $C_b = 41.9\text{pF}$ which stands for the overall capacitance of the circuit board in testing. A square wave signal at the frequency of 10kHz with the duty cycle of 50% and the amplitude of 5V is fed into the system to simulate the process. Models of CMOS inverters of 74HC04 and an EXOR

gate of 74HC86 built in LTSpice software are used.

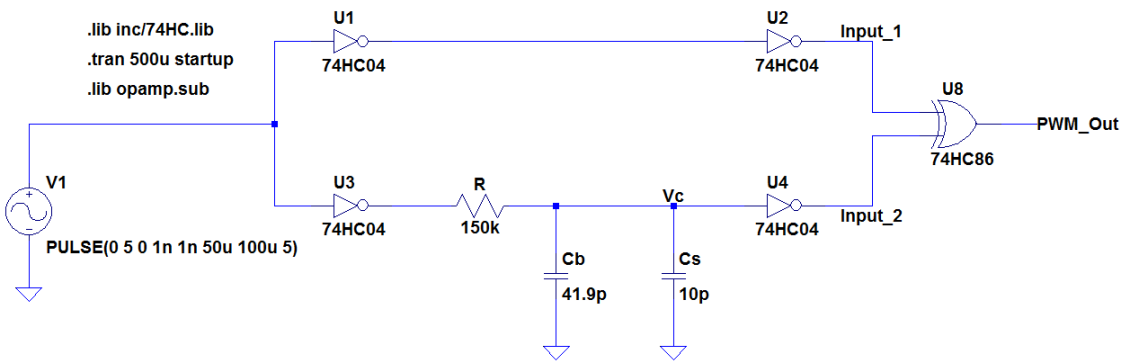

Figure 4.1 Schematic of a traditional RC phase delay interface circuit.

After running a transient simulation of $500\mu s$ i.e. 5 periods of the square wave of 10kHz, the results are plotted in Figure 4.2 where the light blue waveform is probed at the node "Vc" which is the voltage across the sensor capacitors $C_s + C_b + C_g$, the red waveform is probed at the node "Input_1" and the blue one at the node "Input_2" which are the two inputs to the EXOR gate, while the green waveform is probed at the output of the EXOR gate of "PWM_Out" which shows the detected phase difference between the waveforms from "Input_1" and "Input_2".

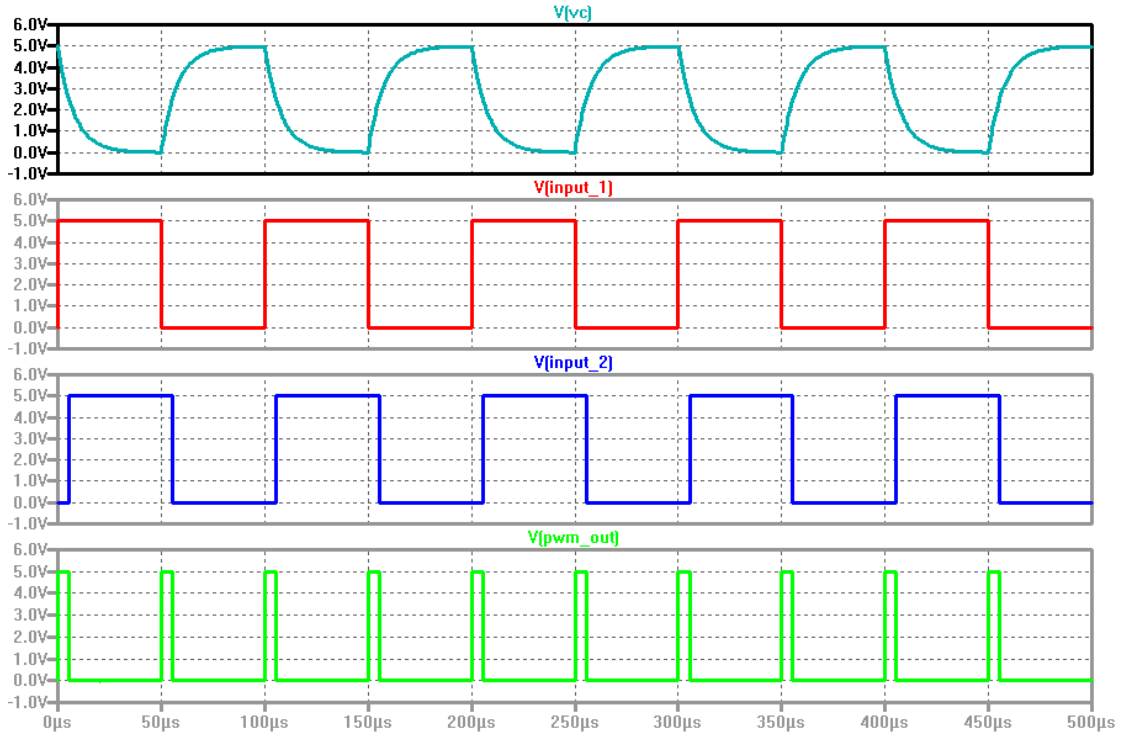

Figure 4.2 Simulation result of the traditional RC phase delay interface circuit with the sensor capacitance of 10pF and the input frequency of 10kHz.

Notice that in Figure 4.2, the waveform at "Vc" shows that the capacitor is nearly charged to 5V (V_{dd}) and fully discharged to 0V in each cycle, which result in a proper linear relationship between the PWM duty cycle and the capacitance as expected. If we increase the sensor capacitance C_s from 100pF to 10pF, thus linearly increase the $t_{0.5}$ of Equation (3.4) to be larger than half of the input signal period, the transient simulation results turns out to be as plotted in Figure 4.3, where it is clear to see from the waveform at node "Vc" that the capacitors are not fully charged or discharged in each cycle. The delay becomes too long before the capacitors have time to be fully charged or discharged, the next change of the invertor logic state has arrived to discharge or charge the capacitors respectively. This observation confirms the theoretical analysis of the limited range of linear relationship. However, the understanding of the mechanism of the problem also cast

lights on the solution: force the capacitors to be fully charged or discharged fast immediately when the voltage increases to the trip voltage of $V_{dd}/2$ or decreases to it respectively.

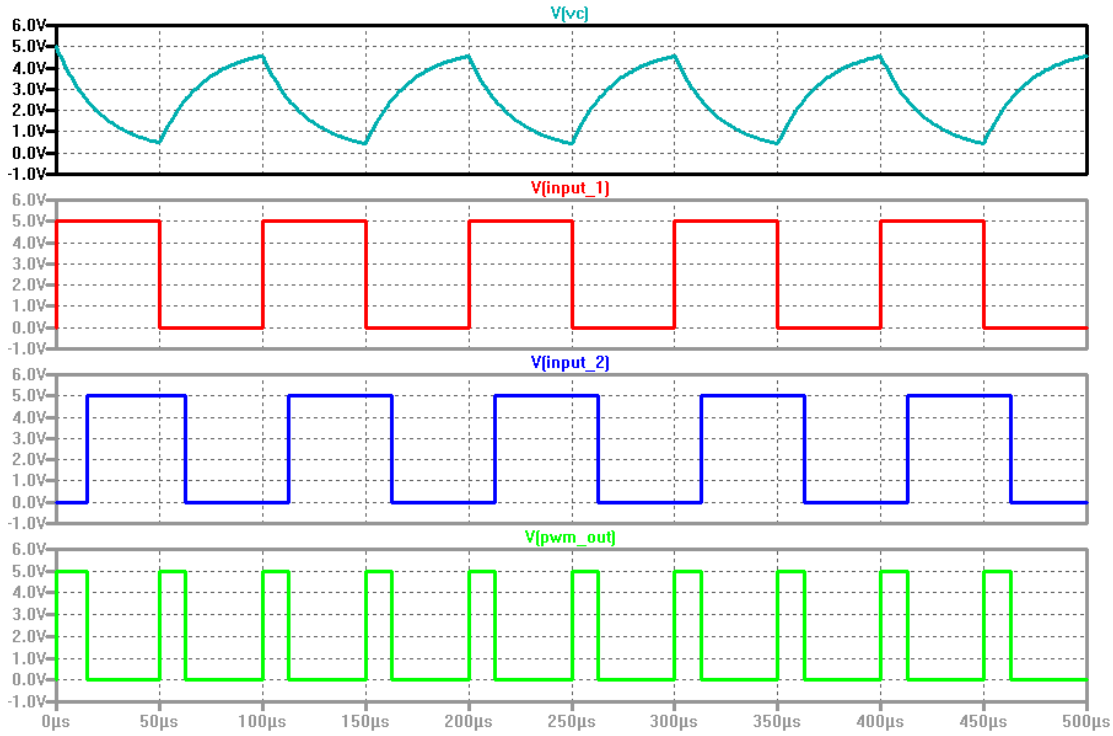

Figure 4.3 Simulation result of the traditional RC phase delay interface circuit with the sensor capacitance of 100pF and the input frequency of 10kHz.

Notice that, in Figure 4.3, "Input_1" and "Input_2" have a phase difference when and only when "Vc" is charging from 0V to 2.5V (the trip voltage of $V_{dd}/2$) or discharging from 5V (V_{dd}) to 2.5V, while "Vc" slowly continues to charge or discharge when "Input_1" and "Input_2" have the same low or high state (opposite because of the inverter). Therefore, the problem can be solved if we can manipulate the voltage at "Vc" in the durations of "Input_1" and "Input_2" having the same state, while leaving it alone for the durations with a phase difference because they are the "eigen" time for the RC phase delay technique to function.

An improved method can be accomplished by adding a p-channel MOSFET (PMOS) as a switch to pull the voltage at "Vc" up to V_{dd} i.e. 5V and an n-channel MOSFET (NMOS) as a switch to pull it down to ground i.e. 0V at proper times, as shown in the schematic in Figure 4.4. Specifically, when "Input_1" and "Input_2" are both in the low state, these two signals are fed into a NOR gate combined with a NOT gate (inverter) to set the gate -source voltage V_{GS} of the PMOS to be low thus switch on the PMOS whose source is connected to 5V and drain to "Vc", which pulls "Vc" up to 5V immediately. Likewise, when "Input_1" and "Input_2" are both in the high state, these two signals are fed into a NAND gate combined with a NOT gate (inverter) to set the gate -source voltage V_{GS} of the NMOS to be high thus switching on the NMOS whose source is connected to ground and drain to "Vc", which pulls "Vc" down to 0V very quickly.

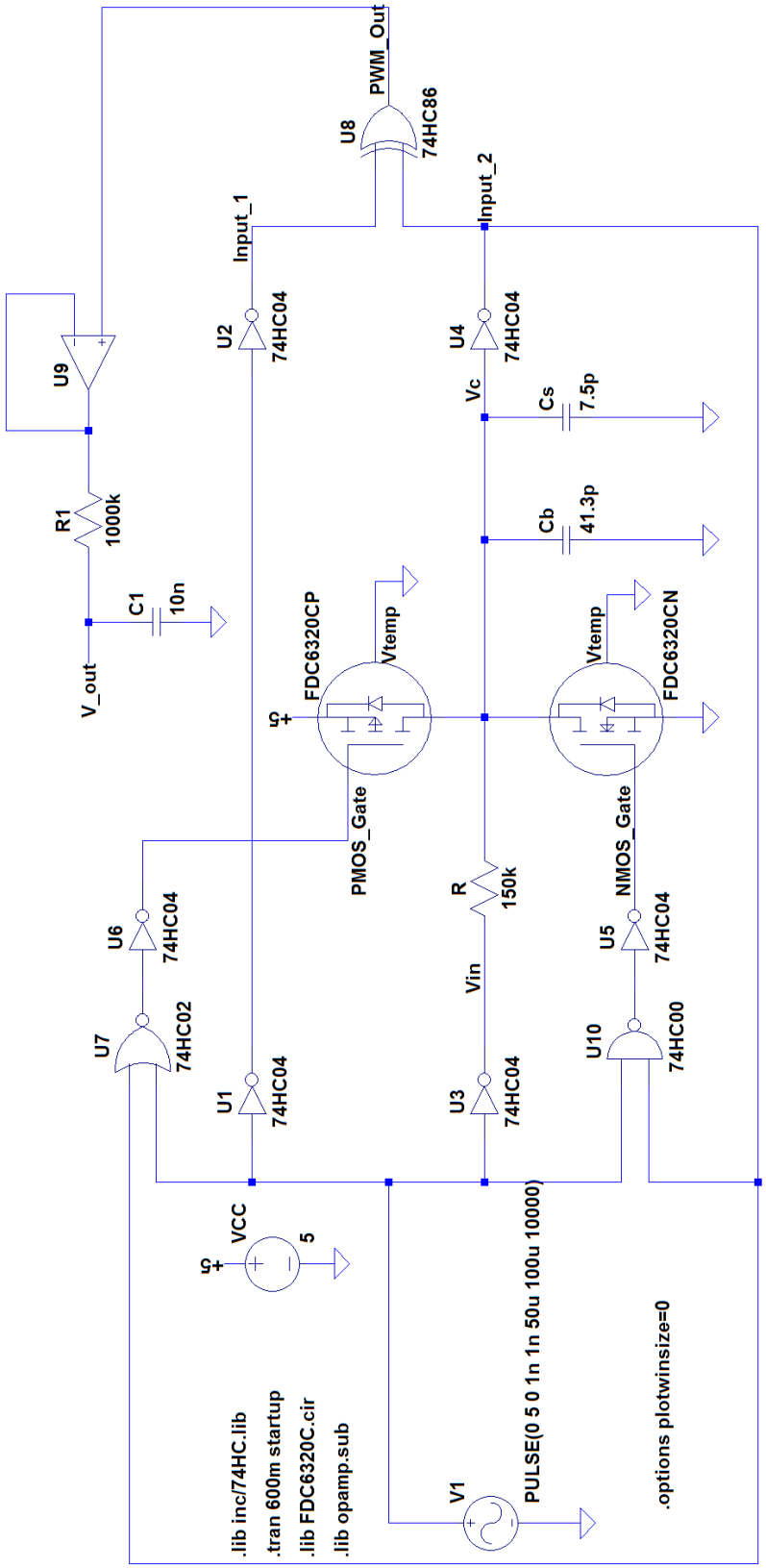

Figure 4.4 Schematic of the MOSFET interface circuit.

It is important to notice that, according to the logic function of the NOR (Table 4.1) and NAND (Table 4.2) gates, when the PMOS is switched on, the NMOS is off, and vice-versa. And both are switched off when the "Vc" is charged or discharged to the trip voltage of 2.5V. This leaves the effective charging and discharging period unaffected, and thus the linear relationship between the PWM duty cycle and sensed capacitance is undisturbed.

The MOSFETs in use are the PMOS and NMOS on a dual p and n channel MOSFET model of FDC6320C by Fairchild Semiconductor. It offers a low on-resistance of 3.1Ω and output capacitances of 9pF for p-channel and 8pF for n-channel at 5V, which is pretty ideal for this application.

Table 4.1 Truth table of a NOR gate

Input		Output
A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0

Table 4.2 Truth table of a NAND gate

Input		Output
A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

Last but not least, the purpose of utilizing the NOR-NOT-PMOS and NAND-NOT-NMOS combinations instead of OR-PMOS and AND-NMOS is to synchronize the state change because the phase is also delayed through the inverters/NOT gates, even though these two sets of combinations have the same logic function.

4.2 Circuit simulation

Figure 4.5 depicts the LTSpice simulation result of the novel MOSFET interface circuit. Notice that although the sensor capacitance is the same 100pF as that in Figure 4.3, the PWM duty cycle is wider because "Vc" is sharply fully charging and fully discharging every time it reaches the trip voltage, which leaves a great potential for expanding the effective phase delay with the approximately $180°$ linear range instead of only about $1/4$ of it.

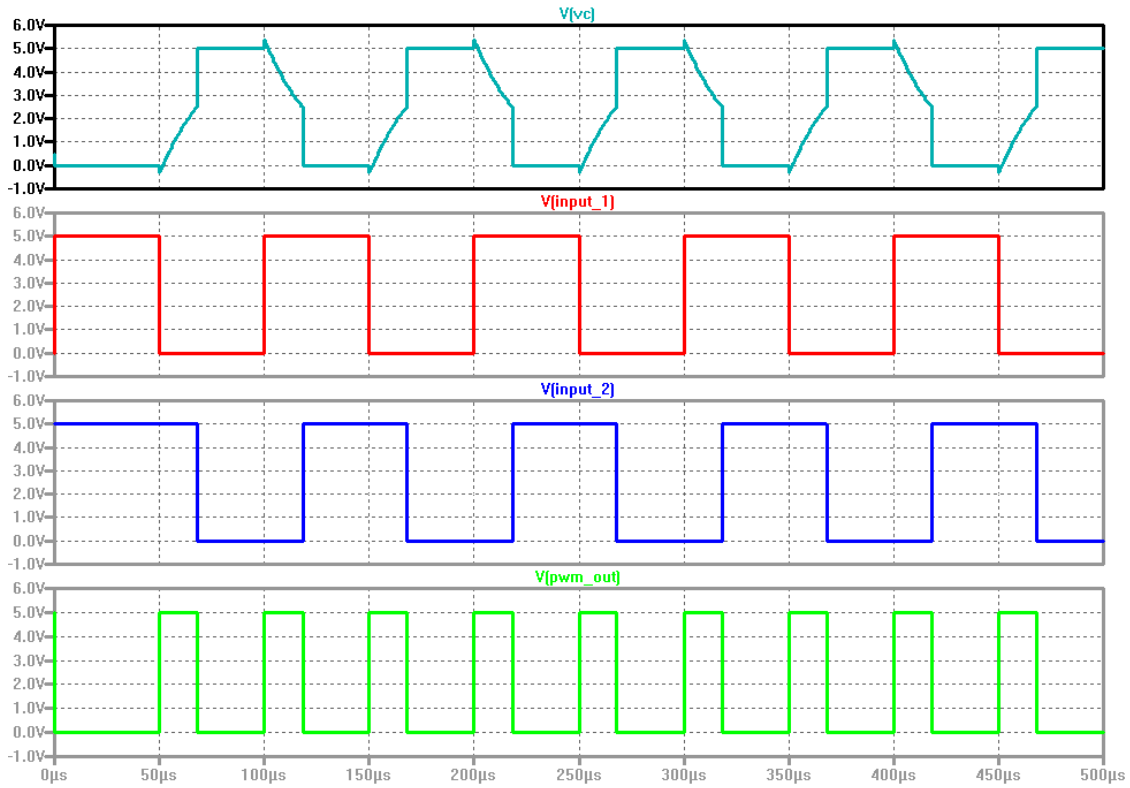

Figure 4.5 Simulation result of the MOSFET RC phase delay interface circuit with the sensor capacitance of 100pF and the input frequency of 10kHz.

In the schematic shown in Figure 4.4, a simple 1st stage single pole RC low pass filter is also applied at the output of the EXOR gate with an ideal operational amplifier (op amp) forming a unity-gain buffer or voltage follower [40] between them to drive any desired filter resistance as a load without loss of signal voltage. The values of resistance and capacitance are designed to have a low cutoff frequency of 16Hz and a small ripple. The result is plotted in Figure 4.6 after running a transient simulation for 200ms.

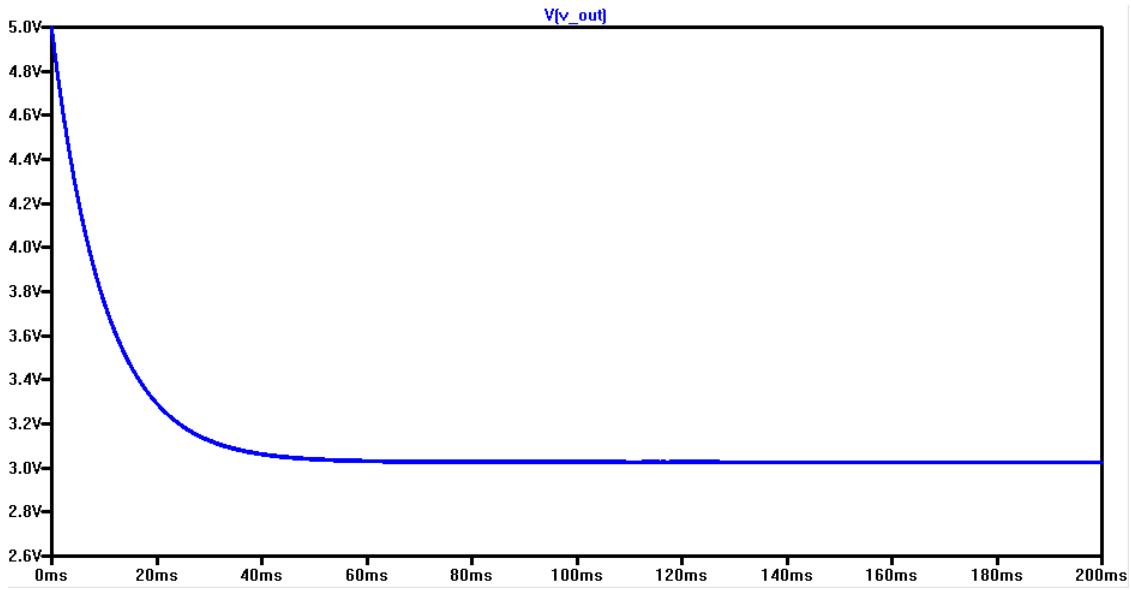

Figure 4.6 Simulation result of the MOSFET RC phase delay interface circuit for the PWM converted to DC voltage with the sensor capacitance of 100pF and the input frequency of 10kHz.

Further experiments are now necessary to collect more data to plot the PWM duty cycle or on-width versus the capacitance and the DC voltage versus capacitance to find out whether they are linear or not, and also to explore the maximum frequency of the system to have linear response. These will be discussed in the next three sections.

4.3 Circuit implementation

The prototype of the 5V MOSFET interface circuit was built on a breadboard (Figure 4.7) using two MC14049 CMOS inverter ICs, an MC14011 CMOS NAND gate, an MC14001 NOR gate, an MC14070 EXOR gate and a FDC6320C dual channel MOSFET.

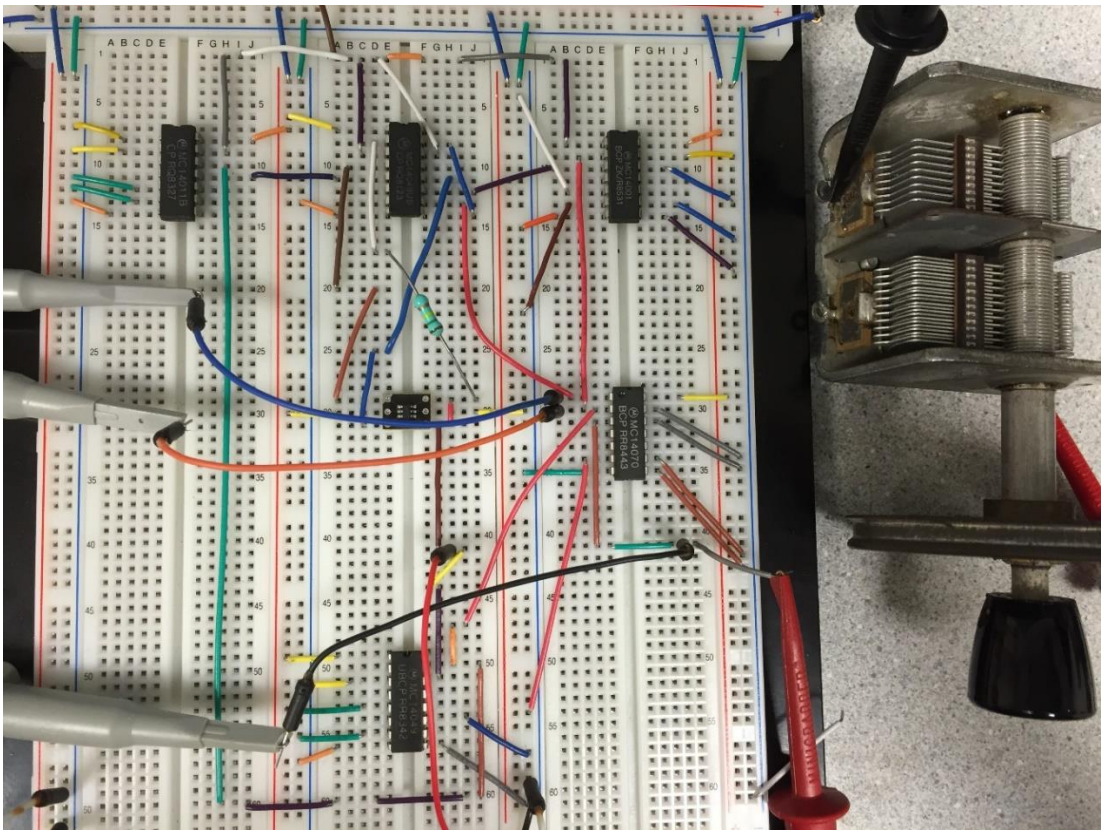

Figure 4.7 MOSFET interface circuit prototype on a bread board.

The resistor for the core RC network is a $150\text{k}\Omega$ film resistor (Figure 4.8) and a variable mechanical multi-plate capacitor (Figure 4.9) with a range of approximately $8\text{pF} - 128\text{pF}$ is used to simulate the sensor capacitor C_s since the range is typical for some capacitance sensing applications. The focus of this thesis is the interface circuit design, thus this variable capacitor is sufficient for these tests.

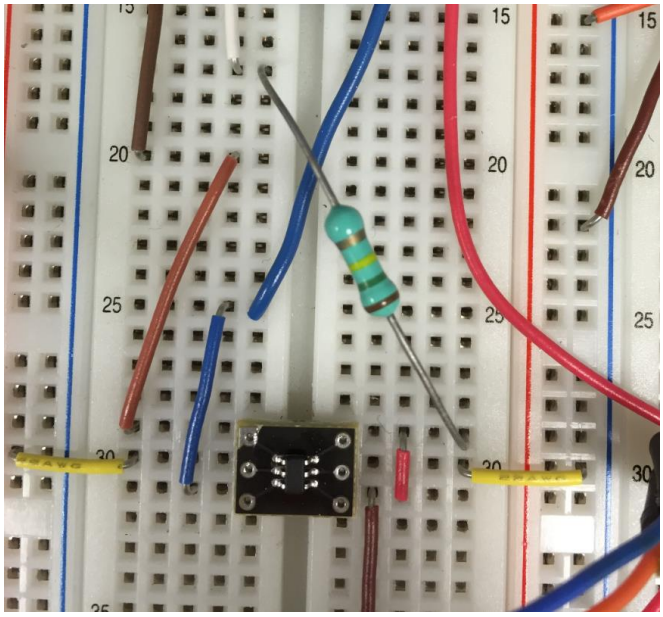

Figure 4.8 A zoomed-in photograph of the dual channel MOSFET of FDC6320C and the resistor of 150kΩ.

Figure 4.9 A zoomed-in photograph of the variable capacitor with a range of 8pF-128pF.

4.4 Circuit testing

To test the circuit, several devices were used. An Agilent E3631A DC power supply was used to provide the 5V DC voltage for the entire circuit. An Agilent 33220A 20MHz function generator (Figure 4.10) generated square waves with a 50% duty cycle and 5V amplitude at selected frequencies (5kHz, 10kHz and 16.67kHz in this application for

comparison) as the V_{in} signal. An Agilent MSO-X 2004A 70MHz 4-channel oscilloscope with a USB connector (Figure 4.11) was used to probe the waveforms at “Vc”, “Input_1” and “Input_2”, and the DC voltage of “V_out” from the low pass filter to save the plots and data in a flash memory for further analysis. A GW Instek LCR-821 LCR meter was used to measure the capacitances of the variable capacitor as the standard values for the testing. Also, the PWM signal was fed into a 8-pole programmable dual channel filter of the model SR640 by Stanford Research Systems used as a low pass filter to convert the PWM to a DC voltage. The output DC voltage was then probed by the 4th channel of the oscilloscope that measured its root-mean-square (RMS) values (Figure 4.13).

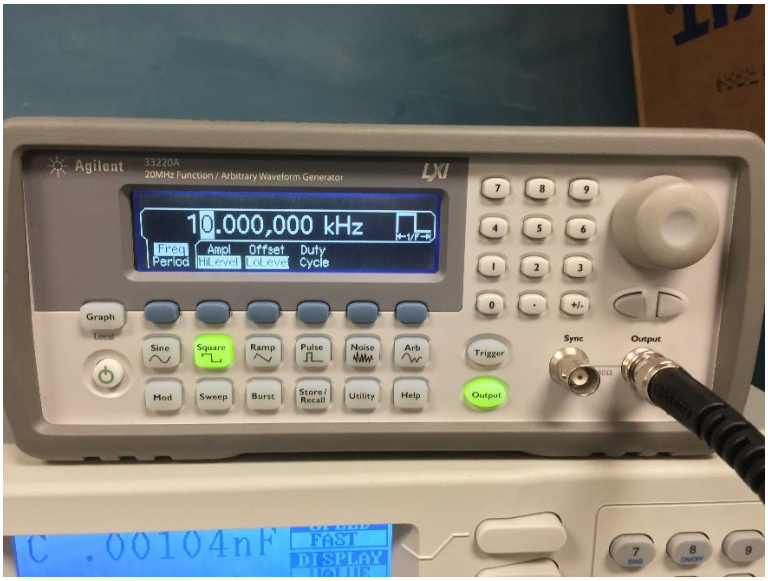

Figure 4.10 Agilent 33220A 20MHz function generator.

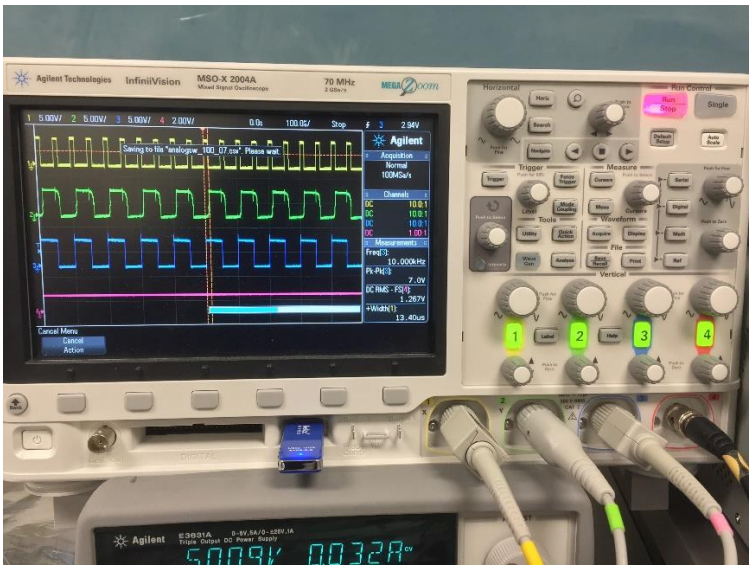

Figure 4.11 Agilent MSO-X 2004A 70MHz 4-channel oscilloscope.

Figure 4.12 GW Instek LCR-821 LCR meter measuring the variable capacitor.

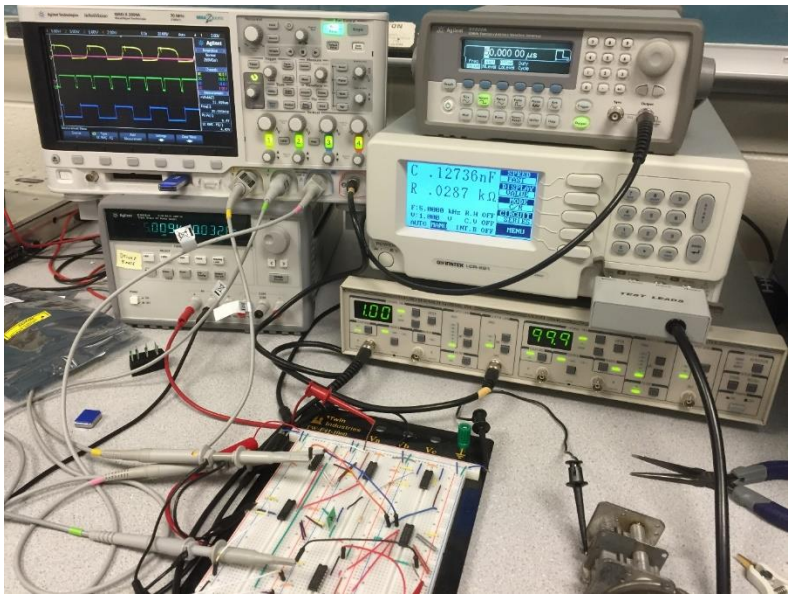

Figure 4.13 The entire set of devices for the testing.

By setting the variable capacitor at the maximum capacitance that is measured by the LCR meter as 127pF, the maximum frequency for the input square wave can be explored by increasing the frequency while monitoring the waveform of node "Vc" probed by the oscilloscope to make sure that it is fully charged and discharged at each cycle. This is necessary because other parasitic capacitances, such as the breadboard capacitance, which is influenced by how the circuit is built, are unknown but large enough to affect the overall capacitance effective in the RC phase delay technique. In this case, the maximum frequency turns out to be 16.67kHz or the minimum period is 60μs.

As comparisons, lower frequencies of 10kHz (100μs) and 5kHz (200μs), along with the maximum frequency, are used both on the MOSFET circuit and a traditional RC phase delay circuit built on the breadboard as well. Figure 4.14-4.16 show oscilloscope plots of the waveforms and measurements at frequencies of 5kHz, 10kHz, 16.67kHz respectively, in all of which the yellow waveforms are probed at "PWM_Out", the green

at “Input_2”, the blue at “Input_1” and the red at “V_out” (nodes marked in Figure 4.4). Also, the width of the PWM and the RMS of the DC output are measured and saved in each measurement. Though these three sets of plots only include waveforms with the maximum and minimum capacitances, from which it is already clear that both the PWM duty cycle and the DC voltage level decrease as the capacitance decreases and the PWM duty cycle has the best use of the phase delay range at the maximum frequency, the tests are performed by changing the variable capacitor in steps of $10pF$ between the maximum and minimum, and detailed sets of data are plotted and analyzed in the next section.

Notice that the PWM signal is not as perfectly symmetric as that in the simulation result. This is due to the real world implementation of two legs of the circuit with a difference in length. However, the asymmetry of the PWM signal can be solved by converting to the DC voltage, since the low pass filter has the function of averaging.

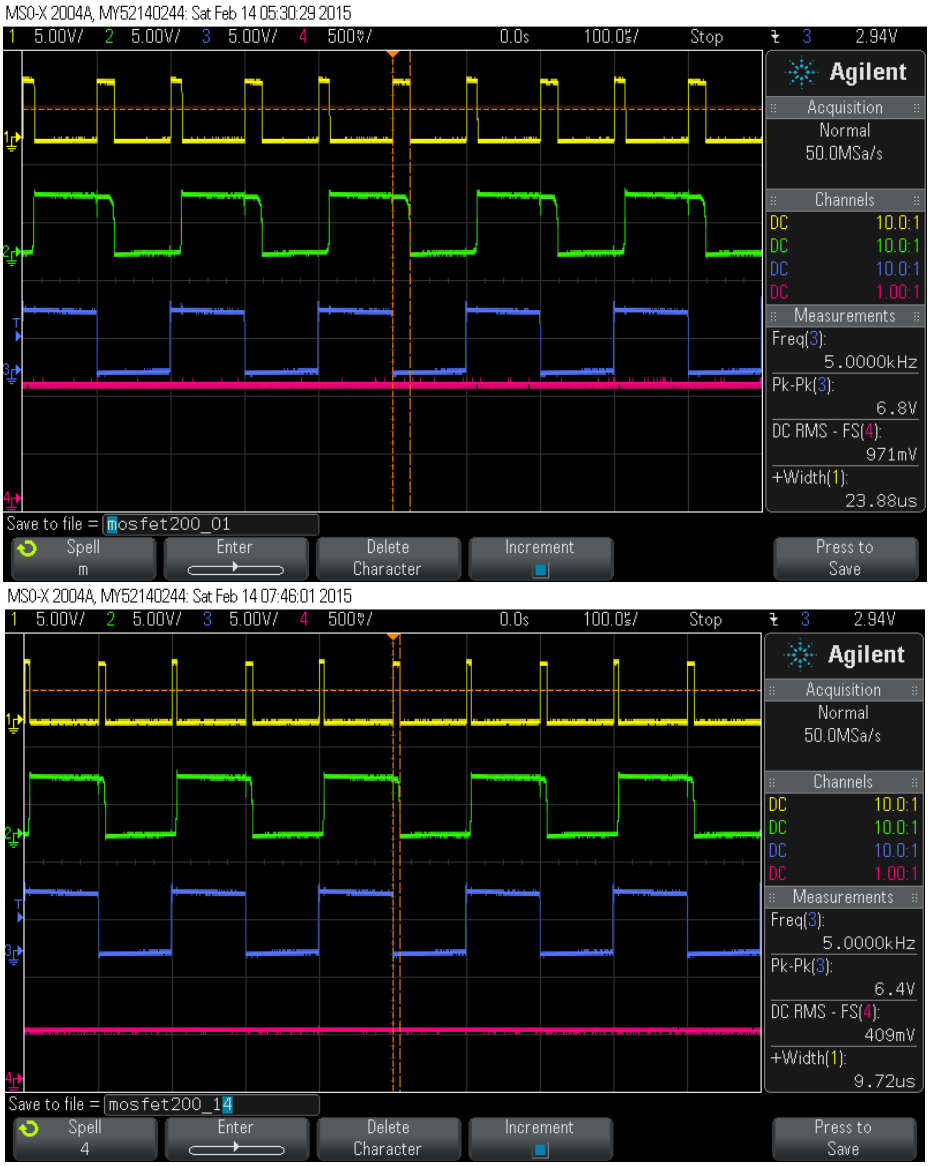

Figure 4.14 Oscilloscope plot of test result at input frequency of 5kHz.

Up: capacitance is 127pF as maximum;

Down: capacitance is 7.97pF as minimum.

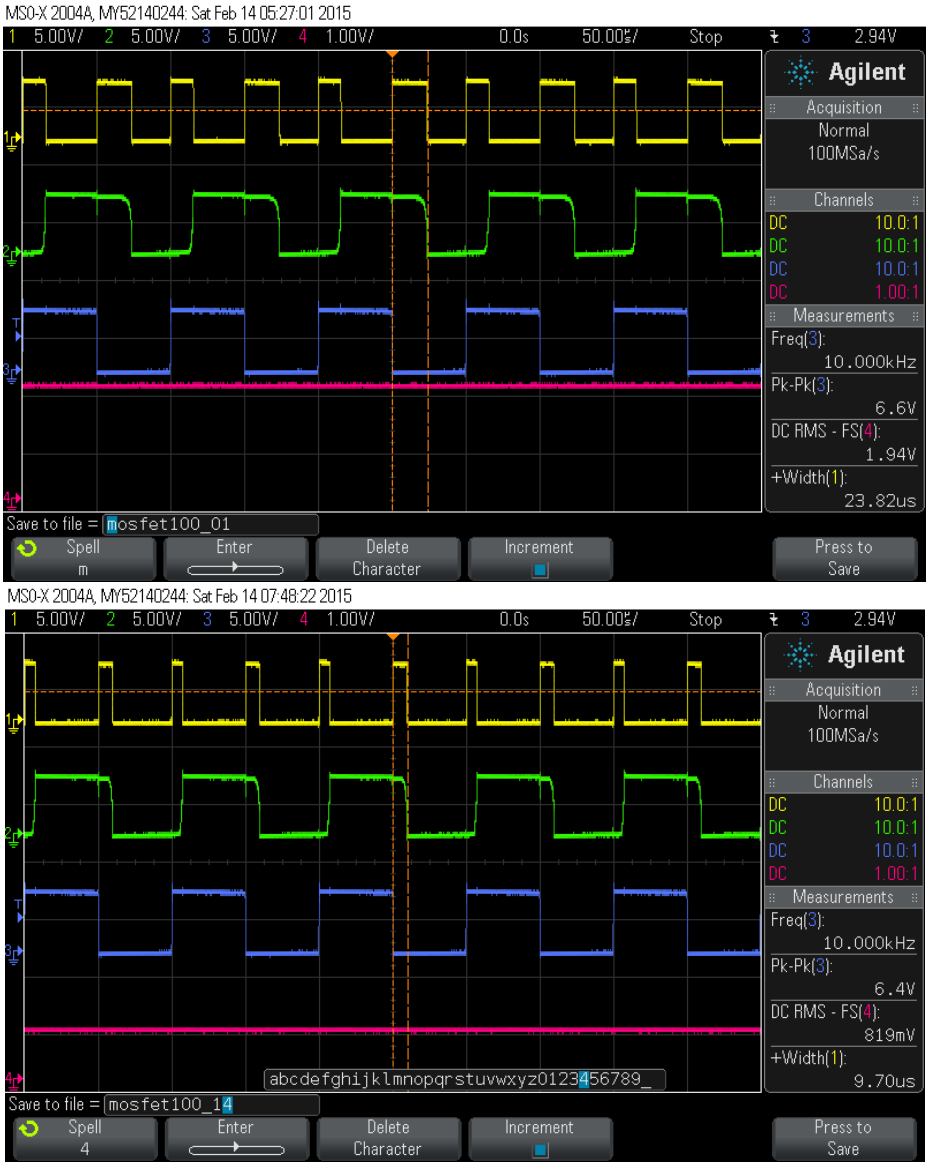

Figure 4.15 Oscilloscope plot of test result at input frequency of 10kHz.

Up: capacitance is 127pF as maximum;

Down: capacitance is 7.97pF as minimum.

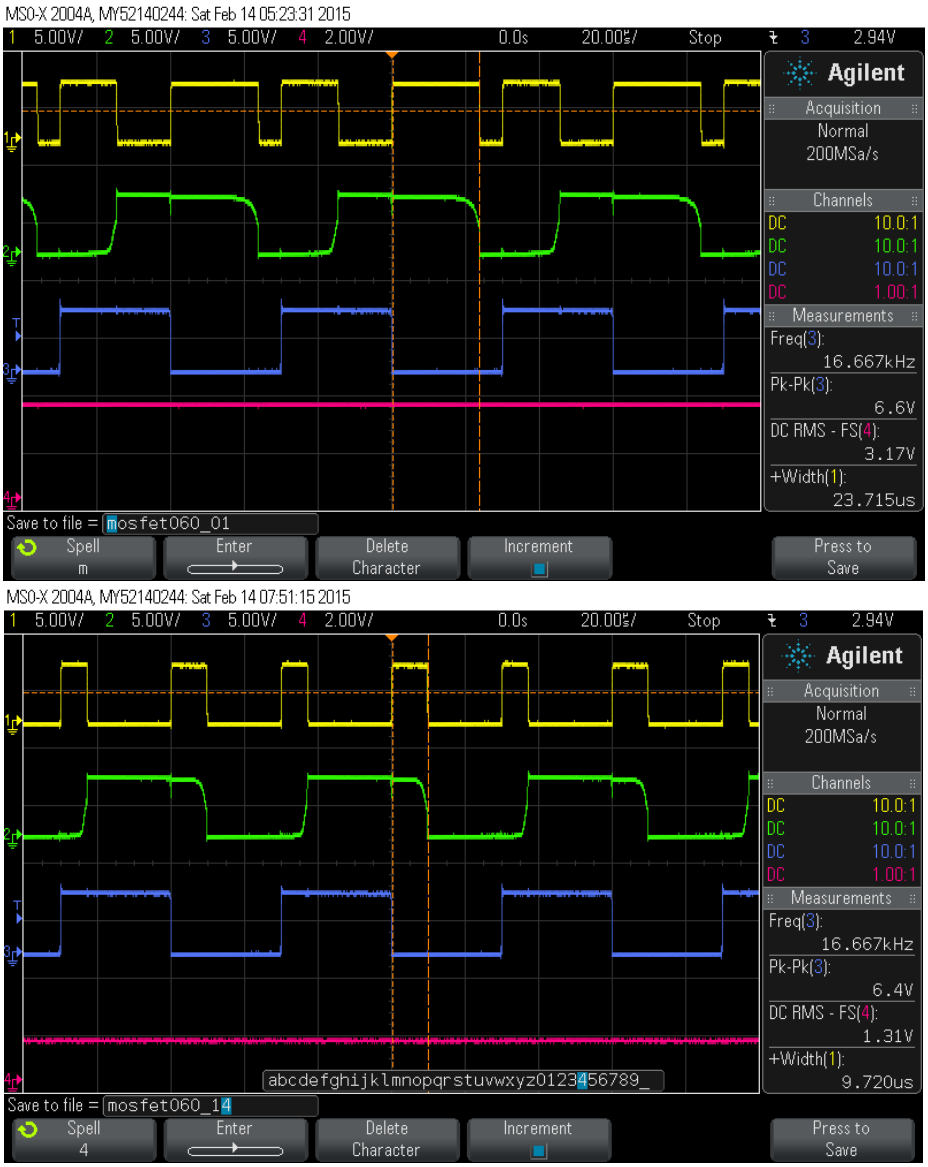

Figure 4.16 Oscilloscope plot of test result at input frequency of 16.67kHz.

Up: capacitance is 127pF as maximum;

Down: capacitance is 7.97pF as minimum.

4.5 Results

Take the test at the input frequency of 5kHz as an example, the data of the PWM pulse width and the DC voltage level results from both the simulation and testing against 14 different capacitance values, minimum and maximum along with 12 other points between them with a step of approximately 10pF, is collected in Table 4.3 and plotted in Figure 4.17. The same procedure is followed for the cases at the frequencies of 10kHz and 16.67kHz in Table 4.4-4.5 and Figure 4.18-4.19 respectively.

As comparisons, the same method of experiment is applied on the traditional RC phase delay interface circuit without the MOSFETs, whose schematic is shown in Figure 4.1, at input frequencies of 5kHz, 10kHz and 16.67kHz, and sets of data are collected in Table 4.6-4.8 and plotted in Figure 4.20-4.22 respectively.

The results from both the simulation and the test turn out to prove that the MOSFET interface circuit works as expected to expand the linear response of the RC phase delay circuit, though the results from the simulation and the test have tolerable differences due to the ideality of the simulated circuit model in the LTSpice software. From Figure 4.17-4.19, along with the increase in frequency, plots from both the simulation (blue plots) and the test (orange plots) keep a good degree of linearity ($R^2 = 1$ for all simulations and $R^2 > 0.999$ for all tests) whether for PWM pulse width versus capacitance or DC voltage versus capacitance. Notice that, when increasing the frequency, not only does the linearity slightly improve, the range of change also covers more, whether for the PWM pulse width for the DC voltage, which is beneficial for more accurate reading. For example, at the

maximum frequency of 16.67kHz, the DC voltage varies from 1.31V to 3.17V within the range of 5V, while it is from 0.409V to 0.971V at 5kHz.

As for the traditional interface circuit, however, the plots have good linearities at 5kHz, start to become apparently nonlinear at 10kHz and become very nonlinear at 16.67kHz. Therefore, the novel MOSFET interface circuit is a good improvement compared to the traditional approach. Specifically, the percentage of linear response range over the potential maximum phase delay range of 180° increases from 25% to 46.7% (increases by 21.7%). This result is limited by the variable capacitor we have and can be even larger if the range of the measured capacitance is larger.

It is also interesting to see that the plots from simulation and test match better for the traditional circuit at lower frequency than they do for the MOSFET circuit. This is due to the simplicity and fewer component models used in the traditional circuit.

Table 4.3 Results for the MOSFET circuit at input frequency of 5kHz.

	Capacitance (pF)	Pulse-simulation (us)	Pulse-test (us)	Vout-simulation (mV)	Vout-test (mV)
C1	127	21.31	23.88	1053	971
C2	119.97	20.54	22.84	1015	928
C3	110	19.45	21.72	961.9	884
C4	100.02	18.35	20.56	908.3	835
C5	90	17.28	19.48	854.5	791
C6	80.03	16.16	18.36	800.7	748
C7	70.01	15.06	17.24	746.5	708
C8	59.98	13.94	15.96	692.1	652
C9	50	12.86	14.68	637.5	602
C10	40	11.73	13.68	583	565
C11	30.03	10.63	12.4	528.1	515
C12	20	9.51	11.28	472.5	470
C13	10.02	8.39	9.92	417.1	424
C14	7.97	8.12	9.72	405.6	409

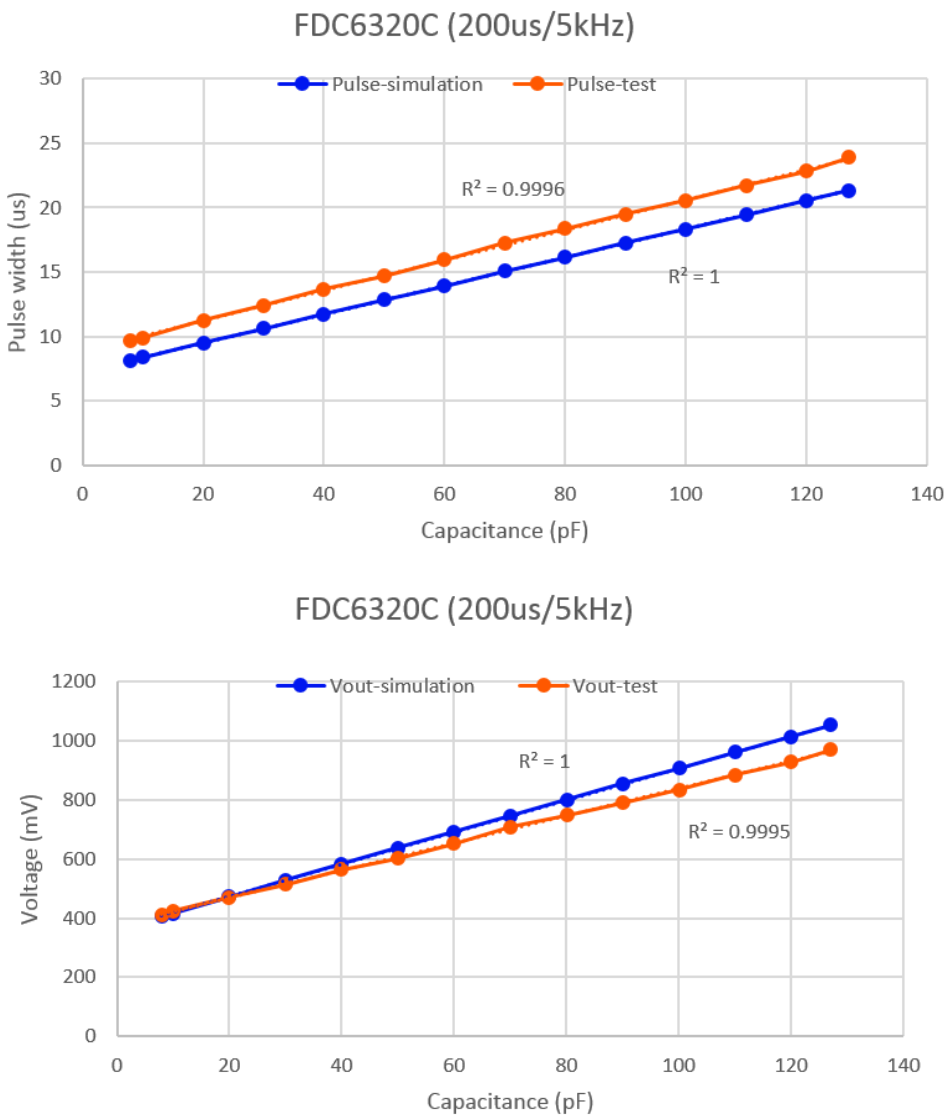

Figure 4.17 Plots of the MOSFET circuit at input frequency of 5kHz.
Up: PWM pulse width versus capacitance;
Down: DC voltage level versus capacitance.

Table 4.4 Results for the MOSFET circuit at input frequency of 10kHz.

	Capacitance (pF)	Pulse-simulation (us)	Pulse-test (us)	Vout-simulation (V)	Vout-test (V)
C1	127	21.31	23.82	2.106	1.94
C2	119.97	20.54	22.86	2.03	1.86
C3	110	19.47	21.8	1.923	1.77
C4	100.02	18.38	20.6	1.816	1.68
C5	90	17.26	19.44	1.709	1.58
C6	80.03	16.17	18.42	1.6	1.5
C7	70.01	15.07	17.28	1.492	1.41
C8	59.98	13.95	15.96	1.383	1.3
C9	50	12.84	14.66	1.275	1.198
C10	40	11.74	13.72	1.166	1.13
C11	30.03	10.62	12.34	1.056	1.026
C12	20	9.5	11.24	0.945	0.939
C13	10.02	8.37	9.96	0.834	0.844
C14	7.97	8.15	9.7	0.811	0.819

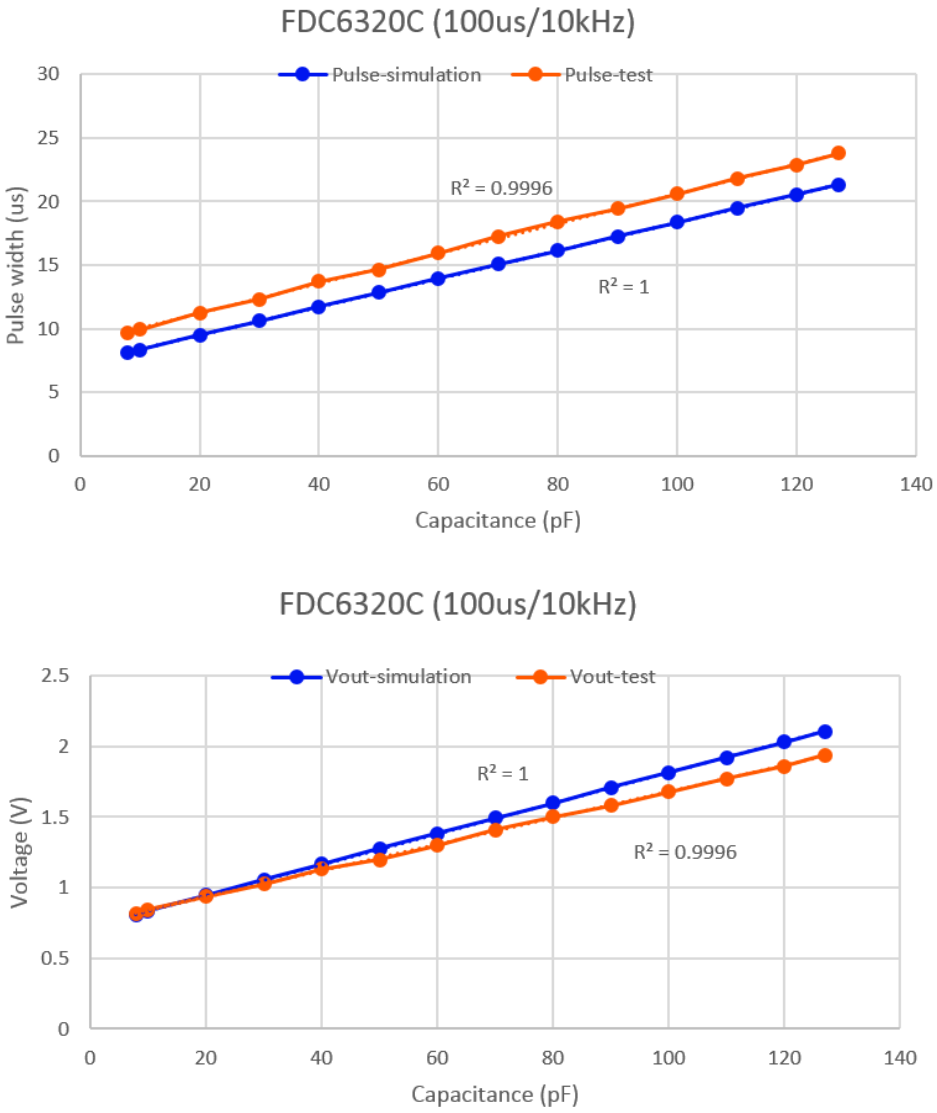

Figure 4.18 Plots of the MOSFET circuit at input frequency of 10kHz.
Up: PWM pulse width versus capacitance;
Down: DC voltage level versus capacitance.

Table 4.5 Results for the MOSFET circuit at input frequency of 16.67kHz.

	Capacitance (pF)	Pulse-simulation (us)	Pulse-test (us)	Vout-simulation (V)	Vout-test (V)
C1	127	21.31	23.715	3.509	3.17
C2	119.97	20.54	22.81	3.384	3.06
C3	110	19.46	21.67	3.205	2.91
C4	100.02	18.38	20.63	3.027	2.74
C5	90	17.26	19.4	2.847	2.59
C6	80.03	16.17	18.39	2.668	2.44
C7	70.01	15.06	17.17	2.487	2.29
C8	59.98	13.96	15.98	2.305	2.11
C9	50	12.84	14.71	2.124	1.95
C10	40	11.71	13.75	1.941	1.81
C11	30.03	10.61	12.36	1.759	1.64
C12	20	9.49	11.34	1.574	1.51
C13	10.02	8.37	9.94	1.389	1.35
C14	7.97	8.14	9.72	1.351	1.31

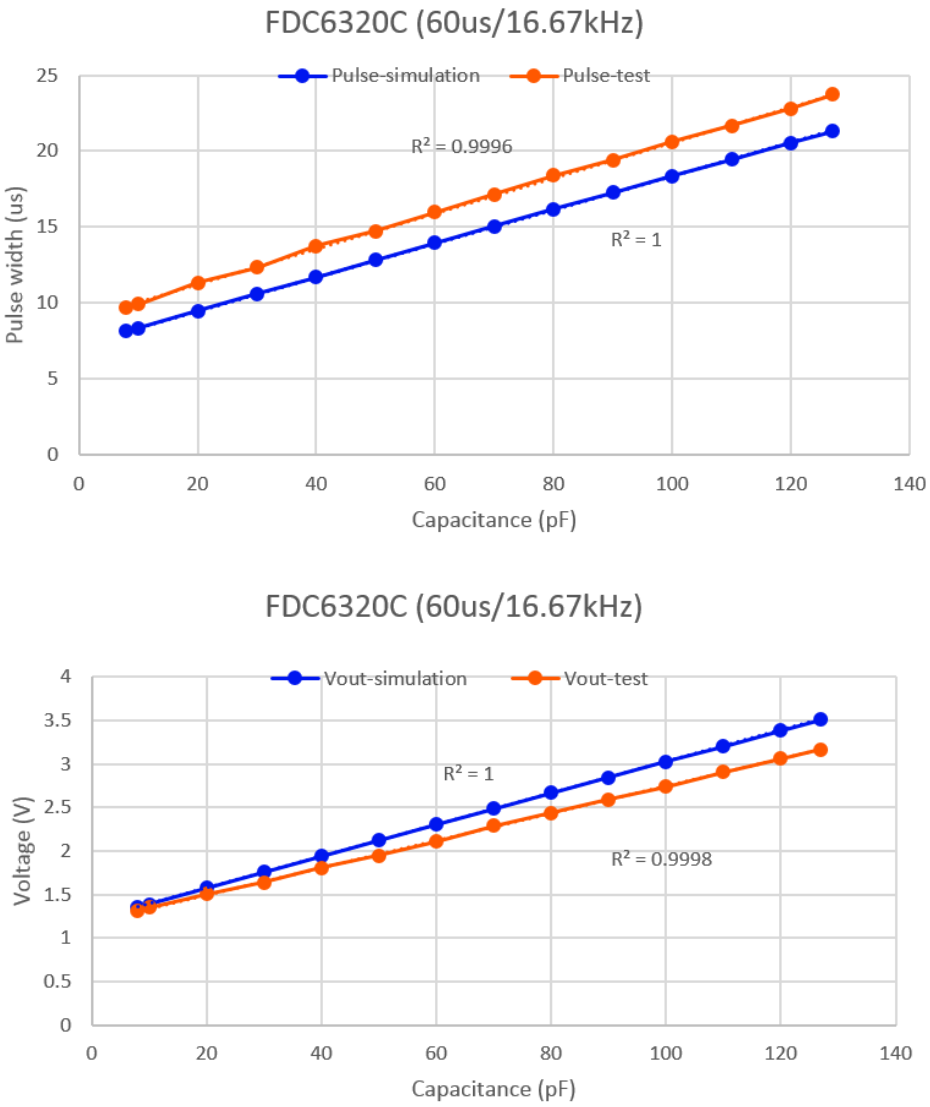

Figure 4.19 Plots of the MOSFET circuit at input frequency of 16.67kHz.
Up: PWM pulse width versus capacitance;
Down: DC voltage level versus capacitance.

Table 4.6 Results for the traditional RC circuit with R=150kΩ at input frequency of 5kHz.

	Capacitance (pF)	Pulse-simulation (us)	Pulse-test (us)	Vout-simulation (mV)	Vout-test (mV)
C1	127.25	17.33	18.56	869.35	894
C2	120	16.68	17.88	836.49	867
C3	110.06	15.76	16.96	789.65	815
C4	100.02	14.82	15.88	743.33	770
C5	90.02	13.85	14.88	694.7	726
C6	80.06	12.88	13.88	645.6	674
C7	69.97	11.87	12.76	594.09	619
C8	60.02	10.88	11.56	544.98	566
C9	50.02	9.84	10.64	493.22	520
C10	40	8.81	9.48	441.4	463
C11	30	7.78	8.44	388.96	408
C12	20	6.74	7.44	337.89	343
C13	10.02	5.72	6.24	286.41	291
C14	7.83	5.48	5.88	275.01	286

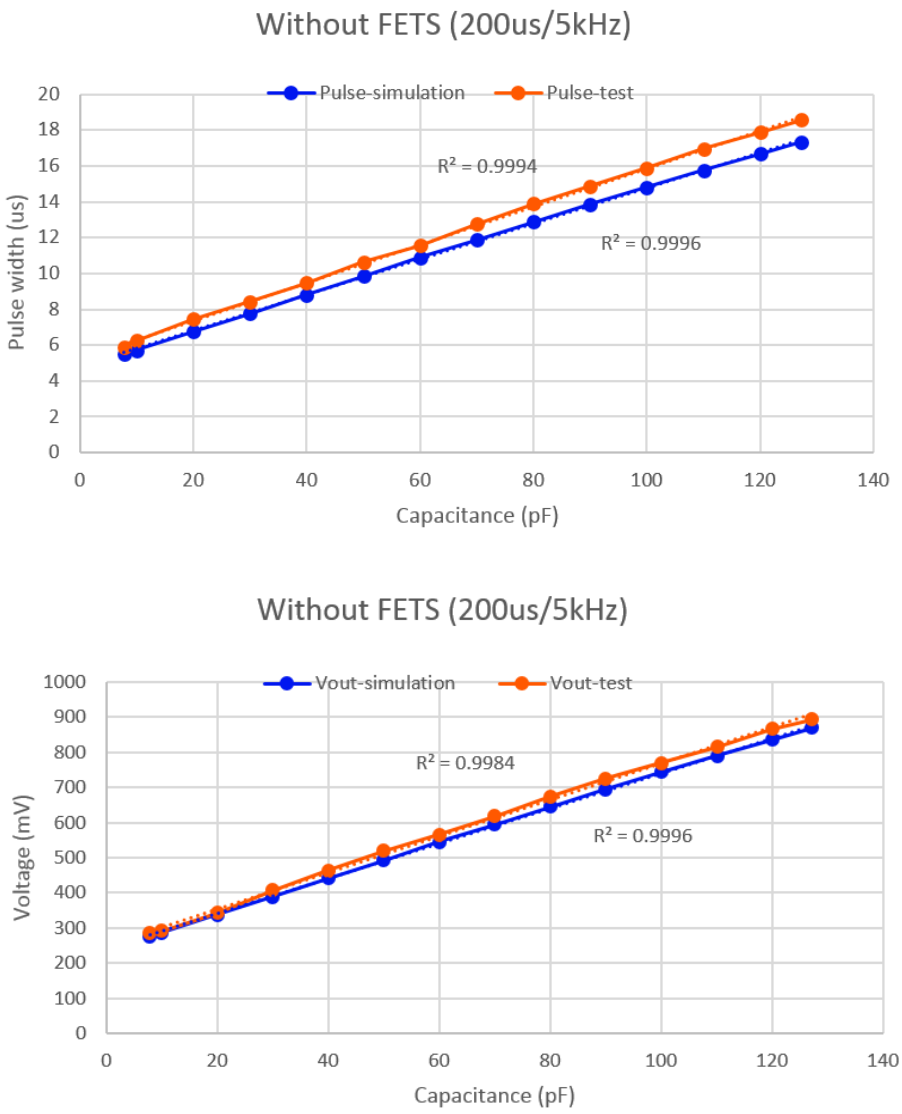

Figure 4.20 Plots of the traditional RC circuit with R=150kΩ at input frequency of 5kHz.
Up: PWM pulse width versus capacitance;
Down: DC voltage level versus capacitance.

Table 4.7 Results for the traditional RC circuit with R=150kΩ at input frequency of 10kHz.

	Capacitance (pF)	Pulse-simulation (us)	Pulse-test (us)	Vout-simulation (V)	Vout-test (V)
C1	127.25	14.38	15.76	1.444	1.5
C2	120	14.03	15.34	1.41	1.47
C3	110.06	13.53	14.8	1.359	1.42
C4	100.02	12.96	14.12	1.301	1.36
C5	90.02	12.36	13.52	1.241	1.3
C6	80.06	11.72	12.84	1.175	1.232
C7	69.97	11.01	11.98	1.106	1.161
C8	60.02	10.25	11.14	1.03	1.077
C9	50.02	9.44	10.24	0.947	0.993
C10	40	8.57	9.26	0.859	0.899
C11	30	7.65	8.34	0.767	0.807
C12	20	6.7	7.26	0.67	0.68
C13	10.02	5.69	6.24	0.571	0.58
C14	7.83	5.47	5.84	0.548	0.572

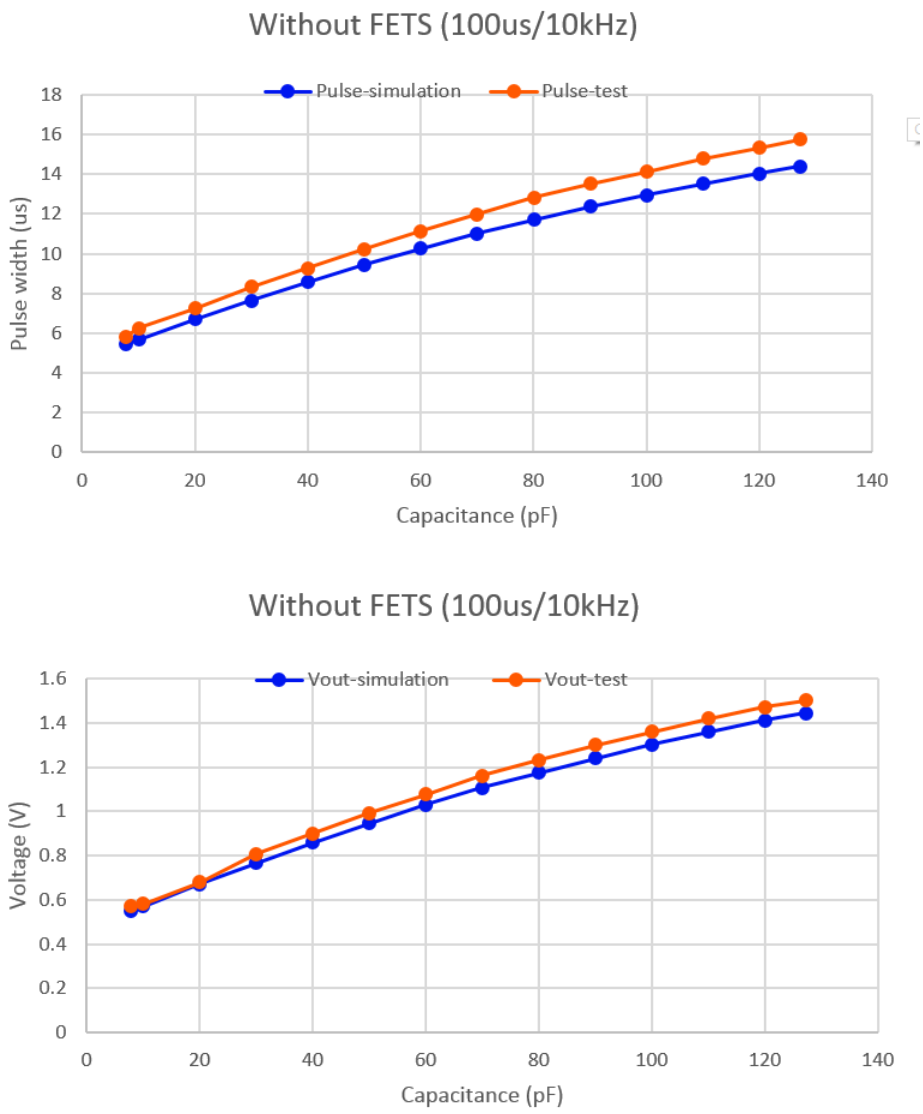

Figure 4.21 Plots of the traditional RC circuit with R=150kΩ at input frequency of 10kHz.
Up: PWM pulse width versus capacitance;
Down: DC voltage level versus capacitance.

Table 4.8 Results for the traditional RC circuit with R=150kΩ at input frequency of 16.67kHz.

	Capacitance (pF)	Pulse-simulation (us)	Pulse-test (us)	Vout-simulation (V)	Vout-test (V)
C1	127.25	10.84	12.16	1.815	1.9
C2	120	10.67	11.99	1.789	1.87
C3	110.06	10.43	11.67	1.747	1.84
C4	100.02	10.15	11.29	1.702	1.8
C5	90.02	9.86	10.98	1.652	1.74
C6	80.06	9.53	10.59	1.596	1.69
C7	69.97	9.14	10.19	1.531	1.62
C8	60.02	8.71	9.61	1.46	1.55
C9	50.02	8.23	9.04	1.375	1.47
C10	40	7.65	8.5	1.282	1.38
C11	30	7.03	7.73	1.176	1.258
C12	20	6.31	7.12	1.056	1.094
C13	10.02	5.5	6.14	0.921	0.956
C14	7.83	5.31	5.81	0.888	0.937

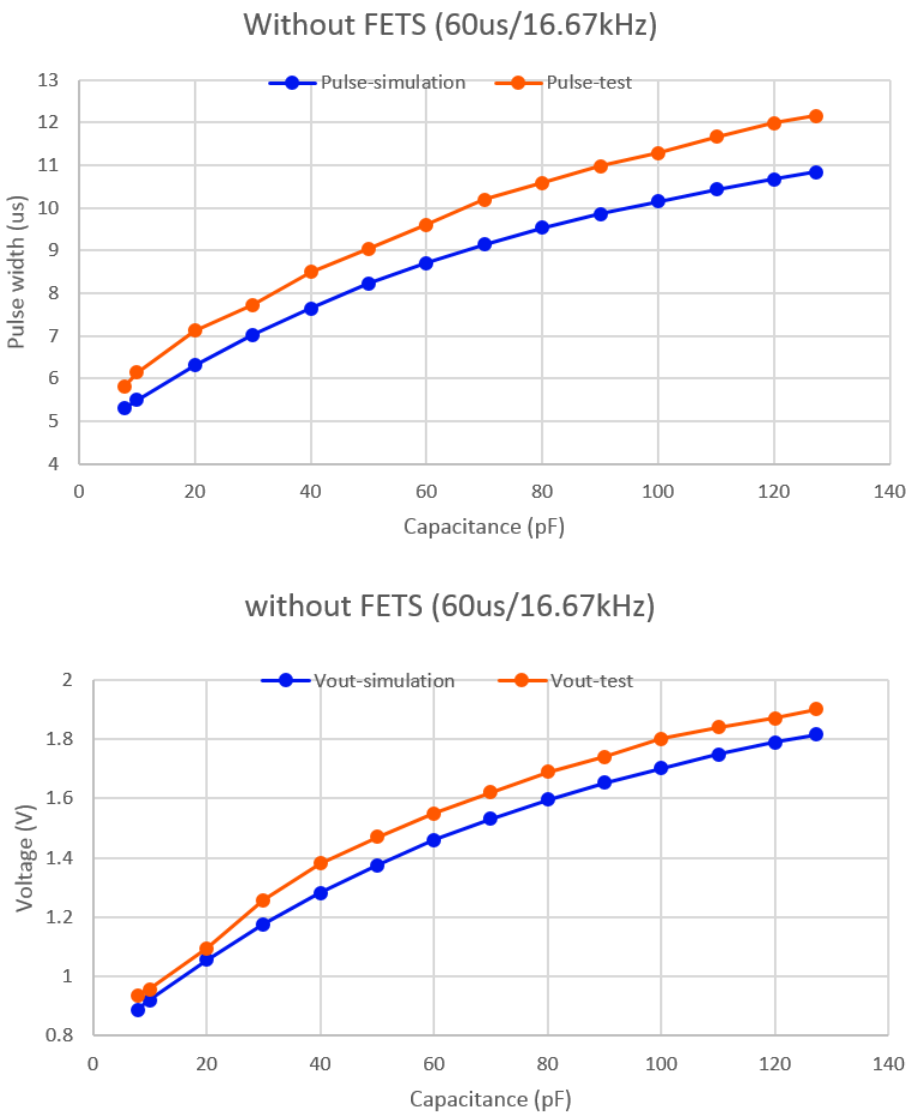

Figure 4.22 Plots of the traditional RC circuit with R=150kΩ at input frequency of 16.67kHz.
Up: PWM pulse width versus capacitance;
Down: DC voltage level versus capacitance.

5. RESISTANCE SWITCHING CIRCUIT

5.1 Circuit design

Since the key to expanding the range of linear response of the RC phase delay interface circuit is to accelerate the capacitor charging and discharging progress as soon as the voltage across the sensor capacitor reaches the inverter trip voltage, instead of manipulating the process using MOSFET switches to pull the voltage up and down, also inspired by the Equation (3.4), it can be achieved by changing the resistance R from originally large to very small so that $t_{0.5}$ is greatly shortened at that time point.

The first attempt was made to replace the resistor with a DS1866 log trimmer potentiometer [41] which has three-digit 8-position binary input and the attenuation is 35dB when the input is 000 and 0dB for the input of 111. Since its standard resistance is $10\text{k}\Omega$, the digital potentiometer is $10\text{k}\Omega$ at 000 and 177.83Ω at 111. When a proper logic circuit is applied to input all 1's/high when acceleration is needed and all 0's/low for the rest, this seems ideal for the new idea. Unfortunately, however, this did not work as desired because its highest resistance level of $10\text{k}\Omega$ is too small so that the feedback PWM pulse width was too narrow to trigger a switch of resistance due to the slow response of the digital pot. In other words, the digital pot was so slow that it never switched

to its low resistance. As this model was the only commercial digital pot not requiring a microcontroller to control it that could be found, this idea seemed to be nonrealistic.

However, the equivalent circuit model (Figure 5.1) designed in the LTSpice software gives another inspiration to build a circuit exactly like the equivalent one. Replacing the ideal voltage controlled switch with a commercial CMOS low voltage 2Ω analog switch of ADG701 by Analog devices [42], the larger resistance of $270\text{k}\Omega$ can be "shorted" by turning the analog switch on when acceleration of charging or discharging is needed. Observe that, back to Figure 4.3, acceleration is needed when "Input_1" and "Input_2" are both high or both low. Therefore, a logic circuit consisting of a NOR gate, an AND gate and an OR gate is built which inputs a high voltage to switch on the analog switch when "Input_1" and "Input_2" are in the same state and inputs a 0 voltage to switch it off otherwise.

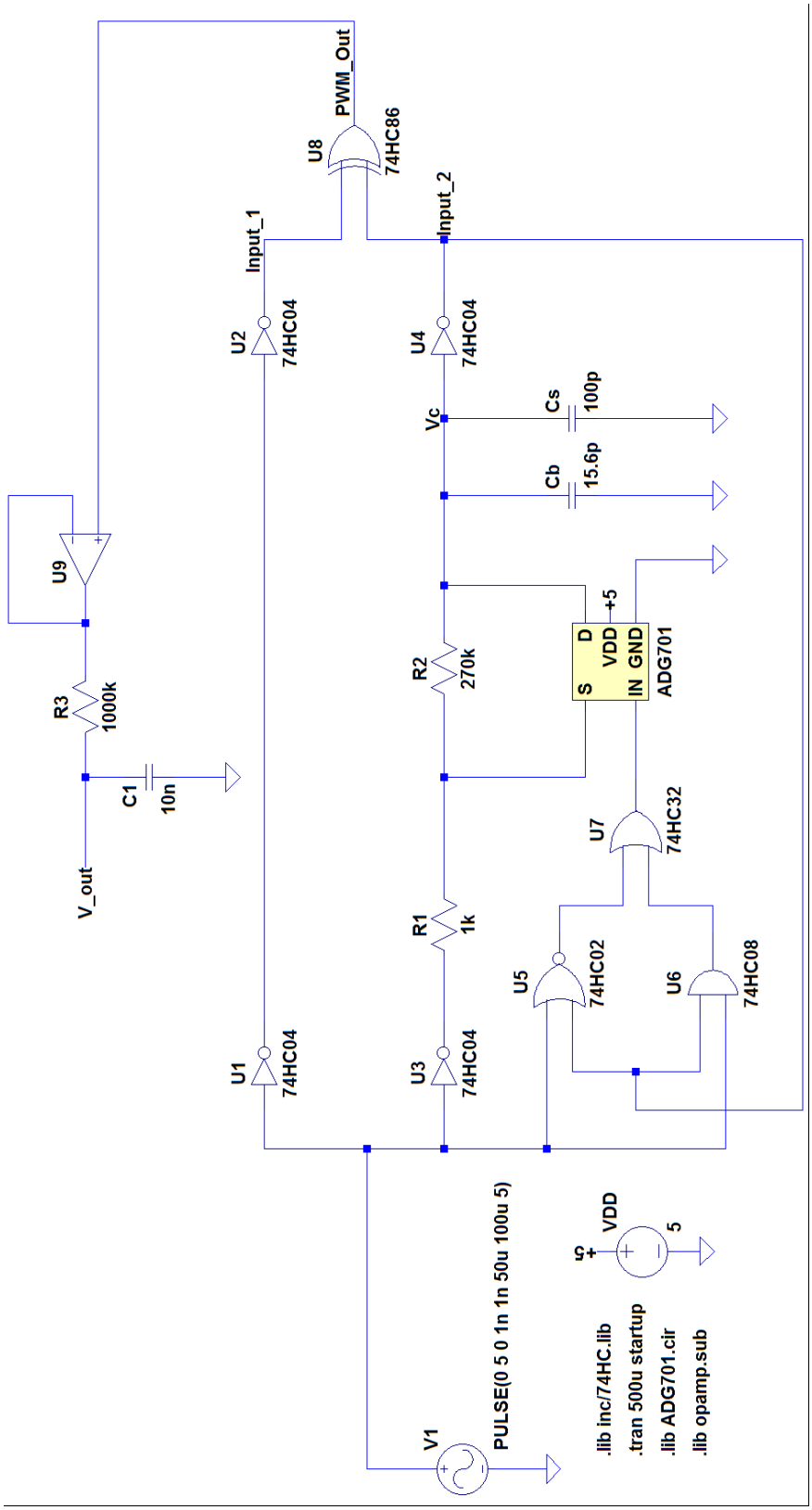

Figure 5.1 Schematic of the resistance switching interface circuit.

5.2 Circuit simulation

Figure 5.2 depicts the LTSpice simulation result of the novel resistance switching interface circuit. Notice that though the sensor capacitance is the same 100pF as that in Figure 4.3, the PWM duty cycle is wider because “Vc” has sharp fully charging and fully discharging every time it reaches the trip voltage which leaves a great potential for expanding the effective phase delay with the approximately 180° linear range instead of only about 1⁄4 of it.

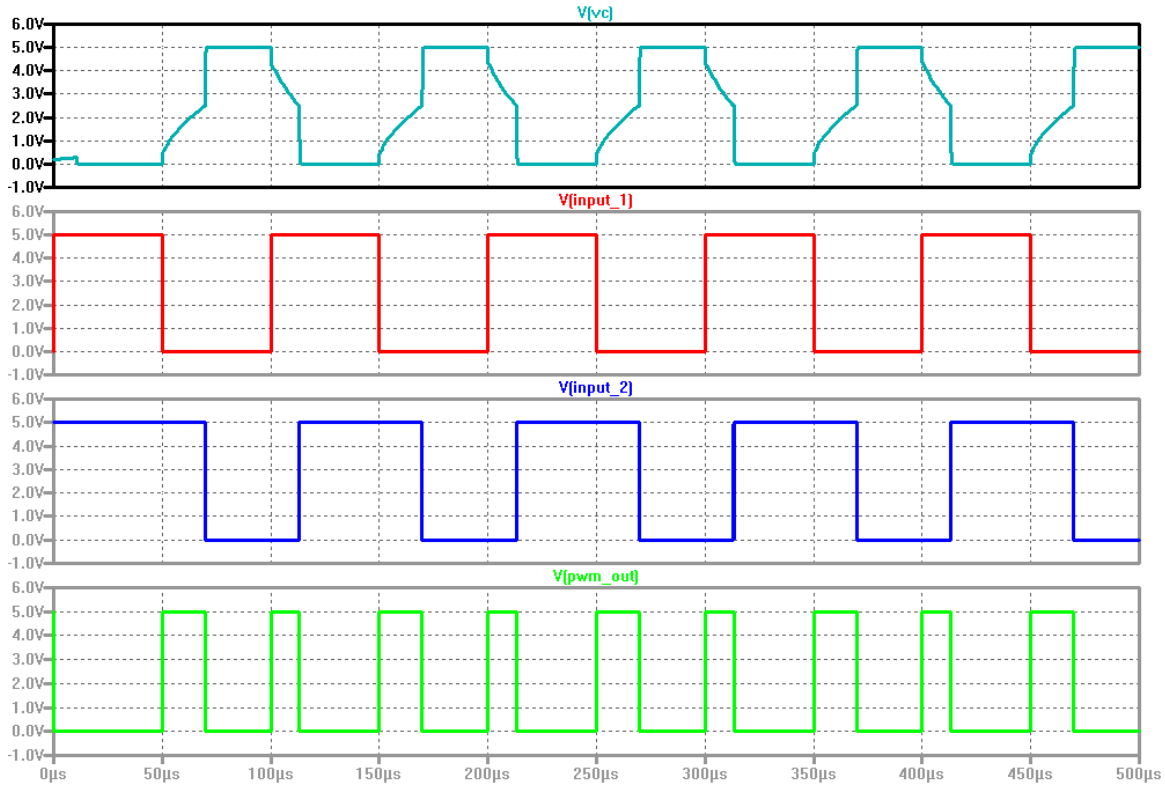

Figure 5.2 Simulation result of the resistance switching RC phase delay interface circuit with the sensor capacitance of 100pF and the input frequency of 10kHz.

A low pass filter is also applied to convert the PWM output into a DC voltage (Figure 5.1). After running a transient simulation for 200ms, or 20,000 periods, a plot indicating the DC voltage is given in Figure 5.3.

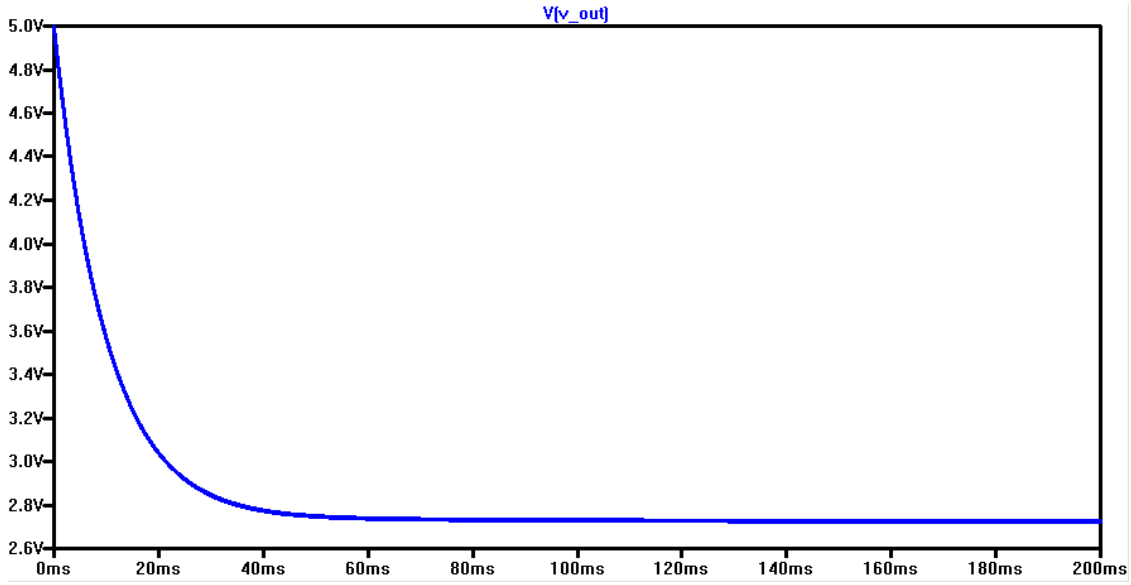

Figure 5.3 Simulation result of the resistance switching RC phase delay interface circuit for the PWM converted to DC voltage with the sensor capacitance of 100pF and the input frequency of 10kHz.

5.3 Circuit implementation

The prototype of the 5V resistance switching interface circuit was built on a breadboard (Figure 5.4) using two MC14049 CMOS inverter ICs, an MC14001 CMOS NOR gate, an HEF4081 AND gate, an HEF4071 OR gate and an ADG701 analog switch.

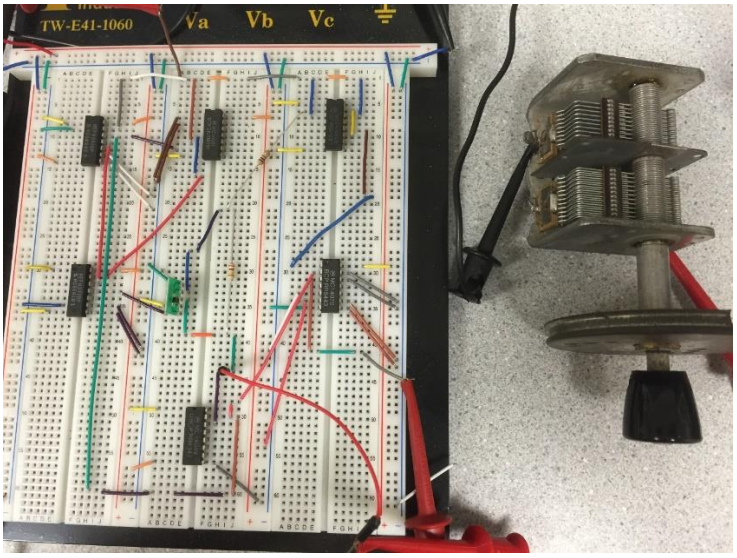

Figure 5.4 Resistance switching interface circuit prototype on a bread board.

The resistor for the core RC network is a $270\text{k}\Omega$ film resistor (Figure 5.5, left side) in series with an $1\text{k}\Omega$ film resistor (Figure 5.5, right side) and a variable mechanical multi-plate capacitor (Figure 4.9) with a range of approximately $8\text{pF} - 128\text{pF}$ is used to simulate the sensor capacitor C_s since the range is typical for small capacitance sensing.

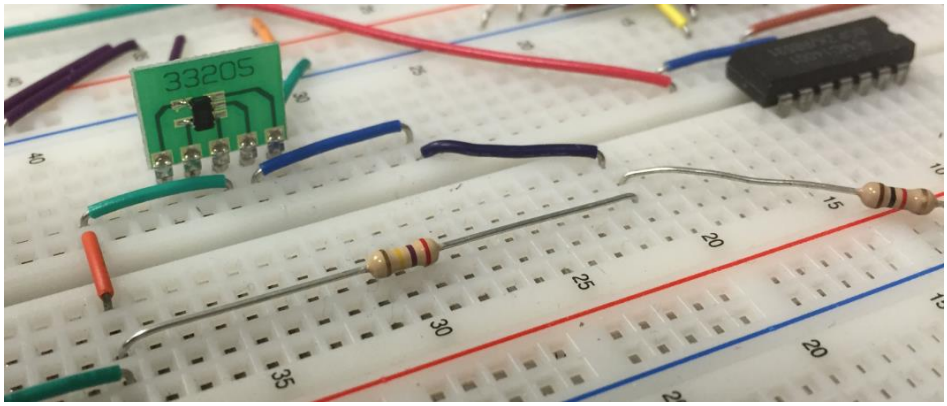

Figure 5.5 A zoomed-in photograph of the analog switch of ADG701 and the resistor of 270kΩ in series with the resistor of 1kΩ.

5.4 Circuit testing

Similar to what was done to test the MOSFET interface circuit, setting the variable capacitor as the maximum capacitance that is measured by the LCR meter as 127.6pF, the maximum frequency for the input square wave turns out to be 16.67kHz or the minimum period is $60\mu\text{s}$ as well.

As comparisons, lower frequencies of 10kHz ($100\mu\text{s}$) and 5kHz ($200\mu\text{s}$), along with the maximum frequency, are used both on the resistance switching circuit and the traditional RC phase delay circuit with the resistance to be $270\text{k}\Omega$ and $1\text{k}\Omega$ in series built on the breadboard as well. Figure 5.6-5.8 show oscilloscope plots of the waveforms and measurements at frequencies of 5kHz, 10kHz, 16.67kHz respectively, in all of

which the yellow waveforms are probed at “PWM_Out”, the green at “Input_2”, the blue at “Input_1” and the red at “V_out” (nodes marked in Figure 5.1). Also, the width of the PWM and the RMS of the DC output are measured and saved in each measurement. Though these three sets of plots only include waveforms with the maximum capacitance and the minimum, from which it is already clear that both the PWM duty cycle and the DC voltage level decrease as the capacitance decreases and the PWM duty cycle has the best use of the phase delay range at the maximum frequency, the tests are performed by changing the variable capacitor in steps of $10pF$ between the maximum and minimum values and detailed sets of data are plotted and analyzed in the next section.

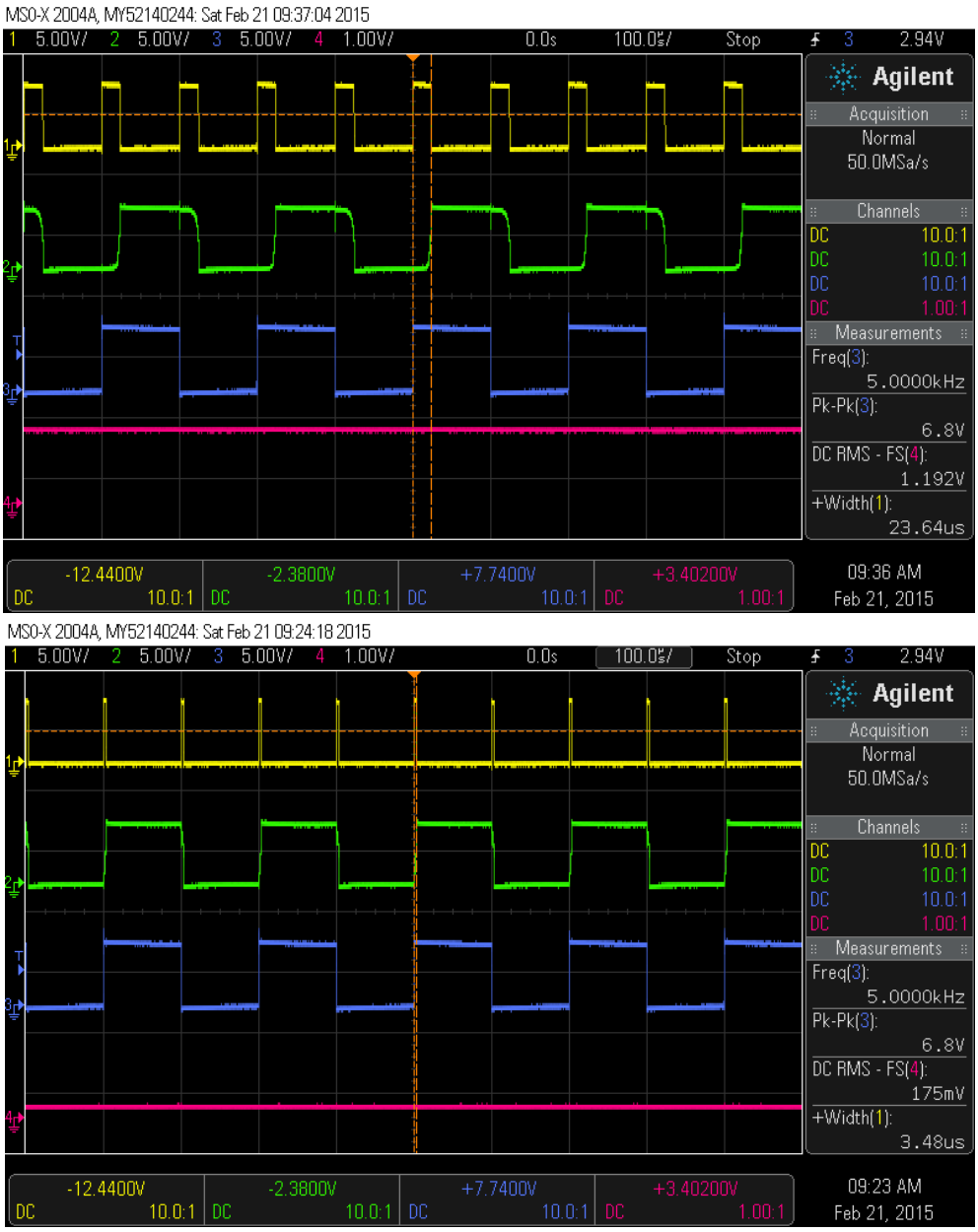

Figure 5.6 Oscilloscope plot of test result at input frequency of 5kHz.

Up: capacitance is 127.6pF as maximum;

Down: capacitance is 7.89pF as minimum.

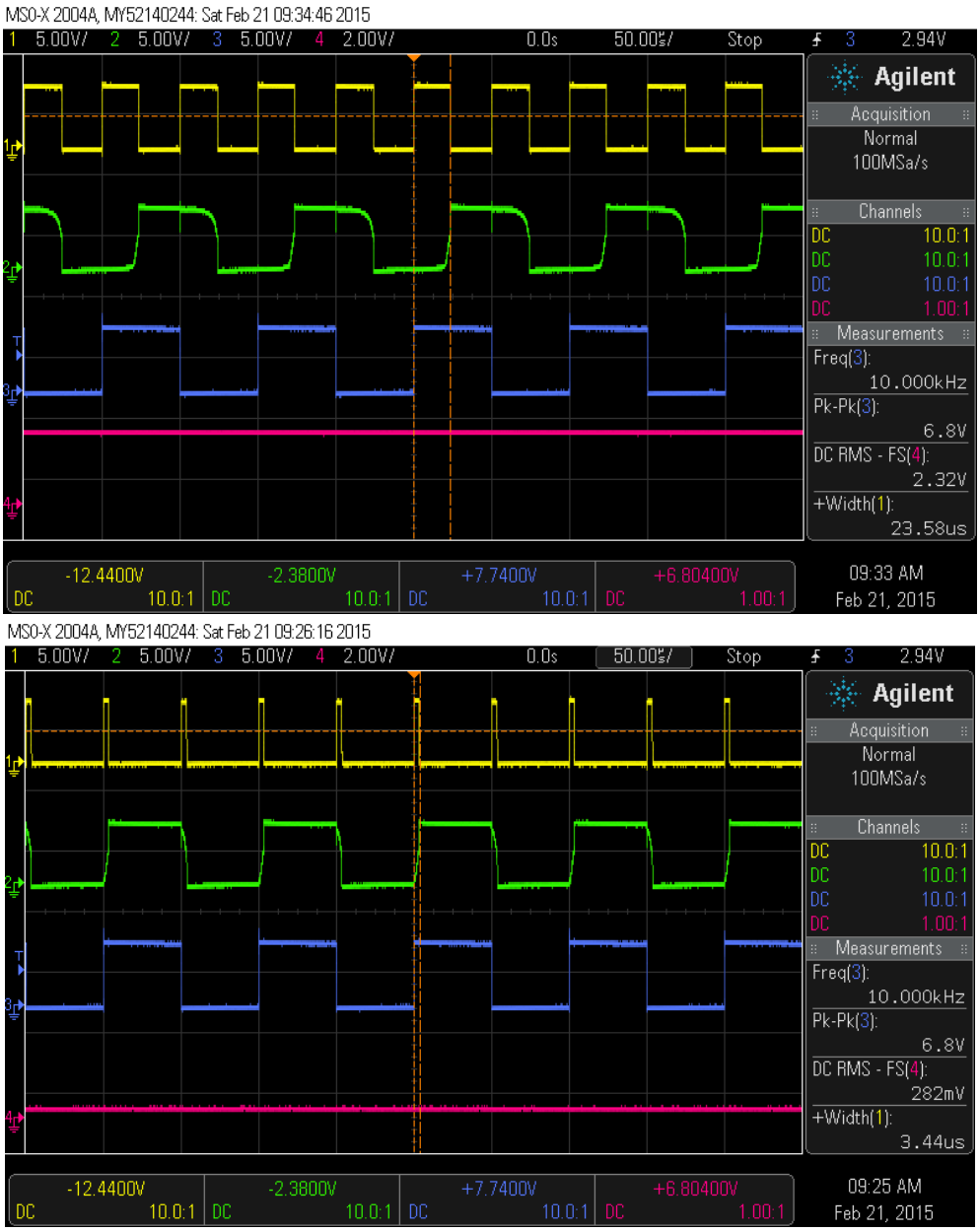

Figure 5.7 Oscilloscope plot of test result at input frequency of 10kHz.

Up: capacitance is 127.6pF as maximum;

Down: capacitance is 7.89pF as minimum.

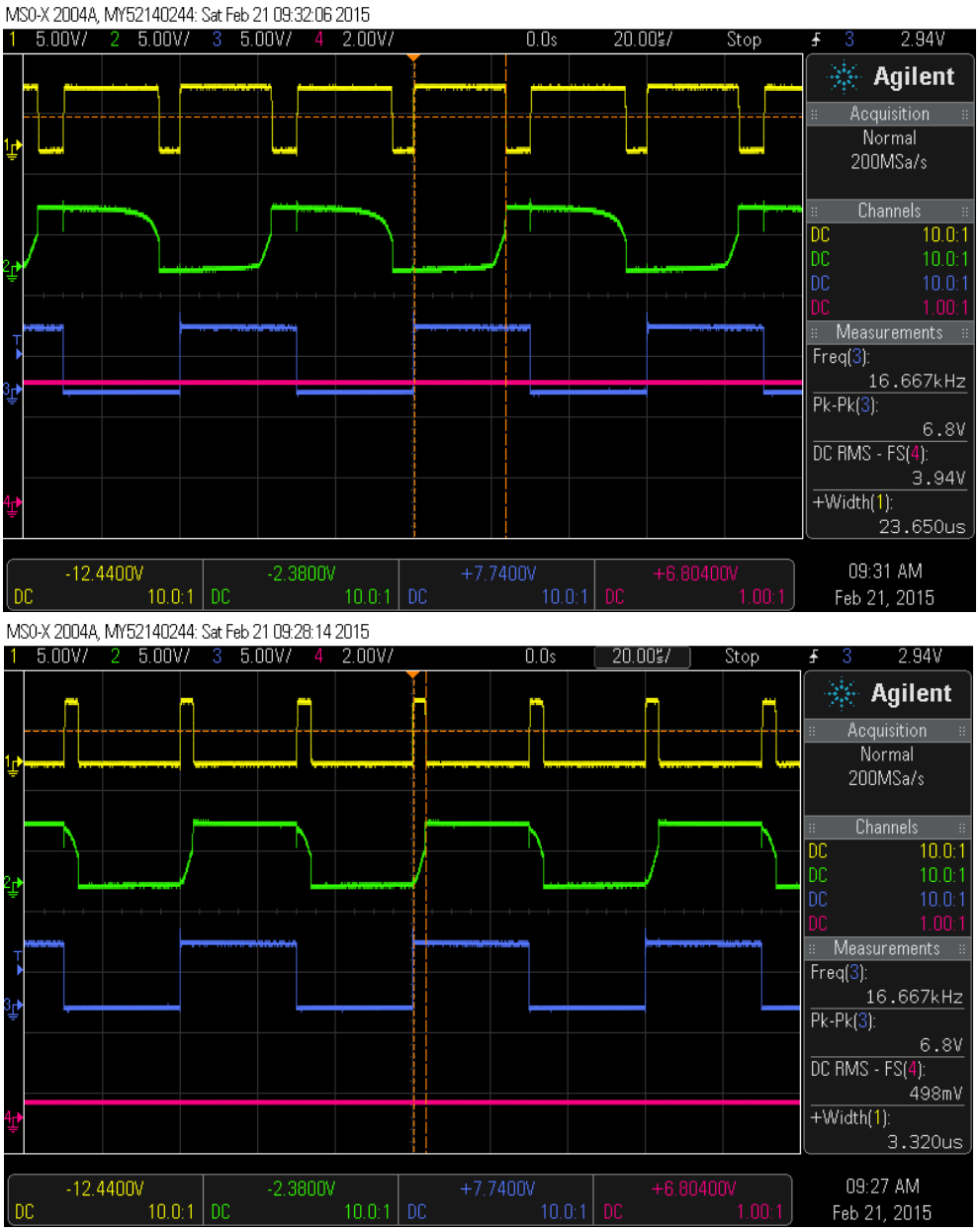

Figure 5.8 Oscilloscope plot of test result at input frequency of 16.67kHz.
Up: capacitance is 127.6pF as maximum;
Down: capacitance is 7.89pF as minimum.

5.5 Results

Take the test at the input frequency of 5kHz as an example, the data of the PWM pulse width and the DC voltage level results from both the simulation and testing against

14 different capacitance values, minimum and maximum along with 12 other points between them with a step of approximately 10pF, is collected in Table 5.1 and plotted in Figure 5.9. The same procedure was used for the cases at the frequencies of 10kHz and 16.67kHz in Table 5.2 -5.3 and Figure 5.10-5.11, respectively.

As comparisons, the same method of experiment is applied on the traditional RC phase delay interface circuit without the analog switch with the logic components, whose schematic is shown back in Figure 4.1, at input frequencies of 5kHz, 10kHz and 16.67kHz, and sets of data are collected in Table 5.4-5.6 and plotted in Figure 5.12-5.14, respectively.

The results from both the simulation and the test turn out to prove that the resistance switching interface circuit works as expected to expand the linear response of the RC phase delay circuit. From Figure 5.9-5.11, along with the increase of frequency, plots from both the simulation (blue plots) and the test (orange plots) keep a good degree of linearity ($R^2 = 0.999$ for all simulations and $R^2 > 0.99$ for all tests) whether for PWM pulse width versus capacitance or DC voltage versus capacitance. Notice that, when increasing the frequency, not only does the linearity slightly improves, the range of change also covers more, whether for the PWM pulse width or the DC voltage, which is beneficial for more accurate reading. For example, at the maximum frequency of 16.67kHz, the DC voltage varies from 0.498V to 3.94V within the range of 5V, while it is from 0.175V to 1.192V at 5kHz.

As for the traditional interface circuit, however, the plots start to become apparently

nonlinear at 10kHz and become very nonlinear at 16.67kHz. Therefore, the novel resistance switching interface circuit is a good improvement to the traditional one. Specifically, the percentage of linear response range over the potential maximum phase delay range of 180° increases from 25% to 69% (increases by 44%). This result is limited by the variable capacitor we have and can be even larger if the range of the measured capacitance is larger.

Table 5.1 Results for the resistance switching circuit at input frequency of 5kHz.

	Capacitance (pF)	Pulse-simulation (us)	Pulse-test (us)	Vout-simulation (mV)	Vout-test (mV)
C1	127.6	24.38	23.64	1018.79	1192
C2	119.99	23.16	22.36	963.28	1120
C3	110.01	21.39	20.6	890.17	1039
C4	100.02	19.69	18.6	815.92	938
C5	90.02	18.1	16.92	742.76	852
C6	80.05	16.44	15.24	672.84	750
C7	70	14.76	13.36	599.5	667
C8	60.03	13.13	11.68	528.57	578
C9	50	11.36	10	453.36	493
C10	40.01	9.77	8.72	383.32	424
C11	30.01	8.1	6.84	315.29	342
C12	20	6.59	5.28	245.08	261
C13	10	4.96	3.92	175.18	191
C14	7.89	4.55	3.48	159.13	175

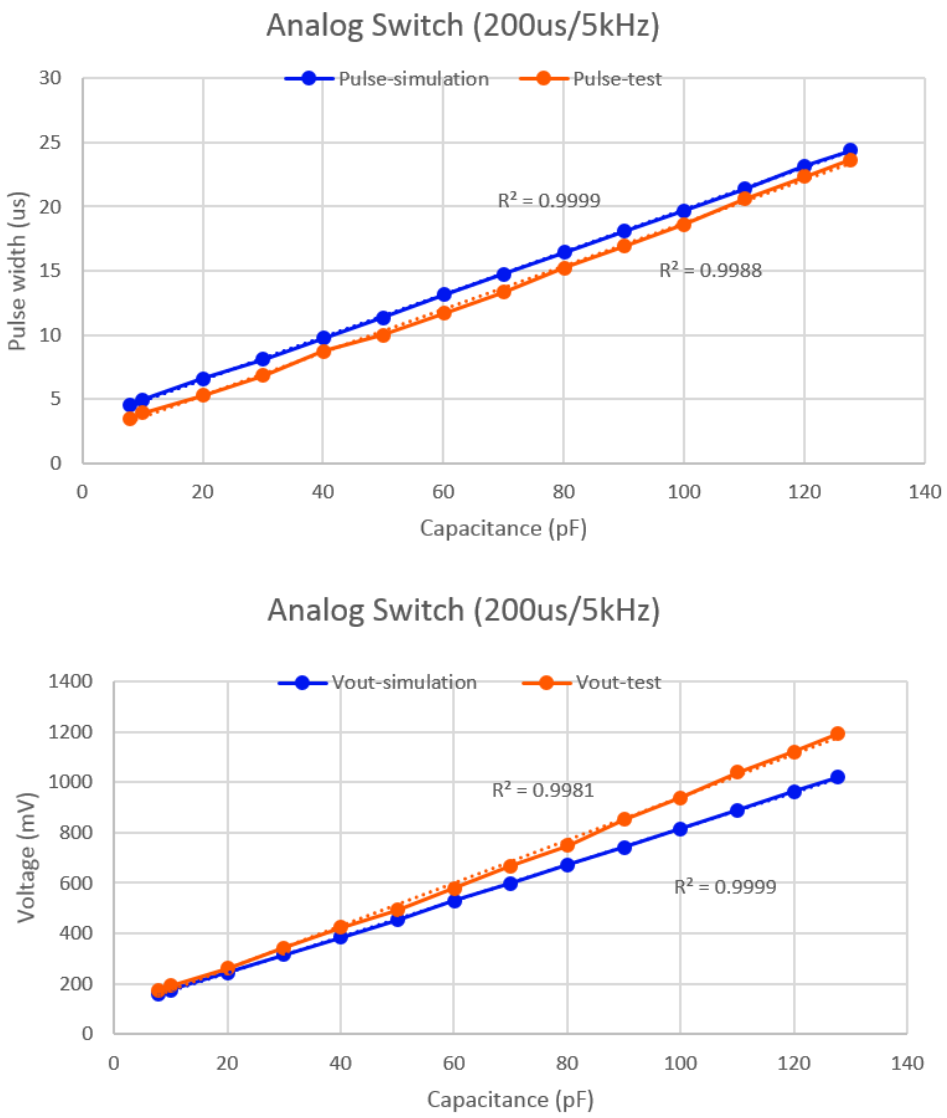

Figure 5.9 Plots of the resistance switching circuit at input frequency of 5kHz.
Up: PWM pulse width versus capacitance;
Down: DC voltage level versus capacitance.

Table 5.2 Results for the resistance switching circuit at input frequency of 10kHz.

	Capacitance (pF)	Pulse-simulation (us)	Pulse-test (us)	Vout-simulation (V)	Vout-test (V)
C1	127.6	24.38	23.58	2.041	2.32
C2	119.99	23.12	22.24	1.93	2.21
C3	110.01	21.42	20.36	1.783	2.02
C4	100.02	19.71	18.48	1.635	1.82
C5	90.02	18.08	16.84	1.488	1.65
C6	80.05	16.47	15.04	1.348	1.47
C7	70	14.77	13.4	1.202	1.267
C8	60.03	13.13	11.76	1.059	1.1
C9	50	11.35	10.16	0.908	0.928
C10	40.01	9.77	8.76	0.768	0.777
C11	30.01	8.18	6.96	0.633	0.618
C12	20	6.58	5.24	0.491	0.456
C13	10	4.908	3.86	0.351	0.31
C14	7.89	4.551	3.44	0.318	0.282

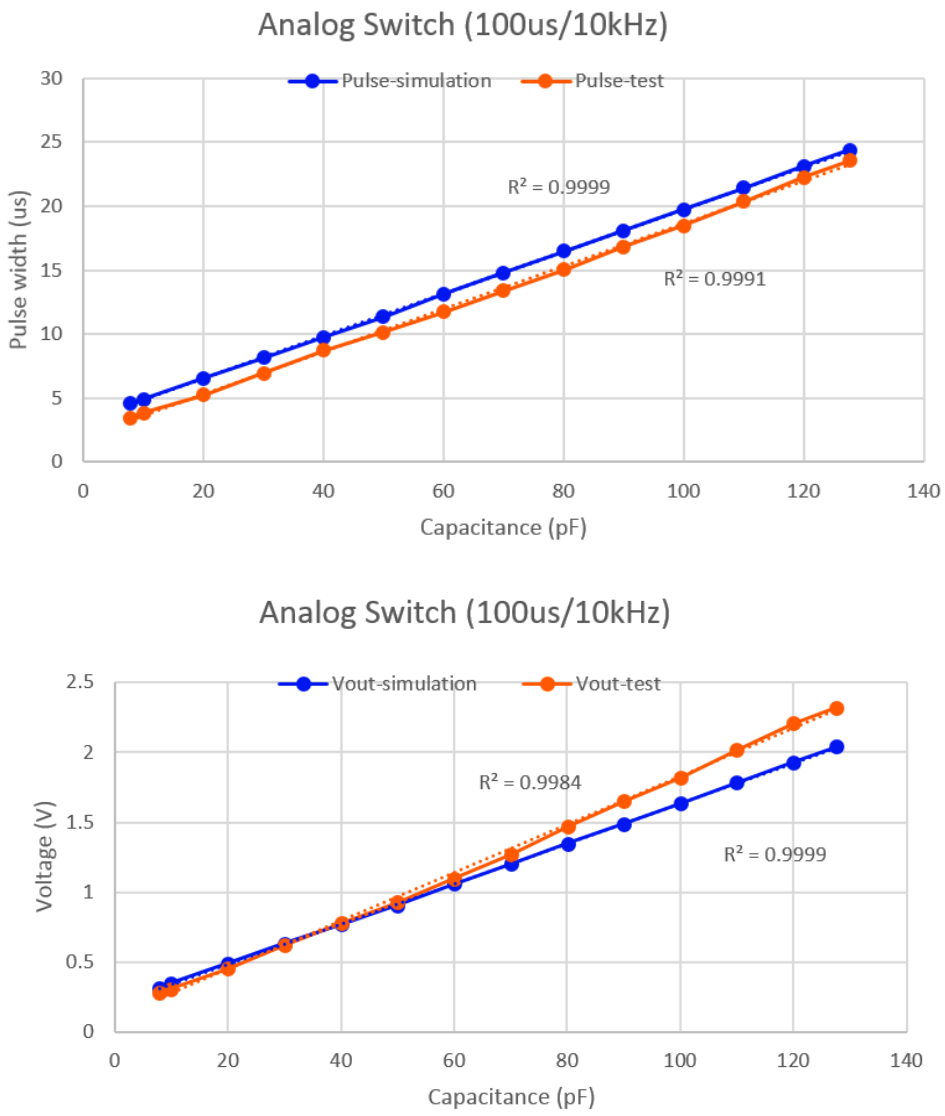

Figure 5.10 Plots of the resistance switching circuit at input frequency of 10kHz.
Up: PWM pulse width versus capacitance;
Down: DC voltage level versus capacitance.

Table 5.3 Results for the resistance switching circuit at input frequency of 16.67kHz.

	Capacitance (pF)	Pulse-simulation (us)	Pulse-test (us)	Vout-simulation (V)	Vout-test (V)
C1	127.6	24.4	23.65	3.41	3.94
C2	119.99	23.11	22.02	3.22	3.69
C3	110.01	21.44	20.4	2.97	3.42
C4	100.02	19.71	18.5	2.73	3.1
C5	90.02	18.01	16.77	2.48	2.78
C6	80.05	16.46	15.03	2.25	2.47
C7	70	14.77	13.39	2	2.21
C8	60.03	13.13	11.69	1.76	1.89
C9	50	11.36	10.09	1.51	1.6
C10	40.01	9.77	8.6	1.27	1.36
C11	30.01	8.18	6.92	1.03	1.09
C12	20	6.59	5.32	0.818	0.819
C13	10	4.96	3.84	0.585	0.584
C14	7.89	4.56	3.32	0.531	0.498

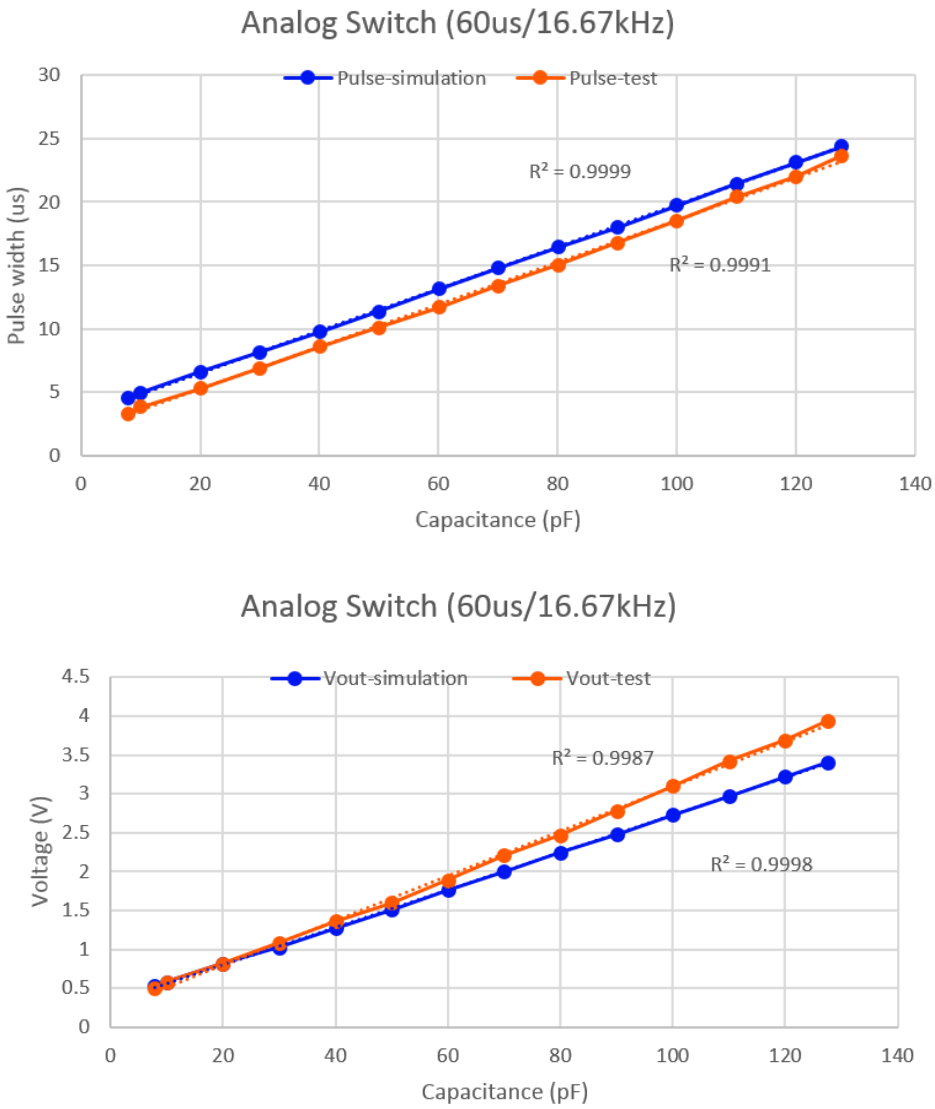

Figure 5.11 Plots of the resistance switching circuit at input frequency of 16.67kHz.
Up: PWM pulse width versus capacitance;
Down: DC voltage level versus capacitance.

Table 5.4 Results for the traditional RC circuit with R=271kΩ at input frequency of 5kHz.

	Capacitance (pF)	Pulse-simulation (us)	Pulse-test (us)	Vout-simulation (V)	Vout-test (V)
C1	127.28	26.76	30.16	1.349	1.4
C2	119.99	26.06	29.08	1.31	1.36
C3	110	24.98	28.08	1.257	1.31
C4	100.01	23.82	26.72	1.198	1.256
C5	90.01	22.59	25.44	1.138	1.19
C6	80	21.26	23.96	1.071	1.13
C7	70.02	19.88	22.4	1	1.054
C8	60.01	18.36	20.72	0.924	0.974
C9	50.03	16.79	18.8	0.844	0.889
C10	39.99	15.12	17.08	0.759	0.812
C11	30	13.4	15.32	0.673	0.722
C12	20	11.6	13.12	0.581	0.624
C13	10.03	9.77	11.36	0.49	0.541
C14	7.94	9.38	10.64	0.471	0.523

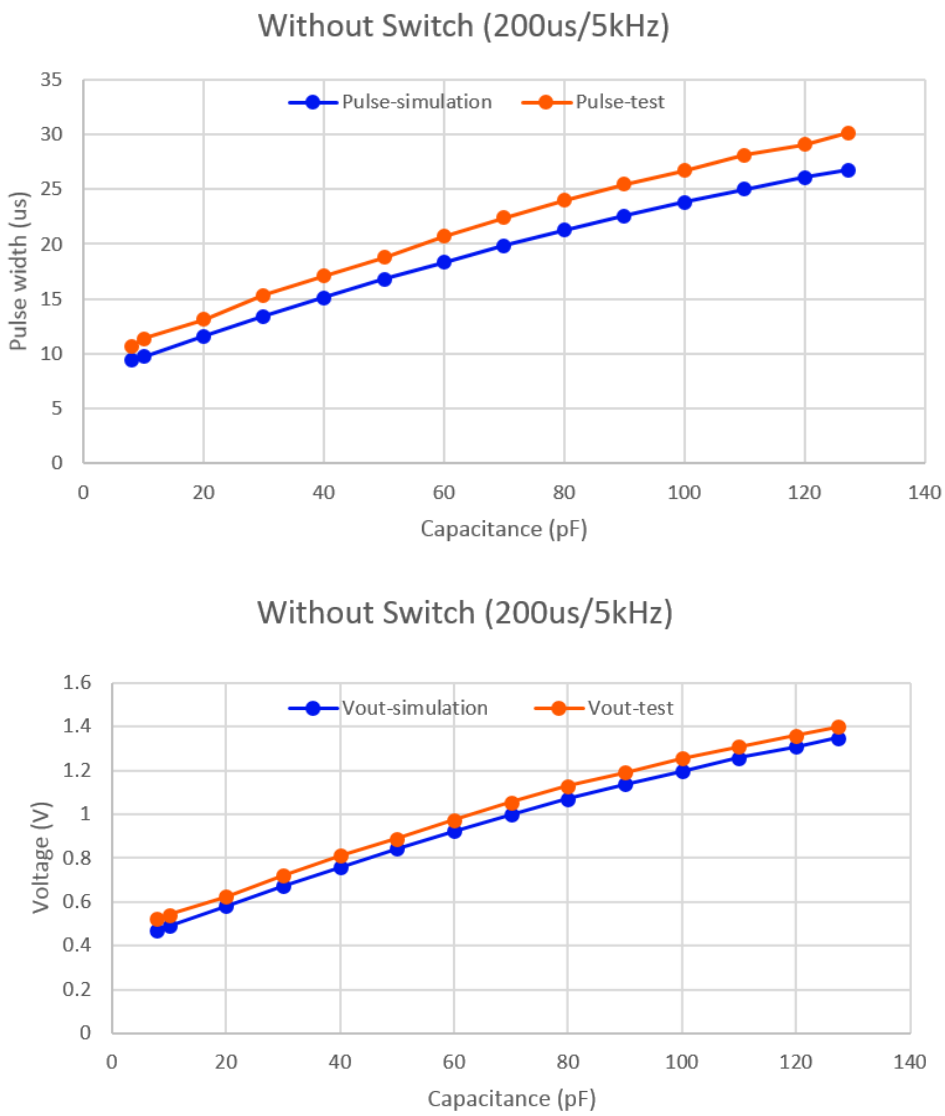

Figure 5.12 Plots of the traditional RC circuit with R=271kΩ at input frequency of 5kHz.
Up: PWM pulse width versus capacitance;
Down: DC voltage level versus capacitance.

Table 5.5 Results for the traditional RC circuit with R=271kΩ at input frequency of 10kHz.

	Capacitance (pF)	Pulse-simulation (us)	Pulse-test (us)	Vout-simulation (V)	Vout-test (V)
C1	127.28	18.39	21.34	1.853	1.93
C2	119.99	18.14	20.98	1.827	1.9
C3	110	17.75	20.46	1.787	1.87
C4	100.01	17.3	20.06	1.745	1.84
C5	90.01	16.8	19.52	1.696	1.79
C6	80	16.25	18.86	1.638	1.74
C7	70.02	15.62	18.08	1.572	1.67
C8	60.01	14.9	17.28	1.5	1.61
C9	50.03	14.09	16.16	1.418	1.52
C10	39.99	13.14	15.22	1.323	1.44
C11	30	12.05	14.02	1.211	1.33
C12	20	10.8	12.44	1.087	1.184
C13	10.03	9.38	10.92	0.942	1.055
C14	7.94	9.06	10.46	0.909	1.015

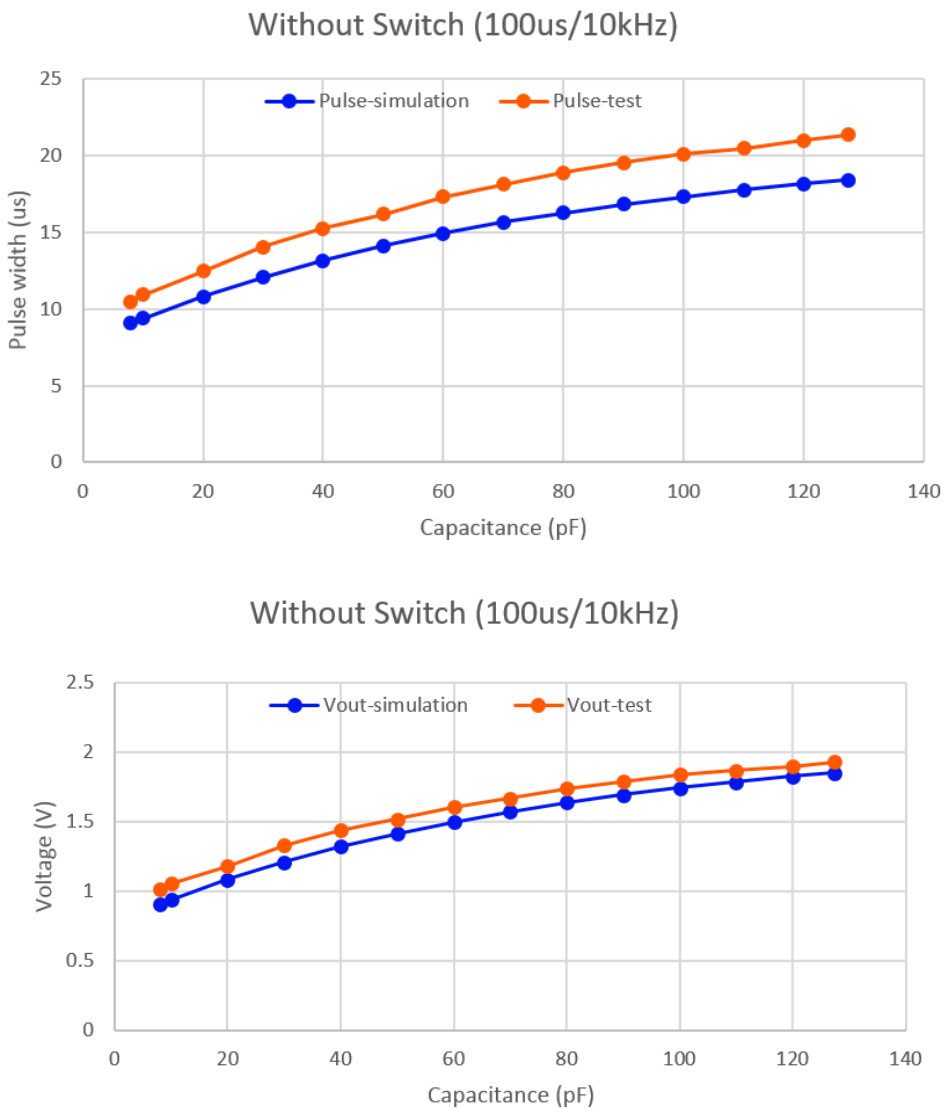

Figure 5.13 Plots of the traditional RC circuit with R=271kΩ at input frequency of 10kHz.
Up: PWM pulse width versus capacitance;
Down: DC voltage level versus capacitance.

Table 5.6 Results for the traditional RC circuit with R=271kΩ at input frequency of 16.67kHz.

	Capacitance (pF)	Pulse-simulation (us)	Pulse-test (us)	Vout-simulation (V)	Vout-test (V)
C1	127.26	12.93	13.53	2.1	2.27
C2	120	12.73	13.43	2.08	2.26
C3	110	12.47	13.25	2.06	2.25
C4	100.01	12.21	13.04	2.026	2.23
C5	90.01	11.94	12.83	1.993	2.21
C6	80	11.68	12.54	1.953	2.18
C7	70.02	11.38	12.15	1.909	2.15
C8	60.01	11.05	11.72	1.856	2.11
C9	50.03	10.69	11.45	1.795	2.07
C10	39.99	10.24	10.97	1.719	2.02
C11	30	9.69	10.45	1.628	1.94
C12	20	9.02	9.9	1.515	1.85
C13	10.03	8.18	9	1.371	1.74
C14	7.94	7.97	8.84	1.336	1.7

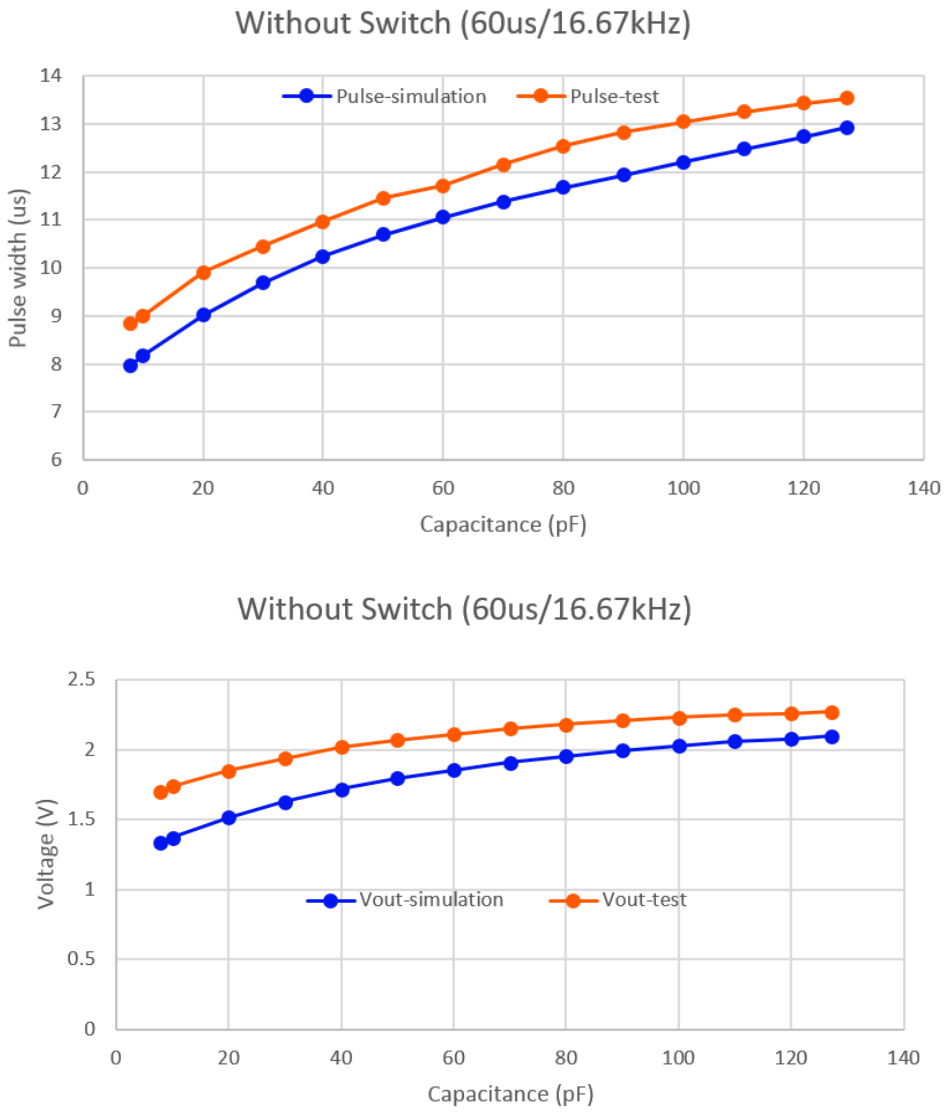

Figure 5.14 Plots of the traditional RC circuit with R=271kΩ at input frequency of 16.67kHz.
Up: PWM pulse width versus capacitance;
Down: DC voltage level versus capacitance.

5.6 Comparison with the MOSFET Circuit

To compare the performances of the MOSFET circuit and the resistance switching circuit, set the resistance of the MOSFET circuit RC network to be the resistor of 270kΩ in series with the resistor of 1kΩ (Figure 5.15), same as the resistance of the resistance switching network. Explore the maximum frequency and it turned out to be 10kHz. Therefore, with the same value of resistance and same scale of capacitance to measure, the resistance switching interface circuit has a higher operating frequency than that the MOSFET circuit could work at.

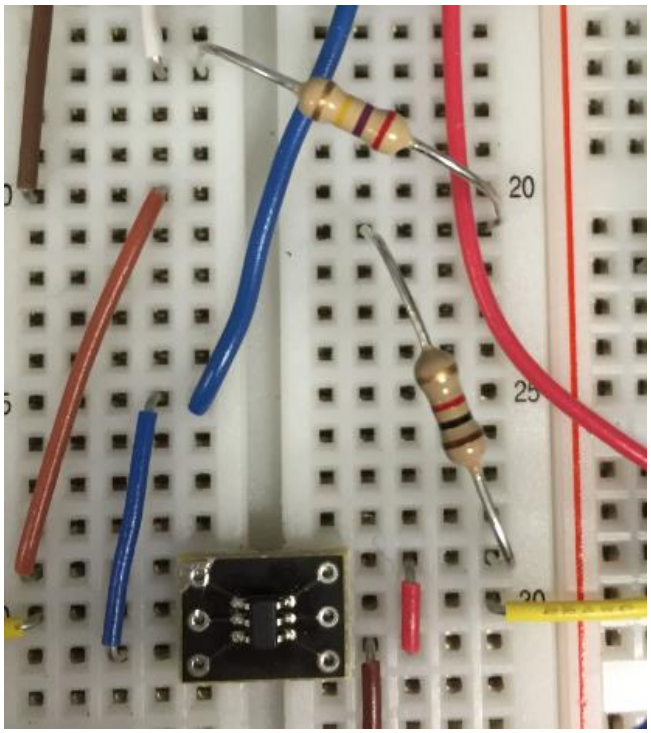

Figure 5.15 A zoomed-in photograph of the MOSFET of FDC6320C and the resistor of 270kΩ in series with the resistor of 1kΩ.

The sets of data are collected in Table 5.7 and plotted in Figure 5.16. Comparing the plots in Figure 5.16 with the ones in Figure 5.10, it can be seen that the MOSFET circuit provides a better linearity than the other method does. For the percent increase in phase

delay range over the 25% of the range useful in the traditional RC phase delay method, however, this MOSFET circuit gives a 39.8% which is still not as good as the 69% given by the resistance switching interface circuit.

Table 5.7 Results for the MOSFET circuit with R=271kΩ at input frequency of 10kHz

	Capacitance (pF)	Pulse-simulation (us)	Pulse-test (us)	Vout-simulation (V)	Vout-test (V)
C1	127.12	38.1	42.4	3.766	3.42
C2	120.05	36.71	40.52	3.63	3.27
C3	109.98	34.75	38.76	3.436	3.13
C4	100.02	32.77	36.38	3.243	2.96
C5	89.99	30.79	34.56	3.049	2.79
C6	80.01	28.83	32.78	2.855	2.65
C7	70	26.81	30.76	2.66	2.5
C8	60.01	24.83	28.52	2.465	2.29
C9	50	22.82	26.28	2.269	2.11
C10	40	20.83	24.28	2.072	1.96
C11	30.03	18.82	21.9	1.875	1.79
C12	20.04	16.82	20.06	1.676	1.63
C13	10	14.79	17.58	1.475	1.46
C14	7.5	14.29	17.22	1.425	1.43

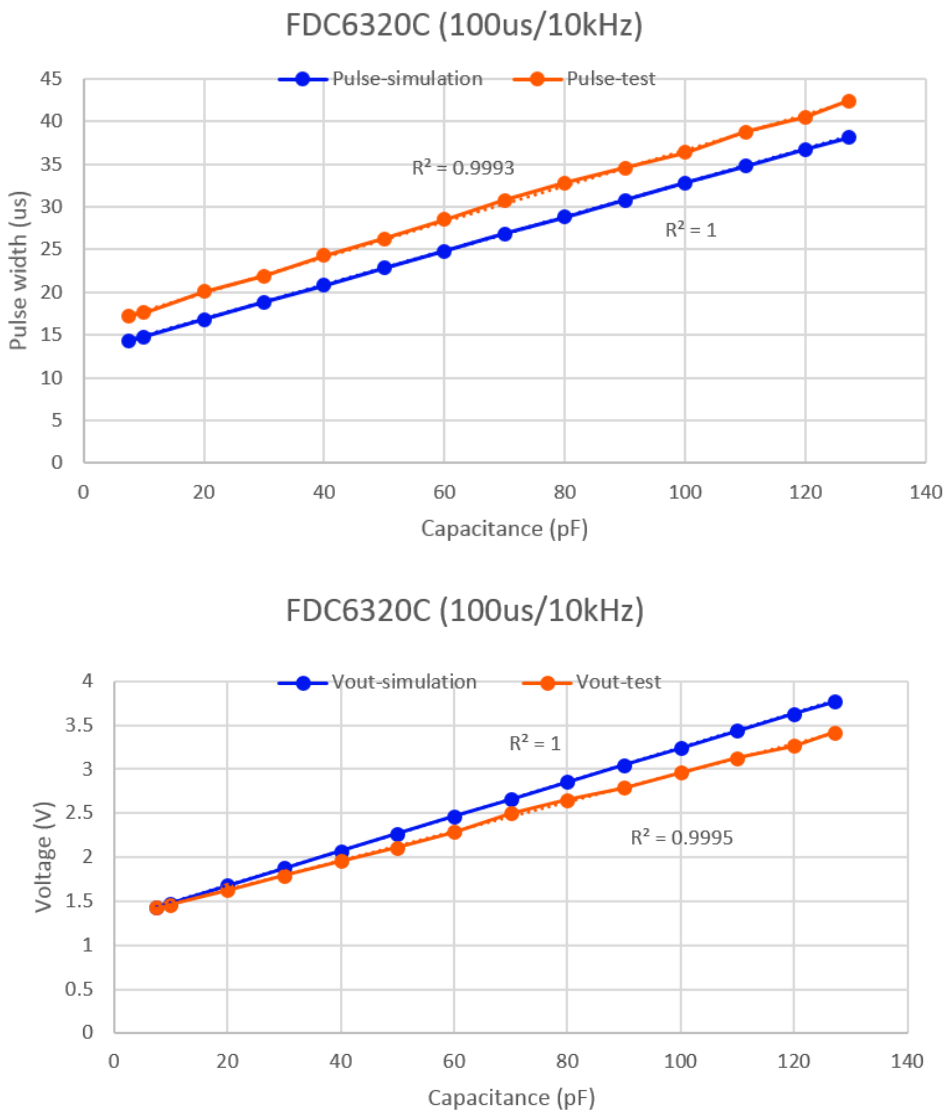

Figure 5.16 Plots of the MOSFET circuit with R=271kΩ at input frequency of 10kHz.
Up: PWM pulse width versus capacitance;
Down: DC voltage level versus capacitance.

6. SUMMARY AND CONCLUSION

In this thesis, a brief review of capacitive sensing techniques and typical interface circuits for capacitance measurement for MEMS technology is given, and the certain kind of phase delay interface circuit utilizing the time delay caused by an RC network, along with relative MOSFET technology, is specifically discussed.

The linear performance and limitation of the traditional RC phase delay interface circuit for capacitance sensing are analyzed and, based on which, two novel designs of advanced interface circuits, the MOSFET circuit and the resistance switching circuit, are presented. Both circuits are simulated in LTSpice software and tested on a breadboard. Both simulation and testing results prove that these advanced interface circuits greatly expand the linear range for capacitance measurement which the traditional RC phase delay circuit is severely limited at.

Compared with the traditional interface circuit, both advanced circuits have yielded measurements linearly proportional to the unknown capacitance at the same input frequency. Compared with each other, with the same resistance and unknown capacitance to measure, the resistance switching circuit can offer a higher maximum frequency and a larger percent in useful phase delay range, while the MOSFET circuit gives better linearity.

7. FUTURE WORK

More accurate tests can be done by building the prototype circuits on PCBs. Also, these advanced circuits can be integrated to real MEMS to test their performance. Additionally, these interface circuits could be tested with other capacitive sensors such as the PCB fringing field sensors.

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