Novel Interface Trap Passivation and Channel Counter-doping for 4H-SiC MOSFETs

by

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Abstract

4H-Silicon carbide (4H-SiC) is the most promising wide band gap semiconductor for next generation high power and high temperature metal-oxide-semiconductor field-effect transistors (MOSFETs). However, the channel mobility for as-grown oxide 4H-SiC is poor due to the high density of electronic traps near the SiO_2/4H-SiC interface. Nitric oxide (NO) post oxidation anneal increased 4H-SiC MOSFET mobility and allowed for commercially available devices. However, there is a limit to the amount of nitrogen that can passivate the electronic interface traps from nitric oxide passivation due to competing nitridation and oxidation reactions.

In the first part of this work, nitrogen plasma passivation, nitridation without oxidation, is explored as an alternative passivation process. Nitrogen plasma passivation is demonstrated to obtain a 50% increase in nitrogen coverage compared to standard NO. However the maximum field-effect mobility remains similar to NO. Explanations for this discrepancy are discussed.

Recent publications reported that nitrogen and phosphorus both passivate interface traps and counter-dope. To further examine these observations, the effects of antimony and arsenic at the interface were studied in this work. Antimony and arsenic are both in the same periodic column as nitrogen and phosphorus, but little is known about whether antimony and arsenic passivate electronic traps. Peak mobilities using several counter-doping processes are presented ($110 cm^2 V^{-1} s^{-1}$ for counter-doping combined with nitric oxide annealing). Evidence is also presented demonstrating that antimony does not passivate interface traps, thus improved field-effect mobility results from antimony are strictly from counter-doping effects.

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List of Abbreviations

As	Arsenic
BOE	Buffered oxide etch
C-Ψ_s	Capacitance-surface potential
CCDLTS	Constant-capacitance deep-level transient spectroscopy
Cs	Cesium
D_{it}	Density of interface traps
DI	Demineralized
DLTS	Deep-level transient spectroscopy
DMOSFET	Double-implanted metal-oxide-semiconductor field-effect transistor
Hi-lo C-V	Simultaneous high-low capacitance-voltage
I_{580}	Intensity of 580.4nm wavelength
LPCVD	Low-pressure chemical vapor deposition

Mo	Molybdenum
MOS	Metal-oxide-semiconductor
MOSFET	Metal-oxide-semiconductor field-effect transistor
N_{it}	Number of interface traps
NO	Nitric oxide
POA	Post-oxidation anneal
PSG	Phosphosilicate glass
RCA	Radio Corporation of America
Sb	Antimony
SCM	Scanning capacitance microscopy
SiC	Silicon carbide
SIMS	Secondary ion mass spectroscopy
SRIM	Stopping and range of ions in matter
TCE	Trichloroethylene
TEOS	Tetraethylorthosilicate
WBG	Wide bang gap
XPS	X-ray photoelectron spectroscopy

Chapter 1. Introduction

1.1 Power electronics and wide band gap semiconductors

Power electronics encompasses a vast array of solid-state electronic devices that control electrical energy. Approximately 30% of energy used in the United States passes through at least one power electronics device at some point between generation and consumption [1]. Forecasts by researchers at Oak Ridge National Laboratory expect this percentage to grow to 80% by 2030 [1]. Power electronics are found in many everyday appliances: cell phones, computers, automobiles, motors, air conditioning/heating units, and power line transformers. They are critical in converting solar, wind, and hydro energy into electricity.

As power electronics becomes more and more important for society, higher efficiency devices are becoming increasingly important because they are both environmentally friendly and cost effective. Increasing the efficiency of power electronics in cars has significant advantages. Lux Research Inc. found that a 20% increase in power savings translates to $6000 or more savings in battery costs for the new Tesla Model S electric car [2]. More efficient power electronics can also reduce up to 90% of power loss during AC-to-DC and DC-to-AC conversions [3].

Most early power electronics devices have been silicon-based technologies. However, silicon technology is approaching the theoretical limits for maximum operating temperature, miniaturization, and switching frequency. In addition, silicon's low thermal conductivity limits heat transfer, making it necessary for cooling system implementation.

Power electronics devices can be made more efficient when silicon is replaced with wide band gap (WBG) semiconductors such as GaN, SiC, or diamond. The intrinsic properties of WBG semiconductors are superior to current silicon-based power electronics devices. Compared to other WBG semiconductors, silicon carbide (SiC) has the advantage that, like silicon, it can grow a native oxide [4]. Not only is SiO_2 a very good insulating oxide, but band alignments between SiO_2 and SiC are suitable for metal-oxide-semiconductor (MOS) devices (Figure 1-1). Furthermore, for commercial manufacturing, many silicon foundries can be readily converted for SiC device processing [5].

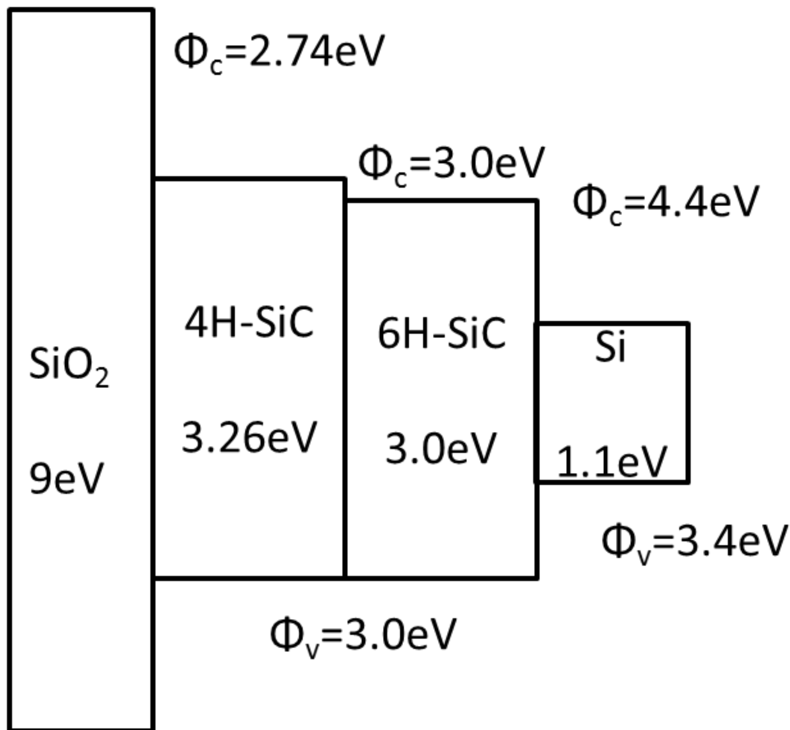

Figure 1-1. Band gap comparison of 4H-SiC, 6H-SiC, and silicon [6-7]. Φ_C is the potential difference between the bottom of the semiconductor conduction band and the bottom of the SiO_2 conduction band. Φ_V is the potential difference between the top of the semiconductor valence band and the top of the SiO_2 valence band.

Silicon carbide has more than a hundred poly-types, but only three are commercially viable at this point. SiC crystals grow in layers, and as these layers stack upon each other, they form certain patterns. The poly-type nomenclature is derived from these patterns. The three commercially viable poly-types are 4H, 6H, and 3C. The letters H and C designate the shape of the crystalline structure: H for hexagonal; C for cubic. The poly-types are denoted by a number indicating how many layers are stacked before repeating. An example of this can be seen in Figure 1-2. Figure 1-2 is a 4H stacking order, as can be seen by the a-b-c-b stacking pattern.

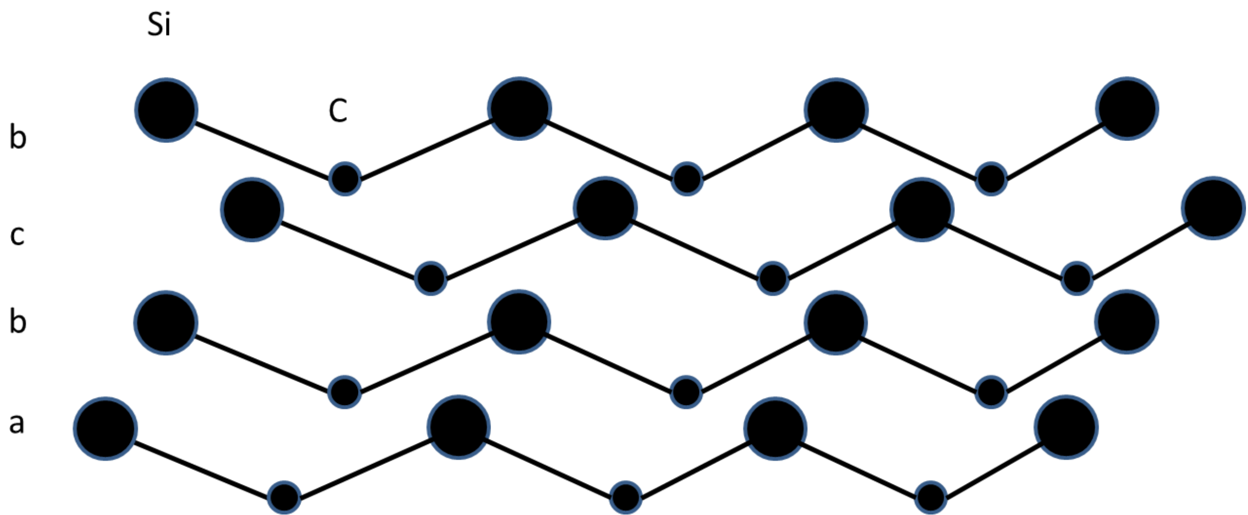

Figure 1-2. Stacking layer pattern for 4H-SiC.

4H-SiC was selected for this study because it has the largest band gap among the three poly-types and the highest bulk electron mobility. 6H-SiC has a higher anisotropy in mobility making it less favorable than 4H for vertical power devices (Mobility will be further discussed in Chapter 2). For these reasons, 4H-SiC is the best candidate for SiC-based power electronics.

The hexagonal structure for 4H-SiC is shown in Figure 1-3. The stacked layers, shown in Figure 1-2, create a layer of silicon across the top and a layer of carbon across the bottom.

This study used the (0001) Si- terminated crystal face of 4H-SiC. The C-face is not as desirable due to a lower oxide breakdown field compared to the Si-face and immaturity in epitaxial growth [8]. The a-face has alternating silicon and carbon atoms across the surface. The a-face was not used in this study, however previous results from several a-face experiments are part of the foundation for this study as described in Chapter 4.

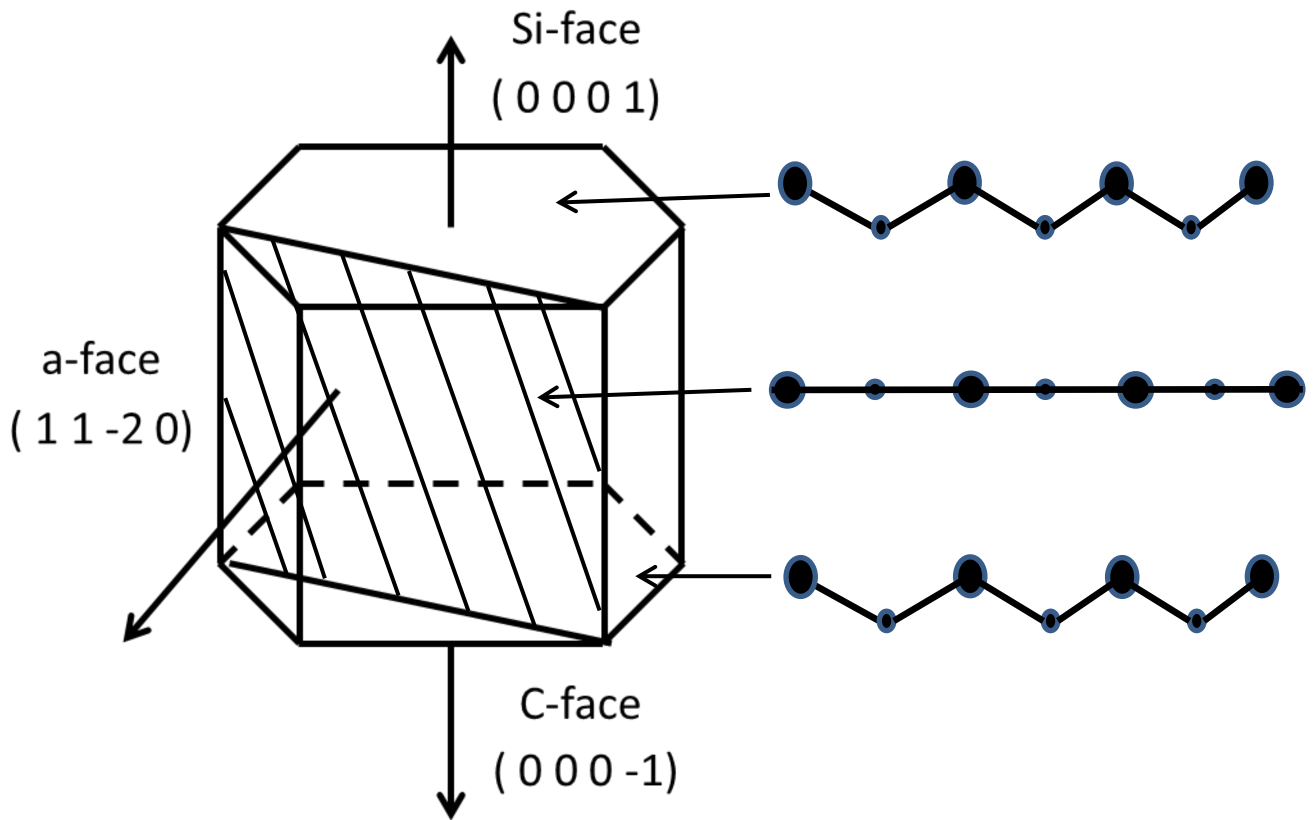

Figure 1-3. 4H-SiC crystal lattice structure.

1.2 Silicon carbide field-effect device comparison to silicon

Field-effect devices using silicon carbide (SiC) have the following advantages over silicon:

- Higher critical field and lower on-resistance
- Less current leakage at a higher temperature
- Higher switching frequency
- Less cooling

1.2.1 Critical field and lower on-resistance

A device with a larger critical field (E_{CR}) can be made proportionally thinner. The critical field determines the largest electric field a semiconductor can withstand before breakdown. Breakdown occurs when the electric field is large enough that a sufficient number of carrier electrons can ionize atoms by impact [9-10]. Each of these newly generated electrons creates more carrier electrons by colliding with atoms, creating a chain reaction of carrier electron generation known as avalanche breakdown. During avalanche breakdown, the secondary carrier electrons generated by electron-atom collisions must have large enough kinetic energies to generate further carrier electrons upon impact. The critical field equations for Si and 4H-SiC are [10-13]

$$E_{CR}, Si\ \left(\frac{V}{cm}\right) = \frac{4\ x\ 10^5}{1 - \frac{1}{3} log\left(\frac{N_D}{10^{16}}\right)} \tag{1.1}$$

$$E_{CR}, 4H - SiC \left(\frac{V}{cm}\right) = \frac{2.49\ x\ 10^6}{1 - \frac{1}{4} log\left(\frac{N_D}{10^{16}}\right)} \quad (1.2)$$

where N_D is the doping density of the semiconductor. The critical field of 4H-SiC is nearly an order of magnitude larger than silicon. This increase in the critical field is due to the larger energy band gap of 4H-SiC (Table 1-1, page 7).

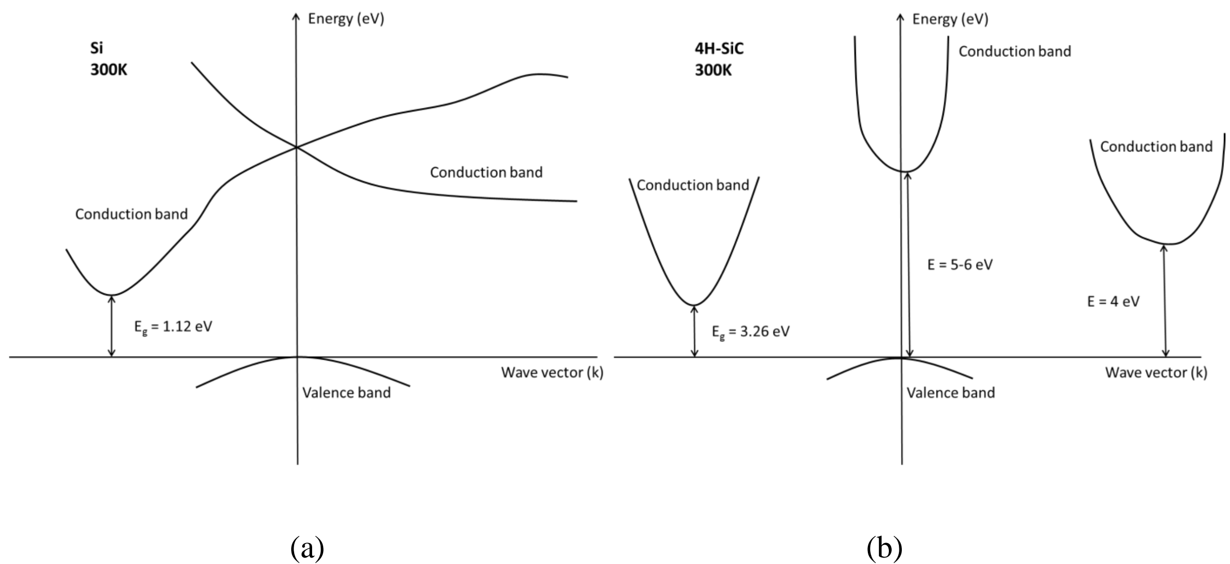

Figure 1-4. Energy band diagrams of silicon (a) and 4H-SiC (b) at room temperature [14]. Wave vector is inversely proportional to wavelength. Band energies in silicon are continuous, while band energies in 4H-SiC are discontinuous.

Within the crystalline electronic structure of a semiconductor, the band gap is an energy region in which no electronic states exist. This region is between the highest point of the valence band and the lowest point of the conduction band (Figure 1-4). Electrons need a specific minimum amount of energy to move from the valence band to the conduction band. The band gap for 4H-SiC is three times as large as silicon (Table 1-1), so the energy needed for impact

ionization is larger. Also, due to the discontinuous energy spectrum in 4H-SiC (Figure 1-4), the ballistic transport model of ionization is not valid [13-14]. In 4H-SiC, the electrons can reach the conduction band only through phonon collisions and quantum tunneling.

Property	**Si**	**4H-SiC**	**6H-SiC**
Band Gap (eV)	1.12	3.26	3.0
Electron Mobility ($cm^2\ V^{-1}\ s^{-1}$)	1400	900	400 ⊥ c-axis 80 ∥ c-axis
Hole Mobility ($cm^2\ V^{-1}\ s^{-1}$)	600	100	90
Critical Field (MV/cm)	0.3	3	3.2
Thermal Conductivity ($W\ cm^{-1}\ K^{-1}$)	1.5	4.9	4.9
Saturation Drift Velocity (10^7 cm/s)	1	2.7	2
Dielectric Constant ε_S (F/cm)	11.8	10	10

Table 1-1. Table of several key intrinsic properties for Si, 4H-SiC, and 6H-SiC. [15-17]

The wider band gap of SiC compared to silicon allows a significant increase in the blocking voltage of SiC power devices. The equation for blocking voltage (V_{Bl}) is [11]

$$V_{Bl} = \frac{\varepsilon_S E_{CR}^2}{2qN_D} \tag{1.3}$$

where ε_s is the dielectric constant, E_{CR} is the critical field, q is the charge and N_D is the doping density. V_{Bl} varies with respect to the square of the critical field, so for the same doping density, SiC blocks 30-60 times the voltage as silicon. SiC power devices can also block voltages beyond the range available for silicon power devices, since the specific on-resistance (resistance per unit area) for silicon power devices with larger blocking voltages becomes too large to be feasible [15].

The specific on-resistance is the measured resistance across the closed path of the power device. Power devices with lower specific on-resistances are more efficient. The specific on-resistance ($R_{ON,sp}$) equation is

$$R_{ONsp} = \frac{4V_{Bl}^2}{\varepsilon_s \mu_n E_g^3} \quad (1.4)$$

where V_{Bl} is the blocking voltage, ε_s is the dielectric constant, μ_n is the electron mobility, and E_g is the band gap energy [11, 18]. E_g for SiC is nearly three times greater than silicon, implying the $R_{ON,sp}$ for SiC will be nearly one-tenth that of silicon devices across a wide range of blocking voltages (Figure 1-5).

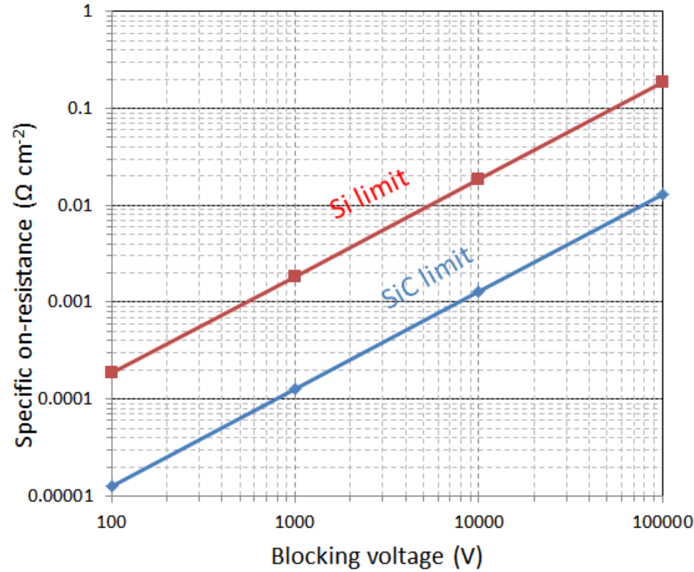

Figure 1-5. Specific on-resistance of silicon metal-oxide-semiconductor field-effect transistor (MOSFET) and SiC MOSFET compared to blocking voltage [11-13]. SiC specific on-resistance is nearly an order of magnitude less than silicon.

1.2.2. Temperature dependence of leakage current

Leakage current is the unintentional flow of current across a semiconductor device. Small amounts of leakage current increase power consumption of the device while sufficiently large amounts of leakage current can cause device failure. In metal-oxide-semiconductor (MOS) devices, one of the primary components of leakage current is subthreshold leakage (I_{sub}): current leakage across the device when the applied gate voltage is below the threshold voltage (i.e. when the device is off) [19-21]. I_{sub} is caused by minority carrier generation [19-20]. Minority carriers have the opposite charge of the majority carriers. In n-doped semiconductors, majority carriers are electrons, and minority carriers are holes.

Minority carriers are generated either by quantum tunneling of electrons across the semiconductor band gap or by impact ionization [22]. Both of these processes create an electron-hole pair (Figure 1-6). Quantum tunneling is a quantum-mechanical event. Unlike classical

mechanics, in quantum mechanics, particles do not stop at the edge of a boundary. If the boundary width is short enough, the particle can tunnel through the boundary and appear on the other side. Applying the concept of tunneling to minority carrier generation, electrons in the valence band have a probability of tunneling through the band gap and into the conduction band. The probability of an electron tunneling through the band gap increases as the energy of the electron increases. The energy can be gained either from thermal energy or photon absorption. Impact ionization occurs when an electron with sufficient kinetic energy collides with a lattice atom and knocks a valence electron into the conduction band.

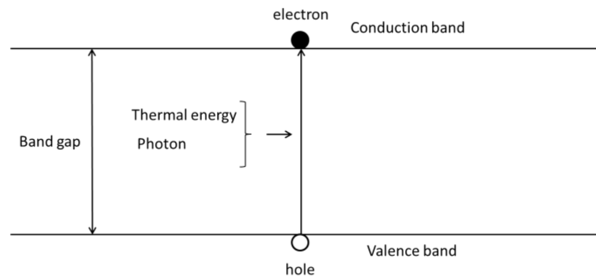

Figure 1.6. Creation of electron-hole pair.

When a semiconductor's temperature rises, the average kinetic energy of its electrons increases. These energized electrons in the valence band gain sufficient energy to jump the band gap and enter the conduction band. Also, as the temperature rises, the average kinetic energy of the carrier electrons increases, increasing the number of electrons available for impact ionization. When the temperature rises to a critical level, both of these electron-hole generation processes generate enough minority carriers to cause either a significant increase in power consumption or a complete device failure. For silicon power metal-oxide-semiconductor field-effect transistors (MOSFETs), the temperature limit is 150°C [18]. However, for SiC, the theoretical temperature

limit can approach 600°C because the wider band gap requires electrons to have a much larger amount of energy to jump across it [18]. Although the theoretical temperature limit for SiC is much larger than silicon, current packaging techniques restrict both silicon and SiC devices to around 150°C operational temperature.

1.2.3 Switching frequency

The maximum switching frequency is mainly limited by the power dissipation during switching and gate charging [23]. Power dissipation can be decreased by decreasing the specific on-resistance. In addition, switching frequency is also affected by drift velocity. The drift velocity is the average velocity that electrons travel inside the semiconductor. A higher drift velocity for SiC (Table 1-1) implies that SiC power devices can operate at faster switching speeds than silicon devices [17-18].

1.2.4 Cooling requirements

Cooling systems are required to disperse the large amounts of heat generated in silicon power devices. The heat is generated from power dissipated in the semiconductor during operation (specific on-resistance and switching loss), leakage current, and environmental conditions. Silicon power devices can only function properly at temperatures less than 150°C, so cooling systems, either forced air or liquid cooling, are required to maintain an appropriate temperature [24]. Silicon also has a relatively poor thermal conductivity compared to SiC, so silicon power devices require a more complex cooling system design. These cooling systems add extra weight, size, and complexity [24].

SiC power devices do not need the extensive cooling systems required by silicon power devices. SiC power devices have about 10 times lower specific on-resistance compared to silicon and have less power dissipation from switching losses. Leakage current is also less in SiC power devices since SiC does not generate as many minority carriers compared to silicon. In addition, the thermal conductivity of SiC is three times larger than silicon (Table 1-1), so SiC can dissipate heat quicker than silicon. All of these advantages of SiC compared to silicon imply that cooling systems for SiC devices can be lighter, smaller and less complex.

1.3 SiC hurdles

While the intrinsic properties of SiC make it very appealing for next generation power MOSFETs, there are hurdles preventing SiC from achieving wide-spread use. Before SiC MOSFETs achieve commercial viability, three critical challenges must be met: increasing channel mobility, improving stability, and establishing a better defined threshold voltage.

SiC MOSFETs using only a thermally grown oxide have mobilities less than $10cm^2\ V^{-1}\ s^{-1}$ [25]. Comparing this experimental mobility to the bulk electron mobility in Table 1-1, $\sim 900cm^2\ V^{-1}\ s^{-1}$, it can be seen there is much room for improvement.

Low mobility in SiC MOSFETs operating below 1500V is primarily caused by the high resistance experienced in the channel. This high resistance is caused by the very high density of interface traps (D_{it}) that are formed at the SiC/SiO_2 interface, two to three orders of magnitude larger than found at the Si/SiO_2 interface [26-27].

Interface traps can form when there is a Si or C deficiency. While there is no unanimity on which atom is vacant [28-31], evidence has shown that near interface oxide traps are reduced

through nitric oxide (NO) passivation (discussed below) [32-33]. Defects create electron traps with the majority having energies located near the conduction band edge [34].

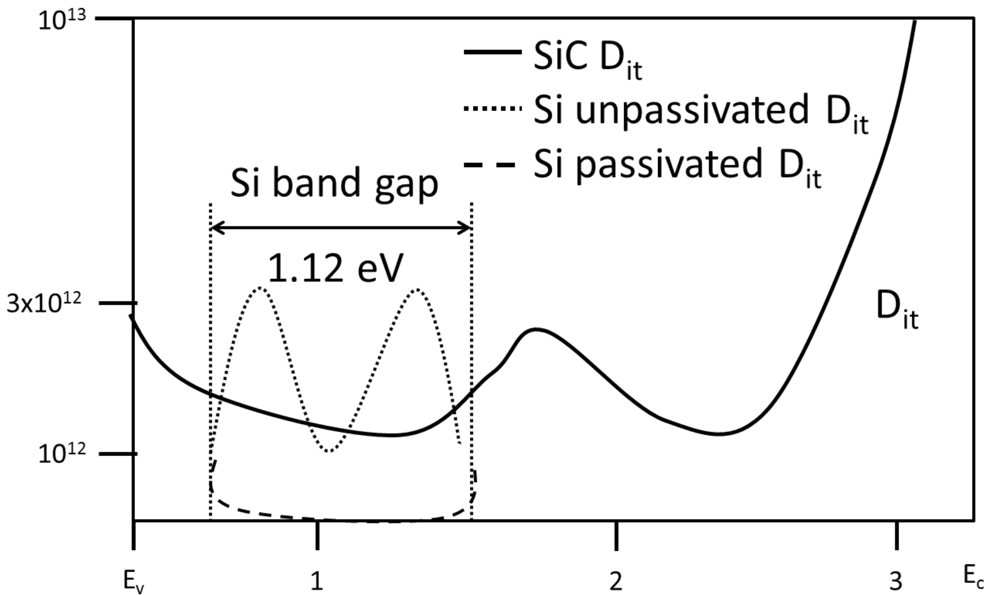

Figure 1-7. Qualitative plot of D_{it} vs. 4H-SiC band gap energy level. Si band gap and D_{it} are shown for comparison with SiC.

Figure 1-7 is a qualitative diagram representing the D_{it} with the corresponding energy level in the SiC bandgap. This large concentration of interface traps decreases the maximum channel mobility in n-channel MOSFETs. Carrier electrons fill these traps before contributing to the mobility. After these electron traps are filled, they cause an additional reduction to channel mobility since they become Coulomb scattering sites (explained further in Chapter 2.6.1). By passivating these interface traps with another atom, the expected mobility of SiC MOSFETs should increase.

This mobility hindrance is not limited solely to SiC. Early development of Si-based MOSFETs also confronted poor mobility due to near interface traps (Figure 1-7 "Si unpassivated

D_{it}"). These traps were Si dangling bonds produced during oxidation, and the traps were passivated with hydrogen (Figure 1-7 "Si passivated D_{it}"). However, hydrogen passivation on SiC MOSFETs only slightly reduced D_{it}, indicating that the interface traps in SiC are different than those found in silicon [35].

1.4 SiC passivation processes

Nitrogen passivation of the SiC MOSFET D_{it} was originally discovered to improve the electrical performance of 6H-SiC [36]. Soon after, nitrogen passivation showed improved electrical performance of 4H-SiC MOSFETs [37-38]. Today, standard industry nitrogen passivation is performed by a post oxidation anneal in nitric oxide (NO) gas for two hours at 1175°C. This temperature decomposes NO into its basic elements (N and O), which then move to the SiC/SiO_2 interface and interact at the defect sites. Nitrogen is believed to take the place of the vacant atom, passivating the electron trap [32-33]. The oxygen atom also interacts at the interface via oxidation to consume SiC, creating additional oxide [39]. The additional oxidation drives the SiC/SiO_2 interface deeper into the material, creating a new interface which requires more nitrogen to passivate. Because of these competing passivation and oxidation reactions, the nitrogen saturation point for the NO passivation process is about $5x10^{14}$ cm^2 [39]. NO passivated samples have been found to be highly stable and reliable, allowing for commercially viable device production. Later, another method combined NO passivation with hydrogen passivation, surpassing the mobility benchmark established by NO passivation. However, the combination process produced an oxide breakdown field much lower than standard NO passivated devices (5MV/cm compared to 7-8MV/cm) [40].

Recent studies of the NO passivation process show a correlation between the nitrogen coverage at the SiC/SiO_2 interface, the number of SiC/SiO_2 interface traps (N_{it}), and mobility [41]. N_{it} is the total number of interface traps across an energy range. It is obtained by integrating the D_{it} across an energy range, normally 0.2-0.6 eV below the conduction band for 4H-SiC. In essence, there appears to be scaling between increasing nitrogen coverage at the interface, decreasing the N_{it}, and increasing the peak mobility. Therefore, it is expected that a process that produces greater nitrogen coverage at the interface should decrease N_{it} and increase peak mobility. To verify this expectation, a study was conducted using a nitrogen plasma process. Chapter 3 has a discussion of this process and results.

Another process for SiC MOSFET passivation uses phosphorus (P). Using $POCl_3$, Okamoto, et. al. first demonstrated 4H-SiC MOSFETs with much lower D_{it} at energies 0.2eV or greater below the conduction band edge [42]. These phosphorus passivated MOSFETs had greater mobility compared to NO (peak mobility $80cm^2 V^{-1} s^{-1}$) [42]. However, a drawback of phosphorus passivation is that the phosphorus reacts with the oxide, transforming it from a standard thermally-grown oxide (SiO_2) into phosphosilicate glass (PSG). PSG is a polar substance, and recent studies of the stability and reliability of phosphorus passivated devices show that PSG has very poor stability at higher temperatures and stronger applied fields [43]. Electric dipoles in the PSG align with the applied electric field, which radically changes the threshold voltage (V_T) of the MOSFET (8V or higher V_T shift) [43]. When the gate is unbiased, due to the relaxation of the aligned dipoles, the threshold voltage will return to its pre-biased state. This voltage shifting makes the device unstable.

However, there is evidence that modifying the phosphorus passivation process can minimize the voltage shift of the PSG. This modified process, developed at Auburn University,

begins with a thin, thermally grown oxide that undergoes the phosphorus passivation process. Next, the device is capped with a much thicker deposited oxide formed using a tetra-ethyl-oxy-silicate precursor [44]. Deal and Snow estimated the thickness ratio of PSG to standard oxide needed to mitigate the polar effects of PSG [45]. The devices are more stable and retain a high mobility (60-70cm^2 V^{-1} s^{-1}) [44].

1.5 Counter-doping

Recent studies of phosphorus passivation revealed that phosphorus acts as a counter-dopant and passivating agent [46]. Further research into nitrogen passivation revealed that nitrogen also counter-dopes in addition to its role as a passivating agent [47]. Since nitrogen and phosphorus both counter-dope and passivate interface traps, the question may be raised, “How much of the improved mobility is a result of passivation and how much is from counter-doping?”

The first step to addressing this question is to differentiate the effects interface trap passivation and counter-doping have on MOSFET mobility. Since antimony and arsenic are in the same periodic column as nitrogen and phosphorus, they should have similar chemical behavior. However, their larger atomic size compared to nitrogen or phosphorus may help to differentiate between the effects of passivation and counter-doping for improved mobility.The question is further addressed in Chapters 4 and 5.

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Chapter 2. MOS systems physics and characterization

The metal-oxide-semiconductor (MOS) system is directly related to most silicon planar devices and integrated circuits [1]. Thus, this chapter introduces the metal-oxide-semiconductor capacitor (MOS capacitor) and the four distinct regimes defined by the relationship between the semiconductor surface potential (Ψ_s) and the semiconductor space-charge density (Q_s) at the oxide-semiconductor interface. The role of interface traps for MOS capacitors is explained, and the simultaneous high-low capacitance-voltage (hi-lo C-V) technique for measuring the number and density of interface traps is described.

Lateral metal-oxide-semiconductor field-effect transistors (lateral MOSFETs) are introduced because these MOSFETs were used in experiments, described in Chapters 3 and 4, to understand and improve SiC MOSFET inversion channel mobility. Inversion channel mobility and the three scattering mechanisms that affect the inversion channel are discussed. All mobility measurements in this study were field-effect mobility measurements, and the concept of field-effect mobility is addressed. A basic introduction to universal mobility lays the foundation for one of the results discussed in Chapter 4. This study also examines counter-doping to improve lateral MOSFET field-effect mobility, and a discussion of p-n junction physics and counter-doping is included. A discussion of the vertical power MOSFET concludes this chapter.

2.1 MOS fundamentals

In an ideal metal-semiconductor system under equilibrium, the Fermi levels (E_{fs} for the semiconductor Fermi level and E_{fm} for the metal Fermi level) are equalized by electron transfer from the material with the higher Fermi level to the material with the lower Fermi level.

However, in the case of an ideal MOS capacitor (Figure 2-1), the oxide prevents the transfer of charge. The accumulation of electrons and holes at the metal-oxide and oxide-semiconductor interfaces creates a surface potential (Ψ_s) at these interfaces. These surface potentials create a potential gradient across the oxide.

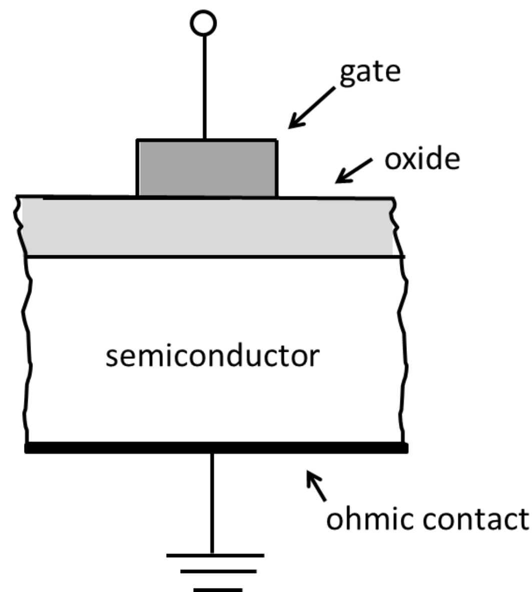


Figure 2-1 Simple diagram of a MOS capacitor.

The surface potential at the oxide-semiconductor interface determines the regime of the semiconductor. Changing the surface potential (normally by applying a voltage on the metal (gate voltage)) allows the semiconductor to move to different regimes. To explain the effect of a changing surface potential (a result of changing gate voltage) of the MOS capacitor, p-type silicon with an aluminum gate is considered (Figure 2-2). For negative Ψ_s, the space-charge density (Q_s) is positive, while positive Ψ_s corresponds to a negative Q_s. The space-charge density is the density and type of charge (positive or negative) at distances across a MOS system. Based upon the functions describing the rate of change between Ψ_s and Q_s (Figure 2-2), the MOS

system has four distinct surface potential regimes: (1) Hole accumulation (2) Flat-band (3) Depletion (4) Inversion. The discussion below is restricted to n-channel MOSFETs with a p-type body, but the same discussion can be extended to p-channel devices [2].

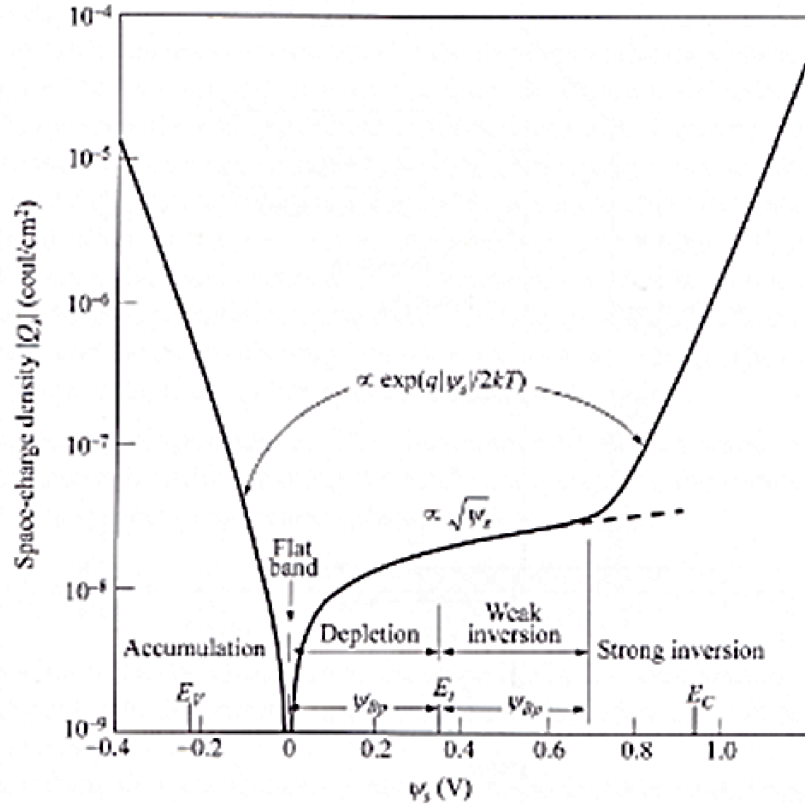


Figure 2-2. Space-charge density (Q_s) variation in a semiconductor compared to surface potential (Ψ_s) for p-type silicon at room temperature [1]. (Permission received from John Wiley & Sons, Inc., S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices, 3rd edition*, © 2007)

2.1.1 Hole accumulation

When a large negative bias is applied to the gate, electrons (-Q) collect at the metal-oxide interface and holes (+Q) collect at the oxide-semiconductor interface (Figure 2-3(a)). The electron build up at the metal-oxide interface raises the metal Fermi level closer to the vacuum energy level (E_0) which is the energy required for an electron to be free from a material (Figure

2-3(b)). Since the oxide prevents current from flowing in the semiconductor, the semiconductor Fermi level does not change at deep distances in the semiconductor. However, near the oxide-semiconductor interface, the semiconductor energy bands bend upward because the Fermi level must be continuous across the entire MOS system. The energy levels of the oxide are also bent due to the electric field in the oxide so that the oxide Fermi level connects the metal Fermi level and the semiconductor Fermi level.

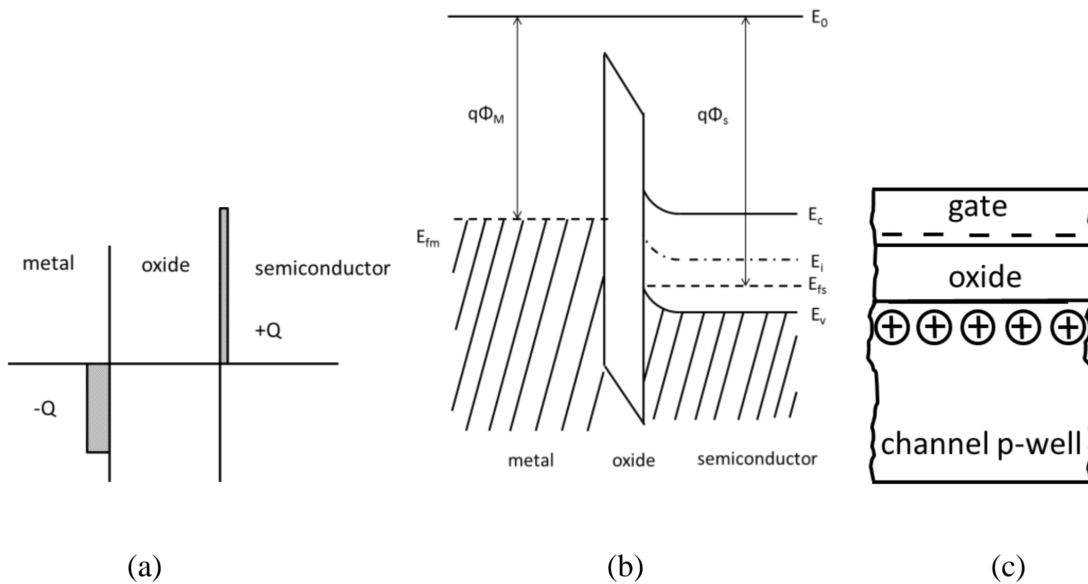


Figure 2-3. Space-charge diagram (a), band diagram (b), and device diagram (c) for a MOS system in accumulation.

The buildup of negative charge at the metal-oxide surface increases the hole density at the surface until the hole density is greater than the acceptor density (Figure 2-3(c)). This condition is called accumulation. As the gate voltage decreases further into accumulation, the surface hole space-charge density increases exponentially as shown in Fig. 2-2.

2.1.2 Flat-band condition

From deep accumulation, as the gate voltage is made less negative, the charges that have accumulated on both sides of the oxide decrease until none remain (Figure 2-4(a)). The point at which there are no accumulated charges on either side of the oxide is important because at this point the metal Fermi level equals the semiconductor Fermi level, and consequently the oxide and semiconductor bands are flat (Figure 2-4(b)).

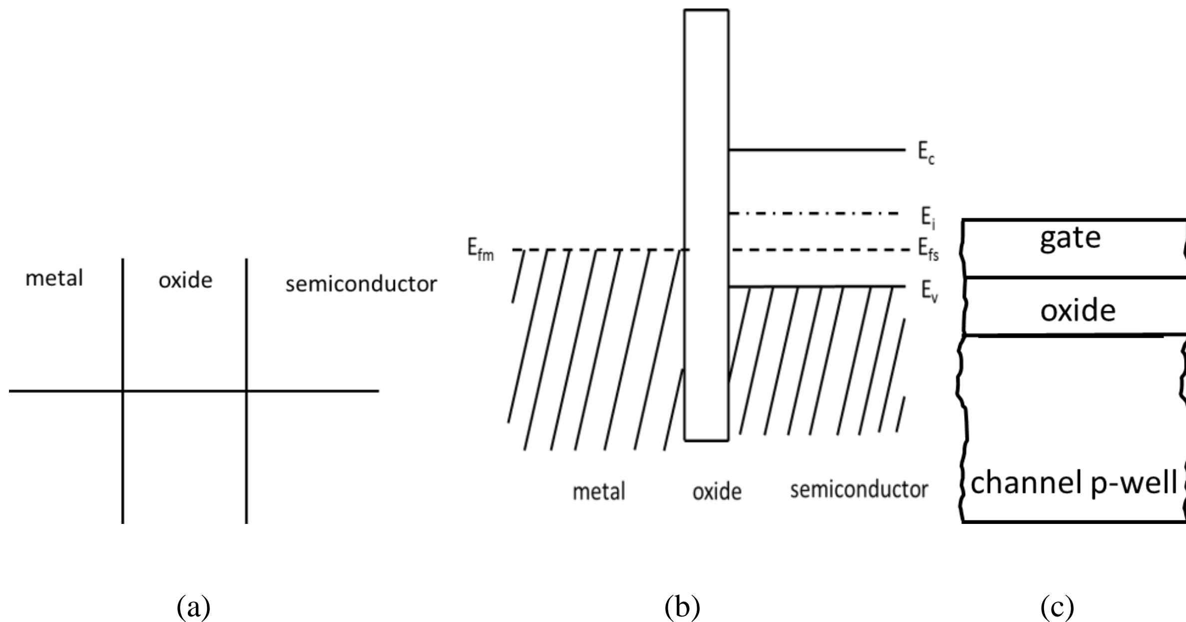


Figure 2-4. Space-charge diagram (a), band diagram (b), and device diagram (c) for a MOS system in flat-band.

For an ideal MOS system, the voltage necessary to reach the point where all of the bands are flat is known as the flat band voltage and defined as

$$V_{FB}^{0} = \Phi_M - \Phi_S = \Phi_{MS} \tag{2.1}$$

where V_{FB}^{0} is the flat band voltage, Φ_M is the metal work function, and Φ_S is the semiconductor work function. The work function is the minimum amount of energy required to remove an electron from a material.

The flat band voltage is an important characterization for two reasons: (1) it influences the threshold voltage for a MOSFET, as discussed later; (2) the difference between the ideal and the experimental flat-band voltages is a measure of defects and trap-related fixed charges located in the oxide as well as near the oxide-semiconductor interface [1]. The experimental flat-band voltage is typically extracted from capacitance-voltage (C-V) measurements by determining the gate voltage at which the device capacitance is equal to flat-band capacitance (C_{FB}).

2.1.3 Depletion

As the gate voltage increases past the flat band voltage, positive charge builds up at the metal-oxide interface. This positive charge causes holes to move away from the oxide-semiconductor interface, leaving behind the negative-charged acceptor core ions (Figure 2-5(a)).

The positive charge at the metal-oxide interface increases the metal work function, which lowers the metal Fermi level below the semiconductor Fermi level (Figure 2-5(b)). The difference between the metal Fermi level and the semiconductor Fermi level causes the semiconductor bands to bend near the oxide-semiconductor interface, and the electric field in the oxide causes the oxide bands to bend, similar to what occurs in the accumulation regime. However, because the electric field and charge build up are opposite to what occurs in the accumulation regime, the bands bend in the opposite direction.

Since the space-charge potential must be equal on both sides of the oxide, the negative charge in the semiconductor is manifested by the depletion of holes (the majority carrier in p-type semiconductors) at the surface region and the negative-charged acceptor core ions which are left behind (Figure 2-5(c)). As higher gate voltage is applied, the depletion region expands, and the negative space charge continues to increase (x_d Figure 2-5(a)).

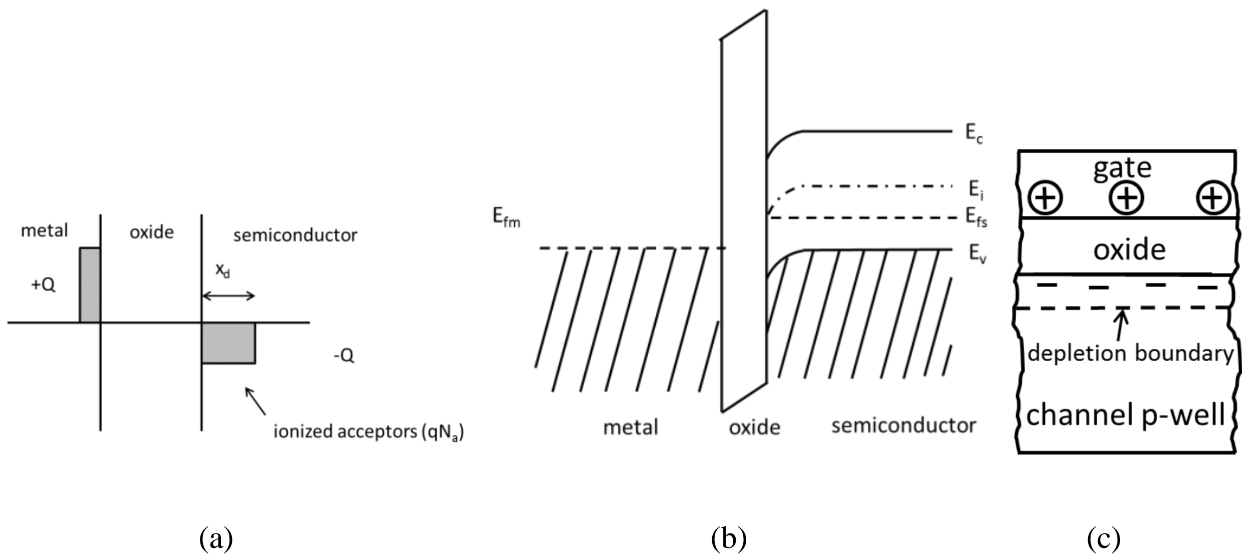


Figure 2-5. Space-charge diagram (a), band diagram (b), and device diagram (c) for a MOS system in depletion.

2.1.4 Inversion

As the gate voltage increases, the depletion region continues to expand until the maximum depletion width is reached (x_{dmax} Figure 2-6(a)). The maximum depletion width is such that the generation of electrons exceeds recombination at the surface, causing the formation of a minority-carrier (electrons in this case) conducting channel, commonly known as the inversion channel (Q_{inv} Figure 2-6(a)). Under this condition, the intrinsic Fermi level (E_i) crosses

the semiconductor Fermi level (E_{fs}), bringing the conduction band edge (E_c) closer to the Fermi level than to the valance band edge (E_v) (Figure 2-6(b)).

This condition is called inversion because the surface has more electrons than holes (Figure 2-6(c)), even though the semiconductor was doped with p-type acceptor dopants. These negative charges "invert" the p-type material at the surface. Because the minority carriers will continue to increase exponentially as the gate voltage increases (Figure 2-2), the depletion width will no longer increase.

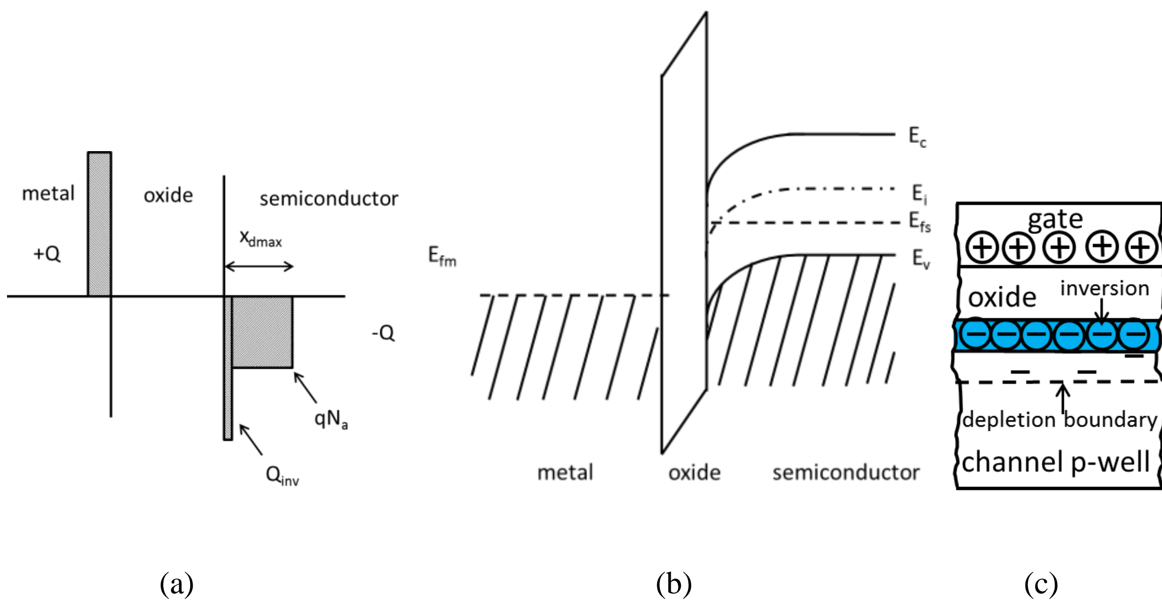


Figure 2-6. Space-charge diagram (a), band diagram (b), and device diagram (c) for a MOS system in inversion.

2.2 Practical MOS capacitor

Thermal oxidation of silicon does not leave a clear-cut separation between the silicon crystal and the oxide. The chemical composition of thermally oxidized silicon consists of the

silicon crystal, a monolayer of SiO_x (incompletely oxidized silicon), a thin strained region of SiO_2 (due to imperfect lattice matching between SiO_2 and silicon), and strain-free amorphous SiO_2 [1] (Figure 2-7). The non-ideal layer of SiO_x and the strained SiO_2 at the oxide-semiconductor interface, along with other non-ideal conditions (i.e. real-world conditions) give rise to oxide charges and interface traps that affect the MOS system. The flat band voltage (V_{FB}) of a non-ideal metal-oxide-semiconductor capacitor (MOS capacitor) is derived from

$$V_{FB} = \Phi_{MS} - \frac{Q_i}{C_{ox}} - \frac{1}{\varepsilon_{ox}} \int_0^{t_{ox}} \rho_{ox}(x)dx \tag{2.2}$$

where Φ_{MS} is the metal-semiconductor work function, Q_i is the interface charge, C_{ox} is the oxide capacitance, ε_{ox} is the oxide dielectric constant, and ρ_{ox} is the oxide charge density.

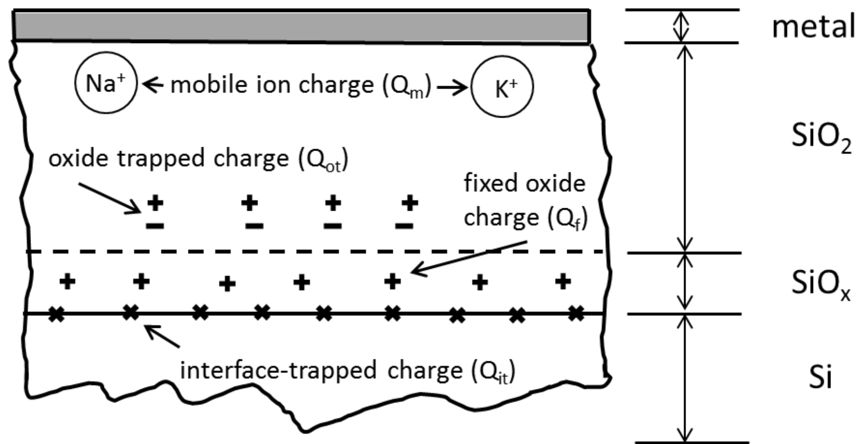


Figure 2-7. Types of charges derived from thermally oxidized silicon [1].

Figure 2-7 shows the basic classifications of interface traps and oxide charges [1]: interface-trap charges (Q_{it}); mobile ion charges (Q_m); fixed oxide charges (Q_f); and oxide trapped charges (Q_{ot}).

2.2.1 Interface traps

Interface traps (Q_{it}) are located at the oxide-semiconductor interface and have energy states that exist within the forbidden band gap of the semiconductor [1]. In silicon MOS systems, these traps can be produced by excess silicon or oxygen, dangling silicon bonds, or impurities [1]. Interruption of the lattice structure at the interface allows these traps to exist within the band gap [1]. The presence of these traps at the Si/SiO_2 interface can be as high as 10^{15} atoms cm^{-2} (though hydrogen annealing reduces the density of interface traps to 10^{10} atoms cm^{-2}) [1]. Interface traps can be either acceptors (Figure 2-8 (a)) or donors (Figure 2-8 (b)).

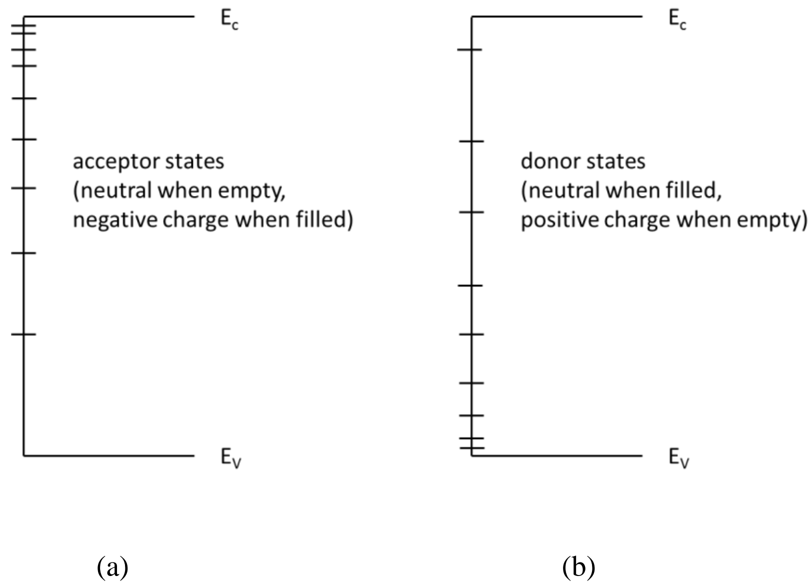


Figure 2-8. Energy diagram of acceptor interface traps (a) and donor interface traps (b).

The occupancy of these traps follows the Fermi-Dirac distribution function, so the probability of donor states being occupied is [1]

$$F_{SD}(E_t) = \frac{1}{1 + {}^{1}\!/_{g_D}\, exp[(E_F - E_t)/(kT)]} \tag{2.3}$$

and the probability of acceptor states being occupied is

$$F_{SA}(E_t) = \frac{1}{1 + {}^{1}\!/_{g_A}\, exp[(E_t - E_F)/(kT)]} \tag{2.4}$$

where E_t is the interface trap energy, E_F is the Fermi level energy, and the degeneracy of the ground-state is represented by g_D which equals 2 for the donor traps and g_A which equals 4 for acceptor traps [1]. A convenient interpretation of the interface traps is to sum all of the traps into an equivalent density of interface traps (D_{it}) and determine the energy level at which the total charge contribution is zero (E_0) (Figure 2-9) [1]. Above E_0, the interface trap states are acceptor types, and below E_0, the interface trap states are donor types. The interface traps are also assumed to be filled if the trap energy state is below the semiconductor Fermi level, and empty if the trap energy state is above the semiconductor Fermi level [1]. Therefore, if the semiconductor Fermi level is above E_0, the interface traps will contribute a net negative charge, while if the semiconductor Fermi level is below E_0, the interface traps will contribute a net positive charge.

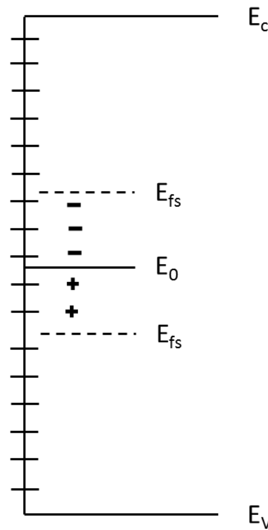
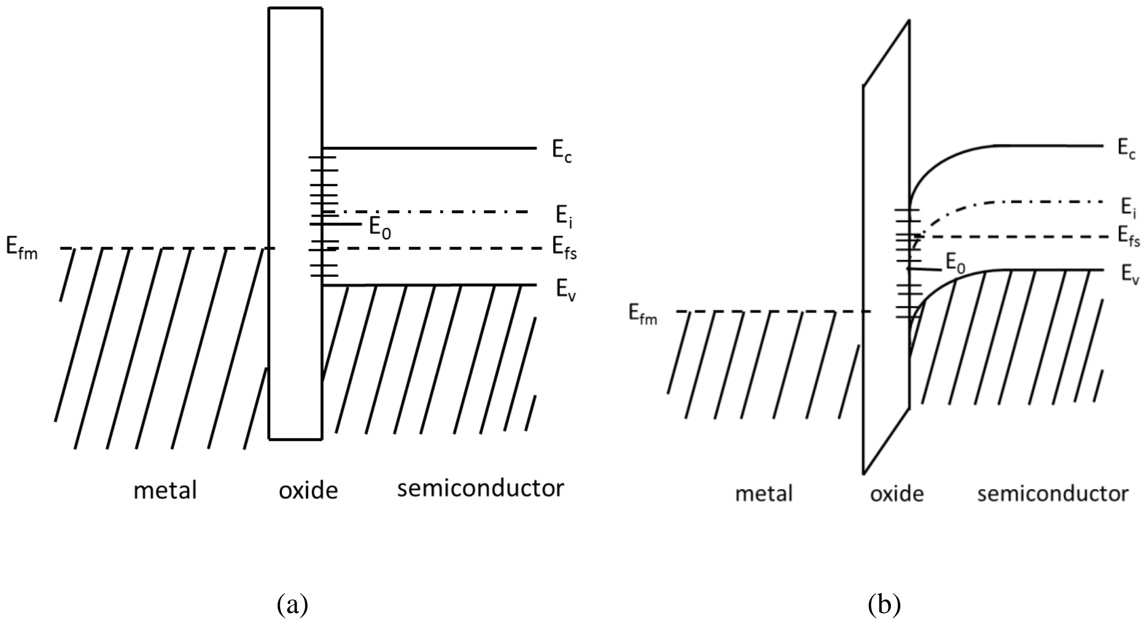


Figure 2-9. Energy diagram of an interface-trap system consisting of both acceptor and donor traps.

Referring back to Chapter 2.1.1-2.1.4, an applied gate voltage causes the semiconductor energy bands to raise or lower (band bending) near the oxide-semiconductor interface. The applied gate voltage also raises or lowers the trap energy level along with the semiconductor energy bands. Thus, as the applied gate voltage is changed, the number of interface traps below/above the semiconductor Fermi level also change. Applying the interface-trap system in Figure 2-9 to a MOS system, at the flat-band regime, the semiconductor Fermi level is below E_0, so the net charge of the interface traps is positive (Figure 2-10(a)). However, once the semiconductor is brought into the inversion regime, the semiconductor energy bands and the interface trap energies have lowered. In this regime, the semiconductor Fermi level is above some of the acceptor traps, so the interface traps contribute a net negative charge (Figure 2-10(b)).



(a) (b)

Figure 2-10. Interface traps in a MOS system at the flat-band regime (a) and in the inversion regime (b).

Interface-trap energy levels are distributed across the entire semiconductor band gap. Therefore, using the assumptions made in the interface-trap system seen in Figure 2-9, the density of the interface traps can be characterized by [1]

$$D_{it} = \frac{1}{q}\frac{dQ_{it}}{dE} \tag{2.5}$$

Equation 2.5 is the concept used to experimentally determine D_{it} in MOS systems (Chapter 2.3).

2.2.2 Mobile ions

Mobile ions (Q_m) are usually metallic ions, such as sodium or potassium, that enter the oxide during oxidation or later during MOS system fabrication since practical MOS processing

cannot be perfectly clean. At room temperature, these ions are fixed, but at biased, high-temperature conditions, these ions become mobile. Mobile ions cause stability issues with MOS systems. Under negative-biased high-temperature conditions, mobile ions migrate to the metal-oxide interface of the MOS system. This concentration of ions at the metal-oxide interface increases the flat-band voltage [3]. However, if the MOS system is switched to a positive-bias at high temperatures, these ions will flow into the oxide and congregate near the oxide-semiconductor interface. These positive charges in the oxide reduce the flat-band voltage [3]. In other words, mobile ions can cause a MOS system operating under bias at high temperatures to have different flat-band voltages depending on the direction of a gate voltage sweep, creating instability in the MOS system.

2.2.3 Oxide trapped charges and fixed oxide charges

Oxide trapped charges (Q_{ot}) are dispersed throughout the oxide. Their creation is associated with several different methods, such as X-ray radiation or hot-electron injection [1]. Fixed oxide charges (Q_f) are located near the oxide-semiconductor interface. Unlike mobile ions, fixed oxide charges are immobile under applied electric fields. There has been much investigation into the creation of these charges, with one of the more recent proposals suggesting that the value of Q_f is determined by the number of interstitial silicon atoms near the oxide-silicon interface [4]. These interstitials are formed during the processes of silicon interstitial generation and recombination at the oxide-silicon interface [4].

2.3 High-low capacitance-voltage characterization

High-low capacitance-voltage characterization (hi-lo C-V) is a technique that obtains data by measuring the capacitance from a small amplitude high-frequency and low-frequency AC input centered around the DC steady state voltage applied to the gate in MOS devices (Figure 2-11). This technique is used to determine several characterization factors. One of the most important characterizations is the density of electron traps near the oxide-semiconductor interface. The density of these interface traps (D_{it}) is important in semiconductor processing, since a greater density of interface traps means there is more Coulomb scattering and reduced reliability. While there are several other methods to calculate the D_{it} of MOS devices, each with their own strengths and limitations, this section will focus solely on the simultaneous hi-lo C-V characterization method used in the experiments described in Chapters 3 and 4.

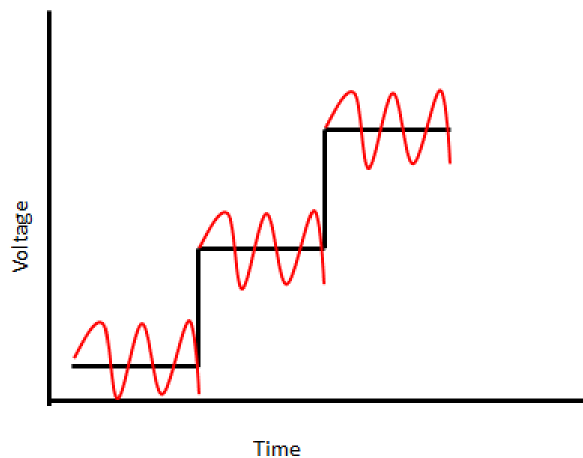
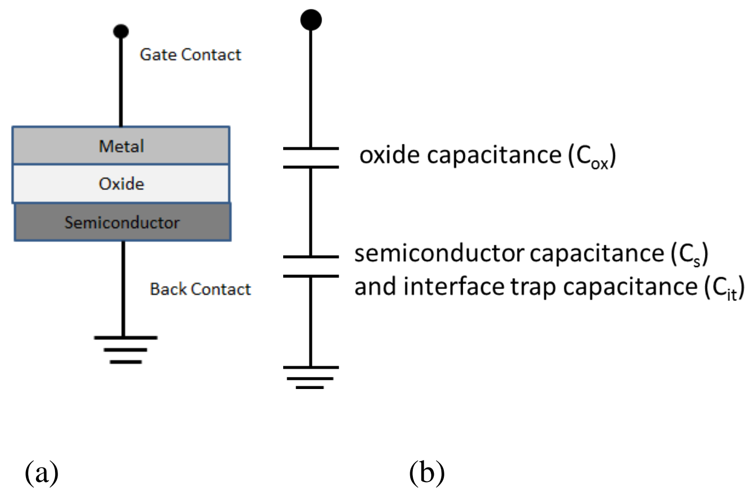


Figure 2-11. Diagram of a hi-lo C-V measurement. The black line represents the DC voltage; the red lines are the AC bias.

The total capacitance of a MOS device is

$$\frac{1}{C_{tot}} = \frac{1}{C_{ox}} + \frac{1}{C_{it} + C_s} \tag{2.6}$$

where C_{tot} is the total capacitance, C_{ox} is the oxide capacitance, C_{it} is the interface trap capacitance, and C_s is the semiconductor capacitance [5]. C_{ox} and C_s are capacitors in series (Figure 2-12).



(a) (b)

Figure 2-12. Simplified MOS device diagram (a) and circuit diagram (b). The oxide and semiconductor are capacitors in series.

Capacitance can be defined as the ratio of change in charge to the change in potential:

$$C \equiv \frac{\Delta Q}{\Delta V} \tag{2.7}$$

When C_{ox} and C_s are known, the C_{it} can be calculated from a measured C_{tot}. In taking hi-lo C-V measurements, the high frequency must be high enough to prevent electron traps from responding to the AC frequency, and the low frequency must be low enough for all traps to respond to the AC frequency. The total capacitance for the high frequency can be written as

$$\frac{1}{C_{tot}^{HF}} = \frac{1}{C_{ox}} + \frac{1}{C_s} \tag{2.8}$$

and the total capacitance for the low frequency can be written as

$$\frac{1}{C_{tot}^{QS}} = \frac{1}{C_{ox}} + \frac{1}{C_{it} + C_s} \tag{2.9}$$

Also, in Equation 2.7, if ΔQ is replaced with D_{it}, then the C_{it} can be written as

$$C_{it} = q\ D_{it} \tag{2.10}$$

since the capacitance associated with the interface traps is the electron charge multiplied by the density of the traps. The hi-lo C-V method usually starts in accumulation and then sweeps the voltage downward toward depletion. In accumulation, all of the electron traps are filled, since the conduction band edge is below the Fermi level. As the DC voltage slowly decreases, the metal Fermi level increases, which begins to bend the semiconductor bands upward. The AC voltage oscillates around each stopping point of the DC voltage (Figure 2-13). The high frequency is too rapid for electrons to respond by moving into and out of the traps with the change in voltage. However, the electrons do respond to the low frequency and move into and out of the traps as the

AC voltage oscillates. The difference between the electron being in the trap and out of the trap creates a difference in the charge Q, so the capacitance is larger for the low frequency than for the high frequency. This extra capacitance from the electron in the trap is the C_{it}. Since the C_{it} is based only around one specific energy level, as determined by the DC voltage, a D_{it} can be extracted from the C_{it}.

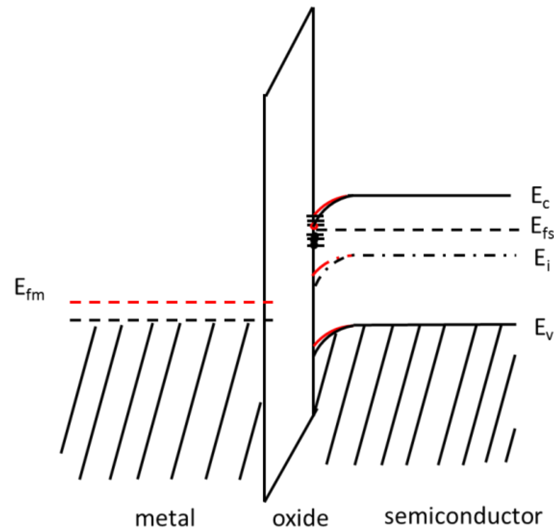


Figure 2-13. Band diagram of hi-lo C-V method. The black lines represent the steady state DC current. The red lines represent a small gate voltage change from the AC current. The red dot represents a filled trap in the DC voltage, but emptied from the low frequency AC voltage. The change from the trap being filled to empty contributes to the C_{it}.

Solving Equation 2.9 for D_{it} yields

$$D_{it} = \frac{C_{ox}}{q}\left(\frac{C_{tot}^{QS}}{C_{ox} - C_{tot}^{QS}}\right) - \frac{C_s}{q} \qquad (2.11)$$

Using Equation 2.8 to solve for C_s:

$$C_s = \frac{C_{ox} C_{tot}^{HF}}{C_{ox} - C_{tot}^{HF}} \quad (2.12)$$

Substituting the equation for C_s into Equation 2.11 results in the standard D_{it} equation [5-8]:

$$D_{it} = \frac{C_{ox}}{q} \left(\frac{C_{tot}^{QS}}{C_{ox} - C_{tot}^{QS}} - \frac{C_{tot}^{HF}}{C_{ox} - C_{tot}^{HF}} \right) \quad (2.13)$$

This equation is only valid if none of the electron traps respond to the high frequency during measurement. If electron traps respond to the high frequency, then the semiconductor capacitance in Equation 2.8 becomes larger. This increase in the semiconductor capacitance increases the total high frequency capacitance. If the total high frequency capacitance increases, then the difference between the quasi-static total capacitance and the high frequency total capacitance is reduced. This underestimates the D_{it} value obtained from Equation 2.13.

2.3.1 Oxide thickness

Hi-lo C-V offers a nondestructive way to measure the oxide thickness. The oxide thickness is calculated from the equation

$$t_{ox} = \frac{A \varepsilon_{ox}}{C_{ox}} \quad (2.14)$$

where t_{ox} is the oxide thickness, A is the area of the device, ε_{ox} is the oxide dielectric constant, and C_{ox} is the oxide capacitance. The oxide capacitance is extracted from the total capacitance

from the high frequency measurement (Equation 2.8). When the device is in strong accumulation, the contribution from the semiconductor capacitance is negligible. Therefore, a close approximation to the oxide thickness can be obtained as oxide capacitance is equal to total capacitance [6].

2.4 Lateral MOSFETs

Lateral MOSFETs (Figure 2-14) are MOSFETs with long channels and are commonly used for audio amplification [9]. These MOSFETs are lightly doped (~$5x10^{15}$ cm^{-3}) p-substrate SiC with highly n-doped ($1x10^{20}$ cm^{-3}) regions for the source and drain. When the applied gate voltage is below the threshold voltage (Figure 2-14(a)), little leakage current occurs and the device is considered to be "off." The n-p-n junction between the source and drain blocks current as long as the gate voltage is below threshold. When the gate voltage is below threshold and a large positive voltage is applied to the source, a depletion region forms at the n-p junction as the electrons in the n-type region flow toward the source, and the holes in the p-type region flow away from the source. If a large negative voltage is applied to the source, a depletion region forms at the p-n junction. The threshold voltage (V_{TH}) is when the MOSFET turns on (inversion). Once the threshold voltage is reached, inversion occurs in the channel and current flows (Figure 2-14(b)).

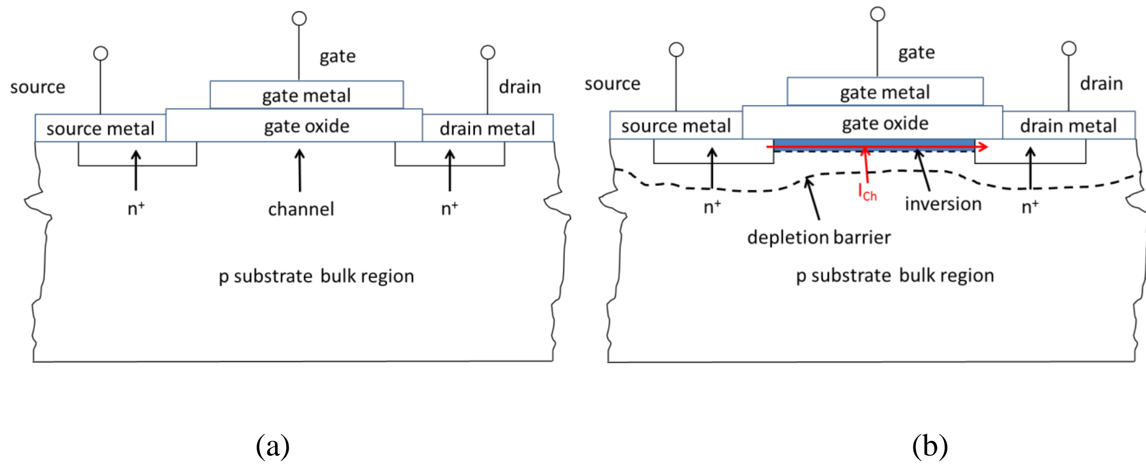


Figure 2-14. Lateral MOSFET diagram in off mode (a). Channel forms under gate oxide during inversion (b).

2.5 Inversion channel mobility

For n-MOSFETs, the inversion channel mobility is the mobility measured through the channel region after inversion has occurred. High mobility devices are efficient because during operation fewer electrons are scattered which reduces power dissipation.

Mobility follows Matthiessen's rule: the inverse of the total amount is equal to the sum of the inverse of each contributing part. Therefore, the total amount will always be less than the smallest contributor. The mobility through the inversion channel region is

$$\frac{1}{\mu} = \frac{1}{\mu_C} + \frac{1}{\mu_{SR}} + \frac{1}{\mu_P} \tag{2.15}$$

where μ_C is the Coulomb mobility, μ_{SR} is the surface roughness mobility, and μ_P is the phonon mobility. These three mobilities are each limited by a separate scattering mechanism.

2.6 Scattering mechanisms

The three scattering mechanisms that deflect the ballistic transportation of carriers in the inversion channel are the following:

- Coulomb scattering
- Surface roughness scattering
- Phonon scattering

Each scattering mechanism has a different dependency on temperature and effective electric field (Chapter 2.6.1-2.6.3). The effective electric field is defined by [10]

$$E_{eff} = (\frac{q}{\varepsilon_{Si}})(N_{dpl} + \eta \cdot N_{Car}) \tag{2.16}$$

where q is the elementary charge, ε_{Si} is the dielectric constant for silicon, N_{dpl} is the surface concentration of the depletion charge, η is a parameter defined to be 0.5 for electron carriers and N_{car} is the concentration of the inversion layer carrier charge [10]. Therefore, a schematic diagram of an expected total mobility would be similar to what is shown in Figure 2-15.

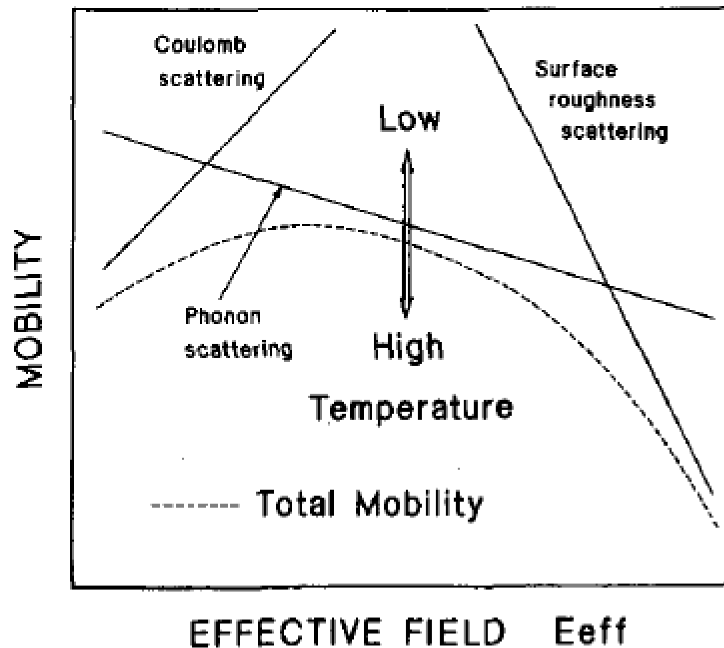


Figure 2-15. The three scattering mechanisms and their effect on the total mobility in the inversion channel [11] (© 1994 IEEE).

2.6.1 Coulomb scattering

In addition to the four types of charges that exist at the oxide-semiconductor near interface region (Chapter 2.2-2.2.3), ionized impurities are fixed charges in the semiconductor that are also scattering sites [12]. Ionized impurities can either be unintentional impurities that are introduced into the device during processing (minimizing these impurities is a prime concern of semiconductor device engineering) or purposely introduced to change the electrical properties of the semiconductor (dopants) [13].

At low transverse electric fields, these five types of charges create a Coulombic interaction among them and the electron transport in the inversion layer [10-11, 14]. The Coulomb mobility is proportional to temperature. As temperature increases, the electron drift velocity increases, reducing the Coulomb scattering cross-section, so less electrons are scattered.

An exact derivation of the scattering rate for an electron with a wave vector **k** is impractical for two main reasons: it requires the actual position of each charge, and the derivation would only be accurate for the current configuration [12]. Therefore, an average charge density approximation is more appropriate to calculate Coulomb scattering mobility. A semi-empirical formula of the Coulomb scattering mobility for weak inversion is [10]

$$\mu_C = \frac{\Gamma_C\, T}{N_T}\left(\frac{n_S}{n_0}\right)^{\xi} \tag{2.17}$$

where μ_C is the Coulomb mobility, Γ_C is a coefficient parameter, T is temperature, N_T is the sum of all the surface charges, n_S is electron surface density, n_0 is a proportionality parameter, and ξ is an empirical parameter [10].

At strong inversion, a Coulomb screening parameter must be added to the equation. Coulomb screening occurs when a large number of electrons are present. These electrons effectively screen any single electron from an outside Coulomb charge, reducing Coulomb scattering. The Coulomb scattering mobility for strong inversion with Coulomb screening is [10]

$$\mu_C = \frac{\Gamma_C\, T}{N_T}\left(1 + \frac{n}{n_{scr}}\right)^{\xi'} \tag{2.18}$$

where n is the electron concentration and n_{scr} and ξ' are empirical parameters [10].

2.6.2 Surface roughness scattering

The interface between silicon and thermally grown SiO_2 is not perfectly flat. Electrons can scatter off the rough boundary created by oxidation. The inversion channel thickness of a MOSFET can be very thin, as little as 10-100 Å [15]. As the gate electric field increases, the electron carriers are attracted with stronger force to the interface, increasing the electron carrier density at the interface [15]. Therefore, surface roughness scattering is primarily dominated by the E_{eff} with a weak dependence on temperature. The surface roughness mobility is weakly dependent on temperature, since a higher temperature indicates electrons have more kinetic energy, reducing their vulnerability to surface roughness scattering [15]. Surface roughness mobility (μ_{SR}) is related to the gate electric field by [15]

$$\mu_{SR}(E_{\perp}) \propto \frac{T^{1/\alpha}}{E_{\perp}^{2}} \quad (2.19)$$

where $E_{\perp}$ is the gate electric field and α is a small positive number.

2.6.3 Phonon scattering

At temperatures above 0 K, atoms in a crystalline structure vibrate. These vibrational modes are called phonons. Phonons can be considered to act as particles that can deflect electrons. The effective electric field has only a small effect on phonon scattering, while the temperature is the principle variable determining phonon scattering. As temperature increases, atoms in the lattice vibrate more and can vibrate at higher modes. The increased vibration

increases the number of phonons, increasing the rate of phonon-electron scattering. This increased scattering decreases the phonon mobility. The equation for phonon mobility is [10]

$$\mu_P = \frac{A}{E_{eff}^{0.3} T^{1.75}} \tag{2.20}$$

where μ_P is the phonon mobility, A is a constant coefficient, E_{eff} is the effective electric field (Equation 2.16), and T is the temperature [10].

2.7 Universal mobility in Si MOSFETs

Extensive studies of silicon MOSFETs led to the discovery of universal mobility [16-18]. Universal mobility is the fundamental inversion layer for silicon MOSFETs with respect to the electric field, regardless of other device parameters (bulk doping concentration, device thickness, oxide thickness, etc.) (Figure 2-16). As shown in Figure 2-16, the mobilities for MOSFETs with different doping concentrations all follow a universal curve if plotted as a function of the E_{eff}.

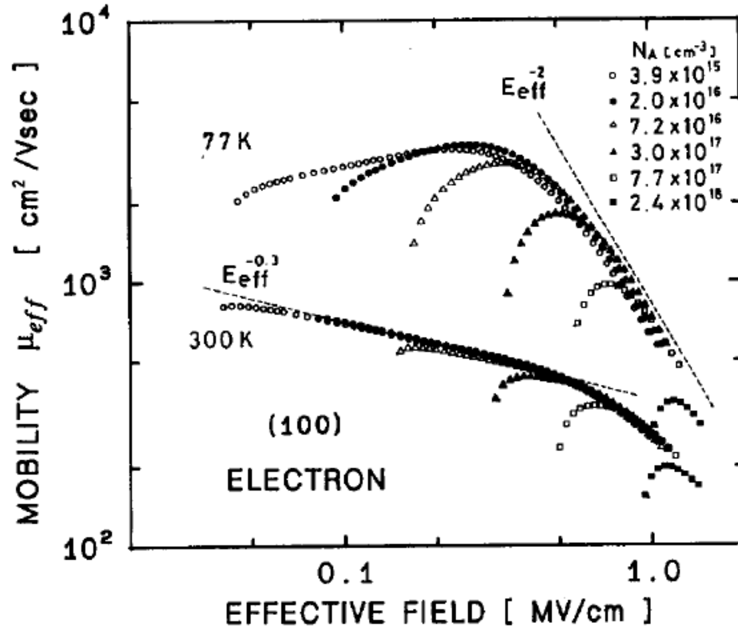


Figure 2-16. Diagram of universal mobility behavior across a range of substrate acceptor concentrations (N_A) [11] (© 1994 IEEE).

This universality is fundamental in understanding how the three main scattering mechanisms (Coulomb, surface roughness, and phonon) depend on the electric field and temperature. These scattering mechanisms are related to the mobility as follows:

$$\frac{1}{\mu} = \frac{1}{\mu_C} + \frac{1}{\mu_{SR}} + \frac{1}{\mu_P} \tag{2.21}$$

where μ_C is the Coulomb mobility, μ_{SR} is the surface roughness mobility, and μ_P is the phonon mobility. For Si MOSFETs, μ_C is proportional to temperature, μ_P is inversely proportional to temperature, and μ_{SR} is inversely proportional to the applied electric field [18].

There has been no conclusive evidence for the universal mobility of SiC MOSFETs. Even NO passivated SiC MOSFETs are unfit for universal mobility studies since the large number of interface traps cause Coulomb scattering to be predominant among the scattering mechanisms [19-20].

2.8 Field-effect mobility

Electron traps at the semiconductor/SiO_2 interface are common in both silicon and SiC. Silicon MOSFETs can be passivated with hydrogen, significantly reducing the number of interface traps. This allows for a sharp turn-on junction for silicon MOSFETs that clearly identifies the threshold voltage. However, in SiC MOSFETs, the interface traps are not passivated with hydrogen. Even with nitric oxide passivation, the industry standard passivation method for SiC MOSFETs, a significant number of interface traps remain. These traps allow current to begin flowing in the subthreshold region of SiC MOSFETs, creating an expanded gate voltage region in which current flows. This expanded gate voltage region indicates a slow turn-on of the MOSFET and makes the exact threshold voltage undeterminable for SiC MOSFETs. Although the field-effect mobility underestimates the true mobility, it is the preferred method for measuring mobility of SiC MOSFETs [21].

Field-effect mobility is the mobility measured for the applied electric field. There are two methods to extract the field-effect mobility from a MOSFET [22]. These two methods are called the saturation method and the linear method, based upon the region examined (Figure 2-17). Since SiC does not have a clear threshold voltage, the simplified field-effect mobility models used for silicon MOSFETs are not practical. Therefore, the field-effect mobility must be

obtained from the transconductance which is only nonzero in the linear region. This restricts the drain voltage to a small value. A typical drain voltage range for SiC MOSFETs is 10-100mV.

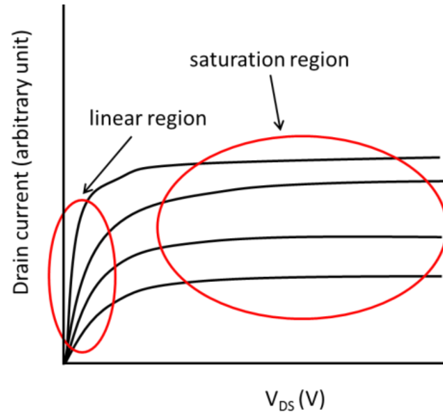


Figure 2-17. Comparison of drain current to the source-to-drain voltage (V_{DS}). The saturation region is the result of pinch-off, which restricts the current from increasing. SiC MOSFET mobility measurements are conducted in the linear region.

The definition for field-effect mobility is [21]

$$\mu_{FE} = \frac{\left(L/_{W}\right)}{C_0 V_D}\left(\frac{dI_D}{dV_G}\right)|_{V_{DS}} \tag{2.22}$$

where μ_{FE} is the field-effect mobility, L is the channel length, W is the channel width, C_0 is the capacitance/cm^2, V_D is the potential applied to the drain, I_D is the current measured between the drain and source, and V_G is the applied gate voltage. The field-effect mobility is the normalized measurement of the current running through the MOSFET. In essence, it is an efficiency

indicator for the device. Since all other components of the field-effect mobility are normalization constants, it is the change in current with respect to the change in gate voltage that determines the mobility.

2.9 Counter-doping of MOSFETs

Compensation of a doped semiconductor material with the dopants of opposite polarity is commonly referred to as "counter-doping." Specifically, this work involves counter-doping p-type SiC with n-type dopants for mobility enhancement in SiC MOSFETs. To explain the effect of a surface counter-doped layer in a MOSFET, the fundamentals of p-n junction physics will be discussed.

2.9.1 P-n junction physics

When a p-type doped semiconductor region is brought into contact with an n-type region (Figure 2-18(a)), electrons flow from the n-type region into the p-type region and holes flow from the p-type region into the n-type region. This cross-migration causes electron-hole pair annihilation in the immediate region around the junction, leaving the ions uncompensated, as shown in Figure 2-18 [23]. These uncompensated ions result in a depleted region that creates an electric field across the p-n junction (Figure 2-18(b)). The electric field forms a "built-in" potential barrier between the two doped materials.

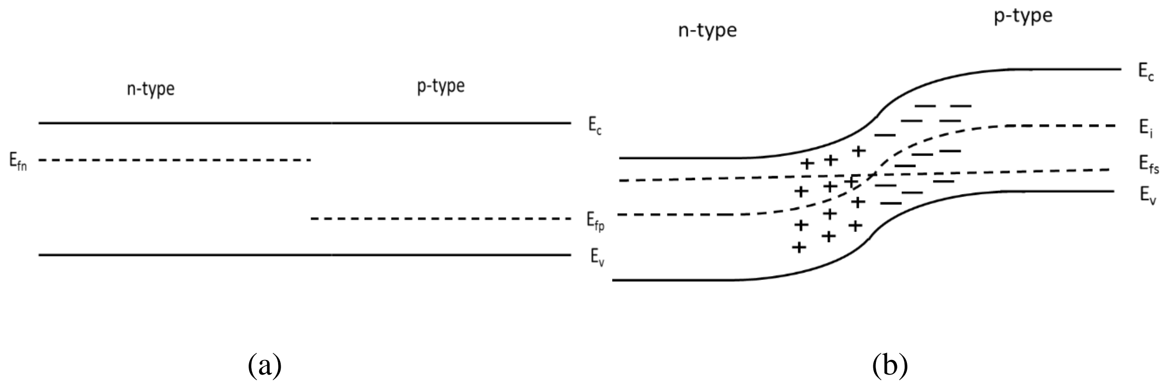


Figure 2-18. Creation of a p-n junction (a) that leads to a depletion region at the interface with an electric field created from the remaining atomic core ions (b).

The electric field across the p-n junction reduces band bending at low electric fields [24]. In addition, the electric field across the p-n junction forms a deeper channel at low electric fields (Figure 2-19(b)). The deeper channel reduces surface roughness scattering and Coulomb scattering cross-section since the electrons can flow further from the interface. For n-MOSFETs, a standard semiconductor/SiO_2 interface bends the bands down as the gate voltage increases (Figure 2-19(a)).

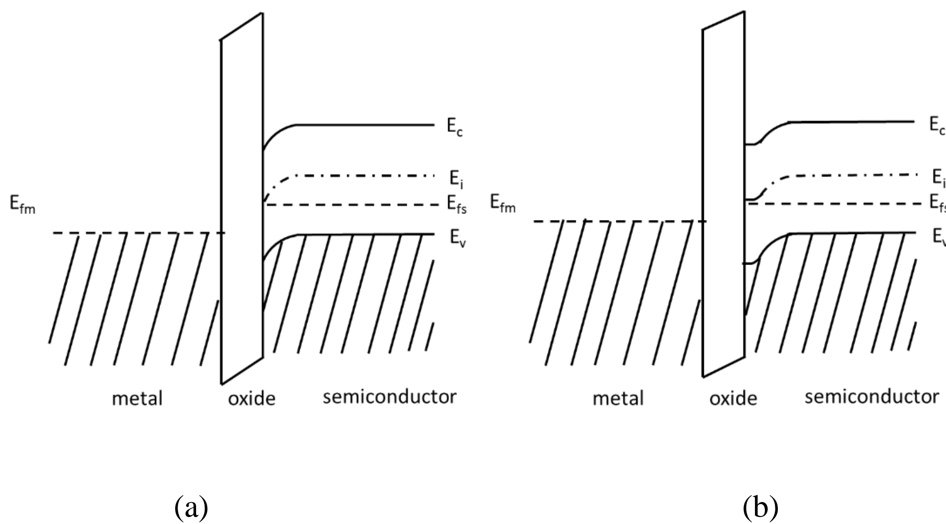


Figure 2-19. Band bending near the interface for a standard MOS (a) and p-n junction (b).

2.9.2 Counter-doping

Counter-doping is doping a doped material with the opposite polarity dopant. This work involves only doping p-type SiC with n-type dopants.

Counter-doping has both detrimental and beneficial effects on multiple properties of metal-oxide-semiconductor devices:

Detrimental effects

- flat band voltage shifts
- threshold voltage shifts
- interface charge

Beneficial effects

- increased carrier concentration
- increased channel depth at low electric fields
- band offset at low electric fields
- Coulomb screening

Counter-doping adds more positive ion cores to the interface, increasing the interface charge. The increased interface charge reduces the threshold voltage of the MOS capacitor and MOSFET. The reduced threshold voltage leads to higher leakage current in MOSFETs when the gate voltage is zero from the equation [24]

$$I_{ds} = I_0 \exp\left(\frac{V_{GS} - V_{TH}}{nV_T}\right) \tag{2.23}$$

where I_{ds} is the source/drain current, V_{GS} is the applied gate voltage, V_{TH} is the threshold voltage, V_T is the thermal voltage $V_T = kT/q$ and n is the factor

$$n = 1 + \frac{C_d}{C_{ox}} \tag{2.24}$$

where C_{ox} is the oxide capacitance and C_d is the depletion layer capacitance.

Counter-doping increases the number of ionized impurities in the semiconductor. Ionized impurities are Coulomb scattering sites, so increasing the ionized impurities near the 4H-SiC/SiO_2 interface decreases the Coulomb scattering mobility.

Counter-doping increases the number of electron carriers at the channel, increasing the concentration of carriers at all applied gate voltages (Figure 2-20). A counter-doped MOSFET has the same number of carriers at a lower gate voltage compared to standard n-MOSFETs. The increased carrier concentration also provides more electron screening, reducing Coulomb scattering.

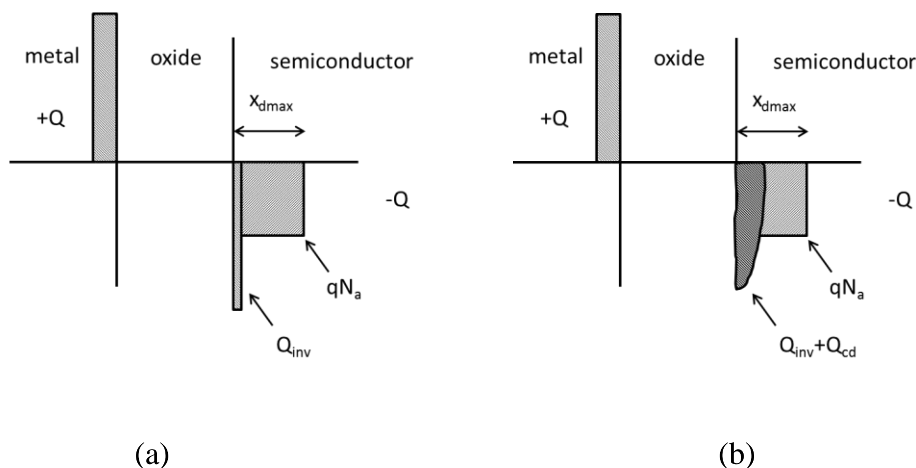


Figure 2-20. Space-charge diagrams for a standard MOSFET at threshold voltage (a) and a counter-doped MOSFET at threshold voltage (b). Q_{inv} is the charge from the inversion layer, Q_{cd} is the charge from counter-doping, q is the standard electron charge, and N_a is the number of acceptor ions.

At higher electric fields, the benefits of a deeper channel are decreased, as the channel region becomes narrower due to continued band bending. The constricted channel forces the electrons closer to the interface, increasing the surface roughness scattering which creates a bottleneck for the total electron mobility. In summary, counter-doping has the following effects on MOS devices:

- decreased threshold voltage
- sharper threshold voltage
- increased peak mobility at lower electric fields
- peak mobility that quickly decays with increased electric fields

2.9.3 Nitrogen and phosphorus counter-doping

Counter-doping is an important tool for understanding the role of passivating agents for 4H-SiC MOSFETs. Recently, it has been demonstrated that both nitrogen and phosphorus counter-dope 4H-SiC in addition to passivating the interface traps [24-25]. P. Fiorenza, et. al. developed a novel method for scanning capacitance microscopy (SCM) along the edge of several MOS capacitor devices (Figure 2-21 (A)) [25]. While the probe scanned the cross-sectional surface, a small amplitude AC (100 kHz) bias was applied to the back side of the sample [25]. The capacitance derivative dC/dV was recorded for each tip position, since the local carrier concentration is related to the amplitude of the capacitance derivative [25]. The SCM was calibrated using two known doping concentrations, the epilayer and the substrate (Figure 2-21(A)).

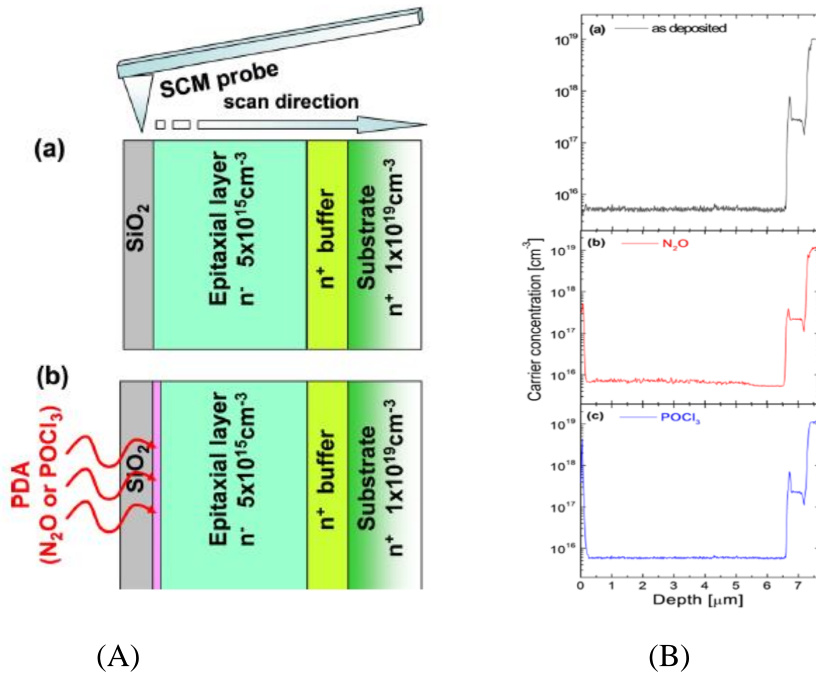


Figure 2-21. Scanning capacitance microscopy diagram [25] (A) and carrier concentration for "as deposited," N_2O passivation, and $POCl_3$ passivation samples [25] (B) (reprinted with permission from P. Fiorenza, F. Giannazzo, M. Vivona, A. La Magna, and F. Roccaforte, "SiO_2/4H-SiC interface doping during post-deposition-annealing of the oxide in N_2O or $POCl_3$," *Appl. Phys. Lett.,* Vol. 103 (2013) 153508. Copyright 2013 AIP Publishing LLC.)

Using the known epilayer and bulk carrier concentrations, P. Fiorenza, et. al. performed SCM on oxidized only, N_2O (nitrogen passivation) passivated, and $POCl_3$ (phosphorus passivation) passivated samples to demonstrate the carrier concentration effects of nitrogen and phosphorus passivated samples as a function of depth (Figure 2-21(B)). They discovered that both nitrogen and phosphorus create a thin counter-doped layer near the interface, with the carrier concentration of phosphorus nearly an order of magnitude greater than nitrogen. These results raise the question as to whether the increase in mobility from post oxidation anneal in NO or $POCl_3$ is mainly due to interface trap passivation or counter-doping effects. This question provided the motivation for the work in Chapter 4.

2.10 Vertical power MOSFETs

Vertical power MOSFETs are typically employed for high voltage power electronics [26]. Among the various vertical power MOSFET designs, the double-implantation metal-oxide-semiconductor field-effect transistor (DMOSFET) is the most popular choice for commercial SiC power switches [27]. The schematic of a DMOSFET and its operational principle are shown in Figure 2-22. The term “double-implantation” refers to the two implantations in the semiconductor (Figure 2-22). The first implantation is a moderately doped ($1x10^{17}$-$5x10^{17}$ cm^{-3}) p-type region of “p-well” that establishes where the MOS channel will form during inversion. The second implantation is a heavy (~$1x10^{20}$ cm^{-3}) n-type implant (denoted n^+ in Figure 2-22) that forms the source.

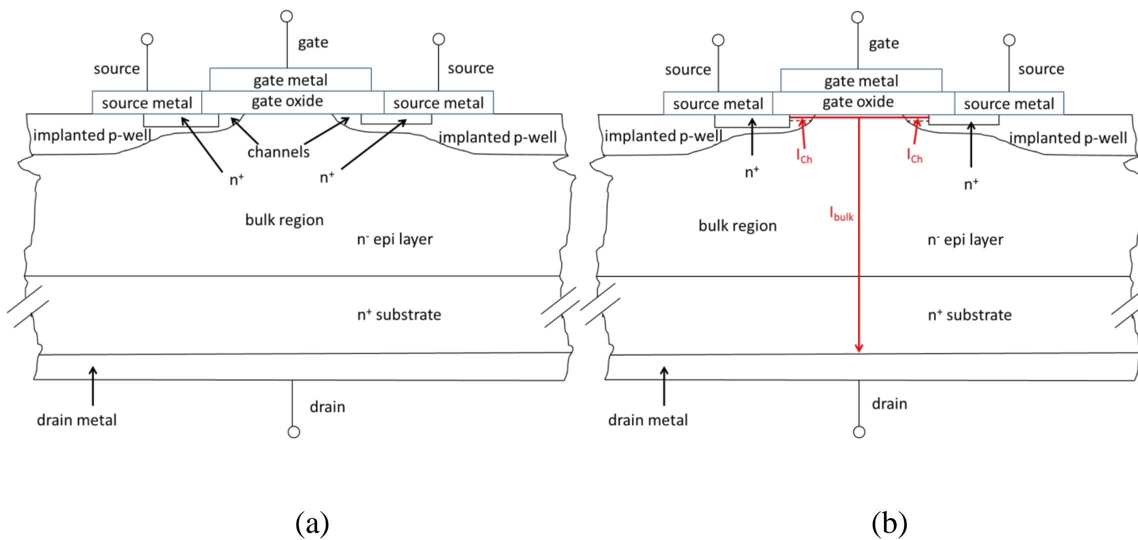


Figure 2-22. n-DMOSFET diagram. When no gate voltage (V_G) is applied, the device is off, since no current flows through it (a). When the threshold voltage (V_{TH}) is reached, inversion occurs forming the channel and current flows through the device (b).

The equation for the total mobility of a vertical power MOSFET is

$$\frac{1}{\mu} = \frac{1}{\mu_{Bulk}} + \frac{1}{\mu_{Ch}} \tag{2.25}$$

where μ_{Bulk} is the bulk mobility, and μ_{Ch} is the mobility in the channel (Figure 2-22(b)). The channel mobility is not the same as the bulk mobility, since the scattering mechanisms in the channel are different than those in the bulk. The scattering mechanisms in the bulk semiconductor are phonon scattering and ionized impurity scattering based on the doping concentration [28].

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Chapter 3. Nitrogen plasma passivation

3.1 Introduction

Nitric oxide (NO) passivation of SiC MOSFETs opened the door to commercially viable devices. Since the development of NO passivation in 2000, many studies have focused on the chemical reactions at the interface in order to improve the NO passivation process [1-5].

One of these studies, reported by Rozen et. al., indicated an important relationship that the authors called “scaling.” This scaling relationship is a proportional relationship between the nitrogen coverage at the SiC/SiO_2 interface, the number of interface electron traps (N_{it}), and the maximum mobility of the device [5] (N_{it} was derived by integrating the density of interface traps (D_{it}) from E_c - 0.2 eV to E_c - 0.6 eV).

Rozen reported that as nitrogen coverage at the interface increases, the N_{it} of the device decreases (Figure 3-1) [5]. Competing nitridation and oxidation reactions limit the maximum nitrogen coverage obtainable from standard NO passivation [3]. This limit is represented by the vertical line in Figure 3-1.

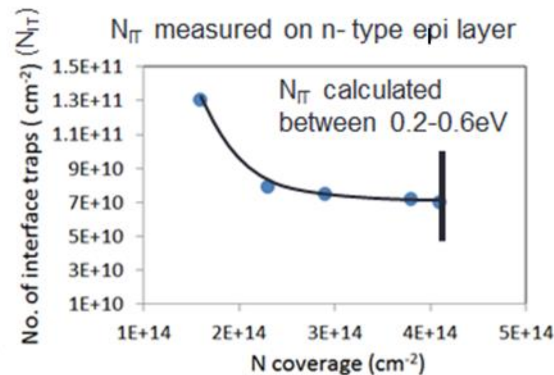
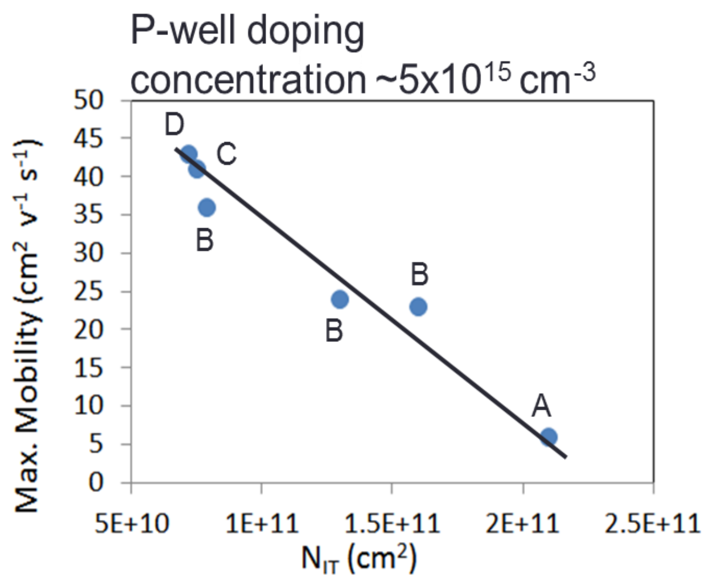


Figure 3-1. NO passivation performed for various amounts of time yielded results demonstrating the relationship between nitrogen coverage and N_{it}. NO passivation was performed at 1175°C (data from Ref. [5]). The vertical line represents the maximum nitrogen coverage obtainable from NO passivation.

The second reported relationship is that as N_{it} decreases, maximum mobility increases (Figure 3-2). Figure 3-2(a) shows increasing mobility with decreasing N_{it} achieved with the different passivation processes listed in Figure 3-2(b). These results led to the following conclusion: increasing nitrogen coverage decreases the N_{it} which increases mobility. Further increasing the mobility requires an alternative method of nitrogen passivation to overcome the limitation of NO passivation.



Letter	Process
A	Unpassivated
B	Various NO passivation times [5]
C	Standard NO passivation
D	NO followed by H_2 passivation [4]

(a) (b)

Figure 3-2. Maximum field-effect mobility versus N_{it}. Data include results from several modified NO passivation processes (a) [4-5]. Graph should be read from right to left indicated by passivation processes (b). As N_{it} decreased, maximum mobility increased.

In 2011, when these investigations commenced, nitrogen plasma passivation presented itself as a strong alternative method to NO passivation for three important reasons: it decreases oxidation; it decreases carbon liberation; it could potentially increase nitrogen coverage. First, minimal oxidation occurs during the passivation process because there is no ambient oxygen. At

Auburn University, Yogesh Sharma, a former graduate student, performed high temperature nitrogen plasma exposure on a bare SiC die with only ~10Å of oxide grown (not published). This oxide was significantly thinner than the ~50Å oxide observed after NO passivation. Secondly, publications indicated that carbon injection into the interface during oxidation was at least partially responsible for poor mobility in SiC MOSFETs [6]. Therefore, with less oxidation, primarily during the passivation process, less carbon was expected to be injected into the interface. Finally, nitrogen plasma passivation without oxidation should increase the nitrogen coverage.

3.2 Previous attempts

Previous attempts using nitrogen plasma revealed the feasibility of passivating interface traps with nitrogen without increased oxidation [7-9]. However, these attempts fell short of their objectives. The earlier processes created devices that did not increase nitrogen coverage at the interface. Also, nitrogen plasma processes created devices with oxide quality too poor for characterizing MOSFETs.

The earlier nitrogen plasma attempts used a low flow rate of nitrogen through a 600W microwave generator. This nitrogen plasma passivation process yielded only one-fifth the nitrogen coverage compared to standard NO [7]. However, two important results from this experiment laid the groundwork for this study. It demonstrated the need for an oxide recovery anneal post plasma passivation. It also confirmed that nitrogen plasma could passivate the SiO_2/4H-SiC interface.

Zhu et. al. reported that a sample cooled in nitrogen plasma had a very poor oxide (breakdown field around 2.5MV/cm compared to NO breakdown field around 9-10MV/cm) [7]. This poor oxide is due to electrical damage from ions and electrons created during the plasma process. However, performing a post passivation anneal in nitrogen with no microwave power improved the oxide breakdown field to about 6MV/cm. Although the oxide still falls short of NO, it is sufficient for MOSFET processing. Following the addition of the oxide recovery anneal, MOS capacitors and MOSFETs were successfully fabricated and characterized.

Zhu also compared D_{it} of 20h nitrogen plasma passivation to standard NO [7]. The plasma process produced nitrogen coverage less than NO, and the N_{it} was greater. However, nitrogen plasma MOSFETs had similar mobilities to NO devices, even with only one-sixth the interfacial nitrogen coverage. Still, these initial results did not reach the original goal of increasing the interfacial nitrogen coverage. Therefore, the nitrogen plasma process required modification.

To lessen the oxide degradation due to the nitrogen plasma, the process required a reduced exposure time. Decreasing the oxide exposure time to the plasma reduces the damage to the oxide. To increase the nitrogen coverage at the interface, modifications to the process included increasing the microwave power (2kW) to the plasma and increasing the nitrogen flow rate [10]. These modifications to the nitrogen plasma process decreased the exposure time and increased the nitrogen atoms available for passivation.

Instead of a thermal oxide, samples were also created starting with a thin, deposited oxide. Deposited oxide was used to minimize oxidation during the entire MOSFET process to limit carbon liberation. These “low carbon” MOSFETs underwent nitrogen plasma passivation

before they were capped with a thicker layer of deposited oxide. Nitrogen coverage and D_{it} in these low carbon MOS capacitors were similar to NO devices. Low carbon MOSFETs that were passivated with nitrogen plasma for four hours had mobilities similar to NO.

When the MOS capacitors were passivated with nitrogen plasma for eight hours, the nitrogen coverage increased nearly 250%, and the D_{it} was halved compared to NO passivated samples [10]. However, oxide quality was poor. Few MOS capacitors and no MOSFETs survived.

Other groups have also attempted nitrogen plasma passivation [8-9]. They reported results of higher nitrogen coverage and a lower N_{it}, but nothing about MOSFET mobility. None of the previous studies on nitrogen plasma passivation fully expanded on Rozen's findings. They have not entirely demonstrated that increasing the nitrogen coverage decreases the N_{it} and increases mobility. Therefore, this study focused on developing a modified nitrogen plasma passivation process that produces a good quality oxide for measureable MOSFETs and achieves a higher nitrogen coverage compared to NO.

3.3 Experimental Procedure

MOS capacitors were fabricated from two 4° off-cut n-type 4H-SiC wafers diced to 5mm x 5mm pieces. Both wafers had a 10μm epilayer with nitrogen doping densities of $4.5x10^{15}$ cm^{-3} and $6x10^{15}$ cm^{-3}. Additionally, n-channel MOSFETs were processed from 4˚ off-cut p-type epilayer 4H-SiC with aluminum doping density of $2x10^{16}$ cm^{-3}. After defining patterns with photolithography, the source and drain regions of the MOSFETs were implanted with nitrogen to a concentration of ~$6x10^{19}$ cm^{-3}. Following implantation, a 1-2μm layer of photoresist was spin

coated onto the sample surface and heated to 600˚C for 30min to carbonize the layer (carbon cap). This preserved the surface morphology during the subsequent high temperature dopant activation anneal. For the dopant activation at approximately $3x10^{19}cm^{-3}$, the samples were annealed at 1550˚C for 30min in a resistively heated annealing system in flowing Ar. The carbon cap was removed by a combination of O_2 ashing and sacrificial oxidation. Standard RCA cleaning was applied to the samples which were then used for various gate oxidation processes.

For the standard NO process, a 65nm oxide was grown by dry oxidation at 1150˚C at atmospheric pressure. A 30min in situ post oxidation anneal (POA) in Ar at 1150˚C followed the oxidation. A 2h NO POA at 1175˚C immediately followed the Ar anneal. After removing the sample from the oxidation furnace, sputtered molybdenum (Mo) was patterned (600μm circles for the MOS capacitor devices and a 200μm x 200μm length and width for the MOSFET channel region) and used for the gate metal. For the MOSFETs, $Ni_{0.93}V_{0.07}$ was sputtered for the source and drain, and a 30s rapid thermal anneal was performed at 750˚C to create a nickel silicide for the source/drain ohmic contacts.

For the nitrogen plasma process, about 15nm of thermal oxide was grown at 1150°C and atmospheric pressure followed by a 30min Ar POA anneal. Samples were then transferred to another furnace for the nitrogen plasma passivation and annealed for various times (2h, 4h, and 6h). The annealing conditions were 1160˚C, N_2 flow rate of 3.0L/min at a pressure of 2.3Torr, and 2kW power from a Cober Electronics, Inc., Stratford, CT, USA Model S6F Industrial Microwave Generator. The passivation anneal was followed by an in situ 2h plasma recovery anneal (no microwave power) at 1160˚C in a nitrogen ambient at atmospheric pressure. Following plasma treatment, about 35-50nm of SiO_2 was deposited in a LPCVD system using a tetraethylorthosilicate precursor at 700˚C and 0.5Torr. A densification anneal in nitrogen for 2h

at 850˚C immediately followed the oxide deposition. The gate and source/drain were fabricated using the same process as previously described. The benefits of using a composite oxide are explained in the following section.

3.4 Initial nitrogen plasma passivation results

Initial MOS devices had thermal oxides of ~60nm. Four hours of nitrogen plasma passivation on these samples showed promising results. However, the nitrogen coverage was similar to standard NO. To increase the nitrogen coverage, the nitrogen plasma passivation duration was increased to eight hours. Eight hours of nitrogen passivation led to MOS capacitors with poor oxide. Few devices reached accumulation during high-low capacitance-voltage (hi-lo C-V) characterization (Figure 3-3). Devices that reached accumulation were often unstable.

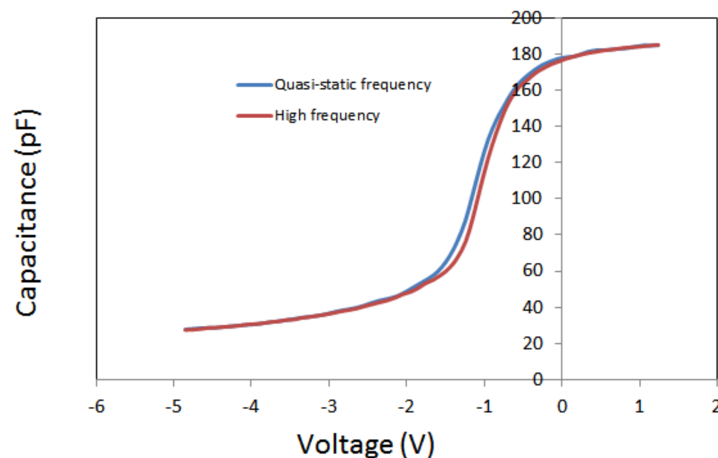


Figure 3-3. Hi-lo C-V curve for an eight-hour nitrogen plasma passivation process on 57nm oxide. The sample became too leaky for measurements going any further into accumulation.

Normal hi-lo C-V measurements have smooth high frequency and quasi-static curves. However, the quasi-static curve in Figure 3-3 has several bumps. Variances in the C-V

measurement indicate an unstable oxide. Also, these variances cause D_{it} calculations to be unreliable.

Although few MOS capacitors survived the eight-hour nitrogen plasma process, several important insights were obtained [10]. Measurements showed only half the N_{it} of NO passivation and a 250% increase of nitrogen coverage [10]. However, no MOSFETs survived eight hours of nitrogen plasma. To increase MOSFET survivability, two modifications to the process were examined.

The first modification reduced the thickness of the initial oxide before the nitrogen plasma process. After the nitrogen plasma process is completed, the thinner oxide is capped with a thick, deposited oxide. Even if the nitrogen plasma damaged the thin oxide, the thicker oxide cap ensures good insulation and allows characterization measurements to be made.

A thinner oxide may also permit qualitative characterizations of the rate-determining step for nitrogen coverage at the interface. The rate-determining step could be either the diffusion of nitrogen through the oxide or the reaction of the nitrogen at the interface. If nitrogen diffusion is the rate-determining step, then the same nitrogen coverage would be obtained in less time for the thinner oxide. Less time in nitrogen plasma reduces oxide damage. If the nitrogen reaction at the interface is the rate-determining step, the oxide thickness will not affect the rate of nitrogen coverage. Although this was not fully explored, no difference in nitrogen coverage was observed between thicker and thinner oxides.

The second modification calibrated the nitrogen plasma system to maximize the density of nitrogen atoms during the nitrogen plasma process.

3.5 Nitrogen plasma optimization

Maximizing the density of nitrogen atoms in the furnace tube increases the concentration of nitrogen available to passivate the interface. A higher density of nitrogen reduces the amount of time the samples are exposed to the plasma. To determine the nitrogen density, a monochromator placed at seven positions along the plasma tube (Figure 3-4) measured the 580nm wavelength intensity (I_{580}). The 580nm wavelength is specific to one nitrogen recombination reaction. The intensity of this wavelength is directly proportional to the square of the nitrogen atoms present in the system [11] (see Appendix L).

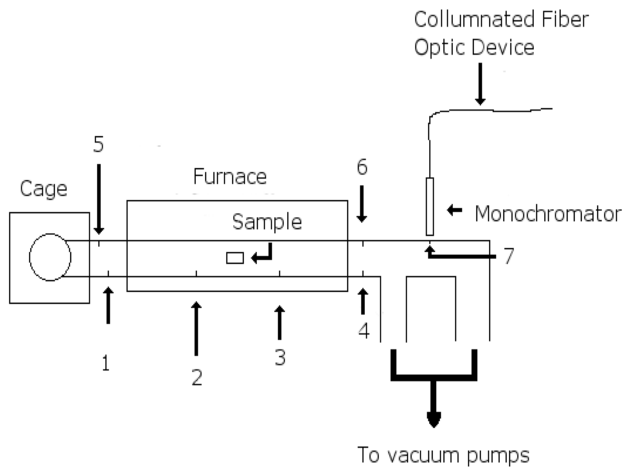


Figure 3-4. Seven positions for monochromator along nitrogen plasma furnace.

Position Number	Distance from cage (cm)
1	6
2	24
3	45
4	64
5	5
6	64
7	84

Table 3-1. Each position's distance from the cage in Figure 3-4.

The calibration was accomplished by maximizing the I_{580} at the seven locations indicated in Figure 3-4. The calibration addressed three variables: microwave power, temperature of the system, and pressure in the system.

3.5.1 Microwave power calibration

Optimum microwave power is achieved when I_{580} is maximized with the minimum amount of microwave power. The most precise I_{580} measurements are near the sample position inside the tube. Access to the tube inside the furnace is not available unless the furnace is off. Therefore, microwave power measurements were taken at room temperature. Positions 1, 2, 3, and 4 were used for the microwave power comparison (Figure 3-4).

Increasing the microwave power produced a larger intensity that also decayed at a slower rate (Figure 3-5). The change in intensity was greatest between 1kW and 1.75kW. Increasing the power above 1.75kW merely increased the length of the nitrogen plasma column. This increased length, produced by applying 2.5kW, may account for the small increases in the intensities at 24cm and 45cm. However, at 64cm, increased power showed only minimal increases in intensity, indicating that nearly all of the nitrogen recombination occurs before this position. Previous experiments at Auburn University used 2kW of microwave power [10]. Since this fell within the range of minimized I_{580} decay between positions 2 (24cm) and 3 (45cm), 2kW was chosen for the microwave power.

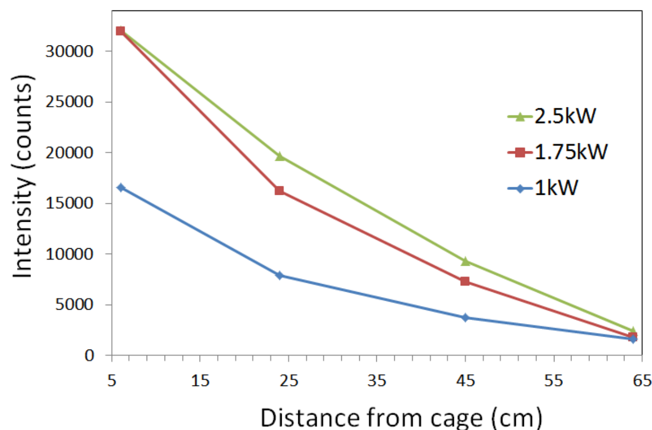


Figure 3-5. Comparison of I_{580} versus microwave power. The sample would be located close to the 35cm mark from the cage. The intensity at each position is corrected by background subtraction.

3.5.2 Temperature calibration

Calibrating temperature requires the furnace to be on. However, the four positions used at room temperature were not accessible (Figure 3-4). Positions 2 and 3 were located inside the furnace. When the furnace lid was closed, the plasma system configuration prevented access to positions 1 and 4. Position 5 replaced position 1. Although Position 5 is 1cm closer to the cage, this position is near the origin of the plasma. No change in intensity was measured between positions 1 and 5.

Position 6 replaced position 4. Although position 6 was the same distance from the cage as position 4, position 6 was on the opposite side of the tube. As the tube had some non-uniform build-up of undetermined material from use, it was not known whether position 6 and position 4 would record the exact same intensities. Therefore, position 6 was given a separate number.

Positions 5 and 6 were the initial measurement positions. However, at 900°C and higher, minimal recombination occurred at Position 6. Unexpectedly, the recombination at 900°C and

higher took place between the two tubes leading to the vacuum pump instead of at the furnace exit (Figure 3-6). To adjust for this unanticipated development, the monochromator was moved to position 7 to measure the largest I_{580} beyond the furnace exit.

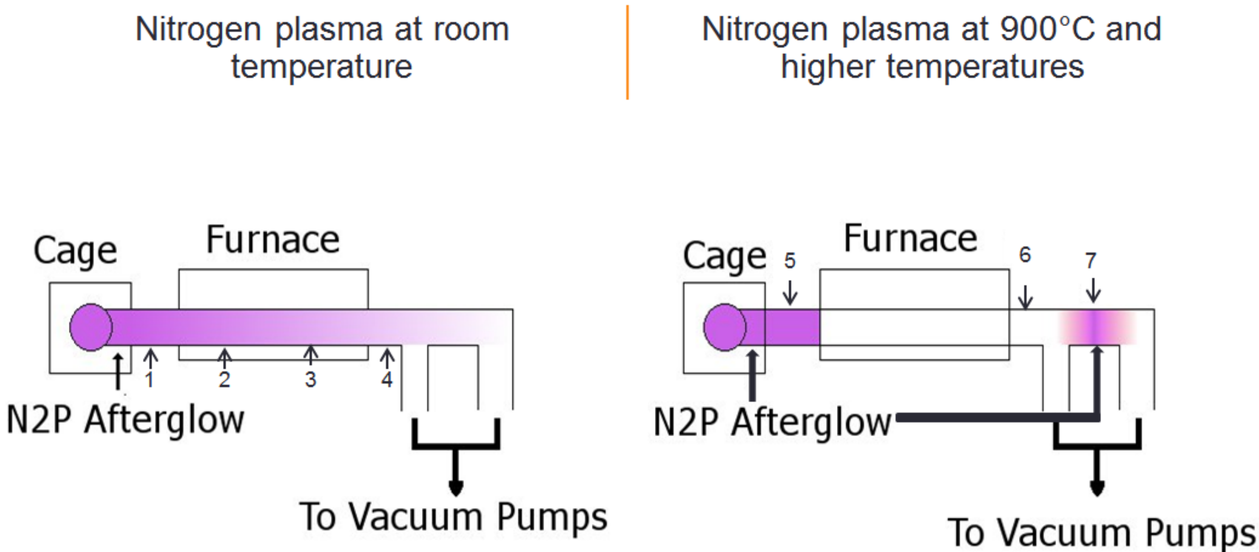


Figure 3-6. Qualitative diagram of the viewed nitrogen recombination afterglow at room temperature (left) and at 900°C and higher (right). At the furnace exit for 900°C and higher, there was no viewed afterglow and no strong I_{580} signal. The strongest I_{580} signal was at position 7, indicating the nitrogen recombination afterglow had shifted to between the two tubes to the vacuum pumps.

Measurements at positions 4 and 7 showed that as temperatures approached 1000°C, I_{580} increased (Figure 3-7). Above 1000°C, the intensity did not vary significantly. These results suggest that temperatures above 1000°C are suitable for the nitrogen plasma process. A question remained about the viability of the process at 900°C.

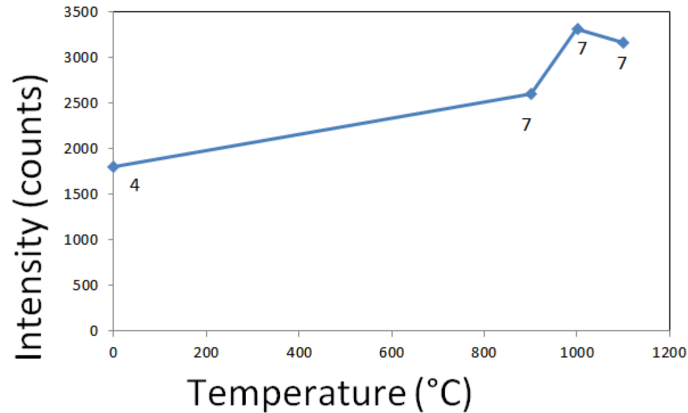


Figure 3-7. Comparison of nitrogen plasma afterglow intensity to temperature at position 4 for the first point and position 7 for the three high points. The last two points are considered to be close enough to fall within expected error range values.

Previous studies at Auburn University used 1160°C for nitrogen plasma [10]. A lower temperature plasma may be less stressful on device oxide. To test the feasibility of performing nitrogen plasma at a lower temperature, a MOS capacitor was processed using eight-hour nitrogen plasma passivation followed by a six-hour oxide recovery anneal at 900°C. However, no devices reached accumulation. Evaluations of the devices found a significantly larger dispersion between the high and low frequencies than NO and previous nitrogen plasma experiments (Figure 3-8). This indicates less nitrogen was present at the interface.

No previous study using nitrogen plasma had reported temperature dependence of the nitridation reaction at the interface. The results of using nitrogen plasma at 900° C raised concerns that the nitridation activation energy required higher temperatures. Rather than attempting to identify the optimal temperature, it was known that previous studies at 1160°C had been successful. Therefore, 1160°C was chosen as the nitrogen plasma temperature.

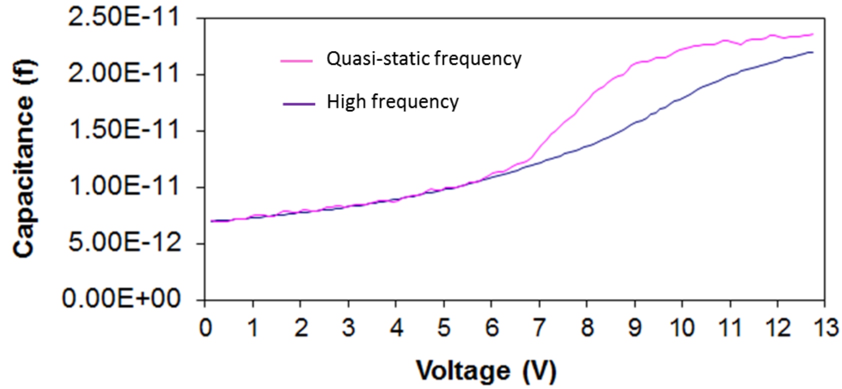


Figure 3-8. Hi-lo C-V for a six-hour nitrogen plasma passivation sample at 900°C. Samples never reached accumulation and appear to have high D_{it}.

3.5.3 Pressure calibration

The I_{580} of nitrogen plasma is sensitive to changes in pressure. To study the pressure dependence of the I_{580}, intensity measurements were conducted between 0.9-3Torr using increments of 0.1Torr. The pressure was increased by increasing the nitrogen density in the plasma tube. The intensity increased as the pressure increased between 0.9-2.2Torr. The increased nitrogen density increased the intensity. The highest intensity was in the range of 2.2-2.3Torr. As the pressure increased higher than 2.3Torr, the intensity began to decrease. This decrease occurred because of the nature of nitrogen recombination (Appendix L).

After optimizing the nitrogen plasma, MOS capacitors and MOSFETs were produced using the modified nitrogen plasma process.

3.6 Oxide quality using modified nitrogen plasma process

Previous investigations using nitrogen plasma resulted in poor oxide quality after eight hours of exposure. MOS capacitors processed by modified nitrogen plasma passivation (2kW microwave power, 1160°C, and 2.3Torr) were tested for oxide quality. These capacitors were separated into three groups based on the duration of nitrogen plasma exposure: one-hour, four-hour, and six-hour. Oxide quality was derived from current-voltage (I-V) characterizations to measure the breakdown field (Figure 3-9). The breakdown fields ranged between 4-7MV/cm, adequate for device characterization but less than NO devices (breakdown field 9-10MV/cm).

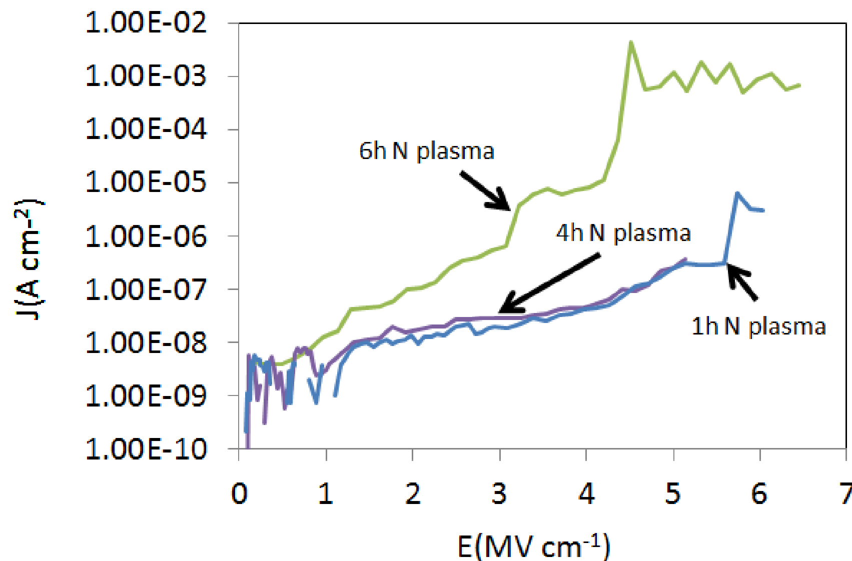


Figure 3-9. I-V characterization for different durations of nitrogen plasma passivation. The termination of the lines indicates the oxide breakdown field. The electric field (E) was obtained by V_g/t_{ox}, where V_g is the gate voltage and t_{ox} is the oxide thickness on the MOS capacitor.

Nitrogen plasma damages the oxide. This damage is repaired by turning off the microwave power and annealing the oxide in nitrogen. This process of repairing the damaged oxide is called oxide recovery. The characterization of devices exposed to nitrogen plasma for one and four hours was similar, however, the devices exposed for six hours leaked significantly

more current. The increased leakage is attributed to oxide degradation. Previous nitrogen plasma studies also reported oxide degradation for plasma exposure exceeding four hours [10]. The oxide degradation suggests a limit to a complete oxide recovery anneal. Once this limit is exceeded, the oxide will not fully recover and will have a lower breakdown field.

3.6.1 Attempts to improve six-hour nitrogen plasma MOS capacitor

To improve the breakdown field of the six-hour nitrogen plasma MOS capacitor, a longer duration of oxide recovery was introduced. Together, two MOS capacitor dies underwent a six-hour nitrogen plasma passivation. After the plasma, one die was removed from the system while the other die experienced a two-hour oxide recovery anneal. After the two-hour oxide recovery, that die was replaced by the other die which experienced a four-hour recovery anneal. Lengthening the oxide recovery reduced the current leakage at lower fields (3MV/cm and less) (Figure 3-10). At electric fields less than 3MV/cm, the die that experienced a four-hour recovery anneal showed less current leakage than the two-hour die. However, the leakage of the two dies at fields greater than 3MV/cm converged until they were nearly identical at a field of 5MV/cm. Although there is less leakage at low electric fields, a longer recovery anneal does not further improve the oxide recovery for MOSFET considerations.

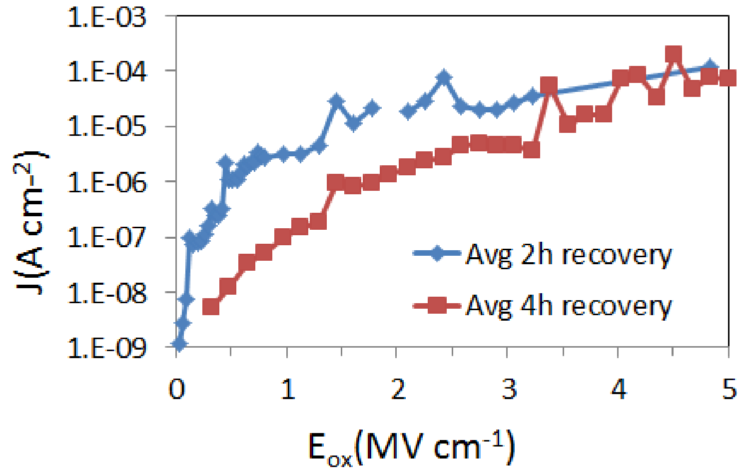


Figure 3-10. Breakdown field strength of two six-hour nitrogen plasma dies with different oxide recovery durations. Passivation and recovery were at 1160°C.

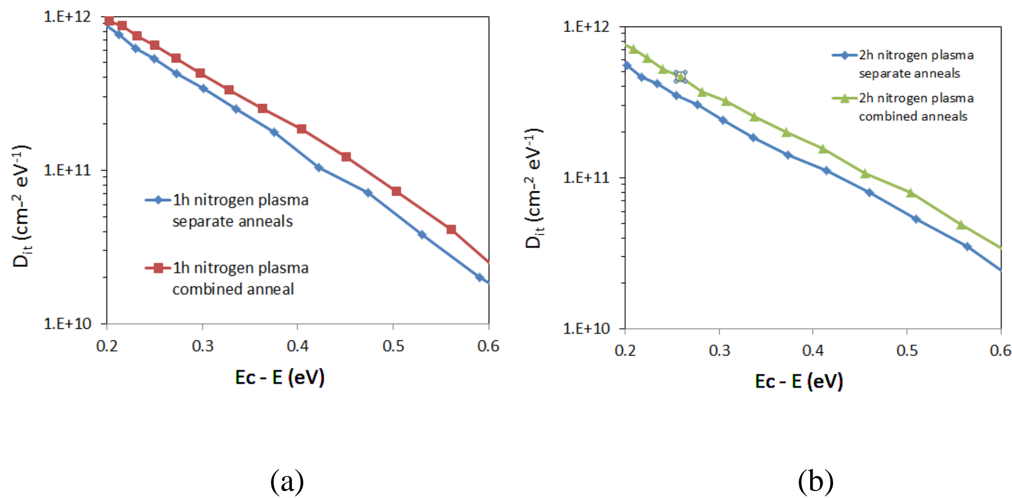
3.6.2 Attempts to shorten production process

After verifying that the oxide quality was acceptable for both MOS capacitor and MOSFET characterization, MOS capacitors were produced using the modified nitrogen plasma process. An attempt to shorten the process was conducted alongside the standard nitrogen plasma procedure. The process could be shortened by several hours if the oxide recovery anneal and the deposited oxide densification anneal could be successfully combined.

A densification anneal improves the oxide quality of deposited oxides. Deposited oxides using tetraethylorthosilicate generate silanol (Si-OH) in addition to SiO_2 [12]. During MOSFET operation, silanol can release a hydrogen atom. When the hydrogen atom departs, the oxygen atom gains a negative charge, transforming the oxygen atom into an additional oxide trap, increasing the D_{it}. However, the –OH group can be removed after oxide deposition by two hours of high temperature annealing (850°C). In order to combine these processes, the oxide anneal immediately after the plasma passivation step was removed and the temperature of the

densification step was increased from 850°C to 1160°C, the optimal temperature for oxide recovery.

Two attempts were made to combine these processes using samples obtained from one-hour and two-hour nitrogen plasma passivation procedures. These attempts were conducted in conjunction with samples produced following the standard modified procedure. This combined process produced unexpected results. For both attempts, the D_{it} was larger for the samples that combined the anneals for oxide recovery and densification (Figure 3-11) compared to samples that were processed following the modified procedure (Appendix C and D). Therefore, the attempts to combine recovery and densification proved unacceptable.



(a) (b)

Figure 3-11. Figures 3-11(a) and 3-11(b) compare the D_{it} for nitrogen plasma devices following different recovery anneal processes. The separate anneals follow the process from Appendix C and D. The combined anneals combined the oxide recovery and the densification at 1160°C.

3.7 N_{it}, nitrogen coverage and field-effect mobility

A time-dependent study of the nitrogen plasma passivation was performed using hi-lo C-V to ascertain that nitrogen plasma passivation could obtain a lower D_{it} than NO. The study

revealed that as the duration of nitrogen plasma increased, the D_{it} decreased. The six-hour nitrogen plasma had lower D_{it} than NO (Figure 3-12). Since N_{it} is derived by integrating D_{it} between E_c - 0.2eV and E_c - 0.6eV, N_{it} was successfully shown to be less for six-hour nitrogen plasma compared to NO.

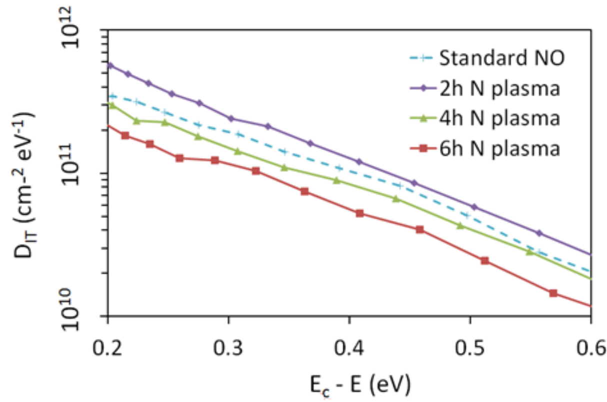


Figure 3-12. Time-dependent study of D_{it} compared to nitrogen plasma passivation duration. Standard NO is the baseline comparison.

The same devices used in the time-dependent study were then measured for nitrogen coverage using x-ray photoelectron spectroscopy (XPS). XPS is a surface-sensitive technique that determines elemental composition. The elemental composition is determined by the number and energy of electrons ejected from the surface of the material. The surface of the material is bombarded with a beam of x-rays. When these x-rays strike electrons in the material, the electrons can absorb these x-rays and gain enough energy to be ejected from their bound states. The number and kinetic energy of emitted electrons are measured from within the top 10nm of the material, the limit of this technique.

Since XPS is a surface technique, the gate oxide was removed from the samples prior to measurement. Previous XPS measurements showed that nitrogen remains at the interface after

oxide etching, similar to results from NO passivation [13]. Also, nitrogen from NO passivation and nitrogen plasma passivation has the same binding energy (Figure 3-13). Although both NO passivation and nitrogen plasma passivation have shown a decreased D_{it} [10, 14], it remained unclear whether the two processes produced different nitrogen reactions at the interface. The XPS similarities between the two processes suggest that the nitrogen serves the same role in both processes. Therefore a comparison between the two processes is valid.

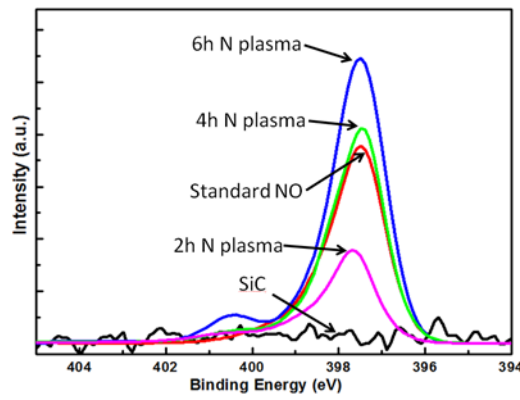


Figure 3-13. XPS profile of the N1s nitrogen at the SiO_2/SiC interface after oxide etch [20] (Courtesy of Y. Xu, Rutgers University).

XPS confirmed expectations that nitrogen coverage from nitrogen plasma passivation samples increased with increased plasma duration (Table 3-2). The nitrogen coverage in six-hour nitrogen plasma passivation was greater than NO, nearly a 50% increase. This correlates to the decrease observed in $D_{it.}$ These results demonstrate that as the nitrogen passivation duration was increased, the nitrogen coverage increased, which in turn decreased the N_{it}.

Process	Nitrogen coverage (cm^{-2})
Standard NO	3.8-4.1 x 10^{14}
2h nitrogen plasma	2.1 x 10^{14}
4h nitrogen plasma	4.4 x 10^{14}
6h nitrogen plasma	5.8 x 10^{14}
12h nitrogen plasma	6.0 x 10^{14}

Table 3-2. Comparison of nitrogen coverage for the various processes studied.

An attempt was made to explore longer nitrogen plasma exposure. A sample obtained from twelve-hour nitrogen plasma passivation produced nitrogen coverage that was only marginally higher than the six-hour nitrogen plasma sample (Table 3-2). The twelve-hour sample could not be characterized because of poor oxide quality.

None of these results achieved the nitrogen coverage previously established by the original nitrogen plasma process performed at Auburn University ($1x10^{15}$ cm^{-2}) [10]. While the nitrogen coverage from the modified nitrogen plasma process was less than previous results, the D_{it} from the six-hour modified plasma process is comparable to the D_{it} obtained from the eight-hour original plasma process [10]. A few possibilities that could account for less nitrogen coverage from the modified nitrogen plasma process are 1) The pump system was replaced on the nitrogen plasma system due to a malfunction that occurred between the two experiments. This may have caused a change in the flow of nitrogen atoms across the samples. 2) The nitrogen plasma tube was replaced due to a malfunction that occurred between the two experiments.

Nitrogen atom quenching characteristics could be different than those of the previous tube. A change in quenching characteristics could have caused an increased recombination at the tube wall, leaving less nitrogen for the passivation process. 3) The process in this study used a 10nm oxide, thinner than the 60-70nm oxide reported by Sharma [10]. This raises the question of whether oxide thickness plays some role in the total nitrogen coverage at the interface.

Although the highest nitrogen coverage obtained between the original nitrogen plasma process and the modified nitrogen plasma process differed, both processes yielded the same results when they were run for four hours. This suggests the rate-determining step for nitrogen coverage is the rate of nitrogen reaction at the interface, not the rate of nitrogen diffusion through the oxide.

For the same nitrogen coverage, the modified nitrogen plasma process has less N_{it} than the results for NO reported by Rozen et. al. [5] (Figure 3-14). This discrepancy was not fully explored, in part, because the nitrogen coverage for both processes is not known before oxide removal.

Another discrepancy between the two processes is that while the N_{it} for the NO passivation process levels off before reaching its maximum nitrogen coverage, the N_{it} for the nitrogen plasma process continues to decline, expressed by a linear relationship between N_{it} and nitrogen coverage.

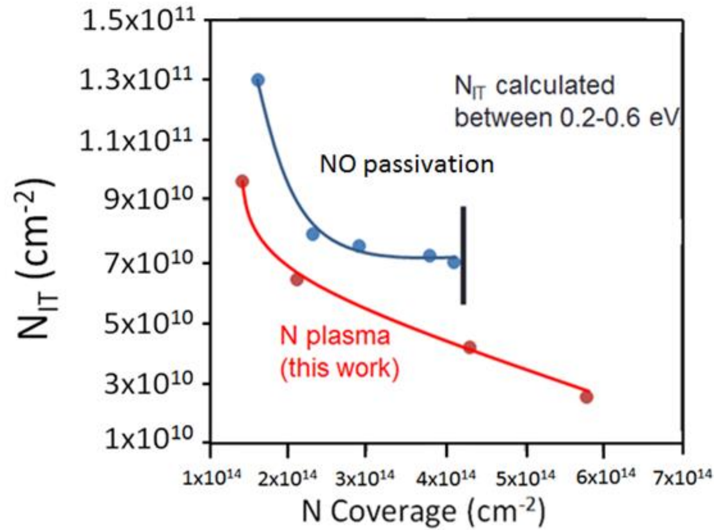


Figure 3-14. Comparison of nitrogen plasma passivation and NO passivation nitrogen coverage to the calculated N_{it}. NO passivation data is from Ref.[5].

The success using the modified nitrogen plasma process for producing the MOS capacitors justified MOSFET production. Considering the inverse proportional relationship between N_{it} and mobility, it was expected that the maximum field-effect mobility for the nitrogen plasma MOSFETs would be significantly larger than standard NO MOSFETs [5]. However, the maximum field-effect mobility of the six-hour nitrogen plasma MOSFET remained unimproved compared to NO. Unexpectedly, the peak mobility for the six-hour nitrogen plasma MOSFETs was less than both the four-hour nitrogen plasma MOSFETs and the NO MOSFETs (Figure 3-15 and Table 3-3). Although the six-hour MOSFET had the highest nitrogen coverage and the lowest measured N_{it}, it did not have the highest peak field-effect mobility among the three processes.

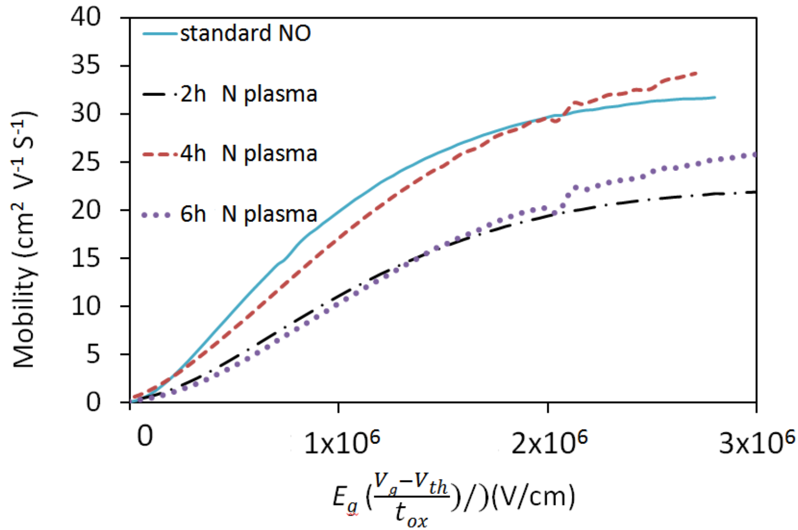


Figure 3-15. Normalized channel mobility for various MOSFET processes. The normalization corrects for different oxide thicknesses and different threshold voltages (Table 3-3).

Process	Oxide Thickness (nm)	Threshold Voltage (V)	Peak Mobility ($cm^{-2}\ V^{-1}\ s^{-1}$)
Standard NO	65	1.6	31
2h nitrogen plasma	50	1.6	22
4h nitrogen plasma	48	2.0	34
6h nitrogen plasma	53	1.2	26

Table 3-3. Comparing oxide thickness, threshold voltage as extracted from linear extrapolation of transfer curves in the linear region, and peak field-effect mobility for each process.

The six-hour nitrogen plasma process achieved the lowest N_{it}, but not the highest peak field-effect mobility, suggesting that the nitrogen scaling relationship (decreasing N_{it} increases maximum field-effect mobility) is not valid above a certain nitrogen coverage. There is a limit to the beneficial effects of nitrogen coverage at the interface. This limit suggests that some other

mobility inhibiting mechanism dominates the field-effect mobility at some threshold for nitrogen coverage.

One possible inhibiting mechanism could be additional oxide charges introduced by the nitrogen plasma. As measured by hi-lo C-V, the average effective negative oxide charge decreased with increased plasma duration (Table 3-4). This suggests that the plasma passivation process introduces more positive charges into the oxide. These positive charges may be nitrogen ions that become Coulomb scattering sites when they are near the 4H-SiC/SiO_2 interface. If the number of scattering sites increased, carrier mobility in the channel would drop. However, this is not likely the case.

Process	Oxide Thickness (nm)	Effective negative charge (cm^{-2})
Standard NO	65	3.91×10^{10}
2h nitrogen plasma	78	3.76×10^{11}
4h nitrogen plasma	68	2.00×10^{11}
6h nitrogen plasma	80	6.08×10^{10}

Table 3-4. Comparison of oxide thickness and effective charge for the various processes studied.

3.8 Nitrogen fast traps

A more likely possibility is the creation of nitrogen “fast traps” first proposed by Yoshioka, et. al. [15]. Reports from this group have linked and described the correlation between increasing the nitrogen coverage at the interface and these observed fast traps [15-16]. The nitrogen fast trap theory postulates that the introduction of nitrogen at the interface removes the

electronic traps created during oxidation. However, nitridation introduces new traps very near the conduction band that can react to the high frequency mode in a standard high-low frequency capacitance-voltage (hi-lo C-V) measurement.

Hi-lo C-V characterization assumes that the high frequency is too high for electrons to react (Chapter 2.3). Therefore, these electrons remain static and do not contribute in calculating the capacitance (ΔQ/ΔV). However, when fast traps are present, electrons in these traps react to the high frequency, increasing the measured high frequency capacitance (Figure 3-16). This causes the true density of interface traps to be underestimated, since D_{it} is derived by comparing the difference between the measured high frequency and the quasi-static frequency capacitances.

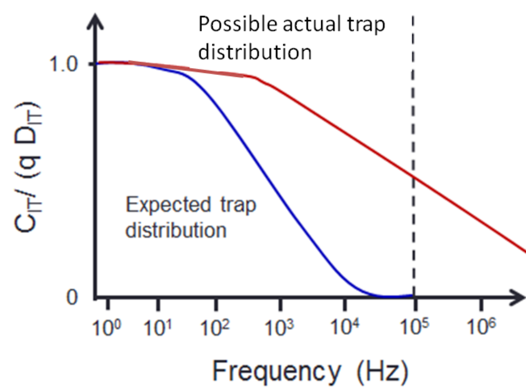


Figure 3-16. Expected trap distribution compared to possible actual trap distribution with fast traps using the percentage of interface trap capacitance (C_{it}). The high frequency may not be high enough to prevent all electron traps from reacting to it.

If standard hi-lo C-V characterization is not detecting fast interface traps, the calculations for D_{it} and N_{it} are unreliable. These errors in N_{it} may account for the field-effect mobility results observed for the six-hour nitrogen plasma. If nitrogen is creating new traps, then the higher nitrogen coverage may have introduced more traps into the interface. This may have caused the

slight decrease in the field-effect mobility for the six-hour nitrogen plasma compared to the four-hour nitrogen plasma and NO.

To overcome the limitations of hi-lo C-V, Yoshioka et. al. proposed a new method to correct for these fast traps (C-ψ_s method) [16]. The C-ψ_s method, or capacitance-surface potential, uses the data from hi-lo C-V measurements to calculate an ideal high frequency capacitance curve to which no traps contribute (Figure 3-17). Since all traps already respond to the quasi-static frequency, no modifications are made to the quasi-static frequency data. Adjusting the high frequency capacitance to ideal values leads to greater accuracy in determining D_{it}.

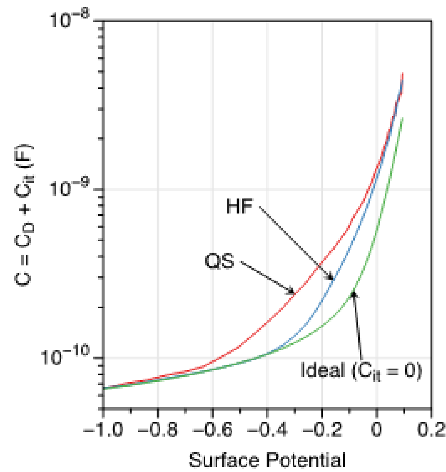


Figure 3-17. Quantifiable quasi-static frequency (QS) and high frequency (HF) compared to the ideal high frequency (Courtesy of D. Morisette, Purdue University).

Hi-lo C-V and C-ψ_s methods were used to evaluate D_{it} results on six-hour nitrogen plasma MOS capacitors (Figure 3-18). The C-ψ_s method produced D_{it} nearly an order of magnitude greater than hi-lo C-V. The C-ψ_s method was used to compare the D_{it} of MOS

capacitors using the six-hour nitrogen plasma, the four-hour nitrogen plasma, and NO (Figure 3-19). The differences in D_{it} among these three MOS capacitors was not nearly as large as measurements obtained by hi-lo C-V.

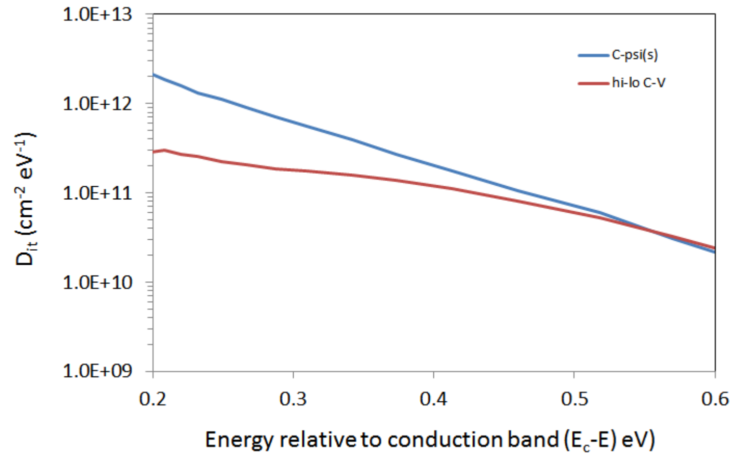


Figure 3-18. C-ψ_s and hi-lo C-V characterization of a six-hour nitrogen plasma passivated MOSFET. D_{it} is relative to the energy from the conduction band. There is nearly an order of magnitude difference in D_{it} between the C-ψ_s and hi-lo C-V method.

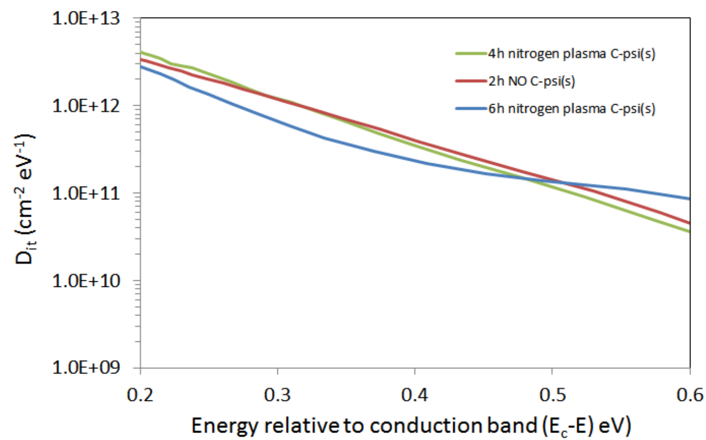


Figure 3-19. C-ψ_s comparison of 2h NO, 4h nitrogen plasma, and 6h nitrogen plasma D_{it}.

The D_{it} obtained from the C-ψ_s method prompted a revisit to the nitrogen scaling relationship proposed by Rozen et. al. [5]. Since the D_{it} was comparable among all three MOS capacitors, the scaling relationship predicted that the field-effect mobility from the MOSFETs should also be comparable. These three mobilities were comparable, providing additional support for the validation of the C-ψ_s method and the scaling relationship.

3.9 Conclusions

The modified nitrogen plasma passivation process successfully calibrated the nitrogen plasma and produced functioning MOS capacitors and MOSFETs. This process produced MOSFETs with a nitrogen coverage nearly 50% higher than the standard NO passivation process. With more refined calibration, it may be possible to further increase nitrogen coverage. Hi-lo C-V and XPS measurements demonstrated decreases in N_{it} associated with increases in nitrogen coverage. Unexpectedly, the decreased N_{it} did not increase the maximum field-effect mobility.

A likely reason for this discrepancy is the creation of nitrogen fast traps, described and studied by Yoshioka et. al. [16-17]. The fast traps react to the high frequency signal during the C-V measurement using the high-low method, resulting in the underestimation of the D_{it} at the 4H-SiC/SiO_2 interface.

The C-ψ_s method corrects this underestimation providing a more accurate value of the D_{it}. This method uses data from hi-lo C-V measurements to create a theoretical model of an ideal C-V curve for which no traps react. This ideal curve is substituted for the measured high frequency in hi-lo C-V, and D_{it} is adjusted accordingly.

Using the C-ψ_s method, D_{it} is comparable for the processes of NO, four-hour nitrogen plasma, and six-hour nitrogen plasma. These comparable D_{it} could account for the similar field-effect mobilities among the three processes. The C-ψ_s method suggests that there is a limit to the beneficial effects of nitrogen passivation at the interface.

Nitrogen removes some electron traps, but it creates other near band edge traps that cannot be measured by standard hi-lo C-V. Therefore, the initial assumption that increasing nitrogen coverage reduces N_{it} is incorrect. Decreasing N_{it} is highly likely to increase the maximum field-effect mobility, but the decrease cannot be achieved with nitrogen alone.

3.10 References

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Chapter 4: Counter-doping with heavy dopants Sb and As

4.1 Introduction

SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) have historically had poor channel mobility due to large numbers of electron traps at the SiO_2/4H-SiC interface. Nitric oxide (NO) passivation of the interface reduces the number of interface traps, which increases the maximum field-effect mobility for these devices. Field-effect mobility continues to increase as the number of interface traps (N_{it}) decreases (Figure 4-1) [1]. Various other processes, including phosphorus passivation, produced a similar scaling relationship between N_{it} and maximum mobility [2-5]. Although phosphorus passivation produced the lowest N_{it} and highest maximum mobility, phosphorus passivation has its own unique set of challenges not associated with NO passivation.

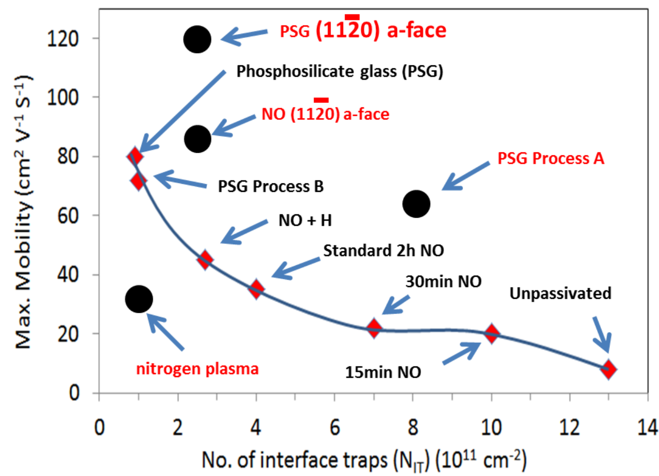


Figure 4-1. A representation plot demonstrating that maximum field-effect mobility increases as the number of interface traps decreases [1-5]. Black circles represent recent studies that do not align with previous scaling results.

Phosphorus interacts with the oxide during annealing in a P_2O_5 ambient, changing the oxide (SiO_2) into phosphosilicate glass (PSG) (P_xSiO_y) [3]. PSG has polar characteristics that introduce additional problems for MOSFET operation. Under an applied electric field, certain PSG bonds align with the electric field, resulting in large shifts of the flat band voltage (V_{FB}) and the threshold voltage (V_{TH}). Large shifts in the threshold voltage during operation cause devices to be unreliable. A process that minimizes the negative effects of PSG while still retaining high mobility during operational conditions was developed at Auburn University [3]. However, this process has been difficult to replicate. This is partly due to the recent finding that instability in PSG is a result of an intricate interplay between polarization and electron trapping that depends on the concentration of phosphorus in the PSG [C. Jiao, Auburn University, unpublished].

Complicating matters further, several recent studies of nitrogen passivation and phosphorus passivation have not aligned with the scaling results in Figure 4-1. These results are indicated with black circles in Figure 4-1 and include results from nitrogen plasma passivation (Chapter 3) [4], a modified phosphorus passivation process performed at Auburn University (PSG Process A), and nitrogen passivation and phosphorus passivation results on the a-face $(11\bar{2}0)$ of SiC [5].

After the groundwork for this study was completed, new studies addressed some of the recently encountered inconsistencies in Figure 4-1. The discovery of nitrogen induced fast traps by Yoshioka et. al. makes the argument for the scaling relationship shown in Figure 4-1 less compelling [6-7]. Using the simultaneous high-low capacitance-voltage (hi-lo C-V) method, measurements showed that as the nitrogen coverage concentration at the interface increases, the number of interface traps decreases. However, the hi-lo C-V method cannot detect the fast traps created by nitrogen passivation, leading to an underestimation of the true number of interface

traps (see Chapter 3.8). Since all N_{it} measurements in Figure 4-1 were obtained from hi-lo C-V, the reported N_{it} is less than the actual N_{it}.

A recent study by Yoshioka et. al. comparing the field-effect mobility to D_{it} on the Si-face, C-face, and a-face suggests that nitrogen passivation on the a-face may produce less nitrogen fast traps than produced on the other two crystalline faces [8]. Less fast trap production might explain why the maximum field-effect mobility of the NO passivation on the a-face of SiC is larger than NO passivation on the Si-face, but other results reported by Yoshioka et. al. showed that, for the same D_{it}, field-effect mobility on the a-face is at least 1.5 times greater than field-effect mobility on the Si-face or C-face [8]. Yoshioka et. al. gave no explanation for this inconsistency, however they established that the increased field-effect mobility for the a-face was not due to changes in the effective mass which is inversely proportional to the field-effect mobility [8].

Since it is known that field-effect mobility measurements on the a-face of SiC result in larger maximum mobilities compared to the Si-face and C-face, the NO a-face and PSG a-face points in Figure 4-1 should only be compared to each other and not with Si-face field-effect mobility points. The NO and PSG a-face points in Figure 4-1 highlight an inconsistency as both points have nearly the same number of interface traps, yet the PSG point has a much higher maximum mobility [5].

Recent studies of phosphorus passivated a-face yielded unexpected results: phosphorus passivates electron traps at the interface, but additionally, it acts as a counter-dopant (see Chapter 2.8 for counter-doping) [5]. Another study has shown that both nitrogen and phosphorus act as counter-dopants and passivating agents (Chapter 2.8.1) [9]. Therefore, it is difficult to determine

whether the increase in field-effect mobility is due to the passivation of interface traps or due to counter-doping.

To differentiate the counter-doping from trap passivation, arsenic and antimony were chosen as donor dopants in this study. Arsenic and antimony are column V elements, as are nitrogen and phosphorus, therefore they share many properties. However, due to the larger atomic radii of arsenic and antimony, these elements were not expected to passivate interface traps. Also, arsenic and antimony have heavier atomic weights (5-8 times heavier than nitrogen), providing more accurate control over thinner ion implantation profiles.

4.2 Antimony and arsenic MOSFET process

Long channel lateral MOSFETs (150μm length x 290μm width) were constructed from 4° off-cut $6x10^{15}$ cm^{-3} Al-doped Si-face SiC 5x5mm dies (Figure 4-2). Implanted square nitrogen wells created source and drain regions. A graphitic carbon cap was formed on the Si-face (Appendix I) to protect the samples before the 1550°C activation anneal. The carbon cap protects the surface of the SiC from roughening during high temperature anneals [10]. Following the activation anneal, a 10nm oxide was grown under the following conditions: 1.15h at 1150°C in O_2. Samples were divided for antimony implantation (Sb) and arsenic implantation (As). Similar arsenic and antimony implantation profiles and concentrations were achieved under the following conditions: $2.2x10^{13}$ atoms/cm^2 dose at 80keV (antimony) and $2.2x10^{13}$ atoms/cm^2 dose at 60keV (arsenic).

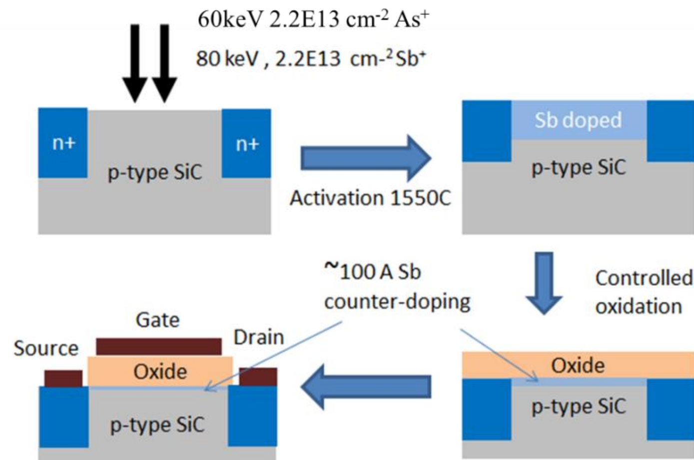


Figure 4-2. Implanted antimony MOSFET process flowchart. Antimony was implanted into SiC followed by antimony activation anneal. Various thicknesses of thermal oxide were grown on SiC during MOSFET production.

Following implantation, a carbon cap was again formed on the surface of the Si-face (Appendix I). The samples underwent a 30min activation anneal at 1550°C for antimony and arsenic. Following the activation anneal, a 70nm gate oxide was grown for 11h at 1150°C in O_2 followed by a 30min argon post oxidation anneal ("Sb only" or "As only"). Other samples received a 30min nitric oxide (NO) passivation anneal at 1175°C ("Sb+NO" or "As+NO").

After gate oxidation, the samples were patterned with 5124-E photoresist and molybdenum was sputtered as the gate metal. Next, the source and drain were patterned and etched using a combination of reactive ion etching and a 10s buffered oxide etch dip immediately before Ni was sputtered as the source and drain contacts. Finally, a 30s rapid thermal anneal at 800°C created a nickel silicide for improved ohmic contacts.

Companion metal-oxide-semiconductor capacitors (MOS capacitors) were processed alongside each antimony and arsenic MOSFET through the gate application process. The MOS

capacitors received a back oxide etch in buffered oxide etch before they were mounted on gold-plated alumina for characterization.

4.3. Results and discussion

Implanted antimony and arsenic SiC dies were processed side-by-side into MOSFETs maintaining identical implantation dosage, implantation profile, activation anneal temperature, and activation anneal time. The measured field-effect mobilities for the arsenic and antimony MOSFETs suggest that in the interface region, arsenic has a smaller ionization energy than antimony (Figure 4-3). Therefore, the difference in the mobilities can be attributed to a larger carrier concentration for arsenic, a consequence of more activated arsenic ions.

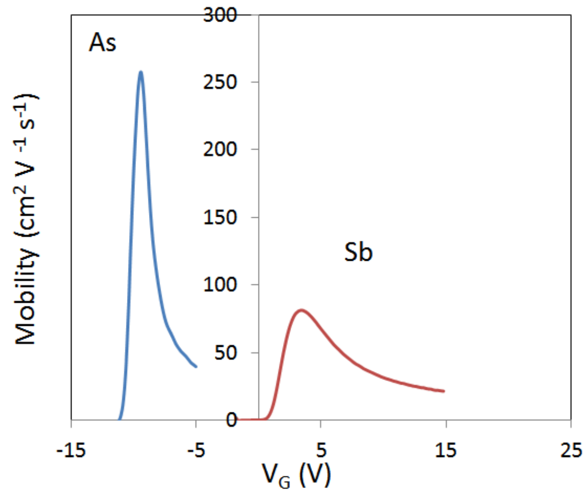


Figure 4-3. Arsenic (As) and antimony (Sb) mobility plot for ~70nm dry, thermal oxide. Arsenic MOSFETs have a large negative threshold voltage, while antimony MOSFETs have a positive threshold voltage.

The large negative threshold voltage, sharp turn-on, and large, but narrow, peak mobility of the arsenic MOSFET are indicative of a buried channel MOSFET. A buried channel MOSFET

is similar in design to a lateral MOSFET, except that an impurity implantation of the opposite type of the substrate (e.g. n-type impurity in p-type substrate) is implanted deeper into the semiconductor, away from the semiconductor-oxide interface (Figure 4-4) [11]. If the implanted impurity generates enough minority carriers in the substrate to switch the type, a channel is formed between the source and drain, including when the applied gate voltage is zero, so the MOSFET is "normally-on."

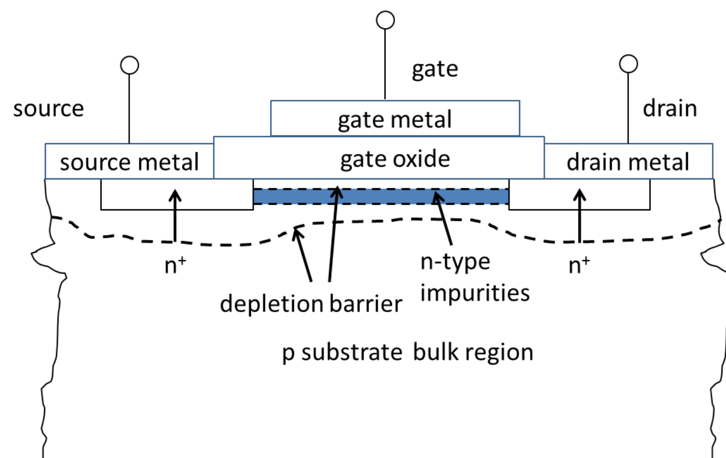


Figure 4-4. Buried channel MOSFET diagram on p-type substrate. The implanted n-type impurities form a n-type channel between the source and drain.

For a p-type substrate, a large negative gate voltage is necessary to turn off a normally-on MOSFET. The large negative gate voltage depletes the n-type channel until the two depletion regions merge and pinch off the current [11]. As the gate voltage increases from the point where the channel is pinched off, the channel forms and the MOSFET field-effect mobility rapidly increases toward its peak.

The large peak field-effect mobility occurs because the channel carriers are not confined to the semiconductor-oxide interface, avoiding the effects of any interface scattering. Antimony and arsenic implantation profiles (Chapters 4.3.1 and 4.3.2.) indicate that the implanted

impurities (antimony and arsenic) are within 60nm of the 4H-SiC/SiO_2 interface. As the gate voltage increases, the electrons in the channel are pulled toward the interface and surface roughness limits the mobility, indicated by the sharp drop in mobility from the peak.

Although the increased carrier concentration and increased maximum field-effect mobility are advantageous for vertical power MOSFETs, the large negative threshold voltage of the normally-on arsenic buried channel MOSFET makes it unsuitable for commercial applications. The antimony MOSFET, however, retained a positive threshold voltage and a maximum field-effect mobility larger than NO passivated MOSFETs. Consequently, this study focused on three effects of antimony as a counter-dopant:

- Modeled and experimental implant profiles and concentrations
- MOS capacitor characterization
- MOSFET field-effect mobility

4.3.1 Secondary ion mass spectrometry

To accurately verify the modeled implantation profile and dosage, experimental antimony implant profiles and dosages were measured. Also, to examine the effects of the activation anneal on the implanted antimony, measurements of the implant profiles and dosage after the activation anneal were necessary. These two measurements required a process that measured both concentration and depth of antimony in the MOS capacitors: secondary ion mass spectrometry (SIMS).

To obtain depth profiles of antimony in the silicon dioxide and silicon carbide, SIMS analysis was performed. To this end, the samples were sent to a commercial vendor[12] In the particular SIMS process used [13], Cs^+ ions were used to sputter surfaces of samples creating secondary ions that are collected by a mass spectrometer. The mass spectrometer identifies the element and concentration of the secondary ions and their depth below the surface of the sample material. SIMS performed in this study has a detection limit of only $5x10^{17}$ atoms/cm^3. Concentrations at this lower limit or less are treated as zero for recorded purposes. The raw SIMS data accounts only for the Sb_{121} isotope, or about 57% of total antimony concentration [14]. All SIMS antimony data is adjusted to account for this discrepancy.

4.3.2 Implantation model and SIMS results

Stopping and Range of Ions in Matter (SRIM) software modeled the implantation profiles for antimony and arsenic (Figure 4-5). In Figure 4-5, the modeled profile is represented by the solid, black line. Two SiC dies implanted with the same species were processed simultaneously until the activation anneal process. Only one die underwent the activation anneal. The experimental implantation profile, measured by SIMS, is represented by the dashed, blue line. The similarity between the two profiles indicates that the modeled profile was accurate.

The red dotted line indicates the antimony profile after the activation anneal. The post activation anneal results indicate that the activation anneal does not cause a significant out-diffusion of antimony.

After the activation anneal, a sacrificial oxide was grown. The purpose of the sacrificial oxide is to clean microscopic carbon cap residue remaining on the SiC surface and to protect the

sample surface during storage. Generally, the sacrificial oxide is removed immediately before MOSFET processing begins. However, to accurately profile the amount of antimony in the SiC after the activation anneal, the sacrificial oxide was not removed.

When SiC is consumed during oxidation, the resultant SiO_2 expands. The resultant SiO_2 is nearly 1.8 times thicker than the consumed SiC, making a direct 1:1 comparison of SiO_2 depth to SiC depth inaccurate. A conversion factor of 0.55 multiplied by the oxide thickness produces an acceptable approximation of the thickness of the consumed SiC.

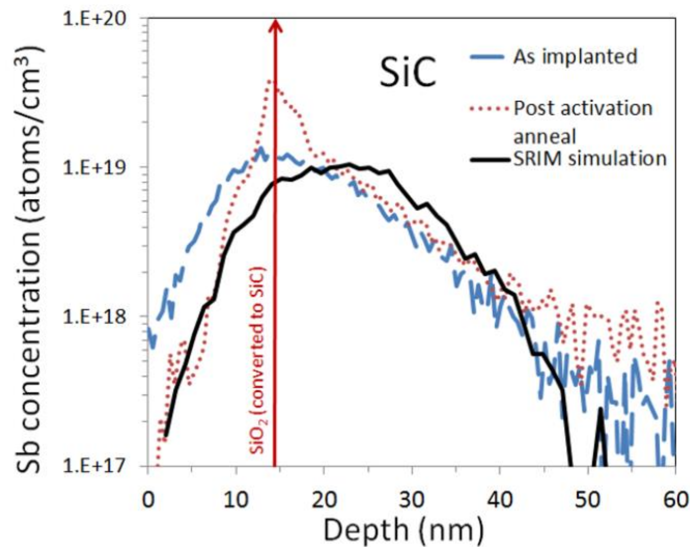


Figure 4-5. Comparison of the modeled antimony profile (SRIM) with the implanted and post activation anneal results obtained from SIMS.

To first order, SIMS measurements may be used to designate the location of the interface between the SiO_2/4H-SiC at the depth where oxygen is half its maximum concentration. In Figure 4-5, the red line labeled "SiO_2 converted to SiC" indicates the location of the sacrificial oxide SiO_2/4H-SiC interface. This interface is only present for the samples that underwent post activation anneal followed by a formation of a thin oxide layer. For the antimony as-implanted

profile, this "interface" is missing since the implantation was performed on a bare SiC surface. Everything to the left of the "interface" line is SiO_2, while everything to the right of the line is SiC. To account for the difference in thicknesses between SiO_2 and SiC, the measurement of the SiO_2 layer was reduced to approximate the amount of SiC consumed by introducing the previously discussed conversion factor of 0.55.

After verifying that the modeled antimony implantation profile was consistent with the experimental antimony implantation profile and that the activation anneal did not significantly affect the antimony implantation profile, MOS capacitors were processed with varying oxide thicknesses (Figure 4-6).

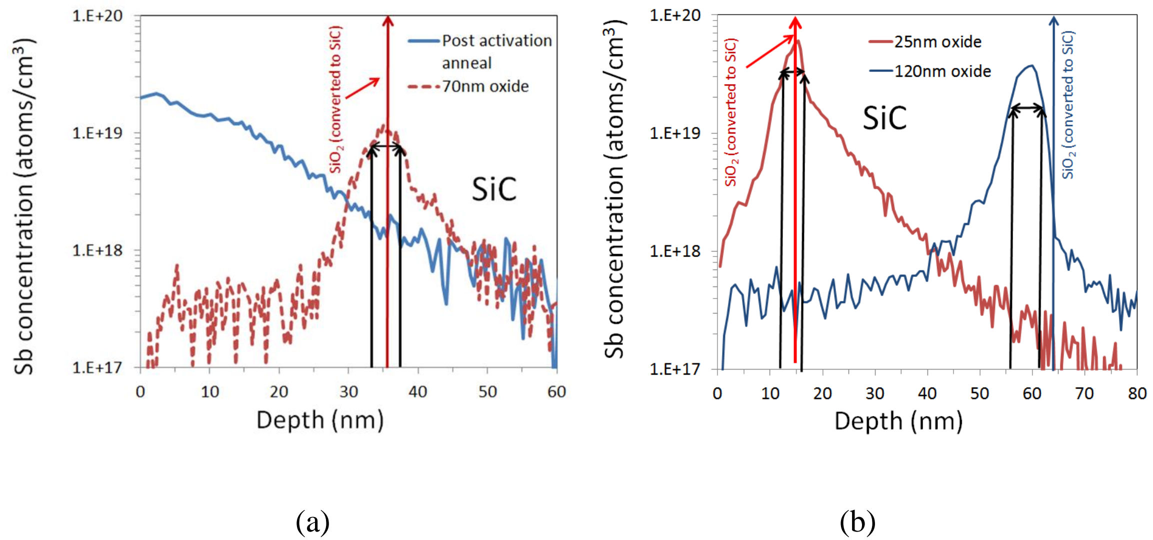


Figure 4-6. Comparison of SIMS results from a post activation anneal and a 70nm oxide (a). Comparison of SIMS results from a 25nm oxide and a 120nm oxide (b).

SIMS was performed on two MOS capacitors from the same implantation batch (Figure 4-6(a)). One of the MOS capacitors was measured after the activation anneal and the other MOS capacitor was measured after 70nm of oxidation. Comparing the two implantation profiles

suggests that the peak concentration of antimony follows the SiO_2/4H-SiC interface. As more SiC is consumed to form SiO_2 during oxidation, the peak antimony concentration moves deeper into the SiC.

Figure 4-6(b) reveals this shifting antimony concentration peak more clearly than Figure 4-6(a). In Figure 4-6(b), implantation profiles for a 25nm oxide and a 120nm oxide are compared. The 120nm oxide consumed enough SiC during oxidation to go deeper into the SiC than the "as-implanted" implantation profile. However, SIMS displays a strong antimony concentration centered at the SiO_2/4H-SiC interface. Comparing the positions of the peak antimony concentrations for the 25nm oxide and the 120nm oxide revealed an approximately 50nm shift of the peak position into the SiC.

In addition to the peak antimony concentration shifting position with the interface, the antimony concentration is larger at the interface for a variety of oxide thicknesses compared to the activated anneal antimony concentration. The antimony concentration at a depth of 35nm is nearly an order of magnitude greater in the 70nm oxide sample compared to the activated annealed sample (Figure 4-6(a)). The antimony concentration for the 120nm oxide at 60nm SiC depth is 10^{19} atoms/cm^3, while the 25nm oxide has no antimony present at a 60nm SiC depth (Figure4-6(b)). The increased antimony concentration at the SiO_2/4H-SiC interface suggests that the oxidation process pushes the antimony deeper into the SiC.

For the different oxide thicknesses, measurements were made of the total antimony, antimony in the oxide, and antimony in the 4H-SiC and compared in Table 4-1. For both sets (activated anneal and 70nm oxide; 25nm oxide and 120nm oxide) of MOS capacitors, the total antimony decreased as the oxide thickness increased. Although the results indicate that some

antimony is lost during oxidation, more experiments are required to determine an accurate antimony loss rate compared to SiC consumed.

Process	Total Sb (atoms/cm^2)	Sb in oxide (atoms/cm^2)	Sb in SiC (atoms/cm^2)
Activation anneal	$2.2x10^{13}$	N/A	$2.2x10^{13}$
25nm oxide	$1.61x10^{13}$	$1.04x10^{13}$	$5.66x10^{12}$
70nm oxide	$5.52x10^{12}$	$4.40x10^{12}$	$1.36x10^{12}$
120nm oxide	$1.24x10^{13}$	$1.19x10^{13}$	$4.4x10^{11}$

Table 4-1. Calculated antimony and location based on SIMS results. The interface location was determined at the point where the oxygen concentration was half its maximum amount. Sb in oxide and Sb in SiC were calculated using antimony only within the full width at half height.

The information from Figure 4-6 and Table 4-1 suggest the following conclusions: 1) antimony is lost during the oxidation process; 2) antimony concentrates near the interface on the oxide side; and 3) oxidation seems to push antimony toward the interface.

Antimony loss due to out-diffusion is a possibility based on previously reported rates of antimony diffusion through SiO_2 [15]. Aoyama, et. al. implanted antimony into SiO_2 and then annealed the implanted SiO_2 for varied lengths of time. SIMS results comparing antimony profiles in the SiO_2 before and after the anneals revealed that antimony can diffuse through

several hundred nanometers of SiO_2 within 10h of annealing at 1200°C [15]. Since the oxide thickness of MOS devices in this study are between 25-120nm, it suggests that out-diffusion of antimony through the oxide is possible. However, more investigation is necessary to understand the out-diffusion process.

4.4 Antimony high-low capacitance-voltage characterization

Simultaneous high-low frequency capacitance-voltage (hi-lo C-V) characterization was performed on antimony implanted MOS capacitors (Figure 4-7). One set of antimony MOS capacitors underwent an activation anneal. Without the activation anneal, the antimony implanted MOS capacitors are similar to unpassivated MOS capacitors (Figure 4-7(a)). The flat band voltage of the unactivated MOS capacitors is larger than the activated MOS capacitors, and the divergence between the high frequency and low frequency measurements is larger. This indicates that the unactivated MOS capacitors have a greater density of interface traps than the activated MOS capacitors.

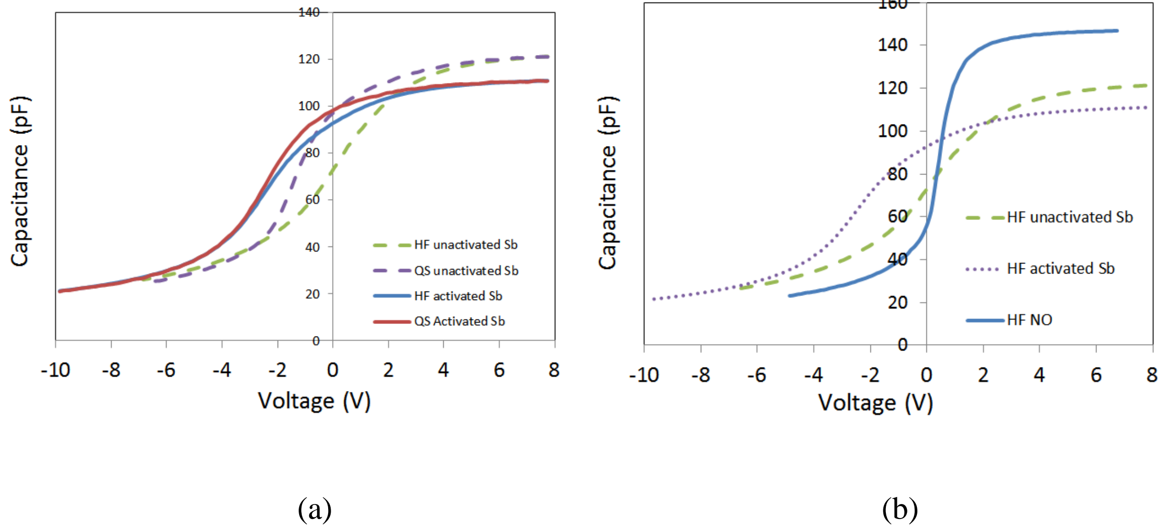


Figure 4-7. High frequency (HF) and quasistatic frequency (QS) of activated and unactivated antimony MOS capacitors. The divergence of the high and low frequency curves is less for the activated sample (a). High frequency (HF) curves for the unactivated antimony, activated antimony, and standard NO MOS capacitors. Both antimony C-V curves are stretched-out compared to the NO curve (b).

The high frequency C-V for unactivated antimony, activated antimony, and NO passivated MOS capacitors is compared in Figure 4-7(b). Both the activated and unactivated antimony MOS capacitors had C-V curves that were stretched out compared to the NO passivated MOS capacitor. Assuming that the stretch-out is mostly attributed to the density of interface traps (D_{it}), antimony passivation appears minimal. Direct D_{it} calculations for antimony were not performed due to the non-uniform doping of the antimony MOS capacitors.

Qualitatively, the simultaneous high-low C-V results appear contradictory. Comparing the C-V measurements for the activated and unactivated antimony MOS capacitors indicates a reduction in interface traps that could be associated with interface trap passivation. However, the stretched out high frequency curves for antimony compared to the high frequency curve for an NO passivated MOS capacitor seems to indicate little passivation occurs. Due to the ambiguity

of the results reported in Figure 4-7(a) and Figure 4-7(b), experiments were performed to determine if activated antimony passivated interface traps in addition to counter-doping near the interface. Other possible reasons for this could be (1) the stretch-out is related to the non-uniform doping, or (2) there are more slow traps in the unactivated sample but the same number of fast traps.

4.5 Antimony acts only as a counter-dopant

Three characterization methods were used to test whether antimony passivated the interface:

- Low temperature mobility
- Constant capacitance deep-level transient spectroscopy (CCDLTS)
- Low temperature hi-lo C-V

4.5.1 Low temperature mobility

If antimony passivates the SiO_2/4H-SiC interface traps, the channel mobility would increase. However, at room temperature, effects other than trap passivation could cause an increase in channel mobility for the antimony MOSFETs. A buried channel MOSFET removes the effects of surface roughness scattering, increasing the channel mobility at low oxide electric fields. Also, the increased number of carriers from counter-doping helps with Coulomb screening. Measuring mobility at low temperatures reduces the effects of counter-doping in two important ways:

1) As the temperature decreases, Coulomb scattering mobility decreases (Chapter 2.6.1). At low temperatures, Coulomb scattering mobility becomes the mobility limiting factor in interfaces with large D_{it} (Matthiessen's rule Chapter 2.5). Therefore, the Coulomb mobility largely controls differences in mobility between different processes at low temperatures.

2) At low temperatures, dopant freeze-out can occur. Dopant freeze-out occurs when significantly fewer donor electrons are elevated into the conduction band. The probability equation for an electron to occupy a donor state is

$$n_d = \frac{N_d}{1 + \frac{1}{2} exp\left(\frac{E_d - E_F}{kT}\right)} \tag{4.1}$$

where n_d is the density of electrons occupying the donor level, E_d is the energy of the donor level, E_F is the Fermi energy level, k is the Boltzmann constant, T is temperature, and N_d is the concentration of donor states [16]. At 300 K, few electrons occupy the donor level, indicating nearly all of the electrons are in the conduction band.

At 0 K, each donor state is occupied by an electron, so $n_d = N_d$ which implies $exp\left(\frac{E_d - E_F}{kT}\right) = 0$ (see Equation 4.1). This occurs when the Fermi energy is greater than the donor energy (Figure 4-8) [16]. As the temperature increases, the probability for electrons to occupy the conduction band increases. Therefore, at temperatures near 0 K, some electrons are thermally excited to the conduction band while the majority occupies the donor level; this is called partial ionization [16].

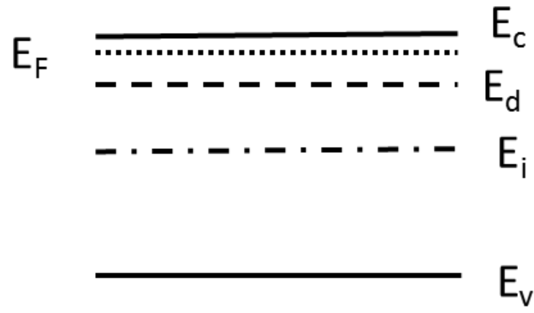


Figure 4-8. Band diagram of dopant freeze-out in semiconductor. The Fermi energy (E_F) is between the dopant energy (E_d) and the conduction band (E_c).

Field-effect mobility was recorded for two groups of MOSFETs: antimony implanted (Sb-only); antimony implanted followed by nitric oxide passivation (Sb+NO) (Figure 4-9). Low temperature measurements were performed in an Advanced Research Systems PSF-10-1-4 vacuum cryo-chamber. Field-effect mobility was measured at 70 K and 298 K.

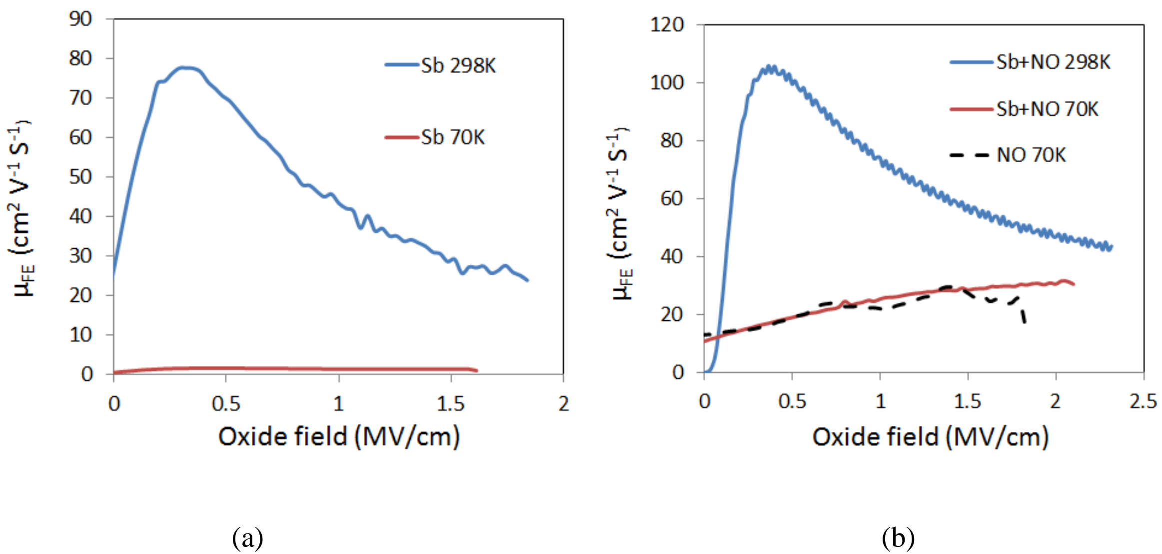


Figure 4-9. Low temperature field-effect mobilities of Sb-only (a) and Sb+NO (b) MOSFETs.

At 70 K, the field-effect mobility for the Sb-only MOSFET was significantly less than the Sb+NO MOSFET. The Sb-only MOSFET has a field-effect mobility less than 10 $cm^2 V^{-1}s^{-1}$, similar to a SiC MOSFET processed with only a thermal oxide. However, the Sb+NO MOSFET field-effect mobility at 70 K was nearly identical to the standard NO MOSFET. The differences between the 70 K field-effect mobility of the Sb-only and the Sb+NO MOSFET imply that the increased mobility of the Sb+NO MOSFET is caused by nitrogen passivation of the interface traps. Antimony does not appear to have any passivation effects, since the Sb-only MOSFET is similar to an unpassivated SiC MOSFET, and the Sb+NO MOSFET is similar to a NO passivated MOSFET at 70 K.

Although antimony has the lowest theoretical ionization energy of dopants in bulk SiC [17], the ionization energy of antimony near the SiO_2/4H-SiC interface is not known. If the ionization energy of antimony is greater at the interface, freeze-out of antimony at the interface would occur at a higher temperature than the temperature for freeze-out to occur for antimony in bulk SiC. Antimony freeze-out is the most likely reason for the increased channel resistance at low temperatures.

4.5.2 Constant capacitance deep-level transient spectroscopy

Deep-level transient spectroscopy (DLTS) is a technique to study electrically active defects in semiconductors and interfaces. All of the DLTS measurements discussed in this study were performed at Simon Fraser University. DLTS measurements are based on changing the occupancy of deep level traps by changing the bias and temperature [18-19]. Changing the bias

fills the deep level traps which are emptied by heating. When electrons leave the deep level traps, the capacitance increases, causing a capacitance transient [19].

In DLTS, the rate of change of the capacitance transient in a fixed emission rate window is measured as the temperature is varied [19]. The transient capacitance is then plotted as a function of temperature. If the measurements produced curves with peaks, each peak represents a specific energy level for traps that have an electron emission rate within the preset time window. Sharp peaks are usually observed for bulk point defects in semiconductors, and broader peaks are typical for interfacial defects.

Constant capacitance deep-level transient spectroscopy (CCDLTS) is similar to DLTS except that instead of measuring the capacitance transient from deep level electron emission, the gate voltage is adjusted to maintain a constant capacitance throughout the emission rate window [20]. The gate voltage variations are related to the number of deep level traps that emit electrons [20].

In this work, CCDLTS at Simon Fraser University was used to compare the defect sites that nitrogen is known to passivate in two different MOS capicitors: NO and Sb+NO (Figure 4-10). The two primary defects are the oxide defects O1 and O2 [21]. Both Sb+NO and NO MOS capacitors had nearly identical concentrations of O1 and O2 defects, indicating that antimony does not perform interface trap passivation. Interface trap passivation is performed by nitridation at the interface.

A third defect, bulk defect B1, was observed in some samples and was independent of device processing. Therefore, the observance of the B1 peak in the NO MOS capacitor and absence in the Sb+NO MOS capacitor measurements does not provide significant insight. The

B1 defect peak was ignored in this study, so the trap passivation comparison between the "NO-30" and "Sb-implanted" (Figure 4-10) was performed by observing only the defect sites O1 and O2.

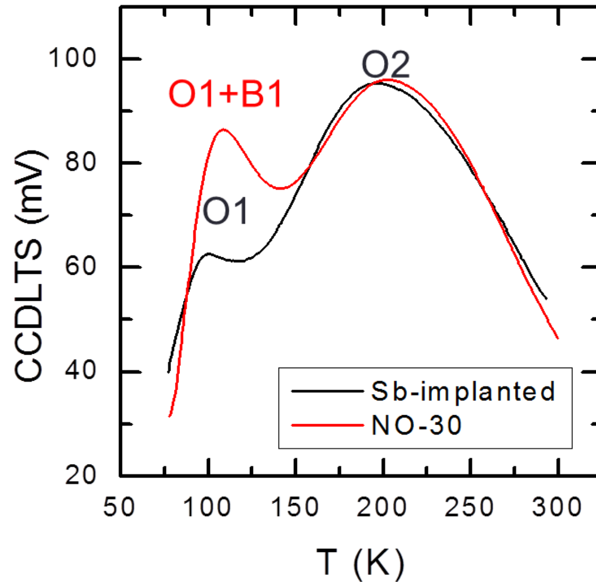


Figure 4-10. Constant capacitance deep-level transient spectroscopy of an Sb+NO (Sb-implanted) and NO passivated (NO-30) MOS capacitor. Defect sites O1 and O2 are nearly identical for both NO and Sb+NO MOS capacitors. For unknown reasons, the B1 defect site was observed in some samples and absent in others, independent of device processing. Thus, defect site B1 is removed from consideration of trap passivation (Courtesy of P. Mooney, Simon Fraser University).

4.5.3 Low temperature C-V

Low temperature C-V measurements of NO and Sb-only MOS capacitors revealed a flat band voltage shift of 9V for the Sb-only MOS capacitors compared to a flat band voltage shift of only 1.5V for the NO MOS capacitors (Figure 4-11). These flat band voltage shifts at low temperatures indicate the amount of acceptor-like traps near the interface that are energetically located close to the conduction band of 4H-SiC. Therefore, the greater shift in the flat band

voltage of the Sb-only MOS capacitors suggests a higher density of interface traps in the Sb-only MOS capacitors.

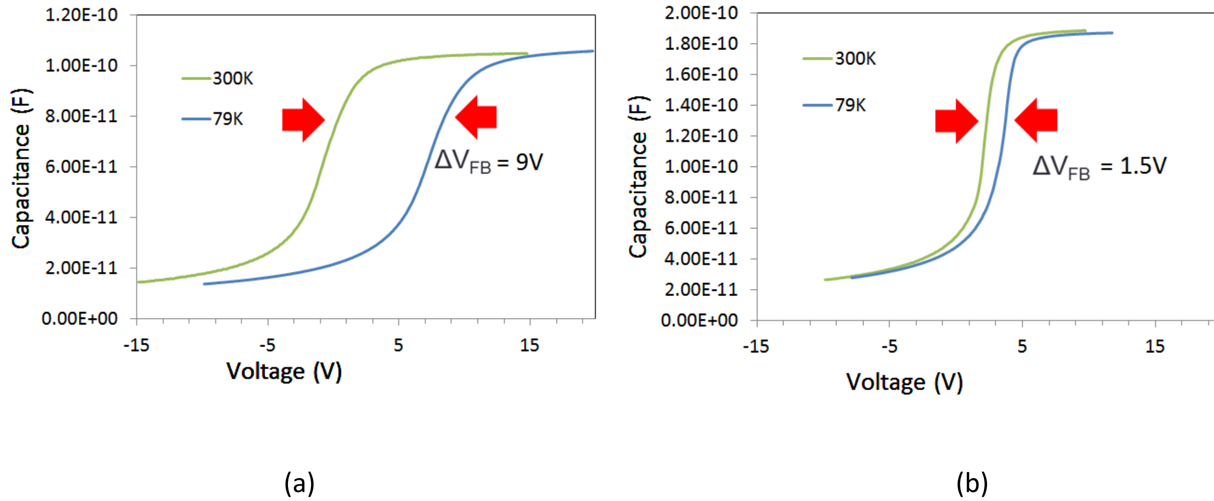


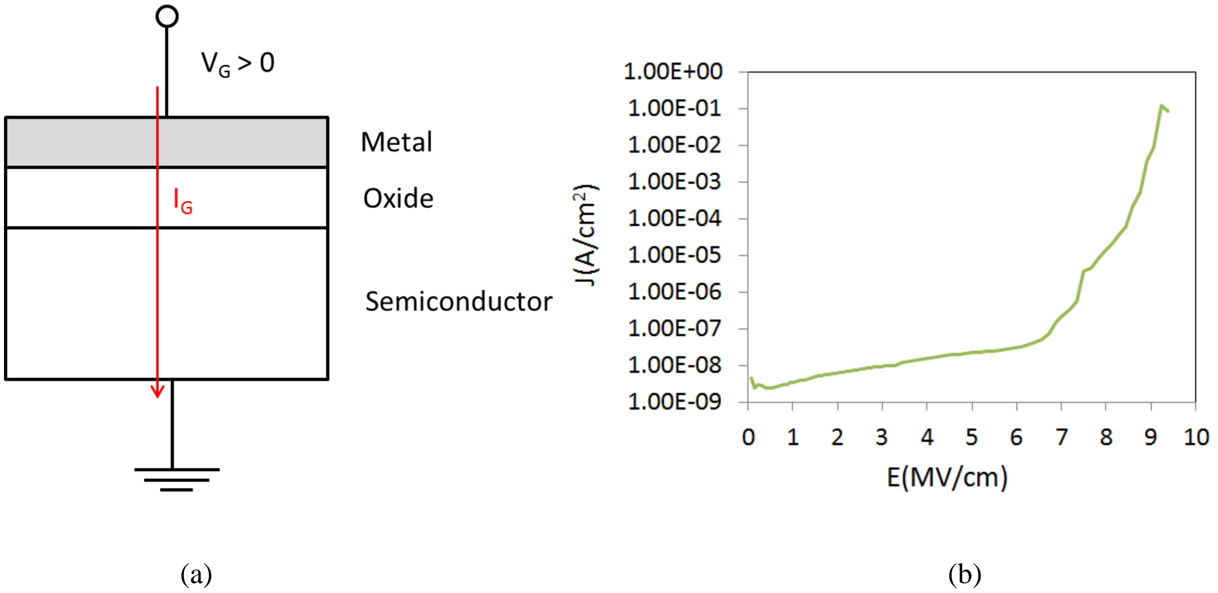
Figure 4-11. Simultaneous hi-lo C-V measurements at 300 K (green line) and 79 K (blue line) for Sb-only MOS capacitors (a) and NO MOS capacitors (b). The red arrows indicate the flat band voltage shift.

4.6 Antimony implanted MOS capacitor breakdown field

The increased number of crystalline defects created during the antimony implantation process raised concerns about the counter-doping process because increasing the crystalline defects increases the leakage of the gate oxide formed from the damaged material.

To examine gate oxide leakage, current-voltage (I-V) characterization was performed on antimony implanted MOS capacitors. For MOS capacitors, I-V characterization measures current leakage across the oxide (Figure 4-12(a)). High quality SiO_2 can effectively block current up to an applied electric field of 8-9MV/cm. Oxide on antimony implanted MOS capacitors effectively

blocked current up to 7-8MV/cm (Figure 4-12(b)), indicating that the antimony implantation did not cause a significant defect increase in the SiO_2.



(a) (b)

Figure 4-12. Diagram of current-voltage characterization (a) and current-voltage plot for an antimony implanted device (b). The breakdown electric field is 7-8MV/cm.

4.7 MOSFET field-effect mobility

The I-V results for the antimony MOS capacitors indicated that implanted antimony MOSFETs are viable. Antimony (Sb) and antimony with NO passivation (Sb+NO) MOSFETs were processed as discussed in Chapter 4.2, and the field-effect mobilities were measured as a function of oxide electric field shown in Figure 4-13. The electric field was approximated using the formula

$$E_{ox} = \frac{V_g - V_{TH}}{t_{ox}} \tag{4.2}$$

where E_{ox} is the oxide electric field, V_g is the gate bias, V_{TH} is the threshold voltage, and t_{ox} is the oxide thickness. The oxide electric field normalizes field-effect mobilities to account for different oxide thicknesses and threshold voltages among MOSFETs.

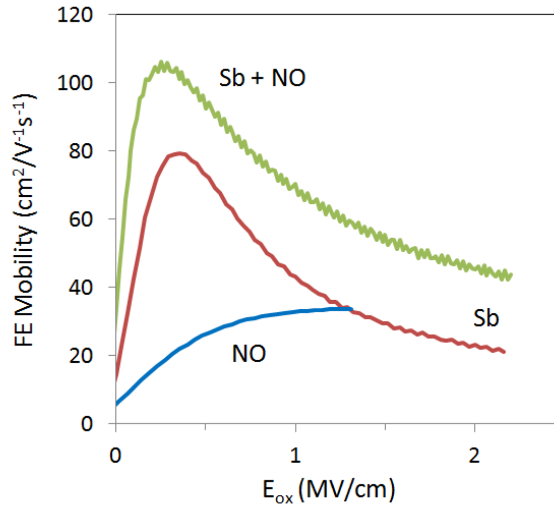


Figure 4-13. Comparison of field-effect mobility for the NO, antimony (Sb), and antimony with NO passivation (Sb+NO) processes. These measurements were conducted at room temperature.

Sb-only MOFSETs have a maximum field-effect mobility of about 80 $cm^2\ V^{-1}s^{-1}$ at low fields, which decreases to ~20 $cm^2\ V^{-1}s^{-1}$ around 2MV/cm. Extrapolating the mobility into higher oxide electric fields indicates that the field-effect mobility may decrease to ~10 $cm^2\ V^{-1}s^{-1}$ or lower. However, the Sb+NO MOSFETs have a maximum field-effect mobility of 110 $cm^2\ V^{-1}s^{-1}$ and the field-effect mobility remains larger than the NO passivated MOSFETs to at least 2.5MV/cm. For both Sb-only and Sb+NO MOSFETs, the sharp decline from the peak field-effect mobility with increased oxide field was expected because surface roughness scattering mechanisms become the dominant limiting factor for field-effect mobility at larger electric fields [22-23].

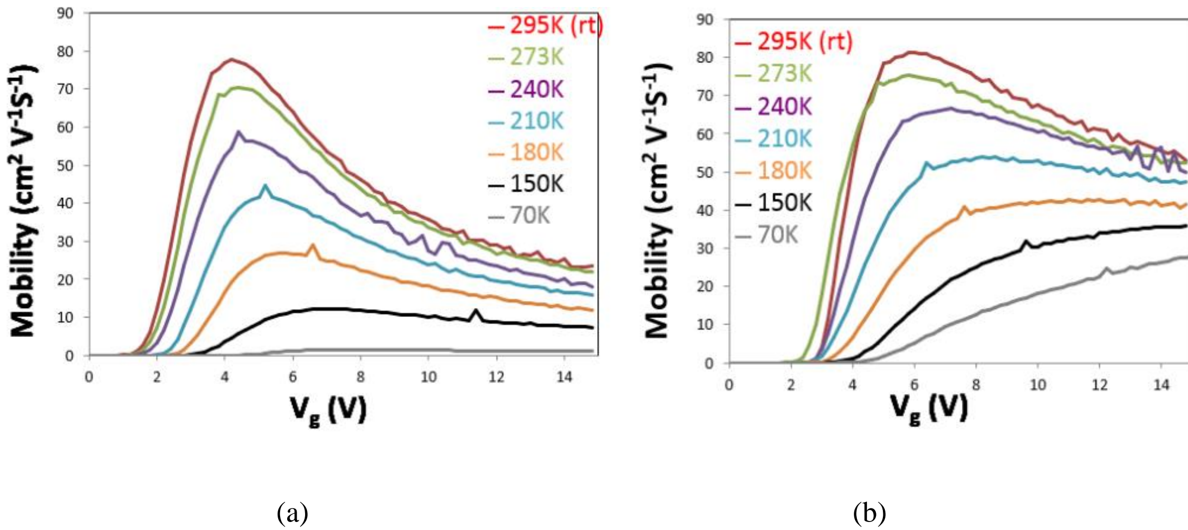
Threshold voltages associated with the different processes are listed in Table 4-2. The threshold voltage of the Sb-only MOSFETs is low compared to NO passivated MOSFETs, as expected for counter-doping [24]. Combining NO passivation with antimony counter-doping further reduces the threshold voltage. However, while counter-doping causes a left-shift in the threshold voltages, all three threshold voltages remain positive, supporting the viability of the antimony counter-doping process.

Process	Threshold Voltage (V)
NO	2
Sb-only	1.5
Sb+NO	1

Table 4-2. Comparison of threshold voltage for standard NO, Sb-only, and Sb+NO processes.

4.7.1 Coulomb scattering mobility

Coulomb scattering has the greatest influence on field-effect mobility at low temperatures and low oxide fields since Coulomb scattering mobility is proportional to temperature (Chapter 2.6.1). The temperature dependence of the channel mobility in the 70 K to 295 K range was performed on Sb-only and Sb+NO MOSFETs in an Advanced Research Systems PSF-10-1-4 vacuum cryo-chamber. The field-effect mobilities as a function of temperature is shown in Figure 4-14.



(a) (b)

Figure 4-14. Temperature dependence of field-effect mobilities for Sb-only (a) and Sb+NO (b) MOSFETs.

At temperatures 240 K and lower, the rate of change of the maximum field-effect mobility is larger for Sb-only MOSFETs than the Sb+NO MOSFETs. The greater rate of change indicates a larger Coulomb scattering effect on the mobility, stemming from the larger number of interface traps.

For Sb-only MOSFETs, field-effect mobility decreases with temperature across the entire range of applied gate voltages. However, for Sb+NO MOSFETs, the field-effect mobilities begin to converge at larger gate voltages. This difference in behavior suggests, at large gate voltages, Coulomb scattering still dominates the scattering mechanisms for the Sb-only MOSFETs, while surface roughness scattering dominates the Sb+NO MOSFETs.

4.7.2 Phonon mobility

At high temperatures, phonon scattering becomes the dominant scattering mechanism in MOSFETs (Chapter 2.6.3). High temperature field-effect mobility measurements of Sb+NO MOSFETs indicate increased phonon scattering since the maximum field-effect mobility decreases with increasing temperature (Figure 4-15). This evidence supports the conclusion that phonon mobility is the limiting factor at low oxide fields and high temperatures. However, as was observed during the low temperature mobility measurements, at larger oxide fields, the mobilities converge, suggesting that a weakly temperature-dependent mechanism, such as surface roughness scattering, dominates the field-effect mobility.

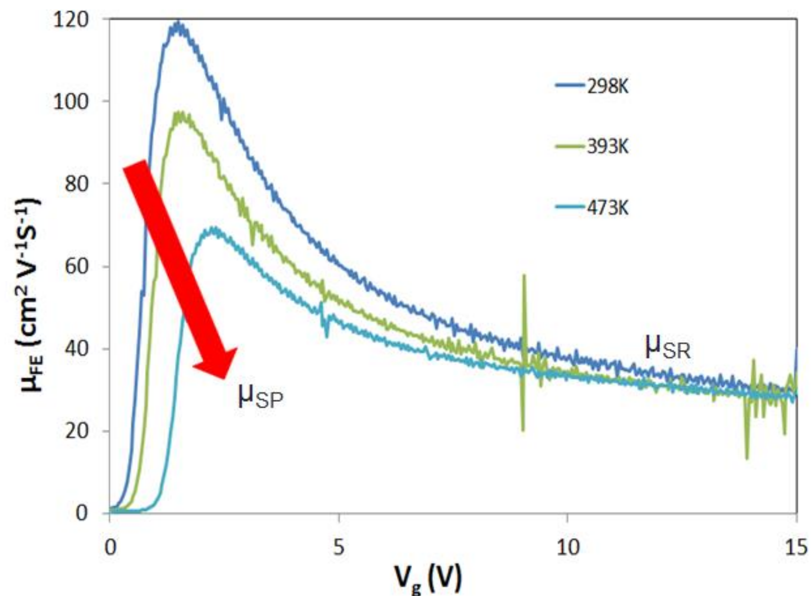


Figure 4-15. High temperature field-effect mobility measurements of a Sb+NO MOSFET. Since the maximum field effect mobility decreases with temperature, this is attributed to phonon scattering.

4.7.3 Surface roughness mobility and universal mobility

Surface roughness mobility is proportional to the inverse square of the transverse electric field in the channel and is weakly dependent on temperature (Chapter 2.6.2). At large oxide fields, both the low temperature and high temperature field-effect mobility measurements converge to ~30 $cm^2V^{-1}s^{-1}$. In addition, mobility measurements of the NO, As+NO, and Sb+NO processes were compared, and at larger oxide fields, the mobilities converged toward ~30-35 $cm^2 V^{-1} s^{-1}$ (Figure 4-16). The convergence of all the measured field-effect mobilities indicates, at large oxide fields, surface roughness scattering becomes the dominant mobility limiting mechanism.

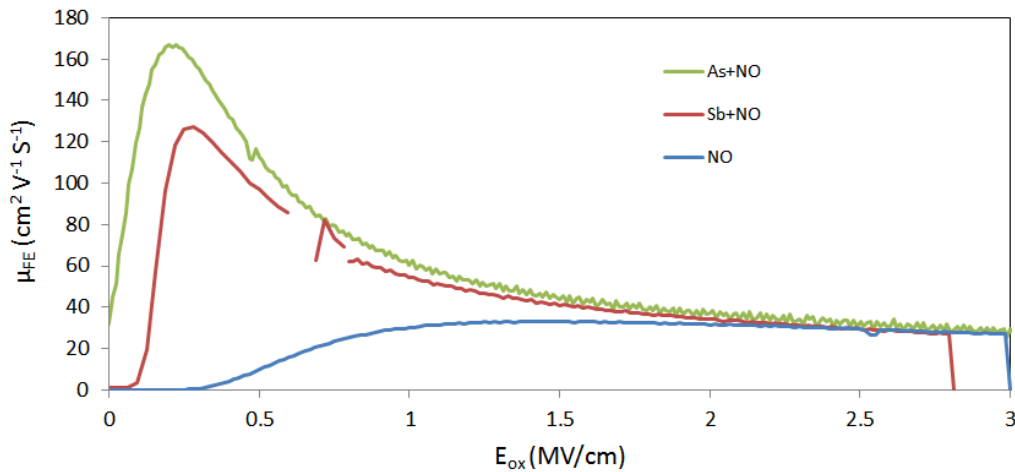


Figure 4-16. Comparison of varied MOSFET processes. The convergence of the field-effect mobilities at large oxide fields could indicate universal mobility for NO passivated SiC.

The observation that field-effect mobilities converge at larger oxide fields, independent of process, suggests that this may be the universal mobility for NO passivated SiC MOSFETs (Chapter 2.7).

Surface implanted antimony was shown to have no significant trap passivation effect at the oxide-SiC interface. Experiments with arsenic, performed as a part of this work, also suggest the same results for arsenic. The differences in mobility between the Sb+NO and As+NO MOSFETs are due to different concentrations of counter-doping as a result of higher rate of dopant activation for arsenic. Therefore, any process which does not passivate the interface, and only counter-dopes, would be expected to follow the observed trend at large oxide fields.

4.8 Conclusion

Antimony and arsenic were successfully implanted into SiC as surface counter-dopants and produced functional MOSFETs. Antimony concentrations in SiC were profiled by SIMS and were found to be similar to modeled profiles. Also, little observed antimony was out-diffused during the antimony post-implantation activation anneal.

Low temperature field-effect mobility measurements comparing Sb-only, Sb+NO, and NO MOSFETS, and CCDLTS measurements comparing Sb+NO and NO MOS capacitors, validate that antimony only counter-dopes but does not passivate interface traps.

Channel mobility measurements as a function of temperature revealed the effects of Coulomb scattering and phonon scattering on the Sb+NO MOSFETs. More importantly, the temperature dependent field-effect mobility measurements on the Sb+NO MOSFETs revealed the surface roughness scattering effects on the field-effect mobility. Measured mobilities for different processes using NO converged at oxide fields ~2-2.5MV/cm, suggesting this range is where surface roughness scattering begins to dominate the scattering mechanisms. The

convergence appears to be independent of process and temperature, suggesting this may be the universal mobility for NO passivated SiC.

4.9 References

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Chapter 5. Conclusions

Silicon carbide (SiC) is a promising wide band gap material for future high temperature and high power electronic devices. 4H-SiC is the most promising SiC poly-type for metal-oxide-semiconductor field-effect transistors (MOSFETs) since it has the largest band gap and the highest electron bulk mobility. However, one of the biggest hurdles to widespread acceptance of SiC MOSFETs is the large number of defects stemming from dangling Si or C bonds at the SiO_2/4H-SiC interface. These defects act as electron traps and result in poor channel mobility in SiC MOSFETs using the as-grown oxide as the gate dielectric. Although research with several passivation processes has reported significant improvements in MOSFET channel mobility, most of these processes resulted in unreliable gate dielectrics. Nitric oxide (NO) passivation is currently the best passivation process for improved channel mobility and reliability.

This dissertation explored two novel processes to understand and to improve the electronic properties of the SiO_2/4H-SiC interface to obtain better results than the NO passivation process. The major findings in this study are

- Nitrogen plasma passivation produced larger nitrogen coverage concentrations than standard NO passivation at the SiO_2/4H-SiC interface. As measured by the simultaneous high-low capacitance-voltage method (hi-lo C-V), the increase in nitrogen coverage was associated with a decrease in the number of electron traps at the interface (N_{it}). However, the maximum field-effect mobility of nitrogen plasma passivated MOSFETs did not scale with the decreased number of interface traps. This indicates a limit to the beneficial effects nitridation of the SiO_2/4H-SiC interface has on channel mobility. The nitridation limit is due to nitridation of the SiO_2/4H-SiC interface which creates “fast traps” that are

not detectable by conventional hi-lo C-V but can be detected using the C-ψ_s method developed by Yoshioka et. al. [1-2].

- Operational MOS devices were produced using antimony-implanted SiC. From these devices, antimony was demonstrated to counter-dope, not passivate, the interface. The counter-doped interfaces significantly improved field-effect mobility at low oxide fields, while the threshold voltage remained positive. At high oxide fields, field-effect mobilities were observed to converge in counter-doped samples passivated with nitrogen. The field-effect mobilities converged independent of temperature and counter-dopant. The convergence suggests surface roughness scattering mechanisms dominate the field-effect mobility at high oxide fields. The convergence may also be indicative of the universal mobility for nitrogen passivated 4H-SiC MOSFETs.

This work examined several processes for improved performance and efficiency of 4H-SiC MOSFETs. If the results of this work prove viable for 4H-SiC power MOSFETs without reducing their stability and reliability, it may point to ways to increase the efficiency of 4H-SiC power MOSFETs or other 4H-SiC power electronics devices. Since the use of power electronics is predicted to grow, more efficient 4H-SiC devices will make the devices greener and more attractive for use (lower operation costs).

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Appendix A. Device cleaning process

1. Use a cotton swab and acetone to remove the glue on SiC sample surface.

The next set of steps removes organic compounds on sample surface.

2. After surface appears clean by inspection with microscope, place sample in a beaker of acetone and place in the ultrasonic cleaner for 5min.
3. Remove sample and place in TCE beaker in ultrasonic cleaner for 5min.
4. Remove sample and place in acetone beaker in ultrasonic cleaner for 5min.
5. Remove sample and place in methanol beaker in ultrasonic cleaner for 5min.
6. Remove sample and place in a second methanol beaker in ultrasonic cleaner for 5min.
7. Remove sample and place in DI water beaker in ultrasonic cleaner for 5min.
8. Remove sample and place in buffered oxide etch (BOE) for 5min.
9. Rinse sample in DI water.

The next set of steps removes inorganic compounds on sample surface.

10. Mix a solution of 1:1 H_2SO_4:H_2O_2 and place sample in solution for 15min.
11. Rinse sample in DI water, then place sample in BOE for 2min.
12. Mix a solution of 3.5:1:1 DI water:H_2O_2:NH_4OH and heat to 100-115°C.
13. Rinse sample in DI water and place in solution for 15min.
14. Rinse sample in DI water and place in BOE for 2min.
15. Mix a solution of 3.5:1:1 DI water:H_2O_2:HCl and heat to 100-115°C.
16. Rinse sample in DI water and place in solution for 15min.
17. Rinse sample in DI water and place in BOE for 2min.
18. Rinse sample and dry with N_2 air gun.

Appendix B. Sample oxidation

1. Vacuum oxidation furnace tube until base pressure is less than 1torr.
2. Prepare argon tank and fill oxidation furnace tube to atmospheric pressure.
3. Flush oxidation furnace tube with argon for 10-15min to remove residual gases.
4. Load samples into oxidation furnace tube.
5. Vacuum oxidation furnace tube for 10-15min.
6. When pressure is less than 1torr, fill and flush with argon for 10-15min.
7. Set oxidation furnace temperature to 1150°C and the ramp rate to 5°C/min.
8. When temperature is at 1150°C, stop argon flow and begin oxygen flow at 750 sccm.
9. Record the start time.
10. Let oxidation run for the desired time.
11. Record finish time.
12. Stop oxygen flow and begin argon flow.
13. Let sample anneal in argon for 30min post oxidation.

Steps 14-22 are for NO passivation. If no NO passivation necessary, skip to step 23.

14. Increase temperature to 1175°C.
15. Flow argon through NO lines.
16. Begin NO flow and turn off argon flow.
17. Set NO regulator to 30 psi.
18. Flow NO at 571 sccm and anneal for 2h.
19. After anneal is finished, stop NO.
20. Let NO pressure drop to zero, and then flush NO lines with argon.
21. Stop argon flow in NO lines and vacuum NO lines until pressure is zero.

22. Stop vacuum of NO lines.
23. Set oxidation furnace temperature ramp rate to 10°C/min and ramp temperature down to oxidation furnace base temperature.
24. Remove samples from oxidation furnace tube.

Appendix C. Plasma furnace operation

1. Vacuum plasma furnace tube to 4-5mtorr.
2. Flow nitrogen in plasma furnace tube.
3. Start microwave generator.
4. Adjust microwave power to 1kW.
5. Adjust reflectors until the reflected power is zero.
6. After plasma ignites, adjust reflectors until reflected power is zero.
7. Increase power to 2kW.
8. Let run for 20-30min to clean the plasma tubes.
9. Turn microwave energy down to zero and turn off the power.
10. Fill nitrogen plasma tube to atmospheric pressure.
11. Load samples at 5L/min.
12. Stop nitrogen flow.
13. Vacuum pressure to 2mtorr.
14. Flow nitrogen at 0.5L/min and increase furnace temperature to 1160°C.
15. Turn on microwave power and adjust to 1kW.
16. Adjust reflectors until reflected power is zero.
17. Adjust power to 2kW.
18. After plasma ignites, adjust reflectors until reflected power is zero.
19. Increase nitrogen flow rate to 3L/min; readjust reflectors if necessary.
20. Adjust pressure inside the plasma furnace tube to 2.3torr.
21. Turn on computer and open photodetector software.
22. Set up an intensity-time graph for 850.01 nm wavelength.

23. Let plasma run for desired time.

24. After plasma time is completed, turn microwave power down to zero.

25. Turn off microwave power.

26. Fill plasma furnace tube to atmospheric pressure with nitrogen.

27. Turn nitrogen flow rate down to 0.5L/min and let samples anneal for 2h.

28. Lower temperature to 850°C.

29. Remove the sample.

Appendix D. LPCVD deposited oxide procedure

1. Two hours before oxide deposition, set TEOS bubbler temperature to 55°C.
2. Load the samples into LPCVD tube.
3. Follow instructions for running LPCVD system.
4. Deposit 50-60nm of oxide.
5. Turn off TEOS bubbler heater.
6. Remove samples.

Appendix E. Mask aligner and spinner procedure

1. Place a drop of 5214E photoresistivity glue on the silicon wafer.
2. Attach sample to the wafer and put it in a 105°C oven. Do not let the oven temperature exceed 110°C.
3. Cook sample for 10min in oven.
4. Begin mask aligner start-up procedure.
5. Remove wafer from oven.
6. Start spinner.
7. Put water in center of spinner.
8. Use a pipet with a disposable tip to cover sample with 5214E photoresist.
9. Run spinner for 30sec at 4000 RPM.
10. Place wafer in oven for 1min. Do not exceed 1min or 105°C.
11. Remove wafer.
12. Place wafer in mask aligner and adjust mask for appropriate pattern.
13. Expose sample to UV lamp for 30sec.
14. Remove wafer and place in a 1:4 ratio of AZ 400:H_2O for ~10sec and then quickly put it under running DI water.
15. The pattern should be visible when viewed under a microscope. If it is not, repeat step 14 for a few seconds.
16. When the pattern is clearly visible, check it under the microscope. If all of the lines are sharp, the pattern has been properly set.

Appendix F. Sputter system procedure

1. Load samples into sputter system.
2. Put correct metal targets on sputter guns.
3. Close sputter system and vacuum pressure to 10^{-7}torr or less.
4. Flow Ultra High Pure Argon through sputter system, adjusting pressure to ~18mtorr.
5. Let argon flow for 3min.
6. Adjust voltage and current to appropriate settings for the selected metal target.
7. Pre-sputter for 2min on dummy sample.
8. Sputter metal onto sample for appropriate length of time.
9. Stop argon flow.
10. Allow vacuum pump to empty chamber.
11. Stop vacuum pump and fill chamber to atmospheric pressure with nitrogen.
12. Remove samples.
13. Complete any necessary steps to return sputter system to stand-by mode.

Appendix G. Reactive ion etch procedure

1. Open glass window of etcher.
2. Remove blank Si wafer.
3. Place and center sample on electrode.
4. Use large tweezers to press down on wafer to ensure it is securely in place.
5. Close the glass window and tighten until snug.
6. Vacuum system for 20-30min or until system reaches base pressure (~9-10mtorr).
7. Open all valves to etch gas line and turn on the appropriate switch on the flow controller.
8. Turn on cooling water and open all water valves to system.
9. Turn on RF power supply.
10. Adjust power setting to about three (3) watts *higher* than the desired power.
11. Once the pressure has stabilized, turn on power supply.
12. If necessary, adjust power to appropriate level and adjust matching network to obtain the lowest possible reflected power.
13. After desired etch time, turn off the RF power.
14. Turn off the etchant gas and allow system to vacuum to base pressure.
15. If no other etching is required, close all valves and turn off system.
16. Fill etchant chamber to atmospheric pressure with nitrogen.
17. Remove the wafer with the sample and replace it with the blank Si wafer.

Appendix H. Ohmic anneal furnace procedure

1. Flow argon through ohmic anneal furnace tube until atmospheric pressure is reached.
2. Adjust argon flow rate to ~8L/min.
3. Open loading area and load samples.
4. Close loading area.
5. Flush ohmic anneal system with argon for 5min.
6. Stop argon flow and vacuum ohmic anneal furnace tube until 10^{-7}torr.
7. Stop vacuuming and flush system with argon for 5min at 12L/min.
8. Insert samples into furnace and start 30sec timer once sample temperature reaches 850°C.
9. After 30sec annealing is finished, transfer samples from furnace to loading area.
10. Remove samples from system.
11. Complete any necessary steps to return ohmic anneal system to stand-by mode.

Appendix I. Carbon cap procedure

1. Mount sample on Si wafer with water soluble wax.
2. Spin on 5214E photoresist at 4000 RPM for 30sec.
3. Remove sample from wafer and put in water for 15min.
4. Bake photoresist-covered SiC in oven at 100-110°C for 15min.
5. Put the sample into the designated carbon cap carbon box, with photoresist facing up.
6. Place this box into a high temperature anneal system.
7. Reduce system pressure to 10^{-7}torr.
8. Fill chamber with argon.
9. Reduce argon flow to 3-4psi.
10. Create a table containing these columns: variac %; system operation time; current temperature of the system.
11. Increase variac to 10% and wait ten minutes and make recordings in table.
12. Increase variac 5% every two minutes and make recordings in table.
13. When temperature nears 600°C, adjust variac until temperature stabilizes near 600°C.
14. Keep the system at 600°C±5°C for 30min.
15. Turn off variac.
16. When temperature is less than 70°C, open high temperature anneal system.
17. Carefully remove sample and return carbon cap box to its storage container.
18. Stop argon flow.
19. Vacuum system to base pressure.

Appendix J. Activation anneal procedure

1. Complete carbon cap process first (Appendix I).
2. Place sample, with carbon cap face down, in designated carbon box for activation anneal.
3. Fill high temperature anneal system with argon, and then load the sample.
4. Vacuum system until pressure is $8x10^{-7}$torr.
5. Stop vacuuming and fill with argon to atmospheric pressure.
6. Flow argon at 12psi.
7. Increase variac 1% every ten seconds until variac is at 60%.
8. When temperature approaches 1550°C, adjust variac until temperature stabilizes ~1550°C.
9. Hold temperature at 1550°C±5°C for 30min.
10. Turn off variac.
11. When temperature is less than 70°C, open high temperature anneal system.
12. Carefully remove sample and return the carbon cap box to its storage container.
13. Stop argon flow.
14. Vacuum system down to base pressure.

Appendix K. Capacitance-Voltage measurement procedure and settings

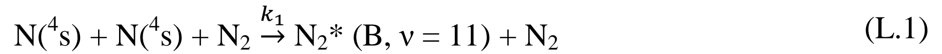
1. Turn on computer and open ICS software.
2. Make sure Kiethley 230, 595, and 590 have been on for at least one hour.
3. Use silver paint to attach samples to gold-sputtered alumina and let dry for 30-60min.
4. On computer, in the File menu, click on Open and use the down arrow for Attribute #1 to see a list from which you must choose the correct initial setup, then click OK.
5. On computer, click the Edit Test Setup icon, then adjust only the start, stop, and bias voltages and time step. Ignore the other conditions.
6. On computer, click OK and then DONE to leave the setup.
7. Open the box lid and place sample on chuck.
8. Gently put the ground probe onto the gold-plated alumina.

Repeat steps 9-14 for each device that is being tested.

9. On computer, click the Measurement icon.
10. On computer, press Zero Cancel icon.
11. In box, make sure probe is removed from the gate before clicking OK on the computer for the disconnect probes button.
12. When zero cancel is done, in box, place the probe onto the gate and close the box, then click OK on the computer.
13. On computer, press the Single Measurement button.
14. On computer, to save the file, click on File, Export, enter a file name less than eight characters, and save it as ASCII.
15. When finished, close the software *without* saving changes, and close the box lid.

Appendix L. Nitrogen plasma recombination

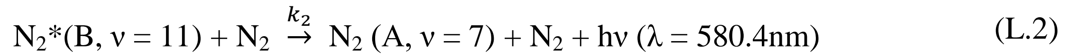
The density squared of atomic nitrogen in the late afterglow region of a nitrogen plasma is proportional to the intensity of emitted photons with 580.4nm wavelengths. The 580.4nm wavelength is emitted at the conclusion of a specific two-part nitrogen recombination reaction. The first part of the recombination involves a three-bodied collision. The equation for this collision is



$$N(^4s) + N(^4s) + N_2 \xrightarrow{k_1} N_2^* (B, \nu = 11) + N_2 \qquad (L.1)$$

where $N(^4S)$ is a nitrogen atom in the ground state, N_2^* is a nitrogen molecule with an electron in an excited state B and energy level ν, and k_1 is the reaction rate [1-2].

It has been reported that radiative decay of N_2^* at pressures larger than 1mbarr (~0.76torr) was negligible compared to quenching by N_2 [2]. The equation for quenching by N_2 is



$$N_2^*(B, \nu = 11) + N_2 \xrightarrow{k_2} N_2 (A, \nu = 7) + N_2 + h\nu\ (\lambda = 580.4nm) \qquad (L.2)$$

where $N_2^*(B,\nu)$ is a nitrogen molecule with an electron in an excited state B and energy level ν; $N_2(A,\nu)$ is a nitrogen molecule with an energy level denoted by ν; k_2 is the reaction rate; and hν is the emitted photon with wavelength λ [1-2].

The equilibrium constant of a reaction

$$aA + bB \rightarrow cC + dD \qquad (L.3)$$

is determined by

$$K_C = \frac{[C]^c[D]^d}{[A]^a[B]^b} \qquad \text{(L.4)}$$

where K_c is the equilibrium constant. The equilibrium reaction rate for Equation L.1 is

$$k_{1c} = \frac{[N_2^*(B, v = 11)]^1}{[N]^2} \; [2] \qquad \text{(L.5)}$$

Equation L.5 displays the relationship between the steady-state concentration of $N_2^*(B, v = 11)$ and the square of nitrogen atoms in the ground state. Equation L.2 displays the proportional relationship between the intensity of the 580.4nm wavelength and the concentration of $N_2^*(B, v = 11)$ [2]. Combining Equations L.2 and L5. shows the relationship between the intensity of the 580.4nm and the square of nitrogen atoms in the ground state.

L.1 References

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