Wide Temperature Range SiGe HBT Noise Parameters Modeling and LNA Design

by

Rongchen Ma

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Approved by

Guofu Niu, Professor of Electrical and Computer Engineering
Fa Foster Dai, Professor of Electrical and Computer Engineering
Bogdan Wilamowski, Professor of Electrical and Computer Engineering

Abstract

This work investigates SiGe HBT noise parameters and impedance matched Low-Noise Amplifiers(LNAs) intended for operation across a wide temperature range from 93 to 393 K. For the IBM 5AM technology used, noise performance improves with cooling until about 150 K, then degrades some due to carrier freeze-out. With a temperature independent bias current, an LNA designed for 300 K operation shows acceptable performance from 93 to 393 K, albeit with some degradation of linearity below 120 K.

Acknowledgments

I would like to express my gratitude to my supervisor, Dr. Guofu Niu. When I first came to Auburn University, I did not know anything about microelectronics. With his guidance and patience, I was able to do my research of SiGe HBT. He taught me everything about doing research from beginning, even how to read papers properly. He not only taught me knowledge and the method to do research, but also showed a strong sense of responsibility. He showed his attitude on research to let me know how serious I should be to do research. Without his help, I could not possibly do this research.

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Chapter 1

Introduction

The Silicon-Germanium heterojunction bipolar transistor (SiGe HBT) has gained world-wide attention, since it could get higher current gain, higher cut-off frequency and lower base resistance compared with Si BJT. Based on those advantages of SiGe HBT, noise figure of SiGe HBT chould be much lower. As noise sets the lower limit of dynamic range, this thesis first researches noise parameters performance including correlation and avalanche noise. In order to make sure the device can be functional on Luna surface, in Arctic region or other extreme environments, another remarkable characteristics of the silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) is needed, which is its ability to operate over extremely wide temperature ranges, from as low as sub-1 K [5], to as high as over 400 K. This fact, together with its excellent total dose radiation tolerance, makes it very attractive for implementing space electronics that can operate over a wide temperature range while in the presence of ionizing radiation such as that found in space environments [6] [8].

In general, the process design kits (PDK) from integrated circuit (IC) foundries fail to run or else give erroneous results outside its intended temperature range, typically from 223 to 393 K [9]. To enable IC designs for extreme environments, we have recently developed a SiGe HBT compact model that can function from 93 to 393 K [10] [11] [12] [13] [14]. Using this new model, we investigate how temperature affects SiGe HBT noise parameters and the nice property of being able to approximately achieve simultaneously LNA noise and impedance matching. The Z_s in Fig. 1.1 is as same as R_s when reactance X_s=0. Transistor size can be optimized for noise matching to get source resistance R_{opt}=50 Ω, or so called real part noise matching. Emitter and base inductors L_e and L_b can also be optimized to get

R_{in}=50 Ω and X_{in}=0, or so called real part and imaginary part impedance matching. As a result, noise matching source resistance X_s=0, so called imaginary part noise matching.

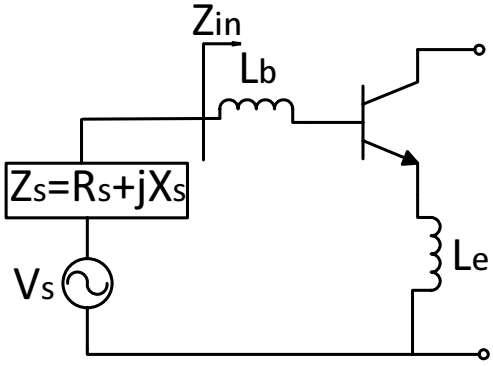

Figure 1.1: Simplified schematic of the LNA consisting of a single SiGe HBT.

The SiGe HBTs used are from IBM's 5AM technology, with 50 GHz peak f_T, typical of a first-generation SiGe technology platform. Verilog-A is used to implement the compact model for circuit simulation and design using the Agilent ADS tool suite. The noise model implemented not only includes thermal noises of base, emitter, collector resistance and base and collector currents shot noise but also considers frequency dependent correlated noise [15] and avalanche noise [18], which is discussed in Chapter 3. But in Chapter 4 and 5, for the technology explored in this work, when f=5 GHz and J_C = 0.1 mA/μm^2, correlation noise decreases noise figure only slightly and when V_{CB} is below 2 V, avalanche noise is small enough to be neglected. Thus, in Chapter 4 and 5, we present only results obtained using the standard noise model, in which correlation noise and avalanche noise are not considered.

1.1 SiGe HBT fundamentals

One of the best choices for low-noise operation is Silicon-Germanium(SiGe) heterojunction bipolar transistor(HBT), due to its excellent analog and RF performance. After decades of study and development, SiGe technology has become practical. SiGe HBT is the heart of SiGe technology, and is the first practical bandgap engineering device realized in silicon,

which can be integrated with the modern CMOS technology. The Fig. 1.2 illustrates the difference between SiGe HBT and Si BJT by showing the energy-band diagrams for both SiGe HBT and Si BJT biased identically in forward-active mode. The Ge profile linearly increases from zero near emitter-base (EB) junction to some maximum value near collector-base (CB) junction, and then rapidly ramps down to zero [1]. Since the energy bandgap of Ge is smaller than that of Si, adding germanium into the base region of the transistor leads to an additional bandgap shrinkage, which is approximately 75 meV for each 10 percent of Ge introduced[6]. The reduction of bandgap decreases band transit time, which gives a higher f_T. Smaller base bandgap also increases electron injection, which leads to a higher β. At same collector current density, compared with normal BJT, SiGe HBT allows us to have a higher base region doping concentration, which reduces base resistance. Based on these three advantages–higher f_T, higher β and lower base resistance, according to Equation (1.1), we can easily make the conclusion that at same collector current density and frequency, F_{min} of SiGe HBT is much smaller than that of Si BJT. Therefore, SiGe HBTs have been widely used in commercial and military wireless communication applications.

$$F_{min} = 1 + \frac{1}{\beta} + \sqrt{2g_m R_b}\sqrt{\frac{1}{\beta} + \left(\frac{f}{f_T}\right)^2} \tag{1.1}$$

1.2 5AM Technology

The SiGe HBTs discussed in this thesis are from IBM's 5AM technology, whose characteristic is showed in Table 1.1 [7].

Table 1.1: IBM's 5AM technology device characteristic at 300 K

	Lithography Node	Peak f_T	Peak f_{max}	BV_{ceo}	BV_{cbo}	$R_b * L_E$	$R_e * L_E$
Unit	μm	GHz	GHz	V	V	$\Omega \cdot \mu m$	$\Omega \cdot \mu m$
Value	0.5	50	65	3.3	10.5	750	30

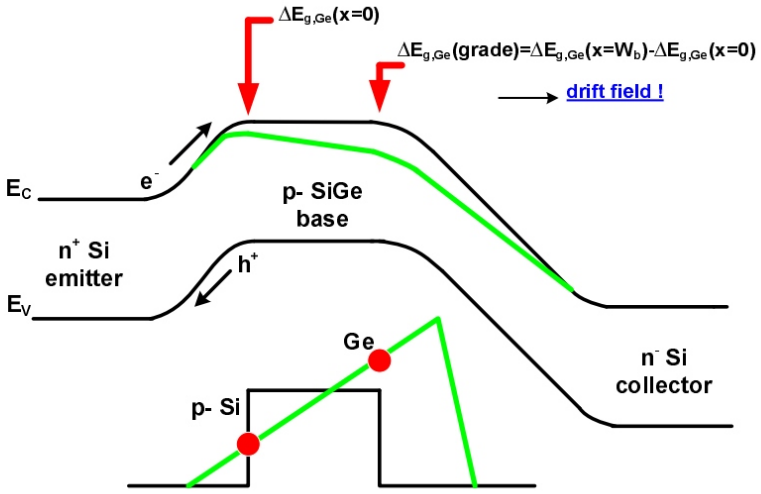

Figure 1.2: Energy band diagrams of a graded-base SiGe HBT and an Si BJT [3].

Fig. 1.3 shows the device structure of IBM's 5AM technology. The two shadow areas on the top of the structure are spacers to isolate the emitter from the extrinsic base. Between two spacers, it is the N-type poly emitter of the transistor. Under the emitter, it is the P-type intrinsic base part of the transistor. Two extrinsic bases are placed at both sides of intrinsic base. N-type collector region is under the intrinsic base. Inside of the collector, there is a selectively implanted collector which can retard the onset of base push-out or kirk effect. Two shallow trenches are placed between collector and extrinsic base to isolate them. Below the collector, it is the buried layer of the transistor. Below the buried layer, substrate layer is placed to keep a low RF lost. One deep shallow trench is placed to isolate the buried layer of adjacent transistors [7].

Fig. 1.4 shows the doping concentration and germanium grading of 5AM technology. In order to have a low emitter resistance, the emitter region has a negative doping concentration over 1e20 $/cm^3$ using arsenic. In the base region, in order to have a low base resistance and base-emitter junction capacitance, after trade off, positive doping concentration is about 1e18 $/cm^3$ achieved by adding boron. In the collector region, in order to have a low base-collector junction capacitance which leads to high f_{max} and have a high break down voltage,

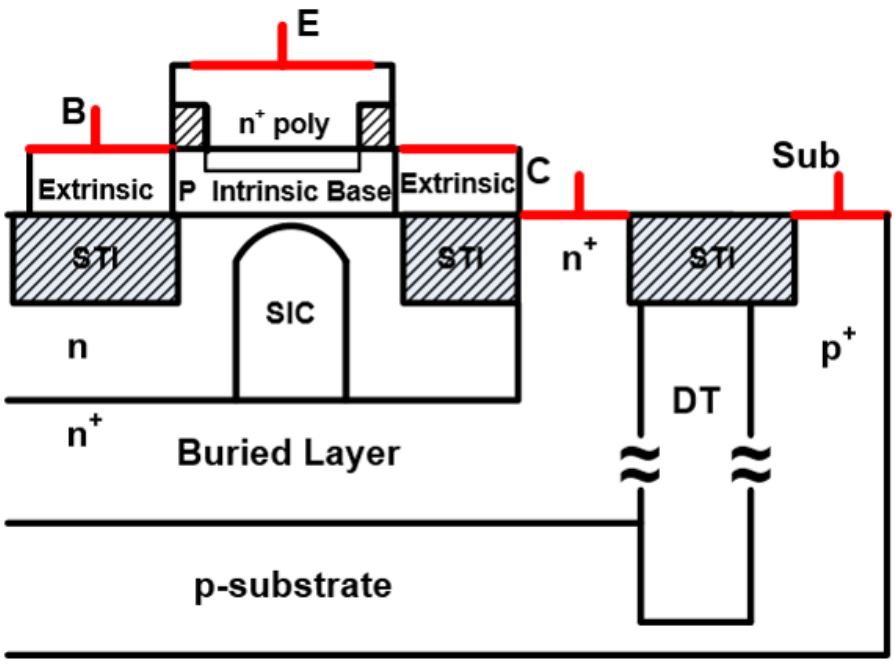

Figure 1.3: 5AM technology device structure

the doping concentration should be low. But we also need to retard the base push-out or kirk effect, the collector doping concentration should be high. So after certain trade off, the collector doping concentration is smaller than base doping concentration. Because we need to make sure that the current from collector to buried layer flows vertically and we want to have a relatively low collector resistance without increasing base-collector junction capacitance. Buried layer doping concentration is almost as high as emitter doping concentration.

In Fig. 1.4, the blue dash line represents the germanium grading in base region. At the beginning of base region, the germanium grading increases rapidly. Then it maintains at a maximum value, which is about 10 percent, a typical value for a first generation SiGe HBT. Once it comes to the end of base region, the germanium grading decreases rapidly to 0.

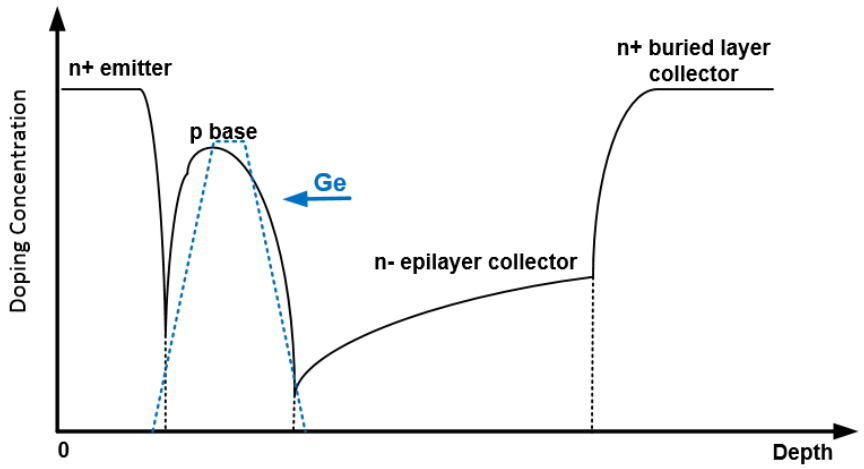

Figure 1.4: Doping concentration and Ge grading of a first generation SiGe HBT

Chapter 2

Compact Model and Device Characteristics

2.1 Wide Temperature Compact Model

SiGe HBT is currently being used to develop electronics for space application due to its excellent analog and RF performance over an extremely wide range of temperature. To enable the design of circuits that can operate over such a wide temperature range, we need to have an accurate compact model. The model used in this thesis is based on Mextram 504.6 [22], with major extensions developed to increase the applicable temperature range [13] [14].

Fig. 2.1 shows the equivalent circuit for the wide temperature range model used in this thesis as it is specified in [2]. Compared with original Mextram model, a forward base tunneling current $I_{B,tun}$, substrate resistance R_{sub} and capacitance C_{sub} are added to enable modeling of DC and AC characteristic.

Since this thesis mainly researches about device and LNA noise performance in a wide temperature range, modeling of main current, freezeout effect and resistance are presented below:

2.1.1 Main Current

In a wide temperature range, the main current I_N is modeled as [2] [14]:

$$I_N = \frac{I_{S,F} e^{\frac{V_{B_2E_1}}{N_F V_T}} - I_{S,R} e^{\frac{V^{\star}_{B_2C_2}}{N_R V_T}}}{q_B}, \tag{2.1}$$

where except for forward and reverse saturation current $I_{S,F}$ and $I_{S,R}$, forward and reverse ideality factor N_F and N_R. N_F and N_R, other symbols have their usual meanings in Mextram.

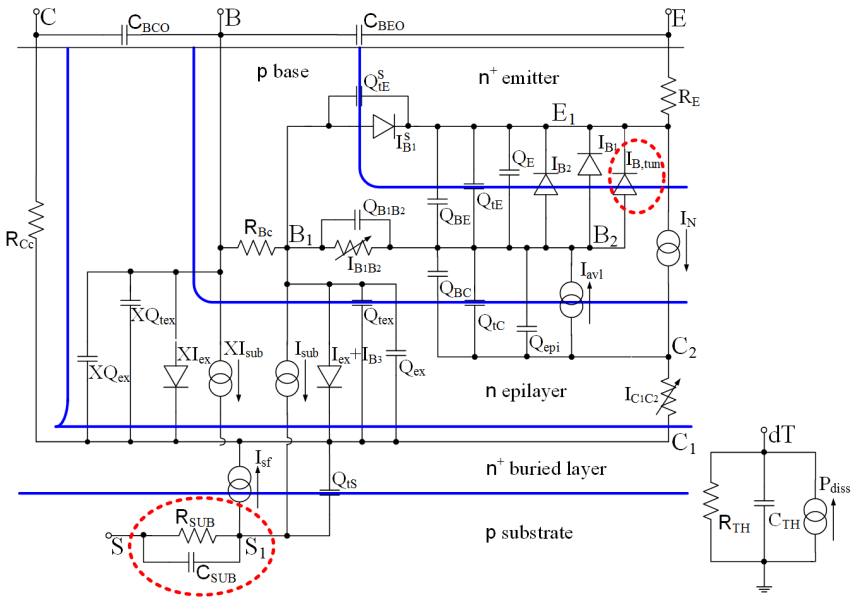

Figure 2.1: The equivalent circuit for the wide temperature range model used in this thesis [2].

Because in the original model, it was believed that q_B is sufficient in modeling the slope of I_C-V_{BE} and using ideality factors could complicate the parameter extraction. Compared with measurement data, however, we found it necessary to introduce a N_F parameter that increases rapidly with cooling below 100K. In addition, the traditional I_S T-scaling equation fails as well, even with the use of a nonlinear T-dependent bandgap E_g [10]. Even though the underlying physics of such departure from Shockley theory remains to be understood, the T-scaling of N_F and I_S (I_{SF} or I_{SR}) can be semi-empirically modeled as [9] [10]:

$$N_F(T) = N_{F,nom}\left(1 - \frac{T - T_{nom}}{T_{nom}}\left(A_{NF}\frac{T_{nom}}{T}\right)^{X_{NF}}\right), \tag{2.2}$$

where T_{nom} is nominal temperature, $N_{F,nom}$ is ideality factor at nominal temperature which is close to 1. A_{NF} and X_{NF} are technology dependent fitting parameters. For I_S:

$$I_S(T) = I_{S,nom}\left(\frac{T}{T_{nom}}\right)^{\frac{X_{IS}}{N_F(T)}} \exp\left(\frac{-E_{a,t}\left(1-\frac{T}{T_{nom}}\right)}{N_F(T)V_T}\right), \tag{2.3}$$

$$E_{a,t} = E_{g,0} + \frac{\alpha\beta T T_{nom}}{(T+\beta)(T_{nom}+\beta)} \tag{2.4}$$

where $I_{S,nom}$ is I_S at nominal temperature. X_{IS} includes the temperature coefficient of mobility and density of states. $E_{g,0}$ is 0K bandgap, α=4.45 $\times 10^{-4}$ V/K, β=686 K are coefficients of nonlinear T-dependence of bandgap. $E_{g,0}$, $I_{S,nom}$, and X_{Is} are model parameters.

2.1.2 Freezeout

It is necessary to model an important temperature effect called freezeout, which affect T-dependence of resistances, junction built-in potentials, and Early effects [2]. There are two existing models for freezeout. One is classical freezeout theory [30] which leads to an ionization rate (IR) that decreases with cooling rapidly depending on dopant ionization energy. Another recent freezeout model of Altermatt [31], which accounts for Mott transition, leads to an *IR* that decreases with cooling first, but then stays at a fixed value equal to the "free" dopant state fraction, or $1-b$, with b being the bound state fraction [14].

An analytical expression of *IR* for this model was derived in [11]:

$$\begin{aligned} IR(T) &= \frac{-G+(1-b)+\sqrt{[G-(1-b)]^2+4G}}{2}, \\ G &= g^{-1}\frac{N_{DOS}}{N_{dop}}\exp\left(-\frac{E_{dop}}{kT}\right), \\ b &= 1-\frac{\theta}{1+\left(\frac{T}{T0}\right)^{\eta}}, \end{aligned} \tag{2.5}$$

where g is degeneracy factor (g=4 for acceptor, g=2 for donor), E_{dop} is impurity activation energy, b is fraction of bound impurity states, N_{DOS} is effective density-of-states (N_V for acceptor, N_C for donor), N_{dop} is the active doping concentration. θ and η are fitting parameters to model b's temperature dependence. Experimentally extracted IR from sheet resistance measurement is somewhere between the classic theory and Altematt's theory [11], which is showed in Fig. 2.2 compared with both theories.

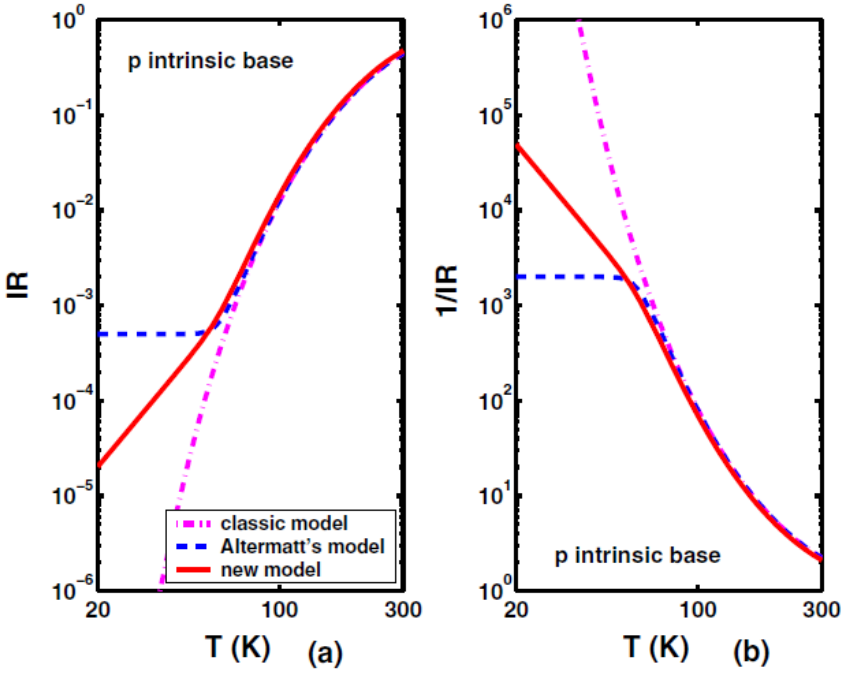

Figure 2.2: (a) Calculated IR(b) Calculated $1/IR$ for intrinsic base using the classic, the Altermatt, and the wide range temperature model used in this thesis [2].

2.1.3 Resistance

T-scaling of resistance is modeled as:

$$R(T) = R_{CI,T0}\left(\frac{T}{T0}\right)^{AR}\frac{1}{IR(T)},$$
$$R_{CI,T0} = R_{T0} \times IR(T0), \tag{2.6}$$

where $R_{CI,T0}$ is nominal temperature resistance under complete ionization, and AR represents the T-dependence of mobility. Except for R_{CV}, IR(T) model parameters are determined from fitting the relevant sheet resistance or resistivity over temperature data. For R_{CV}, further tuning is found to be necessary to fit gain roll-off [14].

2.2 Device Characteristic

Complete DC and S-parameter measurements were made at 393, 300, 223, 162, and 93 K for device characterization, and parameter extraction on a SiGe HBT with an emitter area of 0.5×2.5 μm^2. Additional Gummel measurements were made at many more temperatures, particularly below 162 K, to capture the details of the overall temperature dependence. The model specifically accounts for temperature dependent ideality factors in both I_B and I_C, freeze out, self-heating, and high injection effects.

Fig. 2.3 (a)-(b) show I_C-V_{BE} and I_B-V_{BE} behavior from 393 to 93 K. The I_C corresponding to J_C = 0.1 mA/μm^2, at which LNAs will be designed below, is shown in the dashed line. Fig. 2.4 shows measured and modeled I_C-V_{CE} for forced I_B at 93, 162, 223 and 300 K respectively. Fig. 2.5shows f_T-I_C at 93, 162, 223 and 300 K at $V_{CB} = 0, 1, 2$ V. Fig. 2.6 shows measured and modeled Y-parameters at 162 K, at 1,2,3 and 5 GHz. Fig. 2.7 shows measured and modeled Y-parameters at 300 K, at 1,2,3 and 5 GHz.

Overall, reasonable agreement between modeling and measurement is achieved over a wide temperature range. At 93 K, the modeled f_T is smaller than the measured data, primarily due to an unexpected decrease of base-emitter junction depletion capacitance with cooling, around 93 K, while in the model, junction capacitance increases with cooling following current understanding.

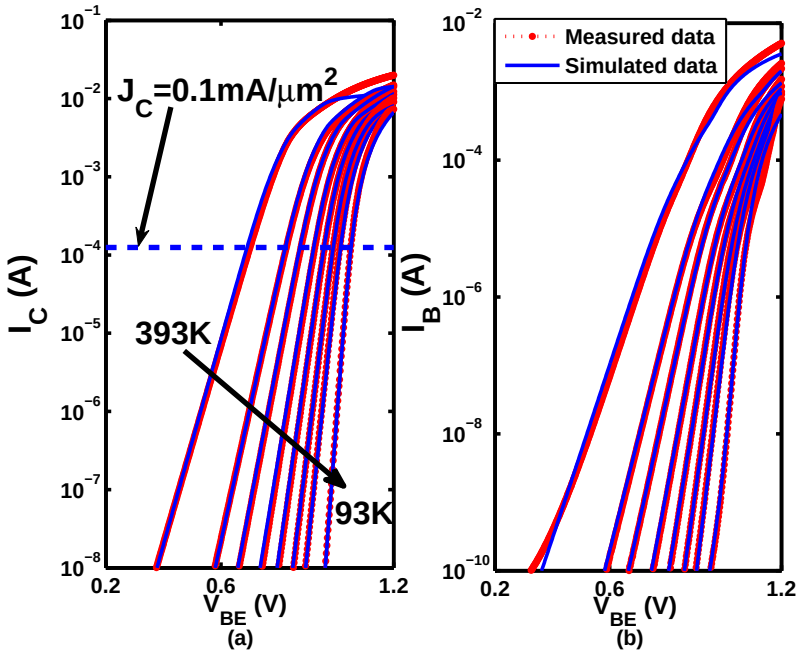

Figure 2.3: (a) Measured and modeled I_C-V_{BE} from 393-93 K. (b) Measured and modeled I_B-V_{BE} from 393-93 K [2].

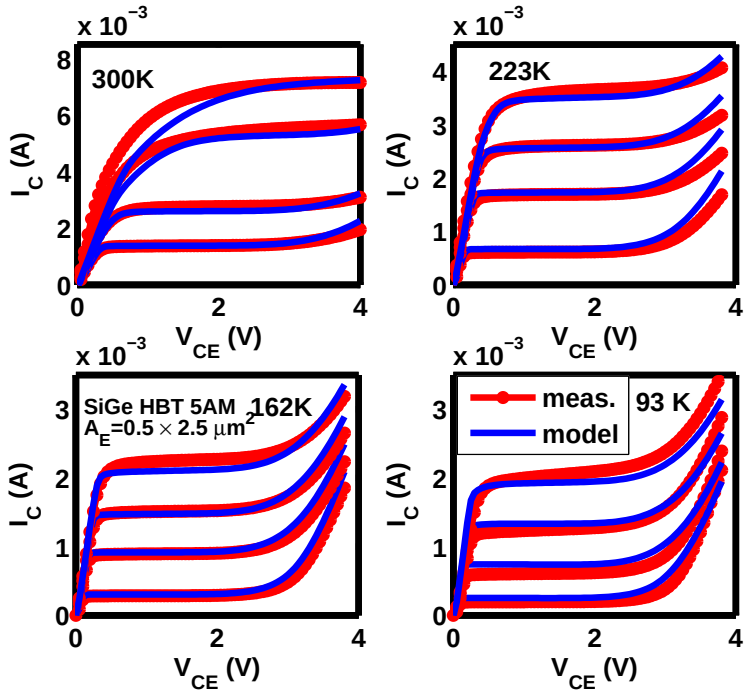

Figure 2.4: Measured and modeled Forced I_B output characteristics from 93 -300 K [2].

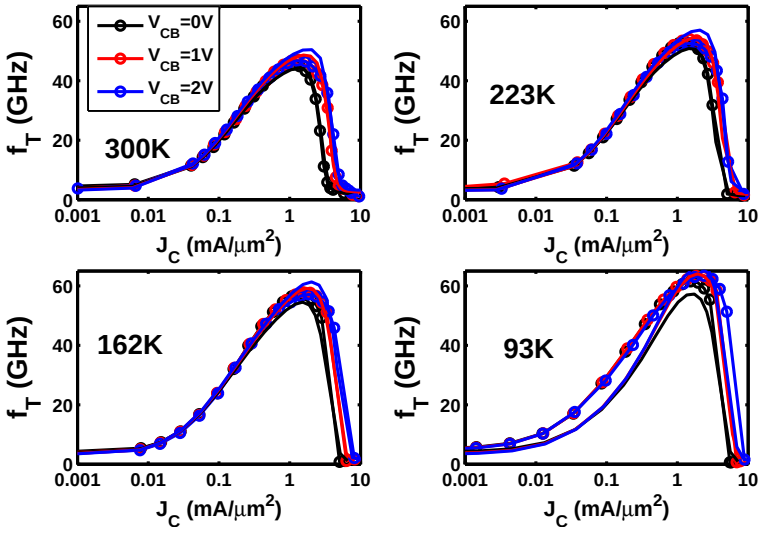

Figure 2.5: Measured (symbol line) and modeled (solid line) f_T-I_C from 93-300 K, $V_{CB} = 0, 1, 2$ V [2].

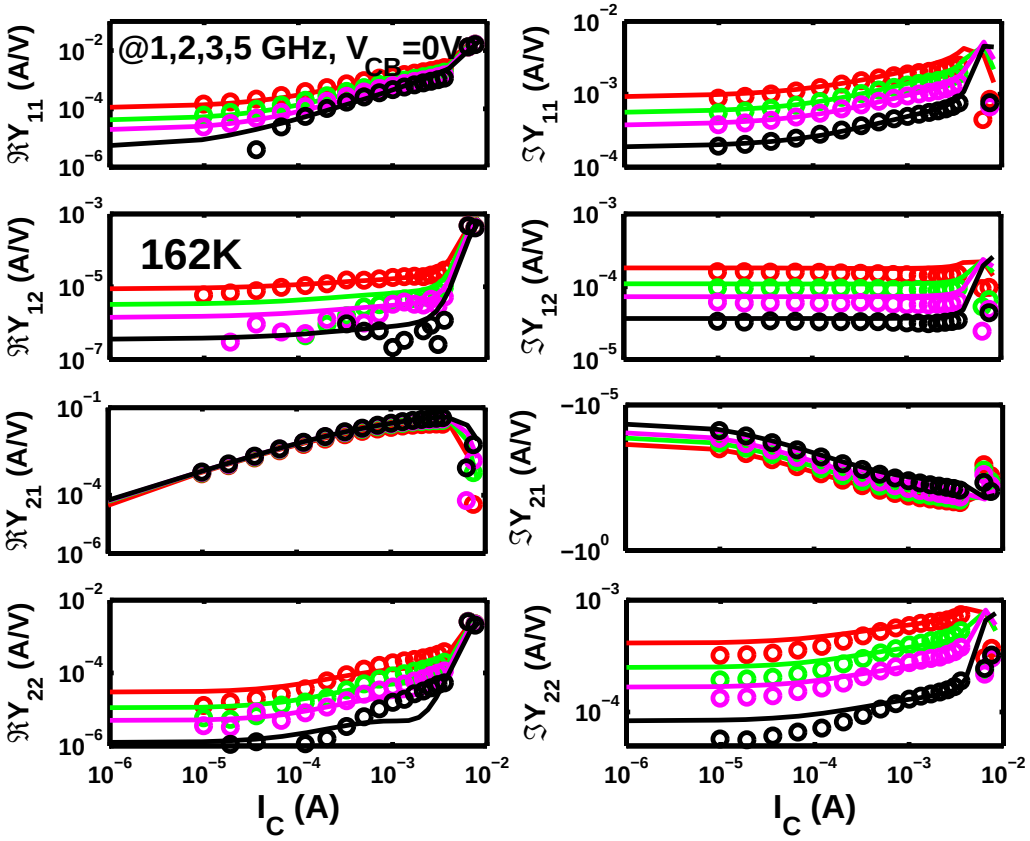

Figure 2.6: Measured (symbols) and modeled (curves) Y-parameters at 1,2,3 and 5 GHz for 162 K, $V_{CB} = 0$ V [2].

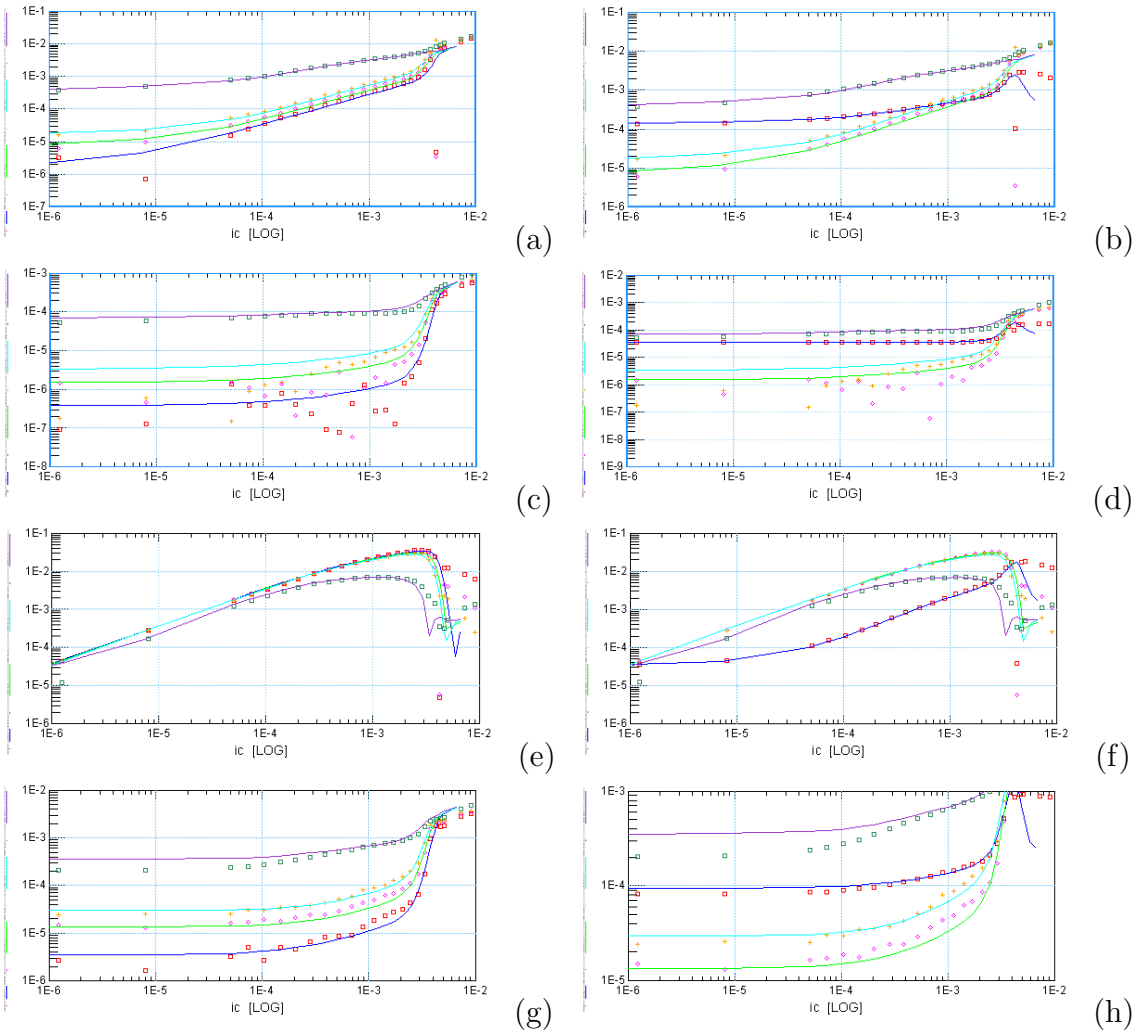

Figure 2.7: Measured (symbols) and modeled (curves) Y-parameters at 1,2,3 and 5 GHz for 162 K. (a) Real part Y_{11}; (b) Imaginary part Y_{11}; (c) Real part Y_{12}; (d) Imaginary part Y_{12};(e) Real part Y_{21}; (f) Imaginary part Y_{21};(g) Real part Y_{22}; (h) Imaginary part Y_{22}.

Chapter 3

RF Noise Sources

Since the lower limit of dynamic range is set by the noise, successful circuit design requires accurate noise compact models that can faithfully and efficiently describe transistor electrical characteristics across a wide frequency, biasing and temperature range. Accurate noise compact model is in particular important for mixed-signal analog and RF circuit design, like low noise amplifier(LNA) design [1]. In industry, the current standard noise model is essentially the same as what was in early SPICE Gummel-Poon model, which is showed in Fig. 3.1 and discussed in the first two sections of this chapter. But at high frequency, the extra correlated terminal current noise should be considered. At high V_{CB}, multiplication of impact ionization occurs, which introduces avalanche current from collector to base. Therefore, extra noise sources due to avalanche effect should be considered.

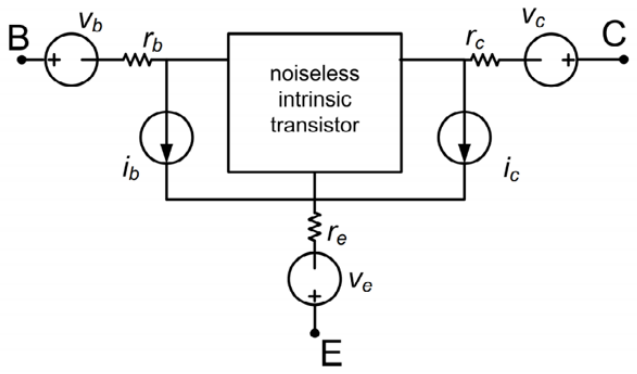

Figure 3.1: RF noise sources of a transistor.

3.1 Thermal Noise

The operation of semiconductor devices is based on free carriers transportation [28]. From the equivalent circuit and compact modeling stand point, the velocity fluctuation caused by majority carrier thermal motion can cause the thermal noises of resistances, which are r_b, r_c and r_e showed in Fig. 3.1.

As described by the Nyquist theorem, the power spectral density (PSD) of thermal noise voltage of a resistance R is usually given by [19]

$$S_{vr,vr^*} = 4KTR, \tag{3.1}$$

and the PSD of thermal noise current is [19]

$$S_{ir,ir^*} = \frac{4KT}{R}, \tag{3.2}$$

where K is the Boltzmann constant and T the standardized noise source temperature 290 K.

3.2 Terminal Current Noise

A classical shot noise theory believes that the base current shot noise is caused by the holes in base moving across the EB junction potential barrier, while the collector current shot noise is caused by the electrons in collector moving across the CB junction potential barrier [28]. However, at high injection, this theory dose not hold. Therefore, it is generally believed that the velocity fluctuation caused by minority carrier thermal motion can equivalently cause the intrinsic terminal current noises [1] [26] [27]. So the base current shot noise is caused by the holes in the emitter moving to base, while the collector current shot noise is caused by the electrons in the base moving to emitter. The PSDs of shot noise are as follow

[19]:

$$\begin{cases} S_{i_c,i_{c^*}} = 2qI_{C0}, \\ S_{i_b,i_{b^*}} = 2qI_{B0}, \end{cases} \tag{3.3}$$

where I_{B0} and I_{C0} are base and collector DC current.

3.3 Correlation Noise

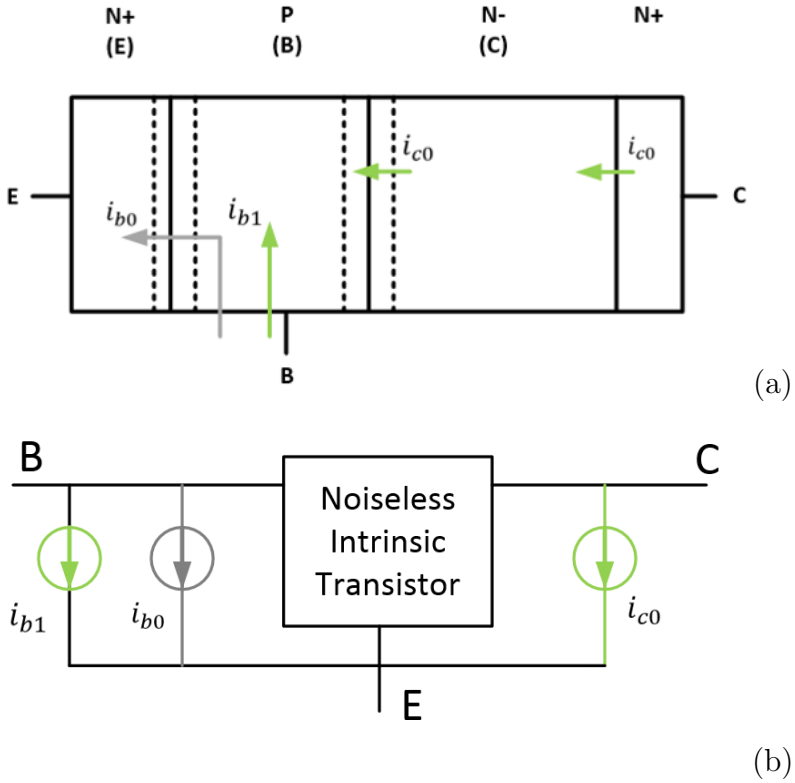

Figure 3.2: (a) Illustration of the terminal noise sources including correlation noise. (b) Noise equivalent circuit including correlation noise.

Considering various noise physics mechanisms, a correlation noise model was developed [17]. Fig. 3.2 illustrates the model including terminal current noises due to minority carrier velocity fluctuation and correlated noise between i_{b0} and i_{c0}. i_{b0} is the base noise current resulting from minority hole velocity fluctuation at emitter, with a PSD of $2qI_{B0}$. i_{c0} is the collector noise current resulting from minority electron velocity fluctuation at base, with a

PSD of $2qI_{C0}$. i_{b0} and i_{c0} are independent of frequency and each other. The extra base current noise i_{b1} is added from base to emitter, using green color in Fig. 3.2 to illustrate that it is correlated with i_{c0}.

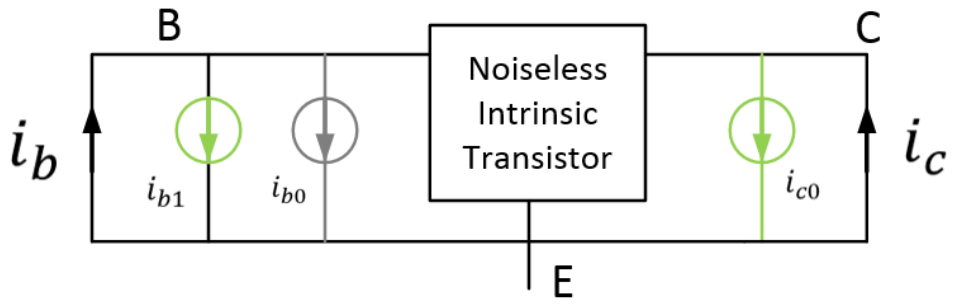

Figure 3.3: Illustration of base and collector terminal noise currents derivation including correlation noise.

Fig. 3.3 shows the base and collector terminal noise currents, in which base-emitter and collector-emitter are both shorted. Assuming base terminal noise current flows from emitter to base and collector terminal noise current flows from emitter to collector, the expressions for both noise currents are:

$$\begin{cases} i_b = i_{b0} + i_{b1}, \\ i_c = i_{c0}, \end{cases} \tag{3.4}$$

Based on Equation (3.3), (3.4) and $i_{b1} = j\omega\tau_n i_{c0}$, the final PSDs of noise model considering correlation noise are:

$$\begin{cases} S_{i_c,i_{c^*}} = \frac{i_{c0}\cdot i_{c0}^*}{\Delta f} = 2qI_{C0}, \\ S_{i_b,i_{b^*}} = \frac{(i_{b0}+i_{b1})\cdot(i_{b0}+i_{b1})^*}{\Delta f} = 2qI_{B0} + 2qI_{C0}\omega^2\tau_n^2, \\ S_{i_c,i_{b^*}} = \frac{i_{c0}\cdot i_{b1}^*}{\Delta f} = -j2qI_{C0}\omega\tau_n, \end{cases} \tag{3.5}$$

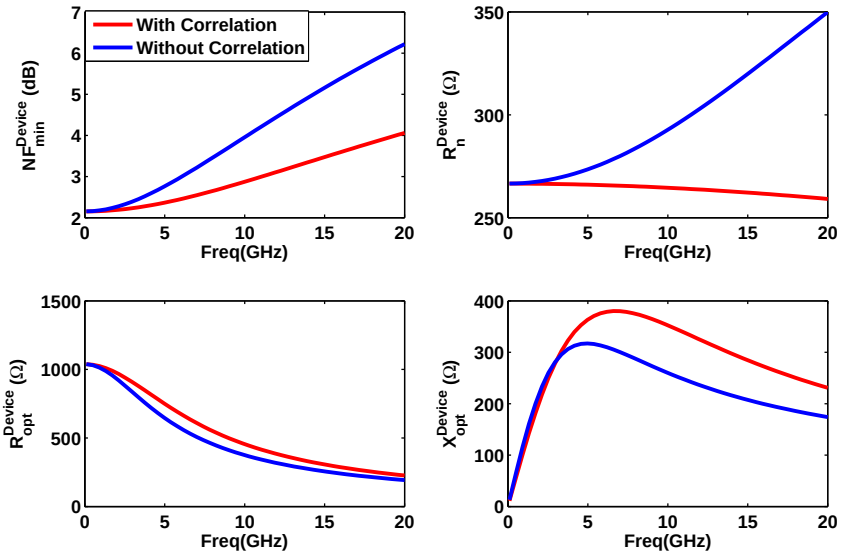

Figure 3.4: Simulation device noise parameters with and without correlation noise versus frequency. $J_C = 1$ mA/μm^2.

where ω=$2\pi f$, τ_n is the noise transit time [17].

$$\tau_n = F_g \frac{Q_{be} + Q_{bc}}{I_N}, \tag{3.6}$$

where Q_{be} and Q_{bc} are BE junction electric charge and CB junction electric charge. I_N is noise main current. F_g is a fraction factor for correlation noise, which is 0.5 for the model used in this thesis.

Fig. 3.4 shows noise parameters versus frequency at $J_C = 1$ mA/μm^2, which approximately gives peak f_T. The red lines represent noise parameters using the model considered correlation noise and the blue lines represent noise parameters using the model without considering correlation noise. At relatively high frequency, the NF_{min} considering correlation noise becomes smaller than the NF_{min} without considering correlation noise. With increasing frequency, the difference between NF_{min} of these two noise models increases.

Fig. 3.5 shows noise parameters versus J_C, at f=5 GHz. Not only the increasing frequency could enhance the effect of correlation noise, but also, at a fixed frequency, with

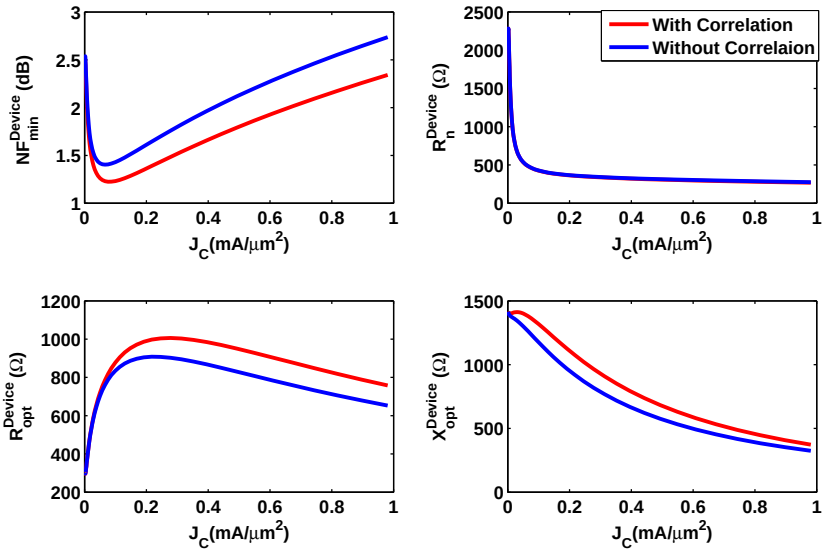

Figure 3.5: Simulation device noise parameters with and without correlation noise versus J_C. f=5 GHz.

increasing J_C, the difference between considering and without considering correlation noise increases.

In Chapter 4 and 5, the temperature dependent device and LNA simulations set J_C = 0.1 mA/μm^2 and f = 5 GHz. It is necessary to understand how important correlation noise is for temperature dependent simulation at different collector current densities and frequencies. Fig. 3.6 shows the device noise parameters with and without correlation noise versus temperature. The difference between NF_{min} considering correlation noise and NF_{min} without considering correlation noise, at J_C = 0.1 mA/μm^2 and f = 5 GHz, is about 0.1 dB in a wide temperature range, which is small enough to neglected for simplification.

Fig. 3.7 shows the device noise parameters with and without correlation noise versus temperature. The difference between NF_{min} considering correlation noise and NF_{min} without considering correlation noise, at J_C = 0.1 mA/μm^2 and f = 20 GHz, is about 1.5 dB in a wide temperature range, which is so large that the correlation noise has to be considered.

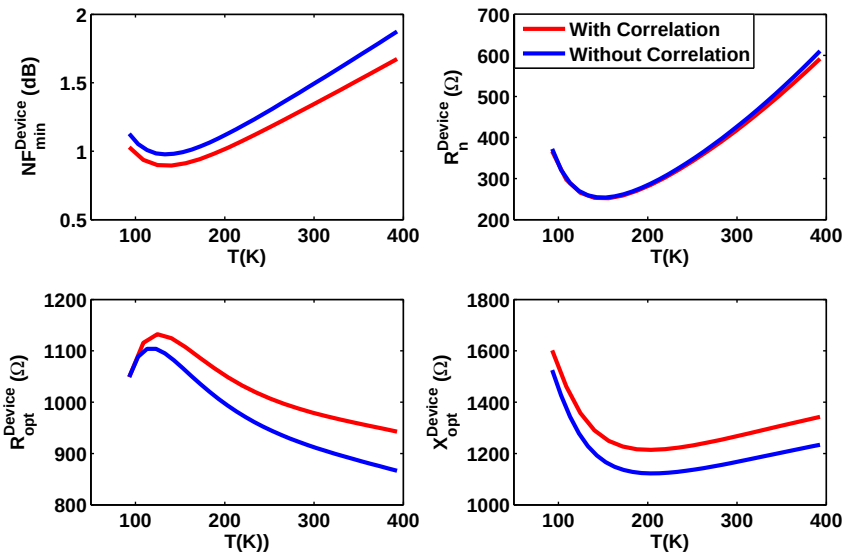

Figure 3.6: Simulation device noise parameters with and without correlation noise versus temperature. $J_C = 0.1$ mA/μm^2, $f = 5$ GHz.

3.4 Avalanche Noise

For a long time, bipolar transistors have been operated within the limits set by the collector-emitter breakdown voltage BV_{ceo}. However, with the large increase of cut-off frequency, this breakdown voltage has decreased. In order to keep some of design freedom, more and more designs use a supply voltage V_{CE} larger than BV_{ceo}, which means a very high V_{CB} [18]. At this circumstance, multiplication of impact ionization occurs.

Fig. 3.8 illustrates the formation of base and collector currents with the impact ionization. Since V_{CB} is very high, the electron flows from base to collector. In the process, multiplication of impact ionization happens. The electron current from base to collector increases from I_{C0} to MI_{C0}, correspondingly, the hole current from collector to base increases from 0 to $(M-1)I_{C0}$. M is the multiplication factor of impact ionization [24] [25].

Fig. 3.9 shows the current equivalent circuit. I_{B0} and I_{C0} represent the original base and collector current and $(M-1)I_{C0}$ represents the avalanche current due to impact ionization. Based on Fig. 3.8, the total collector and base current seen at the terminal now are:

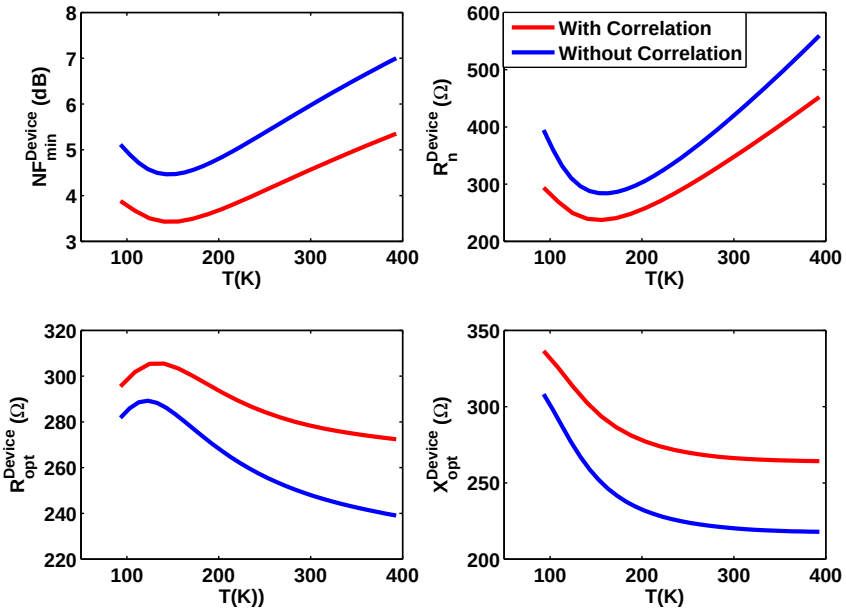

Figure 3.7: Simulation device noise parameters with and without correlation noise versus temperature. $J_C = 0.1$ mA/μm^2, $f = 20$ GHz.

$$\begin{cases} I_C = I_{C0} + (M-1)I_{C0}, \\ I_B = I_{B0} - (M-1)I_{C0}, \end{cases} \tag{3.7}$$

Since the impact ionization introduces an extra current, of course, it introduces extra noises. Fig. 3.10(a) illustrates the terminal noise sources considering avalanche effect. Compared with Fig. 3.2(a), there are two additional noises. $(M-1)i_{c0}$ represents the multiplication of the noise in the collector current due to avalanche effect. i_{II} represents the noise due to impact ionization itself [18] [20].

Fig. 3.10(b) shows the noise equivalent circuit considering avalanche noise. $(M-1)i_{c0}$ is added from collector to base, using green color to illustrate that it is generated from i_{c0}. i_{II} is also added from collector to base, using red color to illustrate that it is a independent noise source from i_{c0} and i_{b0}.

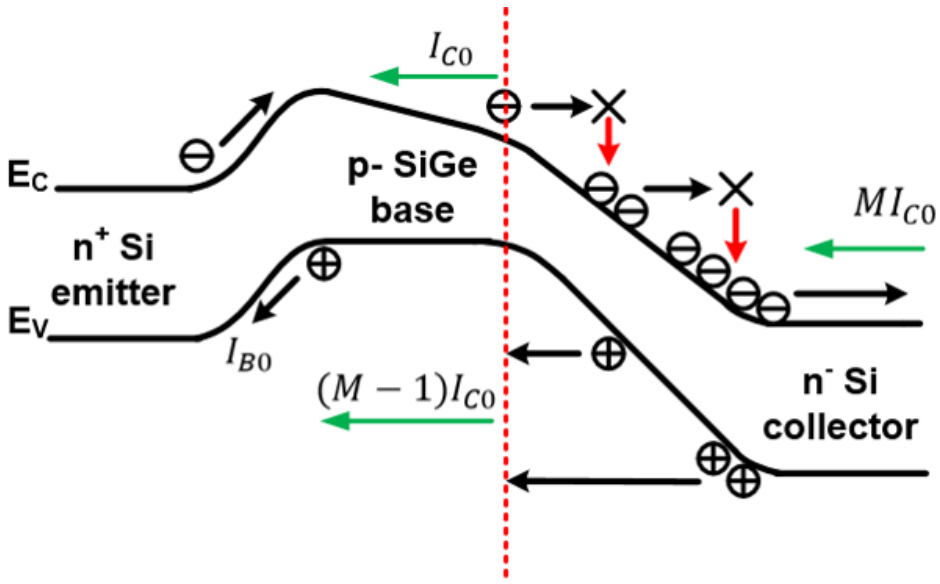

Figure 3.8: Formation of base and collector currents considering avalanche effect.

Fig. 3.11 showed the base and collector terminal noise currents, in which base-emitter and collector-emitter are both shorted. Assuming base terminal current flows from emitter to base and collector terminal current flows from emitter to collector, the expressions for both currents are:

$$\begin{cases} i_b = i_{b0} + i_{b1} - (M-1)i_{c0} - i_{II}, \\ i_c = i_{c0} + (M-1)i_{c0} + i_{II}, \end{cases} \tag{3.8}$$

Based on Equation (3.3), (3.8) and $i_{II} = M(M-1)i_{c0}$, the final PSDs of noise model including both correlation and avalanche noise are [20] [21]:

$$\begin{cases} S_{i_c,i_{c^*}} = \frac{(i_{c0}+(M-1)i_{c0}+i_{II})\cdot(i_{c0}+(M-1)i_{c0}+i_{II})^*}{\Delta f} = 2qI_{C0}(2M-1)M, \\ S_{i_b,i_{b^*}} \frac{(i_{b0}+i_{b1}-(M-1)i_{c0}-i_{II})\cdot(i_{b0}+i_{b1}-(M-1)i_{c0}-i_{II})^*}{\Delta f} = 2qI_{B0} + 2qI_{C0}((M-1)(2M-1)+\omega^2\tau_n^2), \\ S_{i_c,i_{b^*}} = \frac{(i_{c0}+(M-1)i_{c0}+i_{II})\cdot(i_{b1}-(M-1)i_{c0}-i_{II})^*}{\Delta f} = -j2qI_{C0}\omega\tau_n + 4M(M-1)qI_{C0}, \end{cases} \tag{3.9}$$

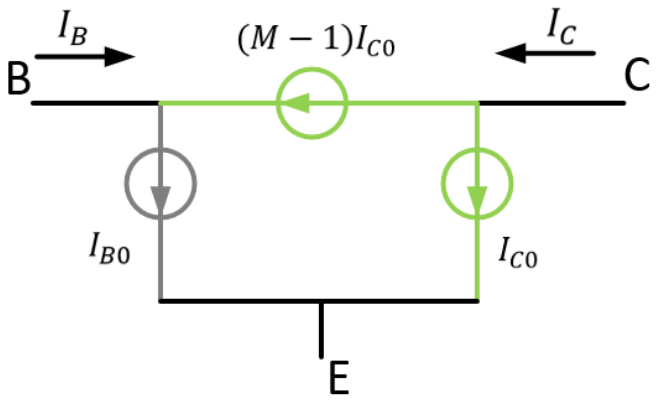

Figure 3.9: Equivalent circuit of base and collector currents including impact ionization.

Fig. 3.12 shows the basic parameters of the transistor, like I_B,I_C,f_T and avalanche factor versus V_{CB}, at 5 GHz. I_B decreases with increasing V_{CB} and eventually becomes a negative number. The black dash lines in the I_B-V_{CB} plot show the corresponding V_{CB} when I_B becomes zero, which means at this V_{CB} the device comes to its collector-emitter break down voltage BV_{ceo}. I_C increases with increasing V_{CB}. Avalanche factor $M-1$ remains about 0 at low V_{CB}. Once V_{CB} is high enough, especially when supply voltage is beyond break down voltage, avalanche factor increases rapidly with increasing V_{CB}.

Fig. 3.13 shows the noise parameters versus V_{CB} with $V_{BE} = 0.85$ V and $f = 5$ GHZ. Once V_{CB} is above 2 V, all the noise parameters considering avalanche noise have a large difference from those without considering avalanche noise. The differences between noise parameters considering avalanche noise and those without considering avalanche noise increase with increasing V_{CB}. NF_{min} considering avalanche noise is at least 2 dB larger than NF_{min} without considering avalanche noise when V_{CB} is about 4 V.

Fig. 3.14 shows the noise parameters versus V_{CE} with $V_{CB} = 3$ V and $f = 5$ GHZ. Since 3 V is relatively high value for V_{CB}, which we can know from Fig. 3.13, NF_{min} with avalanche noise is much larger than NF_{min} without avalanche noise in most bias.

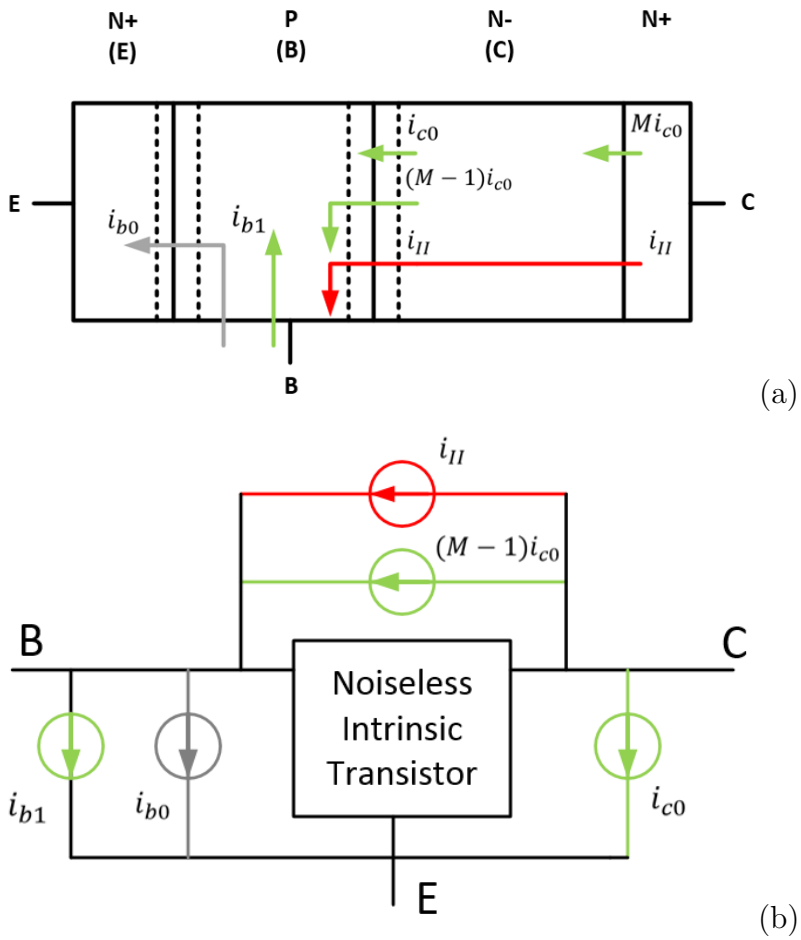

Figure 3.10: (a) Illustration of the terminal noise sources including avalanche noise. (b) Noise equivalent circuit including avalanche noise.

Since this thesis concerns about the noise performance in a wide temperature range, we definitely want to understand with changing temperature how avalanche noise changes and whether it can be neglected or not.

Fig. 3.15 shows the avalanche effect at $V_{CB} = 3$ V in a wide temperature range from 93 to 393 K, which proves that with this high V_{CB}, the difference between NF_{min} considering avalanche noise and NF_{min} without considering avalanche noise is quite large in a wide temperature range. Another characteristic we can observe is that with decreasing temperature, the avalanche effect becomes more and more important, which is because of the increasing multiplication factor of impact ionization with decreasing temperature showed in Fig. 3.16.

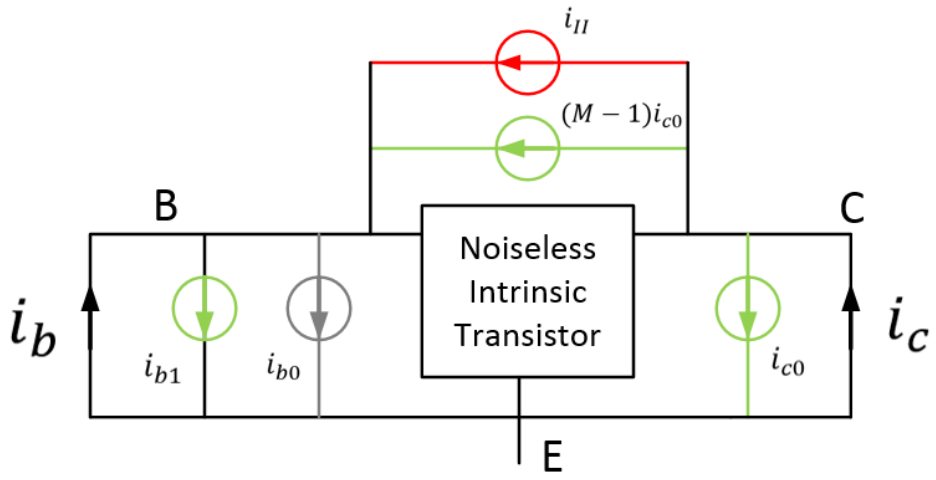

Figure 3.11: Illustration of base and collector terminal noise current derivation including avalanche noise current.

The V_{CB} of device simulation and LNA design showed in Chapter 4 and 5 is below 1.5 V. Based on Fig. 3.13, once V_{CB} is below 2 V, the avalanche noise is safe to be neglected. However, at low temperature, with higher multiplication factor of impact ionization, there is no guarantee that it is still small enough to be ignored. So Fig. 3.17 is showed below. Even at low temperature, with a higher multiplication factor of impact ionization, the NF_{min} considering avalanche noise is almost the same as the NF_{min} without considering avalanche noise. So for the simulations in Chapter 4 and 5, avalanche noise is small enough to be neglected.

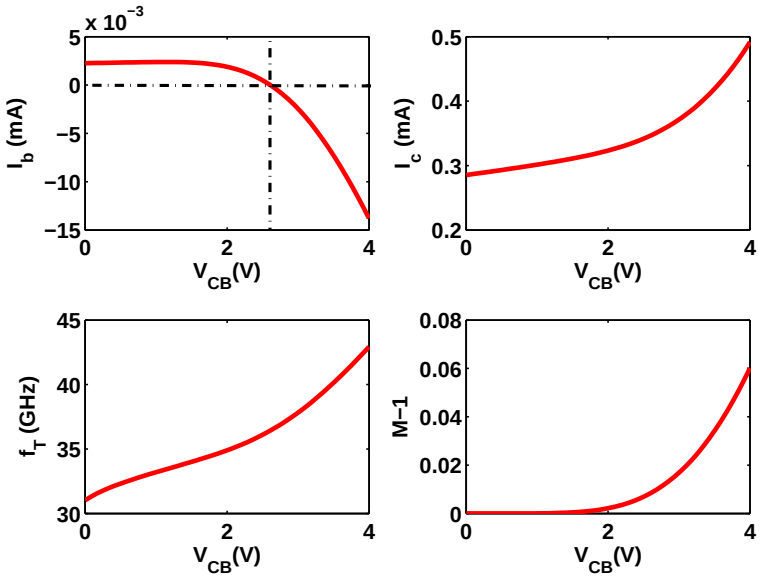

Figure 3.12: Simulated I_B,I_C,f_T and avalanche factor versus V_{CB}.f=5 GHz.

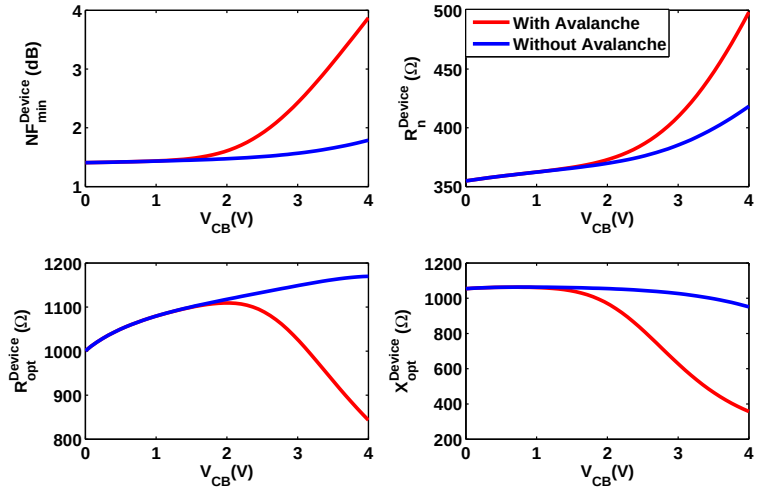

Figure 3.13: Simulation device noise parameters with and without avalanche noise versus V_{CB}. V_{BE}=0.85 V. f=5 GHz.

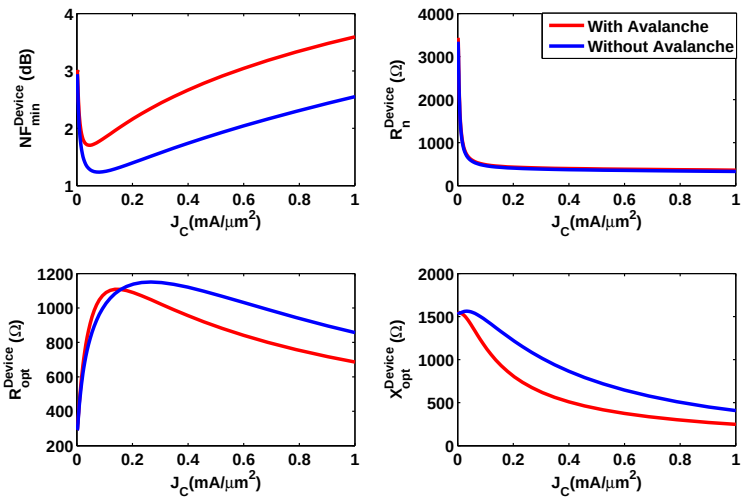

Figure 3.14: Simulation device noise parameters with and without avalanche noise versus V_{BE}. V_{CB}=3 V. f=5 GHz.

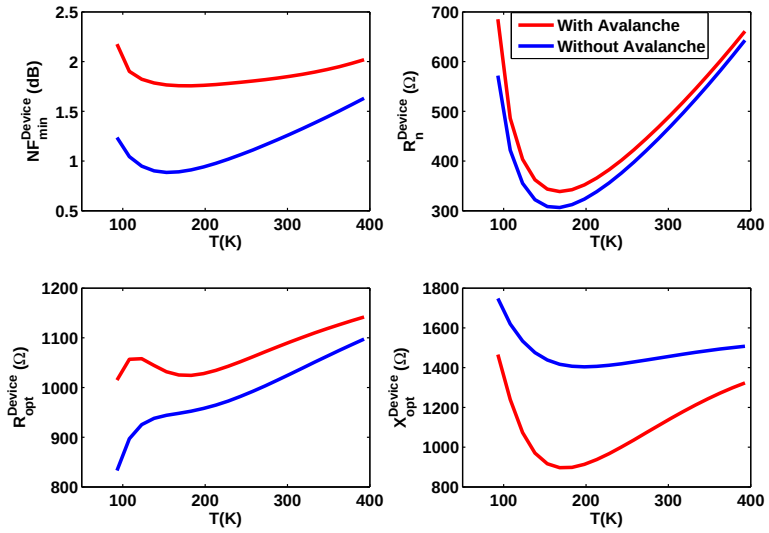

Figure 3.15: Simulation device noise parameters with and without avalanche noise versus temperature. V_{CB}=3 V. f=5 GHz.

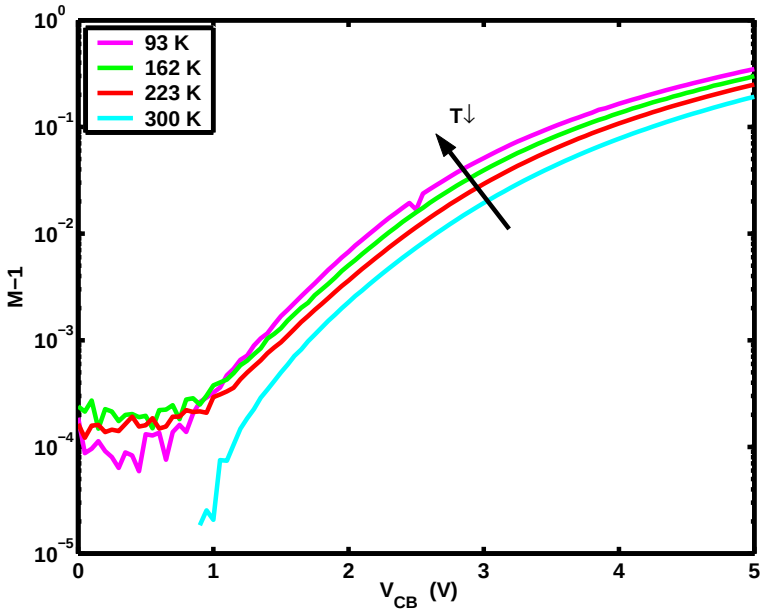

Figure 3.16: Measured $M-1$ versus V_{CB} at 93, 162, 223 and 300 K [2].

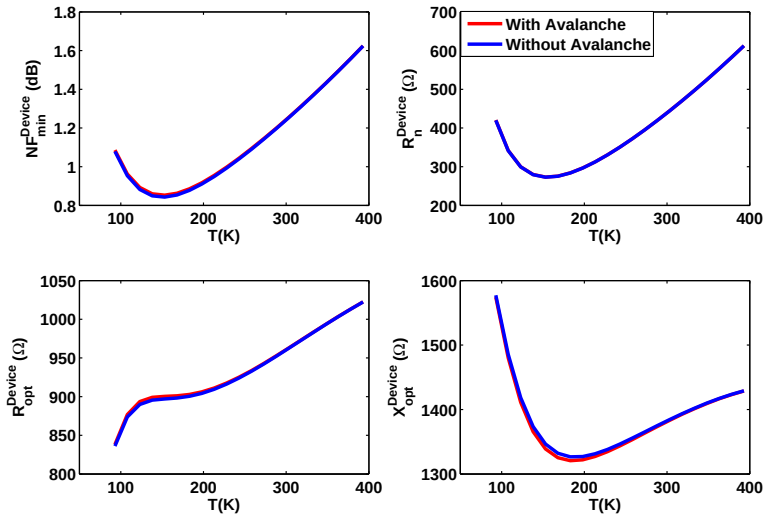

Figure 3.17: Simulation device noise parameters with and without avalanche noise versus temperature. V_{CB}=1 V. f=5 GHz.

Chapter 4

Device Noise Parameters

The noise performance of a transistor can be expressed by several noise parameters, which are minimum noise factor NF_{min}, noise resistance R_n, optimum source admittance $Y_{s,opt}$. So in this chapter, the device noise parameters at different bias and temperatures are discussed.

4.1 Noise Parameters Introduction

The noise factor F of a network is defined as the input signal to noise ratio(SNR) divided by the output signal to noise ratio(SNR) illustrated in Fig. 4.1 and Equation (4.1).

$$F = \frac{S_i/N_i}{S_o/N_o} = \frac{N_o}{Gain \times N_i} \tag{4.1}$$

If the amplifier is perfect, the output noise equals to the input noise multiplied by the gain of the amplifier, which gives same SNR at both the input and output of the amplifier. For any real-world amplifier, the output noise is larger than the input noise multiplied by the gain of the amplifier due to the noise of the amplifier itself. So the noise factor is larger than one. Noise figure NF is simply the noise factor expressed in decibels, as:

$$NF = 10 \times log(F). \tag{4.2}$$

Noise factor is determined by noise parameters and source terminal admittance, which is expressed in Equation (4.3) [29]:

$$F = F_{min} + \left(\frac{R_n}{G_s}\right) |Y_s - Y_{s,opt}|^2 \tag{4.3}$$

where source impedance $Y_s = G_s + jX_s$.

With this equation, we can see that the noise factor F varies as a function of source impedance and three noise parameters. These three noise parameters are minimum noise factor F_{min}, optimum impedance Y_{opt} and noise resistance R_n. When the source impedance equals optimum impedance, noise factor equals to minimum noise factor, which is called noise matching. When source impedance does not equal to optimum impedance, as a sensitivity term, noise resistance controls how fast noise factor degrades.

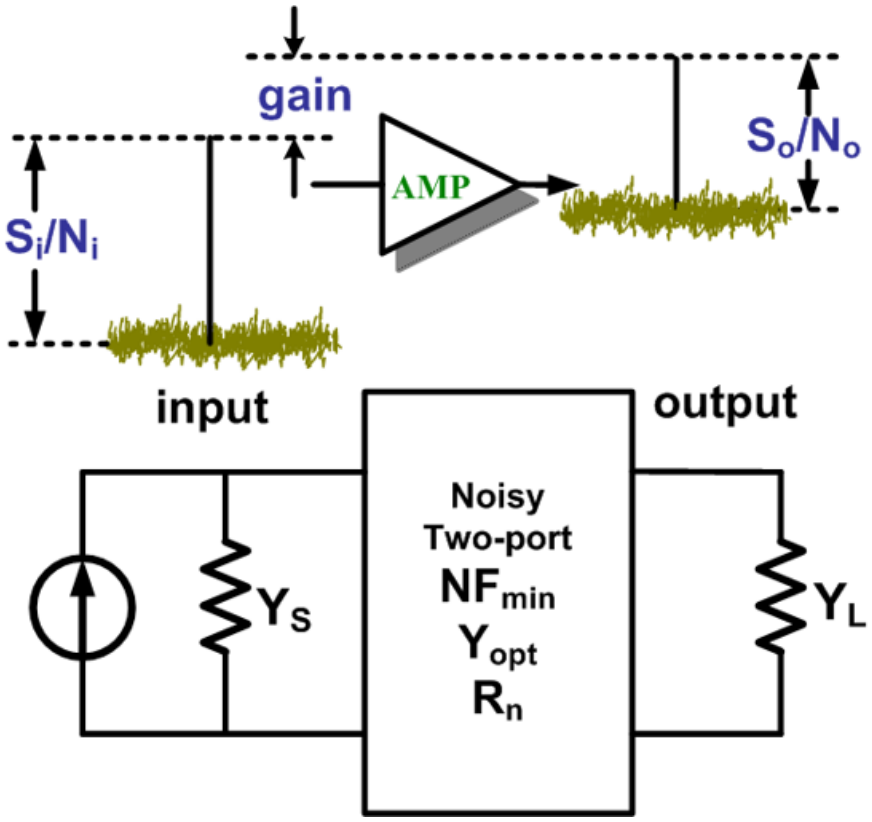

Figure 4.1: Noise factor illustration

4.2 Device Noise Performance

Fig. 4.2 shows simulated transistor noise parameters versus collector current density J_C, including minimum noise figure NF_{min}^{Device}, noise matching source resistance and reactance, R_{opt}^{Device} and X_{opt}^{Device}, and noise resistance R_n^{Device}, using temperature as a parameter. Emitter

area A_E is 0.5×2.5 μm^2. R_{opt}^{Device}, X_{opt}^{Device}, and R_n^{Device} are normalized by emitter length. At all temperatures, NF_{min}^{Device} shows a minimum at a J_C much smaller than the peak f_T J_C. This minimum NF_{min}^{Device} with respect to J_C and the J_C at which the minimum occurs both vary with temperature, as shown in Fig. 4.3. The increase of NF_{min}^{Device} with J_C after the minimum value is more rapid at 93 K than at other temperatures, as can be seen from Fig. 4.2.

At the same J_C, cooling from 300 to 162 K decreases NF_{min}^{Device}, but further cooling to 93 K increases NF_{min}^{Device} slightly. Interestingly, at the same J_C, R_{opt}^{Device}, X_{opt}^{Device}, and R_n^{Device} show fairly weak temperature dependence. A weak temperature dependence of R_{opt}^{Device} and X_{opt}^{Device} is beneficial from a LNA optimization perspective, as noise matching is approximately maintained as the temperature changes. Consequently, noise figure remains minimized at NF_{min}^{Device}, which itself can decrease with cooling. Constant biasing current can be realized with a bandgap reference circuit. Wide temperature range bandgap references have been experimentally demonstrated with the same SiGe HBTs used in this work [5].

Fig. 4.4 shows noise parameters versus temperature at a relatively low J_C of 0.1 mA/μm^2 that is of interest for the LNAs. At this J_C, NF_{min}^{Device} is close to its minimum with respect to J_C variation, at all temperatures. J_C and the corresponding I_C required for noise matching is low. f_T is reasonably high, and increases from 19 GHz at 393 K to 41 GHz at 93 K, which together with the natural decrease of thermal noise help to decrease NF_{min}^{Device} with cooling. Except at the lowest temperatures, cooling decreases NF_{min}^{Device}, X_{opt}^{Device} and R_n^{Device}, and increases R_{opt}^{Device}. The relative changes of R_{opt}^{Device} and X_{opt}^{Device}, however, are small across the whole temperature range. The rise of NF_{min}^{Device} with cooling below 150 K is attributed to the increase of base resistance due to carrier freeze-out. R_b is the sum of a bias independent extrinsic component and a bias dependent intrinsic component due to distributive effect [22].

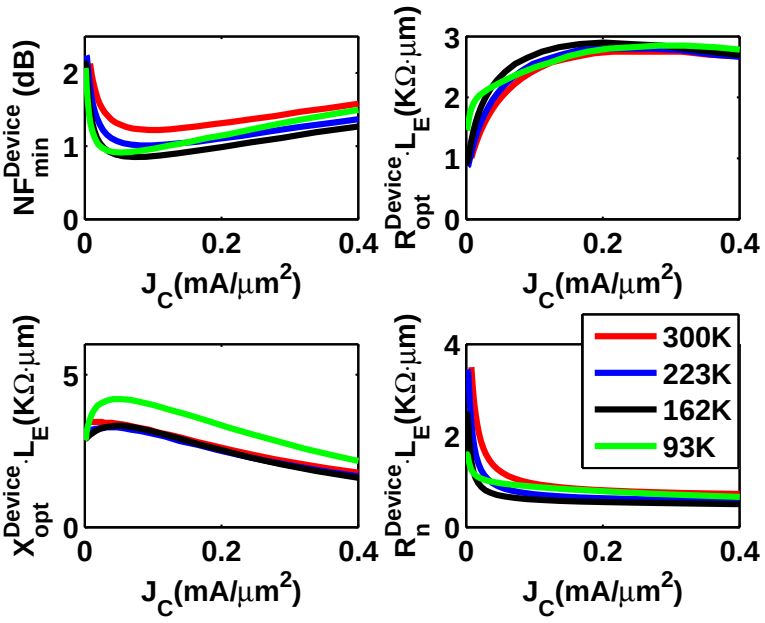

Figure 4.2: Simulated device noise parameters versus J_C at multiple temperatures. f=5 GHz.

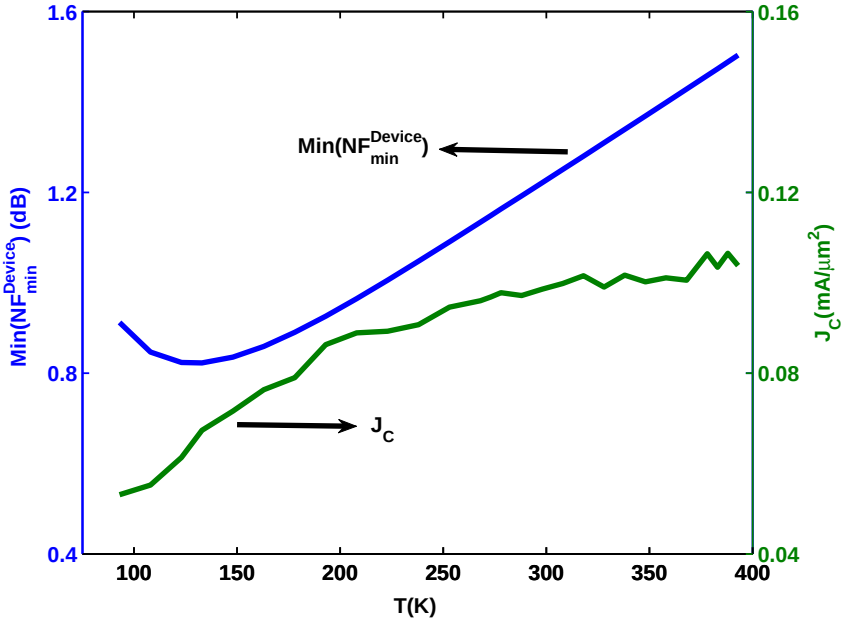

Figure 4.3: Simulated minimum of NF_{min}^{Device} on the $NF_{min} - I_C$ curve and the I_C at which this occurs versus temperature. f=5 GHz.

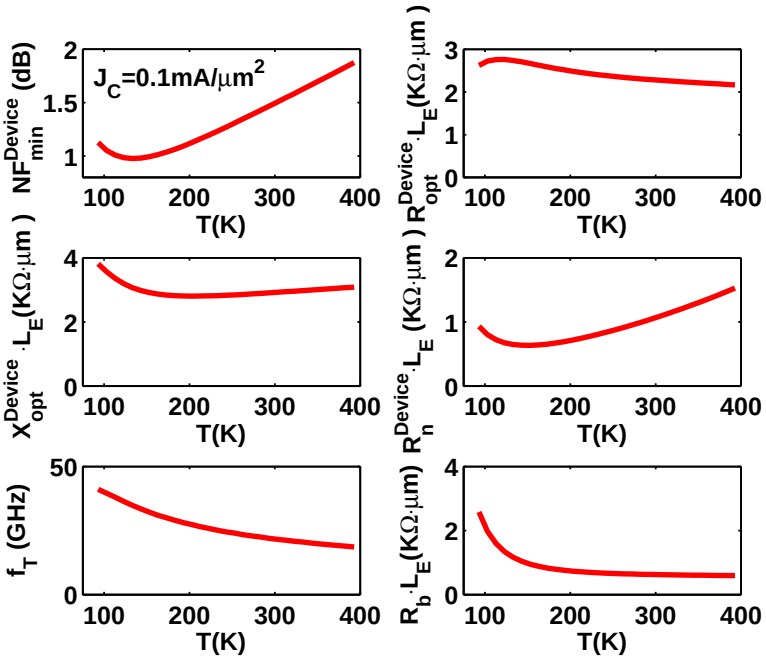

Figure 4.4: Simulated device noise parameters, f_T and R_b versus temperature at J_C=0.1 mA/μm^2. f=5 GHz.

Chapter 5

LNA Design

5.1 Design Methodology

To make a LNA design, our goal is to achieve simultaneous noise and impedance matching, which means $R_{opt} = R_s = 50\ \Omega$, $X_{opt} = 0$ for noise matching and $R_{in} = R_s = 50\ \Omega$, $X_{in} = 0$ for impedance matching.

To investigate temperature dependence of the RF LNA, we designed impedance-matched LNAs following a popular design methodology at various temperatures [23] [6]. A simplified schematic is shown in Fig. 5.1 [15]. Here, C_b is for DC blocking, and L_{bias} is for RF blocking; L_e and L_b are for input impedance matching, and L_c and C_c are for output impedance matching. R_c=500 Ω is used for stability. We chose to use the same emitter length L_E for Q_1 and Q_2 and $V_{CC} = 3$V. $V_{B2} = 2.5$V. V_{B1} is used to set the bias current density J_C.

The essence of the LNA design methodology for wide temperature range operation is as follows. At a given J_C, emitter length L_E is scaled so that R_{opt}^{Device}=R_s=50 Ω, which also sets LNA's R_{opt} to 50 Ω as adding L_e and L_b will not affect R_{opt} to first order [23] [6]. Real part noise matching is now achieved. The emitter and base inductors L_e and L_b are then optimized for input impedance matching, i.e. $Z_{in} = Z_s = R_s$. At 300 K, this typically results in $X_{opt}^{\text{LNA}} \approx 0$, a fortunate case given that the imaginary part of the noise matching is also approximately achieved. Noise matching and impedance matching are then simultaneously achieved, and $NF^{\text{LNA}} \approx NF_{min}^{\text{LNA}}$ [15] [16]. At the simulation condition used in this chapter, correlation noise and avalanche noise are small enough to be neglected, which has been proved in Chapter 3.

5.2 LNAs Performance in A Wide Temperature Range

Using this methodology, we first designed three LNAs for optimal operation at three temperatures, 300, 162 and 93 K, at a J_C of 0.1 mA/μm^2, a value often used for 300 K LNA design using this technology. The good news is that we can still achieve simultaneous noise matching and impedance matching at other temperatures. For each LNA design, we then varied the temperature from 93 to 393 K to examine how the LNA performance responds to operating temperature variations.

The results are summarized in Fig. 5.2 and Fig. 5.3 for all three LNA designs. Fig. 5.2 shows NF_{min}^{LNA}, NF^{LNA}, R_{opt}^{LNA}, X_{opt}^{LNA}, R_{in}, X_{in} versus operating temperature. All three LNAs show nearly identical NF^{LNA}, which is practically the same as NF_{min}^{LNA}, at all operating temperatures, regardless of the original design temperature, as can be seen from Fig. 5.2. This is because of the weak temperature dependence of R_{opt}^{LNA} and X_{opt}^{LNA}, as well as a small noise resistance R_n^{LNA}. The input impedance deviates much more from 50 Ω than R_{opt}^{LNA} does, as can be seen from the R_{in}^{LNA} and X_{in}^{LNA} curves. To first order, $R_{in} = R_b + \omega_T L_e$ [6], which explains the increase of R_{in} with cooling over most temperatures as both R_b and f_T increase with cooling.

Fig. 5.3 shows the corresponding S_{11}, S_{22}, Gain, $IIP3$, $OIP3$ versus operating temperature. Overall S_{11}, however, is still better than -13 dB in the whole temperature range, which is still acceptable from a system perspective. S_{22} shows similar degradation as operating temperature deviates from the design temperature. Gain decreases with cooling because of increasing f_T. With respect to LNA linearity, the third-order input intercept, $IIP3$, and third-order output intercept, $OIP3$, show considerable degradation below 120 K, as expected from the more nonlinear $I_C - V_{BE}$ dependence. This suggests that one may need to increase current density and LNA current to maintain desired LNA linearity at lower operating temperatures.

Fig. 5.4 shows results of LNA design versus J_C at 93, 162 and 300 K. At the same J_C, the emitter length required for R_{opt}^{LNA}=50 Ω and hence I_C of the LNA is not very different at

the different temperatures. NF^{LNA} is practically the same as NF_{min}^{LNA}, despite the deviation of X_{opt}^{LNA} from 0 by as much as 10 Ω, because of small noise resistance at large emitter length [15].

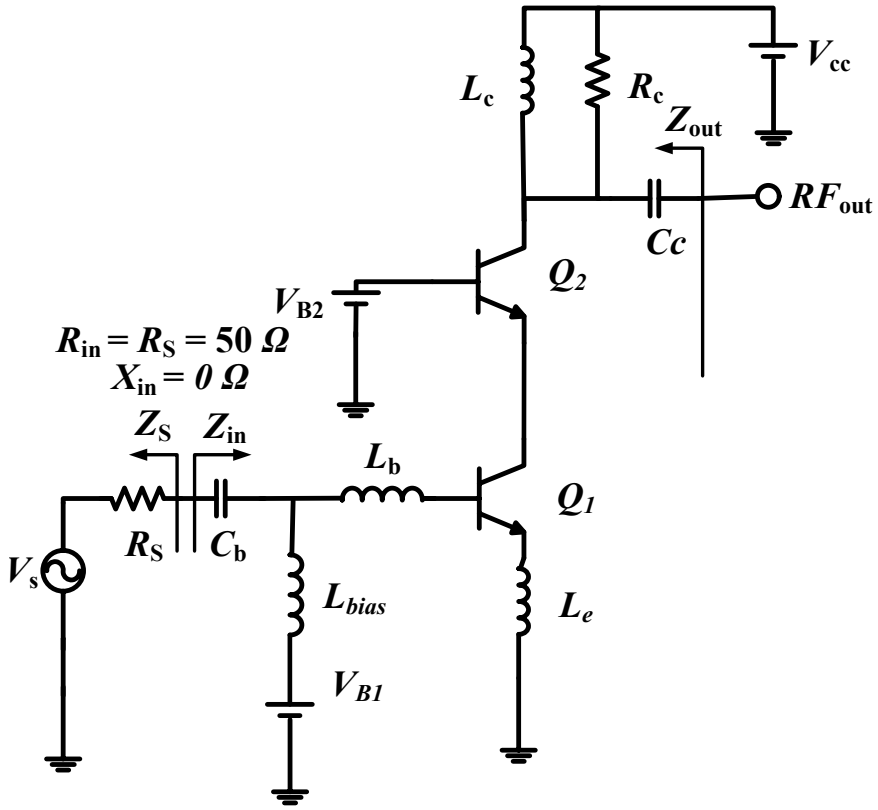

Figure 5.1: A simplified schematic of cascode LNA used.

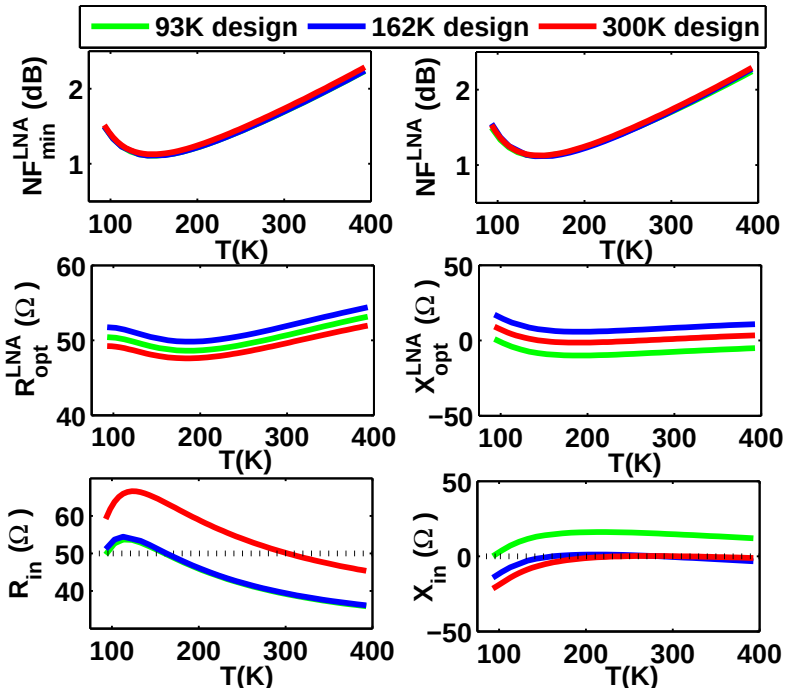

Figure 5.2: Simulated NF_{min}^{LNA}, NF^{LNA}, R_{opt}^{LNA}, X_{opt}^{LNA}, R_{in}, X_{in} versus operating temperature of three LNAs designed at 93 K, 162 K and 300 K. J_C=0.1 mA/μm^2, f=5 GHz.

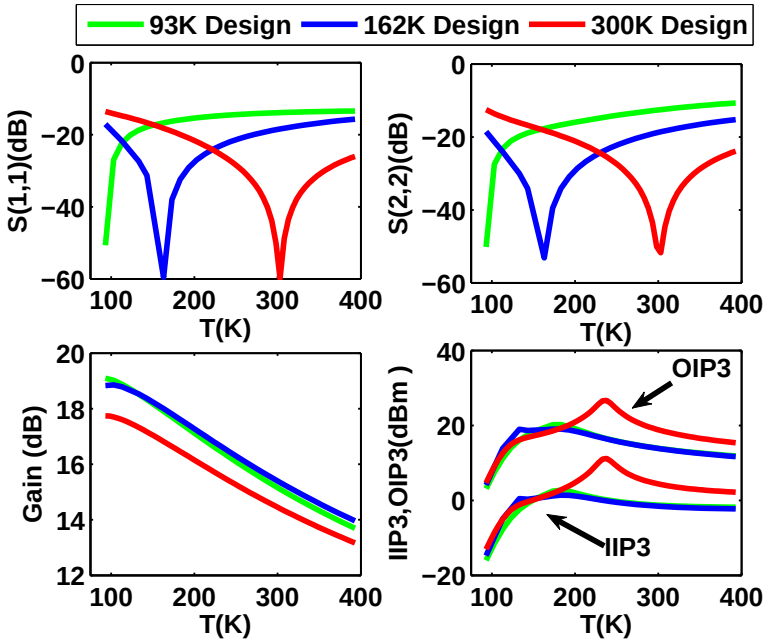

Figure 5.3: Simulated S_{11}, S_{22}, Gain, $IIP3$, $OIP3$ versus operating temperature of three LNAs designed at 93 K, 162 K and 300 K. J_C=0.1 mA/μm^2, f=5 GHz.

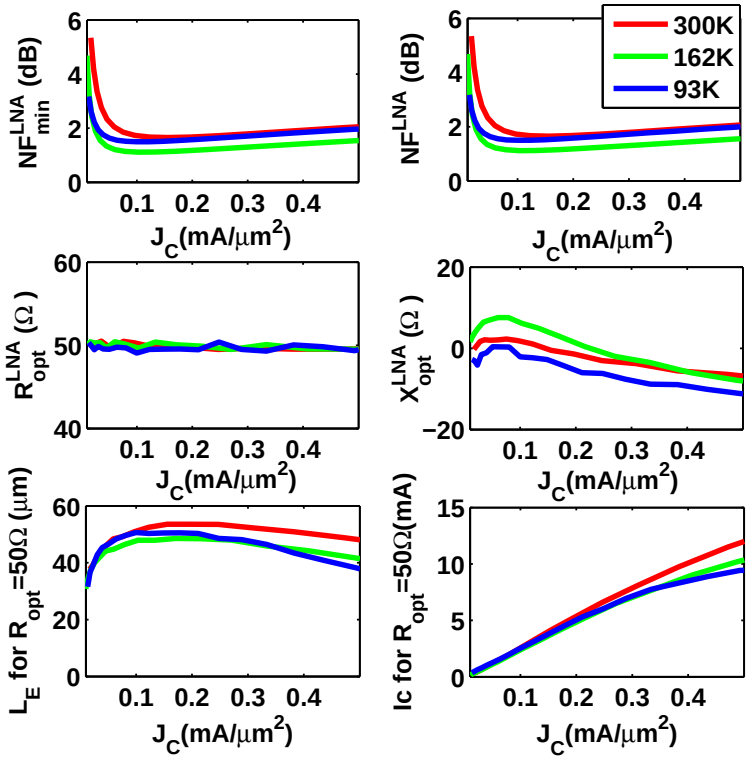

Figure 5.4: Simulated NF_{min}, NF, R_{opt}, X_{opt}, and corresponding L_E and I_C of LNAs versus J_C. f= 5 GHz.

Chapter 6

Summary

The wide temperature range model has been shown and device characteristic of this model has been checked with measurement data. Using this model, correlation and avalanche noise has been introduced to make an accurate noise model. At high frequency, considering correlation between base noise current and collector noise current reduces NF_{min}. The reduction increases with increasing frequency. At high V_{CB}, especially when supply voltage is much larger than BV_{ceo}, avalanche noise should be considered, which increases NF_{min}. With increasing V_{CB} or decreasing temperature, the multiplication factor of impact ionization increases, which leads to a higher avalanche noise.

SiGe HBT RF noise parameters and LNA designs have been investigated for operation across a wide temperature range from 93 to 393K. Minimum noise figure improves with cooling, primarily due to the f_T increase, and shows a slight degradation below 150 K due to rapid increase of base resistance induced by carrier freeze-out. With cooling, an LNA designed at 300 K shows a noise figure that remains close to the minimum noise figure, with higher gain, and worse, but still acceptable, input and output impedance matching, provided that a constant bias current is maintained with cooling. Linearity degradation is observed below 120K, which may require a design adjustment such as the use of a higher bias current for high linearity applications. Taken together, these modeling results provide guidelines for LNA designs for low temperature operation, as well as robust operation across a wide temperature range.

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