SPICE model implementation of a quantum phase-slip junction

by

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Abstract

A quantum phase-slip is a superconducting phenomenon, which is identified as an exact dual to Josephson tunneling. Therefore, the device known as a quantum phase-slip junction is expected to be as significant and fundamental as the Josephson junction in superconductors. Josephson junctions in general, have several applications in millimeter wave detection, the voltage standard, digital circuits and also qubits. The aim of this thesis is to demonstrate a SPICE model of a quantum phase-slip junction to aid the search for analogous classical applications in fields of digital and RF circuits. Derivation of a SPICE model of a quantum phase-slip junction using its known compact model, and implementation in JSPICE using C programming language along with implementation in WRSPICE using Verilog-A have been presented in this thesis. This model includes transient operation of the device. Basic I-V curves along with simulation of example circuits of the device are shown to validate the model.

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Table of Contents

List of Figures

List of Tables

List of Abbreviations

Auburn Auburn University

LoA List of Abbreviations

QPSJ Quantum phase-slip junction

JJ Josephson junction

RCSJ Resistively and capacitively shunted junction

RLSJ Resistive and inductive series junction

CAD Computer-aided design

Chapter 1

Introduction

An exciting field of superconductivity has been originated with the observation of abrupt drop of DC resistance to zero of a sample at low temperatures close to absolute zero by Kamerlingh Onnes in 1911[1]. Several metallic elements, compounds and alloys were then observed to undergo phase transformations at a low temperature, which is characteristic of the material and is called the *transition temperature* below which, the characteristics of superconductivity are observed. These characteristics mainly include persistent currents without dissipation and Meissner effect[2, 3].

These properties are altered in sufficiently thin nano-wires where superconductivity is suppressed well below transition temperature. This change in properties is associated with phase-slips, which are observed as resistive tails below transition[4]. The phenomenon of a quantum phase-slip, explained later, has been identified as a dual process to Josephson tunneling based on flux-charge duality [5]. The subject of this thesis is to use this duality to develop a SPICE model in order to assist in the exploration of circuit applications of the superconducting electronic device, quantum phase-slip junction (QPSJ).

In this chapter, we discuss the theoretical background starting from the basics of superconductivity using Ginzburg-Landau theories[6], which will lead to the origin of the idea of a phase-slip. Experiments in the evolution of a quantum phase-slip phenomenon are then briefly discussed. The idea of flux-charge duality explaining relationship between a Josephson tunneling and a quantum phase-slip will then be presented in some detail. The resistively and capacitively shunted junction (RCSJ) model of a Josephson junction (JJ) will be discussed in detail in parallel with the QPSJ to facilitate the explanation of its complementary

model. A basic introduction to some circuit applications of JJs will be examined which in later chapters is further explored in the context of QPSJs.

1.1 Superconductivity

The change in behavior in terms of resistance to electrical current dropping to zero in some materials at low temperatures close to zero is interpreted as a phase-transition as explained by Ginzburg-Landau (GL) theories[6] in the macroscopic sense. This theory is vaild for explanation of several phenomena in superconductors. At the microscopic level, BCS theory[3] explains it as due to the attraction of electrons in the periodic potential fiels due to the crystal of atoms. However, for our purpose in discussing the idea of a phase-slip and in explaining the compact models corresponding to JJs and QPSJs, the GL theory is sufficient.

1.1.1 Macroscopic wave function and phase in superconductors

According to the GL theory, a phase transition takes place in superconducting materials below transition temperature T_C, where it is energetically favorable for electrons to form a condensate, which is highly ordered compared to a normal metal phase. In this phase, the superconducting state is defined by a complex order parameter given by:

$$\Psi(r) = \sqrt{n(r)}e^{i\phi(r)} = \psi(r)e^{i\phi(r)} \tag{1.1}$$

Here, $|\psi(r)|^2 = n(r)$ is the density of the electrons condensed in the superconducting state and ϕ is the position dependent phase factor of the state.

This implies that all the condensed electrons occupy a single quantum state with their phases overlapped making it continuous while in this condensate. It is noteworthy that the phase factor enters the macroscopic wave function. This factor of phase can only have values

modulo 2π and is usually wiped out when averaged over billions of electrons in distinct quantum states in a normal metal phase. But, in a superconductor, this becomes an element which gives rise to detectable macroscopic quantum phenomena. We will see later that this property of superconductors is significant in explaining the behavior of JJs and QPSJs.

1.1.2 Phase-slip in superconductors

In this section, we discuss the origin of a phase-slip in superconductors. By using the above description of a macroscopic wave function, we can calculate the current density of the dissipation-less currents induced in a superconductor by assuming an induced supercurrent due to an applied magnetic potential (external magnetic field) with the help of time dependent Schrodinger equation. This simple calculation will facilitate the explanation of the origin of a phase-slip due to Josephson tunneling or a quantum fluctuations, which are responsible for quantum phase-slips that will be discussed in detail in later sections. Details of calculations are not shown and only a simple description of the flow of calculation is given below[7].

Let us consider motion of a particle in the presence of a magnetic potential. In our example, the particle is moving in a superconductor. Therefore, the momentum of particles in the superconducting state described by equation 1.1 in case of magnetic potential is given by:

$$\bar{p} = -i\hbar\nabla - eA(r) \tag{1.2}$$

Here, $\bar{p}$ is the momentum operator of the particle, $\hbar$ is the reduced planck's constant, ∇ is the divergence operator and A is the magnetic vector potential.

The behavior in the presence of magnetic potential is considered only for illustrating supercurrent flow in an example that follows. In practice, a supercurrent can be setup using either an electric or a magnetic field.

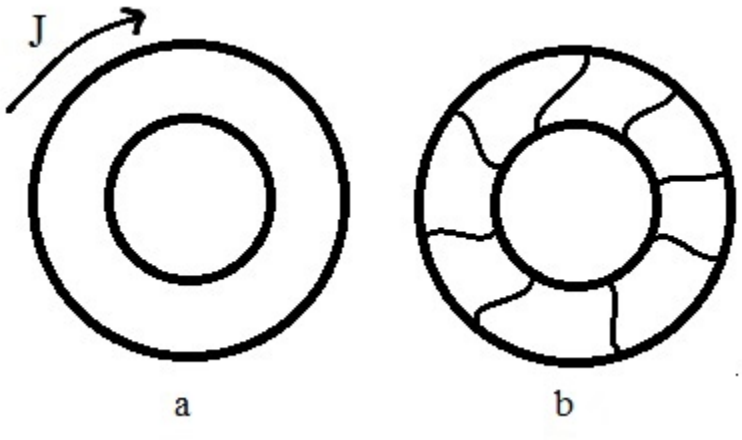

Figure 1.1: a. Persistent current in a superconducting ring. b. Phase of macroscopic wave function around the ring.

Now, let us imagine that we setup a supercurrent in a closed ring shown in the figure 1.1 using an external magnetic field and then turning it down. We see that a persistent current is setup in the ring, which will take infinite time to decay. Using both equations 1.1 and 1.2, the supercurrent can be calculated as shown in equation 1.3:

$$j(r) = \frac{e}{2m} \langle \psi(r) | \bar{p} | \psi(r) \rangle \tag{1.3}$$

$j(r)$ is the current density as a function of position and m is the mass of the electron.

Substituting equation 1.2 in equation 1.3 gives equation 1.4:

$$j(r) = \frac{e}{2m} |\psi(r)|^2 |\nabla\phi(r) - eA(r)| \tag{1.4}$$

In the presence of a magnetic field, $\phi(r)$ is constant and therefore $\nabla\phi(r)$ is zero. Current is only a function of magnetic field in the loop shown in figure 1.1a. But when the magnetic field is turned off, supercurrent persists in the loop without dissipation unless significant changes to the environment are made. In this situation, the supercurrent is a function of $\nabla\phi(r)$, which now cannot be zero and must have a constant value. $\phi(r)$ has values modulo

2π which means $2\pi \pm k$ is equivalent to k. Therefore, in this case of a loop, we can write:

$$\int \nabla\phi(r)dl = 2\pi n \tag{1.5}$$

where n is the winding number.

This is the constant value that is directly proportional to the supercurrent in the loop. The number n is called the winding number of the loop and is illustrated in the figure 1.1b as the number of times the phase of the wave function goes over 2π. This example has been of a superconducting loop but this equation is valid for any continuous superconductor.

Now, the persistent supercurrent without decay is the result of constant winding number as shown in equations 1.4 and 1.5. When the superconducting order parameter is zero at a point in the loop, winding number changes to $n \pm 1$ and this is called as a phase-slip.

Phase-slips are therefore identified as events in the superconductor where the order parameter goes to zero and the winding number changes. This also causes a voltage to develop across the phase-slip region. These events causing suppression of superconductivity in this way are observed in different situations. Some examples include: phase diffusion through thermal fluctuations in JJs, when their Josephson energy is in the regime $E_J \gg e^2/2C_J$ shown in [8]; macroscopic quantum tunneling in JJs whose capacitive energy is much larger than Josephson energy[9], $E_J \ll e^2/2C_J$; thermally activated phase-slips in superconducting nano-wires whose theory is described in [10, 11, 12] and observed in experiments just below critical temperatures in superconducting nano-wires [13, 14]; along with quantum phase-slips due to quantum tunneling of superconducting order parameter between the states whose phases differ by 2π, experimentally observed in [4, 15, 16, 17, 18, 19, 20, 21, 22]. In this thesis, we are mainly interested in quantum phase-slips and the SPICE model that primarily describes the electronic device based on this phenomenon. The theory describing the physics of this phenomenon leading to the formulation of a compact model of the aforementioned

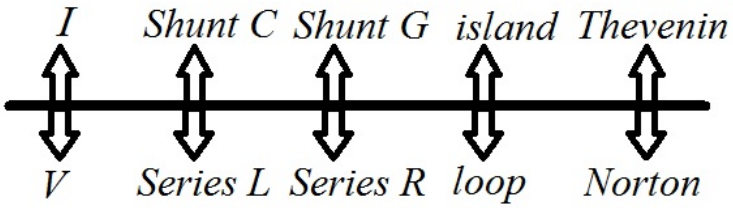

Figure 1.2: Flux-charge duality in electrical circuits (adapted from [29]).

QPSJ device is described in the subsequent sections. Thermally activated phase-slips based on LAMH[10, 11, 12] are also briefly explained as they are relevant in a part of the model.

1.2 Flux-charge duality and quantum phase-slips

Quantum phase-slip phenomenon can be described as a dual phenomenon to Josephson tunneling based on flux-charge duality of maxwell equations, originally described by mooij and co-workers [5]. Later on, this has been extended to define the QPSJ as a dual device to Josephson junction. In the following sub-section, the idea of flux-charge duality in Maxwell's equations, in the context of superconductors will be discussed.

1.2.1 Flux-charge duality

Classical flux-charge duality based on Maxwell's equations can be observed in lumped element circuits as shown in figure 1.2. In continuous case, superconductors and insulators can be shown to be the exact duals of each other, based on charge-flux duality [23, 24, 25, 26, 27, 28]. The quantities charge and flux current densities can be interpreted as sum of bound and free quantities based on Maxwell equations as shown below [29]:

$$J_Q = \rho_Q v_Q + \frac{dD}{dt} \tag{1.6}$$

$$J_\phi = v_\phi \times B_f - \frac{dA}{dt} \tag{1.7}$$

where, J_Q is the current density corresponding to charge, ρ_Q is the charge density moving at velocity v_Q, D is the electric displacement, J_ϕ is the current density corresponding to flux, B_f is the magnetic flux density moving at velocity v_ϕ and A is the vector potential and can be defined in case of superconductors using equation 1.8:

$$A = \wedge \rho_Q v_Q \tag{1.8}$$

where,

$$\wedge = \mu_0 \lambda^2 \tag{1.9}$$

Here, μ_0 is the magnetic permeability and λ is the magnetic penetration depth in superconductors.

Using the equations 1.8 and 1.9 along with $D = \epsilon E$, we can define charge and flux transport in case of superconductors using equations 1.10 and 1.11 respectively [29].

$$\wedge \frac{dJ}{dt} = E \rightarrow L_k \frac{d^2Q}{dt^2} = V \tag{1.10}$$

$$\epsilon \frac{dE}{dt} = J \rightarrow C \frac{d^2\Phi}{dt^2} = I \tag{1.11}$$

Here, L_k is called the kinetic inductance and C is the kinetic capacitance.

These quantities will be encountered in the context of JJs and QPSJs. These equations take the duality between charge and flux to illustrate the dual relation in charge/flux transport in superconductors/insulators.

1.2.2 Josephson junctions and quantum phase-slip junctions

A QPSJ, which is an exact dual to a Josephson junction can now be introduced and defined based on the theoretical description so far. Consider the figure 1.3. A JJ, shown in

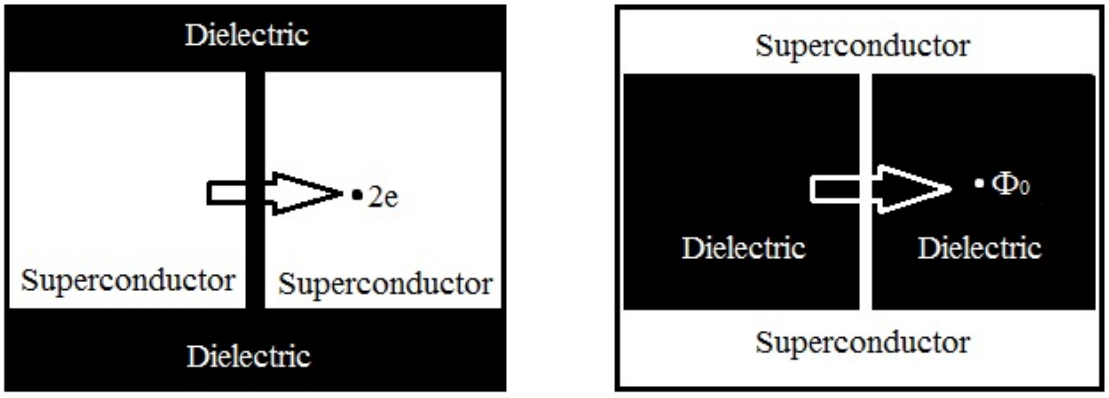

Figure 1.3: Duality between Josephson tunneling in JJs and Fluxon tunneling in QPSJs.

the left, consists of two superconducting islands of cooper pairs separated by an insulating potential barrier, while a QPSJ, shown in right, can be viewed as two insulating *islands* of flux-quanta (referred to as *fluxons* [29]) separated by a superconducting potential barrier. Therefore, the suppression of superconductivity, discussed earlier, associated with a quantum phase-slip is due to tunneling of fluxons across a superconducting nano-wire. The idea of charge-flux duality is not just a classical concept, but the variables-charge and flux, also obey commutation relations when treated as quantum operators.

The behavior of josephson junction depends mainly on the phase difference between the two superconducting electrodes which are seperated by an insulating potential barrier. The tunneling of charges between them is a coherent process, and the current through the junctions is a function of phase difference between these electrodes. Similarly, the tunneling of a fluxon across the superconducting potential barrier sets up voltage between the ends of nano-wire which is a function of charge travelling through the wire. This tunneling of fluxons is also a coherent process. But dissipation occurs in both JJs and QPSJs causing this an incoherent process which will be discussed in detail in later sections.

1.3 Quantum phase-slip junctions

QPSJs are therefore formed from superconducting nano-wires, linking two superconducting electrodes in dielectric region. They show suppression of superconductivity, resulting in dissipation and voltage drop across the nano-wire associated with a phase difference of 2π between the ends of the nano-wire, below the transition temperature. In experiments, these are observed as resistive tails below superconducting transition [30, 31, 18, 20, 32] similar to thermally activated LAMH phase-slips [10, 11, 12, 13, 14]. Josephson tunneling, however is a coherent process without dissipation. Therefore, the Quantum phase-slip which is described by a dual process is also coherent, and has been identified [15, 33] with experimental setups similar to the approach described in section 1.1.2. Using its quantum nature, a quantum phase-slip based qubit has also been proposed [34] which is dual to the charge qubit using Josephson junctions [35]. Nevertheless, we are interested in using QPSJ device in SPICE for use with classical circuits similar to JJs and therefore, will consider the incoherent process where dissipation can be measured. This involves usage of the model for QPSJ similar to RCSJ based device model for a JJ[36]. This model includes parameters to account for dissipation, along with the inductance of the nano-wire, similar to the capacitance in JJ along with the voltage term depicting the coherent quantum phase-slip. A short description of the RCSJ model of a Josephson junction will be explained to facilitate the derivation of QPSJ device model.

1.3.1 Josephson junction and RCSJ model

In this section, we explain and briefly derive the equations governing supercurrent, voltage and phase in DC Josephson effect. Later on, the canonical transformation based on commutation relation between q and ϕ will be used to obtain a model for the QPSJ from the JJ equations [36]. As explained earlier, equation 1.1 defines the charge carriers in superconducting state and can be used to describe either side of the superconducting regions of insulating barrier in a JJ (see figure 1.3). Let us consider the case where voltage

V is applied between the two superconductors. Then the energy and wave function of both superconductor regions are eV, ψ_1 and $-eV$, ψ_2 respectively. We can write time-dependent Schrodinger equation on either side of the superconductor as given by equations 1.12 and 1.13 below:

$$i\hbar\frac{d\psi_1}{dt} = eV\psi_1 + k\psi_2 \tag{1.12}$$

$$i\hbar\frac{d\psi_2}{dt} = -eV\psi_2 + k\psi_1 \tag{1.13}$$

where ϕ is the phase difference across the junction.

Substituting equation 1.1 in the above equations and seperating it into real and imaginary parts gives the result:

$$\frac{d\phi}{dt} = \frac{2e}{\hbar}V \tag{1.14}$$

for the imaginary part, and

$$I = I_C sin\phi \tag{1.15}$$

for the difference of real parts. I_C is the critical current of a JJ. It is the maximum supercurrent that can be carried across the junction.

Equations 1.14 and 1.15 define DC Josephson effect at the device level.

The JJ used in circuits does not behave completely like the equation 1.15 describes. It has dissipation and therefore deviation from completely coherent behavior as described by equations 1.14 and 1.15. The description which includes this behavior of a JJ is called RCSJ model. Resistively and Capacitively shunted junction (RCSJ) model of a JJ takes into

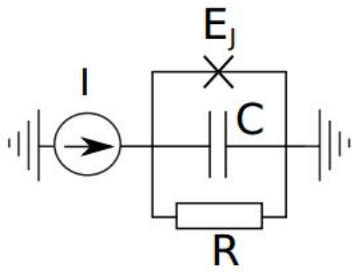

Figure 1.4: Current biased Josephson junction with Resistor and Capacitor in parallel (RCSJ model).

consideration, the junction's intrinsic resistance and capacitance. The current biased junction shown in figure 1.4 represents an equivalent circuit model. When the current applied is above the critical current of the junction, the additional current passes through the elements R and C of the junction. Total current is hence given by:

$$I = I_J + I_R + I_{Cap} \tag{1.16}$$

which gives:

$$I = I_C sin\phi + \frac{V}{R} + C\frac{dV}{dt} \tag{1.17}$$

1.3.2 Charge transport in a quantum phase-slip

A very useful explanation of charge transport in JJs can be derived from RCSJ model. By replacing V in equation 1.17 with its substitute from equation 1.14, we can get a description of JJ in terms of a second order equation in phase. An energy versus phase plot with this description of the model is called as washboard potential shown in the figure 1.5. The slope in the plot is due to the applied bias current. In a JJ, the charge carrier oscillates in a potential well, giving rise to sinusoidal current description given by equation 1.15. But with enough bias current, the height of the potential well is decreased and the charge carrier rolls off to lower potential wells, losing energy due to dissipation. Under low bias current, the

charge carrier can still travel into next potential well through a process called phase diffusion [8], where thermal activation is responsible for the particles to cross the energy barrier.

In highly capacitive Josephson junctions, another possible way exists for charge carriers to transport via tunneling through the potential barrier between potential wells which are stimulated by zero-point fluctuations. These fluctuations are caused due to the energy oscillations between kinetic inductance (see equation 1.10) and junction capacitance. This phenomenon is called as macroscopic quantum tunneling [9].

In superconducting nano-wires, the thermally activated phase-slips can be described by a similar process to that of phase diffusion but at a different enery scale proposed by LAMH [10, 11, 12]. These phase-slips are observed as resistive tails below superconducting transitions in nano-wires, where the value of resistance is given as a function of potential barrier (figure 1.5), which is further defined as proportional to the energy needed to destroy superconductivity, as shown in the following equations.

$$R(T) \propto e^{-U/T} \tag{1.18}$$

$$U \approx \frac{\nu {\Delta_0}^2(T)}{2} S\xi(T) \tag{1.19}$$

where, Δ_0 is the superconducting energy gap , ν represents density of states and ξ is the cross-section of the wire and coherence length at a given temperature T.

Quantum phase-slips follow a similar process as that of macroscopic quantum tunneling but at a different energy scale derived in detail in [29]. The zero-point fluctuations arise as a result of oscillations between inductance of the nano-wire and kinetic capacitance (see equation 1.11). The dissipation in a quantum phase-slip process which allows the charge carrier to settle in lower-energy potential well arises due to the dielectric constant of the conducting material, which acts as an effective mass for the fluxon tunneling across the

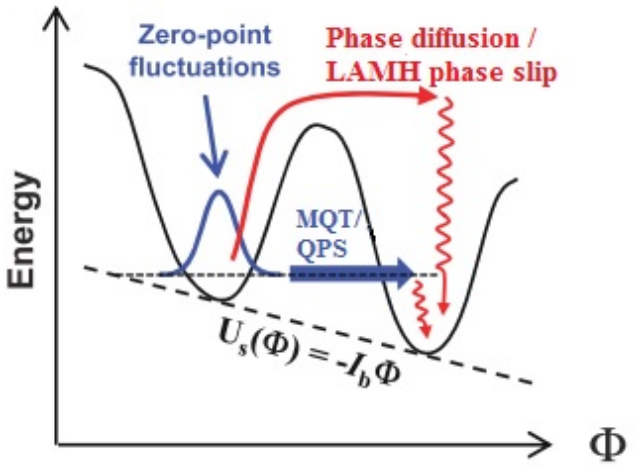

Figure 1.5: Washboard potential description of Phase diffusion/LAMH phase-slip (shown in red) and Macroscopic quantum tunneling/Quantum phase slip (shown in blue) [29].

nano-wire. Therefore, the resistance term that will be shown in resistive and inductive series junction (RLSJ) model of a QPSJ in next sectionl corresponds to the loss due to dielectric for the electric field (or voltage drop) along the nano-wire due to the fluxon tunneling across the wire. This microscopic description manifests as lumped element model in the next section derived from the dual model to JJ which will be ready to implement in a SPICE model.

1.3.3 Resistive and inductive Series junction model of a quantum phase-slip junction

As we have already seen, phase-slips are observed when superconductivity is suppressed and a quantum phase-slip phenomenon can be explained as a dual to Josephson tunneling. Mooij and Nazarov are the first to realize that a quantum phase-slip process can be described by the charge-flux duality using quantum conjugates q and ϕ [5]. Charge and phase quantum operators satisfy the commutation relation:

$$[\hat{q}, \hat{\phi}] = -i \tag{1.20}$$

where q is the electric charge and ϕ is the magnetic flux.

They also proposed a phase-slip energy dual to the Josephson energy which was later derived by [29]. In description given by Mooij and Nazarov in [5], they performed canonical transformation, which satisfies the commutation relations between the resulting expressions, to the Josephson hamiltonian to arrive at a qualitative description of a coherent quantum phase-slip. The details are not discussed here, but the canonical transformations performed are given below.

$$(\hat{q}, \hat{\phi}) \rightarrow (-\hat{\phi}/2\pi, 2\pi\hat{q}) \tag{1.21}$$

$$E_s \rightarrow E_J; E_L \rightarrow E_C; I \leftrightarrow {R_q}^{-1}V; Y(\omega) \leftrightarrow {R_q}^{-1}Z(\omega) \tag{1.22}$$

where E_s is the phase-slip energy, E_J is the Josephson potential energy, E_L and E_C are the inductive and capacitive energies of a QPSJ and a JJ respectively.

Using the above equations, we can perform canonical transformation of equation 1.15 to obtain

$$V = V_C sin(2\pi q) \tag{1.23}$$

with V_C being the critical voltage of the junction and V, the measurable voltage drop across the junction.

The compact model describing the dissipation and inductance of the wire [5, 16] is shown in the figure 1.6. Notice that this is a series circuit as opposed to JJ's parallel circuit which is a result of canonical transformation.

The capacitance and resistance terms from the equation 1.17 transform into the following equations.

$$\frac{V}{R} \rightarrow IR, C\frac{dV}{dt} \rightarrow L\frac{dI}{dt} \tag{1.24}$$

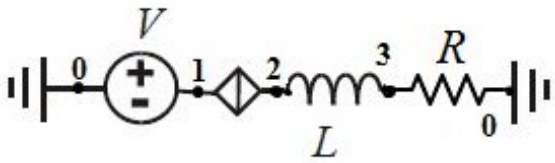

Figure 1.6: Voltage biased QPSJ in RLSJ model

The I-V description of a lumped element model of a QPSJ defined by RLSJ model is therefore given by:

$$V = V_C sin(2\pi q) + L\frac{dI}{dt} + RI \tag{1.25}$$

Equation 1.25 has been used to develop a SPICE model for a QPSJ with additional modifications to incorporate transition between normal and superconducting states, thermally activcated phase slips etc. explained in detail in coming chapters.

1.3.4 Lumped-element superconducting circuits using QPSJs

Apart from flux-qubit mentioned earlier, there can be several circuit applications of QPSJs in RSFQ and quantum circuits. Present-day JJ-based qubits are limited by high-frequency charge noise, which can be replaced by QPSJs [29], whose flux-noise is expected to be much lower. Phase-slip oscillators are proposed [37] along with other circuit applications like charge based memory device [29], single-charge transistor [17] along with quantum phase-slip transistor [16] and some other applications [38, 39]. With the implementation of a SPICE model, there is a possibility to explore many other circuit applications.

Chapter 2

Compact model implementation in SPICE

Circuit simulations are key to design, validate and optimize the circuit for required applications. The development of CAD tools and design methodologies is a major research specialty in the field of semiconductor integrated circuits. But in superconducting digital electroncis, CAD is far less advanced [40]. The development of RSFQ technology has also been limited by the available design tools. [40] compares all the available CAD tools for superconducting electronics. In this work, JSPICE and WRSPICE were used as a platform to develop and implement a SPICE model for the quantum phase-slip junction, which is a dual component to a Josephson junction.

The schematic developed in either graphical or text form in a SPICE simulation environment, is converted to a system of linear or non-linear differential equations based on nodal analysis and the software uses numerical models of these systems of equations to solve them according to specified analysis. These differential equations are effectively the resultant of all the individual components in the circuit. Therefore, each individual component in the circuit simulation software is described by a set of linear or non-linear differential equations called the *compact model* of the circuit. The coefficients of these set of equations are known as model parameters.

A compact model is obtained for every analysis of the component (i.e. transient, DC, AC, temperature etc.) and then represented in a form ready for circuit solutions in SPICE. The purpose of this chapter is to demonstrate the way to prepare or derive a model ready for SPICE to incorporate this device into circuits and solve its equations in the circuit setup. Therefore, this chapter deals with the circuit solutions and numerical analyses usually followed to reach a point where the the tool can understand and implement the device along

with other circuit components under all conditions will be discussed, without considering the details of software tools or programming.

2.1 Modified nodal analysis

Modified nodal analysis (MNA), as the name suggests, deals with improved nodal analysis, suitable for all the cases that will be seen in describing complicated device equations using traditional circuit analysis techniques [41]. In subsequent sections, circuit examples will be used to illustrate the solution methods that are used by a software tool in solving electrical circuits.

2.1.1 Nodal analysis

There are two general approaches for analysis of linear circuits: mesh analysis and nodal analysis. Mesh analysis is generally limited to planar circuits and unique equations can be written for meshes in the circuit described by Kirchoff's voltage law. The unknowns can then be solved from the obtained set of equations. It is difficult for a computer to solve a circuit using mesh analysis when the circuits become complicated and tend to be non-planar. In contrast, nodal analysis has a unique set of corresponding equations, formed using Kirchoff's current law, whether the circuit is planar or not and therefore is easier to implement in computers.

Nodal analysis is based on nodes of the circuit, where the sum of currents incident at that node is zero. We therefore form a current equation at each node and then solve for the unknowns. Using Ohm's law and Kirchoff's current law, the set of equations formed by nodal analysis of a circuit can be represented in matrix form given by equation 2.1.

$$[Y][V] = [I] \tag{2.1}$$

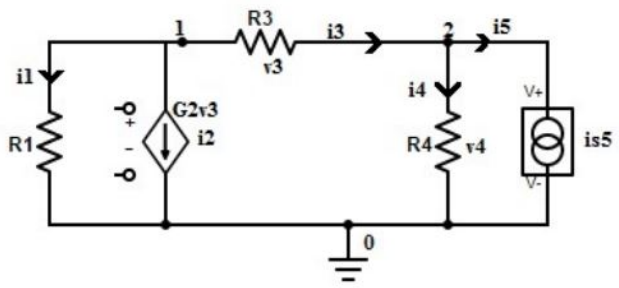

Figure 2.1: Example circuit to show element stamping using nodal analysis.

$[Y]$ matrix and $[I]$ vector are formed immediately from nodal equations and then solved for $[V]$.

2.1.2 Element stamping

The easiest way to form the matrix with nodal equations in a computer is through element stamping. An element stamp which is a matrix $[Y]$ corresponding to that device alone, is defined for each component available in the SPICE tool. It also has an RHS vector $[I]$ if the device is non-linear. This matrix in this stamp has an order which is same as or smaller than the order of the matrix of the entire circuit, and the matrix element of this stamp occupy appropriate positions, corresponding to their nodes, in the larger matrix describing the entire circuit. An example of a simple circuit is shown in the figure 2.1.

We use this circuit to show nodal analysis and element stamping of resistor R3 in the circuit. Let us write the Kirchoff's current law (KCL) equations for nodes 1 and 2.

$$i1 + i2 + i3 = 0 \rightarrow node1 \tag{2.2}$$

$$-i3 + i4 - i5 = 0 \rightarrow node2 \tag{2.3}$$

Substituting branch equations to rewrite KCL in branch voltages:

$$\frac{1}{R1}v1 + G2v3 + \frac{1}{R3}v3 = 0 \tag{2.4}$$

$$\frac{-1}{R3}v3 + \frac{1}{R4}v4 = is5 \tag{2.5}$$

Substitute branch voltages by nodal voltages (using Kirchoff's voltage law (KVL)):

$$\frac{1}{R1}e1 + G2(e1 - e2) + \frac{1}{R3}(e1 - e2) = 0 \tag{2.6}$$

$$\frac{-1}{R3}(e1 - e2) + \frac{1}{R4}e2 = is5 \tag{2.7}$$

By representing it in matrix form given by equation 2.1:

$$\begin{bmatrix} \frac{1}{R1} + G2 + \frac{1}{R3} & -G2 - \frac{1}{R3} \\ -\frac{1}{R3} & \frac{1}{R4} + \frac{1}{R3} \end{bmatrix} \begin{bmatrix} e1 \\ e2 \end{bmatrix} = \begin{bmatrix} 0 \\ is5 \end{bmatrix} \tag{2.8}$$

In the above matrix equation, notice that each element contributes its conductance only to entries with row-column positions corresponding to its node numbers. Consider element $R3$. Its contribution to the matrix is written below:

$$\begin{bmatrix} \frac{1}{R3} & -\frac{1}{R3} \\ -\frac{1}{R3} & \frac{1}{R3} \end{bmatrix} \tag{2.9}$$

This matrix is called as element stamp of resistor $R3$. Every resistor in general, can be expressed in the exact same form as the above stamp. Some elements have an RHS vector along with the matrix, particularly when dealing with non-linear devices or when analyses

other than DC. Therefore, the nodal analysis equation can be rewritten as:

$$[I] = [Y][V] + [RHS] \tag{2.10}$$

A capacitor has an element stamp given by:

$$\begin{bmatrix} G_n & -G_n \\ -G_n & G_n \end{bmatrix} \tag{2.11}$$

with RHS vector:

$$\begin{bmatrix} I_{eq} \\ -I_{eq} \end{bmatrix} \tag{2.12}$$

Here, G_n is the effective conductance of the device, which can have different values when the device is operated in different modes and I_{eq} is the corresponding current through the device. Each device is described as a resistance or conductance at that instant, with effective values described as done in the case of a capacitor. This will be explained in more examples later.

All the elements in the circuit is described by its stamp, and combining all the stamps according to their respective node positions, give the circuit matrix which will then be solved by the SPICE tool for respective node voltages or currents. This technique is valid for DC, AC, transient, temperature, noise etc. analyses that are available in the software tool. However, some devices have different set of element stamps for each of these analyses, which will be discussed in detail in the next section.

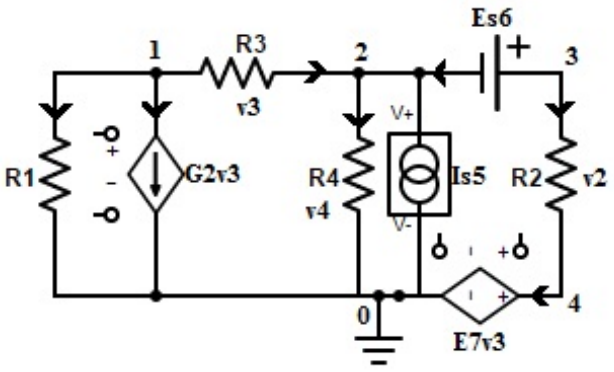

Figure 2.2: Example showing MNA stamp for a voltage source.

2.1.3 Modified nodal analysis

We have seen that nodal analysis is a simple method to obtain the element stamp which can be implemented in SPICE models. But every device cannot be described by using branch equations to get to a set of equations of type 2.1 or 2.10. Some of the examples of this case are voltage sources and inductors. Nodal analysis therefore, leads to a complicated representation of the device equations, which often are very difficult to implement in a computer.

Modified nodal analysis (MNA) [42] is a better approach to handle these situations and is implemented in many CAD tools for circuit simulation [41]. In this method, we add the aforementioned unused branch equations (with voltage sources, inductors etc.) to new row in the matrix as additional equations in the form:

$$[V] = [R][I] \tag{2.13}$$

instead of the form in equation 2.1. An example with voltage sources in the circuit is shown in figure 2.2 to illustrate this concept.

This example has a voltage source and a voltage controlled voltage source, two of the devices for which, nodal analysis is not suitable to derive an element stamp. MNA stamps

for these devices are obtained by using similar analyses as before with additional equations in the matrix. The solution is shown below.

First step is to write Kirchoff's current law equations:

$$i1 + i2 + i3 = 0 \tag{2.14}$$

$$-i3 + i4 - i5 - i6 = 0 \tag{2.15}$$

$$i6 + i8 = 0 \tag{2.16}$$

$$i7 - i8 = 0 \tag{2.17}$$

Using branch equations to eliminate as many branch currents are possible:

$$\frac{1}{R1}v1 + G2V3 + \frac{1}{R3}v3 = 0 \tag{2.18}$$

$$\frac{-1}{R3}v3 + \frac{1}{R4}v4 - i6 = is5 \tag{2.19}$$

$$i6 + \frac{1}{R2}v2 = 0 \tag{2.20}$$

$$i7 - \frac{1}{R2}v2 = 0 \tag{2.21}$$

Now, writing down unused branch equations corresponding to voltage sources:

$$v6 = ES6 \tag{2.22}$$

$$v7 - E7v3 = 0 \tag{2.23}$$

Using Kirchoff's voltage law to eliminate branch voltages from previous equations:

$$\frac{1}{R1}e1 + G2(e1 - e2) + \frac{1}{R3}(e1 - e2) \tag{2.24}$$

$$\frac{-1}{R3}(e1 - e2) + \frac{1}{R4}e2 - i6 = is5 \tag{2.25}$$

$$i6 + \frac{1}{R2}(e3 - e4) = 0 \tag{2.26}$$

$$i7 - \frac{1}{R2}(e3 - e4) = 0 \tag{2.27}$$

$$(e3 - e2) = ES6 \tag{2.28}$$

$$e4 - E7(e1 - e2) = 0 \tag{2.29}$$

All the above equations can be written in matrix equation form to obtain the solution:

$$\begin{bmatrix} \frac{1}{R1} + G2 + \frac{1}{R3} & 0 & 0 & 0 & 0 & \\ \frac{-1}{R3} & \frac{1}{R3} + \frac{1}{R4} & 0 & 0 & -1 & 0 \\ 0 & 0 & \frac{1}{R2} & \frac{-1}{R2} & 1 & 0 \\ 0 & 0 & \frac{-1}{R2} & \frac{1}{R2} & 0 & 1 \\ 0 & -1 & 1 & 0 & 0 & 0 \\ E7 & -E7 & 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} e1 \\ e2 \\ e3 \\ e4 \\ i6 \\ i7 \end{bmatrix} = \begin{bmatrix} 0 \\ is5 \\ 0 \\ 0 \\ ES6 \\ 0 \end{bmatrix} \tag{2.30}$$

The last two colums and rows of the matrix along with last two rows of both left hand side and right hand side vectors of the above equation are the equations added to represent voltage sources in the form of equation 2.13. The element stamp for a voltage source will therefore be:

$$\begin{bmatrix} -- & -- & 1 \\ -- & -- & -1 \\ 1 & -1 & -- \end{bmatrix} \tag{2.31}$$

with RHS vector is:

$$\begin{bmatrix} -- \\ -- \\ V \end{bmatrix} \tag{2.32}$$

where V is the voltage of the voltage source. Similarly, an inductor's element stamp can be obtained which is given below.

The MNA matrix is:

$$\begin{bmatrix} -- & -- & 1 \\ -- & -- & -1 \\ 1 & -1 & -Rn \end{bmatrix} \tag{2.33}$$

with the RHS vector:

$$\begin{bmatrix} -- \\ -- \\ -Veq \end{bmatrix} \tag{2.34}$$

where Rn is the equivalent resistance in a mode of operation and Veq is the equivalent voltage across it. A branch current is introduced as an additional variable with other variables being node voltages, for every device that cannot be worked out using nodal analysis.

2.2 Dynamic element stamping

In all the examples that we have seen so far, we have only considered static elements like voltage sources and resistors. We have however, looked at element stamps of inductors

and capacitors, which are dynamic elements in time. In this section, we will see how to numerically analyze dynamic, linear and non-linear devices to be able to write in a form that a computer can solve, along with other devices in the circuit.

2.2.1 Linear devices and trapezoidal rule

Inductors and capacitors are the most common examples of linear dynamic devices. But other devices might exist like an ideal quantum phase-slip, which will be used in the context of QPSJ etc. Unlike resistors, these dynamic devices behave differently in different modes of operation. In this thesis, we are mainly interested in transient mode operation of the device. But other available operations are also briefly discussed.

Numerical analysis of a linear differential equation can be done using several methods. But the most popular ones suitable in a computer simulation are Forward Euler, Backward Euler and Trapezoidal methods. Trapezoidal rule has been identified as the most efficient method and is often used in many SPICE programs including the ones we are interested in. A short summary of the trapezoidal rule for solving ordinary differential equations is given below:

$$\dot{y}(t) = \frac{dy(t)}{dt} = f(y(t)) \tag{2.35}$$

The above equation can be written as:

$$\frac{y(t_n) - y(t_{n-1})}{h} \approx \frac{1}{2}\left[\dot{y}(t_n) + \dot{y}(t_{n-1})\right] \tag{2.36}$$

where the right hand side is the averaged tangent at the points n and $n-1$.

From equations 2.35 and 2.36, we can write:

$$\frac{y(t_n) - y(t_{n-1})}{h} \approx \frac{1}{2}[f(y(t_n)) + f(y(t_{n-1}))] \tag{2.37}$$

$$\tag{2.38}$$

From equation 2.37, we can write:

$$y(t_n) = y(t_{n-1}) + \frac{h}{2}[f(y(t_n)) + f(y(t_{n-1}))] \tag{2.39}$$

Equation 2.39 is the final equation which is used to solve the device equations as a function of time. Initial conditions of a dynamic element in the circuit are either provided by the user or, default initial conditions are assumed to obtain solution at $n = 1$ or time $t = 0$. Then the solution continues till the end time specified by the user. The MNA stamp of a capacitor is derived with the RHS vector below for transient analysis.

Figure 2.3 shows a simple schematic of a capacitor under transient analysis. It can be represented by the equation 2.40, which can be numerically solved using trapezoidal rule given by equations 2.41 and 2.42.

$$i(t) = C\frac{dv(t)}{dt} \tag{2.40}$$

$$V_t = V_{t-1} + \frac{h}{2}[\dot{v}(t) + \dot{v}(t-1)] \tag{2.41}$$

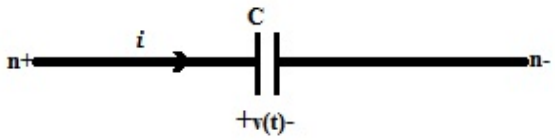

Figure 2.3: Capacitor MNA stamp for transient analysis.

$$i(t) = C\frac{dv(t)}{dt} \approx C\left[-\dot{v}(t-1) + \frac{2}{d}(V_t - V_{t-1})\right] \tag{2.42}$$

which is of the form:

$$I = G_n V + RHS \tag{2.43}$$

From these equations, a MNA stamp based on an examples shown in previous section, is given by:

$$\begin{bmatrix} \frac{2C}{h} & -\frac{2C}{h} \\ -\frac{2C}{h} & \frac{2C}{h} \end{bmatrix} \tag{2.44}$$

with RHS vector:

$$\begin{bmatrix} C(\dot{v}(t-1) + \frac{2V_{t-1}}{d}) \\ C(\dot{v}(t-1) + \frac{2V_{t-1}}{d}) \end{bmatrix} \tag{2.45}$$

In the next chapter, this method will be used to derive a part of MNA stamp of a QPSJ, where the inductor will also be discussed.

2.3 Non-linear devices and Newton-Raphson method

2.3.1 Numerical solutions of circuits using Newton-Raphson method

We have seen linear static and linear dynamic devices and their corresponding numerical analyses in SPICE softwares. But almost all the interesting circuits that require modeling and computer simulation involve non-linear devices. The solution of a circuit with these devices require numerically solving a non-linear I-V equation for a solution which takes several iterations. A common example of non-linear devices is a diode. A non-linear equation is used to describe the I-V relation of a diode given by equation 2.46. Newton-Raphson method is the most common method implemented in SPICE softwares and is explained in this section using the diode example.

$$I = I_S exp(\frac{V_1}{v_t}) \tag{2.46}$$

where, I is the diode current,

$$f(x) = 0 \tag{2.47}$$

Before going into the solution of a circuit with a diode, let us look at the overview of Newton-Raphson method for solving non-linear equations [43]. Figure 2.4 below shows a non-linear curve, given by equation 2.47 with a root at r. Here, the assumption is that $f'(r) \neq 0$. Now let us choose a number x_1, which serves as our initial condition for the first iteration in solving for equation 2.47. The tangent line to the graph of $f(x)$ at the point $(x_1, f(x_1))$ has x-intercept x_2, which is closer to the root r. This calculation is given by equation 2.48.

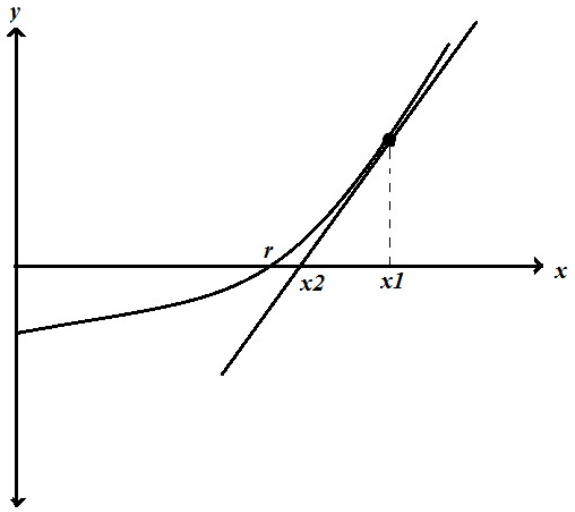

Figure 2.4: Graphical representation of Newton-Raphson method for numerically solving non-linear equations.

$$x_2 = x_1 - \frac{f(x_1)}{f'(x_1)} \tag{2.48}$$

Because of the assumption that $f'(r) \neq 0$, we will not have problem with the denominator being equal to zero. This process is iterated with x_2 as the new value at which a tangent is drawn to obtain an even closer solution to r, which is x_3 and so on till a very close number to r is reached, which is then treated as the solution to the equation 2.47. The equation to represent Newton-Raphson method is therefore given by equation 2.49 below.

$$x_{n+1} = x_n - \frac{f(x_n)}{f'(x_n)} \tag{2.49}$$

Now consider the circuit with a diode shown in the figure 2.5. Using equation 2.46, Kirchhoff's voltage law at node V_1 gives equation 2.50.

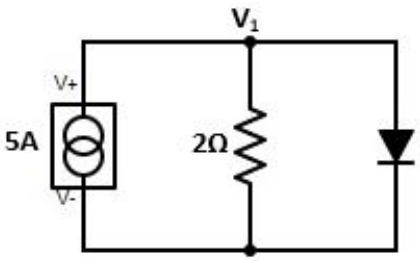

Figure 2.5: Example circuit with a diode for demonstrating Newton-Raphson method.

$$-5 + \frac{V_1}{2} + I_S exp \frac{V_1}{v_t} = 0 \tag{2.50}$$

Applying Newton-Raphson method to solve this equation gives:

$$V_{1_{n+1}} = V_{1_n} - \frac{5 - I_S exp\left(\frac{V_{1n}}{V_t}\right) - 0.5V_{1_n}}{-I_S V_{1_n} exp\left(\frac{V_{1n}}{V_t}\right) - 0.5} \tag{2.51}$$

Coefficients of V_{1_n} can be written as Geq in the MNA matrix of the diode and the remaining terms can be included in the RHS vector. A detailed model of a diode is not provided here. But element stamps for non-linear devices will be derived in this way in the next section while solving for MNA representation of the QPSJ compact model.

2.3.2 Simulation convergence and convergence aids

Newton-Raphson method is the popular method in SPICE tools for circuit simulations, but it can often run into some problems. This algorithm often fails to find a solution when the iteration sequence does not converge. In this method, we only choose one initial guess to start the iteration process to reach the right solution, unlike many methods, where two initial guesses are required where the method determines if the solution lies in between those

two guesses or outside. So in this method, if the initial guess is not appropriately chosen, the iteration process fails to converge, leading to each iteration going further and further away from the root of the equation. SPICE offers some adjustment parameters that can be set by the user, to determine the tolerances for detecting and aborting non-converging iterative processes. In addition, specific models are also modified to obtain better convergence or avoid frequent non-convergence problems. These are discussed in following chapters.

Chapter 3

Compact model and MNA analysis of a quantum phase-slip junction

Overview of the theory of a Quantum phase-slip junction from basic principles to the derivation of a compact model has been presented in chapter 1. In the SPICE model that we implemented in WRSPICE, some small modifications were made to the original compact model given in the equation 1.25 to accomodate operation of the device in normal state of operation above transition, and also the operation of the device in thermal phase-slip region with some assumptions. Below transition, the device behaves as an ideal QPSJ below critical voltage of the device. The compact model and the equation derived in chapter 1 are provided here again with modifications to the model.

$$V = V_C sin(\frac{2\pi q}{2e}) + L\frac{dI}{dt} + R(V)I \tag{3.1}$$

The origin of the voltage drop across a nano-wire along with the geometric inductance and resistance corresponding to dissipation in the device are discussed in the device. But this model is generic and is valid to simulate any device similar to a QPSJ with inductance and resistance values not necessarily corresponding to a valid set to experimentally increase the probability of high quantum phase-slip rate. Additionally, the resistance R is shown in

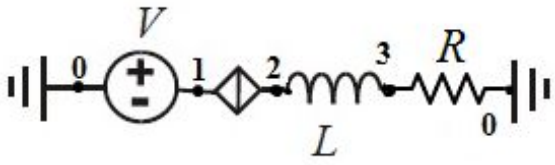

Figure 3.1: Voltage biased QPSJ in RLSJ model.

equation 3.1 as a function of voltage V. It represents a non-linear resistance with its resistance value different in different regions of operation of the device. All the input parameters of the device are discussed below.

3.1 Input parameters of the device

In this section, the input parameters that can be controlled by the user while performing QPSJ simulations are discussed, along with the default values that are assigned to these parameters when the user does not provide values for them.

V_C : From the equation 3.1, we can find that the first term has a parameter V_C, which is the critical voltage of the device. The default value for V_C is $700\mu V$. The range of the values that can be assigned to V_C is from $10\mu V$ to $0.1V$. The range cannot be changed by the user. But it can be modified in the Verilog-A program that will be discussed in the next chapter. Below critical voltage, the device has ideal quantum phase-slip characteristics, along with geometric inductance of the device and a sub-gap resistance that might be caused due to quasi-particles. These parameters can however be set to zero and are discussed later in this section.

The variable name that can be used to vary critical voltage is *vcrit* in all the models that are developed.

Initial charge : In the first term of the equation 3.1, in addition the V_C, the parameter charge (q) exists. q is calculated from the current through the device from previous instant of time in transient analysis and is the total charge that has passed through the junction in time t till that instant. It is given by the equation 3.2 below:

$$q = q_{ic} + \int eI(t)dt \tag{3.2}$$

where $I(t)$ is the current through the junction which is a function of time and e is the charge of an electron, $e = 1.9625 \times 10^{-19}$ Coulombs. A function exists in WRSPICE, which performs numerical integration when equation 3.2 is presented. This is also valid for Verilog-A models. In JSPICE however, a numerical analysis for the integration must be performed manually by defining a time-step and multiplying current at each instant by the time-step (which is the differential element in the integration) to calculate the total charge. q_{ic} is the initial condition charge, that can be assigned by the user to represent a charged device which can aid in convergence. It has a default value of 0 and can take any value.

The variable name for initial condition charge in all the models developed is $ichrg$.

$Inductance$: This is the total inductance of the device as seen in second term of equation 3.1. It can include both the geometrical and kinetic inductance of the device and has a default value of $890nH$. This value is taken from [16].

The variable name for inductance in all the models is ind.

$Sub - gap\ resistance$: As mentioned earlier, the resistance of QPSJ model is divided into three parts. Below transition temperature, QPSJ has a sub-gap resistance, the origin of which can be accounted to any known phenomenon that cause it, like quasi-particle conductance. Its default value is $1 \times 10^9\Omega$.

It has the variable name $rsub$ in all the models.

$Normal\ resistance$: Normal resistance is the resistance of the device above its transition temperature. It has the default value of $1.6 \times 10^6\Omega$.

The variable name used is $rnorm$.

$Drop - back\ current$: Drop-back current is the maximum current through the junction before the superconductor turns normal. Above this current, normal resistance is sec across the device. Its default value is dependent on the inductance and is calculated from the equation 3.3 below:

$$I_{dp} = \sqrt{\frac{L}{1000e}} \tag{3.3}$$

The variable name for drop-back current is *idpback*.

In order to implement a drop-back current to get an effect similar to retrapping in a JJ, the time-step (increment in time after each iteration) of the QPSJ simulation must be limited to $\frac{2}{eI_{dp}}$ for SPICE program to capture this effect.

Transition current : This is an additional parameter used to determine the operation of the device after it goes above critical voltage but before it goes normal. The value of this parameter can be determined to specify if the device is undergoing thermal phase-slips or some other kind of dissipation. It is not designed to represent a particular theory for QPSJ, but can be valid for several theories depending on the choice of the parameters.

It has a default value of $40pA$ and a variable name of *deli*. The resistance of the device during this transition is given by the equation 3.4 below:

$$R = |\frac{1}{\frac{V_C - deli/2}{rsub} - \frac{V_C + deli/2}{rnorm}}| \tag{3.4}$$

3.2 MNA analysis of RLSJ model of a QPSJ

In chapter 2, we have discussed the concept of modified nodal analysis and element stamps. In the next chapter, we will see that once we have a device description in the format of MNA stamp, how we can implement it in programs that are compatible with SPICE softwares. Before that, an MNA stamp must be derived for the QPSJ device based on the compact model shown in figure 3.1 and RLSJ equation given by 3.1.

The QPSJ device is treated as a combination of an inductor, a variable non-linear resistor and an ideal quantum phase-slip in series. Therefore, the resultant MNA stamp of

the device can be obtained from the MNA stamps of these individual devices. The combined MNA matrix is the equivalent conductance sparse matrix as a function of time, which is suitable for transient analysis alone. Let us look at the MNA stamp of each of the devices in the model starting with inductor.

3.2.1 MNA stamp of an inductor

The QPSJ model has a simple inductor without the element of any mutual inductance involved. Therefore, unlike the case of an actual inductor that is used in regular SPICE model, this inductor has a simplified version which can be derived as shown below.

Trapezoidal method shown in the equation 2.39 is used here to obtain the following equation for inductor.

$$L\frac{dI_1}{dt} = L\left(-{I_0}' + \frac{2}{\Delta}(I_1 - I_0)\right) \tag{3.5}$$

Here, Δ is the time step, I_1 is the current in this iteration, I_0 is the current in last iteration, ${I_0}'$ is the derivative of last iteration and L is the inductance.

The term multiplying I_1 in the equation above is $\frac{2L}{\Delta}$, which is the 3×3 element in the MNA matrix and the remaining terms $-L\left({I_0}' + \frac{2I_0}{\Delta}\right)$, which gives the MNA stamp:

$$\begin{bmatrix} -- & -- & 1 \\ -- & -- & -1 \\ 1 & -1 & -\frac{2L}{\Delta} \end{bmatrix} \tag{3.6}$$

and RHS vector:

$$\begin{bmatrix} -- \\ -- \\ -L\left(I_0{}' + \frac{2I_0}{\Delta}\right) \end{bmatrix} \tag{3.7}$$

3.2.2 Non-linear resistor

The next term that will be derived belongs to the non-linear resistor. This is a simple piece-wise linear function with different slopes corresponding to resistances in those regions. Since this is not a linear element, its analysis must be done using the Newton-Raphson method. Instead of resistance, the corresponding conductance is used in the MNA matrix. It has the form, $G(V)$.

Using analysis similar to equation 2.49, we can write:

$$G(V) = G(V_L) + (V - V_L)g \tag{3.8}$$

where, g is the first derivative of the conductance fucntion $G(V)$, V is the voltage across the device of current iteration and V_L is the voltage across the device in last iteration.

The MNA matrix representation of the device is given by:

$$\begin{bmatrix} g & -g \\ -g & g \end{bmatrix} \tag{3.9}$$

with RHS vector given by:

$$\begin{bmatrix} -G(V_L) + gV_L \\ G(V_L) - gV_L \end{bmatrix} \tag{3.10}$$

3.2.3 Quantum phase-slip

This is also a non-linear equation but with slight complication. It has two variables, time and charge. Here, we will make use of the current from previous iteration which relates time and charge.

Quantum phase-slip equation is given by:

$$V(t) = V_C sin\left(\frac{2\pi q}{2e}\right) \tag{3.11}$$

when operated using equation 2.49 gives:

$$V_C sin\left(\frac{2\pi q}{2e}\right) = V_C\left(\frac{2\pi}{2e}\right)(q - q_L) cos\left(\frac{2\pi q}{2e}\right)\frac{dq}{dt} \tag{3.12}$$

$$\frac{dq}{dt} = I_L \tag{3.13}$$

$$\tag{3.14}$$

$$\Rightarrow q = q_L + \frac{\Delta(I + I_L)}{2} \tag{3.15}$$

Therefore,

$$V_C sin\left(\frac{2\pi q}{2e}\right) \succ V_C sin\left(\frac{2\pi q_L}{2e}\right) + V_C\left(\frac{2\pi}{2e}\right)\left(\frac{\Delta(I+I_L)}{2}\right) cos\left(\frac{2\pi q_L}{2e}\right) \tag{3.16}$$

where I_L and q_L are current and charge of previous iteration respectively.

The MNA matrix is therefore given by:

$$\begin{bmatrix} -- & -- & 1 \\ -- & -- & -1 \\ 1 & -1 & V_C\left(\frac{2\pi}{2e}\right)\left(\frac{\Delta}{2}\right) cos\left(\frac{2\pi q_L}{2e}\right) \end{bmatrix} \tag{3.17}$$

and RHS vector is given by:

$$\begin{bmatrix} -- \\ -- \\ V_C\left[sin\left(\frac{2\pi q_L}{2e}\right) + \left(\frac{2\pi}{2e}\right)\left(\frac{\Delta I_L}{2}\right) cos\left(\frac{2\pi q_L}{2e}\right)\right] \end{bmatrix} \tag{3.18}$$

3.2.4 MNA matrix and RHS vector of a QPSJ

All the individual device MNA stamps obtained in the previous three sections can be combined into a single MNA stamp, that can describe the entire QPSJ device. The MNA matrix is given by:

$$\begin{bmatrix} g & -g & 1 \\ -g & g & -1 \\ 1 & -1 & -\frac{2L}{\Delta} + V_C\left(\frac{2\pi}{2e}\right)\left(\frac{\Delta}{2}\right) cos\left(\frac{2\pi q_L}{2e}\right) \end{bmatrix} \tag{3.19}$$

and the RHS vector is given by:

$$\begin{bmatrix} -G(V) + gV \\ G(V) - gV \\ -L\left(I_0{}' + \frac{2I_0}{\Delta}\right) + V_C\left[sin\left(\frac{2\pi q_L}{2e}\right) + \left(\frac{2\pi}{2e}\right)\left(\frac{\Delta I_L}{2}\right) cos\left(\frac{2\pi q_L}{2e}\right)\right] \end{bmatrix} \tag{3.20}$$

These matrices can be together represented in the form of $[I] = [Y][V] + [RHS]$ given by the equation:

$$\begin{bmatrix} I_1 \\ I_0 \\ V_1 \end{bmatrix} = \begin{bmatrix} g & -g & 1 \\ -g & g & -1 \\ 1 & -1 & -\frac{2L}{\Delta} + V_C\left(\frac{2\pi}{2e}\right)\left(\frac{\Delta}{2}\right) cos\left(\frac{2\pi q_L}{2e}\right) \end{bmatrix} \begin{bmatrix} V_1 \\ V_0 \\ I_1 \end{bmatrix} + \begin{bmatrix} -G(V) + gV \\ G(V) - gV \\ -L\left(I_0{}' + \frac{2I_0}{\Delta}\right) + V_C\left[sin\left(\frac{2\pi q_L}{2e}\right) + \left(\frac{2\pi}{2e}\right)\left(\frac{\Delta I_L}{2}\right) cos\left(\frac{2\pi q_L}{2e}\right)\right] \end{bmatrix} \tag{3.21}$$

Chapter 4

QPSJ SPICE model program development in JSPICE and WRSPICE

The next step in the implementation of our QPSJ SPICE model is to develop appropriate programs which are compatible with the softwares JSPICE and WRSPICE, debugging them and then integrating them with respective softwares. The programs were developed in C language to be compatible with JSPICE and C++ to be compatible with WRSPICE. A Verilog-A model has also been developed to make a portable run-time loadable module for WRSPICE and any other softwares which support Verilog-A models. The Verilog-A model is simple to implement and portable but does not comprise in it, the mathematical versatility to describe the device given by MNA stamp of equation 3.21 which is then integrated directly with MNA stamps of other devices in the circuit. Instead, this model only uses the form given by equation 3.1, to derive its own MNA stamp, which is not suitable to describe all the complexities of the device. C and C++ based models have finer-grain control over the mathermatics of the device and are capable of handling the complete MNA description of the device and therefore have the logic flow with other devices in the circuit making them run faster. However, these models are complicated and even the simplest of the devices are time consuming to develop [44]. Each of these models will be discussed in detail in this chapter.

4.1 Verilog-A model of the device

The Verilog-A description of a device for implementation in modern circuit simulator CAD tools has been recently enhanced to provide greater support for compact modeling. It is mainly because of its dramatic improvement over C language which has been a standard language for device modeling since 1985 [44]. C interfaces of all the simulators have existing

functions which are used in the compact models of the device. The Verilog-A description simply has to connect the device description to these existing functions. Since it is a much easier language to develop models in, most of the model simulators incorporate Verilog-A models which are either run-time loadable or pre-loadable modules. But, as already mentioned, Verilog-A models have not yet reached a point in linking themselves with C or C++ libraries of the SPICE simulators, that will give complete privileges in the control of mathematics of the model.

In our Verilog-A model for QPSJ, we use the equation 3.1, by implementing the three parts of the device of picture 3.1 as three different devices in series. The entire Verilog-A code for our QPSJ model has been provided in Appendix B. This code is compatible with all the SPICE programs which support Verilog device models.

The module has been named *qps*, which is short for quantum phase-slip. It has two nodes, opposed to three nodes of Josephson junction SPICE model. The extra node for a JJ is used to determine/measure phase, but its counterpart, charge node has not been included in the QPSJ model in this version. The two nodes are input-output nodes that connect to the rest of the circuit. The resistor, inductor and a quantum phase-slip are connected in series through internal electrical signals of the model. The default parameter and constant values, which are internal to the model as well as those that can be changed by the user are then defined with the default values that are provided in the previous section. The device model equations from the previous chapter are then introduced, but without the MNA analysis. The syntax of the model is based on the description given in [44] and [45].

This model has been made compatible with and included in WRSPICE, where it can be loaded during run-time before loading the circuits. The adms translator converts this Verilog-A model into C++ files using pre-defined functions in WRSPICE to convert this model into an MNA based device similar to others in the program. This translation is however, not as accurate or flexible to use as that of an originally developed C++ model. These C++ files are then compiled to create a loadable file which is then called into the WRSPICE using its

command line input before a circuit with this device is loaded. The letter p denotes a QPSJ along with the module name *qps* for entering all the input parameters in the model section in SPICE program.

4.2 C and C++ based MNA models of QPSJ

Both the C and C++ models are discussed in this section as both of these models are very similar, atleast in the context of development of a device model. The older SPICE softwares used C language as the platform for developing the entire software including the simulation part of the circuits and setting up device models. The latest softwares use C++ models, although, there is a lot of development in including Verilog-A device models as an internal part of these programs to eliminate the requirement of developing additional models added by users to the software in C++. In the context of this thesis, JSPICE uses C and WRSPICE uses C++. They are very similar as WRSPICE is seen as an advanced version of JSPICE.

All of the SPICE programs use MNA analysis in solving circuits along with numerical methods that are already discussed in the previous chapters. The internal details of programming these solution methods are not required by the user developing device models. In this thesis, some of the details of these programs are discussed briefly to provide some understanding into how new device interface with the rest of the SPICE program.

Several pre-defined functions, or macros, or procedures exist in SPICE programs which are used in developing models for devices to simplify the programming. A header file is prepared for each device that includes all the parameter variables, constants, functions and pointers for MNA matrix elements that the device will use. This header file will also include the details of key words that are used in a SPICE circuit program while describing the device. For a QPSJ, in both C and C++ models, the key word *qps* and the letter p denote the usage of the device in the circuit. It has the syntax:

p{name} {node1} {node2} qps

.model qps{parameters}

where the first line defines the position of the input-output nodes of device in the circuit and the second line links the device to QPSJ model and also takes the parameters as inputs from the user. These parameters have *keyword* names defined in the previous chapter. Now, the developed header file is used in all the functions used by the QPSJ model.

A simple function defined as *qps.c* in JSPICE or *qps.cc* in WRSPICE links all these keywords of device and parameters to the actual variables defined in the header file. This program also links the functions defined in the device to the SPICE software.

Programs *qpsmpar.c*,*qpsparam.c*,*qpsask.c* and *qpsmask.c* for JSPICE and *qpsaski.cc*, *qpsaskm.cc*, *qpsseti.cc* and *qpssetm.cc* for WRSPICE have functions which act as the bridge between input-output parameters of the model or an instant. The input parameters given by the user are assigned to the respective variables to instances or the entire models through these functions. Similarly, the output values reach the user interface through these functions. The names of the functions suggest the action of respective functions.

The function *qpsload.c* of JSPICE or *qpsload.cc* of WRSPICE is where the actual calculations take place. Each element of the MNA matrix or the RHS vector is calculated here for the most generic case and the results are assigned to the respective matrix row-column positions. Each element of the matrix is defined by a pointer. All of these pointers are assigned to the MNA matrix and RHS vectors based on the numerical method developed in the previous chapter equation 3.21. The additional calculations to reach this point to obtain final MNA matrix by using currents/charges of previous state or iteration are also defined in this function. The actual code used in calculations or actual assignment commands are not provided here. But they are similar to the already existing devices in SPICE.

The functions *qpssetup.c* in JSPICE or *qpset.cc* in WRSPICE are the functions where the default values for parameters are assigned in a way to take them up when no user values

are supplied for these variables. Along with this, the pointers representing matrix elements are specified their positions in the matrix based on the nodes of the device in the circuit. This action is handled by a predefined function in SPICE which is just called here with their pointers assigned as its variables. Time-step limits are also assigned in this function.

There are additional functions for each device apart from the specified ones so far. But the definitions of these functions are not mandatory always. Programs like *qpsacld.c* or *qpsacld.cc* are to assign matrix elements corresponding to AC analysis of the device. Similarly, there are functions for noise and temperature along with additional functions if required for each of these device. These functions can be left empty if those analyses are not required for the device.

The details of the code are not provided for any of these functions, but they are similar in all the SPICE softwares and can be understood by studying the existing device models in the software.

The JSPICE functions are developed and small changes are made to the existing SPICE software to allow it to recognize the new device. A makefile has been developed to compile and debug these programs. Then the existing setup files are slightly modified to install the software with the new device included in it. Simple circuit simulations with QPSJ are run and the results are provided with explanations in the next chapter.

In the development of WRSPICE model for QPSJ, the Verilog-A model has been used. This Verilog-A model, when used with adms translator, generates C++ files with a loadable output file. The C++ files are then edited, mainly the program *qpsload.cc*, to get an accurate description of the MNA part of the device. Then the setup scripts are modified to include these C++ files instead of Verilog-A file when the QPSJ model is loaded. This approach simplified the programming and debugging process, as the simple non-mathematical functions and header files are already generated by the adms translator from the Verilog-A program. WRSPICE results with QPSJ based circuits are also provided in the following chapter.

Chapter 5

SPICE simulation results and example circuits

The QPSJ model has been implemented in JSPICE and WRSPICE. Although the model is exactly the same, differences in program executions were observed with better performance in terms of convergence of the model and also speed, seen in WRSPICE. Therefore, the simulation results shown in this chapter are performed in WRSPICE. A QPSJ with resistor in series has been simulated to observe the I-V characteristics of the device. Some of the basic example circuits are then designed and simulated to verify the validity and working of the model developed. All the presented examples show efficient operation of the model with valid and interesting results. They are discussed in this chapter.

5.1 I-V characteristics of a QPSJ

An I-V curve of a QPSJ is expected to show different characteristics in different regions of operation, which correspond to respective phases. The circuit used for the simulation of the device is shown in figure 5.1. The SPICE program corresponding to this circuit is given in Appendix A.

The circuit in figure 5.1 has been simulated with a piece-wise linear voltage starting at $0V$ and reaching $1.2mV$ at the end of $4ns$. The sub-gap resistance is $1 \times 10^9\Omega$ and normal resistance is $1.6 \times 10^6\Omega$. Inductance value is $89mH$ and critical voltage is $700\mu V$. The corresponding I-V curve output of the WRSPICE is given by figure 5.2.

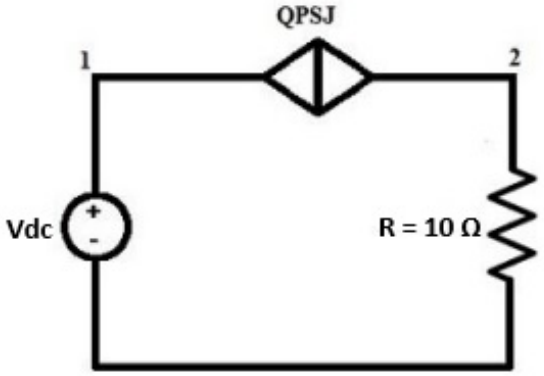

Figure 5.1: QPSJ circuit for transient I-V simulation.

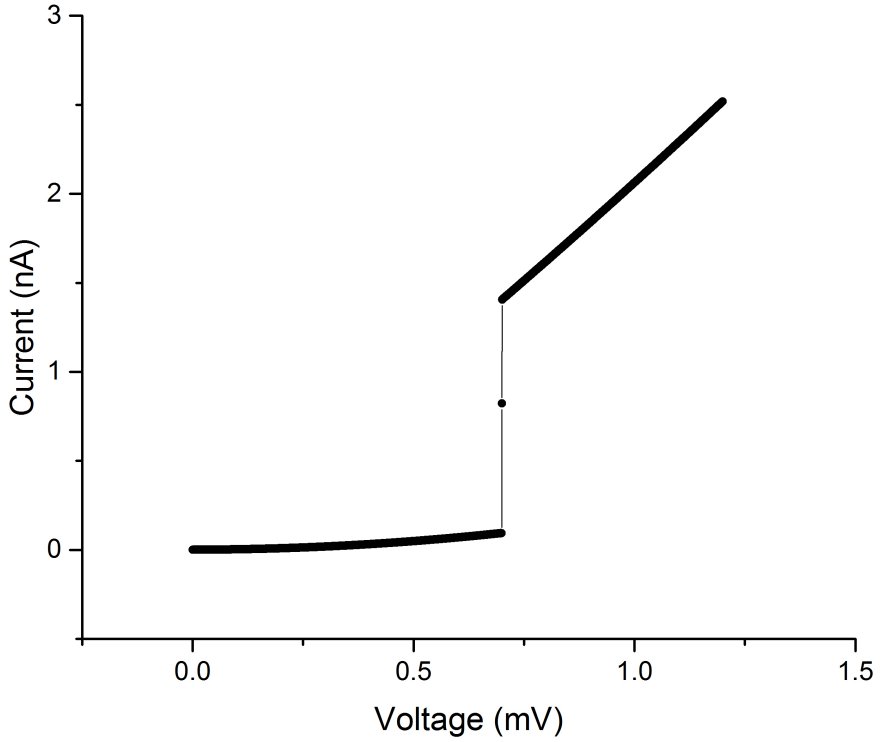

Figure 5.2: I-V characteristics of a QPSJ.

Below $700\mu V$, the device undergoes a phase-slip event which correspond to a voltage drop across the device. When the voltage is further increased, there is a transition from

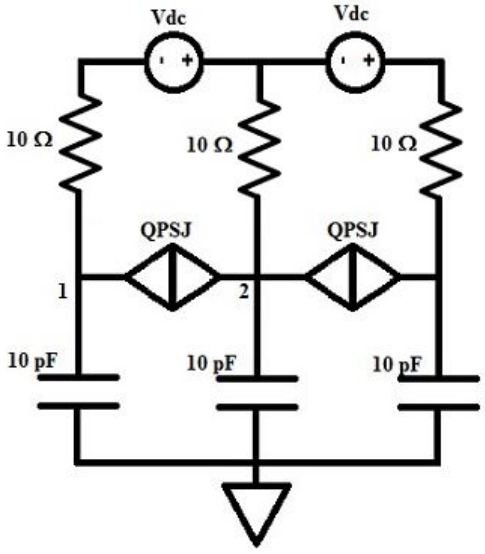

Figure 5.3: Charge-based logic/memory circuit obtained from [29].

superconducting state to normal state. Even in superconducting state, the device exhibits resistance, which can correspond to thermal phase-slips or quasi-particle resistances etc., depending on the experimental or modeling setup. The device then exhibits a normal state above $700\mu V$ till it reaches the applied voltage of $1.2mV$. In this region, the behavior seen is of a resistor. The I-V characteristics are very sensitive to the simulation parameters chosen. A longer transition between normal and phase-slip state can be seen if inductance value is decreased. Similarly, lower dissipation can be seen during phase-slip event when sub-gap resistance is decreased.

5.2 Charge-based superconducting memory

A charge-based memory circuit dual to a flux-based logic has been proposed in [29]. The circuit is provided in the figure 5.3. The corresponding SPICE program has been provided in Appendix B. A clear switching between two states has been observed at the critical voltage along with hysteresis.

The circuit in figure 5.3 has been simulated with a piece-wise linear voltage starting at $0V$ and reaching $2mV$ at the end of $4ns$. The sub-gap resistance is $1 \times 10^9\Omega$ and normal

resistance is $1.6 \times 10^6 \Omega$. Inductance value is $89mH$ and critical voltage is $700\mu V$. All default parameters are chosen for this simulation. The corresponding I-V curve is given by figure 5.4.

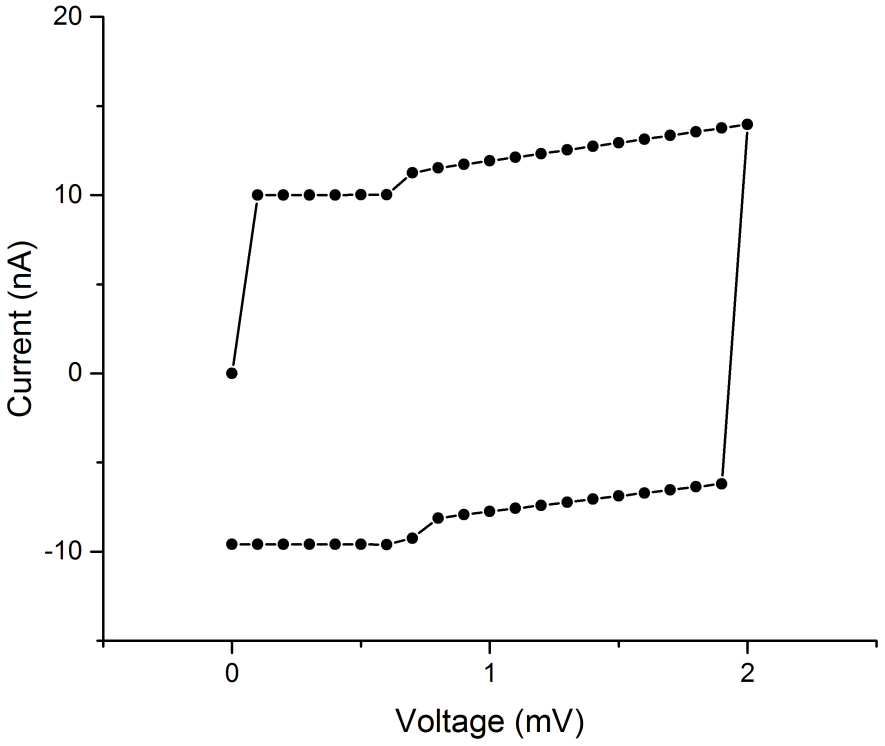

Figure 5.4: I-V curve of Charge-based logic/memory circuit obtained from [29].

The capacitors charge and discharge as the QPSJs switch between phase-slip regions and normal regions respectively giving a two-level loop with currents flowing in opposite directions resulting in hysteresis, while the switching of states between phase-slip and superconducting correspond to the switching behavior seen in the circuit.

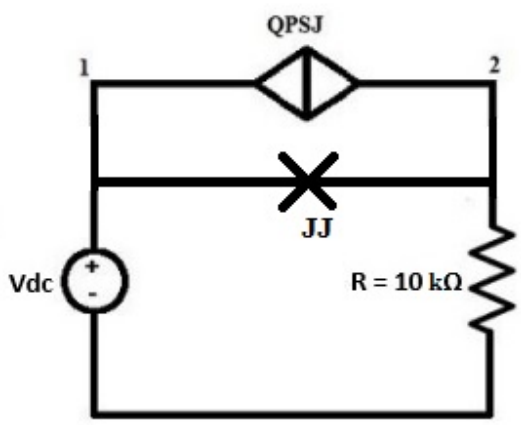

Figure 5.5: QPSJ and JJ in parallel.

5.3 QPSJ and JJ in parallel

A simple circuit with a QPSJ and JJ in parallel has been simulated. The parameters of both JJ and QPSJ are assigned so that the current/ voltage corersponding to their operation is expected to be comparable. The corresponding circuit is shown in figure 5.5.

Critical voltage of the QPSJ is $10\mu V$, and its inductance is $890\mu H$. Sub-gap and normal resistances are $1\times10^5\Omega$ and $1\times10^3\Omega$ respectively. Gap voltage of the JJ is $100\mu V$ and critical current of the junction is $50nA$. A piece-wise linear voltage has been applied with $0V$ at $0ns$ to $3mV$ at $2ns$. The corresponding SPICE program has been provided in Appendix I and the simulation result has been given in figure 5.6.

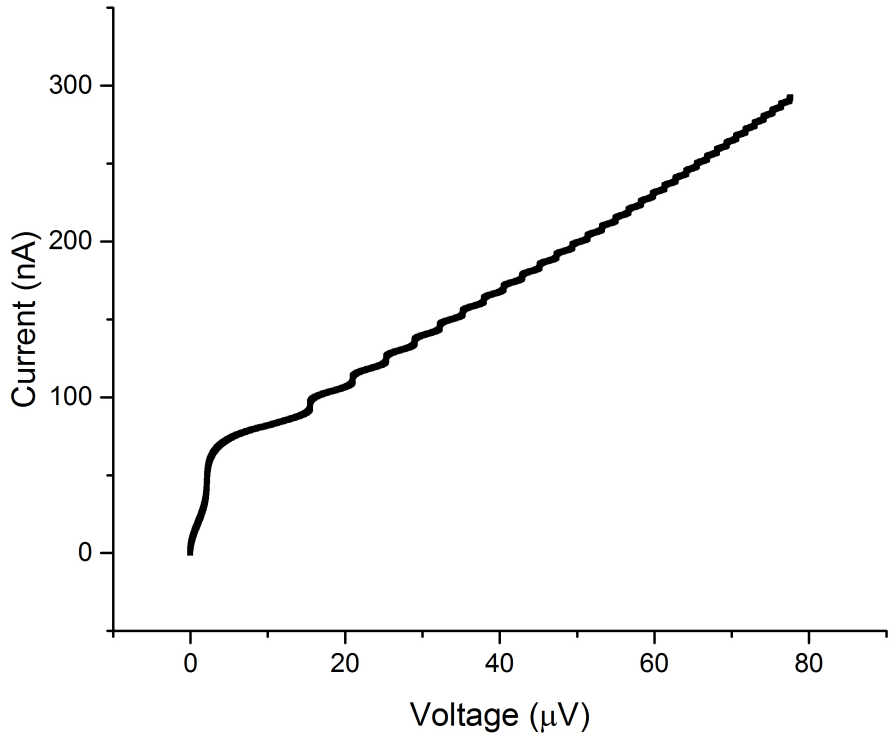

Figure 5.6: I-V simulation result of QPSJ and JJ in parallel.

An initial switching from phase-slip state to superconducting state has been observed at the critical voltage of the QPSJ which then triggered the oscillations in JJ. The result of this is seen as steps in the I-V curve of the circuit with voltage across QPSJ plotted against current through QPSJ.

5.4 QPS and JJ in series

QPSJ and JJ are now arranged in series with a resistor and the simulation has been performed similar to the simulation shown in earlier section. Parameters of both JJ and QPSJ are again adjusted to give an I-V characteristic where both QPSJ and JJ are significant. The circuit corresponding to the simulation is shown in figure 5.7.

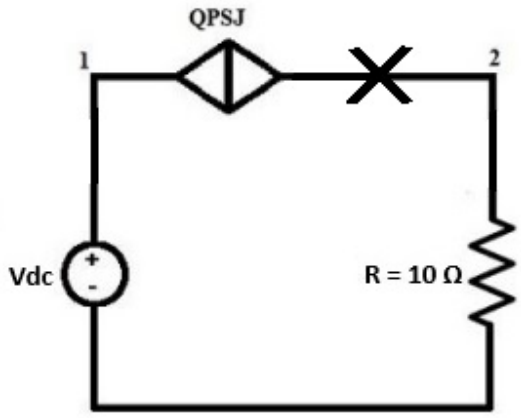

Figure 5.7: QPSJ and JJ in series.

Critical voltage of the QPSJ is $2mV$, and its inductance is $890\mu H$. Sub-gap and normal resistances are $1\times10^{9}\Omega$ and $1.6\times10^{6}\Omega$ respectively. Gap voltage of the JJ is $3mV$ and critical current of the junction is $0.5nA$. A piece-wise linear voltage has been applied with $0V$ at $0ns$ to $4mV$ at $2ns$. The corresponding SPICE program has been provided in Appendix I and the simulation result has been given in figure 5.8.

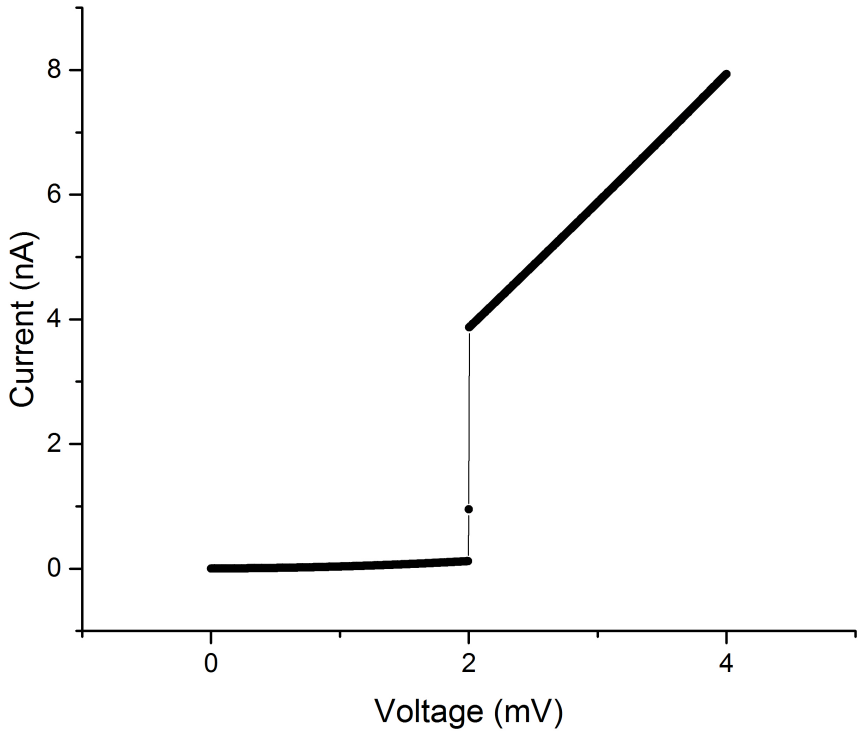

Figure 5.8: I-V simulation result of QPSJ and JJ in series.

The I-V curve seen is dominated by the behavior of QPSJ and therefore the JJ characteristics are hidden. Tuning the parameters of this circuit is required to achieve balance between behavior of JJ and QPSJ.

5.5 QPS loop

A QPS loop circut has been created with parallel Resistor and Capacitor set in series with each QPSJ. The circuit is shown in the figure 5.9. Both the QPSJ devices are identical. This simulation ensures two of the QPSJ devices can be simulated together.

Critical voltage of the QPSJ is $700\mu V$, and its inductance is $89\mu H$. Sub-gap and normal resistances are $1 \times 10^9\Omega$ and $1.6 \times 10^6\Omega$ respectively. A piece-wise linear voltage has been

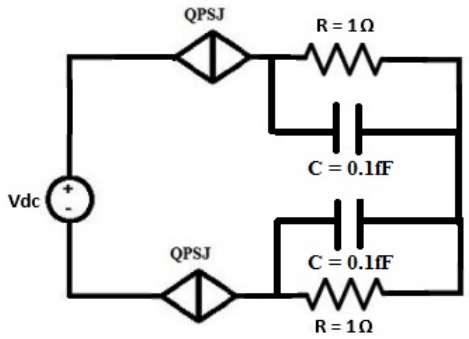

Figure 5.9: Two QPSJ devices forming a loop with resistors and capacitors.

applied with $0V$ at $0ns$ to $2mV$ at $2ns$. The corresponding SPICE program has been provided in Appendix I and the simulation result has been given in figure 5.10.

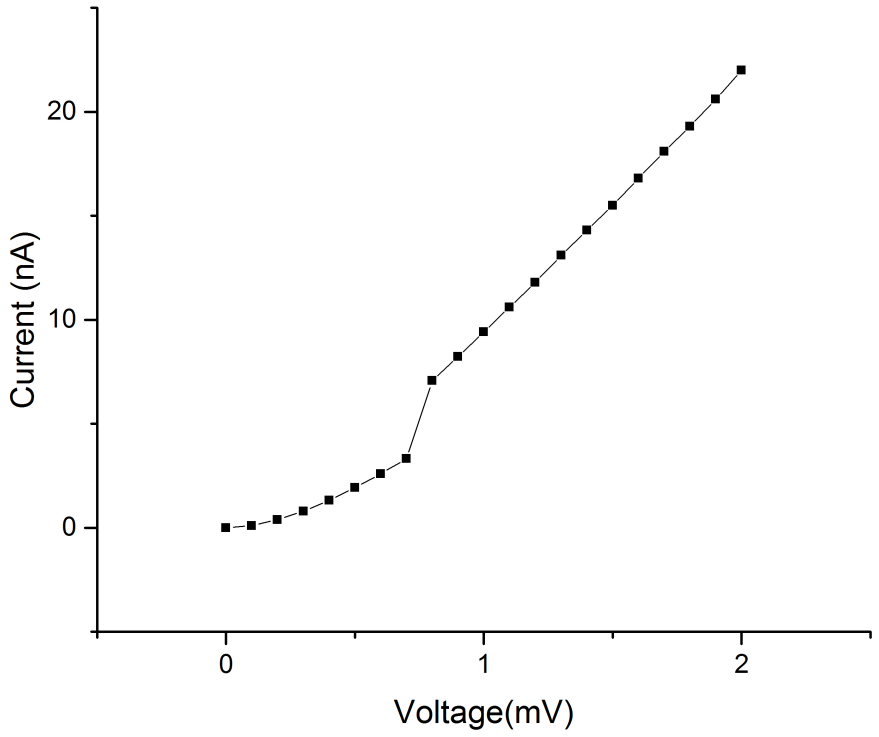

Figure 5.10: I-V simulation result of QPSJ loop circuit shown in figure 5.9.

5.6 Charge base logic using QPSJ

In the earlier section, we have seen charge based memory circuit example of a QPSJ. But that schematic is an exact dual to the Josephson transmission line, which is the building block of all RSFQ circuits. A QPSJ transmission line, therefore can be the building block of charge-based logic, a dual to RSFQ logic, and it is also possible to operate flux and charge complementing each other in a single logic system of complementary quantum logic (CQL). In this section, a single element of a QPSJ transmission line is simulated in WRSPICE using our model and is compared to the simulation of single element of a Josephson transmission line.

Figures 5.11 and 5.12 show Josephson transmission line schematic and QPSJ transmission line schematics respectively.

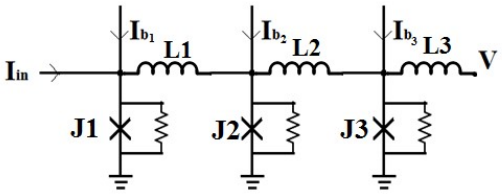

Figure 5.11: Josephson transmission line schematic.

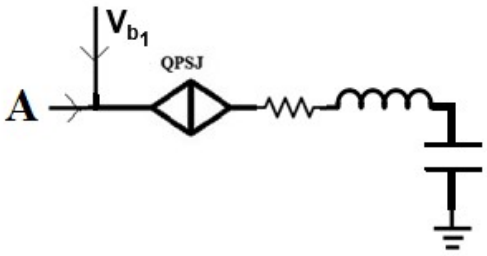

Figure 5.12: Quantum phase-slip transmission line.

A current bias is applied to JJ, which is lower than its critical current. Similarly, a voltage bias is applied to QPSJ, lower than its critical voltage. Now, when an input pulse

$5ps$ wide is applied, current pulse in case of JJ, and voltage pulse in case of QPSJ, both the devices switch causing a shift in phase of 2π in case of JJ, and causing a tunneling of charge of $2e$ across QPSJ. In JJ, the shift in phase can be seen as a flux quantum across the JJ, which is seen in the output voltage pulse (plotted as a function of time, see figure 5.13). Similarly, charge tunneling is seen in I versus time plot (see figure 5.14).

The charge-based logic in QPSJ can be used to construct logic similar to that of RSFQ, and both QPSJ and JJs can be used together in complementary quantum logic (CQL) to obtain better performance in logic operations.

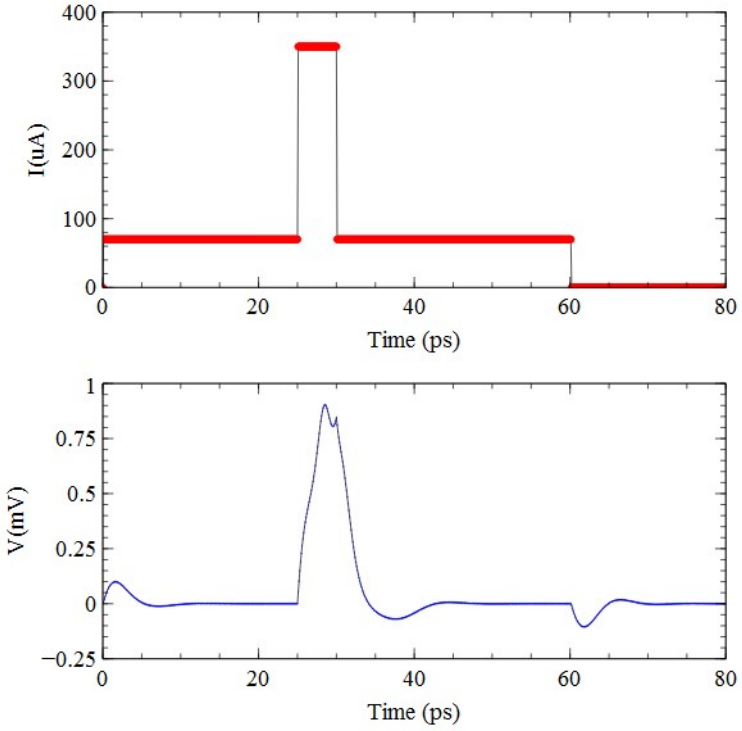

Figure 5.13: Time-domain simulation result of JJ based transmission line.

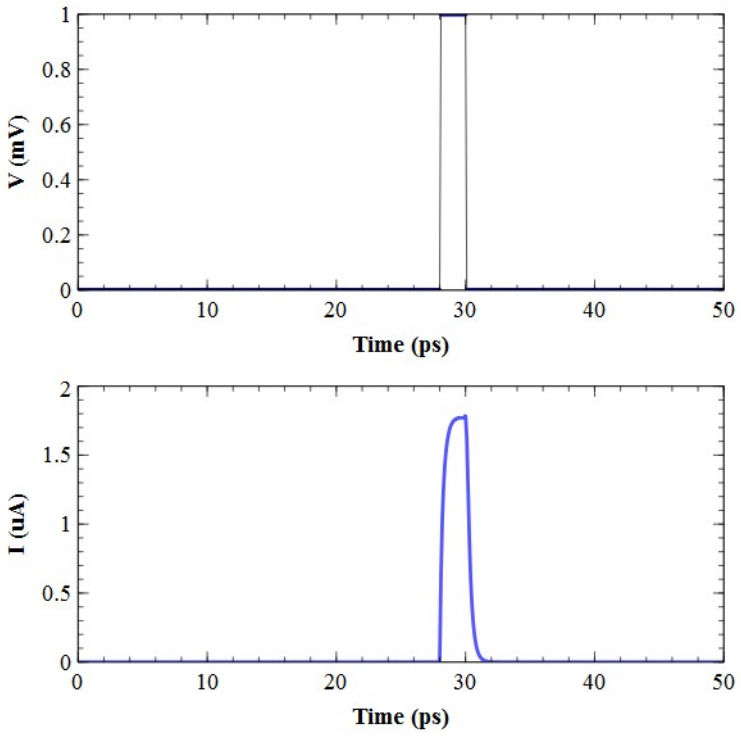

Figure 5.14: Time-domain result of QPSJ based transmission line.

Chapter 6

Conclusion and future work

A generic and simple version of a quantum phase-slip junction has been modeled and implemented in WRSPICE and JSPICE in this work. Many theories and models exist to account for the details of the behavior of a QPSJ in different regions, but there is no single established model to describe a QPSJ as a device in a circuit. The model used in this work is generic and valid for all the models. In the future, we will continue to work on improving the model and provide the end-user of this model, with a set of variables that he can assign based on experiments, while all the internal parameters are derived from these user variables.

This version of the QPSJ SPICE model also has some issues with convergence, especially when we try to modify time-step to observe the effects of plasma oscillations. Although these issues can be addressed by the user by a proper choice of initial conditions, the numerical model can be modified to solve convergence problems while still maintaining consistency with the theory of quantum phase-slips. Implementin this timestep modification to accurately track plasma oscillations will enable the device to latch a single unit of charge when switched even when the input conditions are changed. This will lead to an accurate description of charge-based logic, dual to flux-based logic in JJs and therefore enable the development of this new logic family.

An interesting next step with this model is to develop a complementary quantum logic (CQL) family which uses both charge and flux as the logic levels, and there is a possibility for conversion of flux to charge and vice-versa. Figure 6.1 and 6.2 below illustrate the idea of charge-flux conversion and flux-charge conversion respectively. Simulation results for these schematics are also provided in figures 6.3 and 6.4.

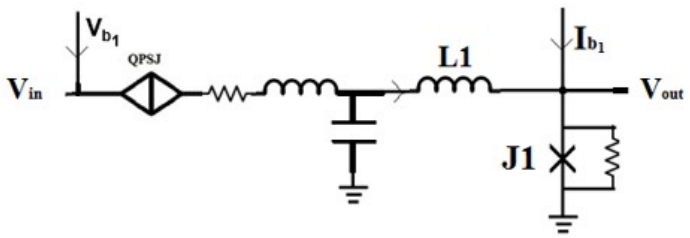

Figure 6.1: Charge-flux conversion scheme based on CQL.

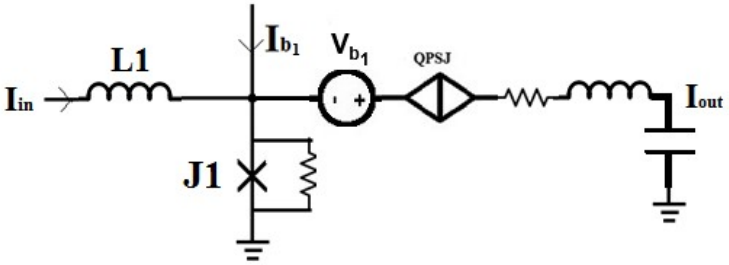

Figure 6.2: Flux-charge conversion scheme based on CQL.

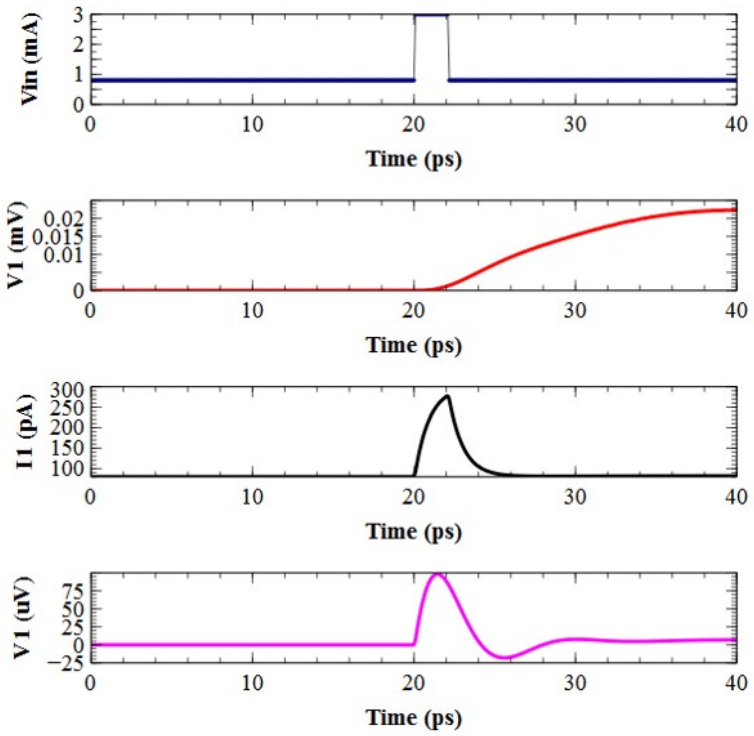

Figure 6.3: Time-domain simulation results of charge-flux conversion scheme based on CQL.

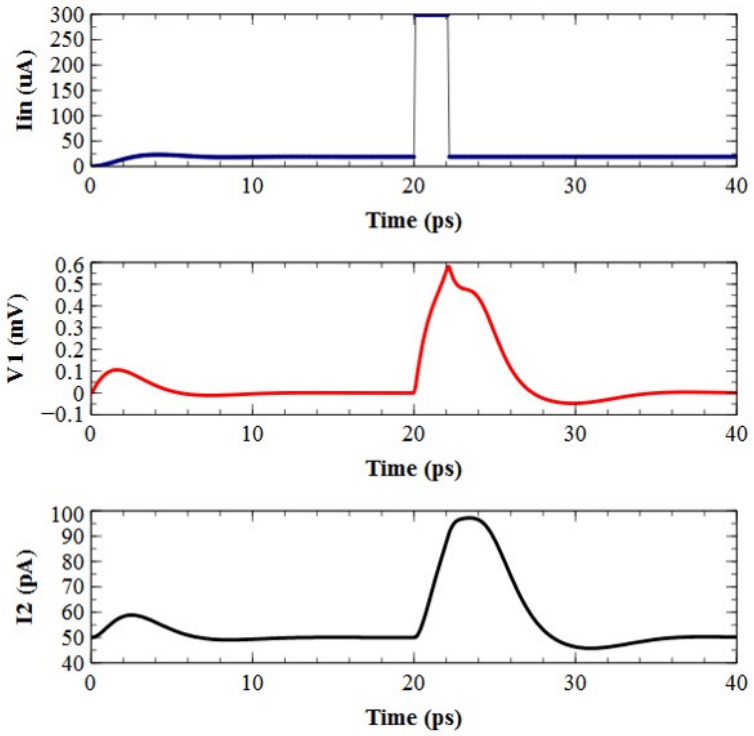

Figure 6.4: Time-domain simulation results of flux-charge conversion scheme based on CQL.

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Appendices

Appendix A

SPICE programs of the circuits discussed in chapter 5

A.1 QPSJ I-V characteristics

SPICE program for the circuit simulation shown in figure 5.1,

```
p1 1 0 qps
v1 5 0 pwl(0 0 4n 1.2m)
r1 5 1 10

.model qps p(level=2, ind=8900u, vcrit=700u, rsub=1e9, rnorm=1.6e6)
.control
tran 2p 4n
plot -v1 branch vs v(1)
.endc
```

A.2 Memory/logic circuit based in QPSJ

SPICE program for circuit simulation shown in figure 5.3,

```
p1 1 4 qps
p2 4 7 qps
r1 1 8 0.001
r2 4 9 0.001
r3 7 10 0.001
v1 8 9 pwl(0 0 2n 2m 4n 0)
```

```
v2 9 10 pwl(0 0 2n 2m 4n 0)
c1 1 0 0.01p
c2 4 0 0.01p
c3 7 0 0.01p

.model qps p(level=2, ind=8900u, vcrit=700u)
.control
tran 100p 4n
plot -v1 branch vs v(1)
.endc
```

A.3 QPS and JJ in parallel

SPICE program for the circuit simulation shown in figure 5.5,

```
p1 1 0 qps
b1 1 0 jj1
r1 1 2 10K
v1 2 0 pwl(0 0 2n 3m)
.model qps p(level=2, vcrit=10u, ind=890u, rsub=1e5, rnorm=1e3)
.model jj1 jj(vg=100u,icrit=50n)
.control
tran 2p 2n
plot -v1 branch vs v(1)
.endc
```

A.4 QPS and JJ in series

SPICE program for the circuit simulation shown in figure 5.5,

```
p1 1 2 qps
b1 1 2 jj1
p2 2 3 qps
r1 3 0 10.0
v1 1 0 pwl(0 0 2n 4m)
.model qps p(level=2, vcrit=2m)
.model jj1 jj(vg=3m, icrit=0.5n)
.control
tran 2p 2n
plot -v1 branch vs v(1)
.endc
```

sectionQPS loop SPICE program for the circuit simulation shown in figure 5.5,

```
p1 1 2 qps
p2 1 3 qps
c1 2 0 0.0001p
c2 3 0 0.0001p
r2 3 0 1
r1 2 0 1
v1 1 0 pwl(0 0 2n 2m)
.model qps p(level = 2, ind=89u)
.control
tran 100p 2n
plot -v1 branch vs v(1)
```

.endc

Appendix B

Verilog-A model for QPS

Although Verilog-A model for a QPS is not mathematically completely accurate or flexible, it is a simple model and can be loaded into any compatible SPICE programs. The entire Verilog-A program is provided here.

```
//Quantum phase-slip junction model

// January 25,2015
//MODULE: qps(node_plus, node_minus)

‘include ”disciplines.vams”
‘include ”constants.vams”

‘define IcR      0.4375e-9 // mV, critical current * normal resistance
‘define Vm       23.333e-6 // mV, critical current * subgap resistance

module qps (n1, n4);

inout n1, n4;
electrical n1, n2, n3, n4;
branch(n1,n2) bj; // QPS branch
branch(n2,n3) bl; // Inductance branch
branch(n3,n4) br; // Resistance branch
```

```
    // initial conditions
parameter real ic_chrg = 0 from [-100:100];

// Add a scaling factor (like length factor) - Currently not added as no standard values from industry exist for QPS

// parameters used in the model

//Critical voltage
parameter real vcrit = 0.7m from [0.01m:100m]; // Range of values specified is randomly chosen

//Inductance of the devices
parameter real ind = 890.1e-5 from [1e-15:1e-2]; // Range is randomly chosen

//Critical current density and spread
parameter real icrit = 4e-10 from [1e-12:1e-5]; // Random range chosen
parameter real deli = 4e-11 from [1e-15:1e-7]; // Random range chosen

//Subgap and normal resistances
parameter real rsub = 1e9 from [1e3:1e12]; //‘Vm/vcrit; //In the actual compiled program, these are assigned to numerical values
parameter real rnorm = 1.6e6 from [1e-6:1e12]; //‘IcR/vcrit;

// pi over e.
parameter phi0 = 1.0/3.291086546e-16;
parameter ch0 = 1.9625e-19;
```

```
//Dropback current
parameter idpback = sqrt((1e-3)*ind/ch0); // Calculate this again. Look into theory

real chrg, dv2, r, avj, rmid, itmp;

analog begin
//Supercurrent.
chrg = idt(ch0*I(br), ic_chrg);
V(n1,n4) <+ vcrit*sin(`M_PI*chrg);

V(ch) <+ ch; // May or may not want this line.
I(ch) <+ ch;
I(ch) <+ -V(ch);
// Voltage across inductor.
V(n1,n4) <+ (ind)*ddt(I(br)); // Use different way to represent voltage at nodes

//Quasiparticle current
dv2 = deli/2.0;
avj = abs(V(br));
if (avj <= vcrit - dv2)
r = rsub;
else if (avj < vcrit + dv2)
begin
v1 = (icrit - dv2)*rsub;
v2 = vcrit; // Come up with a better way for transition from super to normal.
rmid = abs(1/(((vcrit-dv2)/rsub)-((vcrit+dv2)/rnorm)));
```

```
r = rmid;
end
else
r = rnorm;

I(br) <+ V(n1,n4)/r;
// Limit time step. This is important, as the simulator may have
// no other way to recognize the supercurrent and plasma
// oscillation and limit the time step accordingly.
//

itmp = avj;
if (itmp < idpback)
itmp = idpback;
$bound_step(0.2/(ch0*idpback));
end
endmodule
```