Thin Film Multichip Packaging for High Temperature Geothermal Application

by

Kun Fang

A dissertation submitted to the Graduate Faculty of
Auburn University
in partial fulfillment of the
requirements for the Degree of
Doctor of Philosophy

Auburn, Alabama
August 1, 2015

Keywords: thin film, silicon carbide, flip chip,
high temperature packaging

Approved by

R. Wayne Johnson, Chair, Emeritus Professor of Electrical & Computer Engineering
Michael C. Hamilton, Assistant Professor of Electrical & Computer Engineering
Robert N. Dean, Associate Professor of Electrical & Computer Engineering
Dong-Joo Kim, Associate Professor of Materials Engineering

Abstract

A DOE sponsored study by MIT concluded that geothermal energy could provide 100,000 MWe or more in 50 years by using advanced technology knowns as Enhanced Geothermal Systems (EGS). In EGS, the measurement-while-drilling (MWD) tool is a crucial part. The MIT study indicates that high temperature instrumentation for geothermal is a key technology deficiency. In-well EGS electronics must operate at temperatures of >250°C and production monitoring electronics must operate for 10-20 years. In this work, a multilayer thin film substrate technology with flip chip bonding has been developed to interconnect multiple SiC devices along with passive components. Key elements of this high temperature multichip packaging technology include the thin film multilayer interconnection substrate and die assembly with flip chip bonding. New developments in each of these areas for high temperature operation have been discussed in this research.

The multilayer substrate technology based on AlN substrate, thin film metals and insulator has been developed for packaging of digital SiC electronics. The target operating temperature is 300°C with potential for higher temperature use. The conductor was vacuum deposited Ti/Ti:W/Au followed by an electroplated Au. A PECVD silicon nitride was used for the interlayer dielectric. The effect of 300°C storage on the multilayer structure has been studied. In addition, the electrical properties of the dielectric, including leakage current, capacitance and dissipation factor, have also been measured as a functional of

aging temperature and aging time. The leakage current at 300ºC with constant 20V bias has also been investigated.

Thermocompression flip chip bonding of Au stud bumped SiC die was used for electrical connection of the digital die to the thin film substrate metallization. Shear test has been performed on flip chip samples after thermal aging test, thermal cycling test and thermal aging test with shock and vibration. Besides single stud-bump configuration, a double bump configuration has also been developed and evaluated to improve the thermal cycling performance of stud bump assembly.

With thin film multichip packaging technology developed in this project, five kinds of digital circuit boards were fabricated at Auburn University and tested at GE Global Research Center. The reliability of these digital circuit boards based on electrical performance after thermal aging test, vibration test and shock test has been discussed.

Acknowledgments

Table of Contents

List of Tables

List of Figures

CHAPTER 1 INTRODUCTION

1.1   High Temperature Electronics (HTE)

Definitions of high temperature electronics (HTE) vary widely, depending on its application area. Generally speaking, high temperature electronics is taken to mean "devices or systems, which are capable of sustained operation in high temperature environments [1]". The high temperature is defined as the temperature higher than the MIL-SPEC 334 range whose upper limit is 125 ℃. This represents the temperature limit for most commercially available electronics. However, the global demand for electronics with a higher working temperature is pushing the development of high temperature electronics forward.

1.2   Application of High Temperature Electronics

The high temperature is usually caused by a high temperature environment or the high power dissipation of the device itself. When the temperature is too high, the electrical performance and reliability of electronic components are highly affected. For example, the capacitance of a capacitor may decrease significantly with high temperature; for a transistor, the leakage current increases; for solders, the mechanical strength decreases with increasing temperature up to the melting point and polymers may decompose.

In order to address all these issues caused by high temperature, conventional-temperature-range electronics with insulation or cooling are sometimes used. Obviously, electronics capable of high temperature operation provide many benefits in these applications. First of all, the high temperature electronics do not have to be integrated with

thermal sinks, a vacuum-insulated box or a water/air cooling system. In aerospace engineering and the aircraft industry, eliminating the need for this cooling equipment reduces the total weight and the complexity of the device, which also reduce the total cost and potential for failure.

What is more, high temperature electronics also extend device reliability and operating lifetime at conventional temperature range. Honeywell HT SOI electronics rated for 5 years at 225 ℃ have a potential for 10 years at 200 ℃ and 20 years at 150 ℃ [2]. High temperature aging test also serves as an important part of reliability test of conventional-temperature-range electronics.

In recent years, high temperature electronics have been widely used in well logging, combustion systems, industrial processes, space exploration, military electronics, automotive, nuclear reactors and aircraft. For example, the distributed engine control electronics in automotive is required to work near 200°C with a 5000hr lifetime [1]; The engine monitoring, which is extremely essential in the space shuttle, can only be achieved with sensors which can survive the operational temperature of 500-600°C [1]; Electronics in nuclear reactors have to withstand ambient temperature from 25 to 1000°C [4]. Table 1.1 lists a number of high temperature electronics applications and summarizes their operational temperature, minimum duration and other requirements [3] [4].

Table 1.1 Application Area and Parameters for High Temperature Electronics [3][4]

Application	Temperature (°C)	Minimum Duration	Duty	Other Environmental Factors
Well-logging-gas & oil (down-hole) instrumentation	150 to 300	Few hours-years	Intermittent/cyclical, or continuous	Temperature cycling, chemicals, pressure, mechanical stress, possibly radiation
Well-logging-geothermal	150 to 400	Few-100 hours	Intermittent/cyclical	Temperature cycling, chemicals, pressure, mechanical stress
Aircraft systems-on engines & smart transducers	300 to 500	1000 hours	Intermittent/cyclical	Temperature cycling, vibration, stress, fuel/oil/chemicals
Aircraft engine R & D	500 to 600	1000 hours	Intermittent/cyclical (one-shot acceptable)	Temperature cycling, shock/vibration
Automobiles	150 to 250	8000 operating hours, 10 years "shelf"	Intermittent/cyclical	Temperature cycling, vibration, fuel/oil/chemicals, rough handling
Fossil-fuel energy plants	400 to 500	Months-years	Continuous	Radiation
Nuclear reactors	25 to 1000	Months-years	Continuous	Radiation
Space Exploration	125 to 485	Months-years	Intermittent/cyclical, or continuous	Temperature cycling, chemicals, pressure, radiation
Nuclear waste storage	25 to 150	Months-years	Continuous	Temperature cycling, chemicals, radiation
Radars	-55 to 200	Months-years	Intermittent/cyclical, or continuous	Temperature cycling, radiation

1.3   High Temperature Electronics in Enhanced Geothermal System

Geothermal energy is a significant renewable energy besides solar energy, nuclear energy and wind energy. Geothermal energy is the large mount of heat from the earth which can be used in not only a large and complex power plant but also small and simple pumping system. In many regions of the world, geothermal energy is used as an affordable and sustainable replacement of conventional fossil fuels. For example, more than 8,900

3

megawatts (MW) of large, utility-scale geothermal capacity in 24 countries now produces enough electricity to meet the annual needs of nearly 12 million typical U.S. households (GEA 2008a) [5]. Geothermal plants produce 25 percent or more of electricity in the Philippines, Iceland, and El Salvador [5] [6].

The most common way to capture geothermal energy is by taking advantage of the natural hydrothermal convection system. In this system, cooler water seeps into the Earth's crust, heats up by thermal energy, and then rises to the surface. However, this naturally occurring hydrothermal convection system that allows water to circulate to the surface are found in less than 10 percent of Earth's land area, most geothermal energy is in dry and non-permeable rock [7].

A new technology called enhanced geothermal system (EGS) can provide more opportunities to capture geothermal energy in dry and hard rock. This enhanced geothermal system is able to drill wells and create a subsurface fracture system in hot and dry rocks. Then cold water is continuously injected into the injection well, where it heats up as it flows through fractures in the rocks. The water is then brought to the surface in multiple production wells, and its heat is extracted to generate electricity in power plants. Finally, the water, depleted of its heat, is re-injected to be heated again in the fractures, as shown in Figure 1.1 [8]. With the help of EGS, finding existing fractures that contain high flows of hot water is no longer a requirement for using geothermal energy. In the report of the Massachusetts Institute of Technology, "The Future of Geothermal Energy--Impact of Enhanced Geothermal Systems (EGS) on the United States in the 21st Century", the researchers evaluated the technical and economic feasibility of EGS becoming a major supplier of primary energy for U.S. base-load generation capacity by 2050 and they also

estimated that EGS could supply up to 10 percent of the country's electricity needs within 50 years at prices competitive with fossil-fuel fired generation [9].
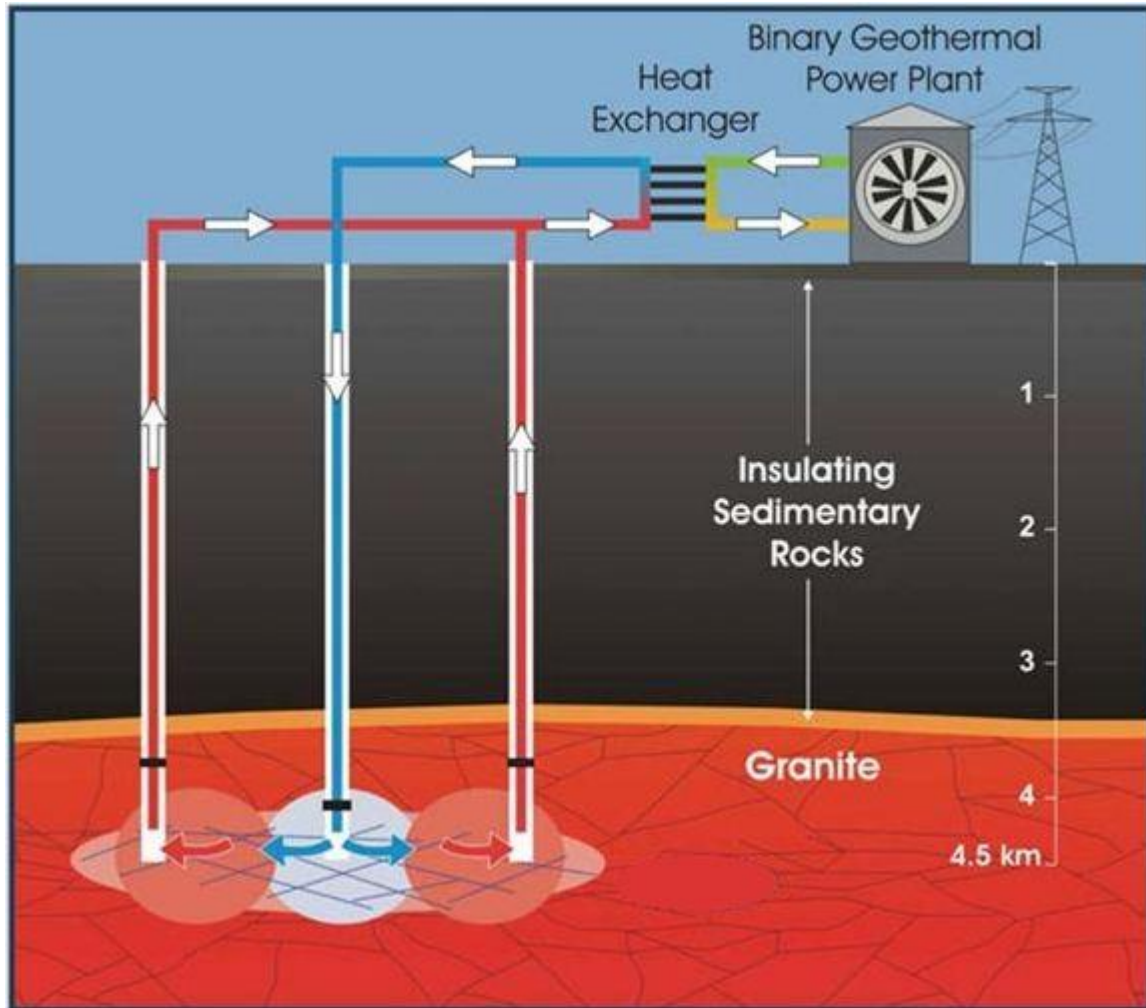
Figure 1.1 Diagram of an Enhanced Geothermal System [8]

In EGS, the measurement-while-drilling (MWD) tool is a crucial part. MWD is a type of well logging which incorporates the measurement devices into the drillstring and provides real time information to help steering the drill. The real time information may include temperature, pressure, strain, inclination, azimuth and fluid flow. All these parameters provide faster drilling, safer drilling and more accurate drilling [10].

Because MWD tools are used in the harshest operating environment, high temperature is always a challenge for the use of measurement while drilling (MWD) tools. Now most MWD tools can work at 150°C. For wireline logging, a Dewar flask is usually used to provide high temperature protection to sensors or digital circuits. This is because the high temperature exposure time is relatively short in wireline logging. However, using a Dewar flask is not practical for MWD tools because the Dewar flask cannot survive long time exposure and many sensors can hardly be flasked. The ideal MWD tools should be able to operate at high temperature for months [11].

1.4   High Temperature Electronics Packaging

A reliable and successful high temperature electronics device requires two elements: high temperature electronics components which can sustain harsh environment (integrated circuits, resistors, capacitor, jumpers, etc.) and stable packaging processes for all these high temperature components. In the following section, the material of these components, the material of packaging and the basic packaging process are discussed.

1.4.1   SiC Device

Since the 1960s, silicon has been used as a dominant semiconductor material in industry. However, due to its comparatively narrow energy bandgap, there are some problems when using silicon in integrated circuits operating at a temperature above 150°C. Even if the oxide-isolated process is used in the fabrication process of silicon CMOS to reduce the leakage current, the device still cannot work properly above 300°C. For example, when the temperature is increased in silicon MOSFETs and MOS integrated circuits, the drain to body leakage currents can increase by orders of magnitude and become comparable

to the drain channel currents. Under this situation, the transistor cannot be turned off by the gate and the leakage current dramatically decreases the noise margins [12].

In order to address the limitations of silicon, some wide bandgap semiconductor materials are considered to be the ideal choice for devices that operate at high temperature, high power levels, high speed and high radiation levels. Comparing to narrow bandgap materials (Si and GaAs), wide bandgap materials (SiC, GaN and diamond) have much lower intrinsic carrier concentrations. This avoids the deteriorating effects of thermally generated carriers. The widely used wide bandgap semiconductor materials include silicon carbide, gallium phosphide, gallium nitride, aluminum gallium arsenide and diamond. Table 1.2 shows some physical properties of the semiconductor materials mentioned above [4] [13] [14] [15].

Table 1.2 Physical Properties of Semiconductor Materials [4] [13] [14] [15]

	Silicon	GaAs	AlGaAs	GaP	SiC	Diamond
Band Gap (eV)	1.1	1.3	1.9	2.34	2.9	5.5
Breakdown Field (kV/cm)	250	300	500	----	2500	10000
Thermal Conductivity (W/cm · K)	1.5	0.5	0.1	0.8	4.9	20
Electron Mobility, R.T. cm^2/v-s	1400	4000	3000	350	250	2200
Hole Mobility, R.T. cm^2/v-s	600	400	----	100	50	1600
Electron Sat. Velocity 10^{7}cm/s	1.0	1.0	1.0	----	2.0	2.7
Dislocation Energy (eV)	13	9	9	----	22	----
Melting Temp. (ºC)	1412	1238	1304	1470	2700	----

The intrinsic carrier density n_i is the most important physics characteristic of semiconductor material. It depends on temperature and the bandgap of the semiconductor, as shown in this equation [4],

$$n_i = (\frac{2\pi kT}{h^2})^{3/2}(m_{dh}m_{dc})^{3/4}e^{-E_g/2kT}$$

Where k and h are Boltzmann's and Planck's constants, T is the absolute temperature, m_{de} and m_{dh} are the electron and hole effective masses, and E_g is the bandgap. The intrinsic carrier density is plotted in Figure 1.2 for Si, GaAs, GaP and SiC. Evidently, at temperatures higher than 300°C, SiC and GaP have much lower intrinsic carrier concentrations than Si and GaAs. This implies that the high temperature electronics devices should be made from wide bandgap semiconductor materials, to avoid the intrinsic carrier density exceeding the dopant density [4].
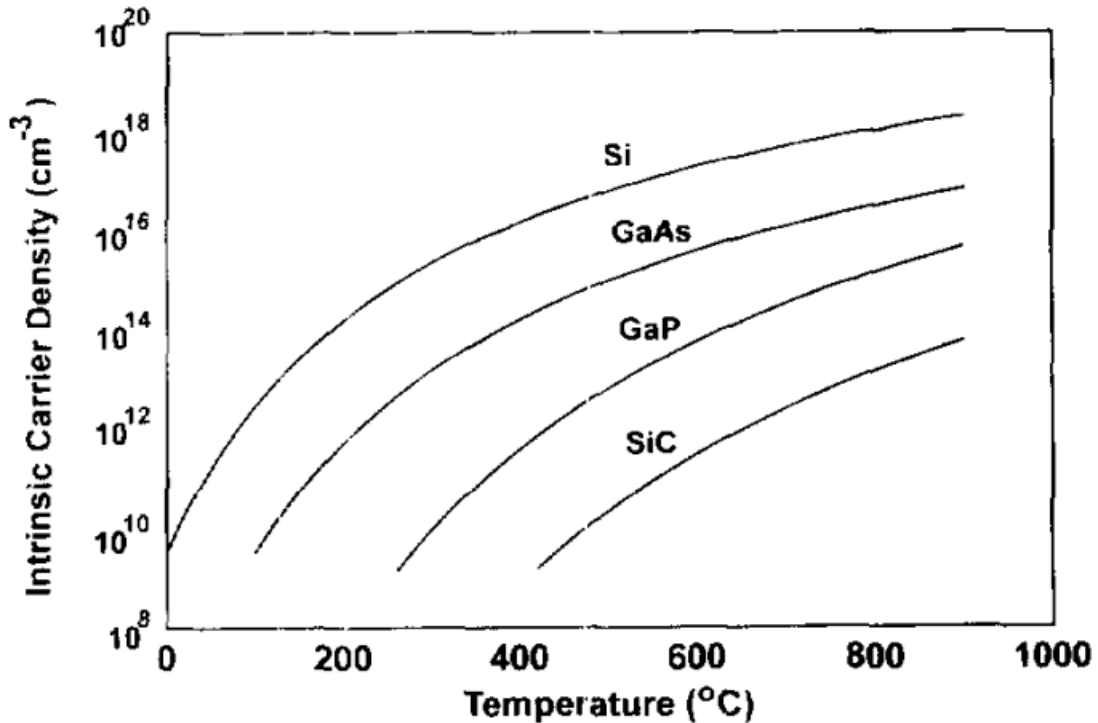
Figure 1.2 Intrinsic Carrier Density versus Temperature for Si, GaAs, GaP and SiC [4]

Among all these wide bandgap semiconductor materials, SiC was one of the first semiconductor materials that was investigated for commercial electronics applications. The favorable properties that make SiC an excellent material for high temperature application are as follows [14]:

- Large bandgap energy: the wide bandgap of SiC (2.2, 3.26 and 3.0eV for 3C-SiC, 4HSiC and 6H-SiC respectively) compared to the bandgap of silicon (1.1eV) avoids the intrinsic conduction effects. This leads to a much smaller intrinsic carrier concentration of SiC at temperature higher than 300°C and enables SiC devices to function at temperatures beyond 600°C.

- High breakdown electric field: the high breakdown electric field of SiC (about 1.8, 3.5 and 3.8MV/cm for 3C-SiC, 4H-SiC and 6H-SiC respectively) are approximately 10 times higher than that of Si (0.3MV/cm). This enables a reduction of the thickness of the conduction regions which results in very low specific conduction resistance. What is more, this allows the fabrication of high voltage, high power electronics devices with SiC. High breakdown electric field can provide increased isolation between devices and high packing densities.

- High thermal conductivity: the high thermal conductivity (~4-4.5W/cm·K) of SiC means that the heat produced by the device can rapidly flow through this material. At room temperature, SiC has even a higher thermal conductivity than any metal. This benefit allows SiC device to operate at high temperatures and high power levels with less cooling equipments. It also permits a power density increase which facilitates a more compact device or much higher power per area.

- High saturation velocity: the saturation velocity of all three types of silicon carbide is high ($\sim 2 \times 10^7$cm/s) compared to the value for silicon (1×10^7cm/s). This property allows SiC devices to operate at high frequencies (RF and microwave) than their silicon or GaAs RF counterparts.

- High bonding energy between Si and C: this makes SiC a thermally and chemically stable material with low friction coefficient and high hardness.

All of these properties of SiC make it an excellent semiconductor material for devices operating at high temperature to 600ºC and above; at high power and high voltage and at frequencies around 20GHz. Now U-shaped trench MOSFETs made from SiC that operate up to 450ºC and thyristors that operate at 350ºC have been presented [15]. SiC MOSFETs have been reported to operate at 650ºC [15].

1.4.2   Substrate Materials

Organic packaging substrates are dominant in the worldwide market not only for high performance and cost performance applications but also stacked memory applications. However, organic substrates have a glass transition temperature (T_g) in the 125-200ºC range. Above its glass transition temperature, the mechanical properties of the organic substrates decreases dramatically. High temperature exposure can also lead to polymer decomposition. Also organic substrates introduce the problem of significant thermomechanical mismatch because of the relatively high coefficient of thermal expansion (CTE). This is why ceramic materials have been considered for high temperature electronics application.

Polycrystalline silicon carbide, aluminum nitride and aluminum oxide ceramics are three most widely used substrate materials in the industry. Several properties of these

ceramics are shown in Table 1.3 [16] [17] [18] [19] [20] [21]. AlN is a covalently bonded ceramic which is synthesized from abundantly available elements Al and N. This ceramic does not occur naturally. Some advantages of AlN are shown as follows [16] [17]:

- High thermal conductivity: AlN, cubic-BN and BeO are the only ceramic materials that possess high thermal conductivity. Although BeO and c-BN show higher values than AlN (~200W/mk), use of BeO has been banned by numerous manufacturers because of its toxicity and c-BN is very difficult to produce. Thus, the nontoxic AlN continues to replace the other two in high temperature applications.

- Close thermal expansion coefficient to SiC: the coefficient of thermal expansion of AlN (4.5ppm/^{o}C) is closely matched to that of SiC (4.3ppm/^{o}C) over a wide range of temperature.

- Chemically stable: AlN has a Wurtzite crystal structure and is stable in inert atmospheres at temperature in excess of 2000°C.

- Resistance to corrosion and erosion: AlN exhibits a very good resistance to a wide variety of materials. Most metals, including Cu, Li, U, ferrous alloys, and some superalloys do not attack AlN. AlN is also stable against molten salts, such as carbonates, eutectic mixtures, chlorides and cryolite.

- High electrical resistivity

All these properties make AlN an ideal candidate for packaging SiC devices operating at high temperature.

11

Table 1.3 Physical Properties of Semiconductor and Substrates Materials [16] [17] [18] [19] [20] [21]

	SiC	Al$_2$O$_3$	AlN	BeO
Density, g/cm^3	3.1	3.89	3.26	2.85
Elastic modulus, GPa	410	375	330	350
Thermal conductivity, W/mK	120	35	140-180	270
Thermal expansion coefficient, ppm/ ^{o}C	4.0	8.4	4.5	9.0
Dielectric constant (@1MHz)	11.0	9.8	9	6.5
Dissipation Factor (@1MHz)	0.09	0.0002	0.0003	0.0004

1.4.3   Die and Substrate Metallization

In high temperature electronic devices or packaging, the semiconductor die or substrate must be connected with other components to become a functional system. The limitations for the high temperature operation are currently set by the stability of the contacts to the semiconductor material rather than semiconductor material itself. The reason is high temperature accelerates the interdiffusion process, with diffusion coefficients several orders of magnitude higher than at room temperature. This interdiffusion process may cause resistivity changes and adhesion issues. The desired characteristics of a metallization scheme are good adhesion to the semiconductor, good electrical conductivity, stable resistivity, low stress and minimal reactions at subsequent processing or assembly steps [22].

For the die metallization in this project, Ni was deposited on the SiC wafer surface. The Ni was then subjected to a high-temperature Rapid Thermal Anneal (RTA), forming a low-resistance nickel silicide. The nickel silicide served as the ohmic contact. On the top

of nickel silicide, a tungsten based metal was deposited with gold bond pads to provide an interconnection and bond pad level [38].

The metal stack on the substrate is typically a three-layer stack: adhesion layer, diffusion barrier layer and conductor layer.

- Adhesion layer: the adhesion layer should be made of a material which is thermodynamically stable contacting the substrate and also can provide good adhesion.

- Diffusion barrier layer: the diffusion barrier is introduced to minimize diffusion and interaction between the adhesion layer and conductor layers.

- Conductor layer: The conductor layer must have good conductivity, good wettability with die attach materials, good wire bonding properties, good solder ball attach properties and good resistance to surface oxidation.

In this project, the Ti/TiW/Au was selected as the substrate metallization for 300°C applications. The Ti was used as the adhesion layer to provide robust adhesion to the substrate. The TiW served as the diffusion barrier layer between Ti and conductor layer Au.

1.4.4   Dielectric Materials

Historically, silicon dioxide formed by thermal oxidation has been used as the dielectric and insulator material in microelectronics fabrication since the mid-fifties and is still the widely used at present. However, silicon dioxide is structurally porous as indicated by its low density ($\sim 2.2 \text{g/cm}^3$) and this porosity has some undesirable consequences [23]. In past few decades, the exploration of new dielectric materials has been prompted.

Dielectric films in microelectronics fabrication and electronics packaging must have a relatively high dielectric breakdown field, a high electrical resistivity, must be pinhole-free and should have a low compressive stress and excellent adhesion property [24].

More dielectric materials have been investigated including polymeric materials including polyimide, fluorinated parylene, polyamide-imide and silicone and ceramic materials including Al_2O_3, TiO_2, Ta_2O_5, AlN and Si_3N_4. Among these dielectric materials, polymeric materials exhibit good mechanical properties but are permeable to moisture and contaminants. For high temperature applications, ceramic materials are preferred become of their thermal stability and high thermal conductivity compared to polymeric materials [25].

In this project, PECVD silicon nitride was selected as the dielectric materials in the multilayer structure on the substrate. The PECVD silicon nitride has good insulating properties and thermal conductivity, ability to withstand thermal cycling (a close CTE to AlN) and it is a good barrier against moisture penetration and contaminant. The PECVD silicon nitride was deposited at $300^{\circ}C$ which is compatible with required package working temperature.

1.4.5 Wire Bonding and Stud Bumping

Wire bonding is the process of providing electrical connection between the pads on the semiconductor chip and the corresponding pads on the substrate by using very fine bonding wires [26]. In the wire bonding process, the tip of the bond wire is melted to form a sphere by electronic flame-off. Then the wire bonding tool, known as a capillary, presses this sphere against the bonding pad, applying mechanical force and ultrasonic energy to

14

create a metallic connection. The capillary next extends the gold wire to the corresponding pad on the substrate and makes a wedge bond with the help of temperature, pressure and ultrasonic energy.

There are many different wire bonding metallurgies used in the microelectronics industry. The most common wires are Au, Al and Cu. The most common wire bond pads are Al, Au, Cu and Ni. Usually, the gold-gold system is highly desired for high temperature application. The gold wire-gold pad is an extremely reliable wire bonding metallurgical system compared to other systems, since it is not susceptible to interface corrosion, intermetallic formation and other mechanisms that damage the bonding. And even non-ideal gold-gold bonding can self-heal itself and increase in strength with time and temperature.

1.4.6   Flip Chip Bonding

Besides wire bonding, flip chip attach is also a principle method for interconnecting ICs. In flip chip bonding, an electronic component or semiconductor device is mounted directly onto a substrate or a board in a face-down manner. The electrical connection between die and substrate is provided by conductive bumps positioned on the surface of the die. For conventional-temperature-range application, the spaces between the flip chip surface and the substrate is filled with a non-conductive underfill material to mechanically reinforce the bumps, increasing the thermal cycle reliability of the assembly. Flip chip bonding technique offers several advantages [27] [28]:

- Reduced package size: Without bond wires and packages, the board area can be reduced by up to 95% and the weight can be less than 5% of a packaged device. Meanwhile, the total height is also reduced.

15

- Low cost: Flip chip can be the lowest cost interconnection for high volume automated production, with cost below $0.01per connection.

- Great flexibility: The use of flip chip allows an increase in the number of I/O. The number of I/O is no longer limited to the perimeter of the chip as in wire bonding.

- Improved performance: Short interconnect between flip chip and substrate delivers low resistance, capacitance and inductance, small electrical delays, good high frequency characteristics and good thermal path.

- High reliability: Eliminating bond wires increase the reliability of interconnection in a vibration environment.

1.5   Research Outline

The goal of this project was to develop a multilayer thin film substrate technology which could interconnect multiple SiC devices along with passive components. The target operating temperature was 300°C with potential for higher temperature use.

In Chapter 2, the thin film multilayer technology is discussed. The effect of 300°C storage on the multilayer structure was studied. The electrical performance of the dielectric, including leakage current, capacitance and dissipation factor, was also evaluated.

In Chapter 3, the reliability of thermocomprossion flip chip bonding is reported. Shear test was performed on flip chip samples after thermal aging test, thermal cycling test and thermal aging test with shock and vibration. A double bump configuration was also been developed and evaluated.

In Chapter 4, the reliability of five digital circuit boards based on electrical performance after thermal aging test, vibration test and shock test is discussed.

In Chapter 5, the conclusion of this project and recommendation for the future work are summarized.

CHAPTER 2 THIN FILM TECHNOLOGY

2.1   Introduction to Thin Film Technology

In the last few decades, thin film has become an extremely important component of modern microelectronics devices. Meanwhile the rapid development of the microelectronics industry also has placed exceptional demands on thin film technology. The term "thin film" here refers to material layers deposited by physical processes or chemical processes, with thickness too small to permit characterization by conventional mechanical testing procedures [29]. Usually, the upper limit of thickness of thin film is around 20μm.

Thin film technology provides a variety of benefits for microelectronics fabrication. First of all, thin film can be processed to provide high wiring density. For example, sometimes only thin film packaging can provide the line width and spacing resolution to match the I/O pitch on the SiC die and a much higher wiring density. Secondly, thin film deposition techniques permit convenient production of high purity materials with highly controlled composition. Thirdly, this thin film layer can be deposited on glass, plastic and even some flexible materials, opening a wide range of possibility for flexible electronics.

Generally, the thin film deposition processes can be classified into three categories: physical vapor deposition (PVD), chemical vapor deposition (CVD) and plating. Classification of the most common deposition processes is shown in Figure 2.1 [30].
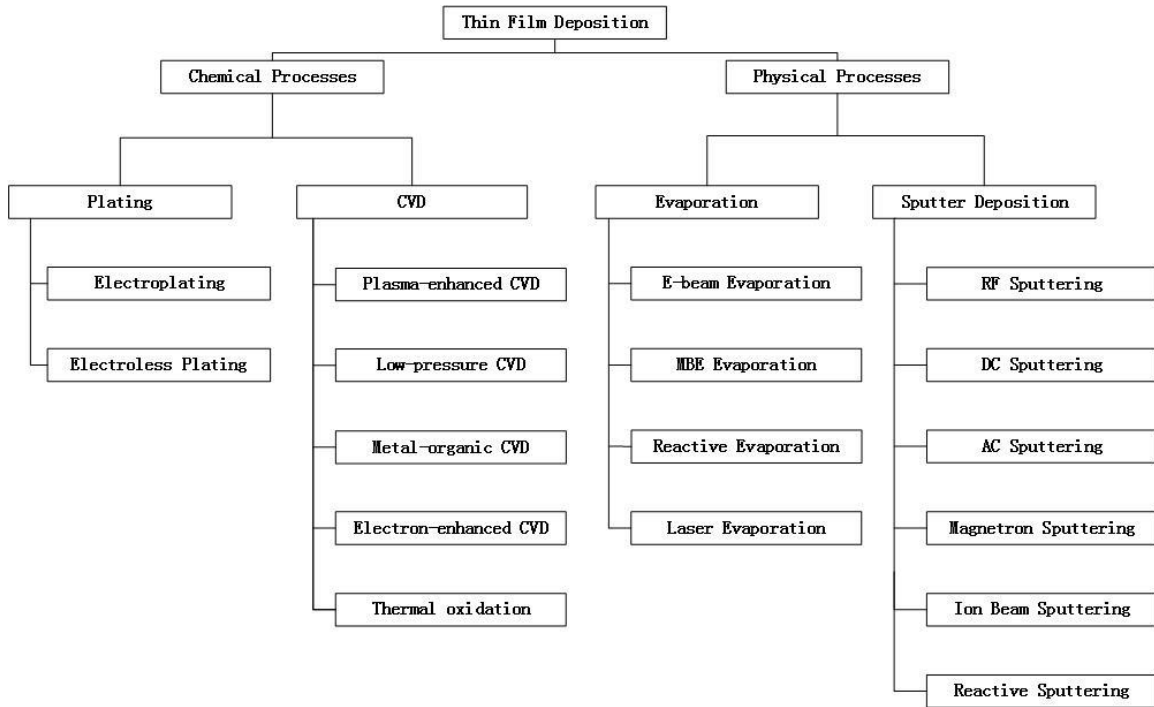
Figure 2.1 Classification of Most Common Deposition Process [30]

In physical vapor deposition (PVD) process, the solid material to be deposited is physically converted into the vapor phase. The vapor phase is then transported from the target to the substrate through a reduced pressure region. Finally, the vapor condenses on the surface of the substrate to form thin film layer. This PVD process is commonly used to produce thin film metal layers.

In chemical vapor deposition (CVD) process, a solid thin film is formed by a material synthesis process in which several vapor reactants react with each other. The chemical vapor reaction is the most essential part of this method. This is why all the parameters related to the reaction of reactants need to be carefully controlled. The CVD process is usually used to produce insulating layers.

Besides PVD and CVD, the growth of inorganic thin films from liquid phases by chemical reactions is accomplished primarily by electrochemical processes (which include

anodization and electroplating), and by chemical deposition processes (which include reduction plating, electroless plating, conversion coating, and displacement deposition).

2.2   Thin Film Metallization

In this project, Ti/TiW/Au was selected as the thin film metallization. As we mentioned in Chapter 1, the bottom layer Ti provided good adhesion to the substrate; the composition of TiW layer was 10%Ti: 90%W and served as the diffusion barrier layer; the Au was the conductive layer. Ti and Au would interdiffuse if in direct contact at 300 ℃. The e-beam and sputtering system we used in this project was a CHA Industries MARK-50. The thin film metallization process began with a 5min in-situ ion gun cleaning process to clean the substrate, then e-beam evaporation of the Ti (250Å), sputtering of the Ti:W (500Å), ion milling for 1min and e-beam evaporation of the Au (500Å). All the metal layers were deposited in sequence and without breaking vacuum.

Evaporation and sputtering are two of the most important physical vapor deposition (PVD) methods, especially for multilayer thin film metal deposition. In e-beam evaporation, thermal energy is applied to the Ti or Au target by heating it with a direct electron beam. As the target material reaches it boiling point, individual atoms fly off the surface and spread in random directions. The whole process is carried out in a vacuum chamber. In this way, atoms can reach the surface of the substrate before colliding with the gases in the atmosphere. The residual pressure in the deposition system, the composition of the residual gases, the temperature of the source, the temperature of the substrate, the distance from source to substrate, and the duration of the deposition are the most important parameters for e-beam deposition [29]. A schematic diagram of an e-beam evaporation system is shown in Figure 2.2 [31].
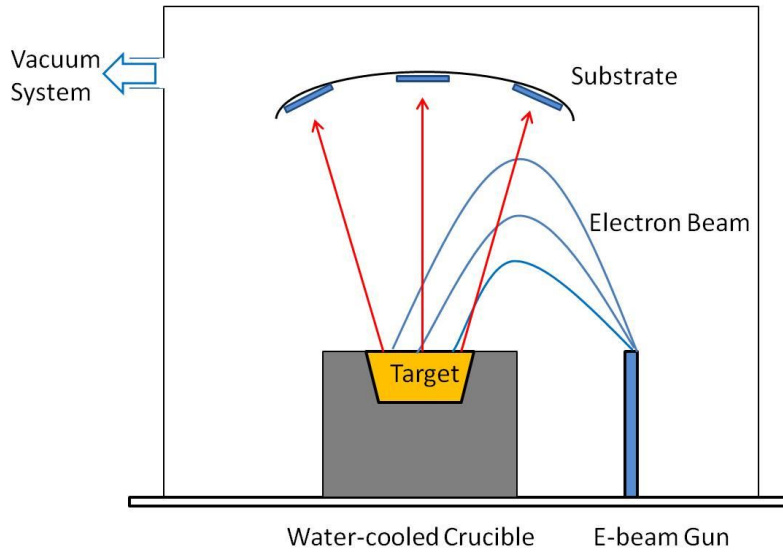
Figure 2.2 Schematic Diagram of an E-beam Evaporation System [31]

In sputtering, the target material, Ti and W, are negatively charged as the cathode in a vacuum chamber filled with inert gas (such as argon). By applying a high voltage, argon atoms enter a plasma state (Ar+ and e-) and the Ar+ ions quickly move toward the target. Under this situation, atoms at the surface of the target material are ejected or knocked out of the surface and travel around the chamber, sometimes steered by electric or magnetic fields. These sputtered atoms finally form a thin film layer on the substrate. An advantage of sputtering is that source materials with low vapor pressure at practical temperatures can be deposited. A schematic diagram of sputtering deposition system is shown in Figure 2.3 [31].
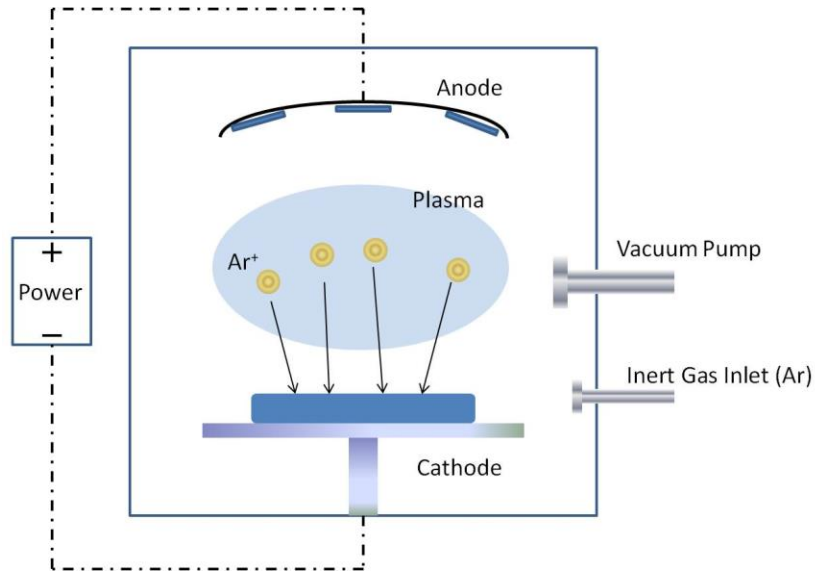
Figure 2.3 Schematic Diagram of Sputtering Deposition System [31]

2.3   Gold Electroplating

As we mentioned in Chapter 1, gold is the most widely used conductor material in thin film metallization, because of its excellent electrical characteristics and high resistance to corrosion and oxidation. However, it is not cost effective to deposit the whole gold layer for wire bonding or stud bumping by e-beam system or sputtering system. A practical way is to deposit a thin seed layer of gold which is only a few hundred angstroms thick. Then pattern the seed layer with photoresist and increase the thickness of gold by electroplating.

In the electroplating process, stress in the gold layer is a critical processing and reliability concern. It usually causes delamination in multilayer structure. The stress in the gold layer is related to plating current density and bath temperature. More details of the gold electroplating in this project will be discussed in Section 2.5 Thin Film Substrate Fabrication.

2.4   **Thin Film Dielectric Layer**

In this project, silicon nitride (Si_3N_4) was selected as the dielectric layer and deposited on the substrate by plasma enhanced chemical vapor deposition (PECVD). In the PECVD system, electrical energy is used to generate a plasma region between two electrodes. In this region, the energy of the plasma is transferred into the gas mixture and brings the gas mixture into a highly excited state. Gas atoms react with each other and form a solid film on the surface of the substrate. With the help of plasma energy, the whole reaction can be maintained at a relatively low temperature. This is a major advantage of PECVD. A schematic diagram of PECVD system is shown in Figure 2.4 [32].
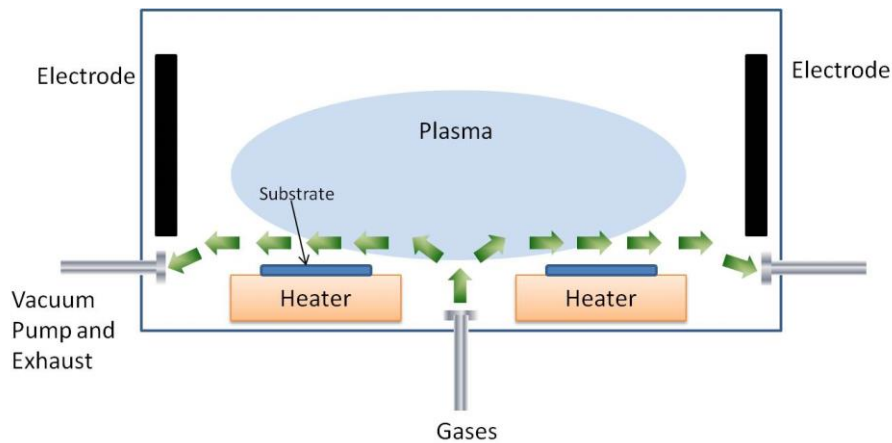
Figure 2.4 Schematic Diagram of PECVD System [32]

2.5   **Thin Film Substrate Fabrication**

The fabrication process of the bottom metal layer is as follows:

● Seed layer deposition: The thin film substrate fabrication process began with a 5 min in-situ ion gun cleaning process, then e-beam evaporation of the Ti (250Å), ion cleaning the surface of TiW target for 5min, sputtering of the Ti:W (500Å), 1min ion gun cleaning of TiW surface and e-beam evaporation of the Au (500Å). All of the metal layers were deposited in sequence and without breaking vacuum. The ion gun

23

cleaning process is shown in Figure 2.5 and TiW sputtering process is shown in Figure 2.6. Details of ion gun cleaning and metal deposition are shown in Table 2.1 and Table 2.2.

Figure 2.5 Ion Gun Milling Process in CHA Industries MARK-50
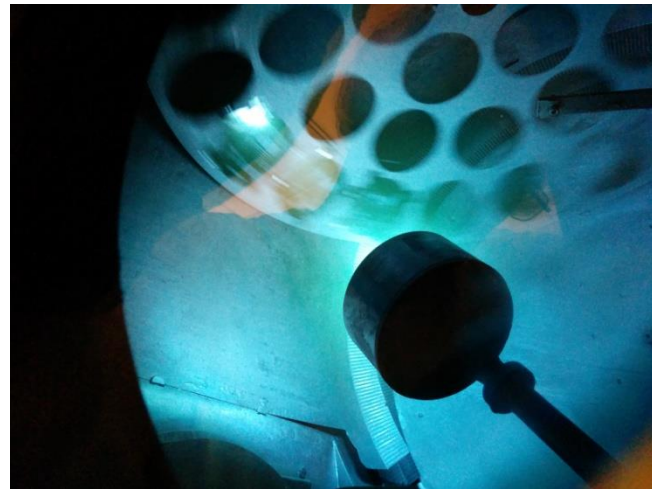
Figure 2.6 TiW Sputtering Process in CHA Industries MARK-50

Table 2.1 Parameters of Ion Gun Cleaning

Cathode Filament Current	5.46A
Discharge Current	3.41A
Discharge Voltage	55.4V
Beam Current	200mA
Beam Voltage	994V
Accelerator Current	2mA
Accelerator Voltage	100V
Neutralizer Emission Current	258mA
Filament Current	4.09A

Table 2.2 Metal Deposition Rates

Ti Deposition Rate	2Å/sec
TiW Deposition Rate	1Å/sec
Au Deposition Rate	2Å/sec
Vacuum Level	3.0E-6torr

- Substrate cleaning: The substrate with seed layer was immersed into 5% hydrocholoric acid for 10sec then briefly rinsed with DI water. This ensures a clean surface without any oxide. Then the substrate was baked at 120 ℃ for 20min. This dehydrating baking step was required to drive off any moisture before photoresist coating.

- Priming: As a noble metal, adhesion to gold is always a challenge. This problem may lead to photoresist crack or photoresist lift-up issues during the gold plating process which can cause gold underplating, as shown in Figure 2.7. In order to increase the adhesion, an adhesion promoter (SIPR-PR20) was spin coated on the substrate at 3000rpm for 20sec. Then the substrate was soft baked at 130 ℃ for 120sec on a hot plate. With this adhesion promoter, a much better gold plating result was achieved, as shown in Figure 2.8.
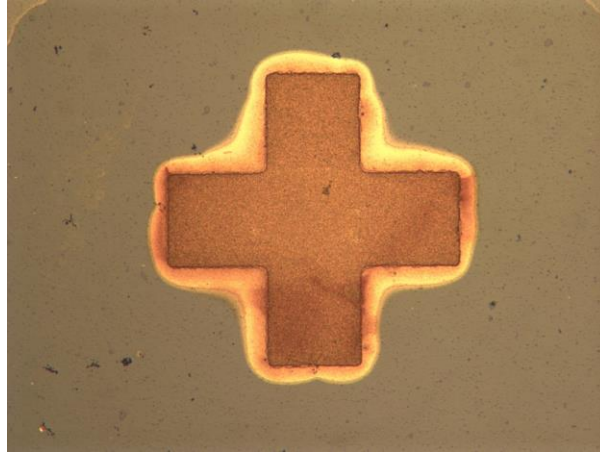
Figure 2.7 Alignment Mark with Au Underplating
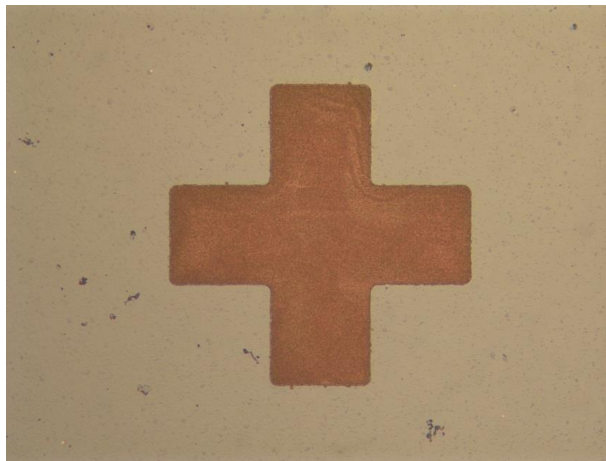
Figure 2.8 Alignment Mark without Au Underpalting

- <u>Spin coating:</u> After cleaning and priming, Photoresist AZ 9245 was spin coated on the substrate at 1700rpm for 30sec. After this, the substrate was soft baked on a hotplate at 110°C for 2 minutes. The total thickness of photoresist AZ 9245 on the substrate was 6.5μm.

- <u>Exposure:</u> The substrate was exposed in Karl Suss MA6 Mask Aligner for 20sec.

- <u>Development:</u> After exposure, the substrate was immersed into 33% AZ400K developer for 1.5min and then rinsed with DI water.

- Striping adhesion promoter: Prior to gold plating, the adhesion promoter layer in the open areas was removed with 20sec O_2 and CF_4 plasma in an STS MESC MULTIPLEX Advanced Oxide Etcher. The gas flows were O_2 with 30sccm and CF_4 with 6sccm. This ensures nothing would prevent gold ions from attaching to the surface of the seed layer.

- Gold electroplating: Gold electroplating was performed in two separate steps. Prior to the gold electroplating process, the substrate was first electroplated in pre-plating solution (Orostrike C, supplied by TECHNIC, Inc.) at 40 °C. This solution is an acid gold strike bath which can provide excellent adhesion between the thin film Au layer and the electroplated gold layer. In this process, the substrate was connected to the cathode of a GS200 DC Voltage/Current Source and a piece of platinum mesh was connected to the anode. Current flowing between the two electrodes drives Au ions to the cathode, depositing on the substrate. A magnetic stir bar was used to improve the solution's uniformity and to reduce bubbles generated in the plating process. The schematic of a typical electroplating system is shown in Figure 2.9. As we mentioned before, the internal stress in the Au layer strongly depends the plating current density. An excessive plating rate usually leads to high internal stress, rough surface, large grain and metal peeling-off. This was why the plating current density was set to 1-2 amps per square foot (ASF), a relatively low current density.
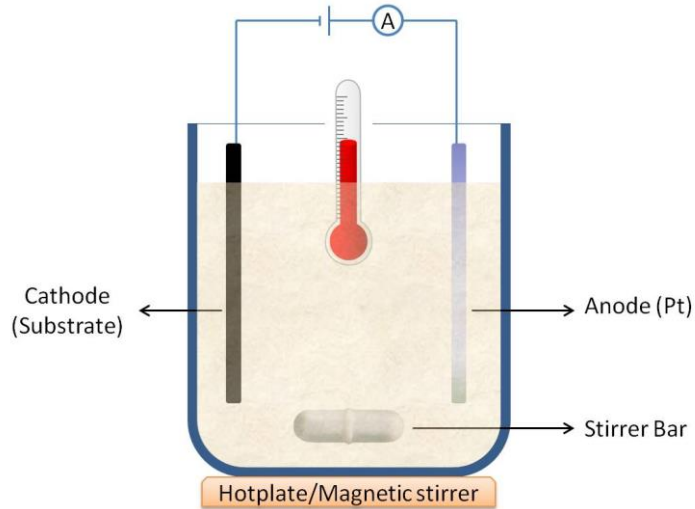
Figure 2.9 Schematic of a Typical Electroplating System

With a thin layer of Au depositing on the substrate, the substrate was rinsed in DI water and immersed into a neutral pure gold plating solution, Techni-Gold 434 HS. This solution can be used to plate semiconductor components, ceramic packages, multi-chip modules, connectors, contacts or a variety of electronic components where high purity gold deposits are necessary [33]. The plating set-up was the same as the one used for pre-gold plating. During plating, the solution temperature was set to 50°C and the plating current density was 1.0ASF. A total thickness of 1.5μm gold is electroplated on the substrate.

● Cr deposition: Once the gold plating was completed, 1min ion cleaning was performed on the substrate and 200Å of Cr was deposited on the substrate directly before removing the photoresist. This thin layer of Cr served as the adhesion layer between the Au and PECVD nitride dielectric layers. Then all of the photoresist was stripped off with acetone. The substrate was then cleaned with isopropyl alcohol and DI water.

● Removing seed layer: At the beginning of this project, the Au seed layer was removed with Gold Etchant type TFA in about 30sec. After that, it took 15min to remove all of

28

the TiW layer with 30% hydrogen peroxide. Finally, the Ti was removed with a 30sec

BOE wet etching process.

However, when a multilayer board was fabricated with this process, the electrical

testing results showed that there were electrical shorts in the cross-over area between

the bottom metal traces and top metal traces. In order to identify the exact location of

the short, a break down test was performed on the multilayer structure. More details

about this break down testing are discussed in Chapter 4, Section 4.4. According to the

test results, the root cause of electrical short on the edge was that after electroplating

the edge of the bottom trace became very rough and some spikes on the edge penetrated

the dielectric layer and caused the electrical short. As shown in Figure 2.10, the edge

of the trace was sharp and the height of edge was larger than that of the center.
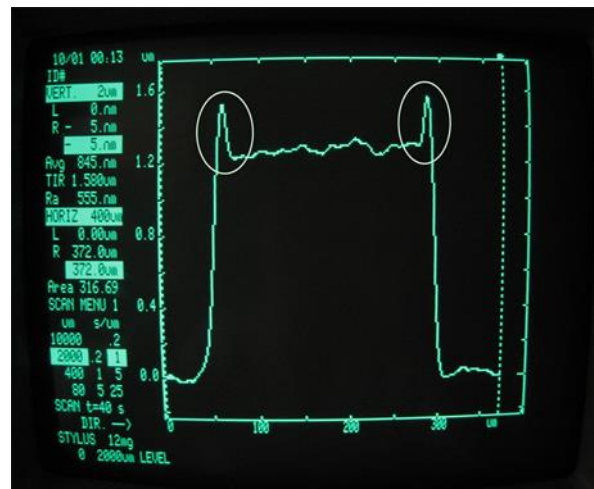
Figure 2.10 Profilometer Image of Plating Wings

In order to solve this plating wings issue, the gold layer was over etched when the

seedlayer was removed. Instead of 30sec, the gold layer was etched for 300sec in Gold

Etchant type TFA. This process perfectly removed the plating wings, even with a Cr

layer on top of the Au layer, as shown in Figure 2.11.

29
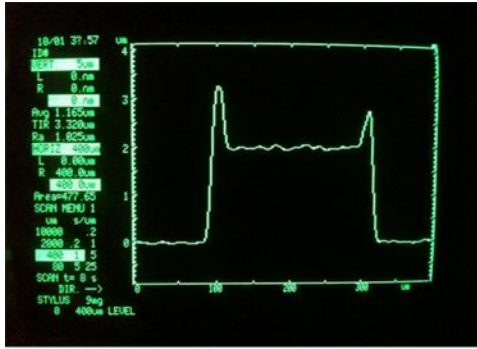
Before over-etching   After over-etching
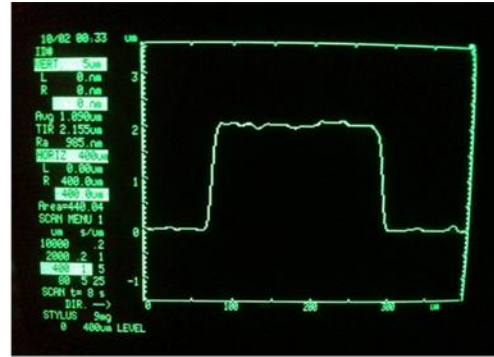
Figure 2.11 Profilometer Image of Plating Wings Before and After Over-etching

The EDS dot map result, as shown in Figure 2.12, indicated that the 200Å Cr layer on top was still uniform and constantly covered the pattern area. No overhang of Cr was observed on the edge of the trace.
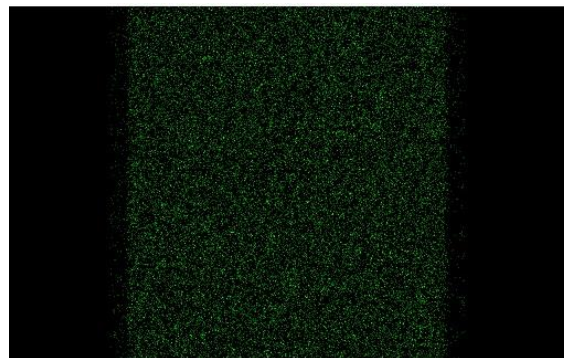
Cr Ka1

Figure 2.12 The EDS Dot Map of Cr Layer

● SST vacuum baking: In the gold electroplating process, hydrogen was available from the water in the plating solution. Because the size of hydrogen atom is much small then the size of a gold atom, the hydrogen can migrate into the crystal lattice of the gold during electroplating of the 1.5μm gold. When the gold layer was covered with dielectric layer and the environment temperature was raised to 300℃, the hydrogen diffused out of the gold layer and formed blisters between the metal and dielectric

layers, as shown in Figure 2.13 and Figure 2.14. In order to address this issue, the substrate was vacuum baked at 150 ℃ with a 8×10^{-7} torr vacuum for 14hr to remove entrapped hydrogen.
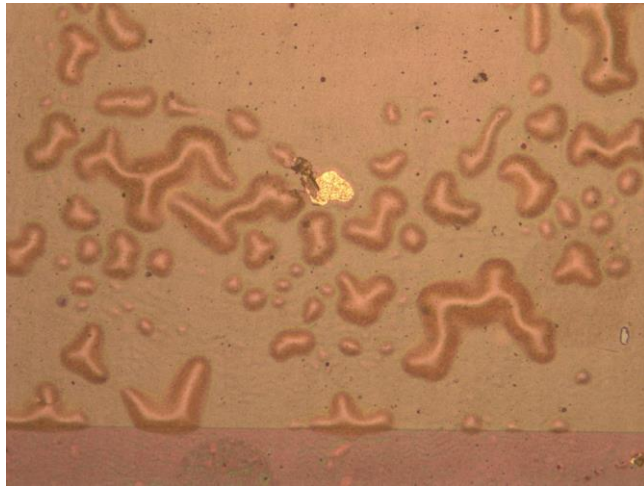
Figure 2.13 Blisters under Dielectric
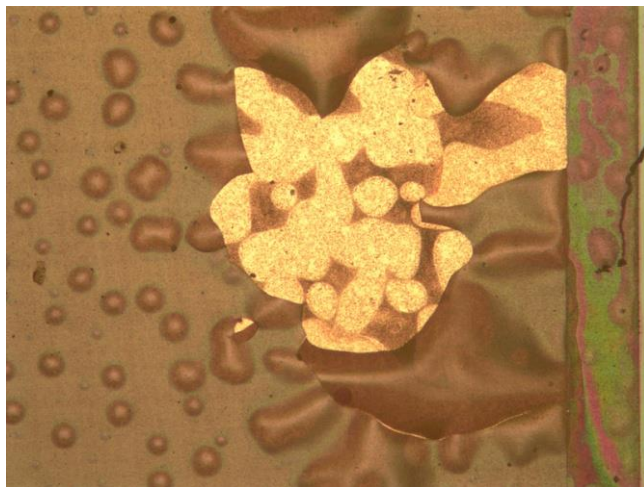
Figure 2.14 Dielectric Breakup Caused by Blisters

The fabrication process of the dielectric layer was as follows:

- <u>PECVD nitride deposition</u>: The dielectric layer fabrication process began with a 1 min in-situ ion gun cleaning of the substrate in the e-beam system. Then 1.5μm silicon nitride (Si_3N_4) was deposited on the substrate with an STS Multiplex PECVD system.

In this project, the deposition pressure in the chamber was 550mTorr and the gas flows were:

N_2: 1000sccm

NH_3: 20sccm

2%SiH_4: 500sccm

The deposition temperatures were: top heater 250℃ and bottom heater 300℃, the RF power was 60W and the deposition time was 5min. The insulator layer was ~1.5μm thick.

- Substrate cleaning: The substrate with dielectric layer was immersed into 5% hydrocholoric acid for 10sec then briefly rinsed with DI water. Then the substrate was baked at 120℃ for 20min. This dehydration baking step was required to drive off any moisture before coating.

- Priming: After the dehydration baking, the substrate was exposed to gaseous Hexamethyldisilazane (HMDS) for 5min in a desiccator. HMDS is used to augment the photoresist adhesion to the silicon nitride.

- Spin coating: After cleaning and priming, Photoresist AZ 4620 was spin coated on the substrate at 3000rpm for 30sec. After this, the substrate was soft baked over a hotplate at 110℃ for 1 minute and contact baked on the hotplate for another 1 minute. The total thickness of photoresist AZ 4620 on the substrate was 6μm.

- Exposure: The substrate was exposed with a Karl Suss MA6 Mask Aligner for 4 cycles. Each cycle consists of 4sec UV exposure and 30sec waiting time.

- Development: After exposure, the substrate was immersed into 33% AZ400K developer for 40sec and then rinsed with DI water.

- Dielectric etching: Once properly patterned, the substrate was placed in buffered oxide etch (BOE) solution. The exposed insulator was quickly etched. The etching time depends on the area of exposed insulator. The substrate was the rinsed with DI water.

The fabrication process for the top metal layer was exactly the same as the bottom metal layer except for the Cr deposition process.

2.6   Adhesion Testing

As thin film is widely used in electronics devices, the reliability of these devices highly relies on how well the thin film sticks to the substrate and each other. In this project, the thin film circuit must maintain good adhesion in a high temperature and high vibration environment. To achieve this requirement, four kinds of adhesion testing vehicles were designed and fabricated to evaluate the adhesion of thin film material.

These four adhesion testing vehicles included adhesion testing of conductor on AlN, dielectric on AlN, conductor on dielectric and dielectric on conductor. All of these test vehicles were fabricated on 3 inch by 3 inch AlN substrate with the fabrication process described. A dielectric on metal test sample along with its mask is shown in Figure 2.15 and Figure 2.16. Details about the pads dimension are shown in Table 2.3.
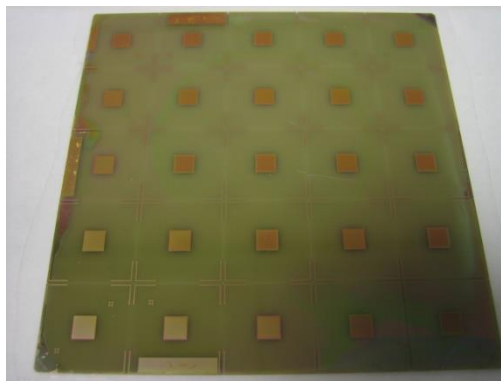
Figure 2.15 Dielectric on Metal Adhesion Test Vehicle
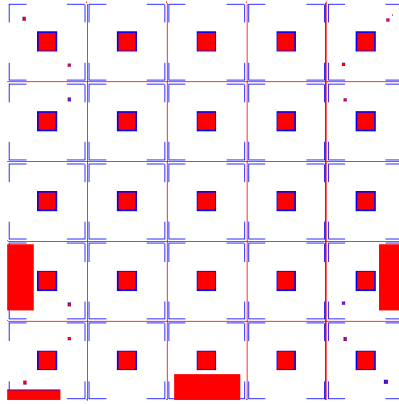
Figure 2.16 Mask of Dielectric on Metal Adhesion Test Vehicle

Table 2.3 Pad Demension of Adhesion Test Configuration

Conductor on AlN	Conductor (130mil $\times$ 130mil)
Dielectric on AlN	Dielectric (130mil $\times$ 130mil)
Conductor on Dielectric	Conductor (130mil $\times$ 130mil) on Dielectric (150mil $\times$ 150mil)
Dielectric on Conductor	Dielectric (130mil $\times$ 130mil) on Conductor (150mil $\times$ 150mil)

Usually, the adhesion testing methods have been classified into three categories: nucleation methods, mechanical methods and miscellaneous techniques [34]. In our research, a stud pull test was selected. Once the test sample was fabricated, the substrate was diced into 25 individual test coupons (0.6 inch by 0.6 inch). Aluminum studs with epoxy-coated ends from Quad Group (Spokane, WA) were adhered to the test pad and the AlN substrate was attached and cured to a ceramic plate coated with epoxy to reinforce the substrate. The pull stud end had a diameter of 106 mils and the epoxy coated on it had a tensile strength of 10000 to 13000 psi. Based on the pull stud diameter and epoxy tensile strength, the epoxy would start to fail when the pull strength reached 88.2-114.7lb (7-9.1kg/mm^2). A clamp was used to clamp the part and the ceramic plate together during epoxy cure at 150 ℃ for an hour, as shown in Figure 2.17. The adhesion test was conducted

at room temperature on samples as built and samples after thermal aging (300 ℃ for 500, 1000, 1500, and 2000 hours) using a Sebastian-V mechanical tester. The pull testing is illustrated in Figure 2.18 and Figure 2.19.

Figure 2.17 Adhesion Testing Sample
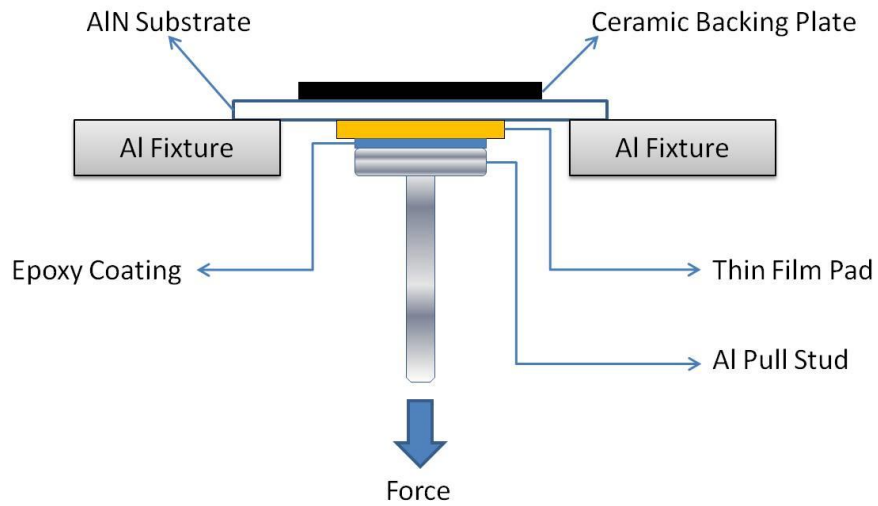
Figure 2.18 Illustration of Pull Testing
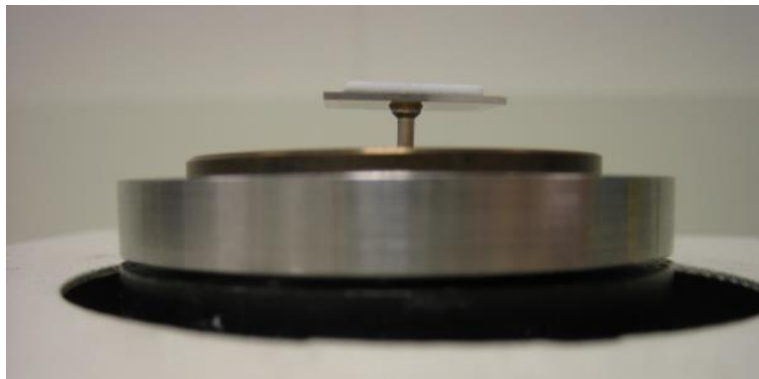
Figure 2.19 Adhesion Testing Sample on Pull Tester

For metal on AlN and dielectric on AlN, high adhesion was maintained through 2000h aging at 300 ℃. All failures were in the epoxy. In the test, 10 data points were obtained at each test interval. The pull strength results of metal on ceramic and dielectric on ceramic as a function of aging time at 300 ℃ are plotted in Figure 2.20. The box plots contain the following information: the bottom end and the top end represent the 25th and 75th percentile. The line in the box is the median. The whisker represents the extent of the data range not considered statistically an outlier. The small dots in the plot indicate data points were statistically considered outliers.
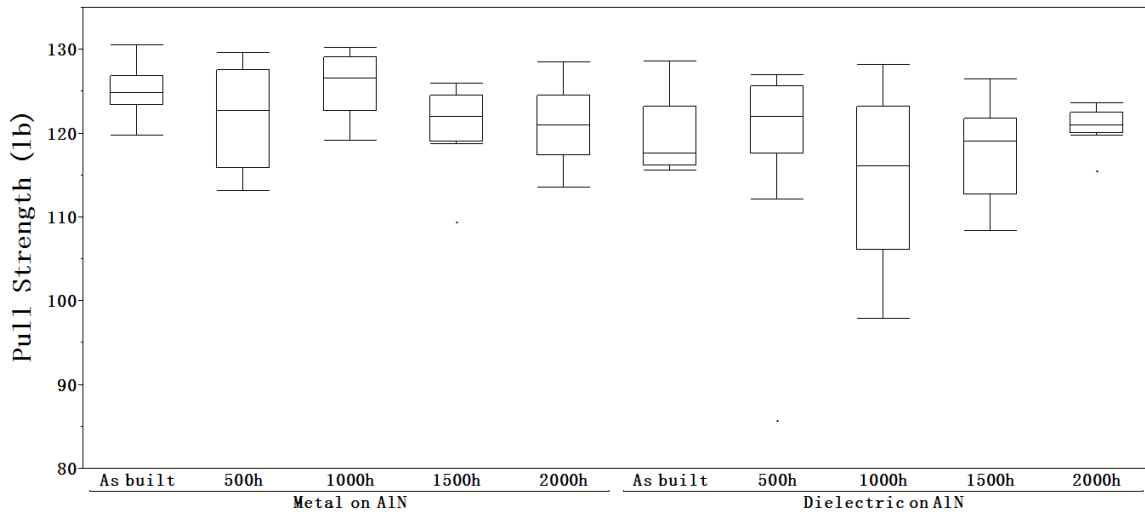
Figure 2.20 Pull Strength of Metal on AlN and Dielectric on AlN as a Function of Aging Hour at 300 ℃

For metal on dielectric pull testing, the pull strength of the sample was very high through 2000h aging at 300 ℃. A very small area of Au was pulled off on several samples at every test interval, as shown in the Figure 2.21. This pulling off phenomenon was totally random and has no obvious relation with aging time. For dielectric on metal pull testing, the pull strength was high through all 2000h aging at 300 ℃. In initial pull testing on samples as built, a small area of both layers was pulled off on some samples. After 500h

aging, all failures were in the epoxy at all subsequent test intervals. The pull strength results of metal on dielectric and dielectric on metal as a function of aging time at 300 ℃ are plotted in Figure 2.22.

Figure 2.21 Metal Surface after Pull Testing
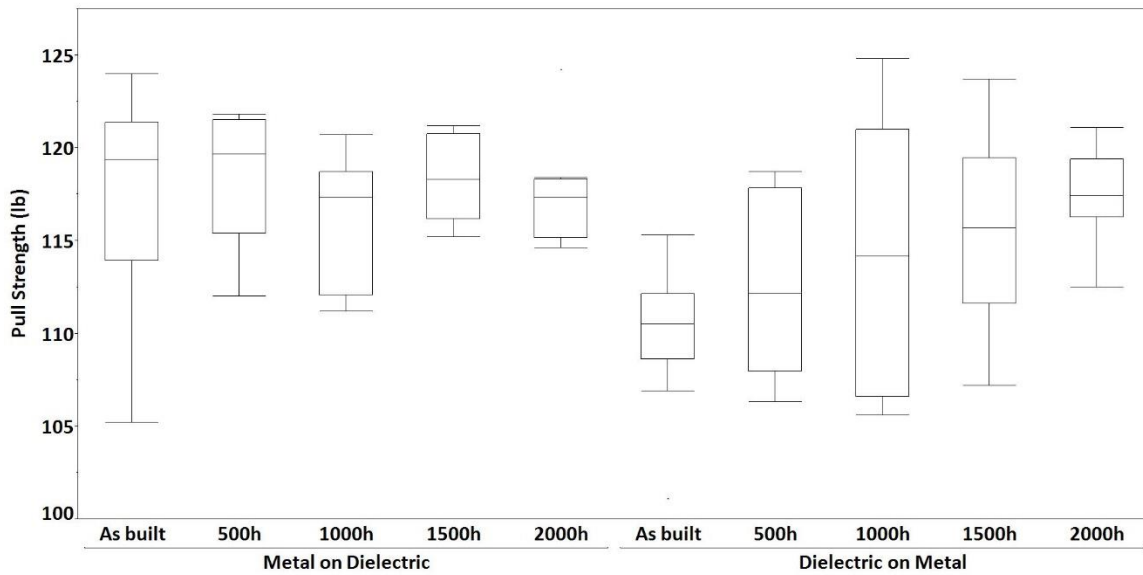
Figure 2.22 Pull Strength of Metal on Dielectric and Dielectric on Metal as a Function of Aging Hour at 300 ℃

2.7 Conductor Resistance Testing

As we mentioned before, thin film multilayer structures have the risk of undergoing severe interdiffusion at high temperature. For Ti and Au, the diffusion process may produce the intermetallic compounds AuTi, Au_4Ti, Au_2Ti and Ti_3Au during annealing at over 300 ℃ and if Ti diffuses through Au up to the surface, TiO_2 may form. All of these can cause an increase in electrical resistance [35]. In order to make sure that the TiW layer indeed reduced or stops interdiffusion between Ti and Au, a serpentine pattern was designed to monitor the resistance change after high temperature aging. The pattern featured 20mil line and space, with a total length of 4000mil. It also had pads for 4-point Kelvin resistance measurement, as shown in Figure 2.23. A real sample is shown in Figure 2.24. The average resistance as a function of aging time at 300 ℃ is plotted in Figure 2.25. No increase in resistance was observed, indicating no Ti-Au interdiffusion.
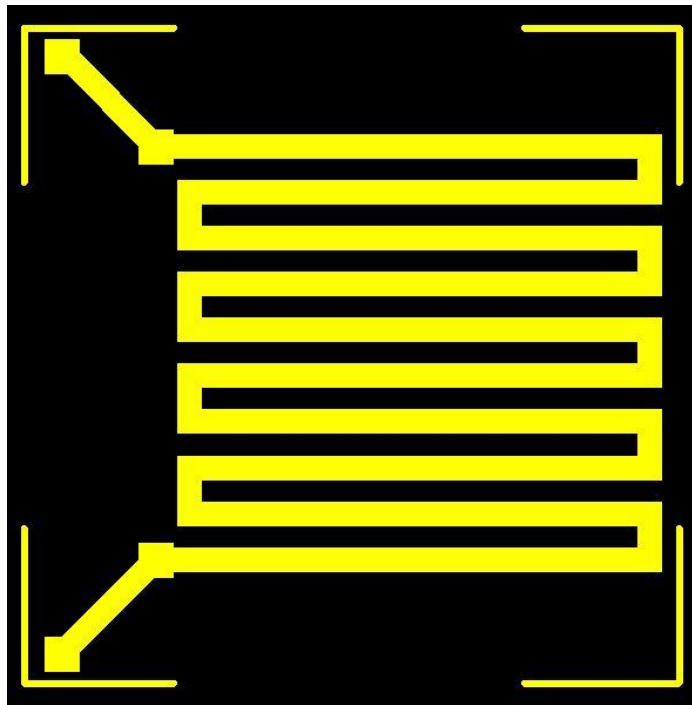
Figure 2.23 Schematic of Serpentine Pattern
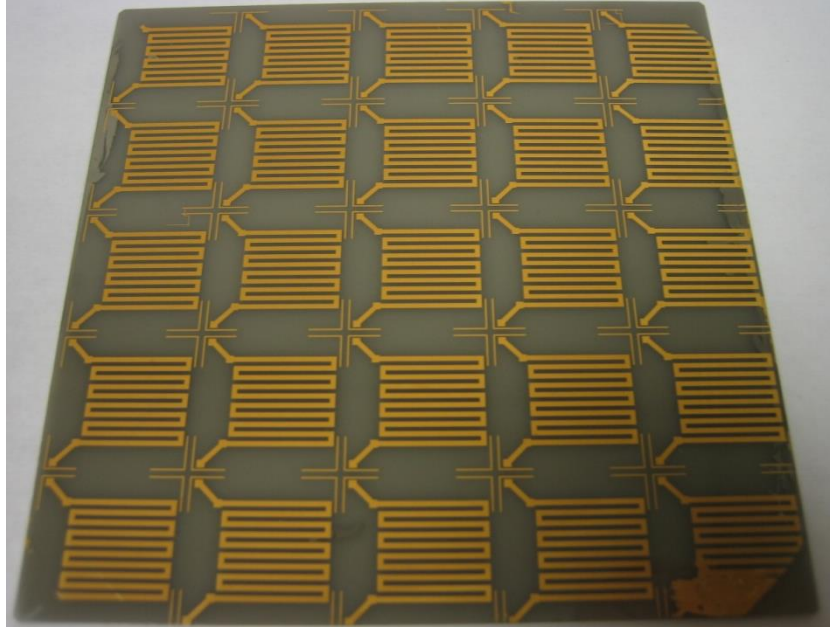
Figure 2.24 Conductor Resistance Testing Vehicle
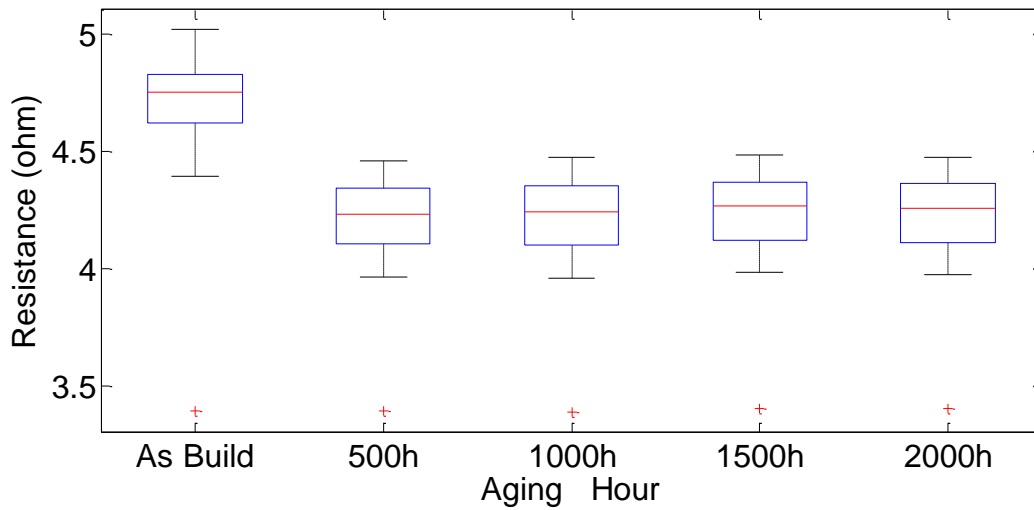
Figure 2.25 Conductor Resistance as a Function of Aging Hour at 300 ℃

2.8 Electrical Testing

The electrical properties and reliability of the PECVD Si_3N_4 at 300 ℃ are very important for the digital circuit's performance. In order to characterize the electrical properties of the dielectric, a multilayer electrical testing vehicle was designed and fabricated on a 3inch by 3inch AlN substrate. The test structures consisted of 7 capacitors,

6 comb patterns, 3 continuity test patterns and a cross-over pattern. These structures are

labeled in Figure 2.26 and a fabricated substrate is shown in Figure 2.27. These structures

provided leakage current measurement, capacitance and dissipation factor measurement

and continuity testing.
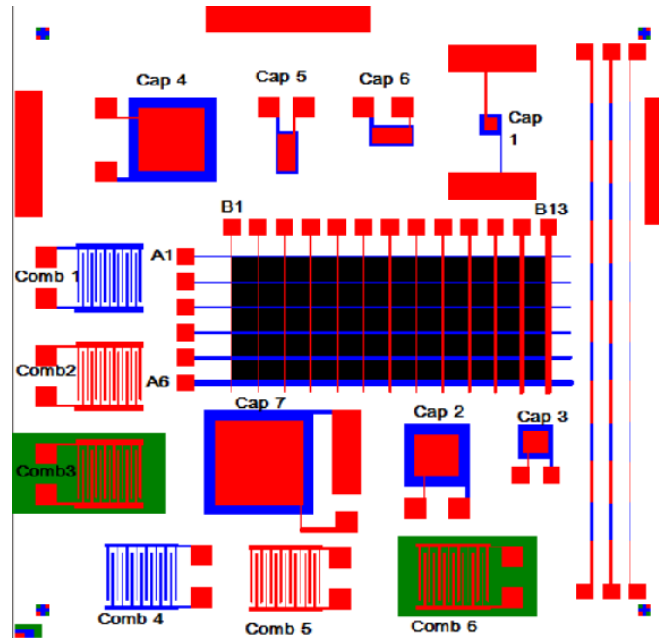
Figure 2.26 Configuration of Electrical Testing Vehicle
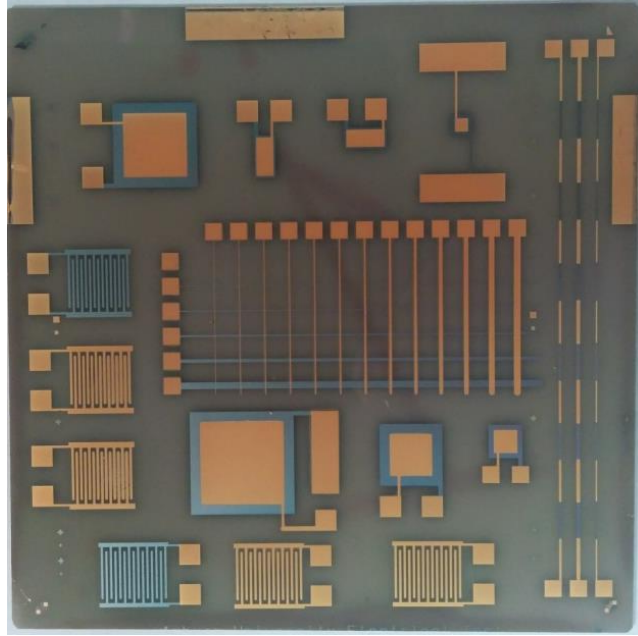
Figure 2.27 Electrical Testing Vehicle Substrate

2.8.1   Leakage Current Measurement

The leakage current measurement was performed on capacitors, comb patterns and cross-over patterns. An HP 4146A Precision Semiconductor Parameter Analyzer applied 20V to the pattern and collected leakage current data, as shown in Figure 2.28. A Signatone Thermal Probing System was used to provide different testing temperatures from room temperature to 300 ℃, as shown in Figure 2.29.

Figure 2.28 HP 4146A Precision Semiconductor Parameter Analyzer

Figure 2.29 Signatone Thermal Probing System

For capacitors, the top electrode was designed a little smaller than the bottom electrode. This was meant to simplify alignment during fabrication. The size of the capacitors is shown in Table 2.4. The leakage current measurement was performed on samples as built and samples after thermal aging (300 °C for 500, 1000, 1500, and 2000 hours) at room temperature, 100 °C, 200 °C and 300 °C.

Table 2.4 Top Electrode Size of Capacitor

Capacitor	Size of Top Electrode
Cap1	60mil $\times$ 60mil
Cap2	200mil $\times$ 200mil
Cap3	110mil $\times$ 110mil
Cap4	300mil $\times$ 300mil
Cap5	80mil $\times$ 180mil
Cap6	180mil $\times$ 80mil
Cap7	400mil $\times$ 400mil

Due to the manufacturing defects in the fabrication process, capacitors with large electrodes had a relatively low yield. So only the data of Cap 1 was collected. The leakage current as a function of temperature at 20V bias for Cap 1 is shown in Figure 2.30. The leakage current was quit low in the initial testing, increased with temperature as expected.

The leakage current slightly decreased after 500h aging and became very stable and consistent after 1000h aging at 300 ℃.
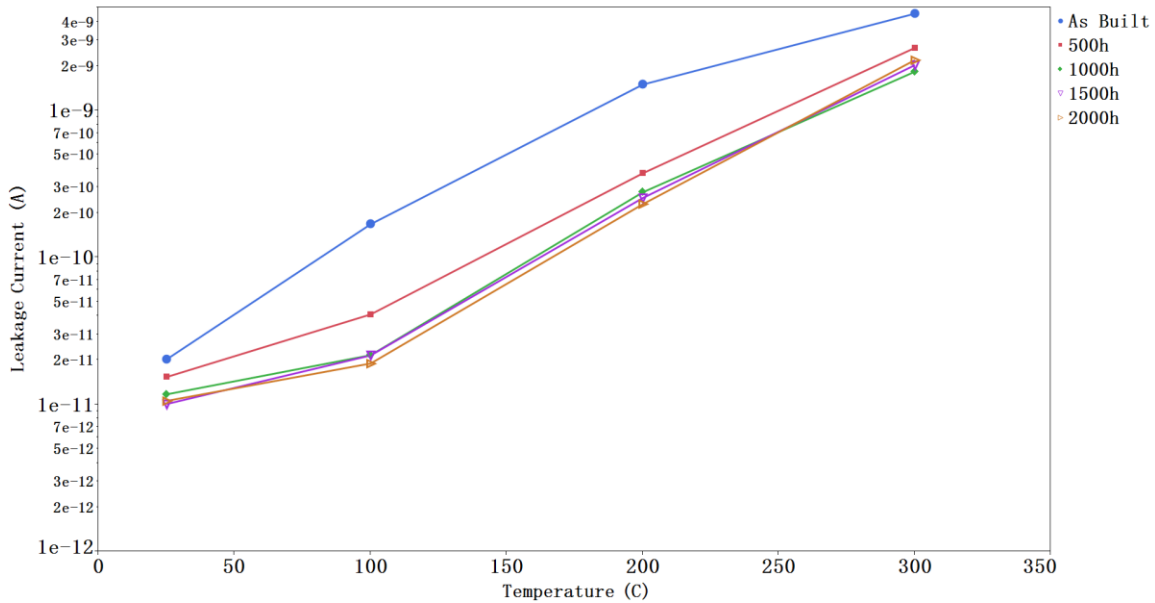
Figure 2.30 Leakage Current as a Function of Temperature at 20Vdc Bias for Cap 1
(Average of 6 Samples)

In the comb pattern, there were 7 lines on one comb and 8 lines on the other comb. Each line was 10mil wide, with a 10mil space for Comb1, Comb 2 and Comb 3 and 12mil space for Comb 4, Comb 5 and Comb 6. The length of each line was 250mil with 225mil overlapped to the near line, as shown in Figure 2.31. Totally, each comb pattern had 3150mil of overlapped length. For Comb 1 and Comb 4, the pattern was under the dielectric layer. For Comb 2 and Comb 5, the pattern was above the dielectric layer. For Comb 3 and Comb 6, the pattern was on the ceramic without dielectric on it, as shown in Table 2.5. The leakage current measurement was performed on samples as built and samples after thermal aging (300 ℃ for 500, 1000, 1500, and 2000 hours) at room temperature, 100 ℃, 200 ℃ and 300 ℃.

Figure 2.31 Comb Pattern

Table 2.5 Finger Spacing on Comb Pattern

Comb Pattern No.	Space Between Fingers	Structure
1	10mil	Pattern under Dielectric
2	10mil	Pattern above Dielectric
3	10mil	Pattern on Ceramic
4	12mil	Pattern under Dielectric
5	12mil	Pattern above Dielectric
6	12mil	Pattern on Ceramic

Figure 2.32 to Figure 2.37 plot measurement results of all 6 comb patterns. The leakage current of every comb pattern was very small. After 500h aging at 300℃, the leakage current decreased and remained relatively stable at subsequent test intervals.
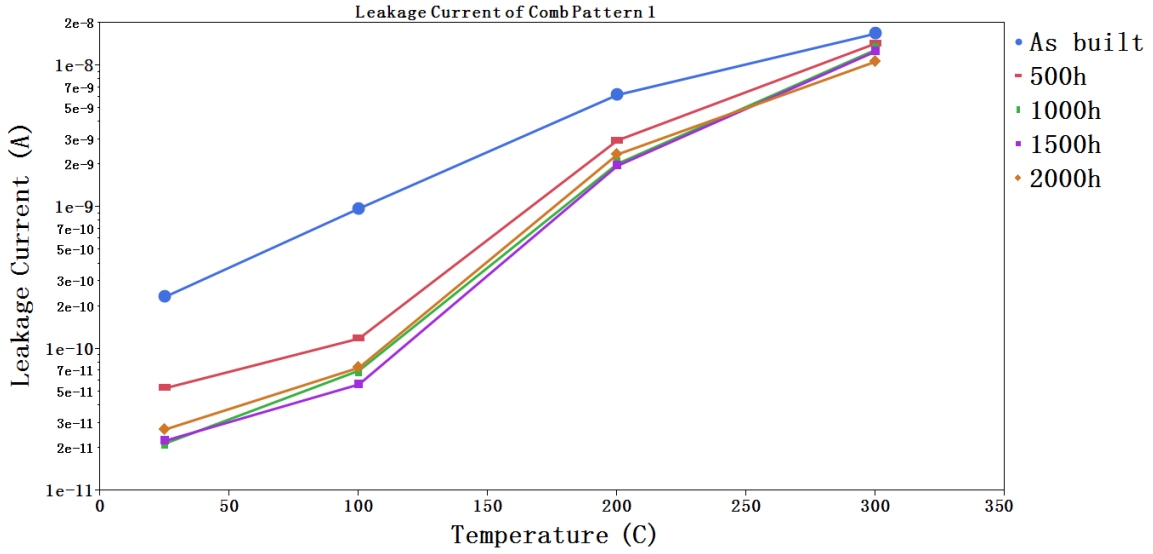
Figure 2.32 Leakage Current of Comb Pattern 1 at 20V Bias as a Function of
Temperature and Aging Hour
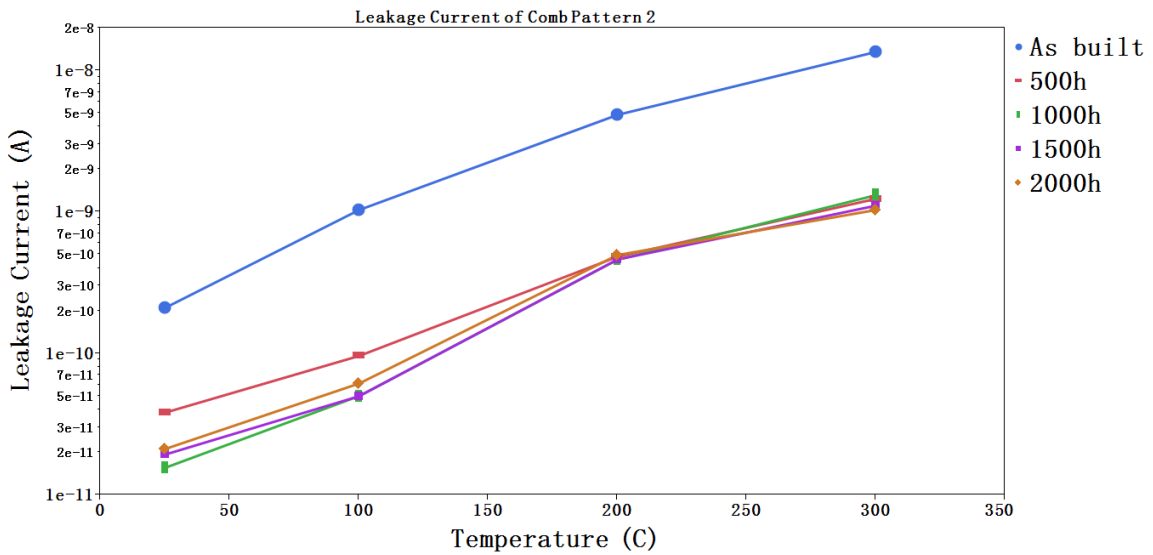
Figure 2.33 Leakage Current of Comb Pattern 2 at 20V Bias as a Function of
Temperature and Aging Hour

Figure 2.34 Leakage Current of Comb Pattern 3 at 20V Bias as a Function of
Temperature and Aging Hour

Figure 2.35 Leakage Current of Comb Pattern 4 at 20V Bias as a Function of
Temperature and Aging Hour

Figure 2.36 Leakage Current of Comb Pattern 5 at 20V Bias as a Function of Temperature and Aging Hour
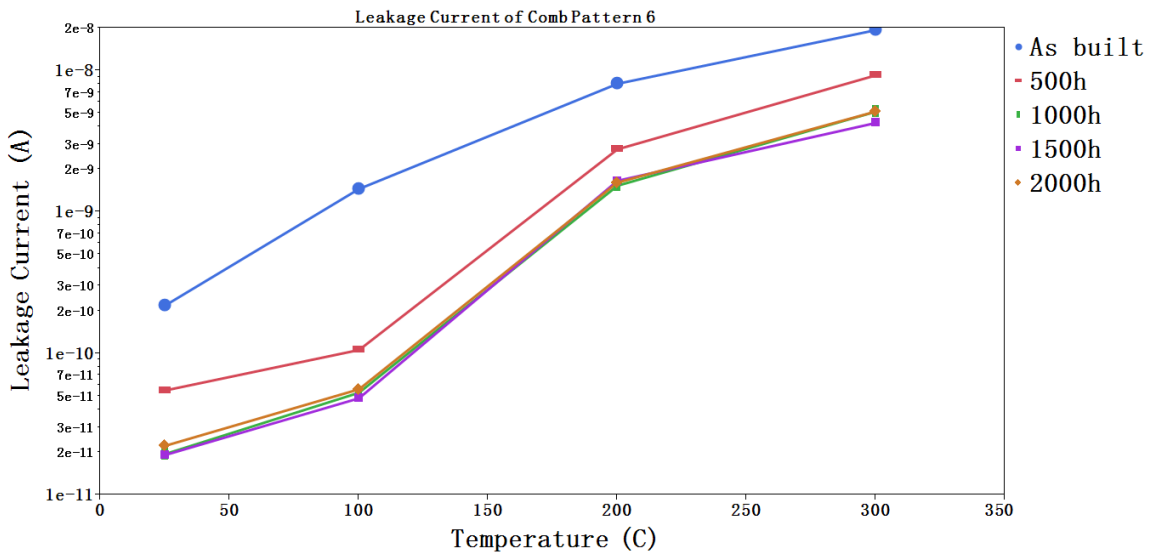
Figure 2.37 Leakage Current of Comb Pattern 6 at 20V Bias as a Function of Temperature and Aging Hour

The leakage current of all comb patterns after 2000h aging as a function of temperature is plotted in Figure 2.38. The plot indicates that patterns under dielectric (Group 1: Comb Pattern 1 and 4) have the largest leakage current at 300 ℃ and patterns above dielectric (Group 3: Comb Pattern 2 and 5) have the smallest leakage current at

47

300 ℃. There is not a big difference in leakage current between patterns with 10mil space and patterns with 12mil space.
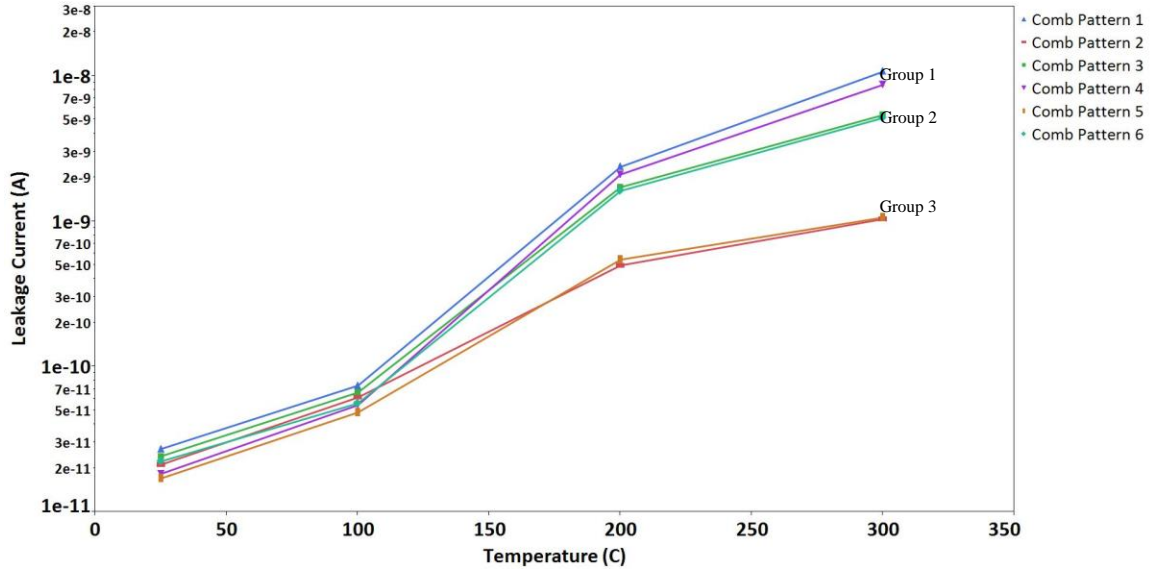
Figure 2.38 Leakage Current of Six Comb Patterns at 20V Bias after 2000h Aging as a Function of Temperature

The cross-over pattern was used to evaluate the leakage current in the cross-over area between the top and bottom traces, as shown in Figure 2.39. The width of trace A1 to A6 and trace B1 to B13 are shown in Table 2.6. The leakage current measurement was performed on cross-over area A1×B1, A4×B7 and A6×B13 on samples as built and samples after thermal aging (300 ℃ for 250, 500, 1000, 1500, and 2000 hours) at room temperature, 100 ℃, 200 ℃ and 300 ℃.
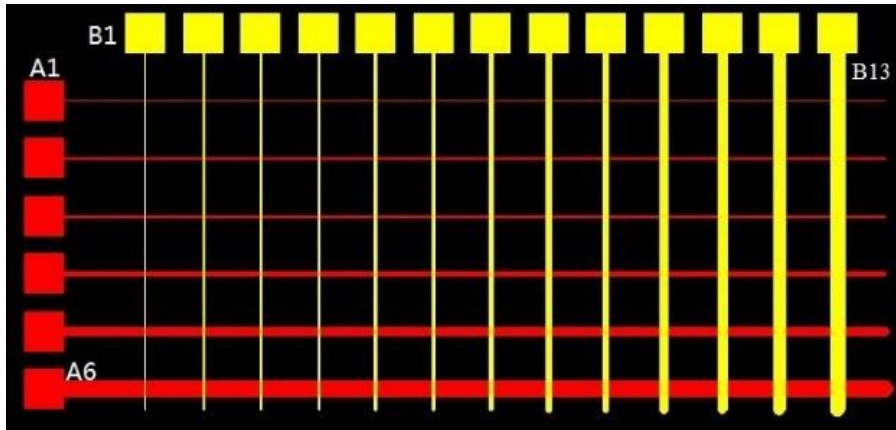
Figure 2.39 Cross-over Pattern

Table 2.6 Trace Width of Cross-over Pattern

A1	A2	A3	A4	A5	A6
1mil	2mil	4mil	8mil	16mil	32mil

B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13
1mil	2mil	3mil	4mil	5mil	6mil	8mil	10mil	12mil	16mil	20mil	25mil	30mil

Figure 2.40 to Figure 2.42 plot measurement results of all 3 cross-over areas. The leakage current of every cross-over pattern was very small. After 500h aging at 300 ℃, the leakage current decreases and remains relatively stable at subsequent test intervals.
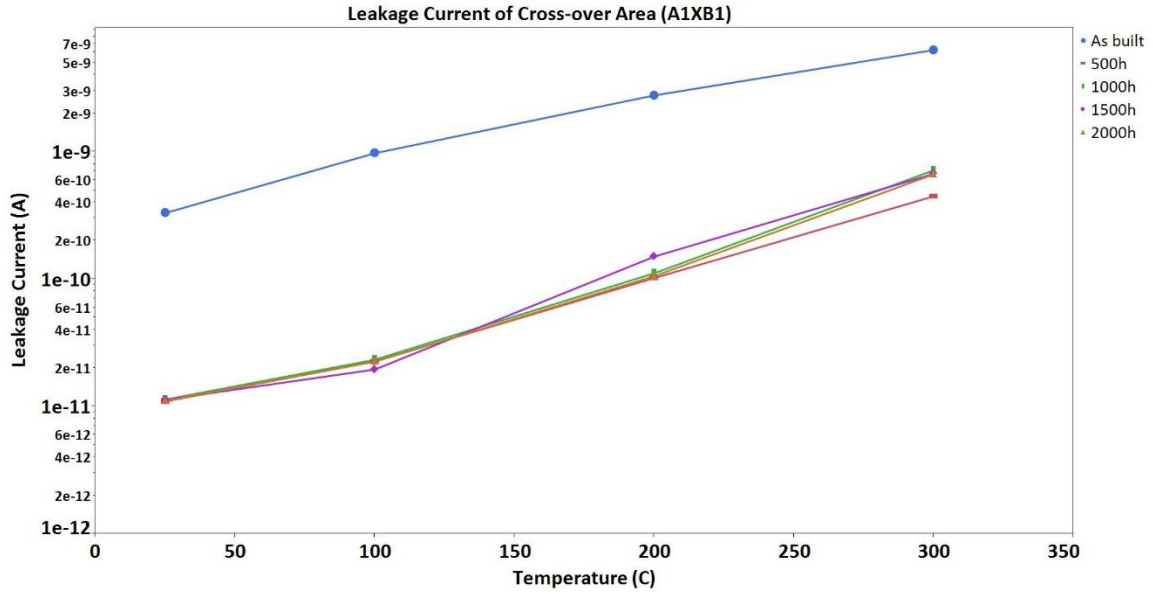
Figure 2.40 Leakage Current of Cross-over Area (A1XB1) at 20V Bias as a Function of Temperature and Aging Hour
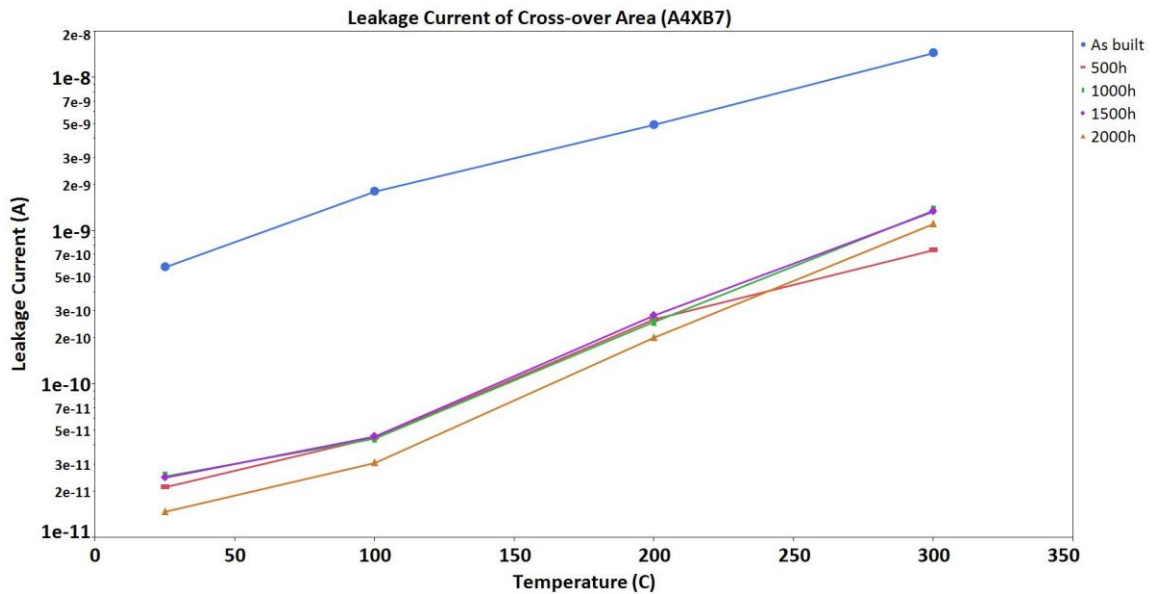
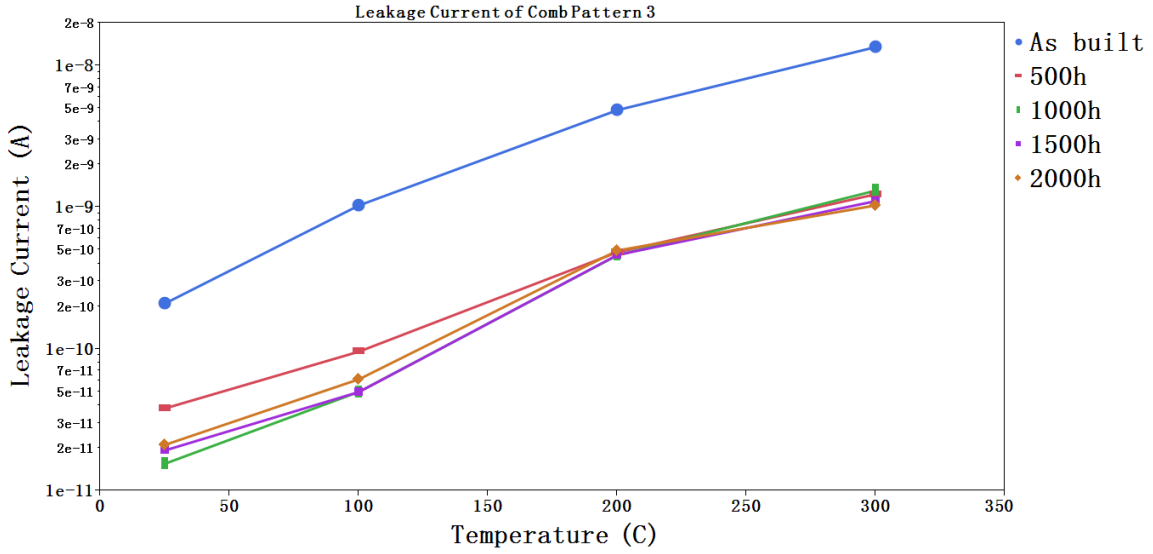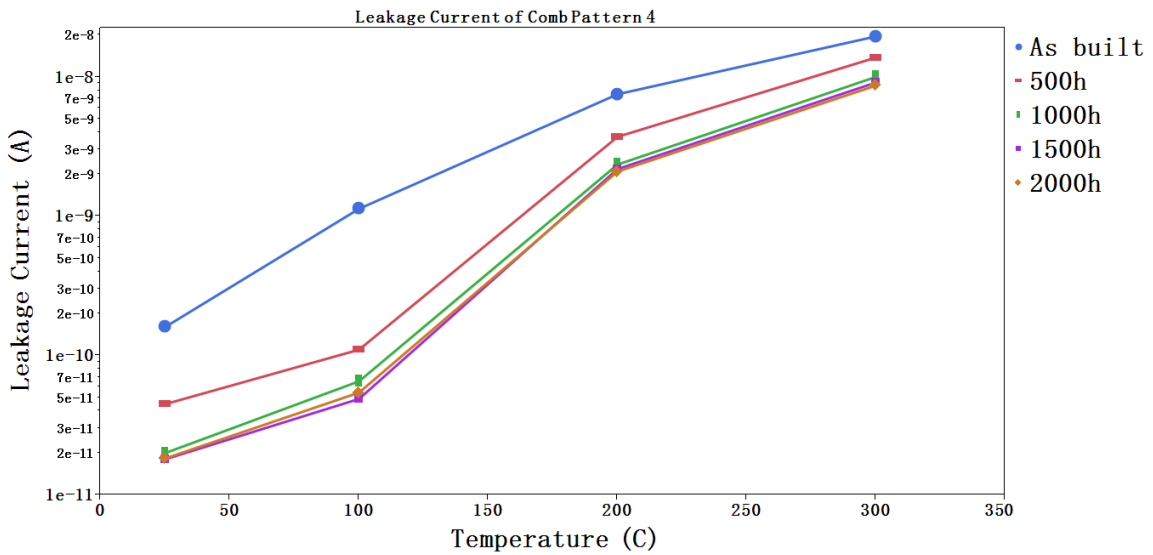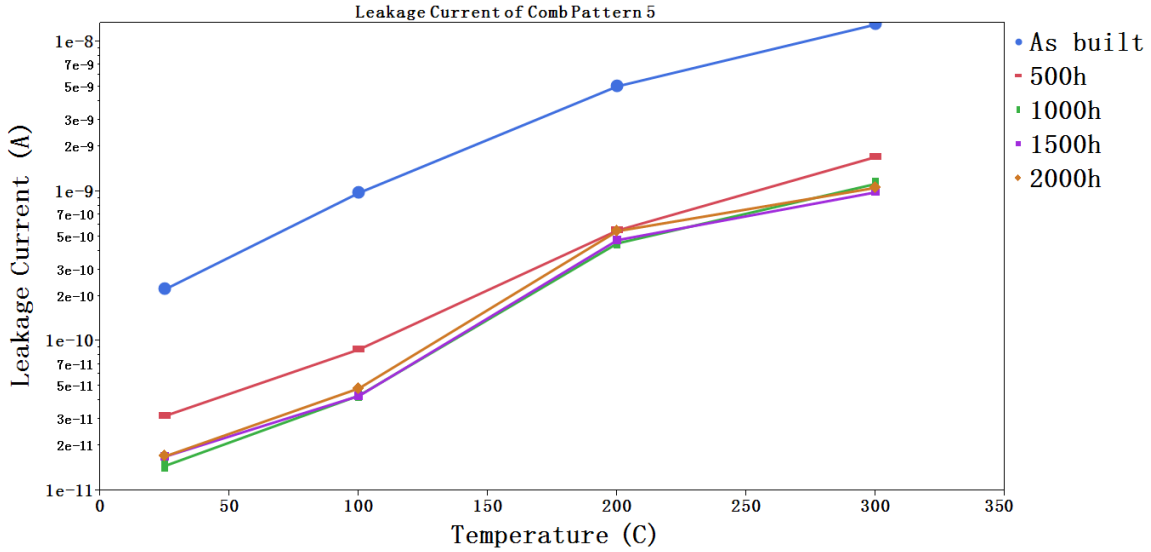Figure 2.41 Leakage Current of Cross-over Area (A4XB7) at 20V Bias as a Function of Temperature and Aging Hour
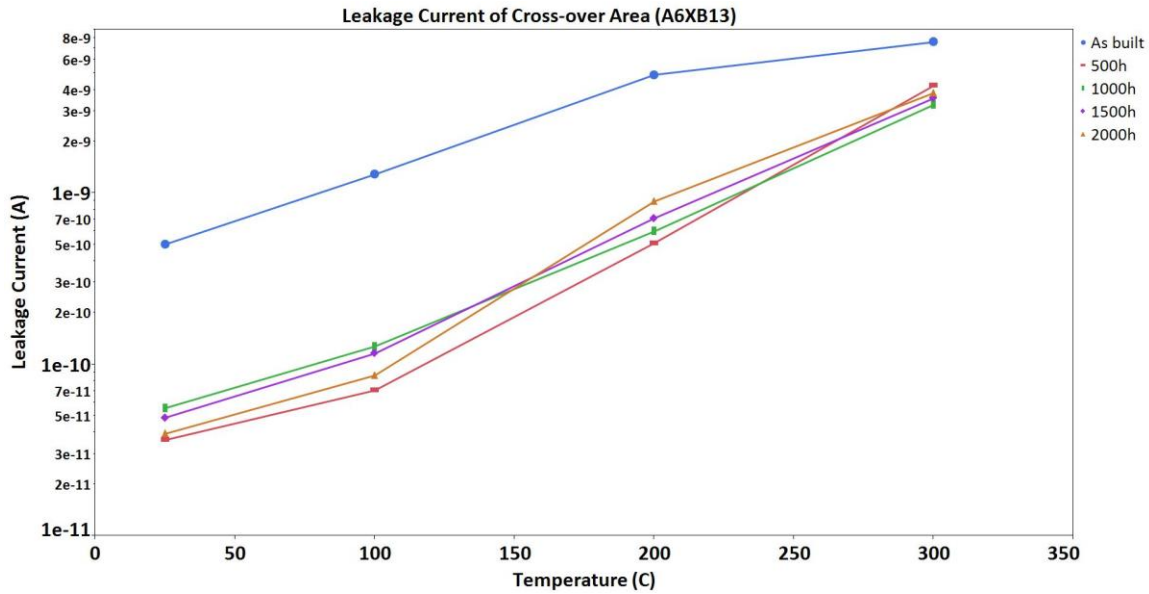
Figure 2.42 Leakage Current of Cross-over Area (A6XB13) at 20V Bias as a Function of Temperature and Aging Hour

2.8.2   Leakage Current Measurement with Bias

Besides the measurement mentioned above, leakage current measurement with bias was also performed on the capacitor "Cap 1". Before the aging, the leakage current was measured with 20V bias at room temperature, 100 ℃, 200 ℃ and 300 ℃. During the aging, 20V bias was constantly applied on the capacitor at 300 ℃ for 250h. The leakage current data was collected every second. Right after the aging, the leakage current was measured again with 20V bias at room temperature, 100 ℃, 200 ℃ and 300 ℃.

For the first sample, the initial leakage current with different bias polarities was shown in Table 2.7. The capacitor was aged at 300 ℃ for 250h with 20V bias. The bias polarity was positive on top and negative on bottom. The leakage current was shown in Figure 2.43. After the aging, the leakage current measurement was performed again with different bias polarities. The result are shown in Table 2.8. There were several peaks in the leakage current plotted in Figure 2.43. We believed that it was partial discharge in the

51

dielectric layer caused by some manufacturing defects in the fabrication process. The partial discharges are small electrical sparks that occur within the insulation of medium. Each discrete discharge is the result of an electrical breakdown of an internal void or defect within the dielectric. These discharges erode insulation and eventually result in insulation failure [36]. This explains why the leakage current increased from 10^{-11}A to 10^{-9}A after 250h aging with 20V bias.

Table 2.7 Initial Leakage Current with Different Bias Polarities

	Top+ Bottom- (Unit: A)	Top- Bottom+ (Unit: A)
25 ℃	2.01E-11	3.95E-11
100 ℃	3.81E-11	1.46E-10
200 ℃	3.04E-10	3.40E-10
300 ℃	2.75E-09	4.55E-09

Figure 2.43 Leakage Current at 20V Bias as a function of Time

Table 2.8 Leakage Current after Aging with Different Bias Polarities

	Top+ Bottom- (Unit: A)	Top- Bottom+ (Unit: A)
25 ℃	6.52E-09	5.42E-09
100 ℃	1.59E-08	1.26E-08
200 ℃	5.54E-08	6.18E-08
300 ℃	1.99E-07	1.93E-07

For another sample, the initial leakage current with different bias polarities is shown in Table 2.9. During the aging, the capacitor was aged at 300 ℃ for 250h with 20V bias. The bias polarity was positive on top and negative on bottom. The leakage current is shown in Figure 2.44. During the 250h test, the leakage current was very stable and consistent. No abrupt current increase or partial discharge was observed. After aging, the leakage current measurement was performed again with different bias polarities. The result is shown in Table 2.10. The leakage was stable and consistent during this testing. In the following tests on several more samples, stable and consistent leakage current during aging with bias was observed once again. This proves that with good dielectric deposition, the device can provide reliable electrical performance at high temperature with constant bias.

Table 2.9 Initial Leakage Current with Different Bias Polarities

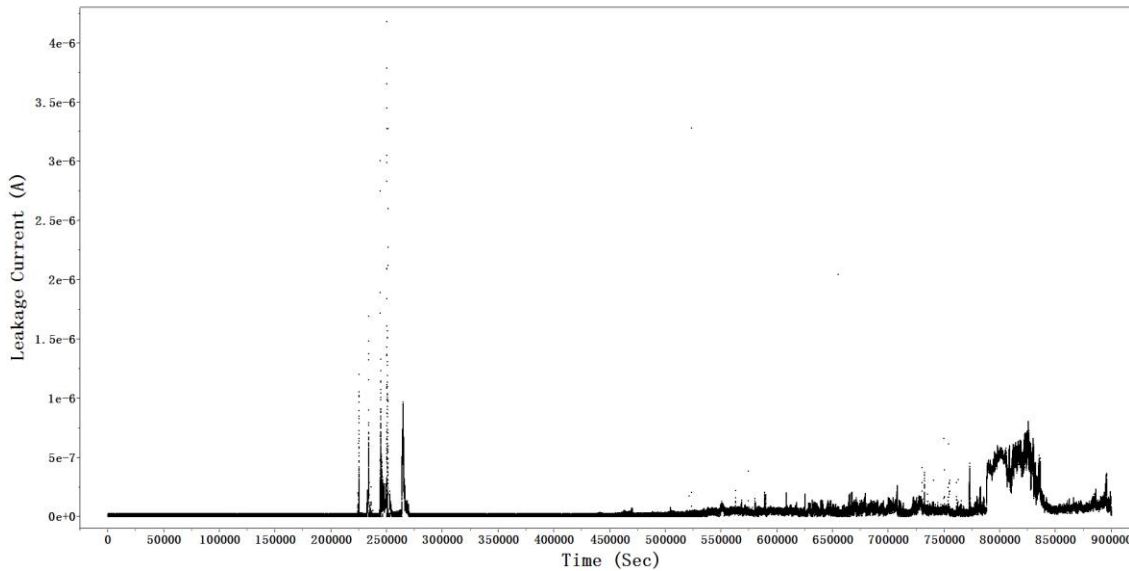|	Top+ Bottom- (Unit: A)	Top- Bottom+ (Unit: A)
25 ℃	2.84E-11	3.77E-11
100 ℃	8.35E-11	1.07E-10
200 ℃	3.53E-10	3.57E-10
300 ℃	2.93E-09	3.33E-09
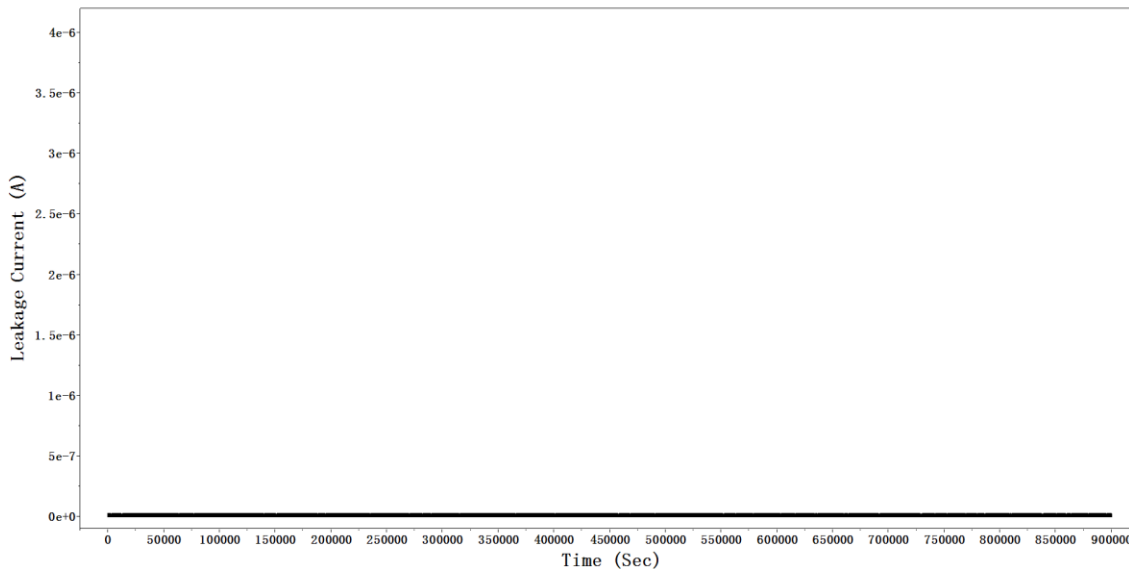
Figure 2.44 Leakage Current at 20V Bias as a function of Time

Table 2.10 Leakage Current after Aging with Different Bias Polarities

	Top+ Bottom- (Unit: A)	Top- Bottom+ (Unit: A)
25 ℃	3.90E-11	3.58E-11
100 ℃	1.68E-10	1.06E-10
200 ℃	1.42E-09	1.13E-09
300 ℃	3.14E-09	5.07E-09

2.8.3   Capacitance and Dissipation Factor Measurement

The capacitor "Cap 1" was designed for capacitance and dissipation factor measurement, as shown in Figure 2.45. A test fixture was used to hold the substrate and provide a reliable contact between coax wires and the capacitor, as shown in Figure 2.46. In the test, the substrate was held by an aluminum substrate and a piece of thick glass ceramic. Four 1-meter (electrical length) coax wires were connected to the capacitor through that glass ceramic. The coax wire was inserted into the ceramic through a channel and fixed by a contact screw. Another screw was used to apply pressure to the contact probe through an insulator ball and a spring.
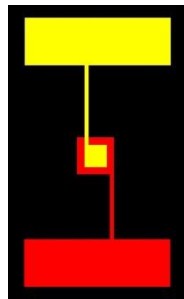
Figure 2.45 Illustration of Capacitor 1
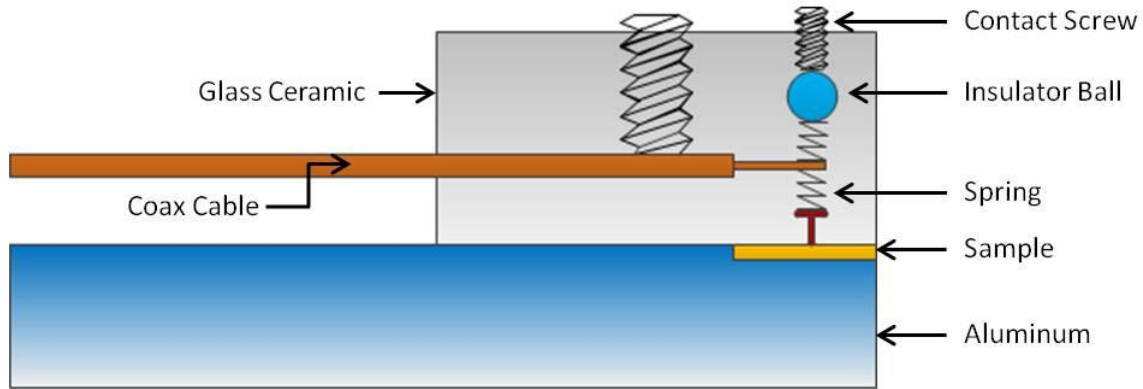
Figure 2.46 Illustration of Test Fixture for Capacitance and Dissipation Factor Measurement

In the test, the whole fixture was placed inside of a Delta Design 9023 oven. Capacitance and dissipation factor was measured with an Agilent 4192A LF Impedance Analyzer (Figure 2.47) at room temperature, 100 ℃, 200 ℃ and 300 ℃ after 500h, 1000h, 1500h, and 2000h thermal aging at 300 ℃.

Figure 2.47 Agilent 4192A LF Impedance Analyzer

The capacitance measurement results of samples as built and after 2000h thermal aging at 300 ℃ are plotted in Figure 2.48 and Figure 2.49. The capacitance is plotted as a function of temperature and frequency. The initial capacitance was very small and decreased with the increasing of temperature and frequency. After 2000h thermal aging at 300 ℃, the capacitance was still very consistent with the initial data.

55
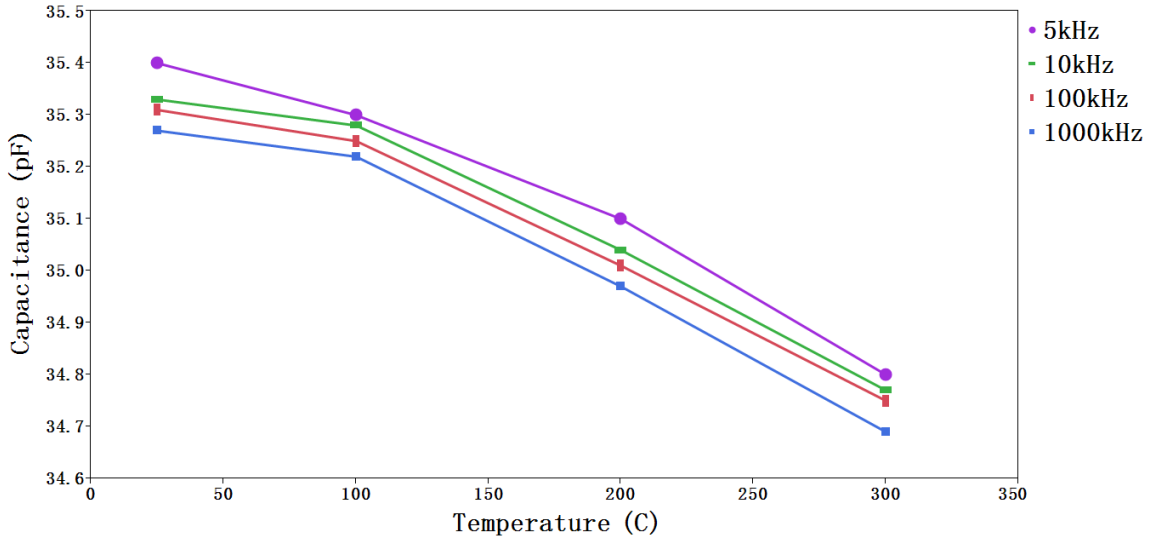
Figure 2.48 Capacitance (Cap 1) as a Function of Temperature and Frequency (Average of 6 samples as built)
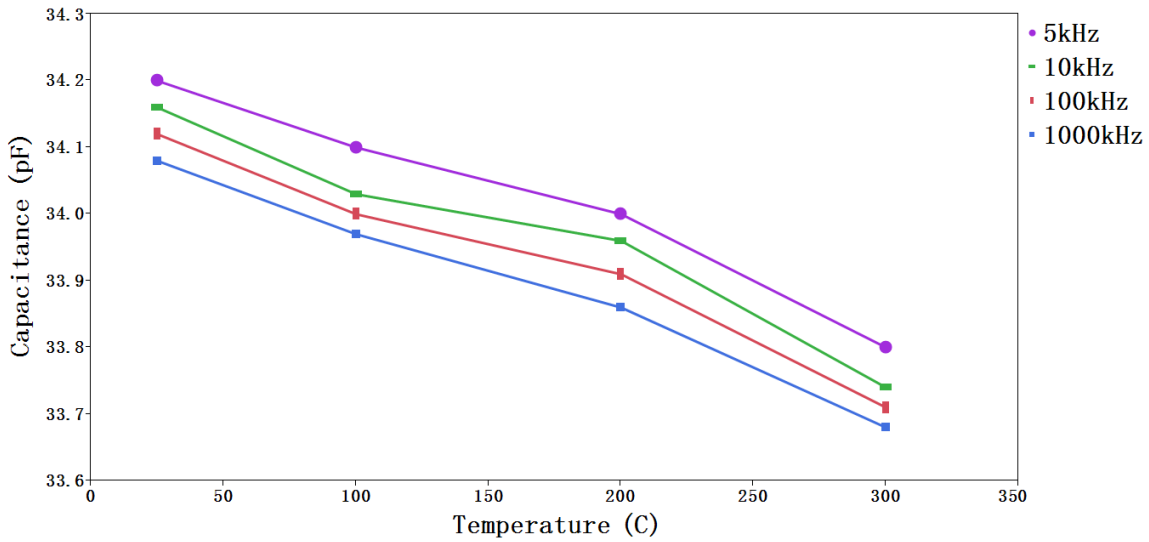
Figure 2.49 Capacitance (Cap 1) as a Function of Temperature and Frequency (Average of 6 samples after 2000h thermal aging at 300 ℃)

The dissipation factor measurement results of samples as built and after 2000h thermal aging at 300 ℃ are plotted in Figure 2.50 and Figure 2.51. The dissipation factor increased with temperature and decreased with test frequency and could hardly be measured at frequencies greater than 100kHz. The dissipation factor of the Si_3N_4 is relatively low over the temperature range and should not impact electrical performance.

After 2000h thermal aging at 300 ℃, the dissipation factor was still very consistent with the initial data.
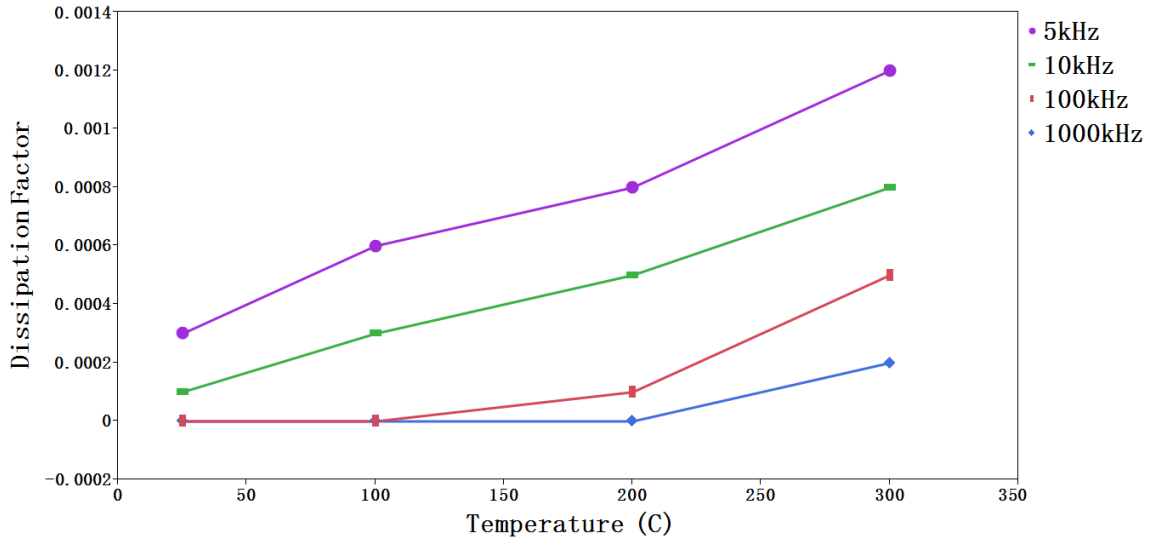
Figure 2.50 Dissipation Factor (Cap 1) as a Function of Temperature and Frequency
(Average of 6 samples as built)
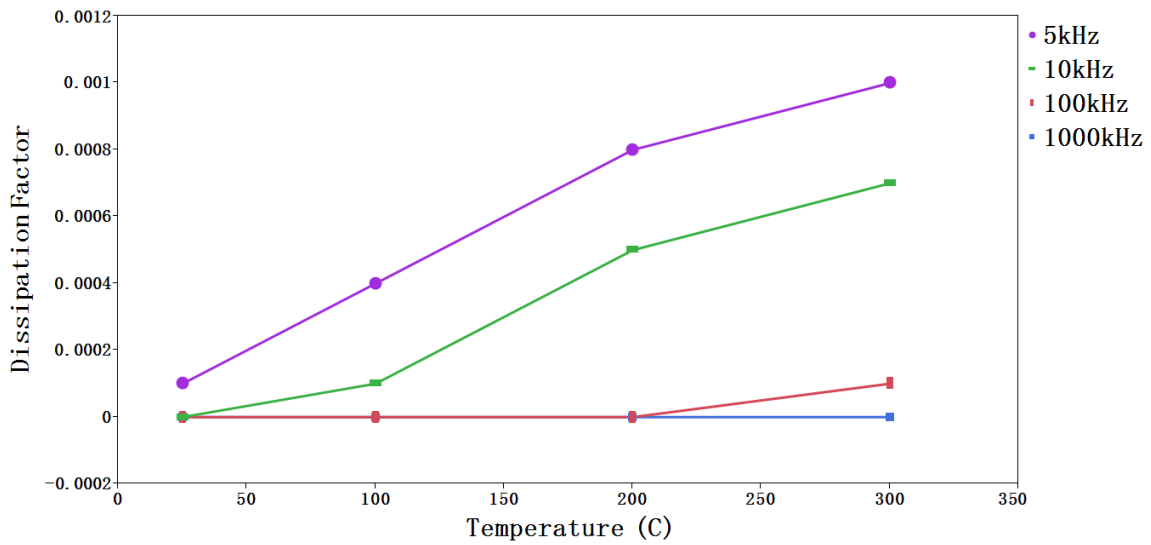
Figure 2.51 Dissipation Factor (Cap 1) as a Function of Temperature and Frequency
(Average of 6 samples after 2000h thermal aging at 300 ℃)

2.8.4   Continuity Testing

In the multilayer digital circuit board, the bottom metal layer and top metal layer are connected through vias in the dielectric layer. Three continuity testing patterns were

57

designed to test if these contacts were reliable after high temperature aging, as shown in Figure 2.52. These lines were 6mil, 10mil and 16mil wide and the corresponding via sizes were 2mil by 2mil, 6mil by 6mil and 12mil by 12mil, as shown in the Figure 2.53, Figure 2.54 and Figure 2.55. The resistance of the pattern was measured on samples as built and samples after thermal aging (300℃ for 500, 1000, 1500, and 2000 hours) at room temperature. Tiny probe pads along traces were designed to locate the possible failure point. During all 2000h aging at 300℃, the resistance of each continuity pattern was very stable and consistent, as shown in Figure 2.56.
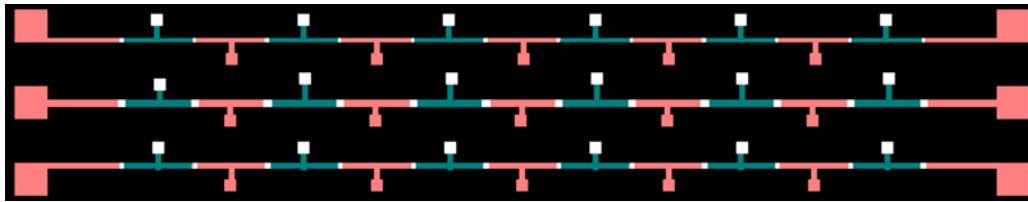
Figure 2.52 Continuity Testing Patterns
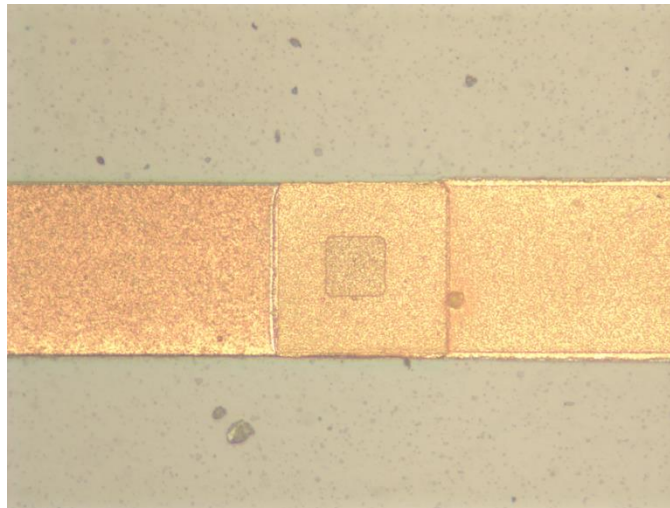
Figure 2.53 6mil Trace with 2mil Via
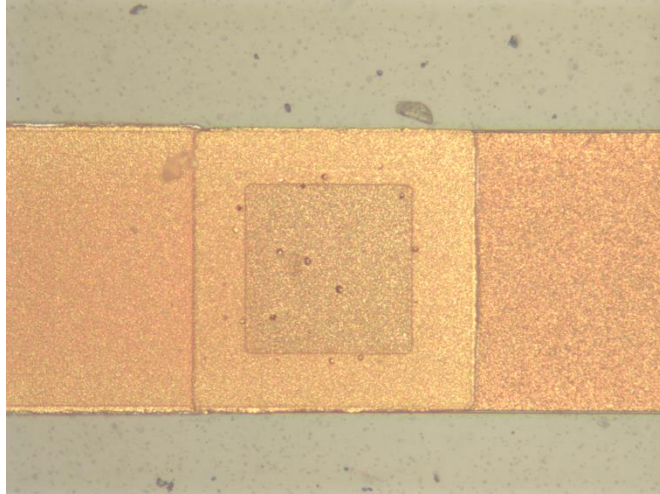
Figure 2.54 10mil Trace with 6mil Via
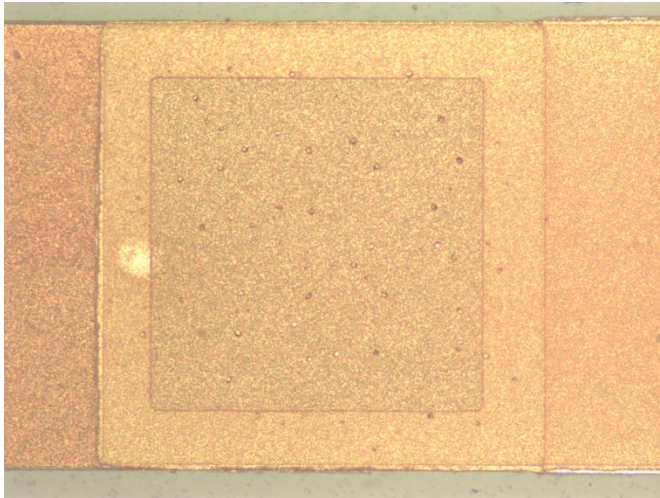
Figure 2.55 16mil Trace with 12mil Via
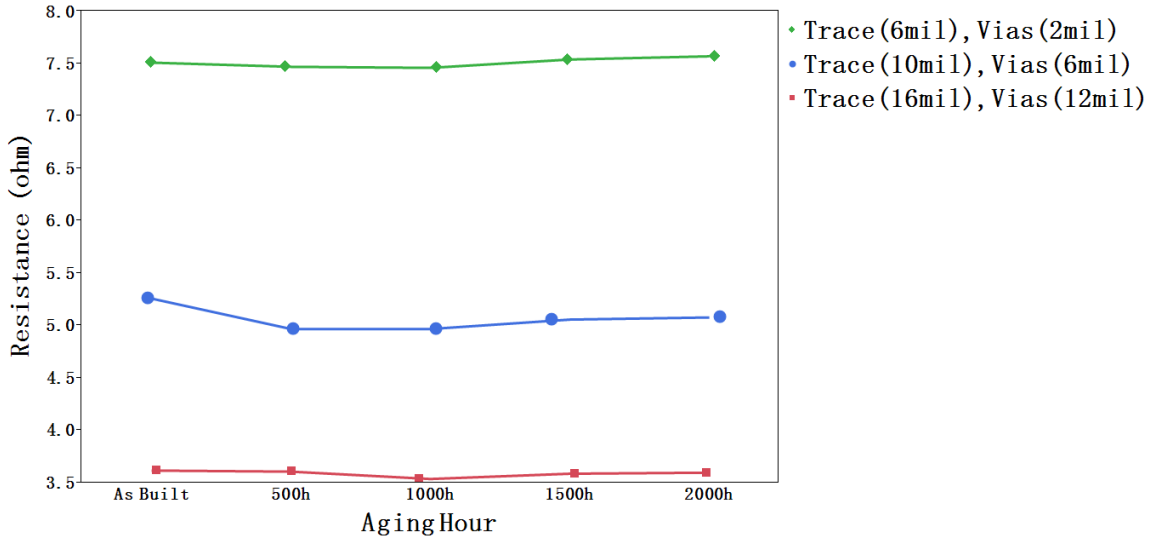
Figure 2.56 Resistance of Three Continuity Patterns as a Function of Aging Hour at
300 ℃

2.9   Summary

A multilayer thin film substrate technology has been developed to interconnect multiple SiC devices on the AlN substrate. The conductor is vacuum deposited Ti/Ti:W/Au followed by an electroplated Au. A PECVD silicon nitride is used for the interlayer dielectric.

Adhesion testing was performed on four test vehicles: conductor on AlN; dielectric on AlN; conductor on dielectric; and dielectric on conductor. The first three test vehicles showed excellent adhesion during 2000h aging at 300 ℃. The adhesion performance of the dielectric on conductor test vehicle was improved by introducing a thin layer of Cr between the electroplated Au and Si_3N_4.

The silicon nitride provided great insulation at 300 ℃. Leak current measurement, capacitance and dissipation factor measurement and continuity testing proved that its electrical performance was stable and consistent during the 2000h aging. When 20V bias was constantly applied on the dielectric at 300 ℃, partial discharge was observed in some

samples. Further study is needed to improve the quality of the dielectric deposition and remove voids or particles in the dielectric layer.

CHAPTER 3 HIGH TEMPERATURE FLIP CHIP ATTACH

3.1   Introduction

Besides good adhesion between conductor and dielectric layer and stable electrical performance, robust flip chip bonding is also another crucial factor for reliable digital circuit assembly. In this project, the digital die was assembled to the substrate using thermocompression bonding. This is because flip chip bonding provides reduced package size, lower cost for high volume automated production, large number of I/O, better electrical performance and higher reliability than wire bonding. Flip chip thermal aging testing, flip chip thermal cycling testing, flip chip shock and vibration testing were performed to evaluate the reliability of flip chip bonding.

Prior to the flip chip bonding process, a stud bumping process was required. The stud bumping process was used to bump die with a modified wire bonding process. This technique made a tiny ball by melting the end of the metal wire. Then the ball was attached to the corresponding pad just as in the first step of the wire bonding process. However, to form tiny bumps instead of wire bonds, the wire bonder was programmed to break off the wire close above the ball. The remaining ball, or stud bump provided a permanent, reliable connection to the underlying pad. After placing stud bumps on a chip, they could be flattened (or coined) by mechanical pressure to provide a flatter top and more uniform height. Every stud could be flattened by a tool right after forming, or all studs on the die could be flattened together by pressure against a flat surface. What is more, multiple bumps

can be stacked to achieve an increased standoff to help reduce some of the strain induced by the CTE mismatch between the chip and the substrate.

3.2   Flip Chip Thermal Aging Test

In order to ascertain whether the gold to gold thermocompression bonding would still be robust after long time thermal aging, a daisy chain pattern was designed. This daisy chain consisted of probe patterns on the AlN substrate and stud bumps and metal traces on the SiC die. The die and substrate were themocompression bonded together. Die shear tests were performed at room temperature on samples as built and samples after thermal aging (300 ℃ for 500, 1000, 1500, and 2000hr). The die shear strength was used to evaluate the bonding quality.

First, the 4 inch SiC wafer was fabricated at GE Global Research Center. This wafer had no functional digital circuitry but contained daisy chain patterns on the topside. The metal stack of the pattern was 250Å Ti, 500Å TiW, and 1μm Au (from bottom to top). Then the wafer was shipped to Auburn University. It was stud bumped using a Palomar 2460 Model V automatic Au thermosonic wire bonder. The height of the stud bump was 2mil and the diameter of the stud bump was 4mil. The stud bump pitch was 16mil. The stud bumping details are:

- Wire:

  Custom Chip Connection: 1mil Au wire

  2-6% elongation

  9 gram minimum tensile strength

- Capillary:

  Gaiser 1820-13-437GM-47(3-11D-8)20D AB10X10

- Bonding parameters:

  85μm free air ball diameter

  Stage temperature: 150°C

  Force: 68 grams

  Time: 70 milliseconds

  Ultrasonics: 70 microinches

Once stud bumping was completed, the SiC wafer was diced into 2.25mm by 2.25mm die with a Disco DAD 3220 dicing saw. The SiC die with stud bumps is shown in Figure 3.1.
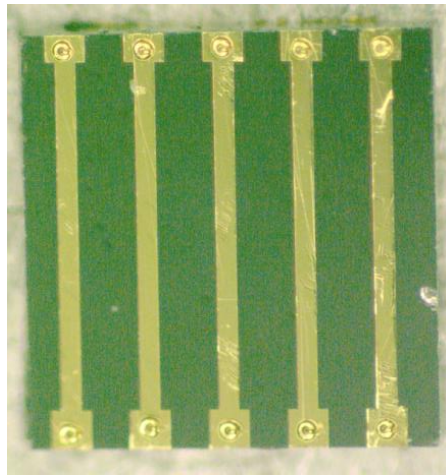
Figure 3.1 SiC Die (2.25mm) with Stud Bumps

The substrate part of the daisy chain was fabricated with the same fabrication process described in Chapter 2. Two big round pads on the two ends of the pattern were for the electrical continuity test before the shear test. This continuity test tells if all of the stud bump connections were electrically good and the shear test tells how mechanically robust those connections were. Once the substrate was fabricated, it was diced into 25

individual test coupons (0.6 inch by 0.6 inch). The substrate and the individual test coupon are shown in Figure 3.2.
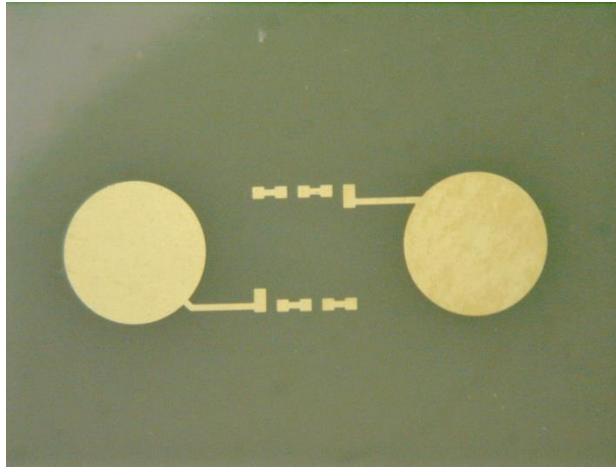
Figure 3.2 Substrate for Flip Chip Thermal Aging Test

Prior to assembly, both the die and substrate were plasma cleaned in a YES-500 plasma cleaner, shown in Figure 3.3. Generally, this argon plasma cleaning removes fluorine, organic contamination and metal oxides via ion bombardment without causing a chemical reaction or oxidation on the surface of the substrate. After this, the bumped SiC die was thermocompression bonded to the corresponding substrate using a SETI FC 150 flip chip bonder, shown in Figure 3.4. The FC-150 bonder was calibrated every time before starting the bonding process to ensure parallelism between the die and substrate. Parallelism was extremely important in the bonding process and could highly influence the reliability of the bond and shear test results. In the bonding process, 100 gram force was applied on each stud bump (1000g/10bumps). The bonding parameter profiles (temperature and force) are shown in Figure 3.5. The top view and an x-ray image of a bonded die are shown in Figure 3.6 and Figure 3.7. Figure 3.8 shows an optical edge view of the bonded die.

Figure 3.3 YES-500 Plasma Cleaner

Figure 3.4 SETI FC 150 Flip Chip Bonder
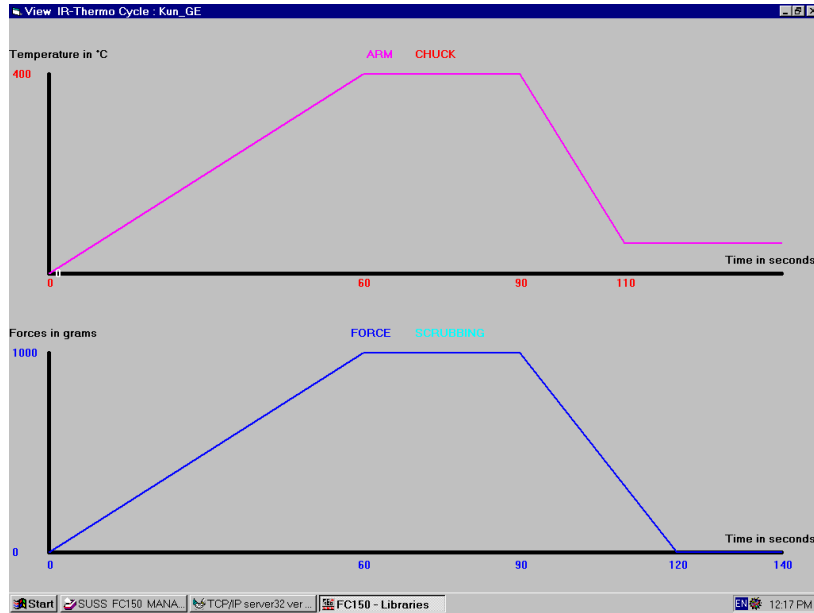
Figure 3.5 Flip Chip Bonding Parameter Profiles
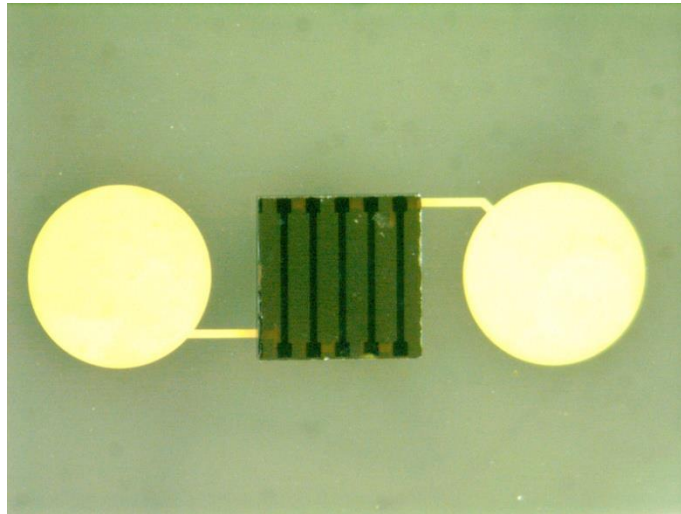
Figure 3.6 Bonded SiC Die (Top View)
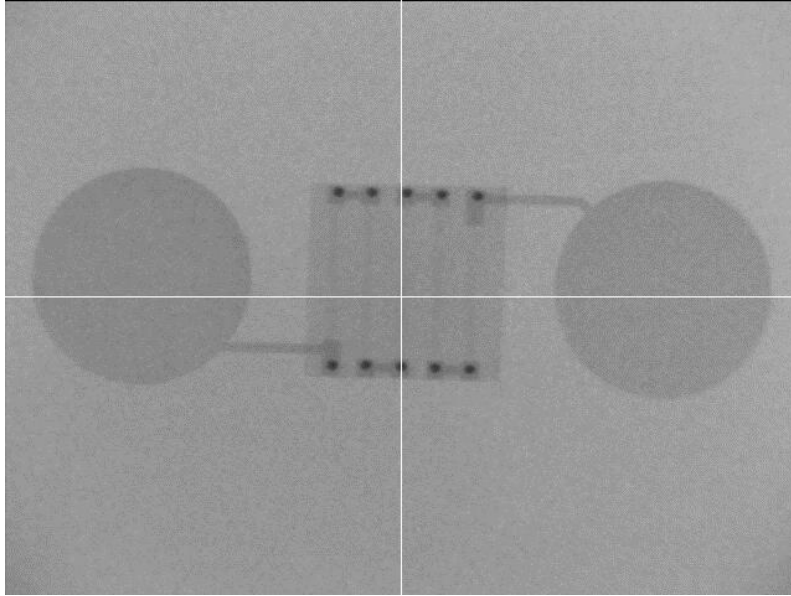
Figure 3.7 X-ray Image of Bonded Die
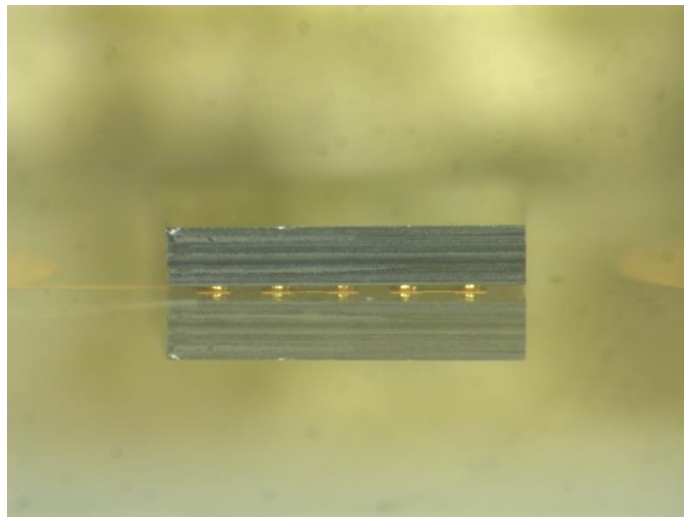
Figure 3.8 Optical Edge View of Assembled Die

The die shear test was conducted at room temperature on samples as built and samples after thermal aging (300 ℃ for 500, 1000, 1500, and 2000hr) using a Dage 2400PC Shear Tester with a 20Kg load cartridge, shown in Figure 3.9. The shear testing parameters are shown in Table 3.1.
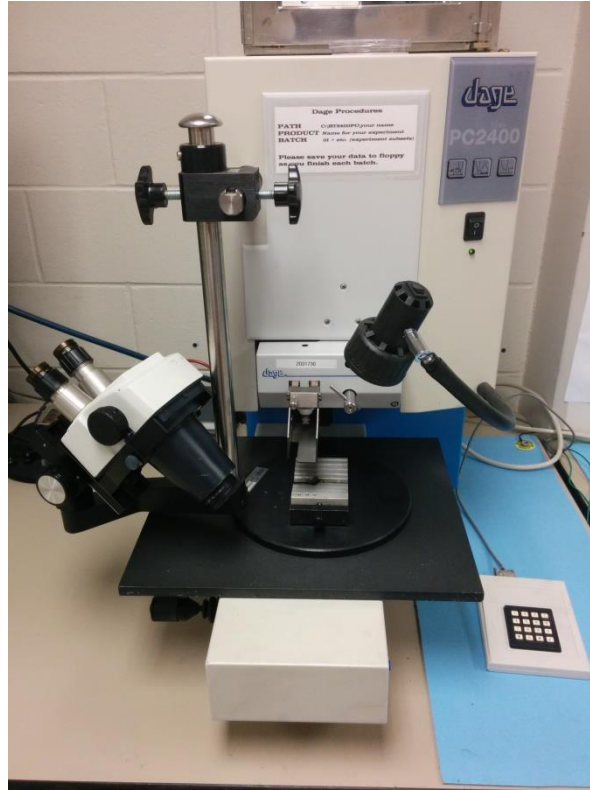
Figure 3.9 Dage 2400PC Shear Tester

Table 3.1 Shear Testing Parameters

Land Speed	5.0mil/sec
Test Height	0.8mil
Test Speed	2mil/sec
Threshold	N/A
Over travel	30mil
Pitch	5.0mil

The die shear testing results are shown in Figure 3.10. The shear strength increases slightly with aging. The die shear failures are mostly (>98% of stud bumps) in the Au stud bump throughout the test. The Au stud bump is shown in Figure 3.11.
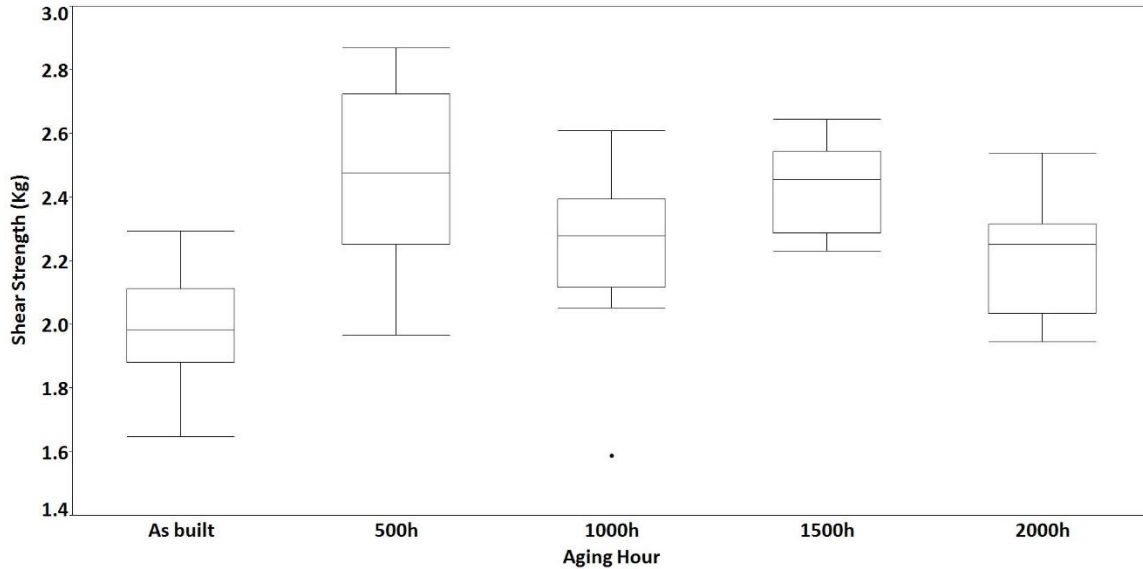
Figure 3.10 Shear Strength as a Function of Aging Hour at 300 ℃

Figure 3.11 Image of New Au Stud Bump

3.3 Flip Chip Thermal Cycling Test

Thermal cycling test was used to determine the ability of the package to withstand cyclical exposures to temperature extremes. In another words, this test was set up to find problems that could possibly occur over time due to the coefficient of thermal expersion (CTE) mismatch between the SiC die and AlN substrate. In this project, both single-bump configuration and double-bump configuration were evaluated.

The thermal cycling test vehicle was similar to the thermal aging test vehicle with some differences. First, a larger SiC test die (4.5mm by 4.5mm) was selected for the thermal cycling test to increase the stress on the gold stud between the SiC die and AlN substrate. The die is shown in Figure 3.12. The corresponding pattern on the substrate also

becomes larger. Because the stress in thermal cycling test is much larger than that in thermal aging test, several tiny probe pads were added on the substrate for the future failure analysis. If there was an opening in the daisy chain, these tiny probe pads help locate where the opening was, as shown in Figure 3.13.
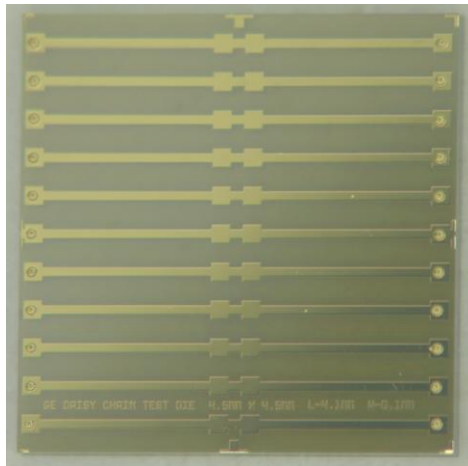
Figure 3.12 SiC Die (4.5mm) with Stud Bumps
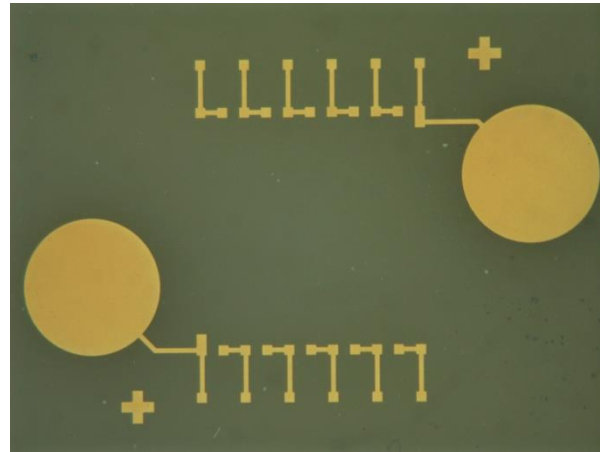
Figure 3.13 Substrate for Flip Chip Thermal Cycling Test

For single-bump flip chip thermal cycling test vehicles, only the die was stud bumped with the Palomar 2460 Model V automatic Au thermosonic wire bonder with the same parameter previously given. Because a larger die was used, the number of stud bump on the die was increased from 10 to 22. Meanwhile, the bonding force in the bonding profile

was also increased from 1000g to 2200g. A top view of an assemble die and substrate is shown in Figure 3.14.
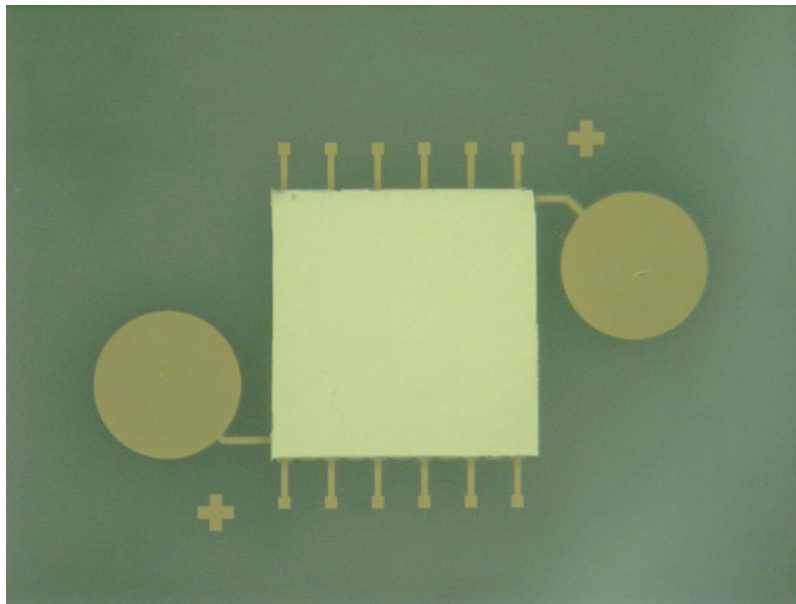
Figure 3.14 Top View of an Assemble Die and Substrate

The thermal cycling test was performed on a custom programmable hot plate. The thermal cycle profile is plotted in Figure 3.15. The shear test results are shown in Figure 3.16. In the initial die shear test, most failures were within the ball. Then more and more failures were at the ball-to-thin film interface. The increase in the number of failures at the ball-to-thin film interface corresponds to the decrease in shear strength seen in Figure 3.16. There were no electrical opens in the total population as-assembled. Of ten die measured after 100 thermal cycles and ten die measured after 500 thermal cycles, there were no electrical opens. However, after 1000 thermal cycles, six of forty die tested had electrical opens. As previously discussed, the CTE of the SiC and the AlN substrate are a near match. The hot plate system heated the test vehicles from the bottom side of the AlN substrate by conduction and the only conduction paths to the SiC die were through the Au bumps. It was likely a temperature gradient existed between the substrate and SiC die, resulting in

72

higher stresses than would occur with uniform heating. A thermal cycling test in a wide temperature range thermal cycle chamber was considered in the new thermal cycling test.
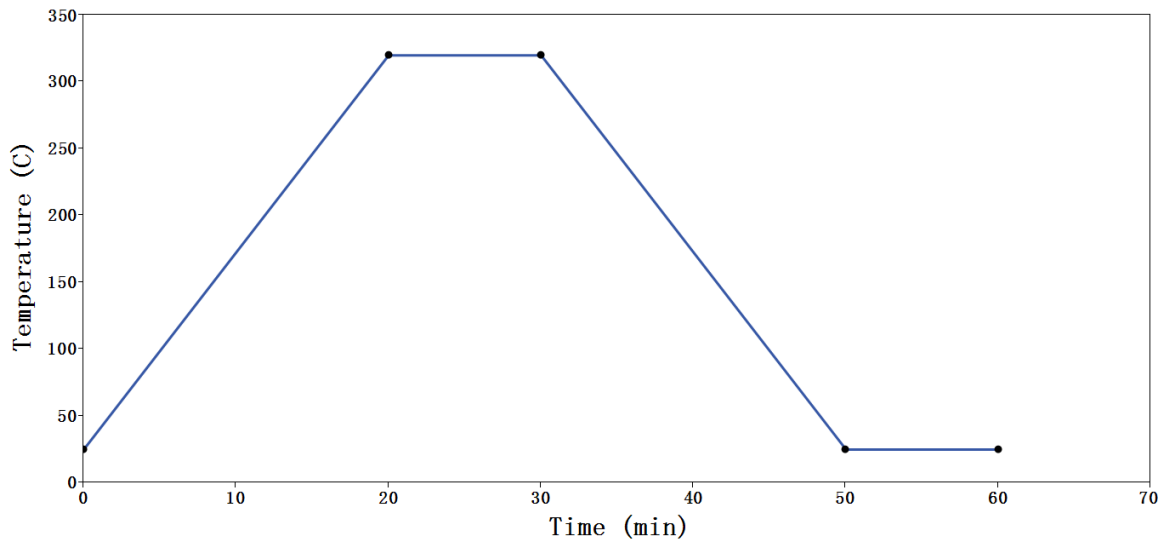
Figure 3.15 Thermal Cycle Temperature Profile
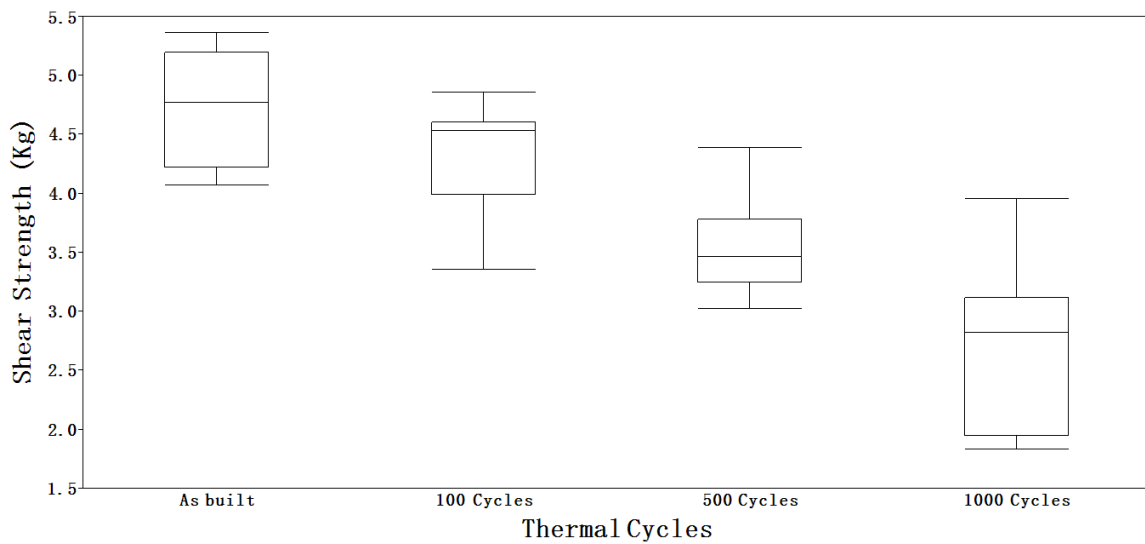
Figure 3.16 Shear Strength as a Function of Thermal Cycles

To improve the thermal cycle performance of the stud bump assembly, a double bump configuration was also evaluated. Both die and substrate were stud bumped with the Palomar 2460 Model V automatic Au thermosonic wire bonder with the same parameters. Double bumps increase the height of the gap between the die and the substrate. This

increase of height decreases the strain on the interconnection for a given CTE or temperature mismatch between the SiC die and AlN substrate. The optical edge view of a double-bump sample is shown in Figure 3.17 and Figure 3.18.

Figure 3.17 Optical Edge View of a Double-bump Sample
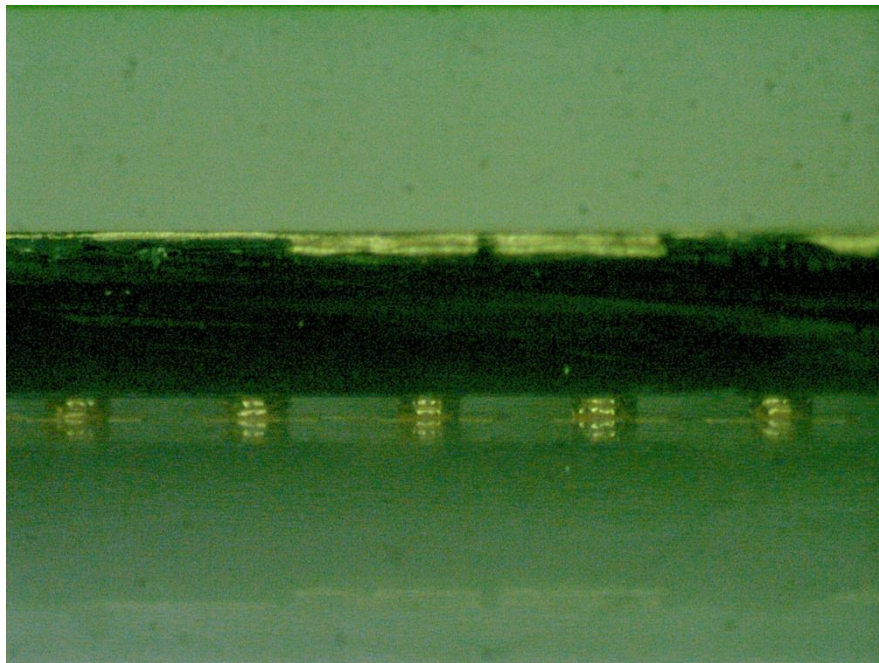
Figure 3.18 Optical Edge View of a Double-bump Sample

74

The thermal cycling samples (single-stud and double-stud) were placed in small pockets of the fixture, as shown in Figure 3.19. Then all fixtures were stacked up together, as shown in Figure 3.20, and placed inside of a thermal cycling chamber in Oak Ridge National Laboratory (ORNL). In each thermal cycle, the temperature was held at round 300℃ for 10min and at around -45℃ for 5min, as shown in Figure 3.20. Each thermal cycle took about 45min.
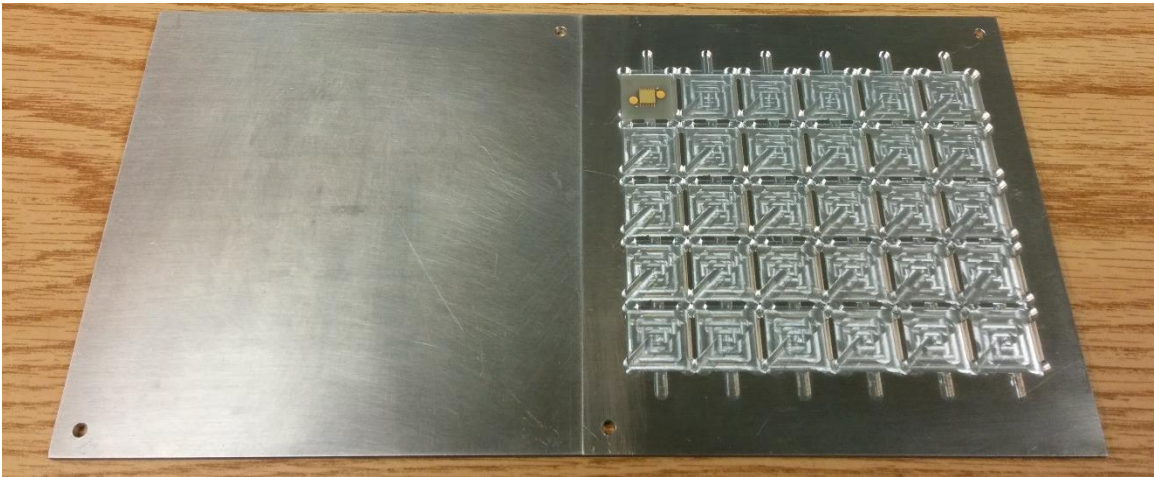
Figure 3.19 Fixtures for Flip Chip Thermal Cycling Test

Figure 3.20 Fixture Bulk
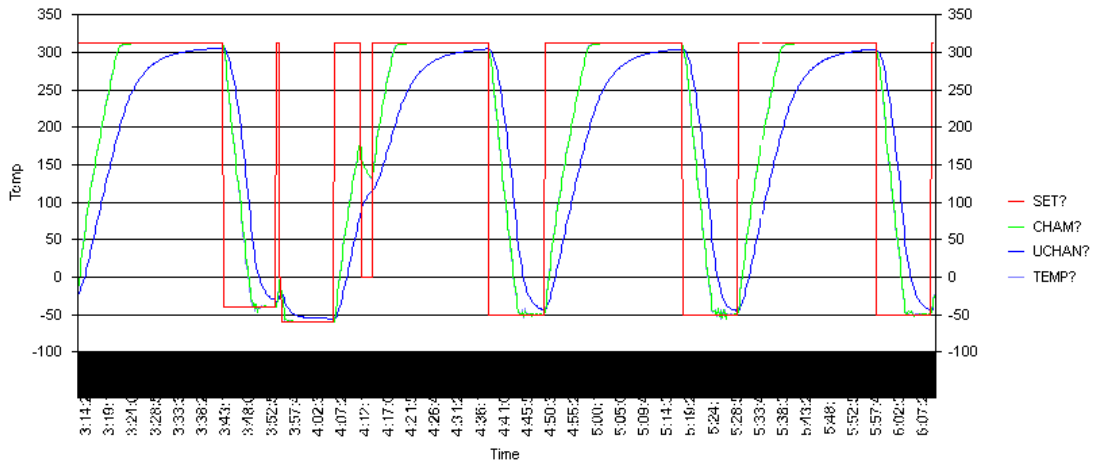
Figure 3.21 Thermal Cycle Temperature Profile

The shear strength of samples as built and after 100 thermal cycles is shown in Figure 3.22. The double bump samples did have a better thermal cycling performance than the single bump samples. The thermal cycling test is still ongoing.
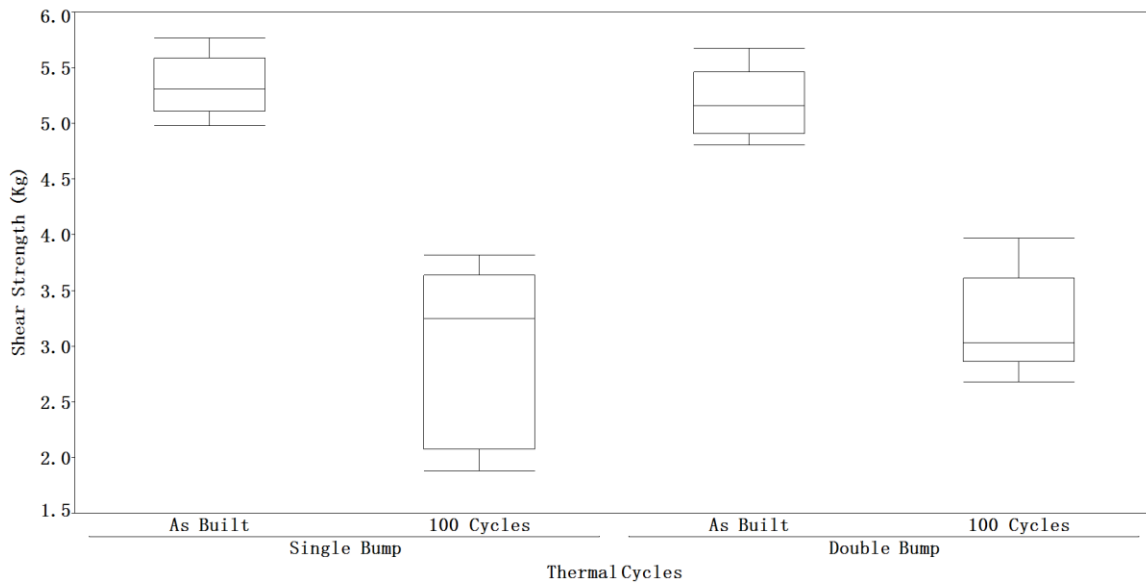
Figure 3.22 Shear Strength as a Function of Thermal Cycles

3.4   Flip Chip Shock and Vibration Test

In an enhanced geothermal system, measurement-while-drilling tools are used in a high shock and vibration environment. The terms shock and vibration are generally used

to refer to the dynamic mechanical excitation that may cause a dynamic response of a physical system, usually a mechanical structure that is exposed to that excitation [37]. There is a slight difference between shock and vibration. A shock is dynamic excitation with a relatively short duration and a vibration is dynamic excitation with a relatively long duration as compared to the time required for a physical system exposed to that excitation to fully respond [37]. Shock and vibration could cause fracture of the ceramic board and could also lead to cracking and displacement of the gold stud bumps. In this project, shock and vibration test samples were fabricated and assembled at Auburn University and shipped to GE Global Research to evaluate the ability of the assembly to withstand a high shock and vibration environments.

3.4.1   Shock Test

Generally, mechanical shock testing replicates events that are encountered regularly during the hour to hour operation of measurement-while-drilling tools. In this project, the fabrication and assembly process of shock test samples were exactly the same as those of thermal cycling test samples. Two daisy-chain test boards were fabricated and assembled. Each board had 13 SiC dies mounted on the AlN substrate with Au stud bump joints. Four dies were at the board corners and the other nine were in the center as a three by three array, as shown in Figure 3.23. One board was tested at room temperature and the other one was tested at 300 ℃. The resistance of each die is measured after certain intervals.
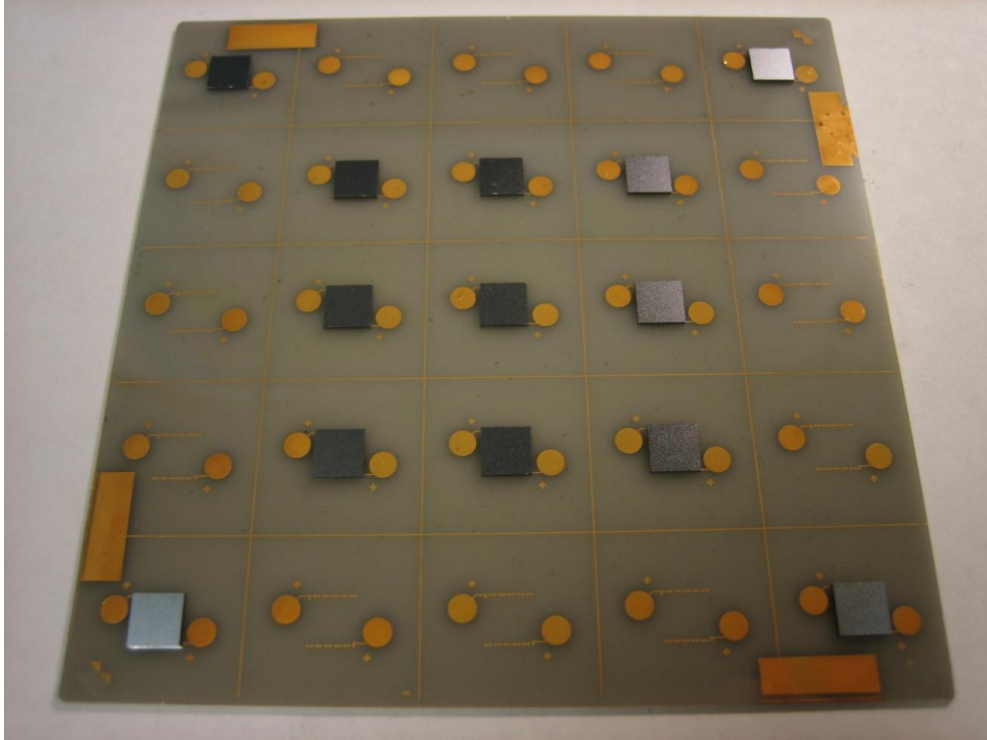
Figure 3.23 Shock Test Vehicle

The shock test was conducted on an Unholtz-Dickie vibration test system. A furnace was added to the system above the shaker table to accommodate the testing at 300 °C, as shown in Figure 3.24 [38]. An accelerometer was mounted on the shaker table to measure the acceleration level during testing. The acceleration waveform was monitored on an oscilloscope and was recorded at predetermined intervals by a LMS Test Lab software package. The board was subjected to mechanical shock testing at a 215G level at both room temperature and 300 °C. An example of acceleration-time curve is shown in Figure 3.25 [38]. A special fixture was designed to hold the substrate firmly during the whole test, as shown in Figure 3.26 [38].

Figure 3.24 Mechanical Shock Testing Setup [38]
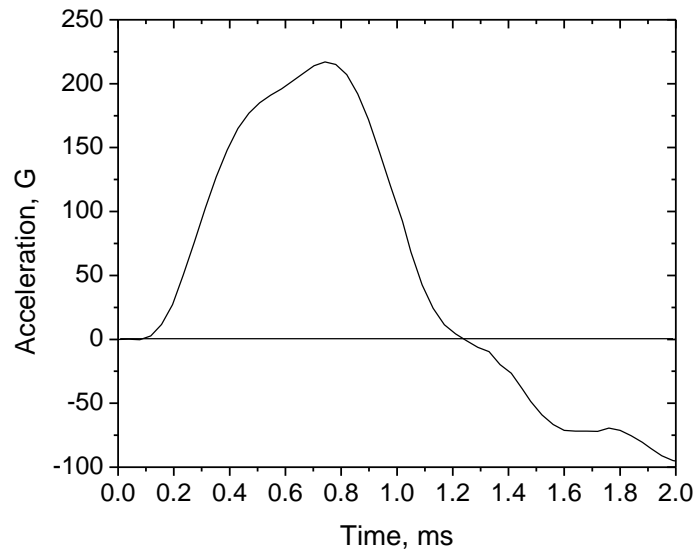
Figure 3.25 Acceleration-time Curve of the 50th Shock Delivered to a Daisy-chained
Test Board at 300 ℃ [38]
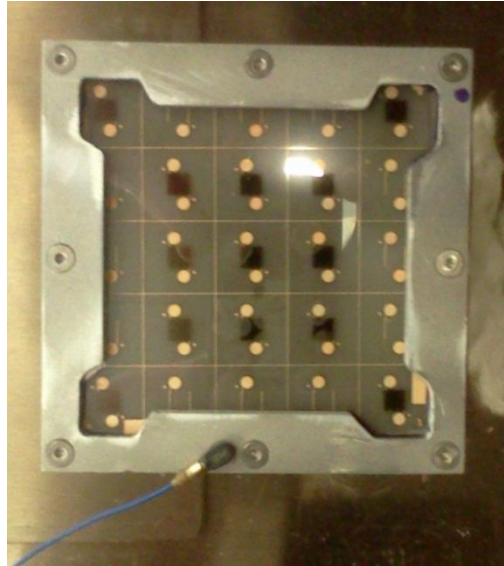
Figure 3.26 Shock Testing Board Mounted Inside the Fixture [38]

On the board tested at room temperature, two corner chips showed open daisy chains after the board was assembled to the shaker table before shocks were delivered to the board, shown as the "X"s in Figure 3.27 [38]. It is believed that the board mounting process damaged the flip-chip joints by introducing excess warpage of the AlN substrate when tightening the fasteners at the corners. It is suggested to improve the design of the mounting fixture for future testing and to use a torque wrench for controlling the fastening process. Two chips are found to have high resistance (>20% higher than original value) after 50 shocks and 250 shocks. Their locations are labeled in Figure 3.27 by the numbers. The resistance increase occurs between 40 and 50 shocks and between 200 to 250 shocks for the two chips respectively, and is indicative of the propagation of fatigue cracks in the flip-chip joints. The initiation of the cracks might occur at earlier shocks, since a partial crack will not lead to a resistance increase. In the end, nine of the thirteen chips survive 2000 shocks without failure.
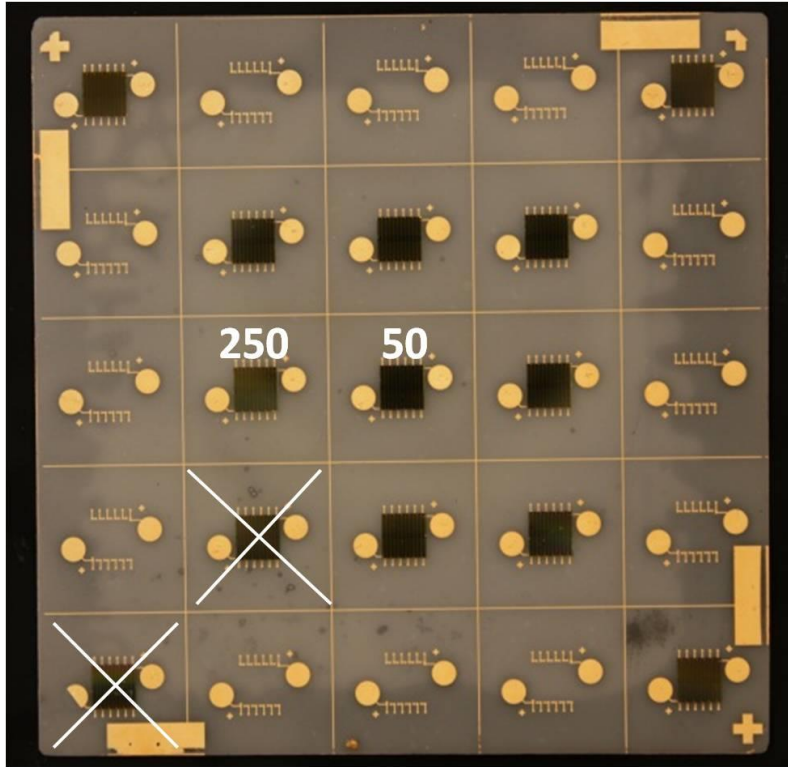
Figure 3.27 Shock Testing Board Tested at Room Temperature

On the board tested at 300˚C, one corner chip failed due to mounting to the shaker table again, shown in Figure 3.28 by the "X" [38]. Two corner chips were found to have high resistance after 50 shocks and 400 shocks. Their locations are labeled in Figure 3.28 by the numbers. The corresponding failure time was 10-50 and 200-400 shocks, respectively. Those two early failures might be attributed to the mounting process as well. The excess board warpage could lead to partial cracks in the flip-chip joints, which propagated in subsequent shocks and eventually caused failure. No failure was seen in the chips in the center 3×3 arrays. This was consistent with the notion that the joints became more compliant and more shock-absorbing at elevated temperature, i.e. 300˚C, compared with those at room temperature. Finally, ten of the thirteen chips survived 1000 shocks without failure.
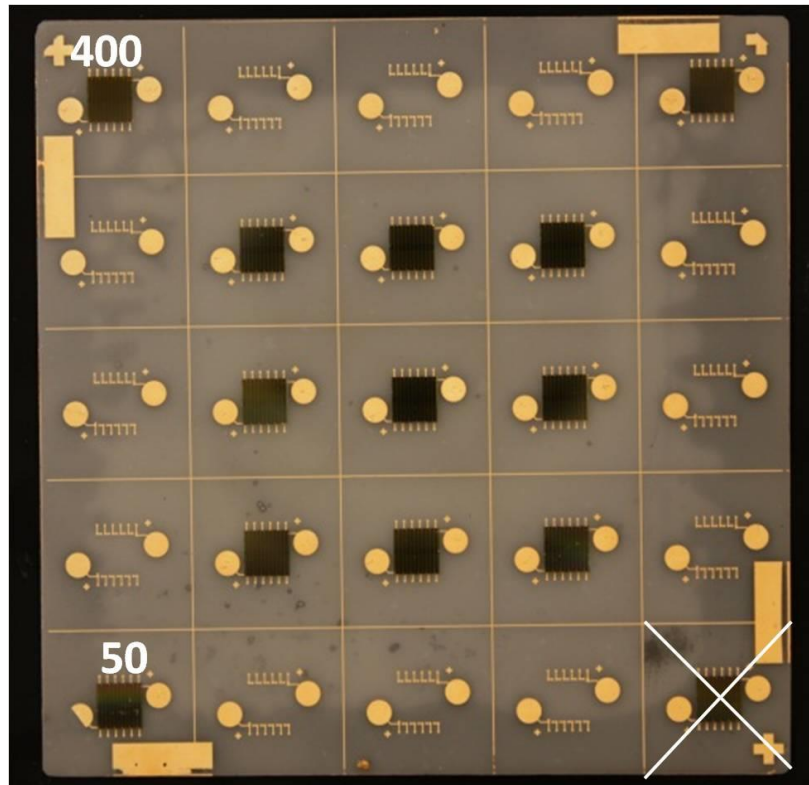
Figure 3.28 Shock Testing Board Tested at 300˚C [38]

3.4.2   Vibration Test

For the vibration test, a test board was fabricated using the daisy chain test pattern and the SiC die which were used for both thermal cycling test and shock test. The daisy chain pattern allows for detection of interconnect failure due to vibration by measuring electrical resistance. Just like the shock test, thirteen SiC dies were assembled to the aluminum nitride ceramic board with Au stud bumps. Four dies were at the corners and nine were in the center in a three by three array. The numbering of the die is shown as well, e.g. A1 or E5, as shown in the Figure 3.29 [38].
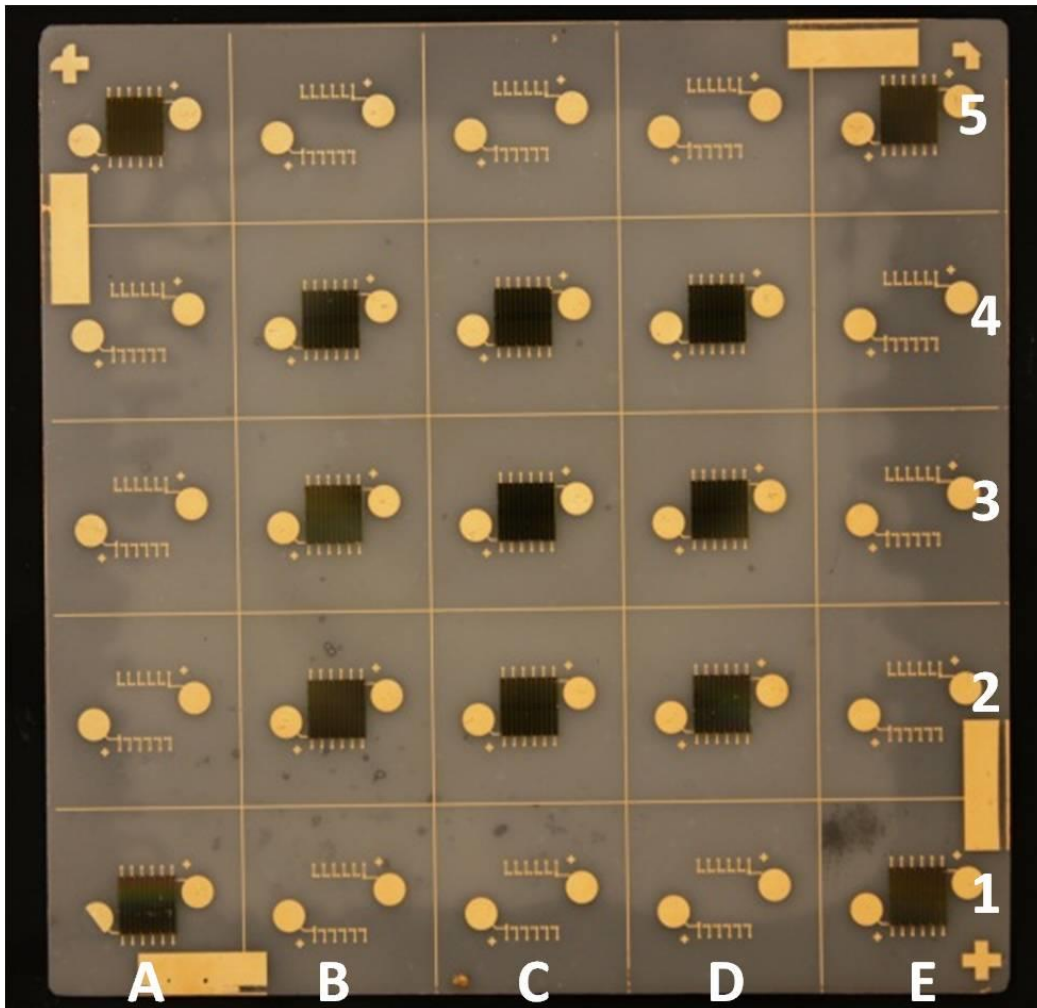
Figure 3.29 Vibration Testing Board [38]

The test setup consisted of a Blue-M oven with capability to reach 593 ℃ and a Labworks ET-126B electrodynamic transducer. The test board was placed horizontally on the bottom of the furnace as shown in Figure 3.30 [38]. An aluminum fixture was used to clamp the AlN board on its 4 edges. A Kapton® tape spacer was inserted between the board and the fixture to maintain a good contact.

Figure 3.30 Mechanical Vibration Testing Setup [38]

The random vibration test of the daisy chained board was conducted at 20G RMS at 300˚C. The test was interrupted at predetermined time intervals for measurement of electrical resistance. Results are summarized in Figure 3.31 [38]. Among the 13 assembled dies, 11 dies survive testing for 190 hour. A1 was found open before vibration testing started and B3 was found to be open between 24 and 40 hour of testing. 10 more failures occur abruptly between 190 and 286 hour. The sudden surge of failures was likely due to the mounting screws that held the fixture coming loose during high temperature vibration, which allowed a new vibration mode.
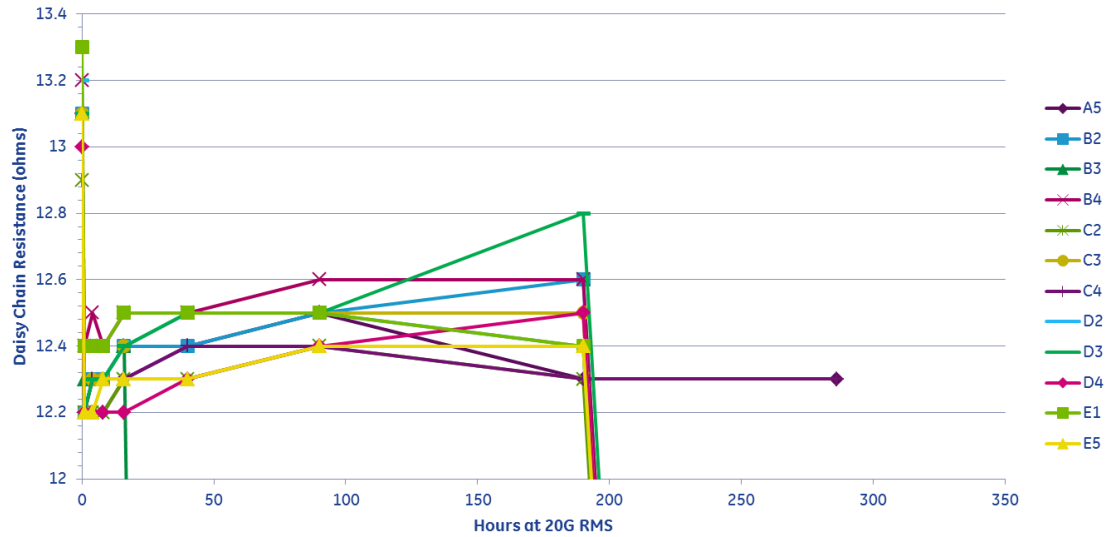
Figure 3.31 Daisy Chain Resistance as a Function of Aging Hour at 20G RMS at 300˚C
[38]

3.5   Summary

The flip chip thermocompression bonding process was selected for die assembly to avoid vibration concerns with wire bonding. What is more, flip chip bonding also provided reduced package size, lower cost for high volume automated production, large number of I/O and better electrical performance than wire bonding.

In the flip chip thermal aging test, shear strength remained stable through 2000h aging at 300˚C. In the flip chip thermal cycling test, a double bump configuration had been developed and evaluated. This double bump configuration potentially improved the thermal cycling performance of stud bump assembly. In the flip chip shock and vibration tests, before test fixture failed, all samples had excellent performance and met our expectation. Attention to fixture design is critical.

85

CHAPTER 4 HIGH TEMPERATURE ELECTRONICS PACKAGING

4.1   Introduction

The main goal of this project was to design and fabricate reliable packages for integrated digital circuits that could sense and transmit pressure measurements from measurement-while-drilling tools at temperature up to 300 ℃. The block diagram of the pressure sensing and transmitting process is shown in Figure 4.1. This project mainly focused on the telemetry module. The ultimate telemetry board was required to accept sensor data from 2 sensors, multiplexing the data and serializing the data out into a single data stream. The functional blocks of the telemetry board are shown in Figure 4.2.
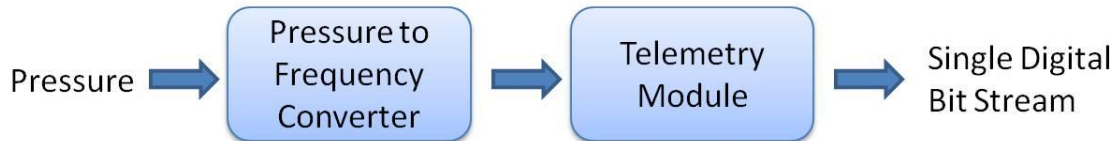
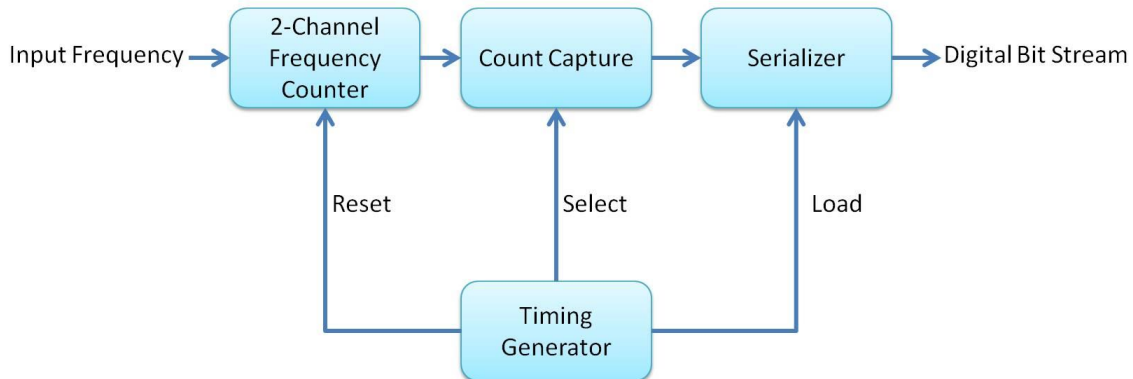Figure 4.1 Block Diagram of the Pressure Sensing and Transmitting Process

Figure 4.2 Functional Blocks of the Telemetry Board

The pressure-to-frequency converter provides a frequency output which is proportional to pressure. Therefore, the telemetry board in this project assumed that its frequency input is the frequency output of a pressure frequency converter.

As shown in the Figure 4.2, the first block of the telemetry system is a frequency counter or a frequency to digital converter. This frequency counter is built to convert the input frequency into a digital value. The counter is reset periodically and the count value is captured just prior to the performing of the reset operation.

The following block is a count capture block. This part is essentially a latching circuit which maintains the most recent count value of the frequency counter.

The last block is a serializer block. This serializer takes the input data from the count capture block and converts it into a serial bit stream.

An additional timing block was designed and built to generate the necessary reset and capture signals for all three blocks mentioned above. In the early design, there was no timing block on the digital board. These timing signals were generated off board. Initially, a breadboard version of each block was built and tested for functionality at room temperature at GE Global Research Center (GRC). The various circuit building blocks were packaged in DIP packages at Auburn University and used in the breadboard test structure at GE. This enabled easy access to internal circuitry and made circuit and topology modification much easier. Once the functional testing of each block and the circuit schematic was completed, the digital circuit boards for high temperature test were fabricated and assembled at Auburn University.

Totally, five kinds of digital circuit boards are fabricated at Auburn University and tested at GE Global Research Center. All designs were done by GE-GRC. They were first

generation frequency counter board; second generation frequency counter board; second generation timing generator board; third generation timing generator board; and third generation telemetry board.

4.2 First Generation Frequency Counter Board

The 1st Gen frequency counter board was comprised of two SiC based four-bit counter dies and a data latch. To simplify the substrate fabrication, the design was accomplished with a single metallization layer. Twelve thin film jumpers are used to provide electrical cross-overs.

The fabrication process of the substrate was the same process described in Chapter 2. Once the substrate was fabricated, it was cleaned in the YES-500 argon plasma cleaner. Then the pattern for the jumpers was stud bumped on the substrate with the Palomar 2460 Model V automatic Au thermosonic wire bonder. The distance between two stud bumps was about 12 mil, as shown in Figure 4.3. The AlN thin film jumper was also fabricated with our standard fabrication process. It had the Ti/TiW/Au seed layer and 1.5μm electroplated gold on it. The size of the thin film jumper was 127mil by 63mil, as shown in the Figure 4.4.
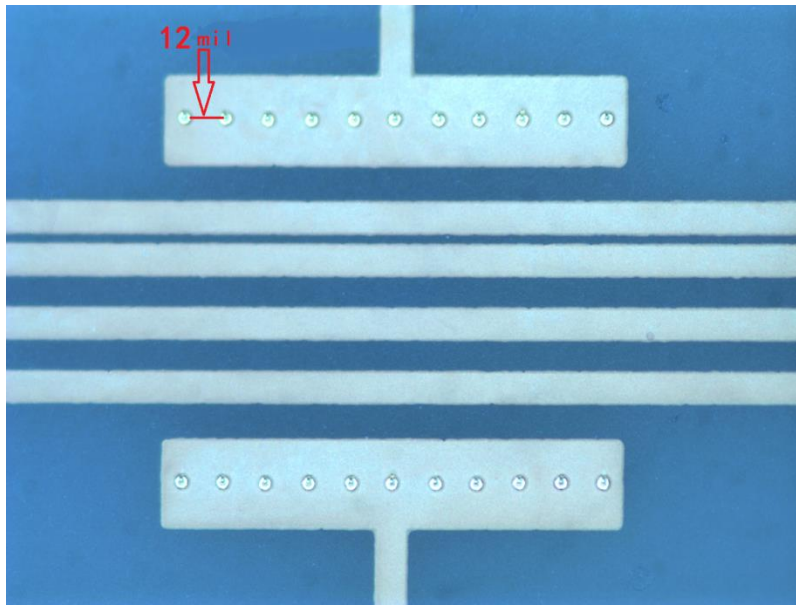
Figure 4.3 Stud Bumps on Pads for Thin Film Jumper
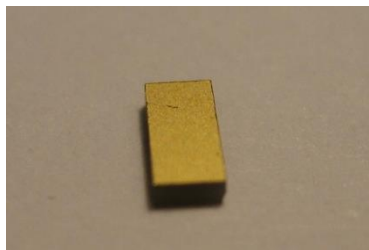
Figure 4.4 Thin Film Jumper

All of the digital dies were designed and fabricated at GE Global Research Center, then shipped to Auburn University in wafer form. All the digital dies on the wafer were stud bumped and diced into individual dies according to a map provided by GE-GRC. Because those digital dies were ESD sensitive, an ESD lab coat, an ESD wrist strap and ESD tweezers were used when handling the dies. These ESD-safe precautions were also used after the assembly was completed.

Finally, digital dies and jumpers were thermocompression bonded to the corresponding pattern on the substrate using a SETI FC 150 flip chip bonder. The layout and the assembled board are shown in Figure 4.5 [38] and Figure 4.6. The bonding profile

was the same as the one used for flip chip aging test except the maximum bonding force is changed. 100 gram force per stud bump was always applied. So the total bonding force was adjusted according to the total number of stud bumps on the die. For example, there were 19 stud bumps on the 4-bit counter die and 17 stud bumps on the d-latch die, so the bonding force for each was 1900g and 1700g, respectively.
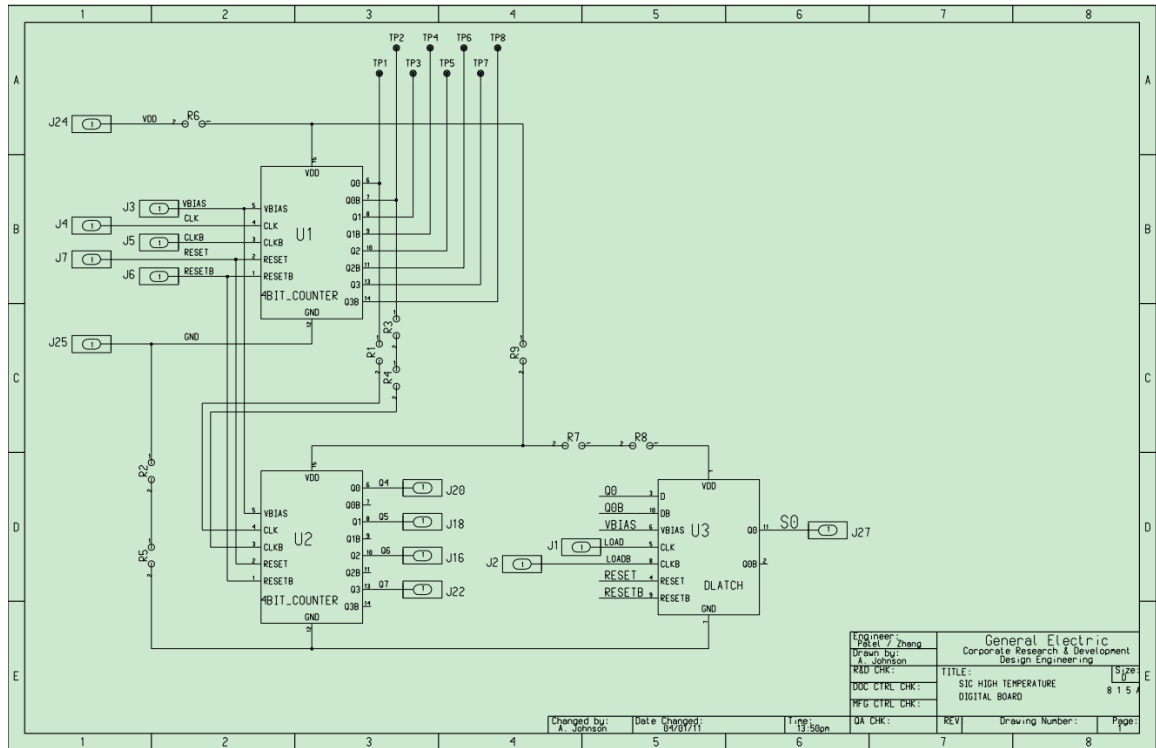
Figure 4.5 Layout of First Generation Frequency Counter Board [38]
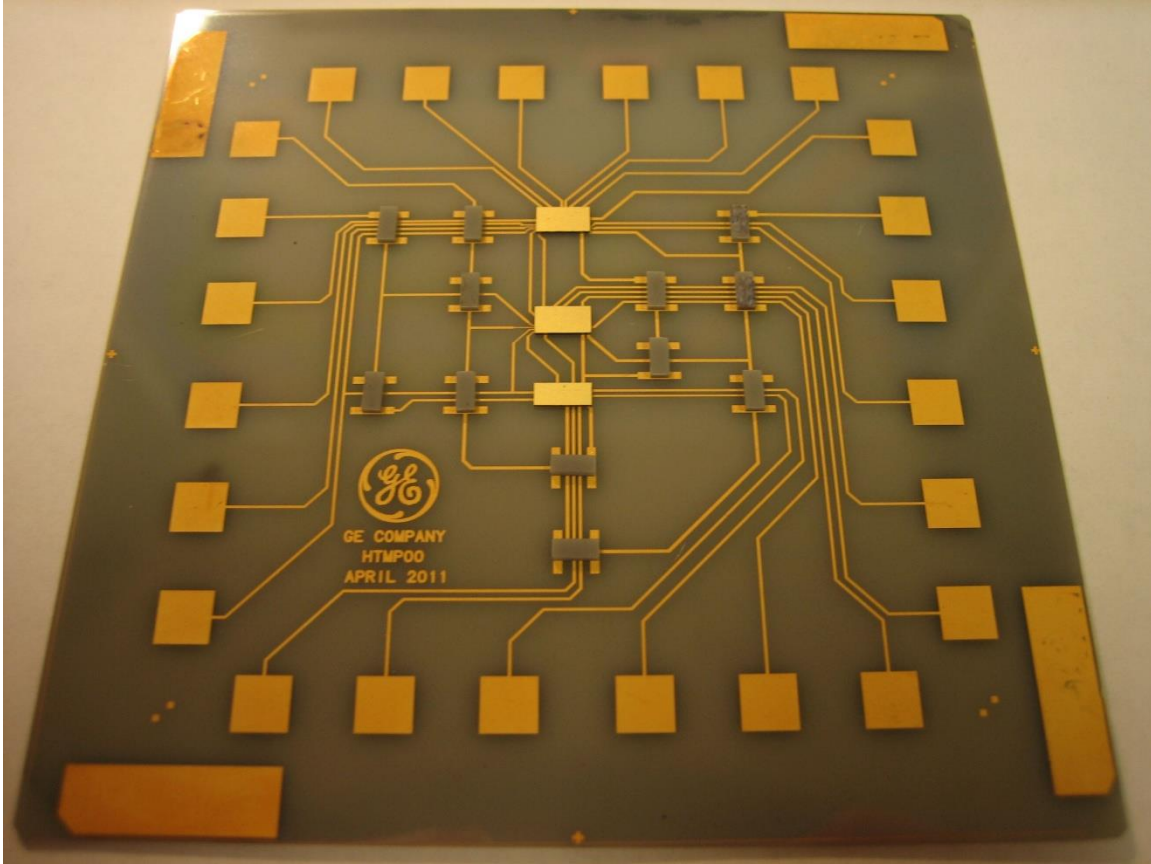
Figure 4.6 First Generation Frequency Counter Board

The board was then sent to GE-GRC for testing. The room temperature and 300 ℃ test results are shown in Figure 4.7 and Figure 4.8 [38]. During testing, it was observed that there was clock-feed through to the Q0 of the 4-bit counter. Therefore, Q1 would divide Clk by 2, Q2 by 4 and Q4 by 8. The 4-bit counter would divide the clock frequency by 8 instead of 16. According to GE's failure analysis, this was due to manufacturing issue in the chip fabrication process.
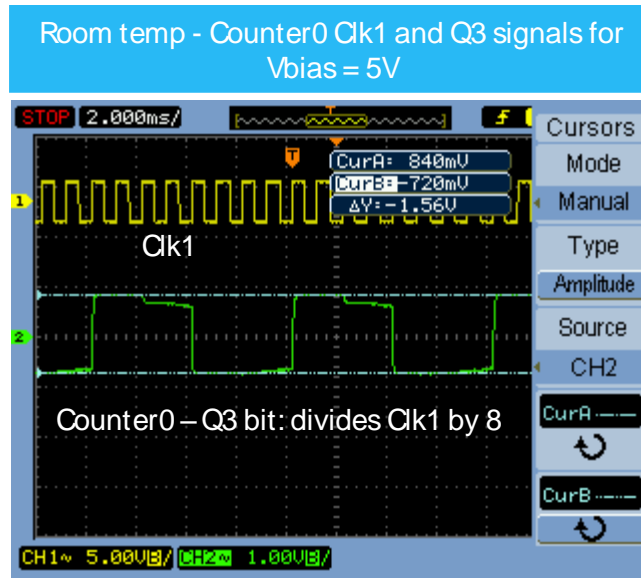
Figure 4.7 Room Temperature Test Result (VDD = 18V, VSS = 0V, Vbias = 5V, Vresetb = 10V, and Vreset = 6V) [38]
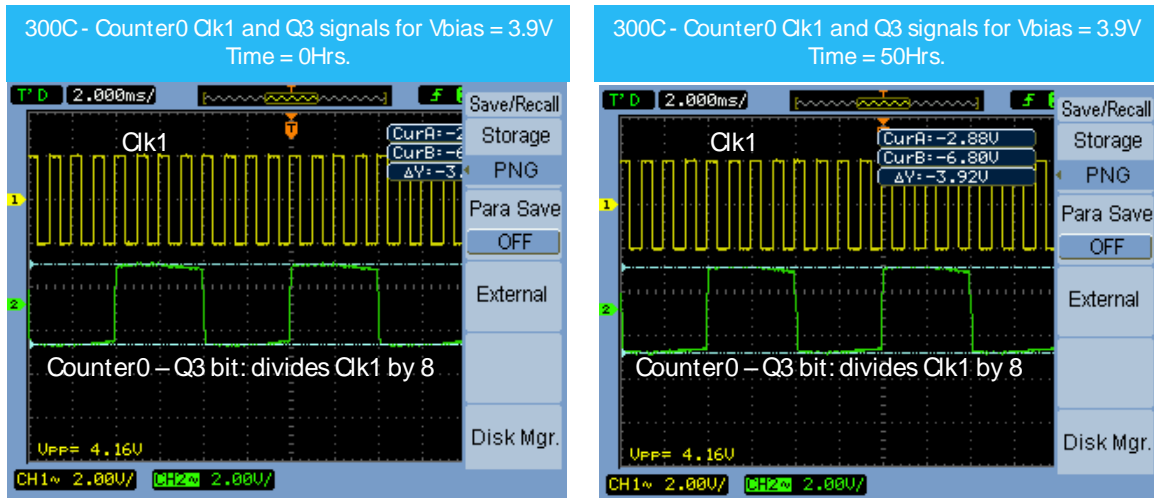
Figure 4.8 Test Result at 300 ℃ (VDD = 18V, VSS = 0V, Vbias = 3.9V, Vresetb = 10V, and Vreset = 6V [38]

To study the long-term reliability of the frequency board at 300 ℃, the board was thermal aged in an oven after the initial test. The board demonstrated stable operation after 500 hours of continuous operation at 300 ℃. There was no change in functionality of peak-peak counter bits. The testing results are shown in Figure 4.9 [38].
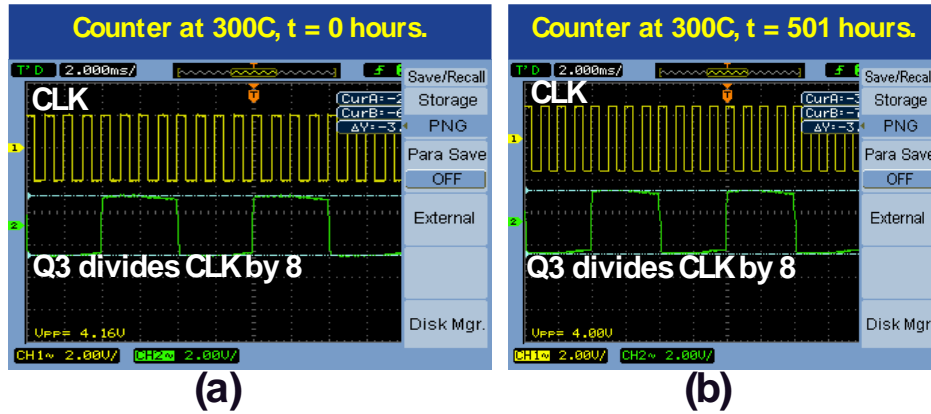
Figure 4.9 Measured Response of Counter Board at 300 ℃ (a) Before Temperature Stress (b) After 501hr of Operation at 300 ℃ [38]

4.3   Second Generation Frequency Counter Board

The 2nd Gen frequency counter board had one 4-bit counter, one shift register and one buffer. It also had a single metallization layer on the AlN substrate. All cross-overs were achieved with 6 jumpers thermocompression bonded on the substrates. The schematic of the 2nd Gen frequency counter board is shown in Figure 4.10 [39]. A sensor output frequency was feed into the clock of the 4-bit counter and was converted into the digital counts. At a specific load time, these digital counts pass through a shift register and were converted into a single bit stream.
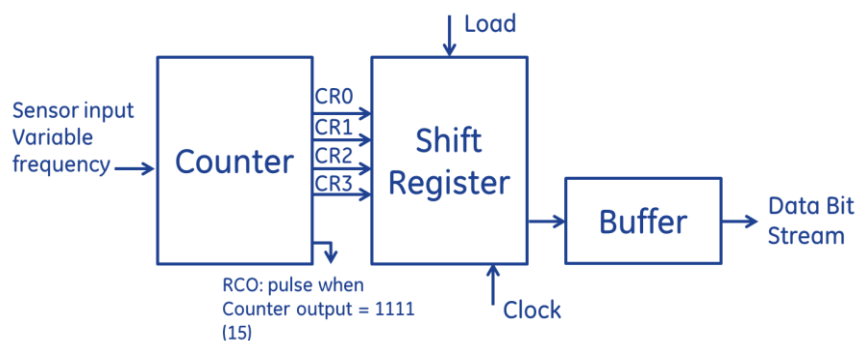
Figure 4.10 Schematic of Second Generation Frequency Counter Board [39]

93

Totally three frequency counter board were fabricated and assembled. The layout and the assembled board are shown in Figure 4.11 [38] and Figure 4.12 [39]. The functionality of these three boards is evaluated with a 1kHz clock signal into the 4-bit counter. None of the boards was fully functional. After failure analysis, the GE team realizes that one of six jumpers failed to provide a good electrical cross-over. The VDD was shorted to the SRR1. This might be caused by a parallelism issue in the flip chip bonding process. If the thin film jumper is not perfectly parallel to the AlN substrate, the conductive layer on the bottom of the jumper may contact the trace under it. The failed jumper location was in the same on all boards, as shown in the red circle in Figure 4.12.
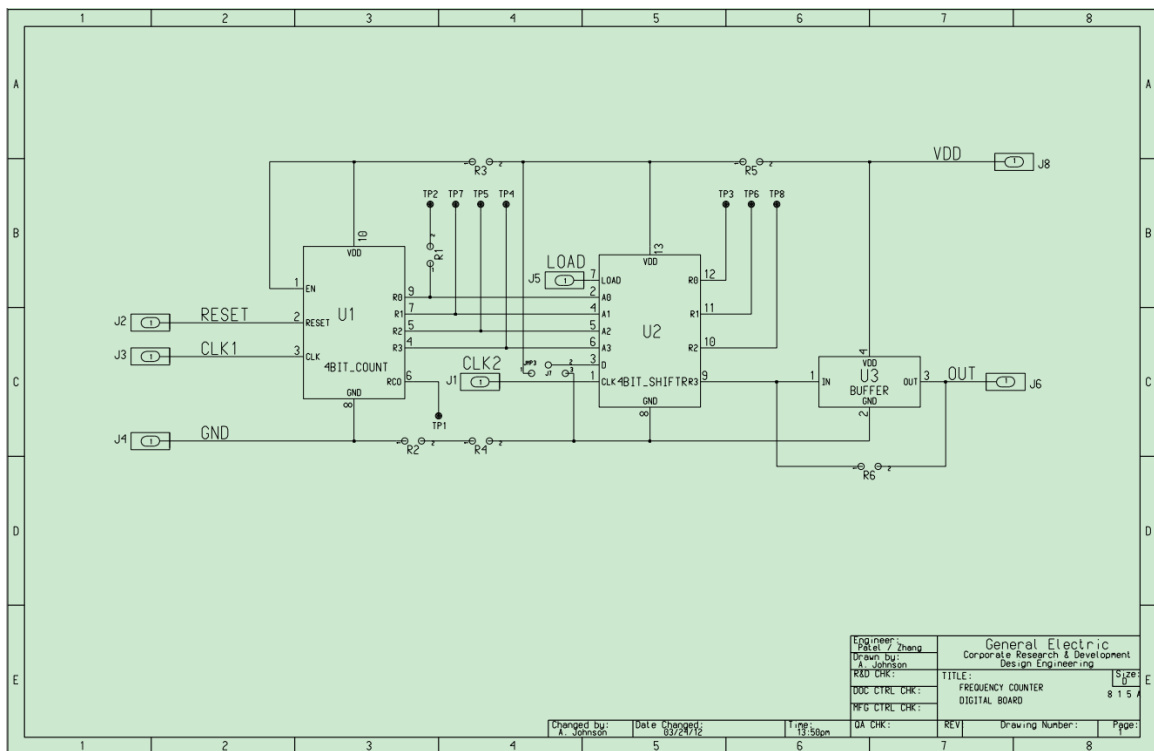
Figure 4.11 Layout of Second Generation Frequency Counter Board [38]
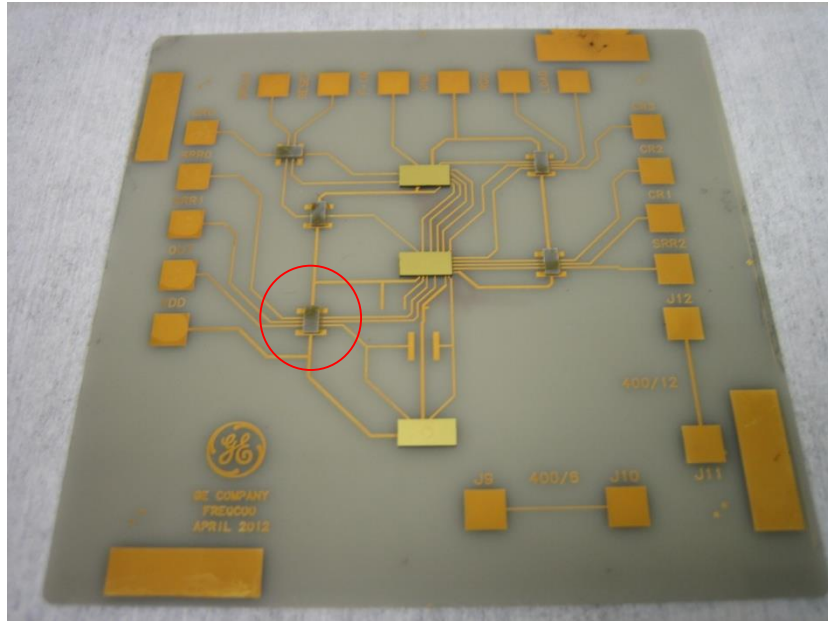
Figure 4.12 Second Generation Frequency Counter Board [39]

Although this jumper issue prevented the shift register from working properly, the 4-bit counter was fully functional. Therefore, the GE team decided to keep evaluating the function of the 4-bit counter. The output results of the counter at room temperature and 300 ℃ are shown in Figure 4.13 and Figure 4.14 [40]. In the output waveform, the 1kHz clock signal is converted into digital counts. CR0 is the least significant bit, followed by CR1, CR2 and CR3. Due to a limitation in the maximum number of oscilloscope channels available, only CR0, CR2 and CR3 with frequency of 500Hz, 125Hz and 62.5Hz are shown in the Figure 4.13 and Figure 4.14 [40].
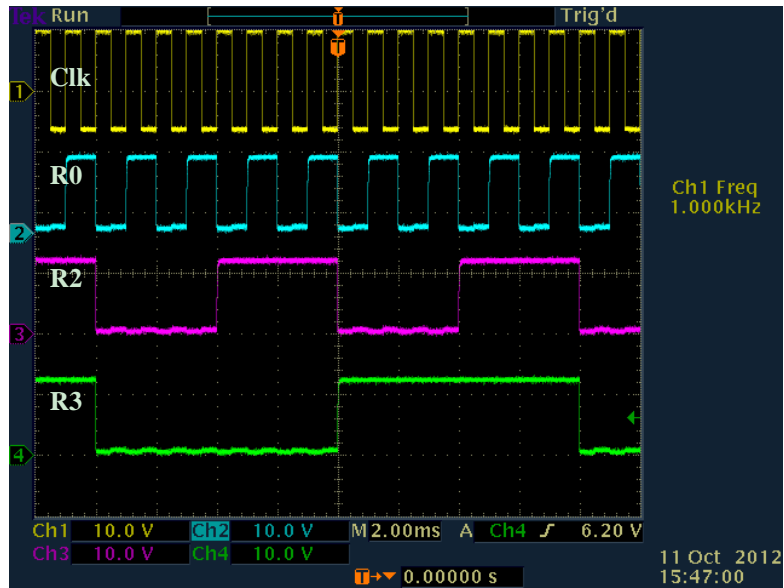
Figure 4.13 Initial Test Result of 4-bit Counter at Room Temperature [40]
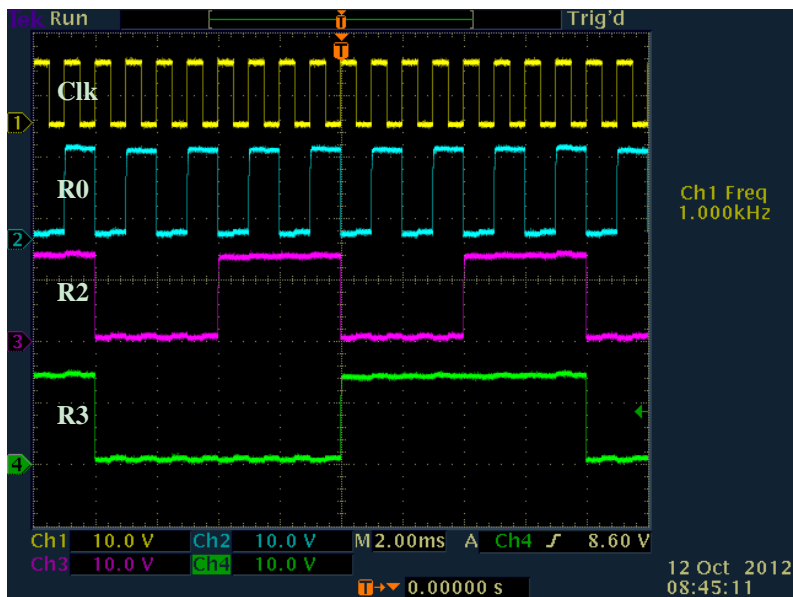
Figure 4.14 Initial Test Result of 4-bit Counter at 300 ℃ [40]

After the initial functional test of the frequency board at 300 ℃, long term stability test was conducted on these three boards. The counters on all these boards were fully functional after 400hr aging at 300 ℃. After this, different reliability tests are conducted on different boards.

For Board 1, vibration reliability test was performed on it after 400hr aging at 300 ℃. The board was subjected to random vibration testing at 20G RMS level at 300 ℃. The electrical functionality of the counter was measured at 4hr, 8hr and 40hr intervals. The device survived after 16hr testing, but partially failed after 40hr vibration testing. The failure analysis of the 4-bit counter was conducted and the failure was speculated to be on the SiC circuit die itself rather than the packaging. Note the project goal for vibration reliability was to survive the random vibration for 4 hours at 300 ℃. The output waveform of the counter after 8hr of vibration testing is shown in Figure 4.15 [40].

Figure 4.15 Functional Test Result (CLK, CR3 and RCO) of 4-bit Counter after 400hr aging and 8hr random vibration at 300 ℃ [40]

For Board 2, the aging test was continued to 1050hr. The output waveform of the sample as built and after 1050hr aging are shown in Figure 4.16 and Figure 4.17 [40]. It is clear that after 1050hr aging at 300 ℃, the board was partially functional with distorted output waveform.
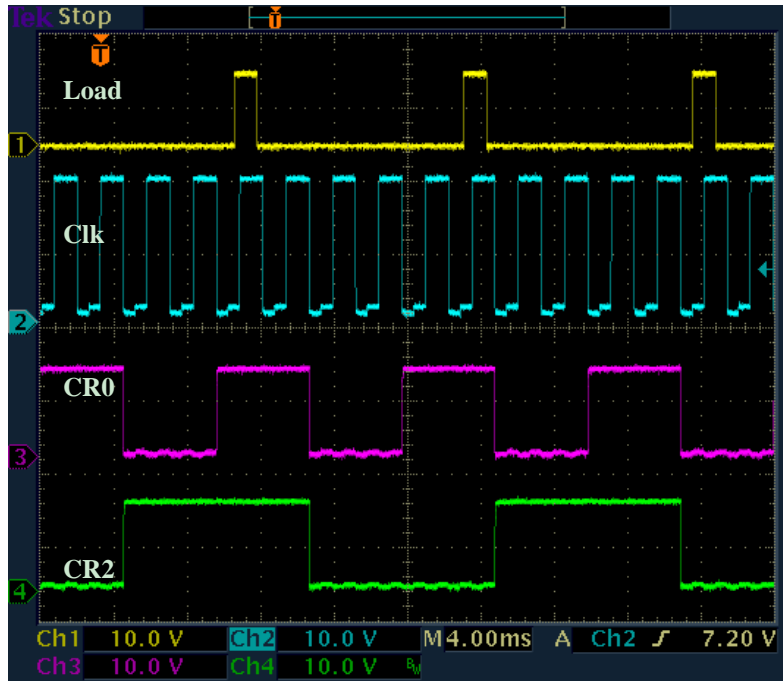
Figure 4.16 Functional Test Result of Sample as Built [40]
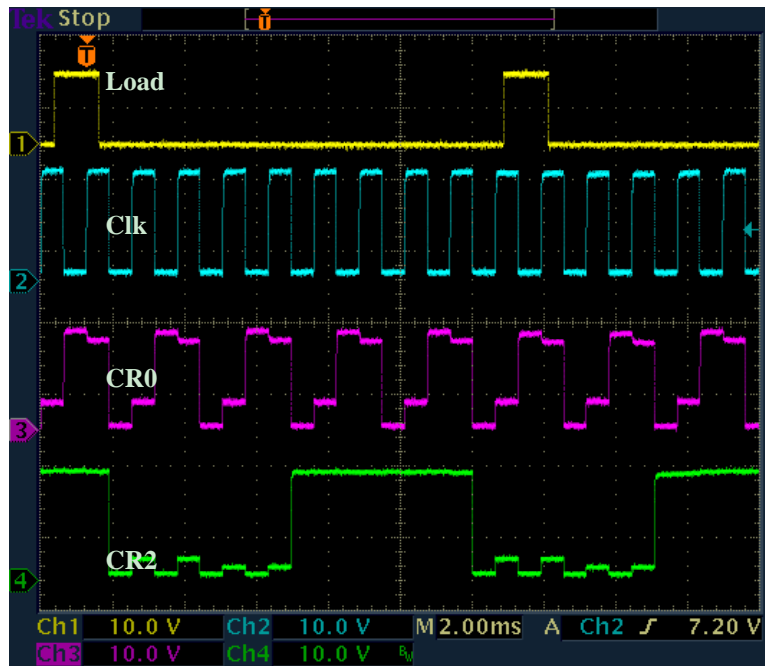
Figure 4.17 Functional Test Result of Sample after 1050hr Aging at 300 ℃ [40]

The Board 3 was subjected to mechanical shock testing at 215G level at 300 ℃, using the same shock testing system described in Chapter 3. The shock testing was

interrupted after 2, 20, 50, 200, 400, 600, 800, and 1000 shocks. At each interval, the board was cooled down and dissembled from the hold in the shaker. Then the electrical performance of the board was tested at room temperature. The board was still fully functional after 1000 shocks. The output waveforms after 1000 shocks are shown in Figure 4.18 [40].
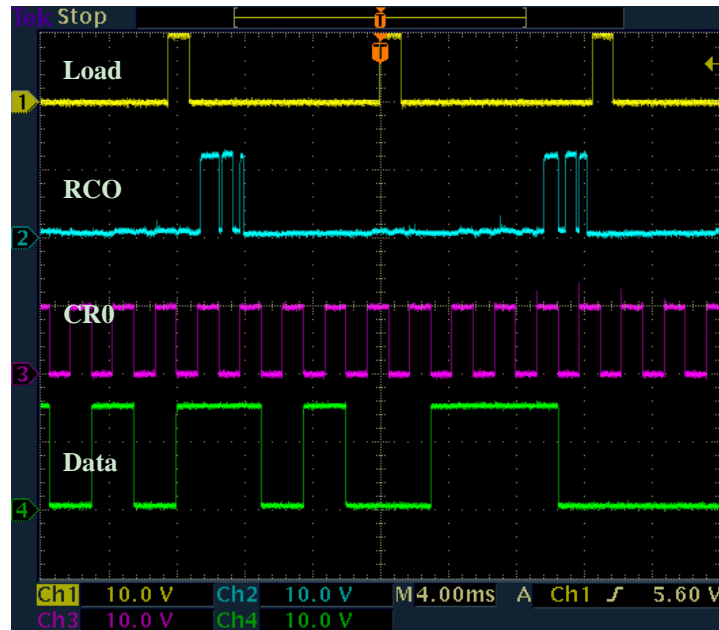
Figure 4.18 Functional Test Result after 400hr aging and 1000 mechanical shocks at 300 °C [40]

4.4 Second Generation Timing Generator Board

The 2nd Gen timing generator board was a multilayer board with two 4-bit counters and two 8-bit comparators. The multilayer structure, including the bottom metal layer, dielectric layer and the top metal layer, interconnects multiple SiC devices without thin film jumpers. The layout and the assembled board are shown in Figure 4.19 [38] and Figure 4.20.
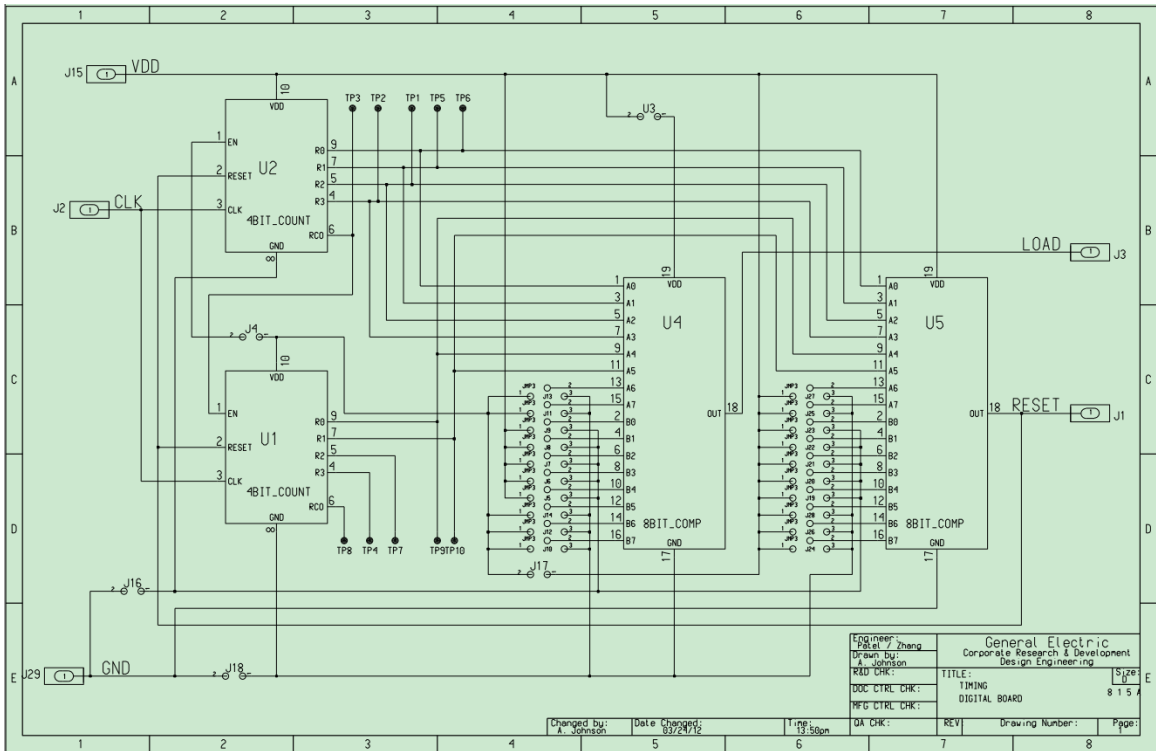
Figure 4.19 Layout of Second Generation Timing Generator Board [38]
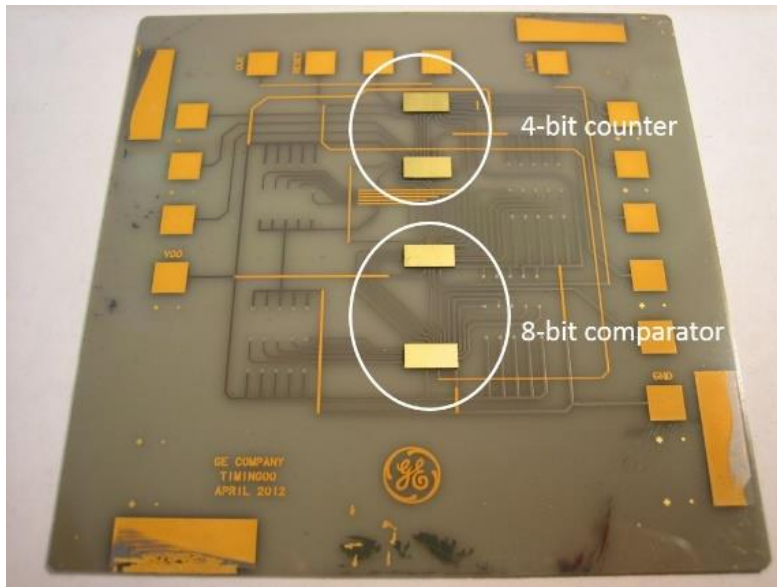
Figure 4.20 Second Generation Timing Generator Board

This board was fabricated and assembled at Auburn University and shipped to GE global research center for electrical testing. The electrical testing result of the multilayer

timing board showed that there were electrical shorts in the cross-over area between bottom

metal trace and the top metal trace, as shown in Figure 4.21. In order to identify where the

short was, the board was shipped back to Auburn University and break down testing was

performed.
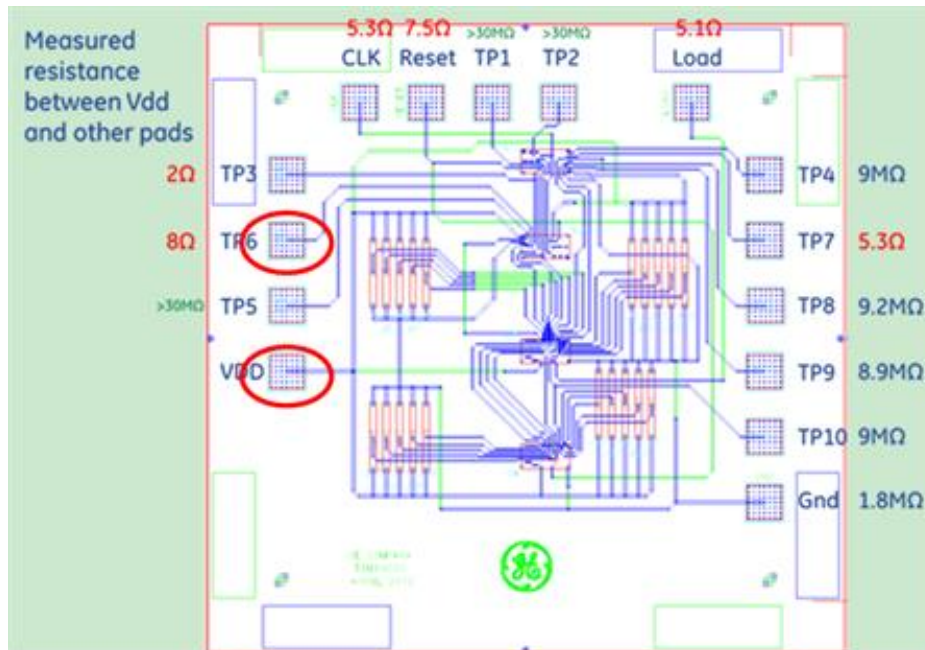
Figure 4.21 Locations of Electrical Shorts

This testing was performed with a probe station and a voltage supply (0-150V, 0-

20A). At the beginning, a voltage was applied to VDD and TP6. The voltage was then

gradually increased. When the leakage current reached about 5A, an electrical arc appeared

in the cross-over area, as shown in Figure 4.22. According to the result, the break down

point was on the edge of the bottom trace. The metal around the break down point was melt

by the high temperature produced by the electrical arc. The location of the break down

point should also be the location of the electrical short.
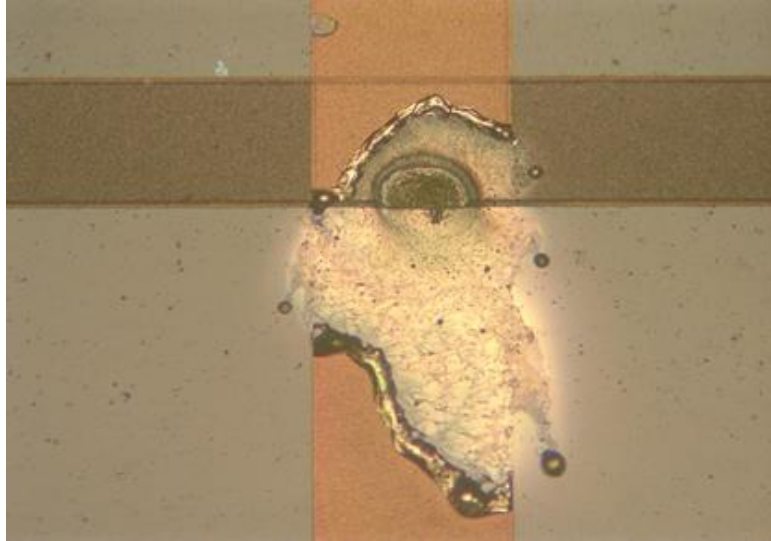
Figure 4.22 Location of Electrical Break Down

It is possible that the edge of the bottom trace was very rough and some spike on the edge penetrated the dielectric layer and caused the electrical short. In order to prove our hypothesis, the thickness of a bottom metal trace was measured by the profilometer. As shown in Figure 4.23, the edge of the trace was sharp and the height of edge was larger than that of the center. It was highly possible that those sharp plating wings on both sides of traces could easily penetrate 1.5μm Si_3N_4 dielectric deposited on the bottom metal layer.
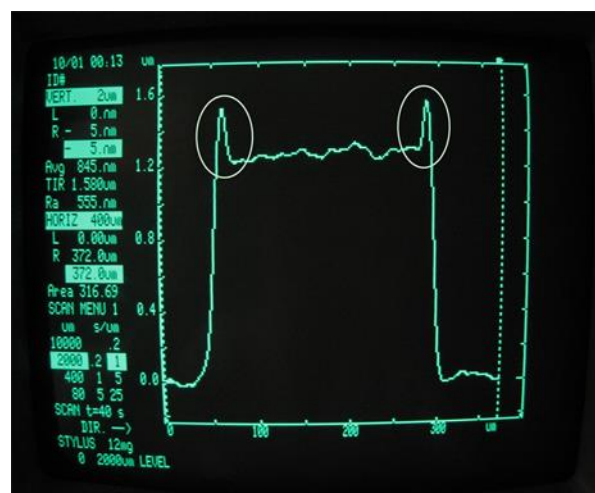
Figure 4.23 Image of Plating Wings under Profilometer

What was more, one substrate (with bottom metal layer and dielectric layer) was carbon coated and examined with an SEM. Two bright lines were observed on the edge of the trace, as shown in Figure 4.24. The bright lines were the plating wings penetrating into the dielectric layer. This was the root cause of electrical short on the edge. This issue was solved by the over etching process described in Chapter 2.
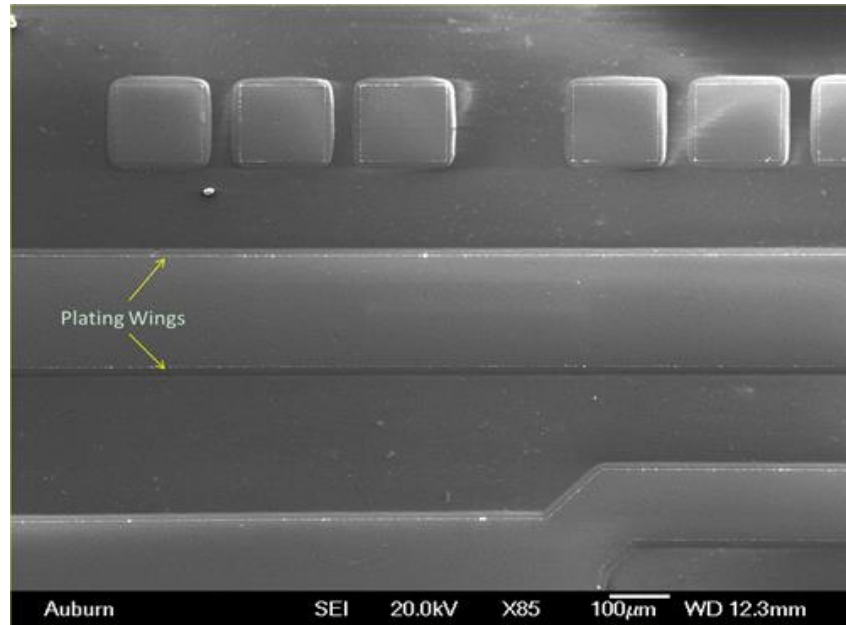
Figure 4.24 Image of Plating Wings under SEM

4.5   Third Generation Timing Generator Board

The 3rd Gen timing generator board was a single metallization layer board with only one digital die on it. The timing generator die used on the board was a highly integrated functional die that contains an 8-bit counter (consists of two 4-bit counters), a D-flipflop and some dedicated logic gates to generate timing pulses for the two 4-bit counters. The block diagram of the timing generator die is shown in Figure 4.25 [41].
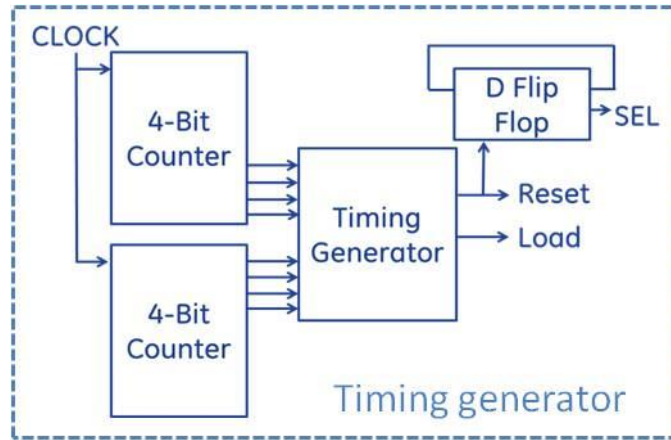
Figure 4.25 Block Diagram of Timing Generator Die [41]

The 6mm by 6mm SiC digital die was thermocompression bonded to the AlN substrate. The assembled circuit board is shown in Figure 4.26.
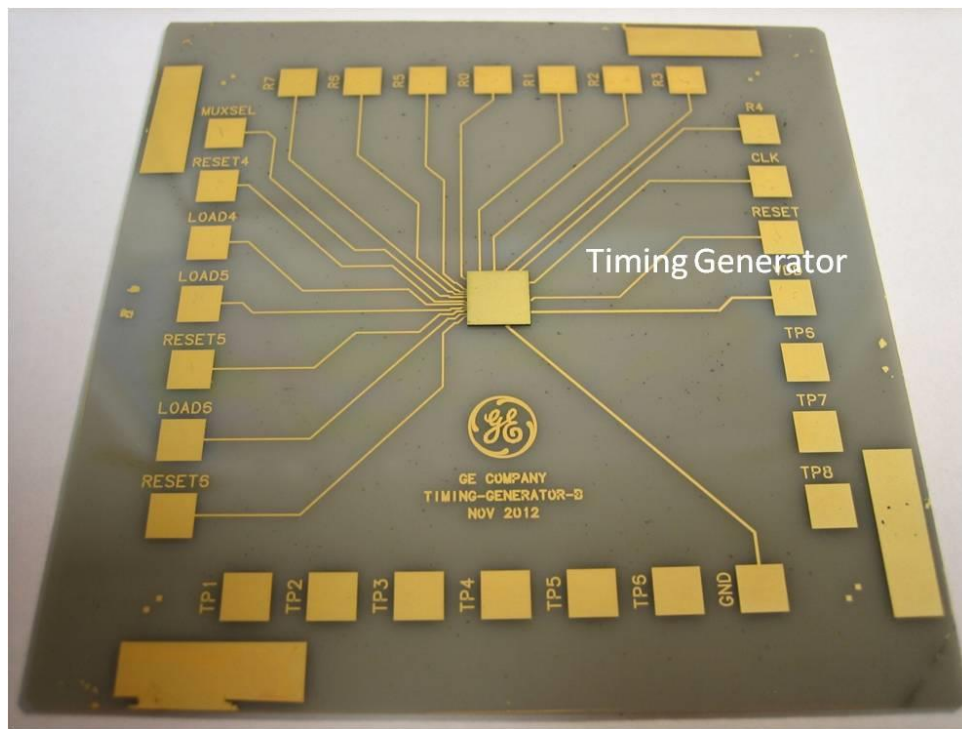
Figure 4.26 Third Generation Timing Generator Board

The board was thermal aged in an oven and operated for 2000hr at 300 ℃. The initial waveform and the waveform after 2000hr aging are shown in Figure 4.27 [41]. Based on the test result, no change in functionality and waveform was observed after aging. CLK

is the input clock signal produced by a function generator and R4 is the circuit output from the counter frequency divider that divides the CLK frequency by 32. Load is the output signal that tells the telemetry module when to sample the frequency count provided by frequency counter. Select is an output signal that toggles between tow analog sensor channels.
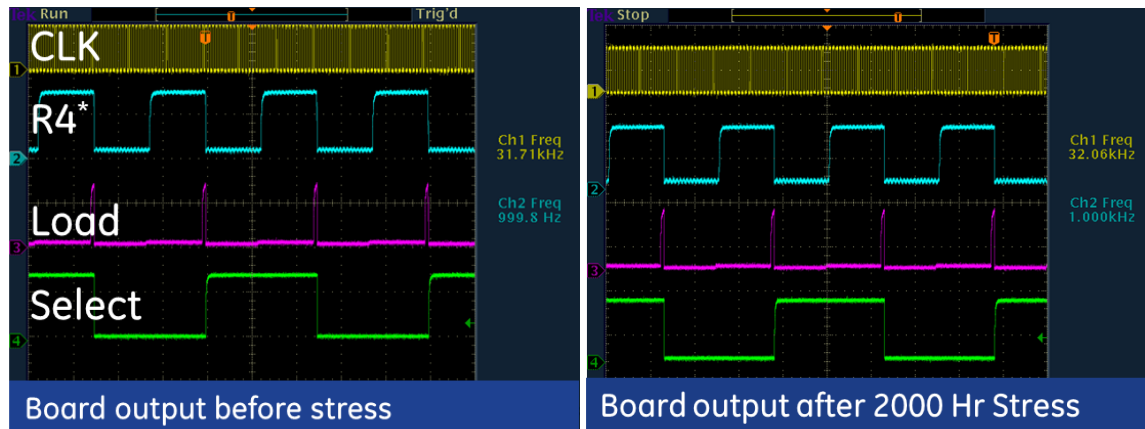
Figure 4.27 Functional Test Result before and after High Temperature Operation for 2000hr at 300 ℃ [41]

4.6   Third Generation Telemetry Board

When the frequency counter board and the timing generator board had been proven fully functional, three telemetry boards were assembled at Auburn University. In this design, a 8–bit frequency counter die, a timing generator die and a buffer die were assembled on an AlN substrate with a single metallization layer. The layout and the assembled substrates are shown in Figure 4.28 [38] and Figure 4.29.
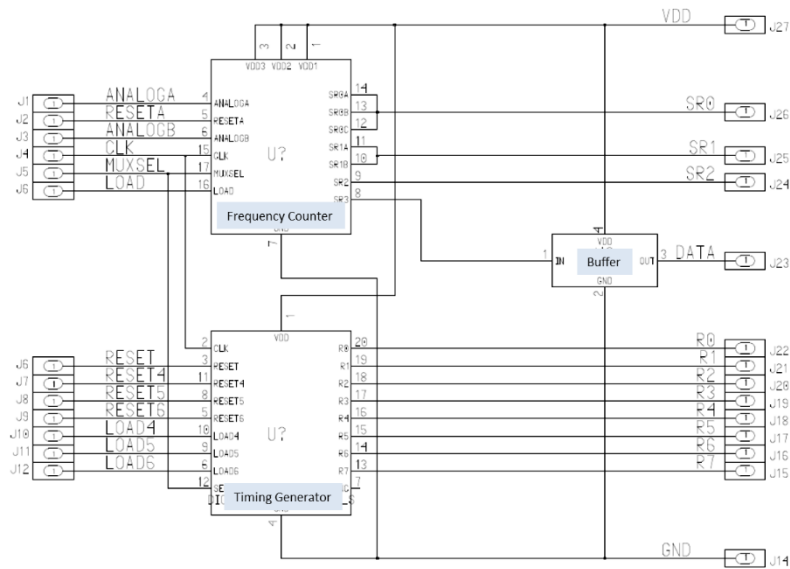
Figure 4.28 Layout of Third Generation Telemetry Board [38]
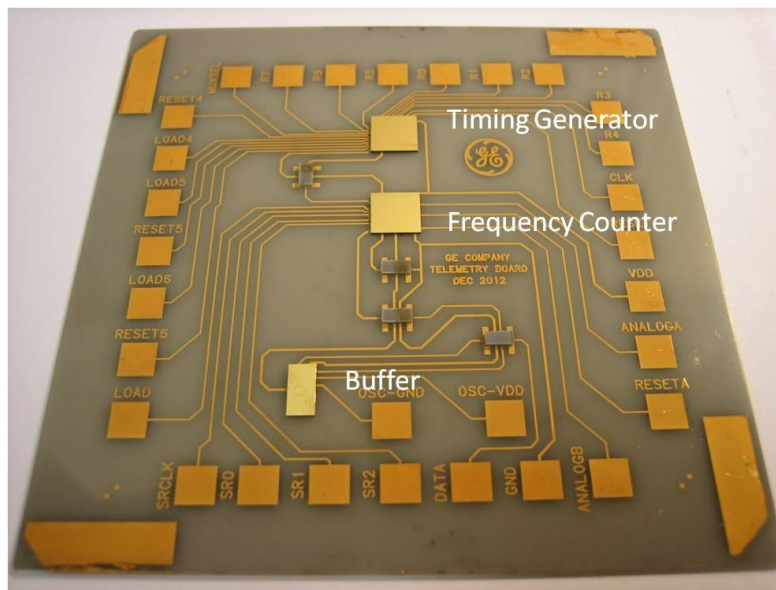
Figure 4.29 Third Generation Telemetry Board

The frequency counter die realized the function of two 4-bit frequency counters, a multiplexer and a shift register, as shown in Figure 4.30 [41]. The buffer die was used to temporarily store the count data from the shift register in the frequency counter die. The timing generator die took a clock input and generated the load and reset signals for the shift register inside the frequency counter die. It provided a select signal to control the

106

multiplexer to select data from two frequency input channels. The block diagram of the timing generator die is shown in Figure 4.31 [41].
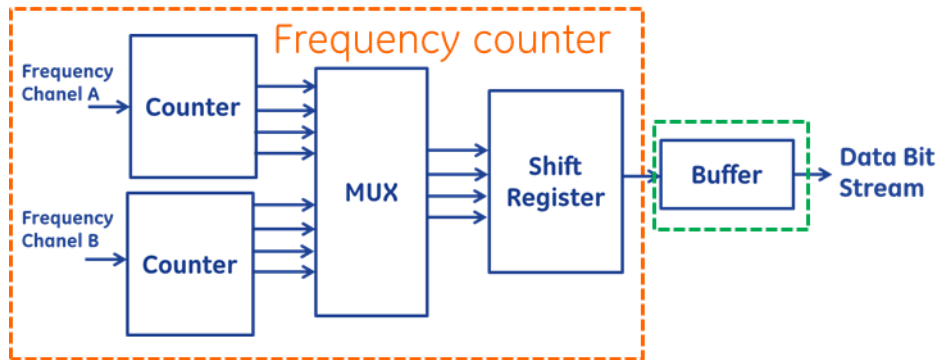
Figure 4.30 Block Diagram of the Frequency Counter Die [41]
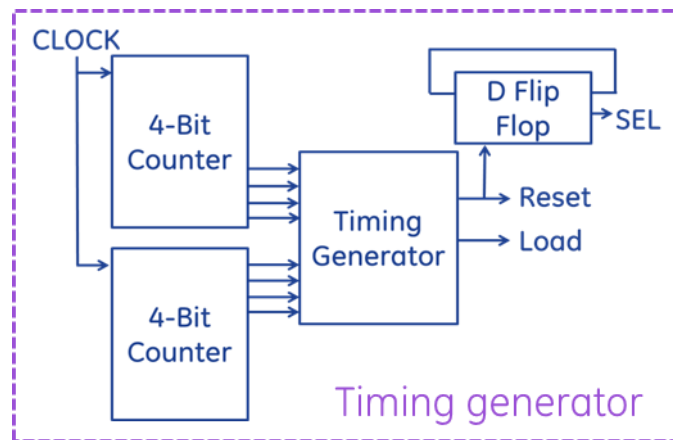
Figure 4.31 Block Diagram of the Timing Generator Die [41]

The initial test of these boards was performed at 300 ℃ in GE-GRC. In the test, square waves with the same frequency were sent into the two frequency input channels of the board. By changing the input frequency (from 10Hz to 2kHz), 16 consecutive states (from 0000 to 1111) were generated through the bit stream output. Then the high temperature stability test was conducted on the same board at 300 ℃. During the first 100hr of continuous operation, the telemetry board worked properly.

CHAPTER 5 CONCLUSION AND FUTURE WORK RECOMMENDATION

5.1 Thin Film Technology for High Temperature Application

A multilayer thin film substrate technology has been developed to interconnect multiple SiC devices on an AlN substrate. The conductor is vacuum deposited Ti/Ti:W/Au followed by an electroplated Au. A PECVD silicon nitride is used for the interlayer dielectric.

The multilayer structure showed excellent adhesion through 2000h aging at 300 ℃. Electrical testing of silicon nitride proved the suitability of Si3N4 as a high temperature multilayer insulation. Its electrical performance was stable and consistent during 2000h aging at 300 ℃. In the thermal aging test with 20V bias of the silicon nitride, partial discharges in the dielectric were observed in some samples. Each discrete discharge is the result of an electrical breakdown of an internal void or defect within the dielectric. Improvements in PECVD silicon nitride manufacturing process are needed.

5.2 Flip Chip Attach for High Temperature SiC Based Devices

The flip chip thermocompression bonding process was selected for die assembly to avoid vibration concerns with wire bonding. In the flip chip thermal aging test, flip chip bonding process has been fully demonstrated. The shear strength remained stable through 2000h aging at 300˚C. In the flip chip thermal cycling test, besides the single bump configuration, a double bump configuration has also been developed and evaluated. Based on early thermal cycling data, the double bump configuration potentially improved the thermal cycling performance of stud bump assembly. In the flip chip shock and vibration

testing, before the test fixture failed, all samples had excellent performance and met our expectation.

5.3 High Temperature Electronics Packaging

Four kinds of integrated digital circuit boards with single layer metallization were assembled and tested. These boards included first generation frequency counter board, second generation frequency counter board, third generation timing generator board and third generation telemetry board. The single layer structure has been fully demonstrated. In the multilayer timing generator board, the plating wing issue has been discovered and solved. The substrate fabrication process has been greatly improved.

5.4 Recommendations for Future Work

Based on the test results presented in this dissertation, some recommendations for future work are:

In the electrical testing of silicon nitride, the leakage current of the capacitor, the comb pattern and the cross-over pattern decreased after 500 or 1000hr aging at 300˚C and were stable with additional aging. The insulation property of silicon nitride improvement with aging at 300˚C was not expected. This anomalous phenomenon needs to be studied and evaluated. In the next step, more analysis could be performed on silicon nitride as built and after 2000h thermal aging to determine the mechanism for this improvement. Furthermore, it could be very interesting to continue the thermal aging beyond 2000hr and determine if the dielectric starts to deteriorate.

In the electrical testing of the silicon nitride, the partial discharge was noticed in the dielectric layer. The discharge eroded the dielectric layer and caused a larger leakage current. An extended study would be of interest to optimize the PECVD deposition process

109

of the silicon nitride. The partial discharge can be eliminated by depositing a defect free PECVD silicon nitride layer.

In the flip chip thermal cycling test, a double bump configuration was developed to improve the thermal cycling performance of the stud bump assembly. Double bumps increased the height of the gap which decreased the strain on the interconnection between SiC die and AlN substrate. The thermal cycling test is still onging. More research is needed to determine if the double bump configuration indeed improves the thermal cycling performance of flip chip assembly.

REFERENCES

[1] C. Johnston, A Crossley, and R. Sharp, "The possibilities for high temperature electronics in combustion monitoring," Proc. Advanced Sensors and Instrumentation Systems for Combustion Processes, 2000, pp. 9/1 –9/3

[2] R. Normann, "First High-Temperature Electronics Products Survey 2005", Sandia National Laboratories

[3] R. Kirschman, "High Temperature Electronics", Wiley-IEEE Press, August 18, 1998

[4] P. L. Dreike, D. M. Fleetwood, D. B. King, D. C. Sprauer and T. E. Zipperian, "An overview of high-temperature electronic device technologies and potential applications", Components, Packaging, and Manufacturing Technology, Part A, IEEE Transactions on (Volume:17, Issue: 4)

[5] Geothermal Energy Association (GEA). 2013. Geothermal: International Market Overview Report

[6] U.S. Energy Information Administration (EIA). 2012. International Energy Statistics. Renewables: Electricity Generation: Geothermal

[7] How Geothermal Energy Works. (n.d.). Retrieved June 13, 2015, from http://www.ucsusa.org/clean_energy/our-energy-choices/renewable-energy/how-geothermal-energy-works.html#.VXxZDvlVhBc

[8] Casey Research, "A Hot Future for Geothermal"

[9] Massachusetts Institute of Technology, "The Future of Geothermal Energy: Impact of Enhance Geothermal Systems (EGS) on the United States in the 21st Century", 2006

[10] How Does Measurement-While-Drilling (MWD) Work? (n.d.). Retrieved June 13, 2015, from http://www.rigzone.com/training/insight.asp?insight_id=296&c_id=1

[11] F. Ng, "Recommendations for MWD Tool Reliability Statistics," SPE Annual Technical Conference and Exhibition (1989)

[12] Materials for high-temperature semiconductor devices. Washington, D.C.: National Academy Press, 1995

[13] V. V. Shields, "Applications of Silicon Carbide for High Temperature Electronics and Sensors"

[14] P. G. Neudeck and L. G. Matus, An overview of silicon carbide device technology. Washington, DC: National Aeronautics and Space Administration; 1992

[15] M. Willander, M. Friesel, Q.-U. Wahab, and B. Straumal, "Silicon carbide and diamond for high temperature device applications," Journal of Materials Science: Materials in Electronics J Mater Sci: Mater Electron, pp. 1–25

[16] G.A. Slack, R.A. Tanzilli, R.O. P ohl and J.W. Vandersande, "The intrinsic thermal conductivity of AIN", Journal of Physics and Chemistry of Solids Volume 48, Issue 7, 1987, Pages 641–647

[17] Advanced Materials & Powders Handbook, from

http://www.anceram.com/pdf/aln_artikel_bull.pdf

[18] "Silicon Carbide, SiC Ceramic Properties," Silicon Carbide SiC Material Properties. [Online]. Available at: http://accuratus.com/silicar.html. [Accessed: Mar-2015]

[19] "Aluminum Oxide, Al$_2$O$_3$ Ceramic Properties," Aluminum Oxide. [Online]. Available at: http://accuratus.com/alumox.html. [Accessed: Mar-2015]

[20] "Aluminum Nitride, AIN Ceramic Properties," Aluminum Nitride. [Online]. Available at: http://accuratus.com/alumni.html. [Accessed: Mar-2015]

[21] "Compressive (Crushing) Strength of Beryllia (Beryllium Oxide, BeO)," Beryllia (Beryllium Oxide, BeO) Material Properties. [Online]. Available at: http://www.makeitfrom.com/material-properties/beryllia-beryllium-oxide-beo/. [Accessed: 2015]

[22] S. Gasser, "High-temperature contact metallization to semiconductors," 1998 High-Temperature Electronic Materials, Devices and Sensors Conference (Cat. No.98EX132)

[23] T. L. Chu, "Dielectric Materials in Semiconductor Devices", J. Vac. Sci. Technol. 6, 25 (1969)

[24] R. A. Levy, Microelectronic materials and processes: proceedings of the NATO Aadvanced Study Institute on Microelectronic Materials and Processes, Il Ciocco, Castelvecchio Pascoli, Italy, June 30-July 11, 1986. Dordrecht: Kluwer Academic, 1989

[25] S. Diaham, M.-L. Locatelli, and Z. Valdez-Nav, "Dielectrics for High Temperature SiC Device Insulation: Review of New Polymeric and Ceramic Materials," Silicon Carbide - Materials, Processing and Applications in Electronic Devices, 2011

[26] Wire Bonding Process, http://www.siliconfareast.com

[27] G. A. Riley, "Stud Bump Flip Chip," Flipchips.com, Jan-2000

[28] H. Tong, "Advanced flip chip packaging", New York: Springer, 2013

[29] E. Suhir and Y. C. Lee, Micro- and Opto-Electronic Materials and Structures: Physics, Mechanics, Design, Reliability, Packaging. Boston, MA: Springer Science Business Media, LLC, 2007

[30] A. Elshabini and F. D. Barlow, Thin film technology handbook. New York: McGraw-Hill, 1998

[31] MEMS Thin Film Deposition Processes, from WWW.MEMSnet.com

[32] "Chemical Vapor Deposition," Chemical Vapor Deposition Variants. Available at: http://www.dowcorning.com/content/etronics/etronicschem/etronics_newcvd_tutorial3.asp. [Accessed: 2015]

[33] "Electrolytic Nickel and Electrolytic Precious Metals", http://www.technic.com/applications/pcb/chemistry/electrolytic-nickel-and-electrolytic-precious-metals?t=4#tab4

[34] K. L. Mittal, "Adhesion Measurement of Thin Films", ElectroComponent Science and Technology Volume 3 (1976), Issue 1, Pages 21-42

[35] K. Masahiro and S. Noboru, "Effects of temperature, thickness and atmosphere on mixing in Au-Ti bilayer thin flims", Journal of Materials Science, 15 September 1933, Volume 28, Issue 18, pp 5088-5091

[36] "What is Partial Discharge Testing?" What is Partial Discharge Testing? [Online]. Available at: http://www.emersonnetworkpower.com/en-us/services/market/industrial/equipment-based-services/predictive-diagnostics/pages/what-is-partial-discharge-testing.aspx. [Accessed: 2015]

[37] C. M. Harris, Harris' shock and vibration handbook, 5th ed. New York: McGraw-Hill, 2002

[38] GE Global Research, "Final Technical Report of Pressure Sensor and Telemetry Methods for Measurement While Drilling in Geothermal Wells"

[39] R. Ghandi, C. Chen, L. Yin, R. Saia, T. Johnson, P. Sandvik, K. Fang, R. W. Johnson, "Reliability of SiC Digital Telemetry Circuits on AlN Substrate", Journal of Microelectronics and Electronic Packaging (2014) 11, 25-29

[40] R. Ghandi, C. Chen, L. Yin, R. Saia, T. Johnson, P. Sandvik, K. Fang, R. W. Johnson, "Reliability of SiC Digital Telemetry Circuits on AlN Substrate", High Temperature Electronics Network (HiTEN), July 8-10, 2013, Oxford, United Kingdom

[41] A. S. Kashyap, C. Chen, R. Ghandi, A. Patil, E. Andarawis, L. Yin, D. Shaddock, P. Sandvik, K. Fang, Z. Shen, R. W. Johnson, "Silicon Carbide Integrated Circuits for Extreme Environments", The IEEE Workshop on Wide Bandgap Power Devices and Application (WiPDA), Oct 27-29, 2013, Columbus, Ohio