Testing and Diagnosis of CMOS Open Defects in the Presence of Common Hazards

by

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Abstract

CMOS open defects are breaks in wires or defective transistors within some library cell causing pull up or pull down failure of the defective gates. Traditionally, TSOF (transistor stuck-open fault) is used to model such open defects, and two pattern tests are required to detect the fault. The first pattern initializes the faulty gate output, while the second pattern activates the fault and propagates the fault effect to an observable output. It has been assumed that since delay caused by such open faults is generally very large, the test patterns are only sequence dependent instead of also being timing dependent as is the case in transition delay fault (TDF) testing. Thus these opens can be detected by either stuck-at tests (for the easy to initialize faults) or two-pattern TDF tests. However, due to the significant leakage current observed in current advanced CMOS technology, stuck-at (DC) tests are no long effective in detecting many open defects which, in effect, behave like delay faults. In addition, recent studies have shown that high quality TDF tests do not detect many open faults due to the fact that the detecting conditions for TDFs cannot always guarantee the explicit targeting of TSOFs. Furthermore, a large number of TSOFs are still undetected by even targeted TSOFs in the LOC scan test mode; many of these can actually cause circuit malfunction. This is because common hazards during normal circuit transitions may activate TSOFs that do not appear to be activated from a functional state in timing unware analysis.

In this work we propose a circuit transformation scheme to use existing ATPG to generate targeted tests for TSOFs in primitive and complex gates in a scan test environment, using both LOC and LOS test modes. To allow the LOS tests to be applied at the highest achievable speed

when an at-speed scan enable is not supported, we present a scan enable timing evaluation methodology. A key contribution of this work is the development of hazard initialized tests for targeting TSOFs undetected by traditional LOC and LOS timing unware tests but can be activated by hazards. To improve test efficiency we also present a new DFT scheme with multiple independent scan enable control signals that allows mixed LOC and LOS tests to be applied to the CUTs to boost TSOF coverage beyond that that achievable from traditional LOC and LOS tests.

Finally, in order to understand the yield loss due to systematic process and layout effects early in the manufacturing process, and assist with yield ramp, it is also important to locate the physical open failures inside the defective chip. The few studies that have addressed TSOF diagnosis so far have been primarily based on stuck-at tests or have employed stuck-at diagnosis tools. We present an improved TSOF diagnosis scheme employing two-pattern scan test that generates diagnostic tests for the all non-redundant TSOFs, including those undetected by stuck-at and TDF tests.

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CHAPTER 1

Introduction

The quality of modern ASICs manufactured with advanced technology feature size of 45nm and below has been significantly influenced by defects and parameter variations induced from manufacturing process. One important category of the manufacturing defects is open. Open defects can result from missing of via or break of wires at both interconnects between library cells or connections within library cells. An open defect within the library cell will cause certain transistor fail or difficult to be turned on. Transistor stuck-open fault (TSOF) has been used to model such open defect. The victim transistor will cause the faulty gate output fail or difficult to be pulled up or pulled down by the intended input vectors, and thus the output either becomes floating or keeps its previous value.

To detect a transistor stuck-open fault we need a two pattern test [1] of which the first vector initializes the gate output to the state during which the target transistor is off and the second vector attempts to turn on the transistor and flip the initial state for fault activation and propagates the fault effect to the circuit's output. It was assumed that as delays caused by the transistor stuck-open faults are very large (due to small leakage current), they are only sequence dependent [1,2], and many of them can be detected by scan based stuck-at test [3,45] as the gate output initialization can be accomplished during test pattern shift in operation; and for those open faults whose gate outputs are difficult to be initialized by the stuck at tests, the widely used two pattern TDF (transition delay fault) timing test [4] can catch them.

However, due to the significant leakage current of the today's advanced CMOS manufacturing technology, many open faults behave like delay faults. The net leakage current at the gate output can charge or discharge the output capacitance within a much smaller time such that the stuck-test may fail to capture the fault effect. For example, more than 70% of the timing faults identified in the industrial study in [6] were detectable by scan based TDF tests at just half the operational clock frequency but not by very slow speed stuck-at tests, suggesting open defects with long charging time constants from leakage currents.

Recall that the two pattern TDF tests are guaranteed to detect any lumped "gross" (large) slow-to-rise or slow-to-fall transition fault at the target circuit node. Thus, a LOC (Launch on Capture) test set that covers all LOC detectable TDF faults, at first glance, appears to detect all functionally relevant large physical delay defects. However, it has become increasingly apparent that high quality transition delay tests fail to detect many open defects causing circuit malfunctions. A recent industrial study [7] has shown that performing detailed "cell aware" testing which targets defects inside the standard cells for high end production parts, resulted in the detection of additional defectivity of as much as 885 DPPM beyond what was screened by industrial grade stuck-at and N-detect (N=5) TDF tests; approximately 87% of these additional defects required two pattern tests for detection, suggesting they are likely to be opens. TSOFs are normally expected to be covered by TDF tests at the transistor inputs; as slow-to-rise faults for NMOS transistors and slow-to-fall faults for PMOS transistors. This appears to be reasonable, since a stuck-open transistor is very (up to infinitely) slow to turn on, and therefore should be adequately modeled by a slow-to-rise or slow-to-fall input at the gate of the transistor. However, in practice a TSOF does not impact delays at the input of the transistor, but only delays the transition at the output of the logic gate containing the stuck-open transistor. This gate output is a different node than the input node which

is the target of the TDF tests. Since TDF tests only require a transition at the target node, and not at all nodes along the detection path to the output, a TDF test for the transistor input node may not require the corresponding gate output to switch, thereby failing to detect a stuck-open fault in that transistor. Although by targeting TDF at the gate output node will create the desired output transition, only one TSOF is targeted by the test and the TDF is dropped from ATPG. However, we need to generate tests for targeting all the TSOFs at the parallel transistor branches. The failure of LOC TDF tests to detect large delays caused by commonly occurring open defects was addressed in [8,9] by explicitly targeting the TSOFs missed by the TDF tests. This was done by modifying the circuit to additionally force ATPG to generate a transition at the gate output when targeting the TDFs at the gate inputs.

However, a significant number of CMOS open faults are still undetected by ATPG targeted open tests. While some of these faults could be functionally redundant, many are undetectable because of the architectural limitations of scan design that restrict two pattern tests to either the launch on capture (LOC) or the launch on shift (LOS) modes. Since LOC tests are launched from a superset of all circuit functional states, it is commonly assumed that only opens that are LOC detectable need be targeted during the test, and any opens undetectable by LOC tests are functionally redundant and cannot cause circuit malfunctions. However, traditional scan based LOC and LOS tests are timing unware tests and transient circuit states are not considered during test generation. In practice CMOS circuits experience many transient states from large number of hazards which may occur during signal transitions. This is because gate delays for individual CMOS gates are strongly input dependent, causing signal arrival at the inputs of the internal gates in a logic block to be highly uncorrelated, therefore generating hazards at the gate output. In fact, hazards in CMOS circuits are so prevalent that they are well known to contribute to nearly half the

switching power consumption. Such hazards can easily initialize a gate output to a faulty value and thereby activate a logical fault that does not appear to be activated from a functional state under timing unware analysis.

It is known that, generally speaking, LOS tests have higher fault coverage than LOC tests. Thus some of the LOC tests undetectable hazard-activated opens can be detected by employing LOS tests. However the requirement of high speed scan enable for LOS tests makes it less favorable for industrial application. Although one can apply clock tree synthesis to the scan enable for fast signal switching, it may result in significant routing overhead.

When targeting TSOFs we can take the advantage of the slower LOS tests as the delay caused by open faults are normally large (such delay can still vary significantly depending on threshold voltages variation and trapped voltage at the open gate terminal of the defective transistor) such that even slow LOS tests can detect many open faults. In practice we would like the LOS tests to be launched at the highest clock rate for detecting as many TSOFs as possible. This requires evaluating the timing of the scan enable signal to find out how fast it can switch.

Furthermore, to ensure the IC quality and reliability for very low DPPM application like automotive industry, all opens must be targeted during test, unless proven benign, not just those that are detectable from functional states or by LOC and LOS tests.

Once the defective chips are identified, it is also important to identify the physical locations of the open defects to help study the yield loss due to systematic process and layout variations in the early stage of the manufacturing process. Recall that due to the significant leakage current of current advanced CMOS technology, stuck-at tests are no longer sufficient to target TSOFs. However, most of the current open diagnosis studies are based on stuck-at tests or stuck-at diagnosis tool. Although diagnosis of TDFs has been recently proposed in [10], the test condition

difference between TDF and TSOF and hazards activation issue for opens makes it difficult to directly apply to TSOFs.

In this work, we address two problems: detection test generation and diagnostic test generation for CMOS open faults, including those hazard-activated faults which are undetectable by LOC and LOS tests. Chapter 2 presents the background and prior works for CMOS open faults detection and diagnosis. We introduce our circuit modification scheme for explicitly targeting opens in Chapter 3. Chapter 4 introduces our methodology for scan enable signal timing evaluation. Experimental results of LOC and LOS tests for targeting open faults are presented in Chapter 5. Chapter 6 discusses the hazard initialized test generation for opens undetected by traditional LOC and LOS tests. Chapter 7 introduces our mixed LOC and LOS test DFT scheme that employs multiple independent scan enable signals for targeting opens undetected by traditional LOC and LOS tests. We present our TSOF diagnosis scheme in Chapter 8. Chapter 9 presents a summary and conclusion of our work, along with suggestions for future work.

CHAPTER 2

Background and Prior Works

2.1 Scan Based Delay Test

Scan structure has been the most widely used DFT schemes for decades. In a full-scan design, all storage elements are replaced with scan cells, which are configured as one or more shift registers (also call scan chains) during the shift operation. As a result, all inputs to the combinational logic, including those driven by the scan cells, can be controlled and all outputs from the combinational logic, including those driving the scan cells, can be observed. The main advantage of full-scan design is that it converts the difficult problem of sequential ATPG into the simpler problem of combinational ATPG. Figure 2.1 shows the full scan design scheme. When

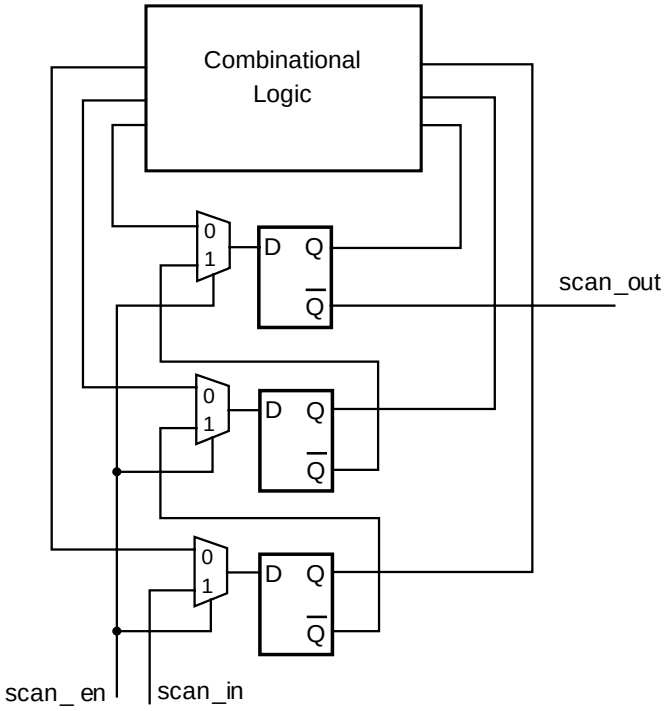

Fig. 2.1 Full Scan Architecture for CUT

scan_en = 0, the circuit operates in the functional mode; when scan_en = 1, the circuit operates in the scan mode where test vector can be shifted in for test launch or test response can be shifted out for observation.

Scan based delay testing involves the application of two test vectors <V1, V2> via the scan chains. The first vector V1, which is used to initialize the internal logic values of CUT (circuit under test), is first scanned into the scan chain when scan_en = 1, typically using a slow scan clock. The second vector V2 is then used to launch transitions at the inputs of the combinational part of the circuit. These transitions propagate to the outputs of the logic block and are then captured back into the scan chain by a fast capture clock pulse, reflecting operational frequency. Finally, the response captured in the scan chain is scanned out of the CUT and compared with the expected correct test response.

Unfortunately, because of the architectural limitations of scan, not all <V1, V2> combinations can be applied by a scan delay test. Depending on how the V2 vector is generated, scan delay tests

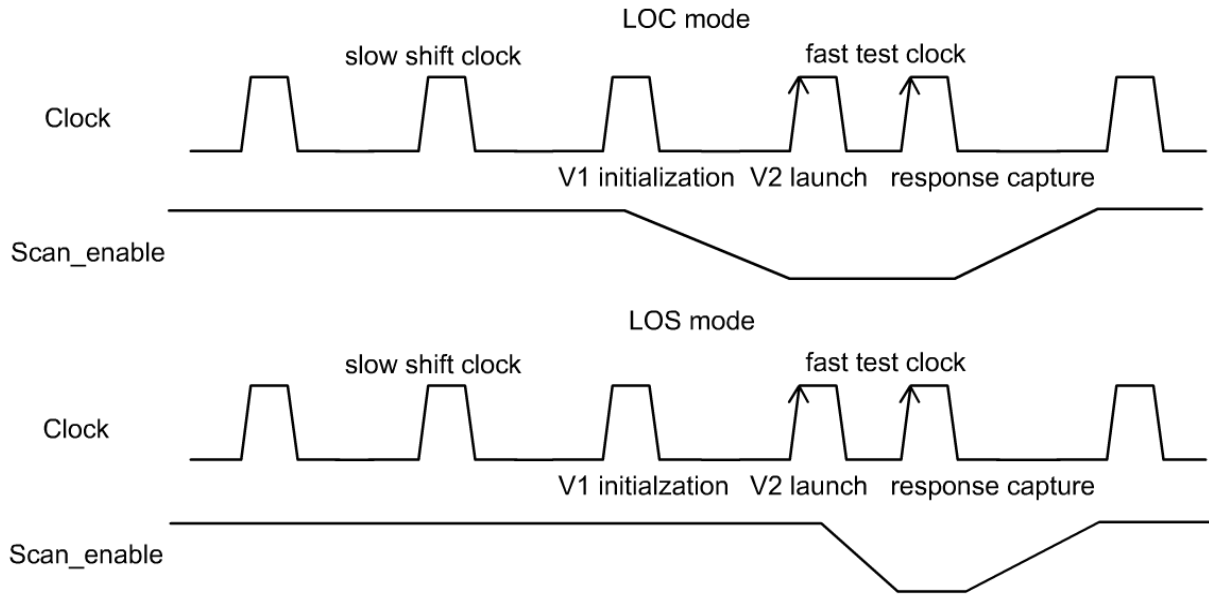

Fig 2.2 LOC and LOS scan_enable timing waveforms

are classified as Launch-on-Shift (LOS) [11, 12], or Launch-on-Capture (LOC)[13, 14]. For the Launch-on-Shift tests, the V2 vector is restricted to a one-bit shift from V1. For the Launch-on-Capture tests, V2 is the response of the CUT to vector V1. In practice, LOS tests are not always supported because they require the scan enable signal to transit at-speed between the shift mode required to launch the test, and the functional mode required to capture the response of the timing test, all safely within a functional clock period. Figure 2.2 shows the clock and scan enable signal waveforms for LOC and LOS tests. Such high speed scan enable signals are expensive to implement, although several CAD vendors now offer tools to support such an implementation. Another concern with LOS tests is that V2 vectors are not obtained from functional operation, which may result in over testing, as some detected delay faults are not supposed to be activated from functional operation. Nevertheless, low cost LOC test are generally preferred. The restrictions on the V2 vector generally limit the TDF and TSOF coverage achievable using both LOC and LOS scan tests. We believe to achieve very high coverage needed for high quality delay testing, greater flexibility in choosing the V2 vector is required.

2.2 Transistor Stuck-Open Fault and the Relationship with Transition Delay Fault

As one important category of CMOS manufacturing defect, transistor open defect has been studied for several decades. Basically it is some open (break) at the terminals of a transistor causing the switching on failure of the transistor. Here we assume the transistor open defect causes a complete break. Figure 2.3 shows all the possible open defects that could occur in a NAND2 gate. Note that Opens o12, o13 and o14 can be seen as interconnect opens and thus we only target o1 to o11 type transistor open defects, which can be modeled as transistor stuck-open faults.

Suppose we would like to detect the PMOS stuck-open fault at input a1 (this fault models the o1, o2 and o3 open defects). A two pattern test is required of which the V1 vector initializes the gate

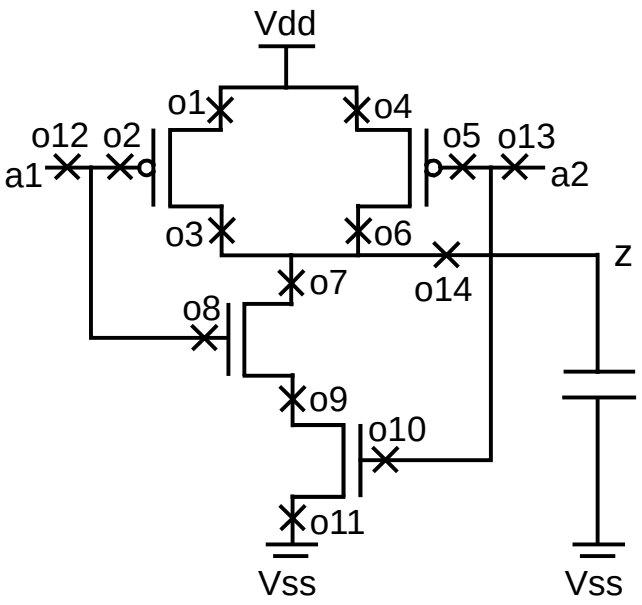

Fig. 2.3 Possible Open Defects inside a NAND2 Gate

output to 0, and the V2 vector attempts to turn on the faulty PMOS transistor and to pull up the gate output to 1. The V2 pattern must also be a test for a stuck-at-1 (s-a-1) test at input a1, i.e. V2 must propagate any incorrect faulty value at output of the gate to an observable node (primary output or scan flip-flop input). If there is a PMOS stuck-open fault at input a1, the gate output will be in a floating (high impedance) state retaining the voltage of the previous state 0 for certain amount of time. Note that the net leakage current from the PMOS transistor at input a2 may still slowly charge the load capacitance to a certain voltage level. For old technologies with large load capacitance and minimal transistor leakage current, the time constants of the gate output retains its previous state would be on the order of micro-seconds [5]. Thus earlier papers [1-3] assumed that transistor stuck-open fault is only test sequence dependent and many of them can be detected by stuck-at tests. However, for today's advanced technology with small load capacitance and relative large leakage current, this time constant could be reduced to the order of nano-seconds [5], depending on the threshold voltages of the pull up and pull down transistors. Thus stuck-at tests are no longer effective for targeting transistor stuck-open fault at the parallel pull up or pull down

branches. In addition, we need to consider a particular situation when the open defect is near the gate terminal of a transistor (etc. o8 or o10 open defect) with certain amount of trapped charges at the floating gate terminal. Such charges might partially turn on the victim transistor, which results in a much higher leakage current and thus much faster charging/discharging time constant at the load capacitance. Depending on the amount of the trapped charges, the time constant could vary up to three order of magnitude. This particular situation makes such open defect much more difficult to detect and at-speed delay fault tests are a must for targeting transistor stuck-open faults result from such open defects. Note for a stuck-open fault due to the o7, o9 or o11 open defect, a stuck-at test is likely to detect it as the open breaks the only pull down path and there is no leakage current discharging the load capacitance.

The commonly used TDF delay fault model assumes a single gross transistion fault at some circuit node. The ATPG tool generates two pattern <V1,V2> delay tests capable of detecting both slow-to-rise and slow-to-fall transition faults at the circuit nodes. The V1 to V2 change creates a rising (falling) transition at the target node, while V2 is also a s-a-0 (s-a-1) test for the target node. Note that while TSOFs are not directly targeted, TDF testing implicitly assumes that TSOFs will be covered by the TDF tests for the transistor gate input. Thus, in the example in Figure 2.1, the PMOS transistor stuck-open fault is expected to be covered by the TDF test for the slow-to-fall delay fault at input a1. If the two pattern TDF test for the slow-to-fall delay fault at input a1 sets a1=1, a2=1 for V1, and a1=0, a2=1 for V2, the TSOF will indeed be detected; the gate output will be initialized low by V1 vector, and fail to be pulled up by V2 vector because of the stuck-open fault. However, not all TDF tests for a slow-to-fall delay fault on input a1 will detect the open fault. A slow-to-fall delay fault at input a1 can also be detected by a TDF test that sets a1=1, a2=0 for V1, and a1=0, a2=1 for V2. Observe that the V1 to V2 change again causes the falling transition

at a1, and the fault effect is sensitized to the NAND output by V2. However, in this case the gate output is initialized high by V1, and remains high for V2 in a fault free circuit. To detect the open fault with such test pattern pair, certain timing constraint needs to be satisfied for the transition from V1 to V2 vector to initialize the gate output to low. The signal waveforms in Figure 2.4 show such condition. As we can see only when the 1 to 0 transition at input a1 occurs later than the 0 to 1 transition at input a2, a transient state in which both a1 and a2 equals 1 can be generated to initialize the gate output to 0, and the fault will be activated by the V2 vector. (This is also the basic idea for our hazard initialized test which will be discussed later in our work). Consequently, a TDF test for input a1 cannot ensure the detection of the PMOS TSOF at input a1. Note that while

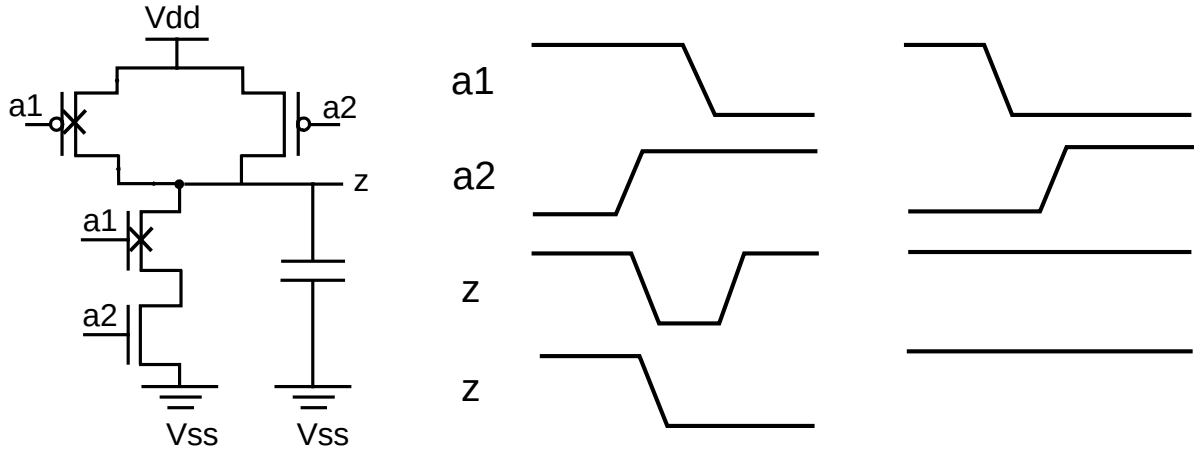

Fig. 2.4 Miss of TSOF by TDF Test

a slow-to-rise TDF test targeting the gate output node z will indeed create a 0 to 1 transition at node z to satisfy the initialization condition for detecting the PMOS TSOF, only one of the two PMOS TSOFs in the NAND2 gate is covered by such test. The detection of TSOFs that are missed by TDF testing has been addressed in earlier papers [8, 9]. The methodology involves first identifying the list of transistor stuck open faults that are not detected by the generated TDF test set, and then rerunning the TDF ATPG for the target faults with the additional constraint that the generated TDF tests also create a transition at the output of the faulty gate. For example, if the

initially generated TDF test set included a test vector pair <V1,V2> for covering the slow-to-fall transition at input a1 in Figure 2.4 that set a1=1, a2=0 for V1, and a1=0, a2=1 for V2, the corresponding transistor stuck-open fault would not be detected as explained above. In this case that TDF ATPG would be rerun with the additional constraint that the test also requires a transition at the output of the NAND gate. This would generate a test vector pair <V1,V2> that sets a1=1, a2=1 for V1, and a1=0, a2=1 for V2, if the structural constraints of scan and the circuit characteristics allow such a test.

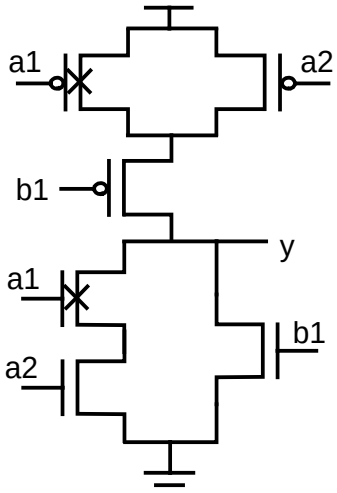

Fig. 2.5 AOI_21 Gate Transistor Schematic

Modern ASIC consists of not only primitive gates but also a large number of complex gates. Figure 2.5 shows a transistor level schematic of AOI_21 gate. A two pattern test for the PMOS TSOF at input a1 would be V1 (a1,a2) = 1 1 or V1 (b1) = 1 to initialize the gate output to 0, and V2 (a1,a2) = 0 1 and V2 (b1) = 0 to activate the fault. However, a slow-to-fall TDF test targeting input a1 would be V1 (a1) = 1, V2 (a1a2) = 0 1 and V2 (b1) = 0. This suggest that the fault coverage of TSOFs in complex gates from TDF tests can be even lower than coverages of TSOFs in primitive gates. Although both tests have the same V2 vector, the V1 vectors are quite different between the two tests and by simply adding some constraints to the ATPG cannot generate the

required V1 vector for the TSOF. Therefore we need new methodologies for targeting TSOFs in complex gates.

2.3 Hazard Activated Transistor Stuck-Open Fault

Even though prior research [8,9] has been proposed to target TSOFs missed by TDF tests (in the context of primitive gates), a significant number of TSOFs in large circuits are undetectable by even ATPG targeted TSOF tests. Some of these faults could be functionally redundant, but many are undetectable because of the architectural limitations of scan that restrict two pattern tests to either the launch-on-capture (LOC) or the launch-on-shift (LOS) modes. Since we can shift in any value into the scan chains as V1 vector, the V1 vectors set is a superset of CUT's functional states.

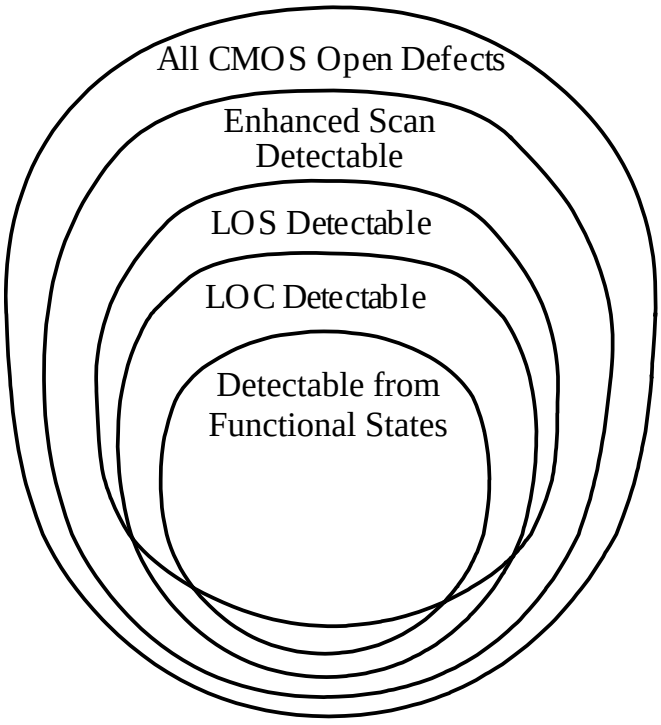

Fig. 2.6 CMOS Open Fault Coverages for Different Tests

And for LOC tests the V2 vectors are the responses of the V1 vectors, V2 vectors set is also a superset of CUT's functional states. Thus LOC tests are launched from a superset of all circuit

functional states, as illustrated in Figure 2.6. And it is commonly assumed that only TSOFs that are LOC detectable need to be targeted during the test, and that any open faults undetectable by LOC testing are functionally redundant and cannot impact circuit operation.

However, traditional test generation and fault simulation only considers timing unware Boolean signal values and ignores transient circuit states. In practice CMOS circuits experience many more transient states from large number of hazards that occur during functional transitions. This is because gate delays for individual CMOS gates are strongly input dependent (e.g. the best and worst case output rise time for a 3-input CMOS NAND gate can vary by a factor of 3), causing signal arrival at the inputs of the internal gates in a logic block to be highly uncorrelated, thereby giving rise to transient logic values at the gate output.

Take a two input NAND gate as an example. Assume two adjacent functional states with V1 = 1 1, V2 = 0 1 at the inputs of the NAND gate does not exist to activate the PMOS TSOF in Figure 2.7. The fault can still be activated by two functional states with V1 = 1 0, V2 = 0 1 which create a transient state (hazard) shown in the figure (Case 1). Such a local hazard can be easily generated if the NAND gate sits deeply inside the combinational logic. Actually even first level

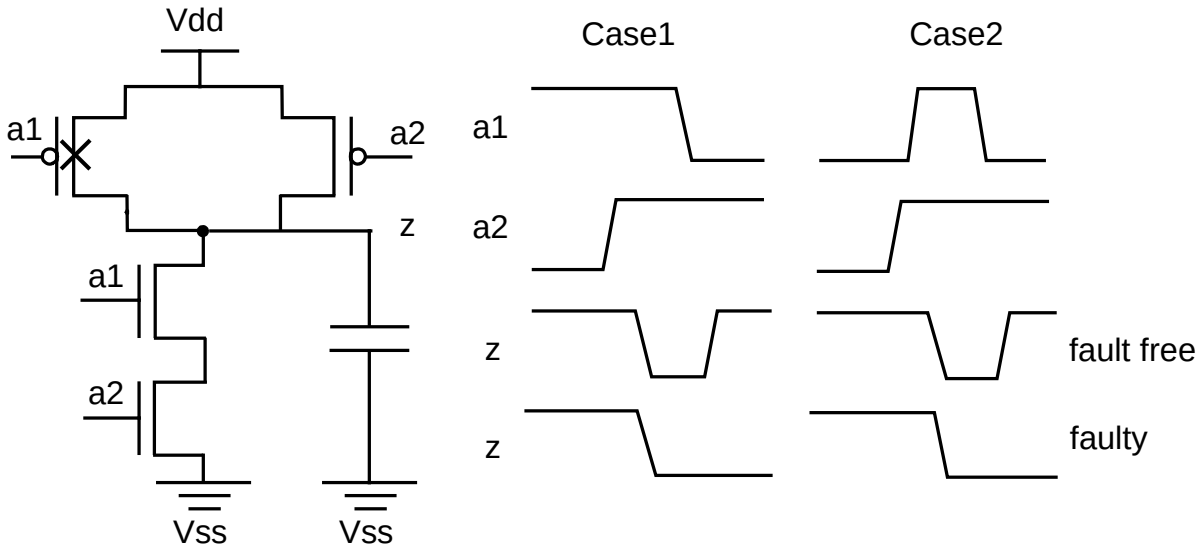

Fig. 2.7 Hazard activations of TSOF in NAND2 Gate

gates driven directly by clocked flip-flops (e.g. Gate 1 in Figure 2.8) are subject to clock skews that can sometimes exceed a gate delay in current designs, resulting in spurious glitches at the gate output before signals stabilize. Furthermore, even two functional states with V1 = 0 0, V2 = 0 1 may activate the open fault if input a1 receives a propagating hazard (Case 2 in Figure 2.7), although the probability of Case 2 to cause circuit errors would be much lower than that for Case 1, as the probability of satisfying both hazard propagating and fault effect sensitizing conditions for Case 2 is generally very rare under normal operation. Note while TSOF at the parallel branches could be activated by both local hazards and propagating hazards, only propagating hazard may activate TSOF at the serial branch (e.g. NMOS TSOF at input a1) to cause errors.

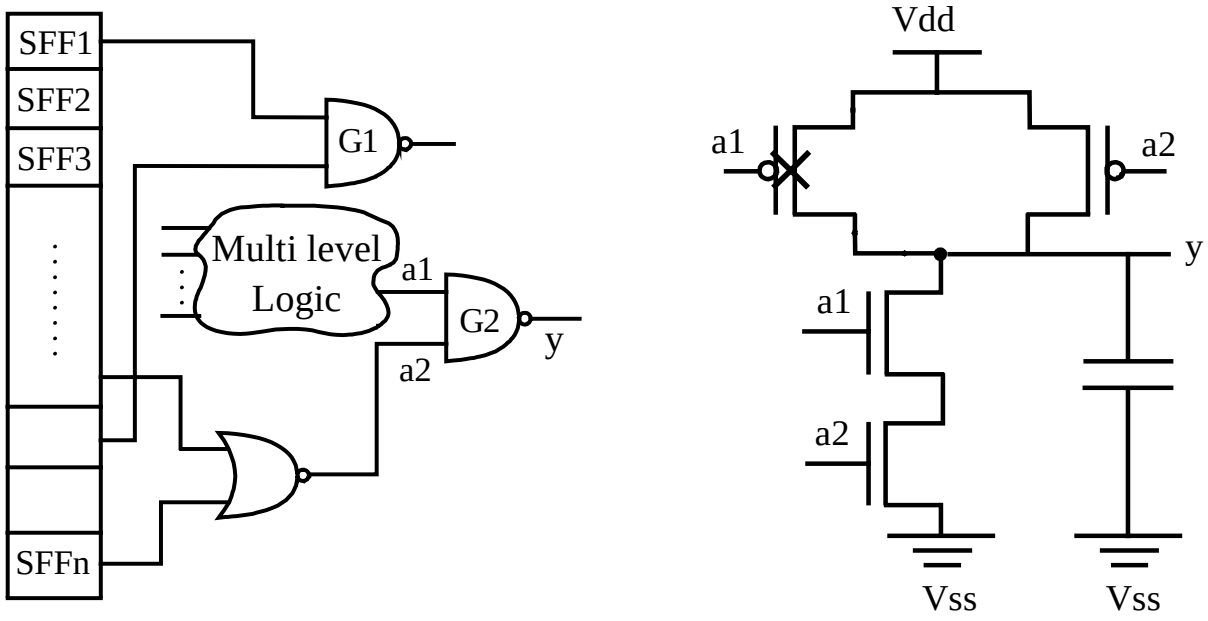

Fig. 2.8 Transistor stuck-open fault activation by switching hazard

Hazards can easily initialize opens to a faulty value and thereby activate a logical fault that does not appear to be activated from a functional state under timing unware analysis. In fact, hazards in CMOS are so prevalent that they are well known to contribute to nearly half the switching power consumption.

One efficient way of targeting LOC undetected opens that could be activated by hazards is to employ LOS tests. It is known that LOS tests can achieve higher fault coverage due to the lower correlation between V1 and V2 vectors for LOS tests than that of LOC tests. Although many designs do not support LOS tests running at the functional clock speed due to the limitation of slow scan enable signal, we can still take advantage of the LOS tests, since many TSOFs behave like relative large delay faults and at-speed clock is not required to capture the faulty effects. To make full use of LOS tests, it is still necessary to find out how fast the scan enable signal can switch from 1 to 0 before the arrival of the capture clock cycle, such that the tests can be applied at the highest speed to achieve its maximum coverage for TSOFs.

To ensure the IC quality and reliability and achieve very low DPPM, all open defects must be targeted during test, unless proven benign, not just those that are detectable from functional states or by LOC and LOS tests. Some studies have been proposed to target delay faults not detectable by traditional LOC and LOS tests. [15,16] used multiple cycle tests to target undetected TSOFs and TDFs. Partial enhanced scan design was proposed in [17,18] to target undetected TDFs from LOC and LOS tests as well. In this work, we propose two methodologies for targeting TSOFs. The first one employs ATPG to generate potential hazards for targeting TSOFs, known as hazard initialized tests generation. The second one utilizes multiple independent scan enable control signals to generate mixed LOC and LOS tests with additional reachable test launch states to target TSOFs.

2.4 Special Case – Cross Wire Open Fault within Complex gate

For primitive gates, TSOFs are the only type of open faults that need to be considered because they can model any open defects in the pull up or pull down path. However, modern ASIC consists of not only primitive gates but also a large number of complex gates, and an additional type of

open faults are found in complex gates only which behave differently from traditional TSOFs – we call them the cross wire open (CWO) faults. This important fault type has not been studied as a target for test generation so far.

Figure 2.9 shows a cross wire open fault d in the schematic of an AOI22 complex gate. To detect this fault, in addition to a V1 vector that initializes the Z output low, we need a V2 vector that either activates only the pull up path a1, b2 or only the pull up path a2, b1, both of which contain the open defect. Thus with V2 (a1, a2) = 01 and V2 (b1, b2) = 10, or V2 (a1, a2) = 10 and V2 (b1,

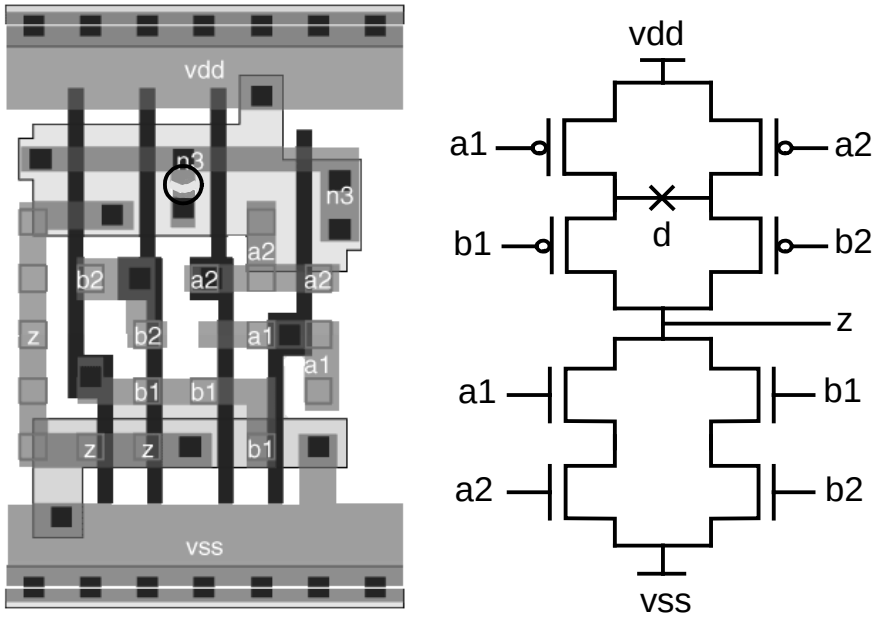

Fig. 2.9 AOI22 gate layout and transistor level schematic

b2) = 01, the cross wire open fault can be activated, as the gate output will stay at its initialized low value and not be pulled up, indicating a fault. Existing TDF timing tests and TSOF tests supported by the commercial ATPG cannot generate test vectors to satisfy the required conditions for V2 described above, and the detection of such faults generally depend on chance.

The recently proposed defect-oriented cell aware tests [7] target all possible defects within the library cells and therefore cross wire open faults are assumed to be included. However, these tests are not explicitly focused on such opens, and target very many other possible defects in the cell

layout, leading to a large increase in the test set. Furthermore, detailed cell level layout information is not always available at test generation. There is, therefore, a need to develop compact and effective tests from a gate level model of the circuit. Note further that the proposed cell aware tests [7] currently only consider open detection under timing unaware Boolean analysis that ignores hazards. They are unable to generate tests for many open faults that appear undetectable from functional states but can actually be activated by hazards and cause circuit errors. Thus in addition to targeting of cross wire opens with traditional LOC and LOS scan tests, it is necessary to target CWOFs that can only be potentially activated by common hazards.

2.5 Diagnosis of Transistor Stuck Open Fault

In order to study the yield loss due to systematic process and layout variations in the early stage of the IC manufacturing process, it is important to not only detect the open defects, but also diagnose these open defects. There are two most commonly used diagnosis methodologies—namely, cause–effect analysis and effect–cause analysis. Cause–effect analysis assumes the causes of failure are due to a specific fault type (generally stuck-at faults). Extensive fault simulation is required to build a fault dictionary for deriving and recording the test responses with respect to the applied test set and fault type. Each fault (or group of faults) inside the dictionary has its unique syndrome with the information of which vectors detecting the fault and at which outputs the fault effect is observed. Once this dictionary is built, the syndrome of the failing chip is compared with the syndromes of the dictionary to find which faults match up with the recorded possible syndromes in the dictionary. Therefore, it is often also referred to as the fault-dictionary based analysis. The problem with this methodology is large memory is required to store the dictionary, since for large circuit with large number of faults and test vectors the size of the dictionary could become significant large, although some fault dictionary compression schemes have been

proposed to reduce dictionary size. Unlike the fault-dictionary-based analysis, effect–cause analysis directly examines the syndrome of the failing chip to derive the fault candidates through Boolean reasoning on the CUD (circuit under diagnosis). The minor drawback of effect–cause analysis is that it takes longer to complete because a unique round of analysis is required for each failing chip. In this work we focus on cause-effect analysis for transistor stuck-open fault diagnosis and diagnose test generation.

Diagnosis of TSOFs has been addressed in papers [21, 22, 23]. [21] discussed TSOF diagnosis based on SAF (stuck-at fault) diagnosis tool and the experiments were conducted on combinational circuit only. Further research [22] improved the method proposed in [21] and full scan test strategy was used in the experiment. But [22] still requires information from SAF diagnosis tool. While these diagnosis methodologies can be applied to circuits with large feature size technology which has very large time constants of charging or discharging of load capacitances from leakage current, for sub-micron or even nanometer feature size technology, due to the large threshold to power supply voltage ratio, the relative large net leakage current can charge or discharge the gate output capacitance within a short amount of time to invalidate the fault effects, such that many TSOFs may behave like large delay faults possibly missed by SAF tests. Thus the stuck-at test based TSOF diagnosis mythologies are no longer effective to target TSOFs found in modern ICs manufactured with advanced technology. A SAT based diagnostic ATPG was proposed in [23] to target arbitrary faults in combinational circuits, including TSOFs. However significant effort has to be made to such ATPG to support large circuits with full scan design. In addition, as what has been discussed in Section 2.4, CMOS circuits experience a large number of hazards during normal operations and many open defects that are assumed to be functionally redundant from timing unaware analysis can in fact be activated by such hazards and cause circuit failure. It is necessary to diagnose these

hazard activated TSOFs as well. TDF diagnosis methodology has been proposed in recent papers [10], but it is now apparent that a large number of TSOFs are missed by high quality TDF tests.

In order to effectively diagnose TSOFs, we use targeted TSOF tests to conduct fault simulation for building an initial fault diagnosis dictionary to separate faults into different groups such that faults from different groups can be distinguished by their own syndromes consisting of indexes of vectors detecting the faults and indexes of the outputs observing the faults effect. We then borrow the exclusive tests generation scheme from [10] to generate exclusive test for undistinguished TSOF fault pairs inside a group and further improve the resolution of the dictionary.

CHAPTER 3

Gate Modification for Directly Targeting Open Fault

Since many TSOFs are undetected by traditional TDF tests, it is necessary to develop methodology to generate tests specifically target TSOFs. Instead of developing new constraints into the ATPG for targeting TSOFs, we modify the circuit logic structure to allow the use of conventional ATPG to target TSOFs. This is done by using the modified logic to convert the test detection conditions of TSOF into the conditions for TDF. Earlier research [8,9] has proposed a similar scheme but it can only be applied to circuits implemented with primitive gates. The following two sections will discuss our gate modification schemes for targeting TSOFs [47] and CWOFs [49] (cross wire open fault).

3.1 Gate Modification for Targeting Transistor Stuck Open Fault

Figure 3.1 shows the transistor level schematic of a two input NAND gate. A test for the PMOS

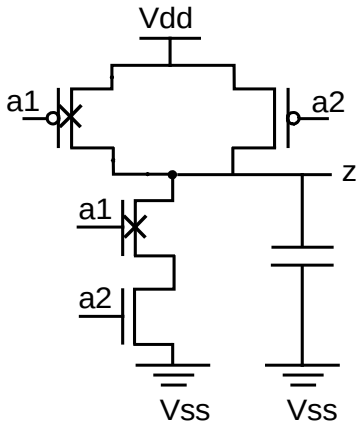

Fig. 3.1 NAND2 transistor level schematic

TSOF at input a1 would be V1 (a1a2) = 1 1, to initialize the gate output to 0, and V2 = 0 1, to

activate the fault. By using the logic structure in Figure 3.2, the ATPG can generate such a test by targeting the slow-to-fall TDF at node d1. Since the V1 vector for node d1 is 1 and d1 is a fan-out branch of gate G1's output, the V1 vector for input a1 and a2 would be a1a2 = 1 1. For the purpose of fault effect activation and sensitization, we need V2 (a1a2) = 0 1. This vector pair is exactly the test for the PMOS TSOF at input a1. Similarly, by targeting the slow-to-fall TDF at node d2, we can generate the test for PMOS TSOF at input a2. To generate a test for the NMOS TSOFs at the serial NMOS path, we can target the slow-to-rise TDF at node d3 (G1's output) of the same logic structure, which is shown in Figure 3.3. To have V1 (d3) = 0, at least one of inputs a1 and a2 need to be 0, and this will initialize the gate output to 1. V2 (d3) = 1 requires a1 = a2 = 1 to pull down the gate output to 0. An NMOS TSOF at a1 or a2 will be activated by this vector pair.

The logic structure in Figure 3.2 is for a NAND type gate. By replacing the AND/NOR gate in the structure with OR/NAND gate, we have the logic structure for a NOR type gate. Figure 3.4

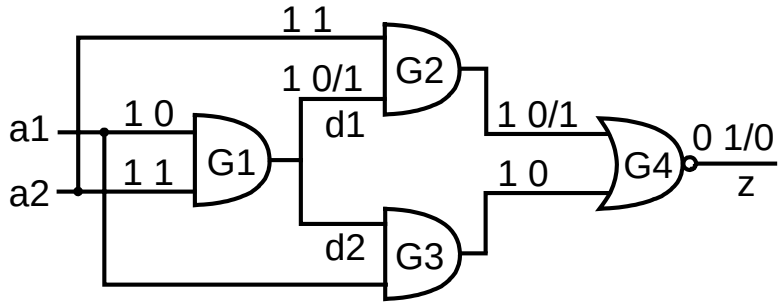

Fig. 3.2 2 input NAND gate modification and test generation for PMOS TSOF at input a1

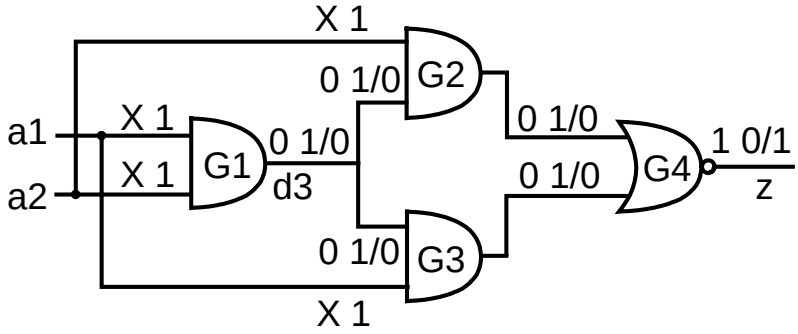

Fig. 3.3 2 input NAND gate modification and test generation for NMOS TSOF at input a1

shows the logic and test generation for a NMOS TSOF in a two input NOR gate by targeting the slow to rise TDF at node d1.

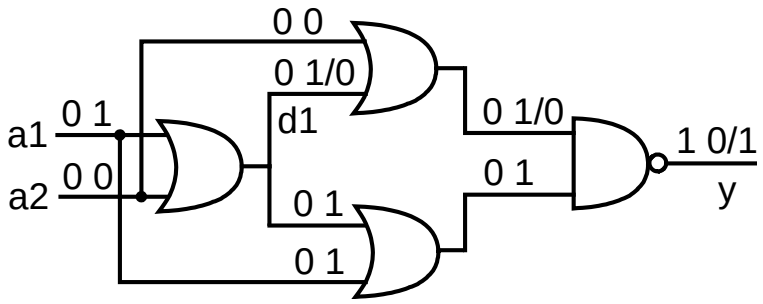

Fig. 3.4 2 input NOR gate modification and test generation for NMOS TSOF at input a1

Now let us discuss the test generation conditions for TSOFs in complex gates. Figure 3.5 shows the transistor level schematic for an AOI21 complex gate. To target a PMOS stuck open fault at

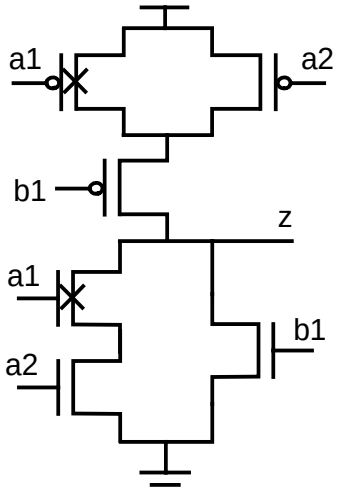

Fig. 3.5 AOI21 transistor level schematic

input a1, the V1 vector must first turn on at least one of the parallel NMOS paths (a1 = 1; a2 = 1 or b1= 1) to pull down output z to 0, and the V2 vector must then turn on the faulty PMOS pull up path (a1 = 0 and a2 = 1 and b1 =0) which contains the target transistor to pull up output Y to 1; additionally Y must be sensitized to an observable circuit output. Note that the PMOS TSOF at input b1 dominates either PMOS TSOF at input a1 or PMOS TSOF at input a2. This is because the PMOS at input b1 is in series with either PMOS at a1 or PMOS at a2, and the detection of

either one will ensure the detection of the PMOS TSOF at b1, therefore there is no need to generate specific test for targeting this fault. To target an NMOS stuck open fault at the input a1 (and input a2, since they are in series), the V1 vector must turn on either one of the PMOS paths (a1 or a2 = 0 and b1 = 0) to pull up the gate output and the V2 vector must turn on the NMOS path containing the target transistor (a1 & a2 = 1 and b1 = 0). As we can see, although the V2 vector requirement for targeting the PMOS TSOF and the NMOS TSOF is the same as the requirement for slow-to-fall TDF and slow-to-rise TDF, the V1 vector for the TSOF test is quite different from the V1 vector for the TDF test. Consequently, TDF test patterns may not be very effective for TSOF detection in complex gates; explicitly targeting the stuck open faults is necessary.

To deterministically target both PMOS and NMOS TSOFs in an AOI21 gate, we replace the complex gate by the structure shown in Figure 3.6. The signal values in Figure 3.6 show the test generation for the PMOS TSOF at the a1 input by targeting node d (second input of G3 gate) slow-

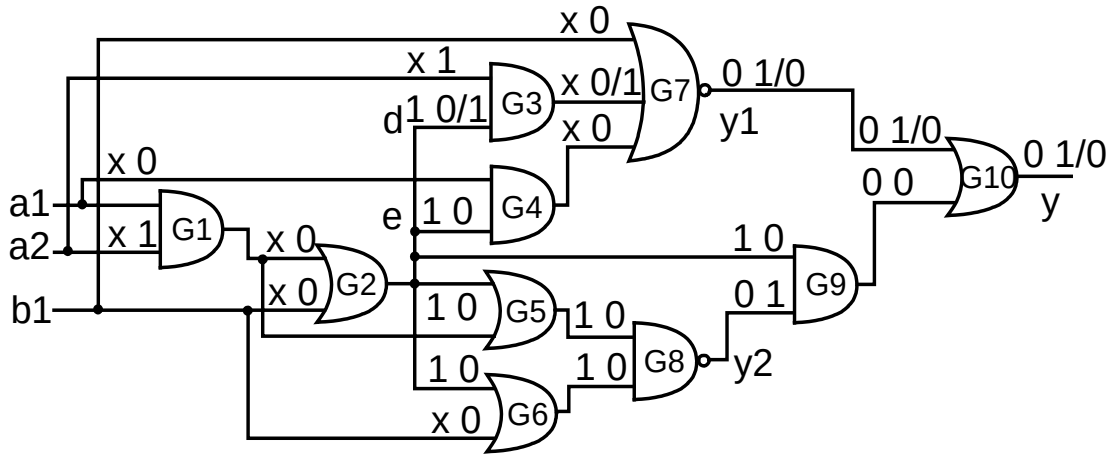

Fig. 3.6 AOI21 Complex Gate Modification Structure for Both PMOS and NMOS TSOFs

to-fall TDF. The resulting two-pattern test V1 V2 must have d = 1 0 and a2 = x 1. Since the node d is a fan-out of gate G2's output, at least one of G2's inputs (G1 output and b1) must be 1 for the V1 vector and both must be 0 for the V2 vector to make d = 1 0. Since G1 output = A1 & A2, (V1 V2) d = 1 0 would give us either a1 = 1; a2 = 1 or b1 = 1 for V1 vector, and A1 = 0; A2 = 1; b1

=0 for V2 vector. Now we have a1 = 1; a2 = 1 or b1 = 1 for the V1 vector (to pull down the AOI21 gate output to 0), and a1 = 0; a2 = 1 and b1 = 0 (to pull up the gate output to 1) for the V2 vector. These are precisely the conditions for the test for PMOS stuck-open fault at A1. Similarly, by targeting slow-to-fall TDF at node e (gate G4's second input), we have the test for PMOS TSOF at a2 input.

To generate the test for the NMOS TSOF at a1 input (and a2, since the two NMOS transistors are in series), we target the slow-to-rise TDF at node f (G6's first input) as shown in Figure 3.7. Node f is also a fan-out of the G2 output. With f = 0 1 it is easy to derive G1 output = 0 1 and b1 = 0 0. Thus we have (V1 V2) a1 & a2 = 0 1 and b1 = 0 0. These are the conditions for detecting NMOS TSOFs at a1 and a2. Similarly the test for the NMOS TSOF at b1 input can be generated by targeting node g (G5's first input) slow-to-rise TDF.

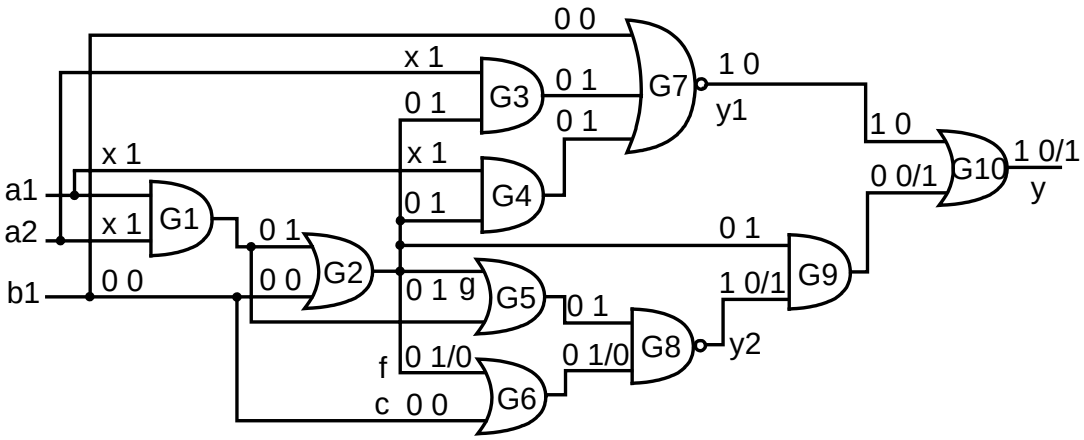

Fig. 3.7 Gate modification for test generation of NMOS TSOFs in AOI21 gate

All the other AOI or OAI type complex gates can be replaced by the corresponding structures accordingly. Note that the functionality of the replacing structure is equivalent to the corresponding original complex gate (i.e. the circuit in Figure 3.7 is functionally equivalent to the AOI21 gate). This allow us to replace all the complex gates with the logic structures and employ ATPG to target all the corresponding TDFs which represent the TSOFs at one time.

3.2 Cross Wire Open Fault Identification and Gate Modification for Detection

To target the CWO faults within the complex gates independent of library cell layout, we need to identify all the possible open faults for all input configurations of the complex gates. This is because without layout information, it is impossible to tell how inputs from the netlist map to physical transistor locations in silicon. For example, Figure 3.8 shows the PMOS networks of an AOI22 gate. It is obvious that by exchanging input a1 and a2 we have two possible network configurations, which create two possible open faults f1 and f2. To activate fault f1 the V2 vector

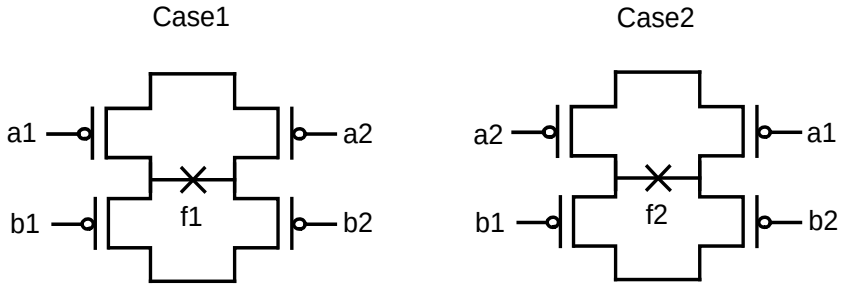

Fig. 3.8 Possible PMOS network configurations for an AOI22 gate

needs to turn on PMOS at input a1 and b2 (a1, b2) only or a2 and b1 (a2, b1) only. Similarly for fault f2 we need PMOS at (a2, b2) or (a1, b1) to be turned on. If the layout information is unavailable, both these CWOs must be targeted during test generation to guarantee fault detection.

Now consider the PMOS network of an AOI33 gate. Figure 3.9 shows some different input configurations. As can be seen in Case 1, the CWO fault f1 separates the upper and lower level of

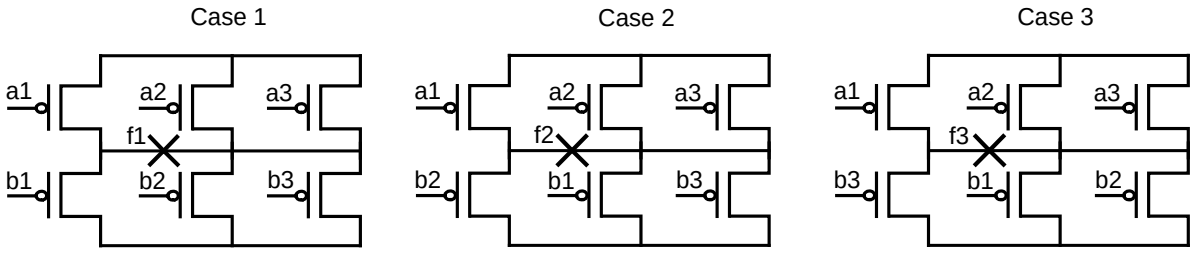

Fig. 3.9 Possible PMOS network configurations for AOI33 gate

inputs into two groups respectively: input a1 on the left side and input a2, a3 on the right side; input b1 on the left side and inputs b2, b3 on the right side. If we keep the input configuration for the upper level inputs the same and list all the possible configurations for the lower level inputs based on different grouping, we have three possible PMOS networks. For Case 1, fault f1 separates input b1 and b2, b3; for Case 2, fault f2 separates input b2 and b1, b3; for Case 3, fault f3 separates input b3 and b1, b2. To activate fault f1 in Case 1, the V2 vector should turn on PMOS at a1 and b2 or b3 (a1, (b2 + b3)), or PMOS at a2 or a3 and b1 ((a2 + a3), b1). Similarly, for fault f2 in Case 2 we need (a1, (b1 + b3)) or ((a2 + a3), b2), and for fault f3 in Case 3 we need (a1, (b1 + b2)) or ((a2 + a3), b3). Since we also have three possible configurations for the upper level inputs, totally we have a total of 3x3 = 9 faults for all possible input configurations of the AOI33 gate. Similarly, for the AOI333 gate, when we consider the open faults at the first and second level of inputs, we have 3x3 = 9 faults; when we consider the second and third level, we have another 9 faults. Thus for the AOI333 gate we have 18 possible faults to target.

Figure 3.10 shows the different PMOS network configurations of an AOI44 gate. For fault f0 which is at the side of the network, the analysis is similar to our discussion of AOI33 gate; for each level of inputs we have 4 possible configurations and totally we have 4x4 = 16 possible side open faults for the AOI44 gate. Now consider fault f1 which is at the center of the network. It separates the upper and lower inputs into two groups respectively: input a1, a2 and a3, a4 for the upper level; input b1, b2 and b3, b4 for the lower level. If we keep the upper level network the same and interchange the lower level network, we have six possible configurations (as shown in Figure 3.10) based on different groups of inputs: input b1, b2 and b3, b4 separated by fault f1; input b3, b4 and b1, b2 separated by fault f2; input b1, b3 and b2, b4 separated by fault f3; input b2, b4 and b1, b3 separated by f4, input b1, b4 and b2, b3 separated by f5, input b2, b3 and b1, b4 separated by f6.

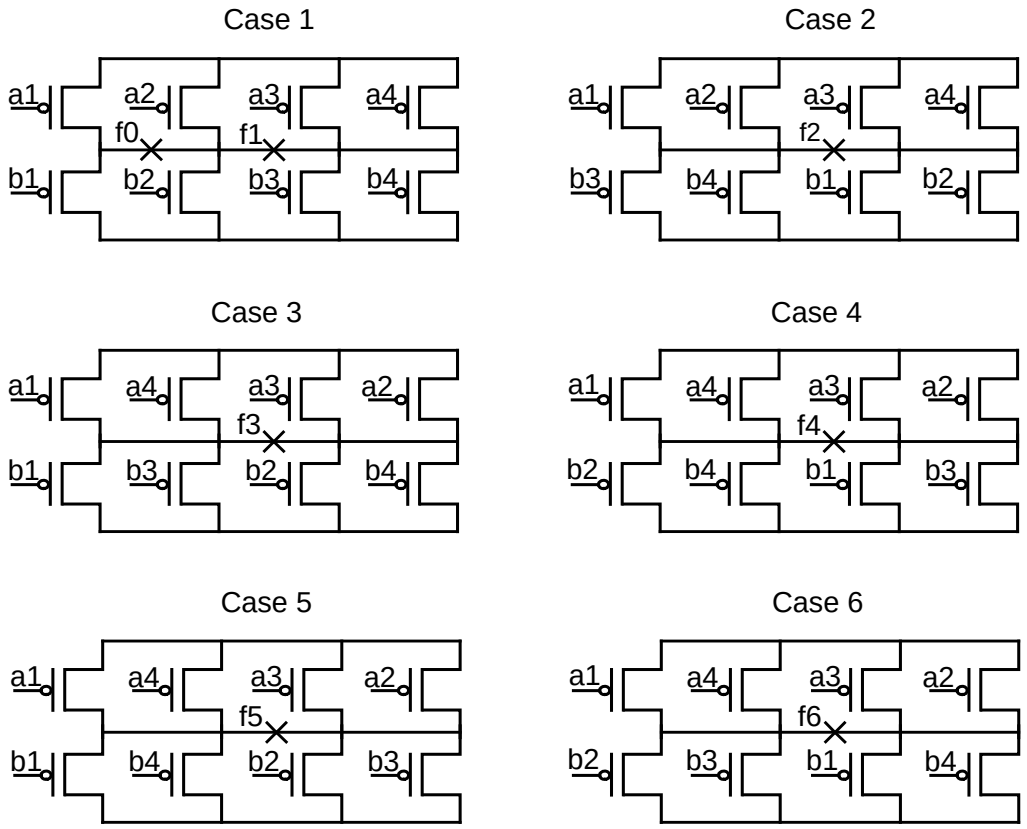

Fig. 3.10 Possible PMOS network configurations for AOI44 gate

As there can be three possible configurations for the upper level network (the reason there are three instead of six configurations as in the lower level is that we interchange the two groups in the lower level to have six configurations, and the interchanging of input groups in the upper level network is redundant since the network is symmetrical), in total we have 6x3 = 18 possible faults at the center of the AOI44 network. Thus the AOI44 gate have 18 + 16 = 34 possible CWO faults.

AOI22, AOI221		AOI222		AOI32, AOI321		AOI322		AOI33	
2	1	4	2	6	2	8	3	9	2
AOI332		AOI333		AOI422		AOI43		AOI44	
15	4	18	4	16	4	30	3	34	3

Table 3.1 Number of possible cross wire open (CWO) faults for sample AOI complex gates with and without layout information

Table 3.1 shows the number of cross wire open faults possible for varying sizes of AOI complex gate cells. The number on the left is the total possible faults from all layout configurations, while the number on the right is the number of faults from a particular configuration assuming we have the cell layout information.

We use a commercial ATPG tool to generate deterministic tests for the timing un-aware cross wire opens in complex gates. This is done by transforming the complex gates into another circuit structure for the purposes of test generation. This converts the detection of open faults into the detection of corresponding transition delay faults with additional test activation conditions. Figure 3.11 shows an example of AOI33 gate transformation. The function of the transformed structure

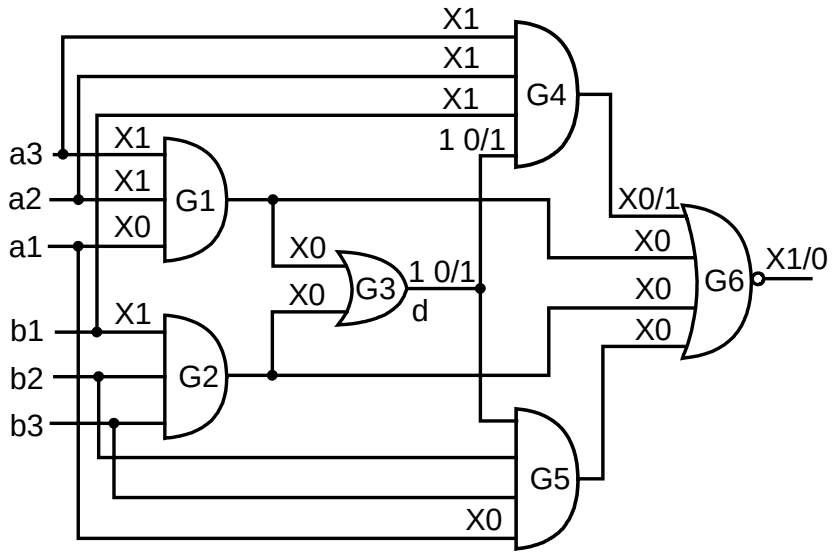

Fig. 3.11 AOI33 gate transformation for targeting CWOF

is the same as that of the AOI33 gate. In the figure we target node d (output of gate G3) slow-to-fall TDF in the transformed circuit. Since (V1) d = 1 and d = (a1 AND a2 AND a3) OR (b1 AND b2 AND b3), we have either (V1) a1 = a2 = a3 =1 or b1 = b2 = b3 = 1 to initialize the output y to 0. The fault effect has two paths (gate G4 or G5) to sensitize to output y. Suppose it sensitizes through gate G4, then we have (V2) a2 = 1, a3 = 1 and b1 = 1. Since (V2) d = 0, we have gate

G1's output = 0 and G2's output = 0, which give us a1 = 0 and b2 or b3 = 0. Thus the V2 vector will try to turn on PMOS at input a1 and input b2 or b3 only. This is exactly one test for the cross wire open fault f1 in Figure 3.10. Similarly, if the fault effect sensitizes through gate G5, we have the V2 vector to set a1 = 1, a2 = 0 or a3 = 0 and b1 = 0, b2 = 1, b3 = 1, which is the other test for fault f1. Thus by using ATPG to target the TDF fault, we have the test for the corresponding cross wire open (CWO) fault. The transformed sub-circuits circuits for other complex gates can be created in a similar way. We use a small script to automate the transformation before the circuit is given to ATPG.

Using the transformed circuit each time we can only run a single test generation for one cross wire open fault of every complex gate. To target all the possible faults within all the complex gates, we need to run test generation on multiple transformed copies of the CUT. The total number of test generation runs needed equals the total number of possible cross wire opens faults in the largest complex gate. This results in a somewhat large fault list and test data volume for the CUTs, which can be greatly reduced if layout information is available.

Note that while we have worked with a traditional circuit structure based commercial ATPG tool, adding the required constraints on two pattern TDF tests to target opens can perhaps be more easily implemented in SAT based ATPG, and also using new commercial tools that support user defined fault models.

CHAPTER 4

Timing Evaluation Tests for Scan Enable Signals

One simple way of targeting those hazard activated TSOFs that are undetectable by LOC open tests is to employ LOS open tests. Recall what has been discussed in Chapter 2, the delay caused by the TSOF can vary several orders depending on the threshold voltage variations and trapped voltage level at the open gate terminal of a transistor. To effectively target the open faults with varying delay effects, it is necessary to find out the maximum speed supported by the LOS test. The speed of the fastest LOS tests that can be applied to the circuits is determined by the speed of the global scan enable signal switching from 1 to 0 during the launch and capture cycle of the test. Since it is a broadcast control signal that fans out to all the scan flip-flops, it's switching speed is generally quite slow compare to clock signals, unless employs clock tree synthesis to the scan enable signal or implements a scan enable pipeline structure into the circuit, both of which will

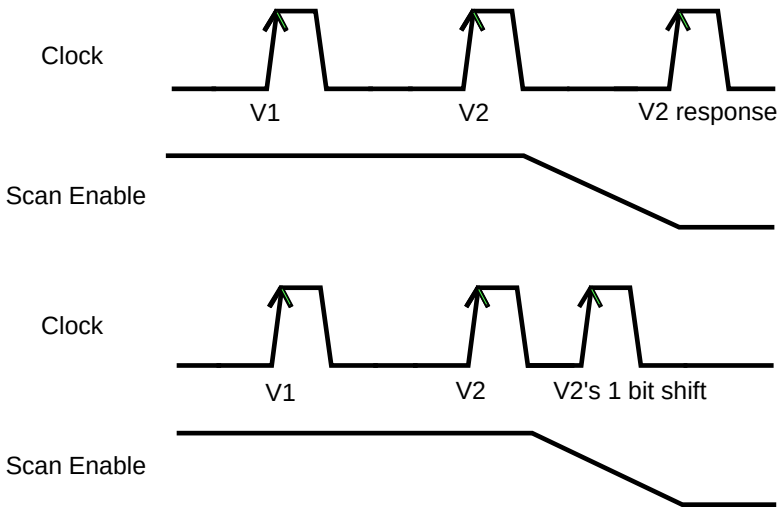

Fig. 4.1 Scan enable waveforms for LOC and LOS tests

result in considerable design overhead. Figure 4.1 shows the timing waveforms of the LOS tests with slow and fast capturing clock. Observe that if the scan enable signal meets timing constraint and switches from 1 to 0 fast enough, the combinational logic's response to the V2 pattern will be captured into scan flip flops. If it does not switch fast enough, the scan flip flop will once again operate in the shift mode and capture the result from the content of the preceding scan flip flop. As the circuit clock speed is increased, narrowing the launch-to-capture window, in any circuit at some point the scan enable will fail to switch in time. Our goal is to develop a test to determine this maximum clock frequency at which the LOS test still works correctly.

4.1 Scan Enable Timing Test Generation Scheme

To detect scan enable signal timing failure during a LOS test, the scan input value at one scan flip-flop should be different from the expected V2 response of the combinational logic. In such a case, scan enable timing failure at any flip flop will cause the incorrect (scan input) value to be captured, and the failure will be detected. Figure 4.2 illustrates the conditions required for the LOS tests to create different values at the scan in and data inputs. Thus developing the desired timing

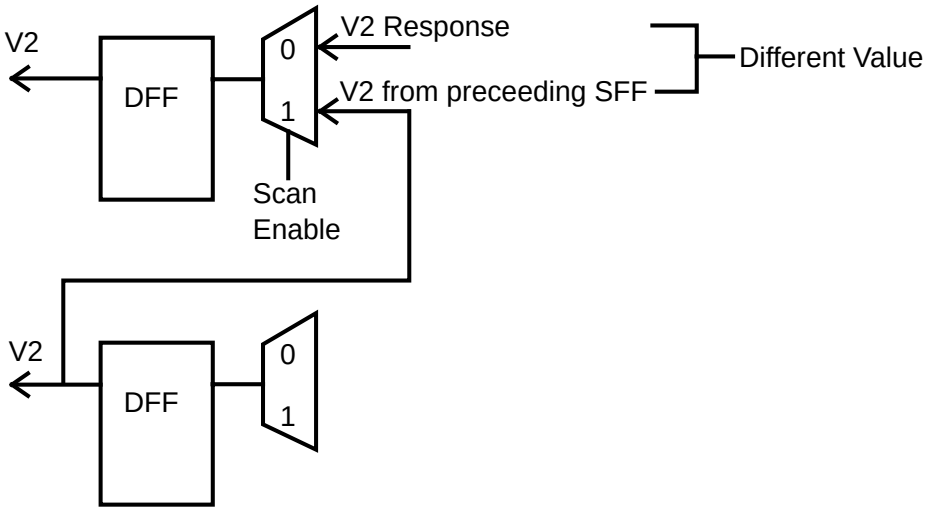

Fig. 4.2 Condition for LOS test evaluation of scan enable timing

tests for the scan enable signal involves developing a LOS test pattern set such that every scan flip-flop is covered by the test set by ensuring different scan-in and functional signals at the scan multiplexer inputs. This LOS test is then repeatedly run at different launch-to-capture frequencies to determine the highest frequency where the test passes [50].

In order to generate such LOS tests, we modify the combinational circuits into the structure shown in Figure 4.3 and employ ATPG to target the corresponding stuck-at 0 faults in the structure. Since our goal is to generate different values at the data input and scan_in input of the MUX when V2 vector is applied to the circuit, we add a XOR gate for each state output of the combinational logic and feed the XOR gate's inputs with value at data input (V2) and value at scan_in input (V2 from preceding flip-flop), the required LOS test can be generated when we use ATPG to target the stuck-at 0 fault at the output of the XOR gate. This is because to detect the stuck-at fault, ATPG

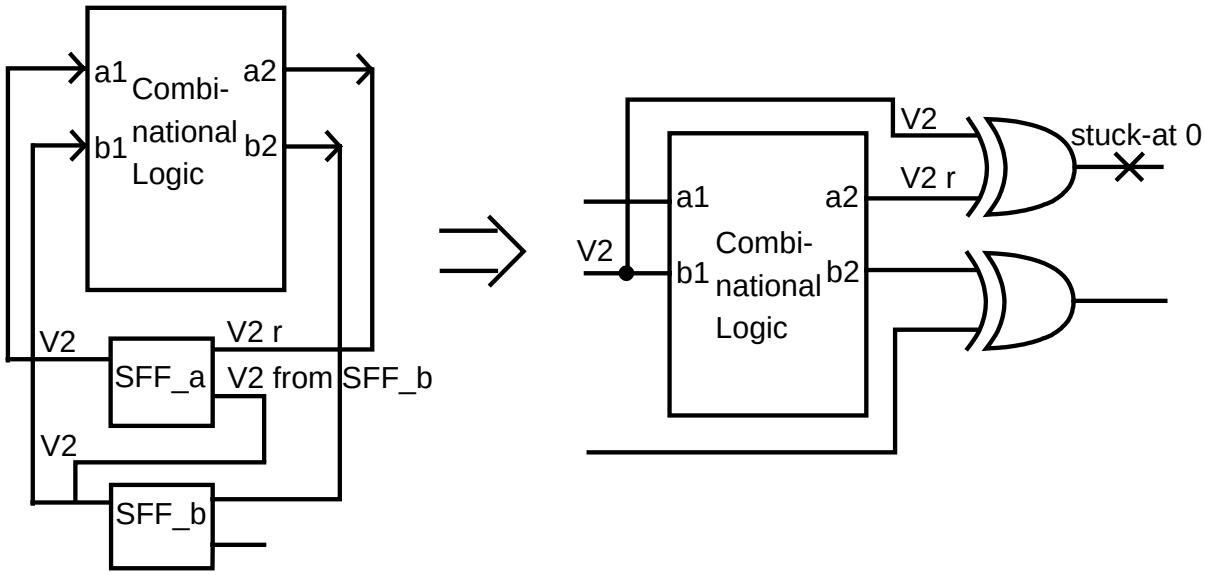

Fig. 4.3 Modified Logic for Scan Eanble LOS Test Generation

needs to set the output to 1, which will in turn set different values at the XOR gate's inputs and give us different V2 response and V2 from preceding flip-flop. If all the stuck-at 0 faults are detected, the generated test set is a scan enable signal timing test set.

However, there remains a further potential problem. Often in designs the scan interconnects are routed with the lowest priority, and a few can be extremely slow. It is possible that if the scan enable is also slow to switch, such a slow scan interconnect between SFF_a and SFF_b in this example may not allow the new V2 value from the output of SFF_b to arrive at the scan_in input of SFF_a before the capture edge, resulting in the capture of the earlier V1 value. If this V1 is different from V2, the XOR gate will always produce a 1 at the output and the scan enable timing error will go undetected. To overcome this problem, a more robust test would require that the test patterns guarantee SFF_b has same logic value for both the V1 and V2 vectors, so that no signal transition and/or propagation is needed during application of V2; furthermore these two identical logic values must be different from circuit response feeding into SFF_a. Figure 4.4 shows the

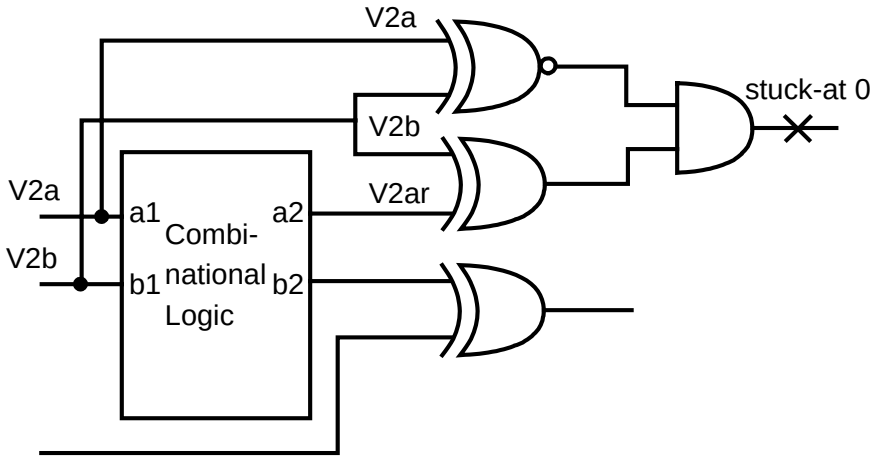

Fig. 4.4 Scan enable timing test generation under the context of slow scan path

structure to generate the more restricted tests. Note that the V1 for SFF_b would be the V2 for SFF_a, as V2 is a one bit shift of V1, thus the test needs to generate identical V2 values for both a1 and b1 state inputs. By adding a XNOR gate for the two inputs and targeting stuck-at 0 fault at the output of the NAND gate, ATPG can generate the more robust test for scan enable signals at each flip-flop.

4.2 Experimental Results for Scan Enable Timing Tests

The experimental results for the test set testing the speed of the scan enable signal are shown in Table 4.1. There are two cases that we considered in the experiments performed on the larger benchmark circuits. In Case 1 in Table 2, we assume that the scan shift paths are always faster than the scan enable signal. Recall that in this case the test only requires that the final steady state values at the data and scan_in inputs at the target flip flop be different during the launch (V2) cycle, because the scan shift signal will not be delayed. Case 2 considers the further constrained case where the scan shift into the target flip flop may be delayed. In this case we do not allow any

CUT	# Gates	# DFF	# Test Patterns	
			Case 1	Case 2
s13207	2573	638	7	16
s15850	3448	534	6	12
s35932	12204	1728	11	15
b14	8567	245	7	15
b15	10871	449	8	28
b20	17158	490	10	29
b21	17482	490	7	23
b22	17482	490	10	31
b17	27852	1415	10	62

Table 4.1 Number of test patterns for scan enable timing evaluation

transition at the scan_in input during the launch cycle, which still ensures that the data and scan_in inputs differ. Obviously Case 2, being further constrained, requires larger test sets because, on average, fewer circuit flip-flops will be simultaneously set up to the needed test conditions by a single two pattern test – more tests will be need to cover all the flip flops. Note however that even for Case 2, the number of tests needed to test the scan enable signal speed at all flip flop in the large benchmarks circuit is quite small; in all cases less than 100. This suggests that the tests can

be repeated at multiple clock frequencies to determine the point of failure at affordable cost. CMOS Open LOS tests can then be run at the fastest speed to detect faults with the smallest delays [50].

CHAPTER 5

Experimental results of LOC and LOS targeted tests for Open Faults

The experiments reported in this chapter were all conducted with commercial ATPG tools on the re-synthesized large ISCAS89 and ITC99 benchmark circuits using an open source 250nm technology standard cell library containing a rich set of complex gates. The XOR, XNOR and multiplexers are implemented using inverters, AOI and OAI gates in our experiments. The ATPG is allowed to switch the primary inputs between the V1 and V2 vectors. Note that in this experiment we not only target the TSOFs at the parallel branches of the gates, but also the those at the serial branch since an open defect near the gate terminal of the transistor in the serial branch may also behave like a delay fault which is undetected by DC tests. Section 5.1 reports the test coverages for transistor stuck open faults and Section 5.2 reports the test coverages for cross wire open faults.

5.1 Test Coverage for Transistor Stuck Open Fault

Tables 5.1 shows the TDF and TSOF fault coverages of TDF and TSOF tests for the circuits under LOC and LOS test modes. Columns 2 and 3 show the TDF and TSOF fault coverages of the LOC TDF tests; Columns 4 and 5 show the TDF and TSOF fault coverages of LOC TSOF tests. Column 6 shows the additional TSOF fault coverage improvement from the LOS TSOF tests; Column 7 shows the combined TSOF fault coverages of the LOC and LOS TSOF tests. It can be seen that although we get more than 90% TDF coverage with LOC TDF tests, the actual TSOF coverage of TDF tests is only 83.76% on average and many TSOFs are not detected. By applying

targeted LOC TSOF tests, on average we get 3.3% TSOF coverage improvement. By comparing Columns 3 and 5 we know with LOC TSOF tests alone we lose about 3% TDF fault coverage. The coverage loss can be easily recovered by applying additional TDF tests for the undetected TDF faults. Allowing tests to be also generated from the LOS mode adds between 5% to 20% additional TSOF coverage. Thus LOS test are very effective for detecting those hazard activated TSOFs to improve open fault coverages.

CUT	LOC TDF Tests		LOC TSOF Tests		Δ LOS TSOF FC	Combined TSOF FC
	TDF FC	TSOF FC	TDF FC	TSOF FC		
s1423	92.20%	85.88%	90.60%	92.01%	4.71%	96.72%
s9234	94.35%	84.85%	91.60%	91.78%	7.59%	99.38%
s13207	89.22%	73.93%	85.76%	79.19%	19.72%	98.91%
s15850	86.09%	79.01%	84.36%	83.06%	16.04%	99.10%
s35932	95.61%	94.94%	95.46%	96.39%	0.88%	97.27%
s38417	98.22%	83.30%	96.42%	85.05%	13.79%	98.83%
s38584	95.52%	91.27%	93.49%	93.90%	5.19%	99.08%
b14	91.31%	84.76%	89.15%	87.61%	8.31%	95.92%
b15	88.20%	80.03%	83.83%	83.54%	8.58%	92.13%
b20	92.85%	86.61%	91.16%	89.53%	7.87%	97.40%
b21	92.86%	86.42%	91.25%	89.43%	7.69%	97.11%
b22	91.93%	86.42%	90.40%	88.50%	7.46%	95.96%
b17	86.03%	78.45%	80.67%	80.37%	10.41%	90.78%
b18	92.98%	76.78%	80.13%	78.67%	16.67%	95.35%
Average	91.96%	83.76%	88.88%	87.07%	9.64%	96.71%

Table 5.1 LOC and LOS TSOF coverage for re-synthesized circuits with complex gates

Note that for the ITC99 benchmark circuits a significant number of TSOFs are still undetected by the LOC and LOS tests. These TSOFs can still be potentially activated by common hazards and new methodologies need to be developed for targeting them. In the later sections we will discuss our proposed method for targeting these undetected faults.

Table 5.2 shows the number of test vectors for each test type. Column 5 shows the percentage of additional number of LOC TSOF and top off TDF tests to the number of LOC TDF tests alone for each CUT. On average with 37% more tests, we get the same TDF coverage and 3.3%

CUT	#LOC TDF Tests	# LOC TSOF Tests	# Top Up TDF Tests	Additional % to LOC TDF Tests	△# LOS TSOF Tests
s1423	117	122	29	29.06%	23
s9234	200	225	57	41.00%	29
s13207	291	278	102	30.58%	127
s15850	243	264	69	37.04%	116
s35932	102	118	10	25.49%	11
s38417	256	231	86	23.83%	69
s38584	379	373	128	32.19%	95
b14	835	935	249	41.80%	165
b15	977	907	473	41.25%	289
b20	1316	1390	366	33.43%	182
b21	1568	1775	416	39.73%	179
b22	1253	1405	407	44.61%	201
b17	1428	1283	850	49.37%	492
b18	1643	1638	767	46.38%	886
Average	NA	NA	NA	36.84%	NA

Table 5.2 Number of test vectors for TDF, LOC and LOS Open tests

additional TSOF coverage. Although the test cost overhead is relative high, the coverage improvement is for the hard to detect faults. Note that significant coverage boost is achieved for each CUT from moderate number of LOS TSOF tests. A drawback is that we may not be able to apply LOS tests at-speed as it requires fast scan enable control signal.

5.2 Test Coverage for Cross Wire Open Faults

The experimental results for targeting CWO faults are shown in Table 5.3 and Table 5.4. Results in Table 5.3 are for all possible CWO faults in a circuit when cell layout information is not available. Results in Table 5.4 are for one set of CWO faults in a circuit with known fixed cell layout information. We initially employ LOC TDF tests to conduct the open fault simulation using the transformed circuit structure discussed in Chapter 3. We then incrementally allow LOC and LOS cross wire open fault test generation to target the faults undetected by LOC TDF tests. The rationale for this order is to maximize the test speed with which most of tests are applied. LOC tests can always be run at speed, so the LOC tests are used to target as many opens as can be detected by such tests. The remaining faults are still targeted by LOS tests because even when LOS tests must be run much slower because of a slow scan enable signal, they can still detect many opens that display very large delay fault behavior.

In Table 5.3, Column 2 shows the total number of possible CWO faults in the absence of layout information. Column 3 shows the percentages of total number of possible CWO faults to the total number of TSOFs for each CUT. Note the percentages are relatively large since we consider all possible inputs configurations of the complex gates. Note that for ITC99 benchmark circuits the percentages of COW faults count are larger than the percentages of COW faults for the ISCAS89 benchmark circuits. This is because ITC99 circuits consist of a larger percentage of complex gates. Column 4 shows the CWO fault coverage (as percentage of the total number of possible CWO

faults) of the TDF LOC tests for the original circuits with complex gates. Column 5 and 6 show the incremental coverage improvement over TDF LOC tests by LOC and LOS cross wire open tests. As we can see, by applying TDF tests alone, on average only 50% of the CWO faults are

CUT	Total CWOs	CWO % of total TSOFs	CWO FC of TDF Tests	ΔLOC CWO FC	ΔLOS CWO FC	Total FC
s1423	82	4.75%	69.51%	19.51%	0%	89.02%
s9234	148	4.91%	45.27%	48.65%	2.03%	95.95%
s13207	580	7.61%	54.83%	22.41%	18.97%	96.21%
s15850	734	7.37%	43.19%	37.87%	11.04%	92.10%
s35932	1674	4.96%	97.85%	2.15%	0%	100%
s38417	2080	6.99%	63.94%	31.54%	1.20%	96.68%
s38584	2653	7.77%	69.05%	21.75%	2.86%	93.67%
b14	2347	12.45%	47.59%	34.73%	8.27%	90.58%
b15	3976	15.04%	31.34%	40.34%	12.60%	84.28%
b20	4395	11.39%	53.11%	32.38%	7.87%	93.36%
b21	4469	10.99%	51.31%	31.17%	9.64%	92.12%
b22	6839	11.50%	49.42%	33.73%	8.77%	91.93%
b17	14837	16.28%	32.04%	39.81%	11.59%	83.45%
b18	34670	14.13%	32.32%	39.95%	17.55%	89.82%
average	NA	9.72%	52.91%	31.14%	8.03%	92.08%

Table 5.3 Incidental CWO coverage of LOC TDF Tests and coverage increase from targeting undetected CWOs in LOC and LOS modes.

detected. By employing LOC and LOS cross wire open tests to target the TDF undetected faults, we can get close to a 40% improvement in CWO fault coverage on average.

CUT	Total CWOs	CWO % of total TSOFs	CWO FC of TDF Tests	ΔLOC CWO FC	ΔLOS CWO FC	Total FC
s1423	31	1.79%	77.42%	22.58%	0%	100.00%
s9234	66	2.19%	50.00%	48.48%	0%	98.48%
s13207	228	2.99%	30.26%	28.51%	37.28%	96.05%
s15850	294	2.95%	37.76%	46.60%	13.61%	97.96%
s35932	558	1.65%	95.88%	4.12%	0%	100.00%
s38417	806	2.71%	60.42%	34.37%	0.12%	94.91%
s38584	907	2.65%	70.23%	20.07%	2.76%	93.05%
b14	991	5.26%	53.28%	27.45%	8.48%	89.20%
b15	1774	6.71%	29.59%	50.34%	6.76%	86.70%
b20	1961	5.08%	54.51%	29.63%	9.43%	93.57%
b21	1985	4.88%	51.28%	29.87%	10.18%	91.34%
b22	2811	4.73%	47.95%	33.48%	11.10%	92.53%
b17	6296	6.91%	34.55%	40.71%	6.40%	81.66%
b18	14377	5.86%	31.01%	41.12%	17.96%	90.10%
average	NA	4.03%	51.73%	32.67%	9.54%	93.25%

Table 5.4 Incidental CWO coverage of TDF tests and improvement from targeted LOC and LOS tests for a fixed layout configuration.

We have repeated the test generation and fault simulation experiments based on a fixed and known transistor configuration in each complex gate (which assumes the cell layout information is available) and the results are shown in Table 5.4. While the number of target CWOs are 2-3X smaller, the coverage results and trends can be seen to be quite similar. The number of test vectors for each test type are shown in Table 5.5. For LOC and LOS CWO tests, the left column shows the number of tests for all possible CWOs when layout information is unknown, the right column

shows the number of tests for the CWOs with fixed layout information. As we can see with known layout information we need significant less number of test vectors. To achieve very low DPPM, targeting of cross wire open faults is a must and the cost of additional number of tests cannot be avoided.

CUT	TDF Tests	LOC CWO Tests		LOS CWO Tests	
		Layout unknown	Known layout	Layout unknown	Known layout
s1423	110	9	4	NA	NA
s9234	215	38	20	2	NA
s13207	228	85	40	33	27
s15850	186	98	55	25	15
s35932	66	5	2	NA	NA
s38417	244	84	42	10	1
s38584	354	158	54	20	7
b14	866	269	116	80	38
b15	953	352	211	122	37
b20	1292	447	245	105	59
b21	1621	469	264	127	69
b22	1307	565	267	131	71
b17	1441	464	258	320	72
b18	1435	586	320	424	211

Table 5.5 Number of test patterns applied in each test mode

CHAPTER 6

Hazard Initialized Test Generation for Transistor Stuck Open Fault

Due to the structure limitation of LOC and LOS scan tests, for large circuits many TSOFs are still undetected by the combined LOC and LOS tests but can potentially be activated by common hazards from normal operations. We use ATPG to generate hazard initialized test for targeting these undetected TSOFs [46,48]. While hazards have been considered in the activation and detection of TDF faults [27, 44], to our knowledge this is the first work to show that hazards in circuit can be used to detect otherwise undetectable open faults that can result in erroneous operation.

6.1 ATPG Hazard Initialized Test Generation

Figure 6.1 shows an example of a PMOS TSOF at input a1 of an AOI22 gate activated by a hazard generated right at the faulty gate. Here a1 (V1V2) = 10 and a2 (V1V2) = 01. Due to the transient state in which both a1 and a2 are 1, output Y can be temporarily pulled down to 0. If a PMOS TSOF presents at input a1, Y will not be pulled up to 1 by the second vector and the fault is activated at the gate output Y. The fault will be detected if V2 vector is also a stuct-at-1 test vector for input a1. This hazard initialized test shown in Figure 6.1 can actually be generated by targeting a slow-to-fall TDF at input a1. Since the PMOS TSOF at a1 input is undetectable under Boolean analysis (no two vector test exists to first initialize gate output with V1 vector a1 = a2 = 1 or b1 = b2 = 1 and then activate the fault with V2 vector a1 = 0, a2 = 1), when ATPG generates

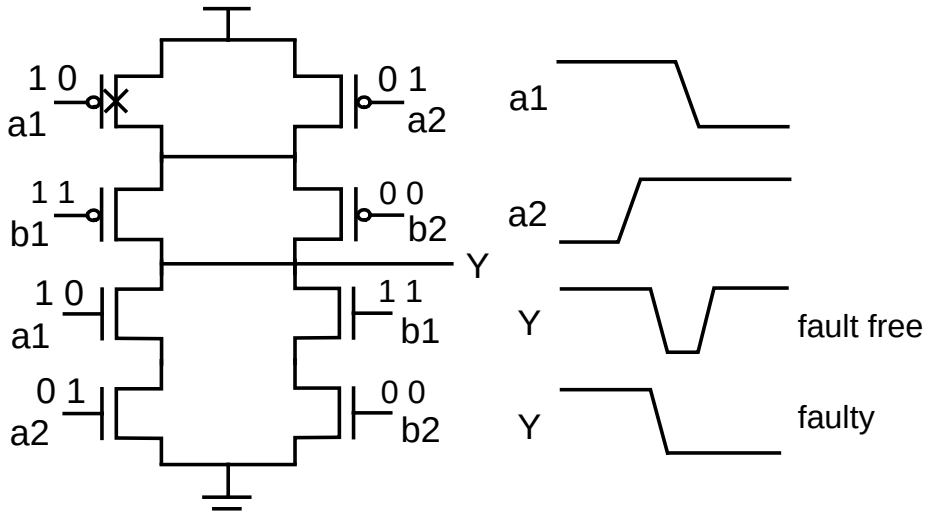

Fig. 6.1 Hazard activation of PMOS TSOF at input a1

a slow-to-fall TDF test for a1 input, the V1V2 vector pairs at a1 and a2 must be a1 = 10 and a2 = 01. Thus this TDF test can be a potential hazard initialized test for the TSOF. By employing N detection tests, we assume among the generated N tests that some of them will satisfy the timing conditions and generate hazards to target the TSOF. Note that the PMOS TSOF at a1 input can be activated by a hazard generated via signals at a1 and a2 inputs. It can also be activated by hazards generated via signals at b1 and b2 inputs. Such hazard initialized test can be generated by adding ATPG constraints which can be achieved either from circuit modification scheme or from modification of the ATPG algorithm, which can be the future work for hazard initialized test generation.

Figure 6.2 shows an example of a potential hazard initialized test for targeting NMOS TSOF at input a1/a2 of the AOI22 gate. Similar to our discussion in the previous paragraph, such test can be generated by targeting a slow-to-rise TDF at input a1 of the AOI22 gate. To satisfy the fault detection conditions ATPG will set (V1V2) a1 = 01 and a2 = x1. Since the NMOS TSOF at a1 is steady state undetectable, no V1 vector exists to initialize output Y to 1, which means the V1 vector for both b1 and b2 should be 1. And since the V2 vector will only turn on the NMOSs at a1

and a2, at least one of inputs b1 and b2 will receive a 0 for V2 vector. If the 0 to 1 transition at input a1 occurs later than the 1 to 0 transition at input b1 or b2, output Y can be temporarily pulled up to 1 and the NMOS TSOFs at inputs a1 and a2 can be activated by the test. Similarly, by targeting a slow-to-rise TDF at input a2, we can have the test generate potential hazard via inputs a2 and b2 to target the fault.

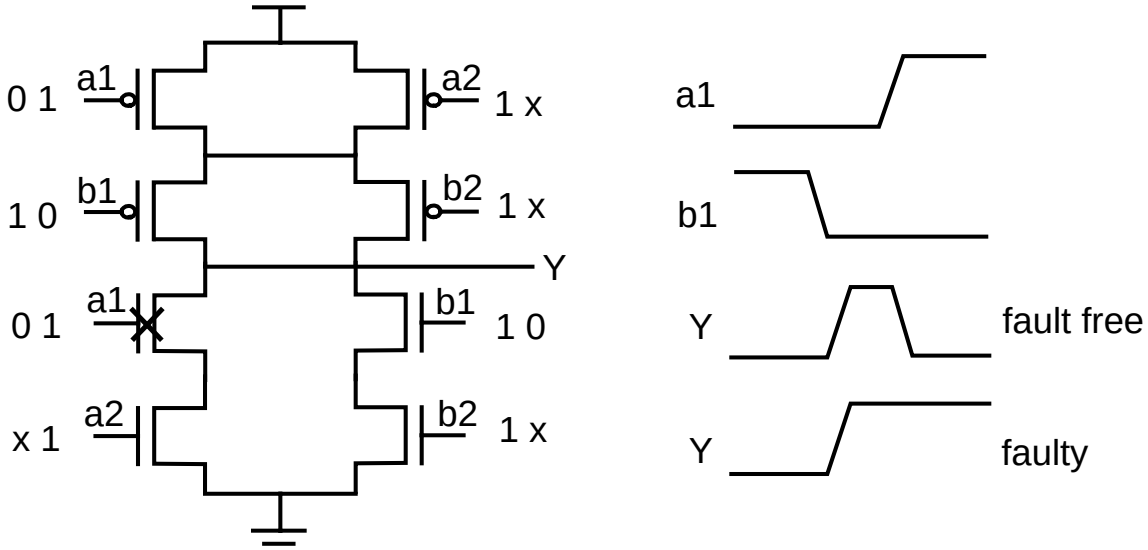

Fig. 6.2 Hazard initialized test for NMOS TSOFs at input a1 and a2

The aim in developing hazard initialized tests is to target those steady state undetectable opens that can potentially be activated by a hazard to cause malfunction. The generation of such tests therefore necessarily requires circuit timing information. Take the NMOS TSOF at the AOI22 gate in Figure 6.2 as an example. This fault can potentially be activated by a hazard during a test that, in steady state, sets a1= 0, b1 = 1 for V1, and a1= 1, b1 = 0 for V2, or a2 = 0, b2 = 1 for V1, and a2 = 1, b2 = 0 for V2. On the other hand, if the transition at input a1 (or a2) is always guaranteed by circuit timing analysis to arrive before that at b1 (or b2), because of the respective input path delays, then the open fault can never be activated and is undetectable. In this case, it need not be targeted in test generation. In the following section we report the experimental results of using

expensive HSPICE simulation to obtain such timing information for small benchmark circuits. The combination of static timing analysis and ATPG would be one solution for large circuits. Note that here we only target the ATPG targeted tests of undetected TSOFs at the parallel branches via local hazards, as TSOFs at the serial branches can only be activated by propagating hazards. Generation of propagating hazards and fault effect sensitization require very strict timing conditions, which might not be practical to be generated in ATPG for targeting TSOFs.

To minimize test escapes, our approach calls for including tests in the test set that target all potentially hazard activate-able (and therefore detectable) opens. These include opens that may be activated in the presence of process (as well as voltage and temperature) variability, even if the fault activating hazard is not observed for nominal parameter values. Such TSOFs can be identified by analyzing the timing difference between the arriving input signals that cause the hazard at the gate output. For example, suppose, because of the switching delays associated with the NAND gate in Figure 6.3, under nominal conditions the transition at the a2 input must arrive one gate delay before the transition at a1 to generate a logical hazard at the output, i.e. a glitch with an amplitude that exceeds the logic switching threshold. Smaller input skews are masked by the switching inertia of the NAND gate. However, if under the extremes of process, voltage noise, and temperature (PVT) variations that can alter circuit timing, the hazard is also activated in gates where the nominal input arrival times are only half a gate delay (or even less) apart, then the open can potentially be activated in functional operation for input skews of the smaller size. Consequently, these TSOFs should also be targeted by hazard initialized delay test to ensure detection.

Clearly, the coverage and effectiveness of our approach depends on the size and “richness” of the initial ATPG generated N-detect TDF test set for a target fault. A larger N increases the

likelihood that if a TSOF can be activated by a hazard in the LOC mode, the corresponding test pattern pair will be in the N-detect TDF test set for the input gate, although this is not guaranteed.

6.2 SPICE Simulation for Verifying The Effectiveness of Hazard Initialized Tests

To study the effectiveness of the N-detect based hazard initialized tests for TSOFs, we employ HSPICE simulation for some of the ISCAS89 benchmark circuits. It is obvious that the proposed hazard initialized test will be most effective when the depth of the circuit (number of gate levels between the inputs and output) is large, maximizing the potential for timing skews at internal gate inputs, and consequently hazards at the gate outputs needed to initialize the tests. This can be expected to be true in practice for most industrial circuits. Because of SPICE simulation time limitations, the ISCAS-89 benchmark circuits used in the experiments here are small by industry standards. It is therefore likely that for large industrial circuits, the fault coverage improvement from hazard initialized delay tests can be reasonably expected to be even higher than observed in these experiments.

Initially we employ LOC targeted TSOF tests for targeting the static state detectable opens, we then apply 5-detect LOC TDF for targeting those undetected faults which can be activated by hazards. The reason we do not apply additional LOS targeted tests for reducing the undetected fault candidates is for the small to medium ISCAS-89 benchmark circuits the combined LOC and LOS targeted fault coverage is very high and there is no much room for the improvement from the hazard initialized tests. To perform the SPICE timing simulations, we converted the original (primitive) gate level benchmark circuits into the transistor level netlists using NCSU's FreePDK 45nm technology standard cell library. For each TDF activated TSOF, we intentionally inserted the fault into the transistor level netlist file and ran HSPICE simulation using the vectors generated by 5-detect LOC TDF test from ATPG to see if some of the opens could be detected by the test.

In addition to observing whether the fault was detected as an erroneous logic value at the output, we also studied the hazard that initialized the test, in particular the timing skew in the arrival of the gate inputs causing the hazard.

The experimental results are presented in Tables 6.1 and 6.2. In Table 6.1, the second column is the total number of TSOFs in each circuit. The third column is the TSOF coverage of the LOC targeted test for each circuit. Column 4 shows the number of additional TSOFs detected by 5-detect TDF (hazard initialized) tests. Column 5 shows the number of TSOFs actually be detected in HSPICE simulations by the hazard initialized tests. Column 6 and 7 show the corresponding fault coverage improvement.

CUT	# TSOFs	LOC TSOF FC	# TSOFs detected by 5-detect LOC TDF tests	# TSOFs detected in HSPICE simulation	5 Detect Tests FC	Actual HI Test FC
s510	848	74.29%	31	9	3.66%	1.06%
s953	1486	56.17%	22	14	1.48%	0.94%
s1423	2328	61.65%	212	127	9.11%	5.46%
s1488	2774	74.52%	107	41	3.86%	1.48%
s9234	15942	78.40%	267	173	1.67%	1.09%

Table 6.1 Number of TSOFs detected and FC improvement from hazard initialized (HI) tests

By comparing Columns 4and 5, notice that for circuit s953, s1423 and s9234, more than 60% of the remaining 5-detect TDF activated TSOFs are detected by hazard initialized tests. Importantly, these additional faults covered are precisely the open defects that are likely to be activated from a functional state. We have already discussed that in practical large industrial circuits, with many levels of gates in the logic, the possibilities of hazards is even greater. Such circuits are likely to allow a larger number of TSOFs to be detected by hazard initialized tests.

Beyond the faults that can be hazard activated for nominal process parameters, default voltage and temperature, it is also important to include in a delay test set, tests for those faults that can be potentially activated and detected at PVT corners. Table 6.2 shows the number of faults that would be detectable if a gate generated a valid initializing hazard for different ranges of input delay skew, measured in terms of a typical inverter gate delay. For example, Column 3 lists the number of the undetected TSOFs that would be detected if any timing skew in the gate input transitions of greater than 25% of a gate delay (in the appropriate direction), results in a initializing hazard at the gate output. Note that in practice this may not always be the case if the switching delay (inertia) of the gate is too large; the transient hazard generating conditions at the gate input (active in this case for 25% of a typical inverter delay) may disappear before the gate output achieves a full logic transition. Gate inertia clearly is depends on the gate drive and output loading of individual gates.

CUT	# TSOFs detected for varying gate inertia values as a % of nominal inverter delay									
	# TSOFs potentially detected for gate inertia = 0%	# TSOFs in left column actually detected for nominal parameter values	# TSOFs for gate inertia = 25%	# TSOFs actually detected	# TSOFs for gate inertia = 50%	# TSOFs actually detected	# TSOFs for gate inertia = 75%	# TSOFs actually detected	# TSOFs for gate inertia = 100%	# TSOFs actually detected
s510	14	9	14	9	10	9	9	8	8	8
s953	15	14	15	12	13	12	12	12	11	11
s1423	132	127	129	124	127	123	118	116	95	94
s1488	48	41	43	35	40	34	37	32	34	30
s9234	205	173	183	162	149	137	130	126	114	113

Table 6.2 Number of TSOFs potentially detected for varying gate inertia values as a % of nominal inverter delay

The columns further to the right show the number of TSOPs detected if a larger timing skew is required to trigger a hazard. In general, a higher level of timing skew is observed at fewer gate inputs in nominal timing simulation.

For example, for undetected TSOFs in s1488, 43 would be detected (Column 3) if input timing skews of 25% of a gate delay or more would be sufficient to produce a hazard at all affected gate outputs. The number in parenthesis indicates that 35 is the number of faults that are actually detected in nominal simulation; the remaining 8 gates appear to have a too high inertia to generate a hazard for this input skew size. Similarly, from Column 6 we see that a fewer number, 34 faults, would be detected if an input skew of a full gate delay is required to generate a hazard, since such a large skew would be observed at the input of fewer gates. However, for our simulated circuit 30 out of these 34 faults are actually detected because very few (only 4) gates have such a large inertia that no hazard is generated for such a large input skew.

6.3 Experimental Results of Hazard Initialized Tests

It has been shown in the previous section that among the faults detected by 5-detect hazard initialized tests, more than 50% of them are actually detected in HSPICE simulation, which means N-detect vectors are capable of generating the required input delay skews for hazards to active the faults. In this section we report the experimental results of employing the 5-detect hazard initialized tests for the medium to large ISCAS-89 and ITC-99 resynthesized benchmark circuits. Table 6.3 shows the potential coverages of hazard initialized test for the LOC and LOS test undetectable TSOFs. Column 2 shows the percentage of LOC and LOS undetected TSOFs at the parallel branches to the total TSOFs. Column 3 shows the potential coverages of hazard initialized tests for these undetected TSOFs and Column 4 shows the maximum coverage we can get from enhanced scan design in which V2 vectors are also fully controllable by the redundant shadow flip-flops. Column 5 shows the number of hazard initialized tests generated. By Comparing Column 3 and 4 we can see for most of the circuits the potential coverages of hazard initialized tests are very close to that can be achieved by enhanced scan architecture.

CUT	LOC and LOS undetected TSOF	Hazard Initialized FC	Enhanced Scan FC	# Hazard Initialized Tests
s1423	2.35%	0.99%	1.61%	48
s9234	0.55%	0.00%	0.03%	0
s13207	0.85%	0.04%	0.04%	15
s15850	0.68%	0.13%	0.15%	31
s35932	1.56%	0.00%	0.00%	0
s38417	1.13%	0.85%	0.97%	266
s38584	0.76%	0.01%	0.01%	11
b14	3.63%	0.89%	1.02%	230
b15	6.93%	3.28%	3.74%	1465
b20	2.23%	0.93%	0.97%	572
b21	2.56%	0.83%	0.87%	470
b22	3.15%	0.86%	0.90%	646
b17	7.32%	2.89%	3.64%	1910
b18	3.91%	2.28%	2.92%	2339

Table 6.3 Potential coverages of hazard initialized test for the LOC and LOS test undetectable TSOFs

Recall that enhanced scan removes all restrictions and arbitrary two-pattern tests can be apply to the combinational logic of a sequential design. It is obvious that an enhanced scan undetectable TSOF can still be activated by hazards, but the fault effect can never propagates to the circuit outputs, and therefore causes no errors in functional operation. First consider the V2 pattern needed for detection. It must attempt to turn on the transistors path that containing the TSOF, turn off any other parallel paths (so that the gate output floats in the presence of the fault), and at the same time sensitize a path from the gate output to a circuit output. For complex gates with multiple inputs, satisfying all the above conditions simultaneously may not always be possible, making the corresponding TSOFs functionally redundant. Note that the V1 vector can always independently

set the faulty gate output to the desired pre-charged logic value (unless the gate output only takes on a single value, in which case the logic itself is redundant) such that an incorrect output value is present if the output floats for V2. Thus the undetectability of any faults in the enhanced scan mode is entirely due to the faults being functionally redundant and not because of a failure to initialize the faults.

The issue with hazard initialized tests is the number of tests can become very large for large circuits since the tests are essentially N-detect tests for the hard to detect faults. To reduce the test set, precise timing simulations are required. However expensive SPICE simulations can get prohibitive for large circuits and large values of N. Improved test generation methods are needed to ensure high coverage of all possible hazard activated opens in practical circuits. To overcome the drawback of N detect potential hazard initialized tests in the next chapter we propose a new DFT scheme that employ mixed LOC and LOS tests to explicitly target the undetected TSOFs that is discussed in the next chapter.

CHAPTER 7

Mixed LOC and LOS Tests for Targeting Hazard Activated Open Fault

7.1 The Mixed LOC and LOS Test Scheme

To improve TSOF test coverage beyond what is reachable by LOC and LOS tests based on steady state analysis, we propose a new DFT scheme [47] that employs multiple control lines to distribute the scan enable signal to the flip-flops. The idea is to use these control lines to allow a simultaneous mix of LOC and LOS tests, wherein some flip flops operate in the LOC mode and others in the LOS mode, and thereby increase the available scan states for launching the TSOF tests beyond those reachable by LOC and LOS test modes alone. This use of multiple scan enable signals to simultaneously have flip-flops operating in the LOC and LOS modes has been proposed earlier to improve the coverage of TDF timing tests, but in a more restrictive manner. This is because the scan enable is generally a slow speed broadcast signal that is unable to support at-speed LOS tests unless specifically designed to meet aggressive timing constraints. To minimize the overhead associated with implementing a high speed scan enable signal to support LOS, the hybrid TDF test generation methodology in [24] and similar methods have selected only a very small number of critical flip-flops to be operated in the LOS mode. This minimized the loading and drive requirements needed to speed up the scan enable signal. [25] avoided the need for an at-speed scan enable altogether by using the LOS flip-flops (along with LOC flip-flops) only to launch the TDF timing test; the test response was only captured and observed by the flip-flops operating in the LOC mode. While this combination of LOC and LOS modes led to an increase in

the available test launch states, restricting the response capture to the LOC flip-flops resulted in a significant loss in test output observability.

The target of our test methodology are open faults which, unlike small delay timing defects, cause delays of much longer durations. We are therefore not significantly constrained by the need for a fast scan enable to support LOS tests, although some low cost methods, such as pipelining to speed up of the enable signals will help support faster test timing and can potentially prevent the test escape of a few very high leakage opens. We therefore assume that we can independently combine LOC and LOS test modes using multiple partitions. In the experiments in the next section, we report simulation results for tests conducted with 2, 4 and 8 scan enable signals, with each case partitioning the flip-flops into an equivalent number of groups, each operated in either the LOC or LOS mode during any test. For example, for two partitions controlled by two independent scan enable lines, the circuit can be tested in the LOC-LOC, LOC-LOS, LOS-LOC and LOS-LOS test modes. For 4 partitions there are 16 such test mode combinations. These result in the availability of a much larger set of test launch states than from the LOC and LOS test modes alone, and increased TSOF detection coverage. In this study, we first of all assign the flip-flops to different scan enable signals randomly. Then we check the assignment to see if there are cases with flip-flops driving inputs of the same gate controlled by the same scan enable signals and re-assign these flip-flops in a simple greedy manner so as to minimize such cases. This can help to remove some of the shift dependence compared to pure LOS tests. More effective assignment of the scan enable lines to flip-flops may be possible [25] and will be the subject of future research.

To implement such tests in ATPG, we modify the original scan design structure into the structure shown in Fig. 7.1. Suppose we would like to employ two independent scan enables to control the two scan flip-flops. An additional MUX is added for each scan flip-flop and its inputs

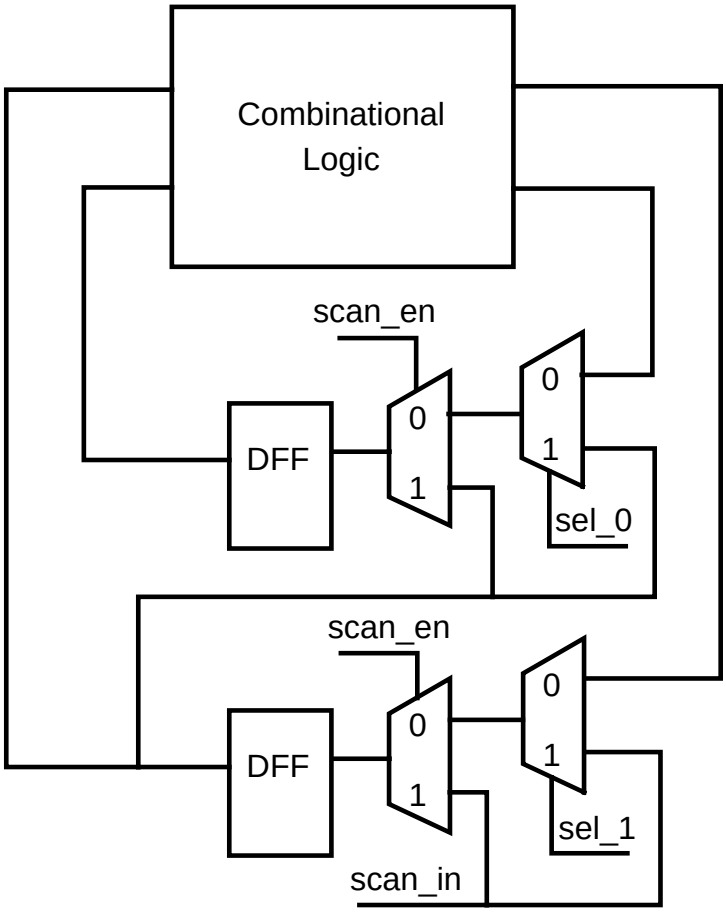

Fig. 7.1 Multiple Scan Enables Structure for Mix LOC and LOS Tests

are fed with data input and scan_in input of the original scan flip-flop. The data input of the scan flip-flop is fed with the output of the added MUX. The select inputs sel_0 and sel_1 of the two added MUXs are added as primary inputs for the circuit. The test generation in ATPG runs at the normal LOC mode as the V2 vector always comes from the output of the added MUX. However the ATPG has full control of both sel_0 and sel_1 inputs. When the V1 vector for the one of the two select inputs is 1 and the other is 0, the added MUX will select the scan path value as V2 vector to feed one scan flip-flop and data path value to feed the other, which means a mixed LOS and LOC test is applied to the circuit. Similarly, when the V1 vector for the two inputs is 0 or 1, a LOC or LOS test is applied to the circuit. And when ATPG sets V2 vector = 0 to the select inputs, the final V2 vector response can be captured back into the flip-flop. Thus the structure allows the

ATPG to generate mixed LOC and LOS tests to the circuits simultaneously and the ATPG will decide whether each flip-flop to be fed by LOC vector or LOS vector during each test launch cycle. Note the add MUXs in the circuit serve as ATPG test generation and fault simulation purpose only, and are they will not be implemented in the actual design.

7.2 Mixed LOC and LOS Tests Experimental Results for TSOF

CUT	LOC and LOS Undetected TSOF	Δ TSOF Coverage beyond LOC + LOS				Enhanced Scan undetected TSOF
		2 Scan_EN	4 Scan_EN	8 Scan_EN	Enhanced Scan	
s1423	3.28%	0.62%	0.80%	0.99%	1.61%	1.67%
s9234	0.62%	0.05%	0.05%	0.05%	0.05%	0.57%
s13207	1.09%	0.02%	0.04%	0.06%	0.06%	1.03%
s15850	0.90%	0.09%	0.14%	0.18%	0.21%	0.69%
s35932	2.73%	0.00%	0.00%	0.00%	0.00%	2.73%
s38417	1.17%	0.28%	0.42%	0.52%	0.97%	0.20%
s38584	0.92%	0.02%	0.02%	0.02%	0.02%	0.90%
b14	4.08%	0.61%	0.79%	0.83%	1.02%	3.06%
b15	7.87%	1.38%	1.85%	2.11%	3.74%	4.13%
b20	2.60%	0.61%	0.72%	0.74%	0.97%	1.63%
b21	2.89%	0.55%	0.63%	0.67%	0.87%	2.02%
b22	4.04%	0.57%	0.63%	0.66%	0.90%	3.14%
b17	9.22%	1.53%	1.94%	2.27%	3.64%	5.58%
b18	4.65%	1.35%	1.93%	2.17%	2.92%	1.73%

Table 7.1 TSOF coverage improvement for multiple scan enable and enhanced scan design

Table 7.1 shows the experimental results of mixed LOC and LOS tests for the undetected TSOFs. Column 2 shows the percentage of targeting TSOFs undetected by LOC and LOS tests. Columns 3 to 5 show the coverage improvement of employing 2, 4 and 8 independent scan enables

tests for the TSOFs. Column 6 shows the maximum coverage improvement in theory we can get from enhanced scan design. Column 7 shows the percentage of remaining undetectable TSOFs which are truly redundant. It can been seen that by employing 8 scan enables the fault coverage improvement is getting close to that from enhanced scan design. Since the enhanced scan undetectable faults are redundant and will never cause errors, we can remove them from the fault list. The total coverage for non-redundant faults is shown in Table 7.2 with enhanced scan design

CUT	LOC + LOS FC	2 Scan_EN	4 Scan_EN	8 Scan_EN	Enhanced Scan
s1423	97.53%	98.39%	98.86%	99.34%	100%
s9234	99.95%	100.00%	99.95%	99.95%	100%
s13207	99.94%	99.96%	99.98%	100.00%	100%
s15850	99.79%	99.88%	99.92%	99.97%	100%
s35932	100.00%	100.00%	100.00%	100.00%	100%
s38417	98.61%	99.04%	99.21%	99.40%	100%
s38584	99.98%	100.00%	99.98%	99.98%	100%
b14	98.56%	99.44%	99.63%	99.69%	100%
b15	94.86%	96.82%	97.62%	97.99%	100%
b20	98.66%	99.47%	99.55%	99.64%	100%
b21	98.79%	99.51%	99.69%	99.71%	100%
b22	98.73%	99.34%	99.58%	99.69%	100%
b17	94.97%	97.00%	97.41%	97.90%	100%
b18	95.90%	97.74%	98.59%	98.96%	100%

Table 7.2 TSOF fault coverage considering only non-redundant faults

approaching 100% coverage. The number of test vectors for each test type is shown in Table 7.3. It can be seen that the number of test vectors for the mixed LOC and LOS test are greatly reduced compared to the tests vectors of hazard initialized tests.

CUT	LOC TDF Tests	LOC TSOF Tests	ΔLOS Tests	ΔTest Vectors Beyond LOC + LOS		
				2 scan_en	4 scan_en	8 scan_en
s1423	117	122	23	5	8	12
s9234	200	225	29	1	1	1
s13207	291	278	127	1	2	3
s15850	243	264	116	4	6	8
s35932	102	118	11	NA	NA	NA
s38417	256	231	69	21	43	50
s38584	379	373	95	4	4	4
b14	835	935	165	44	52	62
b15	977	907	289	149	196	218
b20	1316	1390	182	66	87	94
b21	1568	1775	179	75	76	91
b22	1253	1405	201	79	96	92
b17	1428	1283	492	297	380	447
b18	1643	1638	886	288	413	634

Table 7.3 Number of test vectors for each test type

7.3 Mixed LOC and LOS Tests Experimental Results for Cross Wire Open Faults

CUT	Δ Multiple Scan_en Tests FC			ΔEnhanced Scan FC	Enhanced Scan Undet
	2 scan_en	4 scan_en	8 scan_en		
b14	0.72%	0.77%	0.77%	1.36%	8.05%
b15	5.01%	5.51%	6.24%	7.75%	7.97%
b20	0.98%	1.00%	1.02%	1.34%	5.30%
b21	1.03%	1.12%	1.16%	1.41%	6.47%
b22	1.02%	1.08%	1.13%	1.27%	6.80%
b17	3.67%	4.25%	4.62%	7.82%	8.73%
b18	3.13%	3.58%	3.74%	4.47%	5.70%

Table 7.4 CWO coverage improvement with multiple scan enable tests and enhanced scan tests

We employ the same DFT scheme to target the undetected cross wire open faults (CWO) and the experimental results are reported in the following two tables. Table 7.4 shows the fault coverage improvement for all possible CWO faults when cell layout information is not available and Table 7.5 shows the results for the CWO faults with certain fixed layout information. For most

CUT	Δ Multiple Scan_en Tests FC			ΔEnhanced Scan FC	Enhanced Scan Undet
	2 scan_en	4 scan_en	8 scan_en		
b14	1.41%	2.02%	2.22%	2.72%	8.07%
b15	3.10%	3.78%	4.11%	7.05%	6.26%
b20	1.73%	1.78%	1.89%	1.89%	4.54%
b21	2.07%	2.27%	2.27%	2.57%	6.10%
b22	1.74%	1.92%	1.99%	2.28%	5.19%
b17	3.76%	4.27%	4.75%	9.50%	8.85%
b18	3.67%	4.17%	4.51%	5.65%	4.26%

Table 7.5 CWO coverage improvement with multiple scan enable tests and enhanced scan tests

of the circuits with 8 scan enables we get improvement close to results from enhanced scan tests. Note that there are many CWO faults undetectable by enhanced scan tests. This is because to

CUT	# LOC TDF tests	# 2 Scan_en Tests		# 4 Scan_en Tests		# 8 Scan_en Tests	
		Unknown Layout	Known Layout	Unknown Layout	Known Layout	Unknown Layout	Known Layout
b14	866	16	14	17	16	14	12
b15	953	113	48	131	57	134	65
b20	1292	37	26	35	29	36	34
b21	1621	28	27	33	32	36	28
b22	1307	41	25	51	37	59	39
b17	1441	235	85	294	103	370	137
b18	1435	258	110	347	142	423	178

Table 7.6 Number of multiple scan enables tests for each test type

activate a CWO fault and propagate the fault effect to the state outputs, more constraints need to be satisfied, and the possibility of conflict between the constraints will increase such that many faults become redundant. Table 7.6 shows the number of test vectors for each test type. As we can see, to further improve test coverage of cross wire open faults for very low DPPM production, we still need a significant number of tests compared to the number of TDF test vectors. This is the trade off of between test quality and test cost we have to balance.

CHAPTER 8

Transistor Stuck Open Fault Diagnosis

8.1 Diagnostic Fault Simulation for Transistor Stuck Open faults

Recall that in Chapter 3 we have generated the targeted tests for TSOFs by using the ATPG to target the corresponding TDF faults inside the replacing logic structures. Here we make use of such targeted tests to conduct fault simulation and build an initial dictionary for diagnosis. The dictionary consists of each fault and its corresponding syndrome which contains the indexes of the test vectors detecting the fault and indexes of the outputs observing the fault effect. Faults with the same syndrome are put into one group (single fault with unique syndrome is seen as a group as well). Based on the dictionary information an initial diagnosis coverage can be calculated as number of fault groups divided by total number of detected faults. Note here that fault collapse is considered and only non-equivalent faults are in the fault list. Ideally we want the coverage to be 1, which means for every group there is only one fault (or equivalent faults) and every detected fault can be distinguished from each other. Thus for faults within a group we then employ exclusive test generation to further distinguished the faults and improve the diagnosis coverage.

8.2 Distinguished Test Generation for Transistor Stuck Open faults

A recent paper [10] proposed a methodology to generate the distinguishing test for pair of TDFs using existing ATPG tool. We borrow the idea from the paper and apply it to the TDFs in our

transformation logic structures such that the generated distinguished test can be used for distinguishing the corresponding pair of TSOFs in the original circuits.

Figure 8.1 shows two logic structures for modeling the slow-to-rise and slow-to-fall TDFs at circuit nodes x1 and x2 respectively in ATPG tool. For logic (a), with the presence of the D flip-

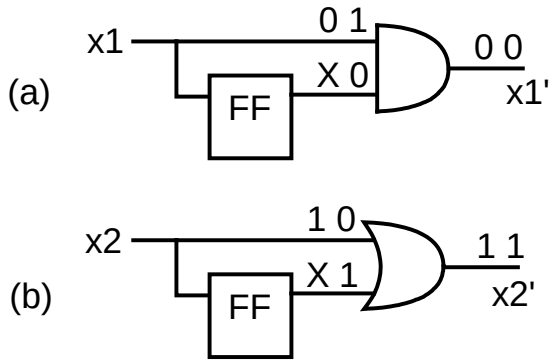

Fig. 8.1 Logics modeling of TDF faults

flop, the first vector received by the input of the NAND gate is always X (unknown), and by applying “00”, “01”, “10” or “11” vector pair to the logic’s input x1, we have x1’ = “00”, “00”, “X0” or “X1”. As we can see the logic creates a slow-to-rise (“01”) fault effect at output node x1’ because only the “01” vector pair received by node x1 will produce “00” at node x1’ such that the second vector “0” at x1’ is different from the second vector “1” at node x1. Similarly, for logic (b) when x2 receives “00”, “01”, “10” or “11” vector pair, at node x2’ we have “X0”, “X1”, “11” or “11”; only “10” will produce the incorrect values “11” at node x2’ and thus logic (b) can be used in ATPG to represent a slow-to-fall TDF fault.

By using a 2 to 1 MUX and feed the two inputs of the MUX with the fault free node x and the fault modeling logic for the node, we can use ATPG to generate a distinguished test for the fault free node and the “faulty” node by targeting a stuck-at fault at the select input node z of the MUX, which is shown in Figure 8.2. This is because in order to detect the stuck at fault, the test needs to produce different values at the two inputs of the MUX, and recall our discussion in the previous

paragraph, only a vector pair (0 1) can do that. Thus this generated test is also a test for the slow-to-rise TDF fault at node x.

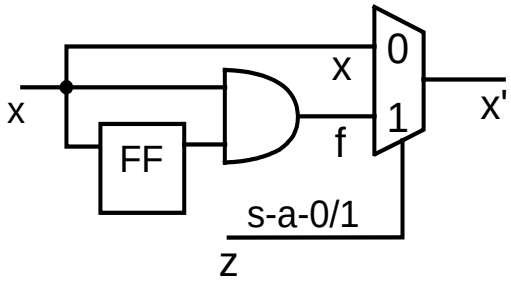

Fig. 8.2 Exclusive test generation for detecting TDF

Similarly, to generate an exclusive test for a pair of faults f1 and f2 at circuit notes x1 and x2, we use the structure shown in Figure 8.3. This structure is inserted between the original circuit nodes x1 and x2. when the shared MUX select input z = 0, only fault f1 is present in the CUT since MUX1 will select the logic modeling fault f1 and MUX2 will select the fault free node x2; similarly when z = 1, only fault f2 is present in the CUT. Thus if the ATPG can generate a test to

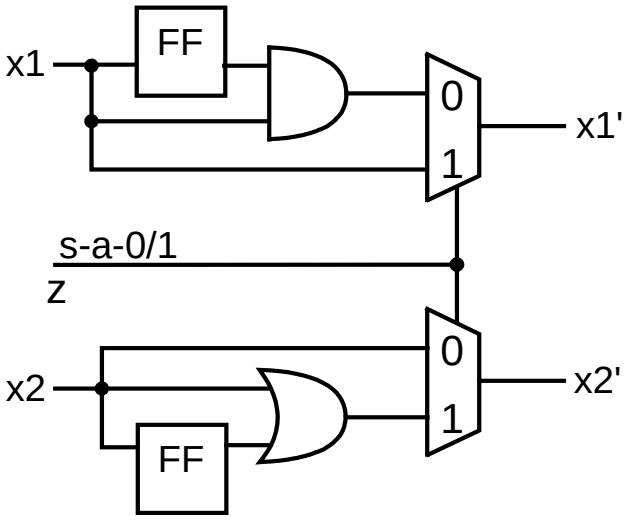

Fig. 8.3 Exclusive test generation logic for a pair TDFs

detect the stuck-at fault at MUX select input z, the test will produce different circuit output responses for the two cases of only fault f1 or fault f2 is present in the circuit. For the output responses to be different, either the test detects one fault but not the other, or both faults are

detected by the test but at different outputs. For either case, faults f1 and f2 is distinguished by the test.

After the initial diagnostic fault simulation using detection test vectors, the TSOFs are distinguished into different groups. For each group having more than one fault, two random faults are selected from the group and the exclusive test generation logic is constructed and inserted into the circuit. We employ the ATPG to target the stuck-at fault at the select input z of the logic. If either stuck-at 0 or stuck-at 1 fault is detected, the fault pair can be distinguished by the test. We then conduct the diagnostic fault simulation for all the faults within the group using this generated test to see if the other faults can also be distinguished by the test. If the test distinguished the faults into different groups, for each sub-group with more than one fault we repeat the exclusive test generation and diagnostic simulation procedure until all fault pairs within the original group are targeted. If the stuck-at fault is identified as redundant fault by the ATPG then the two faults are equivalent and one of them can be removed from the fault list, as one fault can be used to represent

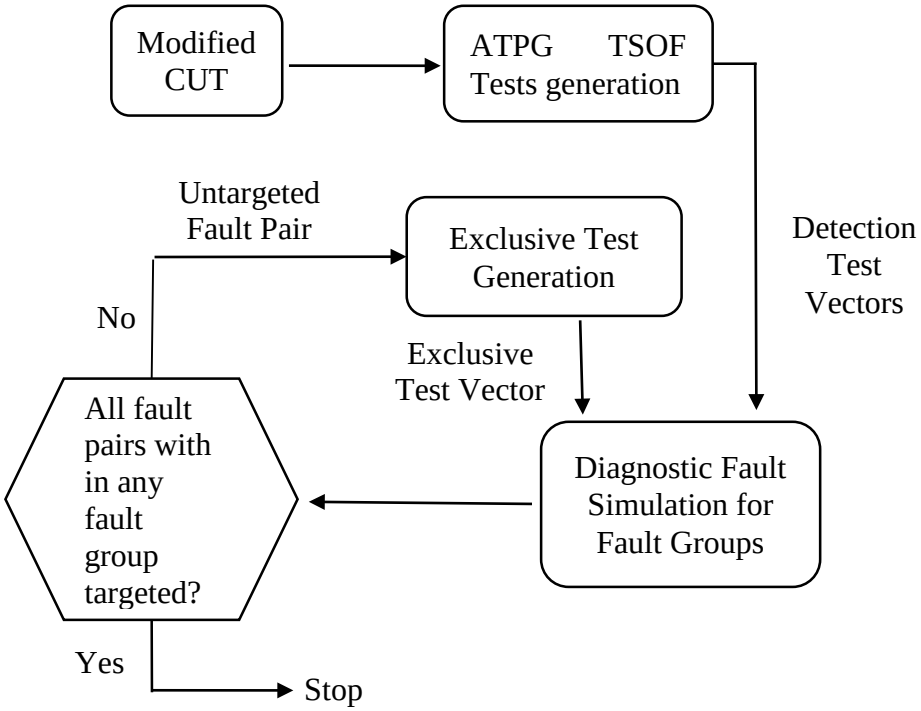

Fig. 8.4 TSOF diagnosis flow

the two faults. If the stuck-at fault is undetected by the ATPG then the two faults are put into an undistinguished group and one of them is picked to continue the exclusive test generation and diagnostic simulation procedure with other untargeted faults. Figure 8.4 shows the flow of diagnostic simulation and test generation procedure.

8.3 TSOF Diagnosis Experimental Results

In Chapter 7 we introduced our DFT scheme which employs multiple independent control lines to distribute the scan enable signals to different set of flip-flops. The idea is to use these control lines to allow a simultaneous mix of LOC and LOS tests, wherein some flip flops operate in the LOC mode and others in the LOS mode, and thereby increase the available scan states for launching the TSOF tests beyond those reachable by LOC and LOS test modes alone. This scheme is also applied to TSOF diagnosis to improve diagnostic coverage. Here we report simulation results from tests conducted using two scan enable signals (each enable signal independently controls the same number of flip-flops), with each partition operated in either the LOC or LOS mode during any test. For two partitions controlled by two independent scan enable lines, the circuit can be tested in LOC-LOC, LOC-LOS, LOS-LOC and LOS-LOS test modes. We initially employ LOC tests to conduct diagnostic fault simulation and exclusive test generation for the targeted TSOFs. We then apply the mixed LOC and LOS tests using the DFT scheme for fault simulation and exclusive test generation.

Table 8.1 shows the result of TSOF diagnosis running in LOC mode. The second column shows the total number of TSOFs in each circuit. Fault collapsing is considered as equivalent faults are undistinguishable. TSOFs that are identified as redundant faults by the ATPG running in LOC mode are removed from the fault list. The number of LOC detection tests for each circuit are shown in the third column. The fourth and fifth column show the TSOF fault coverage and initial

diagnosis coverage from the detection test vectors. The last two columns show the additional diagnosis coverage achieved by the exclusive tests and the number of exclusive test vectors.

Table 8.2 shows the experimental result using two independent scan enables running in mixed

CUT	#Target TSOFs	LOC Mode				
		# Detection Tests	Detection Test FC	Detection Test DC	Exclusive Test △ DC	# Exclusive Tests
s1423	1158	126	92.49%	80.22%	2.76%	32
s9234	1985	209	91.18%	80.60%	2.17%	43
s13207	4990	273	75.95%	64.05%	1.98%	99
s15850	6553	259	82.28%	70.14%	0.98%	64
s35932	19282	118	99.34%	84.30%	0.15%	28
s38417	19562	209	83.04%	71.54%	1.02%	200
s38485	22651	355	93.44%	85.34%	2.60%	589
b14	13045	905	88.59%	80.11%	2.67%	348
b15	18548	887	83.12%	75.71%	0.95%	177
b20	26438	1336	89.91%	81.63%	2.05%	543
b21	28009	1745	89.99%	82.40%	1.71%	479
b22	40369	1385	89.16%	80.68%	1.83%	739

Table 8.1 Experimental results for LOC mode

LOC and LOS mode. By comparing the data in the two tables we can see both detection test fault coverages and diagnosis coverages are greatly improved (roughly 10%). For circuit b15 which has low fault coverage, further coverage improvement can be achieved by employing 4 or even 8 independent scan enables mixed LOC and LOS tests to the circuits.

The reason only moderate additional diagnosis coverage is achieved by the exclusive tests is the ATPG often failed to identify the undetected stuck-at fault at the control input of the MUX as redundant fault or not, due to running in sequential mode. Thus for the reaming undistinguished

faults we do not know if any of them are equivalent or not. It has been studied in [6] that most of the undetected stuck-at faults at the MUX's control input can be identified as redundant faults when two time frame expansion is applied to the circuits and combinational ATPG is employed to target the faults. Thus diagnosis coverage can be further improved if the equivalent faults can be identified.

CUT	#Target TSOFs	Mixed LOC and LOS Mode				
		# Detection Tests	Detection Test FC	Detection Test DC	Exclusive Test △ DC	# Exclusive Tests
s1423	1158	109	98.36%	91.19%	1.38%	16
s9234	1985	201	99.21%	92.49%	2.37%	47
s13207	4990	309	99.18%	92.46%	1.54%	77
s15850	6553	261	99.60%	92.60%	1.30%	85
s35932	19282	110	99.34%	84.37%	0.07%	13
s38417	19562	229	98.80%	92.21%	1.29%	253
s38485	22651	340	99.84%	95.40%	1.24%	280
b14	13045	908	97.14%	89.74%	2.74%	357
b15	18548	879	92.43%	86.93%	0.90%	167
b20	26438	1165	98.56%	91.58%	1.94%	512
b21	28009	1487	98.32%	91.57%	2.15%	601
b22	40369	1158	97.46%	90.02%	1.58%	637

Table 8.2 Experimental results for 2 scan enables mixed LOC and LOS mode

CHAPTER 9

Conclusion and Future Work

Commonly employed LOC TDF timing tests are not sufficient for targeting CMOS open defects capable of generating erroneous circuit outputs. Cell aware tests [7] have been proposed to target defects within the library cells. However due to the structure limitation of scan based LOC and LOS tests, many open defects are still undetected, but can be activated by common hazards. CMOS circuits experience a large number of hazards during switching transitions. Such hazards can activate open defects by pre-charging a faulty gate output to an incorrect value which is then locked in once the inputs stabilize and force the gate output to a high impedance state. Consequently, many open defects that are assumed to be functionally redundant from Boolean timing unaware analysis, can actually cause circuit failure and must be targeted during manufacturing tests. Therefore, all opens must be targeted during test, unless proven to be redundant, not just those that are detectable from functional states or by LOC tests.

Depending on the threshold voltages variation and locations of the CMOS open defects, timing delay due to the net leakage current charging or discharging the gate output can vary significantly, especially when the open occurs near the gate terminal of a transistor with the trapped charges at the gate terminal to partially turning on the victim transistor, that giving rise to significant leakage current. LOS timing tests are known to have better test coverage than LOC tests due to the less correlation between V1 and V2 vectors, and thus can be used to target opens undetected by LOC tests. However, a drawback of LOS tests is the test launch speed is limited by the timing of the

slow scan enable control signal. In order to maximize the detection of CMOS open defects, LOS tests need to be applied at the fastest possible speed (up to the functional clock rate) within the timing limitations of the scan enable. We have presented the first test scheme [50] to reliably evaluate the switching speed of the scan enable signal. This can vary significantly for individually manufactured instances of the same design due to normal process variations at advanced technology nodes, amplified by near quadratic delays in the long interconnect lengths of the broadcast signal. Once the scan enable speed is determined, LOS tests can be applied at the fastest, most effective speed.

To improve the open coverage beyond that of LOC and LOS tests for achieving very low DPPM, we have proposed two methodologies, N detect potential hazard initialized tests [46,48] and multiple independent scan enables mixed LOC and LOS tests [47] for targeting the undetected faults. The experimental results show promising test coverage improvements which are close to the coverage of enhanced scan structure tests. We further show that virtually all of the remaining undetected opens are in fact truly redundant, and do not pose a threat even in the presence of hazards.

Traditional transistor stuck open fault (TSOF) tests are not sufficient to screen out all possible CMOS open defects because another type of open, the cross wire open (CWO) fault, is commonly found in complex gates. We have showed that commonly employed scan based LOC TDF timing tests fail to detect many, between 30% and 60%, of such open faults [49]. We therefore presented a methodology to explicitly target CWO faults using commercial ATPG tools [49]. Our approach uses circuit transformation that converts the detection of CWO faults into the detection of corresponding transition delay faults in the transformed circuit, which can then be conventionally targeted by the ATPG. Furthermore, since such open defects can be expected to exhibit long delays,

first LOC and then also LOS mode tests are generated to maximize CWO fault coverage, even if the LOS tests may need to be run at relatively slow speeds due to timing limitations on the scan enable. Similar to TSOFs, LOC and LOS undetected CWOFs can also be activated by common hazards and we employ the same mixed LOC and LOS tests scheme to target these undetected faults.

To understand the yield loss during early stages of the IC manufacturing process, it is important to identify the possible open defects locations inside the failed chips, as some defects due to process or design issues can be further eliminated to improve the yield. Current stuck-at test based TSOF diagnosis methodologies are no longer effective due to the timing fault behavior of many TSOFs in modern industrial ICs using advanced technology. While TDF diagnostic test generation [10] has been addressed in recent research, it have been accepted that TDF tests cannot effectively target all the TSOFs. In this work we first conducted diagnosis fault simulation using the generated detection tests for TSOFs and built an initial fault dictionary. We then borrowed the idea of TDF exclusive test generation scheme in [10] and applied it to TSOF diagnostic test generation. Our multiple scan enable controls DFT scheme is implemented in the circuit such that many more test launch states are generated in a mixed LOC and LOS mode to help both detect and diagnose those TSOFs that are missed by the traditional scan based timing tests, but can actually be activated by hazards to cause circuit errors. Experimental results show promising diagnosis coverage of the TSOFs. Although for large industrial circuits the dictionary based diagnosis scheme may not be very practical as massive dictionary data storage for large circuits requires lots of memory, dictionary compression schemes can be applied to reduce storage requirement. Also note the proposed exclusive test generation scheme for TSOFs can still be applied to fault candidates during effect-cause diagnostic analysis to narrow down the possible locations of the open defects.

Future work of open fault detection will be hazard initialized tests generation combining ATPG and static timing analysis for reducing the tests volume of current N detection based hazard initialized tests. More efficient test generation schemes for targeting the cross wire open faults need to be addressed, as our technique requires test generation for multiple copies of the CUT. Currently our proposed open faults targeted test generation scheme focuses on AOI and OAI type complex gates only In our future work opens within the XOR, XNOR and multiplexer gates need to be addressed as well.

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