Experimental Investigation of a Liquid Immersion Cooled Electronics Module using Two-Phase Heat Transfer for Thermal Management

by

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Abstract

As society's demand for constant connectivity to one another grows, both from an economic and social perspective, the requirements on high performance data centers throughout the world will as well. The expeditious transfer of data over reliable and efficient networks is as much a problem that must be addressed from a thermal management perspective as it is from a computer science one. The speed at which data is transferred is directly related to the amount and density of heat that a processing element emits. System reliability is tied to the operating temperature at which these high performance computing devices are maintained. The need for energy efficiency of any design will only continue to grow as worldwide consumption increases in the face of dwindling global power resources. With these macro-scale issues in mind, the current study proposes a thermal management solution for near and far-term high performance electronic devices which addresses all three of these concerns. The proposed system is a small form factor, power dense cartridge which houses heated elements meant to simulate the heat output of electronic components typically found in servers or other high performance computing systems. These elements are immersed in a low boiling point dielectric fluid where, when powered to an adequate heat flux, cools the devices through two-phase heat transfer. The combination of latent and convective heat transfer from boiling results in incredibly high heat transfer coefficients, translating to lower operating temperatures and greater system reliability. In allowing the heated elements to boil in a pool of dielectric fluid, power dissipations of over 300 W have been achieved at an operating temperature of 77°C using the bare silicon surface.

By introducing boiling surface enhancements, microporous and microfinned surfaces, operating temperatures at the maximum power dissipation decrease by roughly 18°C. By pumping dielectric fluid through the cartridge, power dissipations over 700 W have been achieved at a surface temperature of only 71°C. At this latter power dissipation, the cartridge, which is only 300 mm x 150 mm x 38 mm (L x W x H), has eight times the volumetric power dissipation capabilities of a similar system that uses air cooling techniques. Particle Image Velocimetry (PIV) measurements, both in the single and two-phase, have been taken to ascertain flow distribution characteristics as well as assist in the development of ways in which to divert flow over critical areas of interest within a densely packed electronics enclosure.

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List of Symbols

a channel width (m)

b channel height (m)

A surface area (m^2)

c_p solid specific heat (J/kg·K)

C_{pl} liquid specific heat (J/(kg·K))

C_{sf} Rohsenow correlation surface factor constant

d diameter

e thermal effusivity (J/(m^2·K·$sec^{1/2}$))

g gravitational acceleration constant (m/sec^2)

h heat transfer coefficient (W/(m^2·K))

h_{lv} latent heat of vaporization (J/kg)

k thermal conductivity (W/(m·K))

L length (m)

L_{heater} length of heated element (m)

N number of fins

q heat transfer (W)

q" heat flux (W/m^2)

$\overline{Nu}_L$ average Nusselt number over the length of the heater

P_l liquid pressure (Pa)

Pr Prandtl Number

Ra_L Rayleigh Number at the trailing edge of the heater

T temperature (K)

Subscripts

b base property

CHF Critical Heat Flux

c condenser property

conv convective property

f fin property

F forced convection related

Gr Graetz number

h heater property

i liquid-vapor interface property

l liquid state property

m mean

mod modified

N natural convection related

p particle property

rad radiative property

s surface property

sat saturation property

tot total

v vapor state property

w heated wall surface property

∞ ambient property

Greek Symbols

α channel aspect ratio (b/a)

Δ change in property

δ_t thermal boundary layer

ε emissivity

ρ density (kg/m^3)

μ dynamic viscosity ($kg \cdot m/sec$)

ν kinematic viscosity (m^2/sec)

η efficiency

σ_{SB} Stefan-Boltzman constant

σ surface tension (N/m)

τ time constant (sec)

Chapter 1: Introduction

Technological breakthroughs have governed society's ability to share ideas and conduct trade throughout our history. From the navigational advancements that brought the first pioneers across the Atlantic, to the first use of the transatlantic telegraph cable in 1858, and on to the development of the internet, people have strived to develop ways in which to communicate and do business with one another faster and more efficiently. With the previously mentioned historical progression, data transfer speeds have accelerated from taking many men and many months to deliver a message via boat, to delivering information over the cloud in a matter of seconds. Clearly these discoveries have broken down cultural and economic barriers in a time frame that once seemed unfathomable.

The desire to exchange information more expeditiously continues today in the form of society's need for constant connectivity to various social networking platforms and the conduction of vital commercial transactions and data storage within cloud based computing. Ecommerce is a giant pecuniary industry representing roughly six trillion dollars of global transactions in 2013 [1] which, according to recent data published by the International Monetary Fund (IMF), is larger than the GDP of all countries save China and the United States [2]. Ecommerce transactions can be broken down into two categories, Business to Consumer (B2C) and Business to Business (B2B). The former represents general online shopping purchases while the latter represents industry transactions such as raw material, equipment, new construction purchases, etc. These categories are indicators of the growth and relevance of data processing

requirements that successful companies will require to be impactful players in a fast-paced and competitive global economy. Figure 1 projects significant growth in the coming years within the B2C sector, topping over two trillion dollars by next year [3]. As for the B2B division of Ecommerce, Figure 2 shows the breakdown of the relative importance for various sectors within commercial transactions. Notice that over half of this division goes to manufacturing, a cornerstone of a strong economy. This indicates the importance of data transfer not just to the success of individual commercial entities but also to the development and prominence of national economies. As more money is transferred over online and cloud based computing, the requirements for faster and more efficient means by which to process the data will grow as well.

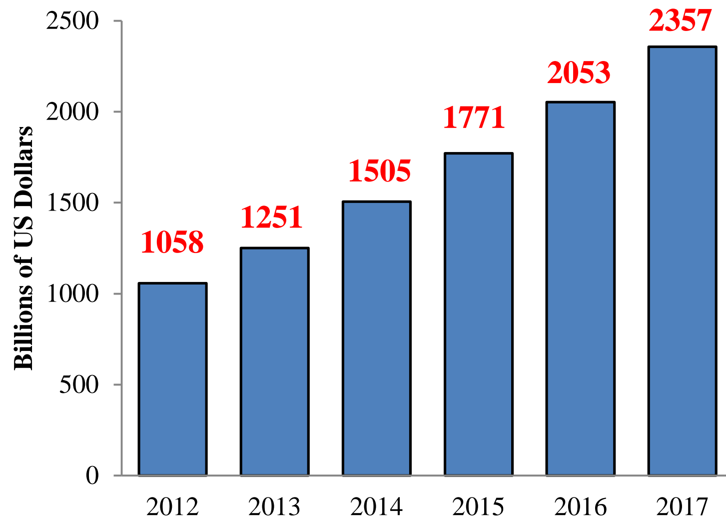


Figure 1 – B2C Ecommerce transactions 2012-2017 **[3]**

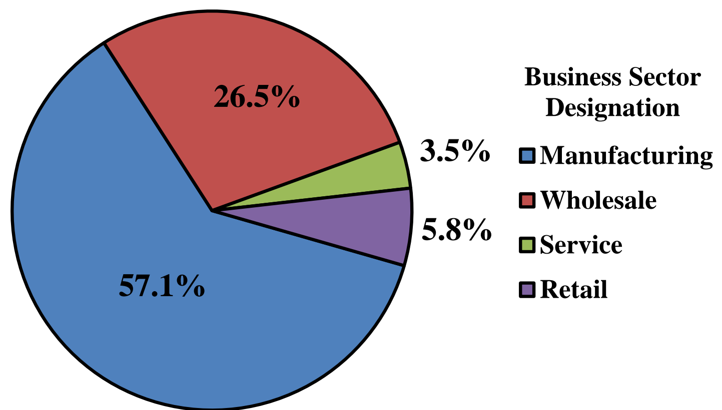


Figure 2 – B2B Ecommerce breakdown **[3]**

As mentioned previously, this need will not be solely based on economics. Cultural mandates for constant connectivity will stress information transfer equipment to new levels. The

primary forms of this strain will come from streaming video transfer services along with the continued explosive growth of social media outlets. An interesting infographic published by Intel©, presented as Figure 3, illustrates the enormous amount of data transferred in any given minute over the internet as well as how this data is distributed [4]. From Figure 3 it is evident that data hungry streaming video transfer accounts for the majority of traffic with Netflix© and Youtube©. The social media giants Facebook© and Twitter© are not that far behind in terms of the amount of information they transfer at any given moment. The most important takeaway

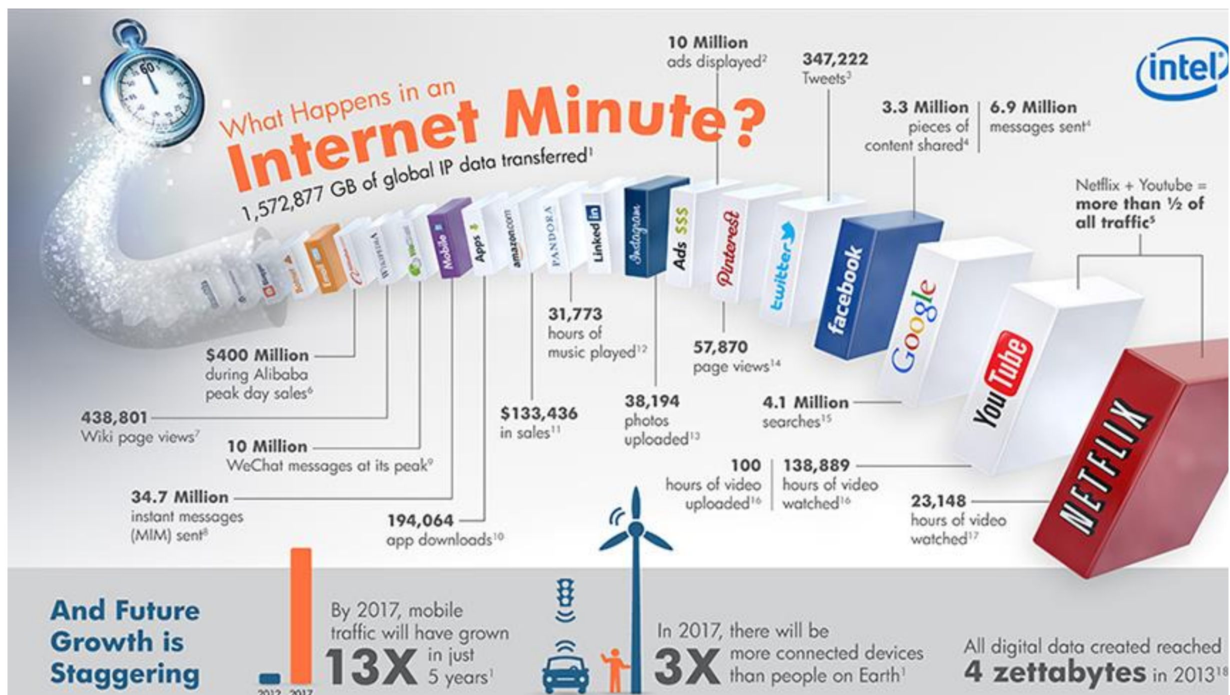


Figure 3 – Social media and video transfer data infographic **[4]**

from Figure 3 however is that while this demand is currently staggering, it is only expected to grow tremendously in the coming years as more devices become connected and society expects that these devices bring them up to the second information on a growing number of fronts. This information can be as far reaching as providing instant vehicular diagnostics and driving patterns for traffic control or monitoring human vitals to help people live a healthier lifestyle. All of

these data logging initiatives can make society be more functional and efficient, but whatever information is transferred and monitored will need to be stored and processed in some fashion. Therefore, it is to be expected that tomorrow's data center demands will grow as people become more connected, both socially and economically.

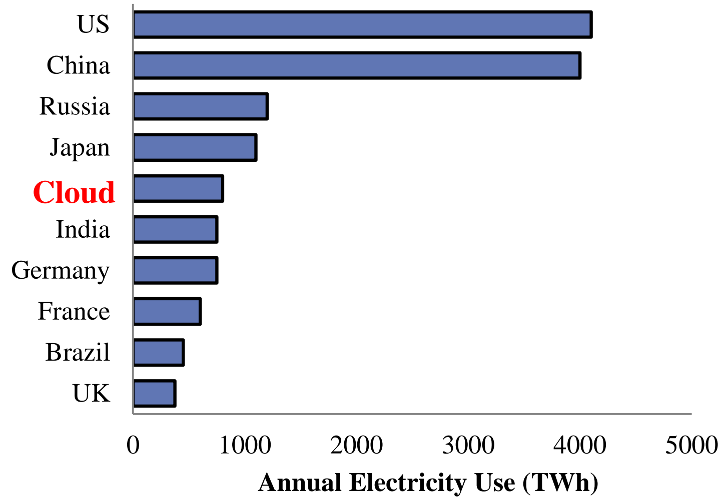


Figure 4 – Cloud power consumption vs. industrialized nations [5]

Note: Cloud consumption here includes telecommunications infrastructure, but not the entire ICT ecosystem

This growth in demand is most evident in the enormous power consumption that data centers presently command as well as in its recent and projected growth. Global Information-Communications-Technologies (ICT) infrastructure, a good measure of cloud based computing systems, is said to consume 1,500 TWh of energy, a number that approaches 10% of the world's total electricity generation [5]. At an assumed average American residential energy consumption value of 10,000 kWh, this number

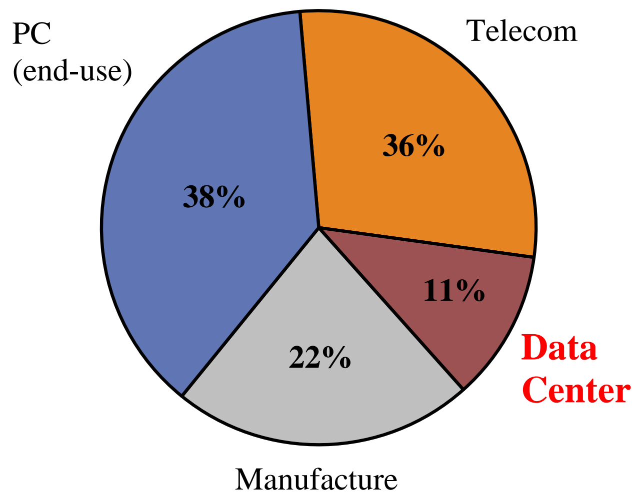


Figure 5 – ICT infrastructure power consumption breakdown [5]

represents roughly 150 million households. From a financial standpoint, at an assumed dollar/kWh value of ten cents, this number represents roughly 150 billion dollars. As shown in Figure 4, cloud based computing consumes more electricity than several industrialized countries including India and the UK [5]. The distribution of energy going to cloud based computing is shown as Figure 5. While the manufacture of the equipment, telecom equipment in the field used to distribute the data as well as the power drawn by the end-users equipment consume a great deal of the energy, the data center itself is power hungry coming in at slightly over 10% [5]. The problem that thermal and packaging engineers face in the near future is that these numbers have increased in recent years and only show signs of rising further. Data center power numbers rose 7% from 2012 to 2013, going from 38 GW to 40 GW [6]. Compounding this problem is the fact that the planet has dwindling energy resources in a time when global energy consumption is significantly on the rise. In 2010, global energy consumption was 153 PWh and projections to 2020 are 185 PWh and even higher in 2040 at 240 PWh [7]. This represents a 21% increase over the next decade and a 57% increase over the next thirty years in electricity demand. Of the power going to the data center, roughly half of it is dedicated to the cooling solution implemented as shown in Figure 6 [8]. Due to the increases in demands on these systems in tandem with a growing global energy crisis, it is incumbent upon engineers to find better and more efficient designs for future systems.

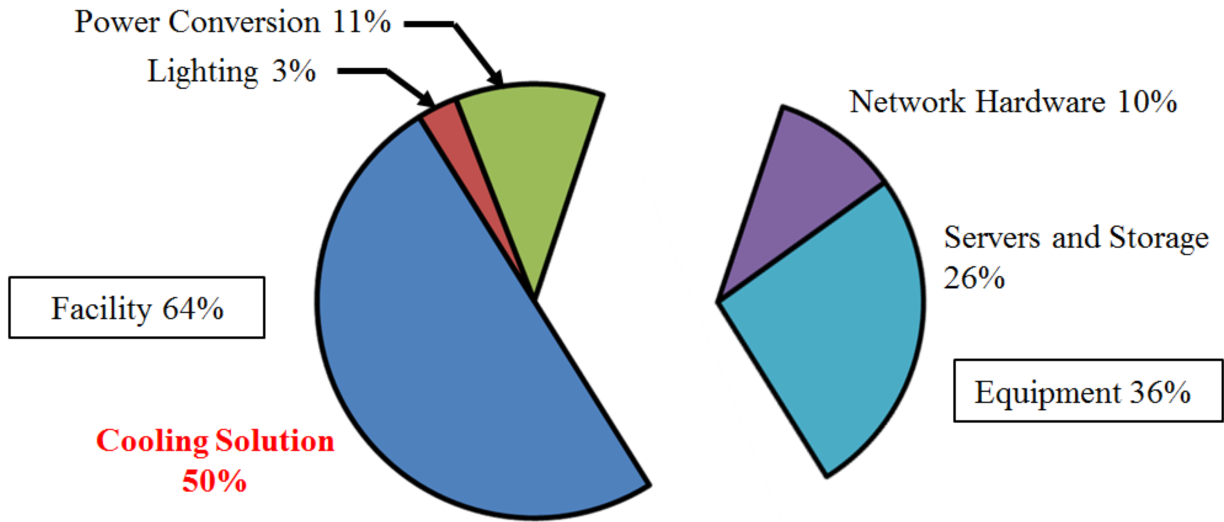


Figure 6 – Data center power consumption breakdown [8]

With such a significant portion of the data center's power draw going to the thermal management solution employed, this is an area where packaging and thermal engineers can make a significant impact. The purpose of this study is to illustrate the effectiveness of a modular small form factor two-phase liquid immersion cooled solution for future data center applications as well as promote new experimental techniques meant to enhance and ensure consistent performance from such a system. While there are still lingering fears within the data center design community about using liquid cooling, even dielectrics, in such close proximity to electronics, the industry has recently studied and implemented a variety of liquid immersion cooled solutions with marked success. Systems similar to that proposed within this study have already been implemented in the industry. Iceotope™ installed a modular Line Replaceable Unit (LRU) system at a company called PSNC© in Poland, reporting a 40.8% reduction in power requirements when compared to a traditional air cooling method [9]. This solution is a single phase natural convection method where buoyancy drives the fluid movement and heat transfer within the cartridge and overall rack assembly. An image showing the Iceotope solution is

provided as Figure 8. A modular two-phase liquid cooling approach very similar to that proposed within this study where the fluid is pumped through the cartridge has also been proposed [10], forming the foundation for LiquidCool Solutions© product line. Green Revolution Cooling (GRC) and Intel© reported a 90% reduction in data center thermal management energy consumption using a single phase liquid immersion cooling approach with mineral oil as the working fluid [11]. This is an Open Bath Immersion (OBI) approach where many complete server boards are immersed in large baths of cooling fluid. A sample image of a GRC installation is provided as Figure 7. A two-phase OBI approach at a Bitcoin mining farm in Hong Kong reported a Power Usage Effectiveness (PUE) of 1.02 [12]. PUE is a common Figure of Merit (FOM) for data centers as it is the ratio of the power drawn by the data center and the processing power yielded by the data center. An ideal PUE value would be one, where every watt of power delivered to the data center was

Figure 8 – Typical Iceotope Installation

Figure 7 – OBI Installation Example

used solely for processing, i.e. no overhead power consumption for operations. Building on the success of the Hong Kong installation, a team of 3M and SGI are currently building a data center using the same method in the United States [13]. The importance of PUE cannot be understated as Google©, a major player in the data center industry, not only tracks and reports the value for all of their data centers but has also made a concerted effort to reduce it year by year as shown in Figure 9 [14].

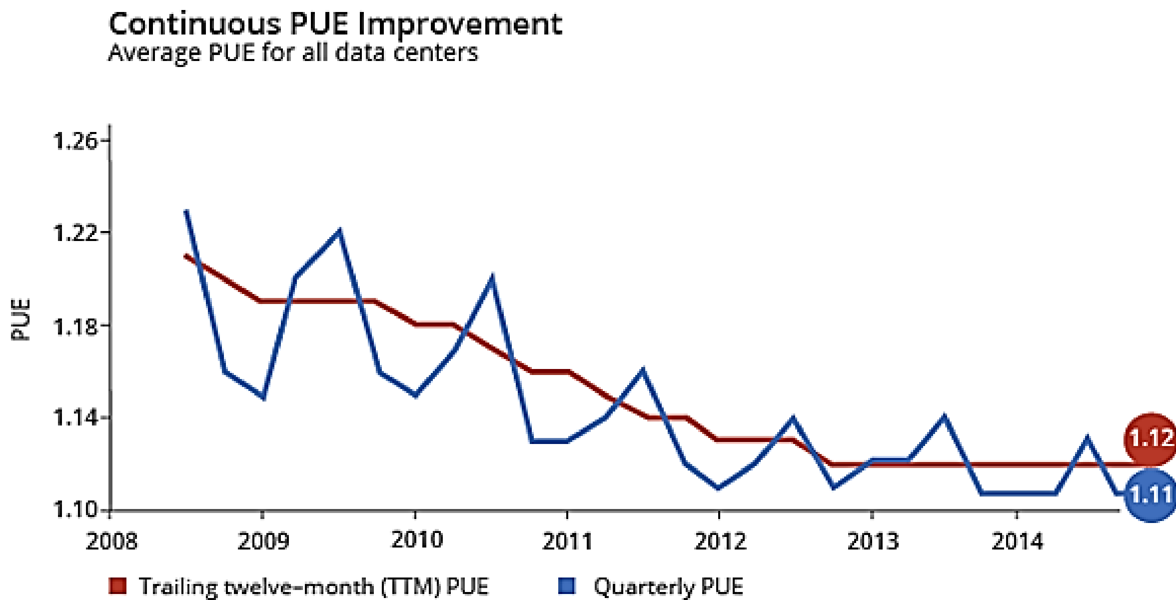


Figure 9 – Google's reduction in data center PUE [14]

The flexibility of forcing fluid through the liquid filled cartridge as opposed to using pool boiling as the sole means of heat transfer is explored in this study. While this study focuses on using low boiling point dielectrics as the working fluid, forced convection methods in liquid filled enclosures with mineral oil has already been studied. Most notably, the work of Eiland *et al* [15] reported a partial PUE (pPUE) of 1.06. This pPUE only takes into account the energy required to deliver the heat into the working fluid and does not take into account the energy required to exhaust the heat from the working fluid into the ambient environment. A total PUE

would be slightly higher once one decided upon a method of extracting the heat from the working fluid. There are a number of state of the art air cooled facilities that are achieving incredible PUE numbers, although not as low as liquid cooled systems. State of the art data centers at Google and Facebook have achieved PUE's of 1.12 [14] and 1.08 [16] respectively. An American Society of Heating, Refrigeration and Air Conditioning Engineers (ASHRAE) innovation award was given to a 7.2 MW data center for Oracle© in West Jordan, UT. Like the Google and Facebook systems, this facility brings in outdoor air to cool servers from the dryer and more moderate temperature surroundings in West Jordan to reduce air conditioning costs, resulting in a PUE of 1.25 [17]. Care and additional design considerations must be taken into account for these types of facilities as air that is too dry can cause a static discharge on the electronics within the data center. Typically, the precaution taken to prevent this failure is an inline humidifier for the incoming air to control moisture content appropriately. The PUE numbers presented for all of these solutions are even more impressive when compared to the current Environmental Protection Agency's (EPA) current best practice value of 1.50 for data centers [18]. A summary bar chart of the PUE case studies presented is shown as Figure 10 highlighting the primarily liquid cooled solutions and their efficiency advantages over more traditional air cooled systems. Even indirect liquid cooling systems, with the working fluid flowing through a thermally attached cold plate, has been shown to reduce facility power requirements by as much as 45% over air cooling methods [19]. The current study builds on elements of liquid cooling solutions already implemented to show how two-phase heat transfer can achieve higher power dissipations in a smaller form factor with lower operating temperatures which promotes cost savings, better reliability and lower system level thermal resistances.

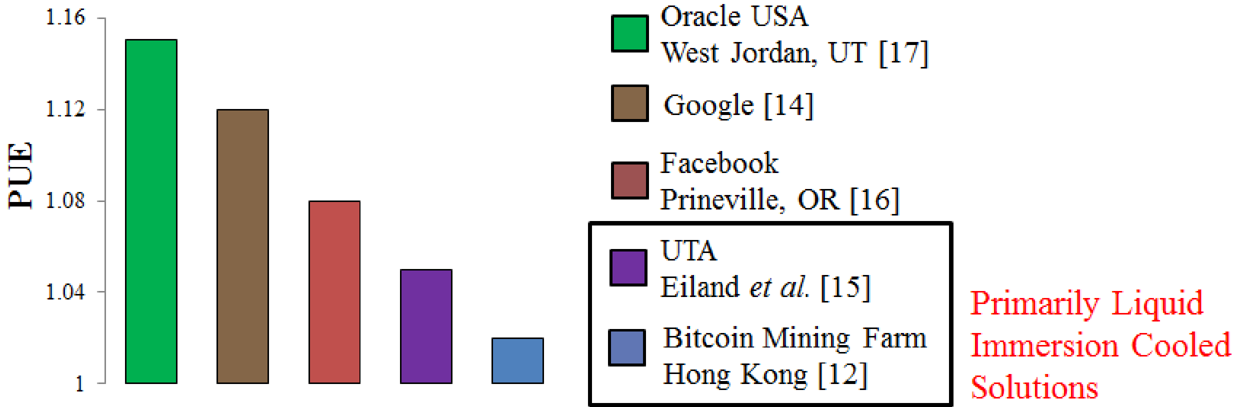


Figure 10 – Case Study PUE Benchmarks

The main factor driving higher operating temperatures is the consumer demand that electronics be constructed in more tightly packaged systems. The classic argument for this

$$q = h * A * (T_s - T_\infty) \tag{1}$$

$$q'' = h * \Delta T \tag{2}$$

relationship uses the terms found in Newton's law of cooling with all terms shown in Equation 1 or with some terms compressed in Equation 2. While there is debate as to whether the failure rate of a processor truly doubles with every 10°C increase in operating temperature, it is generally accepted that increased operating temperatures do have some deleterious effect on system reliability [20] [21]. Therefore, the aim of the thermal engineer is to keep this value as low as possible to keep reliability as high as possible. The amount of heat transfer is directly proportional to the amount of processing taking place within the device, so limiting this to reduce the surface temperature would not be advantageous from a performance perspective. Decreasing the ambient temperature would require additional air conditioning costs so oftentimes reducing this term is not feasible. Increasing the area would reduce the surface temperatures but goes against consumer expectations for smaller systems. The most direct way to increase reliability of the system is to increase the heat transfer coefficient. Oftentimes, the thermal engineer is faced with the problem of a varying heat flux so the same argument with the reference of Equation 2 is

presented. With the desire to have increased processing, or increased heat transfer, with a smaller footprint, or less area, the heat flux must increase. From Equation 2, in order to increase the reliability in a fixed ambient temperature environment, the driving temperature difference, ΔT, must decrease. To accommodate this desired decrease in temperature with the expected rise in heat flux, again the heat transfer coefficient must go up. Unfortunately for the thermal design engineer, heat fluxes for high performance electronics are projected to rise significantly in the coming years. Heat fluxes as high as 250 W/cm^2 [22] are projected in the near term while those near 1000 W/cm^2 are expected within the next decade [23]. Fortunately however, two-phase heat transfer offers several orders of magnitude increases in heat transfer coefficients over more traditional forced convection air cooling methods as illustrated by Figure 11 [24]. Industrial examples have already shown significant increases in efficiency using liquid immersion cooling techniques and the increases in heat transfer coefficients when two-phase heat transfer is added provides a two-pronged attack at cutting operating costs. Even more cost savings can be realized in the construction of a liquid cooled data center as piping and plumbing installation is much easier and cost effective than routing large air ducts. Installation of a traditional air cooled thermal management system can account for as much as 43% of initial construction cost [25].

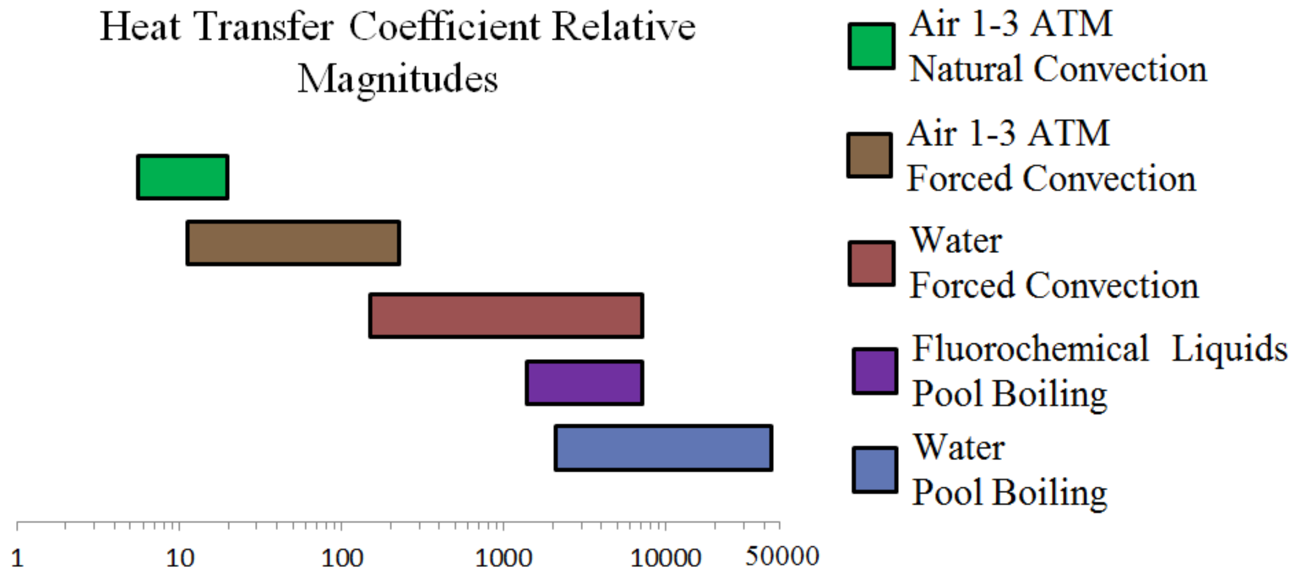


Figure 11 – Cooling method heat transfer coefficient comparison chart [24]

With the current trend of high performance processing equipment attaining heat fluxes that will undoubtedly overwhelm traditional air cooling methods, a fundamental understanding of liquid cooling with these systems is critical for the future as the industry will continue its matriculation to the consistent application of this thermal management solution. The experimentation and analysis conducted within this study will help to answer the questions sure to arise as this solution gains a stronger foothold in the industry.

Chapter 2: Literature Review

There have been a number of fundamental and application oriented studies conducted within the thermal science and fluid mechanics community over the last several decades regarding the use of two-phase heat transfer, liquid immersion cooling, and flow visualizations using Particle Image Velocimetry (PIV) techniques that are of particular pertinence to the current study. This chapter seeks to provide some historical perspective on why the problems currently facing thermal and packaging engineers of high performance electronics are present along with highlighting a number of examples in the literature that have influenced the motivations behind the current study.

2.1 Genesis of Liquid Cooling in the Data Center

The advancements in microelectronic fabrication techniques over the last several decades brought about the necessity for integration of more effective thermal management solutions in high performance computing equipment. The spacing between transistors on an Integrated Circuit (IC) is critical as interconnect length is a main driver of processing speeds. Conventional IC construction involves a number of photolithographic steps that build transistor networks on silicon wafers. The rule of thumb is that economically feasible and commercially producible transistor spacings are limited to the wavelength of the light used for photolithography. The seemingly prescient Dr. Gordon E. Moore stated that the number of transistors on a chip would double every 10 years [26], essentially predicting the advancements of microelectronics fabrication. Until recently this statement had been proven consistently correct and remarkably

accurate. Current limitations with microelectronics fabrication techniques have led to the slowing of transistor density growth resulting in a slight deviation from Moore's Law [27]. The current feature length for state of the art commercially available chips is 14 nm with plans to have 10 nm systems available by 2017 [28], representing a giant leap back on the track set forth by Moore's Law. The consequence for the thermal engineer with the decrease in feature size and increase in transistor density is the amount of power generated in a given area will increase with the predictions of Moore's Law. Given that Dr. Moore himself has recently claimed that adherence to his law will continue for at least another ten years [29], thermal engineers will continue to face growing challenges as heat fluxes for high performance computing equipment will begin to overwhelm conventional cooling techniques.

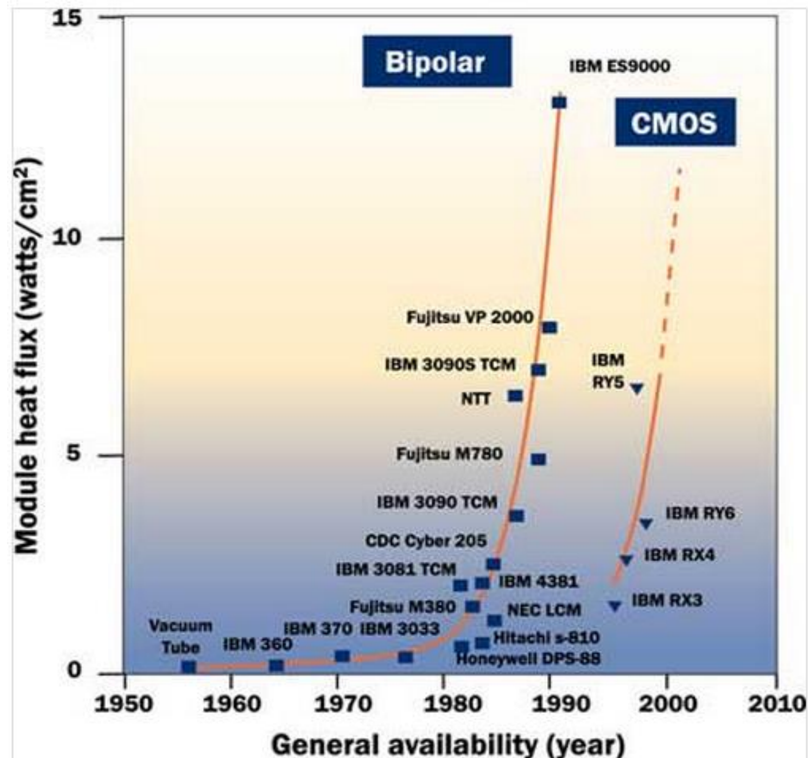


Figure 12 – High performance electronics heat flux rise timeline [30]

The necessity for implementation of liquid cooling in the data center to face these thermal challenges has happened before. Prior to the implementation of the more efficient Complementary Metal Oxide Semiconductor (CMOS) transistor in the early 1990's, bipolar

transistors were the primary switching elements used in IC fabrication. The rise of the heat flux associated with the use of bipolar transistors along with the dramatic reduction realized when the switch to CMOS took place is illustrated in Figure 12 [30]. A number of computing systems that represented significant leaps forward in performance are highlighted on Figure 12 as well. One of the first attempts at bringing liquid into the data center was made with the introduction of the Thermal Conduction Module (TCM) integrated onto the IBM® 3081 computing system in 1982 [31]. A schematic of this device is presented as Figure 13 showing a cutaway view on the left

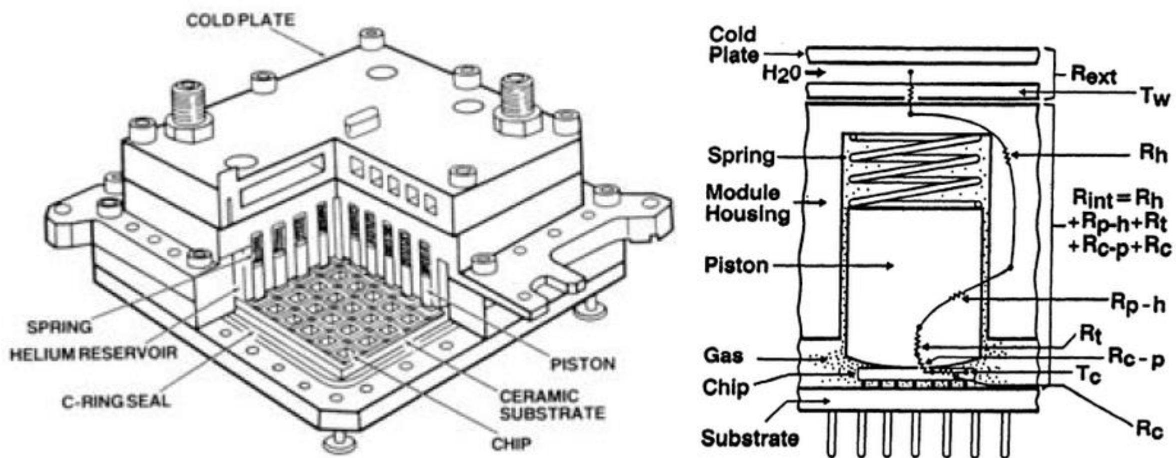


Figure 13 – IBM TCM details [32] [33]

[32] and a zoomed in detail of the pistons [33] used to maintain more direct thermal contact with processing elements. One of the motivations behind the design of this module is to reduce the thermal resistance experienced by the heat flow emanating from the transistor junction to the cooling medium. Thermal Interface Materials (TIMs) are a critical point of increased resistance to heat flow out of the chip into the ambient along with a potentially detrimental junction for increased thermal stresses due to Coefficient of Thermal Expansion (CTE) mismatches between the materials in the chip to heat sink stack-up. When a heat sink is attached to a processor chip with a conventional grease TIM, heat flows primarily through the channels where the heat sink

and the chip are connected by the adhesive. These channels are generated by the peaks and valleys formed during the curing process of the grease. While these connections offer conduction paths, the gaps are filled with comparatively insulative gas gaps which add to the thermal resistance substantially. These peaks and valleys are illustrated by Figure 14 [34]. When the amount of thermal expansion of a TIM differs from that of the expansion experienced by the silicon of an IC, stress and strain is imposed on the processing element resulting in the potential for failure or decreased reliability. The use of springs in IBM's TCM is an attempt to alleviate the stresses induced by CTE mismatch as well as provide a superior heat flow path via conduction through the metallic springs as well as through the surrounding helium gas encapsulated by the module. Low pressure helium sealed within the module has a higher thermal conductivity than the atmospheric air captured in a traditional grease TIM. The combination of these two heat flow path enhancements provide improved heat extraction to the chilled water flowing in the cold plate that sits on top of the module. As an example, a 1 in^2 IC that has a heat sink attached to it with a typical thermal grease can experience a resistance of up to 6.5 K/W at the adhesive interface alone [34]. With a high end thermal grease this value can be reduced to 1.3 K/W [34] but it should be noted that this is not the overall chip to ambient thermal resistance as it does not take into account the junction to case thermal resistance experienced in the encapsulating material surrounding the chip, that experienced via conduction through the heat sink, or that experienced

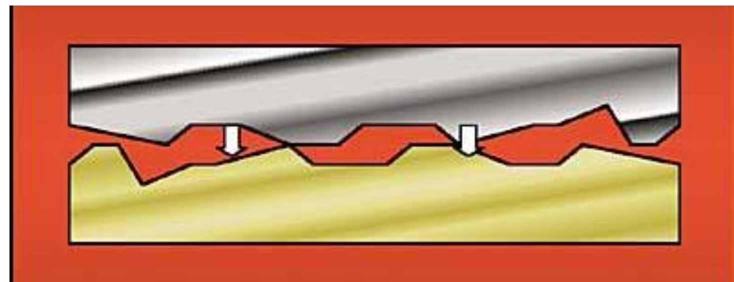


Figure 14 – Air gap contact resistance with traditional TIM's [34]

during the convective removal of heat away from the heat sink surface. IBM's TCM boasts an overall chip to ambient thermal resistance of 4 K/W [35] with a 90 x 90 array of smaller processing elements resulting in an overall heat generation of 300 W [31]. While the omission of the thermal resistance experienced by a traditional grease may have been removed and the piston design of the TCM yielded optimal pressure and thermal contact to the processing elements embedded within, this value is an order of magnitude higher than the chip to ambient thermal resistances yielded by the current study. By immersing the electronic component within the cooling medium itself, not only are the manufacturing complexities associated with attaching heat sinks, TIMs, cold plates, heat spreaders, etc. to processing elements taken away, but the chip to ambient thermal resistance is also reduced drastically by ejecting the heat directly into the coolant. While the TCM was significant for its time, immersion cooling techniques remove the thermal resistances introduced with intricate cold plate style designs or traditional heat sink attachment approaches. Less thermal resistance results in lower operating temperatures for equivalent processing power, increasing the reliability of the system as well. The point at which the TCM was introduced in the heat flux rise timeline shown in Figure 12 is interesting in that it came at a time when heat fluxes from high performance computing equipment was at roughly 2.5 W/cm^2. Liquid had to be introduced into the data center to effectively manage this heat flux and is also the point at which two-phase heat transfer is initiated for the dielectric fluids used within the current study. This highlights the natural progression, and possible inevitability, towards introducing liquid into the data center as systems become increasingly more compact and power dense.

Another historical system that emphasizes the important and growing role of two-phase liquid immersion cooling techniques in the industry is the Cray-2 liquid supercomputer [36]. A schematic from the patent filed in 1982 is provided as Figure 15. The patent touches on another issue that two-phase liquid immersion cooling is suited to handle, namely the rise in volumetric heat dissipations. For example, it is possible to achieve significantly high base heat transfer coefficients within optimally spaced vertically oriented plate fins on a heat sink, nearly 190 W/m^2K as shown by Bar-Cohen *et al* [37]. However, this heat transfer coefficient would be attained for fins that are 675 mm (2.2 feet) tall, prohibitive for most electronics cooling

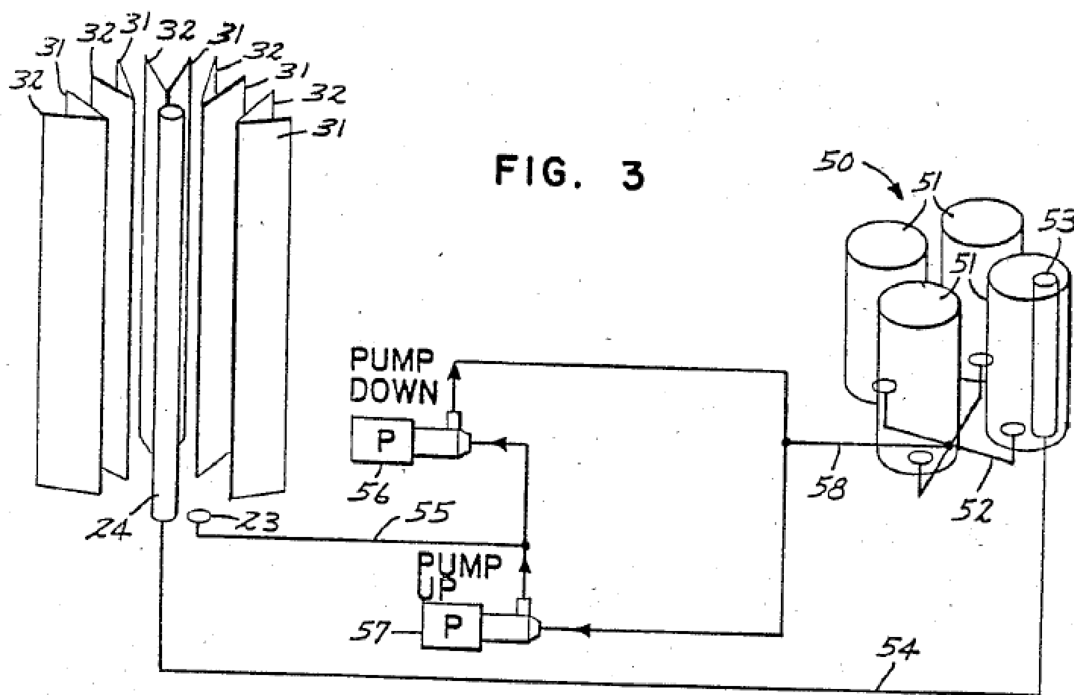


Figure 15 – Schematic of Cray-2 supercomputer cooling system [36]

The radial array of processing boards shown on the left accept the dielectric fluid coolant delivered via the pumps shown in the middle which has been subcooled by the reservoirs shown on the right. These reservoirs also act as the point at which heat is extracted from the system to ambient.

applications. During this time, high performance processing packages could be as small as 4 in x 8 in x 1 in (102 mm x 204 mm x 25.4 mm) dissipating 600 W of heat [36]. An example of the form factor and layout of such a board is provided as Figure 16. From a heat flux perspective this translates to a value of 2.93 W/cm^2, again in the proximity of the value that drove the design behind the previously mentioned TCM. Current high performance processors are above this heat flux with Intel's top of the line processor producing a value of 6.92 W/cm^2 from a reported Thermal Design Power (TDP) of 155 W [38]. Given that heat flux history is repeating itself as suggested by Figure 12 this provides further evidence that liquid cooling must find its way into the data center in some capacity moving forward. The 600 W board level power dissipation translates to a volumetric heat dissipation of 1.13 W/cm^3 for the motherboard only. This value exceeds even current state of the art air cooling capabilities as the top of the line HP Proliant Gen8 server has a volumetric power density of 0.051 W/cm^3 [39]. The design reported that incoming fluid temperatures were 70°F (21°C) while the outgoing temperature was 90°F (32°C) which kept the maximum temperature of any chip within the system at 130°F (54°C) at a flow rate translating to 1 in/sec across the circuit board [36]. The Cray-2 approach also includes many boards in a single bath of fluid, adding complexity to the maintainability of the system should only one of the boards within the array of modules fail. The LRU approach proposed by the current study allows for the potential of hot-swapping modules in case of single failure. Even with the maintainability issues, this

Figure 16 – Sample 1986 high performance processing motherboard

approach and technology was far-reaching for its time. It came at a moment in the evolution of high performance electronics when more aggressive thermal management solutions were necessary, not unlike the current situation in this field.

2.2 Boiling Heat Transfer Performance Historical Studies

The fundamental phenomena governing the two-phase heat transfer that allows the power densities of high performance electronics to be reliably maintained at a suitable operating temperature have been studied in depth. The classic work that begins to characterize the various regimes within pool boiling was conducted by Nukiyama [40]. By supplying current to nichrome, nickel, platinum, iron and fuse wires of known resistance, constant heat flux experiments were conducted to gather portions of the traditional boiling curve shown in Figure 17. For an immersion cooling system of high performance computing equipment, the first regime, leading up to point A on Figure 17, where natural convection dominates is typically of little consequence as heat fluxes of these systems are large enough to initiate boiling with many of the low saturation temperature dielectric liquids used as working fluids in these applications. The benefits of immersion cooling for lower power elements on a computing board can be realized beyond what air cooling can offer. For example, assuming a moderate heat flux of 1 W/cm^2 and using

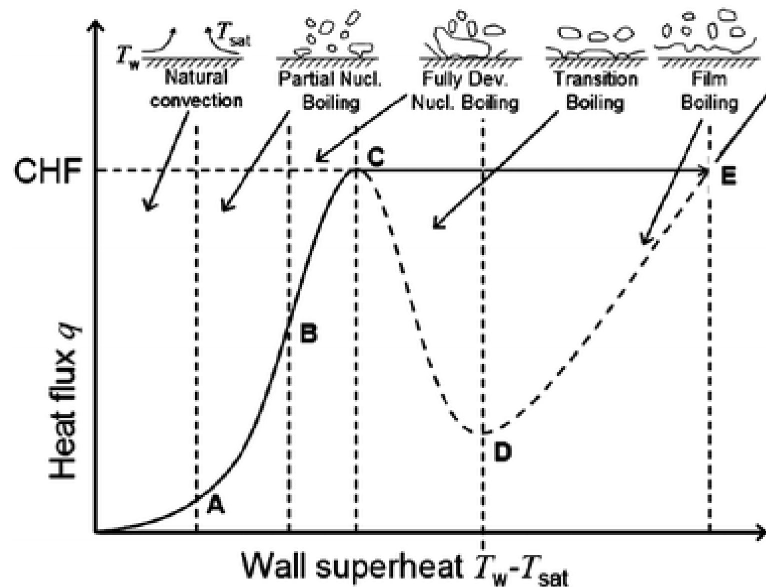


Figure 17 – Pool boiling curve trends and regimes [40]

$$\overline{Nu}_L = \left\{0.825 + \frac{0.387 * {Ra_L}^{1/6}}{\left[1 + \left(\frac{0.492}{Pr}\right)^{9/16}\right]^{8/27}}\right\}^2 \quad (3)$$

the work of Churchill and Chu [41] for free convection on a vertical plate shown as Equation 3, the 1 in^2 element used in the current study is predicted to have a surface temperature of 56°C with an average heat transfer coefficient of 323 W/m^{2}K with Novec 649 as the working fluid at an ambient temperature of 25°C. Although boiling would have developed at some sites on the surface at this temperature given that the atmospheric saturation temperature for Novec 649 is 49°C, this heat transfer coefficient and surface temperature match well with the experimental results yielded through pool boiling from a bare silicon surface. The same conditions with air as the cooling medium yield an average heat transfer coefficient of 13.7 W/m^{2}K with a surface temperature of 753°C. The latter value shows why heat spreaders, sinks and other extended surfaces are necessary to cool computing equipment in traditional air cooled systems.

The area of most interest to the current study is the fully developed nucleate boiling regime, the area between points B and C on Figure 17. The behavior in this regime can be predicted by the well-known Rohsenow semi-empirical correlation [54] shown as Equation 4. For the purposes of the dielectric fluids used in the current study the values of the constants s and r are 0.33 and 1.7 respectively in Equation 4. Interestingly, the seemingly complex equation stems from the assumption that there exists a bubble Nusselt number,Nu_b, that takes the fundamental form of a convective relation, namely $Nu_b = A * Re_b^m * Pr_l^n$. With the appropriate selection of a bubble Reynolds number and a bubble length scale, the fluid properties take the

$$\frac{q"}{\mu_l * h_{lv}} * \left[\frac{\sigma}{g * (\rho_l - \rho_v)}\right]^{\frac{1}{2}} = \left(\frac{1}{C_{sf}}\right)^{\frac{1}{r}} * {Pr_l}^{-\left(\frac{s}{r}\right)} * \left[\frac{C_{pl} * [T_w - T_{sat}(P_l)]}{h_{lv}}\right]^{\frac{1}{r}} \quad (4)$$

form of those shown in Equation 4. The empirical portion comes into play with the selection of the r,s and C_{sf} values. With an adequately determined C_{sf} values, accepted error with this correlation can be in the range of ± 40%.

The point at which the temperature jumps significantly as heat flux is increased, from the point C to point E on Figure 17, is generally referred to as the Critical Heat Flux (CHF). In a typical electronics system, this results in a catastrophic failure of the system as conventional attachment materials cannot withstand the orders of magnitude temperature increase that coincides with this event. Using the work of Lubin [42] to get the convective heat transfer coefficient in the post-CHF film boiling regime shown as Equation 5, the heat transfer coefficient contribution from radiation shown by Equation 6, the simplification of their contributions to the total heat transfer coefficients proposed by Bromley [43] shown as Equation 7, and Newton's Law of Cooling Equation shown previously as Equation 1, the maximum temperature of the heated element used in the current study at the beginning of film boiling,

$$h_{conv} = \left[\frac{k_v * g * \rho_v * (\rho_l - \rho_v) * h_{lv}}{4 * \mu_v * (T_w - T_{sat}) * L_{heater}}\right]^{1/4} \quad (5)$$

$$h_{rad} = \frac{\sigma_{SB} * \left({T_w}^2 + {T_{sat}}^2\right) * (T_w + T_{sat})}{\frac{1}{\varepsilon_i} + \frac{1}{\varepsilon_w} - 1} \quad (6)$$

$$h = h_{conv} + \left(\frac{3}{4}\right) * h_{rad} \quad (7)$$

marked as point E on Figure 17, was found to be 338°C. Conventional electronic equipment attach materials such as solder and indium have melting points of 183°C and 157°C respectively, both sufficiently below the temperature experienced by the heated surface after the CHF event. Given that this event should be avoided in most practical situations, extensive studies have been conducted to quantify the point at which it is reached along with ways in which to predict its

occurrence. Kutateladze [44] and Zuber [45] both independently came to the same equation for predicting CHF, shown as Equation 8. The governing theory for both of their models is that at some point the velocity of the rising vapor becomes so great that the drag induced on the neighboring quenching fluid column completely blocks the liquid's return to the heated surface. A figure to provide clarity to this phenomenon is provided as Figure 18 [46]. By proposing a cross-hatched pattern of columns as Zuber did, the spacing between them was the Taylor wavelength multiplied by the square root of two. Lienhard and Dhir [47] modified this calculation by adjusting the critical spacing to the Taylor wavelength, as would be the case in a uniform square grid array, leading to an adjustment of the CHF model. The resulting Lienhard and Dhir CHF equation substitutes a 0.149 for the 0.131 coefficient shown in Equation 8.

$$q"_{CHF} = 0.131 * \rho_v * h_{lv} * \left[\frac{g * (\rho_l - \rho_v) * \sigma}{\rho_v^2}\right]^{1/4} \tag{8}$$

The theory behind these correlations is limited to horizontal surfaces. Howard and Mudawar [48] executed a visualization study on vapor lift off from heaters at various angles. They proposed to apply a different model for CHF to three different regions. The regions of interest were an upward facing region (between 0 and 60 degrees), a near vertical region (60 to 165 degrees), and a downward facing region (>165 degrees). In the near vertical region, of interest to the

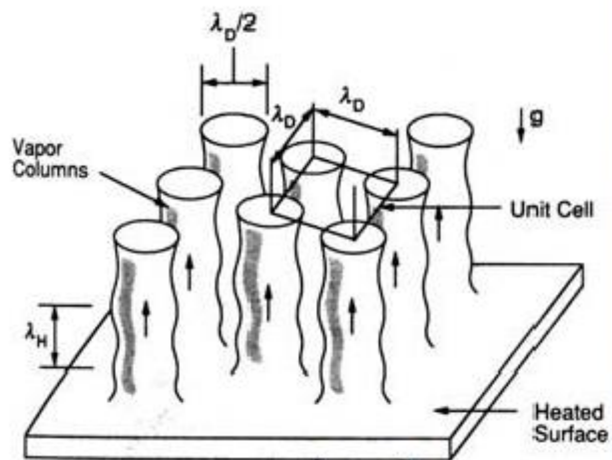


Figure 18 – Liquid/Vapor Column CHF Model [47]

current study as the heated elements are aligned vertically within the module, interfacial wavy vapor layer instabilities with the neighboring liquid region were dominant as the bubbles lifted off from the heated surface. Further refinement of the CHF predictive model was proposed by Arik and Bar-Cohen [49] in the form of the Thermal Management of Electronics (TME) CHF correlation. This lengthy and detailed correlation takes into account the thermal effusivity of the heater material along with its dimensions to account for the spreading of heat to more effectively quenched areas at the heat fluxes leading up to the CHF event. Thermal effusivity, e, is a measure of the material's ability to exchange thermal energy with its surroundings and is defined by the square root of the product of its thermal conductivity and volumetric heat capacity, or $(k \cdot \rho \cdot c_p)^{1/2}$. This heat spreading could allow for the more effectively quenched areas to carry some of the heat load before the catastrophic vapor blanketing event can occur. The heat fluxes leading up to CHF are also characterized by a leveling off of the heat transfer coefficient as experimentally documented by Sridhar [50]

The area of the boiling curve between the points marked C and D on Figure 17 is known as the transition regime and is accessible with temperature varied experiments, such as the quenching of a highly conducting rod or sphere. The nature of this curve is hard to predict given the precision of temperature control required, although a number of researchers have tried. Berenson [51] was the first to discover this region and quantify the heat flux and temperature trends that characterize it. Witte and Lienhard [52] claimed a hysteresis exists in this region due to the mechanisms driving the departure from nucleate boiling, the point marked as C on Figure 17, when temperature is increased versus departure from the minimum heat flux, the point marked as D on Figure 17, when temperature is decreased. They claimed that the phenomenon driving this "jump" between the two sub-regions was the difference in the advancing versus

receding contact angle during these two events. Conversely, Hohl *et al* [53] showed no hysteresis in this region when FC-72 was used, one of the fluids used in the current study. Although the debate still exists as to the influence of contact angle on this region, it is generally of little consequence for the study of immersion cooled electronics as these systems are typically characterized as heat flux controlled, making this region of the boiling curve not accessible.

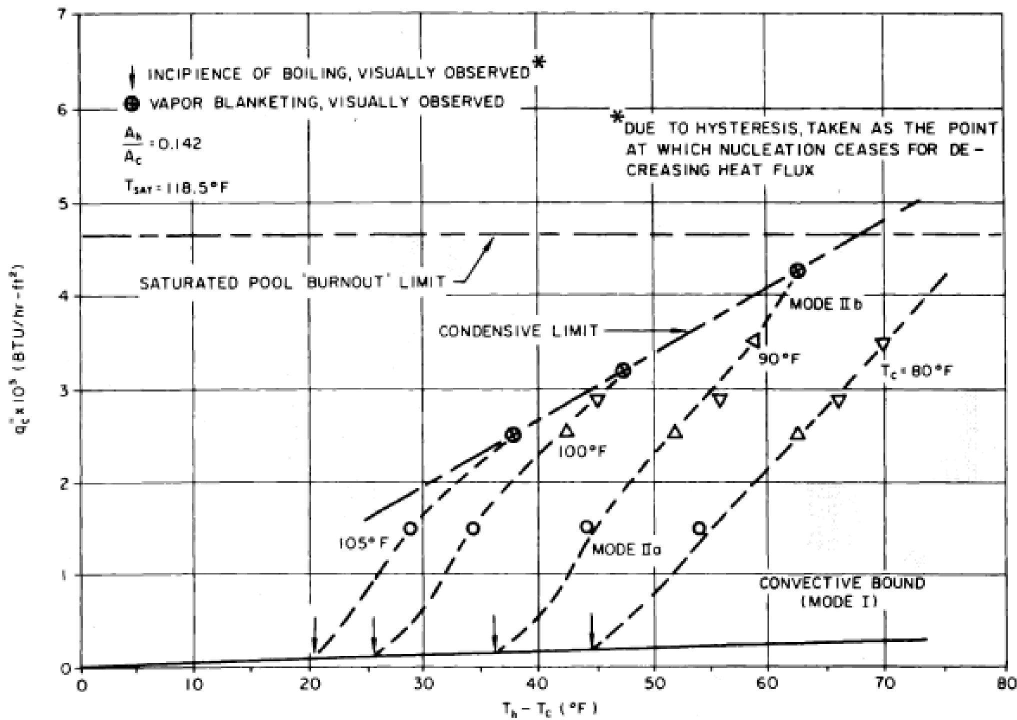


Figure 19 – Condensive limit of Freon-113 trends [55]

2.3 Introduction of Condensation Limitations in Liquid Filled Modules

While the available CHF correlations are useful as an estimate for the potential performance of a two-phase immersion cooled electronics enclosure, there is often another and more limiting factor associated with the extraction of the heat out of the module itself. This is referred to as the condensive limit and was first explored in a Liquid Filled Module (LFM) application by Markowitz [55]. Using a flat horizontal plate for condensation heat transfer

extraction from the module above 0.25” diameter heaters submerged in either water or Freon-113, the limitations of an LFM below the generally accepted CHF value was explored. By plotting the variation in heat flux at the heater versus the driving temperature difference between the heater surface and condensive plate, a clear trend can be seen as to the variation of the burnout heat flux as the condensive plate temperature is varied. This trend is shown by the dashed line in Figure 19 with Freon-113 as the working fluid. As noted in the study of Markowitz, one of the primary factors in the determination of whether an LFM will be condensation limited is the heated area to condensive area ratio, or A_h/A_c. For the data shown in

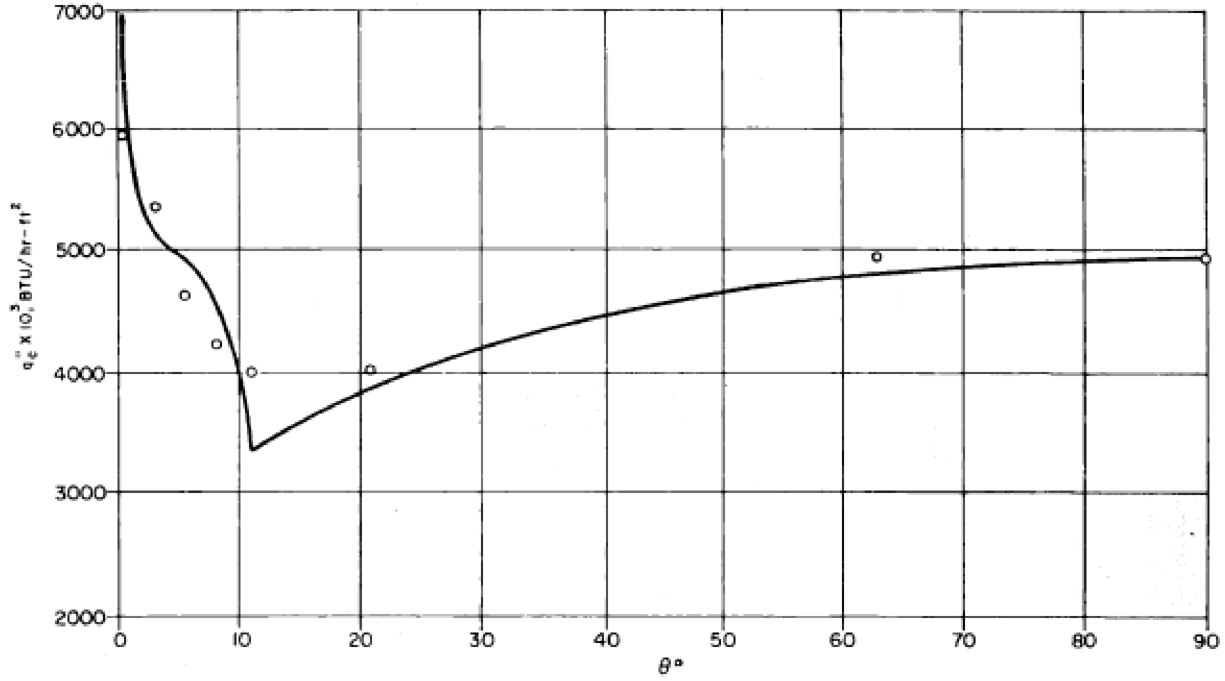


Figure 20 – Trends of LFM angle of inclination on maximum performance [55]

Figure 19, this ratio is 0.142 while for the current study it is 0.078. The latter number is assuming that all of the vertically oriented pin fins and flat area below the chilled water header used for extracting the heat from the module is completely active in the heat transfer process, as would be the case in the horizontally oriented condenser used in the work of Markowitz. The degree of activity and efficiency of the vertically oriented pin fins is an issue addressed in the current study, specifically in an attempt to model this upper limit behavior. The relative activity and contribution of the condenser surface is based on a number of factors. Markowitz showed that by tilting the LFM at various angles, the boiling activity within allowed for the liquid-vapor

$$h_{m,mod} = \frac{k_l}{L_{fin}} * (0.943) * \left(\frac{\rho_l * (\rho_l - \rho_v) * g * h'_{lv} * {L_{fin}}^3}{\mu_l * k_l * (T_{sat} - T_b) * \eta_{fin}}\right)^{1/4} \quad (9)$$

$$h'_{lv} = h_{lv} * (1 + 0.68 * Ja) \quad (10)$$

$$q_{tot,fin} = N * A_{fin} * \eta_{fin} * h_{m,mod} * (T_{sat} - T_b) \quad (11)$$

interface to interact with the condensive film on the condenser wall in addition to immersing a portion of the surface in the coolant thus modifying the overall performance of the system. The effects are competing in that the sloshing can clean the condensate surface allowing for a new film to be generated thus enhancing heat transfer, while immersing a portion of the condenser surface effectively insulates it relative to the condensation heat transfer coefficients experienced on the exposed surfaces. This overall effect is shown in the maximum heat transfer rate achieved at various angles with a 40°F driving temperature difference between the heater and condenser plate with water as the working fluid, shown as Figure 20. Another contributing factor to the performance of the condenser, which is particularly important for the current study, is the fin efficiency of the extended surfaces used there. Iyengar [56] proposed modifying the classic Nusselt [57] laminar film condensation equation for a vertical plate by placing the fin efficiency in the denominator as shown in Equation 9 taking into account the modified latent heat relations proposed by Rohsenow [58] shown as Equation 10. This modified heat transfer coefficient can then be used in the traditional way of calculating heat transfer from a series of fins as shown in Equation 11. The unmodified heat transfer coefficient calculated from the Nusselt laminar film condensation vertical plate equation is used in the determination of the individual fin efficiency. The effect of sloshing and the relative contribution of the vertical fins used as the condenser for the liquid immersion module proposed in the current study will play an important role in modeling the expected behavior of the system.

2.4 Novel Electronics Cooling System Studies

There have been a number of recent achievements and studies with a focus in electronics cooling that have advanced the science, both in terms of power dissipations achieved as well as more reliable operating temperatures manifesting in the form of heat transfer coefficient

improvement. In a similar approach to the current study although in a slightly larger form factor, Campbell *et al* [59] explored the use of chilled water maintained condenser fins to extract the heat from boiling surfaces oriented horizontally and vertically. This study also explored the potential of using a more conductive and immiscible fluid with low boiling point dielectrics such as those used in the current study in the condenser space to enhance heat transfer in this area. A schematic of the proposed solution is shown as Figure 21. This is just one of a number of patents proposed by IBM in this area. Campbell *et al* [60] proposed a LRU rack system where vapor from a collection of modules was captured in a single heat exchanger for condensation and subsequent return back to each individual system under pool boiling conditions. The use of intricate heat sinks at both the heated and condensing surface of a two-phase immersion cooled electronics module was explored by Campbell [61]. While these are primarily pool boiling devices, a system that utilized flow boiling where a Liquid Pumped Cooling (LPC) and Vapor Compression Cooling (VCC) system could be used interchangeably was proposed by Marcinichen *et al* [62]. This study also explored the potential of recovering energy from the cooling loop to be used as power for other devices within the data center. With the already low PUE's possible with the use of two-phase immersion cooling methods as shown in Figure 10, energy recovery methods could bring about

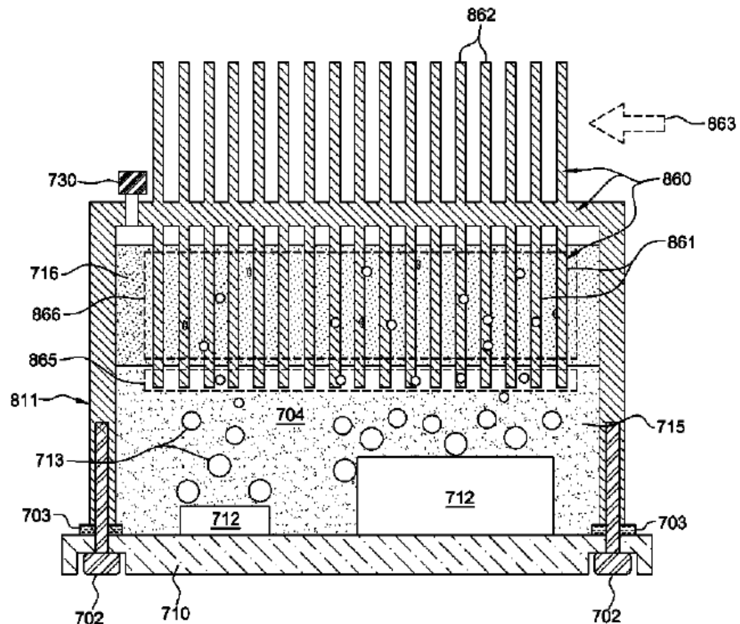


Figure 21 – IBM two-phase immersion cooling module example [59]

the possibility of a PUE less than one. An exergetic analysis of an ionic-liquid based absorption chiller to utilize waste heat generated by processing chips in a data center was conducted by Kim and Gonzalez [63]. The analysis yielded an Exergetic Coefficients of Performance (ECOP) of 1.05 for the best case scenario showing the potential for this technology to capture and utilize cooling energy that would otherwise be wasted. It should be noted that this exergetic analysis represents the ideal energy conversion scenario, so there are other irreversibilities and inefficiencies that would have to be accounted for in a practical installation. The results from the study however indicate the feasibility of such a system, and research such as this will grow ever more important as data center power consumption grows while global energy sources dwindle. Chi *et al* [64] reported energy savings with the integration of Iceotope's solution, similar to the LRU approach proposed in the current study except that fluid is kept in the single phase, over liquid cooled solutions that utilize rear-door liquid-air heat exchangers on the server's racks, a common practice amongst water-cooled cold plate computing solutions. The air/liquid hybrid approach yielded a partial PUE value of 1.48 while that of the direct liquid immersion cooled solution was only 1.14, a 23% reduction in energy savings with the understanding that the partial PUE does not take into account the energy required to exhaust the heat from the server room itself.

2.5 Interface Resistances and Surface Enhancement Possibilities

Thermal performance improvements are available with the use of additional heat extraction infrastructure within the electronics module. Ujerah *et al* [65] explored the use of Carbon Nano-Tubes (CNT's) grown on a bare silicon surface for two-phase heat transfer. In this study, heat fluxes of 11 W/cm^2 with FC-72 as the working fluid were attained with boiling from the bare silicon surface, but the introduction of CNT's increased the maximum heat flux to 15

W/cm^2, a 35% improvement. While there are improvements to be had with the integration of this surface, design considerations for the volatility of boiling damaging the thin and fragile CNTs must be taken into account along with the cost of these materials. Currently, a 1 cm x 1 cm square of Multi-Walled CNT (MWCNT) from Sigma-Aldrich (Part Number: 687804-1EA) costs approximately $1000. Given that the footprint of an Intel Xeon processor is 5.2 cm x 4.5 cm [38], the integration of this surface enhancement for a typical high performance processor may be prohibitively costly. While the potential of using CNTs as a TIM for systems requiring a lower thermal resistance heat sink or spreader attachment method have been explored by Peacock [66], studies directed at overcoming the reliability deteriorating CTE mismatches that exist between TIMs and chip packages using Liquid Metal Alloys (LMAs) have been conducted as well. Roy *et al* [67] have tested various LMAs reporting a specific thermal resistance range of 0.005 cm^{2}K/W to 0.065 cm^{2}K/W. These values when applied to a 1 in^2 (6.45 cm^2) heated surface like that used in the current study translates to a range of thermal resistances of 0.42 to 0.03 K/W. Martin and van Kessel [68] at IBM conducted a study of LMA TIMs where the specific thermal resistance steadily rose from a minimum value of 2 mm^{2}K/W to 7 mm^{2}K/W as the thickness of the material used was varied from 10μm to 200μm. Campbell and Tuma [69] explored the added benefits of using a Boiling Enhancement Coating (BEC) similar to the microporous structure used in the current study. Through numerical analysis and experimental input, they concluded that the use of this surface to initiate two-phase heat transfer in the otherwise single-phase water cooled P575 supercomputer would produce improved thermal management of the high density processing elements contained within. Tuma [70] also showed how this same microporous coating could surpass the performance of several aftermarket heat pipes and thermosyphons. The study reported heat transfer coefficients nearing 90 kW/m^{2}K with

the use of this surface and, with its integration on to the aftermarket products, drove system to fluid specific thermal resistances down to as low as 0.12 cm^2K/W. With this same surface, Moreno *et al* [71] yielded a 50% increase in CHF and 430% increase in heat transfer coefficients over a bare surface using a HFC-245fa refrigerant as the working fluid under pool boiling conditions. Using a patented Aluminum/Devcon Brushable Ceramic/Methyl-Ethyl-Keytone (ABM) coating application technique [72], Rainey and You [73] showed how microfinned structures could have their two-phase heat transfer performance enhanced even further. With a microscale heat sink using 8 mm tall fins, the CHF was taken from 91.7 W/cm^2 to 129.4 W/cm^2 in FC-72 when the structure was coated with the previously mentioned patented method, resulting in a maximum heat transfer coefficient of 17.5 kW/m^2K based on the entire heat sink surface area. The effects of adding more nucleation sites to microfins by placing mesh and porous plate structures on top of them was explored by Pastuszko and Strak [74]. It was found best to not place structures on top of the fins for fluids with low surface tension, like FC-72 and Novec 649. For this design scenario maximum heat transfer coefficients of 8 kW/m^2K and 3.5 kW/m^2K were reported for FC-72 and Novec 649 respectively, near the values yielded in the current study for similar microfinned structures. Diamond particle coated chips were used in the work of Arik *et al* [75] to explore the effects of significant subcooling and pressure variations on microporous surfaces. Heat fluxes between 19.4 W/cm^2 and 47 W/cm^2 were yielded for minimal subcooling under atmospheric conditions and 71K subcooling under 3 atm of pressure respectively. The average CHF enhancement factor over the bare surface condition achieved across all subcooling and pressure conditions tested was 1.6, illustrating again the improvement potential possible when microstructures are integrated. The effect of surface enhancement geometry, specifically thickness and porosity, were studied by El-Genk and Ali [76]. They used

an electrochemical process for creating microscale copper dendrites. As these structures are initially very fragile, a second step was added to provide strengthening of the surface. This second step resulted in rounded cavities which reduced porosity and increased the wetted surface area resulting in the recording of very high CHF's and nucleate boiling heat transfer coefficients, on the order of 27 W/cm^2 and 135 kW/m^{2}K respectively at superheats as low as 2K. In a study of pool boiling with porous graphite structures as the surface enhancement and FC-72 as the working fluid, El-Genk [77] achieved a maximum nucleate boiling heat transfer coefficient of 34 kW/m^{2}K and a CHF of 30 W/cm^2. Incredibly intricate and unique structures can be inspired by regularly occurring structures in nature. Using a nickel plating process on the Tobacco Mosaic Virus (TMV), the surface structure shown in Figure 22 can be grown on bare and microstructured surfaces yielding significant CHF and heat transfer coefficients. Pool boiling heat transfer performance for this surface enhancement was explored by Rahman and McCarthy [78]. Values reported in the study were as high as 247 W/cm^2 for CHF and 74 kW/m^{2}K, much higher than those in the current study as the current work uses much simpler surface enhancements.

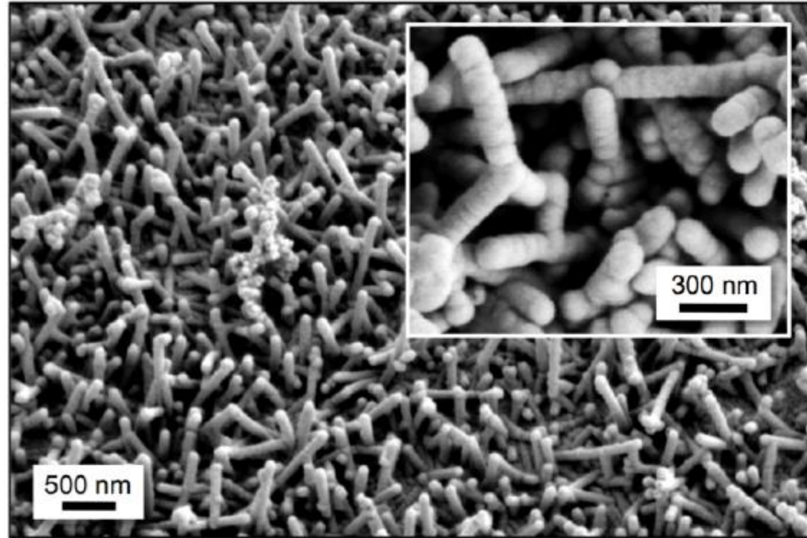


Figure 22- Nature inspired boiling enhancement surface [78]

2.6 Embedded Thermal Management Solutions

While the current study and similar liquid-immersion cooling research offer the ability to effectively manage current and near-term high performance computing elements, trends indicate that coolant must be delivered closer to the junction through embedded thermal management solutions as IC's will need to be constructed in the 2.5D and 3D in order to continue the expectation and consumer demand for higher power density in the face of photolithographic restrictions to present microelectronic fabrication techniques. In order to overcome the limitations of manufacturing IC's in the 2D, transistors can be staggered on multiple levels within the same silicon substrate as shown in the simplified schematic of Figure 23. Here the photolithographic feature size limit pertains to each layer of transistors thus allowing for more processing elements to be placed in a particular area. This allows for the increase in transistor density and computational power within the capabilities of current manufacturing processes. While the cooling solution is not necessarily embedded within the chip for 2.5D structures, the resulting increase in computational power, and consequently heat flux, will have to be managed

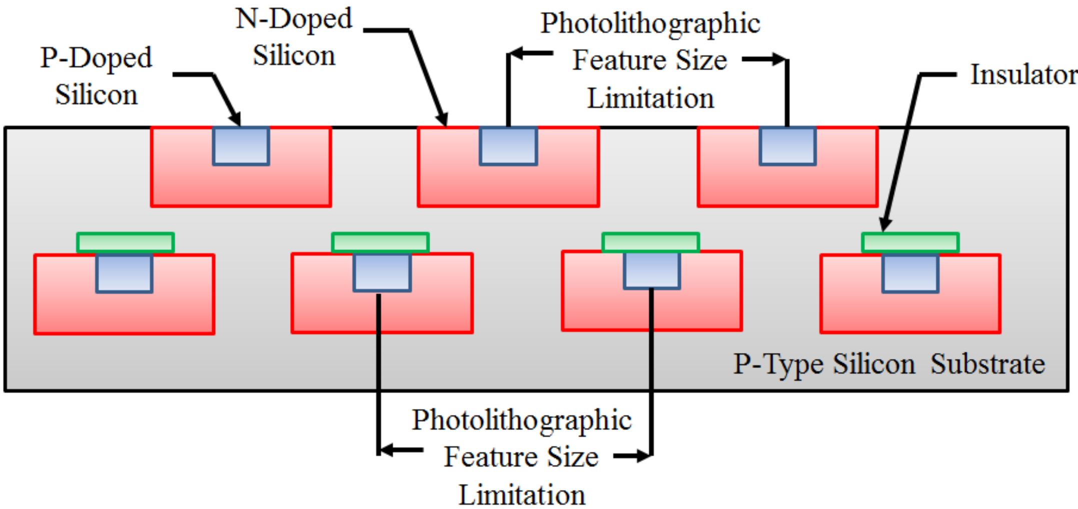


Figure 23 – Simplified 2.5D IC schematic

by more aggressive thermal management methods with heat transfer coefficients capable of maintaining surface temperatures within acceptable levels. This is especially important for this scenario as transistors deeper within the 2.5D structure will experience hotter temperatures given their extended distance away from the cooling surface. By constructing Multi-Chip Modules (MCM's) with stacks of IC's on top of one another, 3D architectures are formed which, while complex both from a manufacture and thermal management standpoint, offer incredibly high volumetric power density possibilities. A simplified schematic of such a 3D IC structure is presented as Figure 24 [79]. One of the ways to deliver the coolant within the MCM structure is with the use of microchannels. Numerical simulations conducted by Madhour *et al* [80] showed that for a four chip stack array using R236fa as the working fluid flowing through embedded microchannels that a volumetric power dissipation of 272 W/cm^3 at a pressure drop of 0.5 bar (50 kPa). Using water as the working fluid, Alfieri *et al* [81] conducted an experimental study on an MCM and reported a potential volumetric power density of 1.3 kW/cm^3. As is often the case, significant heat transfer gains come at the cost of pressure drop in accordance with the classic Reynolds analogy. The pin fin design embedded within the 3D structure incurred a pressure drop of 110 kPa. Fundamental work on microchannels themselves has also been conducted. Heat fluxes of 60 W/cm^2, much higher than those reported in the current study, have been reported by Chen and Garimella [82] by flowing FC-77 through microchannels machined into the silicon substrate. Thiagarajan [83] conducted an experimental study that used a microchannel heat sink consisting of 19 channels each measuring 200 μm in width and 346 μm in depth machined into silicon with FC-72 as the working fluid at a mass flux of 2138 kg/m^{2}sec. A heat flux of 38 W/cm^2 was recorded with a heat transfer coefficient of 5 kW/m^{2}K while incurring a pressure drop of 9.5 kPa across the module. Surface enhancements and structures

can also be applied to microchannels to increase their effectiveness. By placing cavities on the side walls of microchannels, Kuo and Peles [84] reported increases in heat transfer coefficients over bare walls, achieving a maximum heat transfer coefficient of 70 kW/m^2K. Instead of the copper spheres used in the microporous coating for the current study, aluminum spheres were sputtered to microchannel surfaces by Yang and Liu [85] greatly increasing heat transfer performance over plain channel surfaces. By modeling the chips within an MCM as isothermal plates with open spacing between them completely immersed within FC-72, optimal power dissipations for various dimensional design constraints were calculated using available two-phase heat transfer theory by Geisler [86]. For a plate length of 10 mm, die thickness of 0.4 mm and a spacing of 0.2 mm, a maximum volumetric power dissipation of over 500 W/cm^3 was calculated. The potential volumetric power dissipation here is significant given that it is passively cooled, eliminating the need for the pumping power needed to direct coolant into the 3D IC stack.

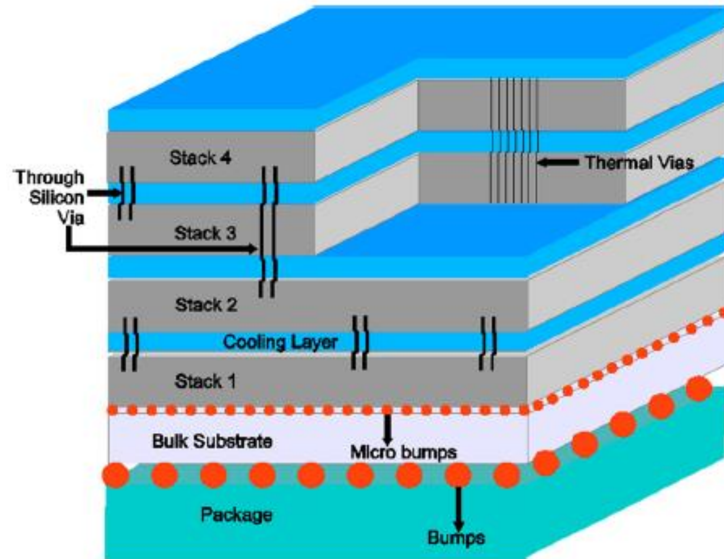


Figure 24 – Simplified schematic of 3D IC structure [79]

2.7 Coolant Flow Modeling and Visualization Techniques

As liquid immersion cooling technology gains a stronger foothold in the industry, fundamental problems regarding flow dynamics within the electronics module are sure to arise. The development of flow visualization and measurement techniques are vital in order to promote acceptance and confidence in this type of thermal management solution moving forward. The need for this experimental assurance extends to the dominant solution for today's data center, namely air cooling. Air flow management studies have been conducted on several design tiers within the data center. Numerical modeling and flow simulations have been conducted on data center systems from the room level by Alkharabsheh *et al* [87], to the rack by Arghode *et al* [88], and down to the chassis itself by Alkharabsheh *et al* [89]. PIV measurements of air flow in a data center system have been conducted by Arghode and Joshi [90]. A sample streamline map is provided as Figure 25. Local air velocity measurements, as high as 7.42 m/sec, are shown on Figure 25 along the centerline between the right end of the cold aisle and the entrance to the server rack. A number of recent studies have been conducted to extend the capabilities of predicting air flow within electronics equipment to predicting coolant distribution and heat transfer performance within liquid filled enclosures under passively and actively cooled conditions. Using rack CFD analysis, Almoli *et al* [91] showed the reduction in heat load on the Computer

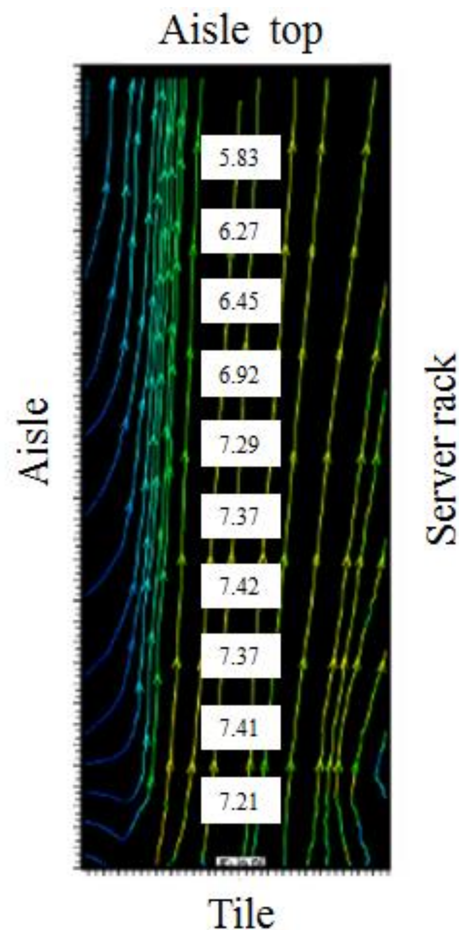


Figure 25 – PIV measurements of air flow in a data center [90]

Room Air Conditioning (CRAC) unit possible with the integration of liquid-air heat exchangers on the sealed server racks. This mandates that a liquid based thermal management solution be used within the server rack but opens up the possibility of using nearby cold climate water reservoirs for free cooling during high load cycles. Nguyen *et al* [92] conducted a numerical analysis where various pool boiling models were utilized and compared to experimental data. This study showed that with very little experimental input, these models could be used to predict thermal performance for a number of design parameters. A numerical investigation using Ansys© software was conducted by Fincher [93] which explored models to predict flow boiling performance and coolant distribution patterns within the liquid cooled immersion module proposed in the current study. The results yielded by this investigation provided design insight into potential flow distribution methods for directing the coolant more effectively over the primary die within the enclosure.

From the flow visualization standpoint, PIV techniques can offer much needed insight into coolant flow within a liquid immersion cooled electronics module. With this information,

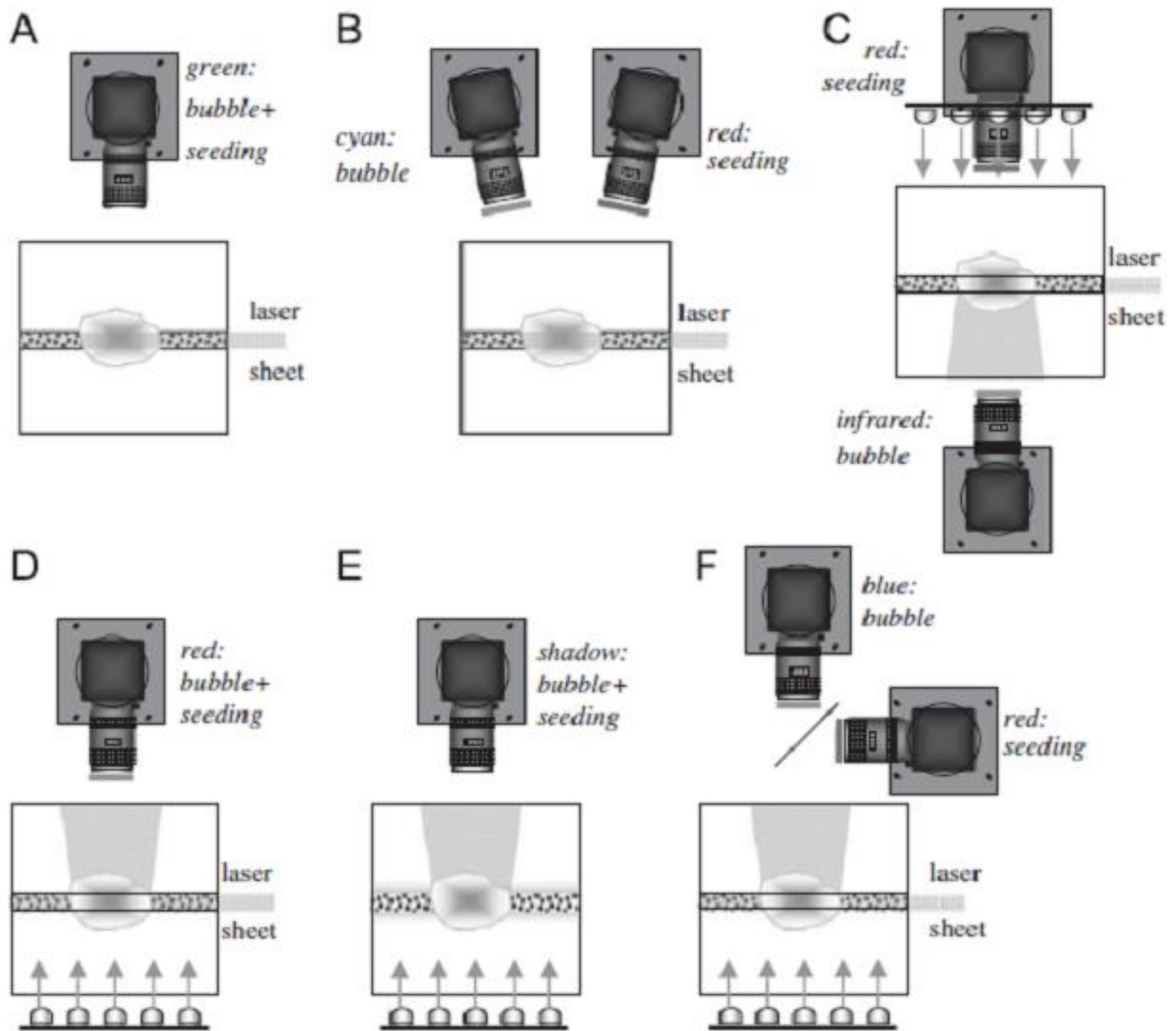


Figure 26 – Two-phase PIV techniques summary [94]

packaging engineers can more effectively place elements on a circuit board so as to assist, or in other cases not inhibit, flow within the device. A number of experimental techniques exist for capturing two-phase flow dynamics and an excellent summary of them is offered by Sathe *et al*

[94]. The primary and very informative diagram highlighting these techniques is presented as Figure 26. These techniques center around a number of options including number of cameras, use of shadowgraphy, fluorescence filter use and particle/fluid compatibility. For the experimental setup used in the current study, the use of shadowgraphy and fluorescence filters are of particular interest. Flashing a light in the background of a bubble projects an image of darkness onto the camera in relation to the surrounding illuminated fluid, the fundamental concept behind using shadowgraphy. Seeded fluorescent particles illuminated by a laser fired in conjunction with this background light allow for both phases to be captured in one image as was done by Lindken and Merzkirch [95] and illustrated by the picture shown in Figure 27. This technique is highlighted as Image D within Figure 26. Some illuminated particles will appear in the relatively darker space as rogue particles in front of or behind the vapor. Information from the shadowgraphy identifying these vapor pockets is used to filter out these particles from the vector analysis. With fluorescence removed, both the light collected from the particles and the bubbles emanating from the background shadowgraphy source can be captured by the camera simultaneously, again capturing both phases in one image as done by Bröder and Sommerfeld [96]. This technique is highlighted as Image E within Figure 26. For this to be effective however, edge detection of the bubble and the particle has to be accurate as the specifications for the nominal diameter of the particles are used as the criteria to determine

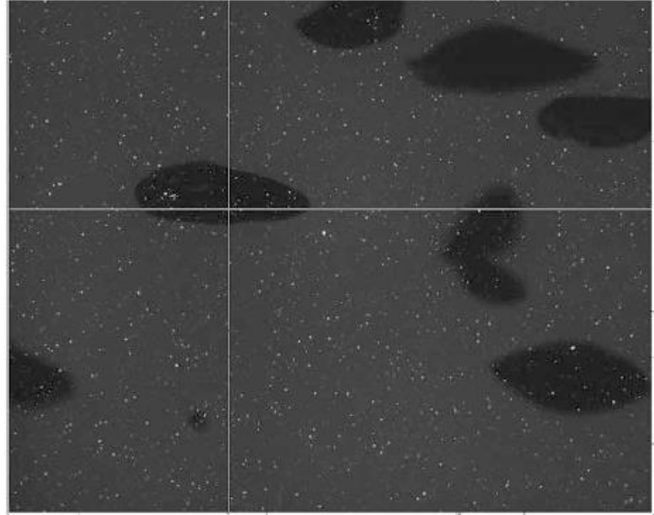


Figure 27 – Two-phase PIV shadowgraphy and fluorescence technique [95]

whether light is coming from a bubble or a particle. Once this distinction is made, the bubble area is filtered out for the vector analysis of the liquid phase. Unfortunately, given the geometric constraints of the current experimental setup, a conventional shadowgraphy technique was not possible. However, as will be shown, an understanding of where the vapor is at the condensing surface is critical to predicting performance of two-phase liquid immersion cooled modules. Therefore, it is expected that some sort of red-dye fluorescence imaging or a technique to distinguish the liquid-vapor interface with the PIV analysis will have to be added. One of the ways that this could be done is be able to accurately predict where the vapor is going to be at any given time. By boiling from structured surfaces as Teodori *et al* [97] did in their analysis of HFE-7100 boiling from a structured surface where bubbles were known to be on the order of 500-800 microns in diameter. As boiling from a bare silicon chip to reduce manufacturing costs is an aim of this study where nucleation site location can vary slightly from chip to chip, this approach is not feasible.

Chapter 3: Experimental Facility

The following sections outline the experimental facility used to conduct the current study. The design motivations and details of the electronics enclosure assembly which houses the heated elements meant to simulate high performance computing devices are discussed. Specific attention was paid to designing the cooling delivery system in such a way as to mimic an actual installation to the greatest degree possible, adding confidence in the reported results that the temperatures, heat transfer coefficients, and coolant flow rates used are representative of any future utilization of the current study's findings. Details as to the implementation of data acquisition within the flow loop and electronics enclosed within the module are discussed. In order to improve the two-phase thermal performance of these elements, surface enhancements were added. The fundamental improvements yielded by these surfaces along with their construction and attachment method are illustrated.

3.1 Electronics Cartridge Assembly Design Motivations and Construction

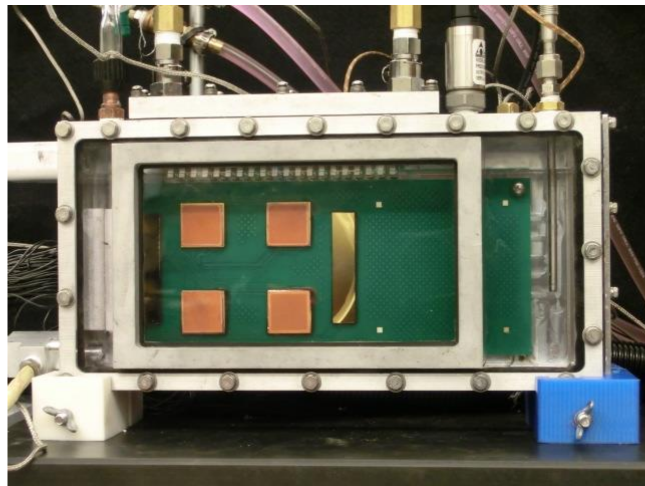


Figure 28 – Electronics Cartridge Assembly

The primary component within the experimental facility is the electronics cartridge assembly which houses the heated elements meant to simulate high

performance processing devices. The construction of this cartridge assembly implements the requisite design features for immersing these elements in a dielectric fluid coolant as well as keeping this fluid sealed within the enclosure and free of outside contaminants. An image showing this assembly is presented as Figure 28. The primary component within this assembly is the housing which is milled out a solid aluminum block and has outside dimensions of 150 mm x 300 mm x 38 mm (H x L x W). The motivation behind deciding to mill the enclosure out of a solid block rather than some other assembly method, such as bolting together all six faces of the enclosure or welding the sides together, is two-fold. Dielectric fluids, like refrigerants in an automobile line or hose, are extremely prone to leaking. Finding cracks in construction and travelling through them is due primarily to the fluid's highly wetting nature. The microscopic cracks that are generated by welding techniques are prime candidates for leak points. Therefore this approach was avoided for the construction of this experimental facility. Gasketed joints, using Ethylene-Propylene-Diene-Monomer (EPDM), with a hole to hole spacing of approximately an inch and applying hand tightening torques to the fasteners proved very effective at sealing the fluid over hundreds of hours of testing and months of containment within the enclosure. In addition to keeping the fluid within the cartridge, it is equally important to keep contaminants, such as water, out. Water, being conductive, would damage the electronics housed within the assembly if they were exposed to it. For the Novec 649 used in the current study, the mixture of these fluids would result in the formation of an acid which could damage the gaskets as well as the electronics. This is not as much of a problem for the FC-72 used in the current study as these two fluids are immiscible. In fact, this immiscibility forms the basis for the two-fluid cartridge design proposed by Campbell *et al* [59] referenced in the Novel Electronics Cooling System Studies section. Again, over hundreds of hours of testing and

months of containment, the sealing and construction method employed protected the fluid and electronics very well, illustrating that the proposed design can effectively prevent contamination of the coolant as well as adequately contain the dielectric fluid within the enclosure. The second reason for designing the cartridge out of a solid aluminum block has to do with the improvement in thermal contact between the condenser fins that are suspended from the top inside face of the cartridge and the exterior channels through which the system level coolant flows to remove the heat from the cartridge for subsequent rejection to ambient. The condenser fin array could take the form of an attached commercial heat sink to the top inside face of the cartridge but this would require some sort of attachment method, introducing another thermal resistance into the heat flow path out of the cartridge. Furthermore, if this attachment method were an adhesive TIM, introduction of an outside material could introduce an unknown incompatibility with the dielectric fluids used. This would probably prove to be more of a problem with the Novec 649

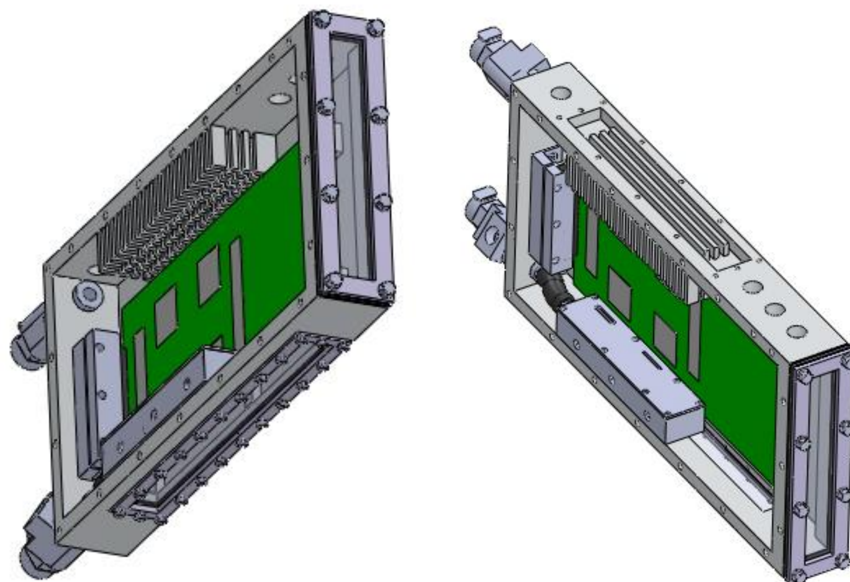


Figure 29 – Condenser fin and external coolant channel images

fluid used than with the more stable, and more expensive, FC-72, but further compatibility studies would be consequently required with the introduction of another material in the system. This system level coolant is an 80/20 mixture of deionized water and Dowtherm SR-1™ ethylene glycol respectively and will hereafter be referred to as Chilled Water (CW). The exterior channels are located at the top external face of the cartridge, illustrated by the right image of Figure 29. There are four channels through which the external coolant flows. Each channel has a width of 0.125" (3.2 mm) and a depth of 0.32" (8.1 mm) and are each separated by a gap of 0.125" (3.2 mm) width and 0.32" (8.1 mm) depth. The internal condenser consists of a 4 x 21 array of fins that reach 0.85" down from the top inside face of the primary enclosure, as illustrated by the left image in Figure 29. All fluid connections to the cartridge assembly are made by quick-disconnect couplings from the Colder© Products LC series. These connectors have done an excellent job over the course of the testing and storage of the experimental facility at containing both the chilled water and dielectric fluids. The drawing depicting the construction of the base enclosure can be found in Appendix I as drawing number AUB-100000.

There are a number of instruments integrated on the cartridge assembly shown in Figure 28 that relay important data and support general conclusions about the effectiveness of the cartridge design. Going from right to left on the image from Figure 28, the first instrument that protrudes down from the threaded port at the top face of the cartridge assembly is a K-type probe style thermocouple from the Omega Engineering M12 series. This thermocouple is placed at the most quiescent point possible in the immersed dielectric fluid during pool boiling heat transfer, therefore it is used as the pool temperature in the determination of heat transfer coefficients for this scenario. The next port going from right to left is plugged so as to provide a place for any additional instrumentation needed in the future. The third port in the sequence is a gage pressure

sensor from the Omega Engineering PX4200 series. The pressure is monitored with the sensor and the attached visual display from the Omega Engineering PM1000 series to be as close to ambient as possible. This operating condition is maintained through the use of a vented Graham Condenser (GC) shown on the far left port on the top external face of the cartridge assembly illustration of Figure 28. In a practical application this condition could be maintained with a collective bellows for all of the cartridge assemblies housed in a server rack. The primary improvement this applications oriented feature would provide is a true sealing of the fluid within the cartridge during operation. With that being said, fluid losses over the course of all the testing conducted and storage of the experimental facility during this study were negligible. In addition to this qualitative assessment, inlet and outlet thermocouples along with a flow meter attached to the coolant delivery line for the Graham condenser gives insight into the vapor losses during operation. By conducting a simple sensible heat gain analysis of this information, the Graham condenser was shown to have not only a negligible amount of heat gain throughout and in relation to the internal primary die power dissipations tested but also illustrate trends associated with fundamental expectations of this device in a temperature controlled laboratory environment.

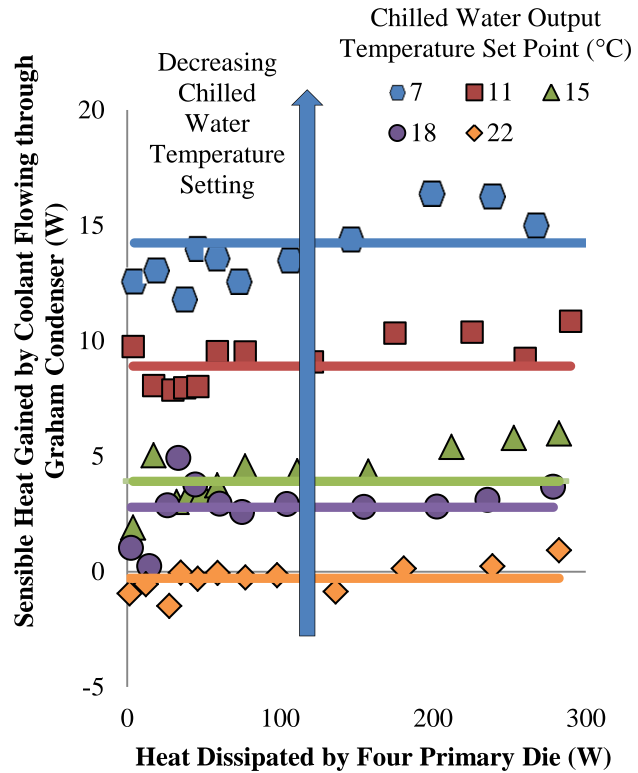


Figure 30 – Graham condenser heat gain analysis

The results of this analysis are presented in Figure 30. The data points represent the actual measurements taken while the solid lines represent the average value of the sensible heat gained over all the data points in that test. As will be discussed in further detail in the Fluid Delivery and Monitoring Subsystems section, the chilled water output to all of the components in this external coolant's flow loop is set to a specified temperature by a chiller. The range of chilled water set points tested for pool boiling conditions was 7°C, 11°C, 15°C, 18°C, and 22°C. From the data presented in Figure 30, an interesting but expected trend is evident. With the decrease in chilled water temperature being supplied to the Graham condenser, an increase in the amount of heat gained by the fluid flowing through it is acquired. This is because of the natural convection heat transfer increase from the ambient environment to the cylindrical surface of the Graham condenser as the driving temperature difference between the fluid travelling through it and that of the laboratory increases. Furthermore, each chilled water set point data set shown on Figure 30 represents roughly five to seven hours of continuous testing. The sinusoidal behavior of the data presented over the course of the primary die heat dissipations tested for each chilled water set point is representative of the air conditioning unit in the temperature controlled laboratory cycling over this extended period of time. The relatively negligible heat gain experienced by the fluid flowing through the Graham condenser along with concurrence with the previously mentioned fundamental expectations supports the conclusion that over the course of the power dissipations tested, fluid loss during operation is negligible as any vapor entering the Graham condenser would have been shown as a noticeable deviation from the sensible heat gain data presented in Figure 30. This deviation would stem from the latent heat of vaporization transfer taking place via condensation within the Graham condenser. This conclusion is important as, in a fundamental application where a bellows or some other design feature is used to seal the unit, it

is important that fluid losses in the form of vapor leaving the cartridge be limited so as to not result in significant pressurization of the system. This pressurization of the system would result in an increase in the saturation temperature of the internal dielectric fluid which would in turn increase the surface temperature required to drive two-phase heat transfer. Consequently, the increase in driving chip junction temperature would lead to a decrease in reliability of the system which runs contradictory to the benefits resulting from the excellent heat transfer coefficients of two-phase heat transfer as illustrated by Figure 11. While the Graham condenser may not represent a large amount of heat loss, the output of its monitoring yields interesting insight into the potential commercial design of this thermal management solution along with expected performance capabilities.

Qualitative and quantitative visualization of the heat transfer and fluid flow performance is made possible through the use of clear polycarbonate windows. These windows are located at the front, right and bottom faces of the cartridge assembly as viewed from the orientation presented in Figure 28. Sample polycarbonate viewing window construction drawings are presented as AUB-100002 and AUB-100003 in Appendix I. It was found that over the course of the two-phase PIV testing conducted as part of the current study, the rhodamine B resin coating of the particles caused them to stick to the polycarbonate surfaces to a degree that made PIV imaging impossible. Replacing the central viewing window on the front face with one of the same size made of quartz proved effective at overcoming the sticking particle problem. In addition, quartz has a higher transmissivity than clear polycarbonate resulting in images that were slightly clearer.

Housed within the electronics enclosure shown immersed in dielectric fluid in Figure 28 is a Printed Circuit Board (PCB) which contains the heated elements meant to simulate high

performance computing devices. Integrated into this board is all the functionality and connectivity necessary to deliver power and relay signals back to the Data Acquisition (DAQ) system for monitoring thermal performance. Power, and thus heat dissipation, delivery is made possible through the use of resistance heaters embedded on the thermal test cells that make up the four square and two rectangular elements seen on the PCB. Temperature measurement is taken from the five-diode series string also embedded on the test cell. A circuit diagram illustrating how these functions are combined onto each cell is shown as Figure 31. Power is supplied to the internal resistance heaters by a constant current source from an AMREL™ SPS series power supply. The five-diode series string is excited by a 2.2 mA current from a Keithley© Model 2401 source meter. The induced voltage drop across the diodes, as well as all of the other measurements taken in the entire experimental facility, are

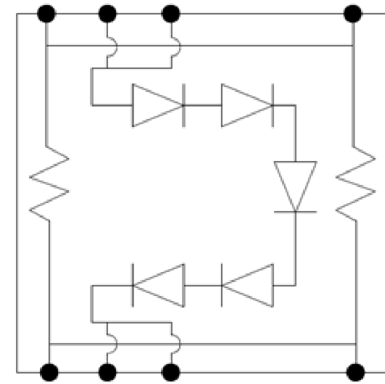


Figure 31 – Thermal test cell circuit diagram

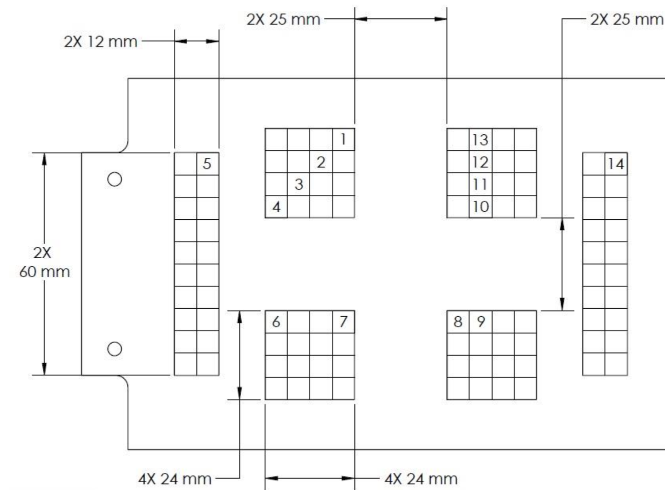


Figure 32 – PCB schematic and thermal test cell layout

Table 1 - Surface Temperature Measurement Locations

Surface	Diode Locations from Fig. FIGURE 32
Bare Silicon	2,6,8,9,10,12
Microporous	1,2,3,4,6,7,8,9,10,11,12,13
Microfinned	3,4,6,7,10,11,13

monitored and processed with a LabView™ Virtual Instrument (VI) from National Instruments©. These test cells are from the Kokomo Semiconductor© PST4 series measuring 0.25" x 0.25" (6.32 mm x 6.34 mm) each. These test cells combine to make the gridded array shown in the PCB schematic Figure 32. Also shown in Figure 32 are the relevant heated element spacings. The test cells have a temperature measurement sensitivity of 10 mV/°C. Both signal and power enters the cartridge through a MIL-STD-83513 100-pin connector from the Glenair© 177-705H series. This panel mount connector press fits with the PCB mounted Glenair GMR 7590 series connector inside the cartridge. From the PCB mounted connector, the signal and power travels through the traces embedded within the three-layer board which has an overall thickness of 0.06" (3 mm). These traces were laid out by the Allegro™ Computer Aided Design (CAD) program. The power and signal finally reach the thermal test cell through solder bump node vias that penetrate through the PCB at precise locations to join with the black filled circles shown on Figure 31. Even though there are 100 pins of connectivity at the external cartridge interface, this is not enough to allow every thermal test cell in the gridded array of each thermal element to measure temperature through the use of its five-diode series string. Consequently, only fourteen locations are connected by the internal PCB traces, which are indicated on the PCB schematic Figure 32. As there are inevitable failures within thermal test cells associated with the yield in the manufacturing process as well as available I/O restrictions due to DAQ system limitations and upgrades over time, each surface condition examined only had certain diodes active during their testing. The locations of these elements for each test surface are indicated by the numbers presented in Table 1 in association with the numbered locations shown on Figure 32. For each test surface, the numbered locations represented in Table 1 indicate the thermal test cells used to determine the average temperature of the four primary die for the data presented in

the current study. Even though only certain locations can measure temperature, all of the heaters on the thermal test cells are active through connectivity within the PCB structure. The tall and slender rectangular elements to the left and right of the four primary die as shown on Figure 32 represent less power dense elements found on a server board, such as a Dual Inline Memory Module (DIMM). The influence of these elements on the performance of the primary components, namely processor chips, must be explored in order to gain a deeper understanding of how this thermal management solution would work in a practical situation.

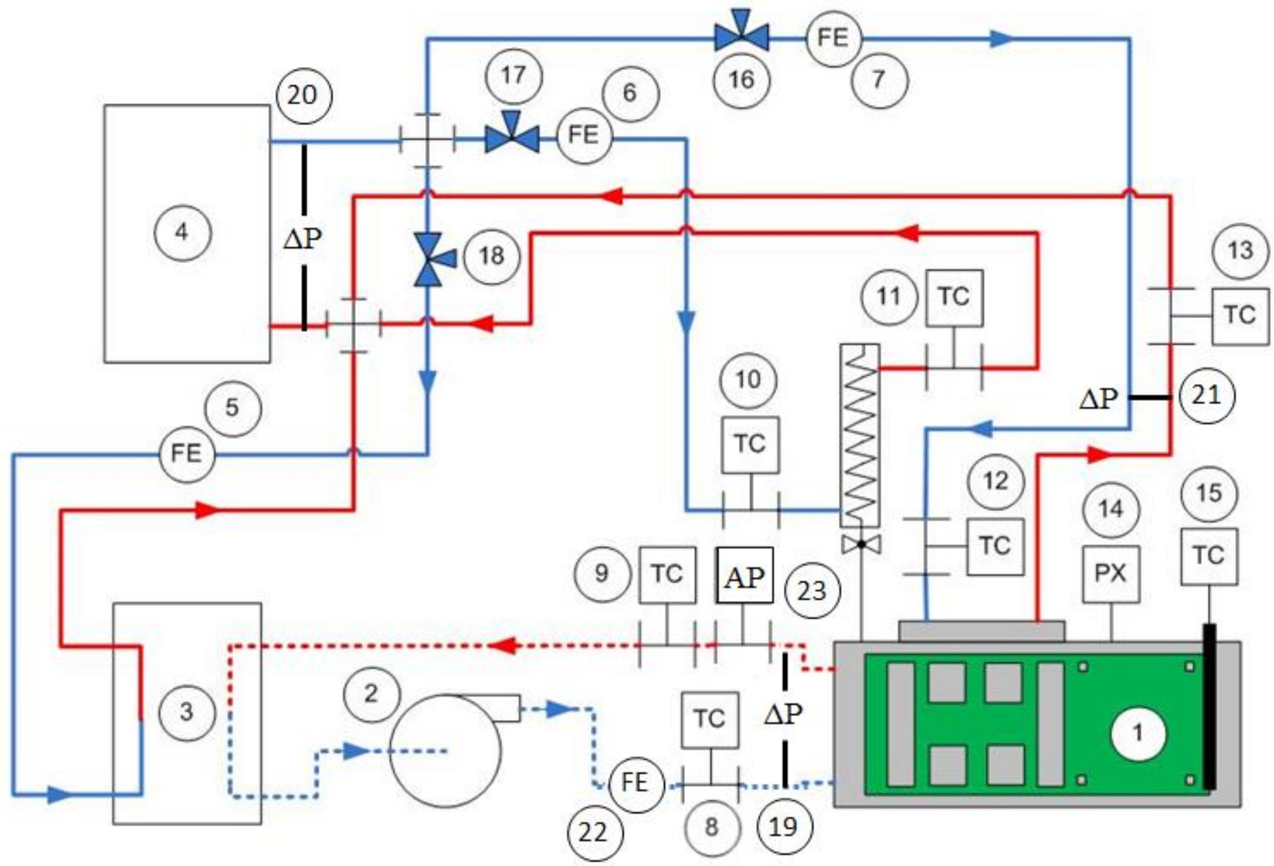
In order to ensure steady-state was adequately reached for the tests conducted within this study, a feedback loop was written into the DAQ programming language which checked the voltage drop across all of the internal resistance heaters being powered. This voltage was selected as a suitable stability criterion due to the relation between the resistivity of the embedded heaters within the thermal test cells and temperature. From the constant current source used to power the heaters mentioned previously, constant voltage would imply constant resistance from Ohm's law. Constant resistance would then imply a stable temperature. This voltage was recorded at a sampling rate of 1 kHz for two minutes. All of these recorded values were subsequently averaged. The program then repeated this process, comparing the latest value with previous average. If this difference was less than 1.5 mV, the program executed temperature measurement throughout the diodes. At each data point, the stabilization criterion was checked for a maximum of 12 iterations, or over 25 minutes, at which point conditions were assumed to be close enough to steady state to proceed. For higher level heat fluxes, those well into the fully developed boiling regime, this criterion was met within 1-3 iterations for all tests conducted. However, for lower heat fluxes, like those in the natural convection regime, steady state conditions usually had to be assumed as the maximum number of iterations for the voltage

drop procedure had been executed. The pool temperature thermocouple was not used in this steady state stabilization check for the pool boiling experiments conducted within this study but certainly could be if further validation of steady state conditions were necessary and more time was available to allow for steady state to be fully reached at these lower heat fluxes. Each experimental surface board was placed in a temperature controlled oven for calibration along with a NIST-traceable thermistor, attaining individual calibration curves for each of these test vehicles. As the oven's temperature set point was varied, the output of the thermistor was monitored. Once the output of the NIST-traceable thermistor was deemed stable for each temperature set point, the induced diode voltages were measured by the DAQ system's calibration program. The thermistor used is accurate to ±0.01°C and the overall uncertainty for the thermal test cell's temperature measurement was calculated to be ±0.09°C. Each surface condition had its own dedicated board, and calibration was conducted after the surface enhancement was attached. Therefore, each surface's test vehicle had its own calibration curve for temperature measurement. Using results from a more conventional pool boiling study and similar surfaces to those used in this study, repeatability of the temperature data was found to be ±1°C [98].

3.2 Flow Delivery and Monitoring Subsystems

The coolant flow delivery system consists of two completely isolated flow loops, one for the chilled water external cartridge heat extraction and another for the dielectric fluid used for electronics immersion cooling. The isolation of these two loops is important for the contamination concerns expressed in the Electronics Cartridge Assembly Design Motivations and Construction section. The schematic presented as Figure 33 represents a Process Flow Diagram (PFD) for the delivery and monitoring of these two coolants throughout the

experimental facility. For ease of referencing, the individual components will be called out by their Find Numbers (FNs) as they are described in the following paragraphs.



<u>Legend</u>

Dielectric Fluid Return Line — Chilled Water Return
Dielectric Fluid Supply Line — Chilled Water Supply

<u>Find Numbers</u>

1 Experimental Cartridge Assembly
2 Dielectric Fluid Pump
3 Liquid-Liquid HX
4 Chiller
5 CW Flow Meter (HX)
6 CW Flow Meter (GC)
7 CW Flow Meter (CW Header)
8 Thermocouple (DF Inlet)
9 Thermocouple (DF Outlet)
10 Thermocouple (GC Inlet)
11 Thermocouple (GC Outlet)
12 Thermocouple (CW Header Inlet)
13 Thermocouple (CW Header Outlet)
14 Cartridge Gage Pressure Transducer
15 Cartridge Pool Temperature TC
16 Header CW Flow Needle Valve
17 GC CW Flow Needle Valve
18 Liquid-Liquid HX Flow Needle Valve
19 Cartridge DF Flow ΔP Sensor
20 Chiller CW Flow ΔP Sensor
21 CW Header Flow ΔP Sensor
22 DF Fluid Flow Meter

Figure 33 – Coolant flow loop and instrumentation schematic

The dielectric fluid flow loop, represented by the dashed lines in Figure 33, delivers subcooled fluid to the heated elements within the cartridge. The fluid is forced through this loop by an Ismatec® MCP-Z standard series pump (FN 2) with an integrated GJ series external gear pump head from Micropump®. The MCP-Z series pump has a feature where the flow rate can be specified and maintained. The calibrated set points at the pump interface are used as the dielectric fluid flow rate values for the results reported in this study. The actual flow rate is monitored by the Sponsler Lo-Flo series flow meter (FN 22). The frequency output of this flow meter (P/N: MF90-MB-PH-A-4X-V) is converted to a 0-5V signal for compatibility with the National Instruments DAQ system by a Sponsler 3 wire analog transmitter (P/N: SP711-3). After passing by the heated elements within the cartridge, the sensible heat gained by the fluid is transferred to the chilled water flow loop by a liquid-liquid heat exchanger (FN 3) from FlatPlate®, P/N: FP3X8-14. This heat exchanger (HX) along with the design and construction methods utilized for the cartridge assembly described in the Electronics Cartridge Assembly Design Motivations and Construction section ensure that this flow path is a completely closed and isolated loop. Since the dielectric fluid properties are governed by its temperature and the temperature of the chilled water interfacing with this fluid through the heat exchanger drives the dielectric fluid temperature, this flow meter was calibrated to each of the chiller output temperature settings tested. Each chiller output temperature setting has its own associated dielectric fluid flow meter calibration curve. Sensible heat gain analysis is made possible through the measurements taken by the flow meter (FN 22) and the thermocouples at the inlet and outlet (FN 8 and FN 9 respectively).

The chilled water distributed throughout the experimental facility is managed by the Fisher-Scientific™ Isotemp™ 1013D series chiller (FN 4). The flow rate is back pressure driven

and adjustable by a threaded rod at the rear of the chiller. However, flow rates to the individual lines shown are adjusted by each flow loop's needle valve (FN 16, FN 17, and FN 18). The flow meters for each individual loop are from the FLR1000 series from Omega Engineering (FN 5, FN 6, and FN 7). The measurements from these flow meters in conjunction with the inlet thermocouples (FN 10 and FN 12) and the outlet thermocouples (FN 11 and FN 13) give the sensible heat gained by the coolant flowing through each of these flow loops (Graham condenser and chilled water header channels respectively). The chiller output set point is adjustable to 0.1°C. This output set point is referred to as the facility water temperature throughout the results reported in this study. An actual installation using this thermal management system solution would be graded on how well it behaves over the course of various chiller outlet temperatures and flow rates given that a certain amount of power input is necessary to manage both of these parameters. For this reason, the thermal performance of the system is graded against variations in the facility water temperature, specifically for the pool boiling scenario. For this condition, the facility water temperature was varied between 7°C, 11°C, 15°C, 18°C, and 22°C. For the flow boiling conditions examined only the 15°C facility water temperature was examined as there were many other variables tested for this scenario.

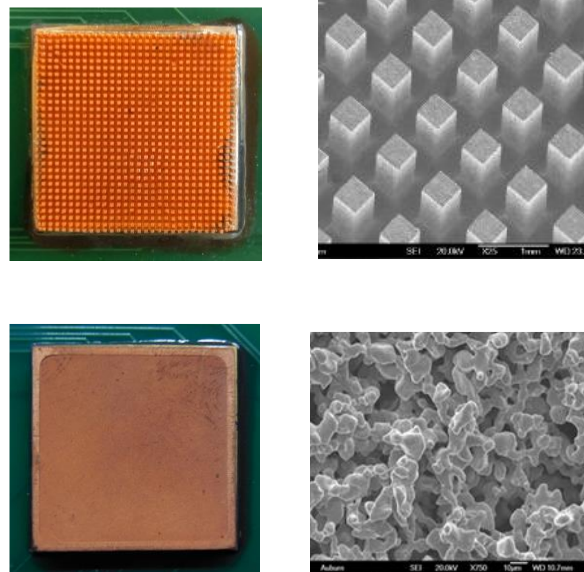


Figure 34 – Two-phase surface enhancement images

3.3 Surface Enhancement Details

While the reduction in manufacturing steps necessary as well as the elimination of

thermal resistances brought about by the inclusion of devices such as heat sinks are attractive benefits of boiling from the bare silicon surface in a liquid immersion cooled server application, the heat transfer coefficient improvements and thus operating temperature reductions possible through the use of two-phase surface enhancement surfaces cannot be ignored. The two surface enhancements studied were the microporous (MP) surface and microfinned (MF) surface. A photograph and Scanning Electron Microscope (SEM) image for each surface is provided in Figure 34 with the microfinned surface featured at the top and microporous surface displayed at the bottom of the figure. Prior to the attachment of the surfaces to the test vehicle, the exposed face of the thermal tests cells and the back face of the surface enhancement are layered with a gold film. These layers assist with the adhesion of the surfaces using a metal foil from the Indium Corporation©. The microfinned surface was fabricated using an Electrical Discharge Machining (EDM) method resulting in a 30 x 30 array of square fins measuring 400 micrometers on each side and spaced at 400 micrometers apart. From a solid copper block, fins of 2 mm in height were machined out leaving a base of 1 mm in height. The microfinned surface offers a number of fundamental benefits. The most straightforward of these benefits is that there is simply more surface area from which heat transfer can take place. This is a result of any traditional heat sink installation for air cooling thermal management as well. However, in two-phase heat transfer this additional surface area offers more sites from which boiling can take place or an increase in the number of nucleation sites. In the lower heat flux, or partial nucleate boiling regime as shown in Figure 17, high speed video has shown how bubbles rising through the fins protruding away from the boiling surface oriented vertically bounce from fin to fin. The generation of the thin microlayer of liquid at the junction between this rising bubble and adjacent fins provides a brief but effective moment of heat transfer. Fundamentally, thinner thermal

boundary layers yield higher heat transfer coefficients which is what is generated by this observed phenomenon. Typically however, for a high performance heat flux application, this partial developing nucleation regime is of little consequence as processing elements would be clocked to generate heat fluxes in the fully developed regime so as to take advantage of the higher heat transfer coefficients available in this portion of the boiling curve. Pushing this heat flux higher can result in a closer proximity to the catastrophic CHF event. The microfinned surface offers advantages in this area as well. While bubble coalescence has a deleterious effect on the heat transfer coefficient for the heat fluxes leading up to the CHF event, the microfins can extend beyond this layer providing a heat flow path past the relatively insulating vapor formation near the base. As long as there are sufficient nucleation sites along the fins that are not insulated by the vapor layer, CHF is delayed thus allowing for more computationally dense processors. A simple illustration of this concept is provided as Figure 35.

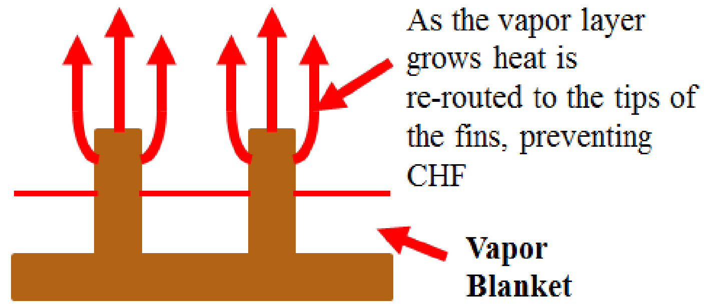


Figure 35 – Microfinned surface CHF benefit

The microporous surface is made by bonding silver coated copper spheres that are approximately 10-50 μm in diameter. Specific details regarding the fabrication of this surface are provided in Appendix II. While the interwoven mesh structure does provide an increased area from which heat transfer can occur, the real improvements this surface offers are an increase in nucleation site density given the porosity of the structure as well as the myriad of avenues quenching fluid can travel to replenish the surface. The surface tension of the fluid travelling through these pores provides an added wicking force that can overcome the shear stresses

induced by the more quickly rising vapor, in effect reaping the benefits of the same properties that cause the fluid to leak through cracks readily as discussed in the Electronics Cartridge Assembly Design Motivations and Construction section. Fundamentally, this added force delays the breakdown of the liquid-vapor interface that would accompany the CHF event which was discussed in the Boiling Heat Transfer Historical Studies section, again allowing for more computationally dense processors to perform safely and at a high level.

3.4 PIV Setup and Execution

The premise behind PIV is the successive image capture of two pictures that show seeded particle locations within a fluid that have been illuminated by a laser at precise time intervals. An example of a base image showing particles within the fluid taken from PIV testing of the current experimental facility is presented as Figure 36. By knowing the time step between images and establishing a calibration distance within the image set, a PIV algorithm can resolve the number of pixels the centroid of the particle has travelled over the known time. The PIV

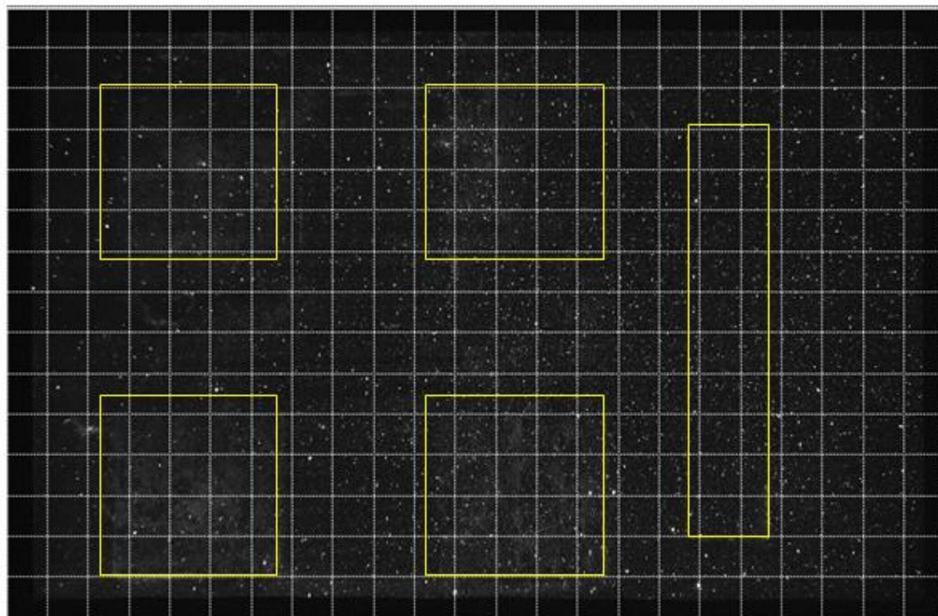


Figure 36 – Sample raw PIV image

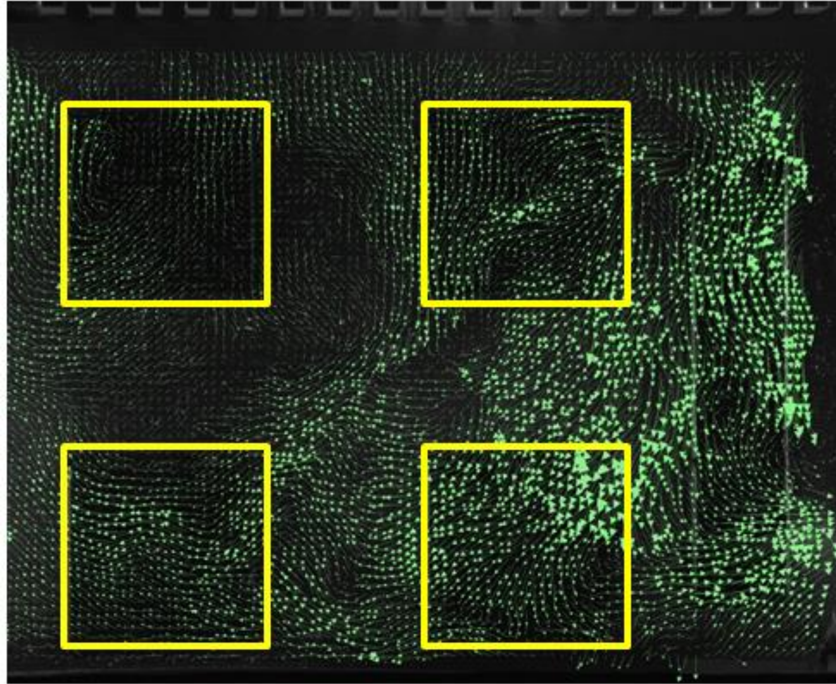


Figure 37 – Sample PIV vector map

analysis method used is a multi-pass algorithm embedded within Quantel's Insight 4G software. The process begins with a 128 x 128 interrogation window (this grid size is represented by the white lines in Figure 36) and converges on a 48 x 48 interrogation window. This convergence results in an 82 x 51 vector set as shown by the sample PIV vector map in Figure 37. In order to get these maps that show the flow over the four primary die, the 200 mJ laser from Quantel illuminates the particles seeded in the fluid from the viewing window on the right side of the cartridge assembly. The camera is oriented perpendicular to that projected laser sheet, or facing the cartridge assembly as shown in the Figure 38 image. These vector maps are then exported to Matlab® to execute the analysis presented in this study.

Seeded particle selection is crucial for successful conduction of PIV experiments. The particle must be large enough to emit a bright enough light for effective signature representation on the raw PIV image. The ability of the PIV algorithm to correctly identify a particle, its

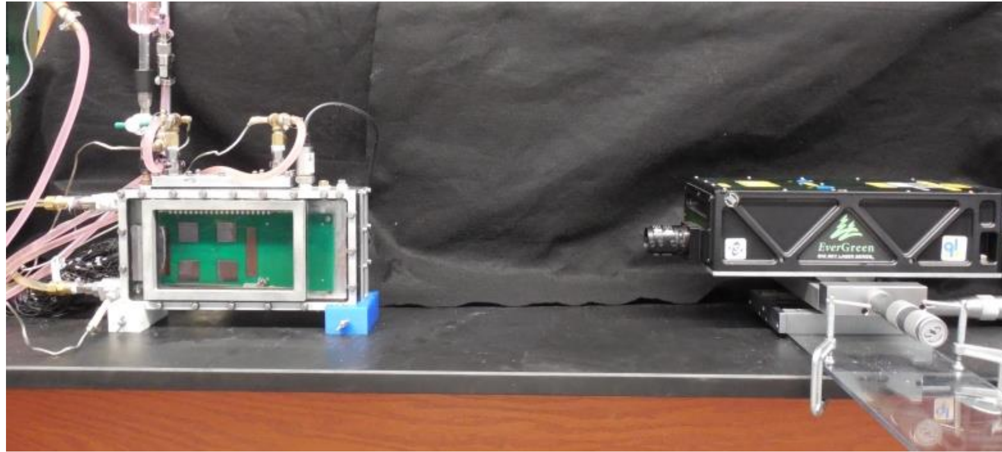


Figure 38 – PIV laser orientation relative to cartridge assembly

centroid and then relative translation to the successive image is tied to this light signature recognition. On the other hand, the particle must not be so big that it occupy too much of an interrogation window. This problem can be mitigated by zooming out, but attention must be paid to the resolution one desires in their resulting vector map. The more you zoom out, the more of the larger particles you can get into an interrogation window but then this window has become larger. With fewer windows in your fixed interrogation area, there are fewer resulting vectors for analysis. The general rule of thumb is that 8-12 particles per initial interrogation window will yield effective vector maps. Most important to ensuring accurate vectors is the selection of a particle that matches the density of the working fluid to the greatest degree possible. For lower acceleration flows like those within the current study, the most direct way to establish particle selection effectiveness is the determination of its time constant, τ_p, and settling velocity, u_s, as shown in Equation 12 and Equation 13 respectively. For the TSI 10089-SLVR particle used in Novec 649 for single phase dielectric fluid flow characterization while the coolant is being pumped through the cartridge, the time constant is 28 μsec while the settling

velocity is 8.3 μm/sec. For the fluorescent two-phase particle used for quenching fluid flow characterization during pool boiling, the time constant is 3 μsec while the settling velocity is -1.8 μm/sec. The negative sign indicates that the particle rises within the fluid given that it is less dense. For perspective, it would take single phase particle 16 hours to sink to the bottom of the

$$\tau_p = \frac{\rho_p d_p^2}{18 \nu_l \rho_l} \tag{12}$$

$$u_s = \frac{\bar{\rho} - 1}{\bar{\rho}} g \tau_p \tag{13}$$

$$\bar{\rho} = \frac{\rho_p}{\rho_l} \tag{14}$$

cartridge assembly from the top of the contained fluid pool while the two-phase particle would take roughly 2 days to rise from the bottom to the top. These are minimal velocities showing that the PIV particles selected are very appropriate for the working fluids used.

For the two-phase flow studies conducted, fluorescent particles were used to distinguish the liquid flow motion without allowing the light reflected from the neighboring vapor to prohibitively interfere with the measurements. The laser emits a light at 532 nm, which on the single phase particles used reflects the light back at the same wavelength. This is also the same wavelength that is reflected off of any generated vapor. To overcome this issue, the fluid is seeded with fluorescent particles that when struck with the 532 nm light, emit light registering at 584 nm. The unwanted 532 nm light that is being reflected from the vapor being generated from the boiling surfaces can be rejected with the use of a filter attached to the camera. The result is an image that shows only seeded particles even though boiling is taking place, which is the condition under which the sample raw PIV image of Figure 36 was taken. Notice that only the

particles are visible in this image and not the vapor being generated from the four square primary elements. With this filtering, the two-phase raw images are processed in the same way as the single-phase raw image sets. Further analysis of the resulting vector sets will be discussed in more proximity to where the data is presented in the Pool Boiling Results and Discussion chapter along with the Flow Boiling Results and Discussion chapter.

3.5 Coolant Distribution Options and Modifications

One of the major advantages offered by the proposed design is the flexibility in coolant delivery options available. If dielectric fluid is pumped through the cartridge, it enters at the fluid connector at the bottom left of the cartridge assembly as shown in Figure 28. When the coolant enters the internal cartridge area, two flow distribution options have been examined. The first, shown on the left of Figure 39 is a simple EPDM tube that injects the flow at a point six

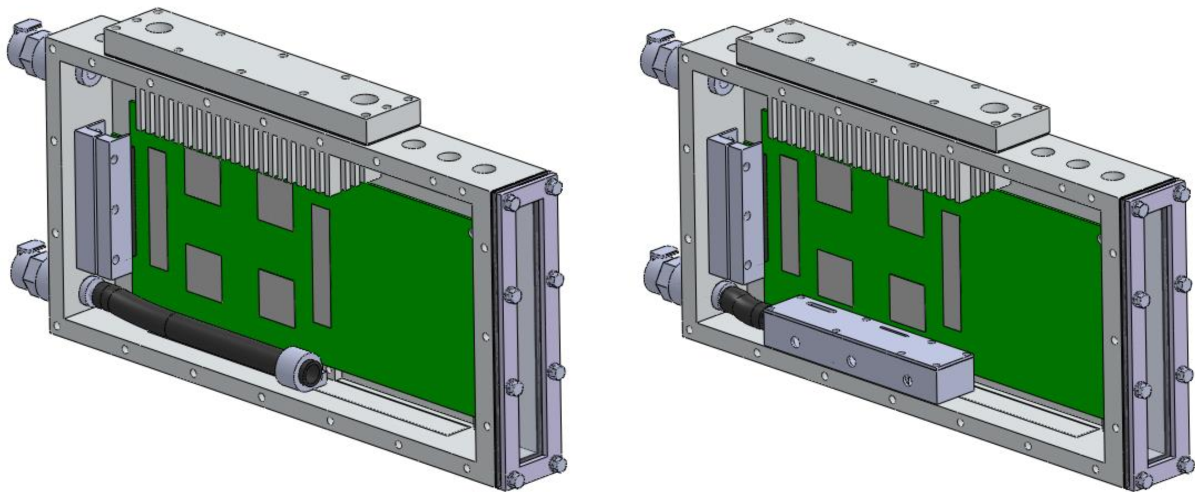


Figure 39 – Two primary dielectric fluid flow distribution methods assessed

inches from the left face of the cartridge and below the four primary heated elements. This tube is secured by a hose clamp affixed to a threaded post on the back inside wall of the cartridge enclosure as shown in the illustration. Preliminary PIV measurements indicated that the flow

was not being distributed over the four primary square heated elements effectively, which was the motivation behind designing a flow distributor as shown in the image on the right of Figure 39. The dimensions and construction of the two pieces that make up this flow distributor are presented as AUB-100034 and AUB-100039 in Appendix II, which are the base and lid respectively. These four square elements are of significant importance as they are tested to a power density both capable of generating two-phase heat transfer as well as representative of high performance processor computational capabilities. For a server application, these are the elements within the electronics housing of most critical importance as they are the workhorse of the data center. Therefore, results will be presented that compare the effectiveness of these two dielectric fluid distribution designs at delivering coolant over these critical components.

In addition to the options on how to deliver fluid within the enclosure, this study examines the benefits and disadvantages of delivering chilled water to the cartridge itself. One of the core issues that data center design engineers and facility maintenance personnel have with the integration of a liquid cooling system is fear about bringing liquid near the costly and sensitive electronics housed within. While bringing dielectric fluid into the data center is unavoidable with the use of a liquid immersion cooling solution, delivery of chilled water to the cartridge is not entirely necessary. The sensible heat gained by the dielectric fluid that flows through the cartridge is rejected into the chilled water by a liquid-liquid heat exchanger that could be placed at a safe distance away from the servers as shown by the Figure 33 PFD. This ability, and the associated thermal performance results reported, should be adequate to mollify these concerns while proving that liquid immersion cooled systems are safe and practical solutions to near-term and future high computational density server installations.

Chapter 4: Pool Boiling Results and Discussion

For the purposes of the current study, the pool boiling scenario will be where the primary means by which heat is extracted from the cartridge is through the chilled water header as shown in Figure 33. The Graham condenser is open and vented, but has been shown to carry negligible heat from the system in the Electronics Cartridge Assembly Design Motivations and Construction section (Section 3.1). Dielectric fluid is not pumped through the cartridge as this condition is considered flow boiling and will be discussed in the Flow Boiling Results and Discussion chapter.

4.1 Bare Silicon Pool Boiling Thermal Performance and Fundamental Trends

With the bare silicon test surface, pool boiling tests were conducted over the range of facility water temperature settings with both working fluids. Table 2 summarizes key thermal performance results yielded over the various facility water temperature settings. The heat fluxes

Table 2 – Bare Die Pool Boiling Thermal Performance Summary

Working Fluid	FC-72					Novec 649				
Facility Water Setting (°C)	7	11	15	18	22	7	11	15	18	22
Heat Flux (W/cm^2)	12.6	11.7	11.8	11.2	11.0	11.8	11.2	10.9	10.8	10.9
Average Surface Temperature (°C)	79.2	78.1	78.6	78.1	77.9	75.2	75.8	76.6	76.8	76.8
Heat Transfer Coefficient (kW/m^{2}K)	4.3	4.1	4.3	4.1	4.2	3.8	3.6	3.5	3.5	3.6
C_{sf}	0.0051					0.0060				

achieved can more than manage current high performance commercially available server applications [38] at a temperature that is well below industry standards for processors. These heat fluxes were calculated assuming uniform heat dissipations across all four bare silicon die, for a total of 4 in^2 or 25.81 cm^2. The heat dissipations are calculated from the measured current and voltage drops across the heaters embedded in the thermal test cells as shown in Figure 31. The average surface temperature that is recorded in Table 2 is the mean value of the temperatures measured from the diode locations listed in Table 1 for the bare silicon surface. The trends and fundamentals influencing these values are discussed in further detail in the Bare Silicon Facility Water Temperature Variation Effects (Section 4.3) and the Condensive Limit Trends and Modelling Attempt (Section 4.6). Typical operating temperatures can range anywhere from 85°C up to 105°C. Even at the lowest point of this range and assuming that the failure rate of a processor doubles for every increase of 10°C [21], these bare silicon results represent a significant improvement in reliability. In addition, this increase in reliability comes with a reduction in manufacturing steps as the addition of heat sinks or spreaders is not necessary. Heat transfer coefficients are in accordance with those expected and documented in Figure 11. The C_{sf} values extracted from the current data set can be used in the Rohsenow equation, shown as Equation 4, to predict performance at intermediate values not recorded experimentally. An example of the C_{sf} extraction equations, process and values used are shown in Appendix III under the C_{sf} Calculation section. The values extracted relate well to those developed in previous studies under more conventional pool boiling conditions. For bare silicon and FC-72, Geisler [86] evaluated a C_{sf} value of 0.0054, while a C_{sf} of 0.0056 was extracted from the data of Ramakrishnan [98] using a saturated pool with a bare silicon single die and Novec 649 as the working fluid.

An interesting trend was discovered when these heat flux results were plotted against wall superheat. For both working fluids, Figure 40 shows the heat flux from the four primary die uniformly heated as a function of the wall superheat with the chiller output setting at 7°C. It is understood that the required surface temperature to initiate boiling as heat flux is increased will be slightly higher than the boiling point of the fluid. The deviation beyond the intersection of the natural convection curve with the fully developed boiling curve is referred to as temperature overshoot and stems from the additional energy necessary to convert liquid within a site to vapor and drive it out of the cavity. As the system is degassed for nearly an hour before each run, nucleation sites are assumed to be rid of dissolved gases to an acceptable degree. These dissolved gases could potentially alleviate the temperature overshoot phenomenon. These

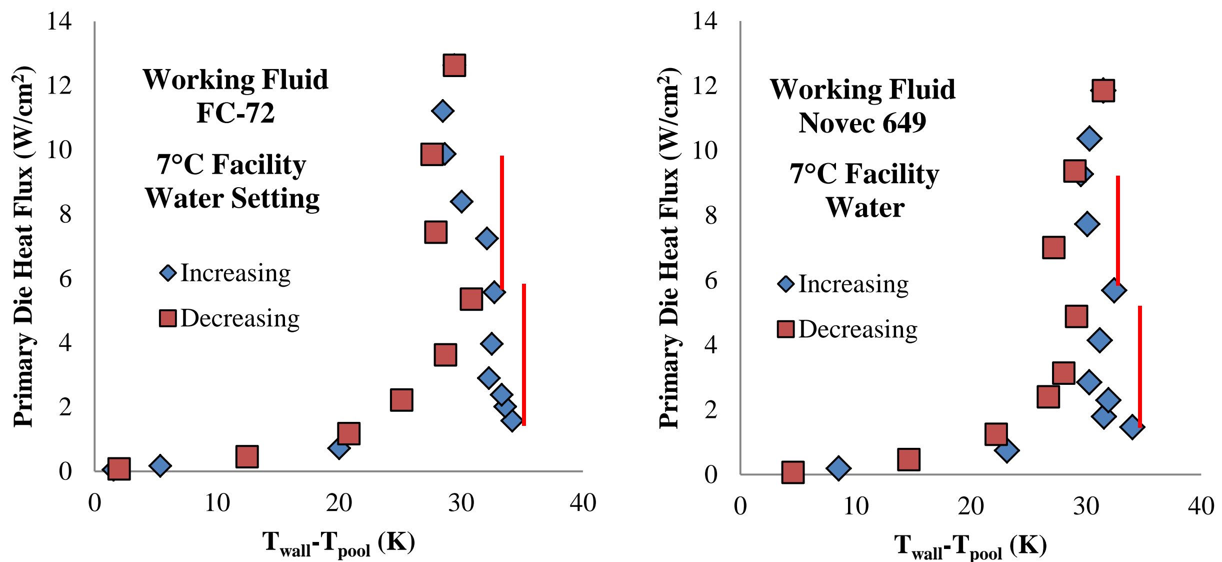


Figure 40 – Primary die heat flux fluid and incipience phenomenon

Red vertical lines on plots indicate the two overshoot locations for the increasing runs

dissolved gases have been naturally trapped in the nucleation site from the advancing contact angle of the fluid to the surface as the coolant initially traverses the surface upon filling. Once these gases are driven out by the duration of degassing previously stated prior to any recorded experimentation, consistent temperature overshoot should be seen on any subsequent runs of increasing heat flux. During degassing and subsequent cooling down of the system before the actual experimental run, site deactivation results in a complete quenching of the cavity with working fluid ideally. This quenching of the site stems from the receding contact angle to the surface as boiling is deactivated and liquid rushes into the cavity. This overshoot is evident in the results of Figure 40 but it seems to occur twice for both working fluids. This double hitch in the boiling curve is atypical for a small single heated surface but is an artifact of the developed boundary layer traversing the top die that was initiated from the natural convection emanating from the bottom die. The relative dimensions have been exaggerated for effect, but the boundary layer development shown in Figure 41 by the red line helps to put this into perspective. Working in conjunction with this developing boundary layer is the fundamental concept laid out by Hsu's model [99] for nucleation site activation requirements. Hsu proposed that a site would activate if it were large enough to

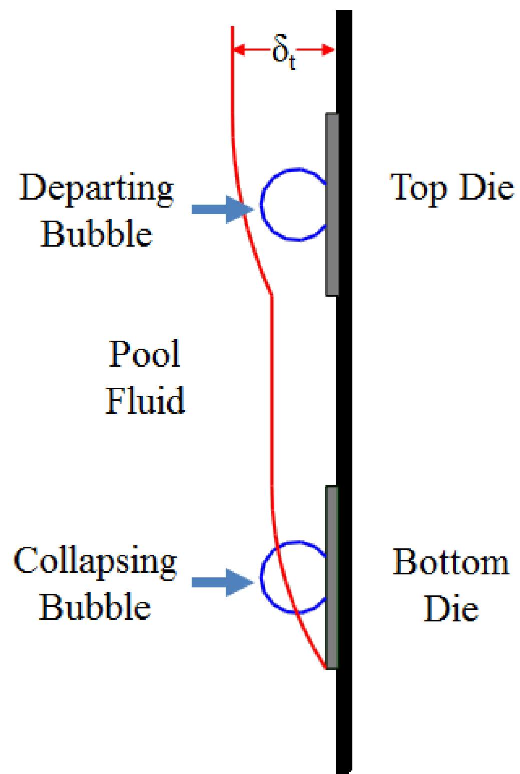


Figure 41 – Hsu model explanation schematic for cartridge incipience phenomenon

overcome the surface tension brought about by the bubble to surface interface around the perimeter of the cavity but small enough so as to not collapse under the exposure of the vapor interface to the ambient saturated pool. The developing boundary layer from the bottom die adds to the effective sites on the top die, thus the top die will begin nucleation before the bottom die. Notice that the two exaggerated bubbles on both the bottom die and top die of Figure 41 are of equal diameter yet the bottom bubble falls outside of the developing boundary layer. Therefore this bubble would not depart from the surface while that of the top die would. Experimentally, this phenomenon is confirmed in the results presented in Figure 43 and Figure 42 for the Novec 649 and FC-72 working fluids respectively. The filled shapes represent the mean value calculated from diode locations 2,10, and 12, assumed to be an adequate representation of the top die average. The unfilled shapes represent the mean value calculated from diode locations 6,8, and 9, assumed to be an adequate representation of the bottom die average. These diode locations are referenced from the locations illustrated on Figure 32. Consistently between both figures, therefore for both working fluids tested, the unfilled shapes representing the bottom die are at a higher temperature than their filled counterparts representing the top die at the roughly 2 W/cm^2 value where the first incipience begins. This is because boiling has been initiated on the top die and, given the higher heat transfer coefficients associated with the two-phase heat transfer mechanism, will present out at a lower temperature. While the recorded data seemed at first atypical, after a review of the fundamental mechanisms involved, the results are in accordance with accepted theory.

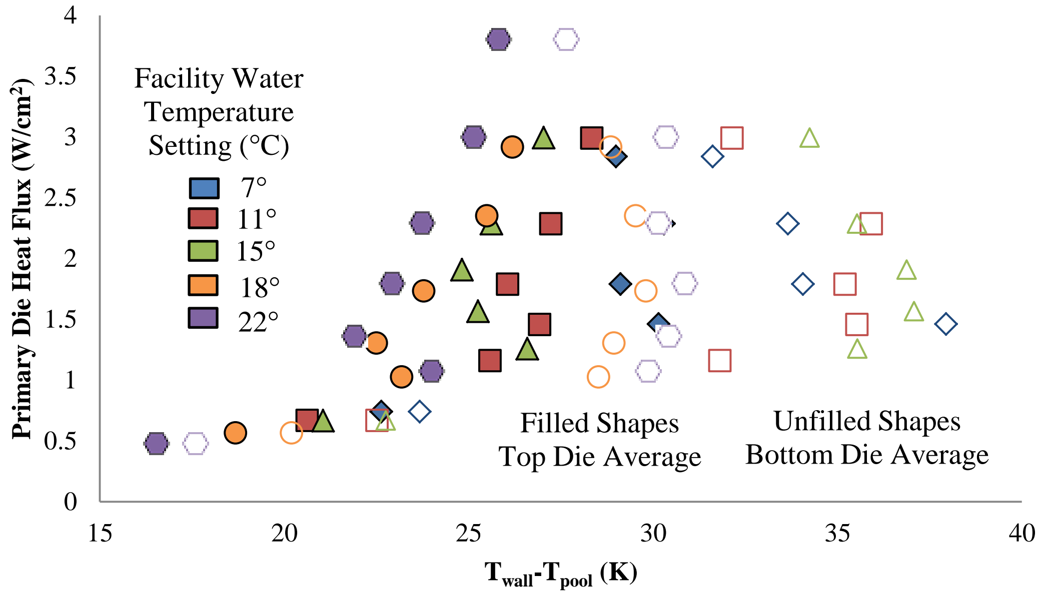


Figure 43 - Bottom vs. top die pool boiling comparison for Novec 649

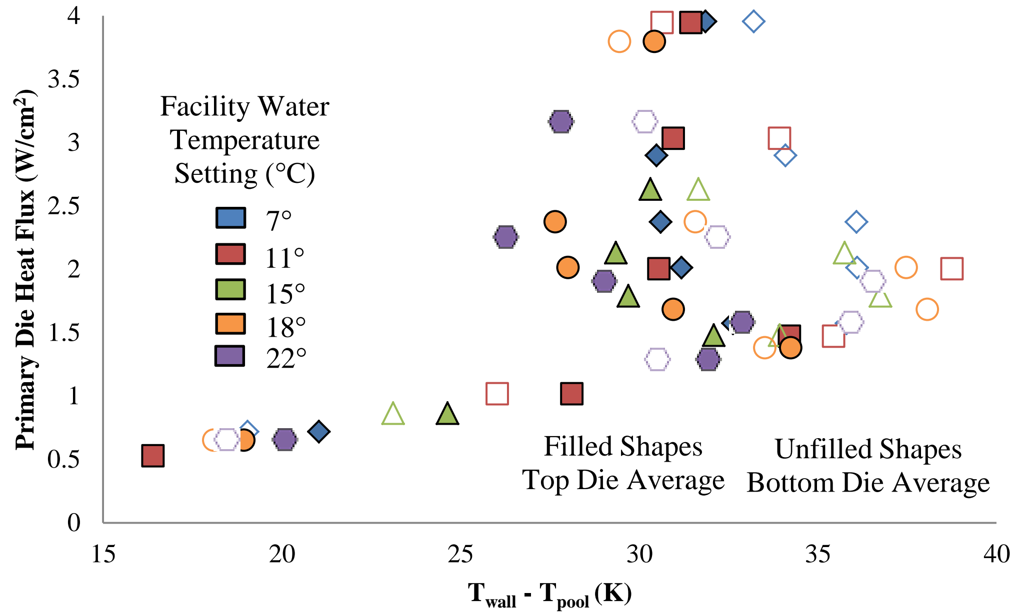


Figure 42 – Bottom vs. top die pool boiling comparison for FC-72

4.2 Pool Boiling Working Fluid Comparison

More fundamental expectations are met when the pool boiling results from both working fluids with the bare silicon surface are compared from an operating temperature standpoint. By defining a Fluid Boiling Enhancement Factor as the ratio of the power dissipation yielded by Novec 649 to that attained with FC-72 at a given surface temperature, a noticeable improvement using Novec 649 over all the facility water temperatures tested is observed at lower surface temperatures. This improvement is reduced as the surface temperature is increased. The reason for the initial improvement is because of the lower saturation temperature of Novec 649 (49°C) versus that of FC-72 (56°C). Boiling is initiated at a lower temperature for Novec 649 than FC-72, so the higher heat transfer coefficients associated with two-phase heat transfer are experienced at this lower operating temperature when Novec 649 is used as the working fluid. Once the temperature gets higher however, FC-72 begins to boil as well, and the improvement experienced by using Novec 649 is lessened. As it is impossible to have the temperatures between experimental runs with each working fluid match exactly, a fifth-order polynomial curve fit of the data is used to acquire a power dissipation versus temperature curve. The temperature at one measured data point is used to extract the power dissipation associated with the other working fluid to be used

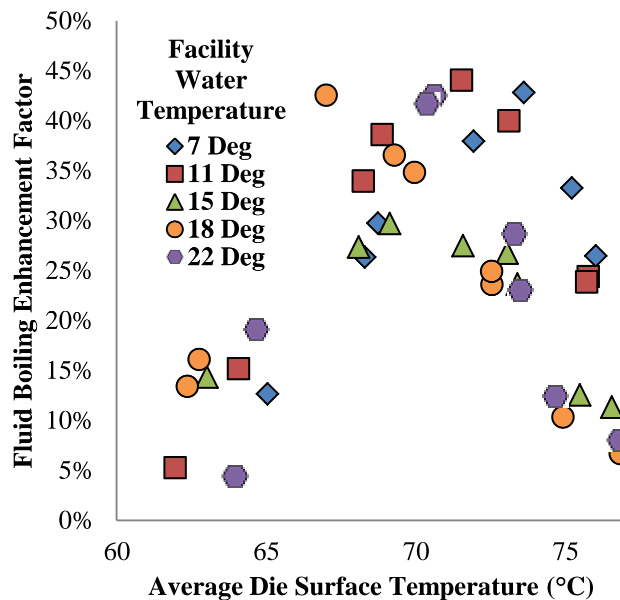


Figure 44 – Working fluid operating temperature comparison

in the proposed ratio. The results showing the improved performance with Novec 649 over a limited range of operating temperatures is presented as Figure 44.

4.3 Bare Silicon Facility Water Temperature Variation Effects

Further theoretical support of the results obtained for pool boiling with bare silicon is shown when the heat flux versus average primary die surface temperature data is plotted with respect to facility water temperature variations. Varying the facility water or condenser temperature should have little effect upon the fully developed boiling heat transfer curves as subcooling in pool boiling has been shown to not alter the performance in this regime significantly [100]. This is not necessarily the case in subcooled flow boiling as will be shown in the Dielectric Fluid Flow Rate Variation and Subcooling Effects section (Section 5.2). Furthermore, pool temperature variation data is presented as Figure 45 to illustrate how, even across variations in the facility water temperature, the pool temperature is only slightly subcooled when compared to the 49°C saturation temperature for Novec 649 and 56°C saturation

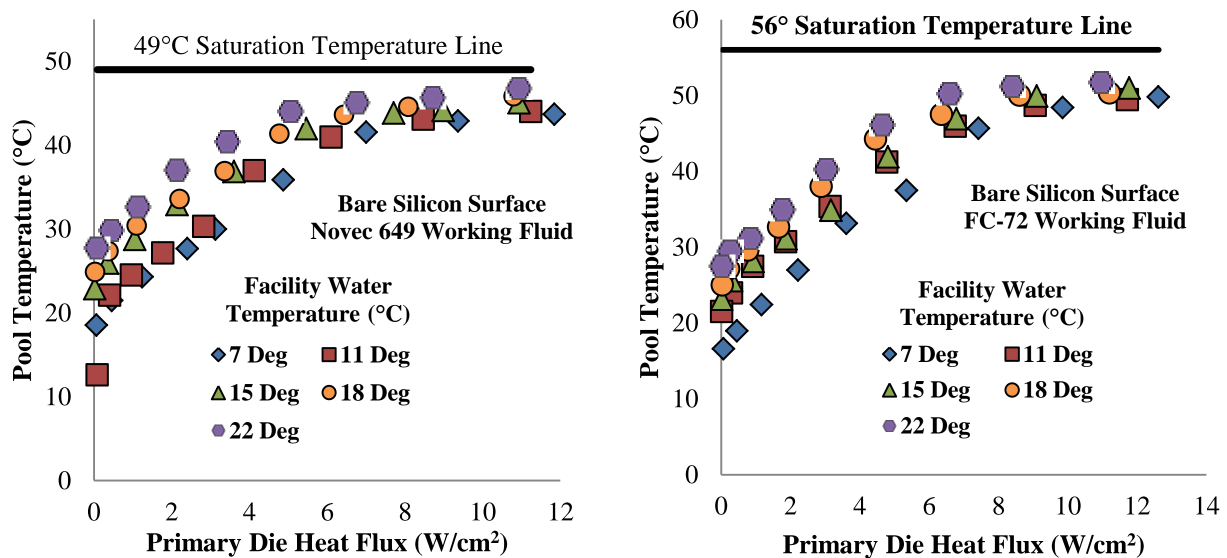


Figure 45 – Bare Silicon Pool Temperature Variations

temperature for FC-72 at the heat fluxes determined to be completely in the fully developed boiling regime. For Novec 649 and FC-72, Figure 46 and Figure 48 respectively, this consistency in the fully developed boiling regime is shown by the area captured between the correlation accuracy margins. In order to show the trends in the heat transfer coefficient data leading up to the maximum values presented in Table 2, heat transfer coefficient values yielded over various facility water temperature settings are presented for Novec 649 and FC-72, Figure 47 and Figure 49 respectively. Figure 47 and Figure 49 illustrate the typical lack of hysteretic effects associated with the decreasing heat flux data of an experimental run. With the relative convergence near saturation of the pool temperatures as shown in the data presented in Figure 45 independent of facility water temperature setting, resultant heat transfer coefficients should coincide with surface temperatures at a particular heat flux independent of facility water temperature setting as well in accordance with Newton's Law of Cooling, shown as Equation 1.

Table 3 – Saturated Fluid Properties for FC-72 and Novec 649

Properties	FC-72	Novec 649
Dynamic Viscosity (μ_l)	4.3×10^{-4} Pa·sec	4.4×10^{-4} Pa·sec
Latent Heat of Vaporizations (h_{lv})	88000 J/kg	87956 J/kg
Liquid Density (ρ_l)	1594 kg/m^3	1517 kg/m^3
Vapor Density (ρ_v)	14.7 kg/m^3	12.6 kg/m^3
Surface Tension (σ)	9.48 mN/m	9.24 mN/m
Liquid Specific Heat (C_{pl})	1100 J/(kg·K)	1118 J/(kg·K)
Saturation Temperature (T_{sat})	56°C	49°C
Liquid Thermal Conductivity (k_l)	0.054 W/(m·K)	0.054 W/(m·K)

In order to assess whether or not a data point was in the fully developed boiling regime, plots were done for both the increasing and decreasing heat flux experiments over all of the facility water temperature settings tested. Those higher heat fluxes that were shown to fall on both the increasing and decreasing curves are considered in the fully developed regime as the hysteresis associated with temperature overshoot should not have any effect in this area. In order to assist with any future theoretical predictions associated with these fluid/surface combinations, C_{sf} values for use in the Rohsenow correlation, Equation 4, have been calculated for the reported data and are presented in Table 2. The saturated fluid properties used to calculate the C_{sf} values for both working fluids are presented in Table 3.

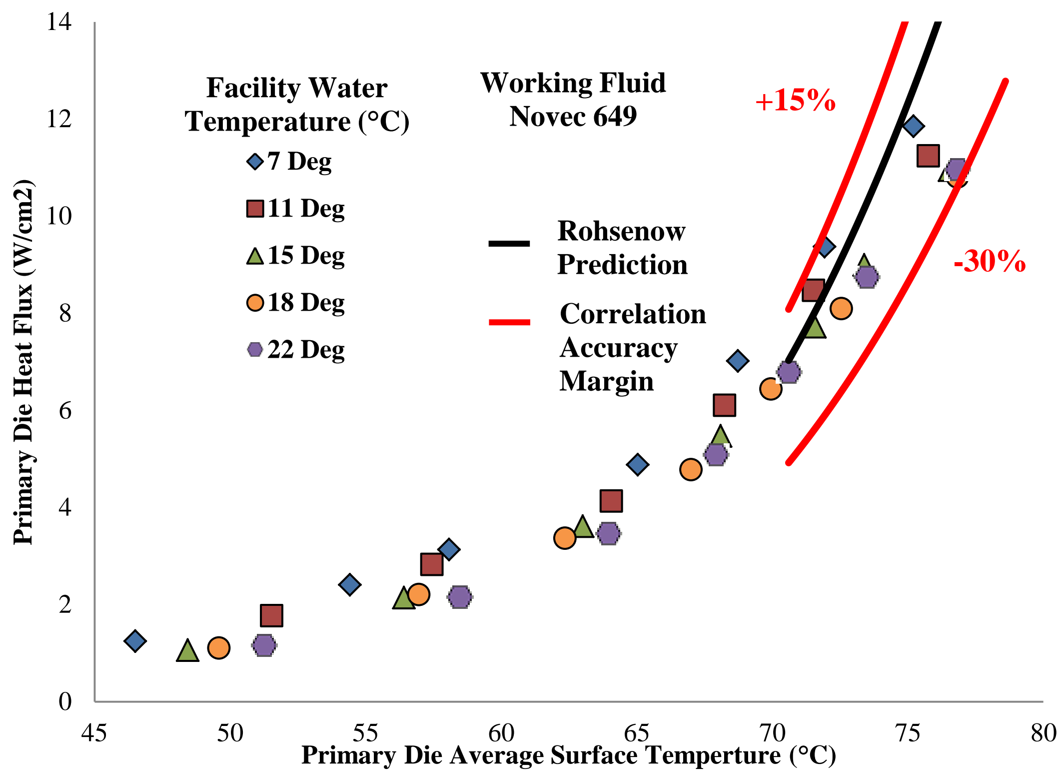


Figure 46 – Novec 649 bare silicon boiling curves over various facility water settings

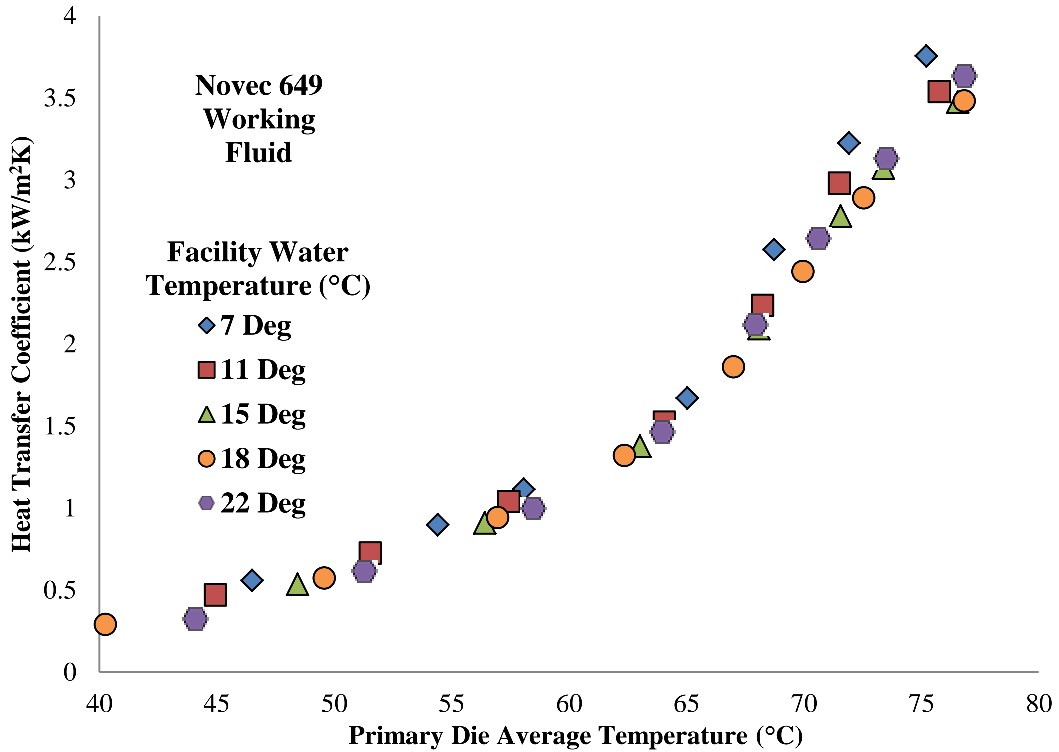


Figure 47 – Novec 649 bare silicon HTC data over various facility water settings

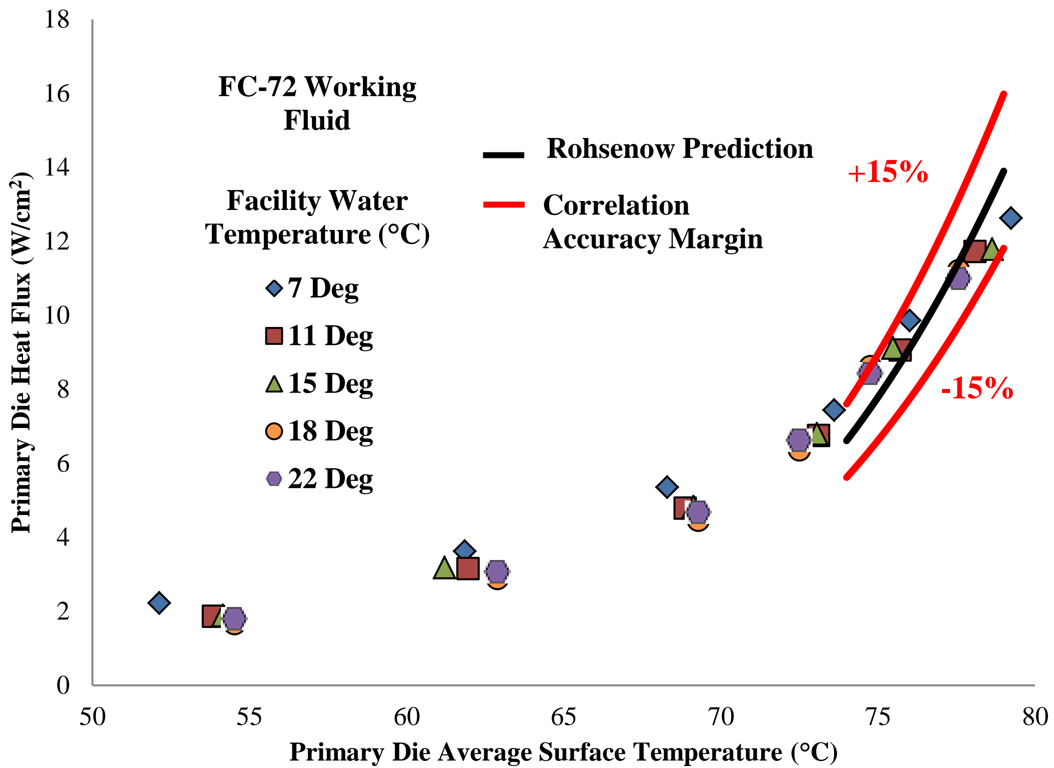


Figure 48 – FC-72 bare silicon boiling curves over various facility water settings

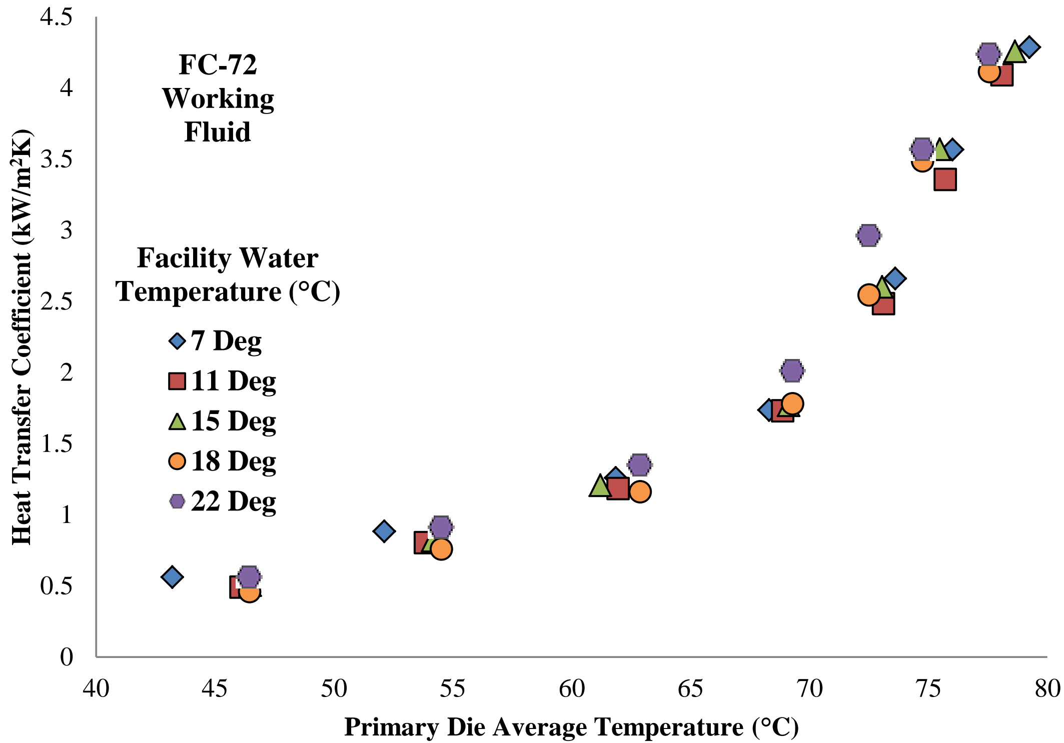


Figure 49 – FC-72 bare silicon HTC data over various facility water settings

4.4 Surface Enhancement Thermal Performance Benefits

While there are additional manufacturing steps associated with the integration of surface enhancements to a processing chip, the thermal performance benefits gained are significant. Slightly more power, and thus computational capability, is available with the integration of both the microporous and microfinned surface, but more important from a reliability standpoint are the increases in heat transfer coefficients

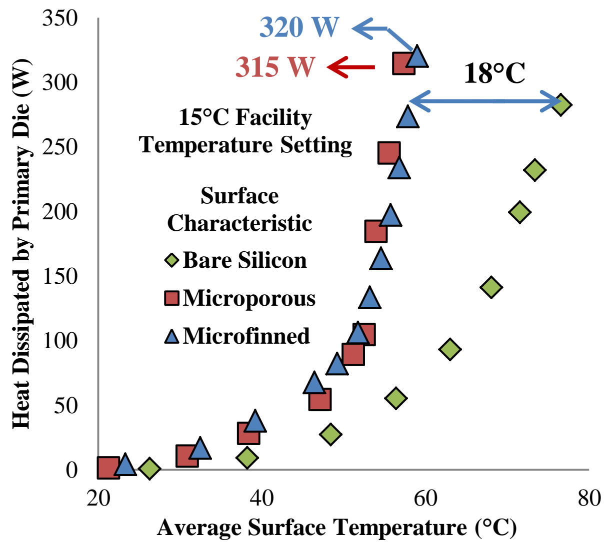


Figure 50 – Surface enhancement power dissipation and operating temperature improvements

and consequent reductions in operating temperature attained. The potential increases in computational and reliability performance are on display in Figure 50. Notice that with the integration of the surface enhancements, volumetric power dissipations under pool boiling conditions are 0.19 W/cm^3, already well over the 0.051 W/cm^3 of current high performance air cooled options [39]. These volumetric power dissipations are available without the need to pump dielectric fluid to the cartridge, ultimately reducing design complexity. These power dissipations achieved are done at a modest operating temperature of roughly 60°C, especially so when compared to typical chip operating temperatures which can be 20°C-25°C higher for even the most effective air cooled thermal management solutions. From a reliability standpoint, the 18°C reduction in operating temperature could represent a substantial decrease in failure rate. Assuming that the failure rate of a processor doubles for every 10°C increase in operating temperature, the use of bare silicon over these surface enhancements could result in a 250% increase in failure rate [21]. These reductions in temperature are in tandem with marked increases in heat transfer coefficients as illustrated by Figure 51. The microporous and microfinned surface yield a 225% and 190% increase in the already high bare silicon heat transfer coefficient respectively. These increases in heat transfer coefficients will prove even more valuable when the module level thermal resistance is analyzed in the Module Level Thermal Resistance Plateaus section (Section 4.7).

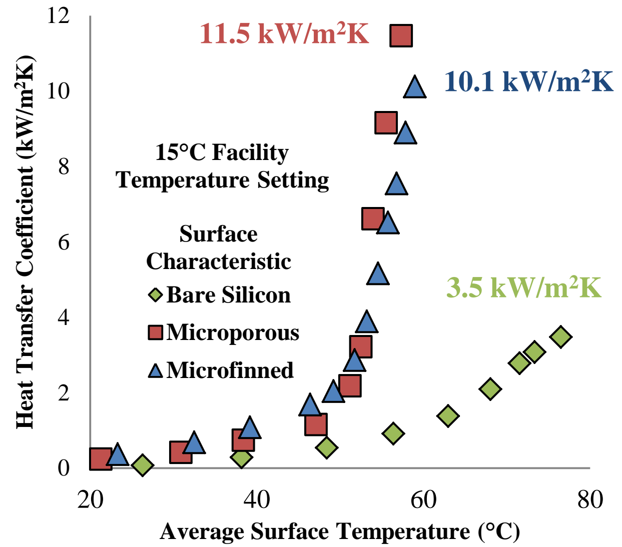


Figure 51 – Surface enhancement heat transfer coefficient improvement

4.5 Surface Enhancement Facility Water Temperature Variation Effects

Like the results of the bare silicon already presented, fundamental expectations are on display with the boiling performance of the surface enhancements when viewed over the various facility water temperature settings tested. A summary of the key performance parameters achieved with the use of these surface enhancements is presented as Table 4. The details regarding the construction and fundamental benefits yielded by the microporous and microfinned surfaces referenced in Table 4 is provided in the Surface Enhancement Details section (Section 3.3). At first glance at the results reported in Table 4, the heat transfer coefficients and average base surface temperatures are substantially higher and lower respectively than equivalent

Table 4 – Surface Enhancement Pool Boiling Thermal Performance Summary

Surface Condition	Microfinned Base Area					Microfinned Total Exposed Area				
Facility Water Setting (°C)	7	11	15	18	22	7	11	15	18	22
Heat Flux (W/cm^2)	13.9	13.0	12.4	11.2	10.1	2.5	2.4	2.3	2.0	1.8
Average Base Surface Temperature (°C)	60.4	60.1	59.0	58.9	58.0	60.4	60.1	59.0	58.9	58.0
Heat Transfer Coefficient (kW/m^2K)	10.1	10.0	10.1	9.5	9.3	1.8	1.8	1.9	1.7	1.7
C_{sf}	0.0018					0.0036				

Surface Condition	Microporous Surface				
Facility Water Setting (°C)	7	11	15	18	22
Heat Flux (W/cm^2)	13.1	11.8	12.2	11.1	10.3
Average Base Surface Temperature (°C)	58.1	57.6	57.4	57.4	57.0
Heat Transfer Coefficient (kW/m^2K)	11.0	10.4	11.5	10.7	10.5
C_{sf}	0.0024				

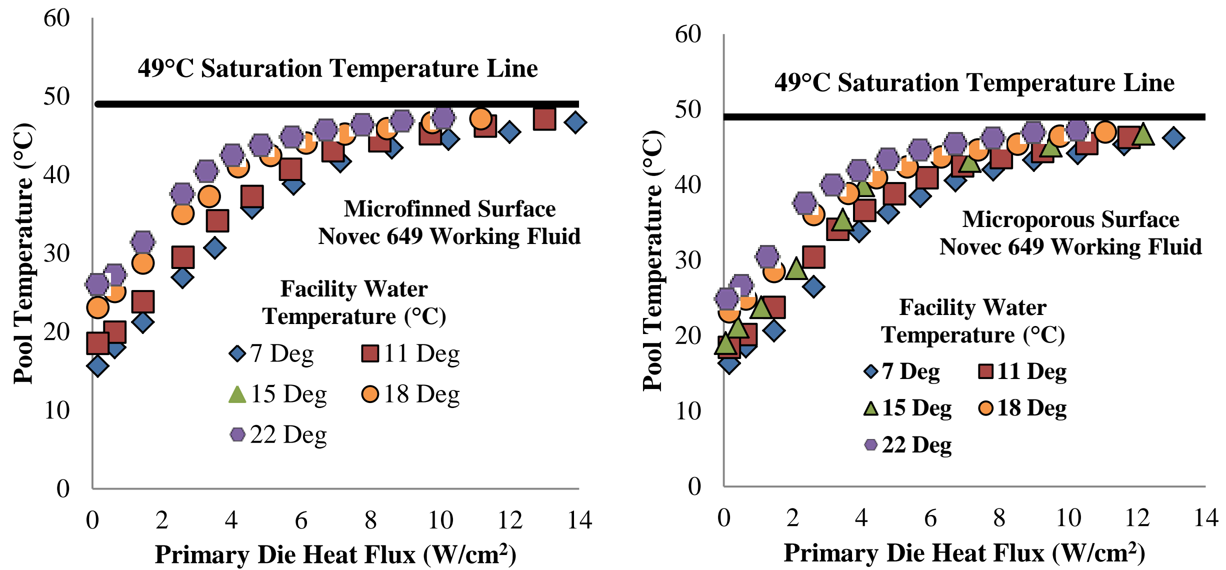


Figure 52 – Surface Enhancement Pool Temperature Variation

benchmarking points presented for the bare silicon case in Table 2. As mentioned in the Surface Enhancement Thermal Performance Benefits section (Section 4.4), two-fold increases in heat transfer coefficients and consequent reductions in operating temperatures are a tremendous advantage to using these surfaces even though additional manufacturing steps are required for their integration. While the microfinned surface is not of prohibitive height to be used in a liquid immersion cooled module even of such tight confinement as that presented in the current study, it is important to understand that it is an extended surface and thus subject to the scrutiny related to the additional volume it occupies. In an effort to address this, Table 4 shows values for the microfinned surface that have been adjusted for its entire exposed surface area, which is 5.5 times that of the base area. The resulting C_{sf} value of 0.0036 from this surface area adjustment could be used for an initial estimate of the fully developed boiling performance of copper and Novec 649, but as with any C_{sf} value, should be experimentally validated with the actual surface and fluid combination. These values were also found to be in good agreement with the results using similar surfaces in a more conventional pool boiling study [50] [98], as mentioned

previously in this chapter. The experimental variations are slightly larger for the enhanced surfaces than those found in the bare silicon results. The most likely contributor to this increased margin is that the Rohsenow correlation is primarily applicable to truly flat surfaces like the bare silicon used. Typical boiling heat transfer predictive error margins can be as high as ±40% and still be acceptable. Therefore, the C_{sf} values shown in Table 4 for these surface enhancements can be used as reasonable initial estimates for fully developed boiling performance with the understanding of their potential margin for error when used in the Rohsenow correlation. The correlation accuracy margins shown on Figure 53 and Figure 54 represent the percentage increase or decrease of the heat flux values predicted by the Rohsenow correlation using the C_{sf} values in Table 4 across the temperature range illustrated. Power dissipation by the primary die with respect to their average surface temperature for Novec 649 as the working fluid over various facility water temperatures along with the correlation accuracy margins are presented as Figure 53 and Figure 54 for the microporous and microfinned surface respectively. The fully developed data for both of these surface conditions do not tend to vary significantly as the facility water temperature setting is varied which is fundamentally expected. Like the bare silicon results, the pool temperature reaches a slightly subcooled plateau for the heat fluxes determined to be in the fully developed regime as shown by Figure 52. Heat transfer coefficients leading up to the maximum values shown in Table 4 are presented as Figure 55 and Figure 56 for the microporous and microfinned surface respectively. As with the argument made previously in the Bare Silicon Facility Water Temperature Variation Effects section (Section 4.3), the convergence of the heat transfer coefficients independent of facility water temperature variation is an artifact of the closeness of the pool temperature independent of facility water temperature setting as shown in Figure 52 and in accordance with Newton's Law of Cooling, shown as

Equation 1. One interesting difference visible in the decreasing heat flux data for the surface enhancements versus that of the bare silicon presented as Figure 47 and Figure 49 for Novec 649 and FC-72, respectively, is the almost immediate transition in the heat transfer mechanism depicted by the sharp shift in the boiling curve. This qualitative assessment is much more evident in the microporous data presented as Figure 55. This is due to the optimal distribution of nucleation site sizes characteristic of these boiling enhancement surfaces allowing for boiling to shut off and initiate with little to no temperature overshoot. This lack of an overshoot for these surfaces was experimentally shown by Sridhar [50] as well.

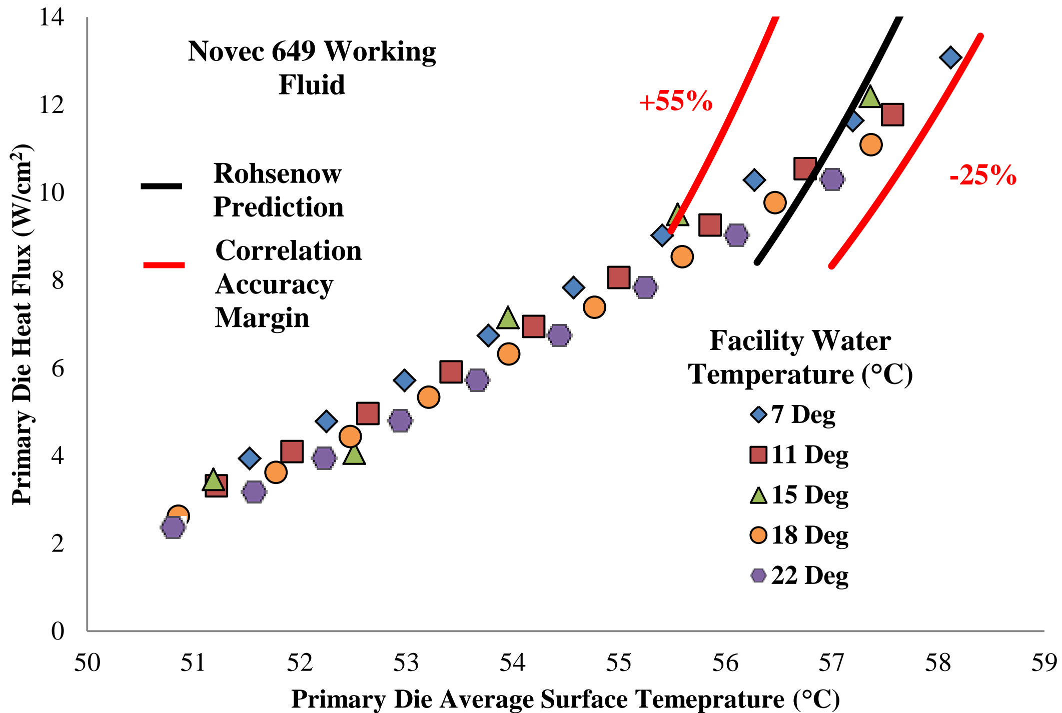


Figure 53 – Microporous surface boiling curves over various facility water settings

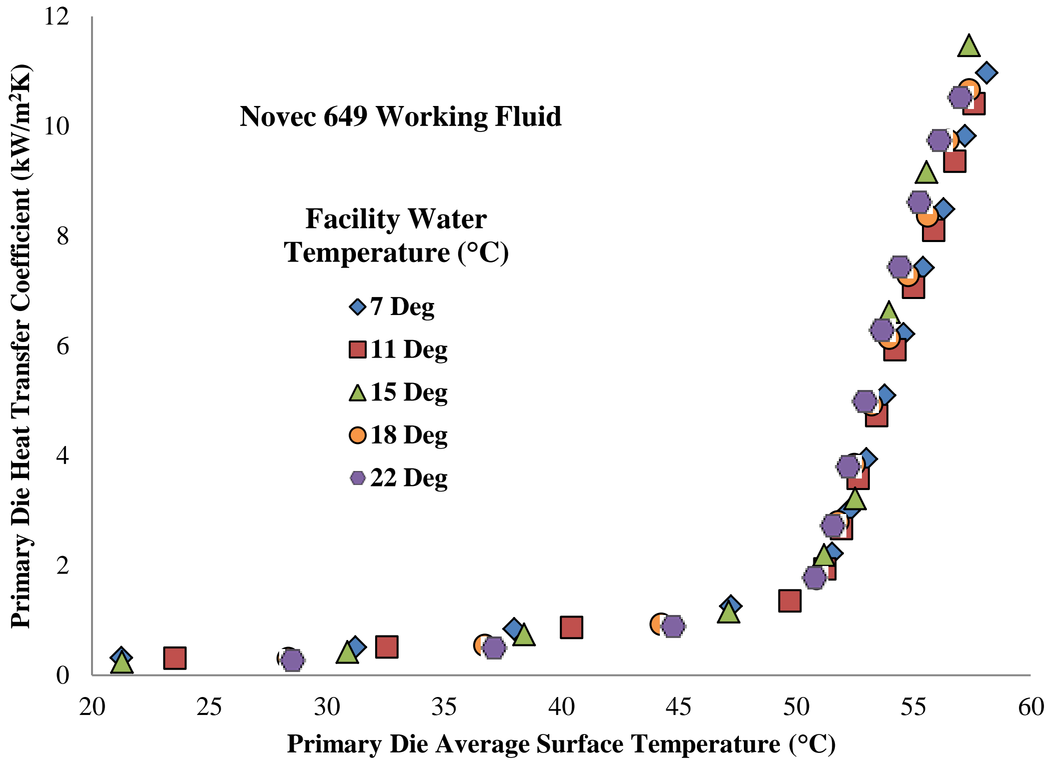


Figure 55 – Microporous HTC data over various facility water settings

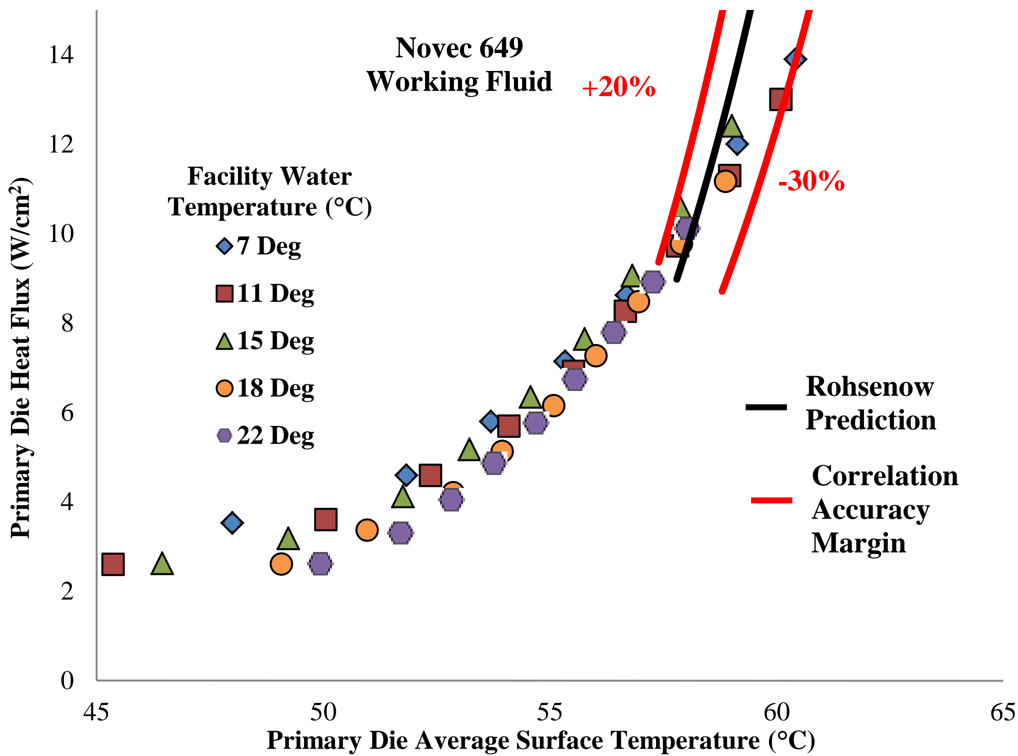


Figure 54 – Microfinned surface boiling curves over various facility water settings

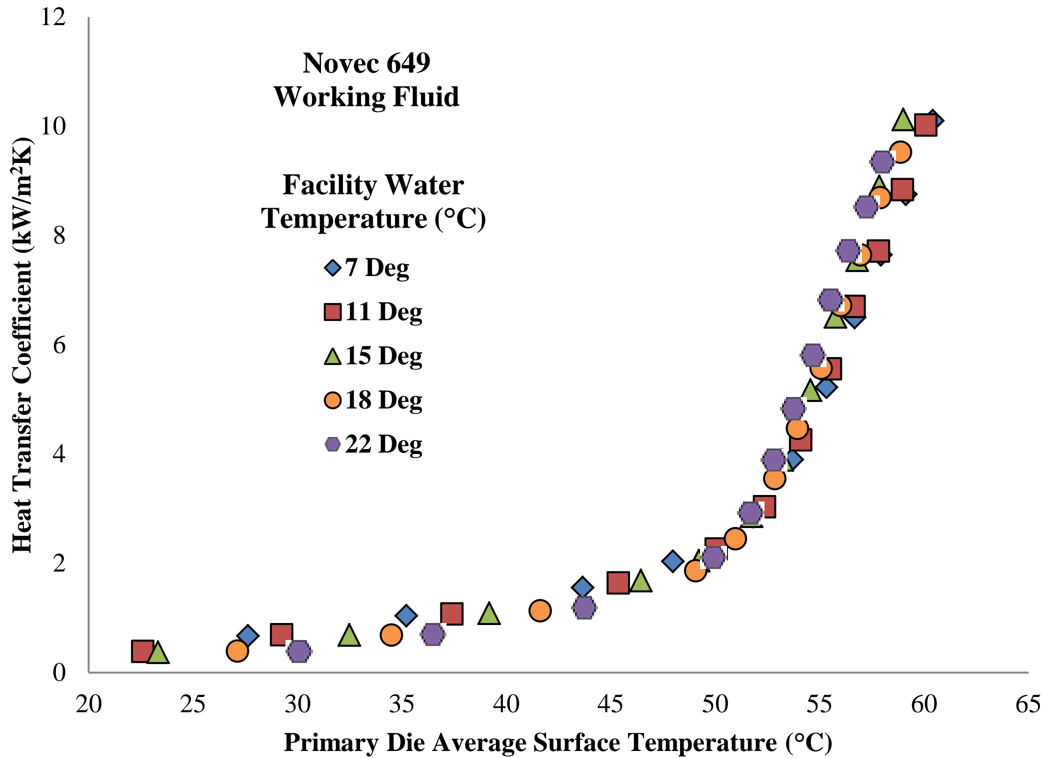


Figure 56 – Microfinned HTC data over various facility water settings

4.6 Condensive Limit Trends and Modelling Attempt

The concept of a condensive limit in an LFM was first introduced by Markowitz [55], and its implications and governing fundamentals are discussed in the Introduction of Condensation Limitations in Liquid Filled Modules section (Section 2.3). The same trends are evident for all of the pool conditions tested in the current study as shown by Figure 57. Further justification for the current design being condensive limited is provided when the maximum heat fluxes attained are compared to theoretical CHF expectations. CHF values of 15.4 W/cm^2 are calculated for FC-72 using the Zuber [46] or Kutateladze [45] equation, shown as Equation 8. An even higher value of 17.6 W/cm^2 is calculated using the modified coefficient form of the Zuber-Kutateladze equation from Lienhard-Dhir [48]. While these correlations are for horizontal surfaces, a CHF value of 16.24 W/cm^2 for FC-72 on a flat vertical surface has been experimentally documented by Howard and Mudawar [49]. These theoretical and experimental

values are slightly greater than the maximum heat fluxes shown on the plots in Figure 57 illustrating that the proposed design is condensation limited. The red dashed “Condensive Limit

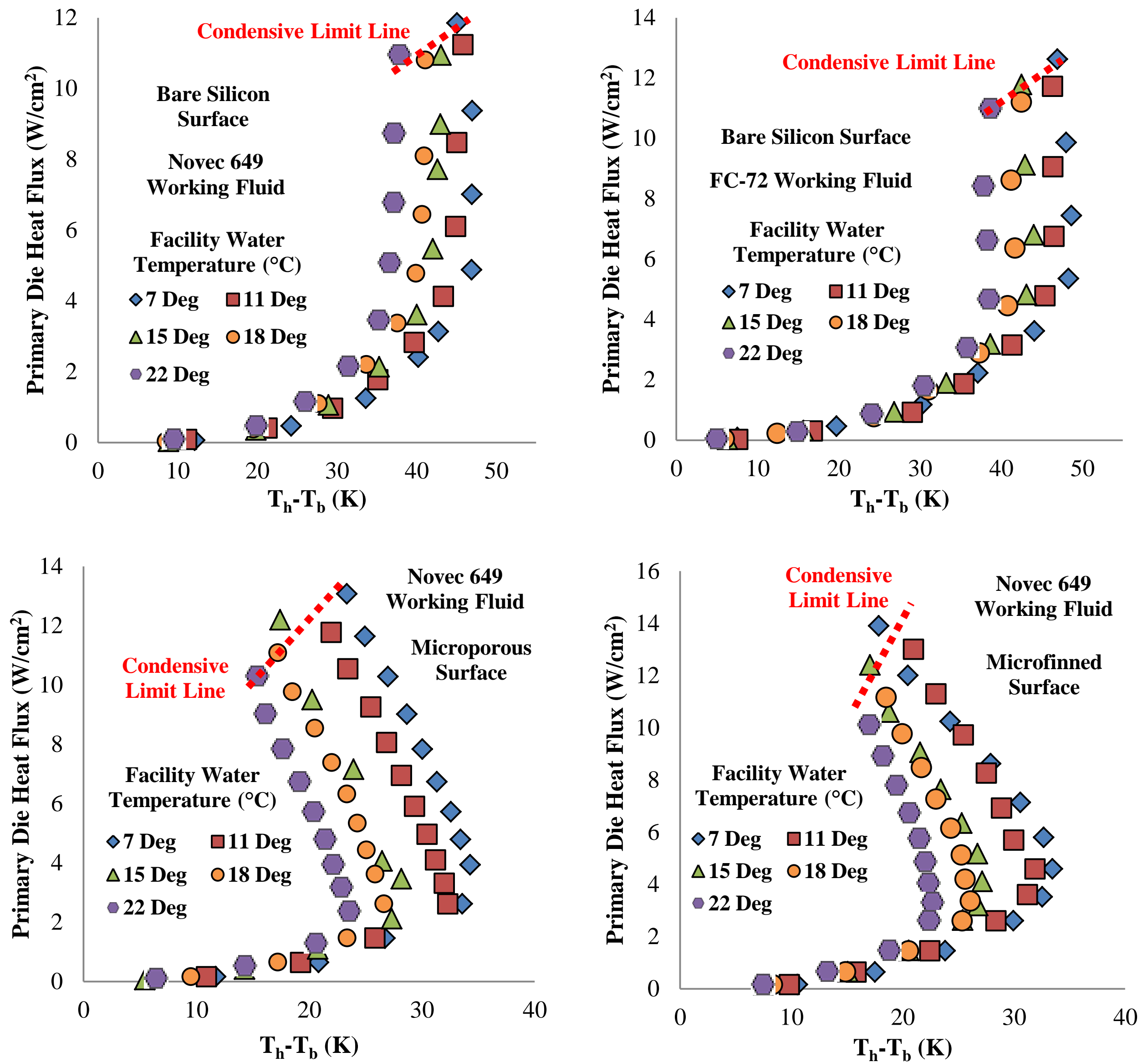


Figure 57 – Condensive limit appearance across all conducted pool tests

T_b is the internal vertically oriented condenser fain array base temperature

Line" is similar to the dashed limit line proposed by Markowitz and shown in Figure 19. Looking at the axes on Figure 19, Markowitz was able relate a heated surface to condenser plate base temperature, shown as T_c in the figure, superheat to the maximum heat flux attained. In his work, the condenser was a flat plate and thus the base temperature was measured readily by the strategic insertion of thermocouples along this condensive surface. Given the complexity of the current design meant to mimic a high performance liquid immersion cooled module, especially with the necessary confinement at the chilled water header location, such a straightforward condenser base temperature extraction method was not feasible. To overcome this issue, making use of the known dimensions of the internal header channels along with the properties and flow rate of the chilled water flowing through them, a developing flow

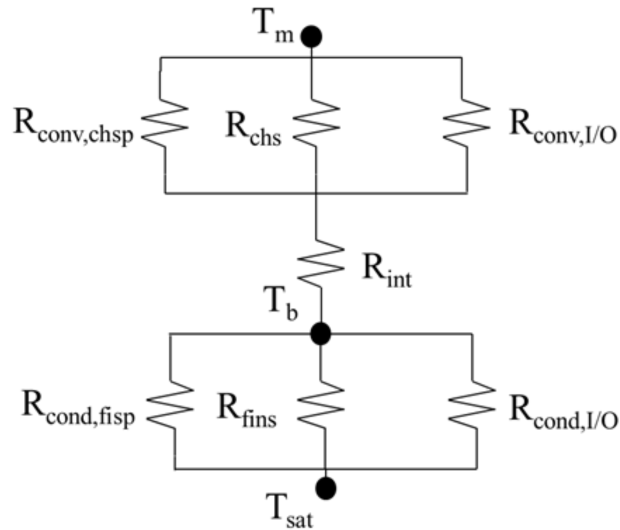


Figure 58 - Thermal resistance network for estimating the condenser base temperature

Table 5 – Summary of thermal resistances used for pool boiling condensive limit model

Resistance	Description	Reference
R_{chs}	Conduction through the plates (dividers) that make up the chilled water header channels	[104]
$R_{conv,chsp}$	Convection from the area between the plates (dividers)	[104]
$R_{conv,I/O}$	Convection from the area under the chilled water inlet and outlet ports	[104]
R_{int}	Conduction through the metal separating the external chilled water plates and the internal condenser	
R_{fisp}	Condensation from the horizontally flat area between the condenser fins	[105]
$R_{cond,I/O}$	Condensation from the horizontally flat area within the cartridge but underneath the chilled water inlet and outlet ports	[105]
R_{fins}	Condensation based upon a vertical flat plate correlation with modifications using the fin efficieny	[57]

heat transfer coefficient correlation along with the proposed thermal resistance model shown in Figure 58 can yield the important T_b value for establishment of true condensive limit trends in the current study using the same parameters Markowitz used. Table 5 is presented to offer details regarding each thermal resistance introduced in Figure 58.

The thermal resistance of the channel plates or dividers was considered as a set of long fins with an adiabatic tip considering that the tip is not in contact with the fluid but in contact with the relatively insulative gasket material. The convective conditions within the channels were slightly more difficult to determine considering that the flow is in the thermally developing regime and, due to the short length of the channels, has a very low Graetz number, on the order of 0.002. For this reason, the work of Lee and Garimella [101] was implemented to determine the average Nusselt number within the channel. The governing and supporting equations are all shown as Equation 15. This number is necessary not just for determining the convective thermal resistances within the header chamber but also each individual channel plate conductive thermal resistance since fin efficiency is tied to the convective conditions it senses. It is assumed that the

$$
\begin{gathered}
Nu_m = \frac{1}{C_1\left(x^*\right)^{C_2} + C_3} + C_4 \\
x^* = \frac{1}{Gz} \\
C_1 = -2.757\times10^{-3}\alpha^3 + 3.274\times10^{-2}\alpha^2 \\
-7.464\times10^{-5}\alpha + 4.476 \\
C_2 = 0.6391 \\
C_3 = 1.604\times10^{-4}\alpha^2 - 2.622\times10^{-3}\alpha - 2.568\times10^{-2} \\
C_4 = 7.301 - \frac{13.11}{\alpha} + \frac{15.19}{\alpha^2} - \frac{6.094}{\alpha^3} \\
\text{For: } 1 \le \alpha \le 10
\end{gathered} \tag{15}
$$

heat transfer coefficient obtained here can be applied to the area directly under the inlet and outlet ports to the chilled water header. With this assumption, and incorporating the convection from the area between the channels, the equivalent thermal resistance between the mean chilled water temperature flowing through the header, T_m, and that of the internal vapor space condenser base, T_b, can now be obtained. With this thermal resistance and sensible heat gain data extracted from the flow meter and thermocouples located in the chilled water header flow loop, T_b is calculated and incorporated into the data presented in Figure 57 for all pool boiling liquid/surface combinations tested.

Assuming negligible losses through the exterior walls of the cartridge, the fundamental expectation is that all of the heat applied to the primary die should be captured by the chilled water header in a pool boiling scenario. This however is not the case considering that the cartridge walls and the chilled water header cover are both made of very thermally conductive aluminum. There is a 1/8" thick EPDM gasket, relatively insulating when compared to aluminum, between the header block and the channels which is used to seal the coolant, but conduction through the highly thermally conductive aluminum header cover cannot be completely ignored. With this in mind, the sensible heat gained by the coolant flowing through the chilled water header for the pool boiling scenario with the microporous test surface used is presented as Figure 59. The right axis shows the amount of heat captured by the fluid flowing through the chilled water header, while the left axis shows the ratio of the heat captured by the chilled water header over the amount of power applied to the primary die. As stated in the Electronics Cartridge Design Motivations and Construction section (Section 3.1), the coolant used in an 80/20 mixture by volume of Dowtherm SR-1 and deionized water. The properties used to calculate the sensible heat gained were taken from vendor provided data at the mean

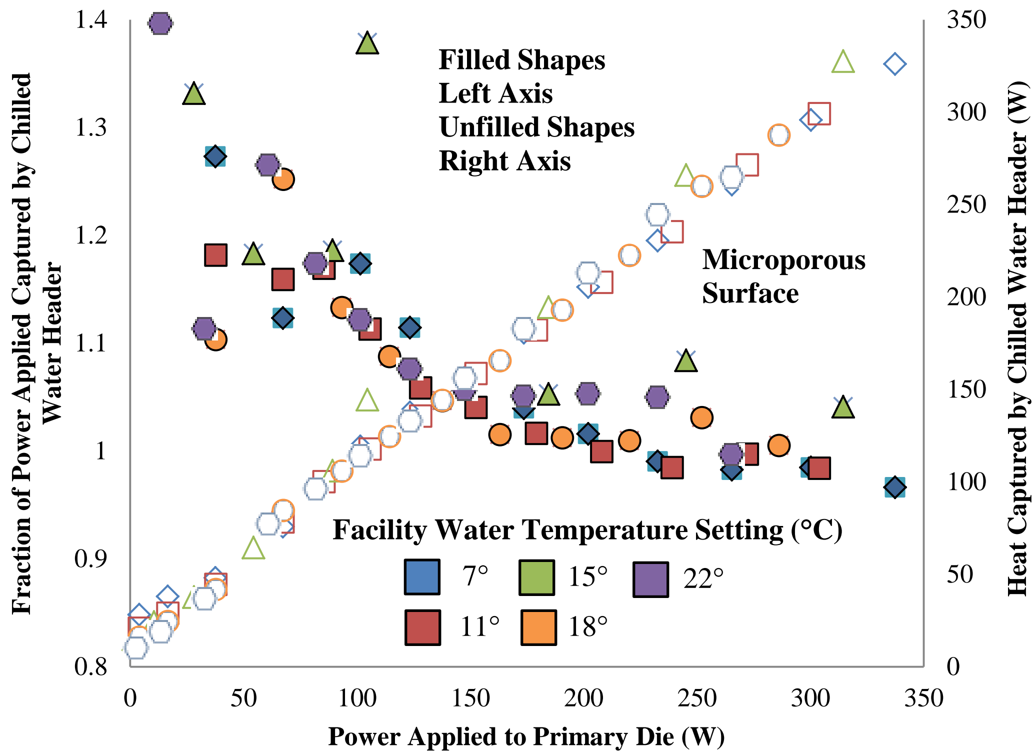


Figure 59 – Sensible heat gained by the chilled water header under pool conditions

temperature of the fluid flowing through the channels at this mixture ratio [102]. The plot initially trends towards an asymptote on the left axis because the denominator of the ratio is tending towards zero watts of power applied to the primary die, while there will always be some sensible heat gain across the header due to the temperature difference between itself and the laboratory ambient environment. The convergence of all the ratio data across the facility water temperatures tested to a value near one is an artifact of the pool temperatures converging on a similar value across the facility water temperature settings as shown in right plot of Figure 52 corresponding to the test condition shown in Figure 59. With this settling upon a constant temperature in the pool, the heat losses through the walls are consistent across the facility water temperature settings as the temperature difference driving natural convection at the wall to laboratory ambient environment interface is now constant.

The theoretical limit for the amount of heat that can be extracted from the vapor space condenser fins and surrounding areas can be obtained by assuming laminar film condensation on these surfaces. The heat transfer from the area between the fins, associated with $R_{cond,fisp}$, and the flat area within the cartridge but under the inlet and outlet ports of the chilled water header, associated with $R_{cond,I/O}$, can be estimated by the correlation proposed by Gerstman and Griffith [103] associated with laminar film condensation from a downward facing horizontal flat plate shown as Equation 16 while h'_{lv} can be calculated using Equation 10.

$$h = k_l \left(\frac{g(\rho_l - \rho_v)}{\sigma} \right)^{0.5} (0.26) \left[\frac{g\rho_l(\rho_l - \rho_v) h'_{lv}}{k_l \mu_l (T_{sat} - T_b)} \left(\frac{\sigma}{g(\rho_l - \rho_v)} \right)^{1.5} \right]^{0.25} \tag{16}$$

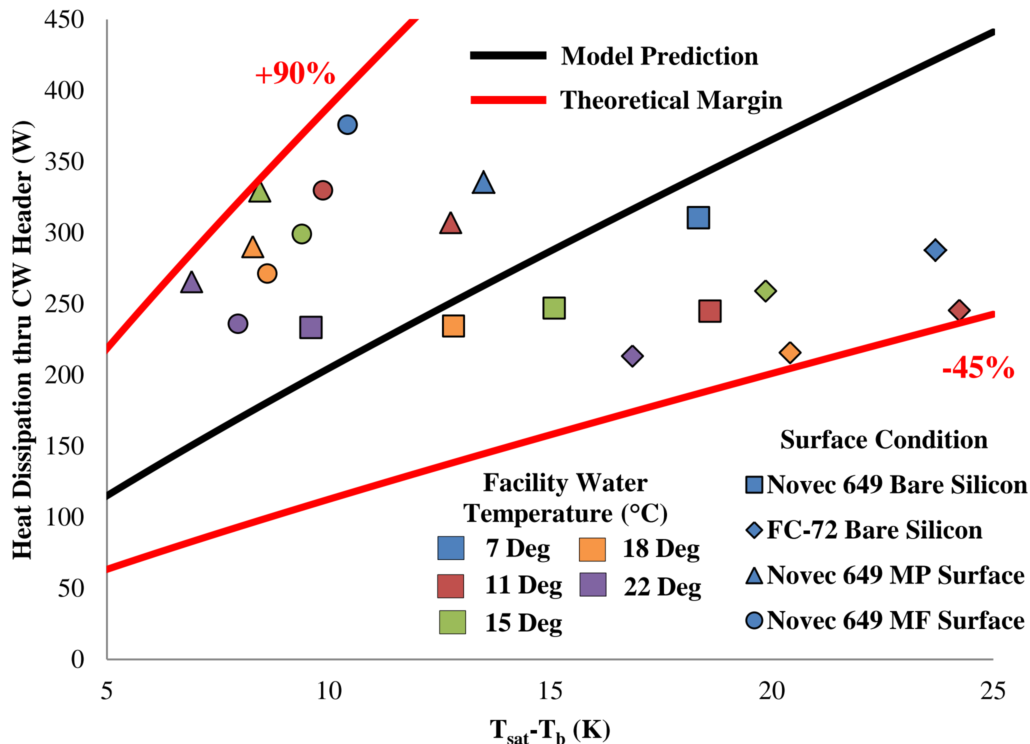


Figure 60 – Actual CW header heat gain versus theoretical condensive limit expectations

The condensation limit of the vertically oriented pin fin array in the vapor space can be calculated using the proposed method by Iyengar [56] introduced and discussed in the Introduction of Condensation Limitations in Liquid Filled Modules section (Section 2.3). The governing equations of his approach are shown as Equation 9, Equation 10 and Equation 11. This method captures the fin efficiency associated with the changing surface temperature along the length of the fin as well as assumes an adiabatic tip. The latter condition is particularly appropriate for the current study as the condenser fin tips are immersed in the relatively insulative dielectric fluid when compared to the high heat transfer coefficients achieved during condensation heat transfer. The pool fill line begins at the tip of the pin fins in the vapor space but, due to the thermal expansion of the liquid brought about by the rise in pool temperature to saturated conditions, immerses slightly more of the fins throughout the experimental run as heat flux of the primary die is increased. With the top portion of the thermal resistance network in Figure 58 used to acquire T_b along with the power dissipated through the chilled water header determined experimentally, these condensation heat transfer equations can be plotted against (T_{sat}-T_b) to model the power that should be dissipated through the chilled water header for comparison. The results of the experimentally achieved maximum power dissipations through the header are compared to this proposed model in Figure 60. The theoretical margin lines shown on Figure 60 represent the percentage increase or decrease of the predicted heat dissipation, determined by the proposed model, through the chilled water header for a given driving temperature difference between the condenser base and the average of the values recorded at the primary die. Shapes on the plot represent the fluid/surface combination tested while the facility water temperature setting is color coded.

Only one theoretical line is presented on Figure 60 even though two fluids are studied which have slightly different properties. The line presented represents an average of the theoretical lines yielded by the model where the saturated properties of both working fluids are incorporated separately. The properties used in the model were shown earlier in Table 3. The properties governing the condensation heat transfer equations used in the model between the two fluids are not that different. In fact, a comparison of the two theoretical lines yielded only 0.1% - 0.2% difference in results along all the driving temperature differences investigated. The primary property that is different between the two fluids, namely saturation temperature, just

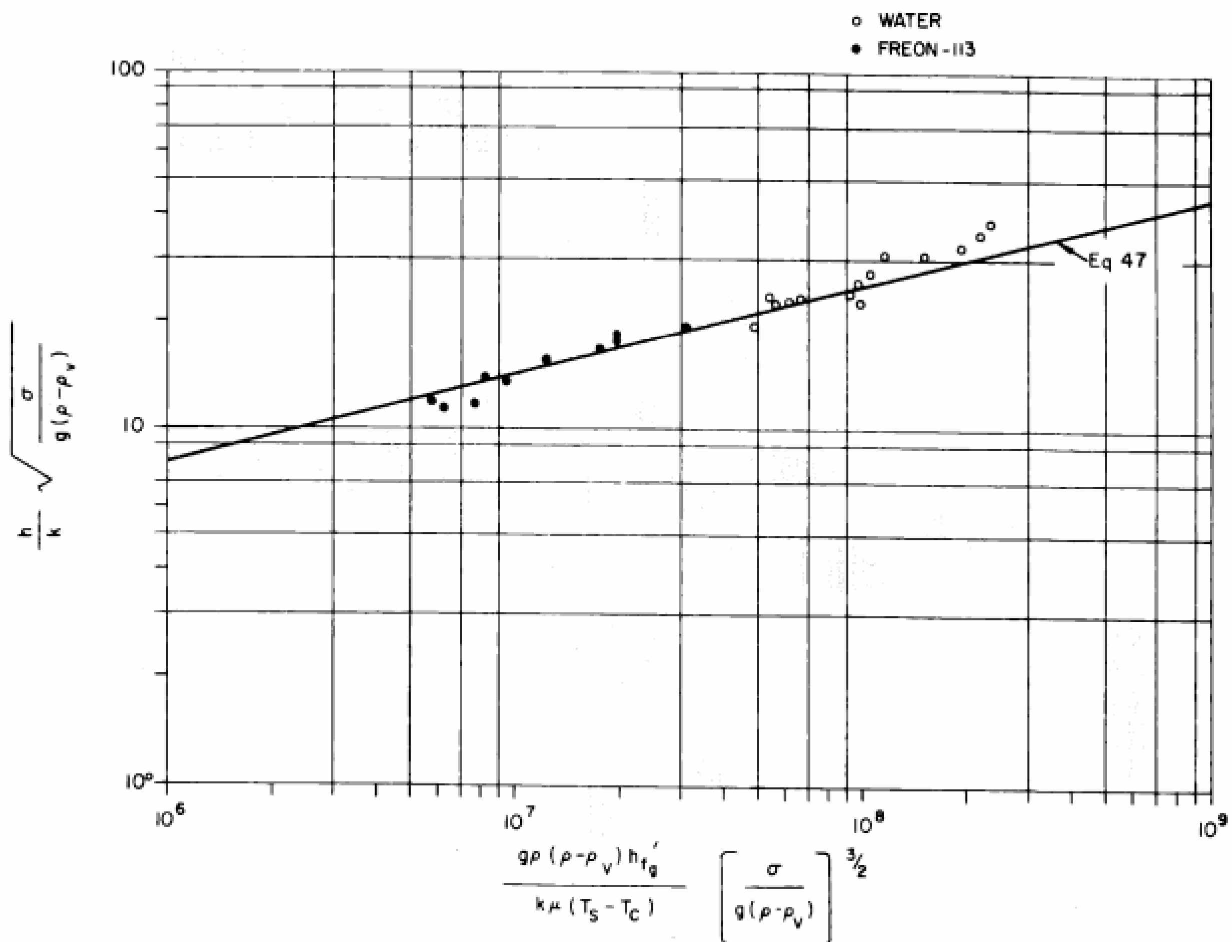


Figure 61 – Single theoretical condensive limit line for two different working fluids [55]

happens to be captured in the dependent variable of the model and throughout the condensation equations used, specifically in the form of T_{sat}-T_b. The similarity of the theoretical line between two different working fluids is also consistent with the work of Markowitz as he presented a single line to capture the condensation limits expected on the horizontal condenser plate used with both Freon-113 and water as the working fluids. For further justification of the single theoretical line approach proposed in the current study, the theoretical line presented by Markowitz to capture the condensive limit expectations for both water and Freon-113 is presented as Figure 61. The axes on Figure 61 is the Gerstman and Griffith equation, shown as Equation 16, split to include terms associated with the heat transfer coefficient on the y-axis and terms associated with the driving temperature difference ($T_{sat} – T_b$) on the x-axis.

While the comparison of the experimental results and the theoretical model presented in Figure 60 show some substantial deviations indicated by the theoretical margins on the plot, there are some important conclusions that can be drawn along with motivation for future work to enhance the accuracy of the model. It appears that for the bare silicon surface and both fluid combinations, the model is reasonably effective given the number of assumptions made as well as the general acceptance that accuracy between ±40% is the norm for many two-phase theoretical models. It is interesting that Novec 649 seems to fall closer to the theoretical prediction than the same surface performance with FC-72 as the working fluid. Given that the saturation temperature of Novec 649 is 49°C while that of FC-72 is 56°C, there is the possibility that the thermal expansion of the latter fluid beyond what would take place with the former fluid may have an effect on the vapor space condenser performance, specifically at the highest heat fluxes recorded. Given the initial low fluid inventory contained with the cartridge under pool boiling conditions, falling just below the bottom tips of the condenser pin fins, the rise from

initial pool temperatures to final saturation conditions for FC-72 results in only a few millimeters of liquid fill level increase, representing only about 10% of the entire pin fin length. To address this, the model was adjusted to account for the thermal expansion of the contained fluid from initial conditions to final saturation conditions, essentially adding to the insulated region of the pin fins in the model as the liquid fill level line rose. This new model only adjusted the values of the previously un-modified model for FC-72 by 0.7%-1.7% over all the driving temperature differences examined. This is not enough on its own to account for the deviations of the FC-72 data from the theoretical model presented in Figure 60. The rise in the liquid level line may be secondary to the omission of sloshing in the current model. As noted by Markowitz and illustrated by the effect of angling the LFM as shown by the plot in Figure 20, essentially creating contact with the liquid-vapor interface and the condenser plate, there is some element of transient condensation occurring when the liquid cleans the condensive surface through the relative volatility of boiling occurring within the cartridge. Where this effect is most evident is the model's severe under-prediction of condensive limits associated with the boiling enhancement surfaces used. The primary advantage of using these surfaces is the increase in boiling activity and thus the resulting increase in activity at the vapor space condenser as the liquid-vapor interface sloshes within the cartridge assembly. Adding the effect of cleaning the condensive surface through sloshing along with how well the condensate film forms during the little time it has before being wiped clean again are the two elements that would add further quality to the proposed model. One of the ways in which this could be done is characterizing the amount of vapor being generated at the heated surface. As will be discussed in the Two-Phase Pool Boiling PIV Visualization and Analysis section (Section 4.9), this technique offers a great opportunity to capture this parameter for inclusion in the model.

4.7 Module Level Thermal Resistance Plateaus

The point at which these experiments were stopped, and thus the maximum power dissipations and heat fluxes reported, are somewhat qualitative in nature as they represent the point at which the author deemed the system to be near a catastrophic burnout event. As mentioned in the Boiling Heat Transfer Historical Studies section (Section 2.2), the materials used to construct the test vehicle, specifically the solder and underfill, could not withstand the massive temperature jump associated with a burnout event. The system could not be allowed to go to this event consistently as doing so would endanger the test board's preservation for all of the pool and flow boiling testing slated to be conducted. With that being said, the consistent appearance of a condensive limit across all of the pool testing conducted lends credence to the author's insight regarding the conditions surrounding the burnout event. Additional support for the stopping point criteria is the consistent module level thermal resistance plateau that each surface/fluid combination yielded in pool boiling across all of the facility water temperatures tested. The module level thermal resistance is calculated by using the measured heater surface and mean chilled water fluid temperatures as the driving temperature difference along with the measured power applied to the primary die within the cartridge assembly as the denominator in this ratio. In each of the four figures (Figure 62, Figure 62, Figure 63, Figure 64) the macro scale view of the levelling trend is displayed to the left, but in order to get a better sense of the final value and convergence of the data across all of the facility water temperatures tested, a certain portion of the plot to the left has been enlarged on the right. The average final value for all of these fluid/surface combinations is highlighted on the zoomed-in plot presented.

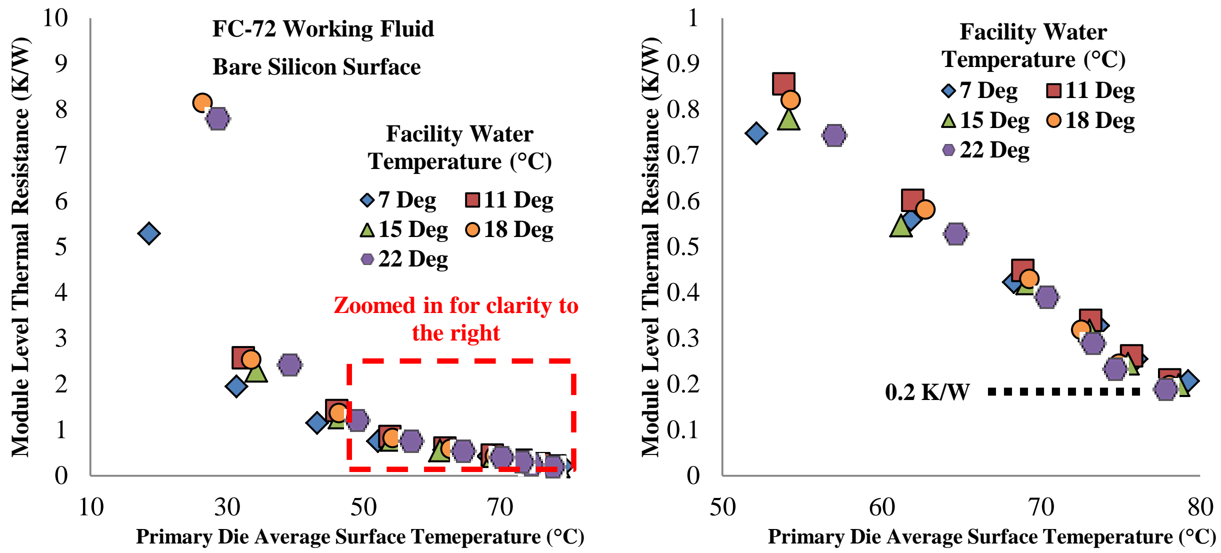


Figure 62 – FC-72 module level thermal resistance results for the bare silicon surface

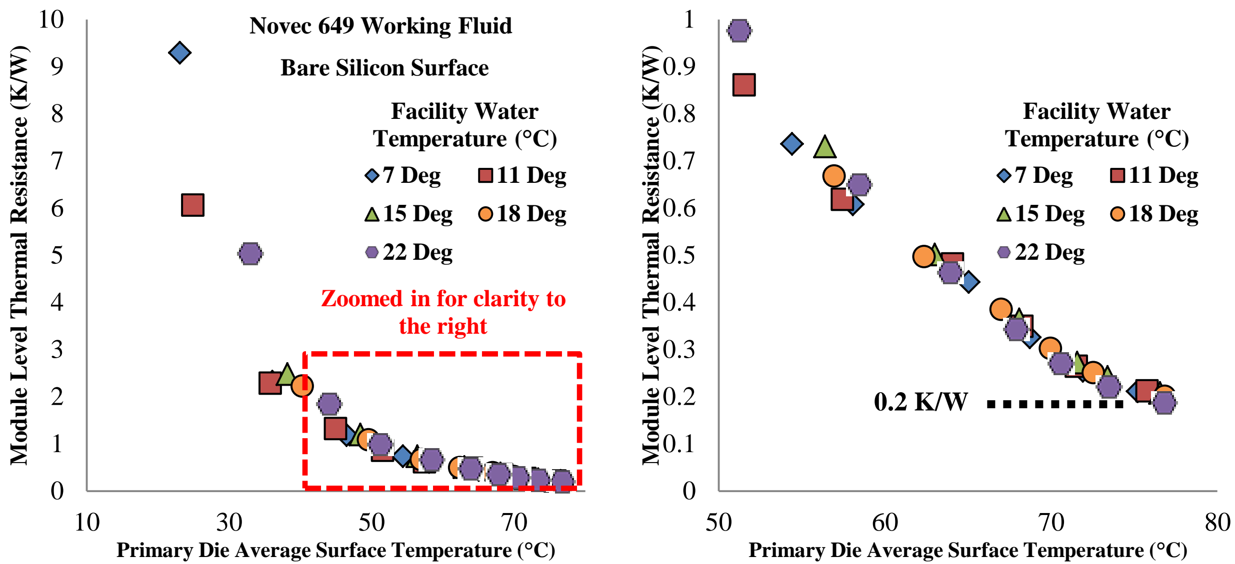


Figure 63 – Novec 649 module level thermal resistance results for the bare silicon surface

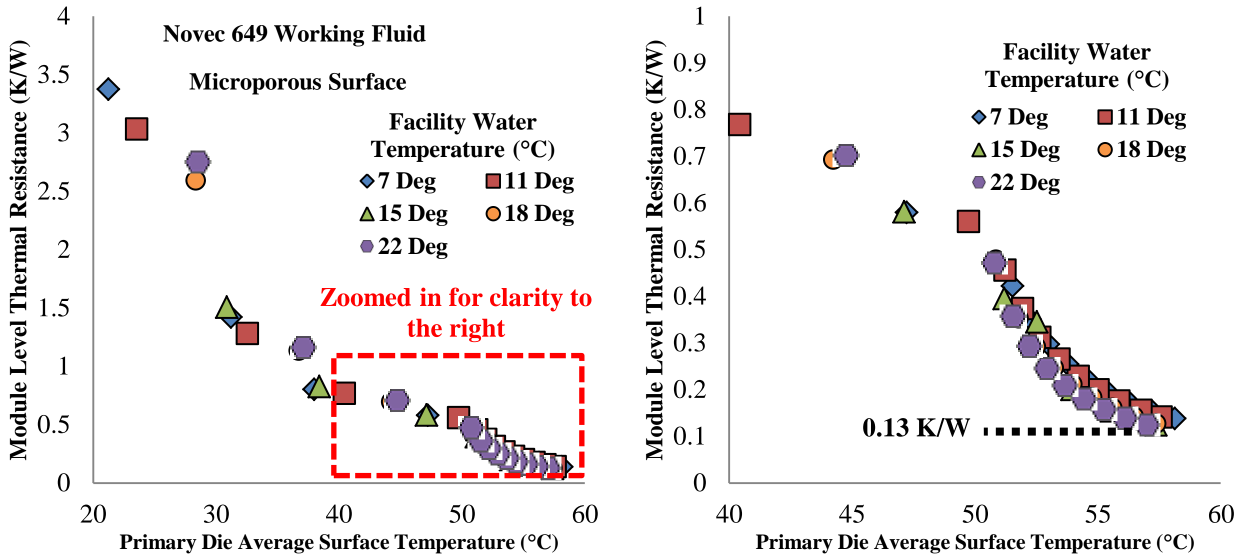


Figure 64 – Novec 649 module level thermal resistance results for the microporous surface

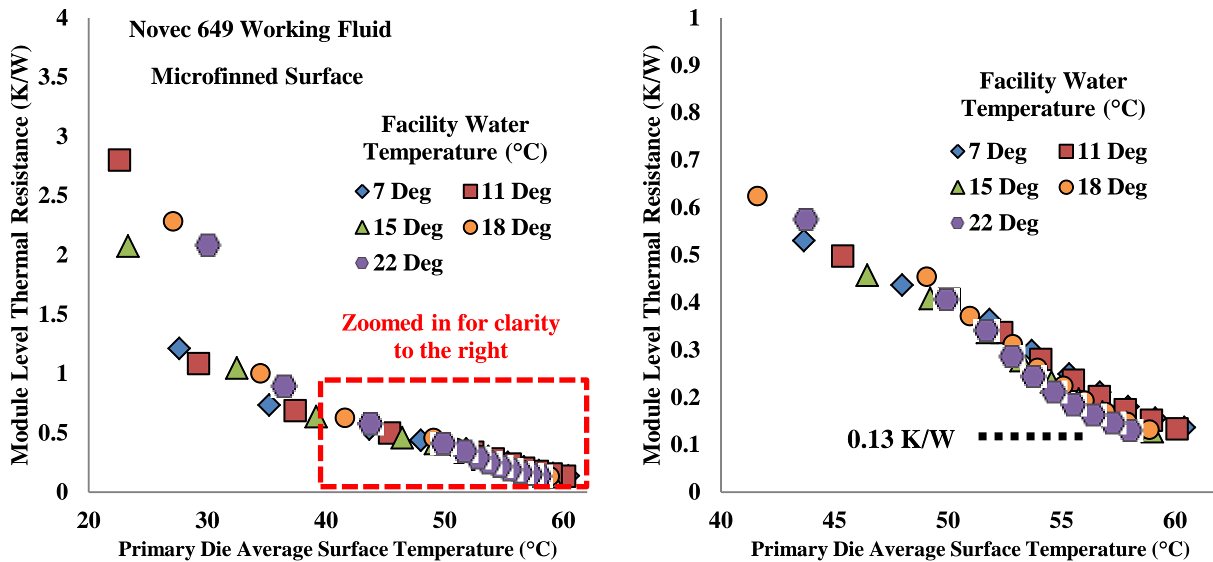


Figure 65 – Novec 649 module level thermal resistance results for the microfinned surface

With the little variation of the module level thermal resistance over the facility water temperatures tested for each fluid/surface combination, some interesting conclusions can be drawn when the results are isolated to the 7°C facility water temperature setting over all the combinations tested as shown in Figure 66. Comparing the working fluid performance, the similar final thermal resistance occurring at a slightly lower operating temperature for the Novec 649 versus that of FC-72 for the bare die scenario is an artifact of the lower saturation temperature for the former fluid. This merger in final thermal resistance performance is also supported by the reduced power dissipation benefit as the operating temperature is increased for Novec 649 versus FC-72. This point is illustrated by the Fluid Boiling Enhancement Factor results of Figure 44. The value of 0.2 K/W that both working fluids converged upon for the bare die scenario closely match the value yielded by the LFM proposed by Markowitz [55] adding credence to the design of the current experimental facility as well as the additional analysis conducted. Further support of the module level thermal resistance model, illustrated by Figure

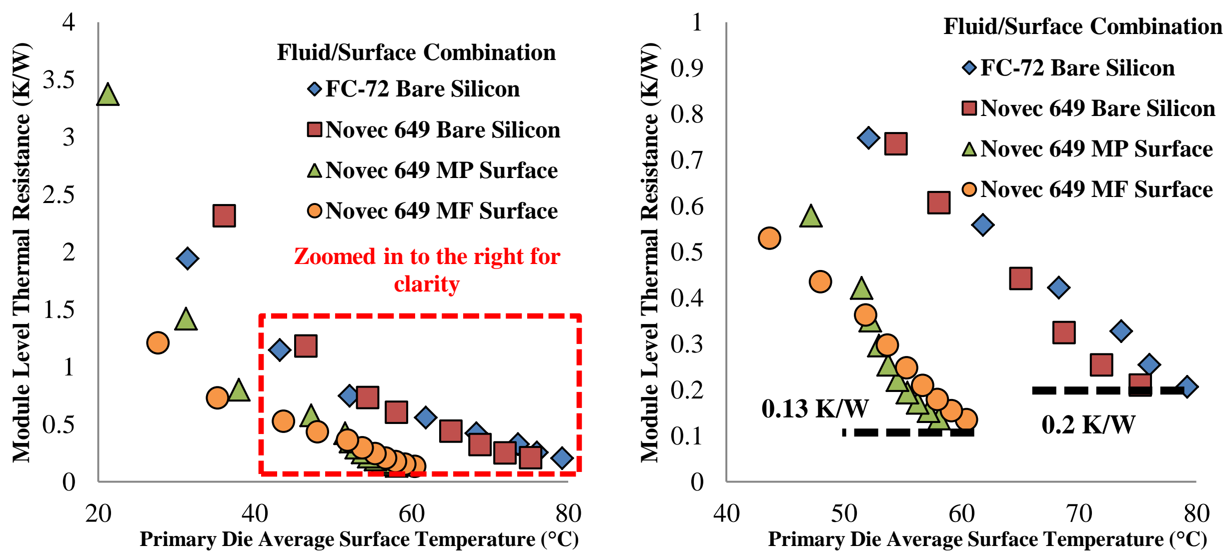


Figure 66 – Final module level thermal resistance comparison with 7°C Facility Water Temperature Setting

58, is attained when the final thermal resistances between both surfaces are compared. Using the maximum heat transfer coefficient data presented in Figure 51 and subtracting the convective heat transfer resistances yielded from those values results in a difference of roughly 0.08 K/W. The details behind this conclusion can be found in the calculations done below. This is roughly the difference between the final module level thermal resistances presented between both surfaces on Figure 66. The module level thermal resistance data not only provides a means by which to estimate the performance of the cartridge assembly at any given temperature, but highlights important trends and substantiates connections within a lot of the theory and fundamentals driving the performance in other aspects of the design.

Microporous heat transfer coefficient from Figure 51: 11.5 kW/(m^2*K)
Microfinned heat transfer coefficient from Figure 51: 10.1 kW/(m^2*K)
Bare Silicon heat transfer coefficient from Figure 52: 3.5 kW/(m^2*K)
4 square inches of total heated area = 2.58 x 10^{-3} m^2

$$R_{conv} = \frac{1}{h * A}$$

Convective Resistance difference between microporous and bare silicon:

$$\Delta R_{conv} = \frac{1}{3.5\ x\ 10^3 \frac{W}{m^2 * K} * 2.58\ x\ 10^{-3}\ m^2} - \frac{1}{11.5\ x\ 10^3 \frac{W}{m^2 * K} * 2.58\ x\ 10^{-3}\ m^2}$$

$\Delta R_{conv} = 0.08$ K/W

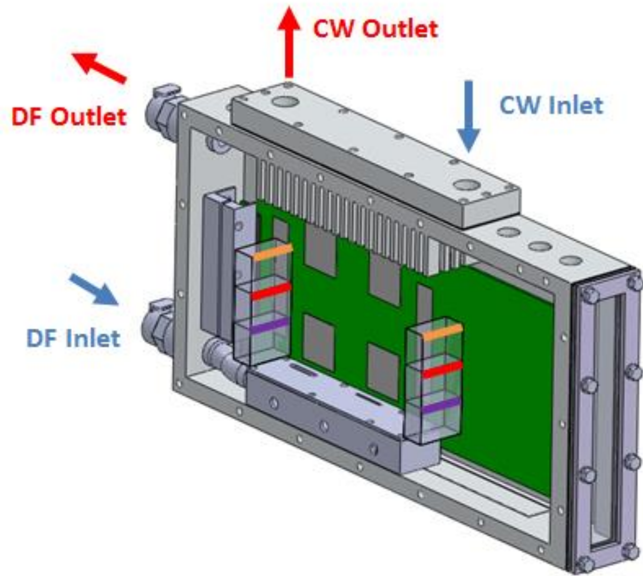
Convective Resistance difference between microfinned and bare silicon:

$$\Delta R_{conv} = \frac{1}{3.5\ x\ 10^3 \frac{W}{m^2 * K} * 2.58\ x\ 10^{-3}\ m^2} - \frac{1}{10.1\ x\ 10^3 \frac{W}{m^2 * K} * 2.58\ x\ 10^{-3}\ m^2}$$

$\Delta R_{conv} = 0.07$ K/W

4.8 Passive Element Integration Effects

It is understood that there are other elements on a circuit board within a conventional server assembly that may impede or hinder thermal performance of the more important processor units. In an effort to determine when these passive elements, such as DIMM's, may begin to have an impact on the thermal performance of these primary components, flow guides meant to simulate these devices have been constructed and integrated into the design. The location of these elements within the cartridge assembly as well as their relative heights is presented in Figure 68. Even though the Dielectric Fluid (DF) inlet and outlet are noted on this illustration, they are not used in the pool boiling scenario. These are indicated on the illustration for future reference when the implementation of these flow guides is



Color Indicator	Flow Guide Height	
ORANGE	57.2 mm	2.25”
RED	38.1 mm	1.50”
PURPLE	19.1 mm	0.75”

Figure 68 – Passive Element Integration Details

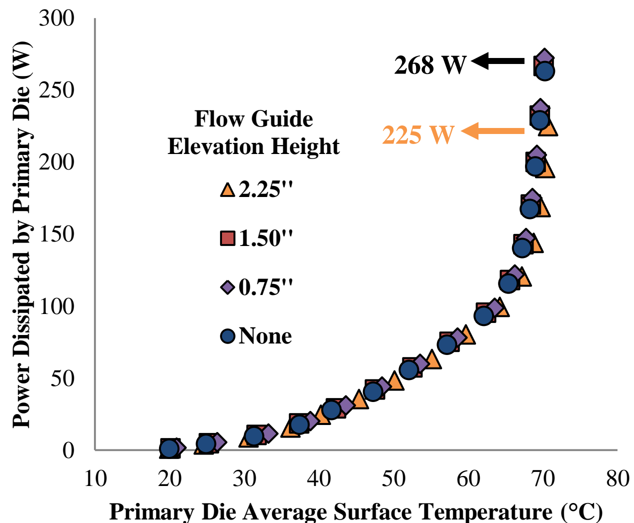


Figure 67 – Maximum flow guide impact on peak thermal performance

explored from a flow boiling performance standpoint. From drawing number AUB-100000 in Appendix I, the internal dimensions of the cartridge are 10.93” x 5.15” x 1.37” (278 mm x 131 mm x 35 mm), L x H x W. Through pool boiling testing over these various flow guides with a 15°C facility water temperature setting, a power dissipation versus the average bare silicon die surface temperature plot, shown as Figure 67, indicates that not until the largest flow guide is implemented is there a significant impact to the thermal performance of the primary elements. This conclusion is significant for the packaging engineer as it implies that roughly half of the periphery surrounding core processing elements can be obstructed in some fashion without endangering the main function of the system with the use of a two-phase liquid immersion cooled thermal management solution. Qualitatively speaking, the boiling became much more vigorous at a lower power dissipation in a strangely instantaneous fashion with the maximum obstruction integrated. It is unclear as to what the fundamentals are that were driving this phenomenon but module level thermal resistance plots support this qualitative claim in the

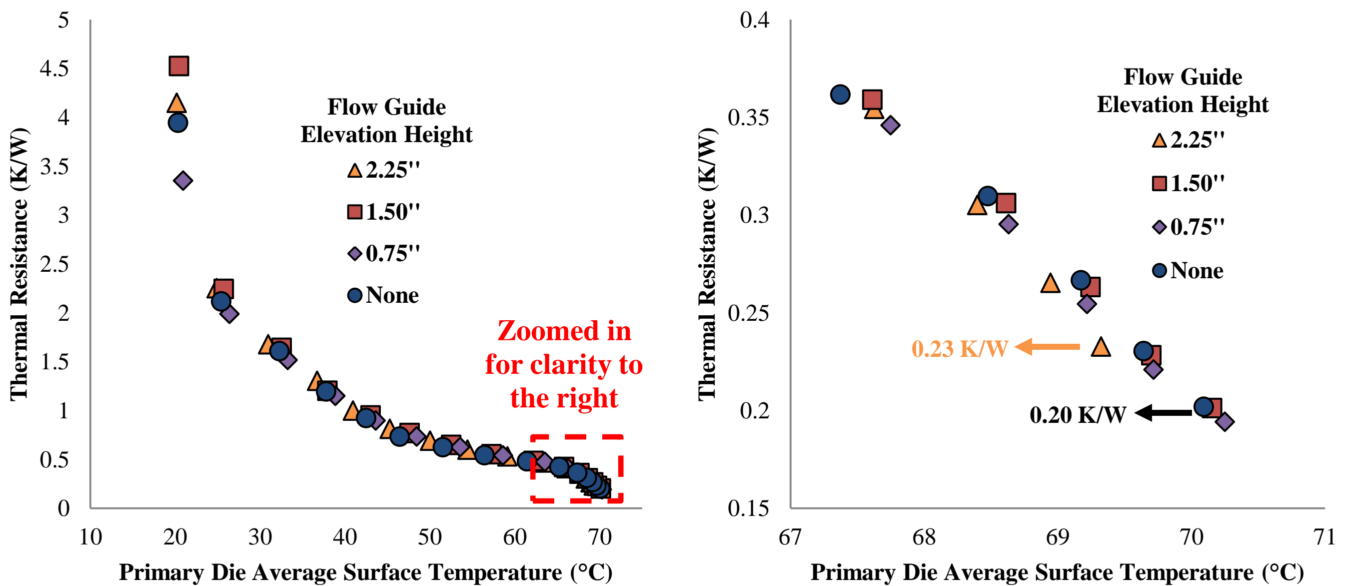


Figure 69 – Module level thermal resistance performance across the various flow guides integrated

deviation shown on the zoomed in right image of Figure 69. Even with this deviation, the final module level thermal resistance for all of the other flow guides implemented settles on the same 0.2 K/W bare silicon die value presented in Figure 62 and Figure 63 for both working fluids. This shows that while care must be taken into implementing passive elements into a two-phase thermal management solution like that proposed in the current study, it takes a significant amount of enclosure around the primary heated elements to impact their performance significantly. This point is very important for the packaging engineer as the functional requirements of these systems, and thus component density, will rise as the realization is made that two-phase thermal management solutions can handle significantly high volumetric power dissipations. The data presented by the integration of these flow guides lends further support to the fact that this thermal management solution is equipped to address the consumer demands for higher performance in tighter confines in the years to come.

4.9 Two-Phase PIV Visualizations and Analysis

Critical to the characterization of a cooling system's performance is a working understanding of how coolant is distributed while it is in operation. Even in current air and liquid cooled systems there has been a tremendous amount of work done to understand this important dynamic as discussed in the Coolant Flow Modelling and Visualization Techniques section (Section 2.7). Therefore, it is important to introduce an experimental technique that can capture coolant distribution and practically characterize its performance for two-phase liquid immersion cooled solutions. Currently, to the author's knowledge, this work in the two-phase of dielectric fluid flow has not been conducted primarily due to what was the lack of a suitably density-matched fluorescent particle for seeding in the fluid. If this technology is going to make significant inroads in the thermal management community for high performance server cooling

applications, fundamental questions regarding how boiling surfaces will be quenched in a practical application are sure to arise. Hopefully, this two-phase work can provide some insight into how these questions can be addressed in the near future.

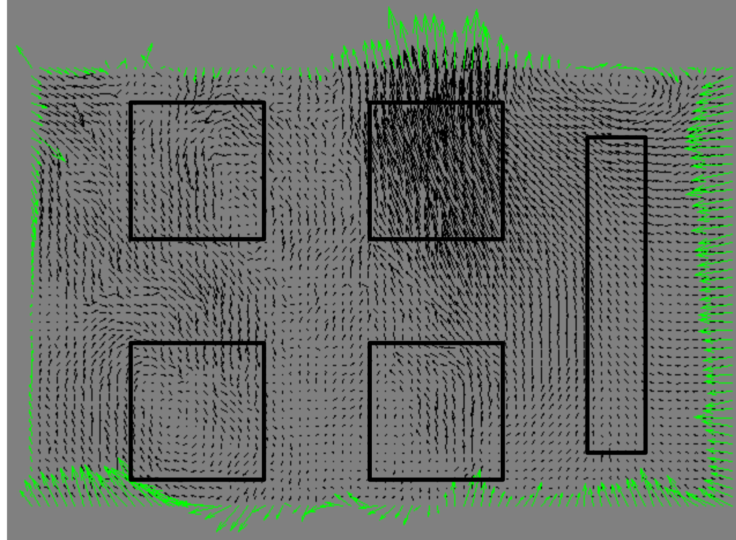


Figure 70 – Vectors highlighted for two-phase PIV analysis

Details regarding particle selection, associated slip velocities, laser/camera setup and orientation as well as the algorithm used to generate the vector sets for analysis are discussed in the PIV Setup and Execution section (Section 3.4). The following will focus on how the vectors are analyzed in the two-phase pool boiling scenario to extract useful data regarding the system's performance. One of the fundamental questions that PIV can help to answer is how much coolant is flowing to the primary heated elements. The first step is to highlight the vectors around the periphery of the resulting maps for incorporation into a control surface analysis. An image showing a sample set of these highlighted vectors is provided as Figure 70.

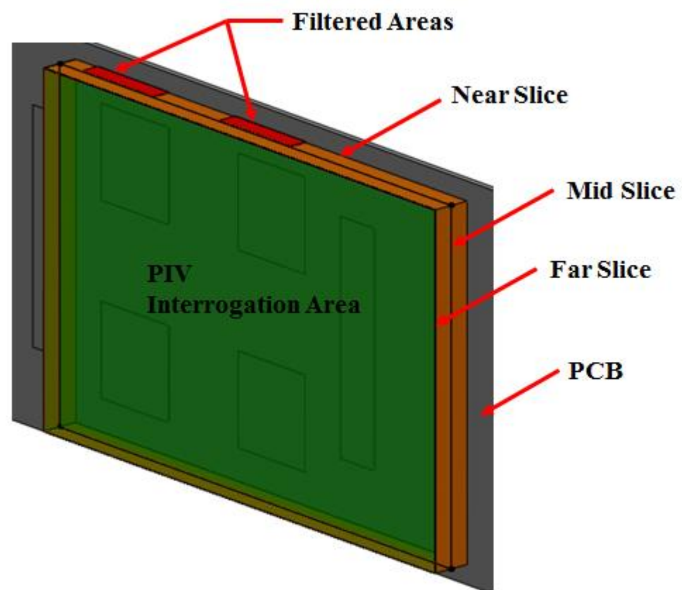


Figure 71 – Control surface definition for two-phase PIV analysis

Vector maps like those shown by Figure 70 are taken at three slices at locations normal to the primary heated elements. The first slice is taken as close as possible to the bare silicon die so as to not obstruct the laser sheet with their height. The second slice is taken 5 mm away from the first and the last is taken 5 mm away from the previous. The near and the middle slice vectors are averaged, and the middle and the far slice vectors are averaged. By then taking the normal component of these highlighted vectors from the pair of resulting averaged maps to the control surface defined by Figure 71, a liquid mass flow rate into the area surrounding the primary elements can be acquired. This liquid mass flow that is shown to be entering the control surface analyzed is either converted into vapor or is accounted for when the vectors facing away from the heated elements are captured, turning the control surface analysis into a true control volume analysis. Further details regarding the latter point specifically will be provided later in this section. One important point, and certainly a candidate for future work, must be made regarding Figure 71. When a raw image map like that presented in Figure 36 indicates that there are no particles in an interrogation window, the algorithm cannot discern whether this is simply a poorly seeded area or vapor. Therefore, some insight into which periphery vectors generated from the analysis fall within a vapor region must be included in the analysis. In the range of power dissipations tested, the filtered area shown on Figure 71 was deemed a suitable assumption for the area which is taken up completely by generated vapor. These vectors were then excluded from the incoming liquid mass flow rate analysis. The resulting net liquid mass flow rate from the control surface analysis is plotted against the power dissipation applied to the primary die in Figure 72. Fundamentally, the plot shows an increase in the amount of quenching fluid to the primary die as power input driving boiling to the primary die is increased. It is expected that this increase would be slightly more linear, but the middle portion that appears

more level is more than likely an artifact of the assumed filtered area in the control surface analysis. At lower power dissipations and with less boiling taking place, the surface area at the top occupied by vapor will be less. Therefore, the algorithm's filter should be adjusted slightly based on the input power. An excellent way to determine an input curve to this filtered area would

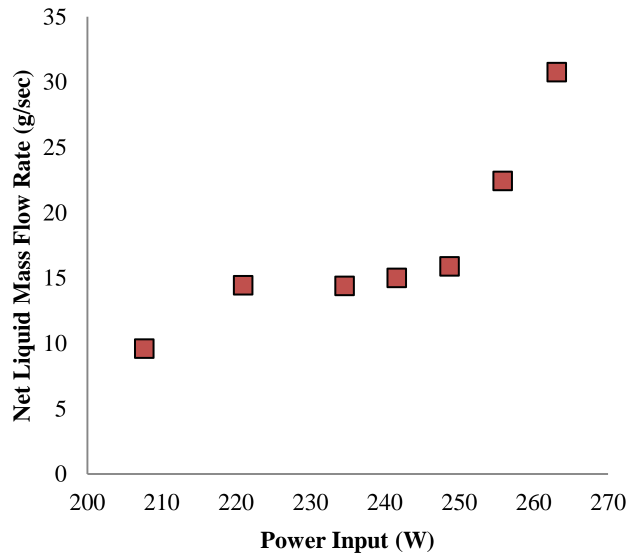


Figure 72 – Quenching fluid mass flow rate variation as a function of input power

be to use a fluorescent die throughout the entire volume of fluid. Once illuminated by a laser, the phases can be separated and measured at various power dissipations. The results from this effort could be applied to the filter definition for higher accuracy and potentially result in a more expected trend with the results shown in Figure 72. With that being said it is reassuring that the expected increase versus power dissipation is evident in the results.

Another issue that is evident with the data is that a simple latent heat of vaporization calculation of the incoming liquid mass flow rate yields a power dissipation that exceeds the power being applied to the die. For example, at the highest power dissipation, the liquid mass flow rate multiplied by Novec 649's saturated liquid heat of vaporization comes out to be 2.7 kW, an order of magnitude higher than the 263 W of input power measured. The limitation of the proposed analysis is that it is only a control surface analysis and not a true control volume analysis. Due to an inability to get acceptable images with the laser/camera setup oriented perpendicularly to the current scenario, the vectors pointing away from the heated elements were

not attainable. Future work could include getting this outward-facing vector set and closing the control volume around the heated elements for a better measurement of the quenching fluid being supplied to the boiling elements. Due to the principle of continuity, the less dense vapor being generated at the boiling surface should push liquid away from the board. Therefore, it is expected that when these outward-facing vectors are yielded, a net liquid mass flow rate out of the front face of the control volume will be calculated. The resulting latent heat of vaporization calculation previously conducted will yield a lower value due to this reduction in coolant entering the control volume.

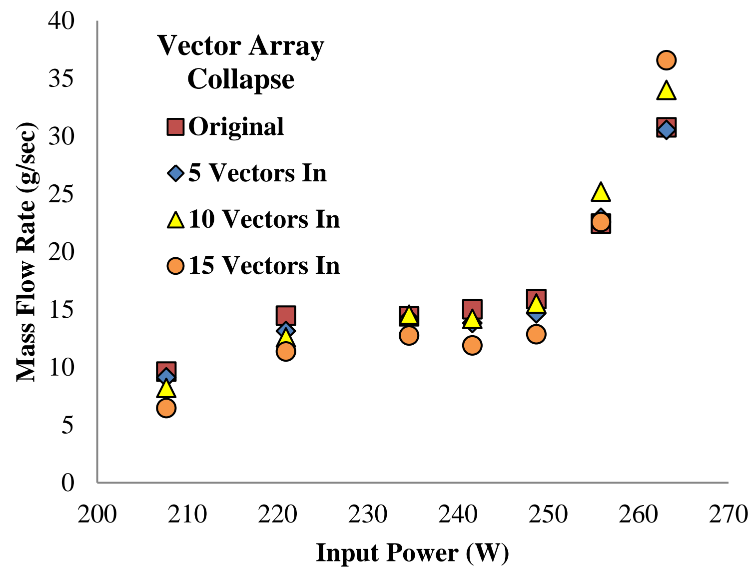
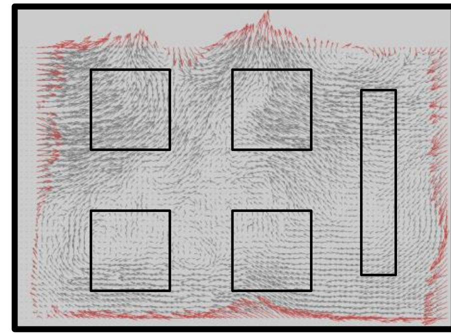


Figure 73 – Vector collapse liquid mass flow rate control surface analysis results

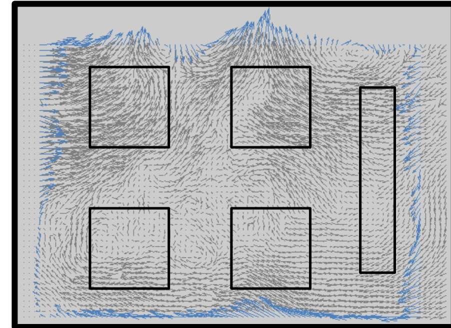
Another concern with this experimental method is accuracy. At roughly 88 J/g for the latent heat of vaporization for Novec 649, an accuracy on the order of 0.1 g/sec is necessary to achieve a resulting latent heat of vaporization calculation accurate to within 8.8 W. Arguably, even further accuracy is needed if this method is to be used to characterize the ability of any surface to capitalize on the convective effects of nucleate boiling naturally occurring in conjunction with latent heat transfer. The goal would be to assess the effectiveness of a boiling enhancement coating, like the microporous surface used in the current study, by calculating a ratio of latent heat converted through the coolant mass flow rate entering the control volume to

the remaining heat left which has to be transferred by the convective effects at the microlayer of the bubble leaving the surface. Analysis such as this could help ascertain the fundamentals explaining the significant increases in heat transfer coefficients attained with the use of the microporous surface over the bare silicon surface as reported in Figure 51. More pertinent to the current study would be to calculate the amount of vapor being generated at the surface through the final control volume analysis so as to add this element to the condensive limit model proposed in the Condensive Limit Trends and Modelling Attempt section (Section 4.6). In order to balance the continuity equation within the control volume, the net liquid mass flow rate shown to enter the region surrounding the boiling elements from the control volume analysis would be assumed to equal the net mass flow rate of vapor leaving the same region.

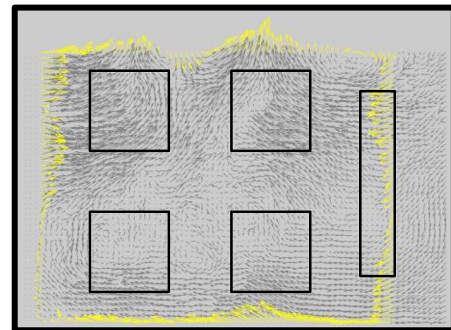
The fundamentals, primarily associated with continuity, governing the control surface approach and need for future work to extend it to a true control volume is on display when the periphery vector set utilized for the current analysis is varied. Ideally, the



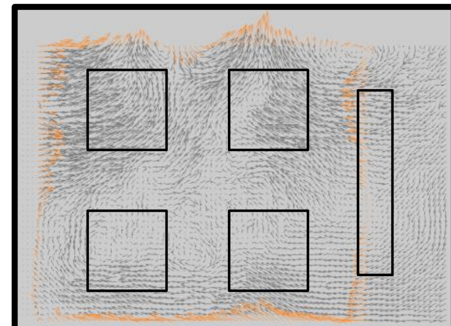
79 x 52 array



74 x 52 array



69 x 52 array



64 x 52 array

Figure 74 – Vector array reduction illustrations for control surface analysis justification

amount of quenching fluid to the boiling elements should be constant for any given power input. Furthermore, so long as the control surface never crosses the boundary of the heated elements, the analysis should yield the same quenching fluid mass flow rate to the primary elements independent of the vector array selection. Figure 74 presents the vector sets used in this analysis as well as illustrates the reduction of the periphery vectors used around the primary heated elements. They are color coded to match the mass flow rate results presented in Figure 73. As expected, the results closely match one another with one subtle but interesting deviation. As the vector set is reduced, the deviation from the largest vector set used grows. This is due to the need for encapsulating the heated elements within a control volume. As the vector set is

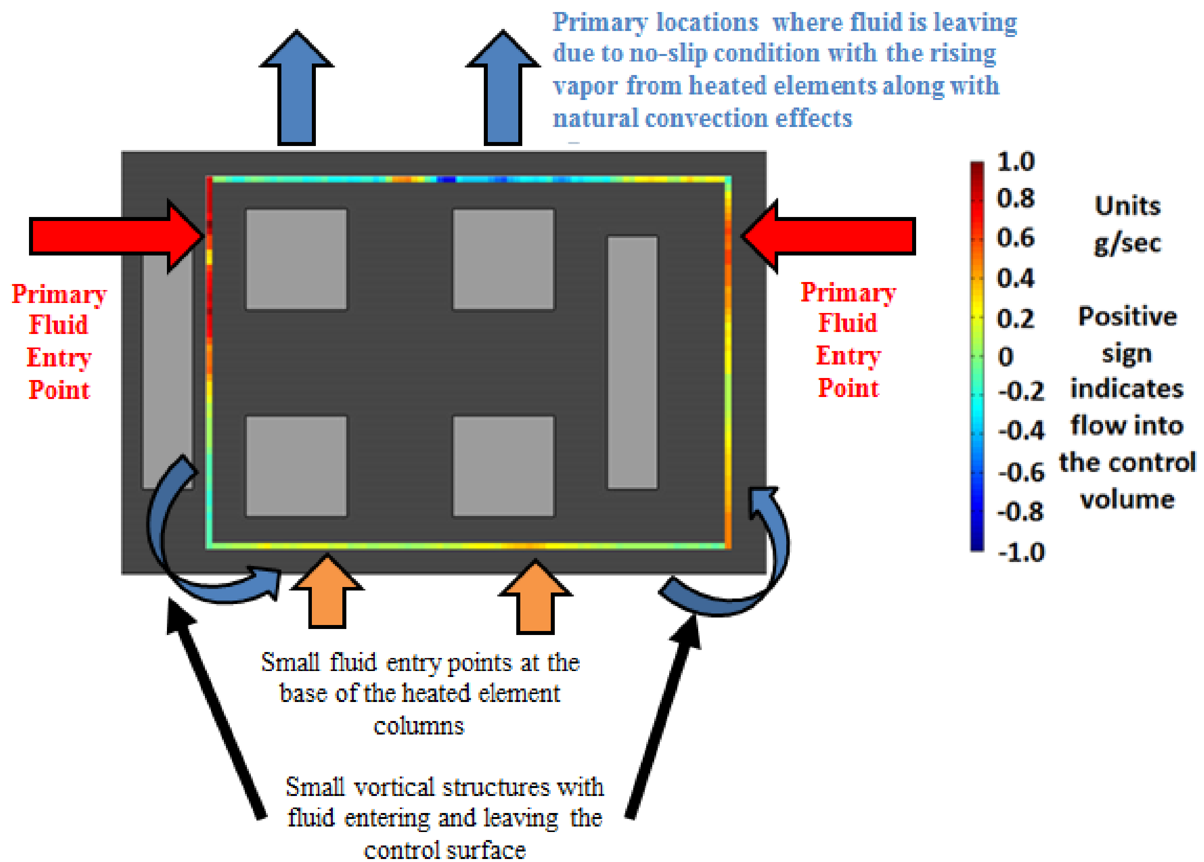


Figure 75 – Discretized flow map showing how quenching fluid enters the area surrounding the boiling elements

reduced, the influence of the mass flux from the unknown vectors facing away from the heated elements grows. It is expected that once this outward facing vector set is incorporated, a similar control volume reduction exercise could be conducted and the results would show little to no deviation across the data sets analyzed due to the principles of continuity.

Practical and useful information to the packaging engineer can be provided by discretizing the results of the control surface analysis. As noted in the Passive Element Integration Effects section (Section 4.8), it is understood that there are going to be other components within the liquid filled immersion cooled module that could obstruct flow paths to more critical elements within the system. In fact, a potential opportunity for future work would be to conduct the same two-phase analysis on the flow guides implemented for pool boiling as discussed in the Passive Element Integration Effects section (Section 4.8). These components were made of clear polycarbonate for this purpose. Without any obstructions, the discretized flow map around the periphery of the boiling elements gives interesting insight into how quenching fluid is entering the area surrounding these critical components as presented in Figure 75. The scale on the right of Figure 75 shows how fluid is entering, with colors on the red end of the spectrum, versus leaving with colors on the blue end of the spectrum. Some interesting fundamental trends and connections are on display with this discretized flow map as noted by the arrows and text boxes shown on and in support of Figure 75. With the no-slip condition invoked between the liquid-vapor interface, it is no surprise that the primary location where liquid is leaving the control surface is near where the vapor is leaving as well. Qualitatively recognized during the experiments and also confirmed by the results of Figure 75 are small vertical structures at the lower corners of the surface area in question. The fundamentals influencing these structures are unclear, but the nature of these structures are most likely governed by

continuity as fluid is rushed to the surface for quenching of the boiling surfaces. Also, the primary locations where coolant is entering the area surrounding the boiling elements is slightly above the lesser two flow guide heights tested in the Passive Element Integration Effects section (Section 4.8). From the results of Figure 67, it wasn't until the maximum flow guide was integrated, which would fall in the path of the fluid entering the boiling area on both sides as indicated by the discretized flow map, was there a noticeable impact on thermal performance both in terms of maximum power dissipation achieved as well as the final module level thermal resistance. Discretized vector maps could provide valuable insight into optimal locations for passive elements that may impede coolant flow on future designs of densely packed boards that are to be integrated into two-phase liquid immersion cooled systems.

Chapter 5: Flow Boiling Results and Discussion

For the purposes of this study, flow boiling will be where dielectric fluid flow is pumped through the cartridge at the inlet and outlet ports located to the left of Figure 28. The heat that is gained by the dielectric fluid flowing through the cartridge is injected into the primary chilled water cooling loop by a liquid to liquid heat exchanger as shown in Figure 33. The Graham condenser will be open and vented, but has been shown to carry negligible heat from the system in the Electronics Cartridge Assembly Design Motivations and Construction section (Section 3.1). Although the potential of deactivating coolant delivery to the chilled water header is explored, the dielectric fluid flow loop will always be active throughout the results introduced in this chapter. When the dielectric fluid coolant loop is deactivated, this is considered pool boiling, and those results were presented in the Pool Boiling Results and Discussion chapter. All flow boiling testing was done with a 15°C facility water temperature setting and Novec 649 as the working fluid.

5.1 Flow Boiling Thermal Performance Benefits and Fundamental Trends

A consistent theme that will be presented throughout the results in this chapter is that the increase in dielectric fluid flow rate does not necessarily shift the traditional boiling curve to the left or right in the fully developed regime but rather allows for further travel up the curve before reaching the catastrophic burnout event. Further support for this statement will be presented in this chapter, but in this section it is shown that increasing the dielectric fluid flow rate through the system from nothing, namely the pool boiling scenario, shows marked improvement. With

the tube inlet design shown in the left image of Figure 39 and a dielectric fluid flow rate of 660 mL/min, the maximum power dissipation achieved increased by over 100 W when compared to the pool boiling scenario as indicated by the power dissipation versus primary die average surface temperature plot presented as Figure 76 when the bare silicon surface is tested. It should be noted that this flow rate is minimal, enough to fill a typical soda can in roughly thirty seconds. Pressure drops through the cartridge as dielectric fluid flow rate is increased will be discussed in further detail in the Effect of Passive Element Integration on Flow Boiling section (Section 5.6.1), but when the mass flow rate yielded by this volumetric flow rate is multiplied by the final pressure drop across the cartridge recorded, an ideal pumping power of only 20 mW is needed. While it is understood that much more pressure drop will occur in delivering the fluid to the cartridge assembly through the required plumbing infrastructure, the ideal pumping power across the cartridge is orders of magnitude less than the computational power applied to the thermally managed heated elements within the enclosure. Efforts to minimize the amount of additional power required to manage and deliver the coolant to the cartridge while maximizing the computational power of the system will ultimately lead to more attractive PUE numbers.

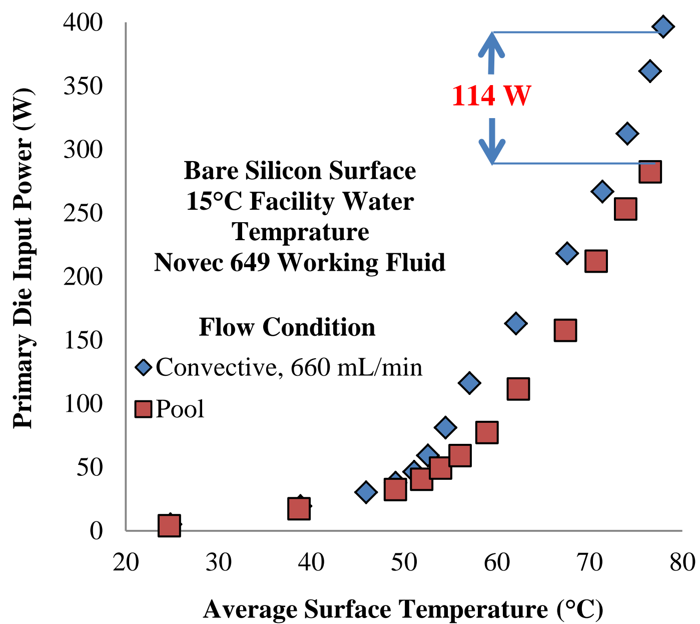


Figure 76 – Basic flow boiling introduction enhancement results

Fundamentally speaking, the plot shown in Figure 76 illustrates an interesting result worth noting. The average surface temperature under flow boiling conditions seems to be

consistently less for all power dissipations recorded. Furthermore, the curve does not seem as steep for the flow boiling conditions as it does for the pool boiling scenario. The steepness of the curve for the pool boiling scenario is tied to the degree of boiling activity occurring at the surface. From Rohsenow's correlation, Equation 4, there is cubic dependence on temperature for the power dissipation achieved. In the flow boiling scenario, this steepness does not seem to occur until much higher power dissipations. With any forced convection scenario, the thermal boundary layer is lessened, hence the associated higher heat transfer coefficients. In boiling however, as shown with the discussion of Hsu's model presented in the Bare Silicon Pool Boiling Thermal Performance and Fundamental Trends section (Section 4.1), this thinning of the boundary layer could impede the ability of bubbles to depart and thus delay the onset of fully developed nucleate boiling. Fortunately, even though some bubble departure is occurring in this regime, convective effects assist with lowering the surface temperature at the cost of the pumping power required to deliver the coolant, as it would be with any forced convection thermal management solution. While this developing or partial boiling regime is typically of little consequence in a data center given the desire to operate closer to the maximum capabilities of the system, discussion and confirmation of fundamental expectations is worth noting with any experimental data set.

5.2 Dielectric Fluid Flow Rate Variation and Subcooling Effects

With the bare die surface integrated, flow boiling tests were conducted with the tube inlet flow distribution design illustrated on the left image of Figure 39. Both the increasing and decreasing heat flux portions of these experiments yielded fundamental trend, support and discoveries when compared to accepted theory and historical works. The increasing run over all of the flow rates, along with that of a pool set for the extreme comparison of no flow rate effects,

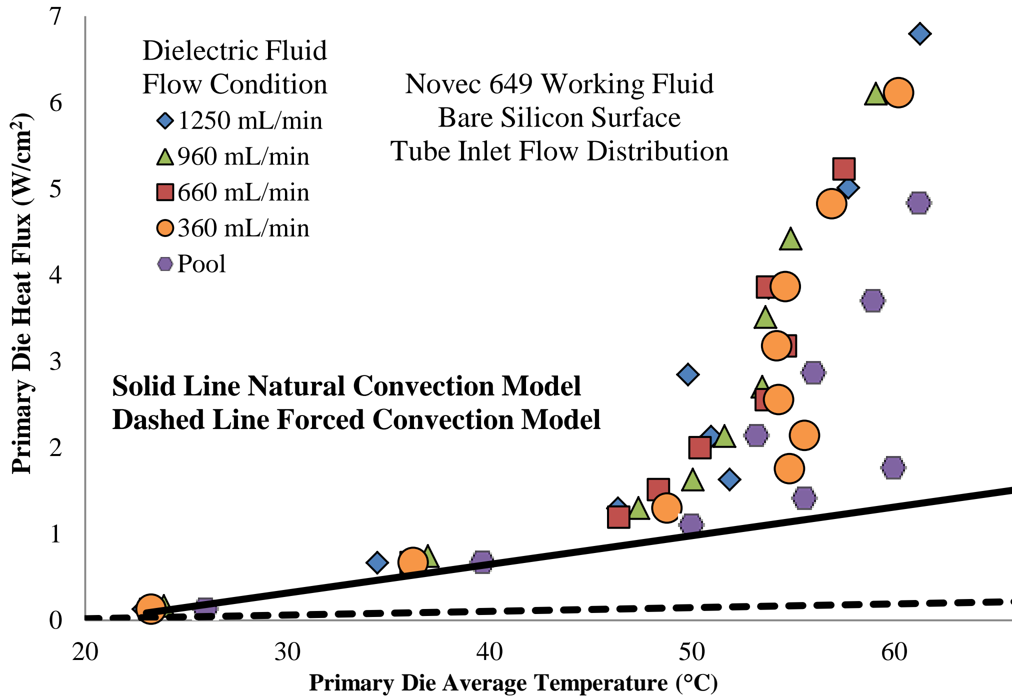


Figure 77 – Bare Silicon Tube Inlet Flow Distribution Boiling Incipience Variations

is presented as Figure 77. Higher level heat fluxes are omitted to focus on the hysteretic effect in boiling curves known as temperature overshoot which occurs before fully developed boiling begins. As discussed in the Flow Boiling Thermal Performance and Fundamental Trends section (Section 5.1), higher flow rates should thin the boundary layer. As discussed in the Bare Silicon Pool Boiling and Fundamental Trends section (Section 4.1), thickening the boundary layer should provide for bubbles to depart more effectively, hence the top nucleation before the bottom die effect that was highlighted there. The results of Figure 77 seemingly offer contradictory evidence to both of the previous statements as the pool boiling scenario has the highest temperature overshoot and the largest flow rate has the smallest. The pool boiling scenario would have the largest thermal boundary layer while the largest flow rate would have the thinnest from the induced flow through the cartridge. The first step to understanding why these results are in line with fundamental understanding is to gain some perspective into how the flow

is spread out over the die once it enters the cartridge. Assuming that the volumetric flow rate is delivered uniformly across the cross section, calculated Richardson numbers (Ri) are above 300 for all of the temperatures recorded in this region. The Richardson number is defined as the ratio of the Grashof number over the Reynolds number squared. Ri >> 1 dictates that forced convection can be generally ignored. With the tube inlet design, this scenario should not be considered as flow boiling per se, but more like consistently subcooled pool boiling. The Chu and Churchill [41] empirical correlation, Equation 3, for external free convection over a vertical plate is shown with the solid line and the isoflux forced convection over a flat plate, shown as

$$\overline{Nu_L} = 0.680 * Re_L^{\frac{1}{2}} * Pr^{\frac{1}{3}} \tag{17}$$

Equation 17, is shown as the dashed line in Figure 77. It is understood that varying dielectric fluid flow rates will bring about different dielectric fluid mean temperatures. Different mean temperatures will dictate the use of different properties for the natural convection and forced convection models. For the dashed and solid line results shown on Figure 77, the variation of the mean temperature yielded negligible differences in the model results. Therefore, an average line of all of the results as the primary die average surface temperature is varied for both of these models has been provided on Figure 77. The Chu and Churchill correlation was selected because some of the Rayleigh numbers leading up to incipience surpassed the 10^9 criteria for turbulence. The laminar isoflux equation was selected as the Reynolds number never exceeded 700 for any of the data points analyzed, well below the critical Reynolds number signifying transition to turbulence of 5 x 10^5. Fluid properties were calculated with a film temperature gathered from the measured average surface temperature from the diode locations specified in Table 1 and the mean dielectric fluid temperature data taken from the inlet and outlet

thermocouples located at these port locations as shown schematically in Figure 33 and illustrated to the left of the cartridge assembly on Figure 28. In accordance with the expectation from the calculated Richardson number, the heat flux and temperature results are much more in line with the free convection prediction rather than with the forced convection prediction. Details regarding the nature of the slopes of the convection curves illustrated in Figure 77 can be found in the Sample Calculations of Appendix III under the Forced versus Natural Convection Comparison Calculation.

With the understanding that the conditions within the cartridge for the tube inlet flow distribution design is convection dominated leading up to incipience, support for the temperature overshoot trends in Figure 77 can be further substantiated with fundamental knowledge regarding subcooling and Hsu's model [99]. A slightly different representation of the classic Hsu's model equation is presented as Equation 18. The goal to decreasing temperature

$$\begin{Bmatrix} r_{c,min} \\ r_{c,max} \end{Bmatrix} = \frac{\delta_t}{4} * \left[1 - \frac{\Delta T_{sub}}{\Delta T_{sat} + \Delta T_{sub}} \begin{Bmatrix} + \\ - \end{Bmatrix} \sqrt{\left(1 - \frac{\Delta T_{sub}}{\Delta T_{sat} + \Delta T_{sub}}\right)^2 - \frac{12.8 * \sigma * T_{sat}}{\rho_v * h_{lv} * \delta_t * (\Delta T_{sat} + \Delta T_{sub})}}\right] \tag{18}$$

Where $\Delta T_{sub} = T_{sat} - T_{\infty}$ and $\Delta T_{sat} = T_{wall} - T_{sat}$

overshoot is to increase the number of sites predicted to be active in Equation 18, or increase the range between the minimum site that is active, $r_{c,min}$, and the largest site that is active, $r_{c,max}$. With it previously shown that forced convection is largely negligible due to experimental results and calculated Richardson numbers, increasing the dielectric fluid flow rate should have minimal impact on the size of the boundary layer. Using the experimental data gathered leading up to the initiation of boiling and the isoflux laminar flat plate average Nusselt number equation shown as

Equation 17, heat transfer coefficients were found to stay consistently around 43 $W/(m^2K)$ with a maximum variation of 2.3%. With the thermal boundary layer approximated as k_l/h, this variation in calculated HTC's isn't enough to alter the thermal boundary layer thickness significantly. While increasing the subcooling, ΔT_{sub}, may not have an effect on the ratios that contain these terms in both the denominator and numerator within Equation 18, it will have an effect on the term under the radical which contains it in the denominator only. Increasing the subcooling reduces this ratio and increases the value under the radical. The radical governs the resulting range and therefore subcooling should increase the number of active sites, reducing the temperature overshoot. Increasing the amount of fluid flow into the cartridge which is being consistently subcooled by the liquid-liquid heat exchanger as shown in Figure 33 should decrease the mean temperature within the cartridge by virtue of a simple sensible heat gain analysis. This reduction of dielectric fluid mean temperature at any given heat flux yielded by increasing the dielectric fluid flow rate is shown by Figure 78. Therefore, by increasing the dielectric fluid flow rate, the temperature overshoot should be decreased for this natural convection governed flow distribution scenario as is experimentally shown by the specific incipience point data in Figure 80. These temperatures are the same as the

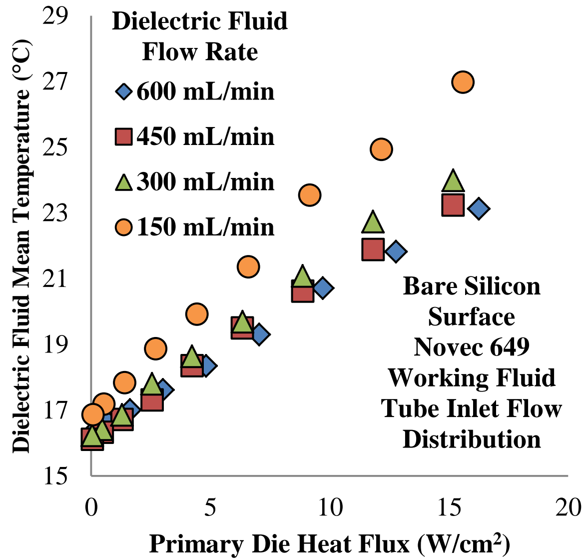


Figure 78 – Influence of increasing dielectric fluid flow rate on internal mean temperature for the tube inlet flow distribution design

overshoot points indicated on the increasing heat flux runs shown in Figure 77 for each flow rate along with a pool test at the same 15°C facility water temperature setting to indicate the extreme case of no flow within the cartridge.

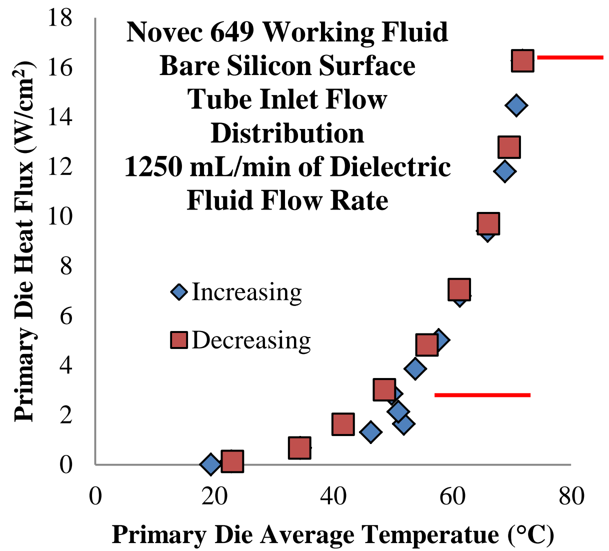


Figure 79 – Increasing and decreasing heat flux comparison of tube inlet flow condition

Red horizontal lines indicate data points of convergence between increasing and decreasing experimental runs

In order to establish a fully developed boiling region for fundamental assessment and potential development of C_{sf} values for extrapolation of intermediate data, similar overlays of the increasing and decreasing heat flux runs was conducted for the bare silicon surface with the tube inlet flow distribution method integrated as was done for fully developed boiling regime establishment method in the pool boiling data. The overlay of these runs is presented as Figure 79. The conclusion in looking at this data is that six points overlay one another on each of these curves and so those six points on the decreasing run should be used to establish a fully developed C_{sf}. This analysis was conducted and the results are shown as Figure 81, but the data is presented as the

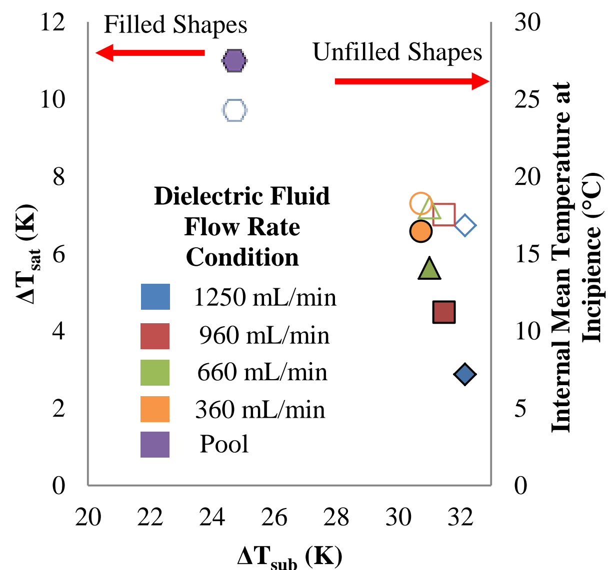


Figure 80 – Temperature overshoot dependence on dielectric fluid flow rate for the tube inlet design

variation of C_{sf} with respect to the mean dielectric fluid temperature within the cartridge at that heat flux to illustrate the potential effect of subcooling on C_{sf}. A sensible heat gain analysis of flow going through the cartridge assembly as well as data presented in Figure 78 shows that the increase in dielectric fluid mean temperature indicates an increase in heat flux as well. Support for the former statement comes in the form of a simplified look at the sensible heat gain equation. At any given instant, the power supplied to the dielectric fluid can be viewed as the product of the mean temperature, the fluid's volumetric heat capacity and the dielectric fluid flow rate. The volumetric heat capacity of the fluid is nearly constant throughout the temperature range tested. By increasing the dielectric fluid flow rate at a given power,

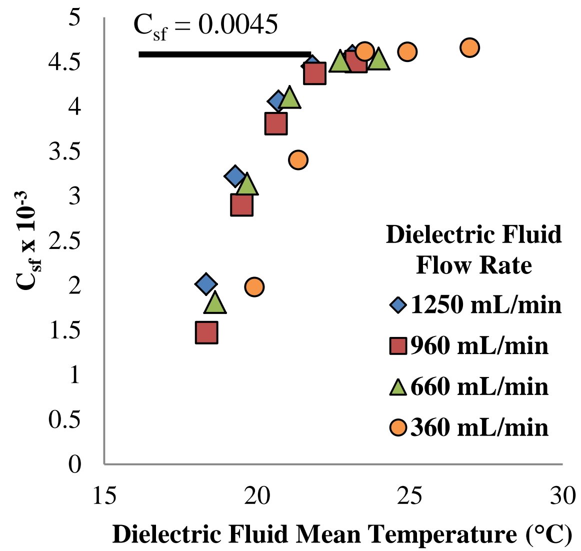


Figure 81 – C_{sf} convergence in flow boiling for bare silicon surface and the tube inlet flow distribution

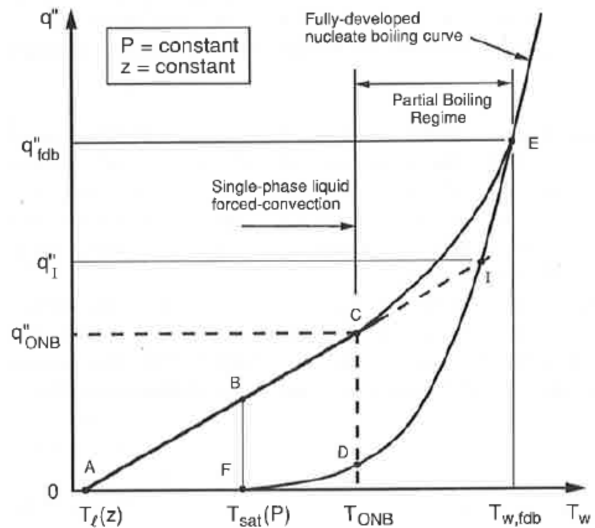


Figure 82 – Fundamental breakdown on subcooled flow boiling regimes [104]

the mean temperature of the fluid must go down in order to balance out the energy equation. Therefore, these data are converging on a consistent C_{sf} across all the flow rates as fundamentally expected, but the C_{sf}'s leading up to that convergence are part of another regime

called partial boiling. The convergence on one fully developed curve independent of flow rate, the partial boiling regime as well as several other important events and regions of the subcooled flow boiling process was introduced by Bergles and Rohsenow [104]. An illustration of these regimes as they relate to key events in the boiling process is shown as Figure 82.

Comparing the decreasing heat flux data taken for the bare silicon surface and the tube

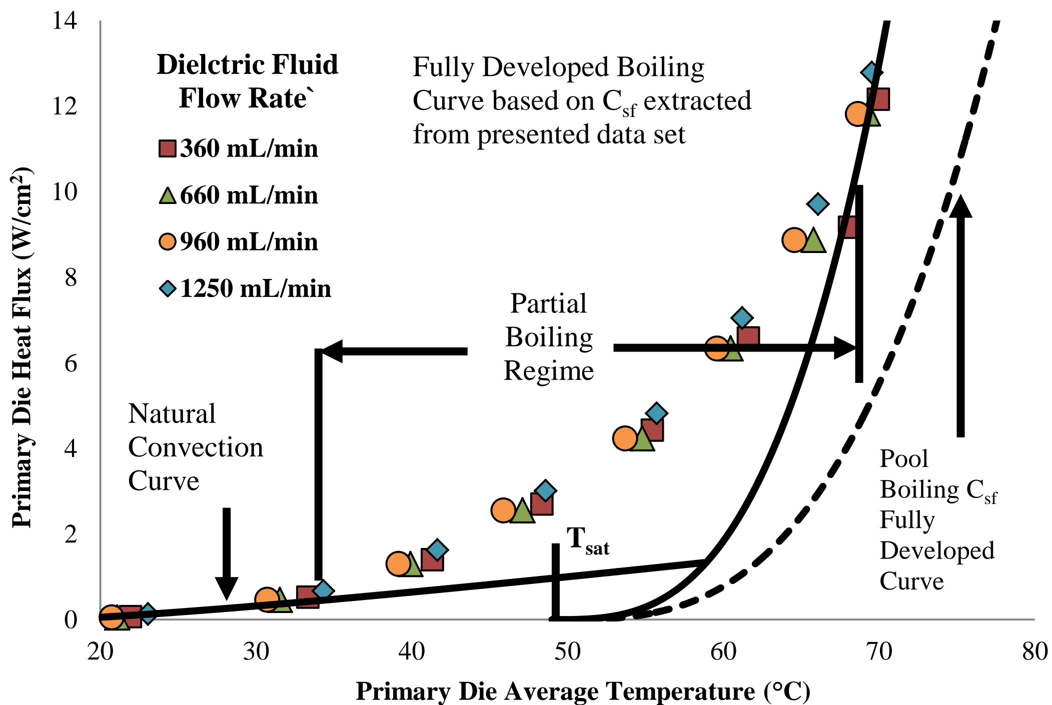


Figure 83 – Subcooled flow boiling curve for the bare silicon surface and the tube inlet distribution

inlet flow distribution method integrated to the Bergles and Rohsenow subcooled flow boiling map shown as Figure 82 shows interesting similarities as well as highlights several deviations associated with the degree of subcooling involved. These decreasing data are shown as Figure 83 along with several lines and labels meant to illustrate these similarities and deviations from the historical work of Bergles and Rohsenow. The subcooled flow map that was proposed suggested that once the boiling curves met after the partial boiling regime to become fully

developed, this area could be characterized by the same C_{sf} from pool boiling independent of subcooling involved. The reported data in Figure 83 show a deviation from this statement by showing the Rohsenow curve resulting from the integration of the C_{sf} acquired in pool boiling, taken from the bare silicon case in Table 2 with Novec 649 as the working fluid, shown by the dashed line shown on the plot to the fully developed boiling curve extracted from the converged C_{sf} independent of flow rate shown as the solid line. This is not surprising given the debate ongoing about whether or not C_{sf} is affected by subcooling.

An illustration from Carey presented as Figure 84, although indicating that subcooling should not have a significant impact in this region, shows that there is some shift to the left of the curve as subcooling is increased. While typical pool subcooling can be anywhere in the range of 5-15K, at the final values taken from the data in Figure 83, subcooling within the cartridge under these flow boiling conditions is as high as 26K. Therefore, it is not surprising that this degree of subcooling could have a substantial effect on the fully developed boiling curve, even in subcooled flow boiling. Another

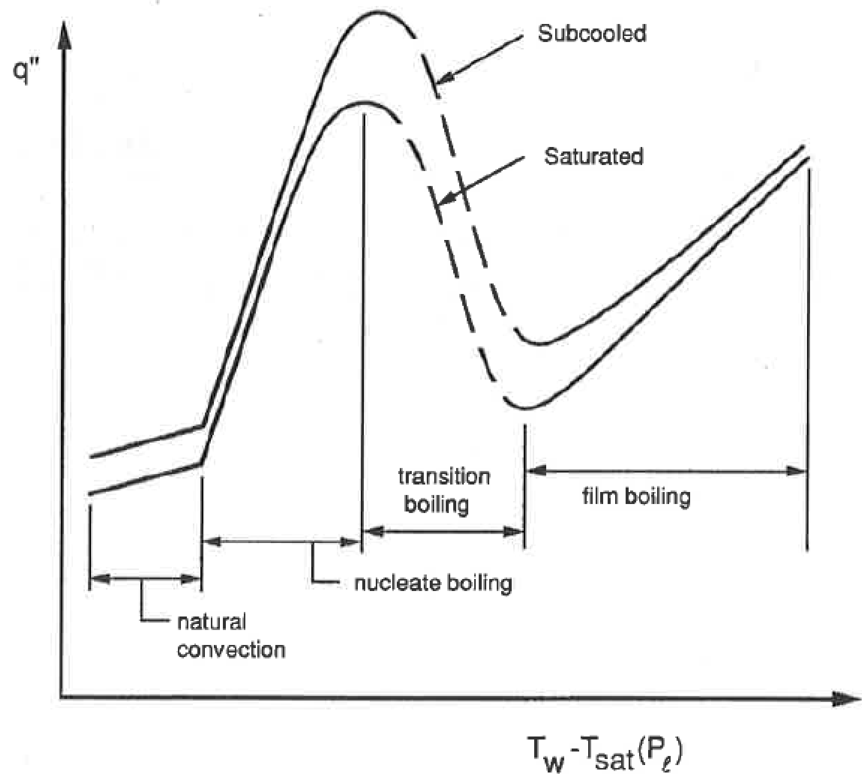


Figure 84 – Illustration of subcooling effects on boiling performance [109]

deviation from the proposed subcooled flow boiling map proposed by Bergles and Rohsenow shown in the data presented in Figure 83 that must be addressed is the early initiation of partial boiling indicated. This regime should not begin before the saturation temperature as the surface must reach this temperature in order to initiate boiling. This is more than likely an artifact of the lack of temperature sensors throughout all of the boiling surfaces. If boiling is still active on some diode locations while not active at other locations where temperature is not being recorded, then at a given heat flux the average surface temperature will yield a lower value than what would be expected given the local high heat transfer coefficients over the diodes that are recording temperature under active boiling conditions. This does not affect however the claims made at the extreme ends of the boiling data presented in Figure 83 by the definition of the phenomenon in these regions, either boiling has overtaken the entire surface or there is no boiling activity at all for the fully developed regime and natural convection regime, respectively. Therefore, all diodes are under the same convective conditions in these regimes and the conclusions drawn at these extremes should be valid regardless of temperature measurement resolution throughout the heated surfaces.

5.3 Surface Enhancement Tube Inlet Flow Distribution Trends

Similar to the thermal performance achieved by incorporating the surface enhancements into the pool boiling configuration, the microporous and microfinned structures yield significantly higher maximum power dissipations at much lower operating temperatures. Additionally, the power dissipated within the cartridge using these surface enhancements rivals the power consumption of many air-cooled 1 Rack Unit (RU) servers commercially available in roughly a quarter of the volume. The maximum heat fluxes attained along with the

corresponding operating temperature with the tube inlet flow distribution design incorporated for the microporous, microfinned and bare silicon surface is presented for comparison as Table 6.

As was done with the previous analyses, to determine which data points could potentially fall in a fully developed boiling curve for development of a C_{sf} along with potential connections to the subcooled flow boiling work of Bergles and Rohsenow [104], increasing and decreasing data runs were overlaid on top of one another to see which data points were connected. If these data points avoided the hysteresis typical in the boiling phenomena, they were further analyzed for an associated C_{sf} value. Increasing and decreasing runs from the 360 mL/min flow test are presented as Figure 85 not just to illustrate the number of points that could potentially be considered in a fully developed boiling regime, but also to highlight the significant lack of temperature overshoot evident in the data for both the microporous on the left and the microfinned surface on the right of Figure 85. This relative lack of overshoot occurs at what was

Table 6 – Tube Inlet Distribution Design Flow Boiling Thermal Performance Summary

Surface Condition	Microfinned Base Area				Microporous Surface			
Dielectric Fluid Flow Rate (mL/min)	360	660	960	1250	360	660	960	1250
Heat Flux (W/cm^2)	17.1	19.4	20.0	20.9	19.7	21.2	22.3	23.4
Average Base Surface Temperature (°C)	64.1	64.9	64.9	65.3	65.5	66.0	67.4	67.5

Surface Condition	Bare Silicon Surface			
Dielectric Fluid Flow Rate (mL/min)	360	660	960	1250
Heat Flux (W/cm^2)	15.6	15.2	15.2	16.3
Average Base Surface Temperature (°C)	72.0	71.2	71.0	71.8

determined to be the worst case flow rate for temperature overshoot in this particular tube inlet flow distribution design by the fundamentals laid out in the Dielectric Fluid Flow Rate Variation and Subcooling Effects section (Section 5.2). The marked improvement in overshoot reduction yielded by these surfaces has also been shown experimentally in a more conventional pool boiling facility by Sridhar [51].

As opposed to converging on a single C_{sf} as the bare silicon did when those data points leading up to the maximum values were analyzed with the tube inlet flow distribution design, both surface enhancements exhibited very different trends. C_{sf} plots yielded for these individual data points for all of the flow rates tested over each surface enhancement are illustrated by Figure 86. The lack of accordance with the expectation of a convergent C_{sf} illustrated with the bare silicon results and the same flow distribution method and non-agreement with the expected trends illustrated in the sub-cooled flow boiling map presented by Bergles and Rohsenow [104] as Figure 82 could be for two reasons. Bearing in mind that the dielectric fluid temperature

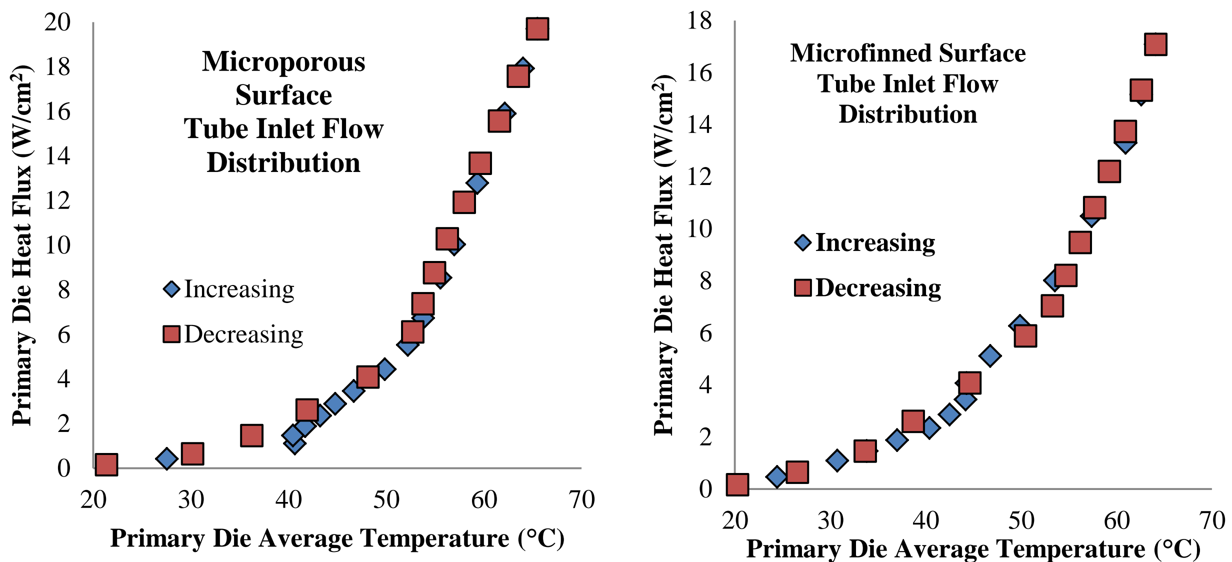


Figure 85 – Lack of temperature overshoot for both surface enhancements

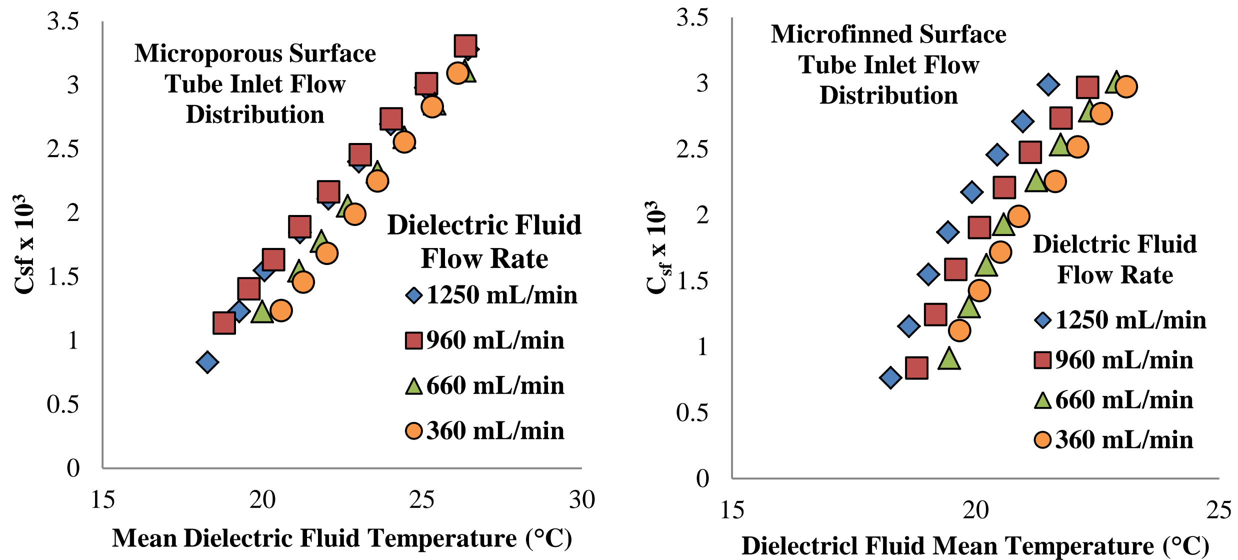


Figure 86 – C_{sf} values leading up to maximum heat fluxes attained in subcooled flow boiling with the tube inlet flow distribution integrated

within the cartridge under these conditions is severely subcooled, as high as 26K, saturated CHF's for the microporous surface was found to be 26.3 W/cm^2 by Rainey and You [73] and a microfinned surface similar to that used in the current study reached a maximum heat flux of nearly 50 W/cm^2 by Sridhar [51]. The previous microfinned heat flux value reported by Sridhar [51] was based on the surface enhancement's base area, not the total surface area exposed to the coolant. The maximum values attained under subcooled conditions, and note that subcooling does increase CHF, are less than CHF values attained in the literature for similar surfaces. It could be that the system is simply not being pushed hard enough to get to the point where the C_{sf} values will level off into a fully developed curve like the bare silicon results showed under a similar flow distribution scenario. An argument against this theory is that subcooling should shift the boiling curve to the left as it did with the resulting C_{sf} from the flow boiling data as shown in Figure 83 and the suggested effects illustration of subcooling proposed by Carey shown as Figure 84. C_{sf} values found for the fully developed region in pool boiling were 0.0018 and 0.0024 for the microfinned and microporous surfaces respectively, while even if the values

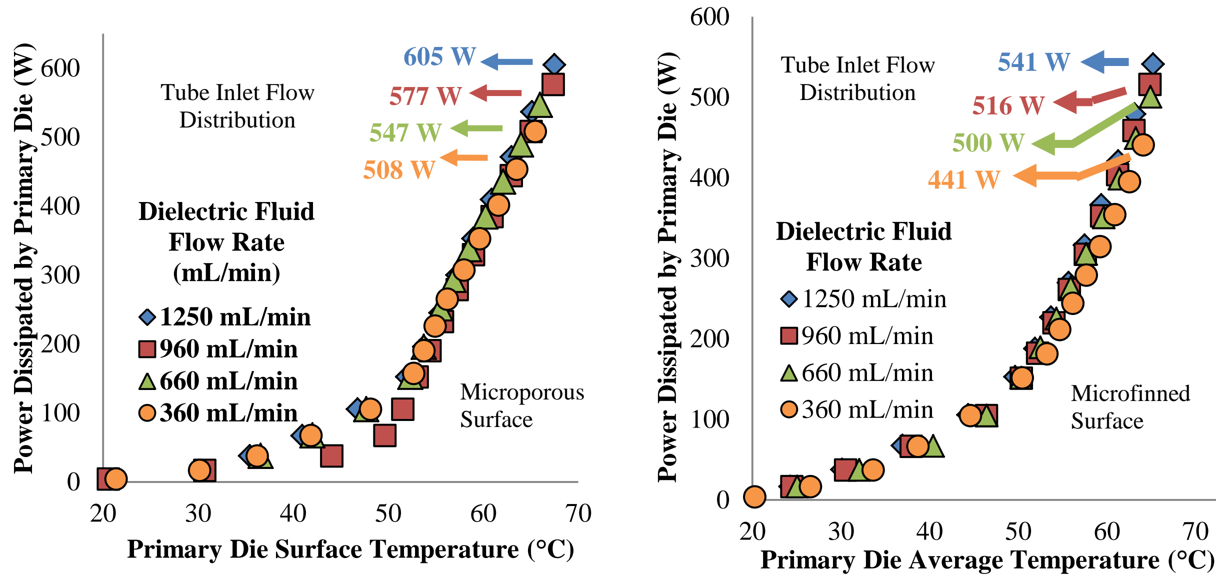


Figure 87 – Decreasing heat flux runs for both surface enhancements with the tube inlet flow distribution

presented in Figure 86 were allowed to converge further it would result in a shift of the curve to the right, contrary to what is expected with increased subcooling. There could be a flow boiling condensation limit to the cartridge as the flow boiling thermal resistance data reaches plateaus similar to those shown earlier in Module Level Thermal Resistance Plateaus section (Section 4.7) and as will be reinforced in the Flow Distributor Impact and Fundamental Trends section (Section 5.5). Ultimately, the use of surface enhancements may deviate from the proposed map of Bergles and Rohsenow much in the same way the C_{sf} yielded for the pool boiling scenario for both of these surfaces showed larger error margins (shown in Figure 53 and Figure 54) over those smaller margins yielded for the bare silicon for both working fluids tested (shown in Figure 46 and Figure 48). Equations like the Rohsenow correlation were originally made for flat surfaces and so their applicability to the surface enhancements like those tested in the current study may be limited. As with any C_{sf} value, they should be used with caution but can be very helpful in estimating thermal performance when enough conditions are known and can be adequately related to the test setup from which one is attempting to use the value.

With the lack of convergence on a C_{sf} value and thus inability to define regimes similar to those proposed by Bergles and Rohsenow, decreasing heat flux plots are offered for both surface enhancements tested using the tube inlet flow distribution as Figure 87. Maximum resulting power dissipation values are highlighted for comparison to highlight the capabilities of a two-phase liquid immersion cooled system to those using more conventional and commercially available thermal management solutions.

Table 7 – Tube Inlet Distribution and Header Deactivated Flow Boiling Thermal Performance Summary

Surface Condition	Microfinned Base Area				Microporous Surface			
Dielectric Fluid Flow Rate (mL/min)	360	660	960	1250	360	660	960	1250
Heat Flux (W/cm^2)	15.1	16.4	17.0	18.8	15.6	20.1	21.9	23.7
Average Base Surface Temperature (°C)	63.7	63.5	62.9	64.0	63.6	66.6	67.9	69.4

Surface Condition	Bare Silicon Surface			
Dielectric Fluid Flow Rate (mL/min)	360	660	960	1250
Heat Flux (W/cm^2)	11.9	14.2	14.9	16.3
Average Base Surface Temperature (°C)	71.3	71.3	70.9	71.8

5.4 Chilled Water Header Impact

One of the primary concerns with introducing a liquid based thermal management solution into the data center is the fear associated with bringing conductive liquid near sensitive electronics. The purpose of the data presented here is to examine the benefits and maximum thermal performance achieved when the chilled water header is deactivated. Under this condition, only dielectric fluid is pumped through the cartridge, allowing for the chilled water to be located remotely for removing the heat gained by the dielectric fluid via liquid-liquid heat exchanger. The maximum heat fluxes attained with the chilled water header deactivated for all three surfaces examined is presented as Table 7. From the table, the microporous surface outperforms the microfinned surface at the higher heat fluxes, but a direct comparison of the surfaces will be conducted in this section. The bare silicon surface seems to perform similarly with the header activated or deactivated, but it will be shown in this section that as the dielectric

fluid flow rate is decreased, the system begins to behave more like the pool boiling condition and consequently the header becomes more beneficial at these lower flow rates.

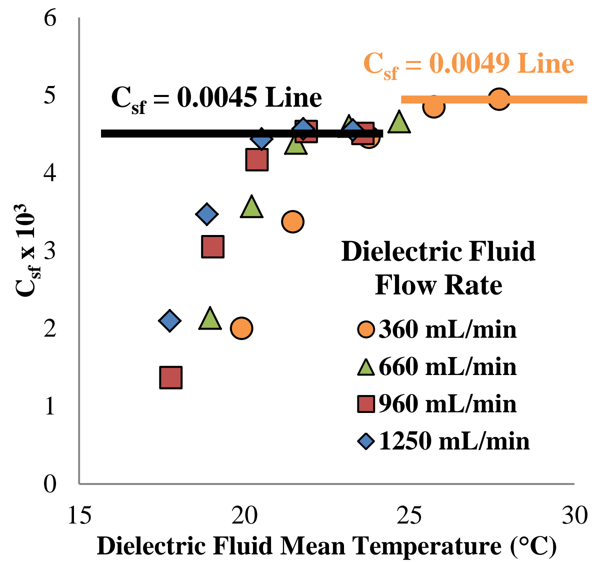


Figure 89 - C_{sf} convergence in flow boiling for bare silicon surface and the chilled water header deactivated

A similar analysis was conducted on the bare silicon results with the header deactivated as was conducted when the header was activated as discussed in the Dielectric Fluid Flow Rate Variation and Subcooling Effects section (Section 5.2). Additionally, the cartridge behaves similarly to the bare silicon data with the header activated at the low end and high end of the heat flux range tested as supported by the fundamental arguments discussed in that section. The analysis of the C_{sf} values leading up the maximum heat flux for the bare silicon surface with the chilled water header deactivated and the tube inlet flow distribution design (as described in Section 3.5) integrated is presented as Figure 89. The results for the highest three flow rates show similar convergence to that of the bare silicon with the header

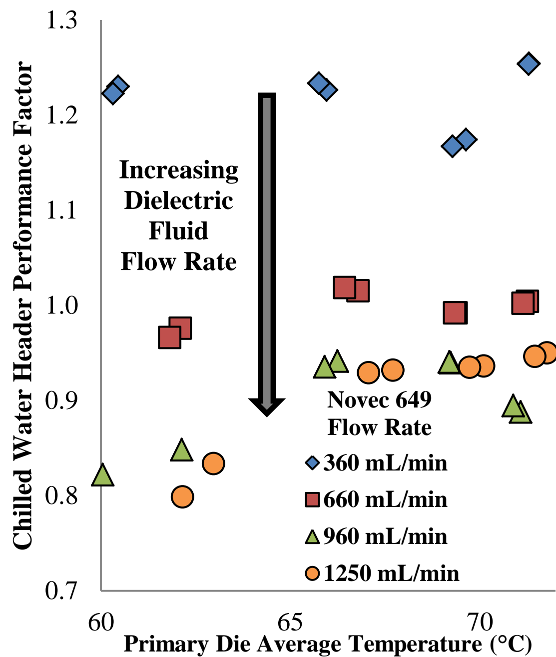


Figure 88 – Bare silicon chilled water header performance factor

activated presented as Figure 81. The values for the header deactivated scenario even converge on the same C_{sf} value as the one for all of the flow rates tested in the header activated scenario, namely 0.0045. It appears, from the results with the header deactivated, Figure 89, that the lowest flow rate tested converges on a slightly higher C_{sf} value. This is more than likely a result of the deviation from the trend of the rate of change of the dielectric fluid mean temperature within the cartridge for this lowest flow rate, as shown in Figure 78. Without the header to support this deviation, the converged upon C_{sf} begins to increase and behave similarly to a slightly less subcooled pool, like the dashed line results shown in Figure 83. Supporting the claim for the need of a chilled water header at the lower flow rates, a plot of a Chilled Water Header Performance Factor versus average primary die surface temperature is presented as Figure 88. This factor is defined as the ratio of the power dissipated with the header activated over that dissipated with the header deactivated. As it is impossible to have measured

$$Chilled\ Water\ Header\ Performance\ Factor = \frac{Power\ Dissipated\ by\ Primary\ Die\ with\ Header\ Activated\ at\ a\ given\ surface\ temperature\ (W)}{Power\ Dissipated\ by\ Primary\ Die\ with\ Header\ Deactivated\ at\ a\ given\ surface\ Temperature\ (W)}$$

temperatures line up exactly between separate experimental runs, a fifth-order polynomial curve fit to the temperature data clearly in the boiling regime was generated for each experimental run, header activated and deactivated, in order to extract the power dissipation necessary for comparison with the other experimental run where a temperature was measured. The results show that as the dielectric fluid flow rate is decreased the thermal performance of the system increases when the chilled water header is active. If ample dielectric fluid flow rates are available, then it is possible to remove the chilled water header, and thus delivery of the conductive fluid directly to the cartridge, from the overall system design. The advantage of the

chilled water header is substantially reduced at the 660 mL/min mark, which is very little when thought of from the perspective that this is enough to fill a soda can in roughly thirty seconds. The need for more in-depth analysis of the trade between pumping chilled water to the cartridge comes in the form of density differences however. The density of dielectric fluid is roughly 1.6 times that of water, and thus will be that much harder to pump. These data are offered to show the potential of removing this element from the design, but further analysis based on other fluid properties such as viscosity as well as distances that must be traversed by pumping either fluid is necessary to truly recommend removal of this design feature.

In order to assess the sensible heat gained by the dielectric fluid flowing through the cartridge as a function of input power, a plot similar to that of Figure 59 is presented that shows

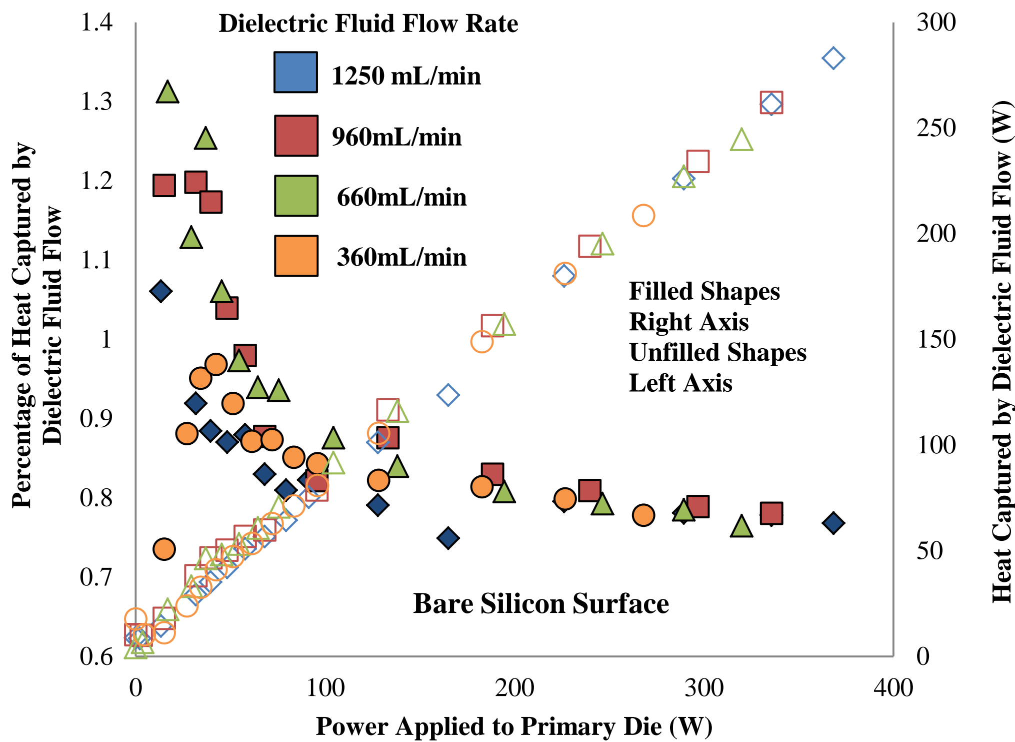


Figure 90 – Dielectric fluid sensible heat gain analysis with the chilled water header deactivated

how the heat captured by the dielectric fluid varies with respect to input power applied to the primary die for the header deactivated scenario presented in this section. With no influence from the chilled water header in this scenario, the fundamental expectation is that the dielectric fluid would capture all of the heat applied to primary die, assuming negligible losses through the cartridge walls. The latter assumption is not entirely valid because of the material used to construct the cartridge itself along with the inlet and outlet ports to the cartridge. All three of these pieces are constructed of highly thermally conductive aluminum. As the results of Figure 90 show, the linear nature of the relationship between input power and heat removed is maintained, as fundamentally expected. The fundamental deviation however from expectation is evident in the percentage analysis shown on the left axis of Figure 90. As opposed to the data of Figure 59 converging on a value near one, this data seems to converge on a value closer to 0.8. With a calibrated flow meter, pump and thermocouples all providing inputs to the sensible heat gain analysis, it is unlikely that these are the reasons behind the deviation. It is possible that there is some vapor exiting the cartridge through the outlet ports. At the flow rate of 1250 mL/min, representing a mass flow rate of 0.034 kg/sec, even just 2.5% of this liquid flow rate remaining vapor represents roughly 75 Watts of power that could be left unaccounted for. Without knowing exactly how much vapor is in this portion of the flow loop, adjusting the simple $c_p\Delta T$ analysis to a more refined enthalpic analysis is difficult. With this potential weakness in mind, the results of Figure 59 show some reasonable agreement with fundamental expectations along with some explanation as to why the deviations may be occurring.

The decreasing heat flux portion data, shown as Figure 91, is labeled to highlight similarities and differencesbetween the fundamental subcooled flow boiling map proposed by Bergles and Rohsenow [104] shown as Figure 82. There are a number of similarities between the data presented in Figure 91 with the header deactivated and that of Figure 83 where the header is activated, as may be expected given the similarity in the flow distribution technique implemented. The one notable difference is the deviation in convergence in the fully developed

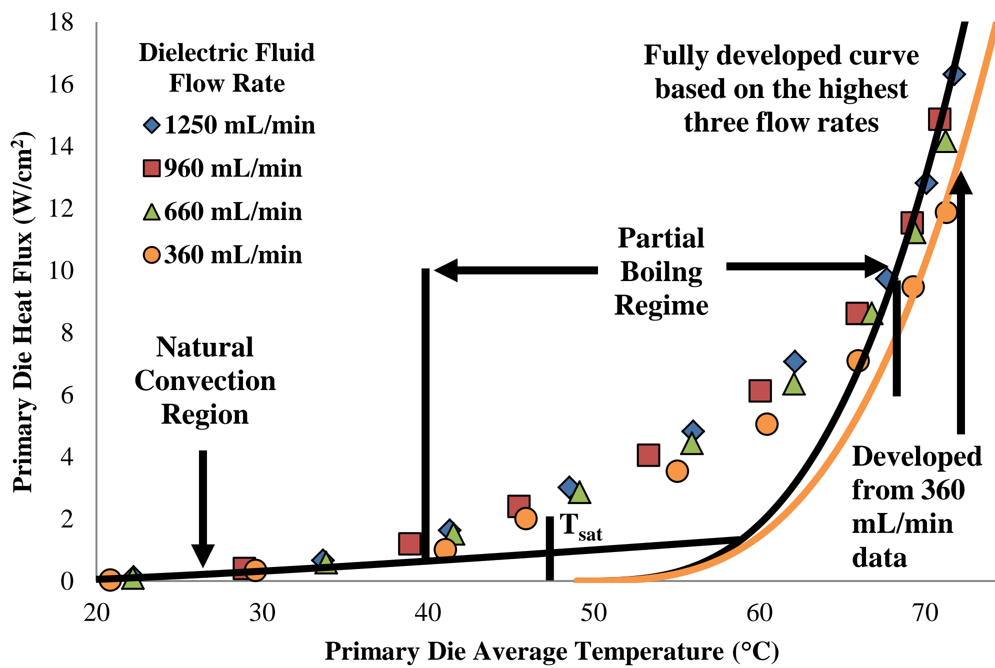


Figure 91 - Subcooled flow boiling curve for the bare silicon surface and chilled water header deactivated

region for the lowest flow rate tested. This is more than likely due to a need for the header at this flow rate, as supported by the data in Figure 88, as well as a shift towards the less subcooled fully developed line, represented by the dashed line in Figure 83. The other three flow rates' convergence on a C_{sf} value of 0.0045 is the same number as what all four flow rates converged upon with the tube inlet flow distribution method and the header activated, showing excellent similitude between all of the experimental runs captured by the header activated/deactivated tests.

Similar to the header activated scenario for the surface enhancements, there was a convergence for the Csf values leading up to the maximum heat flux recorded. In order to this lack of convergence, and inability to correlate the final maps to the historical subcooled boiling map presented by Bergles and Rohsenow, the Csf variation with respect to the mean dielectric fluid temperature within the cartridge, meant to illustrate the degree of involved with the variation, is presented as Figure 92 for both the microporous and surfaces. The same

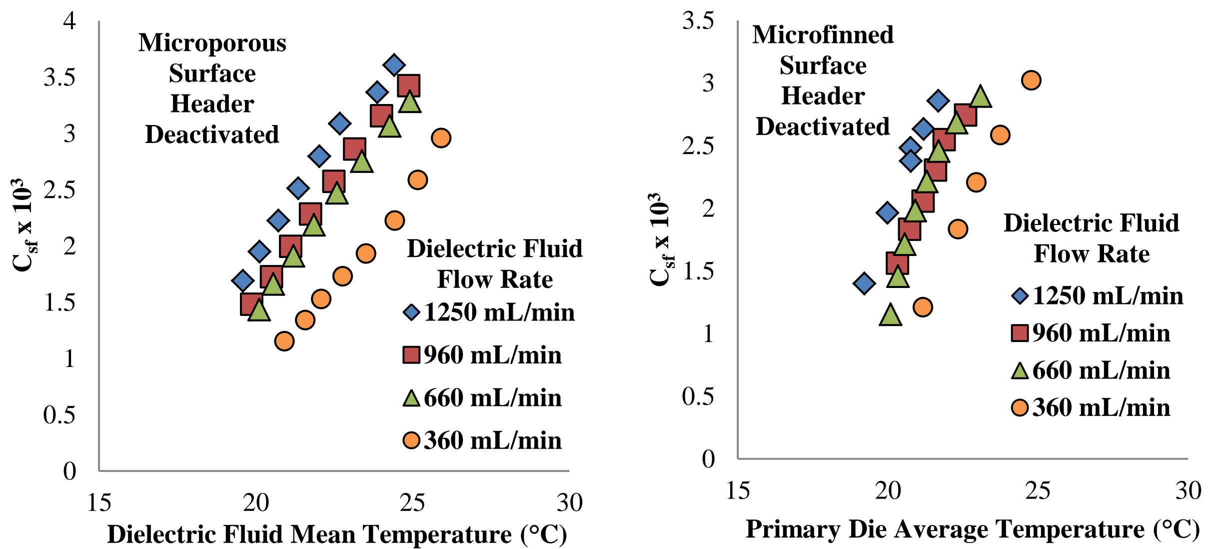


Figure 92 - C_{sf} values leading up to maximum heat fluxes attained in subcooled flow boiling with the chilled water header deactivated

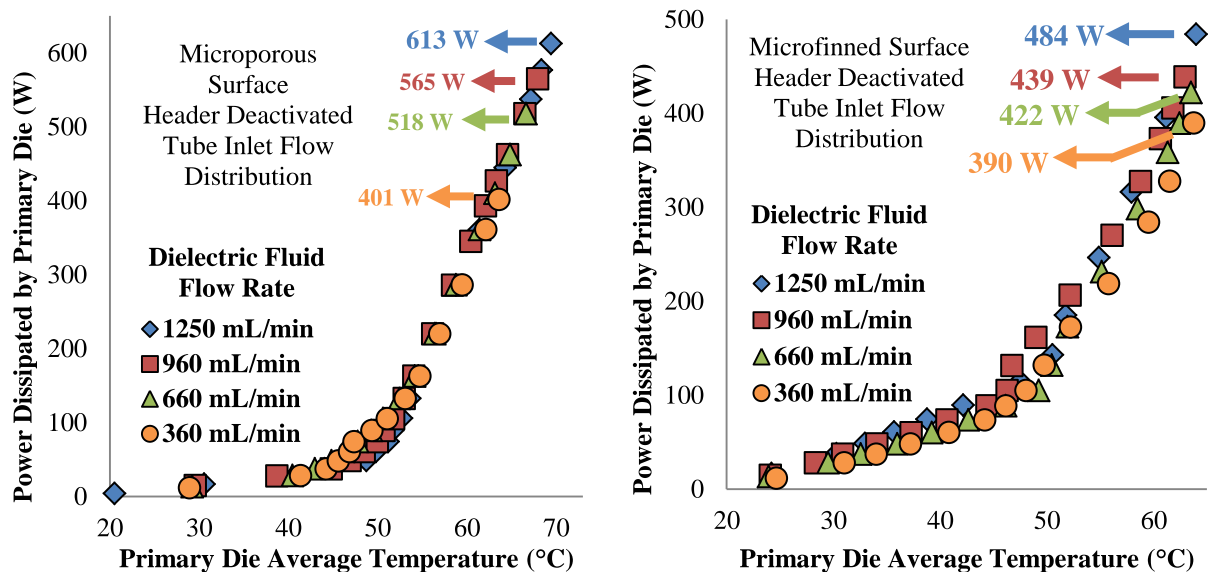


Figure 93 - Increasing heat flux runs for both surface enhancements with the chilled water header deactivated

fundamental points and arguments made as to the reason for this lack convergence are presented in Surface Enhancement Tube Inlet Flow Distribution Trends (Section 5.3). The increasing portion of the data showing the variation of heat flux with to surface temperature are presented as Figure 93 for both the microporous and surface. In an effort to determine the efficacy of the header with regards to these surface enhancements, a Microporous Surface Enhancement Factor is defined which represents of the power dissipated by the microporous surface over that of the microfinned at a given surface temperature. The intermittent data not measured experimentally are collected in the same fashion as that collected for generation of Figure 88. This factor's variation with respect to surface temperature at values in the boiling regime is presented as Figure 94. As the microfinned heat sink has structures that protrude into the dielectric fluid flow, it is no surprise that the microfinned heat sink would perform better than the microporous heat sink for the highest dielectric fluid flow rate tested, 1250 mL/min. As the flow rate is reduced to the lowest value tested, 360 mL/min, the microporous surface begins to have an advantageous

impact. This trend is completed by the much higher enhancements achieved when there is no dielectric fluid flow within the system, namely pool conditions. The results of Figure 94 would suggest that if high dielectric fluid flow rates are available, then the microfinned heat sink is a better option. However, if low dielectric fluid flow rates are mandated or if the system designer would like to deactivate the dielectric fluid flow altogether, the microporous surface enhancement is the better of the two options.

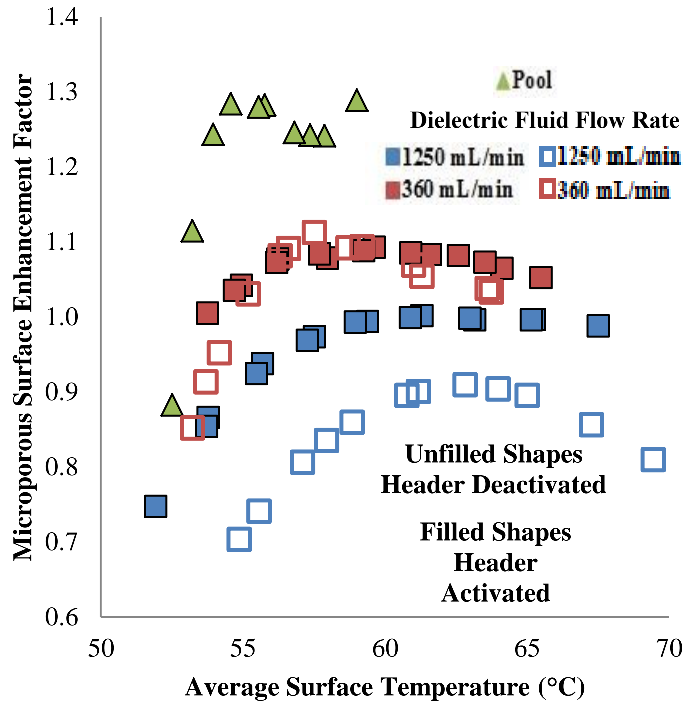


Figure 94 – Microporous surface enhancement factor illustrating potential benefits of chilled water header

5.5 Flow Distributor Impact and Fundamental Trends

PIV measurements indicated that the tube inlet design was not distributing flow effectively over the four primary die within the cartridge assembly. In an effort to improve this, a flow distributor was designed and implemented into the enclosure. An illustration of its orientation and placement is shown as the right image on Figure 39. The microfinned surface was not tested with this flow distribution method but the maximum heat flux achieved along with its corresponding temperature for the bare silicon and microporous surface is shown in Table 8.

Table 8 – Flow Distributor Design Flow Boiling Thermal Performance Summary

Surface Condition	Bare Silicon Surface				Microporous Surface			
Dielectric Fluid Flow Rate (mL/min)	360	660	960	1250	360	660	960	1250
Heat Flux (W/cm^2)	13.5	16.0	17.5	17.9	17.2	20.1	22.0	22.4
Average Base Surface Temperature (°C)	70.9	72.1	72.8	72.7	64.2	66.1	68.4	68.6

While the high end heat flux for the bare silicon surface converges on a very similar C_{sf} to that of the tube inlet design with the header activated, an analysis of the Richardson number at the lower heat fluxes yields an interesting trend. It was numerically concluded by Fincher [93] that the mass flow rate emanating from each slot of the flow distributor was equal. Therefore, knowing the dielectric fluid flow rate yielded a velocity exiting the slot of the distributor. When this velocity was assumed to be the same at the trailing edge of the top heated die as at the slot, Richardson numbers ranged anywhere from 0.03 to 11 across the flow rates tested. This was assumed to be not sufficiently greater than one so that forced convection could be ignored as it was with the tube inlet design, but not sufficiently less than one across the range of flow rates

tested to ignore natural convection. In instances where free and forced convection effects must both be taken into account, it has been suggested that an addition or subtraction of the Nusselt numbers associated with each of these heat transfer mechanisms be employed based on the flow conditions. The suggested equation is shown as Equation 19. For transverse or assisting flows, the latter of which is true for the case of the flow distributor implementation scenario, it is suggested that the two terms on the right hand side of Equation 19 be added. It is also suggested that the exponent n be 3, although much better agreement with the experimental results was found when n was set equal to 1. This is most likely an artifact of the assumption made in the analysis that the natural convection thermal boundary layer is uninterrupted between the two

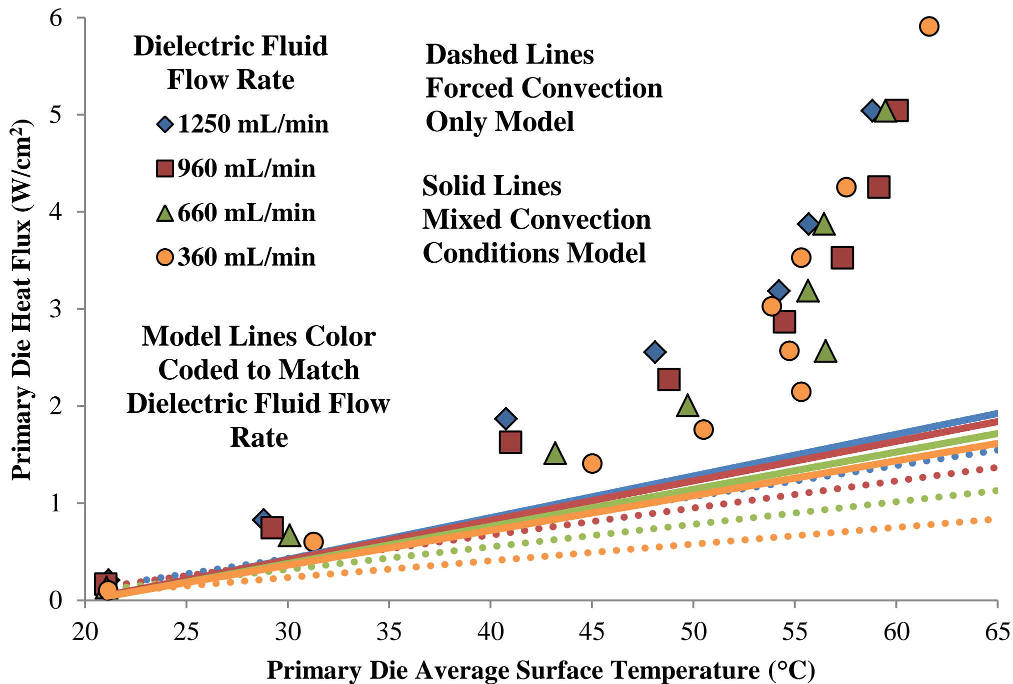


Figure 95 – Combined free and forced convection trend with the flow distributor implemented on the bare silicon surface

heated elements as illustrated in Figure 41 and used in the Forced versus Natural Convection Calculation section in Appendix III. Rather than suggest a substantially different exponent for use in Equation 19, the results from using an exponent of 3 are shown in the solid theoretical trends lines shown in Figure 95. The free convection portion was calculated by Chu and Churchill [41], shown as Equation 3 while the forced convection portion used Equation 17, an isoflux laminar flat plate equation as none of the Reynolds numbers over the course of the flow

$$Nu^n = Nu_F^n \pm Nu_N^n \tag{19}$$

rates tested surpassed the critical value of 5 x 10^5. In an effort to show the benefits of this approach, the portion of the increasing runs leading up to incipience are shown as Figure 95 with the combination modeling results shown as the solid lines color coded to each flow rate and the dashed line representing the results as if only forced convection were taken into account. The model where the Nusselt numbers from both heat transfer mechanisms are allowed to contribute to the overall heat transfer coefficient represent the behavior in this lower heat flux regime better than assuming forced convection only, even though the flow distributor has shown, through PIV measurements presented in the Single Phase PIV Analysis section (Section 5.7), superiority in terms of distributing flow directly over the die. It is this superiority that requires incorporation

of the forced convection element but the fluid is still subcooled to the extent that buoyancy forces of the heated fluid contribute to the heat transfer enough to be accounted for in this lower heat flux regime. The influence of the free convection on the lower heat flux behavior is also evident in the incipience behavior, the fundamentals of which were explained at length in the Dielectric Fluid Flow Rate Variation and Subcooling Effects section (Section 5.2). As the flow rate is increased, the temperature overshoot is reduced which runs contrary to the theory that thinning the boundary layer through increasing the flow rate would increase temperature overshoot. As explained in the section through a parametric assessment of Hsu's model, the subcooling effects are more influential than the fluid flow effects, thus fundamentally supporting the overshoot trend present in the data.

An analysis of the C_{sf} data leading up to the maximum heat flux recorded shows a convergence on a 0.0046 value. The C_{sf} variation as a function of the mean dielectric fluid temperature within the cartridge for the bare silicon surface with the flow distributor implemented and chilled water header activated is presented as Figure 96. The converged value in Figure 96 is very similar to the 0.0045 value converged upon for the tube inlet design with the header activated, showing similarity in performance as well as consistency among the experimental runs. A sample calculation showing how the C_{sf} value was extracted from the Rohsenow correlation, shown as Equation 4, along with

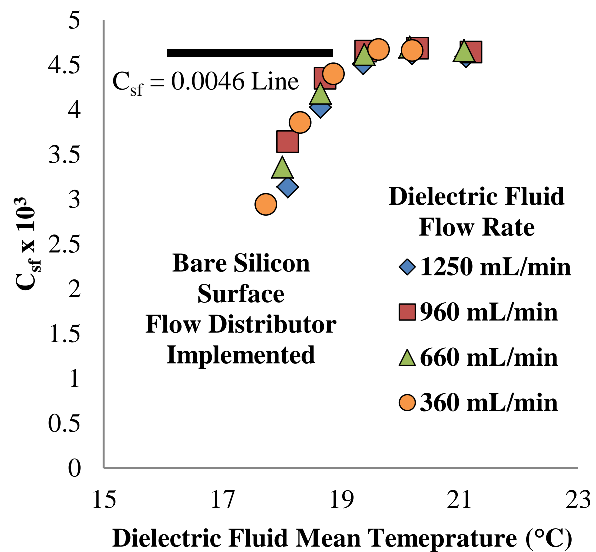


Figure 96 – C_{sf} convergence for flow boiling with the bare silicon surface and the flow distributor implemented

measured data is provided in Appendix III under the C_{sf} calculation section. The decreasing heat flux data for all of the flow rates tested in this scenario is presented as Figure 97 with portions labelled to show similarities and differences with the fundamental subcooled flow boiling map proposed by Bergles and Rohsenow [104], presented as Figure 82. For clarity, the combined natural and forced convection regime on Figure 97 is shown as a straight line. In actuality, this is a series of lines dependent on the dielectric fluid flow rate as presented in the data that highlights the lower heat fluxes leading up to boiling incipience, shown as Figure 95. The same

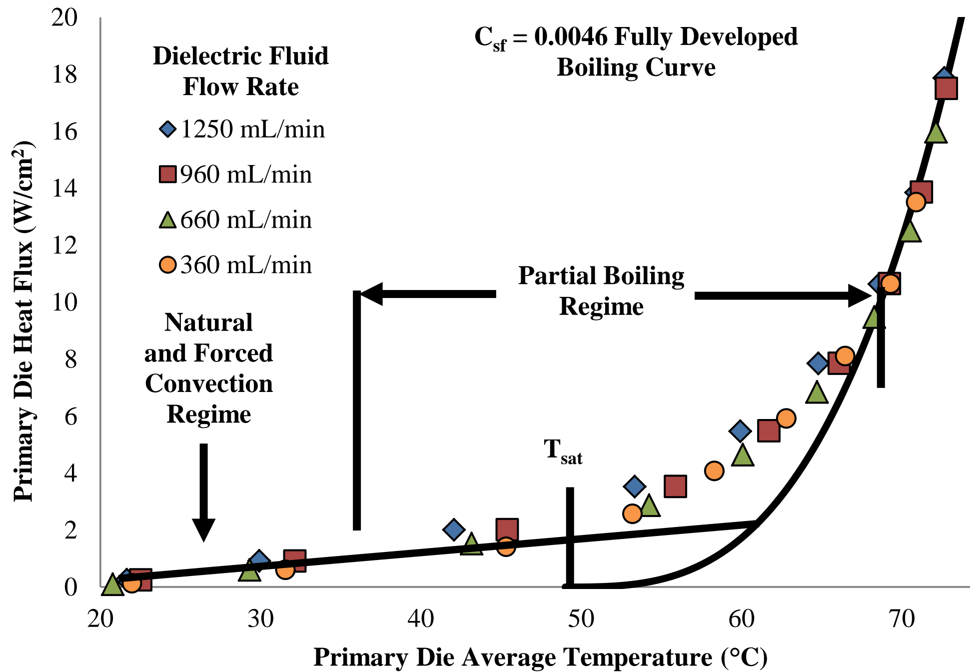


Figure 97 – Decreasing heat flux data for the bare silicon surface and the flow distributor implemented

fundamentals governing the regimes of this presented curve along with the labeling is discussed at length in the Dielectric Fluid Flow Rate Variation and Subcooling section (Section 5.2).

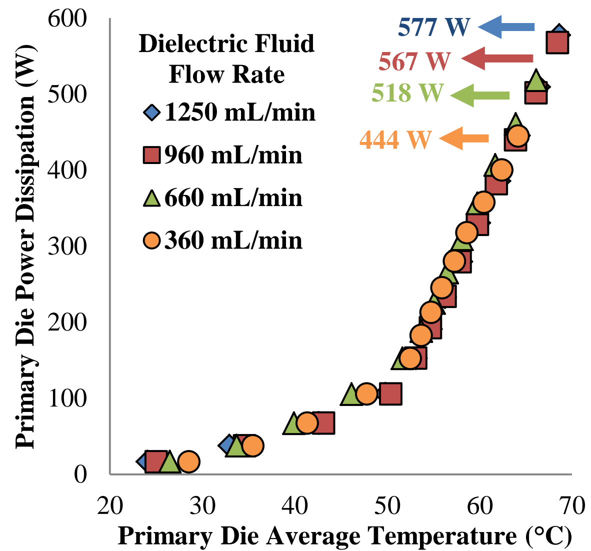


Figure 98 – Decreasing heat flux data for the microporous surface with the flow distributor implemented

As has been the case for a number of scenarios tested within the current study, the surface enhancement failed to yield a convergence upon a stable C_{sf} near the maximum heat fluxes tested with the flow distributor implemented. The variation of the C_{sf} with respect to the mean dielectric fluid temperature within the cartridge is presented as Figure 99. Due to the fact that there was a lack of C_{sf} convergence, the decreasing heat flux data is presented for the microporous surface with the flow distributor implemented to illustrate the maximum power dissipations achieved. These power dissipations, shown as Figure 98, are significant as they rival the computational power input of many commercially available air-cooled servers but operate at a significantly reduced

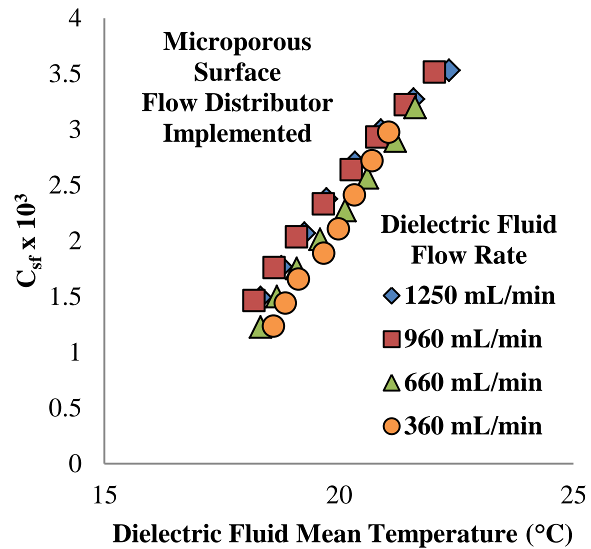


Figure 99 – C_{sf} variation for the microporous surface with the flow distributor integrated

temperatures than what these more conventional cooling methods can offer.

In an effort to compare the performance of the cartridge with and without the flow distributor, a thermal resistance network to characterize behavior at various heat fluxes was generated. The measured power dissipated by the primary die forms the denominator of the proposed thermal resistance network, while the driving temperature difference in the numerator is that between the average surface temperature of the primary die and the chilled water header outlet temperature. The variation of this system level thermal resistance as heat flux to the primary die is varied is presented in Figure 100 for both the bare silicon and microporous surfaces. As will be supported with PIV analysis in Section 5.7, the effect of the flow distributor is minimal on the thermal performance of the die from a system level perspective. The thermal resistance plateaus illustrated in the results of Figure 100 support the claim that the system is at

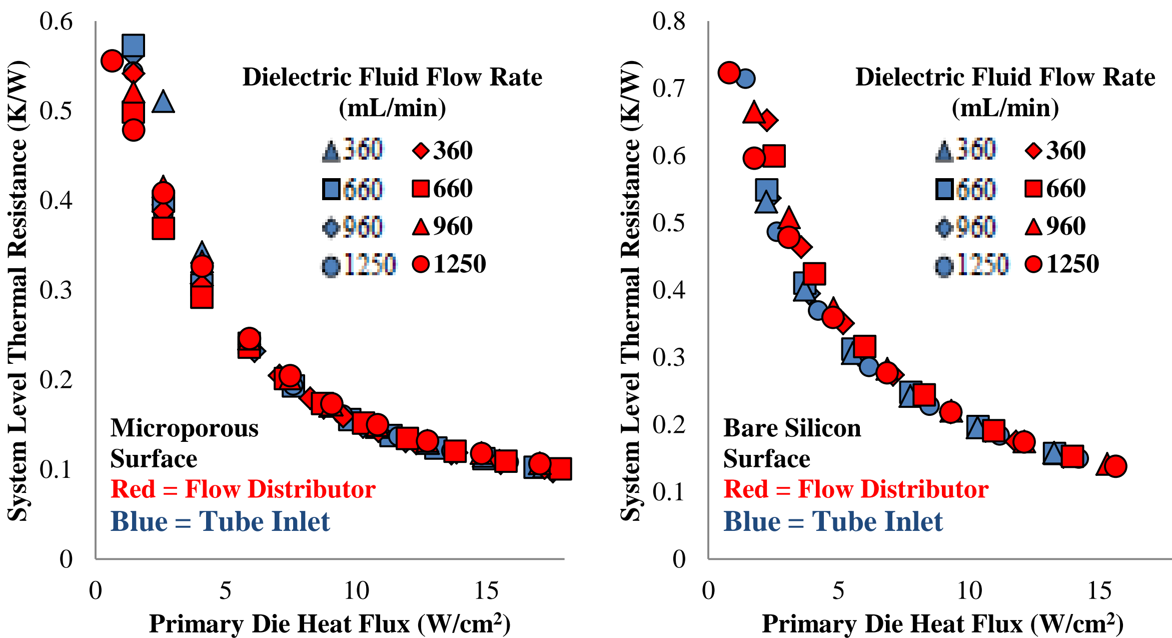


Figure 100 – Flow distributor performance from a thermal resistance perspective

or near the maximum capabilities of the cartridge under these conditions. Final system level thermal resistances attained for the bare silicon surface is 0.14 K/W while that of the microporous surface is 0.10 K/W, less than the values found previously for these surfaces under pool boiling conditions as expected.

5.6 Passive Element Effect on Flow Boiling Thermal Performance

It is understood that there will inevitably be other elements, potentially completely inactive from a power perspective or only moderately power dense such as a DIMM, which must be housed in a server module besides processing chips. The thermal performance of these primary elements acting in isolation has been studied extensively throughout the course of the current study's results thus far. However, this section seeks to illustrate how passive and moderately powered elements can impact and improve performance trends and benchmarking of a two-phase liquid immersion cooled system. This information is important for the packaging engineer as input from the experiments presented in this section will seek to guide decisions regarding the placement and integration of these auxiliary and necessary elements in close proximity to the most important and power dense elements within a server.

5.6.1 Flow Guide Integration Effects on Flow Boiling Performance

Flow guides of various heights have been incorporated into the cartridge assembly, and the primary heated elements have undergone a number of flow boiling tests while varying the flow guide height as well as the dielectric fluid flow rate with the maximum flow guide integrated. The details regarding the construction and implementation of these flow guides can be found in the Passive Element Integration Effects section (Section 4.8), with a specific focus

Table 9 – Passive Element Integration Flow Boiling Thermal Performance Summary

	Bare Silicon Surface			
Flow Guide Elevation Height	None	0.75”	1.50”	2.25”
Heat Flux (W/cm^2)	19.2	19.0	18.6	19.8
Average Base Surface Temperature (°C)	74.6	73.5	73.5	75.3

Maximum Flow Guide Implemented	Bare Silicon Surface			
Dielectric Fluid Flow Rate (mL/min)	360	660	960	1250
Heat Flux (W/cm^2)	14.0	15.7	18.0	19.8
Average Base Surface Temperature (°C)	74.3	74.2	74.7	75.3

on the illustration shown as Figure 68. Only the bare silicon surface has been tested for the results presented in this section. A summary table of the maximum heat flux achieved for each condition along with its corresponding average surface temperature is presented as Table 9. With the flow guides implemented, the bare silicon surface for the first time in the current study has exceeded 19 W/cm^2. This is noteworthy not simply just from the benchmarking of the bare silicon surface within the cartridge assembly, but as will be shown drives new trends at these higher heat fluxes that have yet to be seen thus far in the current study.

The highest heat fluxes for the bare silicon surface were achieved consistently throughout the flow guides implemented with the largest flow rate, 1250 mL/min, being forced through the cartridge as shown in the top table of the summary results presented in Table 9. While only decreasing data was taken for these experimental runs, it was assumed that the last eight data points could be considered in the fully developed regime, or at least were worth analyzing from a C_{sf} perspective. The results for the variation of the flow guide scenario, presented as Figure 102, show an intriguing development at the highest

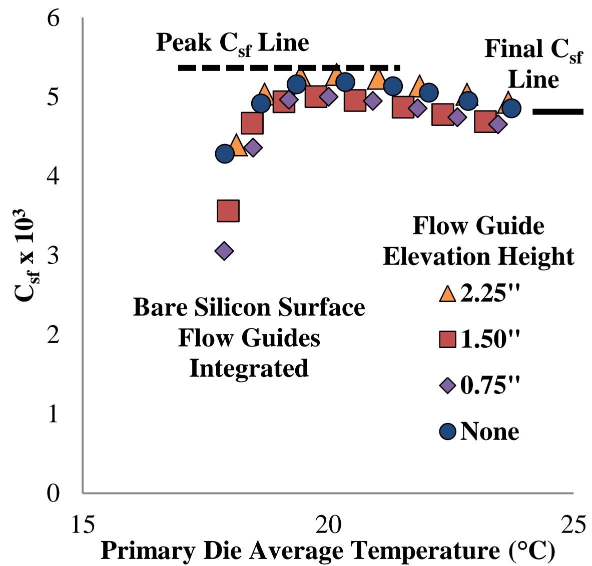


Figure 102 – C_{sf} variation over different flow guide designs with the bare silicon surface

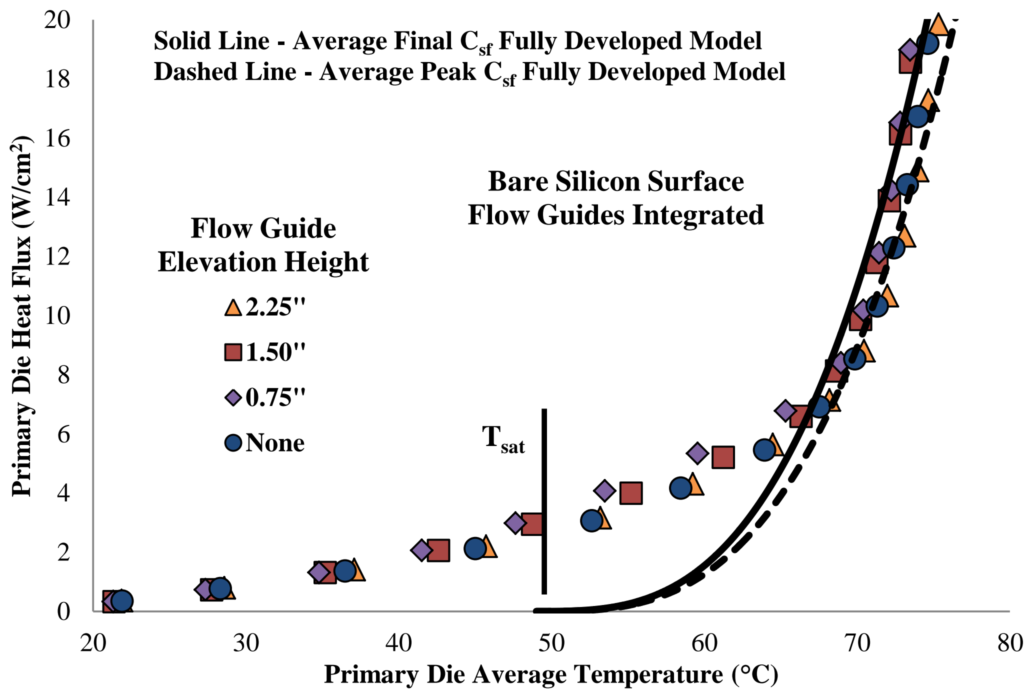


Figure 101 – Decreasing heat flux data for the bare silicon surface as flow guide elevation height is varied

heat fluxes. For all of the previously reported flow boiling data, there seemed to be a solid convergence on a fully developed line for all of the flow rates. In these results, the data seem to peak and then lower slightly past the 17 W/cm^2 mark, which was close to the previous highest heat flux recorded. At first glance, it would appear that perhaps this is the beginning of the region, experimentally determined by Sridhar [51], leading up to a burnout event where heat transfer coefficients begin to decline. By isolating the heat transfer coefficient out of the Rohsenow correlation, Equation 4, a decrease in the C_{sf} value would lead to a steeper curve and thus higher heat transfer coefficients. For further justification that CHF is not looming, calculations using the Zuber correlation [46] that incorporates subcooling, presented as Equation 20, estimated CHF at roughly 40 W/cm^2 for the nearly 26K of subcooling still at play at these higher heat fluxes. The highest measured heat fluxes for this scenario are at roughly 50% of the predicted CHF value. Increased mean dielectric fluid temperatures, and the corresponding reduction in subcooling, at these higher heat fluxes would drive the C_{sf} higher and shift the boiling curve to the right as shown in Figure 83. What ultimately makes this region of more interest is that it is marked by a decrease in C_{sf} and thus increase in heat transfer coefficient,

$$q''_{CHF} = 0.16 * \rho_v * h_{lv} * \left[\frac{g*\sigma*(\rho_l - \rho_v)}{\rho_v^2}\right]^{0.25} * \left\{1 + 5.32 * \left[\frac{g*(\rho_l - \rho_v)}{\sigma}\right]^{0.25} * \frac{(k_l*c_{pl}*\rho_l)^{0.5}*(T_{sat} - T_l)}{\rho_v*h_{lv}} * \left[\frac{\rho_v^2}{g*\sigma*(\rho_l - \rho_v)}\right]^{0.125}\right\} \quad (20)$$

making it an excellent candidate for future study, further analysis and potential improvement of the overall thermal performance at these higher heat fluxes. The decreasing heat flux data for this flow guide variation scenario with the bare silicon surface implemented and a dielectric fluid flow rate of 1250 mL/min is presented as Figure 102. In an effort to show the effects of the slight change in C_{sf} evident in this region along with the resulting change in slope, theoretical fully developed boiling Rohsenow curves based on the average of the peak C_{sf} recorded for each dielectric fluid flow rate is illustrated by the dashed line while the average of the final value for each dielectric fluid flow rate is illustrated by the solid line on Figure 101.

Much in the same way that the maximum flow guide was of particular interest in the Passive Element Integration Effects section (Section 4.8) for pool boiling, it was studied in greater detail for the flow boiling scenario as well. C_{sf} analysis of the heat fluxes leading up to the maximum value recorded as the diel ectric fluid flow was varied between `experimental runs is documented as Figure 103. From the data in Figure 103, it is seen that the same peaking trend evident throughout the flow guide heights at the maximum flow rate shown in Figure 102 is on display at all of the flow rates except there is a noticeable deviation with the lowest flow rate tested. This lowest dielectric fluid flow rate, 360 mL/min, exhibits the same peaking trend as all of the other C_{sf} convergence trends evident in the other dielectric fluid flow rates tested under flow boiling conditions. The only difference

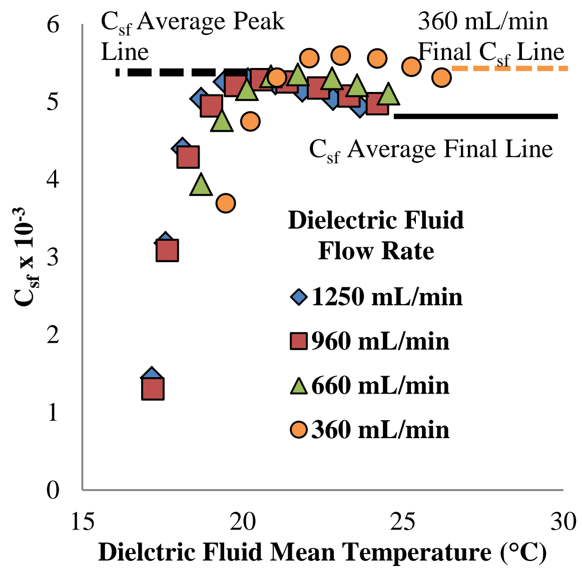


Figure 103 – C_{sf} variation with the maximum flow guide implemented over various dielectric fluid flow rate runs

in this flow rate from the others tested is the sharp divergence in the linear trend of mean dielectric fluid flow rate increase as heat flux is increased as shown in Figure 78. It has also been shown that at this lowest flow rate, the influence and importance of the chilled water header becomes more apparent as shown with the Chilled Water Header Performance Factor variation data in Figure 88. It is unclear what the fundamentals are driving the decrease in performance found at this lower flow rate with the flow guides implemented, but it appears again that there is an increase in performance through the change in the slope of the fully developed boiling curve occurring at higher heat fluxes occurring in tandem with flow guide integration. This is not to suggest that the flow guide integration has allowed the climbing to higher heat fluxes, it may be

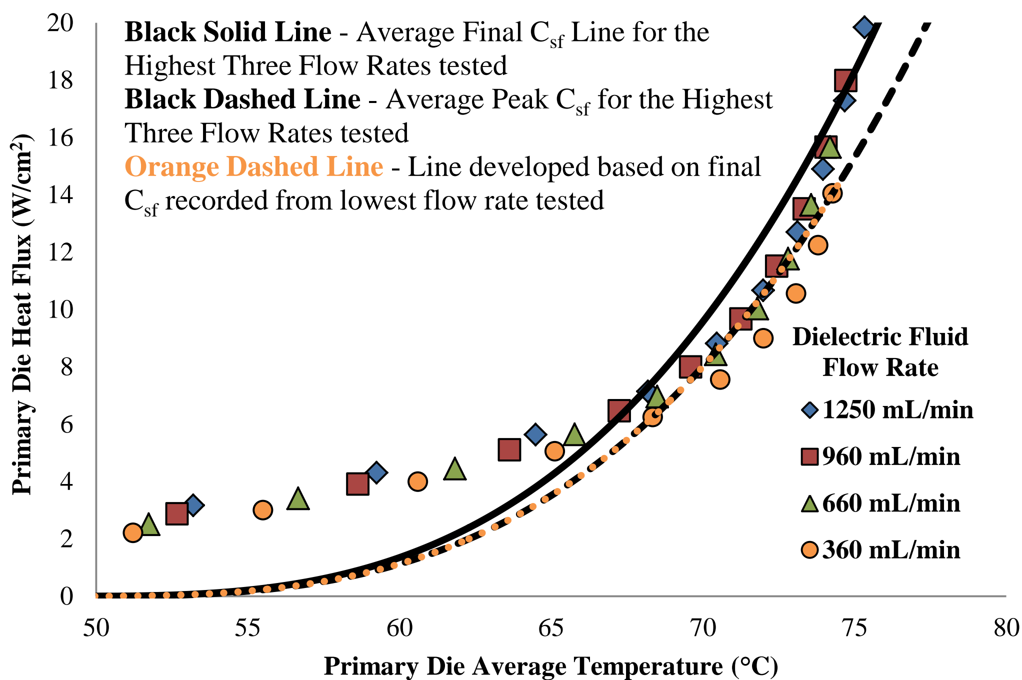


Figure 104 – Decreasing heat flux data for the bare silicon surface with the maximum flow guide integrated over various dielectric fluid flow rate runs

that the cartridge could have been driven to higher heat fluxes for the other design scenarios as well under flow boiling conditions. Thermal performance could have traveled further into the thermal resistance plateau documented for the heat fluxes recorded for all of the other design

scenarios tested under flow boiling conditions. It also could be that the vapor generated at this heat flux, working in tandem with the surrounding flow guide geometry, causes a slight shift in flow dynamics surrounding the boiling surface. This change in the ambient flow characteristics could have a positive effect on heat transfer at the surface through a resulting change in bubble formation and departure characteristics. High speed microscopic imagery analysis as well as two-phase PIV experiments could yield some insight as to what is causing this change in performance. Whatever the case may be, this increase in performance at higher heat fluxes with the flow guides implemented is worth future work to determine if it is in fact the flow guides driving this increased performance. Decreasing heat flux data for the bare silicon surface with the maximum flow guide implemented over various dielectric fluid flow rate experimental runs is shown as Figure 104. Just as with the data presented in Figure 101, Rohsenow curves have been developed based on the average peak and average final C_{sf} values from the data presented in Figure 104, shown as dashed and solid black lines respectively. In addition, to highlight the divergence associated with the lowest flow rate tested, a color coded dashed line has been added to correlate that data based on its final C_{sf} value.

The pumping power required to deliver coolant within the cartridge is an important parameter to at least get a rough order of magnitude for if any future implementation of the technology presented in the current study is to be conducted. By measuring the pressure drop across the cartridge with a strategically placed differential pressure sensor across the cartridge as shown in Figure 33 along with the dielectric fluid flow rate with the flow meter shown in the same schematic, an ideal pumping power can be calculated by the product of these two numbers. The variation of the differential pressure across the cartridge with respect to the power dissipation applied to the primary die is shown as Figure 105. Evident from this data is the expectation that by increasing the dielectric fluid flow rate, the pressure drop increases. Interestingly however, even though vapor is being generated at the highest power dissipations, the pressure drop remains constant owed in large part to the complete condensation of the vapor upon leaving the cartridge, i.e. exit quality is unity. Furthermore, a simple latent heat analysis shows that even at peak power load, and assuming that all heat

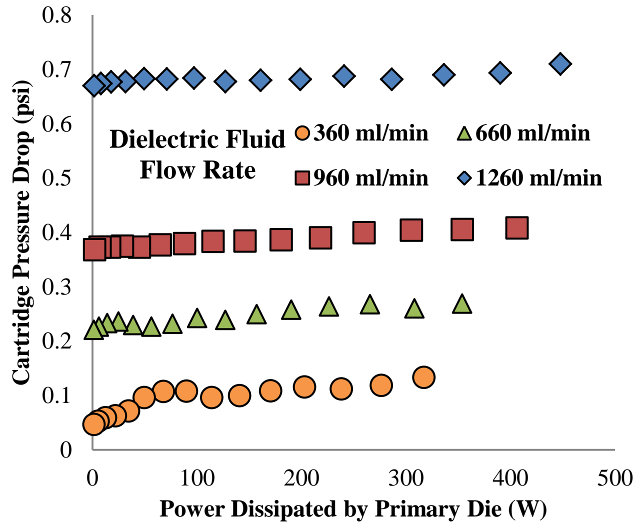


Figure 105 – Pressure drop across the cartridge with the maximum flow guide implemented under flow boiling across the bare silicon surface

Table 10 – Ideal pumping power required to deliver fluid through the cartridge with the maximum flow guide implemented

DF Volumetric Flow Rate (mL/min)	Max Pressure Drop (psi)	Ideal Pumping Power (W)	Maximum Power Dissipation (W)
360	0.13	0.0054	317
660	0.27	0.020	354
960	0.41	0.045	406
1260	0.71	0.10	447

$$Peak\ Load = 448\ W = 448\ \frac{J}{sec} * \frac{kg}{87956\ J} * \frac{m^3}{1517\ kg} * \frac{1\ mL}{1\ x\ 10^{-6}\ m^3} = 3.4\ \frac{mL}{sec}\ or\ 201\ \frac{mL}{min}$$

transferred is through latent heat exchange which is an overestimate considering that there is a great deal of convection occurring at the microlayer between the bubble and the surface, only 3.4 mL/sec or 201 mL/min of dielectric fluid flow is required to quench the surface. The details of this analysis are provided above. This value is below even the lowest flow rate tested with the overestimates made in the rough order of magnitude analysis for fluid required to quench the surface. A table showing the maximum ideal pumping power required for each dielectric fluid flow rate tested is presented as Table 10. It is understood that there is more power required to actually deliver the coolant to the cartridge, but the values presented in this table are presented to give a rough estimate on a per cartridge basis of the pressure drop and thus power needed to send coolant through the cartridge under flow boiling conditions with the bare silicon surface integrated.

5.6.2 Maximum Power Dissipation Recorded

Implementation and understanding of the effects of moderately powered devices, such as DIMM's, within an electronics enclosure is critical to the successful implementation of two-phase liquid immersion cooling technology in the

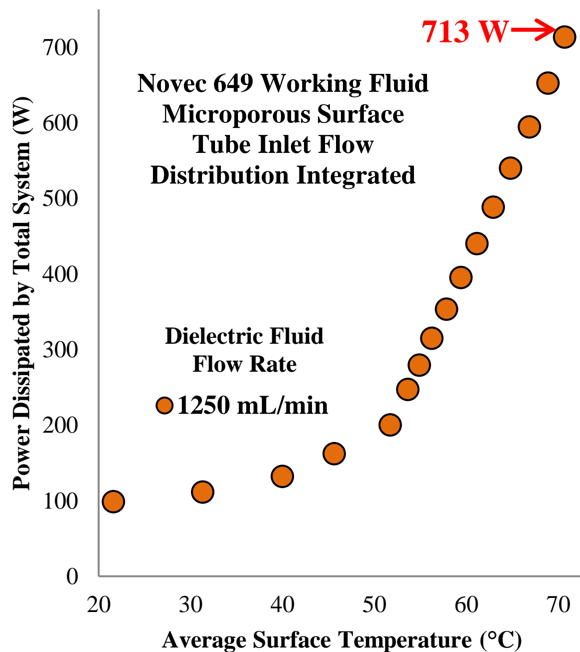


Figure 106 – Maximum power dissipation recorded by the experimental facility

future. With these smaller more slender rectangular heated elements shown to the left and right of the four primary die on the diagram shown as Figure 32 heated to 90 W of total power dissipation, a total system level power dissipation of over 700 W was achieved with the tube inlet flow distribution design implemented and the microporous surface being used. The thermal performance data for the decreasing portion of the experimental run is shown as Figure 106. This total power dissipation, achieved at a comparatively modest surface temperature of only 71°C, is significant as it represents the computational power of high end 1 Rack Unit sized server devices at less than a quarter of the volume. In addition to the increase in reliability achieved by the use of the microporous surface, the data center size itself can be reduced dramatically with the implementation of more volumetrically power dense thermal management solutions such as that presented in the current study.

5.7 Single Phase PIV Analysis

As the use of two-phase liquid immersion cooling technology becomes more widespread, fundamental questions regarding how flow is distributed within an electronics enclosure are sure to arise. The single phase analysis seeks to provide an experimental technique and analytical method of determining how effective flow distribution designs are at diverting flow over its intended target. The lack of availability of two-phase particles as well as their cost made them prohibitive to use in the flow boiling scenario. Particles

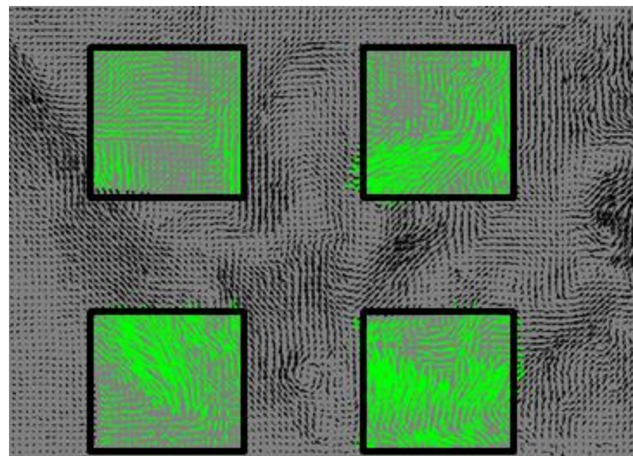


Figure 107 – Highlighted vector set used for single phase PIV analysis

sticking to elements within the dielectric fluid flow loop such as the liquid-liquid heat exchanger and associated fluid delivery tubing made it impossible to implement the precious two-phase particles at this point in the experimental technique development.

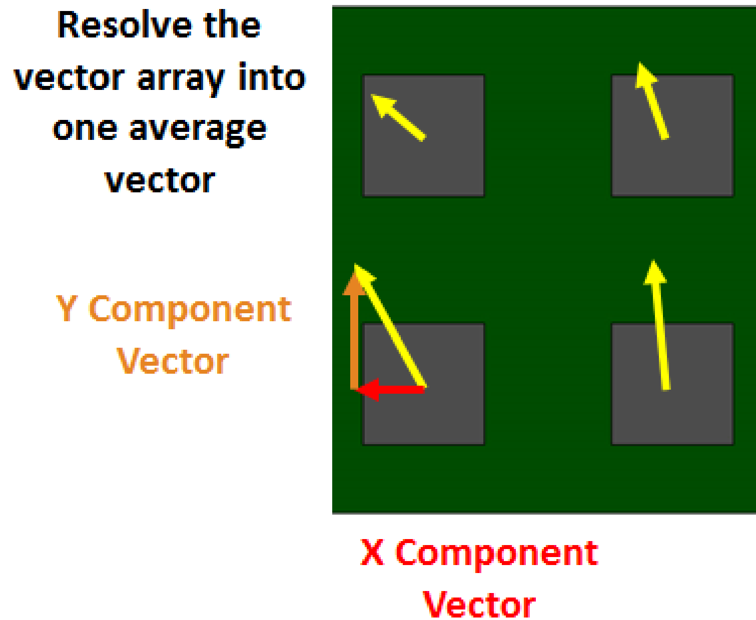


Figure 108 – Resolution of vector set over each of the four primary die for single phase PIV analysis

Details regarding particle selection, associated slip velocities, laser/camera setup and orientation as well as the algorithm used to generate the vector sets for analysis are discussed in the PIV Setup and Execution section (Section 3.4). The focus of this section is the explanation of the method used to single out vectors within the generated vector maps for applicable analysis in order to answer practical questions sure to arise in the near future as this thermal management solution matures commercially. As it is the purpose of the current study to

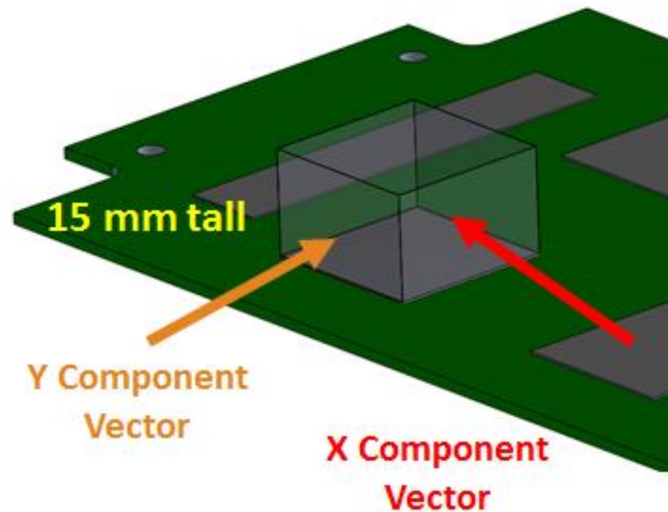


Figure 109 – Resolution of the mass flow rate near the four primary die for single phase PIV analysis

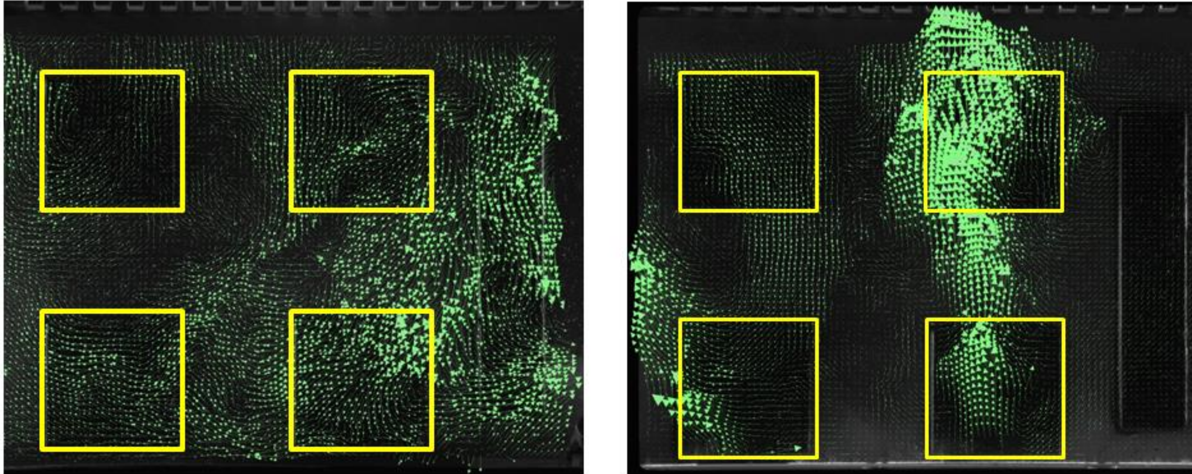


Figure 110 – Sample PIV vector sets from the tube inlet (left) and flow distributor (right) designs

understand how effective the proposed flow distribution methods and passive element locations are at diverting flow over the four primary die of most concern, the vectors directly over these primary elements are highlighted in the algorithm for further analysis. A sample image showing these highlighted vector locations is shown as Figure 107. Vector maps like those shown by Figure 107 are taken at three slices at locations normal to the primary heated elements. The first slice is taken as close as possible to the bare silicon die so as to not obstruct the laser sheet with their height. The second slice is taken 5 mm away from the first and the last is taken 5 mm away from the previous. The near and the middle slice vectors are averaged, and the middle and the far slice vectors are averaged. These vectors are then resolved into one single vector over each die as shown in Figure 108. The x-component and the y-component of the resolved vectors, shown as red and yellow respectively in Figure 108, are used in a u·dA analysis over the surface area traversed by the vector slices resulting in a square tube over each die as shown in Figure 109. This surface area was chosen arbitrarily and does not represent any assumptions about the development, location or size of the velocity boundary layer in these areas. The analysis is meant to be comparative between the flow distribution designs and passive element locations

studied. Development of information regarding the flow within the device beyond this is outside of the scope of the current work but is a suitable candidate for future work.

Using this analysis, the tube inlet and flow distributor designs are compared for their effectiveness at delivering fluid over the four primary heated elements. Sample vectors maps with the four primary die highlighted in yellow are provided as Figure 110 to give a rough idea of the flow distribution across the die as well as generate an expectation for the results of the analysis. In looking at the flow distributor image to the right of Figure 110, it appears that the right slot of the flow distributor, shown in the image to the right of Figure 39, does a good job of delivering flow to the right most column of primary die. The left most column of primary die still seem like they are not getting a good amount of flow distribution, a topic central to the next analysis presented regarding passive element locations.

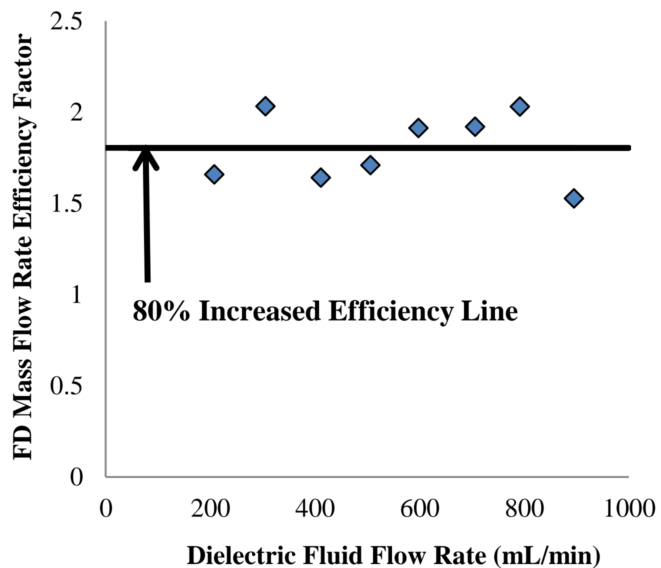


Figure 111 – Flow distributor effectiveness at delivering fluid to the four primary elements over the tube inlet design

It does appear from the image set that the flow distributor design is doing a better job at delivering flow over the four primary heat elements and the results from the analysis prove this as well. By defining a Flow Distributor (FD) Mass Flow Rate Efficiency Factor, which is just the ratio of the mass flow rate calculated by the analysis proposed for the flow distributor over that of the tube inlet design, the flow distributor design shows an average 80% increased

effectiveness at delivering fluid over the four primary heated elements over the flow rates tested, illustrated by the plot in Figure 111. This analysis and confirmation of expectations derived from viewing the images in Figure 110 provides a baseline experimental and analytical technique at ascertaining the effectiveness of a proposed design at delivering fluid to a user defined intended target.

In an effort to address the ineffectiveness of the flow distributor at delivering fluid to the left most column of primary heated elements evident from a viewing of the right image in Figure 110, the same analysis was conducted to compare the ability of the tallest flow guide, depicted as the 2.25" tall element in Figure 68, to distribute flow over the four primary die to that of the flow distributor. Sample PIV vector maps are offered in Figure 112 as a side by side comparison of the two general flow distributions within the cartridge. While the right most column still appears fairly well covered, the top left die still appears bare in both flow distribution methods. It

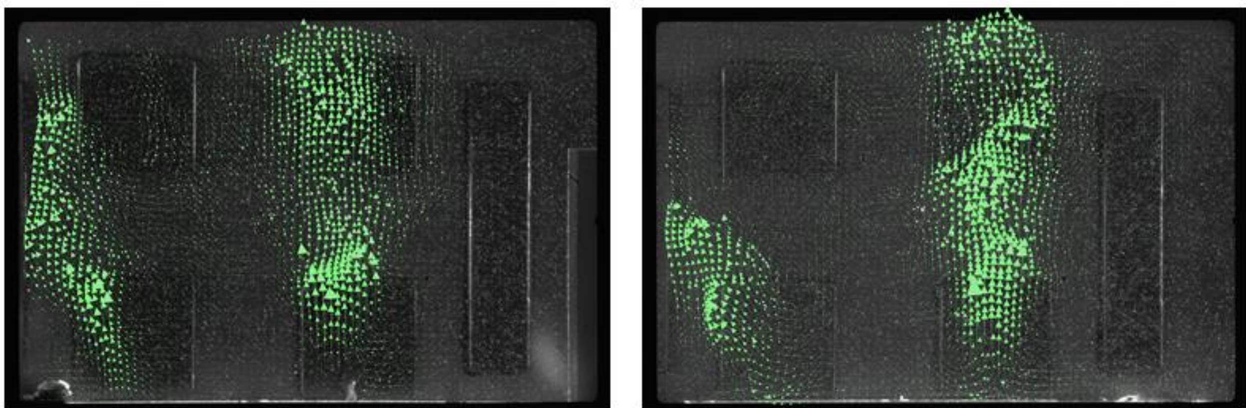


Figure 112 – Sample PIV images of the flow distributor (right) and that of tallest flow guide implemented (left)

appears that the improvements from one flow distribution to the next are negligible. This is the is the result that the proposed analysis concludes as well, presented in Figure 113 as the Flow Guide Mass Flow Rate Efficiency Factor. This factor is the mass flow rate yielded by the

analysis for the tallest flow guide implemented versus that of the flow distributor. The analysis confirms what is qualitatively assessed from the sample images presented in Figure 112.

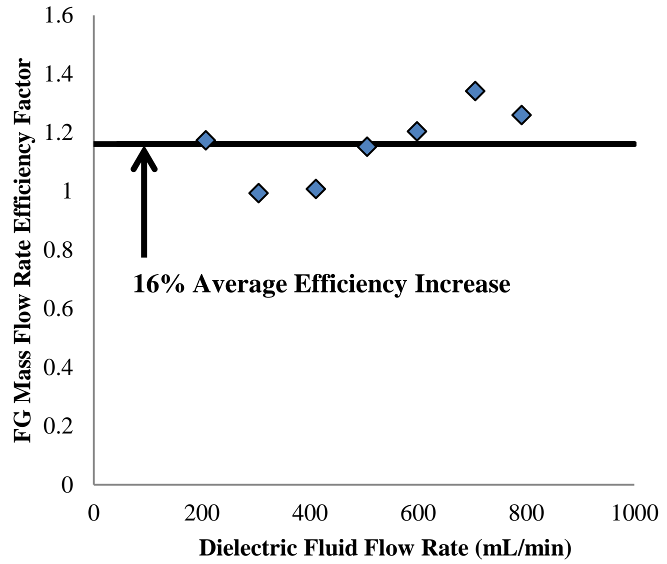


Figure 113 – Tallest flow guide effectiveness at delivering fluid to the four primary elements over the flow distributor design

Chapter 6: Conclusions

Interest in the advancement of the art of electronics thermal management is rising and will only continue to do so as consumer demands and environmental constraints mandate that modules become more compact and efficient. The preceding study offers a historical perspective into how the field has gotten to where it is today, current industrial and research trends that are pushing the community towards more thoughtful and improved thermal engineering, along with a proposed facility designed to capitalize on the theories of predecessors and contemporaries alike to construct a small form factor high performance two-phase liquid immersion cooled module capable of effectively integrating a wide variety of current and near term power dense electronics safely and reliably. The modular LRU design occupies a volume of 150 mm x 300 mm x 38 mm (H x L x W) capable of dissipating over 700 W of heat at operating temperatures in the low 70 degree Celsius range. This is less than a quarter of the volume of a one RU server capable of dissipating similar heat loads thermally managed by conventional air cooling methods, resulting in orders of magnitude increases in volumetric power dissipations, leading to more compact systems and smaller data centers. The drastically reduced operating temperatures presented in the current study represent significant increases in reliability of the system, leading to reduced overhead costs in replacement equipment. Additionally, liquid is generally much easier to distribute than air, both in terms of efficiency and infrastructure required. The latter point is particularly important as over half of the construction cost for a new data center is allocated to building and installing the cooling system alone.

Not only are these improvements being seen in the laboratory, but they are finding their way into the industry as well. There are a number of liquid immersion cooled installations being installed around the world and reporting incredible efficiency numbers along with improved reliability stemming from reduced operating temperatures. While the industry has pushed forward with this technology and will continue to do so given the improvements already attained, engineering problems are sure to arise that will need to be studied fundamentally. This dedication and necessity for fundamental studies has and is being conducted for the more accepted and conventional form of data center thermal management, namely air cooling. With this expectation in mind, the preceding study offers a number of fundamental conclusions about a facility, that while it was in a laboratory setting, was designed to implement many elements that are industry-ready. Therefore, the results and conclusions drawn from the trends recorded are applicable to a practical implementation of the proposed thermal management solution.

The facility was subjected to a number of two-phase and single-phase experiments, where thermal test cells contained within the electronics enclosure were heated and not heated, to extract critical information useful on its own merit but found even more so with the implementation of several novel analytical techniques. The bulk of these useful analytical techniques were those applied to PIV data taken. Using vector maps extracted from PIV software, control surface analyses done in proximity to critical elements within the enclosure gave insight into the effectiveness of flow distribution designs. The most novel of these techniques however came from experimentation and results extracted from the use of a heretofore unused application of a two-phase PIV particle in a dielectric fluid. While boiling, it is perhaps even more crucial to understand flow dynamics within an electronics enclosure as quenching fluid flow paths must be maintained to prevent catastrophic thermal failure of the

system. During boiling, fluid flow paths were captured from vector maps determined from image capture of this fluorescent particle's motion within the two-phase working immersion fluid. Using similar control surface analyses, mass flow rate trends were established of the liquid flowing to these critical elements. By discretizing the control surface analysis around the periphery of the boiling surfaces, color coded maps were generated illustrating the points at which fluid was entering and leaving the area surrounding these critical elements, as typically any element power dense enough to drive boiling is of the most critical nature in an electronics package. This discretized flow map analysis is an important tool for the advancement and integration of this technology into practice as it is vital to understand how flow is being received by the boiling surfaces in order to understand where to place the other less power dense or completely inactive elements that must occupy the board.

Experimental investigation has been conducted and fundamental conclusions have been drawn about the low-end and high-end of the thermal performance for elements that are contained in a cartridge using a two-phase liquid immersion cooled approach. Heat fluxes as high as 19.8 W/cm^2 under flow boiling conditions and as high as 12.6 W/cm^2 have been achieved while boiling from a bare silicon chip, thus reducing the manufacturing complexities associated with the attachments of heat sinks and spreaders. With the use of surface enhancements however, heat fluxes as high as 23.4 W/cm^2 have been achieved under flow boiling conditions with a modest surface temperature of only 67.5°C. This level of operating temperature reduction can yield substantial gains in system reliability over conventional air cooled devices which can have chip operating temperatures anywhere from 85°C-105°C. The heat flux numbers quoted previously for the bare silicon were achieved at surface temperatures of 75.3°C and 79.2°C, respectively. This illustrates the possibility of increasing both reliability and reducing

manufacturing complexity with the implementation of a thermal management solution such as that proposed in the current study. A pool boiling system level thermal resistance as low as 0.13 K/W was attained with the use of microporous surface enhancements, and this number was dropped even further to 0.10 K/W once dielectric fluid flow was introduced into the system. Rivaling many high performance 1RU servers, a maximum power dissipation of 713 W was achieved in a quarter or even an eighth of the volume of an equivalent conventionally air cooled server module. Furthermore, even at this maximum power dissipation, the average surface temperature was kept at 70.7°C. Analyses of the trends of temperature overshoot, just one of the many hysteretic points associated with boiling, have been conducted in order to ascertain under what conditions and by how much temperatures can be expected to rise above the fluid's saturation temperature before the system takes advantage of the incredible heat transfer coefficients associated with two-phase heat transfer. Fundamental explanations regarding the influence of natural and forced convection in the lower heat flux regimes have been explored. Even though fluid may be forced through the cartridge under what one may consider as a flow boiling scenario, it is important to look at important governing parameters, such as the Richardson number, to get an expectation as to the performance of not only the primary elements expected to eventually boil once past incipience, but also how other passive, less power dense elements will be affected by this regime and heat transfer mechanism. While the use of the C_{sf} values calculated in this study should be used with caution, as these are very surface and fluid specific, the analysis of the trends associated with this value leading up to the maximum heat flux attained has shown some fundamental agreement with historical works but also added to the debate as to whether C_{sf} is affected by subcooling. The results of this study show that this value is in fact affected slightly by subcooling, but again, given the nature of the highly specific

association of C_{sf} to fluid surface combinations, must be understood that this conclusion was drawn with a bare silicon surface and Novec 649. Other fluid surface combinations may not yield this same trend. The more interesting conclusions associated with this C_{sf} analysis is the convergence at the high end on a single value, as fundamentally expected and supported by historical works, but the slight increase in performance by the reduction of this value at the highest heat flux tested once flow guides were implemented. It is unclear as to what is driving this improved thermal performance associated with the reduction in C_{sf}, but is an excellent candidate for future work as improved performance at higher heat fluxes is a success that could be had on two fronts.

The limitations of the proposed experimental facility are not found on the boiling end but on the condensation end. This concept of condensation limitation is not a new one, but the published results associated with a practically oriented experimental facility as well as introduction of the phenomenon as a potential roadblock to future integration of such a compact form of this thermal management technology is of vital importance for the community moving forward. More improved capabilities on the condensation heat transfer side of the system's design are critical moving forward. For example, with the surface enhancement used, maximum heat fluxes that are on the order of a half to a third of the maximum heat fluxes recorded by other researchers using the same surfaces were attained when integrated into the proposed experimental facility. Again, it wasn't that the boiling surface couldn't handle the heat fluxes, it was that the condenser couldn't pull the heat out of the system. A model for predicting the condensive limit for the Novec 649 and FC-72 fluids used in the current study under pool boiling conditions is offered, showing good agreement with the results for Novec 649 and marginal agreement with the limitations yielded by FC-72. It was very inadequate at predicting the

performance of both the microporous and microfinned surfaces used. The most likely reason for this is the effect of sloshing at the condensive surface and the necessity for incorporating transient conduction into the model to ascertain how much heat is being gained when the liquid cleans the condensive surface from the volatility of the liquid-vapor interface induced by the vigorous nature of the boiling taking place below. To provide further support for this point, the condensive limit yielded by the surface enhancements, designed to initiate and sustain more vigorous boiling, were underpredicted by the proposed model. The proposed model offers a baseline to address and predict this limitation moving forward but must incorporate these elements in order to more accurately predict the maximum range of operation for this technology.

The information presented in this study offers analytical techniques and fundamental conclusions to address practical questions that have arisen or will surface as this thermal management solution gains more of a foothold in the community. The application of PIV to characterizing the performance of flow distribution and management techniques to critical elements within an electronics enclosure is a novel and useful tool for the thermal engineering community to utilize. The trends associated with the condensive limit of this practically oriented experimental facility are important pieces of information for the community to understand when addressing the operating capabilities of this technology. It also provides an excellent platform for future work to extend the capabilities of systems such as these even further by enhancing heat transfer on the condensation side. The study also emphasizes the importance of understanding basic flow parameters and considerations when predicting theoretical thermal performance limits of two-phase thermal management systems. The power density of near term electronics will overwhelm air cooling systems, mandating that the highest performing electronics must be liquid

cooled in some form. While 3D and 2.5D chip stacks are sure to need some sort of embedded thermal management solution in the long term, this technology offers the bridge to adequately maintain today's highest performing chipsets. The fundamental assessment and study of a practically oriented two-phase liquid immersion cooled system such as that proposed in the current study offers valuable insight to the thermal management community looking to address the perpetually growing problem of power density in high performance computing applications.

Bibliography

[1] United States Census Bureau, “E-Stats 2013: Measuring the Electronic Economy”, U.S. Department of Commerce Economics and Statistics Administration, 2015, Available: http://www.census.gov/econ/estats/e13-estats.pdf.

[2] International Monetary Fund, "World Economic Outlook Database", April 2015, Available: http://www.imf.org/external/pubs/ft/weo/2015/01/weodata/index.aspx.

[3] Emarketer, "B2C Ecommerce Sales Worldwide, 2012-2017," Jan 2015, Available: http://www.emarketer.com/Article/Global-B2C-Ecommerce-Sales-Hit-15-Trillion-This-Year-Driven-by-Growth-Emerging-Markets/1010575.

[4] Intel, "What Happens in an Internet Minute," 2014, Available: http://www.intel.com/content/www/us/en/communications/internet-minute-infographic.html.

[5] Mills, Mark P., “The Cloud Begins with Coal,” August 2013, Available: http://www.tech-pundit.com/wp-content/uploads/2013/07/Cloud_Begins_With_Coal.pdf?c761ac.

[6] DatacenterDynamics, "Powering the Datacenter," 2013, Available: http://www.dcd intelligence.com/Products-Services/Powering-the-Datacenter.

[7] United States Energy Information Administration, “International Energy Outlook 2013,” 2014, U.S. DOE, Washington, DC, Rep. DOE/EIA-0484(2013)..

[8] Info-Tech Research Group, "Typical Data Center Energy Consumption," 2010, Available: http://blog.opower.com/tag/data-centers/.

[9] Iceotope, "New cooling technique supercharges IT performance, reveals Iceotope study," 2014, Available: http://www.businesscomputingworld.co.uk/news/pressrelease/new-cooling-technique-supercharges-it-performance-reveals-iceotope-study/.

[10] C.D. Attlesey, "Case and rack system for liquid immersion cooling of electric devices connected in an array," 2012, Jan 3, Patent US 8,089,764 B2..

[11] LaMonica, M., "Intel servers take a deep dive to cool off," 2012, Available: http://www.technologyreview.com/view/429179/intel-servers-take-a-deep-dive-to-cool-off/.

[12] A. Becker, "Bitcoin Mining Boosts Interest in Liquid Cooling," Dec. 2013, Electronics Cooling. Available: http://www.electronics-cooling.com/2013/12/bitcoin-mining-boosts-interest-liquid-cooling/.

[13] R. Miller, “New from 3M: Boiling Liquid to Cool Your Servers,” April 2014, Data Center Knowledge, Available:

http://www.datacenterknowledge.com/archives/2014/04/09/new-3m-boiling-liquid-cool-servers/.

[14] Google, "Efficiency: How We Do It," 2015, Available: http://www.google.com/about/datacenters/efficiency/internal/.

[15] R. Eiland, J. Fernandez, M. Vallejo, D. Agonafer and V. Mulay, “Flow Rate and Inlet Temperature Considerations for Direct Immersion of a Single Server in Mineral Oil,” in Proc. of the 14th intersociety on thermal and thermomechanical phenomena (ITHERM), 2014.

[16] Facebook, "Prineville Data Center," 2015, Available: https://www.facebook.com/PrinevilleDataCenter/app_399244020173259.

[17] M.K. Khattar, "Free Cooling for Data Center," Oct 2014, ASHRAE Journal, pp. 60-68.

[18] Energy Star Program, "Report to Congress on Server and Data Center Energy Efficiency Public Law 109-431," Environmental Protection Agency, Aug 2007, Available: https://www.energystar.gov/ia/partners/prod_development/downloads/EPA_Datacenter_Report_Congres, s_Final1.pdf.

[19] M. Iyengar and M. Ellsworth Jr., "Energy Efficiency Analyses and Comparisons of Air and Water Cooled High Performance Servers," in proceedings of ASME 2009 InterPACK Conference, July 2009, San Francisco, CA, pp. 907-914.

[20] J. Gu, "Health Assessment and Prognostics of Electronic Products: An Alternative to Traditional Reliability Prediction Methods," Electronics Cooling, May 2009, Available:http://www.electronics-cooling.com/2009/05/health-assessment-and-prognostics-of-elec, tronic-products-an-alternative-to-traditional-reliability-prediction-methods/.

[21] Anthes, G. (2005, August 22). Power Play: The Search for Energy-Efficient Chips. Computerworld. Retrieved from http://www.computerworld.com/s/article/104017/Power_Play.

[22] A. Bar-Cohen, 2013, “Needs and Future Trends for Enhanced Phase Change Heat Transfer-DARPA,” Powerpoint presentation, International Workshop on Micro and Nano Structures for Phase Change Heat Transfer, Needham, MA, from http://micronano.mit.edu/presentat, ions/Bar-Cohen.pdf.

[23] W. Nakayama, “Heat in Computers: Applied Heat Transfer in Information Technology,” 2014, J. of Heat Transfer, vol. 136, no. 1, p. 013001-1.

[24] R.E. Simons, "Direct Liquid Immersion Cooling for High Power Density Microelectronics," May 1996, Electronics Cooling, Available: http://www.electronics-cooling.com/1996/05/direct-liquid-immersion-cooling-for-high-power-density-microelectronics/.

[25] D. Prucnal, "Doing more with less: Cooling computers with oil pays off," 2013, The Next Wave, Vol. 20. No. 2, Available:

https://www.nsa.gov/research/tnw/tnw202/article4.shtml.

[26] G.E. Moore, "Cramming more components onto integrated circuits," 1965, Electronics, Vol. 38, No. 8.

[27] A. Huang, "The death of Moore's Law will spur innovation," Mar 2015, IEEE Spectrum, Available: http://spectrum.ieee.org/semiconductors/design/the-death-of-moores-law-will-spur-innovation.

[28] J. Hruska, "Intel at ISSCC: 14nm in the bag, full steam ahead on 10nm," Feb 2015, ExtremeTech, Available: http://www.extremetech.com/extreme/199636-intel-at-isscc-14nm-in-the-bag-full-steam-ahead-on-10nm.

[29] D. Poeter, "Gordon Moore predicts 10 more years for Moore's Law," May 2015, PC, Available: http://www.pcmag.com/article2/0,2817,2484098,00.asp.

[30] K. Azar, "The history of power dissipation," Jan 2000, Electronics Cooling, Available: http://www.electronics-cooling.com/2000/01/the-history-of-power-dissipation/.

[31] A.J. Blodgett and D.R. Barbour, "Thermal Conduction Module: A High-Performance Multilayer Ceramic Package," Jan 1982, Journal of IBM Research and Development, Vol. 26, No. 1, pp. 30-36.

[32] W. Nakayama and A.E. Bergles, "Thermal Interfacing Techniques for Electronic Equipment - a Perspective," Journal of Electronic Packaging, June 2003, Vol. 125, No. 2, pp. 192-199.

[33] R.C. Chu and R.E. Simons, "Cooling Technology for High Performance Computers: Design Applications," in Cooling of Electronic Systems, 1st ed., Dordrecht, Germany, Springer Science and Business Media, 2012.

[34] D. Blazej, "Thermal Interface Materials," Nov 2003, Electronics Cooling, Available: http://www.electronics-cooling.com/2003/11/thermal-interface-materials/.

[35] R.C. Chu, "Thermal Conduction Module," U.S. Patent 4 226 281, Jun, 11, 1979.

[36] S.R. Cray Jr., "Immersion Cooled High Density Electronic Assembly," U.S. Patent 4 590 538, Nov 18, 1982.

[37] A. Bar-Cohen, M. Iyengar and A.D. Kraus, "Design of Optimum Plate-Fin Natural Convection Heat Sinks," Journal of Electronic Packaging, 2003, Vol. 125, pp. 208-216.

[38] Intel, "Intel® Xeon® Processor E7-8893 v2 (37.5M Cache, 3.40 GHz)," Available: http://ark.intel.com/products/75260.

[39] HP, "HP Proliant DL380p Gen8 Server - Specifications," 2015, Available: http://h20564.www2.hp.com/hpsc/doc/public/display?docId=emr_na-c03235289.

[40] S. Nukiyama, "The Maximum and Minimum Values of the Heat Q Transmitted from Metal to Boiling Water under Atmospheric Pressure," 1934, Journal of Japanese Societ of Mechanical Engineers, Vol. 37, pp. 367-374.

[41] S.W. Chruchill and H.H.S. Chu, "Correlating Equations for Laminar and Turbulent Free Convection from a Vertical Plate," 1975, International Journal of Heat and Mass

Transfer Vol. 18, pp. 1323-1329.

[42] W.M. Rohsenow, "A Method of Correlating Heat Transfer Data for Surface Boiling Liquids," 1952, Transactions of ASME, Vol. 74, p. 969.

[43] B.T. Lubin, "Analytical Derivation for Total Heat Transfer Coefficient in Stable Film Boiling from Vertical Plate," 1969, ASME Journal of Heat Transfer, vol. 91, pp. 452-453.

[44] L.A. Bromley, "Heat Transfer in Stable Film Boiling," 1950, Chemical Engineering Progress, vol. 46, no. 5, pp. 221-227.

[45] S.S. Kutateladze, “On the Transition to Film Boiling under Natural Convection,” 1948, Kotloturbostroenie, 3, 10-12..

[46] N. Zuber, M. Tribus and J.W. Westwater, “The Hydrodynamic Crisis of Pool Boiling in Saturated and Subcooled Liquids,” International Developments in Heat Transfer: Proc. of the 1961-62 International Heat Transfer Conference, Boulder, CO, 1961, pp. 230-236.

[47] V.P. Carey, "Pool Boiling," Liquid Vapor Phase Change Phenomena, 2nd Ed.,Taylor and Francis, New York, NY, 2008, p. 290.

[48] J.H. Lienhard and V.K. Dhir, “The Extended Hydrodynamic Theory of the Peak and Minimum Pool Boiling Heat-Fluxes,” 1973, NASA CR 2270.

[49] A.H. Howard and I. Mudawar, “Orientation Effects on Pool Boiling Critical Heat Flux

(CHF) and Modeling of CHF for Near-Vertical Surfaces," 1999, Int. J. of Heat and Mass Transfer, vol. 42, no. 9, pp. 1665-1688.

[50] M. Arik and A. Bar-Cohen, "Effusivity-based Correlation of Surface Property Effects in Pool Boiling CHF of Dielectric Fluids," 2003, International Journal of Heat and Mass Transfer, Vol. 46, pp. 3755-3764.

[51] A. Sridhar, "Experimental Evaluation of Immersion-Cooled Strategies for High-Powered Server Modules," 2012, M.S. Thesis, Dept. of Mech. Eng., Auburn University, Auburn, AL.

[52] P.J. Berenson, "Experiments on Pool-Boiling Heat Transfer," 1962, International Journal of Heat and Mass Transfer, Vol. 5, pp. 985-999.

[53] L.C. Witte and I.H. Lienhard, "On the Existence of Two 'Transition' Boiling Curves," 1996, International Journal of Heat and Mass Transfer, Vol. 25, pp. 771-779.

[54] R. Hohl, H. Auracher, J. Blum and W. Marquardt, "Pool Boiling Transfer Experiments with Controlled Wall Temperature Transients," 1996, 2nd European Thermal Science and 14th UIT National Heat Transfer Conference, Rome, Italy, pp. 1647-1652.

[55] Markowitz, A., "Boiling and Condensation in a Liquid Filled Enclosure," 1971, Ph.D. dissertation, Dept. of M.E., MIT, Cambridge, MA.

[56] M. Iyengar,"Calculating the Heat Dissipation Rate for a Vapor Condenser Heat Sink," 2013, Electronics Cooling, Available: http://www.electronics-cooling.com/2013/09/calculating-the-heat-dissipation-rate-for-a-vapor-condenser-heat-

sink/.

[57] W. Nusselt, "The Surface Condensation of Steam," 1916, Z. Ver. Deut. Ing, Vol. 60, pg. 541-569.

[58] W.M. Rohseonw, "Heat Transfer and Temperature Distribution in Laminar Film Condensation," 1956, Transactions of ASME, Vol. 60, pp. 1645-1648.

[59] L.A. Campbell, R.C. Chu, M.P. David, M.J. Ellsworth Jr., M.K. Iyengar and R.E Simons, "Multii-Fluid, Two-Phase Immersion-Cooling of Electronic Components," U.S. Patent 8 619 425 B2, Dec 31, 2013.

[60] L.A. Campbell, R.C. Chu, M.J. Ellsworth Jr., M.K. Iyengar, V. Kamath and R.E. Simons, "Appratus and Method for Facilitating Immersion-Cooling of an Electronic Subsystem," U.S. Patent 7 961 475 B2, Jun 14, 2011.

[61] L.A. Campbell, R.C. Chu, M.J. Ellsworth Jr., M.K. Iyengar and R.E. Simons, "Interleaved, Immersion-Cooling Apparatuses and Methods for Cooling Electronic Subsystems," U.S. Patent 8 345 423 B2, Jan 1, 2013.

[62] J.B. Marcinichen, J.A. Olivier and J.R. Thome, "On-Chip Two-Phase Cooling of Datacenters: Cooling System and Energy Recovery," 2012, Applied Thermal Engineering, Vol. 44, pp. 36-51.

[63] Y.J. Kim and M. Gonzalez, "Exergy analysis of an ionic-liquid absorption refrigeration system utilizing waste-heat from datacenters," 2014, International Journal of

Refrigeration, Vol. 48, pp. 26-37.

[64] Y.Q. Chi, J. Summers, P. Hopton, K. Deakin, A. Real, N. Kapur and H. Thompson, "Case Study of a Data Centre using Enclosed, Immersed, Direct Liquid-cooled Servers," 2014, Semiconductor Thermal Measurement and Management Symposium, San Jose, CA.

[65] S.O. Ujereh Jr., I. Mudawar, P.B. Amama, T.S. Fisher and W. Qu, "Enhanced pool boiling using carbon nanotube arrays on a silicon surface," 2005, ASME International Mechanical Engineering Congress and Exposition, Nov. 5-11, Orlando, FL, IMECE2005-80065.

[66] M. Peacock, "Characterization of Structurally-Enhanced Solder Joints using Vertically-Aligned Carbon Nanotubes,"2014, M.S. Thesis, Auburn University.

[67] C.K. Roy, S. Bhavnani, M.C. Hamilton, R.W. Johnson, J.L. Nguyen, R.W. Knight and D.K. Harris, "Investigation into the application of low melting temperature alloys as wet thermal interface materials," 2015, International Journal of Heat and Mass Transfer,, Vol. 85, pp. 996-1002.

[68] Y. Martin and T. Van Kessel, "High Performance Liquid Metal Thermal Interface for Large Volume Production," 2007, International Microelectronics and Packaging Society (IMAPS) Thermal and Power Management, Nov. 11-15, San Jose, CA.

[69] L.A. Campbell and P. Tuma, "Numerical Prediction of the Junction-to-Fluid Thermal Resistance of a 2-Phase Immersion-Cooled IBM Dual Core POWER6 Processor,"

2012, Semiconductor Thermal Measurement and Management Symposium (SEMI-THERM), March 18-22, San Jos, e, CA, pp. 36-44.

[70] P. Tuma, "Indirect Thermosyphon for Cooling Electronic Devices," 2006, Electronics Cooling, Available: http://www.electronics-cooling.com/2006/02/indirect-thermosyphons-for-cooling-electronic-devices/.

[71] G. Moreno, J.R. Jeffers and S. Narumanchi, "Effects of Pressure and a Microprous Coating on HFC-245fa Pool Boiling Heat Transfer," 2014, Journal of Heat Transfer, Vol. 136, No. 10, p. 101502-1.

[72] J.P. O'Connor and S.M. You, "Boiling Enhancement Coating," U.S. Patent US5814392 A, Sep. 29, 1998.

[73] K.N. Rainey and S.M. You, "Pool Boiling Heat Transfer from Plain and Microporous, Square Pin-Finned Surfaces in Saturated FC-72," 2000, Journal of Heat Transfer, No. 122, pp. 509-516.

[74] R. Pastuszko and E. Strak, "Comparison of Pool Boiling Heat Transfer Coefficients for Plain Micro-Fins and Micro-Fins with Sintered Porous Structure," 2015, 9th International Conference on Boiling and Condensation Heat Transfer, April 26-30, Boulder, CO.

[75] M. Arik, A. Bar-Cohen and S.M. You, "Enhancement of Pool Boiling Critical Heat Flux in Dielectric Liquids by Microporous Coatings," 2007, International Journal of Heat and Mass Transfer, Vol. 50, pp. 997-1009.

[76] M.S. El-Genk and A.F. Ali, "Enhanced Nucleate Boiling of Copper Micro-Porous Surfaces," 2010, International Journal of Multiphase Flow, Vol. 36, pp. 780-792.

[77] M.S. El-Genk, "Immersion Cooling Nucleate Boiling of High Power Computer Chips," 2012, Energy Conversion and Management, Vol. 53, No. 1, pp. 205-218.

[78] M.M. Rahman and M. McCarthy, "Biotemplated Nanostructures for Enhancing CHF and HTC during Pool Boiling," 2015, 9th International Conference on Boiling and Condensation Heat Transfer, April 26-30, Boulder, CO.

[79] S.G. Kandlikar, "Review and Projections of Integrated Cooling Systems for Three-Dimensional Integrated Circuits," 2014, Journal of Electronic Packaging, Vol. 136, No. 2, 024001-1.

[80] Y. Madhour, B.P. d'Entremont, J.B. Marcinichen, B. Michel and J.R. Thome, "Modeling of Two-Phase Evaporative Heat Transfer in Three-Dimensional Multicavity High Performance Microprocessor Chip Stacks," 2014, Journal of Electronic Packaging, Vol. 136, No..

[81] F. Alfieri, M.K. Tiwari, L. Zimovik, D. Poulikakos, T. Brunschwiler and B. Michel, "3D Integrated Water Cooling of Composite Multilayer Stack of Chips," 2010, ASME Journal of Heat Transfer, Vol. 132, No. 12, p. 121402.

[82] T. Chen and S.V. Garimella, "Measurements and high-speed visualizations of flow boiling of a dielectric fluid in a silicon microchannel heat sink," International Journal of Multiphase Flow, Vol. 32, pp. 957-971.

[83] N. Thiagarajan, "Experimental Investigation of Thermo-Hydraulic Characteristics of Two-Phase Flow of FC72 in Microchannel Heat Sinks," 2009, M.S. Thesis, Dept. of Mech. Eng., Auburn University, Auburn, AL.

[84] C.J. Kuo, and Y. Peles, "Flow Boiling of Coolant (HFE-7100) inside Structured and Plain Wall Microchannels," 2009, Journal of Heat Transfer, Vol. 131, No. 12.

[85] C.H. Lang and C.F. Liu, "Visualization of Boiling Heat Transfer on Micro Porous Coated Surface in Confined Space," 2013, Proceedings of the eleventh international conference on nanochannels, microchannels and minichannels, American Society of Mechanical E, ngineers, Sapporo, Japan.

[86] K.J.L. Geisler, "Buoyancy-Driven Two Phase Flow and Boiling Heat Transfer in Narrow Vertical Channels," 2007, PhD Dissertation, Dept. of Mech. Eng., University of Minnesota, Minneapolis, MN.

[87] S. Alkharabsheh, B. Sammakia, S. Shrivastava and R. Schmidt, "Using practical fan curves in CFD modeling of a data center," 2013, Semiconductor Thermal Measurement and Management Symposium 2013, San Jose, CA, pp. 211-215.

[88] V.K. Arghode, P. Kumar, Y. Joshi, T. Weiss, and G. Meyer, "Rack level modeling of air flow through perforated tile in a data center," 2013, Journal of Electronic Packaging, Vol. 135, No. 3, p. 030902-1..

[89] S. Alkharabsheh, B. Sammakia, B. Murray, S. Shrivastava and R. Schmidt, "Experimental characterization of pressure drop in a rack," 2014, Proc. of the 14th

intersociety on thermal and thermomechanical phenomena (ITHERM), Orlando, FL, pp. 547-556.

[90] V.K. Arghode and Y. Joshi, "Room Level Modeling of Air Flow in a Contained Data Center Aisle," 2014, Journal of Electronic Packaging, Vol. 136, p. 011011-0-10.

[91] A. Almoli, A. Thompson, N. Kapur, J. Summers, H. Thompson and G. Hannah, "Computational fluid dynamic investigation of liquid rack cooling in data centres," 2012, Applied Energy, Vol. 89, No. 1, pp. 150-155.

[92] J. Nguyen, R.W. Knight, S.H. Bhavnani, D. Harris, J. Gess, A. Sridhar and S. Fincher, "Cooling of Multichip Modules including Effects of Nucleation Site Density and Bubble Departure Diameter Functions," 2015, International Mechanical Engineering Conferen, ce and Exposition (IMECE), Houston, TX.

[93] S.N. Fincher, "Numerical Simulations of Boiling in Dielectric Fluid Immersion Cooling Scenarios of High Power Electronics," 2014, M.S. Thesis, Dept. of Mech. Eng., Auburn University, Auburn, AL.

[94] M.J. Sathe, I.J. Thaker, T.E. Strand and J.B. Joshi, "Advanced PIV/LIF and Shadowgraphy System to Visualize Flow Structure in Two-Phase Bubbly Flows," 2010, Chemical Engineering Science, Vol. 65, No. 8, pp. 2431-2442.

[95] R. Lindken and W. Merzkirch, "A Novel PIV Technique for Measurements in Multiphase Flows and its Application to Two-Phase Bubbly Flows," 2002, Experiments in Fluids, Vol. 33, No. 6, pp. 814-825.

[96] D. Broder and M. Sommerfeld, "Combined PIV/PTV-measurements for the Analysis of Bubble Interactions and Coalescence in a Turbulent Flow," 2003, The Canadian Journal of Chemical Engineering, Vol. 81, No. 3-4, pp. 756-763.

[97] E. Teodori, A.S. Moita and A.L.N. Moreira, "Evaluation of Pool Boiling Heat Transfer over Micro-Structured Surfaces by combining High-Speed Visualization and PIV Measurements," 2013, 10th International Symposium on Particle Image Velocimetry - PIV13, Delf, t, The Netherlands.

[98] B. Ramakrishnan, "Viability of server module thermal management using enhanced heat sinks with low global warming potential dielectric fluids," 2014, M.S. Thesis, Auburn University, Auburn, AL.

[99] Y.Y. Hsu, "On the size range of active nucleation cavities on a heating surface," 1962, Journal of Heat Transfer, Vol. 84, pp. 207-213.

[100] V.P. Carey, "Other Aspects of Boiling and Evaporation in an Extensive Ambient," Liquid-Vapor Phase-Change Phenomena, 2nd Ed., Taylor and Francis, New York, NY, 2008, p. 345.

[101] P. Lee and S. Garimella, "Thermally Developing Flow and Heat Transfer in Rectangular Microchannels of Different Aspect Ratios," 2006, International Journal of Heat and Mass Transfer, Vol. 33, No. 2, pp. 341-347.

[102] Dow Chemicals, "Engineering and Operating Guide for Dowtherm SR-1 and Dowtherm 4000 Inhibited Ethylene Glycol-based Heat Transfer Fluids," 2008,

Available:
http://msdssearch.dow.com/PublishedLiteratureDOWCOM/dh_010e/0901b8038010e413.pdf?filepath=/heattran, s/pdfs/noreg/180-01190.pdf&fromPage=GetDoc.

[103] J. Gerstman and P. Griffith, "The Effects of Surface Instabilities on Laminar Film Condensation," 1965, Technical Report 505-36, Department of Mechanical Enginering, Massachusetts Institute of Technology.

[104] A.E. Bergles and W.M. Rohsenow, "The determination of forced-convection surface-boiling heat transfer," 1964, Journal of Heat Transfer, Vol. 86, pp. 365-372.

[105] Greenpeace International, "How Clean is Your Coal," 2012, Available: http://www.tech-pundit.com/wp-content/uploads/2013/07/Cloud_Begins_With_Coal.pdf?c761ac.

[106] HP, "HP ProLiant DL380p Gen8 Server - Specifications", Available: http://h20564.www2.hp.com/hpsc/doc/public/display?docId=emr_na-c03235289#N10081.

[107] J.C. Passos, L.F.B. Possamai, and F.R. Hirata, "Confined and unconfined FC72 and FC87 boiling on a downward-facing disc," 2005, Applied Thermal Engineering, Vol. 25, pp. 2543-2554.

[108] V.P. Carey, "Convective Boiling in Tubes and Channels," Liquid-Vapor Phase-Change Phenomena, 2nd Ed., Taylor and Francis, New York, NY, 2008, p. 603.

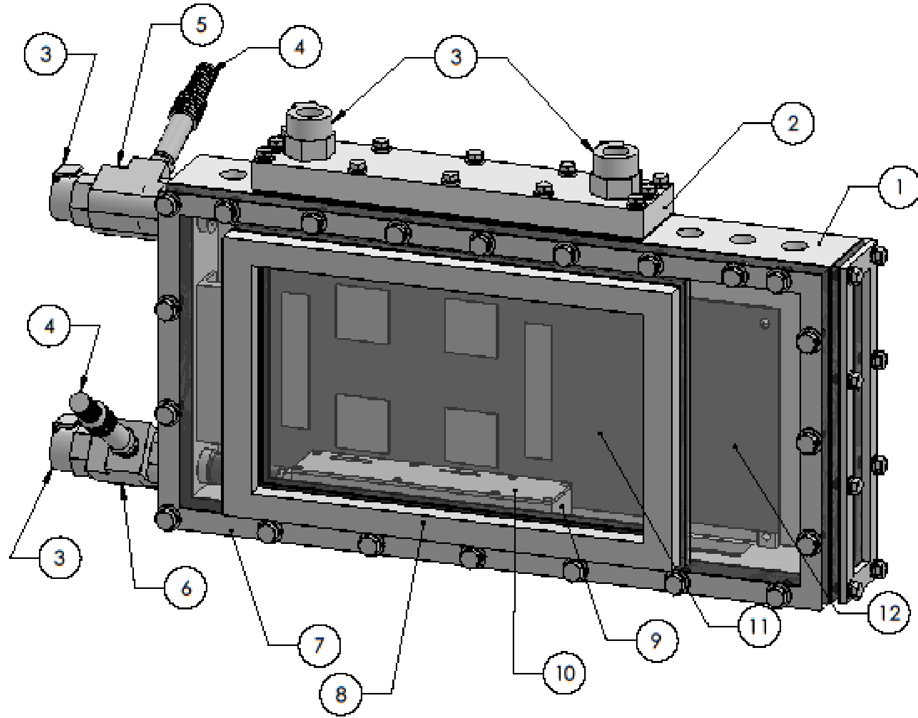
[109] V.P. Carey, "Other Aspects of Boiling and Evaporation in an Extensive Ambient," Liquid-Vapor Phase-Change Phenomena, 2nd Ed., Taylor and Francis, New York, NY, 2008, p. 346..

Appendix I: Mechanical Assembly and Construction Drawings

The following drawings detail how the electronics cartridge assembly was constructed. The drawings follow the AUB-1000XX numbering nomenclature. In the top level assembly drawing, AUB-100001, each individual component is referred to by its corresponding Find Number (FN) as referenced in the parts list in the bottom right corner of the drawing just above the title.

NOTES:

1. MANUFACTURER: PARKER-HANNIFIN
2. MANUFACTURER: OMEGA ENGINEERING
3. USED TO DISTRIBUTE STRESS FROM ARRAY OF FASTENERS UNIFORMLY ON THE INTERNAL GASKET
4. INTERNAL FLOW DISTRIBUTION PLENUM BASE
5. INTERNAL FLOW DISTRIBUTION PLENUM LID
6. PRIMARY HEATED ELEMENT VIEWING WINDOW
7. PERIPHERY ELEMENT VIEWING WINDOW



QTY	FN	PART NUMBER	NOTES
1	12	AUB-100002	7
1	11	AUB-100003	6
1	10	AUB-100039	5
1	9	AUB-100034	4
1	8	AUB-100021	3
1	7	AUB-100007	3
1	6	AUB-100031	
1	5	AUB-100032	
2	4	TC-K-1/8NPT-G-72	2
4	3	2061400	1
1	2	AUB-100005	
1	1	AUB-100001	

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DIMENSIONS ARE IN INCHES
TOLERANCES:
FRACTIONAL ±
ANGULAR: MACH ± BEND ±
TWO PLACE DECIMAL ±
THREE PLACE DECIMAL ±
INTERPRET GEOMETRIC TOLERANCING PER:
MATERIAL
FINISH
DO NOT SCALE DRAWING

	NAME	DATE
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CHECKED		
ENG APPR.		
MFG APPR.		
Q.A.		
COMMENTS:		

NEXT ASSY	USED ON

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TITLE:

SIZE B | DWG. NO. AUB-100001 | REV
SCALE: 1:5 | WEIGHT: | SHEET 1 OF 1

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NOTES:

1. SPOT FACE SURFACE AS REQUIRED TO ALLOW FOR INSTALLATION TOOLING OF FN 2. INSTALL PER MANUFACTURER'S INSTRUCTIONS.
2. SUGGESTED SOURCE FOR FN 1:

   MCMASTER-CARR
3. SUGGESTED SOURCE FOR FN 2:

   PENN ENGINEERING
4. MATERIAL: ALUMINUM, 6061 PER ASTM B221.
5. DRILL A LOOSE #4 SCREW CLEARANCE HOLE APPROXIMATELY .06" PAST THE BOTTOM SHANK OF FN 2. CLEARANCE HOLE SHOULD NOT PROTRUDE INTO FAR SIDE OF INSTALLATION.

QTY	FN	PART NUMBER	NOTES
22	2	F-440-1	1,3,5
1	1	AUB-100000-1	2,4

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ANGULAR: MACH ± BEND ±
TWO PLACE DECIMAL ±
THREE PLACE DECIMAL ±
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FINISH
DO NOT SCALE DRAWING

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MFG APPR.		
Q.A.		
COMMENTS:		

TITLE:

SIZE: B | DWG. NO. AUB-100000 | REV 01
SCALE: 1:2 | WEIGHT: | SHEET 1 OF 3

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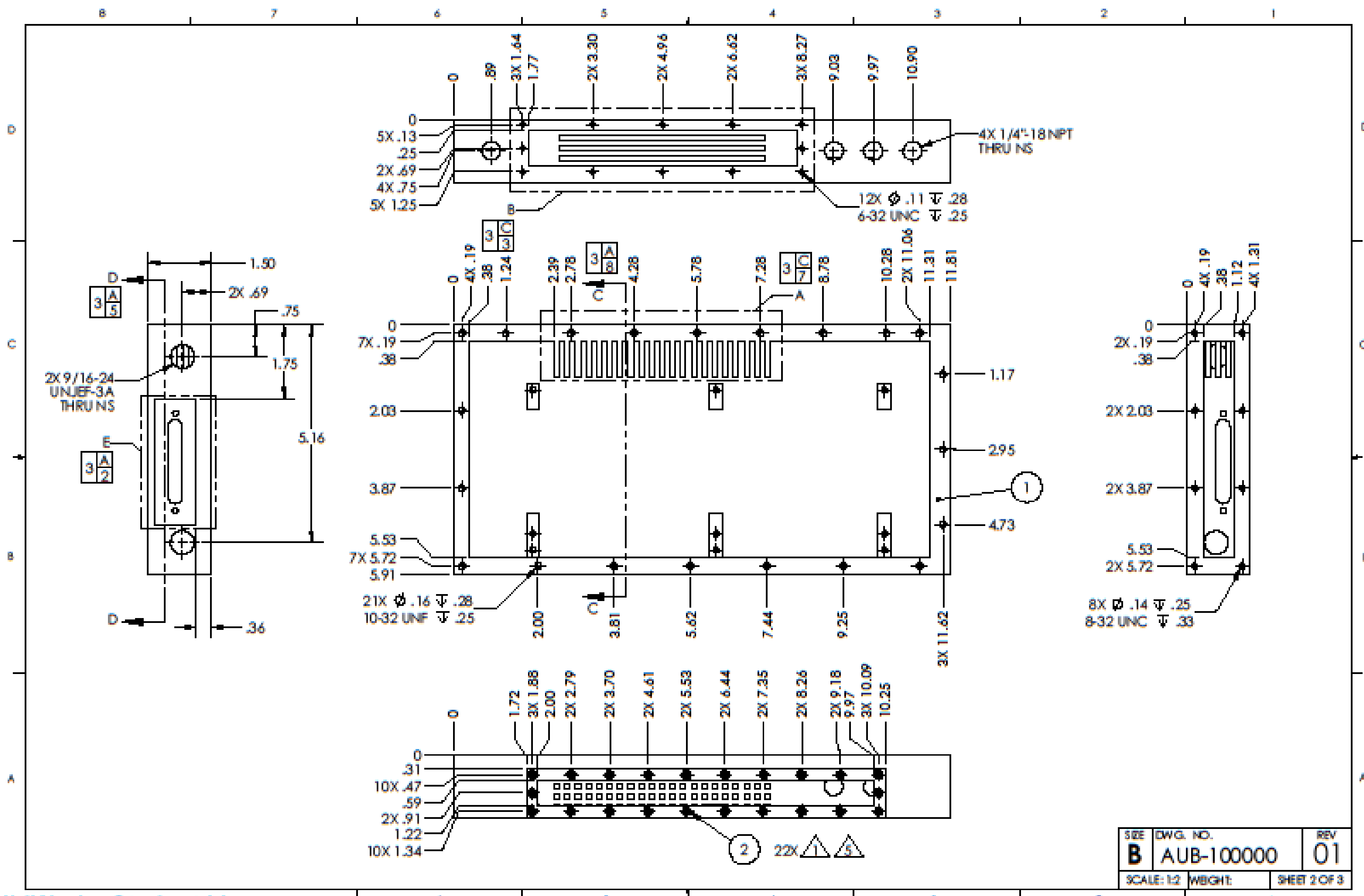

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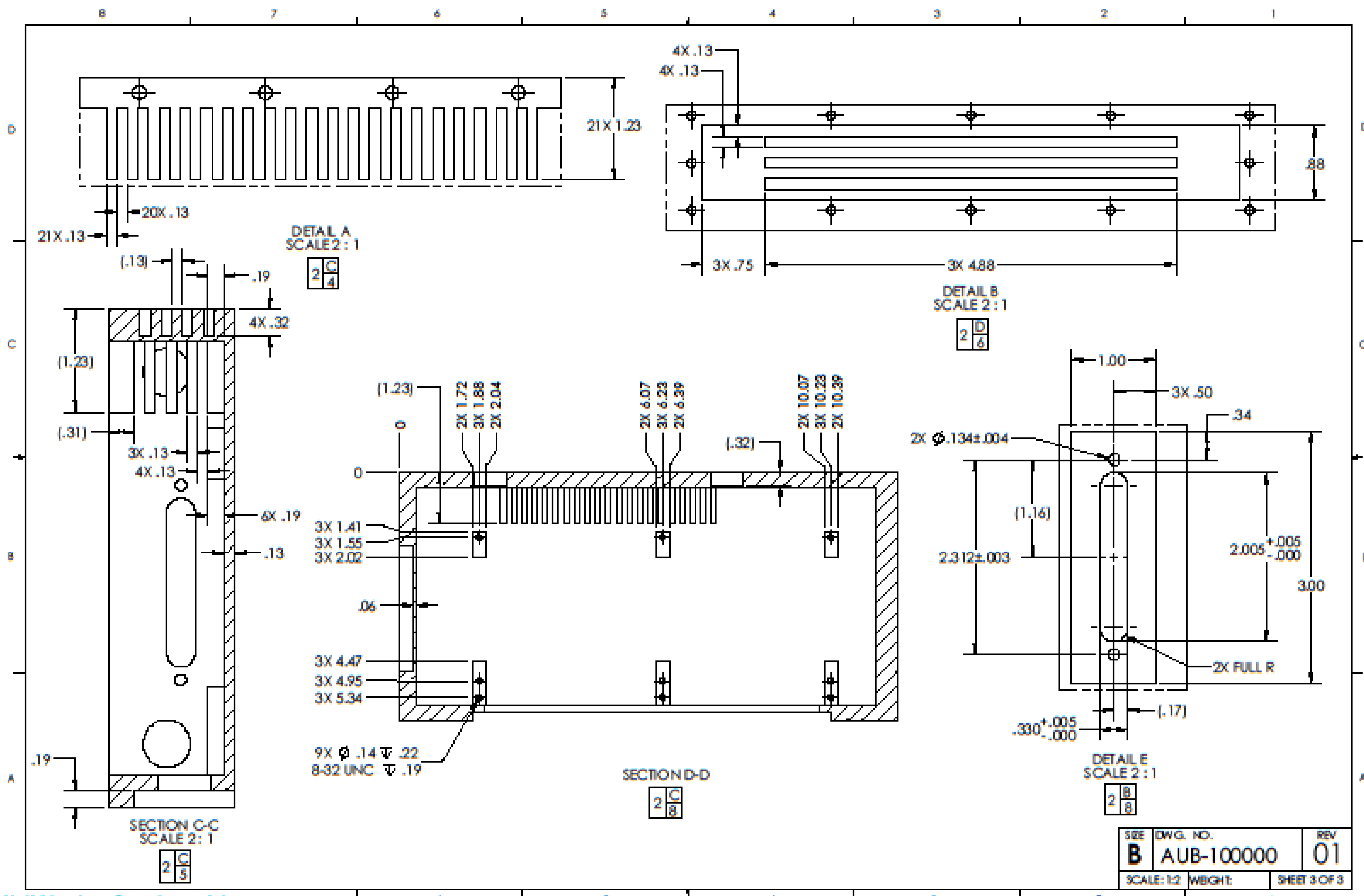

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NOTES:

1. MATERIAL: IMPACT RESISTANT POLYCARBONATE, CLEAR
2. SUGGESTED SOURCE AND P/N:

   MCMASTER-CARR, P/N: 8574K312

(3) ALL HOLES ON RECESSED FLANGE ARE COUNTERSUNK ON FAR SIDE OF VIEW SHOWN.

		UNLESS OTHERWISE SPECIFIED:		NAME	DATE
		DIMENSIONS ARE IN INCHES TOLERANCES: FRACTIONAL ± ANGULAR: MACH ± BEND ± TWO PLACE DECIMAL ± THREE PLACE DECIMAL ±	DRAWN		
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TITLE:

SIZE	DWG. NO.	REV
B	AUB-100002	
SCALE: 1:2	WEIGHT:	SHEET 1 OF 1

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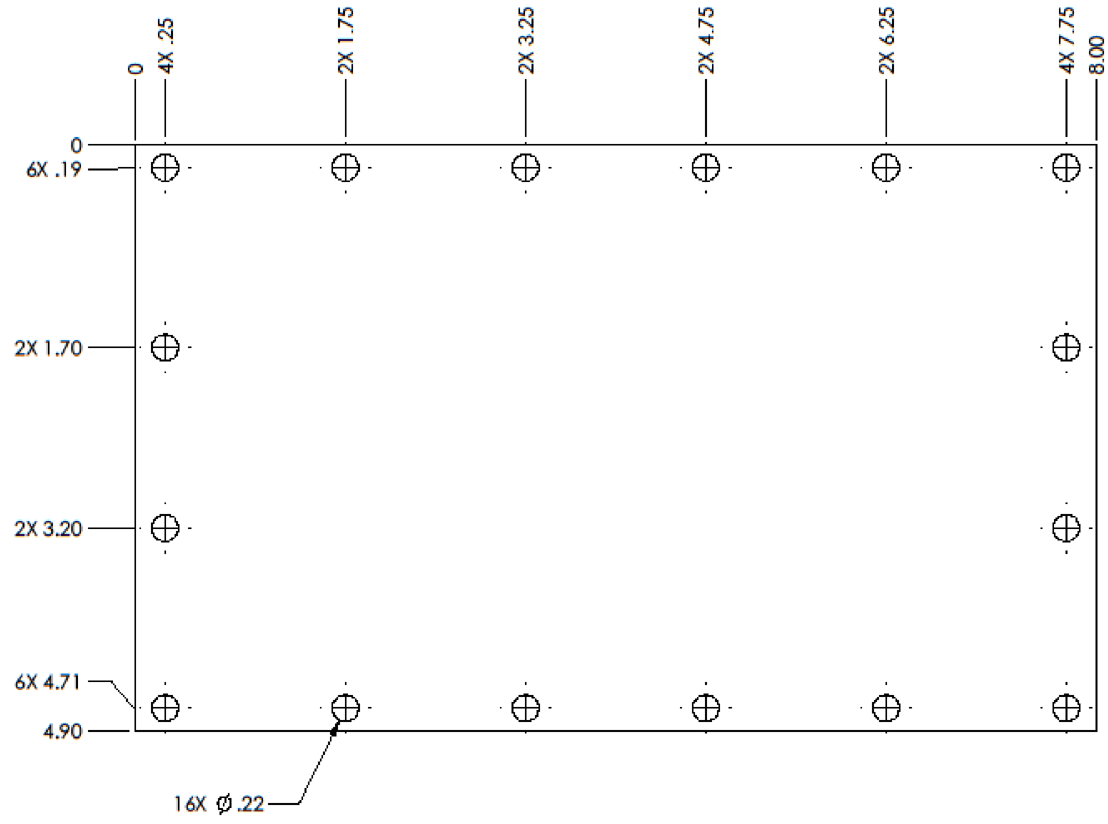
NOTES:

1. MATERIAL: IMPACT RESISTANT POLYCARBONATE, CLEAR, 0.25" THICK
2. SUGGESTED SOURCE AND P/N:
   MCMASTER-CARR, P/N: 8574K282



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TITLE:		
SIZE B	DWG. NO. AUB-100003	REV
SCALE: 1:1	WEIGHT:	SHEET 1 OF 1

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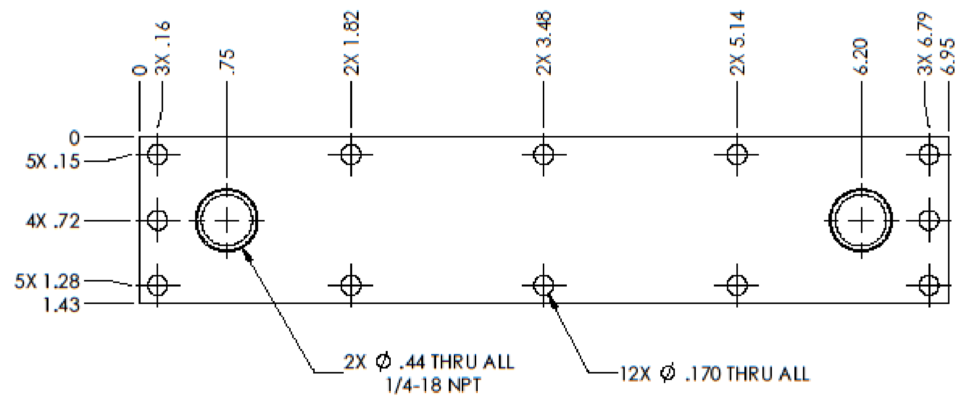
NOTES:

1. MATERIAL: ALUMINUM 6061 PER ASTM B221, .500" THICK



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SIZE	DWG. NO.	REV
B	AUB-100005	01
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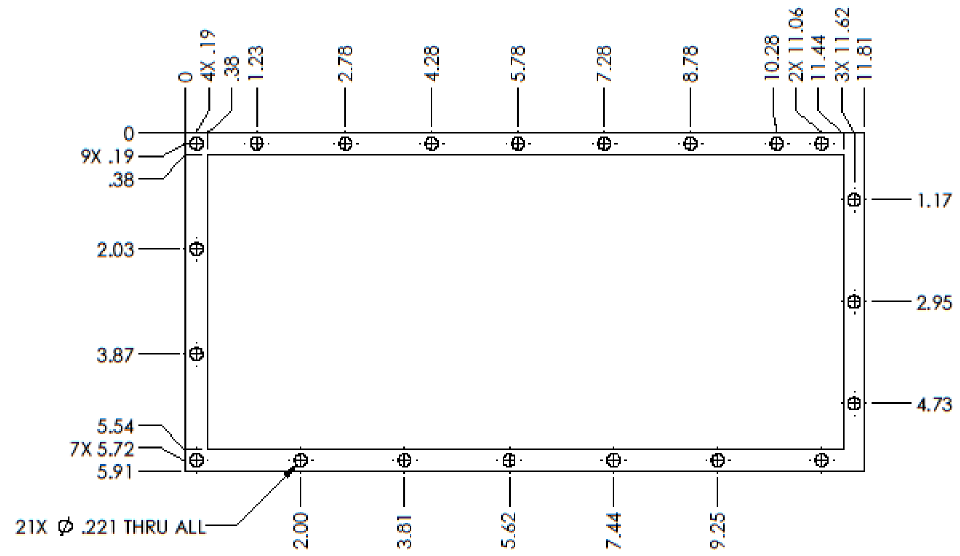
NOTES:

1. MATERIAL: ALUMINUM 6061 PER ASTM B221, .125" THICK



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SIZE	DWG. NO.	REV
B	AUB-100007	
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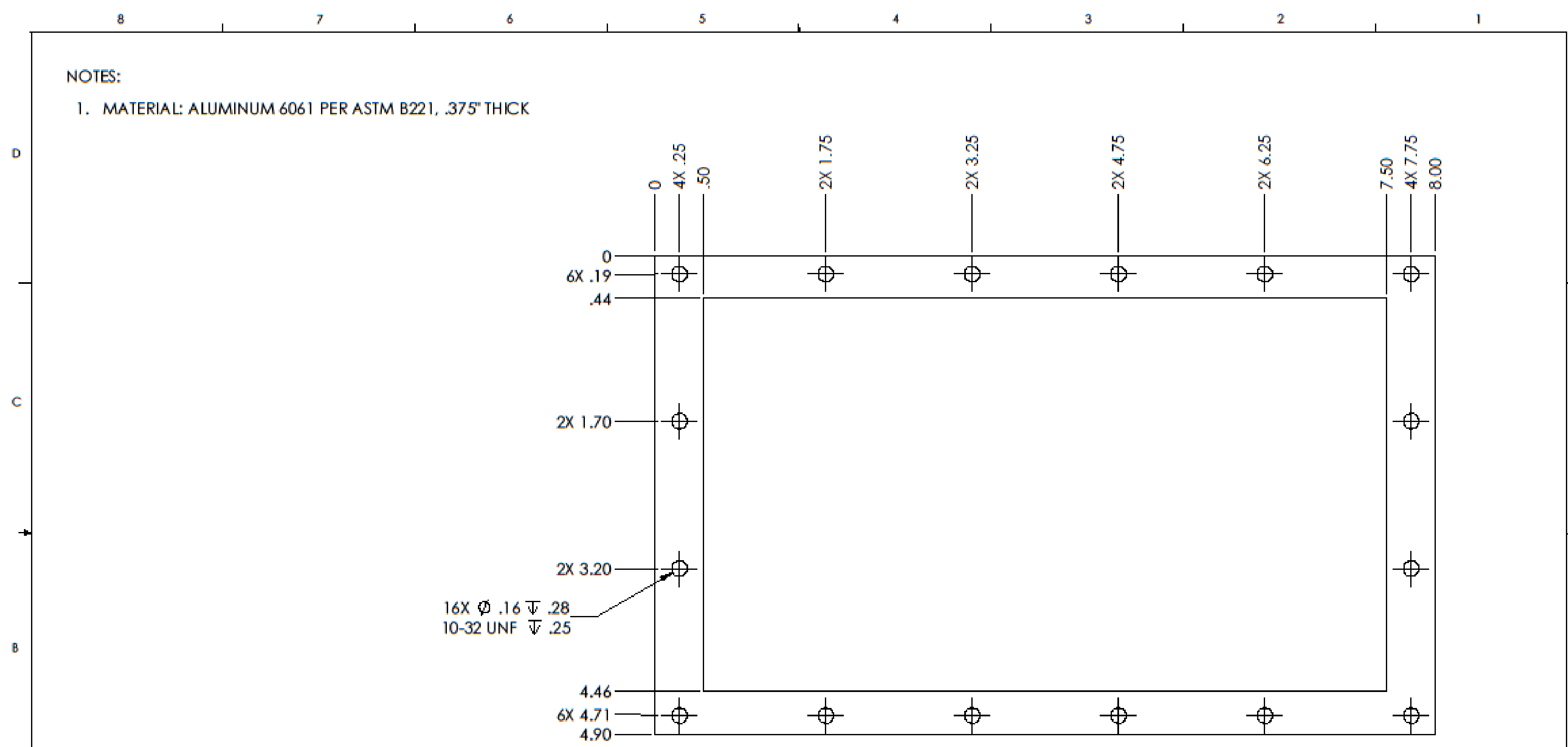
NOTES:

1. MATERIAL: ALUMINUM 6061 PER ASTM B221, .375" THICK



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THREE PLACE DECIMAL ±
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SIZE	DWG. NO.	REV
B	AUB-100021	

SCALE: 1:1 WEIGHT: SHEET 1 OF 1

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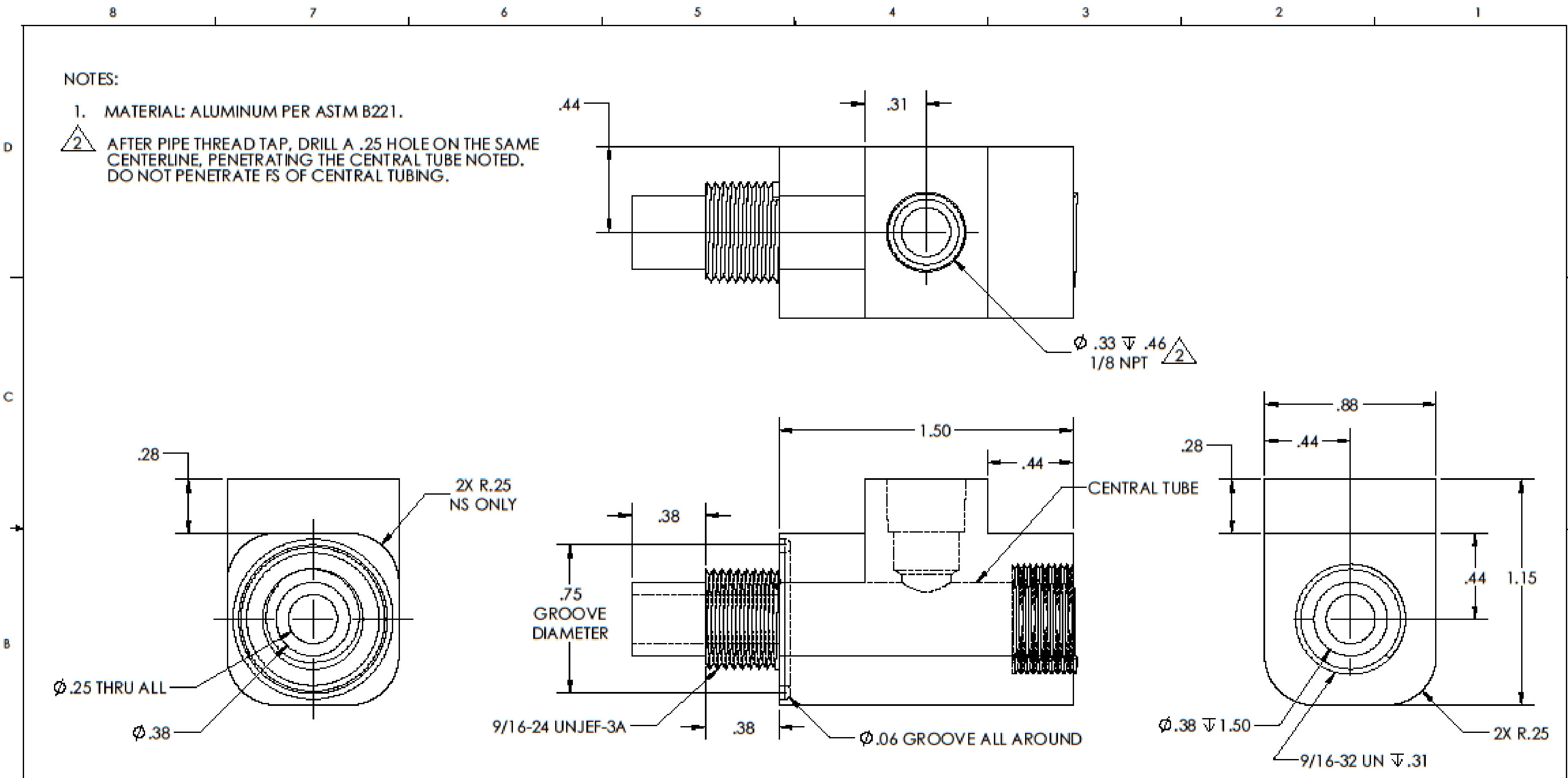
NOTES:

1. MATERIAL: ALUMINUM PER ASTM B221.

2 (in triangle) AFTER PIPE THREAD TAP, DRILL A .25 HOLE ON THE SAME CENTERLINE, PENETRATING THE CENTRAL TUBE NOTED. DO NOT PENETRATE FS OF CENTRAL TUBING.



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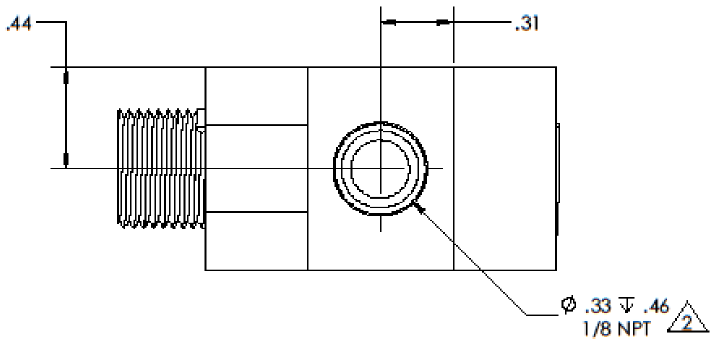
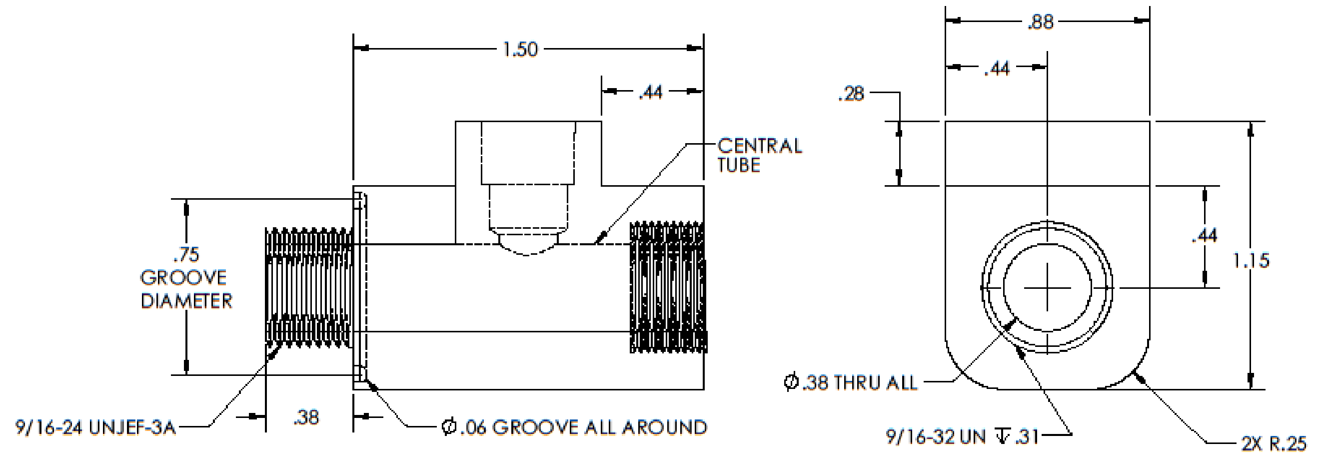
NOTES:

1. MATERIAL: ALUMINUM PER ASTM B221.

2. AFTER PIPE THREAD TAP, DRILL A .25 HOLE ON THE SAME CENTERLINE, PENETRATING THE CENTRAL TUBE NOTED. DO NOT PENETRATE FS OF CENTRAL TUBING.





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THREE PLACE DECIMAL ±
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TITLE:

SIZE	DWG. NO.	REV
B	AUB-100032	
SCALE: 2:1	WEIGHT:	SHEET 1 OF 1

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		DIMENSIONS ARE IN INCHES TOLERANCES: FRACTIONAL ± ANGULAR: MACH ± BEND ± TWO PLACE DECIMAL ± THREE PLACE DECIMAL ±	DRAWN			TITLE:
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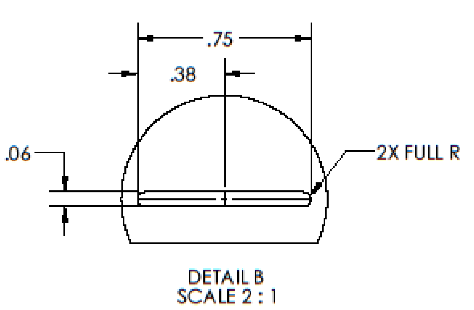
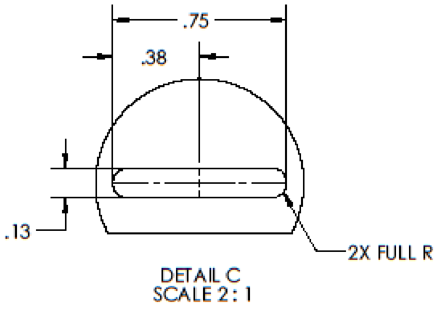
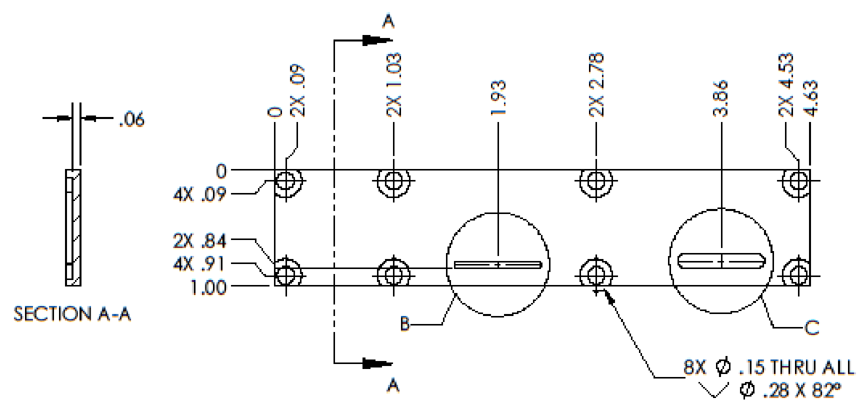
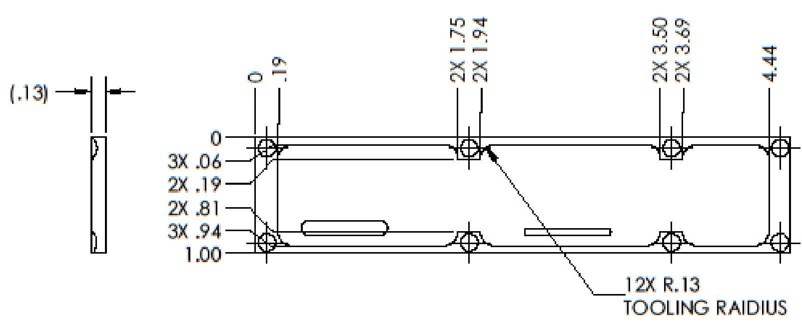
NOTES:

1. MATERIAL: ALUMINUM SHEET PER ASTM B221, 1/8" THICK.









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SCALE: 1:1	WEIGHT:	SHEET 1 OF 1

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Appendix II: Microporous Surface Enhancement Fabrication Instructions

The following is information received from the manufacturer documenting the manufacture of the microporous surface used in the current study. Fundamental benefits of using this surface can be found in the Surface Enhancement Details section.

Introduction

The patented 3M™ Microporous Metallic Boiling Enhancement Coating (MMBEC) was developed to provide optimal boiling heat transfer coefficients with 3M™ Novec™ Engineered Fluids. 3M MMBEC is made with 3M™ developmental material L-20227. This powder is composed of sub-20µm copper particles coated with 0.5 wt% silver. L-20227 particles are applied to a copper substrate in a layer about 150µm thick and then fused at elevated temperature, typically 850ºC in the absence of oxygen. The silver diffuses into the copper, temporarily forming a eutectic that melts and re-solidifies, before cooling, as diffusion progresses. This method provides:

- High thermal conductivity ligament between particles
- Ligaments present at all particle contact points
- Pores size provides optimal nucleation sites for Novec™ fluids
- Coating properties relatively insensitive to processing conditions

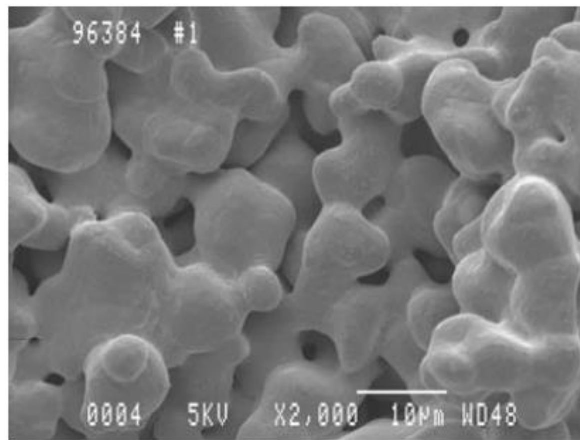


Figure 1 - Scanning Electron Micrograph of 3M MMBCE

Below are directions for the standard 3M technique for applying and fusing L-20227 powder. Other techniques are allowed and may be preferred depending on the equipment available.

Application

L-20227 particles are mixed with Dow 704 silicone diffusion pump oil to achieve a mixture that is 13% oil by weight. This mixture is applied to a flat copper substrate using standard screen printing techniques and a Sefar 45 180 mesh polyester screen (45-180 W IM E11F 0.5 30d STD) with the desired pattern. The resultant coating contains 0.052g/cm2 L20227 particles.

Notes: Particles may be applied dry (for example by knife coating) or using any volatile binder that will be removed in and compatible with the fusing process.

Fusing

Fusing is done at 0.01 milliTorr in a vacuum furnace. Temperature is raised to 300ºC and paused for 20 minutes to remove the oil. Temperature is then raised to 850ºC and held for 1 hour.

Notes: Inert atmospheres may be used in place of or in addition to vacuum to control oxygen levels. Ramp rates and equilibrium times were dictated by oven capabilities and temperature uniformity. Higher ramp rates and shorter equilibrium times may be possible if equipment allows.

Notes

Resultant coating thickness should be approximately 150µm. A minimum thickness of 100µm is required to achieve optimal performance. Heat transfer coefficients will drop precipitously as the thickness is reduced below this level. Thicknesses up to 300µm will perform well.

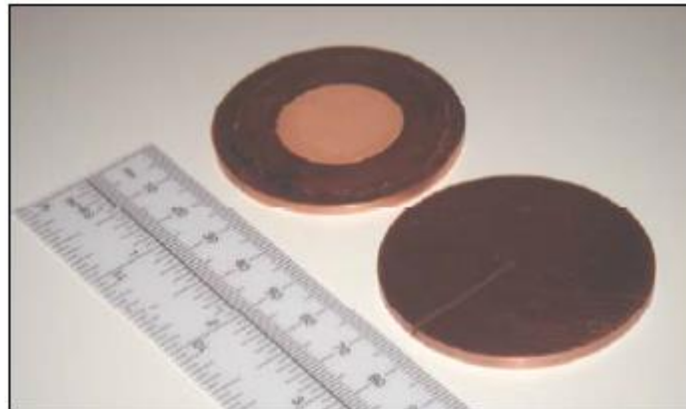


Figure 2 – Photo of 3M MMBCE fused to a copper test disk

Appendix III: Sample Calculations

C_{sf} Calculation

Manipulate the Rohsenow Correlation, Equation 8, to solve for C_{sf}:

$$C_{sf} = \frac{1}{\left\{\frac{q''}{\mu_l h_{lv}} * \left[\frac{\sigma}{g * (\rho_l - \rho_v)}\right]^{\frac{1}{2}} * Pr^{\frac{s}{r}} * \left[\frac{c_{pl} * [T_w - T_{sat}]}{h_{lv}}\right]^{-1/r}\right\}^{r}}$$

As an example, the microporous surface was calculated using the base dimensions, or that interfacing with the 1" x 1" thermal test cell. There are four test cells being uniformly heated for this calculation so that will be reflected in the calculations below. The power supply was limited to ten amps of supply current. Therefore, at these higher power dissipations that required more than ten amps of total supply current to the heaters, the current supply had to be split to supply heat to the bottom row and top row. Voltage drops across the top row and bottom row were measured separately in order to combine with their current counterpart for accurate total power measurement. The heat flux was calculated with the measured voltage and measured current, divided by this base area as shown below:

$$q'' = \frac{(I * V)_{top\ row} + (I * V)_{bottom\ row}}{A}$$

$$q'' = \frac{(50.91\ Volts * 5.92\ Amps) + (51.12\ Volts * 5.93\ Amps)}{4 * 6.45\ x\ 10^{-4}\ m^2}$$

$$q^{"} = \frac{(50.91\ Volts * 5.92\ Amps) + (51.12\ Volts * 5.93\ Amps)}{6.45\ x\ 10^{-4}\ m^2}$$

$$q^{"} = 23.4\ x\ 10^4\ \frac{W}{m^2}\ or\ 23.4\ \frac{W}{cm^2}$$

Establish the mean temperature from the diodes shown on Table 1 as the locations from which temperatures were taken for the microporous surface:

$$T_w = \frac{Diode_1 + Diode_2 + Diode_3 + Diode_4 + Diode_6 + Diode_7 + Diode_8 + Diode_9 + Diode_{10} + Diode_{11} + Diode_{12} + Diode_{13}}{Number\ of\ Diodes\ Used}$$

$$T_w = \frac{68.94\ °C + 57.73\ °C + 58.18\ °C + 75.08\ °C + 76.08\ °C + 66.06\ °C + 74.08\ °C + 67.44\ °C + 71.44\ °C + 63.87\ °C + 63.21\ °C + 67.86\ °C}{12}$$

$$T_w = 67.50\ °C$$

Using Novec as the working fluid, its associated saturated properties from Table 3, along with the measured average surface temperature, the C_{sf} value is calculated below. The average wall temperature used in these calculations is the mean of the values recorded from the diodes located on the microporous test board as noted in Table 1.

$$Pr = \frac{\frac{\mu_l}{\rho_l}}{\frac{k_l}{\rho_l * c_p}}$$

$$Pr = \frac{\frac{4.4\ x\ 10^{-4}\ (Pa * \sec)}{1517\ \frac{kg}{m^3}}}{\frac{0.054\ \frac{W}{m * K}}{1517\ \frac{kg}{m^3} * 1118\ \frac{J}{kg * K}}}$$

$$Pr = 9.11$$

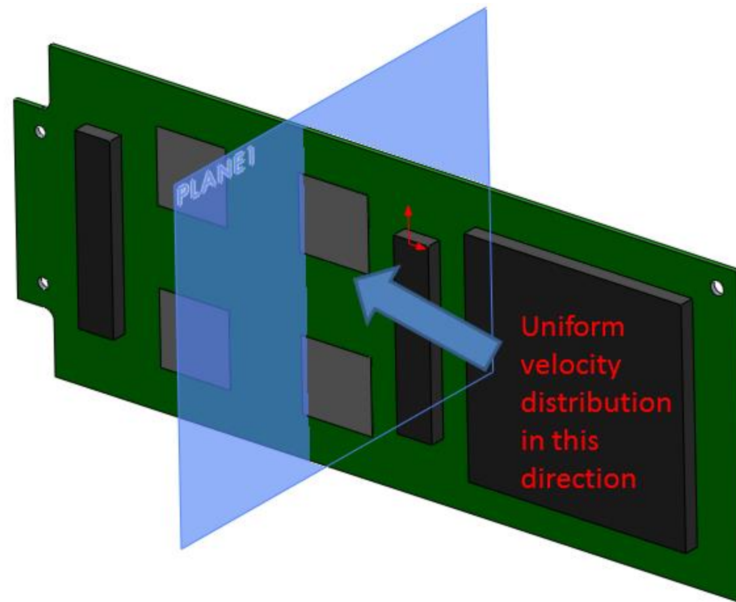
$$C_{sf} = \frac{1}{\left\{ \frac{23.4\ x\ 10^4 \frac{W}{m^2}}{4.4\ x\ 10^{-4}\ (Pa * sec) * 88\ x\ 10^3 \frac{J}{kg}} * \left[\frac{9.24\ x\ 10^{-3} \frac{N}{m}}{9.81\ \frac{m}{sec^2} * \left(1517\ \frac{kg}{m^3} - \ 12.6\ \frac{kg}{m^3}\right)} \right]^{\frac{1}{2}} * 9.11^{\frac{1.7}{0.33}} * \left[\frac{1118\ \frac{J}{kg * K} * [67.5\ °C - 49°\ C]}{88\ x\ 10^3\ \frac{J}{kg}} \right]^{-1/0.33} \right\}^{0.33}}$$

$$C_{sf} = 0.0032$$

This is the final C_{sf} value shown on the left plot for Figure 85 associated with the 1250 mL/min dielectric fluid flow rate data.

Forced versus Natural Convection Contribution Calculation

For this analysis, that associated with the tube inlet flow distribution design, the dielectric fluid is assumed to be uniformly distributed throughout the cross section of the internal cartridge. A schematic of this assumption is shown below:



In order to calculate dimensionless parameters, properties must be determined. Using vendor provided equations for Novec 649, average surface temperatures calculated as the mean from values recorded at the diode locations shown in Table 1 for the bare silicon surface, and the ambient temperature calculated as the mean of the temperatures recorded from the inlet and outlet port thermocouples on the ingoing and outgoing dielectric fluid flow, properties at the film temperature can be calculated:

The third data point in the 1250 mL/min data set for the tube inlet flow distribution design has been selected to execute the following sample calculation. The measured average surface temperature, measured dielectric fluid mean temperature, along with the resulting film temperature, which is an average of the latter two, is presented in the following table:

Average Primary Die Surface Temperature (°C)	Dielectric Fluid Mean Temperature (°C)	Film Temperature (°C)
34.45	16.38	25.42

Kinematic Viscosity (where T_{film} is in °C):

$$\nu_l = e^{\left(\frac{660.0991}{T_{film}+200}-3.8731\right)}$$

$$\nu_l = e^{\left(\frac{660.0991}{25.42+200}-3.8731\right)}$$

$$\nu_l = 0.389\ centistokes\ or\ 3.89\ x\ 10^{-7}\ \frac{m^2}{sec}$$

In order to calculate the Reynolds number, a velocity must be determined. This is determined from the assumption of uniform velocity across the internal cross section of the cartridge along with knowledge of the dielectric fluid flow rate, 1250 mL/min.

The cross section is determined from the drawing AUB-100000 in Appendix I as 5.15" x 1.37" or 0.00455 m^2

$$Volumetric\ Flow\ Rate = Cross\ Sectional\ Area * Velocity$$

$$1250\ \frac{mL}{min} * \frac{1\ x\ 10^{-6}\ m^3}{1\ mL} * \frac{1\ min}{60\ sec} = 4.55\ x\ 10^{-3} m^2 * Velocity$$

$$Velocity = 4.58\ \frac{mm}{sec}$$

For the characteristic length in the Reynolds number calculation, the assumption has been made that the boundary layer is unaffected between the right column of heated elements and the left column of heated elements. Therefore, the characteristic length is assumed to be 2L, where L is the length of one heater or 1 in (0.0254 m).

$$Re_L = \frac{Velocity * L_{characteristic}}{\nu_l}$$

$$Re_L = \frac{4.55\ x\ 10^{-3}\,\frac{m}{sec} * (2 *\ 0.0254)m}{3.89\ x\ 10^{-7}}$$

$$Re_L = 594$$

Since the Reynolds number calculated does not exceed the 5 x 10^5 critical value for transition to turbulence, the laminar isoflux external plate average Nusselt number equation is used:

$$\overline{Nu_L} = 0.680 * Re_L^{\frac{1}{2}} * Pr^{\frac{1}{3}}$$

For calculation of the Prandtl Number:

Liquid Thermal Conductivity (where T_{film} is in °C):

$$k_l = \ -0.188 *\ T_{film} + 63.403$$

$$k_l = \ -0.188 *\ 25.42 + 63.403$$

$$k_l = \ 58.6\ \frac{mW}{m * K}$$

Liquid Density (where T_{film} is in °C)

$$\rho_l = \ -0.002904 *\ T_{film} + 1.674415$$

$$\rho_l = \ -0.002904 *\ 25.42 + 1.674415$$

$$\rho_l = 1.601 \frac{g}{cm^3} \; or \; 1601 \frac{kg}{m^3}$$

Specific Heat Capacity (where T_{film} is in Kelvin)

$$c_p = 1.2946 - 1.8246 \; x \; 10^{-3} * T_{film} + 3.964 \; x \; 10^{-6} * T_{film}^2$$

$$c_p = 1.2946 - 1.8246 \; x \; 10^{-3} * 25.42 + 3.964 \; x \; 10^{-6} * 25.42^2$$

$$c_p = 1.2946 - 1.8246 \; x \; 10^{-3} * (25.42 + 273.15) + 3.964 \; x \; 10^{-6} * (25.42 + 273.15)^2$$

$$c_p = 1.103 \frac{J}{g * K} \; or \; 1103 \frac{J}{kg * K}$$

Prandtl Number:

$$\mathrm{Pr} = \frac{\nu_l}{\alpha}$$

$$\alpha = \frac{k_l}{\rho_l * c_p} = thermal \; diffusivity$$

$$\alpha = \frac{58.6 \; x \; 10^{-3} \frac{W}{m * K}}{1601 \frac{kg}{m^3} * 1103 \frac{J}{kg * K}}$$

$$\alpha = 3.32 \; x \; 10^{-8} \frac{m^2}{sec}$$

$$\Pr = \frac{3.89\ x\ 10^{-7}\,\frac{m^2}{sec}}{3.32\ x\ 10^{-8}\,\frac{m^2}{sec}}$$

$$\Pr = \ 11.7$$

Calculate the average Nusselt Number:

$$\overline{Nu_L} = 0.680 * \ 594^{\frac{1}{2}} * \ 11.7^{1/3}$$

$$\overline{Nu_L} = 0.680 * \ 594^{\frac{1}{2}} * \ 11.7^{1/3}$$

$$\overline{Nu_L} = 37.6$$

Using the definition of the Nusselt number, calculate the forced convection heat transfer coefficient:

$$\overline{Nu_L} = \frac{h_F * (2L)}{k_l}$$

$$37.6 = \frac{h_F * (2 * 0.0254\ m)}{58.6\ x\ 10^{-3}\ \frac{W}{m * K}}$$

$$h_F = 43.4\ \frac{W}{m^2 * K}$$

Using Newton's Law of Cooling, a predicted surface temperature is calculated against the measured heat flux at this data point.

$$q^{"} = h_F * (T_w - \ T_{mean})$$

$$0.667\ x\ 19^4 \frac{W}{m^2} = 43.4\ \frac{W}{m^2 * K} * (T_w - \ 16.38)$$

$$T_w = 170°C$$

While this value, along with other values calculated in the heat fluxes leading up to incipience across all of the dielectric fluid flow rates, form the dashed linear trendline on Figure 76, it is clear that forced convection alone cannot accurately predict the surface temperature. This value is well beyond the saturation temperature of 49°C. Therefore, natural convection must be addressed as a possibility for being the dominant heat transfer mechanism under this flow distribution scenario.

The Richardson number, Ri, is used as a measure of the comparative contributions of forced and natural convection in mixed convection problems. In order to calculate this number, the Grashof number must be calculated:

$$Gr_L = \frac{g * \beta * (T_w - T_\infty) * L^3_{characteristic}}{\nu_l^2}$$

For this analysis, the characteristic length is again assumed to be 2L where L is the length of one heater. It is assumed that the thermal boundary layer is undisturbed between heaters as illustrated by Figure 41. T_w and T_∞ are taken from the average primary die surface temperature and dielectric fluid mean temperature recorded in the table above. The properties are still taken at the film temperature and are the same as previously calculated. The coefficient of thermal expansion, β, is assumed to be 0.0018 K^{-1} from vendor data.

$$Gr_L = \frac{9.81\ \frac{m}{sec^2} * 0.0018\ \frac{1}{K} * (34.45\ °C - 16.38\ °C) * (2 * 0.0254\ m)^3}{(3.89\ x\ 10^{-7}\ \frac{m^2}{sec})^2}$$

$$Gr_L = 2.76\ x\ 10^8$$

To calculate the Richardson number (Ri):

$$Ri = \frac{Gr_L}{Re_L^2}$$

$$Ri = \frac{2.76\ x\ 10^8}{594^2}$$

$$Ri = 782 \gg 1$$

Given the conclusion that the Richardson number is much greater than one, forced convection effects can be neglected and natural convection effects must be dominant. In order to determine the proper equation to use, the Rayleigh number must be calculated:

$$Ra_L = Gr_L * Pr$$

$$Ra_L = 2.76\ x\ 10^8 * 11.7$$

$$Ra_L = 2.76\ x\ 10^8 * 11.7$$

$$Ra_L = 3.23\ x\ 10^9$$

With this value being slightly greater than the critical Rayleigh number for transition to turbulence of 10^9, and for consistency of correlation usage with other values of slightly larger heat fluxes mandating even more turbulent behavior, the Chu and Churchill correlation for free convection on an external vertical plate will be used to evaluate the average Nusselt number:

$$\overline{Nu_L} = \left\{ 0.825 + \frac{0.387 * {Ra_L}^{1/6}}{\left[1 + \left(\frac{0.492}{Pr}\right)^{9/16}\right]^{8/27}} \right\}^2$$

$$\overline{Nu_L} = \left\{0.825 + \frac{0.387 * (3.23\ x\ 10^9)^{1/6}}{\left[1 + \left(\frac{0.492}{11.7}\right)^{9/16}\right]^{8/27}}\right\}^2$$

$$\overline{Nu_L} = 226$$

Using the definition of the Nusselt number to determine the natural convection heat transfer coefficient, h_N:

$$\overline{Nu_L} = \frac{h_N * (2L)}{k_l}$$

$$226 = \frac{h_N * (2 * 0.0254\ m)}{58.6\ x\ 10^{-3}\ \frac{W}{m * K}}$$

$$h_N = 261\ \frac{W}{m^2 * K}$$

Using Newton's Law of Cooling, a predicted surface temperature is calculated against the measured heat flux at this data point.

$$q'' = h_N * (T_w - T_{mean})$$

$$0.667\ x\ 19^4\ \frac{W}{m^2} = 261\ \frac{W}{m^2 * K} * (T_w - 16.38)$$

$$T_w = 41.9°C$$

This value, along with other values calculated in the heat fluxes leading up to incipience across all of the dielectric fluid flow rates, form the solid linear trendline on Figure 76. Looking at the data presented in Figure 76, this value still underpredicts the experimental

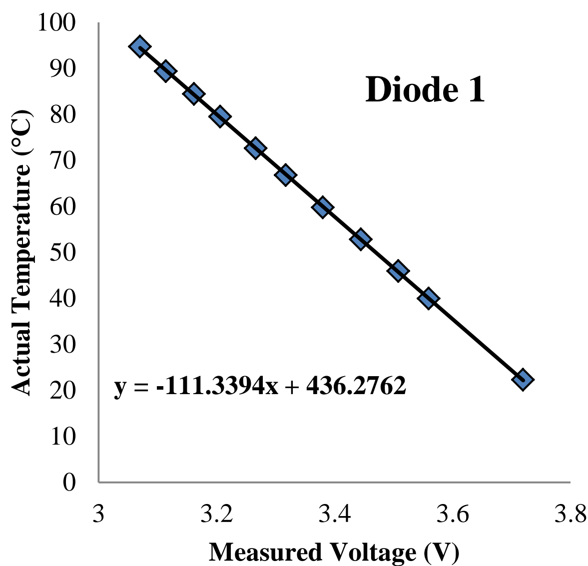
temperature recorded. However, it is much better than the predicted surface temperature yielded by only considering the forced convection model. The solid lines on Figure 76 that use the natural convection values much more closely mimic the trends and values experimentally determined over all of the dielectric fluid flow rates tested. The calculation of the Richardson number, along with working out the forced convection only model to see that it severely overpredicted the wall temperature, was critical to understanding the heat transfer mechanisms at play in this regime leading up to incipience for this particular flow distribution scenario. The slopes of the theoretical lines presented in Figure 76 are tied to the heat transfer coefficients calculated. The relative steepness of the natural convection calculation solid line versus that of the forced convection calculation dashed line is owed to the roughly 500% increase in the heat transfer coefficient with natural convection over forced convection. Qualitatively speaking, the relatively small dielectric fluid flow rate, even at 1250 mL/min, distributed over such a comparatively large cross section, yields gentle velocities across the primary die in the convection regime. Additionally, as shown in the dielectric fluid mean temperature data presented in Figure 77, the severe degree of subcooling taking place within the cartridge is another primary driver of the dominance of natural convection versus that of forced convection. This qualitative assessment along with the parameters, models and temperature values yielded in this sample calculation show that natural convection is dominant for the tube inlet flow distribution design in the heat flux region leading up to boiling incipience.

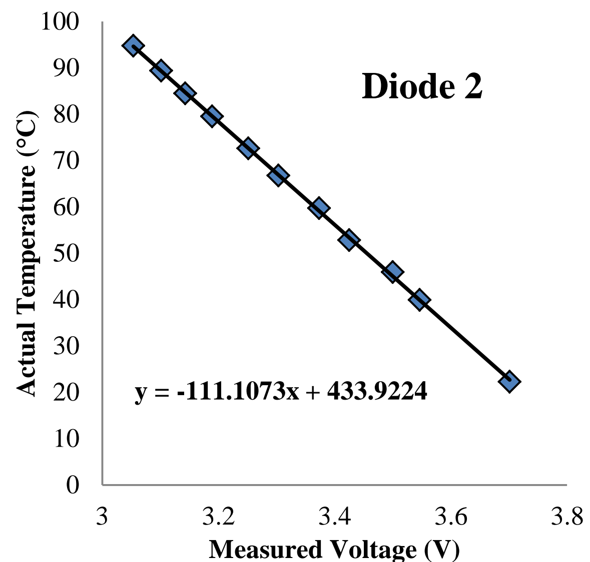
Appendix IV: Calibration

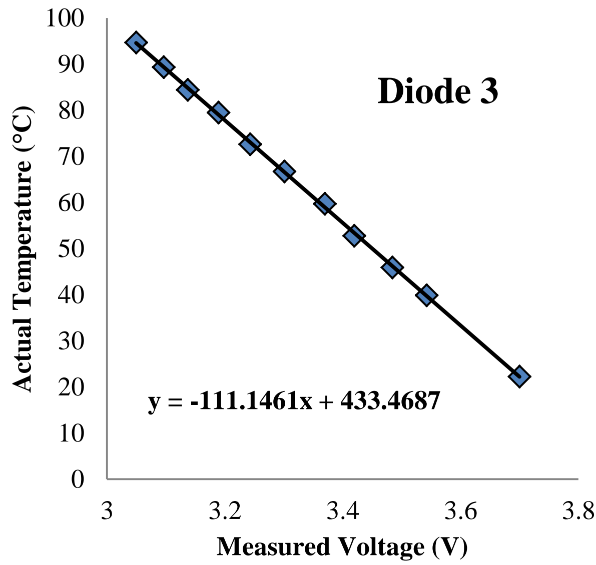
The diodes embedded within each of the three experimental test vehicles, corresponding to each surface condition tested within the current study, were calibrated to the output of a NIST-traceable thermistor induced by the ambient environment within a temperature controlled oven, shown in Figure 1. Further details regarding the functionality and locations of the diodes within the test vehicle can be found in the Electronics Cartridge Assembly Design Motivations and Construction section (Section 3.1). The resistance induced by the temperature within the oven was recorded once it was deemed that the system had reached steady-state, usually occurring after 30 minutes for each data point recorded. In order to build the calibration curves, an initial

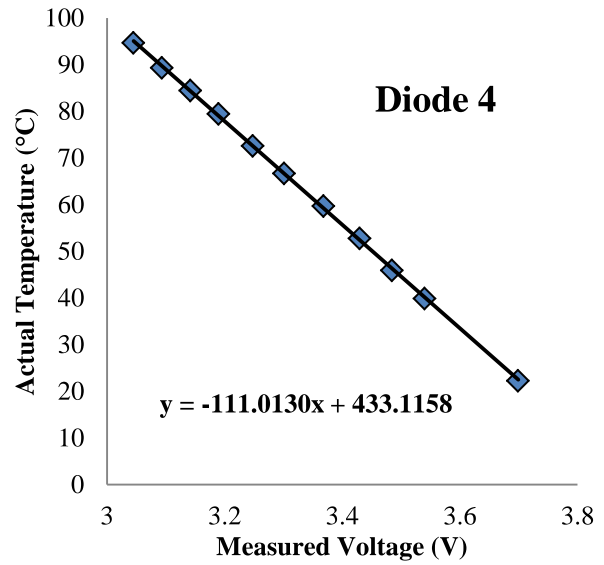
Figure 1 – Temperature controlled oven used for calibration

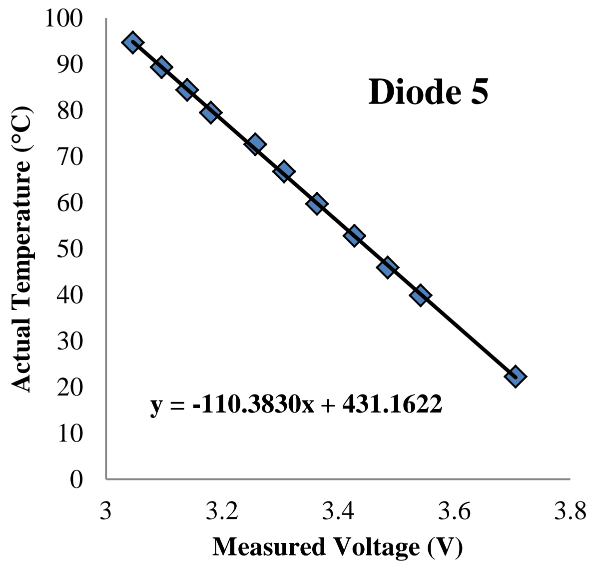
data point at room temperature was recorded. Afterwards, the oven was turned on, and the next data point was recorded at an oven set-point of 38°C-39°C. A total of 10-11 data points were taken where temperature was increased by roughly 5°C-7°C each time after the second data point. To acquire the actual temperature within the oven, the recorded resistance was interpolated using the NIST-traceable calibration curve provided with the thermistor. The thermistor is accurate to within ±0.01°C. In order to induce a voltage within the diodes, a 2.2 mA current was supplied by a Keithley Model 2401 source meter. At a sampling rate of 300 Hz, the induced voltage for each diode is measured for a total of 6 seconds, totaling 1800 measurements for each diode. Precise time measurements for sampling are made possible through the integration of NI 9485 relay cards linked to the Labview VI used for calibration. These relay cards send current to diodes individually throughout the sampling process. With each of the fourteen diodes on a test vehicle acquiring measurements for six seconds each, the total time required for acquisition of all necessary measurements of each data point is roughly a minute and a half. These measurements are averaged to yield the measured voltage seen on the x-axis of the sample curves provided. The sample curves provided are taken from the calibration of the bare silicon surface. Diode 13 was deemed non-operational due to failure of the diode to read a reasonable voltage given the induced current.

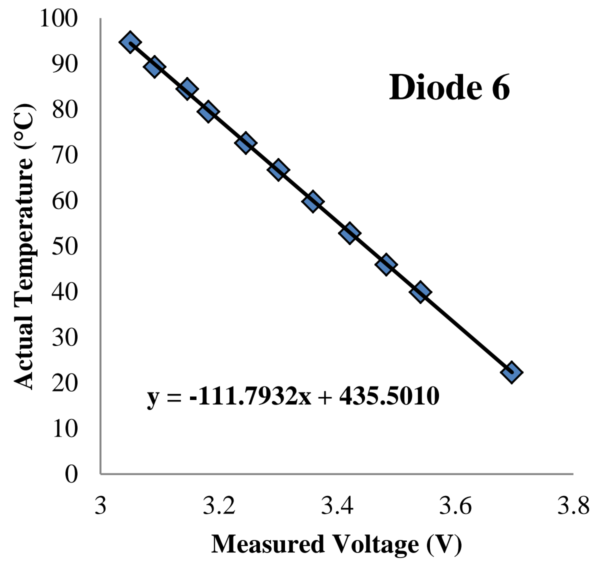


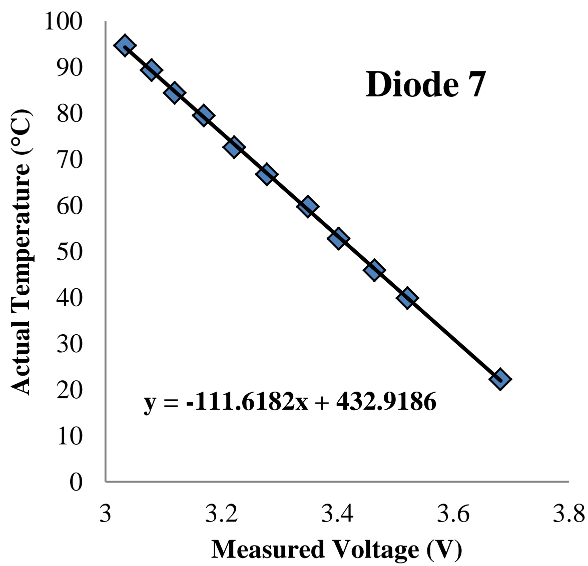


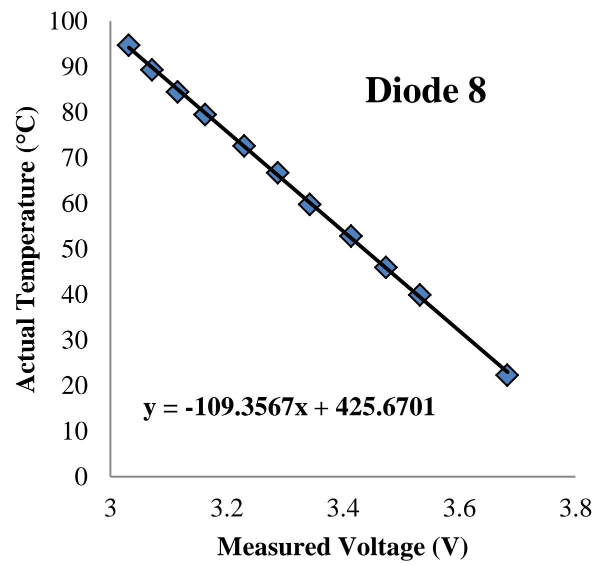

Diode 3
y = -111.1461x + 433.4687
Actual Temperature (°C)
Measured Voltage (V)
0
10
20
30
40
50
60
70
80
90
100
3
3.2
3.4
3.6
3.8

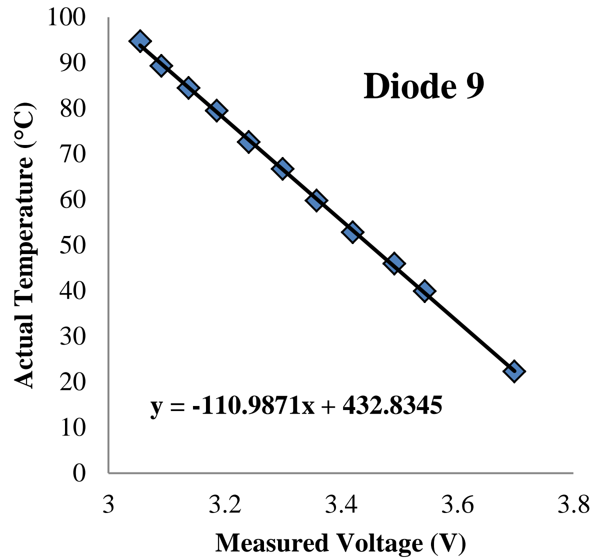

Diode 4
y = -111.0130x + 433.1158
Actual Temperature (°C)
Measured Voltage (V)
0
10
20
30
40
50
60
70
80
90
100
3
3.2
3.4
3.6
3.8

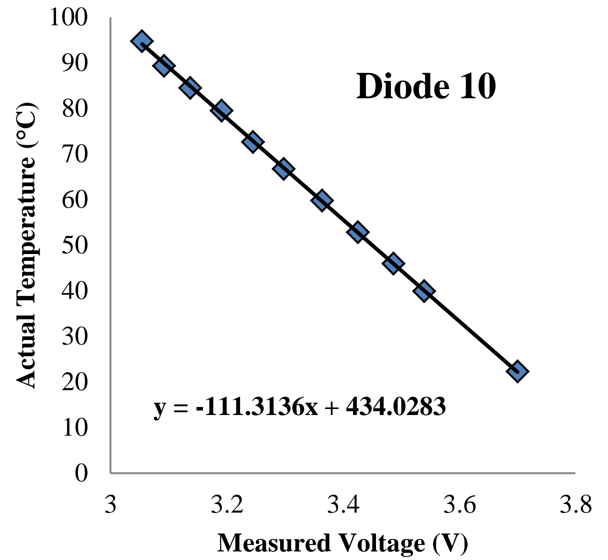

Diode 5
y = -110.3830x + 431.1622
Actual Temperature (°C)
Measured Voltage (V)
0
10
20
30
40
50
60
70
80
90
100
3
3.2
3.4
3.6
3.8

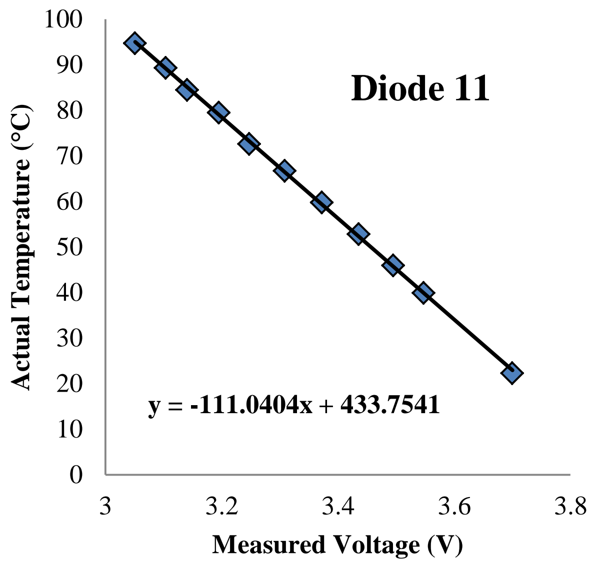

Diode 6
y = -111.7932x + 435.5010
Actual Temperature (°C)
Measured Voltage (V)
0
10
20
30
40
50
60
70
80
90
100
3
3.2
3.4
3.6
3.8

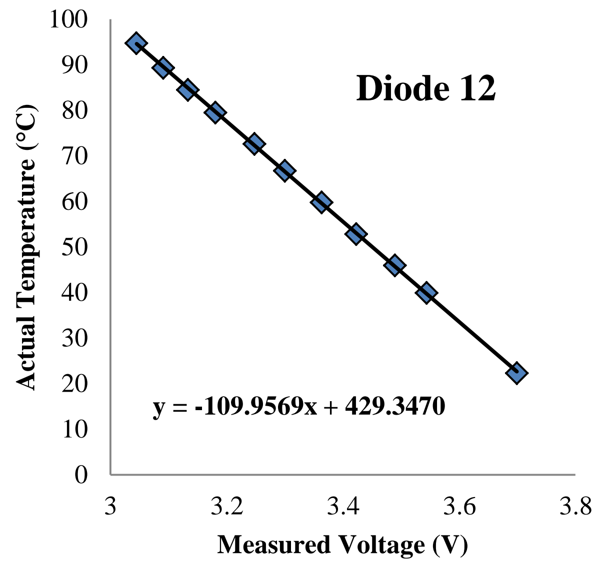

Diode 7
y = -111.6182x + 432.9186
Actual Temperature (°C)
Measured Voltage (V)
0
10
20
30
40
50
60
70
80
90
100
3
3.2
3.4
3.6
3.8

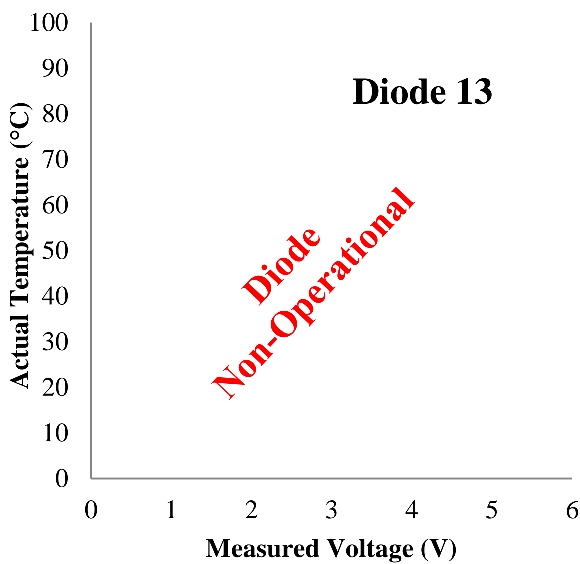

Diode 8
y = -109.3567x + 425.6701
Actual Temperature (°C)
Measured Voltage (V)
0
10
20
30
40
50
60
70
80
90
100
3
3.2
3.4
3.6
3.8

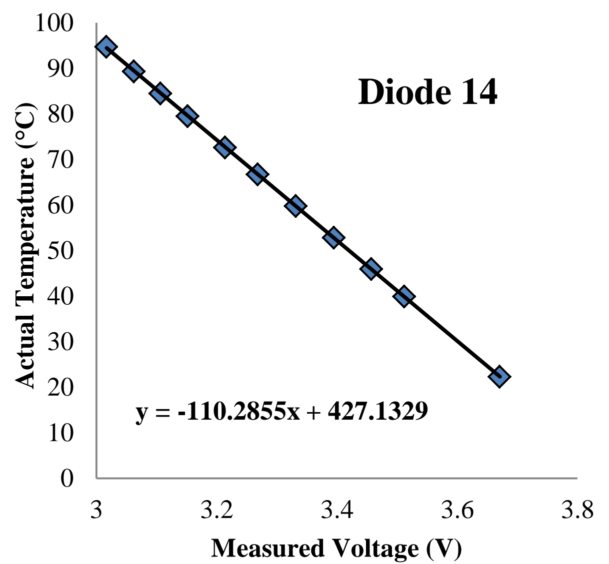

Diode 9
y = -110.9871x + 432.8345
Actual Temperature (°C)
Measured Voltage (V)
100
90
80
70
60
50
40
30
20
10
0
3
3.2
3.4
3.6
3.8


Diode 10
y = -111.3136x + 434.0283
Actual Temperature (°C)
Measured Voltage (V)
100
90
80
70
60
50
40
30
20
10
0
3
3.2
3.4
3.6
3.8


Diode 11
y = -111.0404x + 433.7541
Actual Temperature (°C)
Measured Voltage (V)
100
90
80
70
60
50
40
30
20
10
0
3
3.2
3.4
3.6
3.8


Diode 12
y = -109.9569x + 429.3470
Actual Temperature (°C)
Measured Voltage (V)
100
90
80
70
60
50
40
30
20
10
0
3
3.2
3.4
3.6
3.8


Diode 13
Diode
Non-Operational
Actual Temperature (°C)
Measured Voltage (V)
100
90
80
70
60
50
40
30
20
10
0
0
1
2
3
4
5
6


Diode 14
y = -110.2855x + 427.1329
Actual Temperature (°C)
Measured Voltage (V)
100
90
80
70
60
50
40
30
20
10
0
3
3.2
3.4
3.6
3.8

Since the relationship is linear as shown in the results plotted above for each diode on the bare silicon test vehicle, the calibration curve can be expressed as a linear relationship using the constants "a" and "b" as outlined below:

$$Temperature\ (°C) = a * Measured\ Voltage\ (V) + b$$

The following tables give the constants for the preceding linear equation along with the R-squared value required for uncertainty analysis as shown in Appendix V. The diode locations on the tables below are associated with those shown on Figure 31 and called out on Table 1.

Bare Silicon Surface Test Vehicle

Diode Location	a (1/V)	b (°C)	R-squared
Diode 1	-111.3394	436.2762	0.99993
Diode 2	-111.1073	433.9224	0.99965
Diode 3	-111.1461	433.4687	0.99968
Diode 4	-111.0130	433.1158	0.99976
Diode 5	-110.3830	431.1622	0.99958
Diode 6	-111.7932	435.5010	0.99977
Diode 7	-111.6182	432.9186	0.99970
Diode 8	-109.3567	425.6701	0.99953
Diode 9	-110.9871	432.8345	0.99956
Diode 10	-111.3136	434.0283	0.99973
Diode 11	-111.0404	433.7541	0.99960
Diode 12	-109.9569	429.3470	0.99986
Diode 13	Non-Operational Diode		
Diode 14	-110.2855	427.1329	0.99998

Microporous Surface Test Vehicle

Diode Location	a (1/V)	b (°C)	R-squared
Diode 1	-111.5711	430.1712	0.99998
Diode 2	-111.5947	432.7541	0.99998
Diode 3	-111.4723	429.6801	0.99998
Diode 4	-111.4058	431.9009	0.99998
Diode 5	-109.7515	423.6970	0.99998
Diode 6	-111.1409	430.0801	0.99998
Diode 7	-111.5089	429.6705	0.99999
Diode 8	-111.0504	424.6833	0.99998
Diode 9	-111.2430	423.6530	0.99998
Diode 10	-110.8014	426.7397	0.99998
Diode 11	-110.9069	429.8816	0.99998
Diode 12	-110.9335	430.3837	0.99998
Diode 13	-111.2364	428.6433	0.99998
Diode 14	-110.1650	424.6760	0.99999

Microfinned Surface Test Vehicle

Diode Location	a (1/V)	b (°C)	R-squared
Diode 1	-110.3028	425.2212	0.99998
Diode 2	-110.3753	427.9237	0.99999
Diode 3	-110.2549	424.9122	0.99998
Diode 4	-110.1731	426.9227	0.99998
Diode 5	-110.2206	425.8794	0.99998
Diode 6	-109.9741	427.3755	0.99998
Diode 7	-110.0618	424.2928	0.99998
Diode 8	-110.1014	424.4084	0.99997
Diode 9	-110.0601	427.6947	0.99997
Diode 10	-109.5525	422.7105	0.99998
Diode 11	-109.5758	425.3406	0.99998
Diode 12	-109.5106	425.4940	0.99998
Diode 13	-109.7461	423.5326	0.99998
Diode 14	-109.0296	421.5955	0.99997

Appendix V: Uncertainty Analysis

Average Surface Temperature Analysis:

As shown in Appendix IV: Calibration, linear curves for each diode embedded within the experimental test vehicle were yielded to estimate the surface temperature sensed at a particular location. The average surface temperature used throughout the results presented within this study represents the mean value calculated from the temperature yielded by the locations specified in Table 1 for each surface condition tested. As each diode has a different calibration curve, each diode will have a slightly different uncertainty associated with it. As it is understood fundamentally that the relationship between induced voltage across a diode and temperature is a linear one, a linear regression model was selected to estimate the uncertainty at each diode location. The standard deviation of the slope, σ_a, and that of the intercept, σ_b are calculated using the following equations:

$$\sigma_a = a * \sqrt{\frac{1}{N-2} * \frac{1-R^2}{R^2}} \quad \text{and} \quad \sigma_b = \sigma_a \sqrt{\frac{\sum_i x_i^2}{N}}$$

In these equations, "a" is the slope of the line with units of (1/V), which can be pulled from the tables presented in Appendix IV. The R-squared "R^2" can also be pulled from these same tables for each test surface used. "N" is the number of data points used in the formation of the linear curves shown in Appendix IV. The summation sign under the radical is the sum of the squares of all the dependent variables that make up the data set used to construct the linear

calibration curve. The following table, Table 1, represents the calculation of these values from the bare silicon surface calibration data:

Table 1 - Bare Silicon Surface Calibration Curve Slope and Intercept Standard Deviations

Diode Location	σ_a (1/V)	σ_b (°C)
Diode 1	0.3052	1.0214
Diode 2	2.3023	0.6909
Diode 3	2.1908	0.6585
Diode 4	1.8984	0.5704
Diode 5	2.5107	0.7541
Diode 6	1.8864	0.5672
Diode 7	2.1229	0.6417
Diode 8	2.6074	0.7877
Diode 9	2.5775	0.7749
Diode 10	2.0397	0.6131
Diode 11	2.4763	0.7430
Diode 12	1.4517	0.4365
Diode 13	**Non-Operational**	
Diode 14	0.5790	0.1757

In order to get individual uncertainties for single samples at each diode location, the previous values can be used in a calibration curve uncertainty linear equation as follows:

$$Uncertainty\ (°C) = \sigma_a * Sample\ Voltage\ (V) + \sigma_b$$

The sample voltage used above must take into account the error associated with the NI9220 voltage measurement card. This card's contribution to the uncertainty is accounted for with the following substitution for the sample voltage:

$$Sample\ Voltage\ (V) = Gain\ Error * Voltage\ Reading\ (V) + Offset\ Error$$

From the manufacturer's specifications, the Gain Error above is 0.01% while the Offset Error is ±0.001% of the full operating range, which is 10.5 V. The minimum possible uncertainty is subtracted from the maximum possible uncertainty using the equations above for each data point. These values are then averaged. This average value is then divided by the total

number of samples taken. As it is understood that there is scaling of the voltage involved, it would stand to reason that the maximum possible uncertainty can be expected where the measured voltage is the highest. This is found at the lowest temperatures in the case of diode induced voltage relationships. The following plot shows the reduction of the uncertainty for Diode 1 as the temperature is increased:

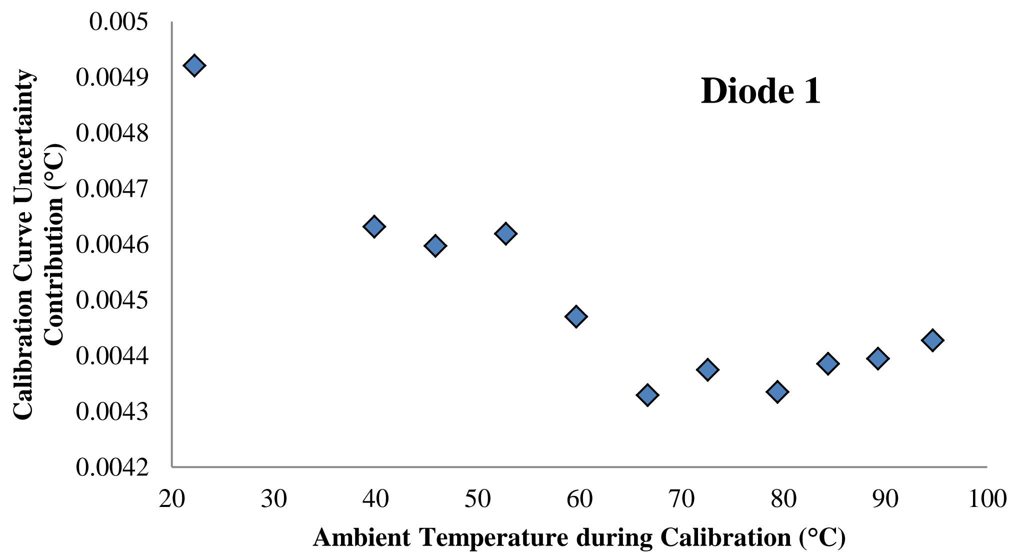


Figure 1 – Plot showing uncertainty reduction as ambient calibration temperature is

With the results of Figure 1 along with expectations regarding the maximum uncertainty occurring at the lowest temperature data point, these beginning points, as opposed to an average, will be used in assessing the worst-case calibration curve uncertainty contribution for each diode location. Table 2 shows the results of this analysis.

When these values are plotted against the diode's respective R-squared value from Appendix IV, shown in Figure 2, the fundamental expectation is illustrated that as R-squared approaches one, uncertainty should be reduced. This lends credence to the assumptions and approach taken thus far in acquiring the uncertainty associated with the calibration curve used at each diode location.

Table 2 - Bare Silicon Surface Calibration Curve Uncertainty Contribution

Diode Location	Calibration Uncertainty Contribution (°C)
Diode 1	0.00492
Diode 2	0.00974
Diode 3	0.00928
Diode 4	0.00814
Diode 5	0.01032
Diode 6	0.00758
Diode 7	0.00859
Diode 8	0.01062
Diode 9	0.01052
Diode 10	0.00842
Diode 11	0.01005
Diode 12	0.00647
Diode 13	**Non-Operational**
Diode 14	0.00298

The contribution to the overall average surface temperature measurement by the calibration curve used to estimate the temperature at each location is all that has been calculated thus far. The other contributing factor to this overall uncertainty is that of the NIST-traceable thermistor, which has a stated accuracy of ±0.01°C. The overall uncertainty is acquired by taking the square root of the sum of the squares

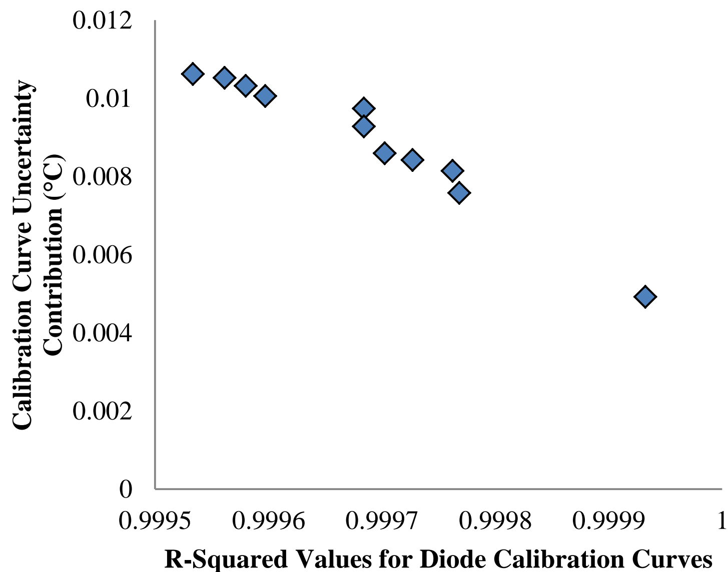


Figure 2 – Plot showing reduction in uncertainty as R-squared value approaches one

of each of these uncertainty contributions. The worst-case diode, Diode 8, is selected for a sample calculation of this overall uncertainty.

$$Overall\ Uncertainty\ (°C) for\ Diode\ 8 = \sqrt{0.01062^2 + 0.01^2} = \pm 0.0146°C$$

As a sample calculation for the uncertainty in the average surface temperature, the highest temperature recorded under pool conditions with FC-72 as the working fluid at a 7°C facility water temperature setting will be conducted.

$$\begin{aligned}&(Diode\ 2\ Temperature\ °C \pm Diode\ 2\ Uncertainty\ °C)\\ &\quad + (Diode\ 6\ Temperature\ °C \pm Diode\ 6\ Uncertainty\ °C)\\ &\quad + (Diode\ 8\ Temperature\ °C \pm Diode\ 8\ Uncertainty\ °C)\\ &\quad + (Diode\ 9\ Temperature\ °C \pm Diode\ 9\ Uncertainty\ °C)\\ &\quad + (Diode\ 10\ Temperature\ °C \pm Diode\ 10\ Uncertainty\ °C)\\ &\quad + (Diode\ 12\ Temperature\ °C \pm Diode\ 12\ Uncertainty\ °C))/6\ Diodes\\ &\quad = Average\ Surface\ Temperature\ Range\ °C\end{aligned}$$

$$\begin{aligned}&((77.61183\ °C + 0.01396\ °C) + (75.957846\ °C + 0.01255\ °C) + (80.605592 + 0.01459)\\ &\quad + (81.661632\ °C + 0.01451\ °C) + (80.155634\ °C + 0.01307\ °C)\\ &\quad + (79.461752\ °C + 0.01191°C))/6\\ &\quad = Maximum\ Average\ Surface\ Temperature\ (°C) = 79.256°C\end{aligned}$$

$$\begin{aligned}&((77.61183\ °C - 0.01396\ °C) + (75.957846\ °C - 0.01255\ °C) + (80.605592 - 0.01459)\\ &\quad + (81.661632\ °C - 0.01451\ °C) + (80.155634\ °C - 0.01307\ °C)\\ &\quad + (79.461752\ °C - 0.01191°C))/6\\ &\quad = Maximum\ Average\ Surface\ Temperature\ (°C) = 79.229°C\end{aligned}$$

$$Recorded\ Temperature = 79.242\ °C$$

$$\boldsymbol{Average\ Surface\ Temperature\ Uncertainty = \pm 0.013\ °C}$$

Heat Flux Analysis:

In order to assess the error in the heat flux there are three measurements that must be properly accounted for, namely the size of the heated elements, the measured current, and the measured power. These three measurements form the heat flux calculation by the following equation:

$$Heat\ Flux\ \left(\frac{W}{cm^2}\right) = \frac{Current\ (A) * Voltage\ (V)}{Heated\ Element\ Area\ (cm^2)}$$

The uncertainty of the heated element area can be attained by the manufacturing tolerance associated with the die cutting process used to shape the features. The saw blade used to cut the silicon wafer is 0.025" thick, and tolerances can be held that are half of a blade width, namely ±0.0125". Manufacturing tolerances are represented by three standard deviations, and can be as high as six. For the purposes of the current analysis, it will be assumed that this tolerance represents three standard deviations. As was done with the previous average surface temperature analysis, two standard deviations will be used to ensure 95% confidence in the resulting value. Since there are four heated elements, each measuring 1 in x 1 in or 1 in^2 (6.452 cm^2) in area, the following calculations show the maximum and minimum surface areas to be used in the overall uncertainty analysis.

$$Maximum\ Single\ Die\ Area\ (cm^2)$$

$$= \left(2.54\ cm + \frac{2}{3} * 0.03175\ cm\right) * \left(2.54\ cm + \frac{2}{3} * 0.03175\ cm\right)$$

$$Maximum\ Single\ Die\ Area\ (cm^2) = 6.560\ cm^2$$

$$Minimum\ Single\ Die\ Area\ (cm^2)$$

$$= \left(2.54\ cm - \frac{2}{3} * 0.03175\ cm\right) * \left(2.54\ cm - \frac{2}{3} * 0.03175\ cm\right)$$

$$Minimum\ Single\ Die\ Area\ (cm^2) = \ 6.345\ cm^2$$

For the current measurement, the manufacturer's specifications for the NI 9227 card used cites a Gain Error of ±0.1% and an Offset Error of ±0.05% based on a range of 7.07 amps. The Offset Error for one measurement is 3.54 mA. However, while the VI is cycling through all 14 diodes for measurements for six seconds each, it is constantly taking current measurements. Therefore, at a sampling rate of 300 Hz, there are a total of 25,200 samples available. Dividing the single sample offset error of 3.54 mA by 25,200 samples, leaves a negligible result. With this number of samples available, the primary source of error in the current measurement is the Gain Error. At the maximum heat flux measured with FC-72 as the working fluid under pool boiling conditions with a 7°C facility water temperature setting, the measured current was 8.67513 A. This measured current was a result of the average of the previously mentioned 25,200 samples. The resulting Gain Error for this value is ±8.68 mA.

For the voltage measurement, the manufacturer's specifications for the NI 9225 card used cites a Gain Error of ±0.05% and an Offset Error of ±0.008% based on a range of 425 V. The Offset Error for one measurement is 34 mV. Just like with the current measurement, the VI is constantly measuring voltage throughout all of the diode cycling. This results in the same number of samples available for measurement, 25,200. Dividing the Offset Error by the number of samples results in a negligible voltage, leaving the Gain Error again as the primary source of error. In the previously cited example from the data, the voltage measured was 37.547 V. The resulting Gain Error for this voltage measurement is ±18.8 mV.

With these values, the following calculations show the maximum, minimum and uncertainty range for the heat flux value at the highest recorded under pool conditions.

$$Maximum\ Heat\ Flux\ \left(\frac{W}{cm^2}\right) = \frac{(8.67518\ A + \ .00868\ A) * (37.547\ V + 0.0188\ V)}{6.345\ cm^2}$$

$$Maximum\ Heat\ Flux\ \left(\frac{W}{cm^2}\right) = \ 12.853\ \frac{W}{cm^2}$$

$$Minimum\ Heat\ Flux\ \left(\frac{W}{cm^2}\right) = \frac{(8.67518\ A - \ .00868\ A) * (37.547\ V - 0.0188\ V)}{6.560\ cm^2}$$

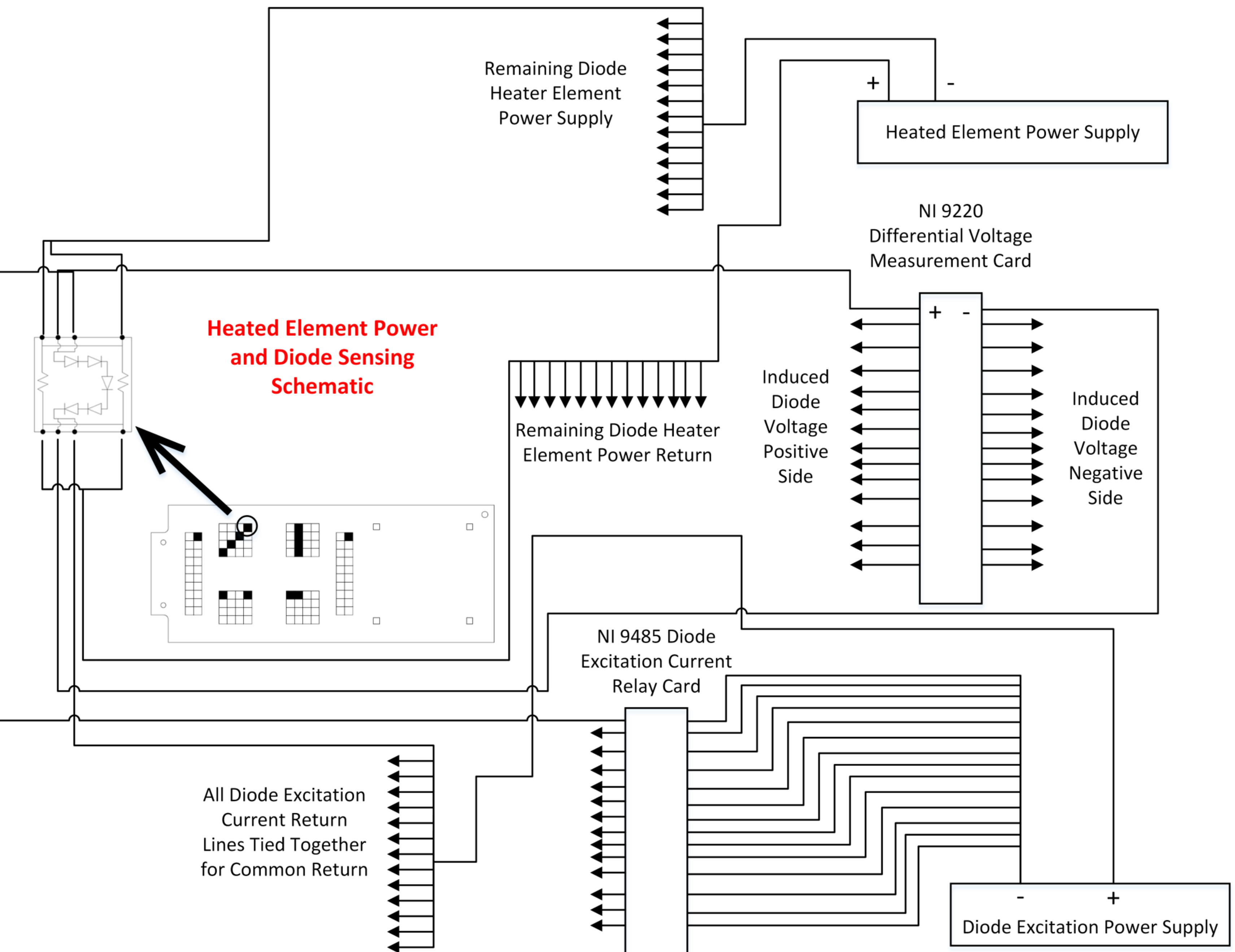
$$Minimum\ Heat\ Flux \left(\frac{W}{cm^2}\right) = \ 12.395\ \frac{W}{cm^2}$$

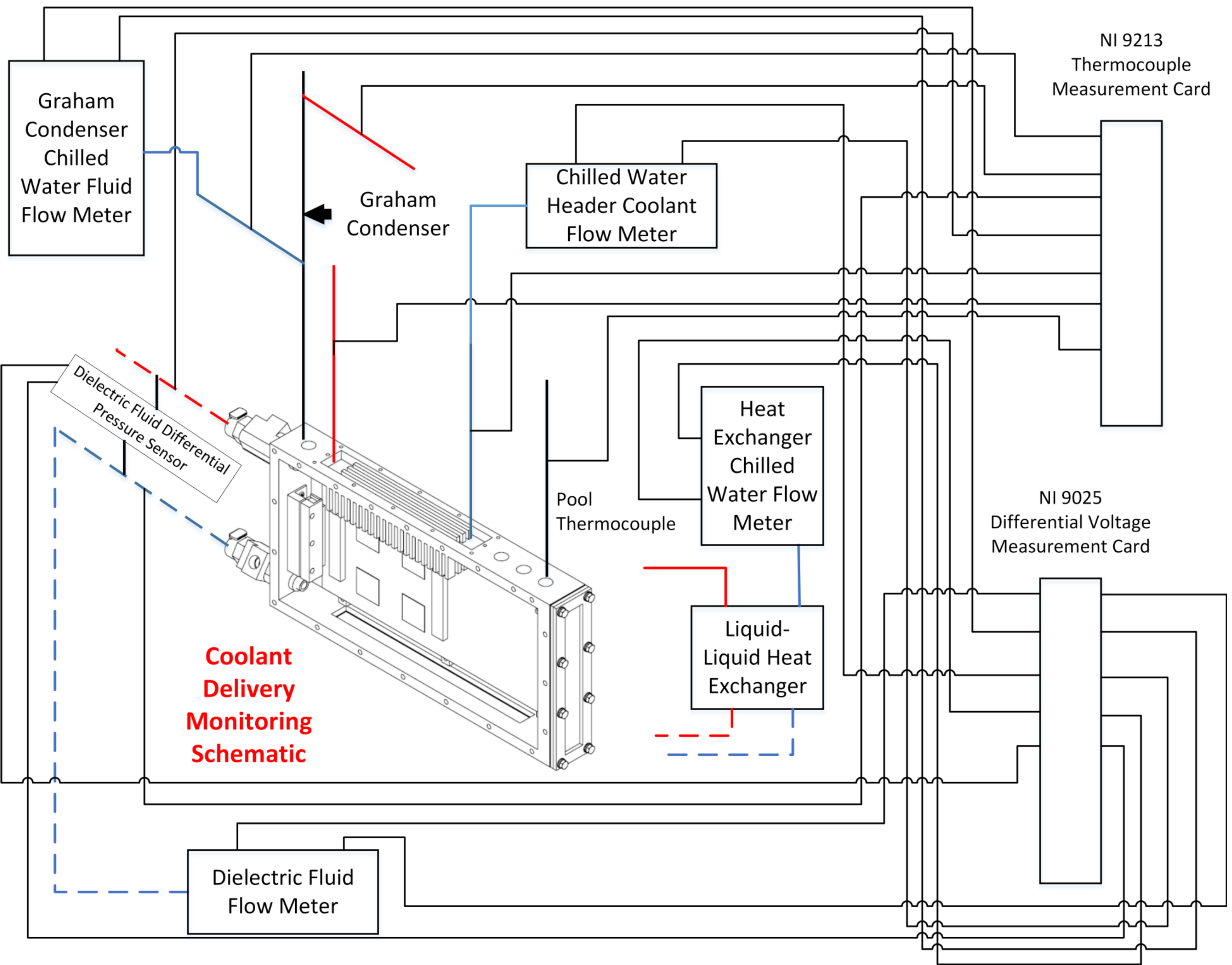
$$Measured\ Heat\ Flux\ Value \left(\frac{W}{cm^2}\right) = \ 12.621\ \frac{W}{cm^2}$$

$$\boldsymbol{Heat\ Flux\ Uncertainty \left(\frac{W}{cm^2}\right) = \ \pm 0.23\ \frac{W}{cm^2}}$$

Appendix VI: Data Acquisition

Strategically placed sensors throughout the experimental facility interfacing with LabView software from National Instruments collected and analyzed the data used within the current study. Further details regarding the design and integration of cooling loop subsystems, embedded temperature monitoring components, and cartridge interfaces can be found in Chapter 3 of the current study. The purpose of this appendix is to provide detailed schematics regarding all of the connectivity necessary to deliver pertinent sensor data to the LabView software via data acquisition card interfaces. There are two schematics provided. The first is that detailing how differential voltages across the diodes for temperature measurement along with power delivery to the heated elements embedded within the thermal test used are delivered. The second schematic presented details how fluid parameter monitoring is connected to the data acquisition software. These fluid parameters include pressure, temperature and fluid flow rate monitoring. All of these parameters are collected with differential pressure monitoring from sensors located at key locations within the experimental facility. Blue lines are meant to indicate cooled liquid, while red lines indicate liquid that has been heated in some way. Dashed lines indicate dielectric fluid flow lines, while solid lines are associated with chilled water fluid delivery. Further details regarding the overall flow loop design is shown in Figure 33.


Remaining Diode
Heater Element
Power Supply
+
-
Heated Element Power Supply
NI 9220
Differential Voltage
Measurement Card
+
-
Heated Element Power
and Diode Sensing
Schematic
Remaining Diode Heater
Element Power Return
Induced
Diode
Voltage
Positive
Side
Induced
Diode
Voltage
Negative
Side
NI 9485 Diode
Excitation Current
Relay Card
All Diode Excitation
Current Return
Lines Tied Together
for Common Return
-
+
Diode Excitation Power Supply


Graham
Condenser
Chilled
Water Fluid
Flow Meter
Graham
Condenser
Chilled Water
Header Coolant
Flow Meter
NI 9213
Thermocouple
Measurement Card
Dielectric Fluid Differential
Pressure Sensor
Pool
Thermocouple
Heat
Exchanger
Chilled
Water Flow
Meter
NI 9025
Differential Voltage
Measurement Card
Liquid-
Liquid Heat
Exchanger
Coolant
Delivery
Monitoring
Schematic
Dielectric Fluid
Flow Meter