DIGITAL IMPLEMENTATION OF CURRENT-MODE CONTROL FOR POWER FACTOR CORRECTION

by

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ABSTRACT

Presented in this dissertation is the implementation of power factor correction (PFC) preregulators controlled by a single microcontroller. Two microcontroller-based PFC preregulator systems, with input voltage sensing and without input voltage sensing, have been constructed and tested experimentally.

By using the on-board peripherals of the microcontroller, hybrid control method is proposed to implement the PFC preregulators, where the analog control loops and digital control loops were integrated into a complete PFC controller. The current loop was constructed by analog peripherals in responding to its fast dynamics, while pure digital control was implemented in the voltage loop. Hardware multiplication was achieved by using an on-board multiplying DAC approach. A ramp signal was generated by a module inside the microcontroller. The amplitude of the ramp signal used to control the switch was modulated and then scaled using the output voltage error. The scaled ramp signal was compared to the inductor current signal to produce the signal which controlled the switch. When implementing PFC preregulator without input voltage sensing, the information related to the input voltage is obtained by sensing the inductor current.

By using the hybrid control method, no complex algorithm or external multiplier was required to perform the PFC function correctly, and thus a one-chip solution has been achieved. Implementation issues for microcontroller-based PFC preregulators were discussed. These issues include system modeling, required functionalities of a

microcontroller, main design procedures, and A/D conversion and time delay, as well as some considerations in hardware and software implementation. The proposed PFC preregulators have been tested successfully in the laboratory, and the measured power factor was above 0.99 at nominal operating conditions, and the output voltage was precisely controlled. Because of the simplicity of the circuit, the proposed PFC preregulator has low cost and high reliability.

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INTRODUCTION

Power factor is a measurement of how efficiently an electrical facility uses electrical energy. When the power factor of an electrical facility is low, power factor correction (PFC) is often required to correct the power factor.

1.1 Overview of Power Factor Correction

In an alternating current (AC) electrical power system, when current waveform has identical shape and phase with the voltage, the power factor reaches its maximum value of 1. When the shape or phase of the current and voltage is different, the power factor is less than 1. A high power factor indicates that electrical capacity is being utilized effectively, while a low power factor indicates poor utilization of electric power.

Low power factors can cause serious problems for electric utility systems, such as lower power capacity, lower efficiency, interference with communication and control signals, errors in metering, and additional heating. For example, a distribution system has to deliver higher current to a load with low power factor than to a load with a power factor closer to 1. The cost of a distribution system that is designed to handle the higher currents is significantly higher than a distribution system that delivers the same useful energy to loads with a power factor closer to 1. In addition, the current with distortion

contains harmonics. Excessive harmonics will seriously deteriorate the power quality and efficiency of the power system.

However, only a pure resistive load has power factor of 1, which is very rare in realistic electrical systems. Thus, power factor correction (PFC) is often required to correct the power factor such that the power factor can be as close as possible to 1. That is, PFC shapes the current drawn from the power system such that the electrical appliance emulates a pure resistor.

PFC can significantly minimize losses and costs associated with the generation and distribution of the electric power with significantly improved power quality. Therefore, PFC is receiving more and more attention these days because of the widespread use of electrical appliances that draw non-sinusoidal current from the electric power systems.

1.2 Power Factor Correction Basics

1.2.1 Power Factor and Power Factor Correction

In an AC power system, power is defined as the rate of energy flow through a given point. Several different kinds of power are used to describe the energy flow. Real power represents a net transfer of energy in one direction in a particular time. Real power is the average of the instantaneous product of current and voltage over a cycle. Meanwhile, energy storage elements such as inductors and capacitors may result in alteration in the direction of energy flow. This portion of power returns to the source in each cycle, and is known as reactive power. Thus, the power in an AC power system can be expressed as:

$$\bar{S} = P + jQ, \tag{1-1}$$

where P is the active power or real power with a unit of watt (W), Q is the reactive power with a unit of volt-amperes reactive (VAR), and $\bar{S}$ is the complex power with a unit of volt-amperes (VA).

It can be seen from (1-1) that the complex power $\bar{S}$ is the vector sum of active and reactive power, and can be illustrated in a complex plane, as shown in Figure 1.1. In Figure 1.1, the phase angle θ is the angle of the voltage relative to the current. The absolute value of the complex power $|\bar{S}|$ is called the apparent power, which is the magnitude of the complex power, and is the product of the rms value of the current and the rms value of the voltage. Equation (1-1) implies that the apparent power is greater than or equal to the real power. This is caused by the stored energy in the load returning back to the source, or because of the non-linear load that distorts the current waveform. The apparent power and the real power are equal only when the reactive power is 0.

The power factor *pf* of an AC electric power system is defined as the ratio of real power to apparent power, or:

$$pf = \frac{P}{|\bar{S}|}. \tag{1-2}$$

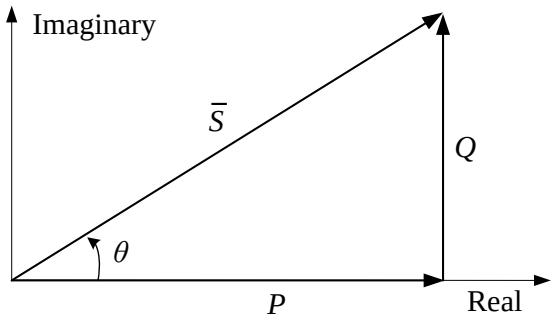


Fig. 1.1 Complex power on a complex plane

Equation (1-2) shows that *pf* is a number in the range of 0 and 1. When both the current and the voltage are sinusoidal, the power factor is the cosine of the phase angle θ between the voltage and the current, or:

$$pf = \cos\theta \tag{1-3}$$

For sinusoidal waveforms, power factor correction (PFC) is to adjust the current phase such that phase angle θ equals 0.

For non-sinusoidal waveforms, (1-3) is no longer valid. Fig. 1.2, for example, illustrates the input voltage and current of an AC/DC rectifier without power factor correction (PFC), as well as the harmonic contents of the input current waveform. The current waveform is not sinusoidal, and the power factor is not one even though the current has the same phase as the voltage. Indeed, the power factor in this case is approximately 0.6.

The degradation of the power factor is caused by harmonics, which can be measure by THD, or total harmonic distortion:

$$THD_I = \frac{\sqrt{I_2^2 + I_3^2 + ...I_n^2}}{I_1}\% \tag{1-4}$$

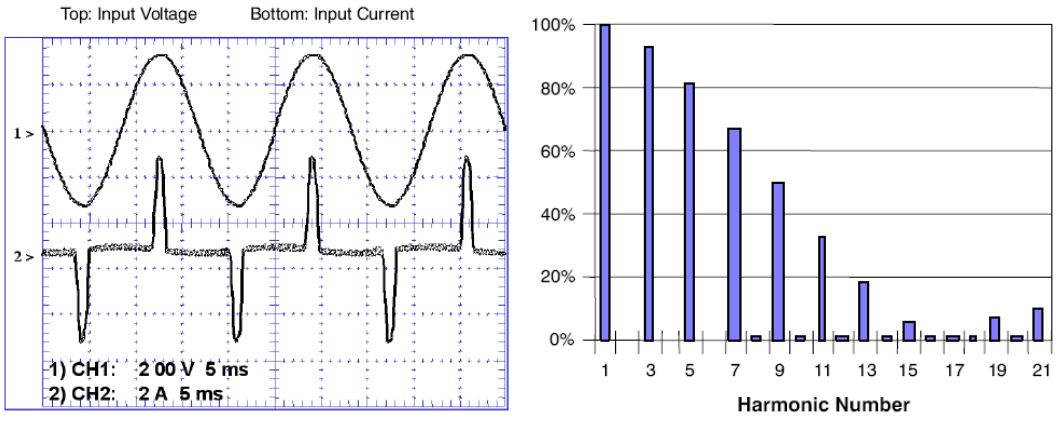


Fig. 1.2 Input characteristics of an AC/DC rectifier without PFC

$$THD_V = \frac{\sqrt{V_2^2 + V_3^2 + ...V_n^2}}{V_1}\% \quad (1\text{-}5)$$

where THD_I is the THD of the input current; THD_V is the THD of the input voltage, I_1 is the current at fundamental frequency; I_2, I_3, …, I_n are the 2nd, 3rd, …, nth harmonics of the input current; V_1 is the voltage at fundamental frequency; V_2, V_3, …, V_n are the 2nd, 3rd, …, nth harmonics of the input voltage.

For non-sinusoidal waveforms, harmonics need to be considered when computing the power factor, which can be expressed as:

$$pf = \frac{P_{in}}{V_1 I_1 \sqrt{(1+THD_V^2)(1+THD_I^2)}} \quad (1\text{-}6)$$

where P_{in} is the input power of the load.

In a practical AC/DC converter, the input voltage and input current are roughly in phase, so the contributions of the harmonics above the fundamental to P_{in} are small. Therefore, $P_{in} \approx V_1 I_1$. Also, THD_V is small, usually less than 10%, so the power factor can be computed by:

$$pf \le \frac{1}{\sqrt{1+THD_I^2}} \quad (1\text{-}7)$$

The equation above implies that, in an AC/DC converter, the main purpose of PFC is to reduce THD. Fig. 1.3 shows the input characteristics of a power supply with PFC, and the harmonic contents of the input current waveform. The power factor of this power supply is approximately 1.0.

1.2.2 Passive PFC

There are two types of PFC, active PFC and passive PFC. Passive PFC uses passive components (capacitors and inductors) to compensate the harmonics and phase

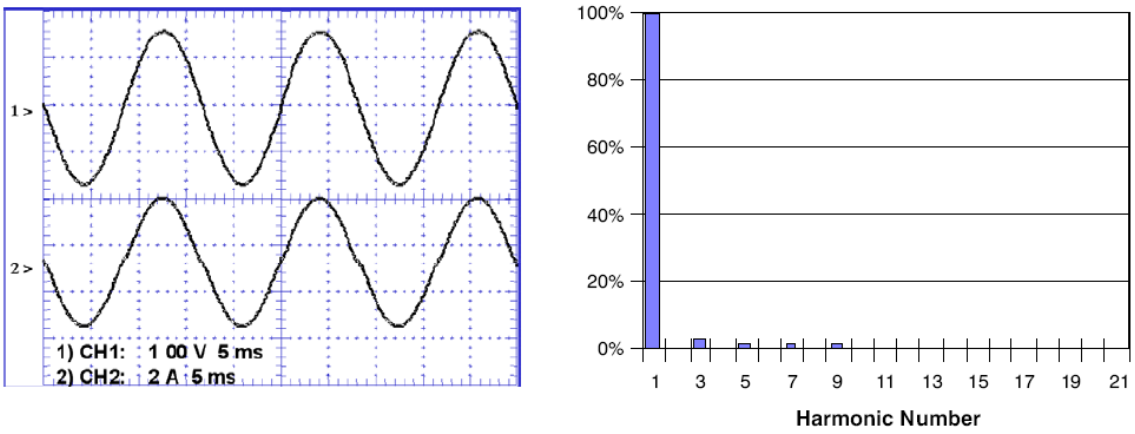


Fig. 1.3 Input characteristics of a power supply with near-perfect PFC

shift. Active PFC employs active components (switches) with control circuitry.

Passive PFC, as a traditional approach, is widely used in power systems. Passive PFC uses low-frequency capacitive and/or inductive filter components to correct the poor power factor. Passive PFC is a simple system and is easy to design because of fewer components, especially the absence of active switches and control circuitry. As a result, passive PFC yields higher reliability, and sometimes smaller size than active PFC. However, it is difficult for a passive PFC to reach high power factor. A typically passive PFC can only yield a power factor of 0.6 or 0.7. When the power is more than 150 Watts, the capacitors become bulky and expensive. Another important disadvantage of passive PFC is lack of flexibility. Usually, a certain passive PFC system is only suitable for limited operating conditions. When the operating condition (such as the input voltage or the load) changes, passive PFC may no longer satisfy the required specifications. For these reasons, passive PFC usually cannot utilize the full energy potential of the AC line. Passive PFC is usually used in a power supply system less than 250 Watts, and high power factor is not critical.

1.2.3 Active PFC

An active PFC system is a power electronic system that controls the current drawn from the utility system in order to obtain a unity power factor. Active PFC is widely used in high-power applications (>250 Watts).

Typically, an active PFC system contains two stages. The first stage is the rectifier. For a single phase system, a full-bridge rectifier consists of four diodes. The second stage, which is the PFC stage, is usually a boost converter or a flyback converter. Some other power converter topologies, such as buck and buck-boost converters, can also be used in active PFC systems.

For example, in a switching-mode power supply, an active PFC preregulator using boost or flyback topology is frequently inserted after the rectifier, and then another switching-mode power converter produces the desired voltage from the DC output of the PFC preregulator. An active PFC preregulator controls the input current in response to the input voltage, such that the input current waveform matches the input voltage waveform. This is the very common type of PFC used in today's power supplies.

An active PFC system requires more expensive and complex circuitry, with a typical efficiency loss of 5 to 10%. However, active PFC has the important advantage of nearly perfect correction. It can make the load look like a simple resistor, that is, the power factor is approximately 1. Active PFC can remarkably diminish THD and is capable of a full range of input voltage.

1.2.4 Boost Converter

In PFC applications, it is desired to shape the waveform of the input current to be identical to the input voltage, and the boost configuration is ideal for current mode

control because the inductor current is the input current. When used in PFC, the boost converter (step-up converter) has the advantages of simplicity of topology, and can achieve near perfect correction for the input current [1].

The boost converter is one of the basic switching-mode dc-dc converter topologies and produces an output voltage higher than the input voltage. When the output voltage needs to be lower than the input voltage, the boost converter is used as the preregulator, and a buck type converter can be attached at its output. For generality and simplicity, boost converter topology is used in this dissertation.

Fig. 1.4 illustrates a boost converter. Obviously, a boost converter is a time-varying nonlinear system because of the switching behavior in the circuit. When the switch is turned on, the current flows through the inductor and energy is stored in it. When the switch is turned off, the stored energy in the inductor tends to collapse and its polarity changes such that it adds to the input voltage. Thus, the voltage across the inductor and the input voltage are in series and together charge the output capacitor to a voltage higher than the input voltage. The key principle that drives the boost converter is the tendency of an inductor to resist changes in current. In a boost converter, the output voltage is always higher than the input voltage.

In order to obtain the transfer function of the boost converter for design purposes, the system must be linearized first. Usually, the averaged switch model [2] is used to

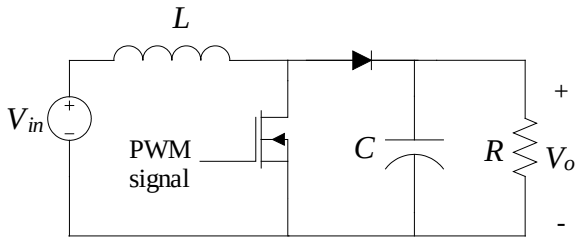


Fig. 1.4 A boost converter

derive the transfer function. In order to simplify the derive process, the equivalent series resistors (ESRs) of the inductor and the output capacitor are ignored.

A boost converter can be viewed as Fig. 1.5, in which Fig. 1.4 is split into two states: the switch is closed (on-state) and the switch is opened (off-state). In the on-state, the energy in the inductor increases with the increasing current, while the energy that stored in the capacitor is delivered to the load. In the off-state, the inductor current transfers the energy accumulated during the on-state into the capacitor which provides energy to the load. In each state, the system is linear. The on-state, shown in Fig. 1.5 (a), can be expressed as:

$$C\frac{dv_o}{dt} = -\frac{v_o}{R} \text{ , and } L\frac{di_L}{dt} = v_{in}. \tag{1-8}$$

That is:

$$\frac{d}{dt}\begin{bmatrix} v_o \\ i_L \end{bmatrix} = \begin{bmatrix} -\frac{1}{RC} & 0 \\ 0 & 0 \end{bmatrix}\begin{bmatrix} v_o \\ i_L \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{1}{L} \end{bmatrix} v_{in}. \tag{1-9}$$

Fig. 1.5 (b) can be written as:

$$C\frac{dv_o}{dt} = i_L - \frac{v_o}{R} \text{, and } L\frac{di_L}{dt} = v_{in} - v_o. \tag{1-10}$$

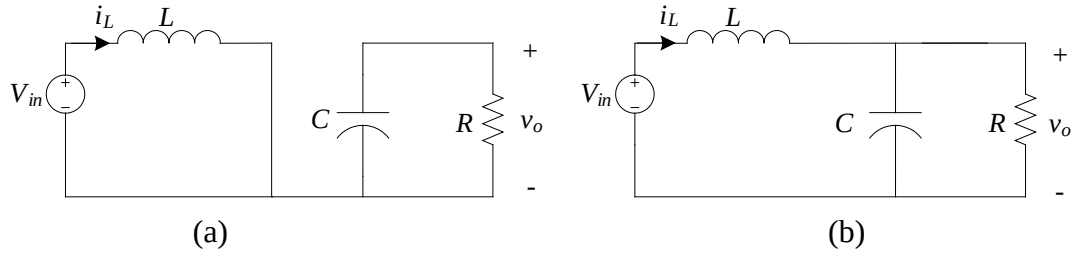


Fig. 1.5 Boost converter: (a) switch is closed (on-state), (b) switch is opened (off-state)

That is:

$$\frac{d}{dt}\begin{bmatrix} v_o \\ i_L \end{bmatrix} = \begin{bmatrix} -\frac{1}{RC} & \frac{1}{C} \\ -\frac{1}{L} & 0 \end{bmatrix}\begin{bmatrix} v_o \\ i_L \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{1}{L} \end{bmatrix} v_{in}. \tag{1-11}$$

When the duty cycle is d, and $d' = 1 - d$, using the averaged switch model, the average of (1-9) and (1-11) can be expressed by:

$$\frac{d}{dt}\begin{bmatrix} v_o \\ i_L \end{bmatrix} = d\left(\begin{bmatrix} -\frac{1}{RC} & 0 \\ 0 & 0 \end{bmatrix}\begin{bmatrix} v_o \\ i_L \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{1}{L} \end{bmatrix} v_{in}\right) + d'\left(\begin{bmatrix} -\frac{1}{RC} & \frac{1}{C} \\ -\frac{1}{L} & 0 \end{bmatrix}\begin{bmatrix} v_o \\ i_L \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{1}{L} \end{bmatrix} v_{in}\right)$$

$$\Rightarrow \frac{d}{dt}\begin{bmatrix} v_o \\ i_L \end{bmatrix} = \begin{bmatrix} -\frac{1}{RC} & \frac{d'}{C} \\ -\frac{d'}{L} & 0 \end{bmatrix}\begin{bmatrix} v_o \\ i_L \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{1}{L} \end{bmatrix} v_{in}. \tag{1-12}$$

For large signals, $v_{in} = V_{in}$, $v_o = V_o$, $i_L = I_L$, $d = D$ and $d' = D' = 1 - D$ all are constant, so:

$$\begin{bmatrix} -\frac{1}{RC} & \frac{D'}{C} \\ -\frac{D'}{L} & 0 \end{bmatrix}\begin{bmatrix} V_o \\ I_L \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{1}{L} \end{bmatrix} V_{in} = 0, \tag{1-13}$$

That is:

$$\begin{cases} \frac{V_o}{V_{in}} = \frac{1}{D'} \\ I_L = \frac{V_o}{RD'} \end{cases}. \tag{1-14}$$

Equation (1-14) is the familiar large-signal dc model for the boost converter and shows that V_o is proportional to D'. However, when D is above 80~85%, (1-14) is no longer valid, because V_o will decrease with an increased V_{in} when the duty-cycle D is above approximately 85%. Fig. 1.6 shows the relationship between output voltage and duty cycle [3], which indicates that a boost converter has two operating point for a given V_o. Obviously, one of the operating points is not stable, so D must be limited to less than 85% to ensure proper operating conditions. Therefore, for a boost converter, a mechanism is needed to limit the maximum duty cycle.

Average small-signal ac model for a boost converter can also be obtained through (1-14). In order to obtain the control effort to output transfer function, $G_{vd}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)}$, it is assumed v_{in} = V_{in} = constant. When there is a positive duty cycle perturbation $D + \hat{d}$ (which is equivalent to $D' - \hat{d}$), both v_o and i_L will increase a little bit. Thus, (1-12) can be written as:

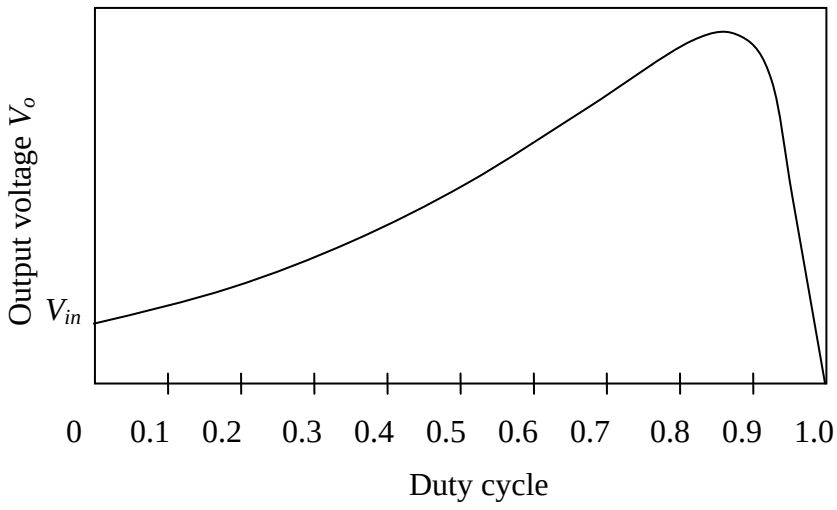


Fig. 1.6 Output voltage change with duty cycle for a boost converter [3]

$$\frac{d}{dt}\begin{bmatrix}\hat{v}_o\\ \hat{i}_L\end{bmatrix}=\begin{bmatrix}-\frac{1}{RC} & \frac{D'-\hat{d}}{C}\\ -\frac{D'-\hat{d}}{L} & 0\end{bmatrix}\begin{bmatrix}V_0+\hat{v}_o\\ I_L+\hat{i}_L\end{bmatrix}+\begin{bmatrix}0\\ \frac{1}{L}\end{bmatrix}V_{in}\,. \tag{1-15}$$

Rearranging (1-15), the following equation can be obtained:

$$\begin{aligned}\frac{d}{dt}\begin{bmatrix}\hat{v}_o\\ \hat{i}_L\end{bmatrix}=&\begin{bmatrix}-\frac{1}{RC} & \frac{D'}{C}\\ -\frac{D'}{L} & 0\end{bmatrix}\begin{bmatrix}\hat{v}_o\\ \hat{i}_L\end{bmatrix}+\begin{bmatrix}0 & \frac{-\hat{d}}{C}\\ \frac{\hat{d}}{L} & 0\end{bmatrix}\begin{bmatrix}V_o\\ I_L\end{bmatrix}\\ &+\begin{bmatrix}-\frac{1}{RC} & \frac{D'}{C}\\ -\frac{D'}{L} & 0\end{bmatrix}\begin{bmatrix}V_o\\ I_L\end{bmatrix}+\begin{bmatrix}0\\ \frac{V_{in}}{L}\end{bmatrix}+\begin{bmatrix}0 & \frac{-\hat{d}}{C}\\ \frac{\hat{d}}{L} & 0\end{bmatrix}\begin{bmatrix}\hat{v}_o\\ \hat{i}_L\end{bmatrix}.\end{aligned} \tag{1-16}$$

Substitute (1-14) into (1-16), $\begin{bmatrix}-\frac{1}{RC} & \frac{D'}{C}\\ -\frac{D'}{L} & 0\end{bmatrix}\begin{bmatrix}V_o\\ I_L\end{bmatrix}+\begin{bmatrix}0\\ \frac{V_{in}}{L}\end{bmatrix}$ is canceled out. Also, considering that $\hat{d}'$, $\hat{i}_L$ and $\hat{v}_o$ are small signal perturbations, their product should be very small. Therefore, the term $\begin{bmatrix}0 & \frac{-\hat{d}}{C}\\ \frac{\hat{d}}{L} & 0\end{bmatrix}\begin{bmatrix}\hat{v}_o\\ \hat{i}_L\end{bmatrix}=\begin{bmatrix}\frac{-\hat{d}\hat{i}_L}{C}\\ \frac{\hat{d}\hat{v}_o}{L}\end{bmatrix}$ is approximately zero. Thus, (1-16) can be rewritten as:

$$\frac{d}{dt}\begin{bmatrix}\hat{v}_o\\ \hat{i}_L\end{bmatrix}=\begin{bmatrix}-\frac{1}{RC} & \frac{D'}{C}\\ -\frac{D'}{L} & 0\end{bmatrix}\begin{bmatrix}\hat{v}_o\\ \hat{i}_L\end{bmatrix}+\begin{bmatrix}0 & \frac{-\hat{d}}{C}\\ \frac{\hat{d}}{L} & 0\end{bmatrix}\begin{bmatrix}V_o\\ I_L\end{bmatrix}. \tag{1-17}$$

Rearrange (1-17) and replace I_L by (1-14), then (1-17) becomes:

$$\frac{d}{dt}\begin{bmatrix}\hat{v}_o\\ \hat{i}_L\end{bmatrix}=\begin{bmatrix}-\frac{1}{RC} & \frac{D'}{C}\\ -\frac{D'}{L} & 0\end{bmatrix}\begin{bmatrix}\hat{v}_o\\ \hat{i}_L\end{bmatrix}+\begin{bmatrix}-\frac{V_o}{RCD'}\\ \frac{V_o}{L}\end{bmatrix}\hat{d}. \tag{1-18}$$

The control-to-output transfer function $G_{vd}(s)$ can be derived as:

$$G_{vd}(s)=\frac{\hat{v}_o(s)}{\hat{d}(s)}=[1 \quad 0]\begin{bmatrix}s+\frac{1}{RC} & -\frac{D'}{C}\\ \frac{D'}{L} & s\end{bmatrix}^{-1}\begin{bmatrix}-\frac{V_o}{RCD'}\\ \frac{V_o}{L}\end{bmatrix}$$

$$G_{vd}(s)=\frac{V_o}{D'}\frac{1-\frac{L}{RD'^2}s}{1+\frac{L}{RD'^2}s+\frac{LC}{D'^2}s^2}. \tag{1-19}$$

Similarly, the control-to-inductor-current transfer function $G_{id}(s)$ can be derived:

$$G_{id}(s)=\frac{\hat{i}_L(s)}{\hat{d}(s)}=[0 \quad 1]\begin{bmatrix}s+\frac{1}{RC} & -\frac{D'}{C}\\ \frac{D'}{L} & s\end{bmatrix}^{-1}\begin{bmatrix}-\frac{V_o}{RCD'}\\ \frac{V_o}{L}\end{bmatrix}$$

$$G_{id}(s)=\frac{\frac{2V_o}{D'^2R}(1+\frac{RC}{2}s)}{1+\frac{L}{D'^2R}s+\frac{LC}{D'^2}s^2}. \tag{1-20}$$

When there is a perturbation $\hat{v}_g$ in the input voltage, both v_o and i_L will change a little bit. In order to obtain the line-to-output transfer function, $G_{vg}(s)=\frac{\hat{v}_o(s)}{\hat{v}_g(s)}$, it is assumed that the duty cycle is constant, that is, $d' = D'$ = constant. Thus, (1-12) can be written as:

$$\frac{d}{dt}\begin{bmatrix}\hat{v}_o\\ \hat{i}_L\end{bmatrix}=\begin{bmatrix}-\frac{1}{RC} & \frac{D'}{C}\\ -\frac{D'}{L} & 0\end{bmatrix}\begin{bmatrix}V_0+\hat{v}_o\\ I_L+\hat{i}_L\end{bmatrix}+\begin{bmatrix}0\\ \frac{1}{L}\end{bmatrix}(V_{in}+\hat{v}_g)\,. \tag{1-21}$$

Rearranging (1-21), the following equation can be obtained:

$$\frac{d}{dt}\begin{bmatrix}\hat{v}_o\\ \hat{i}_L\end{bmatrix}=\begin{bmatrix}-\frac{1}{RC} & \frac{D'}{C}\\ -\frac{D'}{L} & 0\end{bmatrix}\begin{bmatrix}\hat{v}_o\\ \hat{i}_L\end{bmatrix}+\begin{bmatrix}0\\ \frac{1}{L}\end{bmatrix}\hat{v}_g+\begin{bmatrix}-\frac{1}{RC} & \frac{D'}{C}\\ -\frac{D'}{L} & 0\end{bmatrix}\begin{bmatrix}V_o\\ I_L\end{bmatrix}+\begin{bmatrix}0\\ \frac{V_{in}}{L}\end{bmatrix}. \tag{1-22}$$

Substitute (1-14) into (1-22), $\begin{bmatrix}-\frac{1}{RC} & \frac{D'}{C}\\ -\frac{D'}{L} & 0\end{bmatrix}\begin{bmatrix}V_o\\ I_L\end{bmatrix}+\begin{bmatrix}0\\ \frac{V_{in}}{L}\end{bmatrix}$ is canceled out, and (1-22) is simplified to:

$$\frac{d}{dt}\begin{bmatrix}\hat{v}_o\\ \hat{i}_L\end{bmatrix}=\begin{bmatrix}-\frac{1}{RC} & \frac{D'}{C}\\ -\frac{D'}{L} & 0\end{bmatrix}\begin{bmatrix}\hat{v}_o\\ \hat{i}_L\end{bmatrix}+\begin{bmatrix}0\\ \frac{1}{L}\end{bmatrix}\hat{v}_g. \tag{1-23}$$

Then, the line-to-output transfer function $G_{vg}(s)$ can be derived as:

$$G_{vg}(s)=\frac{\hat{v}_o(s)}{\hat{v}_g(s)}=[1\quad 0]\begin{bmatrix}s+\frac{1}{RC} & -\frac{D'}{C}\\ \frac{D'}{L} & s\end{bmatrix}^{-1}\begin{bmatrix}0\\ \frac{1}{L}\end{bmatrix}$$

$$G_{vg}(s)=\frac{1}{D'}\frac{1}{1+\frac{L}{RD'^2}s+\frac{LC}{D'^2}s^2}\,. \tag{1-24}$$

Equation (1-18) is the linearized state space representation of the open-loop boost converter, and (1-19), (1-20) and (1-24) are its corresponding transfer functions.

Notice that (1-13) ~ (1-24) are based on the assumption that variations of the inductor current i_L are very small, known as continuous conduction mode (CCM). This assumption is valid only when the boost converter operates at CCM. Therefore, (1-18) ~ (1-24) only represent the CCM boost converter model. For the discontinuous conduction mode (DCM), where the inductor current i_L is discontinuous, the model described here is no longer valid. Since CCM is selected in this dissertation, the DCM boost converter model is not derived here.

The CCM boost converter model is derived with another assumption that V_{in} and R are constant. When V_{in} or R changes, the system model also changes. Therefore, the compensator designed at nominal conditions may not operate correctly when V_{in} or R changes to other values. Indeed, it is commonly desired that the system can operate correctly under other possible conditions. Therefore, possible operating conditions should be determined first before designing the controller, which should have sufficient stability margins to compensate for the uncertainty.

Equation (1-19) shows that the boost converter has a right half-plane zero. This zero in $G_{vd}(s)$ has negligible magnitude at low frequency. However, at high frequency, it causes a phase reversal. Therefore, the boost converter has a more complicated dynamics than other simple topologies, and it is difficult to obtain a traditional single-loop controller with wide bandwidth.

1.3 Active Power Factor Correction Systems

In the active PFC system shown in Fig. 1.7, the current loop monitors and maintains the inductor current equal to a reference current, acting as a current source. This current source characteristic means that the power converter can shape the inductor

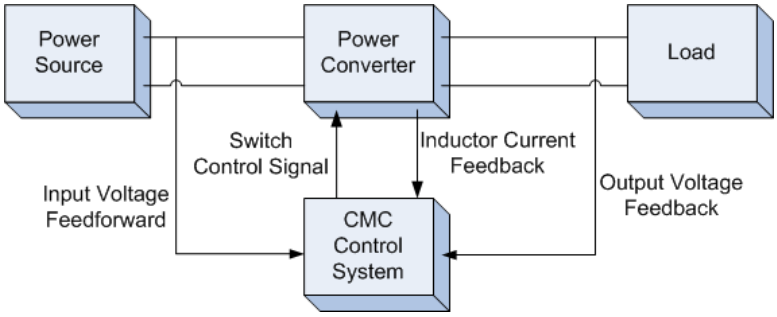


Fig. 1.7 Block diagram of a conventional active PFC system

current by defining the reference current. This current reference is set by the multiplication of the voltage error from the output voltage feedback loop and the waveform from the input voltage feed forward loop, such that the output voltage maintains the desired nominal value while shaping the inductor current always in phase with the input voltage.

1.3.1 Conventional Analog Active PFC

Active PFC systems have been successfully implemented for many years using analog circuit technology and linear system design techniques with good performance and low cost [20][41]. PFC typically utilizes an average current-mode control (ACMC) technique combined with input voltage sensing, and a basic analog active PFC is shown in Fig. 1.8.

In Fig. 1.8, the PFC control system is very like other regular ACMC system, where the current in the inner current loop is programmed according to the compensator output in the outer voltage loop such that the desired output voltage is achieved. However, the current loop compensator programs the input current, not the output current, and the reference of current loop compensator not only relates to the output voltage, but also the line voltage waveform. That is, the current loop reference is

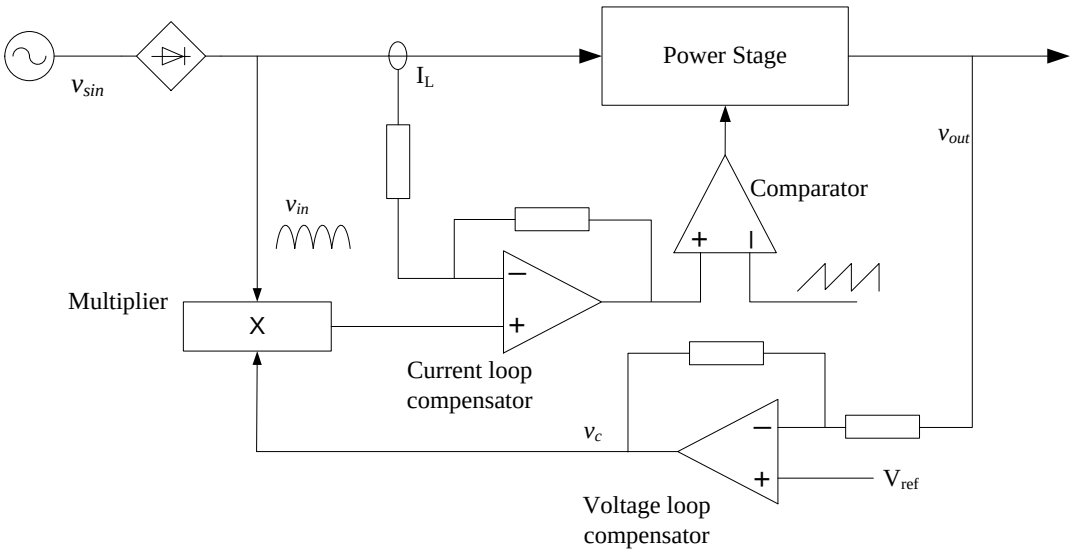


Fig. 1.8 Basic analog active PFC system

proportional to the voltage loop output multiplied by the half sinusoidal waveform derived from the rectified line voltage.

In the basic PFC system, within each half cycle, the instantaneous current must be directly proportional to the instantaneous line voltage in order to have a good power factor. When the load is a constant, the output voltage should not change with the 60Hz sinusoidal variation of the line voltage. This requires strong closed loop intervention to correct, and the voltage control loop bandwidth must be much less than 120 Hz. Typically, the maximum crossover frequency is about 20 Hz at the most.

However, in order to maintain constant power, the line current must be inversely proportional to the line voltage. When the line voltage changes rapidly, the low bandwidth voltage loop will not be able to response fast enough, and thus cause considerable change in the dc output voltage. An effective solution to this dilemma is to add an input voltage feed-forward loop to the main control circuit. With input voltage feed-forward, the control circuit can respond to a line voltage change within a half cycle.

It can be derived that the instantaneous power of the close-loop basic active PFC system is proportional to V_{in}^2, the square of the RMS input voltage [20]. In order to make the overall loop gain and bandwidth independent of V_{in}, the controller loop can be divided by a gain V_{in}^2.

Fig. 1.9 illustrates a PFC system with input voltage feed-forward. In this system, the low-pass filter in the feed-forward loop is simply a RC network. The feed-forward voltage must be constant during each half cycle. Otherwise, any ripple in the feed-forward voltage will be added to the 120 Hz ripple from the error amplifier, resulting in increasing the input current waveform distortion and decreasing power factor. Therefore, the bandwidth of the RC network in the voltage feed-forward loop must be low enough. However, too low bandwidth will result in overshoot on the dc voltage when the line voltage changes rapidly by a large amount, and the voltage feed-forward will not be able

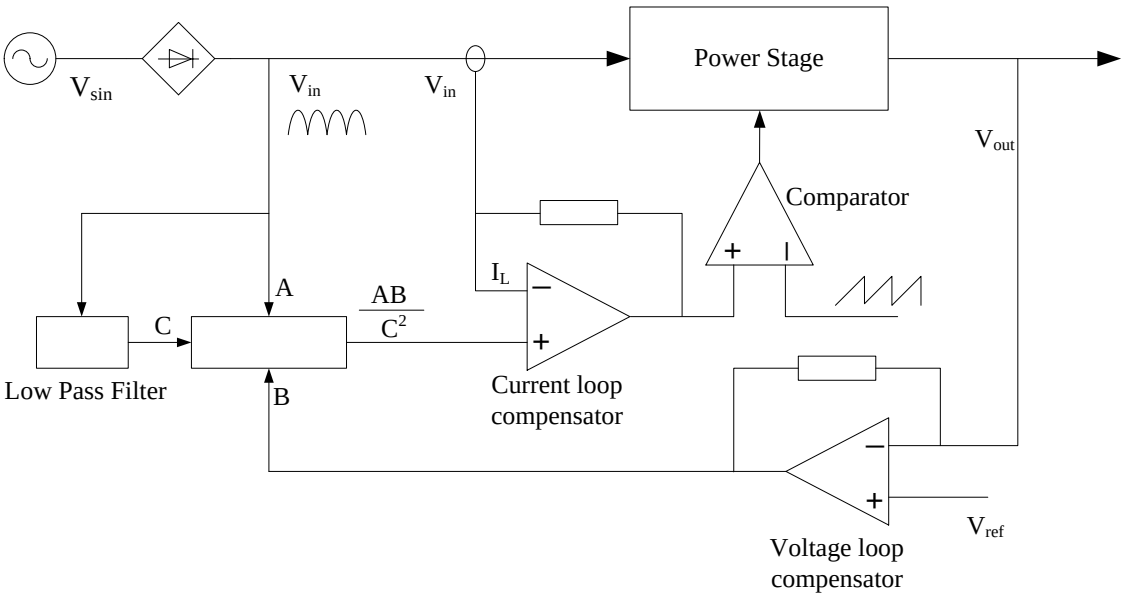


Fig. 1.9 Analog active PFC system with input voltage feed-forward

to function properly to reduce the overshoot. Thus, designing the voltage feed-forward loop becomes a tradeoff between lower overshoot and lower distortion. When the variation of the line voltage is small or slow enough, there is no need to insert the voltage feed-forward loop. For this reason, the voltage feed-forward loop will not be considered in this dissertation.

In an analog active PFC system, both the current loop compensator and the voltage loop compensator are analog components, typically operational amplifiers. Although the control system in Fig. 1.9 looks complicated, some integrated circuits (IC) on the market have integrated the current loop compensator, voltage loop compensator, feed-forward loop, multiplier, divider, gate drives, as well as some other analog ingredients into a single IC chip. Thus, the design of the active PFC system becomes relatively easy by calculating and selecting appropriate passive components (resistors, capacitors, etc.) around the IC.

For example, the UC3854 [21] from Texas Instruments is an analog controller specially designed for power factor preregulators. The UC3854 implements all the control functions necessary to build a power supply with power factor correction capacity. It contains a voltage amplifier, an analog multiplier/divider, a current amplifier, and a fixed-frequency PWM. In addition, the UC3854 contains a power MOSFET compatible gate driver, 7.5V reference, line anticipator, load-enable comparator, low-supply detector, and over-current comparator.

Fig. 1.10 illustrates a complete 250 W Preregulator using the UC3854 [22]. It can be seen that this is a one-chip solution. The whole control system only contains one single UC3854 chip and some resistors, capacitors and diodes.

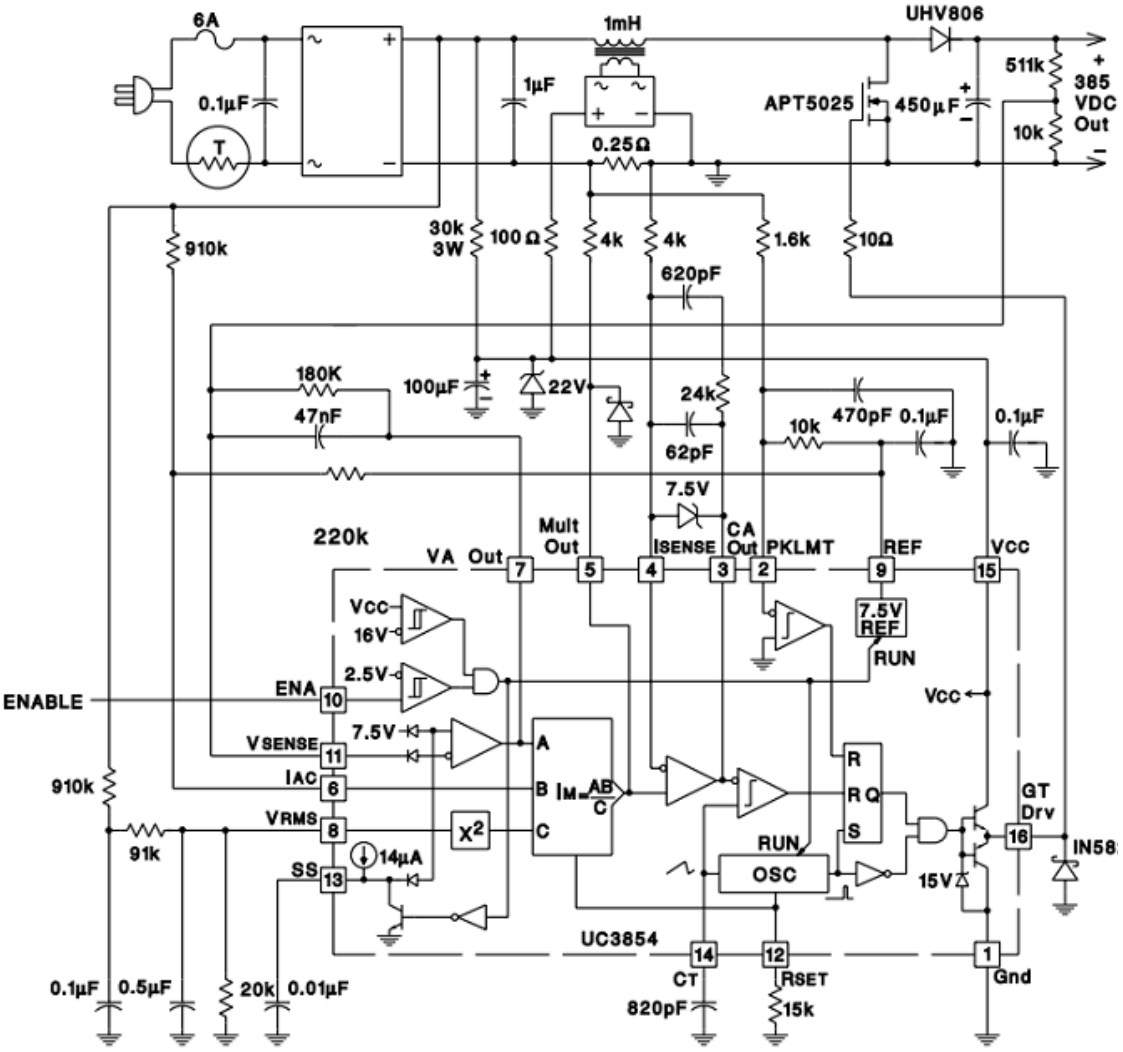


Fig. 1.10 A complete 250 W Preregulator Using UC3854 [22]

The example above clearly demonstrates some advantages of conventional analog PFC system. Those advantages include relatively simple design and low cost. Analog active PFC system also has the advantages of wider bandwidth, finer resolution of time and amplitude. However, analog PFC systems have the disadvantages of susceptibility to noise, aging and drift. Also, analog PFC systems have fixed and relatively simple functionalities.

1.3.2 Digital Implementation of Active PFC

Although active PFC systems have been successfully implemented for many years using analog circuit technology and linear system design techniques with good performance and low cost, digital implementation of active PFC controller is becoming more and more attractive because a digital controller offers several important advantages over an analog controller. It is convenient to implement computational functions in a digital controller. Some of the advanced control methods are solely suitable for the digital controller, such as fuzzy logic control, adaptive control, optimal control, etc. A digital controller is more flexible in design, modification and upgrade. It is less sensitive to noise and environment variations. The digital controller also has some important value-added features, such as system monitoring, self-diagnostics, historical data retrieving, remote communications or display. These features are very useful and suitable for power management, which is attracting more and more attention with the widespread application of portable and handheld electronic devices.

However, a digital implementation also has some disadvantages, such as sampling time delay, computation time delay, limited computation power, control loop bandwidth, and limited resolution due to finite word length of the processor and analog-to-digital (A/D) converter. These disadvantages may result in degradation in performance.

Pure digital implementation of active PFC must obtain the inductor current, line voltage and output voltage by sampling through A/D conversion or estimation through other parameters, and digital active PFC controller faces a critical challenge in dealing with the inductor current.

Fig. 1.11 shows the inductor current waveform in an active PFC power converter

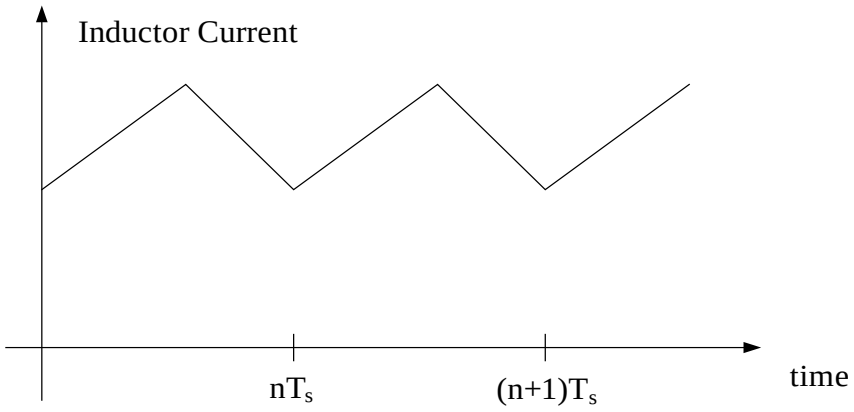


Fig. 1.11 Waveform of the inductor current in active PFC power stage

operating under continuous conduction mode (CCM). The inductor current contains a fundamental frequency equal to the switching frequency, which can easily be in the range of hundreds of kHz. In addition, any change in input voltage or output load reflects at the inductor current instantaneously, so the dynamics of the current loop are fast. Therefore, pure digital implementation of the current loop requires a high speed A/D converter and/or a digital processor with sufficient computational capability to estimate the inductor current and compute the control effort. This may imposes high cost and more complicated hardware.

In this dissertation, digital implementation of active PFC schemes is investigated, and a hybrid control method is proposed. Using this method, two microcontroller-based active PFC systems have been constructed at relatively low cost.

1.4 Efforts on Digital Implementation of Active PFC

In past years, researchers have endeavored to realize digital active PFC. They have investigated various digital platforms using different digital signal processors (DSP) and microcontrollers, and analog active PFC has been transferred into a digital

implementation. They also tried to implement digital PFC system without input voltage sensing.

1.4.1 DSP-Based Power Factor Correction

Digital signal processor (DSP) implementations of all-digital PFC have some limitations. Because of sampling and calculation time, the switching frequency is limited such that the DSP can accomplish computation in one cycle. Higher switching frequency requires faster DSP, and results in higher cost. However, when a DSP has sufficient computational capacity for the fast dynamics of the current loop, a discrete version of the conventional analog design can be directly implemented on a DSP. In addition, various digital control techniques can be used to design the voltage and current loop compensators. By using a DSP, an all-digital implementation for PFC can be achieved. For these reasons, DSP-based digital PFC controllers have been carried out in recent years using commercial DSPs.

For example, in [23], the digital controller, using Analog Devices ADMC-401 DSP Evaluation Board, includes a comb filter (multiples of 120 Hz notch filter) in the voltage control loop, as shown in Fig. 1.12. The comb filter reduces the amount of second harmonic, so the voltage loop bandwidth can be increased, which leads to a faster transient response.

By using the ADMC-401 DSP, the solution presented in [24] utilizes two switching cycles to estimate the average or peak current value, and the estimated current in the second switching cycle is based on the estimation in the first switching cycle.

In [25-26], a DSP-based predictive control scheme for a boost type PFC was presented. As shown in Fig. 1.13, the duty cycles are generated by the predictive

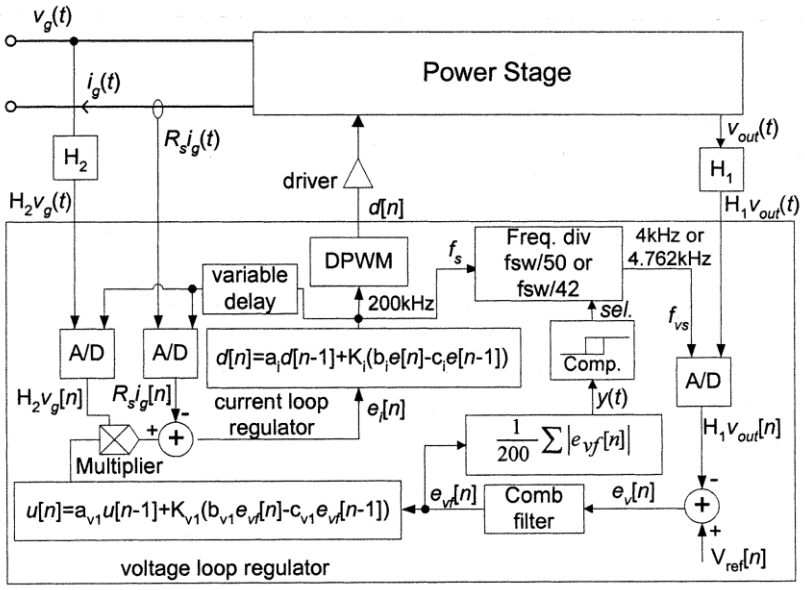


Fig. 1.12 The digital PFC system with the self-tuning comb filter in the voltage loop [23]

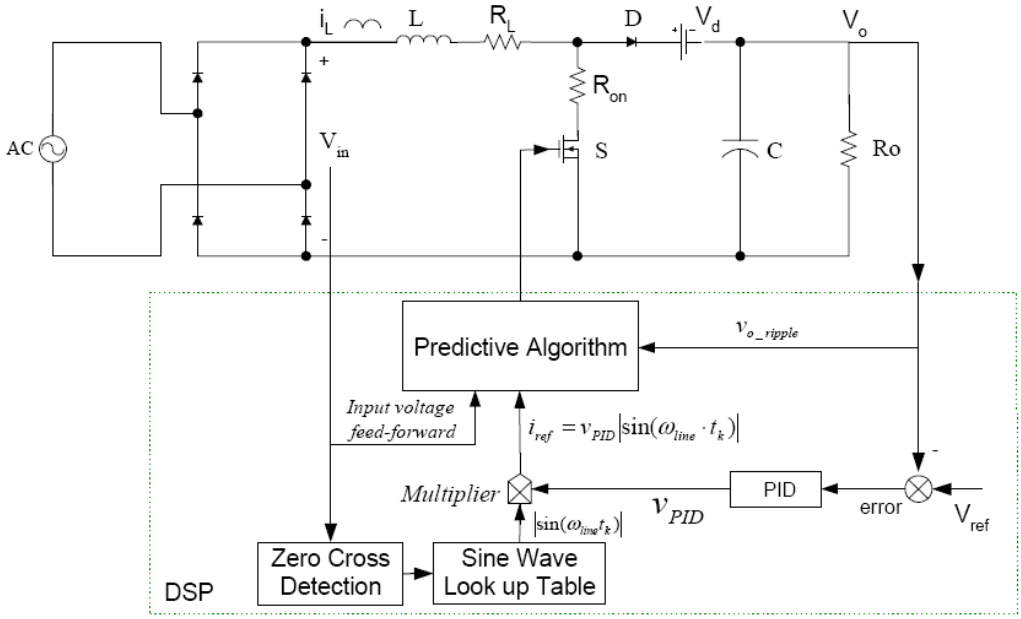


Fig. 1.13 Digital predictive control for a boost PFC [25]

algorithm. The input voltage v_{in} is sensed for peak value and zero crossing signal detection. The peak value of the rectified voltage is used in the predictive algorithm implementation. The reference current, i_{ref}, is from the multiplier. Its amplitude is

determined by the output of the PID controller in the voltage loop, which will finally determine the output voltage of the boost converter. Its phase and sinusoidal waveform are determined by the zero crossing signal and a sine-wave-look-up-table. In this design, the current loop is omitted, since the sensed input voltage can be used to predict the duty cycle.

1.4.2 Microcontroller-Based Power Factor Correction

In order to reduce the cost of digital PFC schemes, some researchers have investigated the use of microcontrollers in the control of PFC systems. Microcontrollers typically do not have an on-board high-speed ADC nor the computational capability to perform current estimation. A few designs have utilized microcontrollers or other low-end digital processors [27-30].

The earliest solution was reported in 1986 [27-28] and utilized a multiplying digital-to-analog converter (DAC). As shown in Fig. 1.14, one input for this DAC was the output from a digital proportional-integral (PI) controller, and the other input was a scaled replica of the rectified input voltage. The output from the DAC was fed to additional control circuitry to implement variable hysteresis current control to produce a sinusoidal input current for the PFC preregulator.

The idea of utilizing a multiplying DAC was also employed in [29]. As shown in Fig. 1.15, the outer voltage loop was realized using an Intel 80C196KB microprocessor, which provided an input to the multiplying DAC to scale a signal proportional to the rectified input voltage. The current loop was implemented with a UC3854 analog control chip, which received a signal from the multiplying DAC.

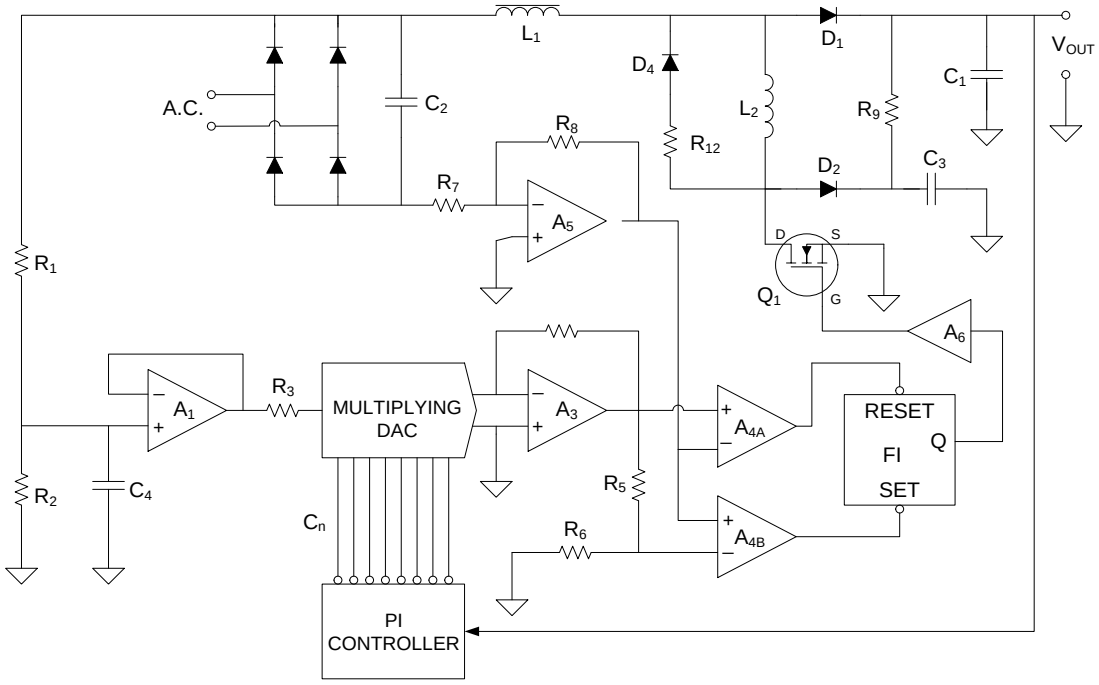


Fig. 1.14 Microcontroller-based predictive control for a boost PFC [28]

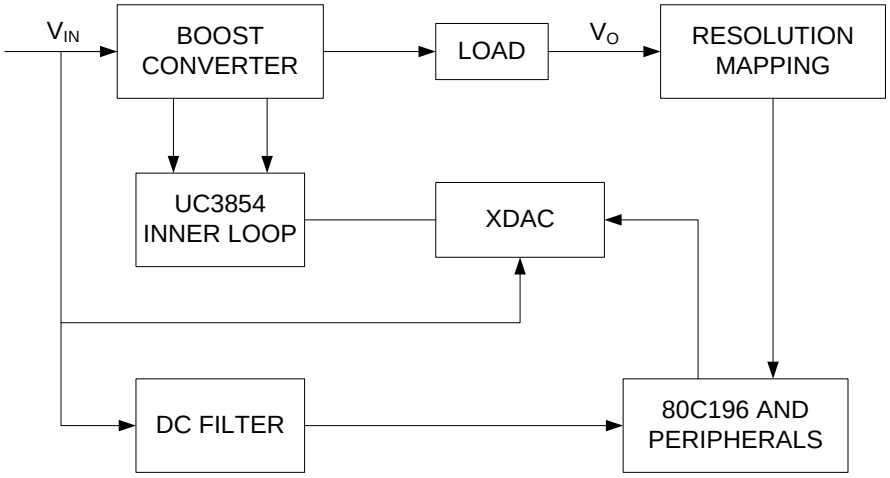


Fig. 1.15 A microcontroller-based PFC scheme using multiplying DAC [29]

Another approach by Jakobsen et al [30] did not utilize a multiplying DAC. Illustrated in Fig. 1.16, the current reference for the average current controller was

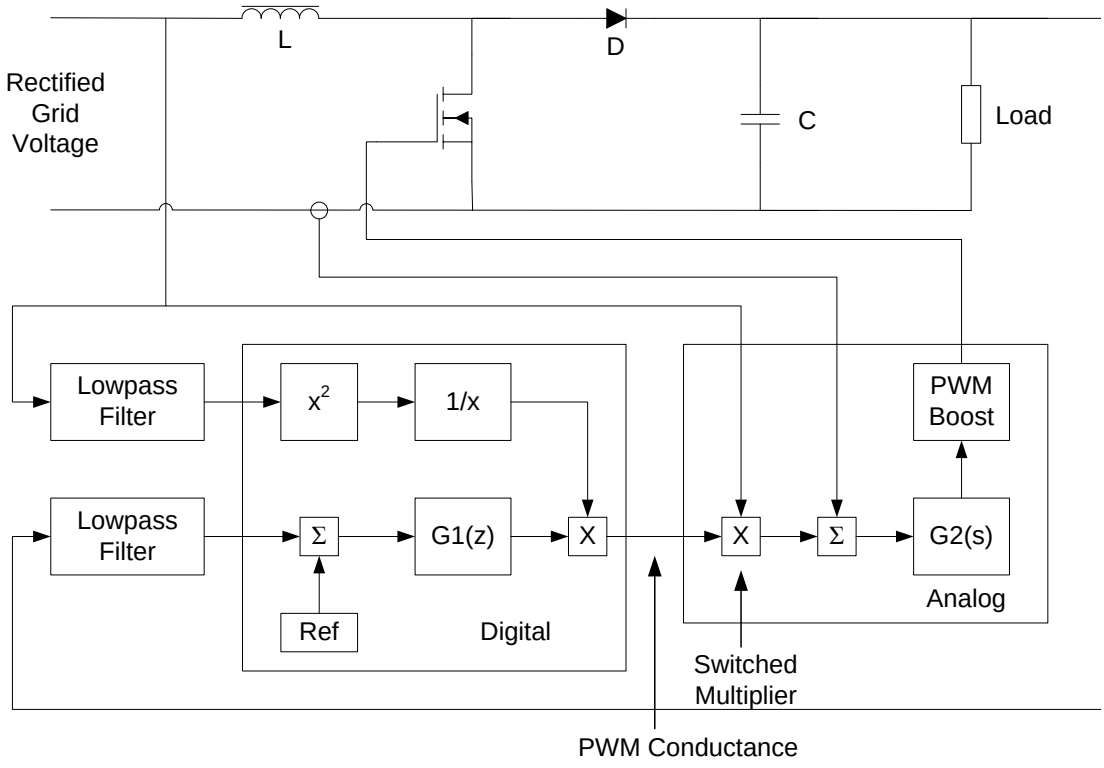


Fig. 1.16 A microcontroller-based PFC scheme using external switched multiplier [30]

generated with an external switched multiplier whose inputs were a scaled replica of the rectified input voltage and a PWM signal from a microcontroller. The duty cycle of this PWM signal is inversely related to the square of the RMS value of the input voltage. The RMS value of the input voltage is determined using an analog second-order low-pass filter. It was necessary for the control algorithm to execute a 16×16 bit multiplication followed by a 24×16 bit division. Because low-end microcontrollers perform multiplications and divisions very slowly, the duty cycles for every combination of input and output voltage were calculated offline and stored in a lookup table in an external EPROM. The PIC16F877A microcontroller fetched the proper duty cycles from the external EPROM during circuit operation.

1.5 Efforts on Power Factor Correction without Input Voltage Sensing

For basic power factor correction (PFC) techniques, the output voltage, input current and input voltage are sensed. The input current is shaped through a current loop which utilizes the sinusoidal input voltage as a reference. An outer voltage loop senses the output voltage and controls the amplitude of the input current. Given the fact that the input current is a function of the input voltage, input current shaping can be achieved by sensing the inductor current, switch current or diode current. As such, the need for input voltage sensing can be eliminated.

In [42-44], a control technique, known as nonlinear-carrier (NLC) control, was introduced to achieve high power factor without input voltage sensing. In the NLC controllers, as shown in Fig. 1.17, the switch duty ratio is determined by comparing a signal derived from the main switch current with a periodic, nonlinear carrier waveform. The shape of the NLC waveform, generated by a NLC generator, is determined so that the resulting input-line current follows the input-line voltage. Using the NLC controller, input voltage sensing, error amplifier in the current loop, and the multiplier/divider circuitry in the voltage loop are eliminated at the expense of overhead of the NLC to shape the current.

Similar control schemes were presented in [45-47]. In [45], as shown in Fig. 1.18, a one-cycle averaging method was used to average the input current by holding the average value of current in one cycle and using it from PWM in the next cycle.

In [46-47], the information related to the input voltage was obtained by sensing the inductor current. As illustrated in Fig. 1.19, a low-pass filter was employed to obtain a signal proportional to the average inductor current. This signal is multiplied by the

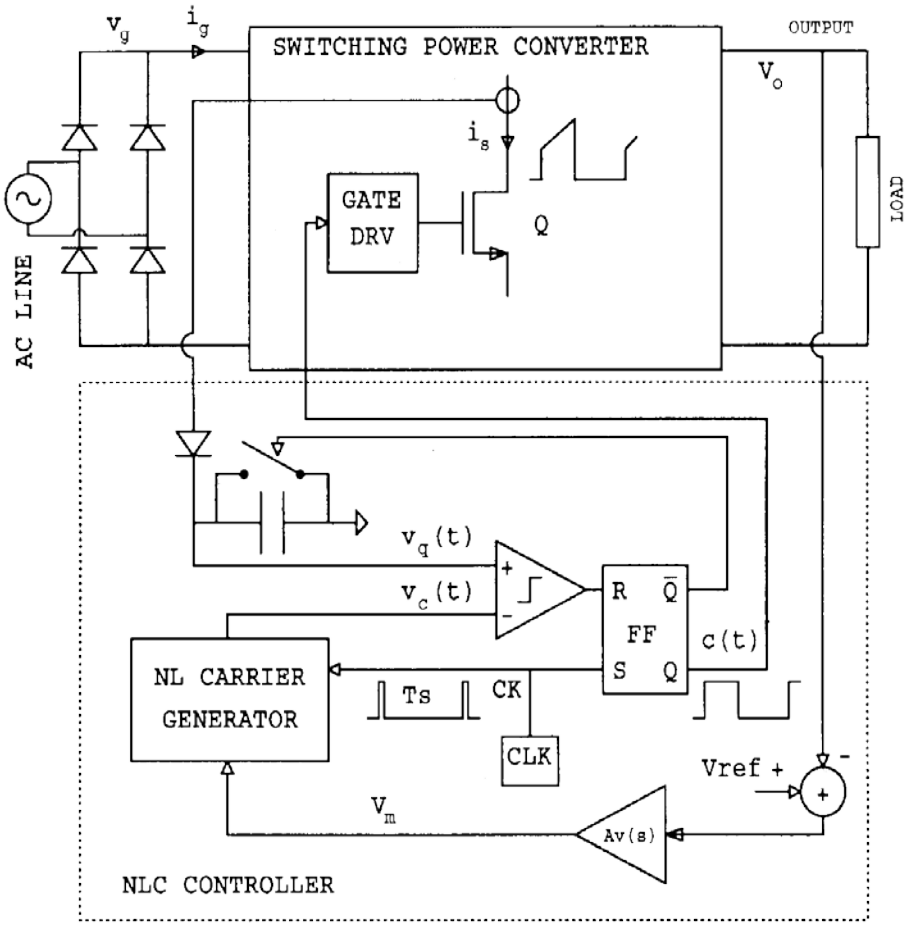


Fig. 1.17 A PFC scheme without input voltage sensing using an NLC controller [44]

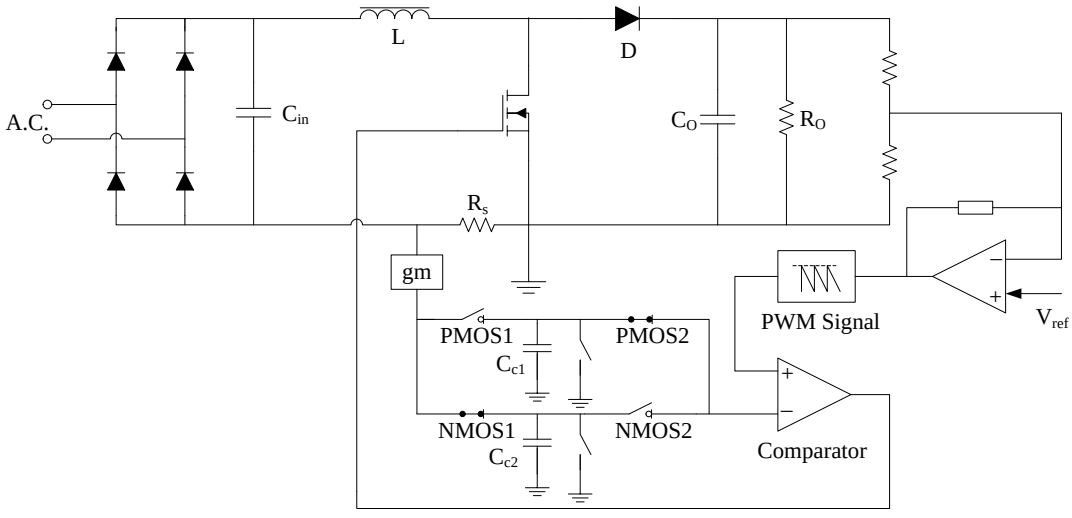


Fig. 1.18 A PFC scheme without input voltage sensing using one-cycle average of input current [45]

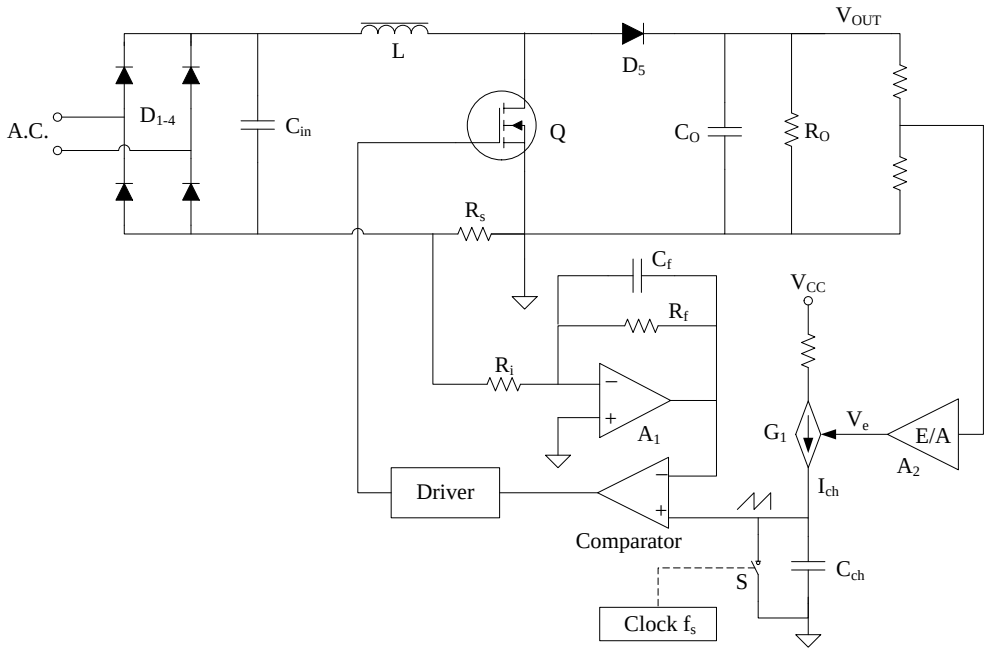


Fig. 1.19 A PFC scheme without input voltage sensing using low-pass filter to average the input current [46]

output voltage error and utilized to control the off-time of the switch in the PFC pre-regulator. Controlling the off-time of the switch to be proportional to the average inductor current yields high power factor. In addition, the multiplier is eliminated by modulating the ramp signal used to control the switch.

Another approach by Barry et al [48] implemented a digital controller without input voltage sensing, as shown in Fig. 1.20. In their scheme, the output voltage and the inductor current were sampled using a Xilinx field programmable gate array (FPGA) digital controller. This controller using the NLC technique [42-44], together with a ΣΔ modulator for control signal dithering, enabled a low-resolution PWM, low-resolution analog-to-digital converter (ADC) and low-clock rate digital PFC controller realization. This approach also eliminates the need for current loop compensation, and is suitable for stand-alone custom-IC implementation.

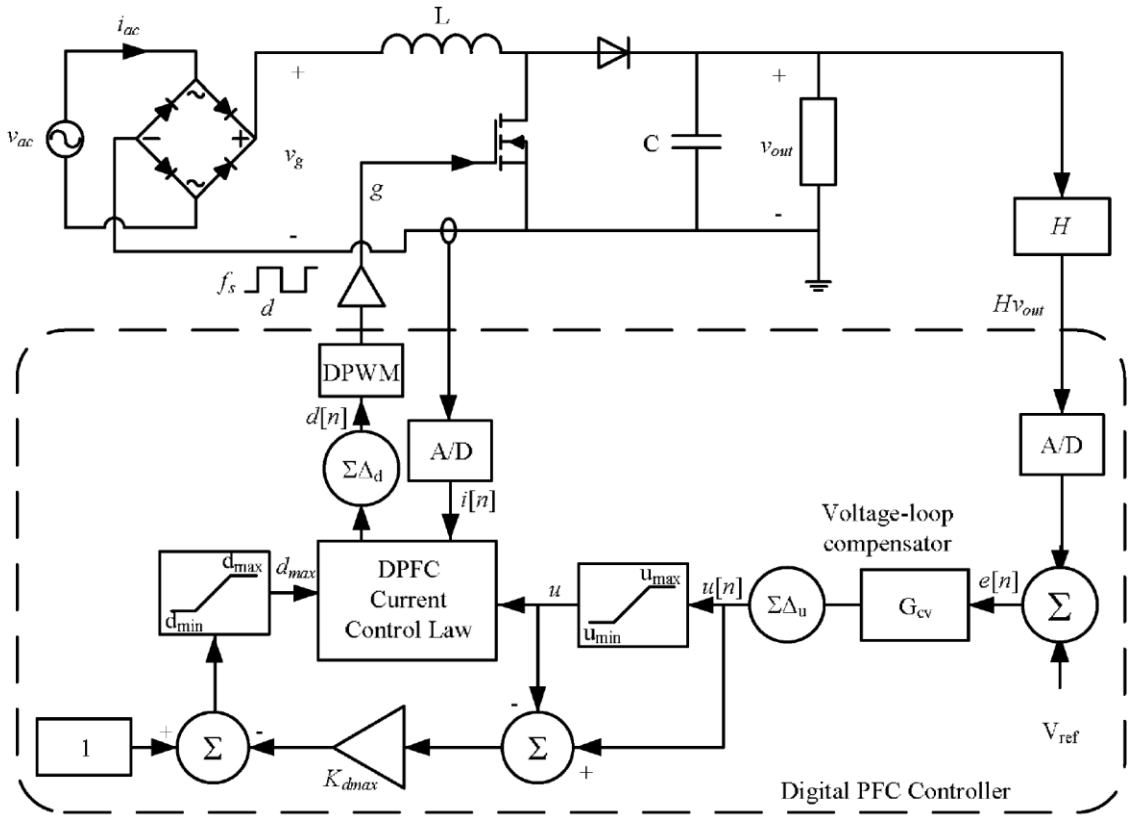


Fig. 1.20 A digital PFC controller with resistive input [48]

1.6 Organization of the Dissertation

This dissertation is organized as follow:

- Chapter 2 introduces the concept of the hybrid control method for active PFC.
- Chapter 3 describes the design of a microcontroller-based active PFC system with input voltage sensing.
- Chapter 4 demonstrates the design of a microcontroller-based active PFC system without input voltage sensing.
- Chapter 5 presents conclusions and suggestions for future work.

CHAPTER 2

HYBRID CONTROL METHOD FOR ACTIVE PFC

In order to implement digital control on active PFC at low cost, a hybrid control method has been proposed. By using a microcontroller with adequate analog peripherals, an active PFC system can constructed at relatively low cost. This hybrid PFC control scheme allows PFC to be implemented on one single microcontroller without sacrificing the performance and reliability.

2.1 Control Systems for Active PFC

The inner current loop programs the input inductor current such that the input current is a half sine wave in phase with the rectified input voltage. Meanwhile, the output voltage and output power of the PFC preregulator shall maintain roughly constants. Therefore, the control system of a PFC preregulator must shape the instantaneous input current directly proportional to the instantaneous line voltage to maintain high power factor, while the rms value of the input current must be inversely proportional to the rms value of the line voltage to maintain constant output power.

As already shown in Fig. 1.7 ~ 1.8, a typical active PFC system has three control loops (output voltage feedback loop, input voltage feedforward loop, and inductor current feedback loop). Typically, an active PFC system uses current-mode control (CMC) technology in its current loop.

2.1.1 Concepts of Average Current-Mode Control

In a CMC system, the inductor current of the converter is directly controlled and the output voltage is controlled indirectly. There are many ways to implement CMC, and peak current-mode control (PCMC) is the earliest and simplest approach [4-5]. In PCMC, the peak inductor current value is monitored and maintained. In contrast, average current-mode control (ACMC) monitors and maintains the average inductor current. ACMC was developed in early 90's [6]. ACMC tracks the average inductor current with a high degree of accuracy, enabling very small harmonic distortion to be achieved with a relatively small inductor.

Advantages of ACMC include large noise margin, excellent noise immunity, no requirement for additional slope compensation, easy current limit implementation, excellent voltage and current regulation, simple compensation, good behavior in both continuous and discontinuous inductor current modes, and has inherent input voltage feed-forward properties. Therefore, ACMC is suitable for applications where a constant current source is needed, since the average current is used as a controlled quantity. The main disadvantage of ACMC is a reduced current loop bandwidth. This is not a problem for PFC application, because the outer voltage loop crossover frequency is significantly lower than the switching frequency. As a result, ACMC is particularly suitable for PFC, where the input current is the controlled quantity. Therefore, ACMC is commonly used in active PFC, and will be used in designing the PFC control systems in this dissertation.

As illustrated in Fig. 2.1, an ACMC system includes a compensator in the inner loop (the current loop) to average and compensate the inductor current. The desired current level, or current reference, is set by the voltage error amplifier in the outer loop

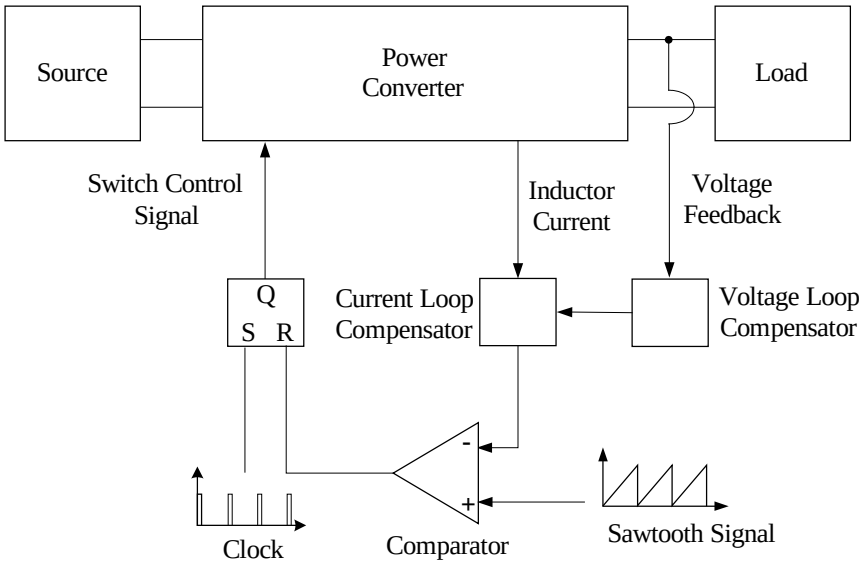


Fig. 2.1 Block diagram of average current-mode control power converter system

(the voltage loop). The current error, or the difference between the averaged current and the current reference, is amplified and compared to a saw-tooth (oscillator ramp) at the comparator inputs, where the PWM control signal is generated.

The current loop compensator in an ACMC power converter acts as a low-pass filter, so it can filter out switching noise while obtaining the average inductor current. ACMC eliminates the need for slope compensation in PCMC, although a ramp signal is needed. This ramp signal is independent of any signal in the power stage and the controller, that is, this ramp signal starts from zero at each switching cycle with a preset (fixed) slope. At the end of each switching cycle, it is driven to zero immediately. Therefore, any current errors in previous switching cycles are washed away, and thus excellent noise immunity is achieved. However, the advantages of ACMC are obtained at the expense of an increased complexity in design and analysis. Compared to PCMC, ACMC has an extra compensator in the current loop. Since this compensator acts like a low-pass filter, the dynamics of the controller are slowed down.

2.1.2 Current Loop Compensator

The current loop compensator is shown in Fig. 2.2, in which i_L is the inductor current, R_i is linear gain of the current-sense network, v_c is the control reference from the voltage loop, d is the duty cycle sent to the boost converter, V_m is the peak-to-peak voltage of the ramp signal, S_n is the sensed inductor current slope when the switch is turned on, and S_n' is the signal slope at the output of the current amplifier (or the input of the comparator).

A switching mode power converter usually has 0 dB loop gain crossover frequency below 1/4 or 1/5 of the switching frequency. But for the PFC preregulator, the crossover frequency is at least decades away from the switching frequency. In a PFC preregulator, large output filter capacitors are usually employed to filter out 120 Hz ripple. For loop stability and waveform distortion considerations, even with line voltage feed-forward, the crossover frequency of the outer voltage loop will be below 120 Hz, and typically is limited to less than 20-30 Hz. Obviously, this frequency is far below switching frequency of the preregulator, and is also considerably lower than that of the

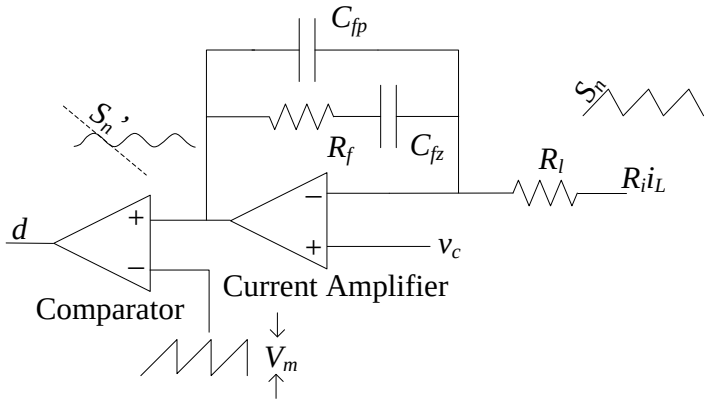


Fig. 2.2 Typical ACMC current loop compensator

inner current loop. When using ACMC technique in the inner current loop, even if the crossover frequency of the inner current loop is below 1 kHz, it is still decades away from that of the outer voltage loop, and the switching frequency ripple and switching noise can be filtered out effectively. In practice, the cutoff frequency of the current loop compensator can be set to a few kHz.

2.1.3 Small Signal Models for Average Current-Mode Control

The control-to-output transfer function with the current loop closed is useful in designing the voltage loop compensator.

Various ACMC models developed in the past years can be used to obtain the control-to-output transfer function $G_{vc}(s)$ [7-15]. In order to obtain a mathematical model for design purposes, a small ripple assumption is typically employed; that is, the ripple is sufficiently small that it can be neglected. However, this assumption may not be valid when the ripple is large, for example, when the power converter is in DCM.

Some ACMC models are based on a small ripple assumption, where the ripple of the output of the current error amplifier is neglected. The model proposed by J. Sun and R.M Bass [7] may be the simplest one. In this model, not only are the feed forward gain of the input voltage and feedback gain of the output voltage neglected, the sampling effect in the current loop is also neglected. Thus, the small signal model of the current loop can be simplified as shown in Fig. 2.3. In this figure, $\hat{v}_g$ is the perturbation of the input voltage of the power stage, $\hat{v}_o$ is the perturbation of the output voltage, $\hat{i}_L$ is the perturbation of the inductor current, $\hat{d}$ is the perturbation of the duty cycle that controls the switch of the power stage, R_i is the effective linear gain (volt/amp) from the inductor

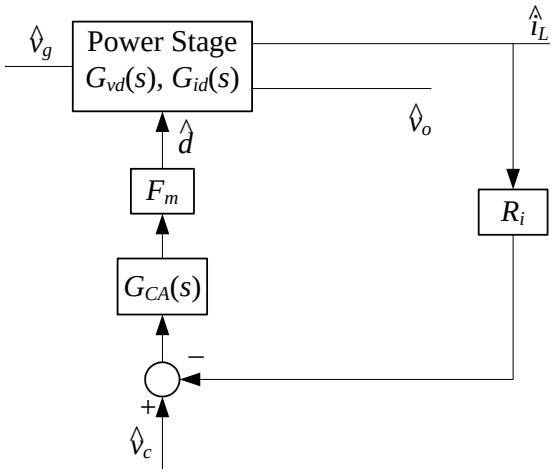


Fig. 2.3 Sun and Bass' small signal model for an ACMC converter [7]

current to the input of the current loop compensator, $G_{vd}(s)$ is the control-to-output transfer function of the power converter, and $G_{id}(s)$ is the control-to-input current transfer function of the power stage. For boost converters, $G_{vd}(s)$ can be found using (1-19), and $G_{id}(s)$ can be found using (1-20).

The modulator gain F_m is the gain introduced by the comparator. F_m is indeed the gain from the output of the current loop compensator to the duty cycle of the gate signal, and it can be computed by:

$$F_m = \frac{1}{V_m}. \tag{2-1}$$

As pointed out in [7], the output of the current loop compensator is directly offset by the control voltage $\hat{v}_c$, so $\hat{d}$ can be expressed as:

$$\hat{d} = F_m\left[\hat{v}_c + G_{CA}(s)\left(\hat{v}_c - R_i\hat{i}_L\right)\right]. \tag{2-2}$$

Therefore, when neglecting the ESR of the output capacitor, $G_{vc}(s)$ can be written as:

$$G_{vc}(s) = \frac{\hat{v}_o}{\hat{v}_c} = \frac{F_m[1 + G_{CA}(s)]G_{vd}(s)}{1 + T_i(s)}, \tag{2-3}$$

where $G_{vd}(s)$ is the transfer function of duty cycle to output voltage for the power stage, $G_{id}(s)$ is the duty cycle to inductor current transfer function of the power, $T_i(s)$ is the current loop gain, and can be expressed as:

$$T_i(s) = R_i F_m G_{CA}(s) G_{id}(s). \tag{2-4}$$

According to (2-3), the equivalent small signal model for Sun and Bass's model can be illustrated as in Fig. 2.4. Although this model is simple, it neglects the feed-forward terms, the sampling effect in the current loop ripple, and the ripple in the output of the current amplifier. When the inductor and capacitor are not large enough, the current ripple in the inductor and voltage ripple at the output may be too large to ignore. In addition, when the gain of the current amplifier is high, the model is inaccurate. All these may lead to an inaccurate design. Therefore, many models have attempted to

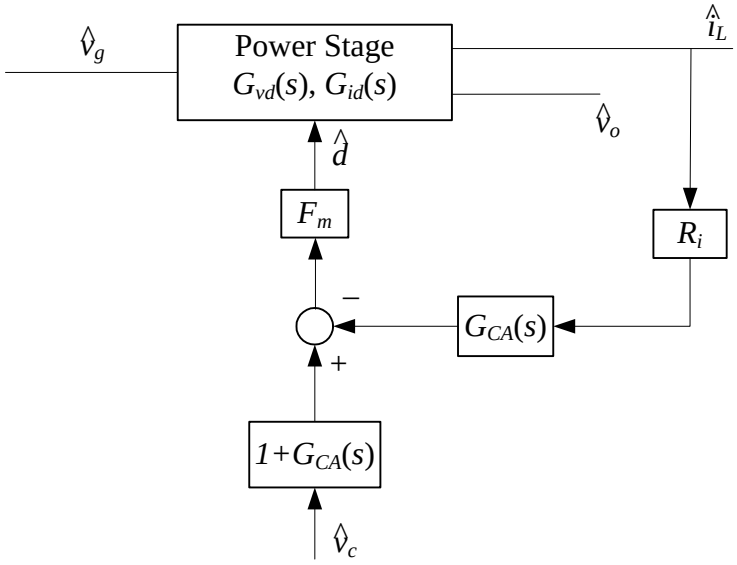


Fig. 2.4 Sun and Bass' equivalent small signal model for an ACMC converter

include the effect of inductor ripple and sampling effect on the dynamics of an ACMC converter [8-16].

T. Suntio, et al. [9-10] expended the previous model by including the dynamic effects of inductor current ripple, and the resulting control-to-output transfer function is:

$$G_{vc}(s) = \frac{\hat{v}_o}{\hat{v}_c} = \frac{F_m[1 + G_{CA}(s)]G_{vd}(s)}{1 + T_i(s) + T_v(s)}, \tag{2-5}$$

where $T_v(s)$ is the voltage loop gain. $T_v(s)$ is computed by:

$$T_v(s) = F_m q_0 G_{vd}(s), \tag{2-6}$$

where q_0 is a coefficient depending on the topology. Comparing (2-5) to (2-3), an extra voltage loop gain $T_v(s)$ is added. The expression of the modulator gain F_m is also different, since one more term is added in the denominator:

$$F_m = \frac{1}{V_m + \dfrac{K_l V_o (D' - D)}{2Lf_s}}, \tag{2-7}$$

where K_l is an coefficient derived from the current loop compensator, and can be expressed as (referring to Fig. 2.2):

$$K_l = \frac{R_f C_{fz}}{R_l (C_{fp} + C_{fz})}. \tag{2-8}$$

For a boost converter, q_0 can be expressed as:

$$q_0 = \frac{K_l DD'}{2Lf_s}. \tag{2-9}$$

Since this model includes the inductor ripple effect, it is more accurate at the expense of more complicated expressions.

In [15-16], another ACMC small-signal model developed by W. Tang et al. is derived utilizing previous results based on Ridley's PCMC model [17-19]. This model is illustrated in Fig. 2.5, K_f is the feed-forward gain, K_r is the feedback gain, and $H_e(s)$ is the sampling gain. $G_s(s)$ and $G_p(s)$ are derived from the current amplifier, and can be computed by (referring to Fig. 2.2):

$$G_{CA}(s) = \frac{K_c\left(1+\frac{s}{\omega_z}\right)}{s\left(1+\frac{s}{\omega_p}\right)} = G_s(s)G_p(s), \tag{2-10}$$

$$G_s(s) = \frac{K_c\left(1+\frac{s}{\omega_z}\right)}{s}, \tag{2-11}$$

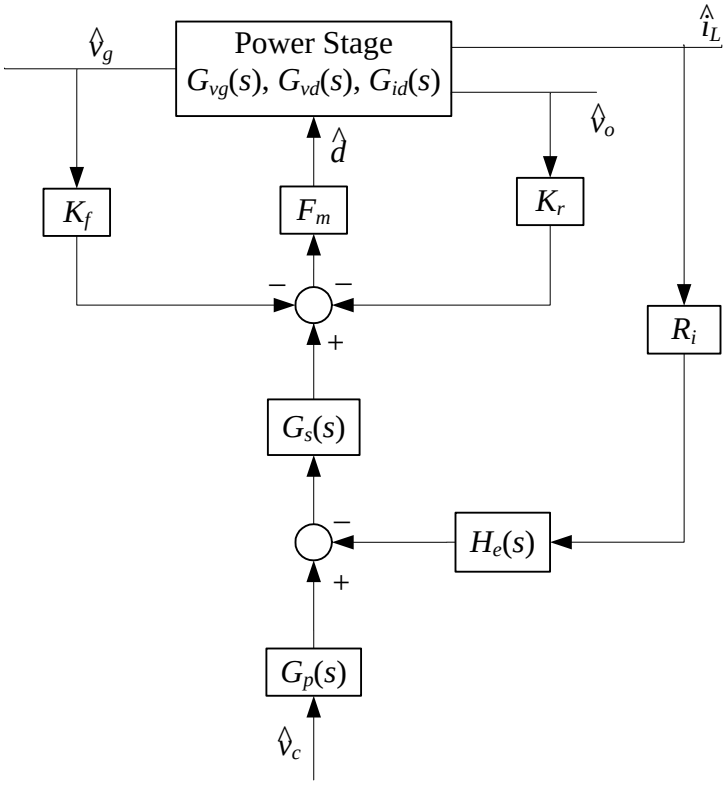


Fig. 2.5 Tang's small-signal model for ACMC converter [15-16]

$$G_p(s) = \frac{1}{\left(1 + \frac{s}{\omega_p}\right)}, \tag{2-12}$$

where K_c, is the gain, ω_p is the pole, and ω_z is the zero of the current loop compensator.

The sampling gain $H_e(s)$ and the modulator gain F_m can be computed by:

$$H_e(s) \cong 1 + \frac{s}{\omega_n Q_z} + \frac{s^2}{\omega_n^2}, \tag{2-13}$$

$$\omega_n = \frac{\pi}{T_s}, \tag{2-14}$$

$$Q_z = -\frac{2}{\pi}, \tag{2-15}$$

$$F_m = \frac{1}{(S_e + S_n^{'})T_s}, \tag{2-16}$$

where S_e is the slope of the external ramp, $S_n^{'}$ is the modified slope of the inductor current waveform, as illustrated in Fig. 2.2. $S_n^{'}$ can be computed by [15-16]:

$$S_n^{'} = K_c S_n \left[DT_s + \left(\frac{1}{\omega_z} - \frac{1}{\omega_p} \right) \left(1 - e^{-\omega_p DT_s} \right) \right]. \tag{2-17}$$

The line voltage feedforward gain K_f and output voltage feedforward gain K_r are different for different types of converters. Table 2.1 lists K_f and K_r for three basic types of converters, where:

$$\xi = \alpha DT_s + \alpha\beta\left(1 - e^{-DT_s/\gamma}\right), \tag{2-18}$$

$$\zeta = \frac{\alpha (DT_s)^2}{2} + \alpha\beta DT_s - \alpha\beta\gamma\left(1 - e^{-DT_s/\gamma}\right), \tag{2-19}$$

Table 2.1 Feedforward gains for ACMC in Tang's Model [15-16]

	Buck	Boost	Buck-Boost
K_f	$\frac{DD'T_s}{2L}\xi + \frac{R_i}{2L}\zeta$	$\frac{D'T_s}{2L}\xi + \frac{R_i}{2L}\zeta$	$-\frac{DD'T_s}{2L}\xi$
K_r	$\frac{D'T_s}{2L}\xi + \frac{R_i}{2L}\zeta$	$-\frac{D'T_s}{2L}\xi$	$-\frac{D'T_s}{2L}\xi$

$$\alpha = \frac{1}{R_f (C_{fp} + C_{fz})}, \tag{2-20}$$

$$\beta = \frac{R_f C_{fz}^2}{(C_{fp} + C_{fz})}, \tag{2-21}$$

$$\gamma = \frac{R_f C_{fp} C_{fz}}{(C_{fp} + C_{fz})}. \tag{2-22}$$

According to Fig. 2.5, the control-to-output transfer function $G_{vc}(s)$ can be expressed as:

$$G_{vc}(s) = \frac{\hat{v}_o}{\hat{v}_c} = \frac{F_m G_{CA}(s) G_{vd}(s)}{1 + R_i F_m H_e(s) G_s(s) G_{id}(s) + \left(K_r + \frac{K_f}{G_{vg}(s)} \right) F_m G_{vd}(s)}. \tag{2-23}$$

This model uses the sampling gain $H_e(s)$ directly from the PCMC model without strict derivation. Therefore, it can be inaccurate if the gain of the current amplifier is high. Also, this model contains a nonlinear expression for the modulator gain, which adds complexity to the model.

Indeed, J. Sun and R.M Bass [7] questioned the inclusion of the sampling term for ACMC. Incorporation of the sampling term shall improve the accuracy of the model at the expense of adding complexity to the model. Although [17] has proven that the

modeling of the sampling effect is valuable to improve the accuracy of PCMC models, but in ACMC, this sampling effect may be neglected. An ACMC system, just like a voltage mode control system, uses an artificial triangular waveform to generate PWM signals. In a voltage-mode controlled PWM converter, its small signal model without incorporating sampling effect has been proven to be accurate up to half of the switching frequency. Therefore, for ACMC systems, especially for PFC ACMC systems, the crossover frequency is decades away from the switching frequency. Therefore, the sampling effect needs not to be considered in an ACMC system.

In order to achieve a more accurate model, P. Cooke [11] extended the model described in [7] by including the feedforward terms. Cooke's model is illustrated in Fig. 2.6. Comparing with Fig. 2.5, it can be seen that the main difference between Tang's model and Cooke's model is the method to include the sampling effect of the current loop

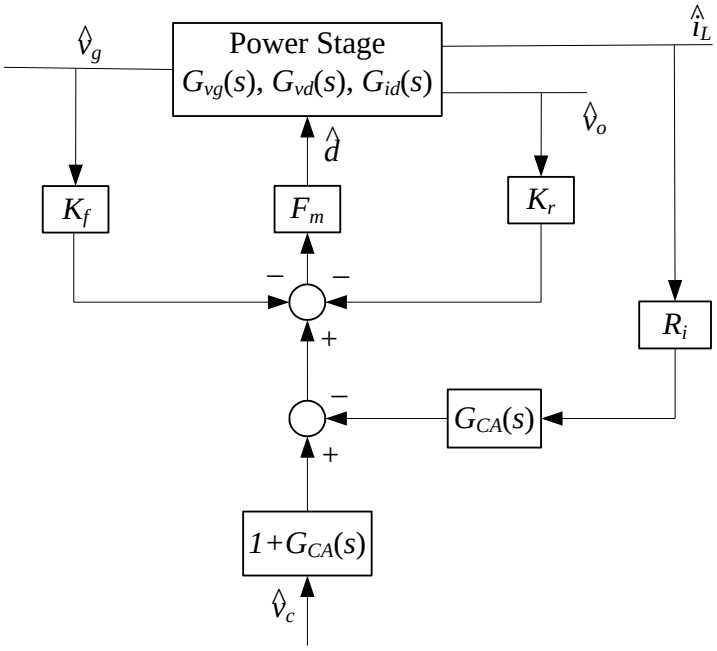


Fig. 2.6 P. Cooke's small-signal model for ACMC converter [11]

due to the sawtooth signal.

In Cooke's model, modular F_m is simplified as:

$$F_m = \frac{1}{V_m}. \tag{2-24}$$

Obviously, (2-24) is identical to Sun's model shown in (2-2). This is because, for ACMC, the peak-to-peak ripple on the output of the current amplifier is small. When this ripple is high, (2-24) is just an approximation, and may not be accurate enough.

P. Cooke's model also uses an approximation to define the expressions for design purposes. The line voltage feedforward gain K_f and output voltage feedforward gain K_r, are simplified in P. Cooke's model, and are listed in Table 2.2 for the three basic types of converters [11].

According to Fig. 2.6, the control-to-output transfer function $G_{vc}(s)$ can be expressed as:

$$G_{vc}(s) = \frac{\hat{v}_o}{\hat{v}_c} = \frac{F_m\left[1 + G_{CA}(s)\right]G_{vd}(s)}{1 + R_i F_m G_{CA}(s) G_{id}(s) + \left(K_r + \dfrac{K_f}{G_{vg}(s)}\right) F_m G_{vd}(s)}. \tag{2-25}$$

In order to compare the models for the ACMC power converters, a dc-dc ACMC boost converter has been constructed. The input voltage of the boost converter is 12 V,

Table 2.2 Feedforward gains for ACMC in P. Cooke's Model [11]

	Buck	Boost	Buck-Boost
K_f	$\dfrac{D^2 T_s R_i}{2L}$	$\dfrac{(2D-1) T_s R_i}{2L}$	$\dfrac{D^2 T_s R_i}{2L}$
K_r	$\dfrac{(1-2D) T_s R_i}{2L}$	$\dfrac{(D')^2 T_s R_i}{2L}$	$-\dfrac{(D')^2 T_s R_i}{2L}$

and the output voltage is 28 V. The boost converter contains a 109.8 µH inductor, total 57.35 µF output capacitor with 150 Ω load, and is operating at 156.25 kHz switching frequency. In the current loop, a 0.1 Ω sensing resistor is used to measure the inductor current. Referring to Fig. 2.2, the parameters of the current loop compensator are C_{fz} = 1500 pF, C_{fp} = 22 pF, R_l = 5.1 kΩ and R_f = 91 kΩ.

The Bode plots of $G_{vc}(s)$ of the four models for the ACMC boost converter used are plotted in Fig. 2.7. The measured transfer function is also plotted for comparison. According to Fig. 2.7, all the four models can provide very accurate predictions at low frequency. However, all of them deviate from the measurement at above half of the switching frequency. It can be seen that J. Sun's model, T. Suntio's model and P.

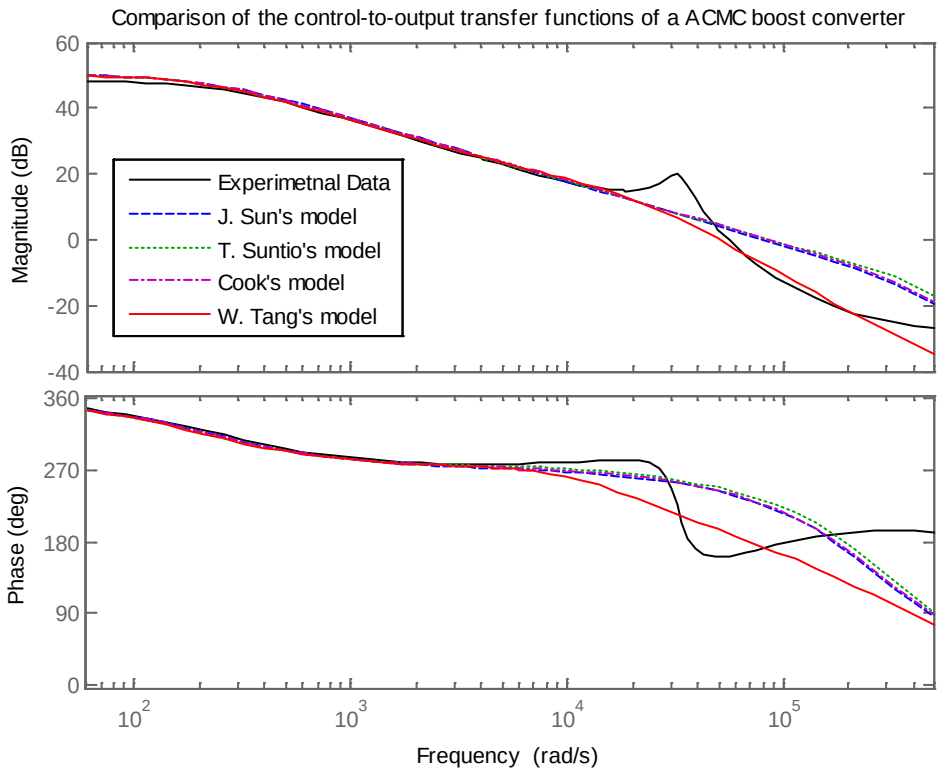


Fig. 2.7 Comparison of the ACMC models

Cooke's model are very similar at high frequency, and W. Tang's model is more accurate at high frequency at the expense of a more complicated expression. Indeed, the main difference between W. Tang's model from other three models is that W. Tang's model includes the sampling effect of the current loop, and thus its modular gain F_m is more accurate. If the modular gains F_m in the three models are replaced by the modular gain F_m in W. Tang's model, all the four models are very similar.

Since the actual $G_{vc}(s)$ has an infinite number of poles, all of the theoretical models are based on some approximations. Therefore, $G_{vc}(s)$ from the experimental measurement is always the first choice when it is possible, as has been implemented in this dissertation.

2.1.4 Outer Voltage Control Loop

The output voltage of a PFC preregulator system is determined by the outer voltage loop. Fig. 2.8 shows the basic voltage control loop when the current loop is closed. The voltage loop compensator should be able to regulate the output voltage to the desired value in spite of variations in the input voltage or the output load.

However, because the rectified line voltage contains a 120 Hz fundamental frequency, varying from zero to the sinusoidal peak, the PFC preregulator has to be able to filter out this variation to reach a steady DC output. This goal may be achieved by using large value capacitors at the output stage. However, the bulk capacitor has to be able to sustain high voltage in addition to the high capacitance value, which increases the size and cost of the bulk capacitors dramatically. When using a boost topology, the DC bus voltage is even higher than the line voltage. As a result, the cost and size of the bulk capacitor is so enormous that this approach is not acceptable in most applications.

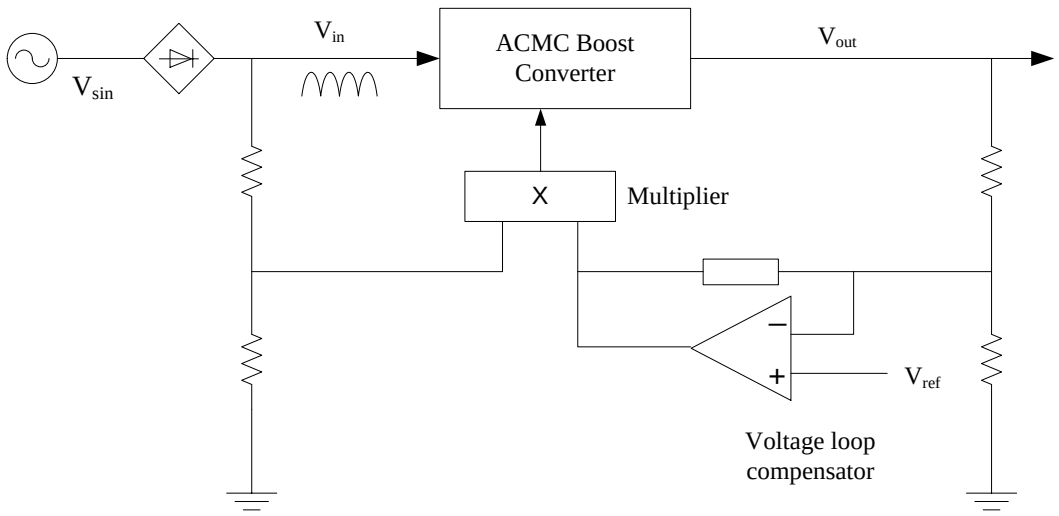


Fig. 2.8 Outer voltage control loop

Another approach to eliminate the 120 Hz ripple at DC output is to limit the bandwidth of the voltage loop of the controller, such that the control voltage will not vary sizably during each line half-cycle, and such that the sine wave distortion at the DC output is decreased to an acceptable level and can be filtered out by smaller bulk capacitor with less value and size. This requires that the control loop bandwidth must be significantly less than 120 Hz.

The selection of the output bulk capacitor has a significant impact on the excursions of the output voltage and the design of the voltage loop compensator. Since the output capacitor needs to filter out the 120 Hz ripple, which is significantly lower than the switching frequency, the switching noise in the output voltage can be filtered out easily, and switching noise is not a concern in PFC implementations.

The instantaneous rectified input voltage $v_{in}(t)$ and input current $i_{in}(t)$ can be expressed as:

$$v_{in}(t) = \sqrt{2}V_{in}\left|\sin(\omega t)\right|, \text{ and} \tag{2-26}$$

$$i_{in}(t) = \sqrt{2} I_{in} \left| \sin(\omega t) \right|, \tag{2-27}$$

where V_{in} is the rms value the of line voltage, I_{in} is the rms value of the input current, and ω is the line frequency, which is 120π rad/s. When the PFC preregulator is properly constructed, the power factor is close to 1, and the output voltage is tightly controlled, therefore, it is reasonable to assume that the output voltage is roughly a constant, and the current passing through the diode is in phase with the line voltage and the inductor current. Fig. 2.9 illustrates the waveforms of the rectified line voltage v_{in}, inductor current i_{in} and the current through diode i_D.

Obviously, the instantaneous input power $p_{in}(t)$ equals to the instantaneous power $p_D(t)$ delivering to the output capacitors through the diode. Therefore,

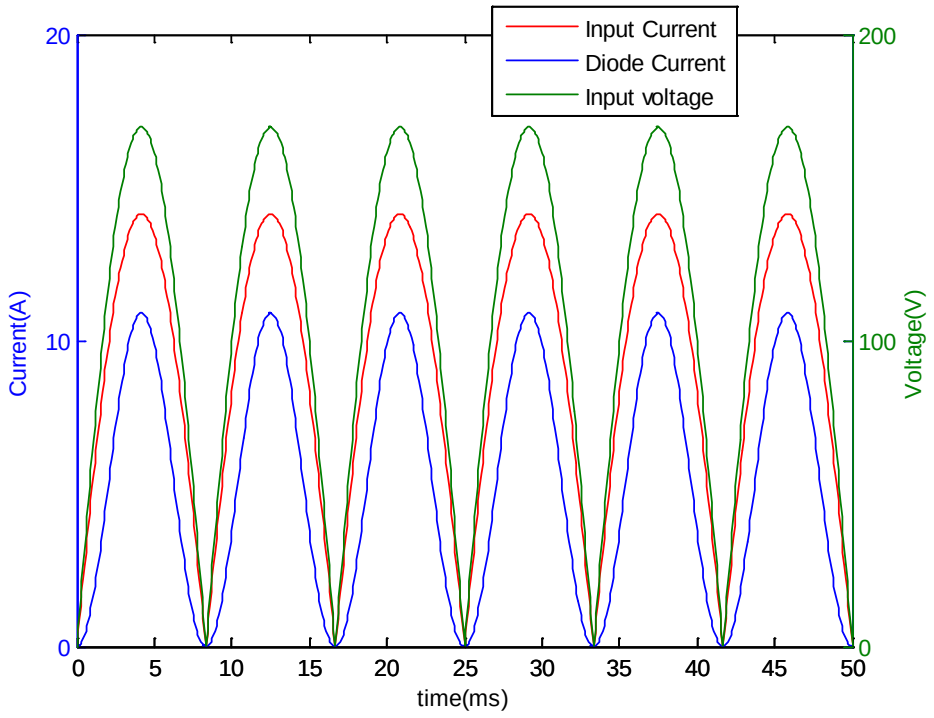


Fig. 2.9 Waveforms of a PFC boost converter

$$p_{in}(t) = v_{in}(t)i_{in}(t) = p_D(t) = V_o i_D(t)\,. \tag{2-28}$$

where V_o is the rms value of the output voltage. Thus:

$$i_D(t) = \frac{v_{in}(t)i_{in}(t)}{V_o} = \frac{2V_{in}I_{in}}{V_o}\sin^2(\omega t) = \frac{V_{in}I_{in}}{V_o}\left[1-\cos(2\omega t)\right], \tag{2-29}$$

$$i_D(t) = \frac{V_{in}I_{in}}{V_o} - \frac{V_{in}I_{in}}{V_o}\cos(2\omega t) = I_D + \Delta i_D(t)\,. \tag{2-30}$$

Equation (2-30) shows that i_D contains a dc component I_D and an ac component $\Delta i_D(t)$. $\Delta i_D(t)$ is the ripple current that flows through the output capacitor and causes the ripple $\Delta v_o(t)$ at the output voltage, which can be calculated by:

$$\Delta v_o(t) = \frac{\Delta i_D(t)}{X_C} = \frac{V_{in}I_{in}}{2\omega C_o V_o}\sin(2\omega t + \pi)\,. \tag{2-31}$$

where C_o is the capacitance of the output capacitors. Thus, the magnitude of the output ripple is:

$$\Delta V_o = \frac{V_{in}I_{in}}{2\omega C_o V_o}\,. \tag{2-32}$$

For a resistive load, (2-32) can be rewritten as:

$$\Delta V_o = \frac{V_o}{2\omega C_o R_L}\,. \tag{2-33}$$

where R_L is the resistance of the load. Equation (2-33) shows that the output voltage ripple is inversely related to output capacitance and load, and adjusting the control loop gain and bandwidth will not have any effect on the output voltage ripple. It provides the practical method to select the output capacitors.

When the output capacitor is selected, the voltage loop compensator shall be designed such that the 120 Hz output voltage ripple is filtered out in the voltage loop. Typically, the bandwidth of the voltage loop shall be between 10 ~ 20 Hz.

The implementation of the voltage loop compensator can be a commonly used PI controller. This controller has the advantages of simple structure and mature design procedures, so it is suitable for the low bandwidth voltage loop compensator.

Fig. 2.10 is the realization of an analog PI controller, and can be expressed as:

$$G_{PI}(s) = K_p + \frac{K_i}{s} = \frac{R_{p2}}{R_{p1}} + \frac{1}{R_i C_i s}. \tag{2-34}$$

where K_p is the proportional gain and K_i is the integral gain. In this realization, it is very easy to adjust both of K_p and K_i accurately by adjusting the three resistors. This PI controller has a pole at origin, and a zero at K_i/K_p.

2.1.5 Input Voltage Feedforward

The control system in Fig. 1.7 has its limitation due to the open-loop correction mechanism for line voltage variations. When the line voltage suffers huge instantaneous change, excessive overshoot or undershoot on the dc output voltage will occur.

For an ACMC boost topology PFC system without input voltage feed-forward, the input current I_L is directly proportional to the output of the voltage loop compensator, V_c. When the input voltage V_{in} is sensed and multiplied by V_c, I_L can be expressed as:

$$I_L = K_I V_{in} V_c, \tag{2-35}$$

where K_I is overall gain of the current loop, including the ratio of the input voltage divider, multiplier gain, sense resistor, and the gain between the voltage loop and the

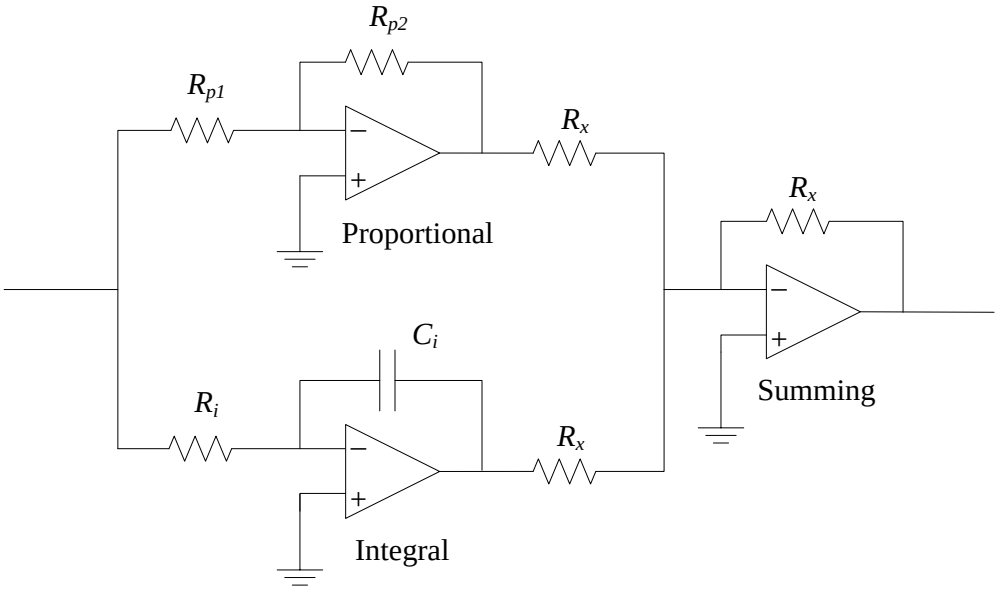


Fig. 2.10 An analog PI controller implementation

current loop (which is set by two resistors).

When the power factor and efficiency are high enough, the output power, P_{out}, approximately equals to the input power, P_{in}. Thus, P_{out} can be computed as:

$$P_{out} = P_{in} = V_{in} I_L = K_I V_{in}^2 V_c \,. \tag{2-36}$$

Equation (2-36) shows that the output power P_{out} varies with V_{in}^2 and V_c proportionally. However, the instantaneous current must be directly proportional to the line voltage to achieve high power factor, while the rms current must be inversely proportional to the rms line voltage. When there is variation in the line voltage and the control loop bandwidth is much lower than 120 Hz, the instantaneous input current will not be able to be adjusted accordingly. For example, when the line voltage experiences over-voltage, the input current may be excessive for several cycles, until the output voltage feedback is sensed and corrected slowly by the controller. This will result in

significant change in input power P_{out} which is proportional to V_{in}^2, and will cause considerable variation at the output voltage V_{out}. Adjusting the controller will not be able to solve this problem, because the control loop has to have limited bandwidth much less than 120 Hz.

An effective approach to resolve this difficult problem is to insert a line voltage feed-forward loop. Fig. 2.11 illustrates the method to implement line voltage feed-forward. In order to eliminate the impact of V_{in}^2 on P_{out} in (2-36), a term Z^2, which is proportional to V_{in}^2, is divided from V_c.

$$Z = K_{ff} V_{in} . \tag{2-37}$$

where K_{ff} is the overall gain of the line voltage feed-forward loop. Thus the V_{in}^2 term can be canceled away, and P_{out} can be expressed as:

$$P_{out} = K_I K_{ff} V_c . \tag{2-38}$$

It can be seen from (2-38) that P_{out} is independent of V_{in}^2 when the feed-forward loop is inserted. Note that Z^2 shall be a constant during each of the half cycle of the line voltage. Otherwise, the ripple in Z^2 would be added to the current loop, and result in distortion in the input current. Therefore, the RC network constructed by R_3, R_4, and C_1 must have a large enough time constant to ensure a high power factor. However, if the time constant is too large, the delay of Z to follow V_{in} will be too long, and will result in excessive overshot or undershoot at output voltage V_{out} when V_{in} changes dramatically.

In Fig. 2.11, the one pole RC network in the line voltage feed-forward loop can have a cut off frequency up to a few Hertz to ensure a constant Z, but the transient

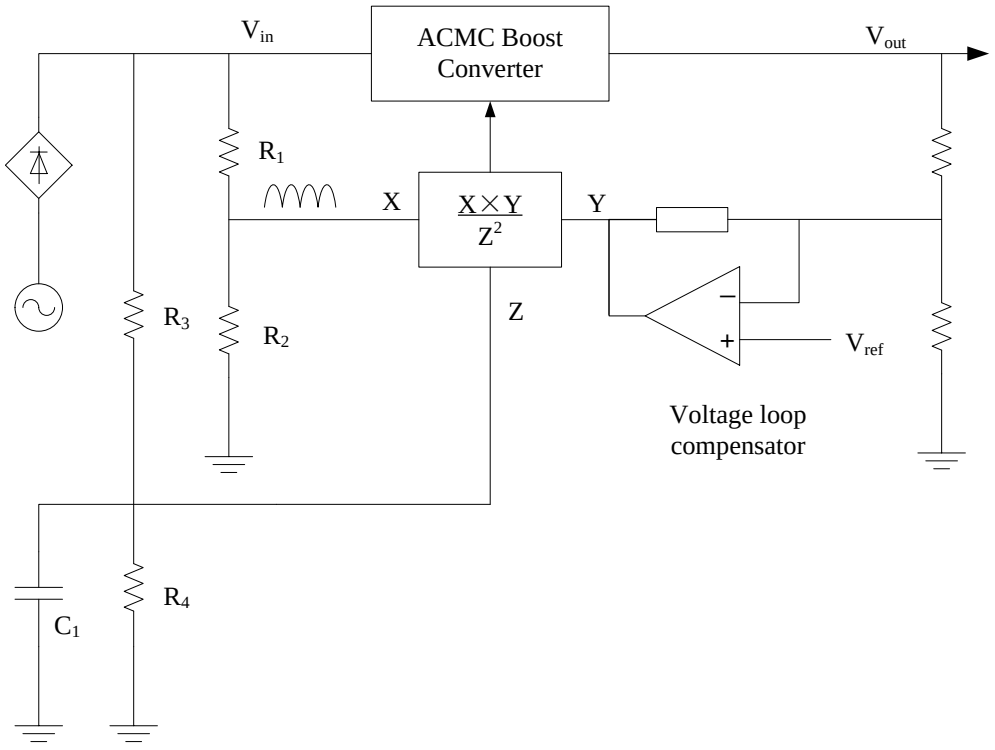


Fig. 2.11 PFC preregulator with line voltage feed-forward

response of the controller may be too slow to reflect the input voltage change. A simple solution is to add an extra pole such that the 2^{nd} and 3^{rd} harmonics are attenuated effectively without too low of a cutoff frequency. Fig. 2.12 illustrates these two line voltage feed-forward solutions. By using this two-pole RC network, the cutoff frequency can be increased to about 20 Hz with a clean feed-forward signal.

With input voltage feed-forward, the controller can respond to a line voltage change within a half cycle, and results in a negligible variation at the dc output and much smaller bulk capacitor in physical size, capacitance value and current rating. The input line voltage feed-forward modifies the current reference of the ACMC regulator to the rectified sinusoidal waveform, and provides the ACMC regulator an inherent open-loop correction mechanism for line voltage variations. Thus, line voltage feed-forward can

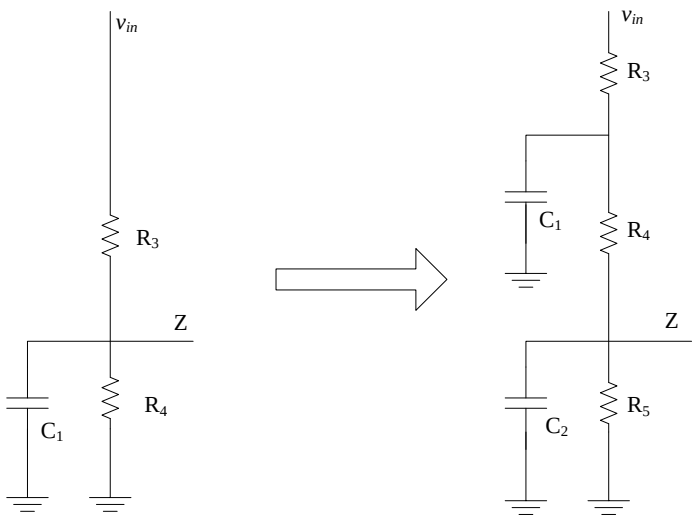


Fig. 2.12 One pole and two pole line voltage feed-forward loops

effectively improve the dynamics of the PFC pre-regulator when line voltage variations have to be considered.

In some applications, the line voltage variation may not be a concern. In this case, line voltage feed-forward loop may be omitted. In this dissertation, line voltage feed-forward is not implemented because of the limitation of the microcontroller used in this research.

2.2 Hybrid Control Method for Active PFC

As depicted in previous chapter, the fast dynamics of the current loop put forward a difficult challenge for digital implementation of the current loop of the active PFC system. Accordingly, analog implementation of the current loop is much easier and more cost-effective than a digital implementation.

In contrast, the dynamics of the voltage feedback loop are much slower than that of the current loop mainly because of the energy storage components (inductors and

capacitors) in the power stage. For example, the resonant frequency ω_0 of the power stage (boost converter) can be expressed as:

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{2-39}$$

where L is the inductor value and C is the capacitor value. Equation (2-39) suggests that the power stage bandwidth can be just a few kilo Hertz.

As for the line voltage feed-forward loop, it needs to filter out the 120 Hz ripple of the rectified line voltage, so the bandwidth is extremely slow. As a result, standard digital compensators can be used in both of the voltage feedback loop and voltage feed-forward loop straightforwardly.

In order to resolve the fast dynamics in the current loop, a hybrid control scheme is proposed. In the hybrid control scheme, the compensator of the voltage loops can be pure digital controllers, and the current loop compensator is an analog controller.

Some microcontrollers have on-board analog features such as operational amplifiers and comparators. By using these analog features, the current loop contains only analog signals. Hence, this "analog" current loop combines with a "digital" voltage loop to construct a hybrid controller. Fig. 2.13 is an example of a microcontroller to control a hybrid active PFC power converter.

Fig. 2.13 indicates that the microcontroller should contain some required peripherals before it is suitable as a hybrid active PFC power converter. An on-board A/D converter is required to convert the output voltage signal into a digital value. Since the output voltage has relatively slow dynamics, the voltage change in adjacent switching cycles is small. Therefore, A/D conversion for the output voltage does not have to be performed on a cycle-by-cycle basis. Instead, the output voltage can be sampled every

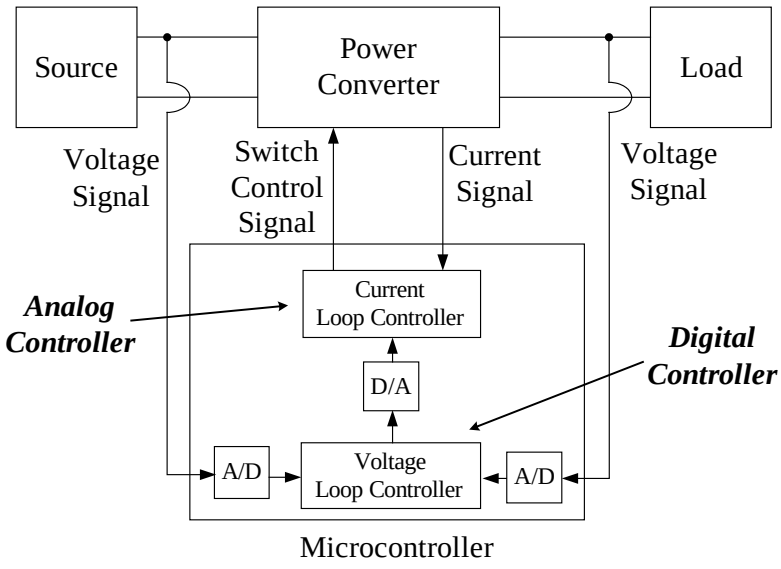


Fig. 2.13 Block diagram of hybrid active PFC system

several switching cycles, as long as the sampling frequency is much higher than the crossover frequency of the power stage. Since the on-board A/D converter will not be used to sample the inductor current, it does not have to be very fast.

In the current loop, an analog comparator is necessary. This comparator is used to generate the gate signal by comparing a ramp signal to the computed control effort. Therefore, an on-board comparator is required for a hybrid PFC system.

The current loop also needs an analog operational to average the current signal. Since the input of the operational amplifier is the output of the voltage loop, a D/A converter is required to convert the digital signal in the voltage loop to an analog signal.

It is desired to have a PWM module inside the microcontroller when the converter operates at a constant switching frequency. An on-board PWM module can make the procedure to generate the gate signal simpler and more reliable. Without a PWM module, a timer must be used as an interrupt source to set the switching frequency. Many microcontrollers do not have priority levels in their interrupt sources. In order to ensure

constant switching frequency, no other interrupt can be allowed, which may increase the difficulty in the software design. In addition, a synchronous ramp signal is also required as the reference to generate the gate signal. Therefore, a mechanism to generate a synchronous ramp signal is required to implement hybrid active PFC system.

The above analysis shows that the microcontroller used in the hybrid active PFC system should have comprehensive analog peripherals. Key peripherals include: an A/D converter, a D/A converter, an analog comparator, an analog operational amplifier, a PWM module, a mechanism to generate ramp signal, and a mechanism to limit the maximum duty cycle.

Although it is easy to find microcontrollers that contain some of the desired peripherals, it is not trivial to select an appropriate microcontroller that contains all the required functionalities. For example, in [30], a single phase PFC system using ACMC technique is controlled by a hybrid controller. This controller has a microcontroller (the PIC16F887A) to control the voltage loop. An external 512 kB EPROM is connected to the PIC16F887A to store a lookup table. In the current loop, an analog IC chip UC3854 is implemented to control the inductor current. In this system, extra external components are added to compensate for the deficiency in computation power of the microcontrollers. This hybrid approach has the disadvantages of a more complicated circuit, less reliability and higher cost than a pure analog controller due to the extra components used in the circuits. Therefore, it is important to select appropriate microcontrollers that contain the required analog peripheral features.

As long as an appropriate microcontroller can be selected, the hybrid CMC method combines the advantages of analog control and digital control. It can handle a

high frequency current signal, while maintaining simplicity and flexibility in design. Because the fast current loop contains only analog signals, performance will not be sacrificed. Advanced digital control techniques can be implemented in the voltage loop compensators. The current loop design is very similar to analog controllers, so design methods and guidelines are fully established. Meanwhile, the analog current loop is not simply an addition to the digital voltage loop. Since the analog signal and components are inside the microcontroller, they are controlled by the microcontroller directly. For this reason, the resulting system still can maintain the valued added features of digital controllers, and have the full potential for power management. Compared to DSP-based systems, this microcontroller-based system has lower cost.

2.3 The PIC16C782 Microcontroller

The PIC16C782 manufactured by Microchip Inc. is an 8-bit microcontroller, and was released in 2001 [31]. The pin diagram of the PIC16C781/782 microcontroller is illustrated in Fig 2.14. The only difference between the PIC16C781 and the PIC16C782 is that the PIC16C781 has 1K × 14 on-board program memory while the PIC16C782 has 2K × 14. The PIC16C782 has a 13-bit program counter capable of addressing an 8K × 14 program memory space. Accessing a location above the physically implemented address causes a wraparound.

The maximum clock frequency for this 20 pin microcontroller is 20 MHz. Its instruction cycle is 4 times a clock cycle, or 200 ns with a 20 MHz clock frequency. It has a RISC (Reduced Instruction Set Computer) CPU core with only 35 single word instructions. Each instruction word has 14 bits. These instructions can be completed in a single instruction cycle, except for program branches which need two instruction cycles.

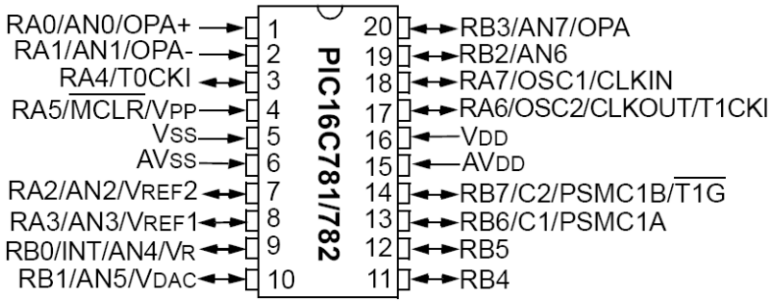


Fig. 2.14 Pin diagram of the PIC16C781/782 [31]

The PIC16C782 has 128 general purpose registers and 39 special function registers. All the registers are 8-bit. The data memory is partitioned into four banks, which contain the General Purpose Registers and the Special Function Registers. Each bank extends up to 128 bytes with some unimplemented bytes. The lower locations of each bank are reserved for the Special Function Registers. Some frequently used Special Function Registers from one bank are mirrored in other banks for code reduction and quicker access. The General Purpose Registers are at the higher locations of each bank, and are implemented as static RAM.

The PIC16C782 has totally 16 I/O pins, 8 of them can be either analog or digital input pins. It has up to 8 internal/external interrupt sources without priority. When an interrupt occurs, it blocks all other interrupt sources.

The PIC16C782 has many peripheral features, and many of these features are critical in a hybrid CMC implementation. Following is a list of important peripheral features included in the PIC16C782:

- Two Timers
  - Timer 0: 8-bit timer/counter with 8-bit prescaler
  - Enhanced Timer 1: 16-bit timer/counter with prescaler

- Analog-to-Digital Converter (ADC): 8-bit resolution; programmable 8-channel input
- Digital-to-Analog Converter (DAC): 8-bit resolution; reference from AVDD, VREF1, or VR module; output configurable to VDAC pin, comparators, and ADC reference
- Analog Operational Amplifier Module (OPA): firmware initiated input offset voltage Auto Calibration module; programmable Gain Bandwidth Product (GBWP)
- Dual Analog Comparator Module (C1 and C2): programmable speed and output polarity; fully configurable inputs and outputs; reference from DAC, or VREF1/VREF2 pins
- Voltage Reference Module (VR): 3.072V +/- 0.7% @25°C, AVDD = 5V; configurable output to ADC reference, DAC reference, and VR pin; 5 mA sink/source
- Programmable Switch Mode Controller Module (PSMC): PWM and PSM modes; programmable switching frequency; slope compensation output available; programmable minimum and maximum duty cycle.

These peripheral features of the PIC16C782 indicate that this microcontroller can be used for a hybrid CMC system. Fig. 2.15 illustrates the connections of the analog peripherals inside the PIC16C782 [31]. These analog components are integrated inside the chip, and can be configured and controlled by the microcontroller through multiplexers and control bits.

However, the PIC16C782 has limited computational ability that imposes

challenges in hardware and software design. When the PIC16C782 was selected to implement hybrid current-mode control, there were some common issues in hardware and software design that had to be taken into account. For example, the PIC16C782 does not have multiplication/division instructions. Instead, it has only 8-bit unsigned addition/ subtraction instructions. Therefore, the software to perform direct multiplication/division calculations can be very complicated and very time-consuming to execute. Therefore, direct multiplication/division is not practical for on-line control of power converters, and must be avoided. One solution is to employ power-of-two arithmetic, where multiplication/division can be done by simply shifting register bits left/right. However, this arithmetic may limit the available gains, and hence may degrade the performance.

The PIC16C782 does not have a sign bit. No negative numbers can exist in the system, and the software must keep track of the sign during calculation procedure, which increases the size and complexity of the code considerably.

Although the PIC16C782 has the ability to address 8 kB program memory, it has a limited internal memory space of 2 kB. External memory can increase the cost and complexity of the circuit considerably. Therefore, the software shall be concise and shall be limited to 2 kB of size.

The ADC module for the PIC16C782 captures a snapshot of the scaled output voltage and holds it for an A/D conversion. Because of the limited sampling rate and computation power of the PIC16C782, switching noise in the output voltage must be avoided or filtered out in “hardware” instead of by a digital filter to ensure on-time control. Therefore, the output voltage should be sampled during the period that has minimum switching noise, and the sampling moment must be controlled precisely. This

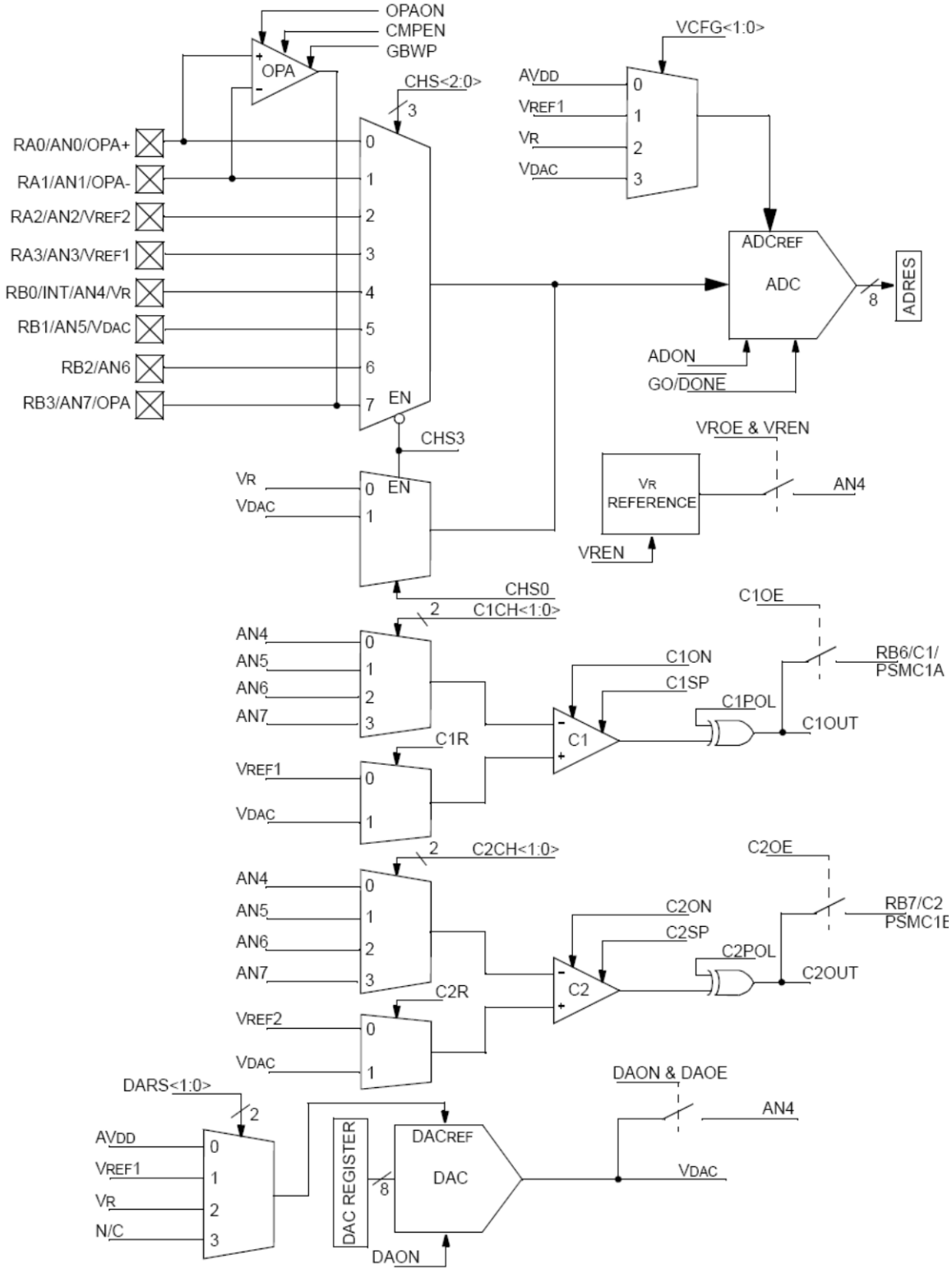


Fig. 2.15 Analog multiplexing diagram of the PIC16C781/782 [31]

can be achieved by sending back the PWM signal to an I/O pin to trigger an interrupt that starts an A/D conversion. As a result, the sampling moment can be controlled, and the output voltage can always be captured at a fixed point in the switching cycle after the switching noise has subsided. However, the PIC16C782 does not have priority levels for interrupts, so any other interrupt can interfere with the correct timing. In order to ensure the proper sampling moment, an interrupt from any other source should not be allowed. When the oscillator frequency is 20 MHz, an A/D conversion cycle requires 15.2 μs, which equals 2.375 switching cycles. Typically, this is much faster than the total calculation time. Therefore, the controller sampling frequency is directly determined by the speed of the calculations instead of A/D conversion speed.

Although the PIC16C782 has limited computational ability, its adequate analog peripheral features can largely overcome its weakness. Therefore, it has been selected to implement various hybrid current-mode control schemes and active PFC system [32-37].

2.4 Digital Controller Design

When using a hybrid CMC method, the voltage loop compensator is indeed a typical digital controller. Therefore, digital control techniques are needed to design the voltage loop. The voltage loop compensator is a standard digital controller, and can be designed in either the *s*-domain or the *z*-domain. When designing the digital controller in the *s*-domain (emulation method), the controller $G_c(s)$ is first designed directly in *s*-domain just as an analog control system. Then $G_c(s)$ is mapped to $G_c(z)$ in the *z*-domain. In contrast, when designing the digital controller in the *z*-domain, the analog plant $G_p(s)$ is mapped to $G_p(z)$ first, then direct digital design techniques are utilized to design a

digital controller $G_c(z)$ directly. In both cases, analog systems (plants or controllers) need to be mapped into digital systems.

There are many existing mapping methods to perform mapping from the *s*-domain to the *z*-domain [38]. These methods can be clarified into three categories: matched pole-zero methods, input hold methods (zero-order-hold and first-order-hold) and numerical approximations. Followings are some of the commonly used methods to perform this transformation, given T as the sampling period:

1. Standard *z*-transform (matched pole-zero method)

The standard *z*-transform method is suitable only for band-limited signals with maximum frequency less than half of the sampling frequency. It can be expressed as:

$$z = e^{sT} \quad \text{or} \quad s = \frac{1}{T}\ln z\,. \tag{2-40}$$

The standard *z*-transform method requires a partial-fraction expression to complete the mapping of

$$\frac{1}{s+a} \rightarrow \frac{1}{1-e^{-aT}z^{-1}}\,. \tag{2-41}$$

In order to simplify the calculation, a simplified matched pole-zero method can be used to perform the mapping:

$$s+a \rightarrow 1-e^{-aT}z^{-1}\,. \tag{2-42}$$

The simplified matched pole-zero method achieves a one to one mapping of poles and zeros. This method produces the same poles as the standard *z*-transform, but the zeros are different. As a result, the simplified matched pole-zero method can be used on

non-band-limited inputs. This method is especially useful to transform an analog controller/filter to an equivalent digital controller/filter.

2. Zero-order-hold (ZOH)

The transfer function of a ZOH can be expressed as:

$$G_{ZOH}(s) = \frac{1 - e^{-sT}}{s}. \tag{2-43}$$

Thus, $G_p(z)$, the mapping of analog system $G_p(s)$ using ZOH method, can be expressed as:

$$G_p(z) = \mathcal{Z}\left[G_p(s) \frac{1 - e^{-sT}}{s} \right] = \frac{z-1}{z} \mathcal{Z}\left[\frac{G_p(s)}{s} \right], \tag{2-44}$$

where $\mathcal{Z}$ represents the standard z-transform. $G_p(z)$ is known as a pulse transfer function. The ZOH method is commonly used to transform an analog plant to its digital representation to design its digital controller in the z-domain.

3. Numerical approximations.

By using difference equations to approximate integral and differential equations, numerical approximation methods can be used to transform designed analog controllers or filters to digital ones. The forward rule, backward rule and trapezoidal rule are several of the most commonly used numerical approximation methods:

- Forward rule. The forward rule can be expressed as:

$$s = \frac{z-1}{T}. \tag{2-45}$$

The forward rule maps the left half-plane in the s- plane to the region of left side

of $z = 1$ in the *z*-plane, so some stable analog designs may be unstable when they are mapped to the *z*-plane.

- Backward rule. The backward rule can be expressed as:

$$s = \frac{(z-1)}{zT}. \tag{2-46}$$

The backward rule maps the left half-plane in the *s*-plane to a circle inside the unit circle in the *z*-plane. Therefore, stable analog designs always yield stable digital designs. Indeed, even some unstable analog designs result in stable digital designs.

- Trapezoidal (Tustin/Bilinear) rule. The trapezoidal rule can be expressed as:

$$s = \frac{2}{T}\frac{(z-1)}{(z+1)}. \tag{2-47}$$

This rule maps the left half-plane in the *s*-plane to the region inside the unit circle in the *z*-plane, and the imaginary axis is mapped to the unit circle.

When the sampling frequency is high enough, all of the above methods can deliver similar mapping results.

Traditional analog control systems are designed in the *s*-domain, and there are many familiar and mature design methods. The emulation method is useful to transform existing analog designs into digital ones. Some designers prefer the emulation method because they are familiar with *s*-domain techniques. When A/D conversion speed and controller calculation are small compared to the sampling period, one may neglect the sampling effect and design the controller in the *s*-domain, and then transform the design into the digital domain using some of the mapping methods described above, i.e.,

matched pole-zero method and numerical approximation. The emulation method ignores A/D conversion delay and controller time delay. Therefore, the emulation method is an approximate approach to design digital controllers,

Notice that the A/D conversion delay and controller time delay are different from the actual sampling period. The A/D conversion delay is the time required for an A/D converter to perform an A/D conversion. Controller time delay is derived from the time required to compute the control effort. In many low-speed systems, the actual sampling period may be much longer than the A/D converter sampling and controller time delay, so the time delay due to the A/D conversion and computation can be ignored. Sampling and computation delay introduce additional phase shift. When the sampling period is close to the A/D conversion delay or controller time delay, this phase shift may not be negligible any more. At this time, the phase margin is reduced, and the system may show more overshoot, or even be unstable. Therefore, more phase margin is desired when designing a digital controller using the emulation method.

Indeed, it is more desirable to design digital controllers directly in the *z*-domain. When using this method, the analog system transfer function $G_p(s)$ is transformed to the *z*-domain first. A ZOH is commonly used method to perform the mapping, and the mapping can be expressed as (2-6). Note that (2-6) ignores the time delay due to A/D conversion and computation.

However, in power converter applications, in order to achieve fast response, it is desired to update the control effort as soon as possible, ideally on a cycle-by-cycle basis. Since the switching frequency can easily be in the hundreds of kilo Hertz, the sampling frequency must be at least several kilo Hertz. In this case, the A/D conversion time delay

or controller time delay usually directly determines the possible maximum sampling frequency, and the overall time delay should be the maximum of the A/D conversion delay and controller time delay. Typically, the controller time delay is much longer than the A/D conversion time. This time delay should be considered when mapping $G_p(s)$ to the z-domain, and can be expressed as e^{-sT_d} in the s-plane, where T_d is the controller time delay. In this case, the sampling period equals the overall time delay, plus a short slice of waiting time to start the next sampling for a fixed sampling frequency. When using the ZOH method, $G_p(z)$, the mapping of $G_p(s)$, can be expressed as:

$$G_p(z) = \mathcal{Z}\left[G_p(s)\frac{1-e^{-sT}}{s}e^{-sT_d} \right]. \tag{2-48}$$

When the time slice is short enough to be ignored, the time delay T_d approximately equals the sampling period T. Thus, (2-10) is converted to:

$$G_p(z) = \mathcal{Z}\left[G_p(s)\frac{1-e^{-sT}}{s}e^{-sT} \right] = \frac{z-1}{z^2}\mathcal{Z}\left[\frac{G_p(s)}{s} \right]. \tag{2-49}$$

Once $G_p(z)$ is obtained, it can be used to design the digital controller $G_c(z)$ using design techniques like z-domain root locus. Some existing s-domain techniques, such as Bode plot and Routh-Hurwitz criterion, cannot be used in the z-domain directly. In order to use those techniques, $G_p(z)$ needs to be transformed to $G_p(w)$:

$$G_p(w) = \mathcal{W}\{G_p(z)\} = G_p(z)\Big|_{z=\frac{1+(T/2)w}{1-(T/2)w}}. \tag{2-50}$$

Equation (2-50) indicates a bilinear transformation, which maps the region inside the unit circle in the z-plane to the left half-plane in the w-plane. In the w-plane, those

familiar techniques can be used to design the digital controller $G_c(w)$. After $G_c(w)$ is designed, it needs to be transformed back to the z-plane:

$$G_c(z) = \mathcal{Z}\{G_c(w)\} = G_c(w)\Big|_{w=\frac{2}{T}\frac{z-1}{z+1}}. \tag{2-51}$$

MATLAB is a powerful tool to perform various transformations. In addition, MATLAB can be used to design digital controllers directly and conveniently. For example, the SISO Design Tool, which is opened by command *sisotool*( ), can be used for this purpose [39]. Its graphical user interface allows a user to design single-input/single-output (SISO) compensators by putting zeros and poles visually and freely in the root locus or Bode and Nichols plots of the open-loop system, and getting the controller directly.

In Chapter 3 and Chapter 4, a method which combines the direct digital design method and the emulation method is proposed to design the digital controllers. In this method, the analog plant $G_p(s)$ is transformed to $G_p(z)$ just as in the direct digital design method. In this procedure, the effects of time delay and ZOH are included. Instead of designing the controller in the z-plane or the w-plane, the controller is designed in the s-domain. In MATLAB, command *bode*( ) plots the Bode diagram of a model. When the model is a discrete-time transfer function, *bode*( ) maps the model into the s-plane using $z=e^{j\omega T}$. This procedure is equivalent to map $G_p(z)$ back to the s-plane, with the effects of time delay and ZOH. Based on the Bode diagram, the controller $G_c(s)$ can be designed. Then, using a numerical approximation, $G_c(s)$ is converted to $G_c(z)$. This method has the advantage of the emulation method that some existing design techniques like a Bode diagram can be used directly without mapping to the w-plane. Meanwhile, the proposed

method considers the effects of time delay and ZOH, and thus can result in a more accurate design.

When $G_c(z)$ is obtained, it needs to be transformed to difference equations to realize the control law. There are unlimited ways to realize the control law. $G_c(z)$ is essentially a digital filter, and can be represented by simulation diagram. Many digital filter structures can be used to construct the simulation diagram [38]. The third direct structure (3D) is one of the commonly used methods. When using this method, $G_c(z)$ can be written as:

$$G_c(z) = \frac{V_c(z)}{E(z)} = \frac{\sum_{i=0}^{n} a_i z^{-i}}{\sum_{i=0}^{n} b_i z^{-i}}. \tag{2-52}$$

where $V_c(z)$ is the controller output, and $E(z)$ is the controller input. Therefore,

$$V_c(z) = \sum_{i=0}^{n} a_i z^{-i} E(z) - \sum_{i=1}^{n} b_i z^{-i} V_c(z). \tag{2-53}$$

In time domain, (2-53) can be expressed as:

$$v_c(k) = \sum_{i=0}^{n} a_i e(k-i) - \sum_{i=1}^{n} b_i v_c(k-i). \tag{2-54}$$

Another commonly used method is to transform analog systems into discrete state-space representations, and then use pole placement or other techniques to design the digital controller. There are two approaches to perform the transformation to the discrete state space model. In the first approach, the discrete state-space model is obtained from z-domain transfer function $G_p(z)$. At first, a simulation diagram for $G_p(z)$ is obtained based on the selected digital filter structure. Then, the state-space model can be derived

from the simulation diagram. Some typical state space representations can be directly written out based on $G_p(z)$ without the assistance of a simulation diagram. For example, if $G_p(z)$ can be expressed as:

$$G_p(z) = \frac{b_{n-1}z^{n-1} + ... + b_1 z + b_0}{z^n + a_{n-1}z^{n-1} + ... + a_1 z + a_0}, \tag{2-55}$$

then its controllable canonical form can be expressed as:

$$\begin{bmatrix} x_1(k+1) \\ x_2(k+1) \\ \vdots \\ x_{n-1}(k+1) \\ x_n(k+1) \end{bmatrix} = \begin{bmatrix} 0 & 1 & \cdots & 0 & 0 \\ 0 & 0 & \cdots & 0 & 0 \\ \vdots & & \ddots & \vdots & \\ 0 & 0 & \cdots & 0 & 1 \\ -a_0 & -a_1 & \cdots & -a_{n-2} & -a_{n-1} \end{bmatrix} \begin{bmatrix} x_1(k) \\ x_2(k) \\ \vdots \\ x_{n-1}(k) \\ x_n(k) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ \vdots \\ 0 \\ 1 \end{bmatrix} u(k)$$

$$y(k) = \begin{bmatrix} -b_0 & -b_1 & \cdots & -b_{n-2} & -b_{n-1} \end{bmatrix} \begin{bmatrix} x_1(k) \\ x_2(k) \\ \vdots \\ x_{n-1}(k) \\ x_n(k) \end{bmatrix} \tag{2-56}$$

Another approach to obtain a discrete state-space model is to compute it from the continuous state-space model. If the continuous state space model is expressed as:

$$\begin{aligned} X(t) &= AX(t) + BU(t) \\ Y(t) &= CX(t) \end{aligned}, \tag{2-57}$$

then the discrete model can be expressed as:

$$\begin{aligned} X(k+1) &= A_d X(k) + B_d U(k) \\ Y(k) &= C_d X(k) \end{aligned} \tag{2-58}$$

where :

$$
\begin{aligned}
A_d &= \Phi(T) = \mathcal{L}^{-1}\left[(sI - A)^{-1}\right]_{t=T} \\
B_d &= \left[\int_0^T \Phi(T-\tau)d\tau\right]B \\
C_d &= C
\end{aligned}
\tag{2-59}
$$

The transformation also can be easily realized using MATLAB. As long as a discrete state-space model is obtained, the digital controller can be designed directly based on the model. Pole placement is one of the commonly used methods to design the controllers. Desired poles are mapped from the *s*-plane to the *z*-plane using $z=e^{sT}$, and then the feedback gain matrix K is selected to ensure that the eigenvalues of $[A_d - B_dK]$ equal the desired poles. Observers are usually needed to estimate the states.

The state-space control method, also known as the modern control method, has become a very powerful approach to analyze and design control systems. However, the state-space control method usually requires a more accurate system model. In addition, this method usually involves many floating point calculations and its feedback gains need to be accurate. Therefore, the state-space control method may be difficult to apply to ill-defined systems. For nonlinear power converter systems, their transfer functions are approximations. Even worse, their transfer functions may change with operating conditions. Microcontrollers usually have limited resolution and computation capacity. Therefore, when using microcontrollers to control power converter systems, state space control method may not be able to compute an accurate control effort fast enough to ensure proper operation of the power stage. Therefore, the state-space control method is not used in this dissertation. Though, it is still useful to analyze the systems off-line.

CHAPTER 3

MICROCONTROLLER-BASED ACTIVE PFC WITH INPUT VOLTAGE SENSING

A single-phase PFC preregulator controlled by a single microcontroller with input voltage sensing is described in this chapter. By using the on-board peripherals of the PIC16C782 microcontroller, no complex algorithm or external multiplier was required to perform the PFC function correctly, and thus a one-chip solution has been achieved. Experimental results indicate that the hybrid PFC preregulator can operate satisfactorily over a wide range of input voltages and output loads.

3.1 System Overview

A basic analog active PFC system was illustrated in Fig. 1.7. This system contains two control loops: inner current loop and outer voltage loop with input voltage sensing. A microcontroller-based active PFC system with input voltage sensing employs a similar system structure, which also contains two control loops with input voltage sensing, and is implemented in a single microcontroller by using a hybrid control technique.

Using the hybrid control scheme, one-chip solutions for hybrid ACMC power converters was achieved at low cost [33-35, 40]. Employing a similar hybrid approach, a

hybrid PFC boost preregulator using a single PIC16C782 microcontroller has been implemented. By using these analog features properly, the hybrid PFC preregulator system, as shown in Fig. 3.1, can be realized with a single microcontroller chip without the use of external circuits such as a UC3854 analog control chip or an external EPROM.

In the hybrid control scheme in Fig. 3.1, the analog current loop is combined with the digital voltage loop to construct a hybrid controller. The dynamics of the voltage loop are much slower than the current loop, so a pure digital compensator can be utilized in the voltage loop. The analog current loop controls the average inductor current. The current reference for this loop is obtained by multiplying the control voltage from the digital voltage loop and a scaled replica of the rectified input voltage; thus, the input current is shaped to a sinusoidal waveform. Variations in the input voltage and output load can be quickly reflected in the inductor current, so the power converter can

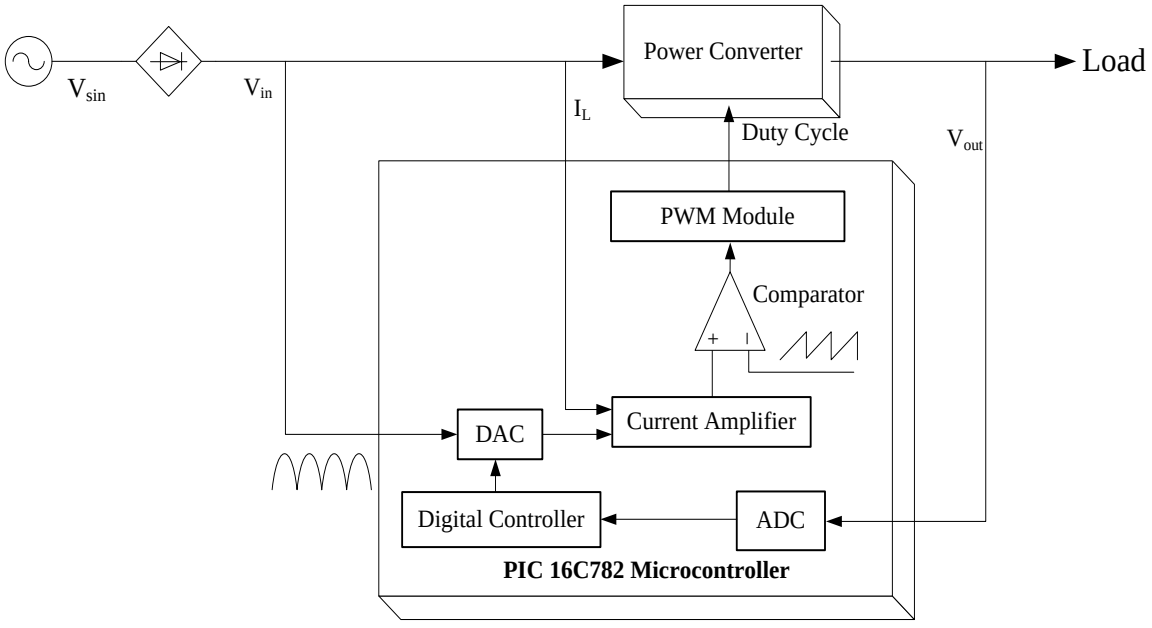


Fig. 3.1 Block diagram of a hybrid PFC preregulator controlled by a PIC16C782 microcontroller

operate satisfactorily over a wide range of input voltages and output loads as has been verified by experimental results.

Because of the on-board analog peripherals on the PIC16C782, no complex algorithm, external multiplier, or external EPROM was required to perform the PFC function correctly. Only two external op-amps were required to condition the output voltage before it was sampled by the on-board ADC. The PIC16C782 has only unsigned 8-bit integer addition/subtraction instructions. Therefore, no negative or fractional numbers can exist in the system. Direct multiplication/division calculations are too time-consuming to be practical for control. Also, it is desired that all arithmetic calculations and results should be in the range of 0 and 255. Since it has a limited internal memory space of 2 kB, the program must be concise.

The on-board ADC sampled the scaled output voltage to calculate the error signal utilized in the digital voltage loop. In order to get higher ADC resolution, a level-shift circuit was designed such that the 8-bit ADC result represented a “windowed” range of the output voltage around its nominal value.

The on-board DAC permitted the use of the multiplying DAC approach in this design. A scaled replica of the rectified input voltage was connected to pin 8 of the microcontroller, which is the reference for the on-board DAC. The other DAC input was determined by the digital voltage loop and was calculated internally using a digital proportional-integral (PI) controller.

The output of the DAC is connected via a voltage divider to one input of the on-board operational amplifier OPA. The other input for the OPA is a signal proportional to the inductor current. The feedback network for the OPA is a low-pass filter; therefore,

the output of the OPA is proportional to the average inductor current. On-board comparator C2 compares the output of the OPA and a reference sawtooth waveform from the PSMC module on the microcontroller to produce a PWM signal for the MOSFET switch in the power converter.

3.2 Modeling Active PFC with Input Voltage Sensing

General small signal models for PFC preregulators were discussed in Chapter 2. This section will further analyze and simplify the models for design purpose. For small signal models, the high value output capacitor is close to a voltage source, and the inductor can be roughly treated as a current source, and thus, the small signal models of the PFC preregulators can be simplified to a controlled current source [20].

A switching mode power converter usually has a 0 dB loop gain crossover frequency below 1/4 or 1/5 of the switching frequency. But for the PFC preregulator, the crossover frequency is at least decades away from the switching frequency. For loop stability and waveform distortion considerations, even with line voltage feed-forward, the crossover frequency of the outer voltage loop shall be below 120 Hz, and typically is limited to less than 20-30 Hz. Obviously, this frequency is far below the switching frequency of the preregulator, and is also considerably lower than that of the inner current loop.

Equation (1-19) shows that a boost converter contains a right half-plane zero, and this zero is so much higher than the overall crossover frequency of the PFC preregulator that it is no longer a consideration that may impact the performance of the PFC preregulator. Equation (1-19) does not include a zero introduced by ESR of the bulk

capacitor of the output stage of the boost converter. This zero is at even higher frequency, thus can be completely ignored in PFC applications.

Although low crossover frequency in the outer loop decreases the response time, this wide frequency separation in the inner current loop and the outer voltage loop provides some advantages in analysis and design of the PFC preregulator. Therefore, the outer voltage loop and the inner current loop can be analyzed and designed separately without significantly affecting the performance of the overall system.

The inner current loop has much higher frequency dynamics. At high frequency:

$$1 << \frac{RC}{2} s , \tag{3-1}$$

and:

$$1 + \frac{L}{D'^2 R} s << \frac{LC}{D'^2} s^2 . \tag{3-2}$$

Thus, the control-to-inductor-current transfer function of a boost converter $G_{id}(s)$ depicted in (1-20) can be simplified as:

$$G_{id}(s) = \frac{V_o}{Ls} . \tag{3-3}$$

This simplified $G_{id}(s)$ in (3-3) can be used to design the current loop compensator.

Similarly, the control-to-output transfer function of the power stage $G_{vd}(s)$ depicted in (1-19) can be simplified to:

$$G_{vd}(s) = \frac{V_o D'}{LC} \frac{\left(1 - \frac{L}{RD'^2} s\right)}{s^2} . \tag{3-4}$$

This simplified control-to-output transfer function of the power stage $G_{vd}(s)$ in (3-4) can be used to design the voltage loop compensator.

The control-to-output transfer function with the closed current loop $G_{vc}(s)$ can also be simplified. When line voltage feed-forward is not implemented, (2-36) is still valid, and can be written as:

$$P_{out} = P_{in} = K_I V_{in}^2 V_c = V_o I_o . \tag{3-5}$$

where I_o is the output current. When there is a perturbation in the system, (3-5) can be rewritten as:

$$K_I (V_{in} + \hat{v}_g)^2 (V_c + \hat{v}_c) = (V_o + \hat{v}_o)(I_o + \hat{i}_o), \tag{3-6}$$

where $\hat{i}_o$ is the perturbation of the output current.

Expanding (3-6) yields the following equation:

$$K_I (V_{in}^2 \hat{v}_c + 2V_{in} V_c \hat{v}_g + 2V_{in} \hat{v}_g \hat{v}_c + V_c \hat{v}_g^2 + \hat{v}_g^2 \hat{v}_c) = V_o \hat{i}_o + I_o \hat{v}_o + \hat{v}_o \hat{i}_o . \tag{3-7}$$

Since $\hat{v}_g$, $\hat{v}_c$, $\hat{v}_o$ and $\hat{i}_o$ all are small signal perturbations, it can be assumed that:

$$\hat{v}_g^2 \approx 0, \hat{v}_g \hat{v}_c \approx 0, \hat{v}_o \hat{i}_o \approx 0 . \tag{3-8}$$

Thus, (3-7) can be simplified as:

$$K_I (V_{in}^2 \hat{v}_c + 2V_{in} V_c \hat{v}_g) = V_o \hat{i}_o + I_o \hat{v}_o . \tag{3-9}$$

Therefore:

$$\hat{i}_o = \frac{K_I V_{in}^2}{V_o} \hat{v}_c + \frac{2K_I V_{in} V_c}{V_o} \hat{v}_g - \frac{I_o}{V_o} \hat{v}_o . \tag{3-10}$$

That is:

$$\hat{i}_o = g_c \hat{v}_c + g_g \hat{v}_g + \frac{1}{r_o}\hat{v}_o = \hat{i}_c + \hat{i}_g + \hat{i}_r . \tag{3-11}$$

where:

$$g_c = \frac{K_I V_{in}^2}{V_o}, \tag{3-12}$$

$$g_g = \frac{2K_I V_{in} V_c}{V_o}, \tag{3-13}$$

$$R_L = \frac{V_o}{I_o}. \tag{3-14}$$

$$r_o = -R_L . \tag{3-15}$$

According to (3-11), the small signal model for voltage loop at low frequency can be developed using the circuit in Fig. 3.2. Notice r_0 has a negative sign, therefore:

$$r_o // R_L = \infty . \tag{3-16}$$

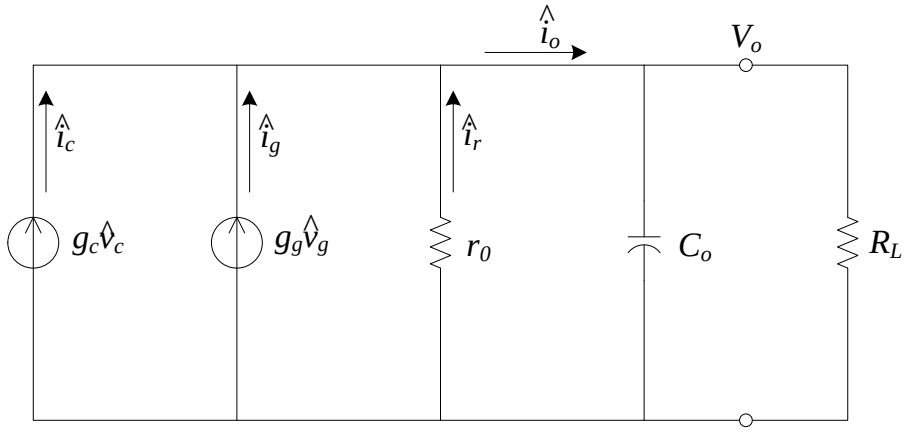


Fig. 3.2 Low-frequency small signal model for voltage loop of PFC preregulator

It can be seen from (3-16) that resistances are canceled, and the model can be further simplified to a current source driving a capacitor, as shown in Fig. 3.3. In this figure, $\hat{i}_e$ is the current of the equivalent current source, and can be expressed as:

$$\hat{i}_e = \hat{i}_c + \hat{i}_g = g_c \hat{v}_c + g_g \hat{v}_g \,. \tag{3-17}$$

Fig. 3.3 shows that the small signal model of the outer voltage loop is approximately a one pole system, and the pole is roughly at zero.

In order to obtain the control-to-output transfer function G_{vc}, it can be assumed that $\hat{v}_g = 0$. It can be derived from Fig. 3.3 that:

$$\hat{i}_e = \hat{i}_c = g_c \hat{v}_c = \frac{\hat{v}_o}{C_o s} \,. \tag{3-18}$$

Therefore:

$$G_{vc}(s) = \frac{\hat{v}_o}{\hat{v}_c} = \frac{g_c}{C_o s} = \frac{K_I V_{in}^2}{V_o C_o s} \,. \tag{3-19}$$

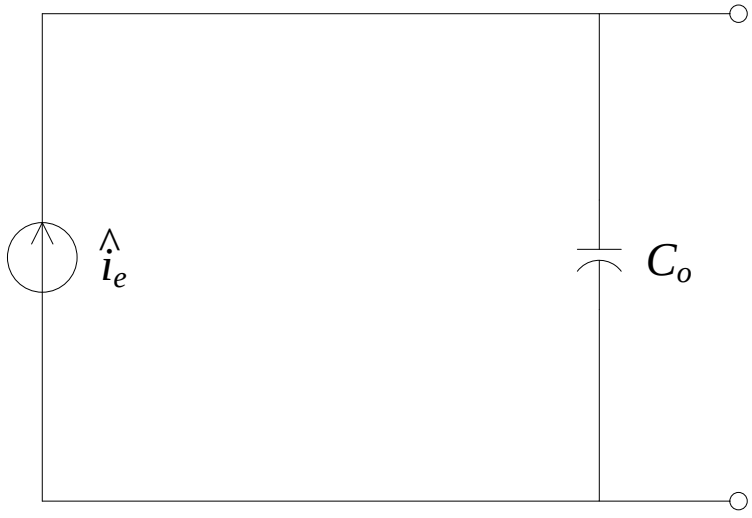


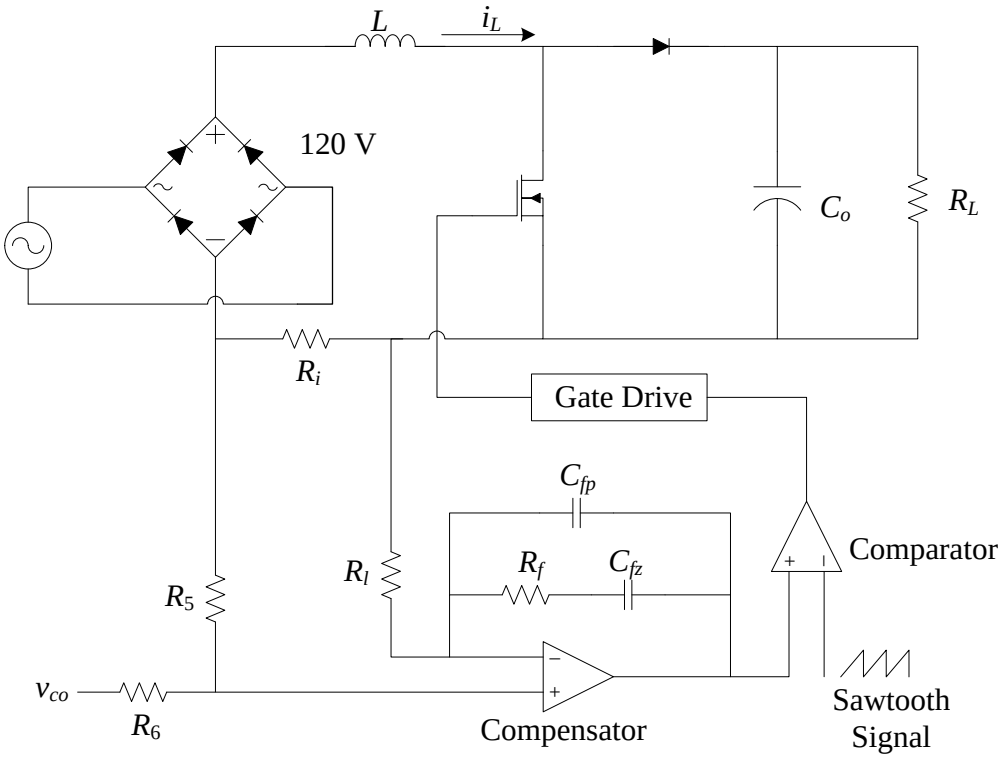
Fig. 3.3 Simplified low-frequency small signal model for voltage loop of the PFC preregulator

It has been pointed out previously that K_I is overall gain of the current loop, everything from the output of the voltage loop compensator to the inductor current, including the ratio of input voltage divider, multiplier gain, sense resistor, and the gain between the voltage loop and the current loop (which is set by two resistors).

Fig. 3.4 shows the analog implementation of the current loop, and K_I can be derived from Fig. 3.4. In this figure, v_{co} is the control output including the multiplier, and can be computed as:

$$v_{co} = K_m K_{in} V_{in} v_c \,. \tag{3-20}$$

where K_m is the multiplier gain and K_{in} the input voltage divider. Referring to Fig. 2.11, K_{in} can be set by the two resistors R_1 and R_2:



$$K_{in} = \frac{R_2}{R_1 + R_2}. \tag{3-21}$$

Fig. 3.4 shows that the voltage across R_i is determined by v_{co} through a voltage divider constructed by R_5 and R_6. That is:

$$R_i i_L = \frac{R_5}{R_5 + R_6} v_{co} = K_s v_{co}. \tag{3-22}$$

Thus:

$$v_{co} = \frac{R_i}{K_s} i_L. \tag{3-23}$$

Substitute (3-23) into (3-20):

$$i_L = \frac{K_m K_{in} K_s}{R_i} V_{in} v_c = K_I V_{in} v_c. \tag{3-24}$$

Therefore,

$$K_I = \frac{K_m K_{in} K_s}{R_i}. \tag{3-25}$$

Substitute (3-25) into (3-19) and the following equation is obtained:

$$G_{vc}(s) = \frac{\hat{v}_o}{\hat{v}_c} = \frac{K_m K_{in} K_s V_{in}^2}{V_o C_o R_i s}. \tag{3-26}$$

Equation (3-26) is the low frequency approximation of the control-to-output transfer function. In addition to the ESR of the output capacitors and the left half plane zero of the boost converter, this model ignores the frequency response of the inner current loop. This model is still accurate for the PFC preregulator because of the fact that the cutoff frequency of the outer voltage loop is considerably lower than 120 Hz, and is far below the switching frequency and the cutoff frequency of the inner current loop. It

can be seen from (3-26) that $G_{vc}(s)$ is a function of the input voltage V_{in}. Thus, the frequency response of the system varies with the V_{in}, and adding a feedforward loop can cancel away the V_{in}^2 term in (3-26).

3.3 System Design

3.3.1 Power Stage Design

The design process is started from the design of the power stage. A boost converter is selected in the design. For the laboratory prototype, the nominal input voltage (RMS) was 120 V, the nominal output was 207 V, and the nominal load was 100 W. The maximum power output is 300 W.

In order to select appropriate components of the power stage, the switching frequency must be selected first. The higher the switching frequency, the smaller the component sizes are required to filter out the switching noise. Meanwhile, the higher the switching frequency, the lower the efficiency can achieve. Therefore, the selection of switching frequency is largely a tradeoff between component size and efficiency. For low power PFC applications, the switching frequency is usually between 20 kHz to 300 kHz that can reach an acceptable compromise. Lower switching frequency is more desirable for higher power level PFC preregulators.

Although the selection of the switching frequency can be arbitrary as long as the switching frequency is in the acceptable range, in digital implementations, the switching frequency may have limitations that the switching frequency has to be a fraction of power of two of the oscillator frequency of the digital processor. For example, in the PIC16C782, when the crystal clock frequency is 20 MHz, the available switching

frequencies are 1.25 MHz, 625 kHz, 312.5 kHz, and 156.25 kHz. In this research, 156.25 kHz (1/128 of the 20 MHz oscillator frequency) is selected as the switching frequency. The frequency of the PWM signal generated by the PSMC module in the PIC16C782 is programmed by two bits of a control register. The other two bits of this control register can be utilized to determine the maximum duty cycle (1/2, 5/8, 3/4 and 15/16). In this implementation, 3/4 was selected.

The inductor of a boost converter defines the switching frequency ripple in the input current, which is the main consideration in selecting the inductor. The inductor limits the maximum value of the input sinusoidal current, which can be computed by:

$$i_{L\_\max} = \frac{\sqrt{2}P_{in\_\max}}{V_{in\_\min}}. \tag{3-27}$$

where $P_{in\_\max}$ is the maximum input power, and $V_{in\_\min}$ is the minimum line voltage. Notice that $i_{L\_\max}$ is the peak value of the 60 Hz current, and Δi_L, the peak-to-peak ripple at switching frequency, is added to $i_{L\_\max}$, so the instantaneous peak value of the inductor current is:

$$i_{L\_peak} = i_{L\_\max} + \Delta i_L . \tag{3-28}$$

Once the allowed i_{L_peak} is determined, Δi_L can be computed easily from (3-28). Normally, Δi_L is selected to be 20% of $i_{L\_\max}$.

When the switch is turned on, the inductor current starts to increase. For a certain period Δt, the change in inductor current Δi_L can be expressed by following equation:

$$\frac{\Delta i_L}{\Delta t} = \frac{V_{in}}{L}. \tag{3-29}$$

Thus, in on-time of one duty cycle, the change of the inductor current is:

$$\Delta i_L = \int_0^{DT_s} \frac{V_{in}}{L} dt = \frac{DT_s V_{in}}{L} = \frac{DV_{in}}{f_s L}. \tag{3-30}$$

where T_s is the switching period, f_s is the switching frequency, and D is the duty cycle.

For boost converter, D can be calculated by:

$$D = \frac{V_o - V_{in}}{V_o}. \tag{3-31}$$

Rearranging (3-30) yields:

$$L = \frac{DV_{in}}{f_s \Delta i_L}. \tag{3-32}$$

Inductor can be selected based on (3-32). In order to ensure that the peak inductor current is under the limit, the inductor value should be bigger than the value calculated by (3-32). Assume V_o is a constant, according to (3-31) and (3-32), the inductor value reaches its maximum when V_{in} equals half of V_o. Therefore, when half of the output voltage V_o is inside the operating range of the input voltage V_{in}, then the inductor value must satisfy following equation:

$$L \geq \frac{V_o}{2 f_s \Delta i_L}. \tag{3-33}$$

In this implementation, Δi_L is set to be 0.5 A. Since V_o is 207 V, and f_s is selected to be 156.25 kHz, according (3-33), the inductor value should be larger than 1.32 mH, and actual inductor value is 1.56 mH.

In a PFC preregulator, the output filter capacitor must be large enough to filter out the 120 Hz ripple. According to (2-33), the output capacitor C_o must satisfy following condition to filter out the 120 Hz ripple:

$$C_o \geq \frac{V_o}{2\Delta V_o \omega R_L}. \tag{3-34}$$

In this implementation, assuming $\Delta V_o < 1\%$ of V_o when the PFC preregulator is operating at nominal output power (100 W), then C_o should be bigger than 310 μF.

Another consideration is the hold-up time of the preregulator output [22, 41]. Hold-up time is the remaining time length of the output voltage within a specific range after the line voltage has been absent. Assuming the allowed minimum output voltage is $V_{\min}$, and the required hold-up time is Δt, then the energy consumed during the hold-up time is:

$$P_o \Delta t = \frac{1}{2} C_o V_o^2 - \frac{1}{2} C_o V_{\min}^2. \tag{3-35}$$

Thus, the minimum output capacitor C_o is:

$$C_o = \frac{2\Delta t P_o}{V_o^2 - V_{\min}^2}. \tag{3-36}$$

The hold-up time Δt may dominate any other considerations in selecting the output capacitors if the output power is high or the required hold-up time is long. In this implementation, nominal P_o is 100 W, nominal V_o is 207 V. If $V_{\min}$ is 180 V, and the required hold-up time Δt is three cycle (60 ms), then C_o is 1.15 mF. If the hold-up time Δt is one cycle (20 ms), then C_o is 382 μF. In this implantation, C_o is selected to be 560 μF, which can limit the output voltage ripple to 0.57 V, and Δt is 30 ms when $V_{\min}$ is 180 V.

In order to sense the inductor current, a sense resistor or a current transformer must be used. The cost of a sense resistor is low, and it is very flexible to set the resistance values using a sense resistor. To minimize the power dissipation on the sense resistor, the resistance value should be as small as possible. However, if the sense resistor is too small, the voltage across the resistor is too low, and it will be very susceptible to noise; As a result, it is very difficult to control the inductor currently satisfactorily. Therefore, a sense resistor is especially suitable when the power level or the inductor current is low.

When the power or current is high, the power dissipation on a larger sense resistor may be too high to be acceptable. For example, if the current is 20 A, the voltage across a 0.03 Ω resistor is only 0.6 V, but the power dissipated on this resistor is 12 W. In this case, current transformers shall be used. Usually, when the power is over 1 kW, current transformers shall be used to sense the current.

Note that a current transformer cannot sense DC values of the inductor current directly; therefore, one single transformer cannot sense the inductor current correctly. Instead, when using current transformers to sense the current, two transformers must be used: one is used to sense the diode current, and another one is used to sense the switch current, and then the sensed diode current and switch current are added together. The secondary side of the current transformer cannot be opened to avoid dangerous high voltage, and a sense resistor must be connected securely to the secondary side, and the voltage across the sense resistor reflects the current. Fig. 3.5 illustrates a setup for the current transformers, where the current passing through the sense resistor R_i is proportional to the inductor current by the turns ratio of the current transformers.

Because the current in the secondary side is much lower than the primary side, the sense resistor can be selected to be much higher, such that the voltage across the sense resistor is high enough to achieve a high signal-to-noise ratio with low power dissipation on the sense resistor. In addition, the output of the current transformer can be configured as a negative voltage easily by simply changing the direction of the diodes in Fig. 3.5. This configuration may be useful when using some analog PFC IC chips such as the UC3854 [21 - 22].

In this implementation, since the maximum power is only 300W, corresponding to the inductor current less than 2 A, a 0.1 Ω sense resistor is selected in the design.

3.3.2 Current Loop Design

When designing the hybrid PFC controller, the current loop should be designed first. Considering the fact that the line frequency is far less than the switching frequency, the input voltage can be treated as a constant at any given switching cycle, which is similar to an ACMC DC-DC converter. Once the current loop is designed, the converter with the closed current loop can be treated as a "new" open-loop plant, and the voltage

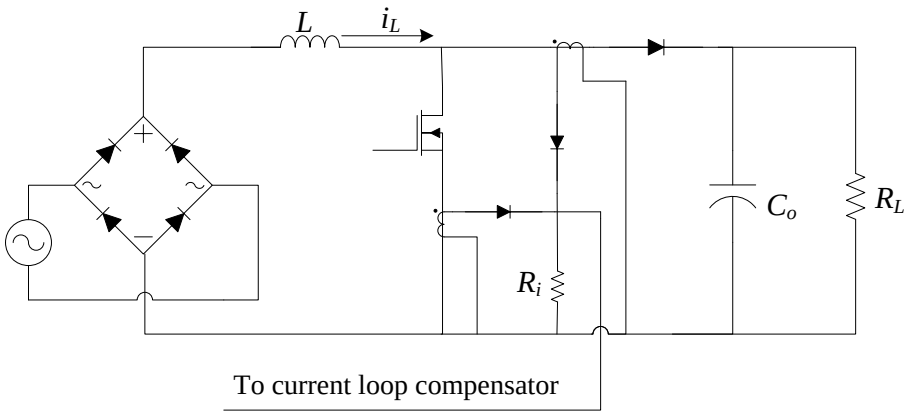


Fig. 3.5 Current transformers setup

loop compensator can then be designed to control the "new" plant. The new system is a typical digital control system. A digital PI controller was designed to compensate the output voltage error.

The current loop compensator has been illustrated in Fig. 2.2. In designing the current amplifier, its gain should be chosen first. Because the OPA module of a PIC16C782 microcontroller is an analog peripheral, the current loop design procedure is exactly the same as a traditional analog ACMC case.

The down slope of the amplified inductor current error must not exceed the slope of the external ramp. As a result, there is an upper limitation on G_{CA} at the switching frequency, which indirectly establishes the maximum current loop gain crossover frequency. G_{CA} is approximately R_f/R_l at the switching frequency [6, 10-11], and can be expressed by:

$$G_{CA} \cong \frac{R_f}{R_l} < \min\left\{\frac{2V_m f_s L}{V_g R_i}, \frac{V_m f_s L}{V_o R_i}\right\}, \tag{3-37}$$

where f_s is the switching frequency and V_o is the output voltage of the boost converter.

The gain of this current amplifier can be expressed as:

$$G_{CA}(s) = \frac{K_c(1+s/\omega_z)}{s(1+s/\omega_p)}, \tag{3-38}$$

where $K_c = \frac{1}{R_l(C_{fp}+C_{fz})}$, $\omega_z = \frac{1}{R_f C_{fz}}$, $\omega_p = \frac{C_{fp}+C_{fz}}{R_f C_{fp} C_{fz}}$. Equations (3-37) and (3-38) set the criterion to choose R_f and R_l. According to the desired locations of the pole and zero, capacitor values can be selected. In this implementation, V_m is set to be 3 V, the zero ω_z is placed at a decade below switching frequency to maximize the current loop crossover

frequency. The high frequency pole ω_p is placed at one-half of the switching frequency f_s to filter out the switching frequency ripple.

The current amplifier in the current loop can be designed by using the on-board analog operational amplifier module (OPA module) on the PIC16C782 microcontroller with several external capacitors and resistors. The complete current loop realized is shown in Fig. 3.6. Since both the OPA module and the comparator C_1 are analog peripherals inside the microcontroller, the current loop is the same as a traditional analog case. Therefore, no complex algorithm is required to estimate the inductor current. The following steps are employed to design the current amplifier:

1. Compute R_f and R_l such that the current amplifier has a smaller gain than the maximum gain allowed at switching frequency:

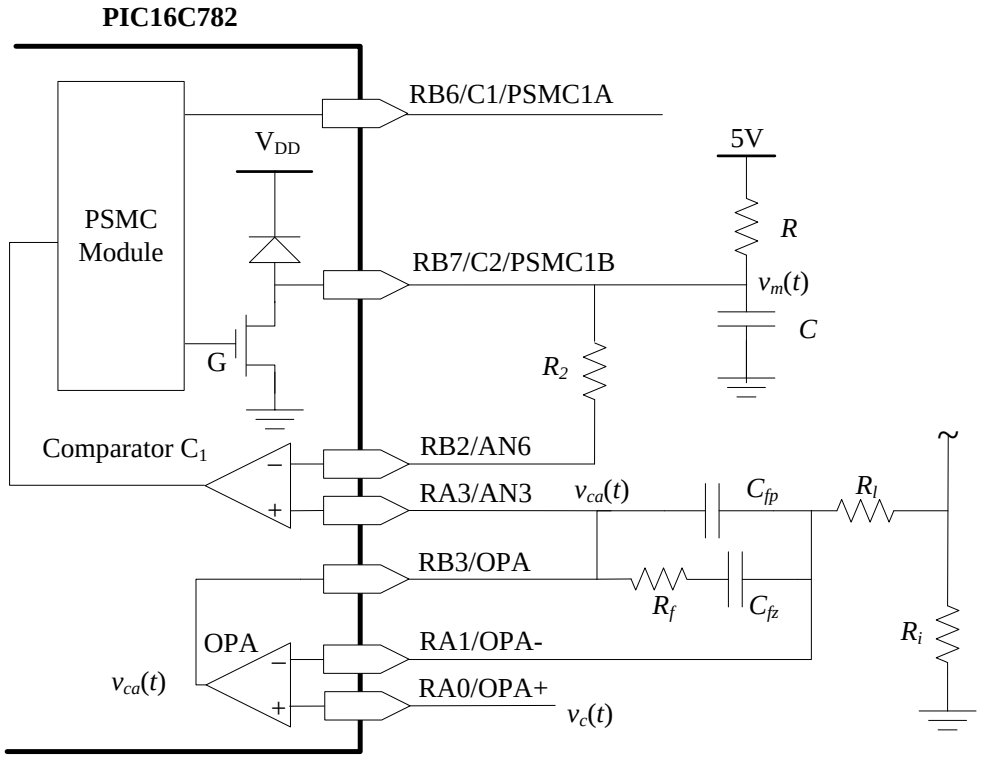


Fig. 3.6 Current loop of a PFC preregulator realized on a PIC16C782

$$\frac{R_f}{R_l} \le G_{CA\max} = \frac{V_m f_s L}{V_o R_i} = \frac{3 \times 156.25 \times 10^3 \times 1.56 \times 10^{-3}}{207 \times 0.1} = 35.3 . \qquad (3\text{-}39)$$

Ideally, V_m should be 5 V (which is the supply voltage of the microcontroller) to achieve the maximum gain. However, the signal v_m is generated by an RC network, which will be discussed in detail later, so V_m has to be set below 5 V to ensure an approximate linear ramp signal. Select R_f = 160 kΩ and R_l = 20 kΩ, so $\frac{R_f}{R_l} = 8$, which satisfies the requirement in (3-39) that $\frac{R_f}{R_l} \le 35.3$.

3. Compute C_{fz} according to the location of the zero ω_z. In this implementation, ω_z is placed at a decade below switching frequency ω_s:

$$\omega_z = \frac{1}{R_f C_{f_z}} = \frac{\omega_s}{10} . \qquad (3\text{-}40)$$

$$C_{fz} = \frac{10}{R_f \omega_s} = \frac{10}{160 \times 10^3 \times 2\pi \times 156.25 \times 10^3} = 6.4 \times 10^{-11} \text{ F} = 64 \text{ pF} . \qquad (3\text{-}41)$$

In this implementation, C_{fz} is selected 100 pF instead of 64 pF such that the zero is a little lower than one-tenth of the switching frequency. Thus, the zero is actually at:

$$\omega_z = \frac{1}{160 \times 10^3 \times 100 \times 10^{-12}} = 6.25 \times 10^4 \text{ rad/s} = 9.95 \text{ kHz} . \qquad (3\text{-}42)$$

4. Find C_{fp} according the location of the pole ω_p. The typical ω_p location is between one-third and one-half of the switching frequency. In this implementation, one-half of the switching frequency is selected:

$$\omega_p = \frac{(C_{fp} + C_{fz})}{R_f C_{fp} C_{fz}} = \frac{2\pi f_s}{2} = 156.25\pi \times 10^3 \text{ rad/s} . \qquad (3\text{-}43)$$

Substitute $R_f = 160\ \text{k}\Omega$ and $C_{fz} = 100\ \text{pF}$ into (3-43), we have:

$$C_{fp} + 100\times10^{-12} = 156.25\pi\times10^{3}\times160\times10^{3}\times100\times10^{-12}\times C_{fp}\,. \tag{3-44}$$

$$C_{fp} = 1.46\times10^{-11} \cong 15\ \text{pF}\,. \tag{3-45}$$

Thus, the pole is actually located at:

$$\begin{aligned}\omega_p &= \frac{(C_{fp}+C_{fz})}{R_f C_{fp} C_{fz}} = \frac{(15+100)\times10^{-12}}{160\times10^{3}\times15\times10^{-12}\times100\times10^{-12}} \\ &= 4.79\times10^{5}\ \text{rad/s} = 7.63\ \text{kHz}.\end{aligned} \tag{3-46}$$

At this time,

$$K_c = \frac{1}{R_I(C_{fp}+C_{fz})} = \frac{1}{20\times10^{3}\times(15+100)\times10^{-12}} = 4.35\times10^{5}\,. \tag{3-47}$$

The Bode plot of this current amplifier is shown in Fig. 3.7.

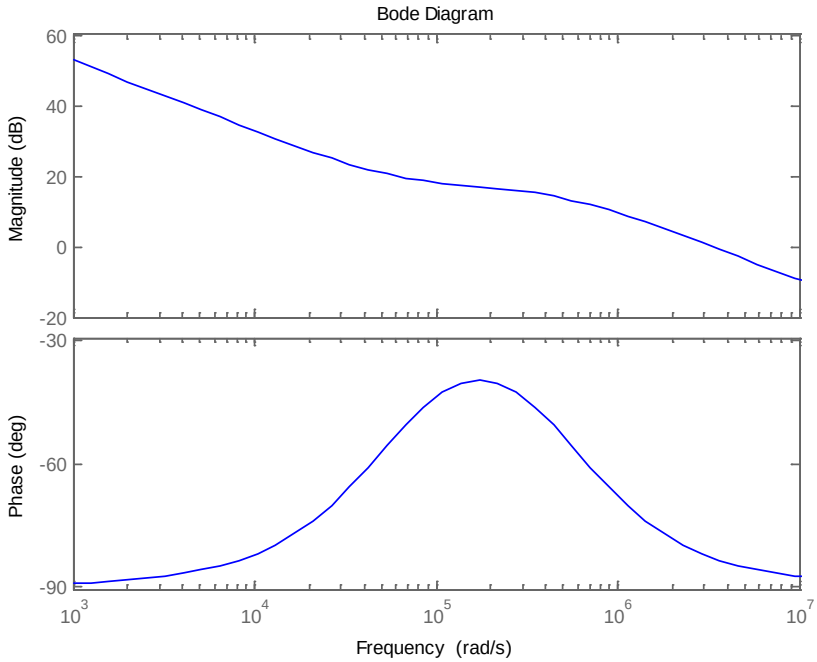


Fig. 3.7 Bode plot of the current amplifier

Notice that both of the inputs of the current amplifier should be within the normal operational range of the OPA module. In addition, the magnitude difference of the two inputs should not be too large to avoid possible saturation. The reference of the current amplifier v_c, referring to Fig. 3.6, is the output of the digital voltage loop through a D/A converter. In order to ensure enough resolution, the D/A output should be around 2.5 V at nominal operating condition. Therefore, it is desired that the sense resistor should provide adequate linear gain R_i such that the sensed voltage $v_s = R_i i_L$ is around 2.5 V. However, for a low value R_i = 0.1 Ω, the actual v_s is well below 0.1 V, much lower than the reference voltage v_c. The simplest way to solve this problem is to increase the value of the sense resistor. However, this approach will significantly increase the power loss in the power stage, so it is not a preferable method.

A commonly used approach is to amplify the sensed current signal by an opamp, as shown in Fig. 3.8. This amplifier also acts as a low-pass filter to filter out switching spikes. Indeed, many power converters use this method to condition the sensed current. However, this method requires an extra opamp that increases the cost and complexity of the circuit.

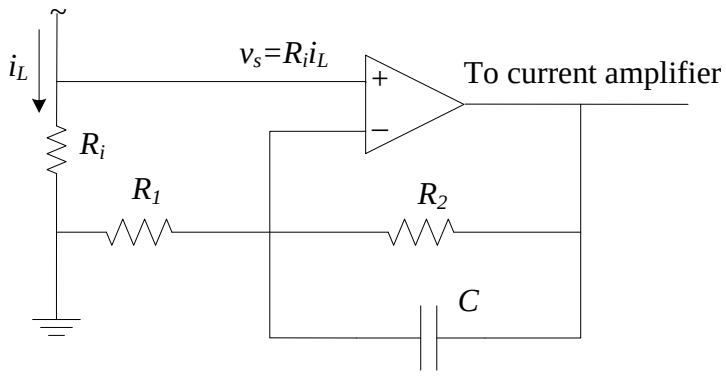


Fig. 3.8 Sensed current signal is amplified by an opamp

In this implementation, instead of manipulating the sensed current signal, the current reference of the current amplifier is modified. As shown in Fig. 3.9, the D/A output, instead of being sent directly to the current amplifier, is connected to a voltage divider. This method scales down the D/A output, such that it is compatible with the value range of the sensed current signal. This method is simple and low-cost, but it can effectively solve the problem.

Since there is no internal analog path between the OPA module and the on-board comparator C_1, the output of the current amplifier v_{ca} is sent out of the PIC16C782 through an analog IO port, and then is sent to C_1 through another analog IO port. In order to obtain the PWM signal to control the switch, a ramp signal v_m is needed as the reference for the comparator. v_m can be generated by using the PSMC module with an external RC network. The waveforms at C_1 inputs are shown in Fig. 3.10, where v_m is the ramp signal at the C_1 negative input.

It can be seen from Fig. 3.10 that the ripple in v_{ca} is very small and can be ignored. This is because of the fact that the voltage loop bandwidth is significantly lower than the switching frequency, so the ripple in v_{ca} is negligible.

For a fixed supply voltage (5 V in this implementation), referring to Fig. 3.6, v_m is directly defined by R and C. For an RC circuit, the time constant is $\tau = RC$, and R and C

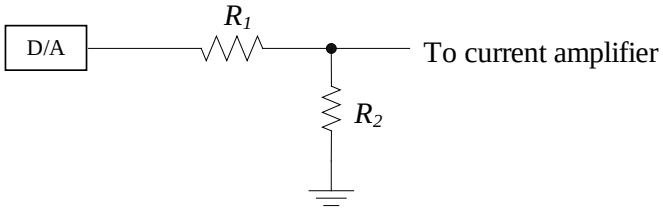


Fig. 3.9 D/A output is scaled down by a voltage divider

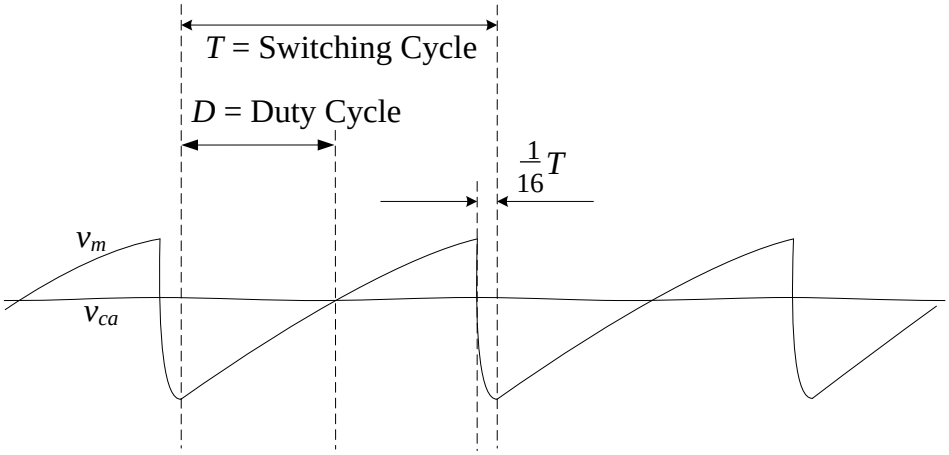


Fig. 3.10 The waveforms at C_1 inputs

can be selected by:

$$v_m(t) = 5 - 5e^{-t/RC} \Rightarrow RC = -\frac{t}{\ln\frac{5 - v_m}{5}}. \tag{3-48}$$

When designing the RC network to generate v_m, its peak value V_m should be chosen as high as possible while maintaining the linearity of v_m. Therefore, v_m should not be close to 5 V at any possible duty cycle. When the maximum duty cycle is specified, v_m should be below 5 V at maximum duty cycle. For example, in this implementation, let v_m equal 3.8 V at 75% duty cycle. Since the switching frequency f_s = 156.25 kHz, so the switching period T_s = 6.4 μs. Thus,

$$RC = -\frac{6.4\times10^{-6}\times0.75}{\ln\frac{5-3.8}{5}} = 3.363\times10^{-6}\ \text{s}. \tag{3-49}$$

Choose C = 100 pF, then R = 33.63 kΩ ≈ 33 kΩ. Based on experimental measurements, the actual value of v_m reaches 3.4 V at 75% duty cycle (D_{max}, maximum duty cycle). The equivalent V_m is:

$$V_m = \left.\frac{v_m(t)}{D_{max}}\right|_{t=D_{max}T_S} = \frac{3.4}{0.75} = 4.6 \text{ V} . \quad (3\text{-}50)$$

3.3.3 Analog to digital conversion (ADC) and time delay

In the proposed PFC preregulator scheme, the voltage loop is implemented digitally. Therefore, the output voltage v_o of the power stage must be sampled as the feedback to the voltage loop compensator. The ADC module inside the PIC16C782 captures a snapshot of the sampled signal and holds it for an A/D conversion.

It is required that the A/D conversion should have adequate resolution to ensure proper measurement of the output voltage. This resolution is determined by the range of measurement and the word length of the digital value. In this implementation, the nominal output voltage of the PFC preregulator is 207 V, so the output voltage can easily be higher than 230 V during transient period. Since the ADC module has an 8-bit resolution, the A/D conversion error can be easily close to 0.9 V when the possible full range of output voltage (0 V – 230 V or more) is measured, which is a steady state error at the output voltage.

In order to get higher A/D resolution, a level-shift circuit was designed such that the A/D result represents a “windowed” range of the output voltage around the nominal value. In this implementation, the “window” is in the range of 189.8 V and 224.2 V for a 207 V nominal output voltage. The level shifter can be built from an external operational amplifier with several external resistors. A voltage buffer (voltage follower) is used to ensure accurate measurement of the output voltage. In this implementation, shown in Fig. 3.11, the dc bias voltage is set to 2.5 V, and the gain of the opamp is set to 12. In this system, since the OPA module is used as the current amplifier, two external opamps,

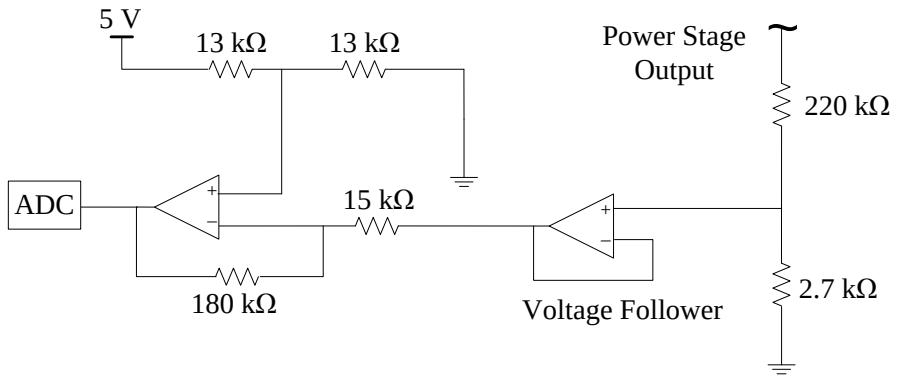


Fig. 3.11 Level-shift circuit

although they are integrated in one IC chip, are used to construct the level-shift circuit and the voltage buffer. Since the current-loop is constructed using analog components, the signal in the current loop instantaneously varies with the inductor current without time delay. Therefore, it is desirable to update the current reference, which is the output of the voltage loop, at the beginning of each switching cycle.

However, this ideal situation is difficult to achieve when using a PIC16C782 to control a power converter. Because of the limited computation power of the PIC16C782 and the fast dynamics of the power stage, the delays due to A/D conversion and control computation cannot be neglected.

For example, in this implementation, the switching frequency is 156.25 kHz for a switching period of 6.4 μs. When the oscillator frequency is 20 MHz, an A/D conversion cycle requires 15.2 μs, which equals 2.375 switching cycles. For a 20 MHz oscillator frequency, the instruction cycle (the time to execute an instruction) is 0.2 μs, so only 32 instructions can be executed in each switching cycle. This implies that even a very simple control law is difficult to be completed in a single switching cycle. Indeed, in this

implementation, nearly 3 switching cycles (or nearly 19.2 μs) are needed to finish the calculation of the control law. A/D conversion and calculations can be performed simultaneously, but the A/D conversion time is much faster than the calculation time (controller time delay), so the calculation time directly determines the sampling period.

In order to achieve a constant sampling frequency, there is a short waiting period (less than one switching cycle, or less than 6.4 μs) before starting the next sampling period. When this waiting period is neglected, the controller sampling period approximately equals the controller time delay, or 19.2 μs. In order to update the current reference as soon as possible, the controller time delay should be as short as possible. Therefore, compact software design is critical in this implementation.

Switching noise in the output voltage is inevitable. In order to achieve concise software, switching noise in the output voltage should be avoided or filtered out in "hardware" instead of by a digital filter. A digital filter is indeed not practical in this implementation, because the switching noise contains harmonics with frequency much higher than the possible sampling frequency. Therefore, the output voltage should be sampled during the period that has minimum switching noise. In this implementation, the PWM signal is sent back to another I/O pin to trigger an interrupt that starts an A/D conversion, so the sampling moment can be controlled accurately, and the output voltage can always be captured after the switching noise has subsided. Since the PIC16C782 does not have priority levels for interrupts, an interrupt from any other source should not be allowed to ensure constant sampling rate and the proper sampling moment. The starting point of each A/D conversion cycle can be controlled precisely at a 0.2 μs (one instruction cycle) precision.

3.3.4 Voltage Loop Design

Once the current loop is designed, the converter with the closed current loop can be treated as a new open loop plant with $G_{vc}(s)$ as its control-to-output transfer function. $G_{vc}(s)$ shall also include the effect of the feedforwad loop when the feedforward loop is implemented, and the voltage loop compensator $G_c(s)$ is designed to control the "new" plant $G_{vc}(s)$. The "new" system, shown in Fig. 3.12, is essentially a typical digital control system, and the voltage loop compensator is a standard digital controller. Usually, the digital controller can be designed using either the emulation method or the direct digital design method. In this implementation, a method combining the emulation method and the direct digital design method is used.

As stated before, $G_{vc}(s)$ can be computed using the small signal models described previously or measured experimentally. The simplified first order model defined by (3-26) is used in this implementation. It can be seen from (3-26) that $G_{vc}(s)$ is no longer a function of $G_{vd}(s)$ or $G_{id}(s)$, since the voltage loop has very slow dynamics compared to the current loop, all the high frequency dynamics are ignored in the model.

It can be seen from (3-26) that $G_{vc}(s)$ is a function of the input voltage. Thus, the frequency response of the system varies with the input voltage. In order to ensure the

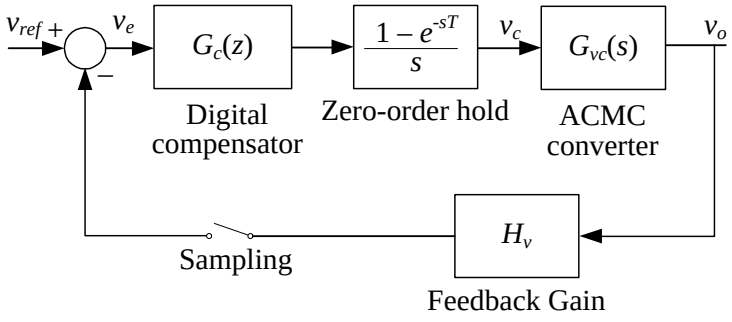


Fig. 3.12 System block diagram of a PFC preregulator with closed current loop

stability of the system for different input voltages, the system with the highest input voltage (which is 180 V) was chosen to design the voltage loop compensator.

Once $G_{vc}(s)$ is obtained, it can be converted to a discrete-time model $G_{vc}(z)$ using the zero-order hold (ZOH) method. The continuous time ZOH, as expressed in (2-43), introduces a phase lag and magnitude reduction to the system. This can be seen clearly in its Bode plot shown in Fig. 3.13. In this implementation, the total time delay is approximately three times the switching period (6.4 μs), so 19.2 μs is used as the controller sampling period. According to (2-44), $G_{vc}(z)$ can written as:

$$G_{vc}(z) = \frac{z-1}{z} \mathcal{Z}\left[\frac{G_{vc}(s)}{s}\right]. \tag{3-51}$$

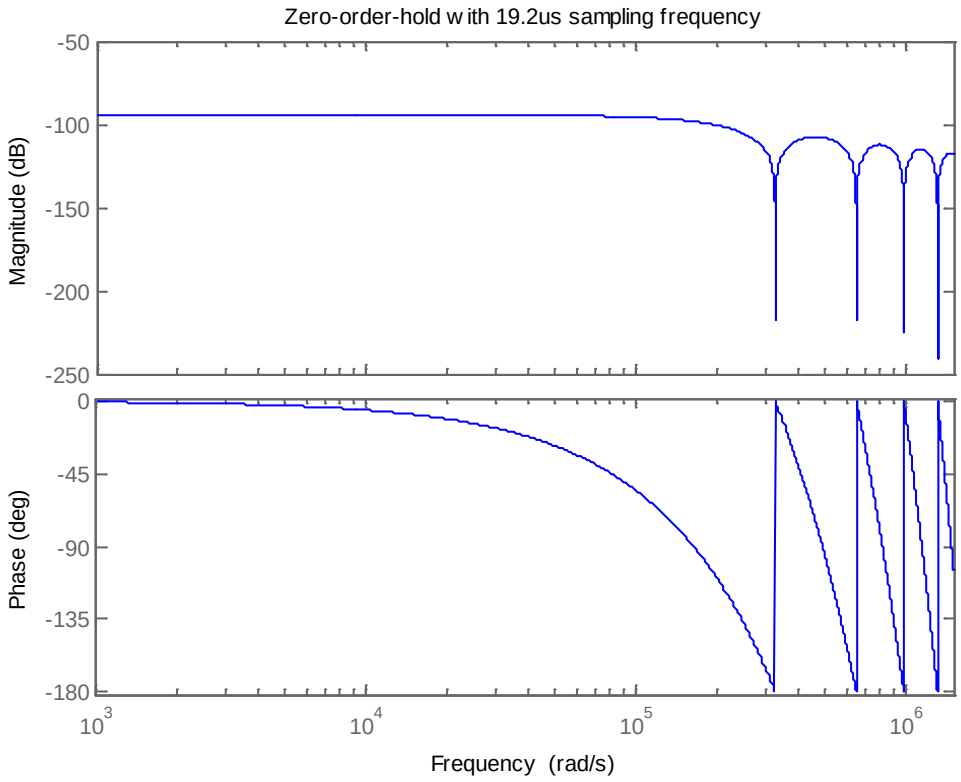


Fig. 3.13 Bode plot of zero-order-hold when sampling frequency is 19.2 μs

As stated previously, the calculation time is approximately equal to the sampling period. Considering the time delay, the mapping of $G_{vc}(s)$, referring to (2-49), can be expressed as:

$$G_{vc}^{'}(z) = z^{-1}G_{vc}(z) = \frac{z-1}{z^2}\Im\left[\frac{G_{vc}(s)}{s}\right], \tag{3-52}$$

In Fig. 3.14, the Bode plots of $G_{vc}(s)$, $G_{vc}(z)$, and $G_{vc}^{'}(z)$ are compared when input voltage is 120 V, where the transformation $z = e^{j\omega T}$ is used to map the unit circle to the real frequency axis. Notice that the Bode plot of $G_{vc}^{'}(z)$ is indeed obtained from mapping $G_{vc}^{'}(z)$ to $G_{vc}^{'}(s)$ in the *s*-domain using $z=e^{sT}$, or:

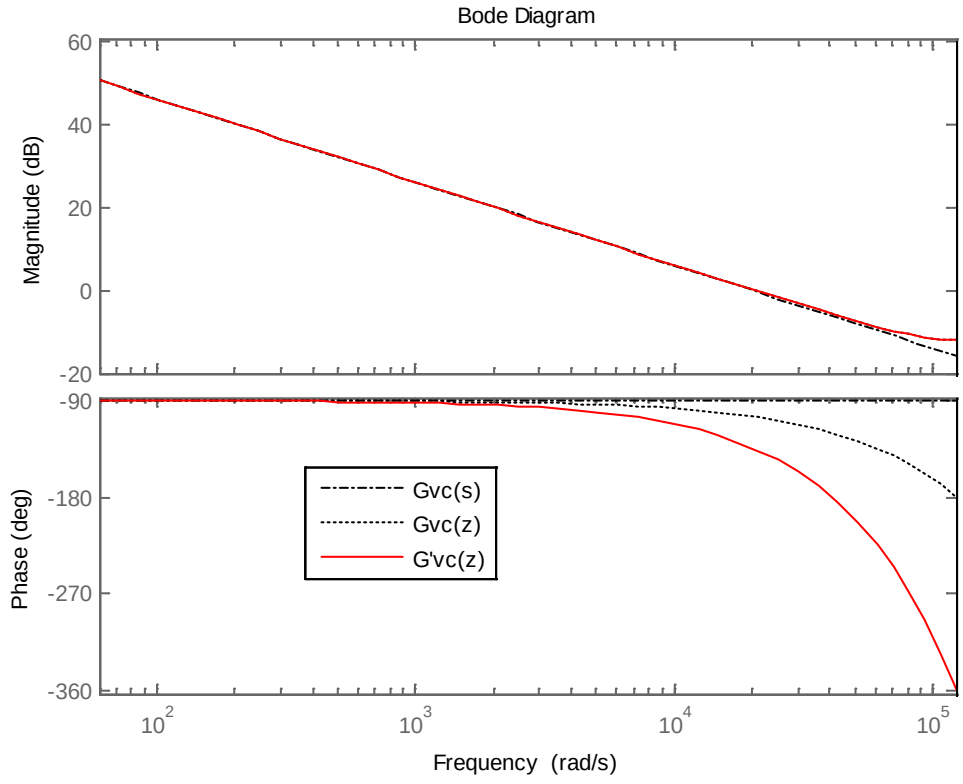


Fig. 3.14 Bode plot of control-to-output transfer function of the PFC preregulator

$$G_{vc}^{'}(s) = G_{vc}^{'}(z)\Big|_{z=e^{sT}} . \quad (3\text{-}53)$$

Fig. 3.14 indicates that the ZOH and controller time delay introduce considerable phase delay at high frequency when mapping the system from the *s*-plane to the *z*-plane. Therefore, $G_{vc}^{'}(z)$ should be used to design the voltage loop compensator.

A PI controller can be used as the voltage loop compensator in a PFC preregulator. A PI controller is essentially a phase-lag compensator. It can eliminate steady-state error, since it has high gain at low frequency (a pole at zero).

However, a PI controller cannot be designed directly in the *z*-plane. Usually, a digital PI controller is designed using the emulation method or in the *w*-plane. However, the direct emulation method is not suitable when the ZOH and time delay need to be considered. Designing in the *w*-plane requires that the model be transformed between the *z*-plane and the *w*-plane. In this work, instead of mapping the system from the *z*-plane to the *w*-plane, the system is mapped from the *s*-plane to *z*-plane.

The Bode plot cannot be generated in the *z*-domain, so the Bode plot of $G_{vc}^{'}(z)$ is actually the Bode plot of $G_{vc}^{'}(s)$. It could be difficult to develop a mathematical equation for $G_{vc}^{'}(s)$, but it is very easy to obtain its Bode plot using MATLAB. The difference between $G_{vc}^{'}(s)$ and $G_{vc}(s)$ is that the ZOH and time delay are included in $G_{vc}^{'}(s)$, so $G_{vc}^{'}(s)$ is more accurate for design purposes. Once the Bode plot of $G_{vc}^{'}(s)$ is obtained, it can be used to design the controller.

In this implementation, a PI controller is designed in the *s*-domain using the Bode plot of $G_{vc}^{'}(s)$. The *s*-domain compensator can be expressed as:

$$G_c(s) = K_P + \frac{K_I}{s} = \frac{K_I(1+s/\omega_0)}{s}, \tag{3-54}$$

where K_P is the proportional gain and K_I is the integral gain. Equation (3-54) shows that the zero ω_0 is located at K_I/K_P, and its high frequency gain is K_P. Equation (3-54) also shows that a PI controller will not change the phase of the system at high frequency. Suppose the phase margin is specified to be φ_m at a certain frequency, and the phase margin of $H_v G_{vc}^{'}(s)$ is φ_m at ω_1. Assume that the dc gain of $H_v G_{vc}^{'}$ is adjusted by a factor of K_c to meet the low frequency specification, then the following equation must be satisfied when designing the controller:

$$K_P K_c H_v G_{vc}^{'}(j\omega_1) = 1\angle -(180° - \varphi_m). \tag{3-55}$$

Equation (3-55) shows that K_P should be adjusted such that the open loop gain of the compensated system has unity gain at ω_1. In order to ensure that the compensator introduces very little phase lag at ω_1, the zero ω_0 should be placed far enough from ω_1, and one tenth of ω_1 is a suitable value. Equation (3-55) neglects any phase lag of the compensator. Indeed, when choosing $\omega_0 = 0.1\omega_1$, the phase lag at ω_1 is about 5°. Thus, following equation is used to determine K_P:

$$K_P = \frac{1}{\left| K_c H_v G_{vc}^{'}(j\omega_1) \right|}, \tag{3-56}$$

where ω_1 is the frequency when the phase of $G_{vc}^{'}(j\omega_1)$ equals – (180° – φ_m – 5°). When K_P is obtained, K_I can be computed by:

$$K_I = \omega_0 K_P = 0.1\omega_1 K_P. \tag{3-57}$$

Referring to (3-55), since dc gain of $H_v G_{vc}^{'}$ has been adjusted by the factor K_c, the

dc gain should be adjusted back by a factor of K_c, so the complete PI controller transfer function is:

$$G_c(s) = K_c\left(K_P + \frac{K_I}{s}\right). \tag{3-58}$$

As stated before, $G_{vc}(s)$ is a function of input voltage in this implementation. Therefore, it is desired that at any possible input voltage, the following condition should be satisfied:

$$\left|K_P K_c H_v G_{vc}^{'}(j\omega_1)\right| \le 1. \tag{3-59}$$

Equation (3-59) implies that, in order to ensure proper phase margin, the input voltage V_{in} selected for the purposes of design should be the value at which $H_v G_{vc}^{'}(s)$ has its largest magnitude. In this implementation, assume that there is no need to adjust the dc gain of $H_v G_{vc}^{'}$ to meet the low frequency specification, that is, K_c = 1.

Considering the worst case scenario that a maximum input voltage is 180 V and a minimum input voltage of 80 V, the Bode plot of the digitalized $H_v G_{vc}^{'}(s)$ at these operating conditions is shown in Fig. 3.15. Set the phase margin φ_m to 55°， so the phase of $G_{vc}^{'}(j\omega_1)$ is – (180° – 55° – 5°) = –120°. For 180 V input voltage, ω_1 is 1.37×10^4 rad/s, corresponding to a magnitude of 3.29 dB. For 80 V input voltage, ω_1 is the same, but corresponding to a magnitude of -10.8 dB. Since $H_v G_{vc}^{'}(j\omega_1)$ has the largest magnitude at 180 V input voltage (highest input voltage), the system with the highest input voltage should be chosen for the design of the voltage loop compensator.

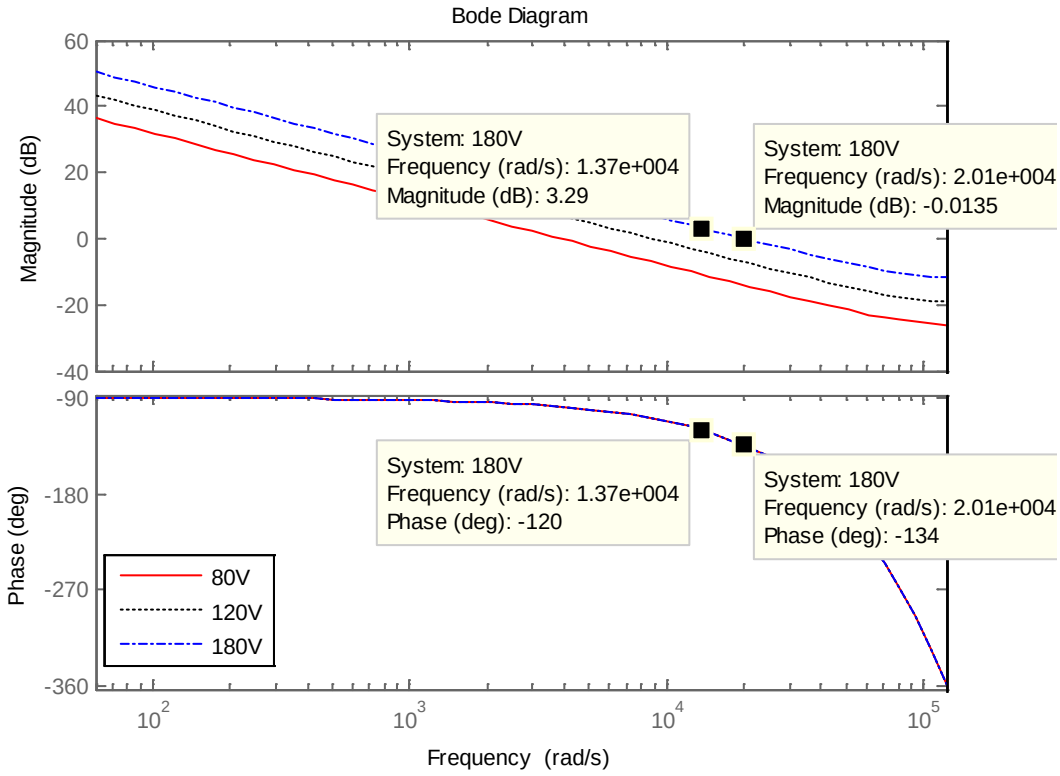


Fig. 3.15 Bode plots of $H_vG'_{vc}(j\omega)$ at different input voltage

Substitute $\left|H_v G_{vc}^{'}(j\omega_1)\right| = 3.29\,\text{dB}$ into (3-56):

$$K_P = \frac{1}{\left|H_v G_{vc}^{'}(j\omega_1)\right|} = \frac{1}{10^{3.29/20}} = 0.685\,. \tag{3-60}$$

Thus, K_I can be computed according to (3-57),

$$K_I = 0.1\omega_1 K_P = 0.1\times 1.37\times 10^4 \times 0.685 = 938\,. \tag{3-61}$$

Hence, the zero ω_0 of the PI controller is:

$$\omega_0 = \frac{K_I}{K_p} = \frac{938}{0.685} = 1369.4\,\text{rad/s}\,. \tag{3-62}$$

The voltage loop compensator can be expressed in the s-domain by:

$$G_c(s) = K_p + \frac{K_I}{s} = 0.685 + \frac{938}{s}. \tag{3-63}$$

In this implementation, the sampling period is 3 times of switching period, or 19.2 μs. Using the backward rule, the *s*-domain PI controller is then converted to a *z*-domain transfer function as:

$$G_c(z) = K_P + \frac{K_I T_s z}{z-1} = K_P + \frac{K_I' z}{z-1} = 0.685 + \frac{0.018z}{z-1}. \tag{3-64}$$

According to $G_c(z)$, the control effort $v_c(k)$ can be computed using the following difference equation:

$$v_c(k) = K_P e(k) + K_I' \sum_{j=0}^{k} e(j) = 0.685e(k) + 0.018\sum_{j=0}^{k} e(j), \tag{3-65}$$

where $e(k)$ is the error signal which is computed digitally by:

$$e(k) = V_{ref}(k) - V_o(k), \tag{3-66}$$

where $V_o(k)$ is the ADC result of the output voltage, and $V_{ref}(k)$ is the voltage reference, $V_{ref}(k)$ is fixed at 7Fh and represents a fixed nominal output voltage.

Because of the limited computation capacity of the microcontroller, power-of-two arithmetic was employed, that is, either of K_P and K_I' must be a power-of-two number. Thus, multiplication/division can be done by simply shifting resister bits left/right. In order to ensure proper margin, K_P should not be larger than the calculated value. In this implementation, K_P = 1/8, K_I' = 1/256 were selected, where the zero is at 777 Hz.

The PIC16C782 microcontroller does have a sign bit, so the software must keep track of the sign. In this implementation, the sign of *e(k)* is stored in the flag bit, so the proportional term and the integral term are computed without considering their signs, and every possible sign combination has a separate code path to compute the control effort. Though this method increases the size and structure complexity of the code considerably, the calculation time is reduced and calculations in each code path are simplified.

As stated earlier, a level-shift circuit was designed such that the 8-bit ADC result represented a "windowed" range of the output voltage around its nominal value. An external voltage follower was needed to ensure accurate measurement of the output voltage. Because of the limited sampling rate and computation power of the PIC16C782, switching noise in the output voltage must be avoided or filtered out in hardware. In this implementation, the PWM signal was sent back to another I/O pin to trigger an interrupt that started an analog-to-digital conversion. As a result, the output voltage can always be captured at a fixed point in the switching cycle after the switching noise has subsided.

3.3.5 Multiplying Digital-to-Analog Converter

The on-board DAC module of the PIC16C782 was used to convert the digital value from a PI controller to an analog signal. The operation of the DAC can be expressed as:

$$V_a = V_{DAC} \times V_d \,, \tag{3-67}$$

where V_d is the digital value of the DAC input, V_{DAC} is the voltage reference of the DAC, and V_a is analog value of the DAC output. For the PIC16C782 microcontroller, the reference voltage V_{DAC} may be supplied by one of the three sources: the power supply of

the microcontroller, the on-board bandgap voltage reference (3.072 V), or the comparator C_1 reference pin. In this implementation, the DAC reference voltage was set to be the voltage at the comparator C_1 reference pin. Connecting this pin to the voltage divider at the output of the rectifier, the reference voltage of the DAC becomes a scaled replica of the rectified input voltage. This operation is expressed in (3-67) where a scaled replica of the input voltage is scaled by the digital control voltage.

In order to ensure accuracy, the output of the voltage divider for the rectified input voltage should be as high as possible. Because the input voltage peak is 170 V at nominal conditions and the power supply of the microcontroller is 5 V, the voltage divider is designed to satisfy the condition that its output is 4.5 V when V_{in} is 170 V.

Meanwhile, it is desired that the current sense resistor R_s should be big enough to provide adequate linear gain so that the current signal is compatible with the analog control voltage from the DAC. However, in order to ensure efficiency of the power stage, the sense resistor has to be as small as possible. As a result, sensed current signal may be too small to be compatible with the analog control voltage from the DAC. This incompatibility seriously reduces the DAC resolution and results in output voltage ripple. One solution to improve the DAC resolution is to add a simple voltage divider made of two external resistors at the DAC output, as has been depicted in Fig. 3.9. The insertion of the voltage divider is equivalent to introducing a constant gain in the current loop.

3.4 Experimental Results

For the laboratory prototype, the nominal input voltage (RMS) was 120 V, the nominal output was 207 V, and the nominal load was 100 W. The measured value of the inductor was 1.56 mH, the output capacitor value was 560 μF, and the sense resistor was

0.1 Ω. The boost converter operated in the continuous conduction mode when the switching frequency was 156.25 kHz. The controller sampling frequency was 52 kHz (or 19.2 μs), while the PIC16C782 operated at 20 MHz. The gains of the digital PI controller were K_P = 1/8 and K_I = 1/256. The system diagram for the microcontroller-based hybrid PFC preregulator is shown in Fig. 3.16.

The circuit in Fig. 3.16 has been constructed and tested in the laboratory. All experimental results were captured with a TDS 7054 oscilloscope using the average acquisition mode where 16 waveforms were averaged for the display. In addition, the TDSPWR2 (Power Analysis Measurements Package) software from Tektronix was utilized to calculate total harmonic distortion (THD) and power factor. The RMS value of the input voltage was varied over a wide range of 80 V to 140 V. The load was varied between 50 and 300 W. Under these variable conditions, the output DC voltage of the single-phase PFC preregulator was maintained at 207 V.

The THD for the input current was calculated using following equation:

$$THD = \frac{\sqrt{I_2^2 + I_3^2 + ...I_n^2}}{I_1} \times 100\%, \tag{3-68}$$

where I_1 is the RMS value of the fundamental component of the input current, and I_2, I_3, ……I_n are the RMS values of the harmonic components of the input current. Harmonics through the 40th were included in the calculation of the THD. The power factor (*pf*) can be calculated by:

$$pf = True\ power\ /\ Apparent\ power, \tag{3-69}$$

Fig. 3.17 is a plot of the input voltage and current when the RMS value of the input voltage was 120 V and the load was 100 W. It can be seen from this figure that the

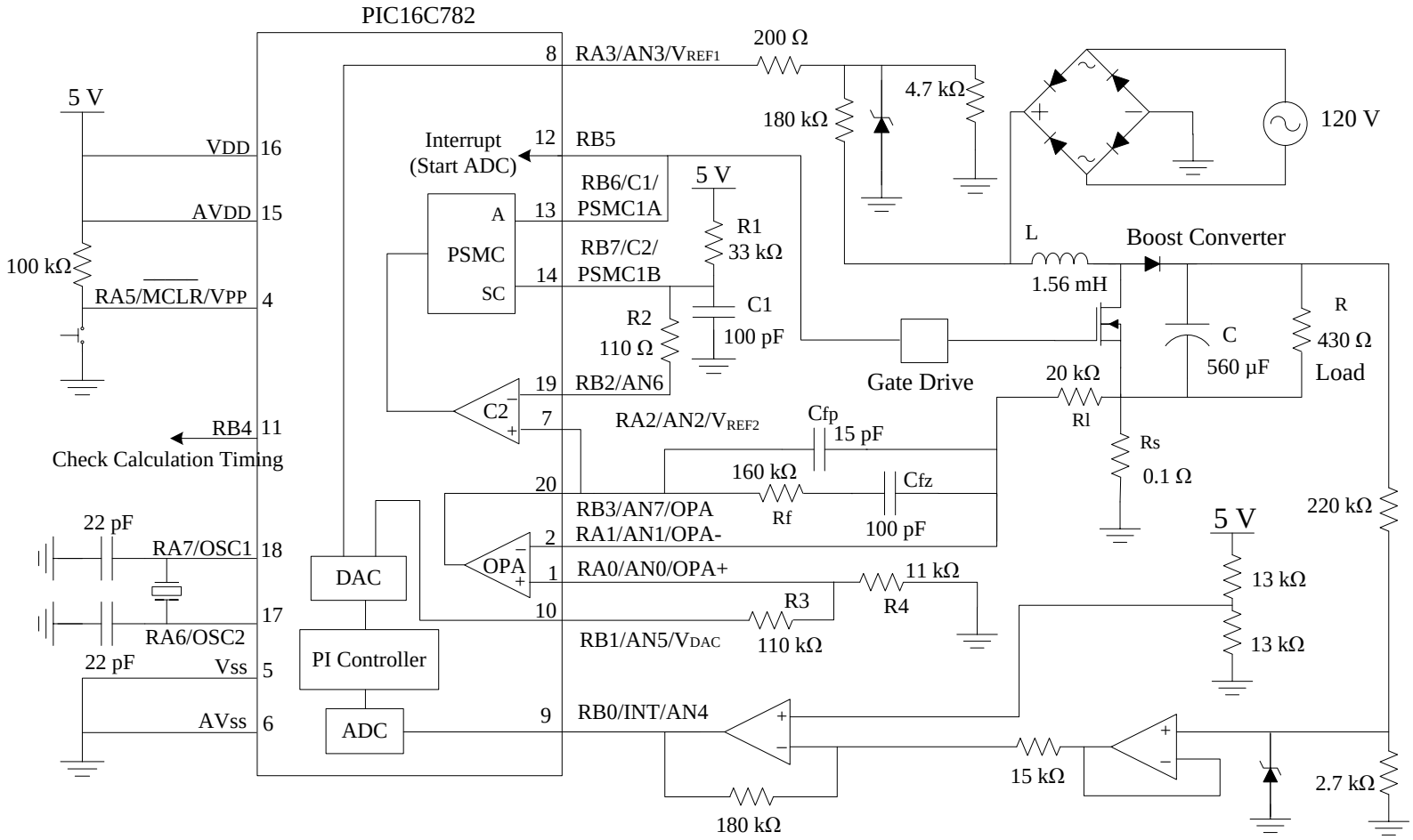


Fig. 3.16. Hybrid PFC preregulator controlled by a PIC16C782

input current was sinusoidal and very smooth with unnoticeable distortion. The phase difference between the input voltage and current, as measured by the oscilloscope, was only 1.976°. The calculated power factor was 0.9937. The measured THD of the input current was 5.9566%. At this time, the fundamental component dominates the current harmonics, as illustrated in Fig. 3.18 and Fig. 3.19.

Fig. 3.20 is a plot of the input voltage and the inductor current when the RMS value of the input voltage was 120 V and the load was 100 W. Fig. 3.20 shows that the inductor current is a rectified sinusoidal waveform in phase with the input voltage.

Fig. 3.21 and Fig. 3.22 contain plots of the input voltage and current versus time at different input voltages and loads. Slight distortion can be observed at the zero crossings of the current waveforms in both figures. The effect of variations in the input voltage and load power on the THD of the input current was also examined. The RMS value of the input voltage was varied between 120 V and 140 V, and the load was varied from 50 W to 300 W. The result of this examination is plotted in Fig. 3.23. Note that the input current THD varied between 3.1% and 16%, with the largest THD occurring at the lowest load level and the highest input voltage. The power factor and peak-to-peak output voltage ripple were also determined for the same range of input voltages and loads. As shown in Fig. 3.24, the power factor varied between 0.9843 and 0.9978. Variations in the peak-to-peak output voltage ripple with input voltage and load is plotted in Fig. 3.25. Note that the output ripple varied between 1.2% to 4.7% of the 207 V nominal output voltage. When the output load increased, the output voltage ripple is increased, and the output voltage ripple decreased when the output load decreased.

Fig. 3.26 summarizes the efficiency of the proposed system when operating at varies input voltages and different loads. It can be seen from Fig. 3.26 that the proposed PFC can achieve high efficiency of more than 96% at nominal operating condition. In most cases, the efficiency is high than 90%. The efficiency is lower than 90% only when the load is higher than 200 W and input voltage is lower than nominal voltage.

In conclusion, by using the on-board peripherals of a PIC16C782 microcontroller, a one-chip solution of a practical design for a microcontroller-based PFC preregulator has been achieved. The proposed PFC preregulator has demonstrated satisfactory experimental results. The power factor is above 0.99 for load power in excess of 100 W.

Experimental results also show that the PFC preregulator can operate satisfactorily over a wide range of input voltages and load powers. Because of the simplicity of the circuit, the proposed PFC preregulator has low cost and high reliability. This design has proven that it is possible to implement a high-performance PFC controller on a single microcontroller without using more expensive DSPs or other complicated hardware.

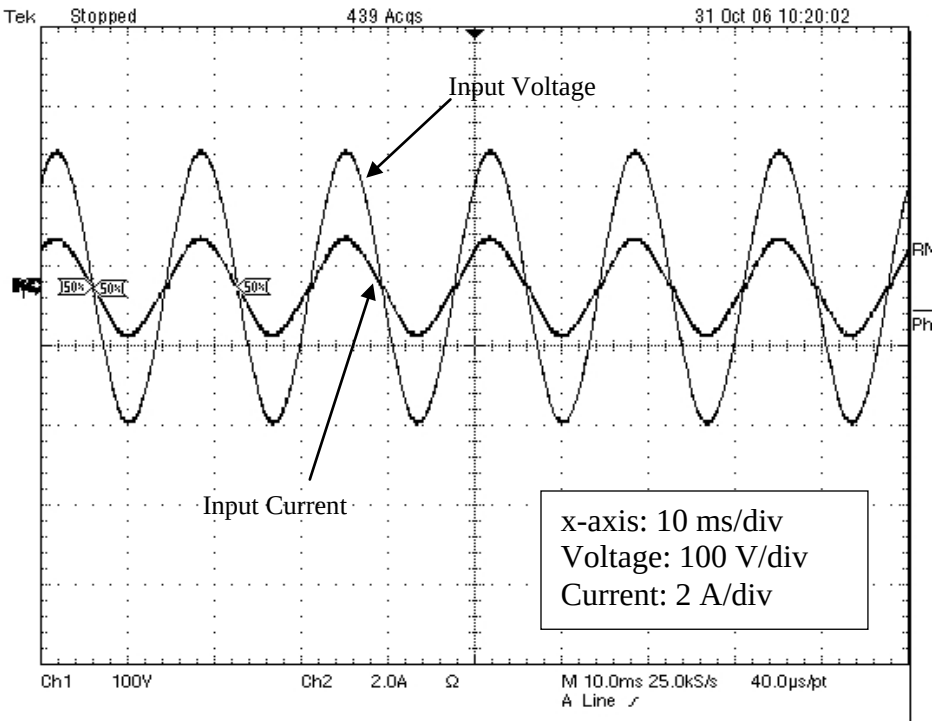


Fig. 3.17 Input voltage and current when V_{in} = 120 V and P_{load} = 100 W

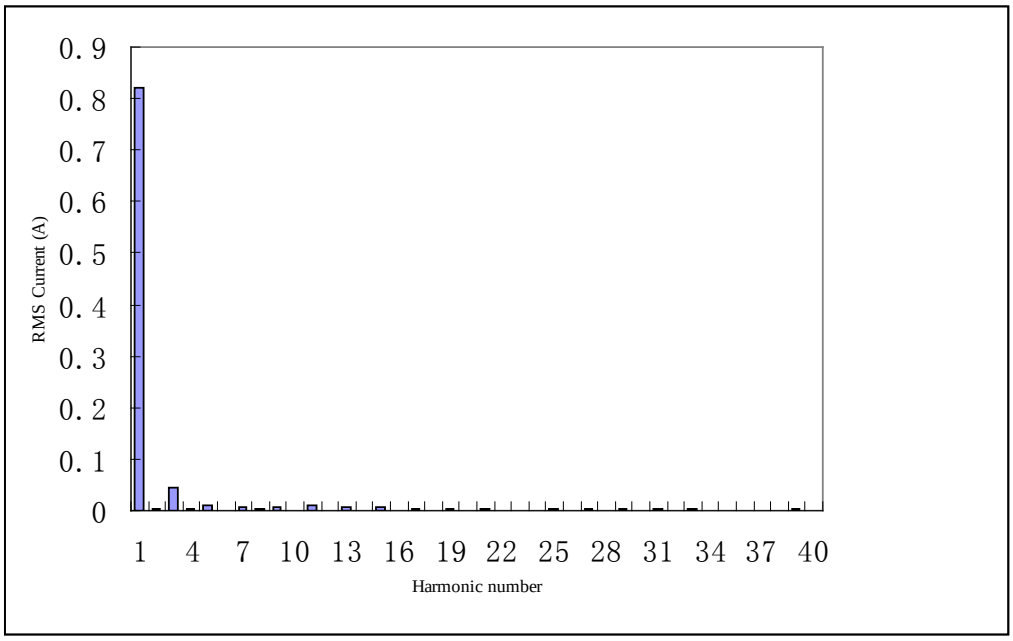


Fig. 3.18 Current harmonic spectrum when V_{in} = 120 V and P_{load} = 100 W

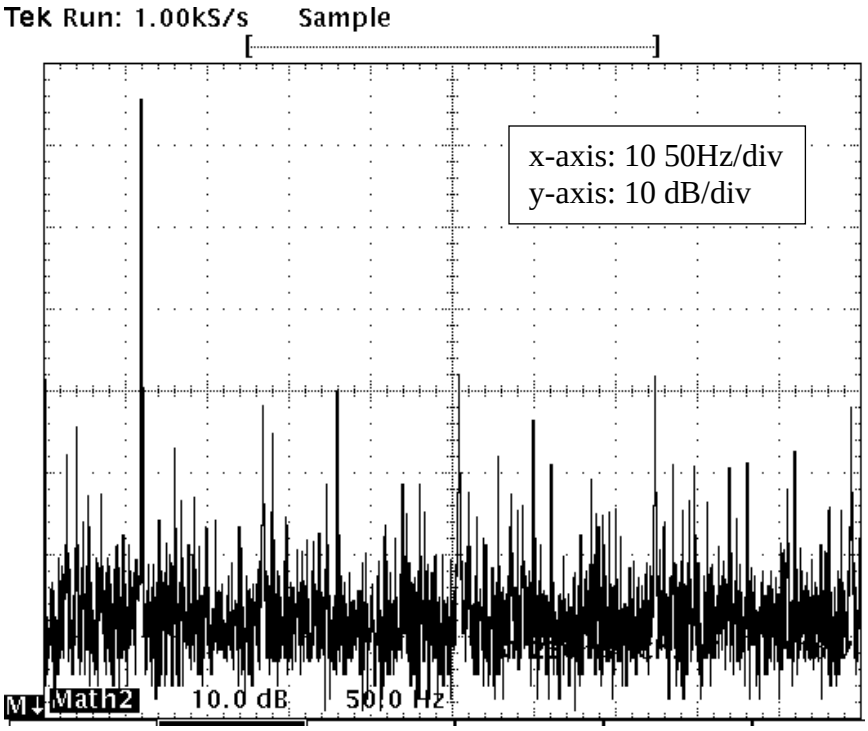


Fig. 3.19 Oscilloscope recorded current harmonic spectrum when V_{in} = 120 V and P_{load} = 100 W

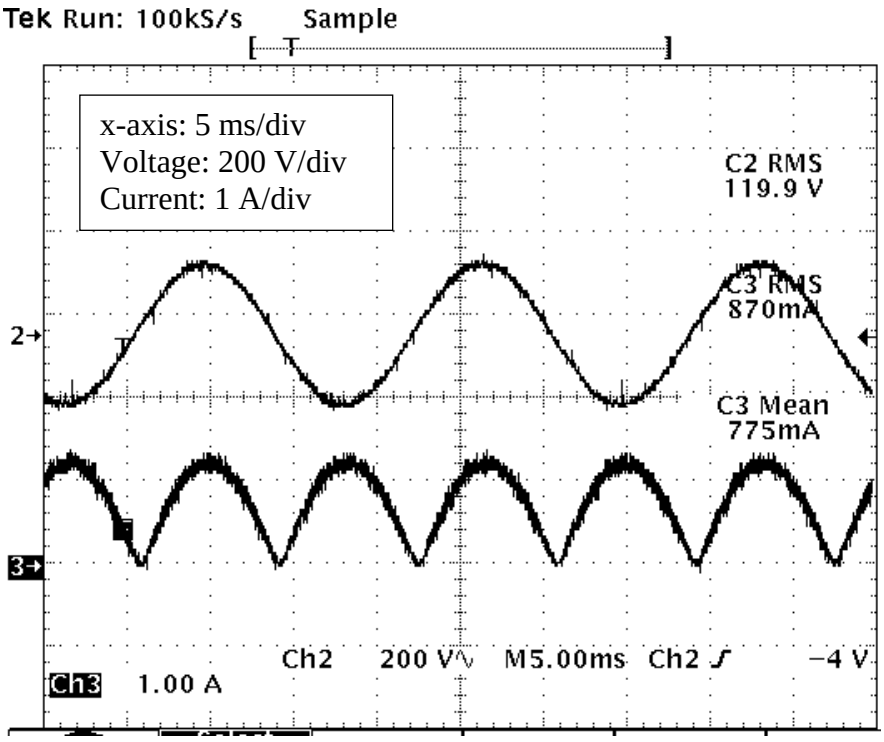


Fig. 3.20 Input voltage and rectified inductor current when V_{in} = 120 V and P_{load} = 100 W

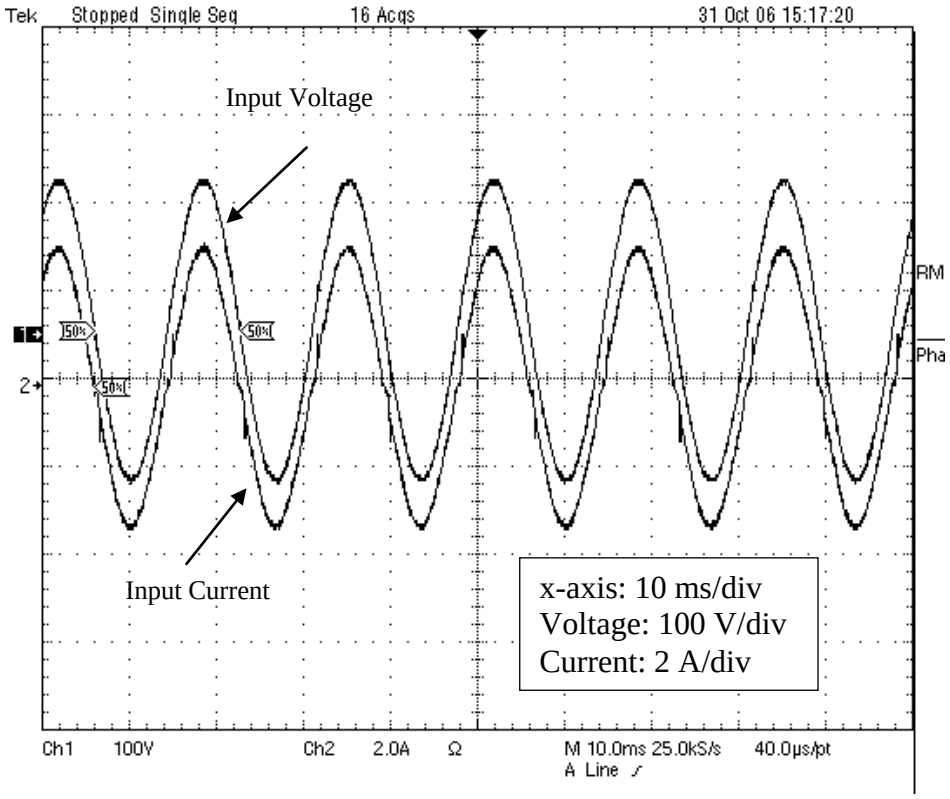


Fig. 3.21 Input voltage and current when V_{in} = 120 V and P_{load} = 250 W

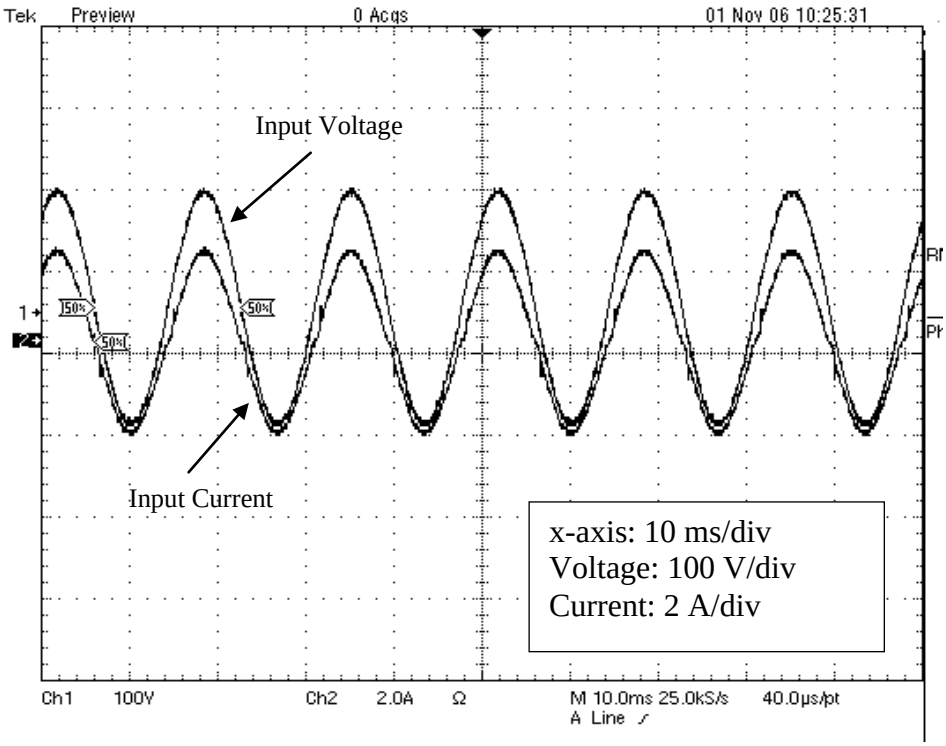


Fig. 3.22 Input voltage and current when V_{in} = 100 V and P_{load} = 150 W

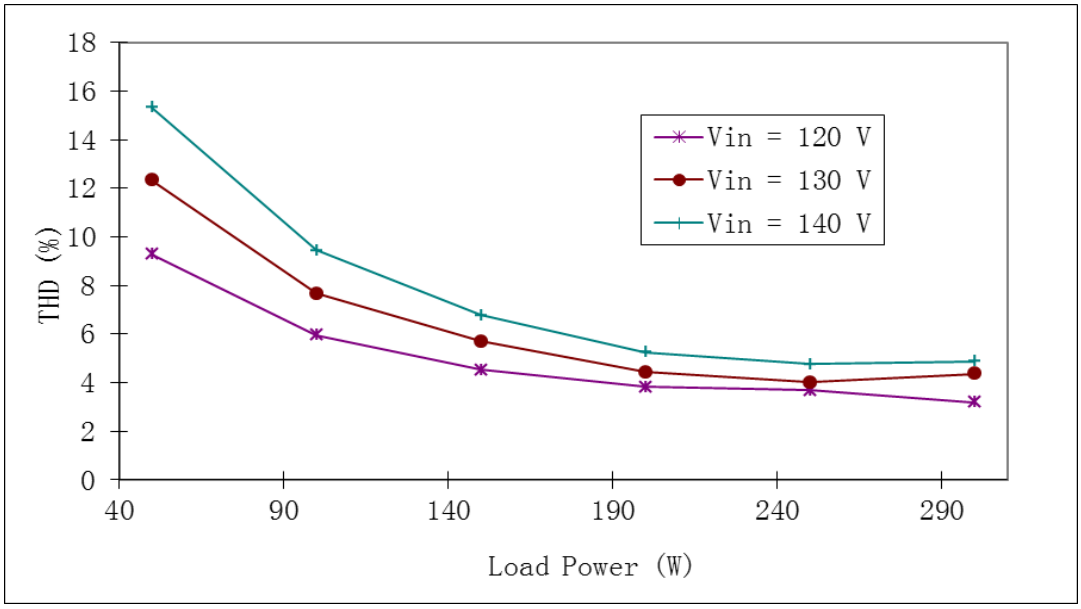


Fig. 3.23 Input current THD for different input voltages and loads

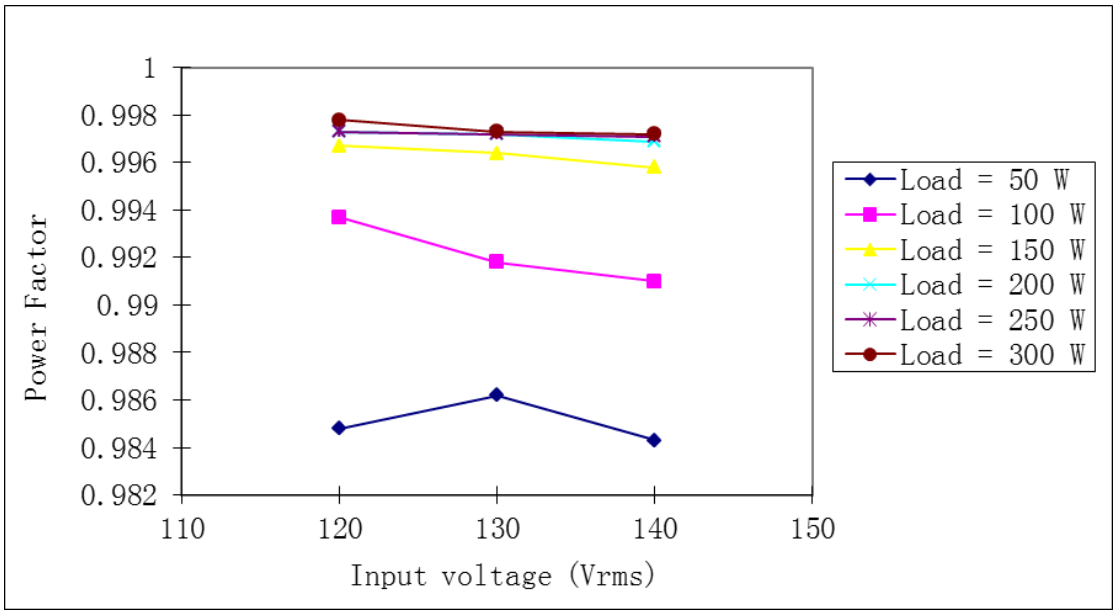


Fig. 3.24 Power factor varying with input voltage and load

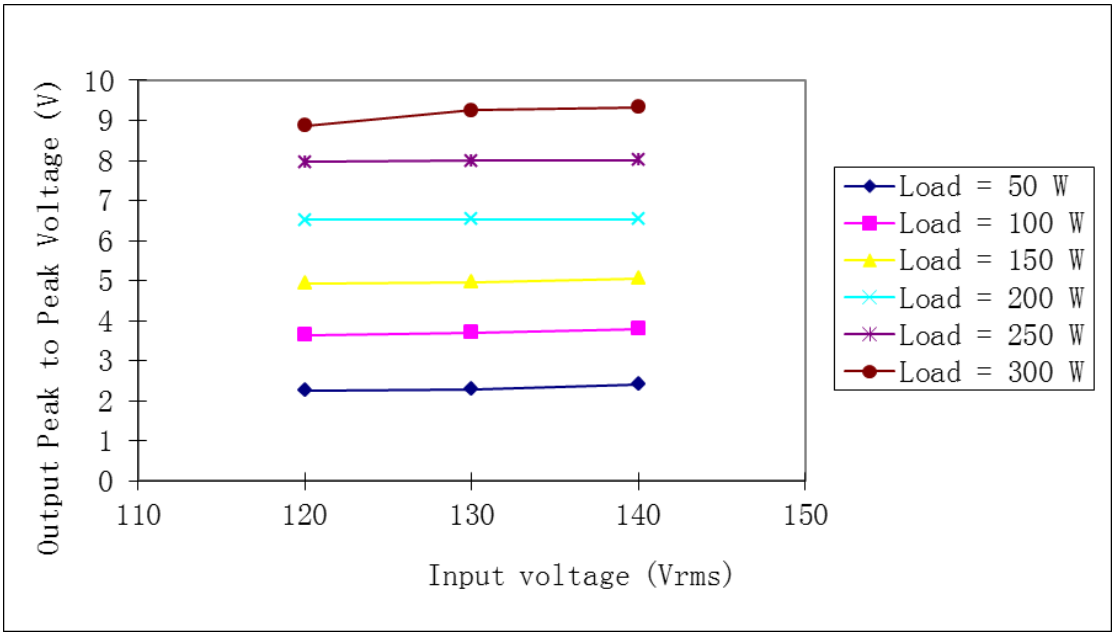


Fig. 3.25 Output voltage ripple varying with input voltage and load

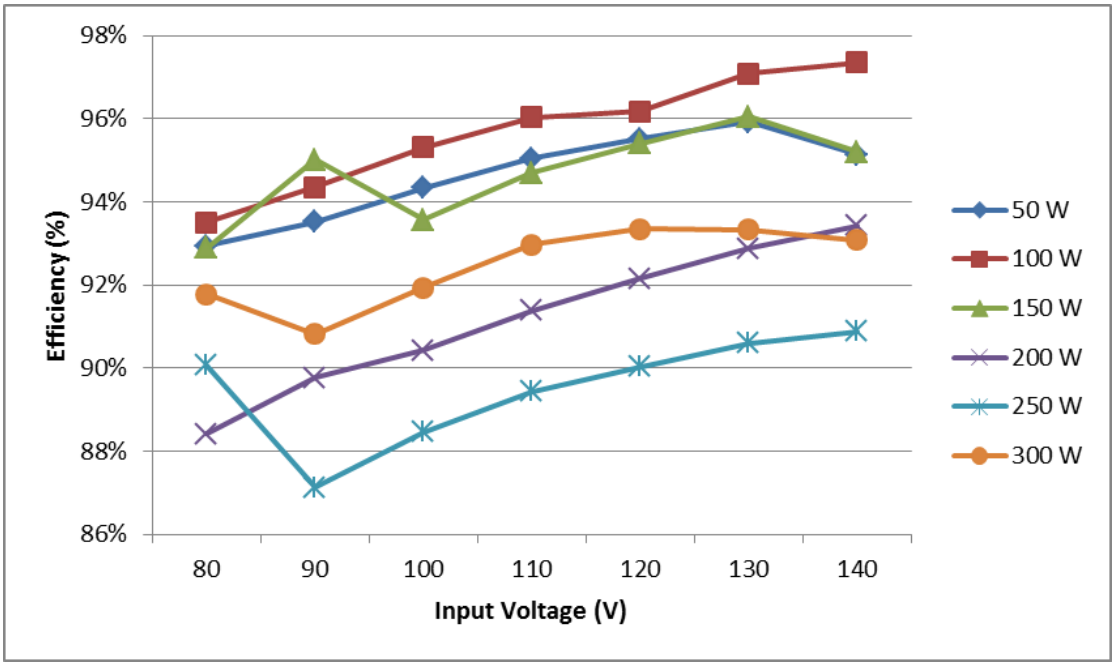


Fig. 3.26 Efficiency of the power stage varying with input voltage and load

CHAPTER 4

MICROCONTROLLER-BASED ACTIVE PFC WITHOUT INPUT VOLTAGE SENSING

This chapter presents a practical implementation of a single-phase PFC pre-regulator controlled by a single microcontroller without input voltage sensing. By extracting the waveform and phase information of the input voltage from the input current, input voltage sensing is eliminated, and a one-chip solution can be achieved, and has been verified by experimental results.

4.1 System Overview

In typical power factor correction (PFC) techniques, the output voltage, input current and input voltage are sensed. The outer voltage loop senses the output voltage and controls the amplitude of the input current. The input current is sensed, and then shaped through the current loop which utilizes the sinusoidal input voltage as a reference. Given the fact that the current inside the power stage is a function of the input voltage, input current shaping can be achieved by sensing the inductor current, switch current or diode current. As such, the need for input voltage sensing can be eliminated.

Microcontroller-based active PFC system without input voltage sensing employs similar system structure as the system with input voltage sensing, which also contains two control loops and is implemented in single microcontroller by using the hybrid

control technique. However, the reference of the multiplying DAC is no longer directly from sensing the input voltage. Instead, the reference of the DAC is obtained from the input current, which needs to be sensed to implement ACMC.

Employing similar hybrid approach, a hybrid PFC boost pre-regulator using a single PIC16C782 microcontroller has been implemented. The block diagram of this system is shown in Fig. 4.1. In this system, the analog current loop is combined with the digital voltage loop to construct a hybrid controller. A digital compensator is utilized in the voltage loop. The analog current loop controls the inductor current. The current reference for this current loop is obtained by multiplying the control voltage from the digital voltage loop and a scaled replica of the inductor current, and the input current is automatically shaped to a sinusoidal waveform like the input voltage. Variations in the input voltage and output load can be quickly reflected in the inductor current, so the

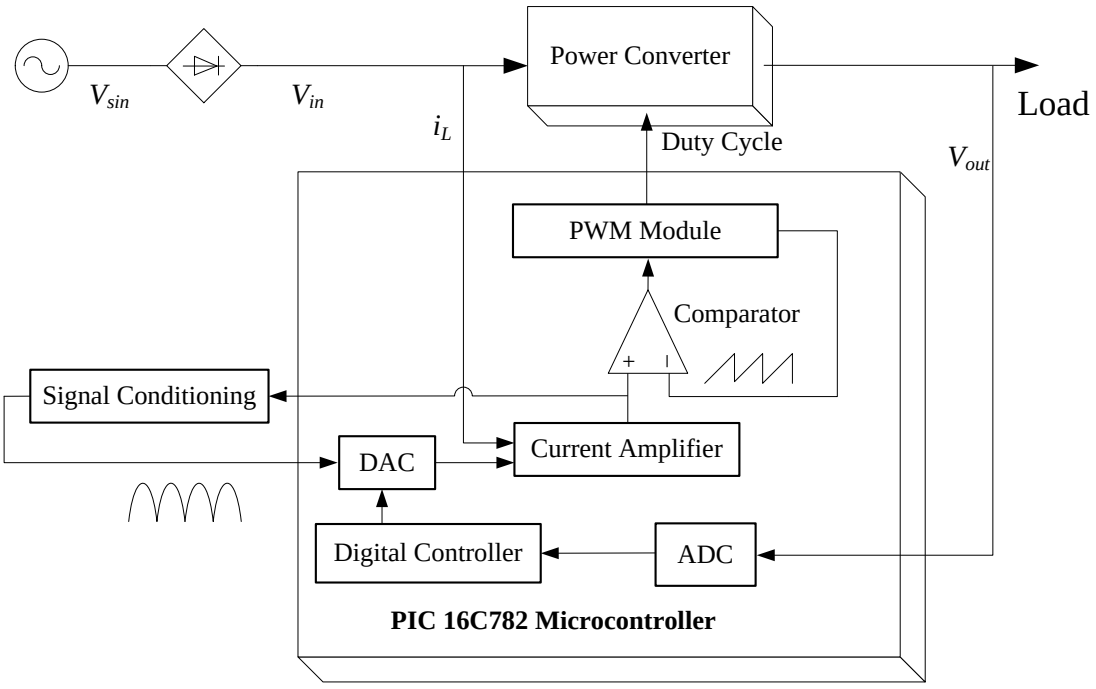


Fig. 4.1 Block diagram of a hybrid PFC pre-regulator controlled by a PIC16C782 microcontroller without input voltage sensing

power converter can operate satisfactorily over a wide range of input voltages and output loads as has been verified by experimental results.

The on-board DAC permitted the use of the multiplying DAC approach in this design. A scaled replica of the rectified inductor current was sent to the microcontroller, which is the reference for the on-board DAC. One extra op-amp was needed to condition the sensed inductor current before it can be used as the DAC reference. The other DAC input was determined by the digital voltage loop and was calculated internally using a digital proportional-integral (PI) controller.

4.2 Modeling Active PFC without Input Voltage Sensing

In Chapter 2, the small signal models of the ACMC system was investigated, and the results and similar approach are used to investigate and to derive the practical small signal model for PFC pre-regulators without input voltage sensing in this section.

As shown in Fig. 4.1, active PFC system without input voltage sensing does not sense the input voltage. Instead, the output of the current loop amplifier, which indeed is a replica of the inductor current, is sent back and multiplied with the control voltage, which is the output of the voltage loop compensator. An extra operational amplifier may need to be inserted into this loop to provide appropriate gain. As stated previously, the dynamics of the voltage loop are significantly slower than the current loop, and this extra operational amplifier can also be used to filter out high frequency signals.

Fig. 4.2 illustrates this additional operational amplifier inserted into the DAC reference feedback, where v_{CA} is the output of the current amplifier of the current loop, v_T is the output of the operational amplifier and is sent back to the microcontroller as the DAC reference. A voltage divider is constructed by R_3 and R_4 to provide an offset V_T to

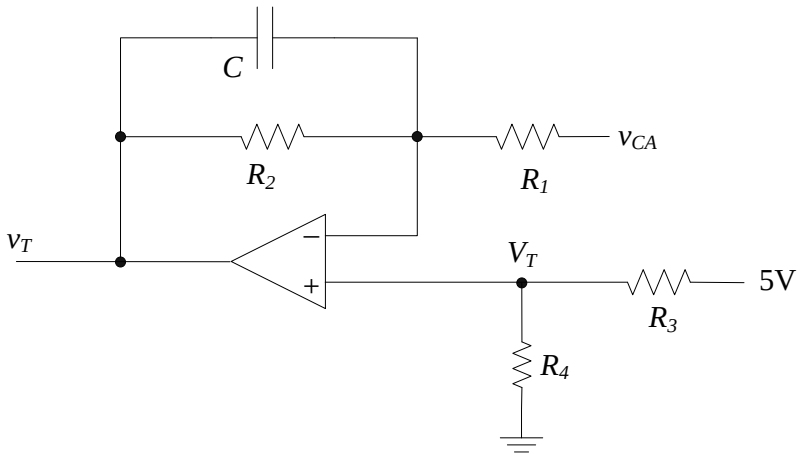


Fig. 4.2 Operational amplifier in DAC reference feedback loop

v_{CA} waveforms. This offset V_T adjusts the dc component in v_{CA}, and will be explained in details in section 4.3.4. This extra operational amplifier may not be necessary when current transformers are used to sense the inductor current, because the current transformer network can provide adequate gain. In this case, the sensed signal can be directly sent to the microcontroller as the DAC reference.

The system in Fig. 4.2 is indeed a first-order low-pass filter with appropriate dc gain. Its transfer function $G_T(s)$ can be expressed as:

$$G_T(s) = \frac{R_2}{R_1(1+R_2Cs)} = \frac{K_T}{1+\tau s}. \tag{4-1}$$

It can be seen from (4-1) that the DC gain K_T is set by R_1 and R_2, and the cut off frequency f_c of this low-pass filter is:

$$f_c = \frac{1}{2\pi R_2 C}. \tag{4-2}$$

According to the discussions in Chapter 2, the model of a PFC pre-regulator without input voltage sensing can be illustrated as in Fig. 4.3, where v_C is control voltage

of the current loop (output of the voltage loop), v_O is the output voltage of the power stage, i_L is the inductor current, d is the duty cycle that controls the switch of the power stage, R_i is the effective linear gain (volt/amp) from the inductor current to the input of the current loop compensator, K_s is the gain between the multiplier and current loop compensator (which is set by a voltage divider), v_{CA} is the output of the current amplifier, F_m is the modular gain, and V_T is the dc offset of the v_{CA} feedback, $G_{CA}(s)$ is the current loop amplifier, $G_T(s)$ is the feedback transfer function from the output of the current loop compensator to the multiplier, $G_{id}(s)$ is the duty-cycle to inductor current transfer function of the power stage, and $G_{vd}(s)$ the duty-cycle to output voltage transfer function of the power stage. This system borrows the ideas from the Sun and Bass's small signal model [7] as well as Cooke's small signal model [11] for ACMC converters. Based on the fact that the dynamics of the voltage loop are significantly slower than that of the current loop in an active PFC system, the accuracy of the model in the high frequency range is not a concern. Thus, it is reasonable to ignore the feed-forward gain and feedback gain, as well as the sampling effect, as shown in the model of Fig. 4.3.

Thus, it can be derived from Fig. 4.3 that:

$$v_{CA} = v_C(V_T - v_{CA})G_T(s)K_s\left(1+G_{CA}(s)\right) - v_{CA}F_mR_iG_{id}(s)G_{CA}(s)\,. \tag{4-3}$$

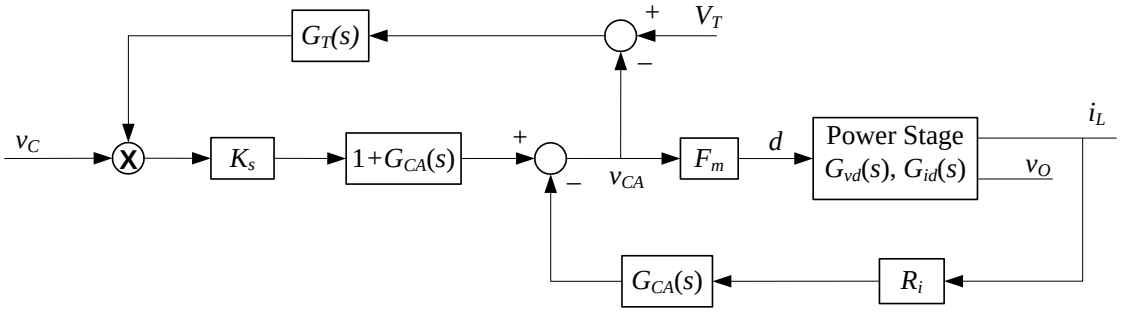


Fig. 4.3 Model for active PFC preregulator without input voltage sensing

Rearranging (4-3), we can get:

$$v_{CA} = \frac{v_C V_T K_s G_T(s)\left(1 + G_{CA}(s)\right)}{1 + v_C K_s G_T(s)\left(1 + G_{CA}(s)\right) + F_m R_i G_{CA}(s) G_{id}(s)}. \tag{4-4}$$

It can also be derived from Fig. 4.3 that:

$$v_O = v_{CA} F_m G_{vd}(s). \tag{4-5}$$

Substitute (4-4) into (4-5):

$$v_O = \frac{v_C V_T K_s F_m G_T(s) G_{vd}(s)\left(1 + G_{CA}(s)\right)}{1 + v_C K_s G_T(s)\left(1 + G_{CA}(s)\right) + F_m R_i G_{CA}(s) G_{id}(s)}. \tag{4-6}$$

Expanding (4-6), we get:

$$\begin{aligned} &v_O + v_O v_C K_s G_T(s)\left(1 + G_{CA}(s)\right) + v_O F_m R_i G_{CA}(s) G_{id}(s) \\ &= v_C V_T K_s F_m G_T(s) G_{vd}(s)\left(1 + G_{CA}(s)\right) \end{aligned}. \tag{4-7}$$

In (4-7), v_O can be expressed as the summation of the dc component V_O and its small signal perturbation $\hat{v}_o$, and v_C can be expressed as the summation of the dc component V_C and it small signal perturbation $\hat{v}_c$. Thus, (4-7) can be rewritten as:

$$\begin{aligned} &(V_O + \hat{v}_o) + (V_O + \hat{v}_o)(V_C + \hat{v}_c) K_s G_T(s)\left(1 + G_{CA}(s)\right) + (V_O + \hat{v}_o) F_m R_i G_{CA}(s) G_{id}(s) \\ &= (V_C + \hat{v}_c) V_T K_s F_m G_T(s) G_{vd}(s)\left(1 + G_{CA}(s)\right) \end{aligned}. \tag{4-8}$$

For small signal perturbations, we can assume that:

$$\hat{v}_o \hat{v}_c \approx 0. \tag{4-9}$$

Substituting (4-9) into (4-8) and then simplifying yields:

$$\begin{aligned} &\hat{v}_o + (\hat{v}_o V_C + \hat{v}_c V_O) K_s G_T(s)\left(1 + G_{CA}(s)\right) + \hat{v}_o F_m R_i G_{CA}(s) G_{id}(s) \\ &= \hat{v}_c V_T K_s F_m G_T(s) G_{vd}(s)\left(1 + G_{CA}(s)\right) \end{aligned}. \tag{4-10}$$

Thus, the control-to-output transfer function $G_{vc}(s)$ can be expressed as:

$$G_{vc}(s)=\frac{\hat{v}_o}{\hat{v}_c}=\frac{K_s G_T(s)\left(V_T F_m G_{vd}(s)-V_O\right)\left(1+G_{CA}(s)\right)}{1+V_C K_s G_T(s)\left(1+G_{CA}(s)\right)+F_m R_i G_{id}(s) G_{CA}(s)}. \tag{4-11}$$

In (4-11), F_m is the modular gain that can be calculated by (2-1), where F_m is simply the reciprocal of V_m, the peak-to-peak voltage of the ramp signal at the comparator of the current loop. The output voltage of the power stage V_O is defined by the design and is a fixed known value. In this implementation, V_O is 202 V.

The dc value of the control signal V_C is a fixed value during normal operation, and can be computed. Rearranging (4-3), the following equation can be obtained:

$$v_C=\frac{v_{CA}\left(1+F_m R_i G_{id}(s) G_{CA}(s)\right)}{K_s G_T(s)\left(1+G_{CA}(s)\right)\left(V_T-v_{CA}\right)}. \tag{4-12}$$

According to (4-1), the dc gain of $G_T(s)$ is K_T, which can be computed by:

$$K_T=\frac{R_2}{R_1}, \tag{4-13}$$

where R_1 and R_2 are the resistor values of the low pass filter defined in Fig. 4.2.

According to (3-37), the dc gain of $G_{CA}(s)$ is K_c, which can be computed by:

$$K_c=\frac{1}{R_l\left(C_{fp}+C_{fz}\right)}, \tag{4-14}$$

where R_l, C_{fp} and C_{fz} are components of the current amplifier defined in Fig. 2.2.

According to (1-20), the dc gain of $G_{id}(s)$ can be obtained:

$$G_{id}(s)\big|_{s=0}=\frac{2V_O^3}{R_L V_{in}^2}, \tag{4-15}$$

The dc component of v_{CA}, V_{CA}, can be computed by:

$$V_{CA} = \frac{D}{F_m}. \tag{4-16}$$

where D is the duty cycle of the power stage.

According to (4-12), the dc component of v_C, V_C, can be computed:

$$V_C = \frac{\frac{D}{F_m}\left(1 + F_m R_i K_c \frac{2V_O^3}{R_L V_{in}^2}\right)}{K_s K_T (1 + K_c)\left(V_T - \frac{D}{F_m}\right)} = \frac{D\left(R_L V_{in}^2 + 2F_m R_i K_c V_O^3\right)}{K_s K_T R_L V_{in}^2 (1 + K_c)(F_m V_T - D)}. \tag{4-17}$$

It can be seen from (4-17) that V_C can be computed through known constants.

Although the model in (4-11) ignores feed-forward gain and feedback gains as well as the sampling effect, it is still accurate for the PFC pre-regulator because of the fact that the cutoff frequency of the outer voltage loop is considerably lower than 120 Hz, and is far below the switching frequency and the cutoff frequency of the inner current loop.

4.3 System Design

4.3.1 Power Stage Design

In this research, a boost converter is selected in the design. For comparison, the power stage is identical to the power stage in Chapter 3, where an active PFC system with input voltage sensing is investigated. In both systems, output capacitor C_o is selected to be 560 μF, the inductor value is 1.56 mH, switching frequency is set to 156.25 kHz. In order to increase the signal-noise ratio, a 0.3 Ω sense resistor is selected in the design. The maximum duty cycle is set to 3/4. For laboratory prototype, the nominal

input voltage (RMS) is 120 V, the nominal output was 202 V, and the nominal load is 100 W, and the maximum power output is 300 W.

4.3.2 Current Loop Design

The current loop design process for the active PFC system without input voltage sensing is very similar to that with input voltage sensing, as was described in Chapter 3. In this implementation, the current sense resistor R_s is selected to be 0.3 Ω to compromise the requirements of low power loss and adequate signal-to-noise ratio.

As in Chapter 3, the current compensator in the current loop is designed by using the on-board analog operational amplifier module (OPA module) on the PIC16C782 microcontroller with several external capacitors and resistors. The complete current loop realized has been shown in Fig. 3.6.

The design of the current loop compensator starts from selecting R_f and R_l:

$$\frac{R_f}{R_l} \le G_{CA\max} = \frac{V_m f_s L}{V_o R_i} = \frac{3\times 156.25\times 10^3 \times 1.56\times 10^{-3}}{202\times 0.3} = 120.66. \qquad (4\text{-}18)$$

Select R_f = 160 kΩ and R_l = 20 kΩ, so $\frac{R_f}{R_l} = 8$, which satisfies the requirement in (4-8) that $\frac{R_f}{R_l} \le 120.66$.

As long as R_f and R_l have been selected, the identical approach as Chapter 3 is employed to compute C_{fz} and C_{fp}. In this research, C_{fz} is selected 100 pF, and C_{fp} is selected 15 pF, which are identical to the values of the current loop compensator in Chapter 3. Thus, according (4-14), K_c, the dc gain of $G_{CA}(s)$, can be computed to be 4.35×10^5.

Also, as already shown in Fig. 3.9, the D/A output is scaled down through a voltage divider with identical ratio K_s as in Chapter 3:

$$K_s = \frac{R_2}{R_1 + R_2} = \frac{11\text{k}}{110\text{k} + 11\text{k}} = \frac{1}{11}. \tag{4-19}$$

Similarly, the design process of the RC network to generate the saw-tooth signal v_m is identical to that of Chapter 3, and C = 100 pF and R = 33 kΩ are selected in this implementation. Based on experimental measurements and (3-49), V_m, the equivalent peak value of v_m, is 4.6 V.

4.3.3 Multiplying Digital-to-Analog Converter

In this implementation, the on-board DAC module of the PIC16C782 is used to convert the digital value from a PI controller to an analog signal. The DAC reference voltage V_{DAC} was set to be the voltage at the comparator C_1 reference pin. Connecting this pin to the output of the current loop compensator through a low-pass filter $G_T(s)$, the reference voltage of the DAC reflects the low frequency portion of the sensed current signal, which indeed is a scaled replica of the rectified sinusoidal input voltage. Although the reference of the current loop compensator is from the voltage loop, the influence of the dc output voltage can be neglected because of the significantly lower cutoff frequency of the voltage loop.

The low-pass filter $G_T(s)$ in the DAC reference loop abstracts the 60 Hz sinusoidal waveform from the inductor current information. Therefore, only the 60 Hz low frequency is our interest, and the high frequency dynamics, such as switching noise, in the current loop should be filtered out. In order to obtain fast response at 60 Hz, the low-pass filter $G_T(s)$ should have a cutoff frequency f_c higher than one decade of 60 Hz.

Meanwhile, in order to filter out the switching frequency, the cutoff frequency f_c of the low-pass filter $G_T(s)$ should be at least one decade below the switching frequency of 156.25 kHz.

The dc gain of $G_T(s)$, K_T, needs to be carefully selected such that the DAC reference feedback is in the range of 0 to 5 V. It can be seen from (4-11) that the dc gain of K_T has a direct impact on the dc gain of the control-to-output transfer function $G_{vc}(s)$. Fortunately, the overall dc gain can be adjusted when designing the voltage loop compensator. Therefore, the selection of K_T has some flexibility, as long as the DAC reference is in the appropriate range. Referring to the system in Fig. 4.2, in this implementation, C = 1 nF, R_1 = 10 kΩ and R_2 = 20 kΩ. According to (4-1), K_T = 2, f_c = 8 kHz, and $G_T(s)$ can be expressed as:

$$G_T(s) = \frac{K_T}{1+\tau s} = \frac{2}{1+2\times 10^{-5} s}. \tag{4-20}$$

In order to be compatible with the sensed current while maintaining resolution, the DAC output is scaled down by a voltage divider, as has shown in Fig. 3.9.

4.3.4 Voltage Loop Design

The control-to-output transfer function $G_{vc}(s)$ described in (4-11) can be used to design the voltage loop compensator $G_c(s)$. The resulting system structure is identical to that shown in Fig. 3.12. Similarly, a method combining the emulation method and the direct digital design method is used in this implementation.

It can be seen from (4-11) that $G_{vc}(s)$ is a function of $G_T(s)$, $G_{vd}(s)$ and $G_{id}(s)$. It can be seen from (4-17) that V_C will be affected by input voltage and load. At nominal operation condition:

$$D = \frac{V_O - V_{in}}{V_O} = \frac{202 - 120}{202} = 0.406 . \quad (4\text{-}21)$$

The full range of v_{CA} shall be from 0 to V_m, where V_m is peak value of the sawtooth signal at the comparator input. When v_{CA} is higher than V_m, D has reached its maximum value. Therefore, the dc offset of v_{CA}, V_T, shall be set to half of the V_m, which is the center of effective operation range of v_{CA}. That is:

$$V_T = \frac{1}{2} V_m . \quad (4\text{-}22)$$

At nominal operating conditions, the output power is 100 W, which corresponds to a load of 408.04 Ω. Substitute all the known parameters into (4-17):

$$V_C = \frac{0.406 \times \left(408.04 \times 120^2 + 2 \times \frac{1}{4.6} \times 0.3 \times 4.35 \times 10^5 \times 202^3 \right)}{\frac{1}{11} \times 2 \times 408.04 \times 120^2 \times \left(1 + 4.35 \times 10^5\right) \times \left(0.5 - 0.406\right)} = 4.34 \text{ V} . \quad (4\text{-}23)$$

Substitute (4-21) ~ (4-23) into (4-11):

$$G_{vc}(s) = \frac{\hat{v}_o}{\hat{v}_c} = \frac{\left(0.5 G_{vd}(s) - 202\right) G_T(s) \left(1 + G_{CA}(s)\right)}{11 + 4.34 G_T(s) \left(1 + G_{CA}(s)\right) + 0.7174 G_{CA}(s) G_{id}(s)} . \quad (4\text{-}24)$$

According to (3-3), the control-to-inductor-current transfer function of the boost converter $G_{id}(s)$ can be computed as:

$$G_{id}(s) = \frac{1.295 \times 10^5}{s} . \quad (4\text{-}25)$$

Also, according to (3-4), the control-to-output transfer function of the boost converter $G_{vd}(s)$ can be obtained:

$$G_{vd}(s) = \frac{1.488 \times 10^3 (s - 9.235 \times 10^4)}{s^2}. \quad (4\text{-}26)$$

Substituting (4-21), (4-25) and (4-26) into (4-24), the control-to-output transfer function $G_{vc}(s)$ can be computed. Fig. 4.4 illustrates the Bode Plot of the resulting control-to-output transfer function $G_{vc}(s)$ of the proposed system.

Using the zero-order hold (ZOH) method, as described in Chapter 3, the discrete-time model $G_{vc}(z)$ can be obtained from the continuous-time model $G_{vc}(s)$ using (3-51). Considering the time delay due to calculation, which is approximately equal to the sampling period, $G_{vc}(s)$ is mapped to $G_{vc}^{'}(z)$, and can be calculated using (3-52). In this

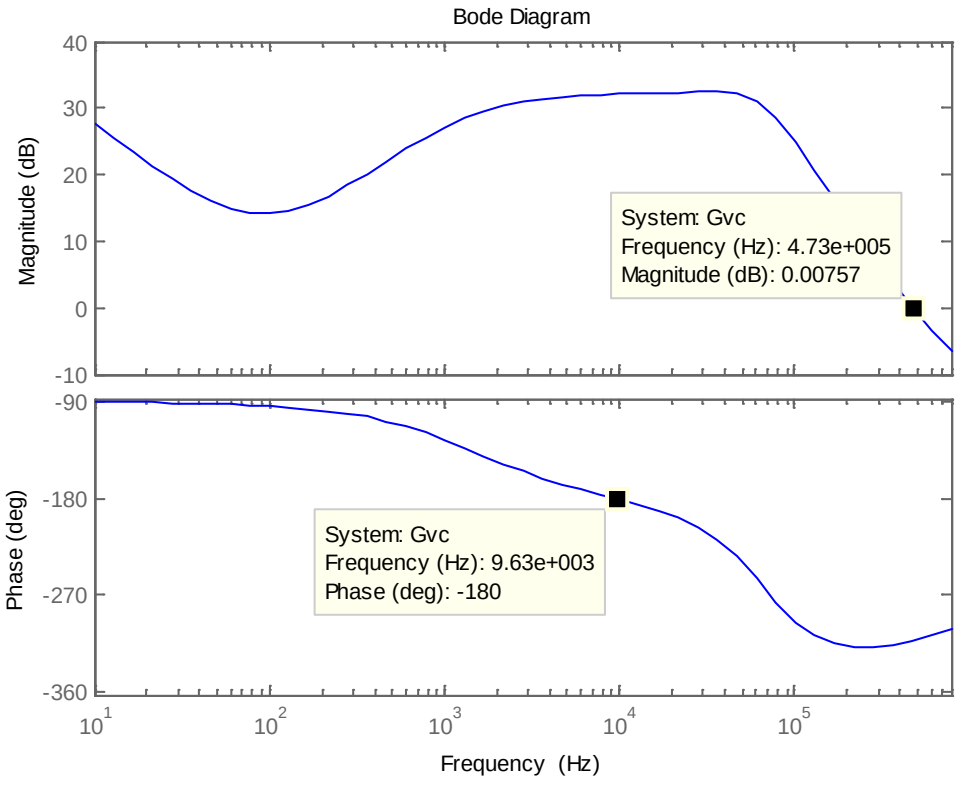


Fig. 4.4 Bode plot of *s*-domain control-to-output transfer function of the PFC pre-regulator

implementation, the time delay is approximately three times the switching period (6.4 μs), so 19.2 μs is used as the controller sampling period.

The Bode Plot of $G_{vc}(s)$, $G_{vc}(z)$ and $G_{vc}^{'}(z)$ can be obtained easily using MATLAB. Bode plots of $G_{vc}(s)$, $G_{vc}(z)$ and $G_{vc}^{'}(z)$ are illustrated in Fig. 4.5, where the transformation $z = e^{j\omega T}$ is used to map the unit circle to the real frequency axis. Fig. 4.5 indicates that the ZOH and controller time delay introduce considerable phase delay at high frequency when mapping the system from the *s*-plane to the *z*-plane. Therefore, $G_{vc}^{'}(z)$ should be used to design the voltage loop compensator.

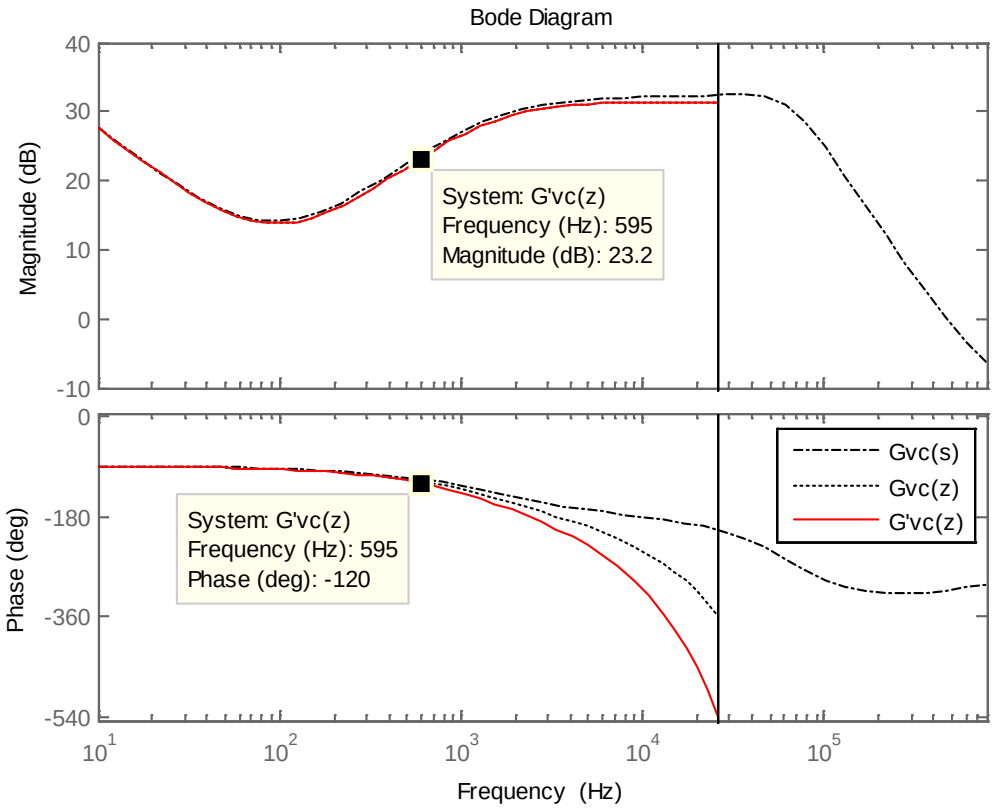


Fig. 4.5 Bode plot of control-to-output transfer function of the PFC pre-regulator

Notice that the Bode plot of $G_{vc}^{'}(z)$ is indeed obtained from mapping $G_{vc}^{'}(z)$ to $G_{vc}^{'}(s)$ in the *s*-domain using $z=e^{sT}$. The difference between $G_{vc}^{'}(s)$ and $G_{vc}(s)$ is that the ZOH and time delay are included in $G_{vc}^{'}(s)$, so $G_{vc}^{'}(s)$ is more accurate for design purposes, and is used to design the controller.

A PI controller has been used as the voltage loop compensator in the PFC pre-regulator without input voltage sensing. A similar method in Chapter 3 was used to design the voltage loop compensator, where the PI controller is designed in the *s*-domain using the Bode plot of $G_{vc}^{'}(s)$. Equation (3-56) is used to determine K_P, and Equation (3-57) is used to determine K_I, and then this PI controller in *s*-domain is converted to *z*-domain, such that the control effort $v_c(k)$ can be computed accordingly.

Set the phase margin φ_m to 55°， so ω_1, which is the frequency when the phase of $G_{vc}^{'}(j\omega_1)$ equals –(180° – φ_m – 5°) = –120°, is 595 Hz, or 3.74×10^3 rad/s, corresponding to a magnitude of 23.2 dB. Substitute $\left|H_v G_{vc}^{'}(j\omega_1)\right| = 23.2$ dB into (3-56), proportional gain K_p of the PI controller can be obtained:

$$K_P = \frac{1}{\left|H_v G_{vc}^{'}(j\omega_1)\right|} = \frac{1}{10^{23.2/20}} = 0.0691. \tag{4-27}$$

Thus, the integral gain K_I of the PI controller can be computed according to (3-57),

$$K_I = 0.1\omega_1 K_P = 0.1\times 3.74\times10^3 \times 0.0691 = 25.84. \tag{4-28}$$

Hence, the zero ω_0 of the PI controller is:

$$\omega_0 = \frac{K_I}{K_p} = \frac{25.84}{0.0691} = 374 \text{ rad/s}. \tag{4-29}$$

The voltage loop compensator can be expressed in the s-domain by:

$$G_c(s) = K_p + \frac{K_I}{s} = 0.0691 + \frac{25.84}{s}. \tag{4-30}$$

In this implementation, the output voltage of the power stage feeds back to the voltage loop compensator through a voltage divider and voltage-level-shift network, as already shown in Fig. 3.11, which introduces two extra gains to the voltage loop. Accordingly, the voltage loop compensator needs to consider these extra gains. Assuming the gain of the voltage divider is K_{div} (0.012124 in this implementation) and the gain of the voltage-level-shift network is K_{shft} (12 in this implementation), then the voltage loop compensator in the s-domain can be expressed as:

$$G_c(s) = \frac{1}{K_{div}K_{shft}}\left(K_p + \frac{K_I}{s}\right) = \frac{0.0691 + \frac{25.84}{s}}{0.012124 \times 12} = 0.4755 + \frac{177.61}{s}. \tag{4-31}$$

In this implementation, the sampling period is 3 times of switching period, or 19.2 μs. Using the backward rule, the *s*-domain PI controller is then converted to a *z*-domain transfer function as:

$$G_c(z) = K_P + \frac{K_I T_s z}{z-1} = K_P + \frac{K_I' z}{z-1} = 0.4755 + \frac{0.00341z}{z-1}. \tag{4-32}$$

Because of the limited computation capacity of the microcontroller, power-of-two arithmetic was employed. In order to ensure proper margin, K_P should be smaller than the calculated value. In this implementation, K_P = 1/4, K_I' = 1/256 were selected, where the zero is at 188.44 Hz.

According to $G_c(z)$, the control effort $v_c(k)$ can be computed using the following difference equation:

$$v_c(k) = K_P e(k) + K_I' \sum_{j=0}^{k} e(j) = \frac{1}{4} e(k) + \frac{1}{256} \sum_{j=0}^{k} e(j), \tag{4-33}$$

where $e(k)$ is the error signal which is computed digitally by:

$$e(k) = V_{ref}(k) - V_o(k), \tag{4-34}$$

where $V_o(k)$ is the ADC result of the output voltage, and $V_{ref}(k)$ is the voltage reference, $V_{ref}(k)$ is fixed at 7Fh and represents a fixed nominal output voltage.

The programming techniques used in Chapter 3 was also utilized in this implementation. In order to reduce the calculation time, the sign of $e(k)$ is stored in the flag bit, so the proportional term and the integral term are computed without considering their signs, and every possible sign combination has a separate code path to compute the control effort. Also, the PWM signal was sent back to another I/O pin to trigger an interrupt that started an analog-to-digital conversion, such that the output voltage can always be captured at a fixed point in the switching cycle after the switching noise has subsided.

4.4 Experimental Results

For the laboratory prototype, the nominal input voltage (RMS) was 120 V, the nominal output is 202 V, and the nominal load is 100 W. The measured value of the inductor was 1.56 mH, the output capacitor value was 560 μF, and the sense resistor was 0.3 Ω. The boost converter operated in the continuous conduction mode when the switching frequency was 156.25 kHz. The controller sampling frequency is 52 kHz (or

19.2 μs), while the PIC16C782 operated at 20 MHz. The gains of the digital PI controller were K_P = 1/4 and K_I = 1/256. The maximum duty cycle for the boost converter was set to 15/16. The system diagram for the microcontroller-based hybrid PFC pre-regulator without input voltage sensing is shown in Fig. 4.6.

The circuit in Fig. 4.6 was constructed and tested in the laboratory. All experimental results were captured with a TDS 7054 oscilloscope using the average acquisition mode where 16 waveforms were averaged for the display. In addition, the TDSPWR2 (Power Analysis Measurements Package) software from Tektronix was utilized to calculate total harmonic distortion (THD) and power factor. The RMS value of the input voltage was varied over a wide range of 50 V to 140 V, and the load was varied between 50 and 250 W. Under these variable conditions, the output DC voltage of the single-phase PFC pre-regulator was maintained at 202 V.

Fig. 4.7 - 4.60 are waveforms recorded experimentally. These plots illustrate the input voltage and current waveforms at different operating conditions, and the circuit performance can be ascertained using the waveforms.

Fig. 4.7 - 4.16 are the waveforms when the load was 50 W while the RMS value of the input voltage varied from 60 V to 140 V. It can be seen from these waveforms that the input current is in phase with the input voltage in the full voltage range. All of the current waveforms are close to sinusoidal waveforms with slight distortion at the zero crossing areas. When the voltage is extremely low, say 60 V, the input current has higher distortion, due to much higher current value to maintain the same output power. When the input voltage is lower than 60 V, the output voltage cannot be maintained at 202 V due to the maximum current limit when the duty cycle reaches its maximum, thus the

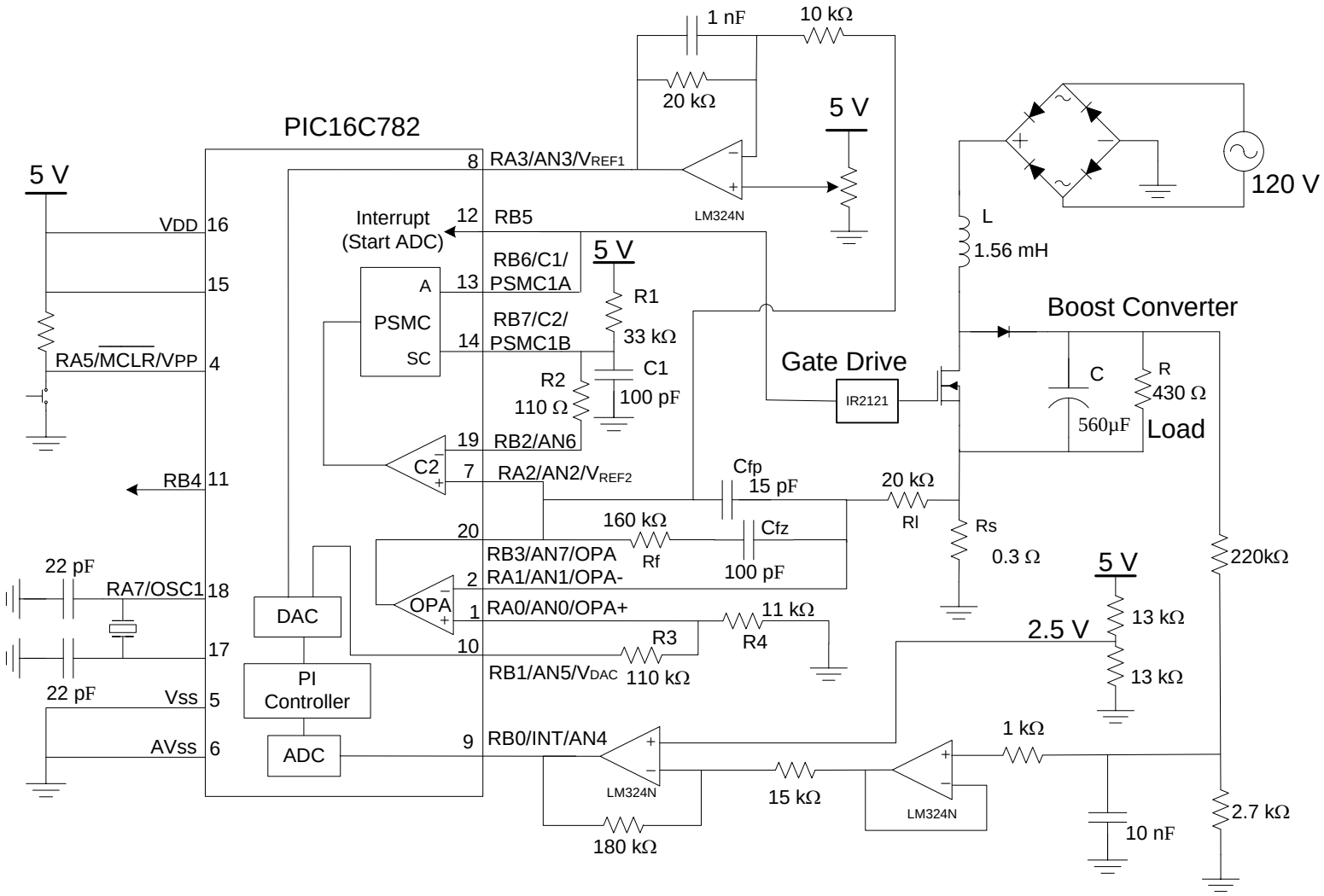


Fig. 4.6 Hybrid PFC preregulator without input voltage sensing controlled by a PIC16C782 microcontroller

output voltage is lower than 202 V, and the output power is lower than 50 W. When the output power is 50 W, the peak-to-peak output voltage ripple is around 2.3 V, with negligible variations at different input voltages. Notice the frequency of the output voltage ripple is 120 Hz, which reflects the 120 Hz rectified sinusoidal input voltage, not the switching frequency of the power stage.

Fig. 4.17 - 4.24 are the waveforms when the load was 75 W while the input voltage varied from 80 V to 140 V. It can be seen from these waveforms that the distortion at the zero crossing areas is slightly better than the condition when the load is 50 W. When the input voltage is lower than 80 V, the input current is so high that the maximum duty cycle is reached, and the output voltage is lower than desired value. When the input voltage is higher than 140 V, obvious distortion in input current can be observed when the current reaches its peak value during each cycle. When the output power is 75 W, the peak-to-peak output voltage ripple is around 3.7 V.

Fig. 4.25 - 4.32 are the waveforms when the load was 100 W while the input voltage varied from 85 V to 140 V. The output voltage cannot be regulated to 202 V when the input voltage is lower than 85 V. Improvement in distortion at the zero crossing can be observed. When the input voltage is higher than 130 V, distortion in the peak current area of each cycle becomes obvious. When the output power is 100 W, the peak-to-peak output voltage ripple is around 3.7 V.

Fig. 4.33 - 4.39 are the waveforms when the load was 125 W while the input voltage varied from 93 V to 140 V. The output voltage cannot be regulated to 202 V when the input voltage is lower than 93 V. When the input voltage is between 93 V and 130 V, the input current is a smooth sinusoidal waveform in phase with the input voltage,

and the distortion is unnoticeable. When the input voltage is higher than 130 V, peak current area has some distortion. When the output power is 125 W, the peak-to-peak output voltage ripple is around 5.4 V.

Fig. 4.40 - 4.45 are the waveforms when the load was 150 W while the input voltage varied from 100 V to 138 V, Fig. 4.46 - 4.50 are the waveforms when the load was 175 W while the input voltage varied from 108 V to 140 V, and Fig. 4.51 - 4.55 are the waveforms when the load was 200 W while the input voltage varied from 115 V to 140 V. For different output loads, the input voltage must be high enough such that the output voltage can be regulated to 202 V. For example, when the output power is 200 W, the input voltage needs to be higher than 115 V. When the input voltage is lower than 130 V, the input current is a sinusoidal waveform in phase with the input voltage. When the input voltage is higher than 130 V, the peak current areas always have some distortion. When the output power is 150 W, 175 W and 200 W, the peak-to-peak output voltage ripple is around 5.7 V, 6.7 V and 8.2 V, respectively.

Fig. 4.56 - 4.58 are the waveforms when the load was 225 W while the input voltage varied from 122 V to 140 V, and Fig. 4.59 - 4.60 are the waveforms when the load was 250 W while the input voltage varied from 130 V to 140 V. All the waveforms show distortions in the peak current area in each 60 Hz cycle due to the maximum duty cycle limit. Also, the input voltage has to be higher than the nominal voltage to maintain the desired output voltage.

Quantitative analysis of the performance of the system can be obtained by investigating the harmonic spectrum, THD and power factor. The THD for the input

current was calculated using (3-68), and harmonics through the 40th were included in the calculation of the THD. The power factor (*pf*) was calculated using (3-69).

When the proposed PFC pre-regulator without input voltage sensing is operating under nominal conditions, where the input voltage is 120 V and the load is 100 W, the power factor is 0.9959, and the THD of the input current is 8.3%. At this time, the fundamental component dominates the current harmonics, as illustrated in Fig. 4.61. When the input voltage is 110 V and the power is 150 W, the power factor is still 0.9959, but the THD of the input current is only 6.29%.

Fig. 4.62 summarizes the power factor at different operating conditions, where the RMS value of the input voltage varies between 100 V and 140 V, and the load varies from 50 W to 200 W. As shown in Fig. 4.62, the power factor varied between 0.9702 and 0.9972, with the lowest power factor occurring at the lowest load level and the highest input voltage. The PFC pre-regulator is able the maintain power factor above 0.995 at normal operating condition as well as most operating conditions when the load is higher than 75 W. When the load is low, the sensed inductor current is also low, which results in a low signal-to-noise ratio and distortion in the input current. The problem is especially true when the load is low and input voltage is high. It can be seen clearly in Fig. 4.15 and Fig. 4.62 when the load is 50 W and the input voltage is 140 V, where the power factor is only 0.9702 and the THD of the input current is 13.396%.

The effects of variations in the input voltage and load power on the THD of the input current were also examined. The result of this examination is plotted in Fig. 4.63, where the RMS value of the input voltage varies from 100 V to 140 V, and the load varies from 50 W to 200 W. Note that the input current THD varies between 5.24% and

13.4%, with the largest THD occurring at the lowest load level and the highest input voltage. When the load is above 100 W, the input current THD is below 8.32%.

Fig. 4.64 illustrates the variations in the peak-to-peak output voltage ripple with output load range from 50 W to 200 W. Note that the output voltage ripple varies between 2.68 V to 8.7 V, representing 1.32% to 4.3% of the 202 V nominal output voltage. Clearly, the output voltage ripple decreased when the output load decreased.

In conclusion, by using the on-board peripherals of a PIC16C782 microcontroller, a one-chip solution of a practical design for a microcontroller-based PFC pre-regulator without input voltage sensing has been achieved. The proposed PFC pre-regulator has demonstrated satisfactory experimental results. Experimental results show that the PFC pre-regulator can operate satisfactorily over a wide range of input voltages and load powers. The power factor is above 0.99 for load power in excess of 75 W.

Because of the simplicity of the circuit, the proposed PFC pre-regulator has low cost and high reliability. This design has proven that it is possible to implement a high-performance PFC controller on a single microcontroller without using more expensive DSPs or other complicated hardware.

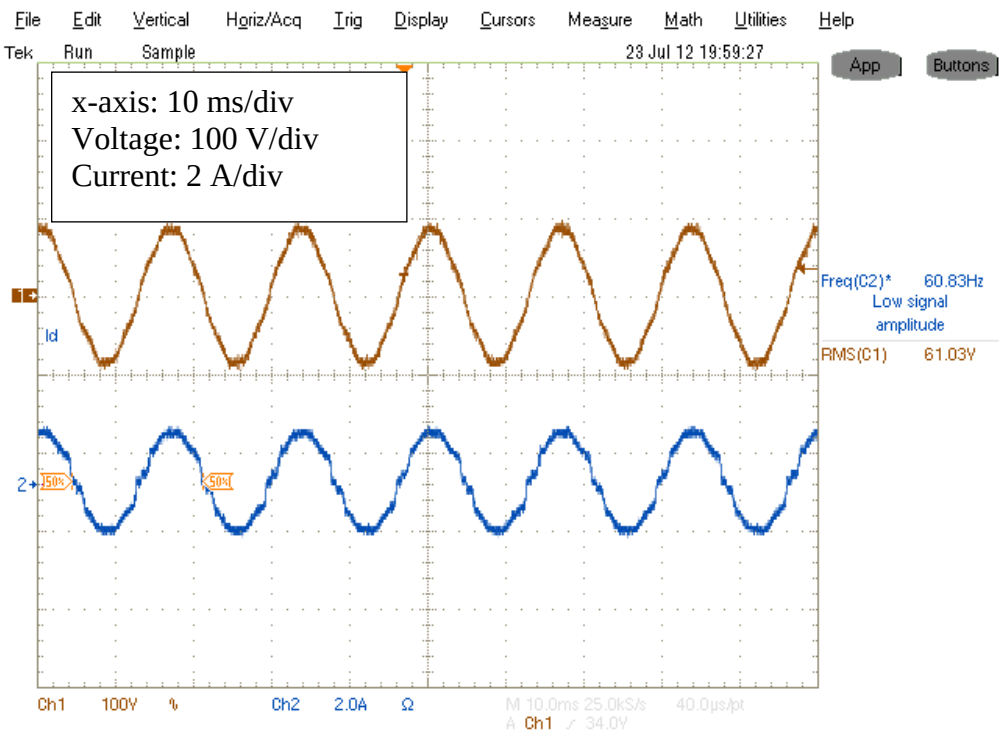


Fig. 4.7 Input voltage and current when V_{in} = 60 V and P_{load} = 50 W

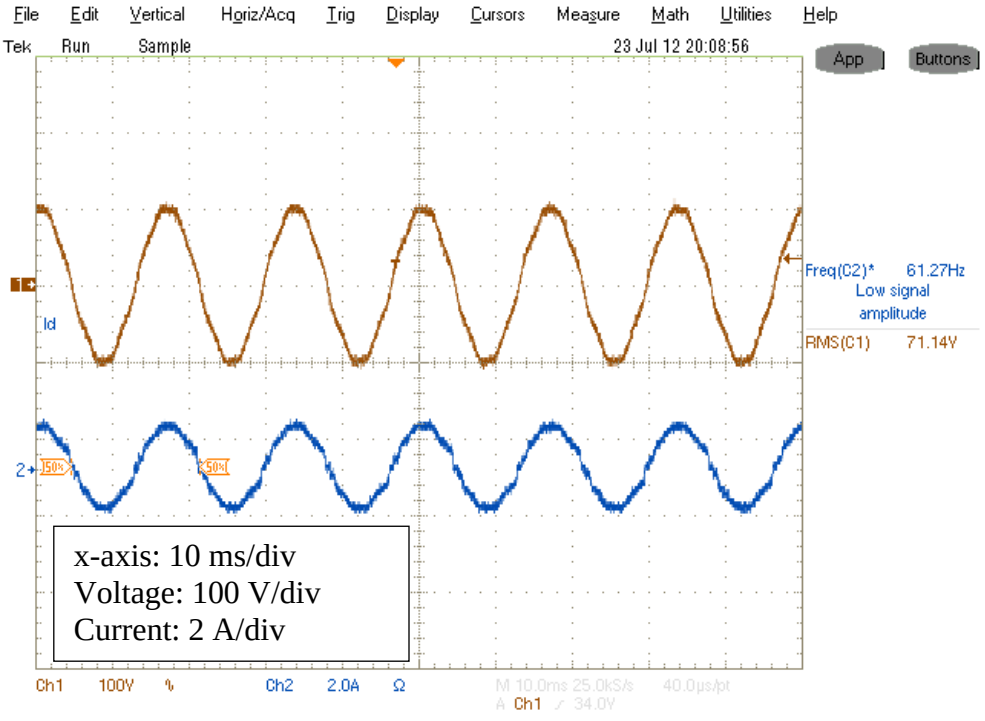


Fig. 4.8 Input voltage and current when V_{in} = 70 V and P_{load} = 50 W

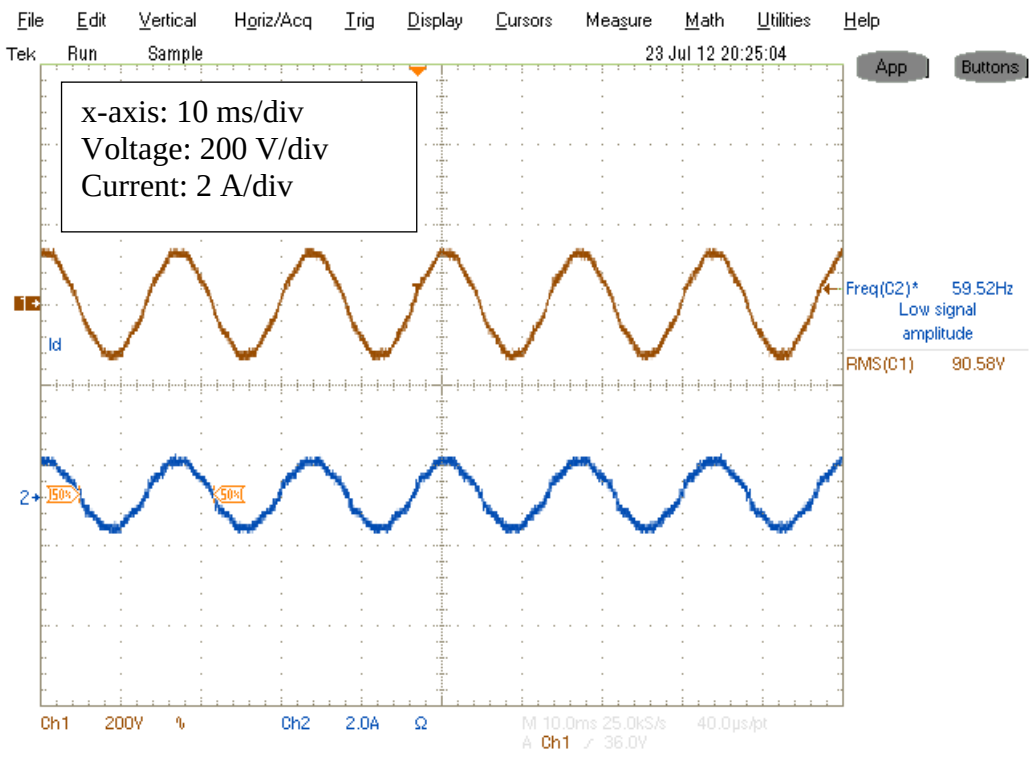


Fig. 4.9 Input voltage and current when V_{in} = 80 V and P_{load} = 50 W

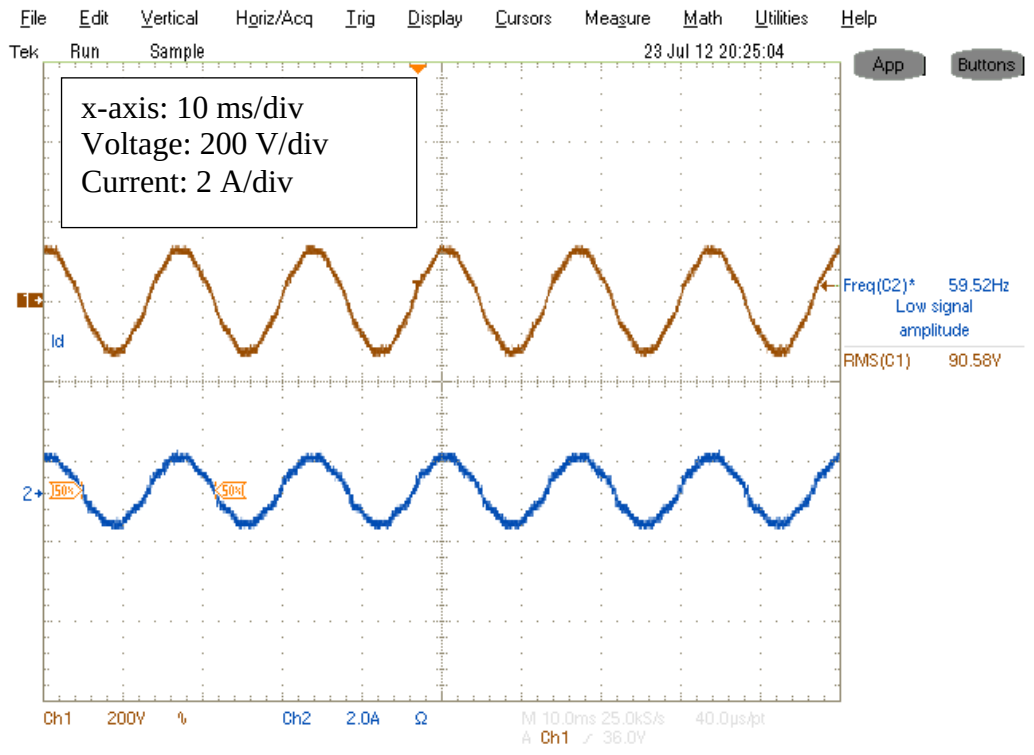


Fig. 4.10 Input voltage and current when V_{in} = 90 V and P_{load} = 50 W

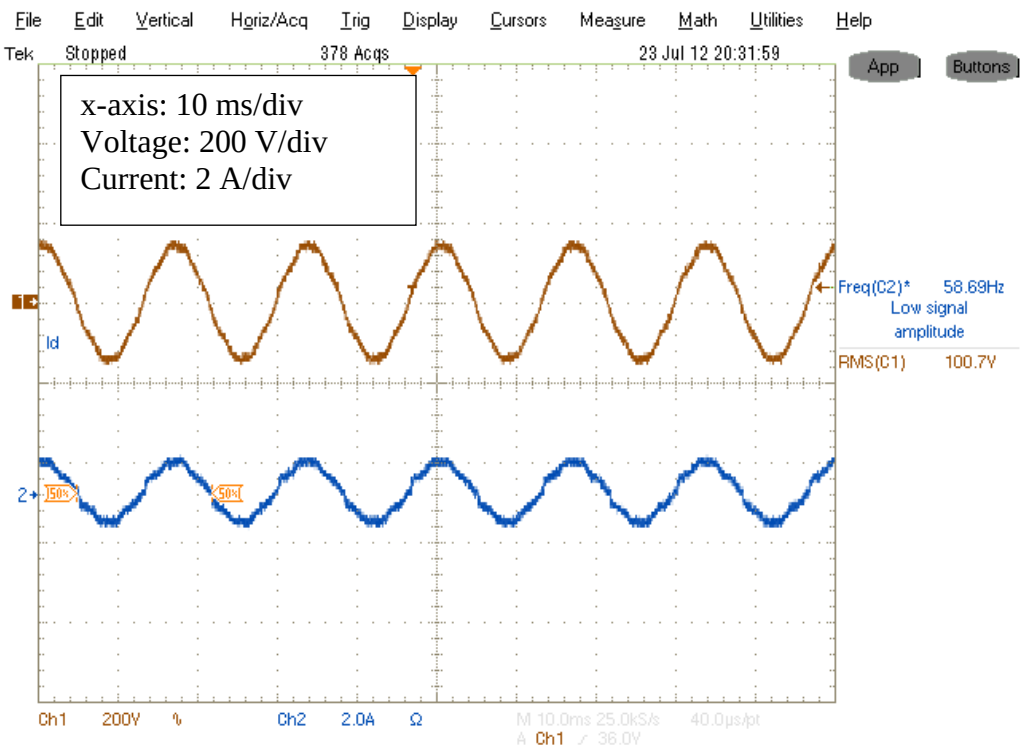


Fig. 4.11 Input voltage and current when V_{in} = 100 V and P_{load} = 50 W

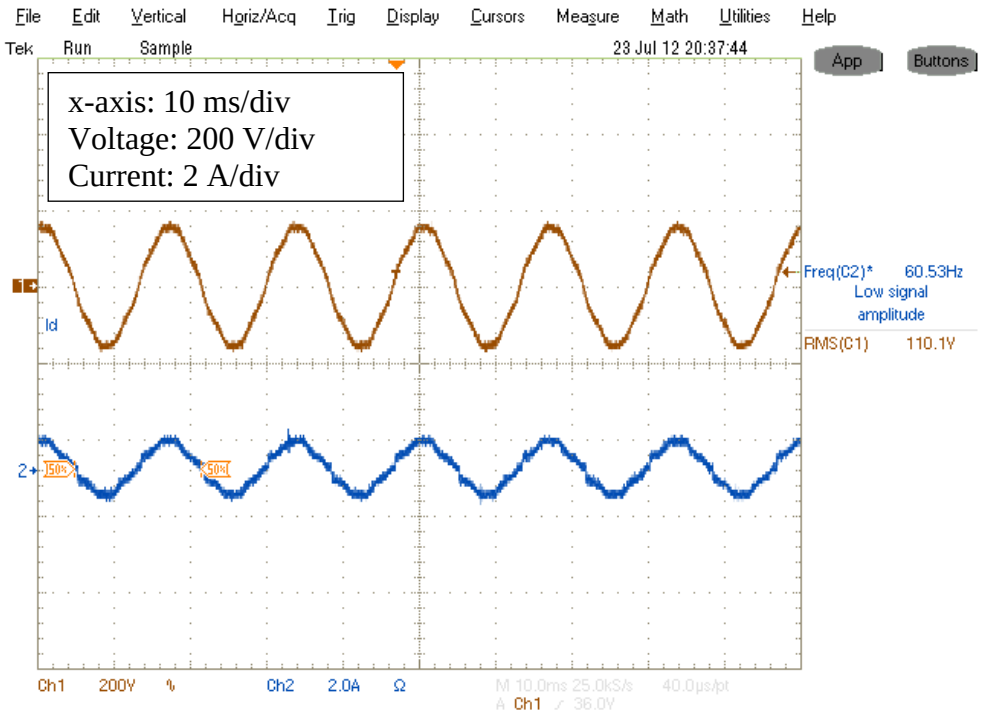


Fig. 4.12 Input voltage and current when V_{in} = 110 V and P_{load} = 50 W

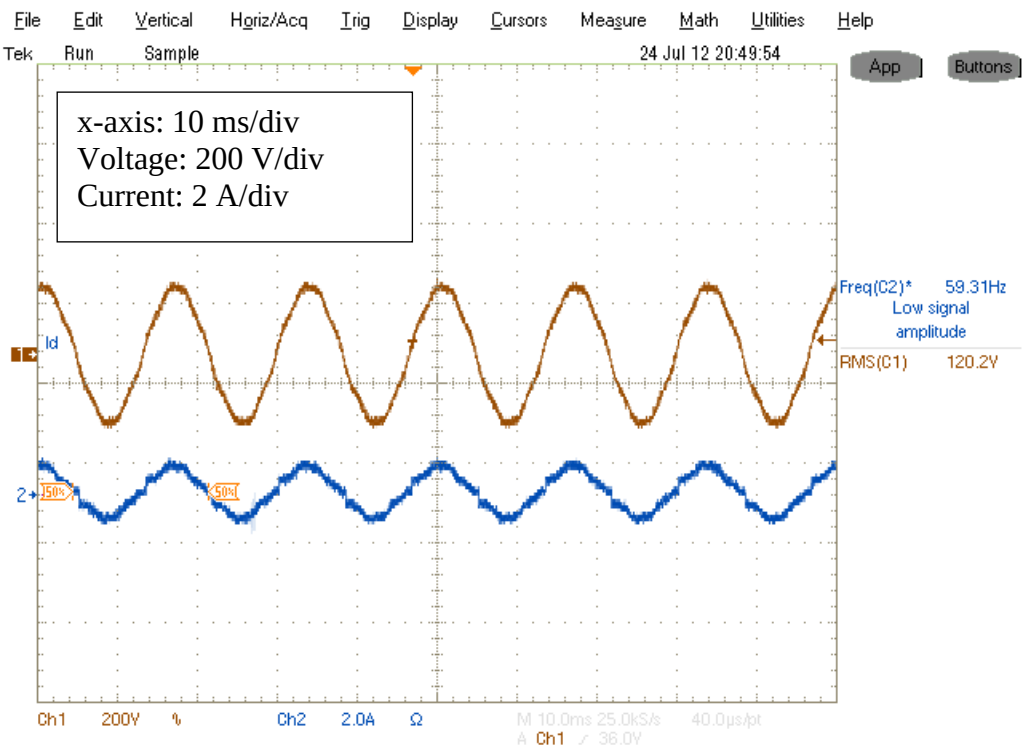


Fig. 4.13 Input voltage and current when V_{in} = 120 V and P_{load} = 50 W

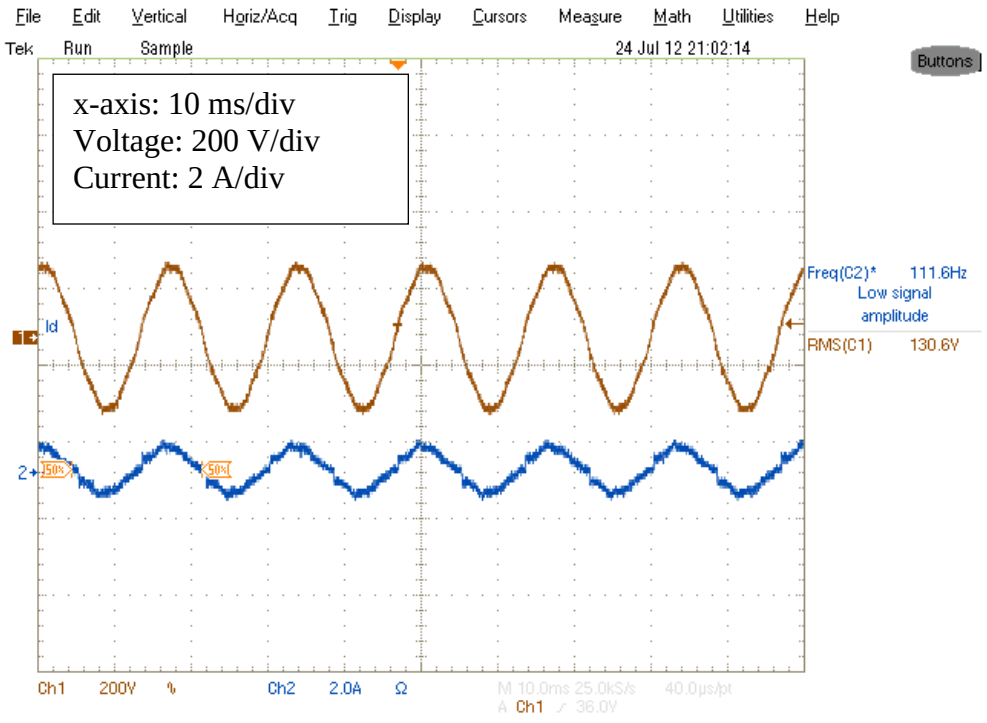


Fig. 4.14 Input voltage and current when V_{in} = 130 V and P_{load} = 50 W

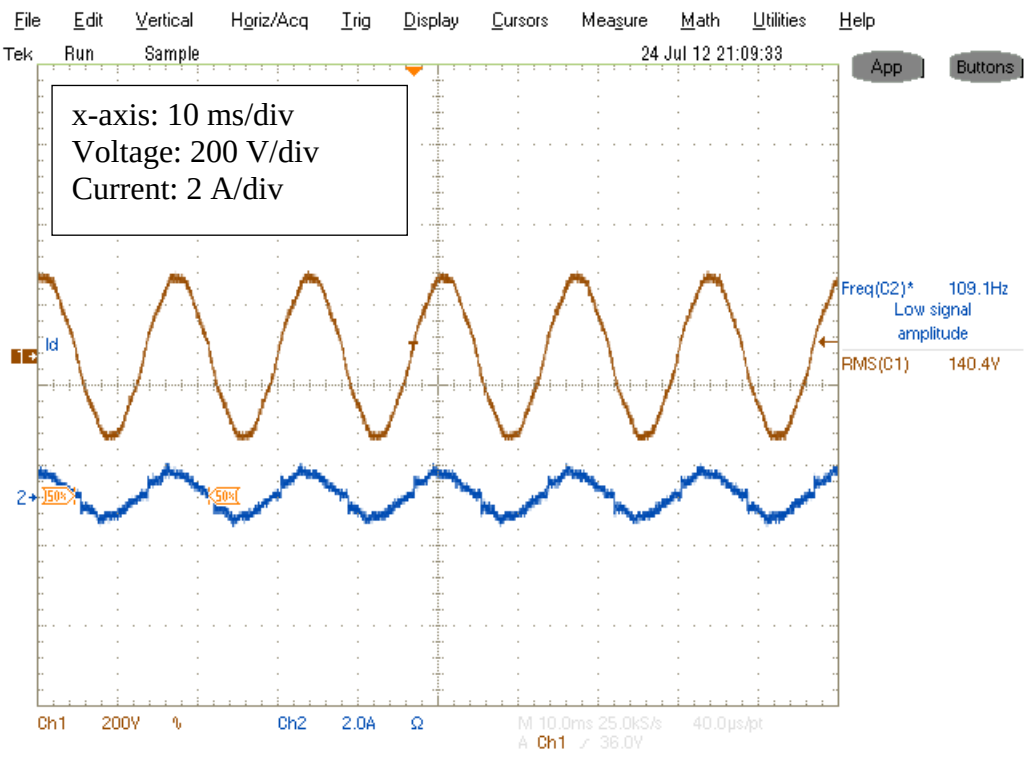


Fig. 4.15 Input voltage and current when V_{in} = 140 V and P_{load} = 50 W

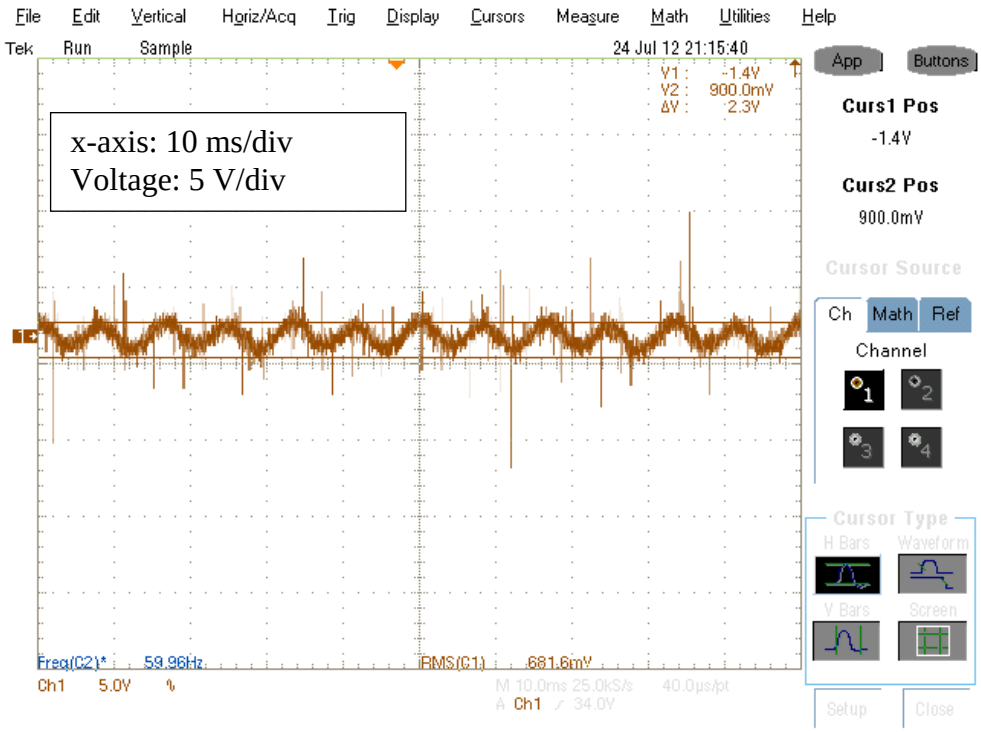


Fig. 4.16 Output voltage ripple when P_{load} = 50 W

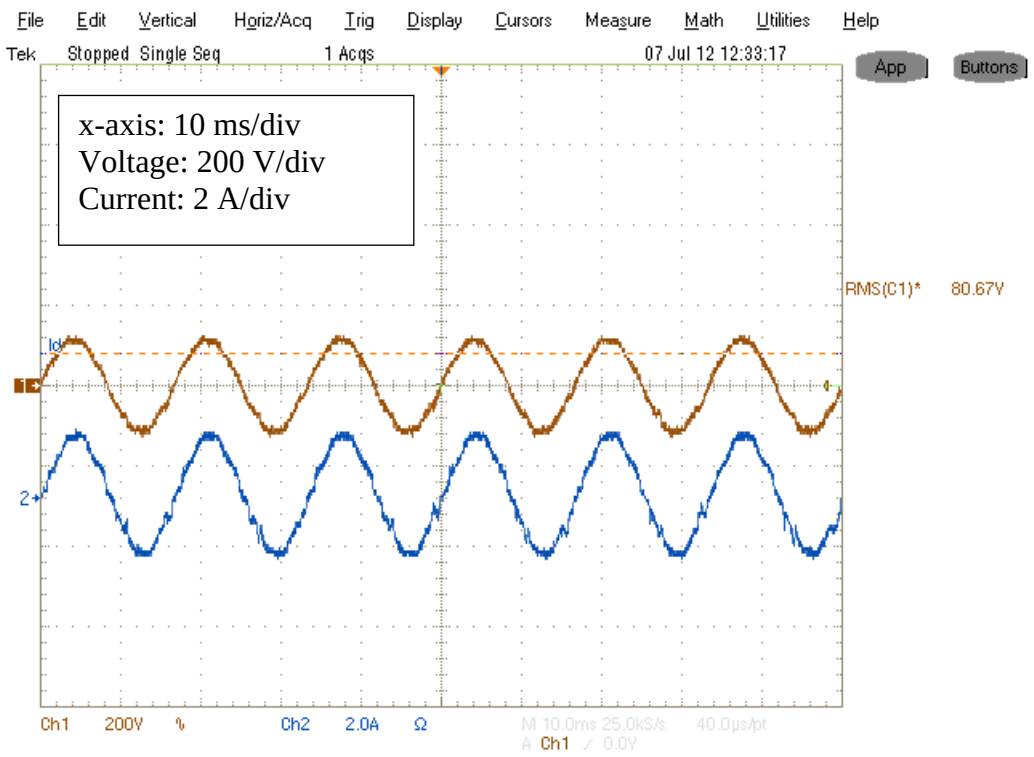


Fig. 4.17 Input voltage and current when V_{in} = 80 V and P_{load} = 75 W

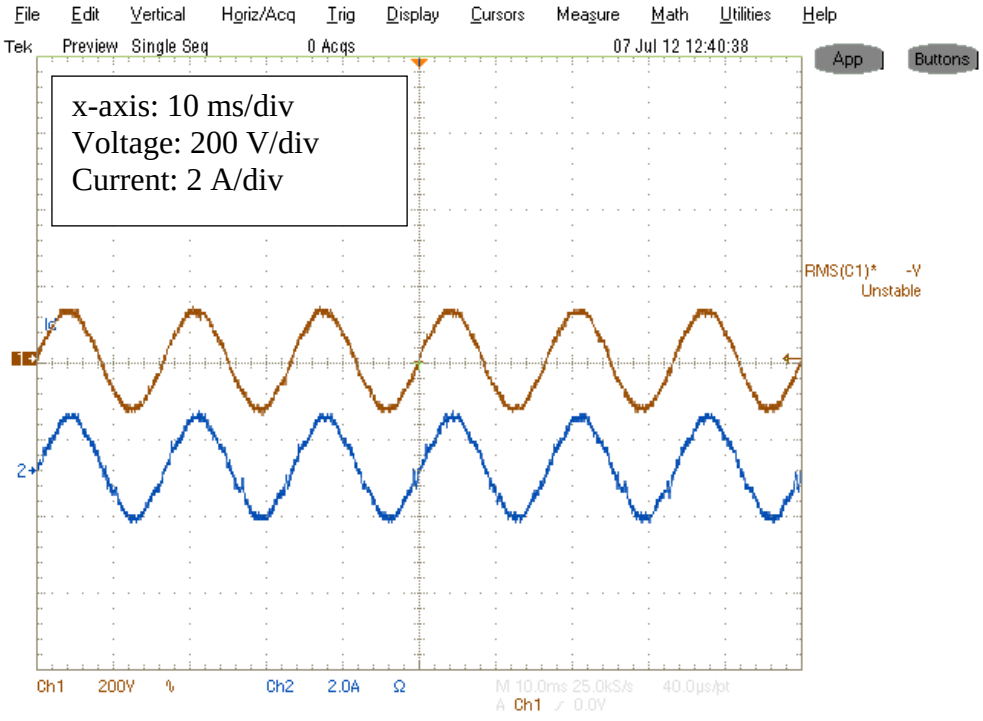


Fig. 4.18 Input voltage and current when V_{in} = 90 V and P_{load} = 75 W

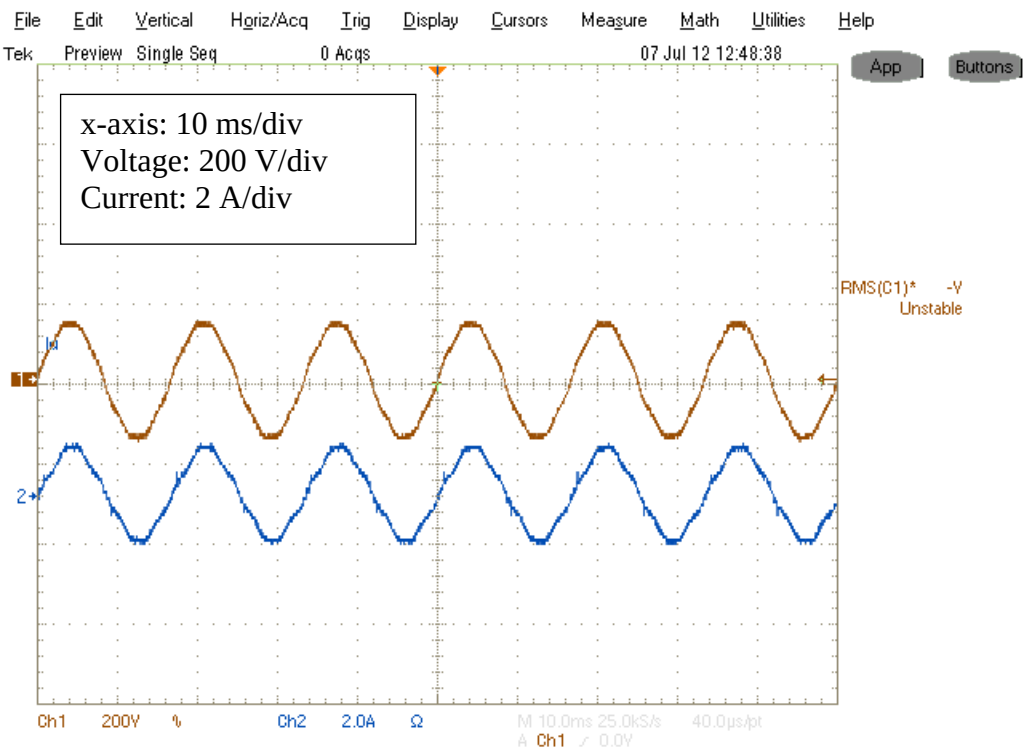


Fig. 4.19 Input voltage and current when V_{in} = 100 V and P_{load} = 75 W

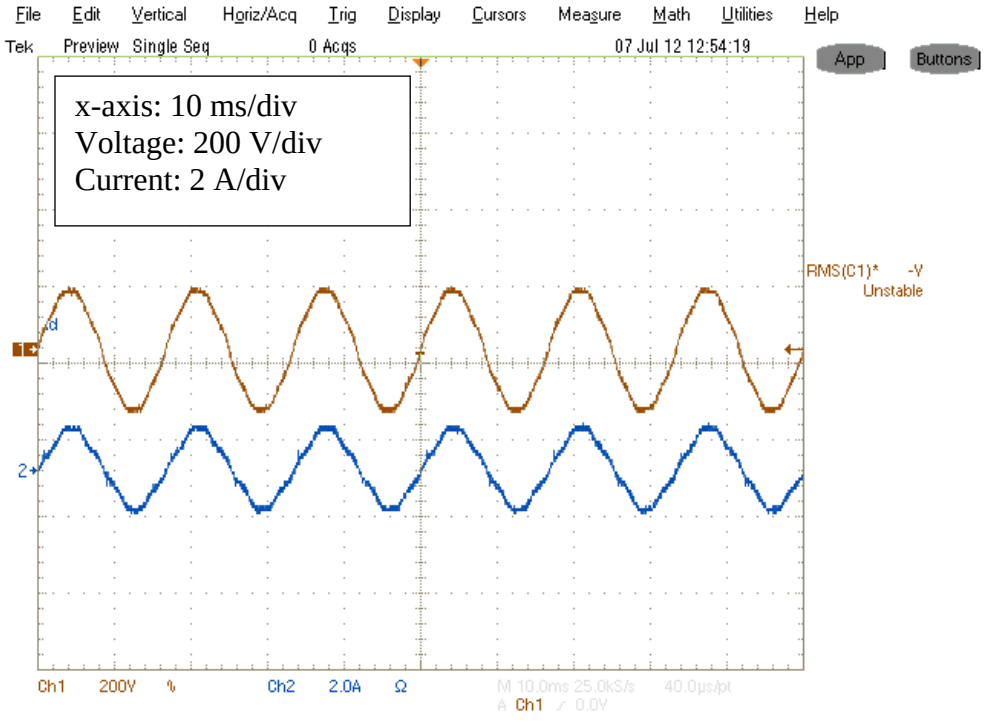


Fig. 4.20 Input voltage and current when V_{in} = 110 V and P_{load} = 75 W

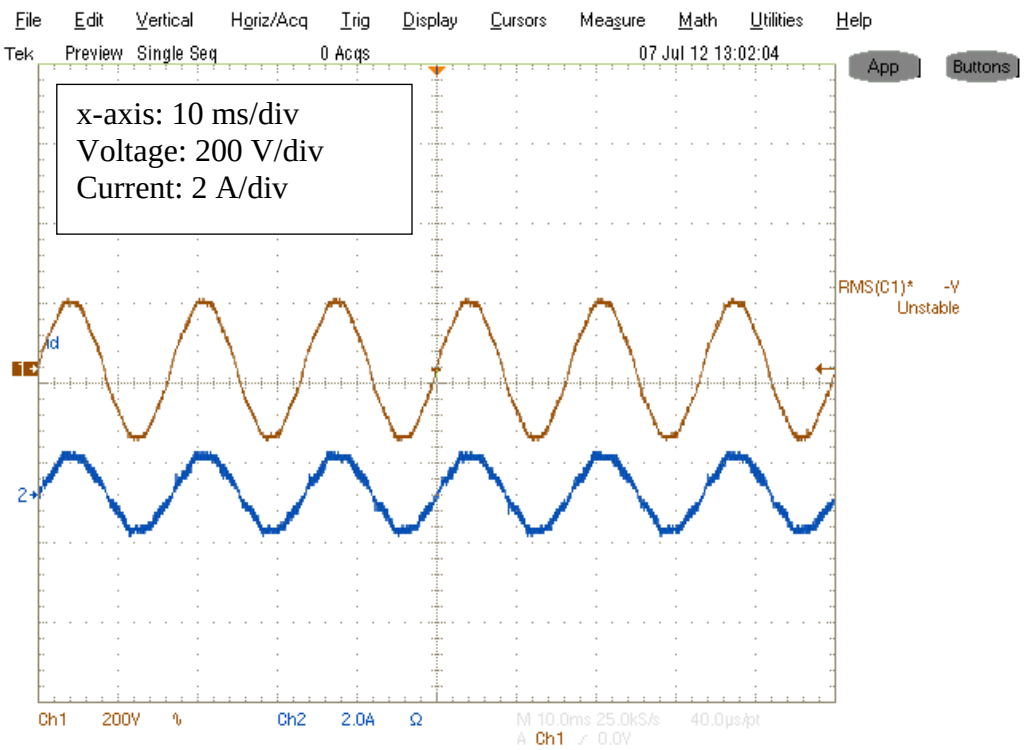


Fig. 4.21 Input voltage and current when V_{in} = 120 V and P_{load} = 75 W

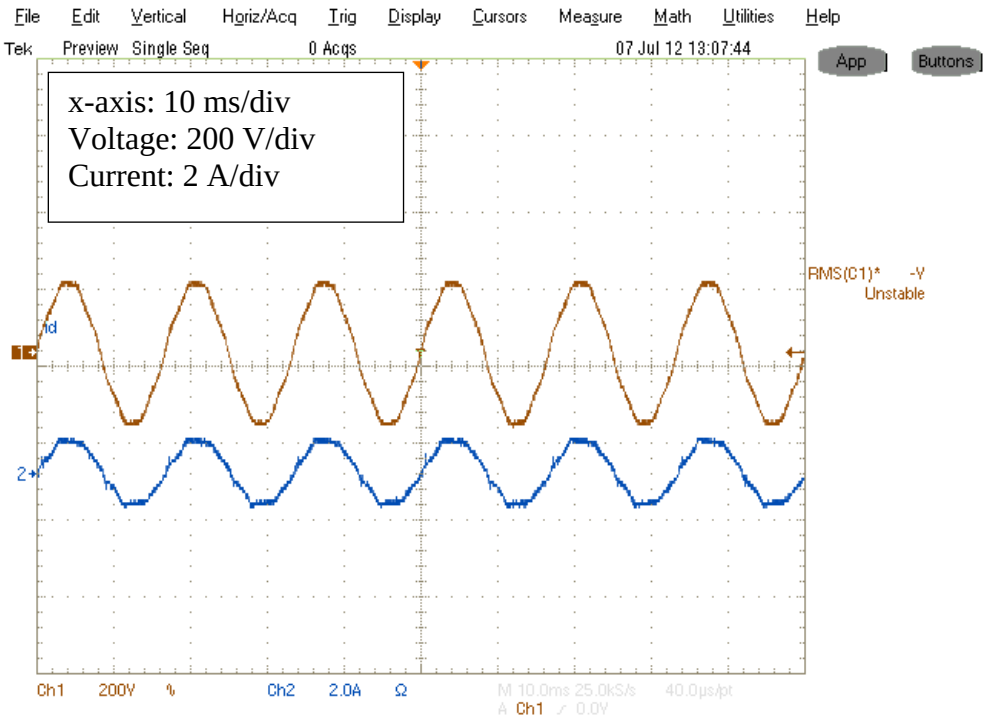


Fig. 4.22 Input voltage and current when V_{in} = 130 V and P_{load} = 75 W

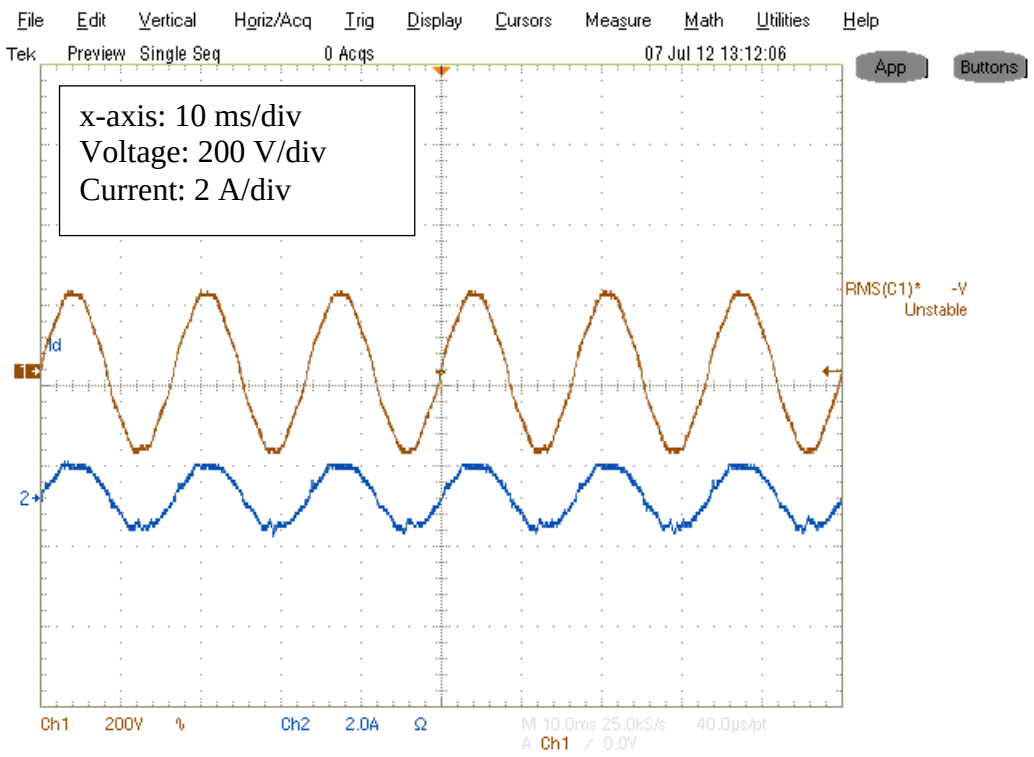


Fig. 4.23 Input voltage and current when V_{in} = 140 V and P_{load} = 75 W

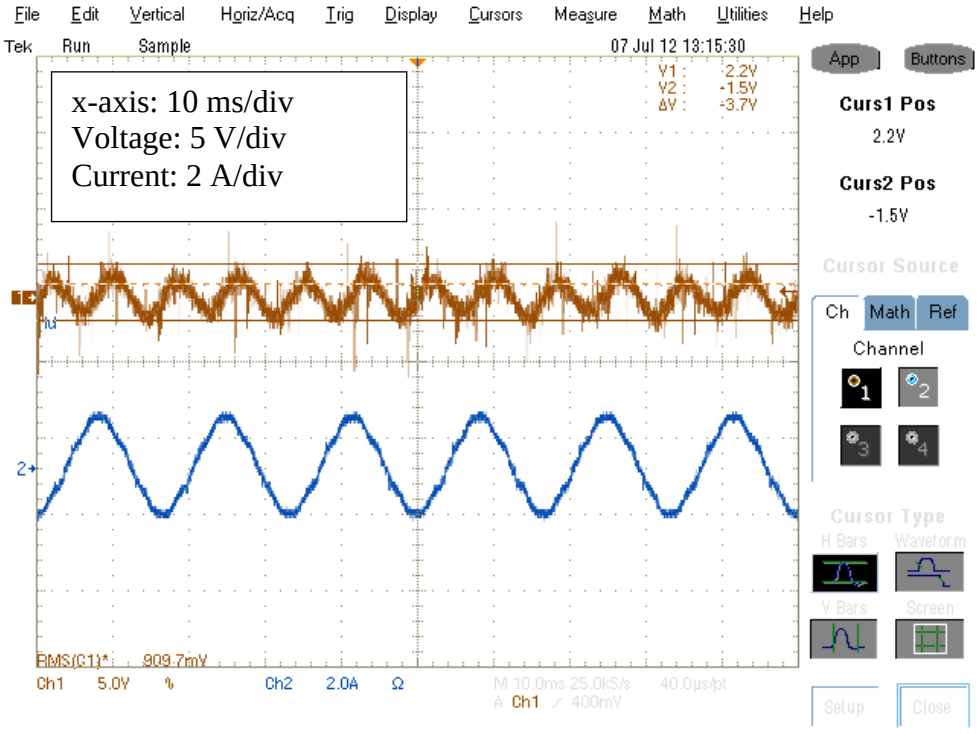


Fig. 4.24 Output voltage ripple and input current when V_{in} = 100 V and P_{load} = 75 W

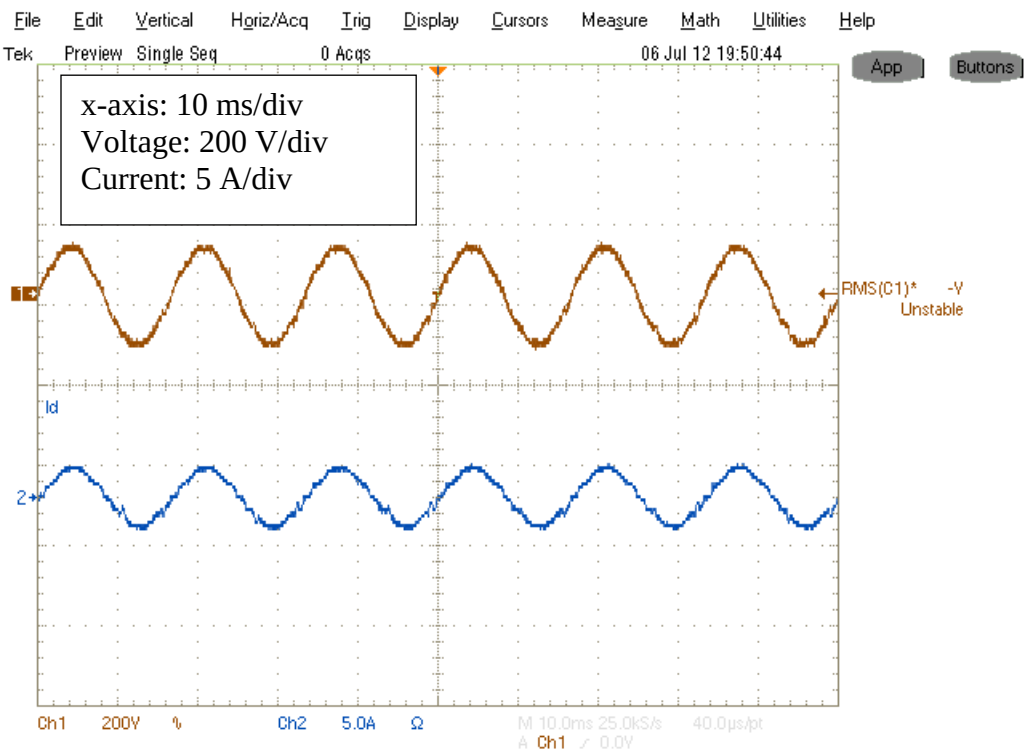


Fig. 4.25 Input voltage and current when V_{in} = 85 V and P_{load} = 100 W

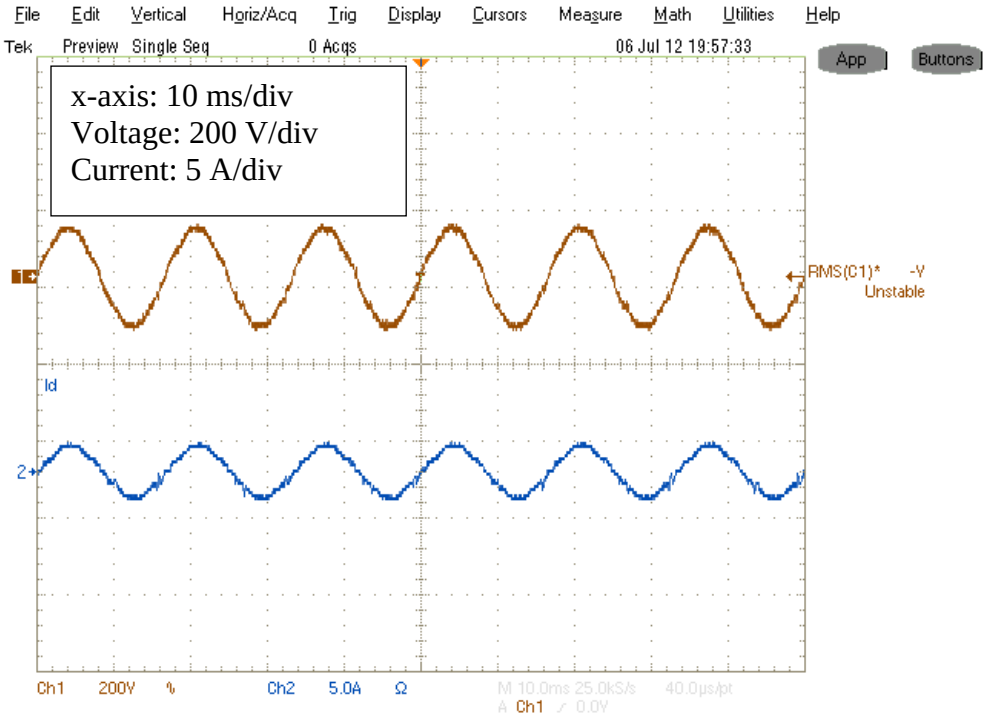


Fig. 4.26 Input voltage and current when V_{in} = 90 V and P_{load} = 100 W

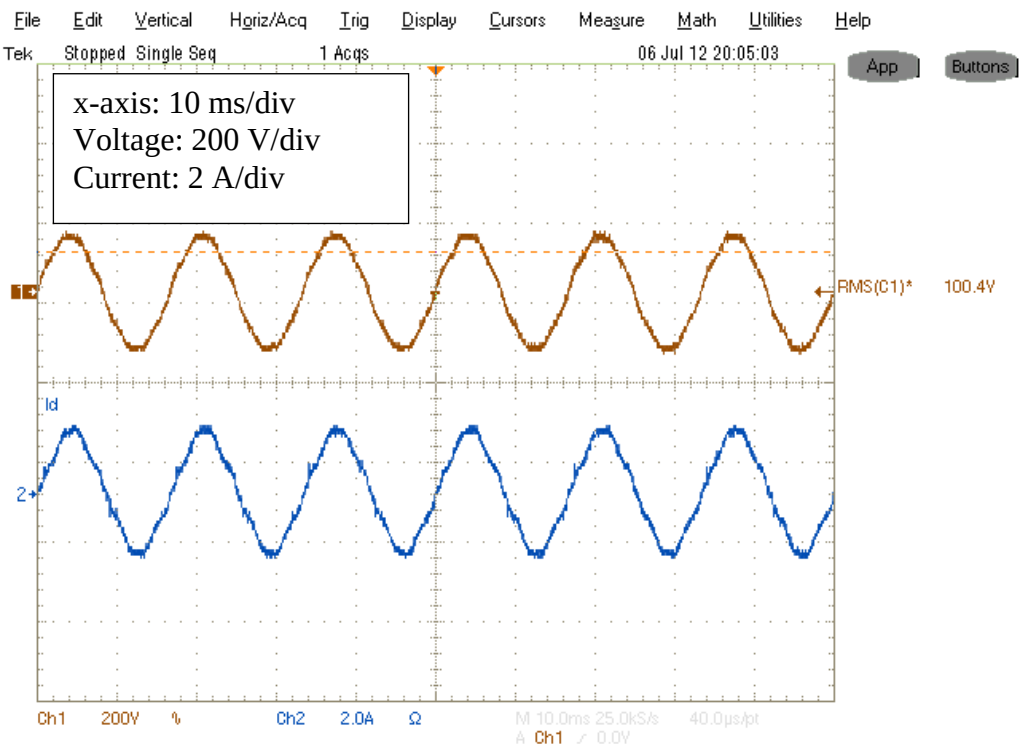


Fig. 4.27 Input voltage and current when V_{in} = 100 V and P_{load} = 100 W

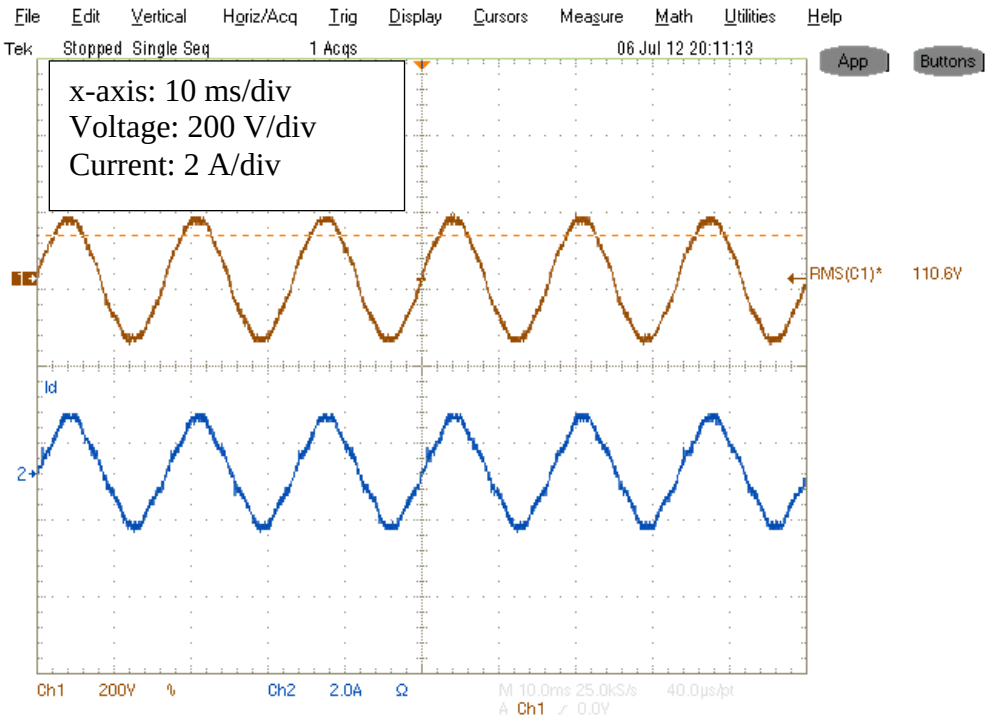


Fig. 4.28 Input voltage and current when V_{in} = 110 V and P_{load} = 100 W

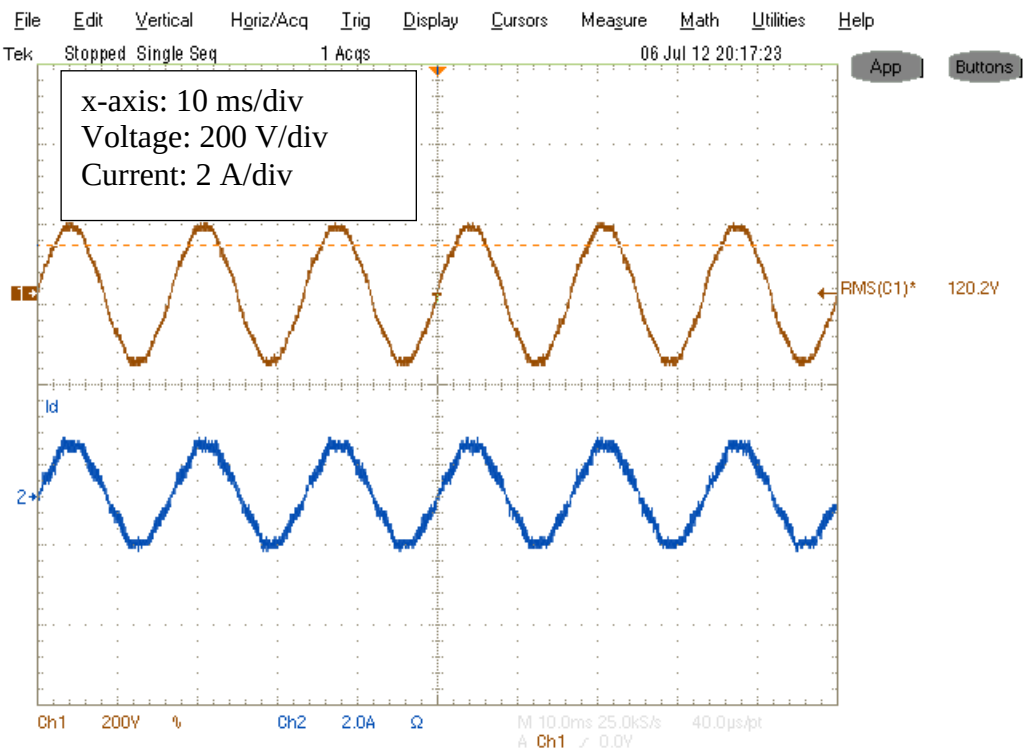


Fig. 4.29 Input voltage and current when V_{in} = 120 V and P_{load} = 100 W

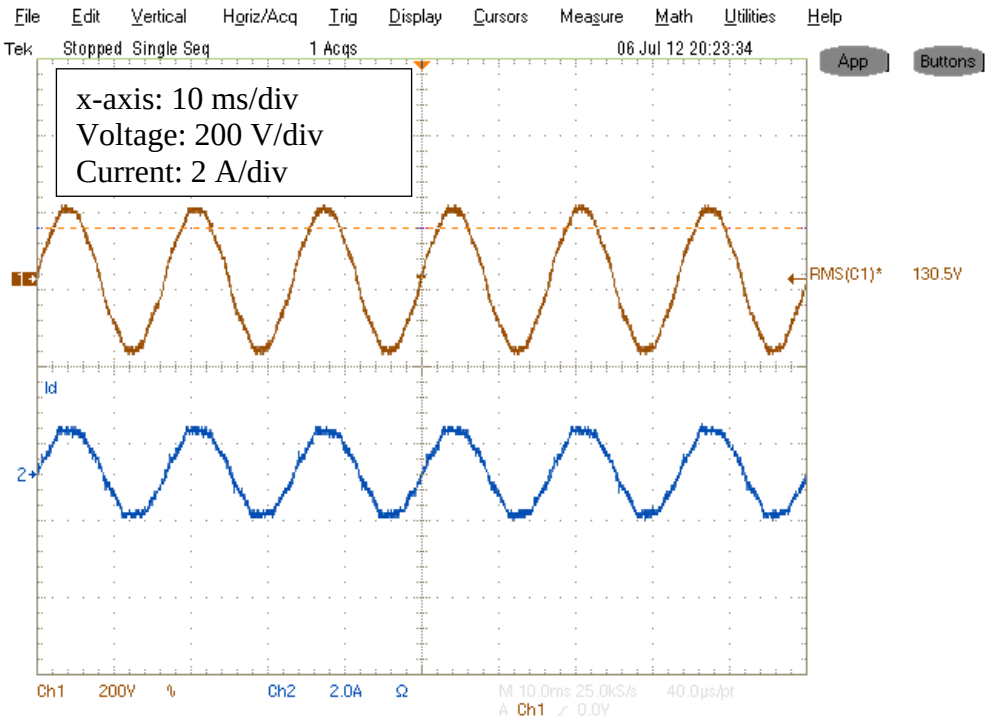


Fig. 4.30 Input voltage and current when V_{in} = 130 V and P_{load} = 100 W

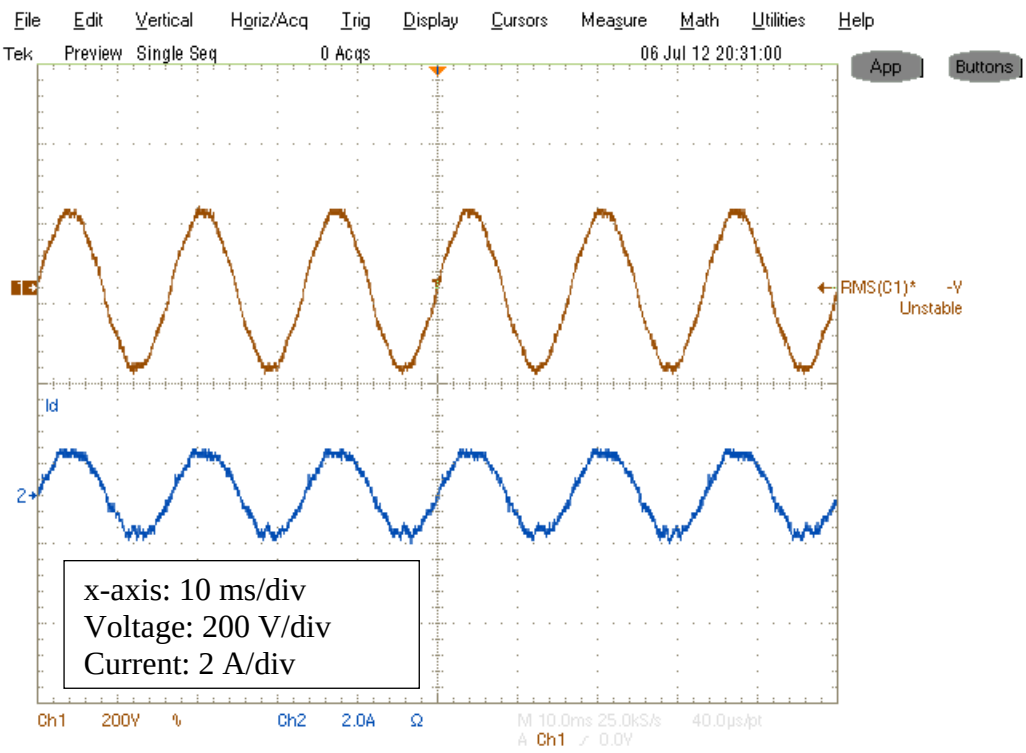


Fig. 4.31 Input voltage and current when V_{in} = 140 V and P_{load} = 100 W

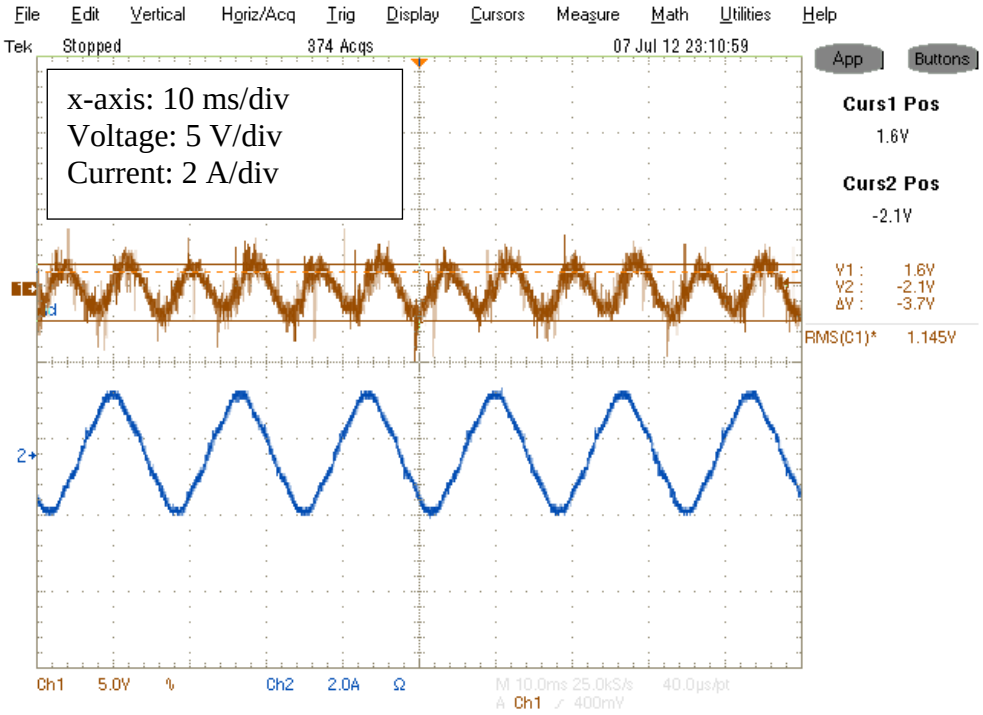


Fig. 4.32 Output voltage ripple and input current when V_{in} = 100 V and P_{load} = 100 W

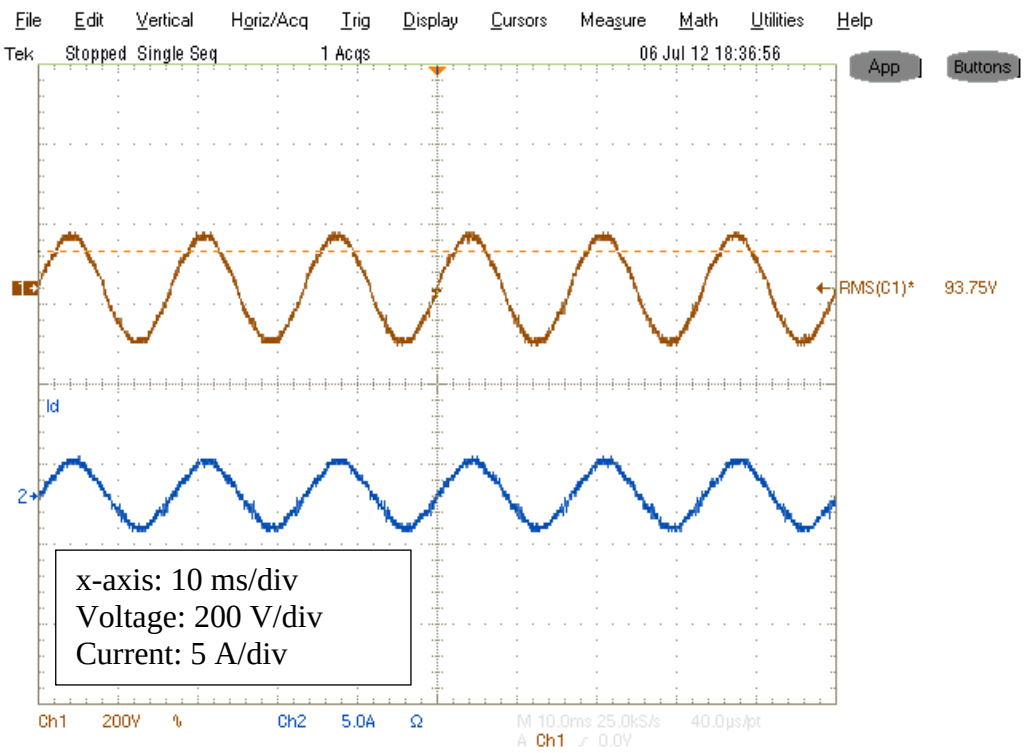


Fig. 4.33 Input voltage and current when V_{in} = 93 V and P_{load} = 125 W

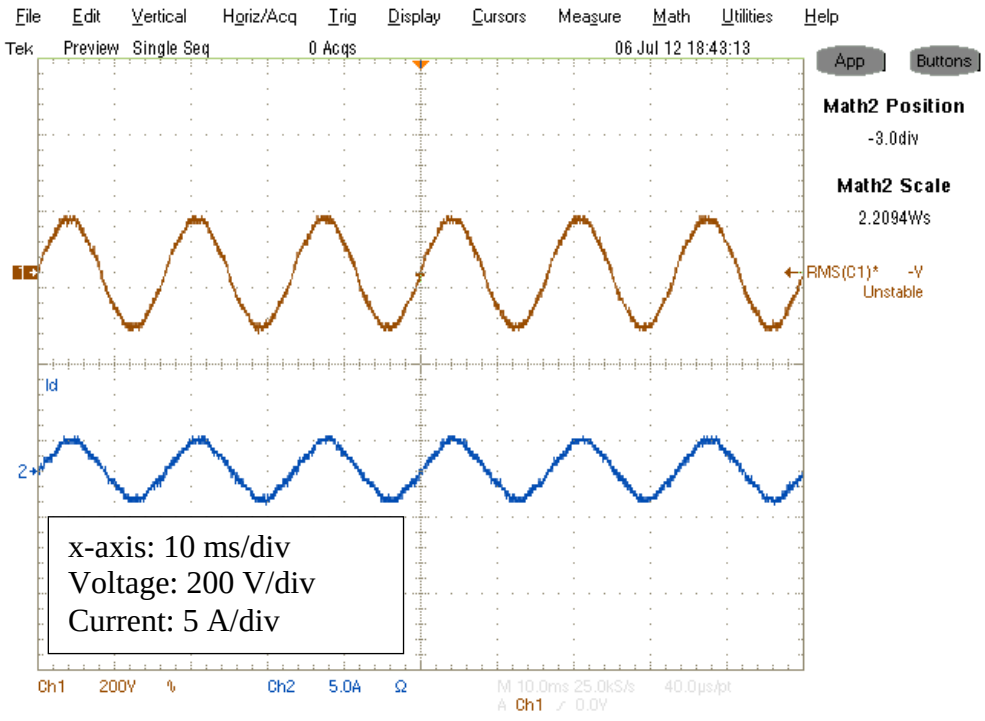


Fig. 4.34 Input voltage and current when V_{in} = 100 V and P_{load} = 125 W

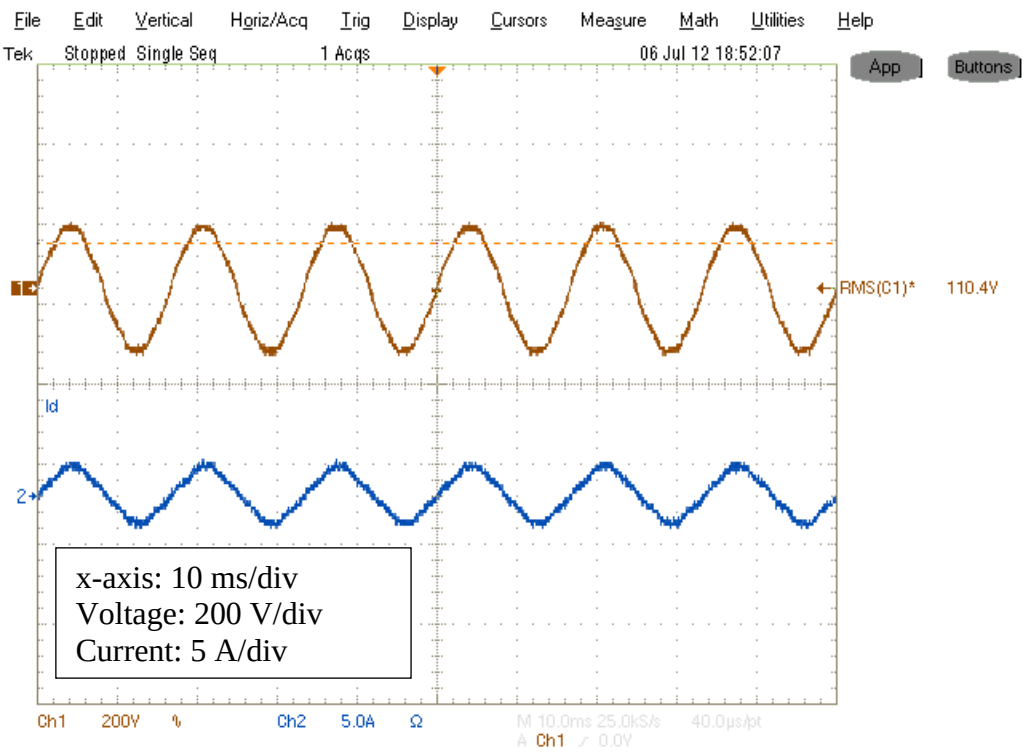


Fig. 4.35 Input voltage and current when V_{in} = 110 V and P_{load} = 125 W

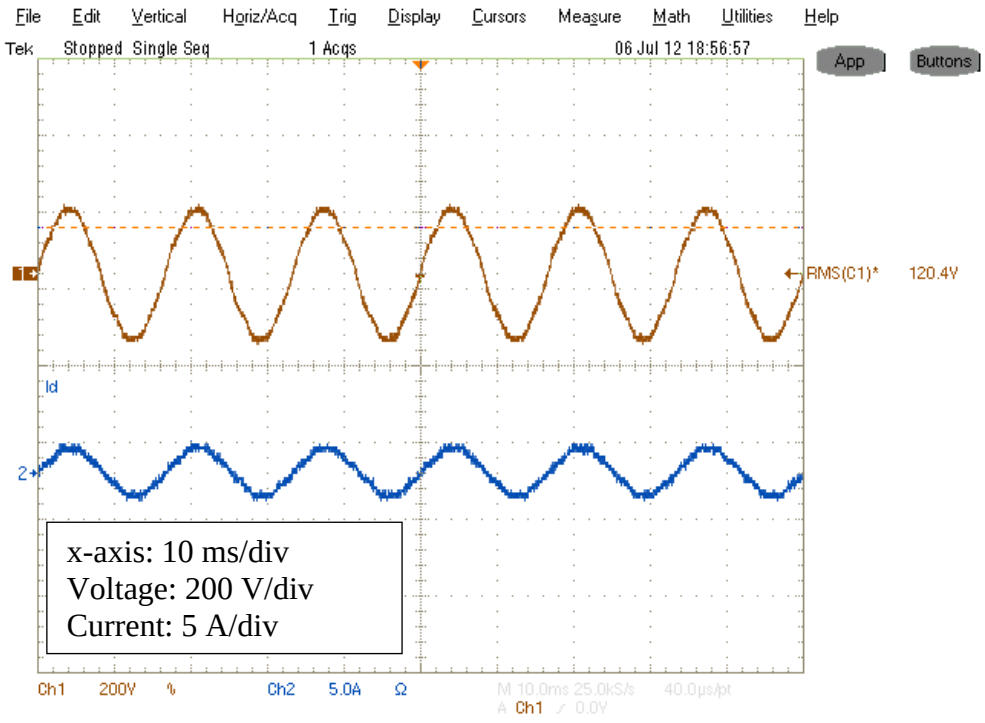


Fig. 4.36 Input voltage and current when V_{in} = 120 V and P_{load} = 125 W

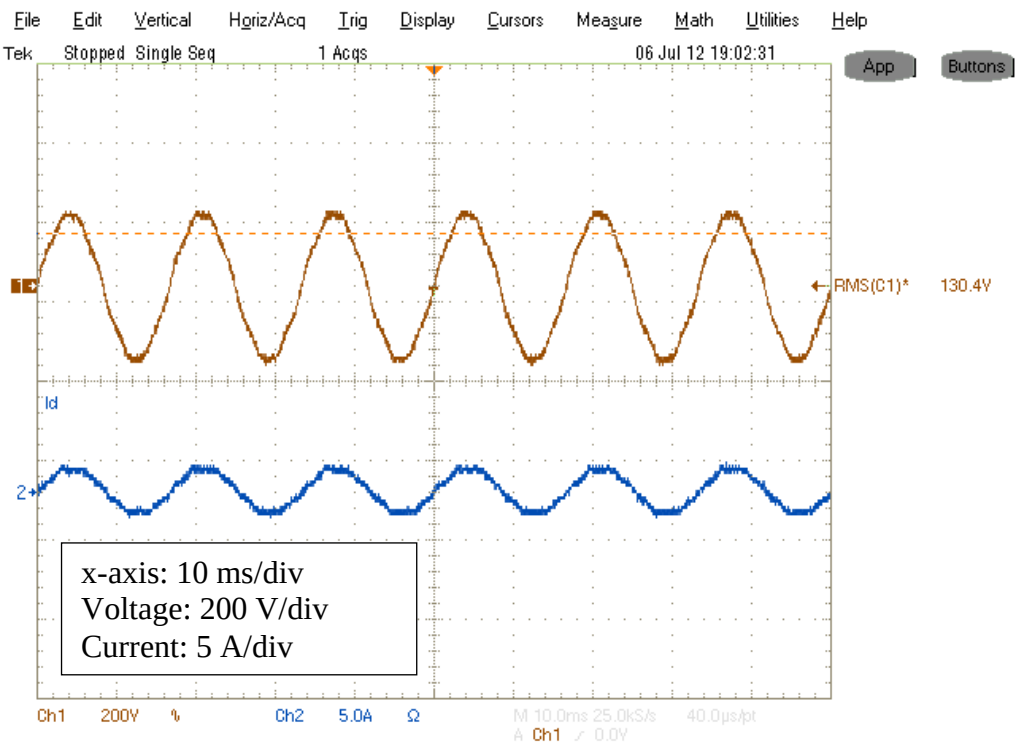


Fig. 4.37 Input voltage and current when V_{in} = 130 V and P_{load} = 125 W

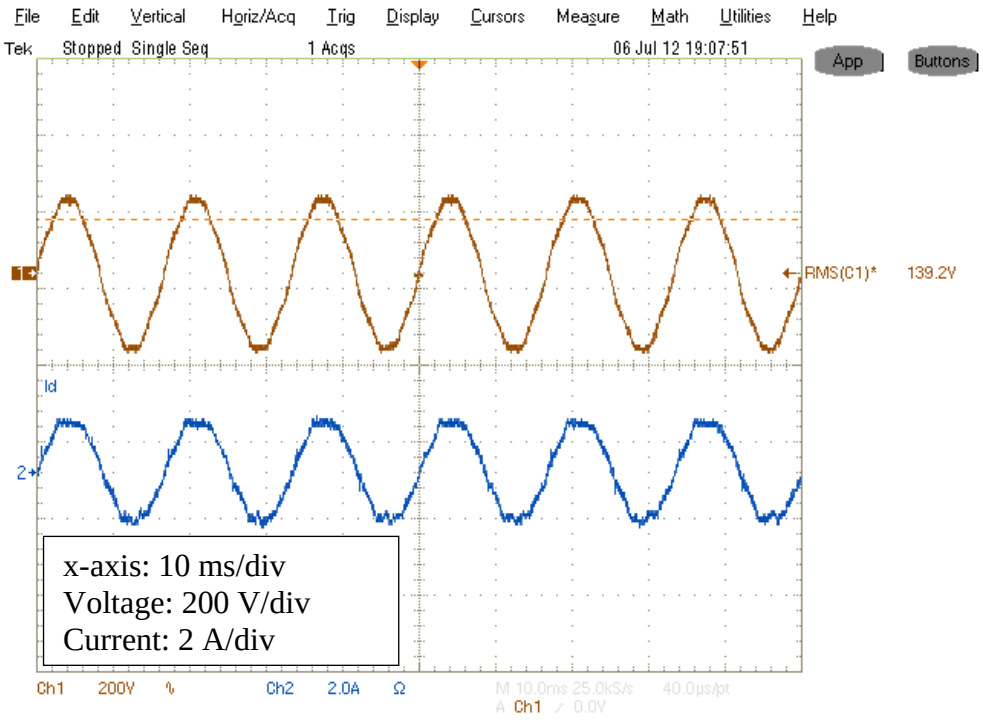


Fig. 4.38 Input voltage and current when V_{in} = 140 V and P_{load} = 125 W

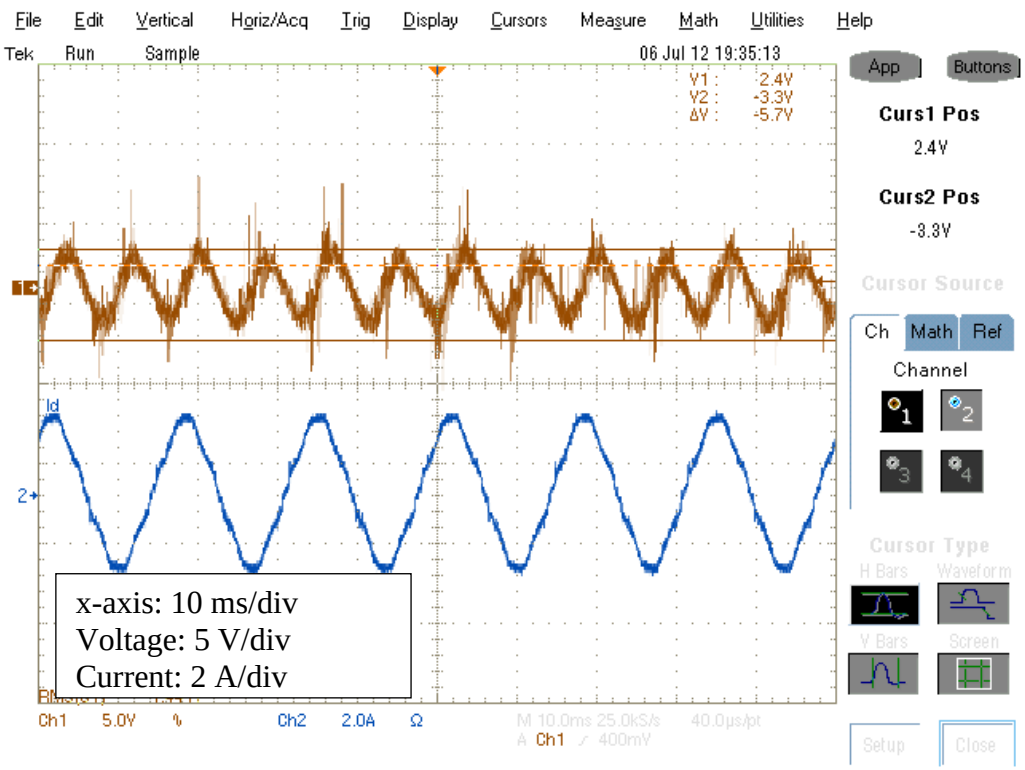


Fig. 4.39 Output voltage ripple and input current when V_{in} = 100 V and P_{load} = 125 W

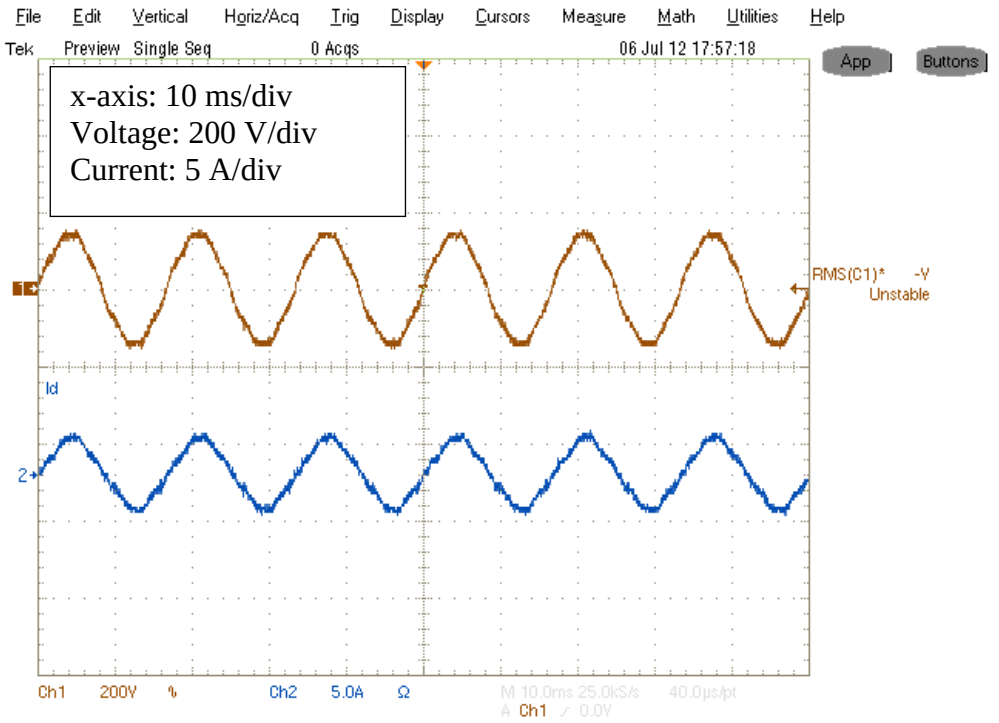


Fig. 4.40 Input voltage and current when V_{in} = 100 V and P_{load} = 150 W

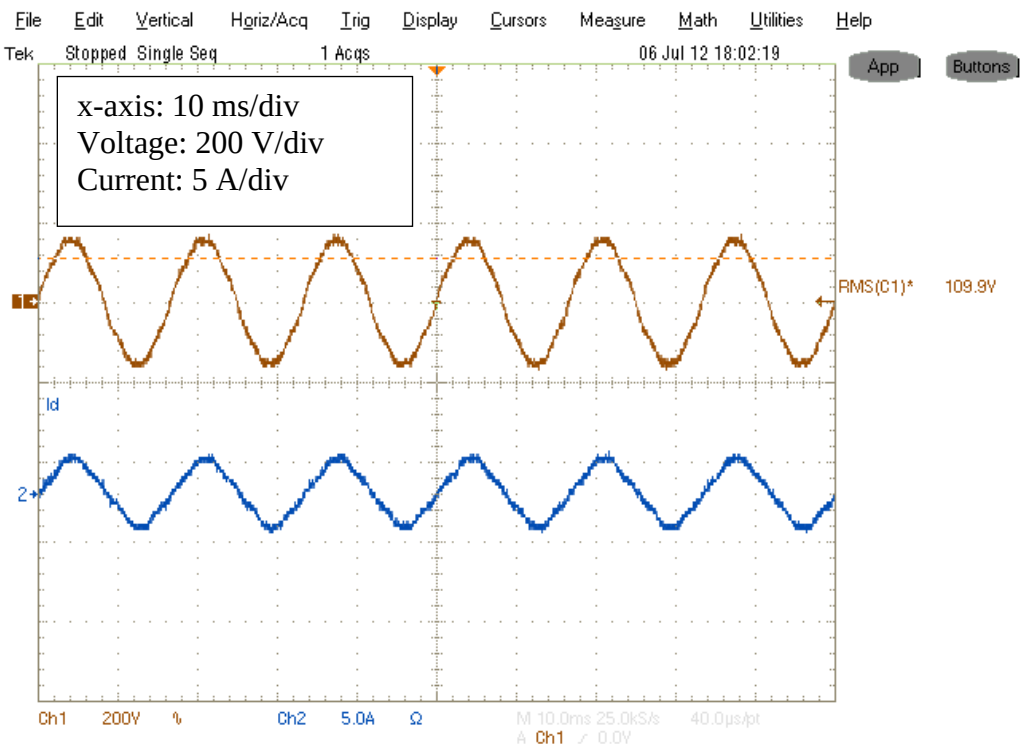


Fig. 4.41 Input voltage and current when V_{in} = 110 V and P_{load} = 150 W

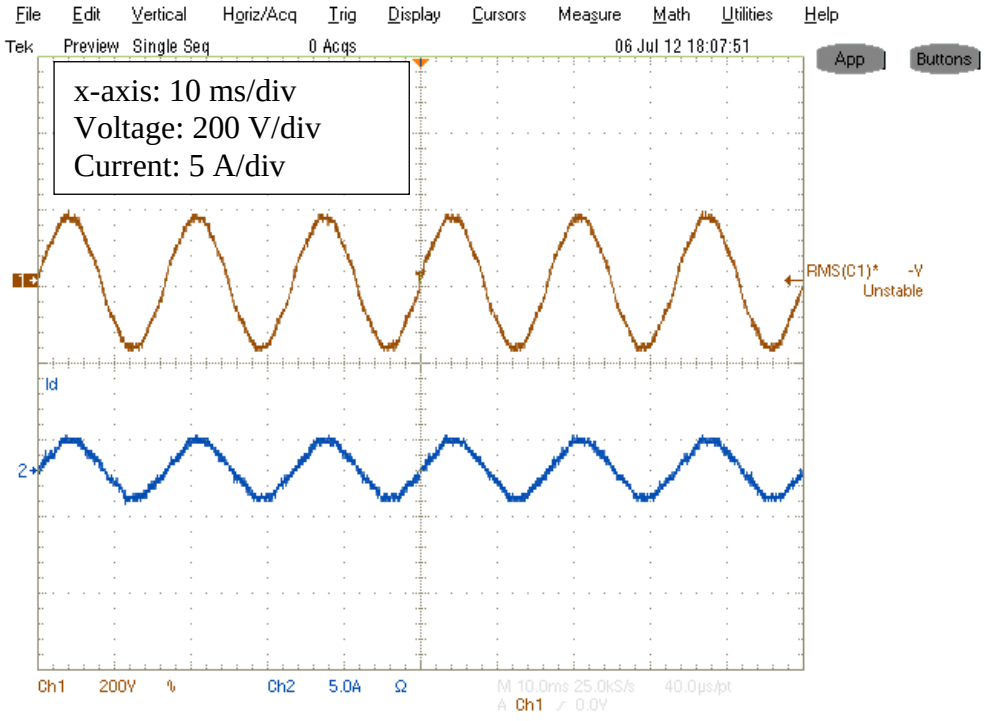


Fig. 4.42 Input voltage and current when V_{in} = 120 V and P_{load} = 150 W

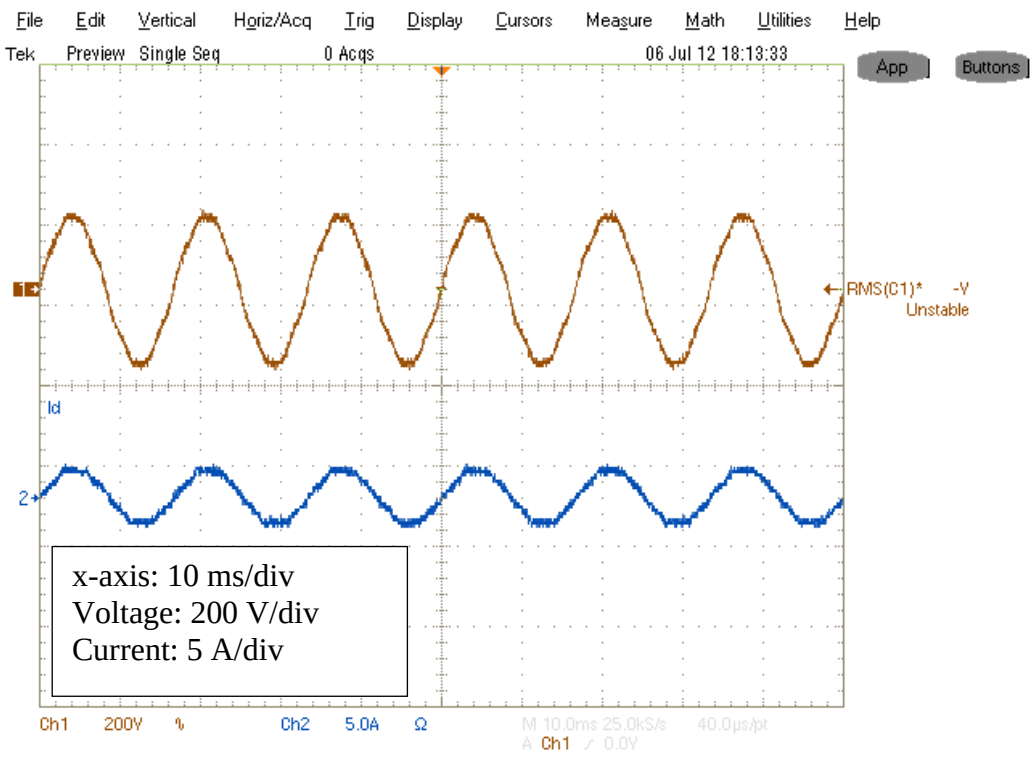


Fig. 4.43 Input voltage and current when V_{in} = 130 V and P_{load} = 150 W

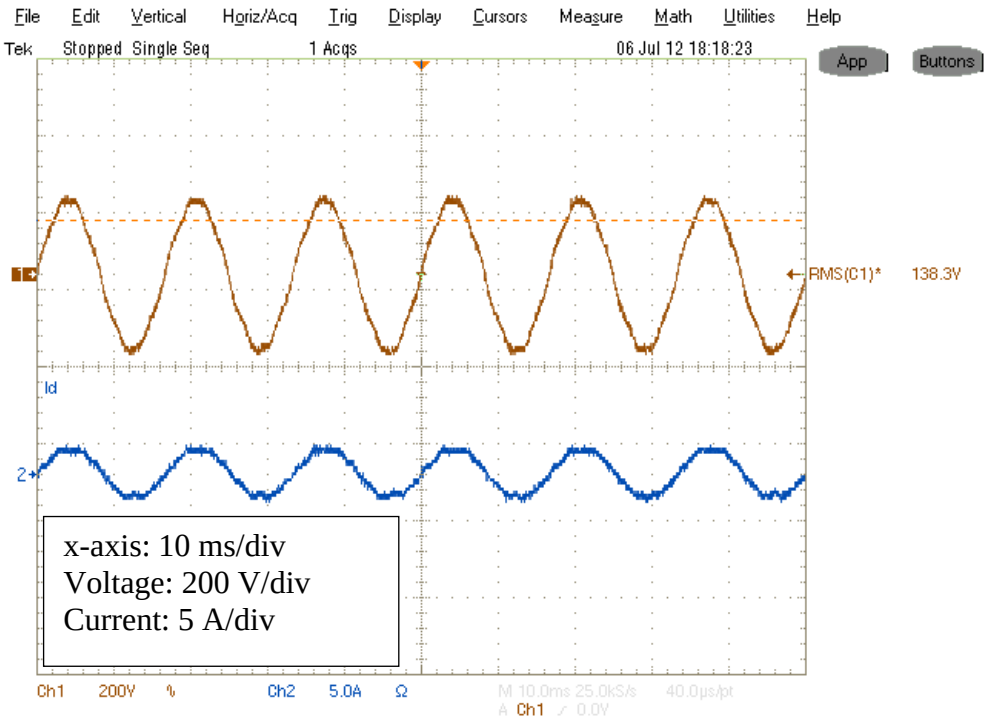


Fig. 4.44 Input voltage and current when V_{in} = 138 V and P_{load} = 150 W

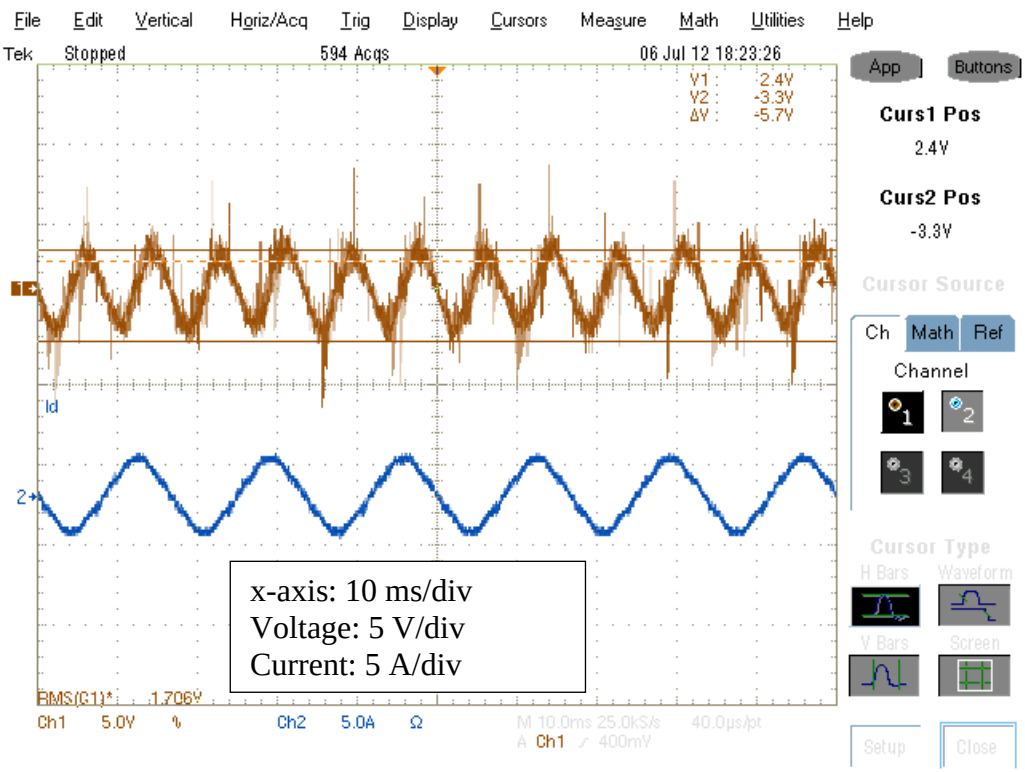


Fig. 4.45 Output voltage ripple and input current when V_{in} = 110 V and P_{load} = 150 W

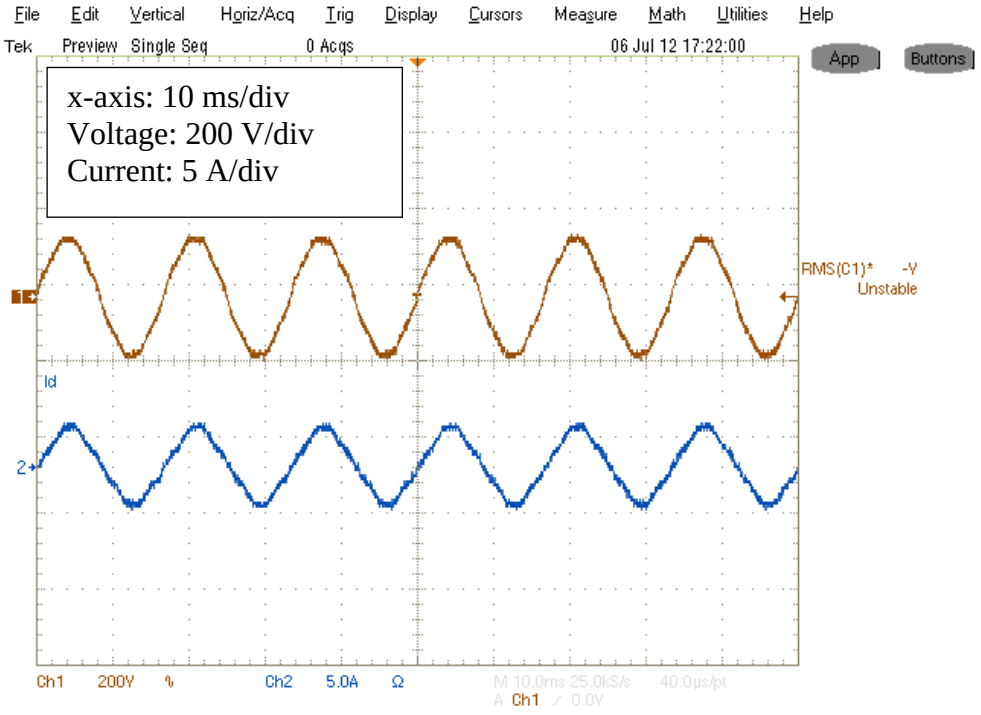


Fig. 4.46 Input voltage and current when V_{in} = 108 V and P_{load} = 175 W

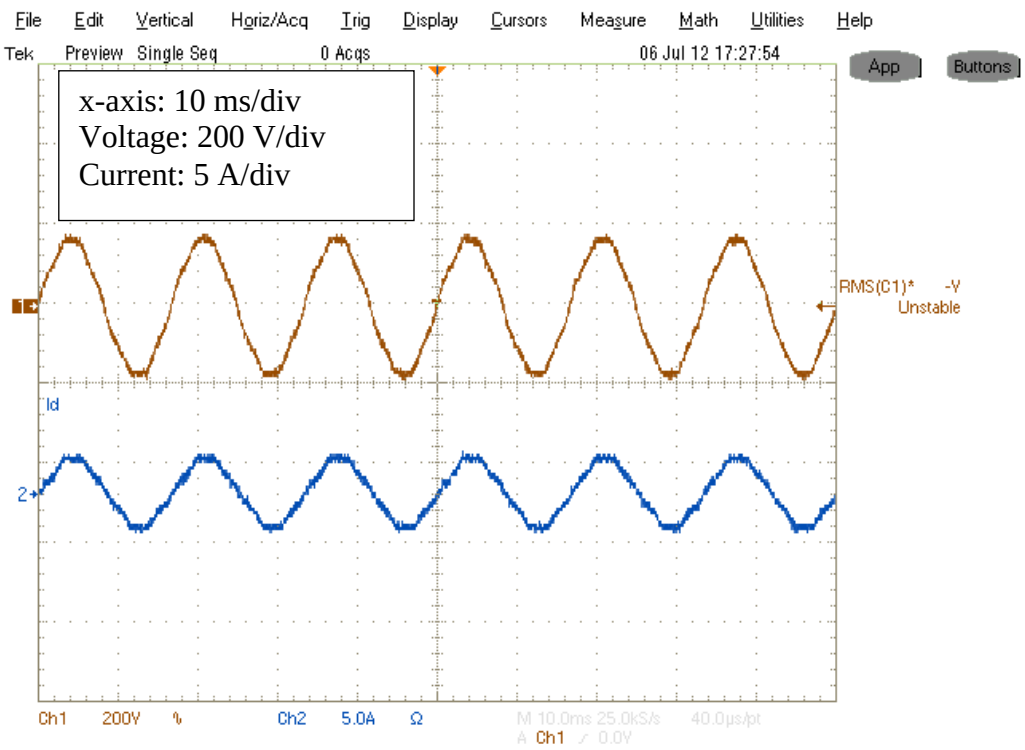


Fig. 4.47 Input voltage and current when V_{in} = 120 V and P_{load} = 175 W

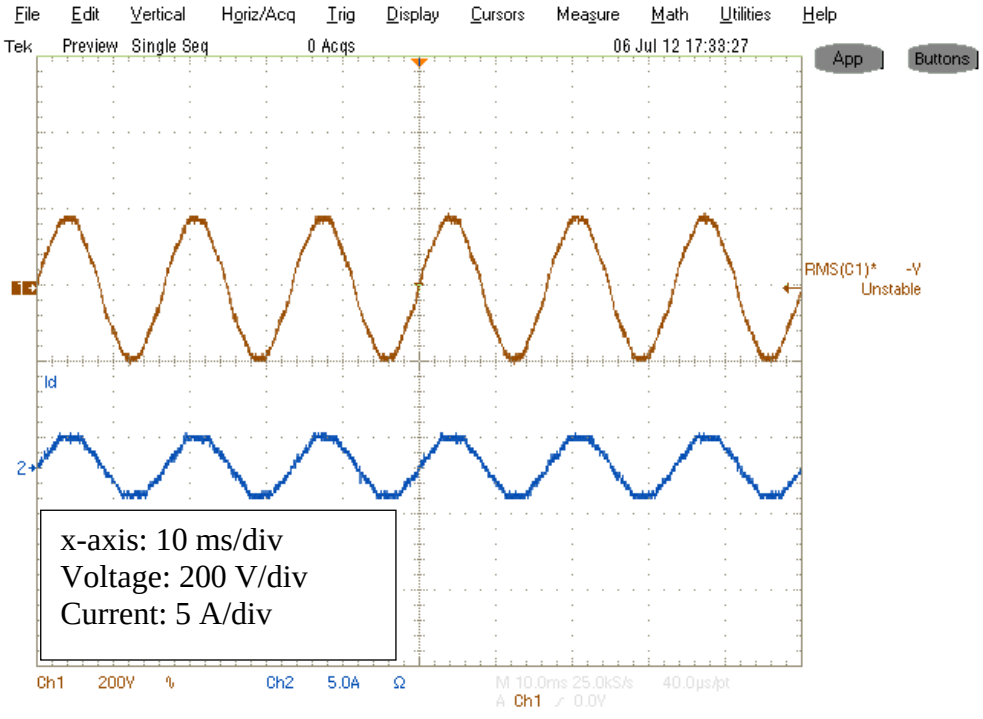


Fig. 4.48 Input voltage and current when V_{in} = 130 V and P_{load} = 175 W

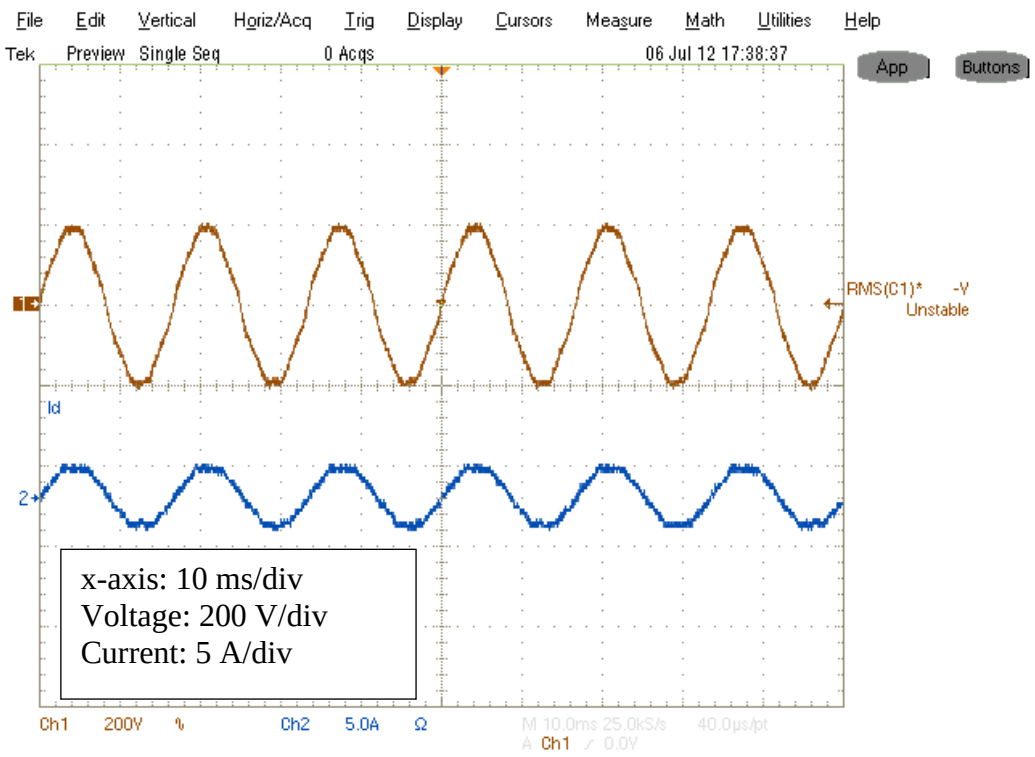


Fig. 4.49 Input voltage and current when V_{in} = 140 V and P_{load} = 175 W

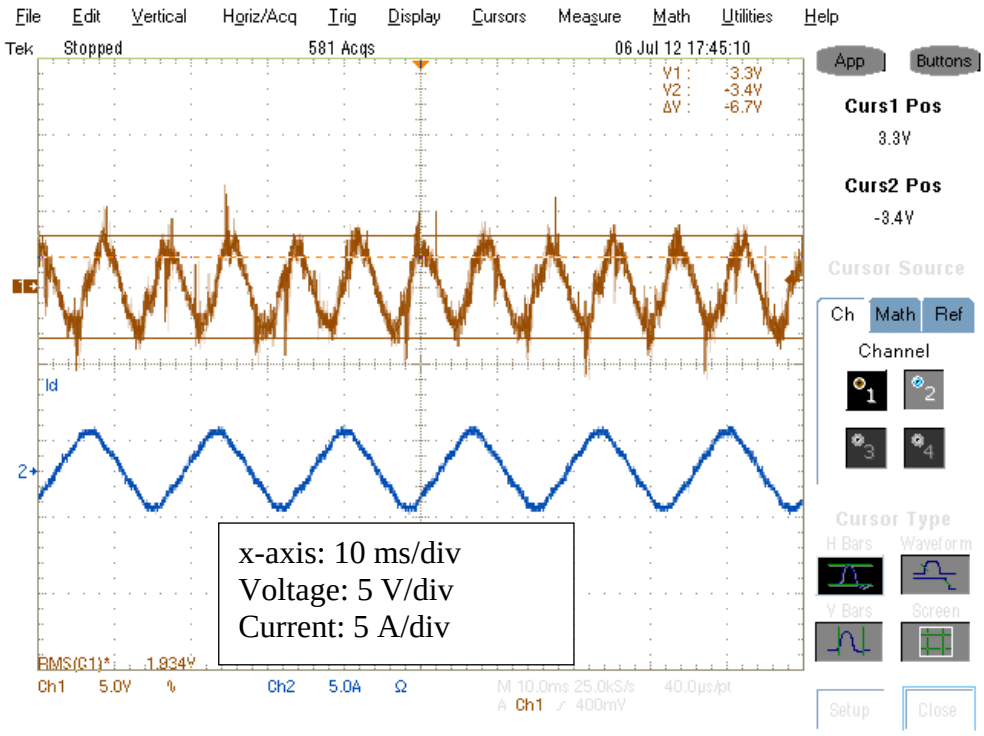


Fig. 4.50 Output voltage and input and current when V_{in} = 120 V and P_{load} = 175 W

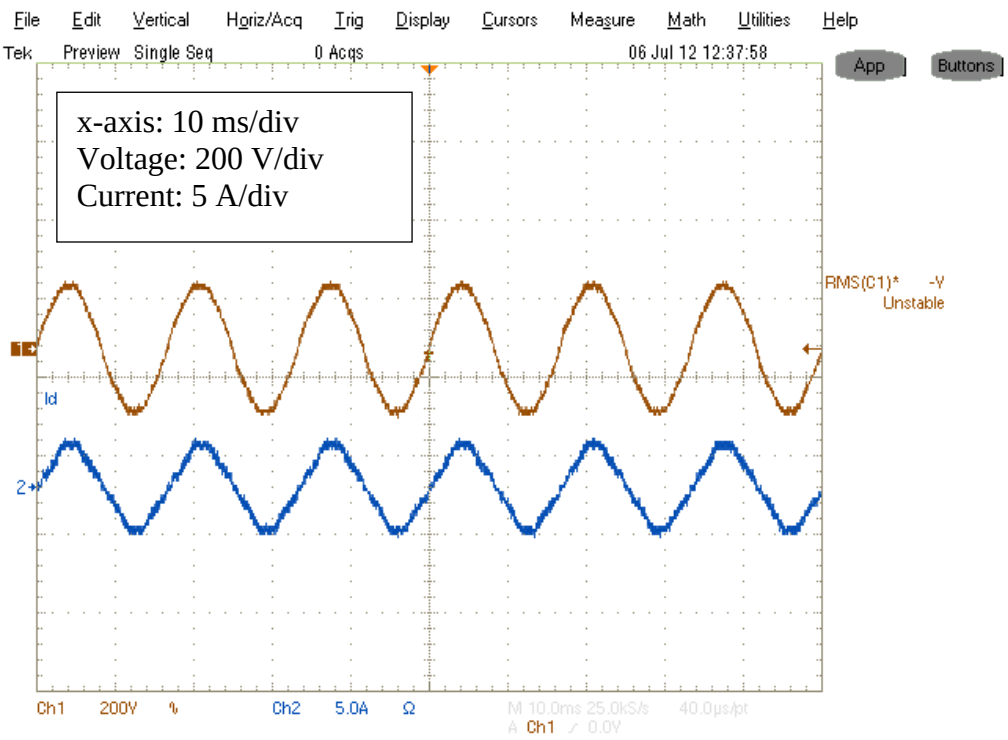


Fig. 4.51 Input voltage and current when V_{in} = 115 V and P_{load} = 200 W

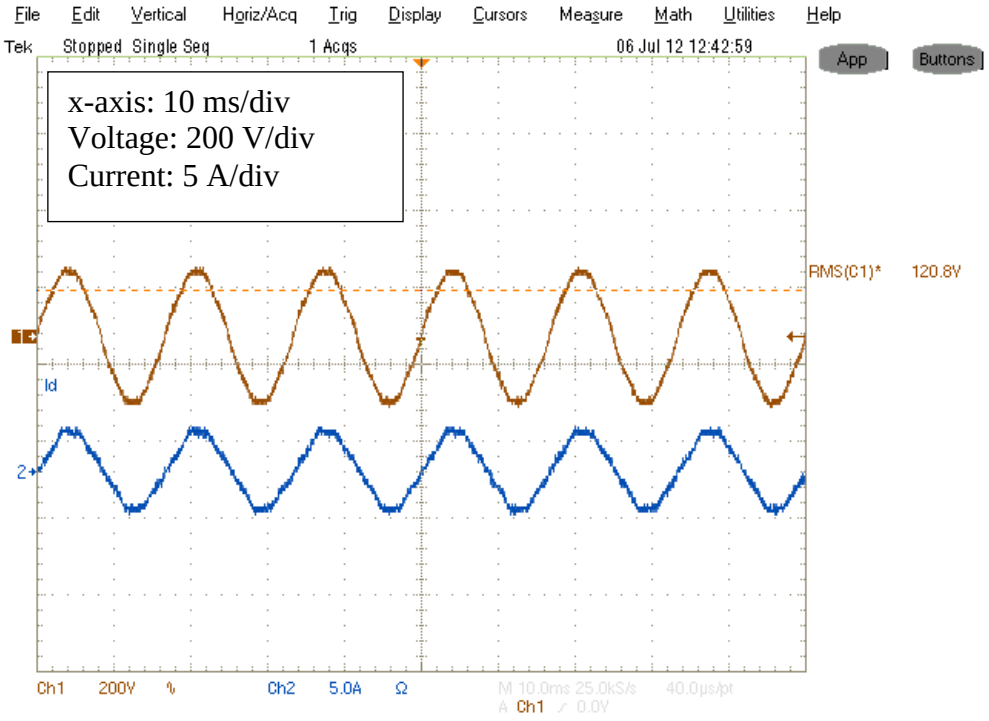


Fig. 4.52 Input voltage and current when V_{in} = 120 V and P_{load} = 200 W

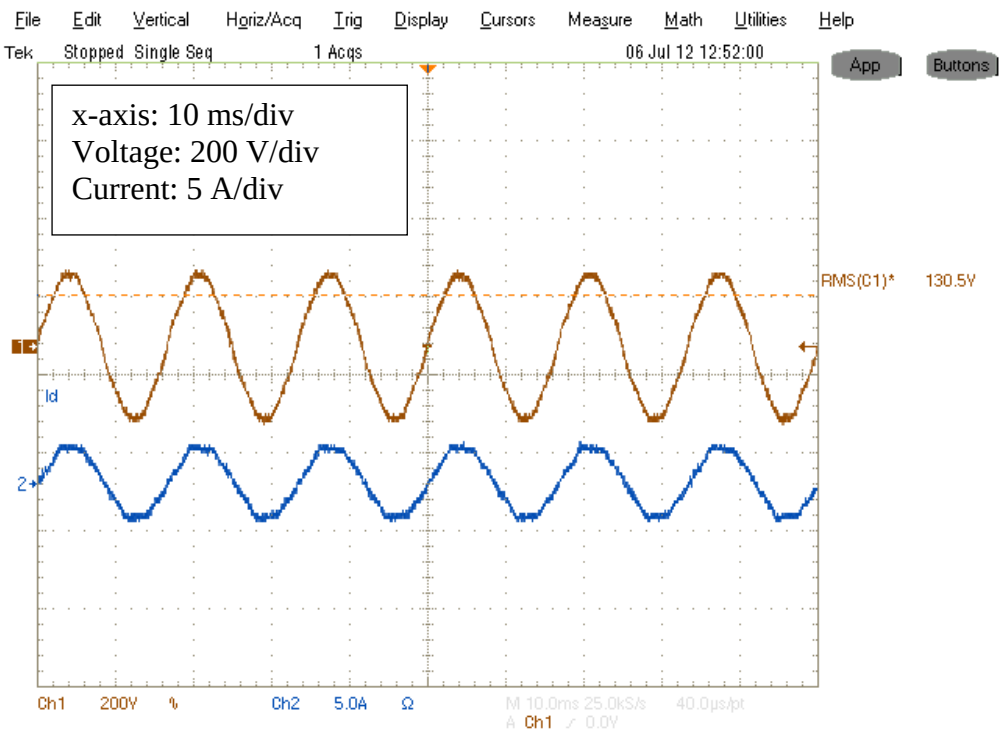


Fig. 4.53 Input voltage and current when V_{in} = 130 V and P_{load} = 200 W

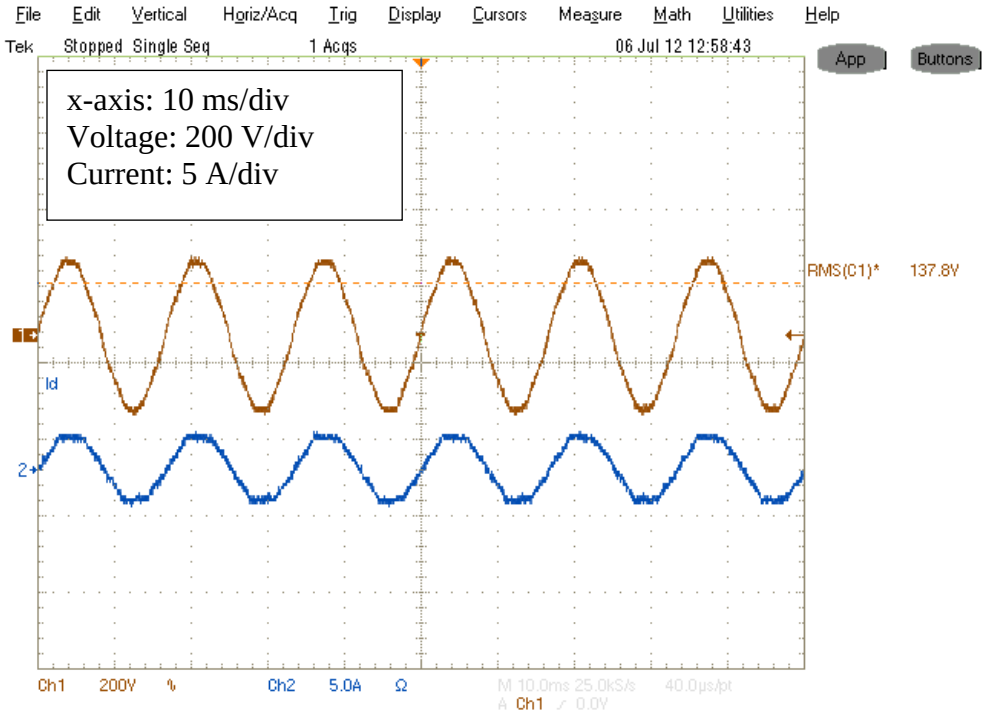


Fig. 4.54 Input voltage and current when V_{in} = 140 V and P_{load} = 200 W

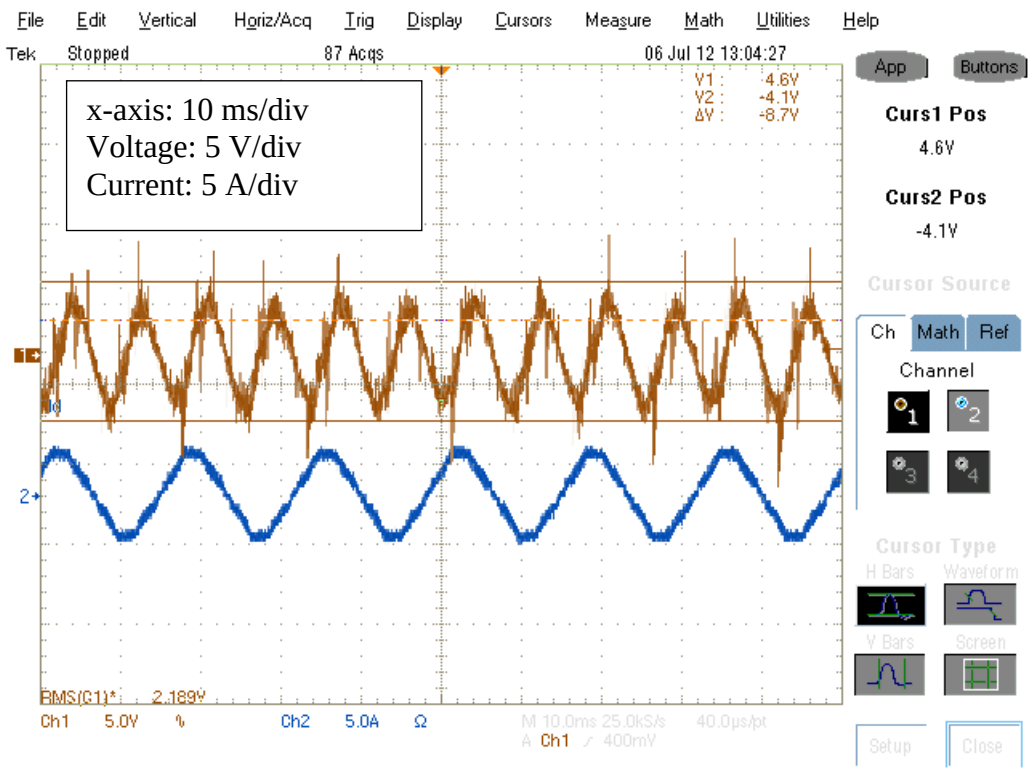


Fig. 4.55 Output voltage ripple and input current when V_{in} = 120 V and P_{load} = 200 W

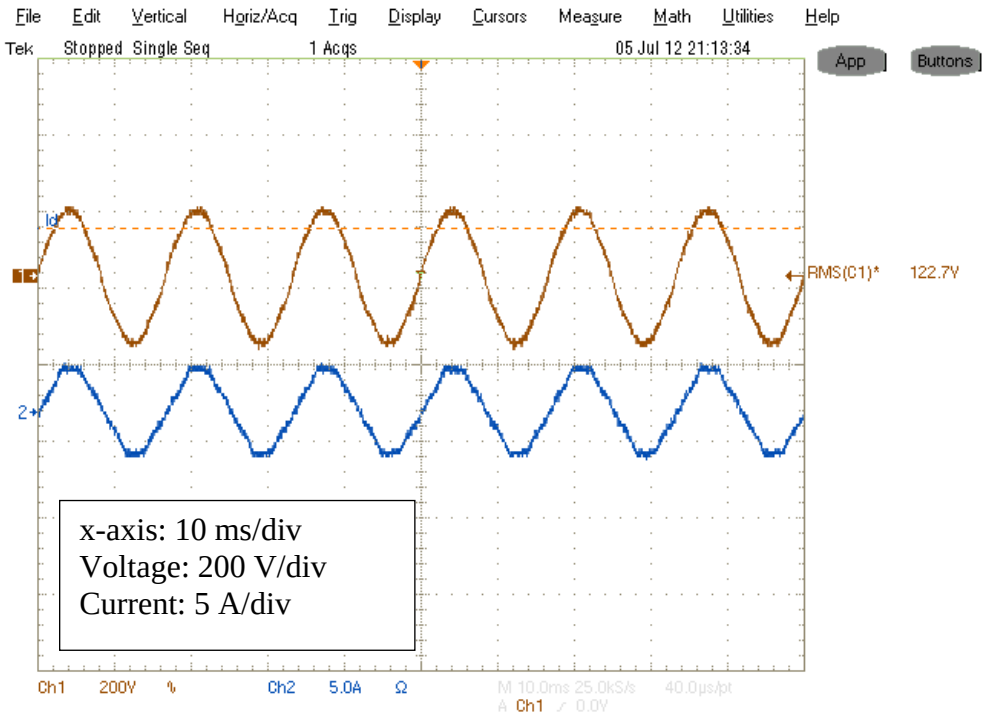


Fig. 4.56 Input voltage and current when V_{in} = 122 V and P_{load} = 225 W

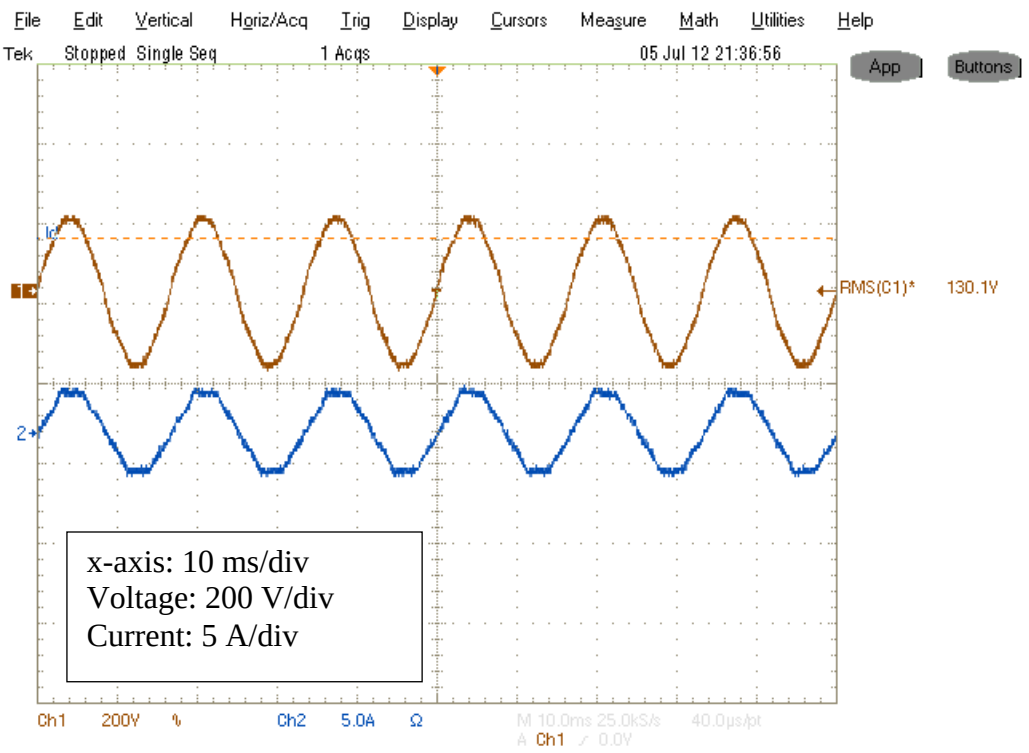


Fig. 4.57 Input voltage and current when V_{in} = 130 V and P_{load} = 225 W

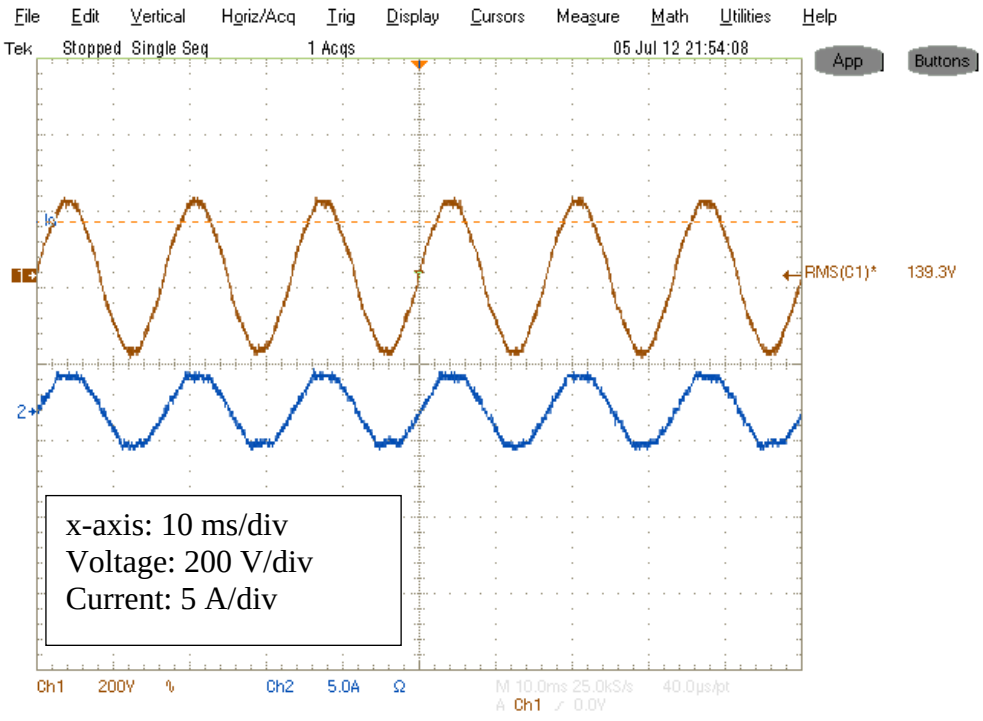


Fig. 4.58 Input voltage and current when V_{in} = 140 V and P_{load} = 225 W

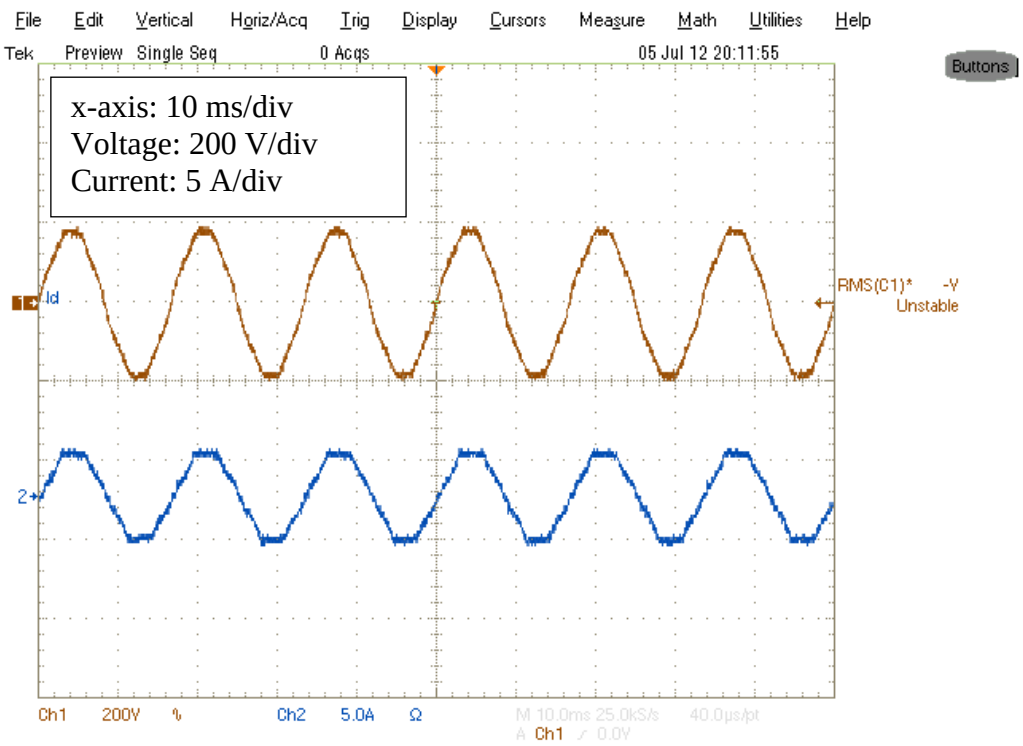


Fig. 4.59 Input voltage and current when V_{in} = 130 V and P_{load} = 250 W

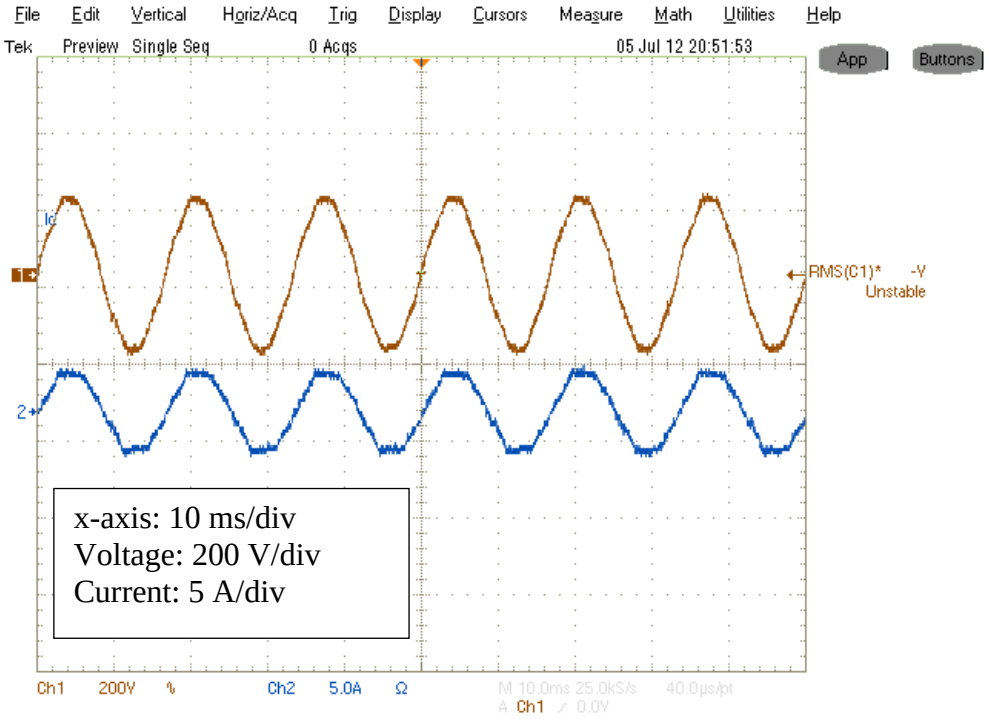


Fig. 4.60 Input voltage and current when V_{in} = 140 V and P_{load} = 250 W

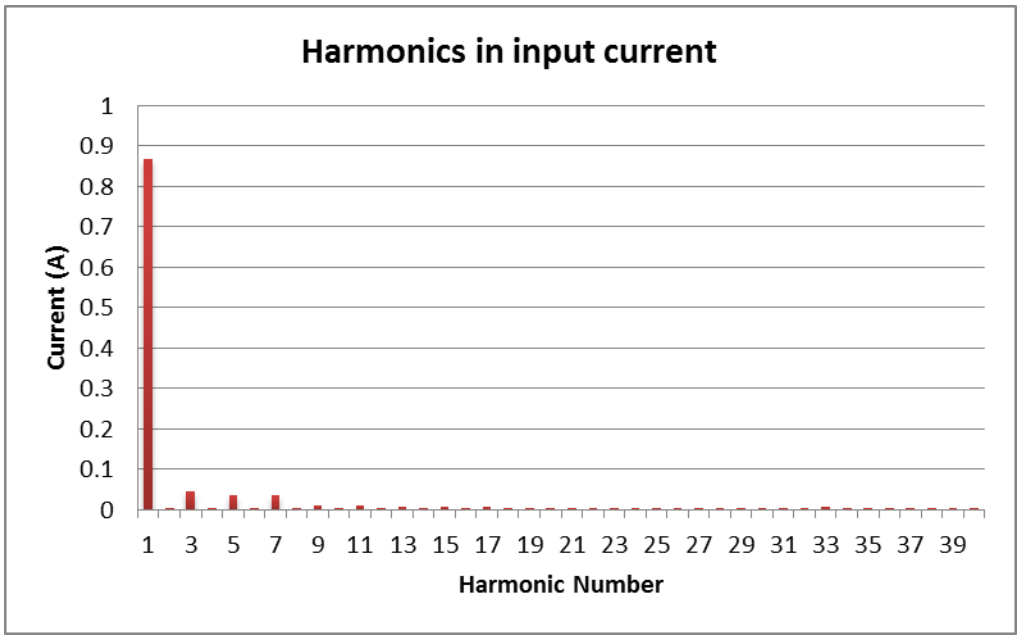


Fig. 4.61 Current harmonic spectrum when V_{in} = 120 V and P_{load} = 100 W

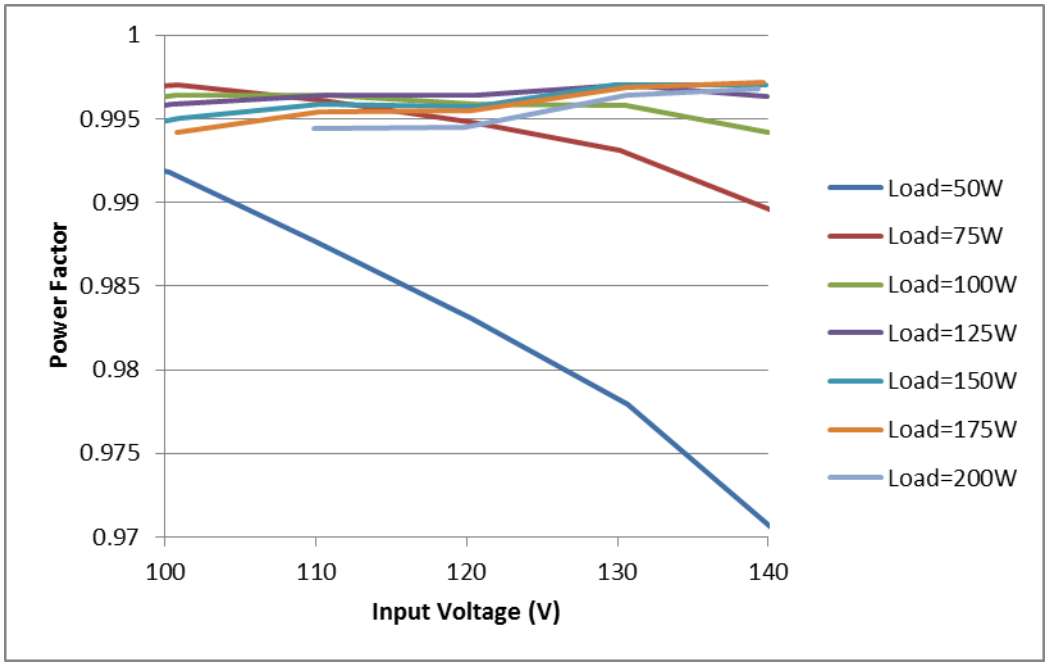


Fig. 4.62 Power Factor varying with input voltage and output load

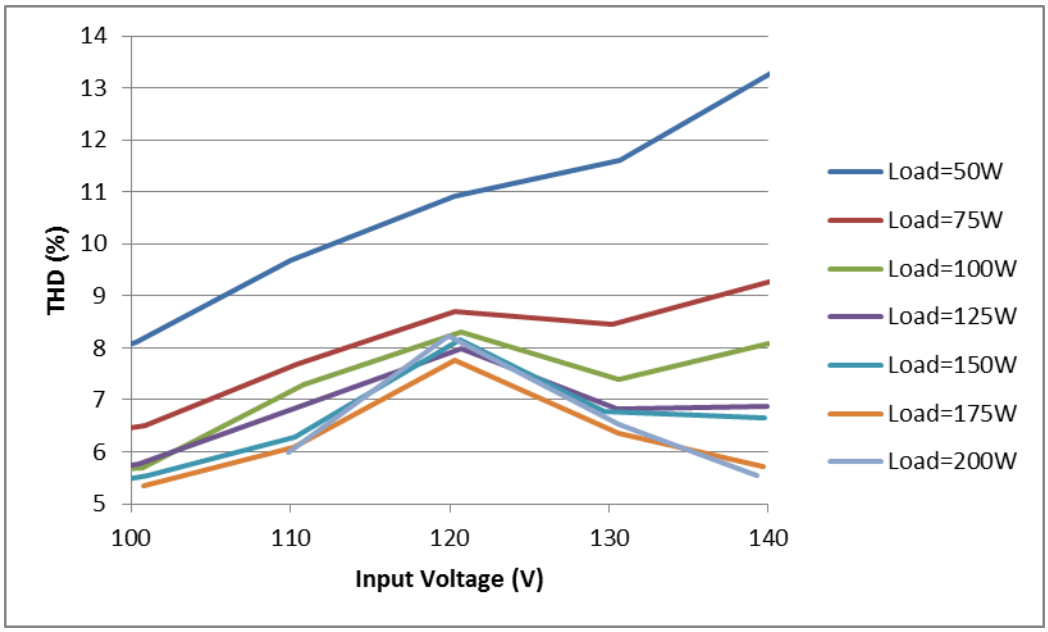


Fig. 4.63 Input current THD varying with input voltage and output load

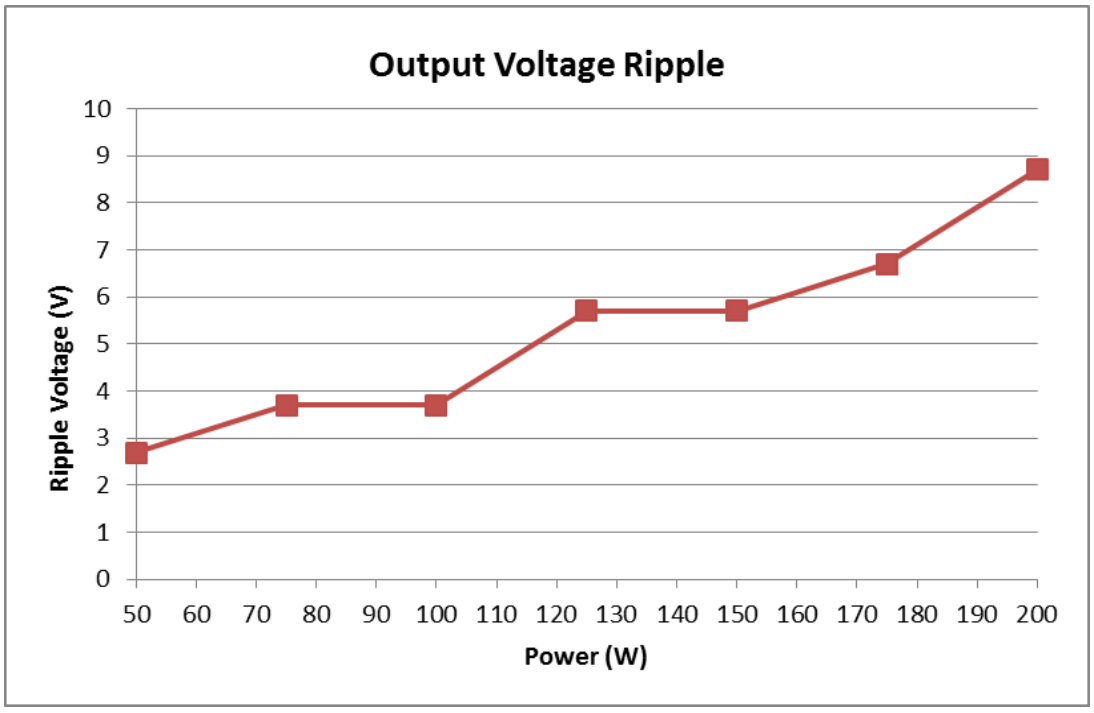


Fig. 4.64 Output voltage ripple varying with output load

CHAPTER 5

CONCLUSIONS AND FUTURE DIRECTIONS

Presented in this dissertation are the implementations of microcontroller-based active PFC pre-regulator systems with or without input voltage sensing. ACMC and hybrid control methods are employed in the implementations.

Typically, a microcontroller system is simpler, faster and cheaper than a DSP system or other kinds of digital hardware. Meanwhile, a microcontroller system has some hardware and software limitations. One purpose of this dissertation is to examine the practical solutions to control active PFC pre-regulators using low-cost microcontrollers. A typical PFC control system has three control loops: output voltage feedback loop, input voltage feedforward loop and inductor current feedback loop. By using the hybrid control approach, it is possible to integrate all three loops on a single microcontroller, as has been realized in this dissertation.

Another purpose of this dissertation is to investigate the feasibility of an active PFC pre-regulator without sensing the input voltage, while controlled by a low-cost microcontroller. The voltage feedforward loop and the multiplier can be realized by using the on-board DAC module properly.

A boost topology was selected as the PFC power stage, and the ACMC technique was utilized in this implementation. Small signal model and design considerations of the boost converter and ACMC controller were examined. An ACMC controller contains a

fast current loop and a slow voltage loop. A hybrid control method was employed such that one-chip solutions have been achieved to control active PFC pre-regulators with the ACMC technique; and PI controllers were designed to compensate the voltage loop. By using on-board analog peripherals, the current loop can be designed using analog components, and a pure digital controller can be implemented in the voltage loop.

Implementation issues for active PFC pre-regulators were discussed. These issues include power stage design, system modeling, as well as some considerations in hardware and software implementation. Two active PFC pre-regulators were constructed and verified by experimental results. The PIC16C782 microcontroller was used to control a PFC pre-regulator with input voltage sensing and another PFC pre-regulator without input voltage sensing. Experimental results encouragingly demonstrated satisfactory performance of the microcontroller-based active PFC pre-regulators.

Since this dissertation has proved the feasibility of microcontroller-based active PFC pre-regulator systems, one obvious future work is to apply the design principles described in this dissertation to other active PFC pre-regulator systems. Although only boost converters were implemented in this dissertation, many different topologies can be used to realize active PFC pre-regulator systems, and similar control scheme using ACMC hybrid method can be employed.

In this dissertation, the PIC16C782 microcontroller was selected to implement the control systems. However, this microcontroller has limited speed and computation capacity. Therefore, a more powerful microcontroller or DSP with appropriate analog peripherals can be used to implement active PFC pre-regulator systems. By using more advanced microcontroller or DSP, the digital controller will have higher computing

power and higher resolution, such that more advanced control techniques can be used with better performance.

According to the experimental observation, the active PFC pre-regulator without input voltage sensing is still susceptible to switching noise when the input current is at the zero crossing area in each 60 Hz cycle. Since the sensed inductor current is very tiny at zero crossing area, switching noise in the current loop may result in triggering the switch erroneously, and result in distortions in the inductor current. This problem is especially severe when the load is light.

In future research, this problem can be solved by using pure digital control for the whole control system, where the current-loop is also implemented digitally. With the improvement of digital technology, the cost of a DSP or high performance microcontroller is lower and lower with increasing speed and performance. Digital implementation of the current loop becomes feasible and cost-effective when the A/D conversion time and the calculation time are fast enough. Clean digital sinusoidal waveform in phase with input voltage can be obtained by manipulating sensed inductor current through a digital filter or digital phase lock loop.

Finally, because of the nonlinear characteristics of the active PFC system and the approximation of the linear model, the accuracy of the theoretical model needs further investigation, and more theoretical analysis and experimental testing needs to be performed to verify the theory.

BIBLIOGRAPHY

[1] Huai Wei, Batarseh, I., *Comparison of basic converter topologies for power factor correction*, Proceedings of IEEE SoutheastCon 1998, pp. 348-353, April 1998.

[2] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*, 2nd Edition, Kluwer Academic Publishers, 2001.

[3] P. T. Krein, *Elements of Power Electronics*, Oxford University Press, Inc., New York, NY, 1998.

[4] G. W. Deisch, "Simple Switching Control Method Changes Power Converter into a Current Source," Record of 1978 IEEE Power Electronics Specialists Conference, PESC 1978, pp. 300-306, June 1978.

[5] A. Capel, G. Ferrante, D. O'Sullivan and A. Weinberg, "Application of the Injected Current Model for the Dynamic Analysis of Switching Regulators with the New Concept of LC3 Modulator," Record of 1978 IEEE Power Electronics Specialists Conference, PESC 1978, pp. 135-147, June 1978.

[6] L.H. Dixon, "Average Current Mode Control of Switching Power Supplies," Unitrode Power Supply Design Seminar Handbook, Application Note U-140, 1990.

[7] J. Sun and R. M Bass, "Modeling and practical design issues for average current control," 14th Annual IEEE Applied Power Electronics Conference and Exposition, APEC 1999, Vol. 2, pp. 980-986, March 1999.

[8] Y.-S. Jung and M.-J. Youn, "Sampling effect in continuous-time small-signal modelling of average-current mode control," IEE Proceedings of Electric Power Applications, Vol. 149, No. 4, pp. 311 -316, July 2002.

[9] T. Suntio, J. Lempinen, I. Gadoura and K. Zenger, “Dynamic effects of inductor current ripple in average current mode control,” 32nd Annual IEEE Power Electronics Specialists Conference, PESC 2001, Vol. 3, pp. 1259-1264, June 2001.

[10] T. Suntio, M. Rahkala, I. Gadoura and K. Zenger, “Dynamic effects of inductor current ripple in peak-current and average-current mode control,” The 27th Annual Conference of the IEEE Industrial Electronics Society, IECON 2001, pp. 1072-1077, November 2001.

[11] P. Cooke, “Modeling average current mode control of power converters,” 15th Annual IEEE Applied Power Electronics Conference and Exposition, APEC 2000, Vol. 1, pp. 256-262, February 2000.

[12] C. Sun, B. Lehman and J. Sun, “Ripple effects on small signal models in average current mode control,” 15th Annual IEEE Applied Power Electronics Conference and Exposition, APEC 2000, Vol. 2, pp. 818-823, February 2000.

[13] C. Sun, B. Lehman and R. Ciprian, “Dynamic modeling and control in average current mode controlled PWM DC/DC converters,” 30th Annual IEEE Power Electronics Specialists Conference, PESC 1999, Vol. 2, pp. 1152 -1157, July 1999.

[14] Y.-S. Jung, J.-Y. Lee and M.-J. Youn; “A new small signal modeling of average current mode control,” Record of 29th Annual IEEE Power Electronics Specialists Conference, PESC 1998, Vol.2, pp. 1118 -1124, May 1998.

[15] W. Tang, F. C. Lee and R. B. Ridley, “Small-signal modeling of average current-mode control,” IEEE Transactions on Power Electronics, Vol. 8, No. 2, pp. 112 -119, April 1993.

[16] W. Tang, F. C. Lee and R. B. Ridley, “Small-signal modeling of average current-mode control,” Proceedings of 7th Annual IEEE Applied Power Electronics Conference and Exposition, APEC 1992, pp. 747 -755, February 1992.

[17] R. B. Ridley, “A New, Continuous-Time Model for Current-Mode Control,” IEEE Transactions on Power Electronics, Vol. 6, No. 2, pp. 271-280, April 1991.

[18] R. B. Ridley, “A New, Continuous-Time Model for Current-Mode Control,” Virginia Polytechnic Institute and State University, PhD Thesis, April 1990.

[19] R. B. Ridley, “A New Continuous-Time Model for Current-Mode Control with Constant Frequency, Constant On-Time, and Constant Off-Time, in CCM and DCM,” Record of 21st Annual IEEE Power Electronics Specialists Conference, PESC 1990, pp. 382 -389, June 1990.

[20] L.H. Dixon, “High power factor preregulators for off-line power supplies,” Unitrode Seminar Manual SEM700, Sec. 12, pp. 1-16, 1990.

[21] Texas Instruments, “High Power Factor Preregulator”, UC1854/UC2854/UC3854 Data Sheet, September 2011.

[22] Philip C. Todd, “UC3854 Controlled Power Factor Correction Circuit Design”, Unitrode Application Note U-134, 1999.

[23] A. Prodic, J. Chen, R. W. Erickson, and D. Maksimovic, “Self-tuning digitally controlled low-harmonic rectifier having fast dynamic response,” IEEE Transactions on Power Electronics, Vol. 18, No. 1, pp. 420–428, January 2003.

[24] Jingquan Chen, Aleksandar Prodić, Robert W. Erickson and Dragan Maksimović, “Predictive digital current programmed control,” IEEE Transactions on Power Electronics, Vol. 18, No. 1, pp. 441-419, January 2003.

[25] W. Zhang, G. Feng, Y.-F. Liu, B. Wu, “DSP implementation of predictive control strategy for power factor correction (PFC),” 19th Annual IEEE Applied Power Electronics Conference and Exposition, APEC 2004, Vol. 1, pp.67-73, 2004.

[26] W. Zhang, G. Feng, Y.-F. Liu, and B. Wu, “A digital power factor correction (PFC) control strategy optimized for DSP,” IEEE Transactions on Power Electronics, Vol. 19, No. 6, pp. 1474–1485, Nov. 2004.

[27] C. P. Henze and N. Mohan, “A Digitally Controlled AC to DC Power Conditioner that Draws Sinusoidal Input Current”, Record of 1986 IEEE Power Electronics Specialists Conference, PESC 1986, pp. 531-540, 1986.

[28] Christopher P. Henze, “Digitally Controlled A.C. to D.C. Power Conditioner,” United States Patent 4,761,725, August 2, 1988.

[29] A. H. Mitwalli, S. B. Leeb, G. C. Verghese, and V. J. Thottuvelil, "An Adaptive Digital Controller for a Unity Power Factor Converter," IEEE Transactions on Power Electronics, Vol. 11, No. 2, pp. 374–382, March 1996.

[30] L. T. Jakobsen, N. Nielsen, C. Wolf and M.A.E. Anderson, "Hybrid Control Method for a Single Phase PFC using a Low Cost Microcontroller," Proceedings of the 20th Annual IEEE Applied Power Electronics Conference and Exposition, APEC 2005, Vol. 3, pp. 1710-1715, March 2005.

[31] Microchip Technology Inc., "8-Bit CMOS Microcontrollers with A/D, D/A, OPAMP, Comparators and PSMC," Microchip PIC16C781/782 Data Sheet, 2001.

[32] D. He and R.M. Nelms, "Peak Current-Mode Control for a Boost Converter Using an 8-bit Microcontroller," Proceedings of 34th Annual IEEE Power Electronics Specialists Conference , PESC 2003, pp. 938-942, June 2003.

[33] D. He and R.M. Nelms, "Average Current-Mode Control for a Boost Converter Using an 8-bit Microcontroller," Proceedings of the 2004 IEEE International Symposium on Industrial Electronics , ISIE 2004, pp. 1185-1190), May 2004.

[34] D. He and R.M. Nelms, "Current-Mode Control of a DC-DC Converter Using a Microcontroller: Implementation Issues," Proceedings of the 4th International Power Electronics and Motion Control Conference, IPEMC 2004, Vol. 2, pp. 538-543, August 2004.

[35] D. He and R. M. Nelms, "Fuzzy Logic Average Current-Mode Control for DC-DC Converters Using an Inexpensive 8-Bit Microprocessor," Conference Records of 39th IEEE Industry Applications Society Annual Meeting, IAS 2004, pp. 2615-2622, October 2004.

[36] D. He and R. M. Nelms, "Fuzzy Logic Peak Current-Mode Control for DC-DC Converters Using an Inexpensive 8-Bit Microprocessor," Proceedings of the 20th IEEE Applied Power Electronics Conference and Exposition, APEC 2005, pp. 2000-2006, March 2005.

[37] Yijing Chen, Dake He and R. M. Nelms, "Control of a Single Phase PFC Preregulator Using an 8-Bit Microcontroller," Proceedings of the 22nd Annual IEEE Applied Power Electronics Conference and Exposition, APEC 2007, pp. 1454-1460, February 2007.

[38] The MathWorks, Inc., MATLAB 6.0 Help on Continuous/Discrete Conversions, The MathWorks, Inc., 2000.

[39] The MathWorks, Inc., *Control System Toolbox for Use with MATLAB*, The MathWorks, Inc., 2000.

[40] Dake He, "Microcontroller-Based Current-Mode Control for Power Converters", Ph.D. Dissertation, Auburn University, December 2005.

[41] Lloyd Dixon, "High Power Factor Switching Preregulator Design Optimization", Unitrode Power Supply Design Seminar Manual, SEM800, 1991.

[42] D. Maksimovic, Y. Jang and R. Erickson, "Nonlinear–Carrier Control for High-Power-Factor Boost Rectifier," IEEE Transactions on Power Electronics, Vol. 11, No. 4, pp. 578-584, July 1996.

[43] R. Zane and D. Maksimovic, "Nonlinear –Carrier Control for High Power Factor Rectifiers Based on Flyback, Cuk or Sepic Converters," Proceedings of the 11th Annual IEEE Applied Power Electronics Conference and Exposition, APEC1996, pp. 814-820, March 1996.

[44] Regan Zane and Dragan Maksimovic, "Nonlinear-Carrier Control for High-Power-Factor Rectifiers Based on Up–Down Switching Converters", IEEE Transactions on Power Electronics, Vol. 13, No. 2, pp. 213 – 221, March 1998.

[45] Jay Rajagopalan, Fred C. Lee and Paolo Nora, "A General Technique for Derivation of Average Current Mode Control Laws for Single-Phase Power-Factor-Correction Circuits Without Input Voltage Sensing," IEEE Transactions on Power Electronics, Vol. 14, No. 4, pp. 663-672, July 1999.

[46] S. Ben-Yaakov, "PWM Converters with resistive Input," IEEE Transactions on Industrial Electronics, Vol. 45, No. 3, pp. 519-520, June 1998.

[47] S. Ben-Yaakov and I. Zester, "The Dynamics of a PWM Converter with resistive Input," IEEE Transactions on Industrial Electronics, Vol. 46, No. 3, pp. 613-619, June 1999.

[48] B. Mather, B. Ramachandran and D. Maksimovic, “A Digital PFC Controller without Input Voltage Sensing,” Proceedings of the 22nd Annual IEEE Applied Power Electronics Conference, APEC 2007, pp. 198-204, February 2007.