Small Signal Equivalent Circuit Extraction and RF Noise Analysis in 28nm High-k/Metal Gate RF CMOS

by

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Abstract

This work extracts RF noise in a 28nm high-k/metal gate RF CMOS technology using a small signal equivalent circuit. All extrinsic and intrinsic small-signal parameters are extracted from measured data as well as scaling result of each parameters. For noise analysis, $S_{id}/4kTg_{d0}$ is extracted, and its intrinsic value remains less than 2 despite a large increase from 1 at 90nm gate length, as well as a much stronger increase with V_{DS}. The gate resistance noise is shown to be a significant noise performance limiter in such technology due to a large vertical metal interface component that is inversely proportional to gate area, $W \times L$.

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Chapter 1

Introduction

1.1 Trend in RF CMOS

RF CMOS is widely used to implement for high-frequency integrated circuits for its high speed and high level of integration. Accurate models are critical in order to reduce design cycles and to achieve first-time success in implementation. Moreover, the understanding and modelling of noise is essential for the usage of highly scaled CMOS in RF circuit application.

As the Moore's law drives CMOS density integration, a drastic down-scaling of the transistor sizes, in order to increase the performance and to decrease the cost [3], has been required during the last four decades. During this period, the transistor's minimum layout dimensions have decreased by a factor of more than 200. More generally, the dimensions of transistor from one technology to another one decreased by a factor of 0.7. As the silicon dioxide insulator thickness(T_{OX}) becomes increasingly thinner, a DC gate leakage current related to the tunnelling effect occurs, which is critical for both digital and analog applications. In order to get rid of such a gate leakage current, the solution lies in the replacement of classical poly-Si gate/SiO_2 gate stack by High-k/Metal Gate(H-k/MG) ones [4].

The recent introduction of new Gate stack using High-k dielectrics and Metal Gate (H-k/MG) for CMOS has been a key point to downscale the "equivalent oxide thickness" (EOT). Within this context, this work investigates RF noise performance of 28-nm H-k/MG CMOS Technology using small-signal equivalent circuit based on parameter extraction and noise de-embedding.

1.2 Small signal model of MOSFET transistor

Small-signal equivalent circuit accurately modelling both AC and noise characteristics of MOSFET is very useful for RF circuit design as well as understanding of device physics. The topology of equivalent circuit determines the physics effects that can be accounted for, accuracy of final AC and noise characteristics, and affects circuit parameter extraction procedure as well as the physical soundness of extracted equivalent circuit parameters [7].

1.2.1 Useful effect

The useful effect of a MOSFET is its ability to control its output current(i_{ds}) when a voltage is applied to the gate(v_{gs}). This behavior can be modelled using a voltage controlled current source connected between the device source and drain. A preliminary equivalent circuit, modelling the useful effect of the device, can be drawn (Fig. 1.1).

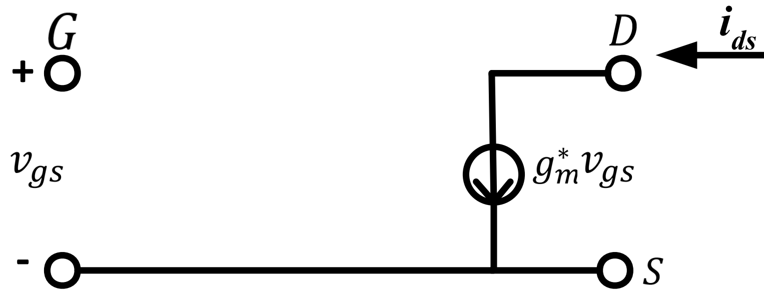

Figure 1.1: Small signal model of the useful effect of MOSFET.

G, D and S represent gate, drain and source node, respectively. The transconductance(g_m) is qualified as intrinsic element, because it is simple representation of the physical phenomenon, that occurs inside of the transistor channel. The transconductance is defined as follow:

$$g_m^* = \frac{\partial I_{DS}}{\partial V_{GS}} \tag{1.1}$$

where I_{DS} is simply drain current and V_{GS} refers to gate voltage.

Even if it denotes the useful effect of the MOSFET, the equivalent circuit of Fig. 1.1 is not efficient enough to describe the behavior of the device if the operation frequency is raised, as no parasitic elements are taken into account.

1.2.2 Extrinsic and intrinsic capacitances

We should take capacitance between every two terminals into consideration.

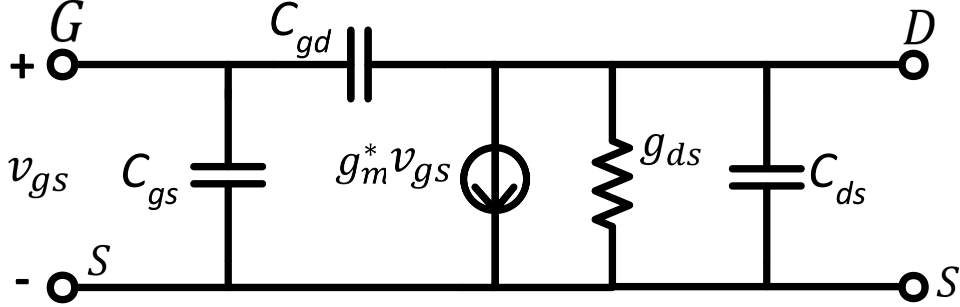

Figure 1.2: MOSFET including capacitances.

As shown in Fig. 1.2, g_{ds} is an output conductance representing channel resistance. C_{gs}, C_{gd} and C_{ds} are the lumped capacitances between gate and source node, gate and drain node, drain and source node, respectively. Each of them is composed of extrinsic and intrinsic components:

$$C_{gs} = C_{gsx} + C_{gsi} \tag{1.2}$$

$$C_{gd} = C_{gdx} + C_{gdi} \tag{1.3}$$

$$C_{ds} = C_{dsx} + C_{dsi} \tag{1.4}$$

The intrinsic elements(C_{gsi}, C_{gdi} and C_{dsi}) are within intrinsic circuit, which depend on the device dimension and on the applied bias. They are named intrinsic capacitances and noted with index "i". Because of its geometry, some extrinsic elements(C_{gsx}, C_{gdx} and C_{dsx}) are surrounding the active part of the device and they are mainly bias independent

and proportional to the transistor width. They are named extrinsic capacitances and noted with index "x".

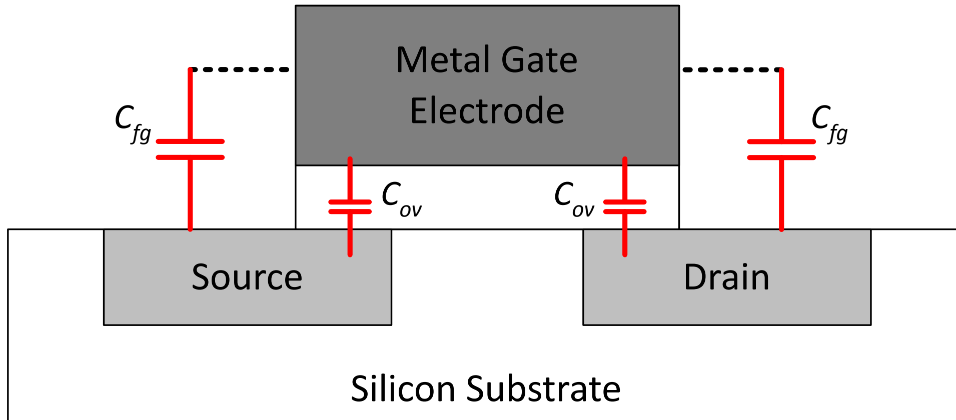

Figure 1.3: Location of components of extrinsic capacitances in cross section of MOSFET.

Fig. 1.3 shows the extrinsic gate to source (C_{gse}) and gate to drain (C_{gde}) capacitances are composed of two different elements. They include overlap capacitances C_{ov}, located between the gate oxide and the diffusion of the source and the drain under the gate, and fringing capacitances C_{fg} from the gate sides to the source and drain implants. Note that C_{ov} is independent of length and C_{fg} depends on length, which will be discussed in following chapter.

1.2.3 Extrinsic resistances

As shown in Fig. 1.4, there are three extrinsic resistances connected to outside of capacitance of previous small signal circuit. These distributed elements are modelled by using lumped resistances called R_g, R_s and R_d. They are connected to the gate, the source, and the drain terminal, respectively.

In traditional layout, the resistances R_d and R_s include the metallic losses and the contact resistances between the metal and the source and drain implants. They are proportional to the inverse of the transistor width. The resistance R_g includes the resistance of the gate

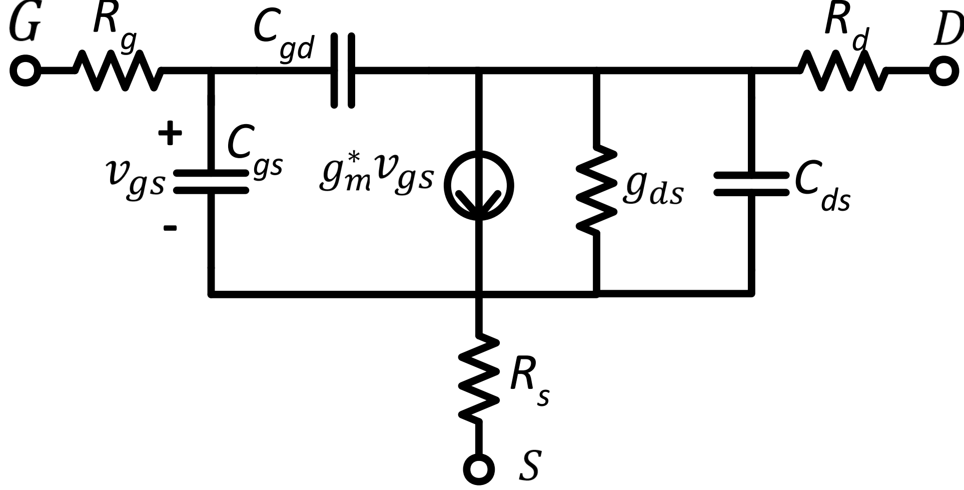

Figure 1.4: MOSFET with extrinsic capacitances and distributed resistance connected to terminals.

fingers, which is proportional to the transistor width, and the resistance of some metallic lines. In most of the cases, the resistance of the gate finger is much higher than the others.

1.2.4 Substrate network

Lots of issues need to be considered for an accurate RF MOSFET model. A substrate network is generally introduced to describe the resistive path in the well from the intrinsic body node to the body contact. Especially, the substrate resistance significantly affects the small signal output characteristics of MOSFETs at high frequencies.

As shown in Fig. 1.5, the effect of substrate parasitics is described by subcircuit extension of the conventional MOSFET model using a simple lumped substrate resistance R_{sub} and one capacitance between junction and drain called C_{jd}.

1.2.5 The equivalent circuit used in this research

The small signal equivalent circuit we used is shown in Fig. 1.6. The intrinsic and extrinsic capacitance between gate, source and drain terminal are lumped respectively as C_{gs}, C_{gd} and C_{ds}. For convenient extraction, the intrinsic and extrinsic region have also been

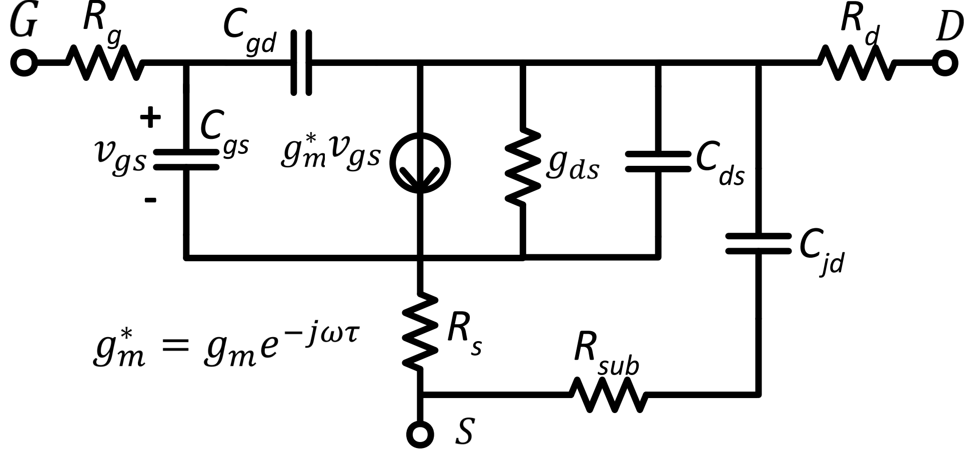

Figure 1.5: Equivalent circuit of RF MOSFET including substrate network.

labelled: the components in the intrinsic region have bias dependence and the components in the extrinsic region other than in intrinsic region should be independent of bias. The regions labelled by "Block *I*" and "Block *II*" are just used to perform extraction for convenience. Finally, the pad and interconnect parasitics are not drawn in this diagram which should be initially removed by open-short de-embedding process.

1.3 Noise parameters for two-port network

This section aims to introduce different noise representation for a linear noisy two-port network. The transformation between one noise matrix to another is also presented, which will frequently used in following noise parameter extraction and noise de-embedding process.

1.3.1 Measured noise parameters

The noise level of two-port networks can be measured in terms of "Noise Factor", F, which is defined as:

$$F = \frac{(SNR)_{input}}{(SNR)_{output}}. \tag{1.5}$$

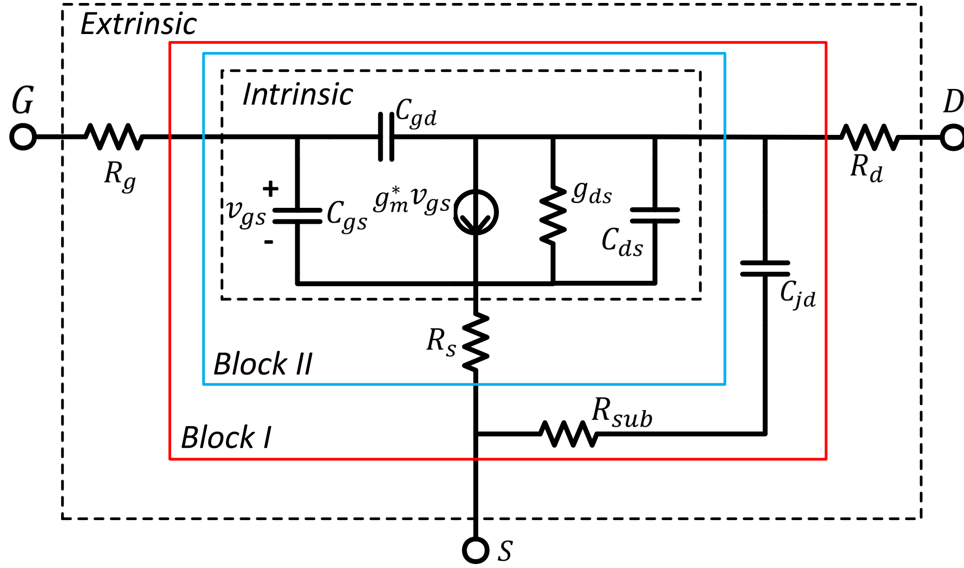

Figure 1.6: The small signal equivalent circuit for parameter extraction and noise de-embedding at on-state bias.

where SNR is the signal-to-noise power ratio. F is usually measured in dB and its value is referred as the “Noise Figure”, NF according to [6]:

$$NF = 10\log_{10}(F). \tag{1.6}$$

The noise figure of a two-port network is determined by the source admittance $Y_S = G_S + jB_S$, and the noise parameters of the circuit, including the minimum noise figure NF_{min}, the noise resistance R_n and the optimum source admittance $Y_{opt} = G_{opt} + jB_{opt}$, through [6]

$$F = F_{min} + \frac{R_n}{G_S}|Y_S - Y_{opt}|^2, \tag{1.7}$$

$$NF_{min} = 10\log_{10}(F_{min}), \tag{1.8}$$

The noise parameters can be measured using noise measurement facilities, and their meanings can be explained as follows:

1. F_{min}, the minimum noise factor. Its value in dB is the so called minimum noise figure NF_{min}, i.e. $10\log_{10}(F_{min})$.

2. R_n, the noise resistance, is commonly normalized by the intrinsic impedance $Z_0 = 50\Omega$, and thus is unitless.

3. Y_{opt}, the optimum noise matching admittance, is a complex number with a real part G_{opt} and an imaginary part B_{opt}. Its inverse value is denoted as Z_{opt}. Experimentally, the reflection coefficient Γ_{opt} is measured instead of Y_{opt}. Note that $\Gamma_{opt} = Mag \cdot e^{(jAngle/180\pi)}$. Y_{opt} can be obtained from Γ_{opt} as [6]

$$Y_{opt} = \frac{1}{Z_0}\frac{1-\Gamma_{opt}}{1+\Gamma_{opt}}. \tag{1.9}$$

(1.7) implies that if a two-port network is noise matched ($Y_S = Y_{opt}$), the noise figure is minimized. The available power gain under noise matching condition is known as the associated power gain, G_A^{ass}. It can be calculated by [6]

$$G_A^{ass} = \left|\frac{Y_{21}}{Y_{11}+Y_{opt}}\right|^2 \frac{G_{opt}}{\Re[Y_{22} - (Y_{12}Y_{21})/(Y_{11}+Y_{opt})]}. \tag{1.10}$$

1.3.2 Noise source representations

The noise parameters of a two-port network are fully determined by the noise sources that are distributed within the network. All of the distributive noises can be lumped into two equivalent noise sources located at the port terminals, and they are generally correlated [8]. Fig. 1.7 shows four commonly used representations for lumped noise sources, (a) admittance or Y-representation, (b) impedance or Z-representation, (c) chain or $ABCD$- or A-representation, and (d) hybrid or H-representation. Note the source polarities in (c) and (d). For each representation, the noise Power Spectre Density (PSD) of the two noise sources, as well as their correlation, can be described

by a noise correlation matrix at each frequency point (ω). PSD matrices for the four representations are defined as

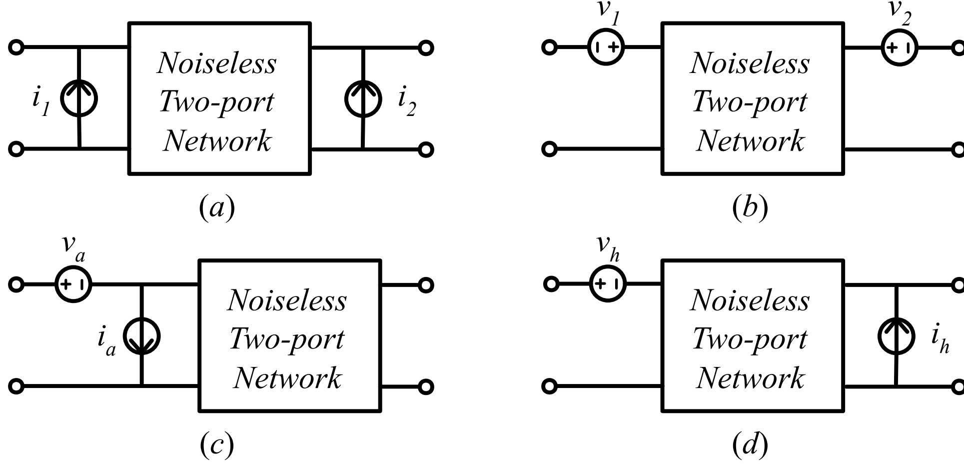

Figure 1.7: Two-port noise representations. (a) Admittance (Y-) representation. (b) Impedance (Z-) representation. (c) Chain ($ABCD$-) representation. (d) Hybrid (H-) representation.

$$S^{Y}(\omega) = \begin{bmatrix} S_{i_1 i_1^*}(\omega) & S_{i_1 i_2^*}(\omega) \\ S_{i_2 i_1^*}(\omega) & S_{i_2 i_2^*}(\omega) \end{bmatrix} \tag{1.11}$$

$$S^{Z}(\omega) = \begin{bmatrix} S_{v_1 v_1^*}(\omega) & S_{v_1 v_2^*}(\omega) \\ S_{v_2 v_1^*}(\omega) & S_{v_2 v_2^*}(\omega) \end{bmatrix} \tag{1.12}$$

$$S^{A}(\omega) = \begin{bmatrix} S_{v_a v_a^*}(\omega) & S_{v_a i_a^*}(\omega) \\ S_{i_a v_a^*}(\omega) & S_{i_a i_a^*}(\omega) \end{bmatrix} \tag{1.13}$$

$$S^{H}(\omega) = \begin{bmatrix} S_{v_h v_h^*}(\omega) & S_{v_h i_h^*}(\omega) \\ S_{i_h v_h^*}(\omega) & S_{i_h i_h^*}(\omega) \end{bmatrix} \tag{1.14}$$

Each of these matrices, denoted as S^{origin}, can be transformed into another, denoted as $S^{destination}$, by

$$S^{destination} = T S^{origin} T^{\dagger} \tag{1.15}$$

Here the superscript † represents the transpose conjugate operator. The specific transformation between two noise matrix can be looked up in Appendix.A.

Noise parameters, determined by lumped noise sources, can be directly calculated from the chain representation noise matrix elements, i.e. S_v, S_i and S_{iv^*} as [8]

$$R_n = \frac{S_v}{4kT} \tag{1.16}$$

$$G_{opt} = \sqrt{\frac{S_i}{S_v} - \left[\frac{\Im(S_{iv^*})}{S_v}\right]^2} \tag{1.17}$$

$$B_{opt} = -\frac{\Im(S_{iv^*})}{S_v} \tag{1.18}$$

$$NF_{min} = 1 + 2R_n \left[G_{opt} + \frac{\Re(S_{iv^*})}{S_v}\right] \tag{1.19}$$

Inversely, the chain representation noise matrix can be calculated from noise parameters using (1.16) - (1.19) as

$$S^A = \begin{bmatrix} S_v & S_{vi^*} \\ S_{iv^*} & S_i \end{bmatrix} = 4kT \begin{bmatrix} R_n & \frac{NF_{min}-1}{2} \\ \frac{NF_{min}-1}{2} - R_n Y_{opt} & R_n |Y_{opt}|^2 \end{bmatrix} \tag{1.20}$$

(1.20) will be used in the noise de-embedding procedure in following chapter.

Chapter 2

Small signal parameter extraction

The purpose of small signal parameter extraction is to develop a systematic characterization scheme allowing to determine correct equivalent circuits of MOSFET transistors. Accuracy parameter extraction is challenging in practice due to the large number of parameters involved, in spite of the various methods proposed, including both direct of analytical methods and numerical optimization based method [7]. Hence, based on the general equivalent circuit proposed previously, assumptions should be made and various measurements are used to describe the different steps of extraction method in following subsection in order to simplify the equivalent circuit and extract desired parameters.

The devices used are from a 28nm high-k metal gate RF CMOS technology [2]. S-parameters are measured on wafer from 1GHz to 30 GHz. For the studied devices, dimensions are varied in N_f, W_f and L to display the scaling of extracted parameters. Pad and interconnect from pads to device terminals are needed to be firstly removed using standard open-short de-embedding.

2.1 Open-short de-embedding

Fig. 2.1 shows the equivalent circuit used for open-short de-embedding [9], that is, the actual transistor is embedded in surrounding parasitics, including both the parallel parasitics Y_{p1}, Y_{p2}, Y_{p3} and the series parasitics Z_{L1}, Z_{L2} and Z_{L3}.

As shown in Fig. 2.2, S-parameters of open structure and short structure can also be measured and used to de-embed the parallel and series parasitics. Denote the measured S-parameters of device as S_{dut}, the measured S-parameters of open structure as S_{open} and S-parameters of of short structure as S_{short}. Using relation between Y- and S- parameters,

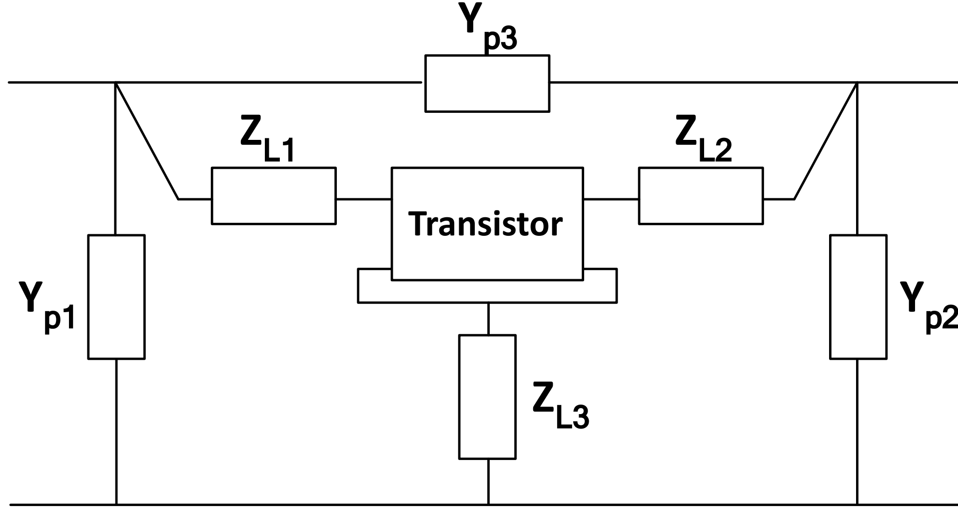

Figure 2.1: Equivalent circuit used for open-short de-embedding, including both the parallel parasitics Y_{p1}, Y_{p2}, Y_{p3} and the series parasitics Z_{L1}, Z_{L2} and Z_{L3} surrounding the transistor [9].

the Y-parameters of device, open and short structure, Y_{dut}, Y_{open} and Y_{short} can be obtained respectively.

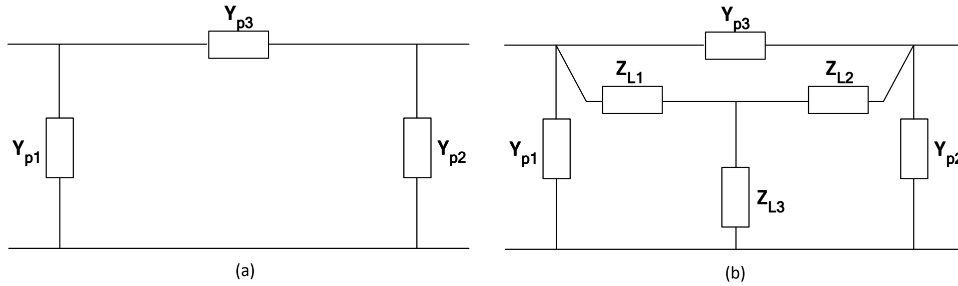

Figure 2.2: (a). The equivalent circuit of open structure including the parallel parasitics Y_{p1}, Y_{p2}, Y_{p3}. (b). The equivalent circuit of short structure including the parallel parasitics Y_{p1}, Y_{p2}, Y_{p3} and the series parasitics Z_{L1}, Z_{L2} and Z_{L3}.

So Y-parameters of actual transistor can be expressed by [9]:

$$Y_{transistor} = ((Y_{dut} - Y_{open})^{-1} - (Y_{short} - Y_{open})^{-1})^{-1}. \tag{2.1}$$

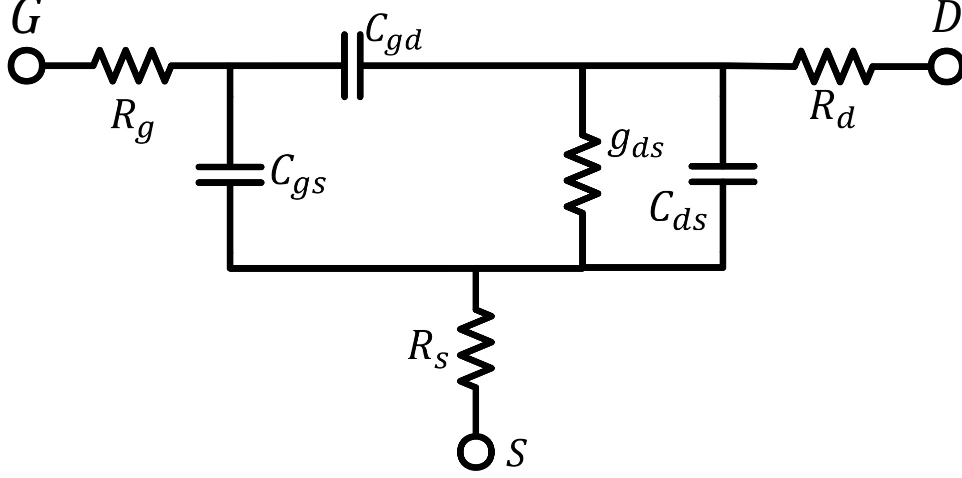

Figure 2.3: Equivalent circuit used in strong inversion $V_{DS} = 0V$.

2.2 Resistance extraction

The extraction of the extrinsic parasitic resistances R_g, R_d and R_s is of much importance. As pad and interconnect parasitics have been removed, the equivalent circuit used to extract extrinsic parasitic resistances is simplified as in Fig. 2.3 at $V_{DS} = 0$V, where substrate network is neglected. Assuming $C_{gs} \approx C_{gd} = C$ and $\frac{-C^2 - 2CC_{ds}}{4g_{ds}^2 C^2}\omega^2 \ll 1$, the expression of Z-parameters can be approximated by [10]:

$$\Re(Z_{22} - Z_{12}) \approx R_d + \frac{1}{2g_{ds}} \tag{2.2}$$

$$\Re(Z_{12}) \approx R_s + \frac{1}{2g_{ds}} \tag{2.3}$$

$$\Re(Z_{11} - Z_{12}) \approx R_g - \frac{1}{4g_{ds}} \tag{2.4}$$

where $\Re(Z)$ refers to real part of Z-parameters. In the MOSFET theory, the drain to source conductance is proportional to the gate voltage in the linear regime. The output conductance is given by:

$$g_{ds} = \frac{\mu W_f C_{ox}}{L}(V_{GS} - V_{TH} - nV_{DS}) \tag{2.5}$$

That is, the resistances are extracted using linear regression of the real part of Z-parameters versus $1/(V_{GS} - V_{TH})$ at $V_{DS} = 0$V. μ is assumed to keep constant in our limited ranges of V_{GS}.

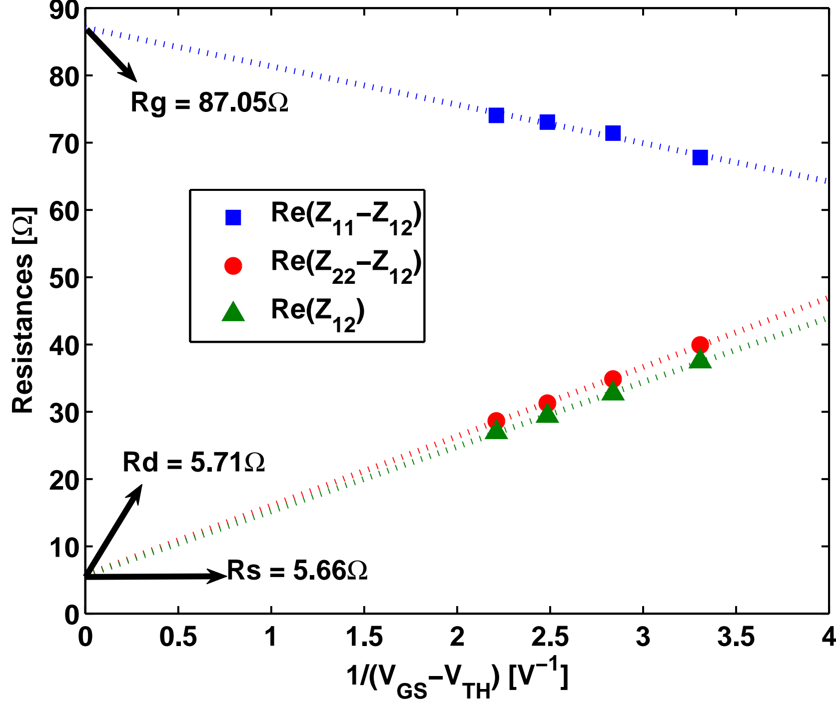

Figure 2.4: Extraction of R_g, R_d, R_s from Z-parameters at $V_{DS} = 0$V for $L = 30$nm, $W_f = 1\mu$m, $N_f = 8$.

Fig. 2.4 illustrates the extraction of R_g, R_s and R_d from $V_{DS} = 0V$ Z-parameters. $\Re(Z_{11} - Z_{12})$, $\Re(Z_{22} - Z_{12})$, and $\Re(Z_{12})$ at 10GHz are plotted versus $1/(V_{GT})$, with $V_{GT} = V_{GS} - V_{TH}$ being the gate overdrive. V_{TH} is determined using extrapolation at the peak g_m gate bias for a low V_{DS} of 0.01V. The resistances are extracted from y-axis intercepts, as shown in Fig. 2.4. Note that only data in the linear range are used for extraction. Except at the lowest frequencies, the results are fairly independent of the frequency used.

Fig. 2.5 (a), (b) and (c) show extracted R_g, R_s and R_d versus $1/L$, $1/W_f$, and $1/N_f$, respectively. L, W_f and N_f are gate length, gate finger width, and number of fingers respectively. Observe that R_g shows a linear dependence on $1/W_f$ for $W_f < 2\mu$m i.e.

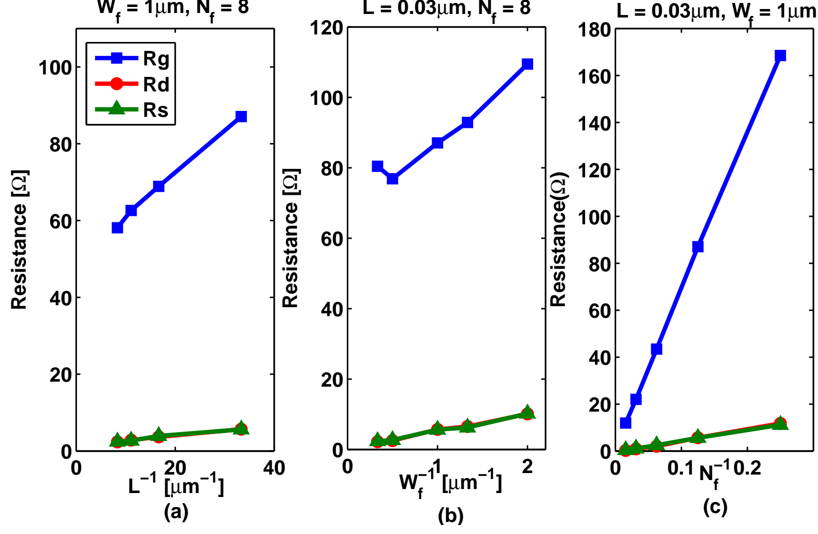

Figure 2.5: (a)R_g, R_d, R_s versus $1/L$. (b)R_g, R_d, R_s versus $1/W_f$. (c)R_g, R_d, R_s versus $1/N_f$.

$1/W_f > 0.5\mu\text{m}^{-1}$, that is, R_g *increases* with decreasing finger width, which is opposite to what one would expect from a gate current flow along the channel width direction. This indicates a vertical component of the gate resistance inversely proportional to gate area, which can be a significant problem for noise, as the common practice of reducing gate finger width is no longer effective in reducing gate resistance and its thermal noise. Such vertical component of gate resistance could be caused by the contact resistance between two different layers of metals in the gate metal stack, i.e. the workfunction metal and the gate metal.

The dependence of R_g on L, W_f and N_f can be modelled with an additional vertical component inversely proportional to gate area as follows:

$$R_g = \frac{1}{N_f}(R_1 + \frac{\rho_c}{W_f L} + R_2 \frac{W_f}{L}), \tag{2.6}$$

where R_1, ρ_c and R_2 are model parameters. The measured R_g can be fitted well as in Fig. 2.6 and Fig. 2.7 with $R_1 = 400\ \Omega$, $\rho_c = 6.8\ \Omega \cdot \mu\text{m}^2$ and $R_2 = 1.66\ \Omega$. The measured results clearly show that for small W_f vertical component inversely proportional to gate area become increasingly significant.

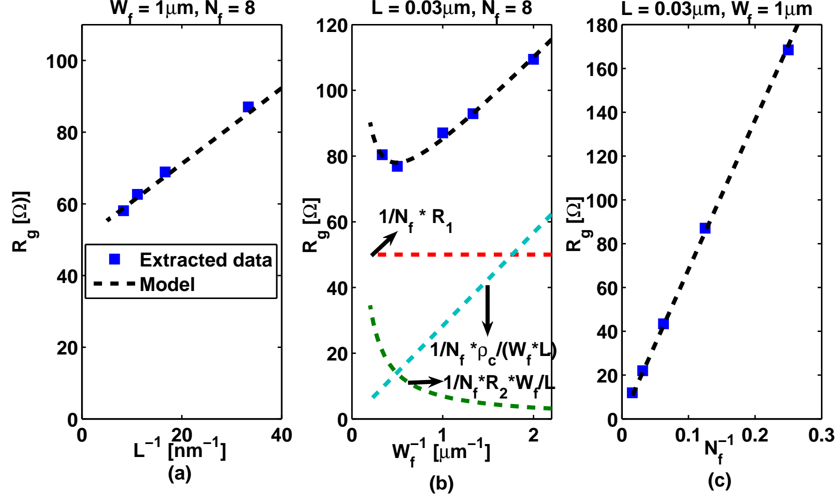

Figure 2.6: (a)R_g versus $1/L$. (b)R_g and its three components versus $1/W_f$. (c)R_g versus $1/N_f$ modelled using (2.6).

2.3 Substrate network

The effect of substrate parasitics can be described by a simple subcircuit extension of the conventional MOSFET model by using a single lumped substrate resistance R_{sub}. At the bias of $V_{GS} = V_{DS} = 0$V, most intrinsic components can be neglected. The equivalent circuit is further simplified as shown in Fig. 2.8 due to small R_s and R_d. C_{gd0} and C_{gs0} refer to gate-drain and gate-source capacitance at zero bias, respectively. C_{gb} represents the gate-body capacitance. Both C_{js} and C_{jd} are junction capacitance, usually the C_{js} is neglected and only one junction to drain capacitance is calculated, since drain current mainly flows through C_{jd}.

A method for extraction of these components can be from Y-parameters by assuming $j\omega$ items $\gg j\omega^3$ items, $\omega^2 C_{gb}^2 R_{sub} R_g \ll 1$, $\omega^2 C_{gg}^2 R_g^2 \ll 1$ and denoting $C_j = C_{js} + C_{jd}$, $C_{gg} = C_{gb} + C_{gd0} + C_{gs0}$ [11]:

$$\Re(Y_{11}) \approx \omega^2 (C_{gd0} + C_{gs0} + C_{gb})^2 R_g + \omega^2 C_{gb}^2 R_{sub} \tag{2.7}$$

$$\Im(Y_{11}) \approx \omega (C_{gd0} + C_{gs0} + C_{gb}) \tag{2.8}$$

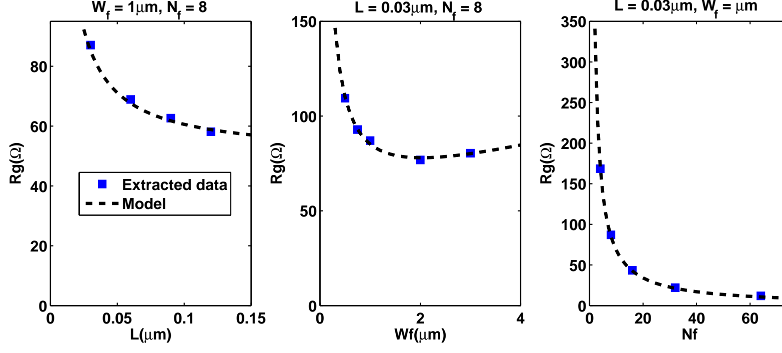

Figure 2.7: (a)R_g versus L. (b)R_g and its three components versus W_f. (c)R_g versus N_f modelled using (2.6).

$$\Re(Y_{21}) \approx \omega^2 C_{jd} C_{gb} R_{sub} - \omega^2 (C_{gd0} + C_{gs0} + C_{gb}) C_{gd0} R_g \tag{2.9}$$

$$\Im(Y_{21}) \approx -\omega C_{gd0} \tag{2.10}$$

$$\Re(Y_{22}) \approx \frac{\omega^2 C_{jd}^2 R_{sub}}{1 + \omega^2 C_{jd}^2 R_{sub}^2} + \omega^2 C_{gd0}^2 R_g \tag{2.11}$$

$$\Im(Y_{22}) = \frac{\omega (C_{jd} + C_{gd0})}{1 + \omega^2 C_{jd}^2 R_{sub}^2} \tag{2.12}$$

where $\Re$ refers to real part and Im refers to imaginary part. So substrate resistance R_{sub} and junction capacitance C_{jd} can be extracted by solving above equations. As shown in Fig. 2.9, the measured Y-parameters can be fitted well with modelled Y-parameters using extracted values. As shown in Fig. 2.10, R_{sub} shows linear relation with large W_f and decreases only for $W_f = 0.5\mu$m. R_{sub} shows linear relation with whole $1/N_f$ and interception with y-axles is almost 0.

2.4 Extrinsic and intrinsic capacitances

Because of charge redistribution with change in voltage as capacitance, here we use the capacitance C_{gs} and C_{gd} to model the change in the depletion charge with respect to the gate-source and gate-drain voltages respectively. The drain-source capacitance C_{ds} is

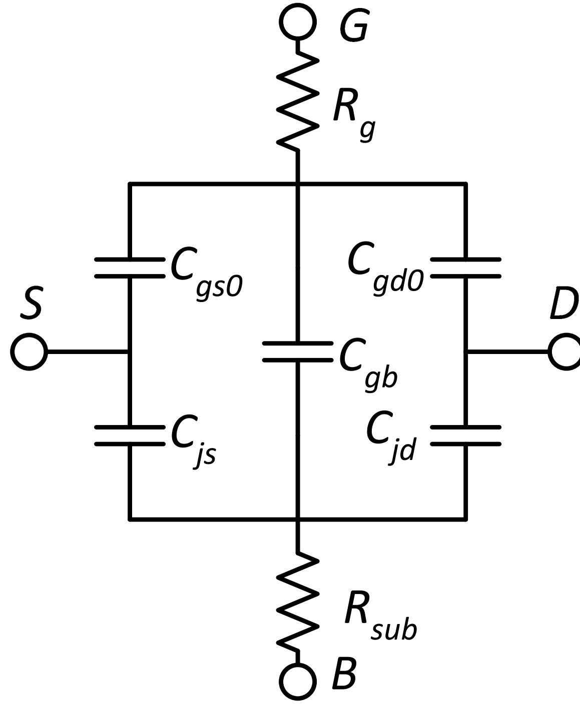

Figure 2.8: Small signal equivalent circuit for substrate network at $V_{GS} = V_{DS} = 0$V.

also included to account for geometric capacitance effects between the sources and drain electrodes.

After de-embedding R_g, R_d and R_s from Z-parameters and transforming it to Y-parameters and further removing substrate network extracted above, the C_{gs} and C_{gd} can be extracted from imaginary of Y-parameters at $V_{DS} = 0V$ [12]:

$$C_{gs} = \Im(\frac{Y_{11} + Y_{12}}{\omega}) \tag{2.13}$$

$$C_{gd} = \Im(\frac{-Y_{12}}{\omega}) \tag{2.14}$$

Fig. 2.11 shows that both C_{gs} and C_{gd} at $V_{GS} = 0V$ are very high compared to those at high V_{GS}. With considering bias dependence, we divide each of them into two parts, extrinsic and intrinsic parts. For further extraction of these numerical components it is reasonable to assume:

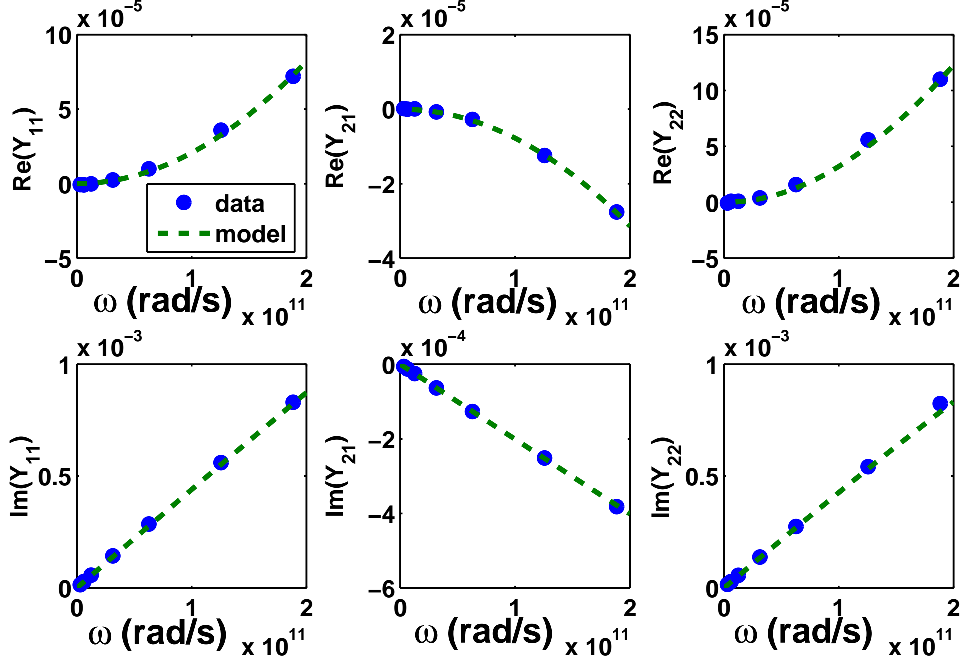

Figure 2.9: Measured and modelled Y-parameters using extracted parameters shown in Fig.2.8 for $L = 30$nm, $W_f = 1\mu$m, $N_f = 8$ at $V_{GS} = V_{DS} = 0$V.

1. Extrinsic components are independent of bias with footnote of "x";
2. Intrinsic components are symmetric and depend on bias with footnote of "i".
3. C_{gb} is the difference between gate to drain and gate to source, which is located in gate to body.

Furthermore, due to bias dependence of intrinsic capacitance, $V_{GS} = 1V$ is chosen as the reference bias to determine each intrinsic component. The steps of extraction of each extrinsic and intrinsic component are written as:

1. Extrinsic gate to drain capacitance can be directly extracted from zero bias due to its independence of bias:

$$C_{gdx} = C_{gd}(V_{GS} = 0V) \tag{2.15}$$

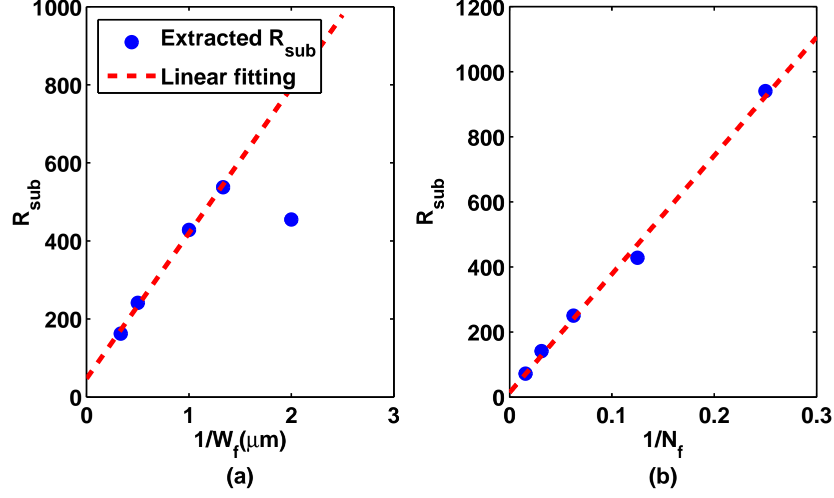

Figure 2.10: (a)Extracted R_{sub} versus $1/W_f$ for $L = 30$nm, $N_f = 8$. (b) Extracted R_{sub} versus $1/N_f$ for $L = 30$nm, $W_f = 1\mu$m.

2. Intrinsic gate to drain capacitance is responsible for increasing value extracted from $V_{GS} = 0$V to 1V:

$$C_{gdi} = C_{gd}(V_{GS} = 1V) - C_{gd}(V_{GS} = 0V) \tag{2.16}$$

3. Intrinsic gate to drain and gate to source capacitance are regarded symmetric and equal:

$$C_{gsi} = C_{gdi} \tag{2.17}$$

4. Extrinsic gate to source capacitance is independent of bias which can be determined by subtraction of intrinsic gate to source capacitance at $V_{GS} = 1V$:

$$C_{gsx} = C_{gs}(V_{GS} = 1V) - C_{gsi} \tag{2.18}$$

5. C_{gb} is taken into account together with extrinsic gate to source capacitance at $V_{GS} = 0V$:

$$C_{gsx} + C_{gb} = C_{gs}(V_{GS} = 0V) \tag{2.19}$$

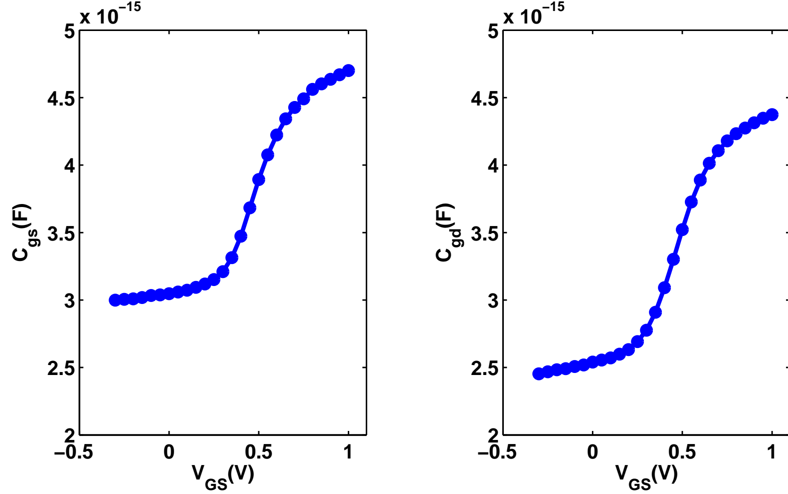

Figure 2.11: C_{gs} and C_{gd} extracted from 10GHz versus gate bias for $L = 30$nm, $W_f = 1\mu$m, $N_f = 8$ at $V_{DS} = 0$V.

In above calculations, $V_{GS} = 1V$ is referred to determine intrinsic components for $V_{DS} = 0V$. The L, W_f, N_f dependence of each extracted components are shown in Fig. 2.12. From W_f and N_f dependence, each component is expected to be proportional to the finger width and number of finger. For L dependence, C_{gb} increase with L and that is expected to explain the difference between extrinsic or lumped gate to drain and gate to source value. Moreover, as extrinsic gate to source capacitance seems independent of L, it can be concluded that overlay capacitance whose value almost keep constant with L is the dominant compared to fringing capacitance whose value is proportional to L.

2.5 Extraction of intrinsic parameters

After all the previous extraction, the reference for experimental data can be moved into intrinsic part in order to have direct extraction of intrinsic elements by removing the effect of gate, drain, source resistances and substrate elements based on Fig. 3.2 and following below steps [13]:

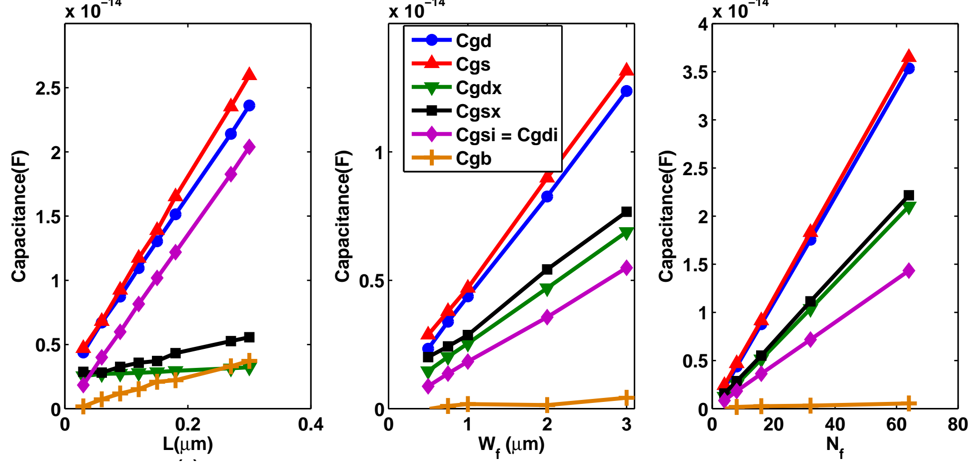

Figure 2.12: (a)Each component versus L. (b)Each component versus W_f. (c)Each component versus N_f.

1. De-embedding R_g and R_d. This step can be done as follows:

$$Z_I = Z^{ext} - Z_1, \tag{2.20}$$

$$Z_1 = \begin{bmatrix} R_g & 0 \\ 0 & R_d \end{bmatrix}, \tag{2.21}$$

where Z^{ext} is the matrix obtained from conversion of the de-embedding S-parameters to the corresponding Z-parameters. Z_I is the Z-parameters of block I.

2. De-embedding substrate elements. De-embedding R_{sub} and C_{jd} from block I to block II is:

$$Y_{II} = Z_I^{-1} - \begin{bmatrix} 0 & 0 \\ 0 & \frac{j\omega C_{jd}}{1+j\omega C_{jd}R_{sub}} \end{bmatrix}, \tag{2.22}$$

3. De-embedding R_s. Finally, the intrinsic Y-parameters are obtained by applying:

$$Y_{int} = \begin{bmatrix} Y_{11}^{II} & Y_{12}^{II} \\ Y_{21}^{II} & Y_{22}^{II} \end{bmatrix} = \left(Y_{II}^{-1} - \begin{bmatrix} R_s & R_s \\ R_s & R_s \end{bmatrix} \right)^{-1}. \tag{2.23}$$

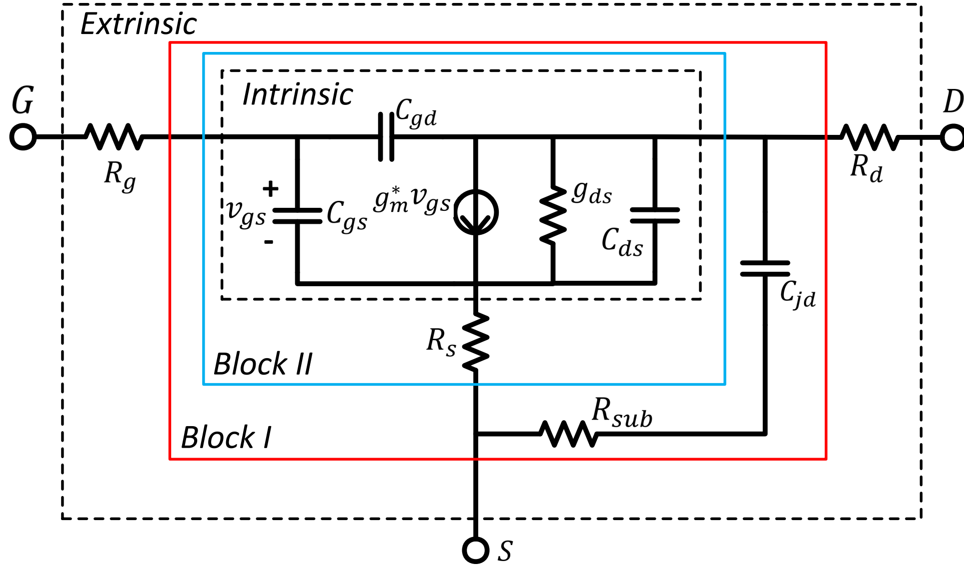

Figure 2.13: Small signal equivalent circuit for parameter extraction and noise de-embedding.

Once the above components is de-embeded, the intrinsic parameters can be directly obtained from the intrinsic Y-parameters. The expressions are:

$$Y_{11}^{II} = j\omega(C_{gs} + C_{gd}) \tag{2.24}$$

$$Y_{12}^{II} = -j\omega C_{gd} \tag{2.25}$$

$$Y_{21}^{II} = g_m e^{j\omega\tau} - j\omega C_{gd} \tag{2.26}$$

$$Y_{22}^{II} = \frac{1}{R_{ch}} + j\omega(C_{sd} + C_{gd}) \tag{2.27}$$

where τ is the phase delay and accounts for the reduction of the complex transconductance at high frequencies. The output conductance $g_{ds} = \frac{1}{R_{ch}}$ can be expressed by channel resistance.

Even though the intrinsic parameters can be determined by solving (2.24)-(2.27), it is necessary to guarantee that the extracted data will properly represent the MOSFET's behavior within the desired range. Therefore, a regression procedure must be used to extract adequate values for the elements. This procedure, based on (2.24)-(2.27), consists of the following steps:

1. According to (2.25), C_{gd} can be determined from the slope of the linear regression of the $-\Im(Y_{12}^{II})$ versus ω. The extraction of C_{gd} is illustrated in Fig. 2.14(a).

2. Subsequently, as can be seen in Fig. 2.14(b), the sum of C_{gs} and C_{gd} is obtained from the slope of the linear fit of the $\Im(Y_{11}^{II})$ versus ω.

3. Similarly, C_{sd} is obtained by subtracting C_{gd} from the slope of the linear fit of the $\Im(Y_{22}^{II})$ versus ω. This extraction is shown in Fig. 2.14(c).

4. R_{ch} is determined from the inverse of $\Re(Y_{22}^{II})$. An important point to be marked here is the fact that $\Re(Y_{22}^{II})$ must be independent of frequency, as shown in Fig. 2.14(d). Otherwise, the substrate elements have not been properly removed from the extrinsic data.

5. To determine g_m, the real part of Y_{21}^{II} can be written in the form:

$$\Re(Y_{21}^{II}) = g_m cos(\omega\tau) \tag{2.28}$$

   Since $\omega\tau \ll \pi/2$, $cos(\omega\tau) \approx 1$ and the transconductance can be obtained as:

$$g_m = \Re(Y_{21}^{II}) \tag{2.29}$$

   Fig. 2.14(e) shows that $\Re(Y_{21}^{II})$ does not show a frequency dependence, making valid this approximation within the measured range.

6. τ is obtained by manipulating 2.25 and 2.26 to be:

$$\tau = -\frac{1}{\omega} sin^{-1}\left(\frac{\Im(Y_{21}^{II}) - \Im(Y_{12}^{II})}{g_m}\right) \tag{2.30}$$

   This parameter is plotted versus ω in Fig. 2.14(f).

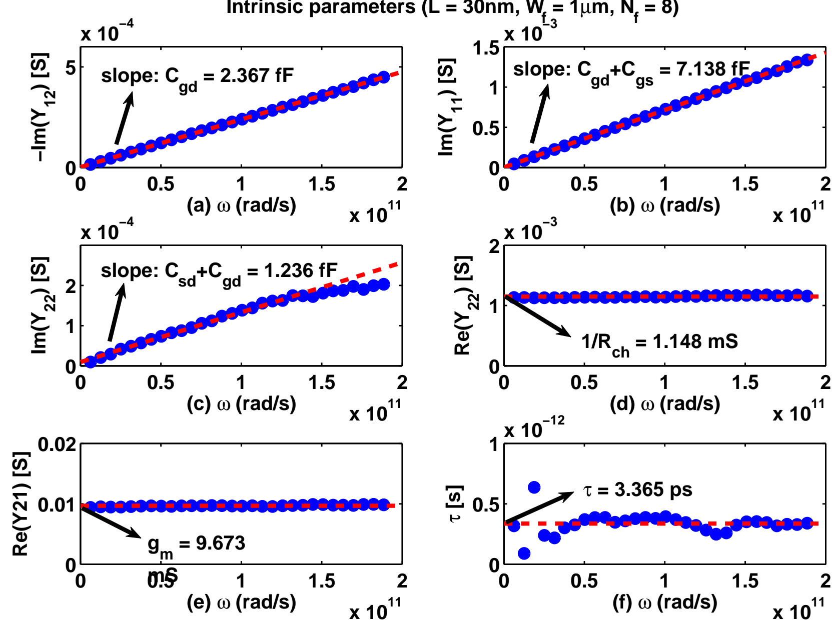

Figure 2.14: Intrinsic Y-parameters versus ω used to extract the intrinsic parameters at V_{GS} = 0.6V, V_{DS} = 0.8V for L = 30nm, W_f = 1μm, N_f = 8.

2.6 Model validation

Once the parameter extraction is carried out for this 28nm device(L = 28nm, W_f = 1μm, N_f = 8), Y-parameter using extracted values are calculated according to the small signal equivalent circuit in 3.2 and compared with measurement. It is shown in Fig. 2.15 for $V_{GS} = 0.6V$ and in Fig. 2.16 for $V_{GS} = 0.9V$ at the same $V_{DS} = 0.8V$ that the extrinsic simulated Y-parameters using all the extracted elements and measured Y-parameters converted from measured S-parameters after open-short de-embedding versus frequency. As can be seen, results show the great accuracy of implementing a simple equivalent circuit model to represent the high frequency characteristics since the substrate losses are taken into account by just adding two directly determined elements.

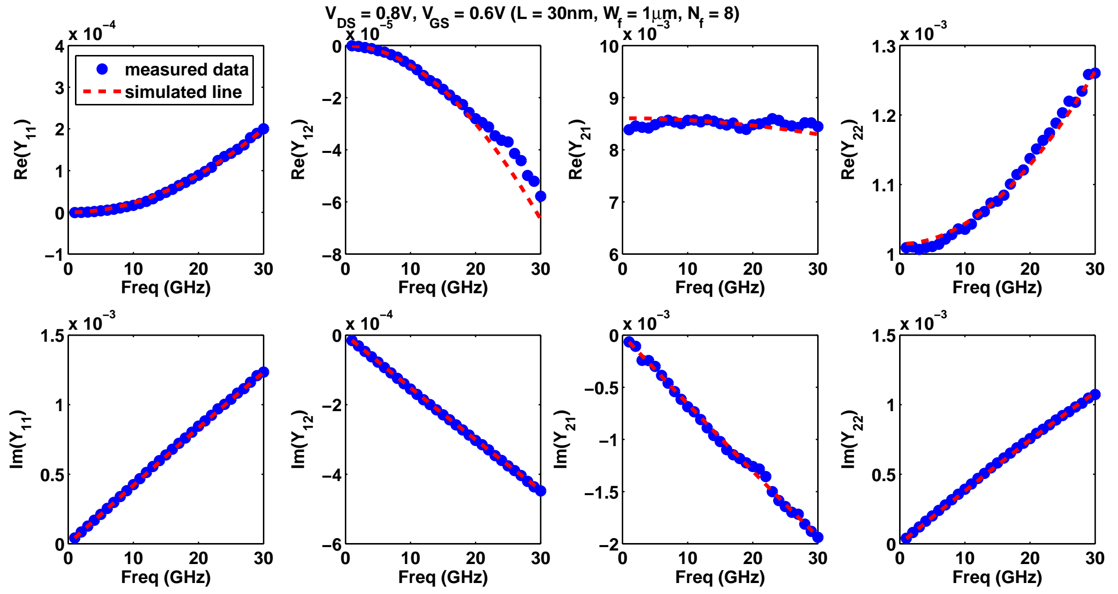

Figure 2.15: Real and imaginary parts of Y-parameters showing the agreement between simulated line and measured data at $V_{GS} = 0.6\text{V}$, $V_{DS} = 0.8\text{V}$ for $L = 30\text{nm}$, $W_f = 1\mu\text{m}$, $N_f = 8$.

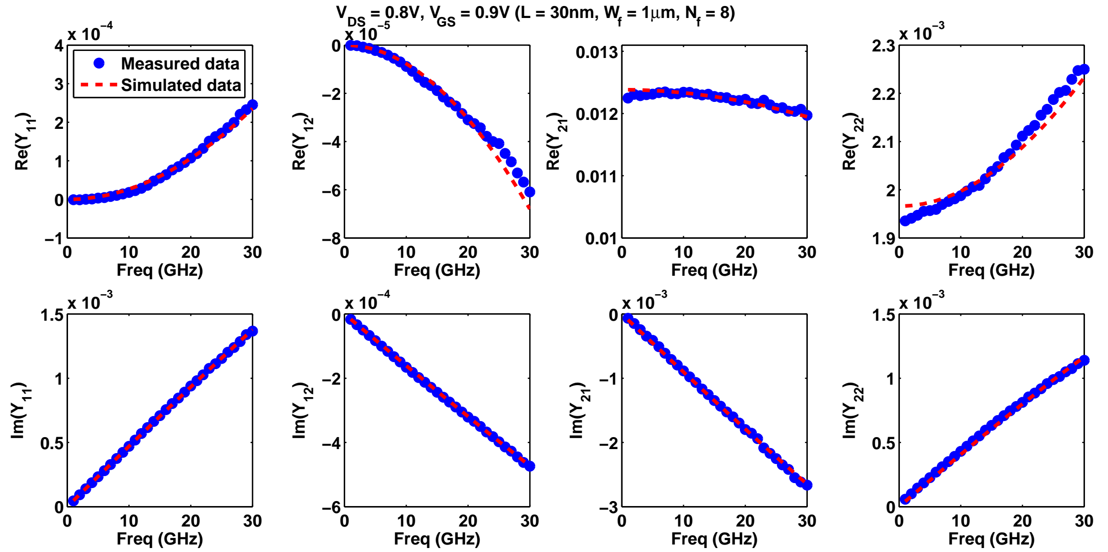

Figure 2.16: Real and imaginary parts of Y-parameters showing the agreement between simulated and measured data at $V_{GS} = 0.9\text{V}$, $V_{DS} = 0.8\text{V}$ for $L = 30\text{nm}$, $W_f = 1\mu\text{m}$, $N_f = 8$.

Chapter 3

Noise extraction

Transistor RF noise is an important issue to characterize and model for RF and analog design. We investigate in this chapter RF noise performance of a 28nm high-k metal gate RF CMOS technology. Drain current noise normalized by its equilibrium value, $S_{id}/4kTg_{d0}$, is extracted from measured noise parameters as a function of gate and drain biases for three gate lengths, 30nm, 60nm, and 90nm, respectively. Gate resistance is found to be a significant contributor to device overall noise. The intrinsic channel $S_{id}/4kTg_{d0}$ remains below 2 and shows a much stronger V_{DS} dependence compared to at 90nm.

Measured noise parameters are converted first to a chain-representation noise correlation matrix, which is then converted to a Y-representation noise correlation matrix, from which drain current noise S_{id} is extracted.

The drain current noise S_{id} after open-short de-embedding is denoted as S_{id}^{ext}, extrinsic drain current noise. The small signal equivalent circuit of Fig. 1.6 is then used to de-embed the noise of gate resistance R_g, drain resistance R_d, substrate resistance R_{sub} and source resistance R_s. The resulting S_{id} is denoted as S_{id}^{int}, intrinsic drain current noise. In Fig. 1.6, we also show gate source capacitance C_{gs}, gate drain capacitance C_{gs} and junction capacitance C_{jd}. Channel current is expressed by voltage controlled current source with transconductance g_m. g_{ds} is the output conductance of the channel and C_{ds} includes channel capacitance and drain source terminal capacitance.

3.1 Extrinsic noise extraction

Fig. 3.1 shows typical dependence of the measured noise parameter including minimum noise figure NF_{min}, noise resistance R_n and the optimum source admittance Y_{opt} on frequency after open-short de-embedding.

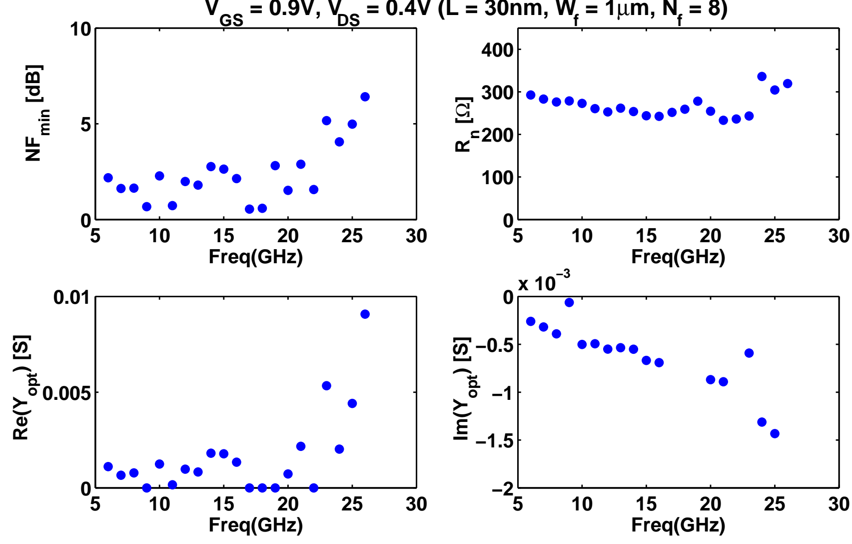

Figure 3.1: Extrinsic noise parameters versus frequency at $V_{GS} = 0.9V$, $V_{DS} = 0.4V$.

Chain representation noise-correlated matrix C_A can be expressed by using noise parameters NF_{min}, R_n and Y_{opt} [14]:

$$C_A = 4kT \begin{bmatrix} R_n & \frac{F_{min}-1}{2} - R_n Y_{opt}^* \\ \frac{F_{min}-1}{2} - R_n Y_{opt} & R_n |Y_{opt}|^2 \end{bmatrix}, \tag{3.1}$$

where k is the Boltzman constant and T is absolute temperature.

Then the extrinsic drain and gate current noise (S_{i_d}, S_{i_g}) as well as their correlation ($S_{i_g i_d^*}$, $S_{i_g^* i_d}$,) are calculated from C_A [14]:

$$C_Y^{ext} = \begin{bmatrix} S_{i_g} & S_{i_g i_d^*} \\ S_{i_g^* i_d} & S_{i_d} \end{bmatrix} \Bigg|_{ext} = T C_A T^{\dagger}, \tag{3.2}$$

$$T = \begin{bmatrix} -Y_{11} & 1 \\ -Y_{21} & 0 \end{bmatrix}, \tag{3.3}$$

where $T^{\dagger}$ is the transpose conjugate of T. Below we denote $C_Y^{ext}(2,2)$ as S_{id}^{ext}. Note that from above formula:

$$S_{id}^{ext} = Y_{21} R_n Y_{21}^*, \tag{3.4}$$

that is, S_{id}^{ext} is mainly determined by Y-parameters and R_n after open-short de-embedding.

3.2 Intrinsic noise extraction

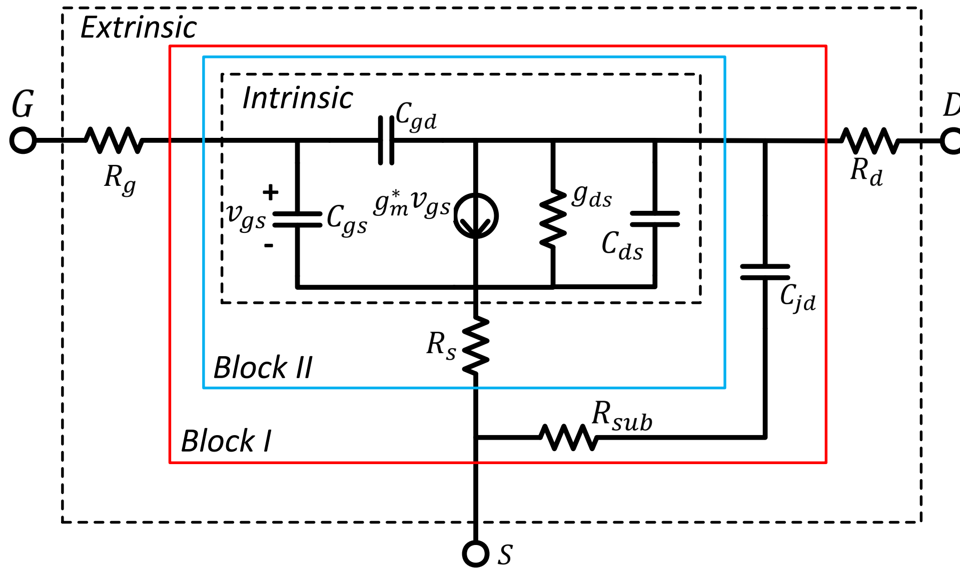

Figure 3.2: The small signal equivalent circuit for parameter extraction and noise de-embedding.

In Fig. 3.2, R_g, R_d and R_s as well as R_{sub} all have the usual $4kTR$ thermal noise voltage. To obtain the intrinsic noise, we need to perform the following de-embedding steps [14]:

1. Denote Z-parameter that consists of R_g, R_d as Z_1, then remove it from extrinsic Z-parameter and its Z-noise representation matrix from C_Z^{ext} converted by C_Y^{ext} in (3.2). So Z-parameter of block I, Z_I and its Z-noise representation matrix, C_{Z_I} can

be obtained as:

$$Z_I = Z^{ext} - Z_1, \tag{3.5}$$

$$Z_1 = \begin{bmatrix} R_g & 0 \\ 0 & R_d \end{bmatrix}, \tag{3.6}$$

$$C_{Z_I} = C_Z^{ext} - 4kT\Re[Z_1]. \tag{3.7}$$

$$C_Z^{ext} = T_{Y-Z} C_Y^{ext} T_{Y_Z}^{\dagger}, \tag{3.8}$$

$$T_{Y-Z} = \begin{bmatrix} Z_{11}^{ext} & Z_{12}^{ext} \\ Z_{21}^{ext} & Z_{22}^{ext} \end{bmatrix}. \tag{3.9}$$

2. Denote Y-parameter of the branch of C_{jd} and R_{sub} as Y_2, then remove it from Y-parameters matrix of the block I, Y_I and Y-noise representation matrix of the block I, C_{Y_I}, then the Y-parameter of block II, Y_{II} is:

$$Y_{II} = Y_I - Y_2, \tag{3.10}$$

$$Y_2 = \begin{bmatrix} 0 & 0 \\ 0 & \frac{j\omega C_{jd}}{1+j\omega C_{jd} R_{sub}} \end{bmatrix}, \tag{3.11}$$

and Y- noise representation matrix of block II, $C_{Y_{II}}$ can be obtained as:

$$C_{Y_{II}} = C_{Y_I} - 4kT\Re[Y_2], \tag{3.12}$$

where C_{Y_I} is converted from C_{Z_I}:

$$C_{Y_I} = T_{Z-Y} C_{Z_I} T_{Z-Y}^{\dagger}, \tag{3.13}$$

$$T_{Z-Y} = \begin{bmatrix} Y_{11}^I & Y_{12}^I \\ Y_{21}^I & Y_{22}^I \end{bmatrix}. \tag{3.14}$$

3. Denote Z-parameter of R_s as Z_3, then remove it from Z-parameter matrix of the block II to obtain intrinsic Z-parameter:

$$Z^{int} = Z_{II} - Z_3, \tag{3.15}$$

$$Z_3 = \begin{bmatrix} R_s & R_s \\ R_s & R_s \end{bmatrix}, \tag{3.16}$$

then intrinsic noise matrix is Z-representation noise matrix of block II that have R_s removed:

$$C_Z^{int} = C_{Z_{II}} - 4kT\Re[Z_3]. \tag{3.17}$$

Fig. 3.3 shows the result of each step of de-embedding S_{id} and R_g has the most significant effect in de-embedding of extrinsic resistance noise. Observe that S_{id} increases after de-

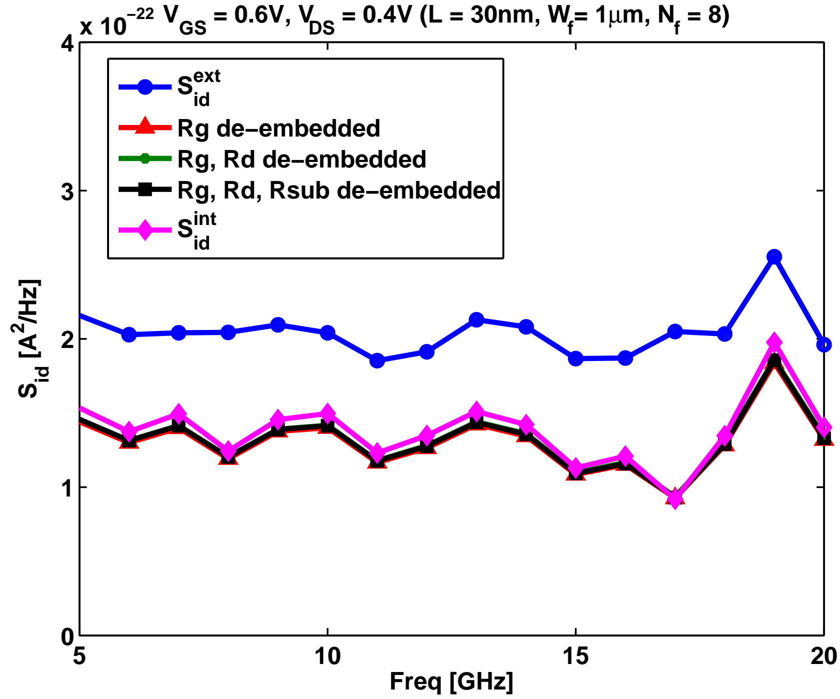

Figure 3.3: Step by step result of S_{i_d} de-embedding versus frequency.

embedding R_s. This increase can be understood using the relationship between S_{id} before

and after R_s de-embedding expressed by [15]:

$$S_{id}^{int} = \frac{1}{\alpha^2}(S_{id}^{(\text{before } R_s \text{ de-embedding})} - 4kT(g_m + g_{ds})^2 R_s), \tag{3.18}$$

$$\alpha = \frac{1}{1 + (g_{ds} + g_m)R_s}. \tag{3.19}$$

At V_{GS}=0.6V, V_{DS}=0.4V, g_m is extracted from $\Re(Y_{21})|_{w^2=0}$ and g_{ds} is extracted from $\Re(Y_{22})|_{w^2=0}$ [16]. Then g_m is 7.02mS, g_{ds} is 1.08mS and R_s=5.66Ω. S_{id} before R_s de-embedding is 1.41A^2/Hz. The S_{id}^{int} calculated using (3.18) is 1.48A^2/Hz consistent with that extracted from noise two-port de-embedding, 1.49A^2/Hz.

3.3 g_{d0} extraction

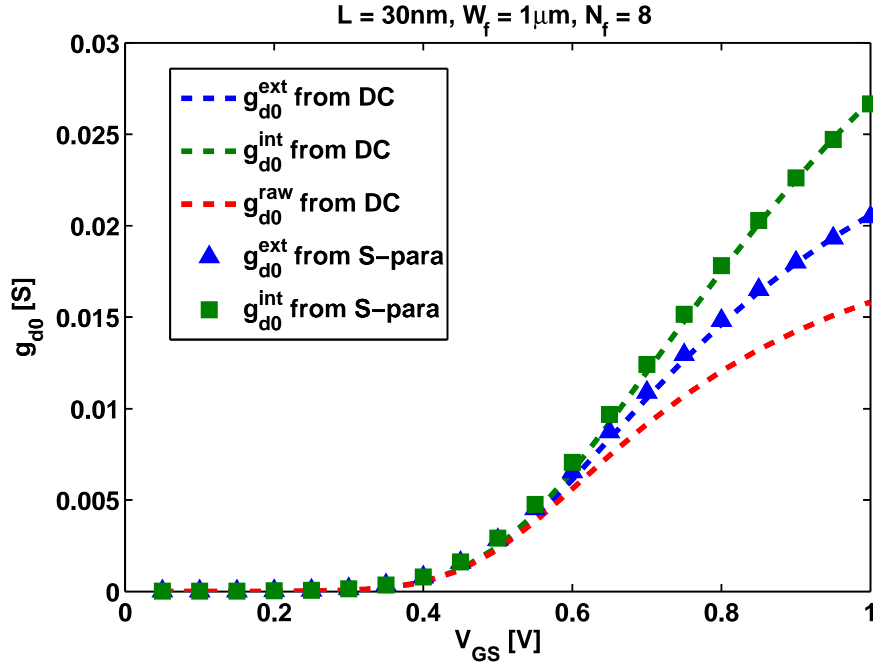

Figure 3.4: Extraction of extrinsic and intrinsic g_{d0} from DC and S-parameter measurement.

g_{d0} is the output conductance of the channel g_{ds} measured in the cold bias. Fig. 3.4 shows extrinsic and intrinsic g_{d0} extracted from $V_{DS} = 0V$ S-parameters. The extrinsic g_{d0} from $V_{DS} = 0.01V$ DC $I_{DS} - V_{GS}$ measurement is also shown, which is fairly consistent with

the g_{d0} obtained right after open short de-embedding. The short line resistance is removed from raw resistance obtained as V_{DS}/I_{DS}. At $V_{GS} > 0.7V$, the difference between extrinsic and intrinsic g_{d0} becomes important.

3.4 γ_{gd0} extraction

In device modelling the ratio $S_{id}/4kTg_{d0}$ is often denoted as γ [15], [17], [18]. For circuit design, however, $S_{id}/4kTg_m$ is more relevant [19], [20], [21], which is often denoted as γ as well. Here to avoid confusion, we will use γ_{gd0} to denote $S_{id}/4kTg_{d0}$. The extrinsic γ_{gd0} is defined as:

$$\gamma_{gd0}^{ext} = \frac{S_{id}^{ext}}{4kTg_{d0}^{ext}}. \tag{3.20}$$

The intrinsic γ_{gd0} is defined as:

$$\gamma_{gd0}^{int} = \frac{S_{id}^{int}}{4kTg_{d0}^{int}}. \tag{3.21}$$

At V_{GS} = 0.6V, V_{DS} = 0.4V, then $\gamma_{gd0}^{ext} = 1.91$ and $\gamma_{gd0}^{int} = 1.28$. γ_{gd0}^{int} is less than γ_{gd0}^{ext} because $S_{id}^{int} < S_{id}^{ext}$, $g_{d0}^{int} > g_{d0}^{ext}$.

3.5 Result and discussion

Fig. 3.5 shows $S_{id}/(4kTg_{d0})$ at each step of de-embedding versus length for four biases. Both S_{id} and g_{d0} vary at each step. R_g dominates the change from γ_{gd0}^{ext} to γ_{gd0}^{ext}. R_g noise is the most significant at 30nm due to higher g_m and gate resistance value.

Fig. 3.6 shows the dependence of γ_{gd0}^{ext} and γ_{gd0}^{int} on V_{GS} at V_{DS}=0.4V for different length. γ_{gd0} shows overall weak V_{GS} dependence, just slightly stronger dependence at lower V_{GS}.

Fig. 3.7 shows γ_{gd0}^{ext} and γ_{gd0}^{int} versus V_{DS} at V_{GS}=0.6V for different length together with γ_{gd0}^{ext} and γ_{gd0}^{int} at V_{GS}=0.9V, V_{DS}=0.05V. The $\gamma_{gd0}^{ext} \approx \gamma_{gd0}^{int} \approx 1$. γ_{gd0} increases with V_{DS} and the increase is stronger and significant at 30nm. Also, de-embedding R_g makes a larger difference at 30nm at high V_{GS}.

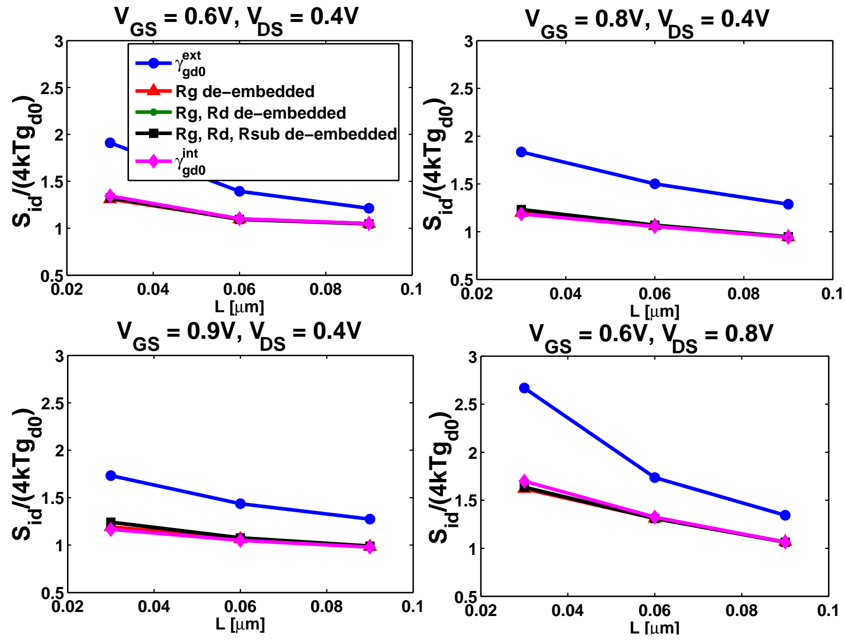

Figure 3.5: γ_{gd0} versus length.

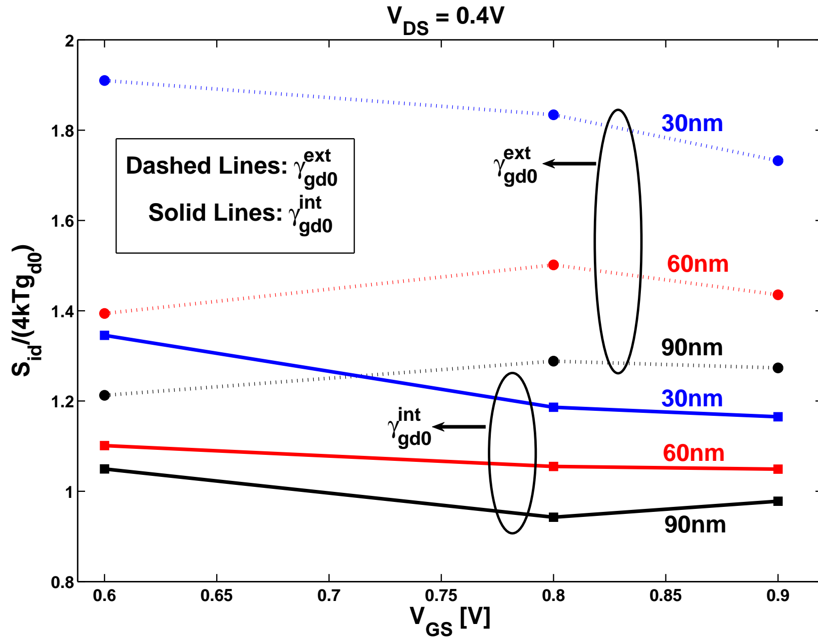

Figure 3.6: V_{GS} dependence of γ_{gd0}^{ext} and γ_{gd0}^{int}.

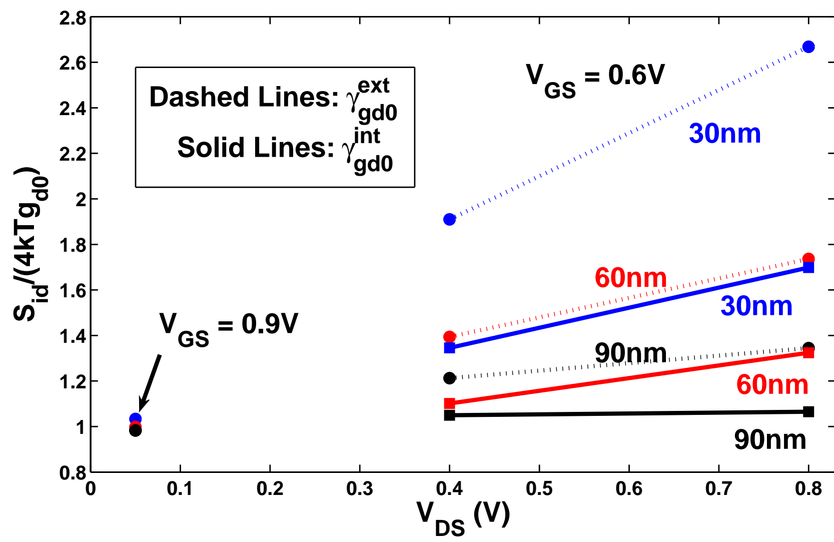

Figure 3.7: V_{DS} dependence of γ_{gd0}^{ext} and γ_{gd0}^{int}.

Chapter 4
Conclusion

In this work, the widely used small signal equivalent circuit has been performed to extract all small-signal parameters and then its accurate high-frequency description by comparison between simulation and measurement have been presented and demonstrated. Based on the small signal equivalent circuit, noise de-embedding from raw data to intrinsic has been performed to analyse noise parameter γ as well as the bias and dimensional dependence.

The proposed extraction relies on the physical significance of each parameters. The width dependence of extracted gate resistance implies a large vertical metal interface component that is inversely proportional to gate area. The traditional scaling rule about lumped substrate resistance need to be revised for the exception of width dependence of our extracted value at $W_f = 0.5\mu m$. Based on bias dependence of extrinsic and intrinsic components, we perform a new method to distinguish and determine each components at $V_{DS} = 0V$. After all extrinsic components have been extracted and de-embedded, the frequency dependence of intrinsic components can then be extracted and matches our model. The overall performance of our proposed model is demonstrated with great accuracy.

To evaluate RF noise performance and further obtain extrinsic and intrinsic γ_{gd0}, a noise de-embedding process is carried out by de-embedding each components in our established small signal equivalent circuit. Among all the resistive component, the noise from R_g is the most significant for $W_f = 1\mu m$. The intrinsic channel $S_{id}/4kTg_{d0}$ remains below 2 and shows a much stronger V_{DS} dependence compared to at $90nm$.

In a nutshell, gate resistance is expected to be a dominant component of AC analysis and noise analysis in further shrinking size and the vertical metal interface component will perform increasingly important role in determining scaling rule of gate resistance in future

smaller size. Moreover, the complexity of width dependence of substrate resistance should be attached much attention in the compact model and design kit.

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Appendices

Appendix A

Transformation of noise representation matrix

The $ABCD$-, Y-, Z-, and H- noise representations can be transformed to another by the matrix operation:

$$S^{destination} = TS^{origin}T^{\dagger}, \tag{A.1}$$

where S^{origin} and $S^{destination}$ are the original and resulting noise correlation matrices respectively, T is the transformation matrix given in A.1, and $T^{\dagger}$ is the transpose conjugate of T. The $ABCD$, Y, Z and H two-port network parameters are used in A.1. The specific conversion is:

	Original Representation			
	S^Y	S^Z	S^A	S^H
S^Y	$\begin{bmatrix}1 & 0\\0 & 1\end{bmatrix}$	$\begin{bmatrix}Y_{11} & Y_{12}\\Y_{21} & Y_{22}\end{bmatrix}$	$\begin{bmatrix}-Y_{11} & 1\\-Y_{21} & 0\end{bmatrix}$	$\begin{bmatrix}-Y_{11} & 0\\-Y_{21} & 1\end{bmatrix}$
S^Z	$\begin{bmatrix}Z_{11} & Z_{12}\\Z_{21} & Z_{22}\end{bmatrix}$	$\begin{bmatrix}1 & 0\\0 & 1\end{bmatrix}$	$\begin{bmatrix}1 & -Z_{11}\\0 & -Z_{21}\end{bmatrix}$	$\begin{bmatrix}1 & -Z_{12}\\0 & -Z_{22}\end{bmatrix}$
S^A	$\begin{bmatrix}0 & A_{12}\\1 & A_{22}\end{bmatrix}$	$\begin{bmatrix}1 & -A_{11}\\0 & -A_{21}\end{bmatrix}$	$\begin{bmatrix}1 & 0\\0 & 1\end{bmatrix}$	$\begin{bmatrix}1 & A_{12}\\0 & A_{22}\end{bmatrix}$
S^H	$\begin{bmatrix}-h_{11} & 0\\-h_{21} & 1\end{bmatrix}$	$\begin{bmatrix}1 & -h_{12}\\0 & -h_{22}\end{bmatrix}$	$\begin{bmatrix}1 & -h_{11}\\0 & -h_{21}\end{bmatrix}$	$\begin{bmatrix}1 & 0\\0 & 1\end{bmatrix}$

Table A.1: Transformation matrices to calculate other representation.