Stress Analysis in Bipolar Transistors

by

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Abstract

Stress effects in semiconductor devices have gained significant attention in semiconductor industry nowadays. Stress effect in semiconductor devices is used as a beneficial effect in sensor applications and strain engineering and efforts are taken to increase these effects. Strain engineering is widely used for MOSFETs. Performance of SiGe based heterostructure bipolar transistors (HBTs) is improved by bandgap and strain engineering. However this approach is not fully developed for Si bipolar junction transistors (BJTs). While stress effects are useful in some areas there are some unwanted stress effects as well. The unintentional stresses developed during fabrication, processing and packaging are harmful in semiconductor devices and efforts are taken to mitigate these stress effects.

In this research work, stress-induced changes were investigated in the perspective of improvement for strain engineering in Si BJTs as well as mitigation of stress effects in precision analog circuits. npn and pnp BJTs on (100) and (111) planes were studied using experimental and modeling approaches. Modeling approach was mainly used for this study in order to overcome the practical difficulties associated with fabrication of devices with different orientation and sizes and controlled application of stress in various orientations for measurements. Measurements were taken for in-plane normal stress and the validity of the model was verified. A new one-dimensional numerical model was developed in Matlab in order to make the stress analysis easier and more in-depth with short running time. Simulation results of the 1-D model and Sentaurus TCAD tool were compared and both results showed very good

agreement. While commercial TCAD tools usually takes tens of minutes for 2-D or hours for 3-D simulations for this type of stress analysis, the newly developed 1-D model gives comparable results in seconds and without any loss of information generated. This model can be used for fast stress analysis/prediction in vertical or lateral npn/pnp BJTs in any plane and will help in developing optimal design for strain engineering in BJTs or stress mitigation in analog circuits.

The stress induced changes in vertical and lateral bipolar transistors on (100) plane were quantitatively analyzed for different stress orientations. Our analysis revealed that for a vertical npn transistor substantial enhancement in collector current (I_C), dc current gain (β), cutoff frequency (f_T), and maximum oscillation frequency (f_{max}) can be achieved using an uniaxial in-plane compressive or an out-of-plane tensile stress. In a vertical pnp considerable improvement in I_C can be achieved with an in-plane or an out-of-plane compressive stress while the changes in β, f_T and f_{max} are minimal. Lateral pnp BJTs showed much higher improvement for in-plane longitudinal compressive stress. In addition, lateral npn BJTs showed higher improvement for out-of-plane compressive stress. These results revealed a promising opportunity for strain engineering in both vertical and lateral Si BJTs.

This study also revealed that the transport limited BJTs are less sensitive to stress than injection limited BJTs. In addition, vertical pnp on (100) silicon is less sensitive to stress than the vertical npn on (100) plane or vertical npn or pnp on (111) plane. On (111) silicon vertical npn BJTs are less sensitive than the vertical pnp BJTs. Finally, stress effects in precision analog circuits have been explored with the help of Spice simulations incorporating the 1-D theoretical model. Some methods for stress mitigation in precision analog circuits are also suggested including usage of less sensitive BJTs whenever possible, keeping the matching BJTs in close

proximity to avoid stress gradients, avoiding high stress regions in chips, usage of enclosed lateral devices for stress compensation.

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CHAPTER 1

INTRODUCTION

1.1 Stress effects in semiconductor devices

Stress induced mobility improvement in semiconductors have been known since 1950s [1]. However, until 1990s the main attention was focused on sensor applications only [2-4]. Several research works have reported on two main types of stress sensors, the piezoresistive stress sensors and the piezojunction stress sensors [5-10]. The piezoresistive stress sensors are based on the stress-induced changes in the majority-carrier mobility of a device and utilize majority-carrier devices such as resistors and MOSFETs. However, piezojunction stress sensors are based on the mechanical stress-induced changes in the saturation current of a minority-carrier device and use bipolar junction transistors or p-n junctions. Initially sensors were fabricated with resistors and bipolar transistors. Later in 1960s with the introduction of MOSFETs, piezoresistive stress sensors based on MOSFETs were introduced to replace the resistor based stress sensors. As stress sensors both MOSFETs and bipolar transistors offer certain advantages over the traditional resistor based sensors. Such potential advantages include size reduction, better sensitivity, wide temperature range capability and easier integration with circuits [9]. Solid-state sensors based on piezoresistive and piezojunction effects are widely used for structural stress analysis in microelectronic fabrication in industrial applications [11, 12].

During the past 50 years the semiconductor industry has achieved a massive development in areas such as smaller sized devices, low power consumption and cost effective designs. In 1965, the Intel co-founder Gordon Moore predicted that the number of transistors on a microprocessor chip will nearly double every 2 years or so [13]. With technological innovations

and scaling down of transistor geometries Moore's law had prevailed for several decades. This has resulted in chips that are significantly faster and have greater complexity in each generation while continuously bringing the cost per transistor down. Until 2000 scaling down was the main technology for improving the performance of MOSFETs. As the transistors scale down to nm technology, due to the practical limitations such as short channel effects, semiconductor industry emerged to seek for other alternatives. Several new innovative technologies such as strained-silicon, high-K gate dielectric, ultrathin body SOI MOSFET, double-gate MOSFETs, double-gate on Si Fin, multi-gate transistor on multiple fins, and tri-gate MOSFETs were developed to keep up with the trend of emerging market demand. The introduction of new technologies, materials and advanced processing steps all together increased the complexity of the chips and packages. The stress distribution also changed rapidly over small scales and the mechanical stress effects become more significant in IC circuits.

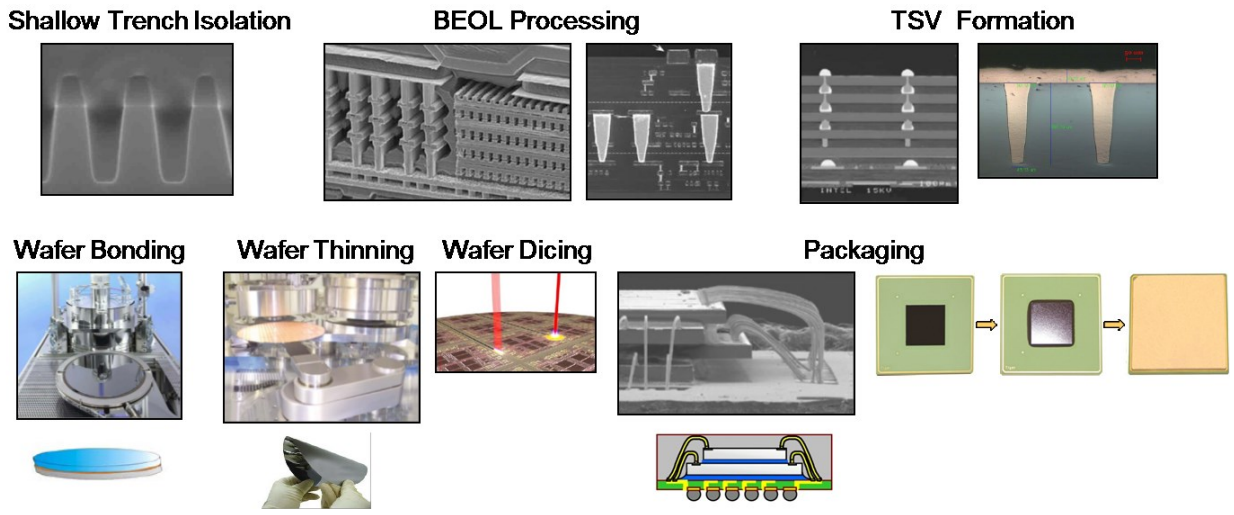


Figure 1.1 – Sources of mechanical stress generation in integrated circuits

Stresses are produced in integrated circuits (IC) by thermal and mechanical loadings. IC chip processing involves several steps with a variety of materials of different thermal and elastic properties. Stress develops during thermal cycling of the chips. Formation of many structural elements such as chemical vapor deposition (CVD) process of silicon dioxide, silicon nitride, polycrystalline silicon, etc. exhibits intrinsic stresses. Large localized stresses are induced in the silicon substrate near the corners and edges of such structural elements [14]. Another cause for mechanical stress is the lattice mismatch of materials used in different processes. Furthermore, shallow trench isolation (STI), back-end-of-line (BEOL) processing, through-silicon-via (TSV), wafer bonding, wafer thinning, wafer dicing, and electronic packaging etc. results mechanical stresses (Figure 1.1). All these stresses may significantly influence the reliability of the semiconductor devices [14-18]. These stresses may collectively lead to failure of the package resulting in cracking of the die, breaking of connections, bond failure, solder fatigue, and encapsulant cracking [6]. Even without producing these adverse effects, stresses may lead to parametric shifts that affect the performance and tolerances of integrated circuits and make them to work out of the specifications [6].

Stress effects are more significant in precision analog circuits such as temperature sensors, bandgap references, current mirrors, PTAT (proportional to absolute temperature) circuits and operational amplifiers. Stress induced parametric shifts affect the reliability of these circuits which mainly work upon precise matching of the transistors. In bipolar transistors the stress induced changes in the mobility and the bandgap affect various parameters such as saturation current, base emitter voltage, dc current gain and make them to work out of specification. Hence, it is extremely important to take steps to mitigate these stress effects.

With the advancements in technology, reducing the process and packaging induced stress effects has become extremely important. Hence, stress investigation and mitigation has become an important area of research. Several researchers have demonstrated the use of silicon stress test chips based on piezoresistive and piezojunction stress sensors to investigate die stresses in electronic packages [6-10]. Currently, in most of the IC processing, stress sensors are incorporated for real-time monitoring of the stress-induced changes during fabrication, processing and packaging to ensure high quality and reliability.

Stress investigations in semiconductor devices gained special attention in 2000s with the introduction of strain engineering. The stress effects in semiconductors differ depending on the direction of current flow, orientation of stress and the type of material. This property is used as an advantage to enhance the mobility of MOSFETs, which is known as strain engineering. Strain-induced mobility enhancement was introduced for MOSFETs at the 90 nm technology node and has since been an active area of research [19]. This is an intentional stress induction widely used in industry at present. For example, SiGe pockets are introduced into the source and drain of PMOS to create the compressive stress in the p-channel area in order to increase the mobility. In the case of NMOS, a highly tensile silicon-nitride capping layer is deposited at the end of the NMOS process covering the source, drain, and gate stack in order to create tensile stresses in the n-channel (Figure 1.2) [19-21]. Currently, strain-induced mobility enhancement is used as an efficient and practical aid for downscaling of MOSFETs.

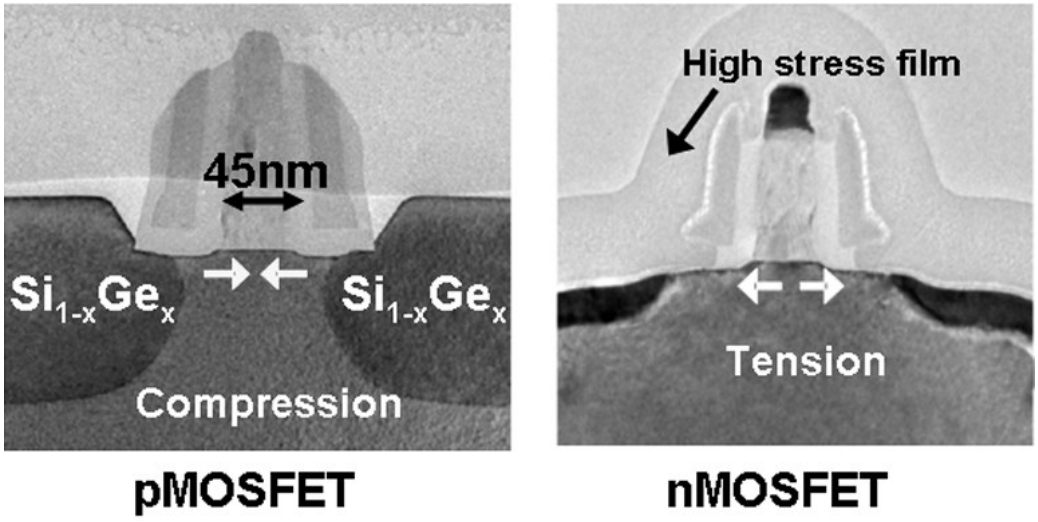


Figure 1.2 – Transmission electron micrographs of 45-nm p-type and n-channel transistors [21]

Similar concept is applicable for bipolar transistors as well. Bandgap and strain engineering is used in SiGe based heterostructure bipolar transistors (HBTs) to improve the performance [22]. In the base of these heterostructures addition of Ge to Si makes the effective base bandgap smaller. Furthermore the compressive stress associated with SiGe alloys produces additional bandgap shrinkage. It is estimated that for each 10% of Ge introduced there will be a net base bandgap reduction of about 75 meV [23]. The major goal of the above processes is the improvement of current gain and frequency by reducing the bandgap of base of BJT. Another way for improvement is mechanical stress induced performance enhancement. Though some studies reported mechanical strain-induced performance enhancement in Si based BJTs [24-28], this approach is not fully developed. Most of these investigations in BJTs or HBTs are focused on the influence of biaxial stresses. However, in fabrication processes biaxial stresses are less preferred because of their integration challenges, process complexity, and higher cost involvement [20]. In contrast uniaxial stresses are more preferred over biaxial stress due to easy integration, higher percentage enhancement [29, 30] and cost effectiveness. Uniaxial stress can

be introduced using an extrinsic stress layer [24] or post fabrication using a cap layer or with packaging [20].

As described above stress effect needs to be improved and applied as beneficial effects in some instances and needs reduced when deemed undesirable in other instances. Main beneficial effects are their usage in sensor applications and strain engineering. However, unintentional stress effects generated during fabrication, processing and packaging are more deleterious in analog and digital circuits. Overall a comprehensive understanding of stress effects in semiconductor devices is necessary to improve the stress effects for sensor applications or strain engineering or to reduce the stress effects when deemed harmful.

1.2 Previous research works on stress effects in bipolar transistors and analog circuits

The saturation current of the bipolar transistor is modified by mechanical stress through the piezojunction effect [31]. Piezojunction effect was first described by Hall, Bardeen, and Pearson in 1951 for hydrostatic pressure on p-n junctions [32]. The theory was based on bandgap widening caused by isotropic stress. In 1962 Rindner observed that the resistance of shallow p-n junction was highly stress-sensitive for anisotropic elastic stresses [33]. During 1960s researchers repeated and extended the experiments where they produced the stress by pressing a stylus on a point of a p-n junction [34-45]. They often reported impressive results including the changes in the current-voltage characteristics, base current, break down voltage, and generation-recombination currents [46-50]. For several years the researchers used very high compressive stress with large stress gradient generated by styli. In 1973 Monteith and Wortman obtained much smaller stresses using cantilever beams instead of styli and reported different behavior for tensile and compressive stress [51].

In 1964 Wortman, Hauser and Burger extended the piezojunction theory to anisotropic high stresses in the range of GPa based upon the stress-induced variations in energy band structure and their effect on minority carrier densities [50]. They developed the equations for the current-voltage characteristics of diodes and transistors under stress. Their results showed that at stress levels greater than 1 GPa the device currents can change by several orders of magnitude when stress levels are changed by a factor of 2. In 1967, the theory was further refined by Kanda considering the changes in effective masses for stresses over 1GPa [52]. Kanda calculated the current change in p-n junction by considering the stress-induced change in minority carrier concentration and mobility. The difference of heavy-hole mass and light-hole mass and their stress dependence were taken into account in addition to the stress dependence of band edge energies when calculating the change in minority carrier concentration. In 1973, Kanda developed a basic framework for the stress dependence of the common-emitter transistor current gain and showed that the stress dependence of current gain of the npn and pnp transistors can be explained by the combined effects of the stress dependence of the emitter efficiency and the stress dependence of the base transport factor [53]. All above research work and models were based on hydrostatic pressure and stress-inducing styli, quite successful for high stress levels, usually over 1 GPa. However, they were not intended for the moderate stress levels usually occur during the fabrication, processing and packaging of semiconductor devices. Until 1980, most investigations of the piezojunction effect have been focused on the design of mechanical sensors.

In 1980s a research group from Delft University started to focus their research work on moderate stress levels ($\approx$200 MPa) that usually occur during the semiconductor fabrication processes. In 1982, Meijer proposed that the mechanical stress might be a dominant factor limiting the accuracy of bandgap references and temperature transducers based on his

experimental work [54, 55]. Fruett researched on piezojunction effect in silicon, its consequences and its applications for integrated circuits and sensors and it's temperature dependences [56] and proposed a new test structure based on cantilever technique to characterize the devices under stress at different temperatures. He used the characterization results of vertical and lateral bipolar transistors on (100) silicon wafers to extract the first- and second-order piezojunction coefficients and temperature dependence and compared with the piezoresistive coefficients. He also investigated about the piezojunction effect related errors caused in temperature-reference voltages used in bandgap references and temperature transducers. He suggested methods to minimize the piezojunction effect in integrated circuits based on the fact that the transistor stress sensitivity depends on the type of the transistor and the stress orientation. He also showed that appropriate transistor selection and proper layout design can be used to mitigate the piezojunction effect in analog circuits [56].

In 2002 Creemer and French developed an analytical model of the effect of mechanical stress on the saturation current of bipolar transistors [31, 57]. They recommended the model for circuit and sensor design, which can be used for tensile as well as compressive stress and suitable for lower than 200 MPa that generally developed during the semiconductor fabrication processes. This model can be used for any orientation with respect to the axis of crystal from which the transistor is fabricated. The model was verified by comparing the results with experimental results of npn and pnp transistors under different stress levels. They extracted the piezojunction and piezoresistive parameters and compared with literature values. Their research focused on the transistor saturation current at normal, forward bias, and at low-level injection. Fruett, Creemer, French and co-workers of Delft University extensively published their research

work on stress effect in saturation current and base emitter voltage of silicon bipolar transistors [5, 57].

In another study Creemer and French modeled the piezojunction effect as a combination of the stress-induced effects in the intrinsic carrier concentration and the carrier mobility. Here the stress effects on the saturation current were expressed as an equivalent change in the base-emitter voltage. Theory was verified with experimental results for npn vertical and pnp lateral transistors for a stress range of -155 MPa to 155 MPa. They observed that, while stress-induced changes in the mobility strongly depended on the orientation of current flow in the base, the changes in intrinsic carrier concentration did not. Based on this observation it was suggested that for a given stress orientation the changes in intrinsic concentration is fixed, but the mobility can still be influenced by giving the transistor a different orientation with respect to the crystal axes. In this way, the mobility change could either amplify or compensate for the intrinsic concentration effect [58].

1.3 Scope of the research

Even though several theoretical and experimental studies have been conducted in stress induced effects in bipolar transistors, the models were based on traditional "piezojunction effect" that characterizes the variation of the saturation current of a pn junction device in terms of a second order set of piezojunction coefficients. This approach provides a solid experimental characterization of the device and allows very good fitting of the stress dependent changes in transistor characteristics. Combined effect of all stress induced variations is straight forwardly modeled by the piezojunction approach. Much of the underlying device behavior may however be masked by merging of variations in mobility and intrinsic carrier concentration in the

piezojunction formulation. This results in the loss of predictive understanding for optimum design. Separation of stress dependent mobility variations from the stress dependent intrinsic carrier concentration in modelling would avoid this short coming. This approach would provide a direct insight regarding transistor design and layout necessary to improve the stress effects for strain engineering or to mitigate the impact of process or packaging induced stress effects on analog circuits.

The focus of this research is as follows:

- To develop a numerical model for rapid stress analysis in bipolar transistors
- To investigate and include appropriate models to represent the stress effects on bipolar transistors
- To characterize the possibility for potential strain engineering in bipolar transistors
- To provide techniques to mitigate the stress effects on bipolar transistors and precision analog circuits.

1.4 Structure of this dissertation

The dissertation is structured as follows:

In chapter 1 an introduction and an overview of stress effects in semiconductor devices especially bipolar transistors, a review of previous research work in this area and the scope of this research work are presented.

Chapter 2 provides a review of the theories on the stress effect on band structure and the carrier mobility.

Chapter 3 describes the theoretical and experimental work of this study. Improved experimental methods used for this work and the characterization results of npn and pnp bipolar transistors in (100) plane are also presented.

Chapter 4 describes the 2-D and 3-D model development with Sentaurus to interpret the stress effect in bipolar transistors. It also includes the comparison of 2-D and 3-D simulation results.

Chapter 5 illustrates a 1-D numerical model development with MATLAB for rapid stress analysis in bipolar transistors and comparison of results with the Sentaurus simulation, and experimental results. It also presents the application of 1-D model to verify the textbook approaches. The early voltage and the current based on Gummel approach are verified in this section. Then stress models are included and the simulation results are analyzed and compared with the experimental results. The residual stresses in bipolar transistors are successfully quantified using this 1-D model. Stress dependent changes in saturation current of npn and pnp transistors are analyzed and compared.

Chapter 6 describes an analysis of opportunities for performance enhancement in vertical and lateral npn and pnp bipolar transistors using uniaxial stress on (100) plane.

Chapter 7 presents a study of stress effects in analog circuits and methods to minimize these stress induced unwanted effects. Spice simulation was performed for some simple analog circuits by including the theoretical models developed in chapter 3 to include the stress effect and the results are presented here.

Finally, Chapter 8 provides the summary and conclusion.

CHAPTER 2

A REVIEW ON STRESS EFFECTS ON SEMICONDUCTOR BAND STRUCTURE AND CARRIER MOBILITY

2.1 Introduction

Mechanical stress in semiconductor devices influences the band structure and the carrier mobility. First the stress generates a mechanical strain, which deforms the band structure. The changes in bands modify the parameters of carrier transport such as the bandgap, intrinsic carrier concentration and carrier mobility through which they change the electrical characteristics of semiconductor devices. This chapter reviews the theories behind the stress effects in semiconductor devices such as the deformation potential theory and piezoresistive theory.

2.2 Stress, strain and tensors

The general state of stress for an infinitesimal unit element (Figure 2.1) can be represented by a symmetric 3 x 3 matrix stress tensor as follows [59, 60]:

$$\sigma_{ij} = \begin{bmatrix} \sigma_{XX} & \sigma_{XY} & \sigma_{XZ} \\ \sigma_{YX} & \sigma_{YY} & \sigma_{YZ} \\ \sigma_{ZX} & \sigma_{ZY} & \sigma_{ZZ} \end{bmatrix} \tag{2.1}$$

where the diagonal elements σ_{XX}, σ_{YY} and σ_{ZZ} are called the normal stresses and, the off-diagonal elements are called the shear stresses. Because of the static equilibrium requirements the stress tensor is always symmetric and it yields:

$$\sigma_{XY} = \sigma_{YX}, \quad \sigma_{XZ} = \sigma_{ZX} \quad \text{and} \quad \sigma_{YZ} = \sigma_{ZY} \tag{2.2}$$

Hence the stress tensor has only 6 independent stress components: 3 normal stress components $\sigma_{XX}, \sigma_{YY}, \sigma_{ZZ}$ and 3 shear components $\sigma_{XY}, \sigma_{YZ}, \sigma_{XZ}$.

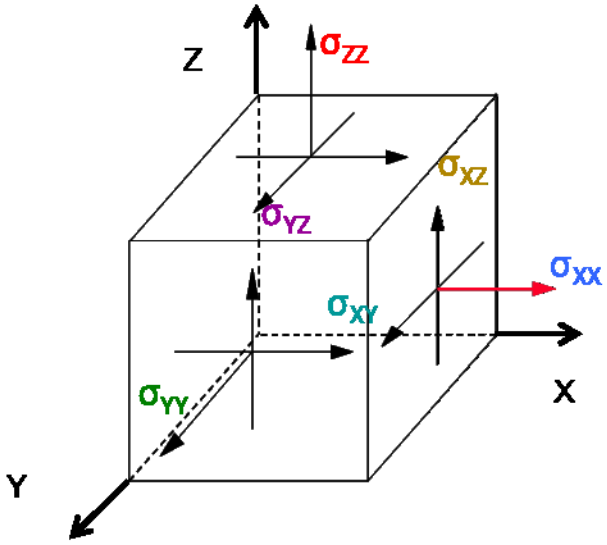


Figure 2.1 – Stress states on an infinitesimal unit element (for clarity, stresses on negative faces are not depicted)

Mechanical strain represents the state of deformation resulting from mechanical stresses. In a similar way, mechanical strain also can be represented by a symmetric second-order tensor as follows:

$$\varepsilon_{ij} = \begin{bmatrix} \varepsilon_{XX} & \varepsilon_{XY} & \varepsilon_{XZ} \\ \varepsilon_{YX} & \varepsilon_{YY} & \varepsilon_{YZ} \\ \varepsilon_{ZX} & \varepsilon_{ZY} & \varepsilon_{ZZ} \end{bmatrix} \tag{2.3}$$

where $\varepsilon_{XX}, \varepsilon_{YY}, \varepsilon_{ZZ}$ are the normal strain components and $2\varepsilon_{XY}, 2\varepsilon_{YZ}, 2\varepsilon_{ZX}$ are the shear strain components. Hook's law states that, for an isotropic, homogeneous material, stress is linearly proportional to the strain [61]. Hence for a solid body within the elastic limit the stress and strain tensors are related by Hooke's law and the following relationships can be obtained between the stress and strain tensors:

$$\sigma_{ij} = C_{ijkl}\varepsilon_{kl} \tag{2.4}$$

where C_{ijkl} are the stiffness constants and

$$\varepsilon_{ij} = S_{ijkl}\sigma_{kl} \tag{2.5}$$

where S_{ijkl} are the compliances.

Since the mechanical stress and strain are symmetric, the compliances and the stiffness constants also acquire this property. Hence the 81 components can be reduced to 36 constants. The equations (2.4) and (2.5) also can be simplified by using only one index for σ and ε, and two indices for S and C. Table 2.1 shows the different notations used in stress analysis.

Table 2.1 – Different notations of stress subscripts and reduced forms

General notation 1	XX	YY	ZZ	YZ=ZY	XZ=ZX	XY=YX
General notation 2	11	22	33	23=32	13=31	12=21
Contracted form	1	2	3	4	5	6

For silicon number of independent compliance coefficients further reduced because of the cubic symmetry. With this reduction (2.4) and (2.5) becomes [59]

$$\varepsilon_i = S_{ij}\sigma_j \quad \text{and} \quad \sigma_i = C_{ij}\varepsilon_j \quad \text{where i, j =1, 2, 3, ….6.} \tag{2.6}$$

$$S_{ij} = \begin{bmatrix} S_{11} & S_{12} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{11} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{12} & S_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & S_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & S_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & S_{44} \end{bmatrix}$$

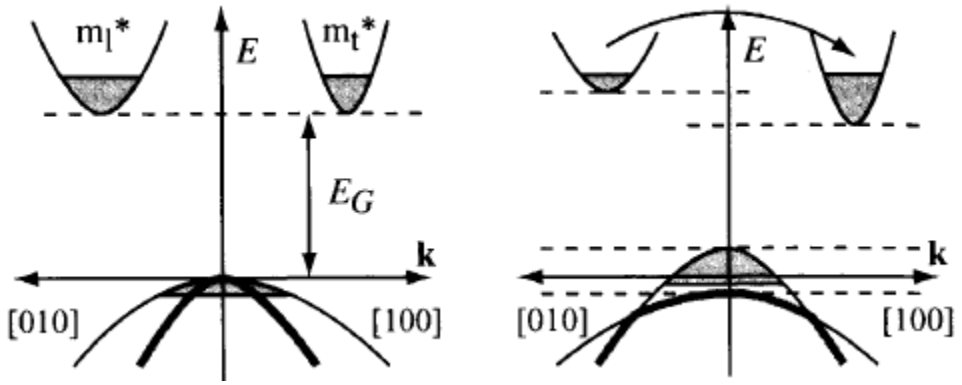
A similar matrix can be written for C as well. The components of compliance and stiffness coefficients are accessible in Table 2.2 [62].

Table 2.2 – The compliance and stiffness coefficients of silicon [62]					
S_{11} [/TPa]	S_{12} [/TPa]	S_{44} [/TPa]	C_{11} [/TPa]	C_{12} [/TPa]	C_{44} [/TPa]
7.68	-2.14	12.6	16.57	6.39	7.96

2.3 Stress effects on semiconductor band structure

In solid-state-physics, the conducting electrons of a crystal behave as quantum-mechanical waves subject to the periodic boundary condition. The electron wave functions adopt the symmetry of the lattice. Since the wave description of electrons is more complex it is often replaced by energy bands, in which the electrons can be considered as semi-classical particles. These bands represent the energy of independent electrons in a material as a function of the wave vector. They are also called band structure or band diagram [57]. In band structures the electrons are located around the minima of the conduction bands and the holes are located around the maxima of the valance bands, which are called the band edges. The band edges are separated by a bandgap, E_G (Figure 2.2(a)). The band structure is characterized by bandgaps, and band curvatures. These curvatures can be interpreted as the inverse effective mass of the carriers [57, 63]. When there is no stress, the edges of each band type have the same energy. But they have different effective masses since they have different curvatures for a given current direction. As the valence band edges degenerate in k=0 due to the symmetry of the crystal they strongly interact and influence each other's masses [5, 63].

Mechanical stress in crystals results in strains on the interatomic distances. The stress shifts the band edges and deforms the curvature. In addition, stress distorts the symmetry of the edges and the edges are no longer at the same energy level. Hence the bandgap is no longer uniquely defined. This influences on the electronic band structure of the crystal. These effects are illustrated in Figure 2.2 (a), in which two edges of the six conduction bands are separated from the two edges of the valence bands by the bandgap in a silicon band structure. The forbidden gap is modified when stress changes the interatomic distances and shifts the band edges to other energies. These shifts are different for each band edge and the forbidden gap splits up as shown in Figure 2.2 (b). In addition, the curvatures of the valence band maxima change when stress destroys the crystal symmetry. This lifts the degeneracy at k=0. Hence strong coupling changes and therefore the effective masses also changes [57].



(a) (b)

Figure 2.2 – Schematic band structure of silicon in the (a) stress-free and the (b) stressed case [57].

2.4 Deformation potential theory

In semiconductors the band structure determines many properties, mainly the conductivity. Initially $\vec{kp}$ method was used to determine the shape of the energy bands around

the band edges, which was based on the perturbation theory and the symmetry of the crystals. Then it was extended to deformed crystals by the formation of deformation potential theory. Deformation potential theory was originally developed by Bardeen and Shockley for the conduction bands [64]. Later it was generalized to include different scattering modes (transverse, longitudinal acoustic modes) by Herring and Vogt [65]. Their model was well suited for n-type silicon but not so for p-type because of its degeneracy and warping of the valence band. Deformation potential theory for the more complicated valence band was initiated by Adams [66] and supplementary contribution was made by Kleiner and Roth [67]. The deformation potential theory was further improved and a comprehensive model was established by Bir and Pikus [63].

Creemer researched on modeling the piezojunction effect of bipolar transistors as a function of uniaxial stress [57]. He modeled the bandstructure from the first principle of Bir and Pikus deformation potential theory [63]. The saturation currents of npn and pnp transistors were determined for different values of stresses in different current-stress orientations. The measurement data were identified with model equations and the piezojunction coefficients were extracted and compared with the literature values. The following two important factors were also reported regarding the stress-induced effects on the conduction band and the valence band of the semiconductors [57]:

(a) Uniaxial strain only shifts the conduction band edges and shear strains has no influence on the conduction band edge energies. However, experiments and theory have shown that shear strain does have some influence.

(b) In the case of valence bands the strain shifts the valance band edge. In addition, strain also deforms the equi-energy surfaces. The deformation of the valance band surface is much

stronger than the deformation of the conduction band surface. This is because in the absence of stress the valance bands are very close to each other, enabling them to influence each other's shape. Consequently, the equi-energy surfaces are warped instead of spherical. However, in the presence of strain the bands are split. This decouples them partially and decreases the warping. Very high strains completely decouple the bands, resulting in ellipsoidal equi-energy surfaces, as in the case of conduction bands. In addition, for specific orientations, strain presses the light-hole band through the heavy-hole band.

The changes in intrinsic carrier concentration ($\Delta n_i^2/n_i^2$) were plotted [57, 68] for a variety of stresses from calculations based upon solid-state physics, incorporating full stress/strain relationship with deformation potentials from the theory of Bir and Pikus. The plots of $\Delta n_i^2/n_i^2$ and the quadratic fit equations to simulation results shown in [69] are presented in Figure 2.3 and Table 2.3 respectively.

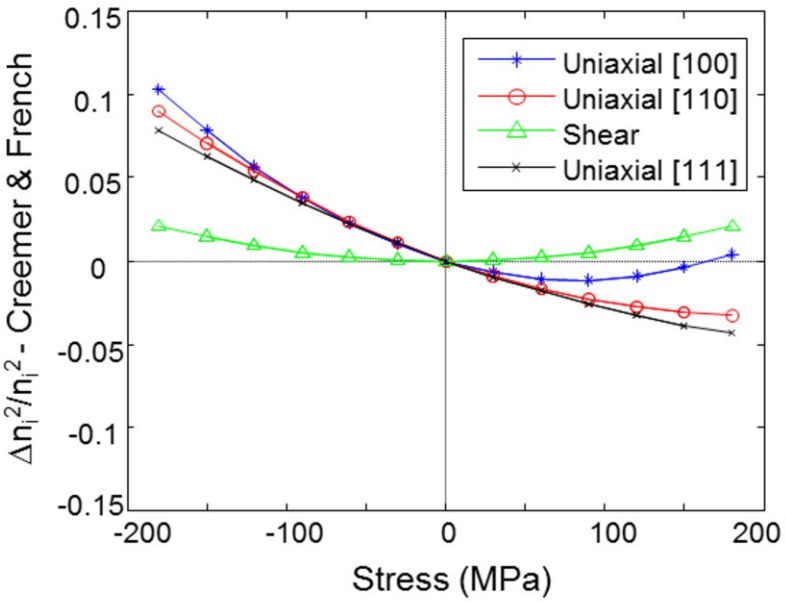


Figure 2.3 – Stress induced change in $\Delta n_i^2/n_i^2$ from Creemer & French [57, 68]

Table 2.3 – Quadratic fits to simulation results of Creemer & French [69]	
Stress orientation	$\Delta n_i^2 / \Delta n_i^2$
<100>	$1.644x10^{-6}\sigma^2$-$2.755x10^{-4}\sigma$
<110>	$8.873x10^{-7}\sigma^2$-$3.403x10^{-4}\sigma$
<111>	$5.285x10^{-7}\sigma^2$-$3.387x10^{-4}\sigma$
Shear	$6.353x10^{-7}\sigma^2$

2.5 Stress effect in mobility

In semiconductor band structure electrons are populated near the edges of the 6 equivalence conduction band valleys along <100> direction. The equi-energy surfaces of six conduction band edges in k-space are shown in Figure 2.4(a). In an individual conduction band valley, the electrons maintain their longitudinal and transverse effective masses (m_l, m_t) to be about $0.91m_o$ and $0.19m_o$ respectively, where m_o is the effective mass of the unstrained Si. Application of mechanical stress breaks the crystal symmetry and split the previously degenerate Δ_6 valleys. Stretching (tensile strain) along <100> axis elevate the energy of the 2-fold valleys on that axis and reduces the energy of the 4-fold valleys on orthogonal axes. Splitting the energy between Δ_2 and Δ_4 valleys results in removal of the degeneracy and suppression of scattering between them. As shown in Figure 2.4(b), tensile strain along [001] direction elevates the energy of the two longitudinal Δ_2 valleys and reduces the energy of the four transverse Δ_4 valleys Figure 2.4(c)). Since lower energy states are favorable for electrons, a redistribution of electrons occurs and more electrons preferably occupy the four lower energy Δ_4 valleys. This results in more electrons with transverse mass and reduction of effective mass in [001] direction. Reductions of effective mass and scattering increase the mobility of electron in [001] direction. The

compressive stress along [100] direction also removes the degeneracy between the Δ_2 and Δ_4 valleys. But the energy of Δ_2 valleys reduces with respect to Δ_4 valleys. As a result more electrons transfer to Δ_2 valleys and move with longitudinal effective mass reducing the mobility. In general, average mobility of electron is increased in the direction of tension (longitudinal effect) and lowered transverse to that direction (transverse effect). Compression has the opposite effect. For conduction band the strain mainly shifts the band edge while keeping the shape unchanged.

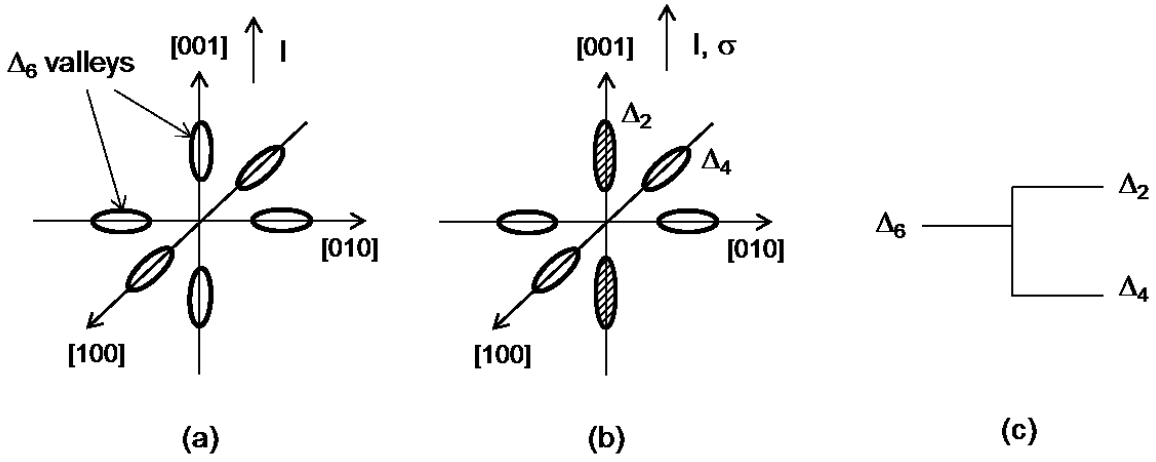


Figure 2.4 – Conduction band (a) unstrained (b) uniaxial tensile strain in [001] direction (c) band energy splitting

Stress effects in hole mobility is more complex. The application of strain splits the normally degenerate light-hole and heavy-hole bands, causing the light-hole band to shift upwards to the top of the valence band. Further, the curvature of the bands is modified, changing the hole effective mass parallel and perpendicular to the interface. The applied strain changes the shape of the valence band also. Due to the complexity of the valence band structure and the band warping, stress effects in hole mobility was not well understood for a long time. However,

computational advances have aided a better understanding of hole mobility changes with stress. This was possible because most research and commercial semiconductor devices are p-type and models of this successful technology had been mostly based on empirical results. Theoretical studies based on the strain Hamiltonian and on deformation potentials in strained silicon as well as cyclotron resonance experimental results have revealed several factors such as band warping and band splitting, mass change etc. that affect hole mobilities in semiconductors. Earlier, piezoresistive technology drew from mainstream IC research and continues to do so. More recently, with the strong interest in ‘‘strain engineering’’ to increase transport speed in ICs, mainstream semiconductor technology is drawing on findings of piezoresistive research [60]. Figure 2.5 shows hole mobility enhancement factor for uniaxial longitudinal compressive and biaxial tensile-stress on (100) wafer and (110) wafer surfaces (channel orientation <110>).

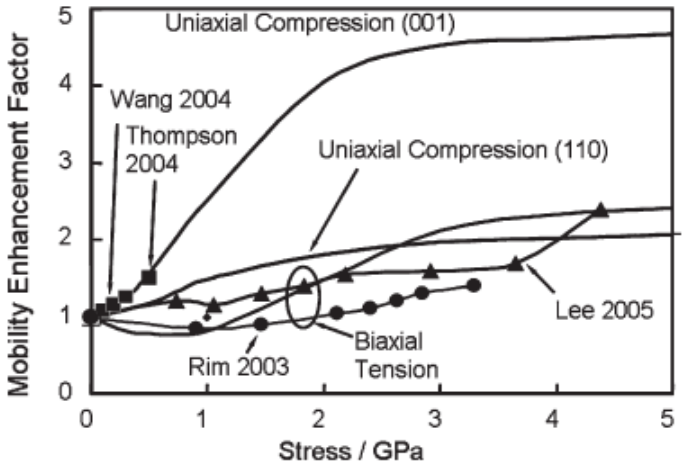


Figure 2.5 - Calculated and experimental data for uniaxial longitudinal compressive and biaxial tensile-stress-enhanced hole mobility versus stress (biaxial stress = $\sigma_{XX}+\sigma_{YY}$) [29].

As illustrated, generally experimental piezoresistive coefficients are used as successful quantitative predictors for stress-induced changes in carrier mobility in both research and

industrial applications. A review on piezoresistive theory and its development are presented in detail below.

2.6 Piezoresistive concept development

In 1954 Smith observed that uniaxial tension causes a change of resistivity in both n- and p-types Si germanium Ge. He measured the resistance for different electrode configuration (longitudinal and transverse) by applying uniaxial tensile stress to several single crystal Si and Ge rods. By repeating the measurements for several different crystal orientations, and for longitudinal and transverse measurement of resistance, all elements of piezoresistive tensor were able to be deduced. The piezoresistive coefficients from his experimental work for lightly doped Si are presented in Table 2.4 [1] where π_{11}, π_{12}, are the longitudinal and transverse piezoresistive coefficients and π_{44} is the shear coefficient. He also reported that in these materials the change in resistance caused by stress induced dimensional changes is small that allows any remaining effect to be expressed as a change in resistivity, ρ. The resistivity may be stress dependent through either the mobility or the number of the charge carriers. He reported the effect of stress on the mobility of the charge carriers for many so-called "piezoresistive materials" and also mentioned that in semiconductors the stress may be expected to change the number of charge carriers. Since then, extensive research work has been conducted to study the piezoresistive effect and its relation to other parameters like resistivity, mobility, impurity concentration, temperature, etc. [1, 70-74].

Table 2.4 – Piezoresistive coefficient values for lightly doped silicon $(TPa)^{-1}$ [1]		
Piezoresistive Coefficient	n-type silicon	p-type silicon
π_{11}	-1022	66
π_{12}	534	-11
π_{44}	-136	1381

The change in resistance of a piezoresistive conductor can be expressed in terms of the applied stress, the piezoresistive coefficients and the temperature coefficient of resistance [6]. Piezoresistive coefficients and their dependency on doping and temperature were experimentally studied by several researchers [73, 75, 76]. In 1982, Kanda provided a graphical representation of the longitudinal and transverse piezoresistive coefficients in silicon as a function of the crystal directions for orientations in the (100), (110), and (211) planes [74]. He also presented about the dependency of piezoresistive coefficients on temperature and impurity concentration of the material. In addition, several experimental and analytical studies for the first and second order piezoresistive coefficients in both p- and n-type silicon have also been provided [52, 53, 77, 78]. Cho, Jaeger and Suhling presented temperature dependence of piezoresistive coefficients for silicon for a wide temperature range from -150° C to 125° C based on their experimental characterization results [79].

2.7 Piezoresistive theory

Relationship between resistance and mobility in piezoresistive material

The resistance R of a rectangular conducting material is given by

$$R = \rho \frac{l}{wt} \tag{2.7}$$

where ρ is the resistivity, l , w and t are the length, width and thickness of the conducting material respectively. When a stress is applied the material will deform and the relative dimension changes will be Δl/l, Δw/w, Δt/t, and all of which contribute to the resistance change. The resistivity ρ may also change for so-called "piezoresistive materials" such as Si and Ge. For the materials like metals the dimensional change dominates since there is no piezoresistive effect. But for the materials with piezoresistive effect the change in resistivity dominates and dimensional change can be neglected. Therefore, the change in resistance for the piezoresistive materials can be given as

$$\frac{\Delta R}{R} \cong \frac{\Delta \rho}{\rho} \tag{2.8}$$

The conductivity of a semiconductor material is determined by both majority and minority carrier concentration and their mobility as

$$\sigma = qn\mu_n + qp\mu_p \tag{2.9}$$

For a doped semiconductor with complete ionization, the majority carrier concentration is very much higher than the minority carrier concentration and is almost equal to the doping concentration. Hence, neglecting the minority carrier concentration, the conductivity of n-type silicon can be rewritten as

$$\sigma \cong qn\mu_n \tag{2.10}$$

It is analogous for p-type material. As per (2.10) the conductivity is proportional to the mobility. The resistivity is the reciprocal of the conductivity. All of these relationships yield the following associations for the piezoresistivity.

$$\frac{\Delta R}{R} = \frac{\Delta \rho}{\rho} = -\frac{\Delta \sigma}{\sigma} = -\frac{\Delta \mu}{\mu} \tag{2.11}$$

Piezeresistive effect in an arbitrarily oriented conductor

Piezoresistivity is an anisotropic property can be modelled mathematically as

$$\rho_{ij} = \rho_{ij}^{o} + \pi_{ijkl}\sigma_{kl} + \Lambda_{ijklmn}\sigma_{kl}\sigma_{mn} + ... \tag{2.12}$$

where ρ_{ij}^{o} is the isotropic resistivity of stress free material, and $\pi_{ijkl,}$ Λ_{ijklmn} are components of fourth, sixth order piezoresistance tensors which characterize the stress-induced resistivity change, and σ_{kl}, σ_{mn} are components of the stress tensor. For sufficiently small stress levels, (2.12) can be truncated so that the resistivity components are linearly related to the stress components as

$$\rho_{ij} = \rho_{ij}^{o} + \pi_{ijkl}\sigma_{kl}. \tag{2.13}$$

In practice, it is very common to use the off-axis primed coordinate system for mechanical stress analysis. Primed coordinate system is a coordinate system rotated with respect to the principal crystallographic axis.

For an arbitrarily rotated orthogonal primed coordinate system (2.13) can be written as

$$\rho'_{ij} = \rho_{ij}^{o}{}' + \pi'_{ijkl}\sigma'_{kl}. \tag{2.14}$$

where π', σ' are the fourth order piezoresistance tensor, and the second order stress tensor respectively in the rotated coordinate system. Using reduced index notation, (2.14) further reduced as

$$\rho'_{\alpha} = \rho_{\alpha}^{o}{}' + \bar{\rho}\pi'_{\alpha\beta}\sigma'_{\beta} \tag{2.15}$$

$$\frac{\Delta\rho'_{\alpha}}{\bar{\rho}} = \pi'_{\alpha\beta}\sigma'_{\beta} \tag{2.16}$$

where $\bar{\rho}$ is the mean unstressed resistivity, $\alpha, \beta = 1, 2, 3 \ldots, 6$, and

$$\pi'_{\alpha\beta} = T\,\pi_{\alpha\beta}\,T^{-1} \tag{2.17}$$

and $\pi_{\alpha\beta}$ is the 6x6 piezoresistance coefficients matrix tensor given by [10]:

$$\pi_{\alpha\beta} = \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{bmatrix} \tag{2.18}$$

with $\pi_{11,}$ $\pi_{12,}$ π_{44} are the longitudinal, transverse and shear coefficients respectively. T is a 6x6 transformation matrix related by the direction cosines for the unprimed and primed coordinate systems as follows [10]:

$$T = \begin{bmatrix} l_1^2 & m_1^2 & n_1^2 & 2l_1n_1 & 2l_1n_1 & 2l_1n_1 \\ l_2^2 & l_2^2 & l_2^2 & 2l_2n_2 & 2l_2n_2 & 2l_2n_2 \\ l_3^2 & l_3^2 & l_3^2 & 2l_3n_3 & 2l_3n_3 & 2l_3n_3 \\ l_1l_3 & m_1m_3 & n_1n_3 & (l_1n_3 + l_3n_1) & (m_1n_3 + m_3n_1) & (l_1m_3 + l_3m_1) \\ l_2l_3 & m_2m_3 & n_2n_3 & (l_2n_3 + l_3n_2) & (m_2n_3 + m_3n_2) & (l_2m_3 + l_3m_2) \\ l_1l_2 & m_1m_2 & n_1n_2 & (l_1n_2 + l_2n_1) & (m_1n_2 + m_2n_1) & (l_1m_2 + l_2m_1) \end{bmatrix} \tag{2.19}$$

where l_1, l_2, l_3, m_1, m_2, m_3, n_1, n_2, n_3, are direction cosines for the primed and unprimed coordinate systems which can be given as [10]

$$a_{ij} = \cos(x'_i, x_j) = \begin{bmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{bmatrix} = \begin{bmatrix} l_1 & m_1 & n_1 \\ l_2 & m_2 & n_2 \\ l_3 & m_3 & n_3 \end{bmatrix} \tag{2.20}$$

Let's consider an arbitrarily oriented filamentary conductor in an orthogonal coordinate system (x_1,x_2, x_3), where the unprimed axes x_1 =[100], x_2=[010], and x_3=[001] are the principal crystallographic directions of a cubic silicon crystal as shown in Figure 2.6.

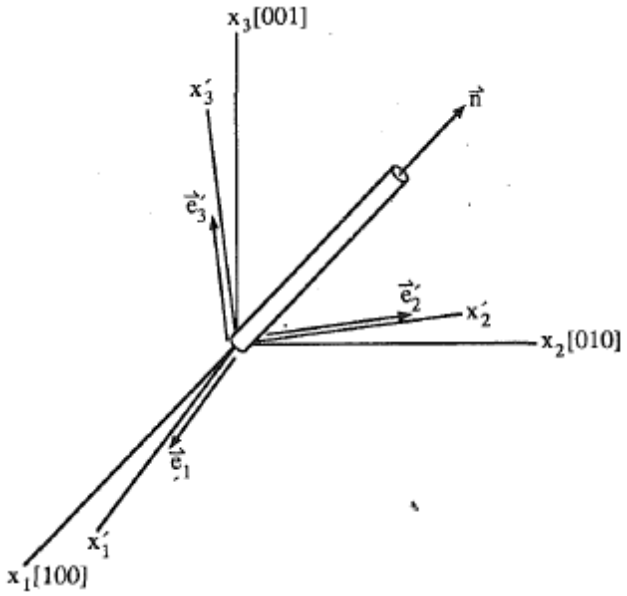


Figure 2.6 - Filamentary conductor arbitrarily oriented with respect to an off-axis coordinate system [10].

The normalized change in the resistivity for the above conductor in terms of the off-axis stress components is given as

$$\frac{\Delta\rho'}{\rho} = (\pi'_{1\alpha}\sigma'_{\alpha})l'^2 + (\pi'_{2\alpha}\sigma'_{\alpha})m'^2 + (\pi'_{3\alpha}\sigma'_{\alpha})n'^2 + 2(\pi'_{4\alpha}\sigma'_{\alpha})n'l' + 2(\pi'_{5\alpha}\sigma'_{\alpha})m'n' + 2(\pi'_{6\alpha}\sigma'_{\alpha})l'm' \tag{2.21}$$

where l′, m′, n′ are the direction cosines of the conductor with respect to the primed coordinate system (x'_1, x'_2, x'_3).

Piezoresistive effect in (100) wafer plane

Figure 2.7 shows a general (100) silicon wafer plane most commonly used in semiconductor industry.

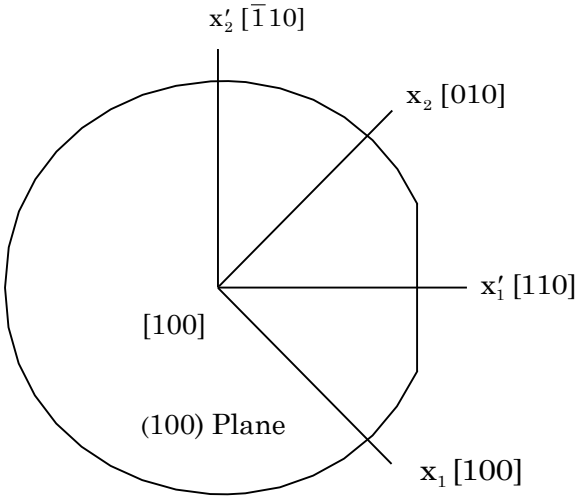


Figure 2.7 - (100) Wafer plane [10]

The crystallographic (unprimed) coordinate axis x_1=[100], x_2=[010], x_3=[001] and the primed axes $x_1' = [110]$, $x_2' = [\bar{1}10]$, and $x_3' = [001]$ are shown. The primed coordinate system coincides with the wafer coordinate system where the axis x_1', x_2' are parallel and perpendicular to the primary wafer flat and the x_3' axis is perpendicular to the wafer plane. Using (2.21) the resistance change of an arbitrarily oriented conductor may be expressed in terms of the stress components derived in this primed coordinate system. For the unprimed and primed coordinate systems shown in Figure 2.5, the appropriate direction cosines for the primed axes are shown as follows:

$$a_{ij} = \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & 0 \\ -\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{2.22}$$

For a vertical transistor on this plane the current direction is perpendicular to the wafer plane, and the direction cosines of the conductor l′, m′, n′ with respect to the primed coordinate system

will take the values {l′,m′,n′} = {0,0,1}. Substituting the direction cosines in (2.17) the piezoresistance coefficients in primed coordinate system for (100) plane can be calculated as

$$\pi'_{\alpha\beta} = \begin{bmatrix} \frac{\pi_S + \pi_{44}}{2} & \frac{\pi_S - \pi_{44}}{2} & \pi_{12} & 0 & 0 & 0 \\ \frac{\pi_S - \pi_{44}}{2} & \frac{\pi_S + \pi_{44}}{2} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{11} - \pi_{12} \end{bmatrix} \tag{2.23}$$

where $\pi_S = \pi_{11} + \pi_{12}$.

Plugging the above piezoresistance coefficients and direction cosines in (2.21) the resistivity equation for vertical transistor on (100) plane reduces to the form

$$\frac{\Delta\rho'}{\rho} = \pi_{12}(\sigma'_{11} + \sigma'_{22}) + \pi_{11}\sigma'_{33} \tag{2.24}$$

Hence the stress dependent of mobility becomes

$$\frac{\Delta\mu'}{\mu} = \frac{\Delta\mu}{\mu} = \frac{\Delta\mu_{100}}{\mu_{100}} = -\pi_{12}(\sigma'_{11} + \sigma'_{22}) - \pi_{11}\sigma'_{33} \tag{2.25}$$

where μ is the doping dependence mobility.

Piezeresistive effect in (111) wafer plane

The next common silicon wafer orientation used in semiconductor fabrication is the (111) plane. A general (111) silicon wafer is shown in Figure 2.8.

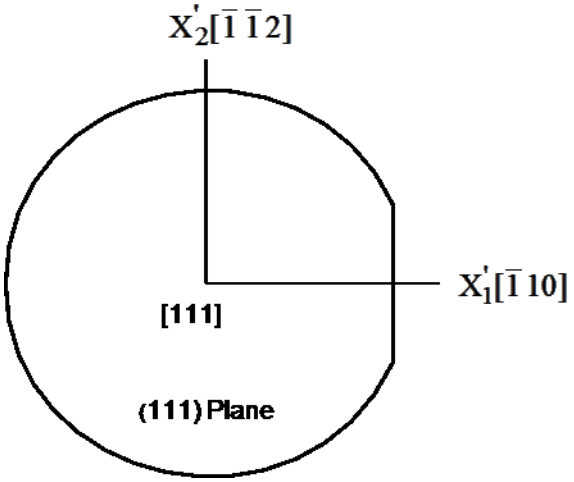


Figure 2.8 - (111) Wafer plane [10]

The surface of the wafer is a (111) plane, and the [111] direction is normal to the wafer plane. The principal crystallographic axes x1 = [100], x2 = [010], and x3 = [001] do not lie in this wafer plane. The natural wafer coordinate system for this plane is $x_1' = [\bar{1}\,10]$, $x_2' = [\bar{1}\,\bar{1}\,2]$, $x_3' = [111]$ where x_1' and x_2' are parallel and perpendicular to the primary wafer flat respectively, and x_3' is normal to the plane. For the primed coordinate system indicated in Figure 2.7, the appropriate direction cosines for the primed axes are as follows:

$$a_{ij} = \begin{bmatrix} -\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & 0 \\ -\frac{1}{\sqrt{6}} & \frac{1}{\sqrt{6}} & \frac{2}{\sqrt{6}} \\ \frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} \end{bmatrix} \tag{2.26}$$

Similar to the previous case, for a vertical transistor the current direction is perpendicular to the wafer plane and the direction cosines of the conductor l′, m′, n′ with respect to the primed coordinate system will take the values {l′,m′,n′} = {0,0,1}.

In a similar way, stress dependent of mobility for vertical transistor on (111) plane can be given as

$$\frac{\Delta\mu}{\mu} = \frac{\Delta\mu_{111}}{\mu_{111}} = -B_3(\sigma'_{11} + \sigma'_{22}) - (B_1 + B_2 - B_3)\sigma'_{33} \tag{2.27}$$

where $B_1 = \frac{\pi_{11} + \pi_{12} + \pi_{44}}{2}$, $B_2 = \frac{\pi_{11} + 5\pi_{12} - \pi_{44}}{6}$, $B_3 = \frac{\pi_{11} + 2\pi_{12} - \pi_{44}}{3}$

are a set of linearly independent combined piezoresistive parameters.

2.8 Summary

This chapter starts with a basic explanation about the stress, strain, tensor, notations and the relationship between the mechanical stress and strain. Then a detailed explanation on the theories behind the stress effects in semiconductor materials is given. A review on development of two main theoretical concepts, the deformation potential theory and the piezoresistive theory are explained. Literature studies indicated that the piezoresistive effect for holes was dominated by deformation of the equi-energy surfaces of the valance bands whereas the piezoresistive effect for electrons was dominated by the shifts of the conduction band edges. The expressions for the stress-induced mobility changes in an arbitrary conductor and the expressions for the stress-induced changes in mobility for vertical transistor on (100) and (111) silicon planes are also given.

CHAPTER 3

STRESS EFFECTS IN BIPOLAR TRANSISTORS-THEORETICAL AND EXPERIMENTAL

3.1 Introduction

This chapter demonstrates the bipolar transistor structures used in this study, modeling of stress effect in bipolar transistor, a one-dimensional theory for the stress effects in bipolar transistors, an improved technique developed for the experimental works, the characterization procedures, and some characterization results of bipolar transistors on (100) plane.

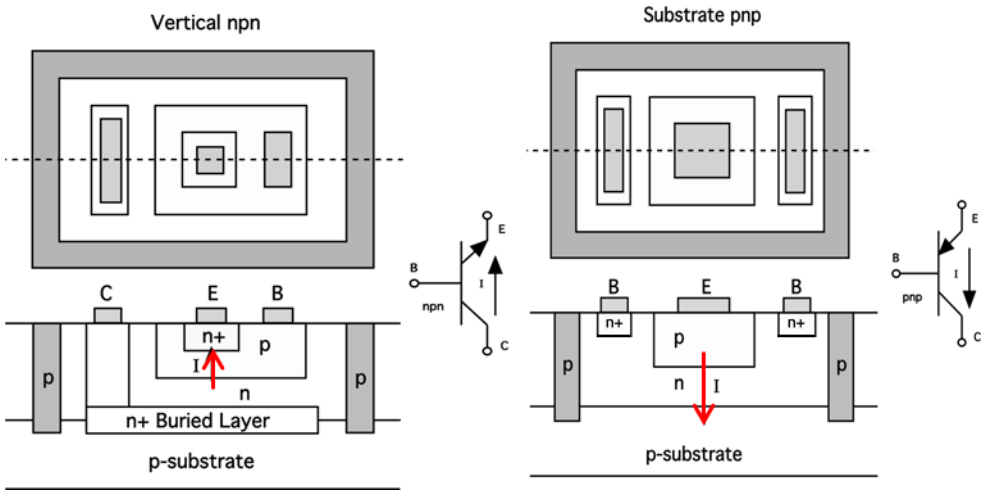
3.2 Bipolar devices used for characterization and simulation

Vertical and lateral npn/pnp transistors on (100) and (111) planes were utilized in this study. The experimental characterization was performed on vertical npn and pnp transistors on (100) plane and npn transistor on (111) plane. Numerical simulation was performed on both vertical and lateral transistors on (100) and (111) silicon planes.

3.2.1 Vertical transistors

These are the most common transistors used in circuit design. In vertical transistors the main current flow in the base is normal to the wafer surface as indicated in Figure 3.1. The carriers are commonly collected by a highly doped buried layer. These collected carriers are transported to the top surface using sinker structures. The buried layer and sinker structures are highly doped to keep the resistivity low. The base is very thin in vertical transistors making them to work very faster than lateral transistors. Vertical npn transistors are suitable for high performance applications because of their high dc current gains. Another main advantage of

vertical transistors over the lateral devices is that they will not be affected by surface non-idealities since the current does not flow near the surface. Therefore they are suitable for temperature sensors. The vertical transistors have better exponential relationship between the collector current and the base-emitter voltage and hence they are preferred over the lateral transistors in temperature-reference voltage circuits. Vertical pnp transistors are used for voltage references and temperature sensors.



(a) (b)

Figure 3.1 – Vertical bipolar devices (a) vertical npn transistor (b) vertical pnp transistor (substrate pnp transistor). The main current flow directions are indicated, C is the collector, B is the base and E is the emitter

3.2.2 Lateral transistors

In contrast to the vertical transistors, the dominant current flow is in a direction parallel to the wafer surface in lateral bipolar transistors as shown in Figure 3.2. This difference plays an important role when considering the mechanical stress effects. Again lateral transistors can be categorized into two as unidirectional devices (Figure 3.2(a)) and multidirectional devices (Figure 3.2(b)). Lateral transistors are widely used in linear integrated circuits as active load

devices, current sources and level shifters. In comparison with vertical npn transistors, the lateral pnp transistors have a lower current gain (<50), low maximum transit frequencies (<100MHz), and lower collector currents [80].

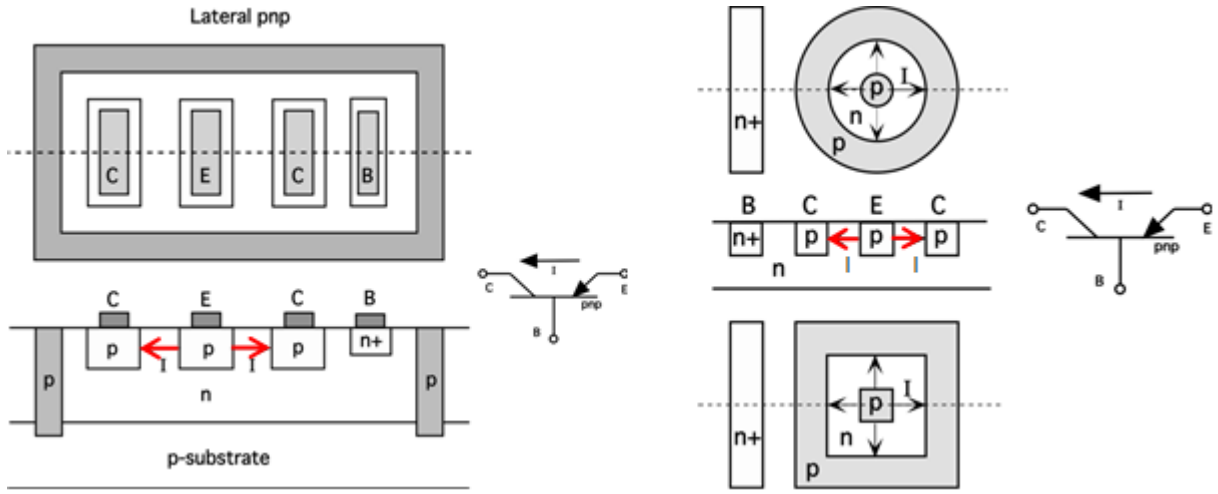


Figure 3.2 – Lateral bipolar devices (a) unidirectional pnp transistor (b) multidirectional pnp transistor. The main current flow directions are indicated, C is the collector, B is the base and E is the emitter

3.3 Modeling the mechanical stress effects in bipolar transistor

For a bipolar transistor shown in Figure 3.3, the collector current (I_C) and the base current (I_B) are related to the base-emitter voltage (V_{BE}) and the base-collector voltage (V_{CE}) in the forward-active region as per the following well-known relationship

$$I_C = \beta I_B = I_S \exp\left(\frac{qV_{BE}}{kT} - 1\right)\left(1 + \frac{V_{CE}}{V_A}\right) \quad \text{and} \quad \beta = \frac{I_C}{I_B} \tag{3.1}$$

where β is the dc current gain, I_S is the saturation current, V_A is the Early voltage, q is the electron charge, k is the Boltzmann constant, and T is the absolute temperature. Stress induced changes in I_S, β, and V_A makes changes in the current-voltage characteristics of bipolar transistor

and affect the performance. Based upon (3.1) the fractional changes in the collector current and the current gain at a given operating point can be given as

$$\frac{\Delta I_C}{I_C} = \frac{\Delta I_S}{I_S} - \left(\frac{V_{CE}}{V_A + V_{CE}}\right)\left(\frac{\Delta V_A}{V_A}\right) \quad \text{and} \quad \frac{\Delta \beta}{\beta} = \frac{\Delta I_C}{I_C} - \frac{\Delta I_B}{I_B} \tag{3.2}$$

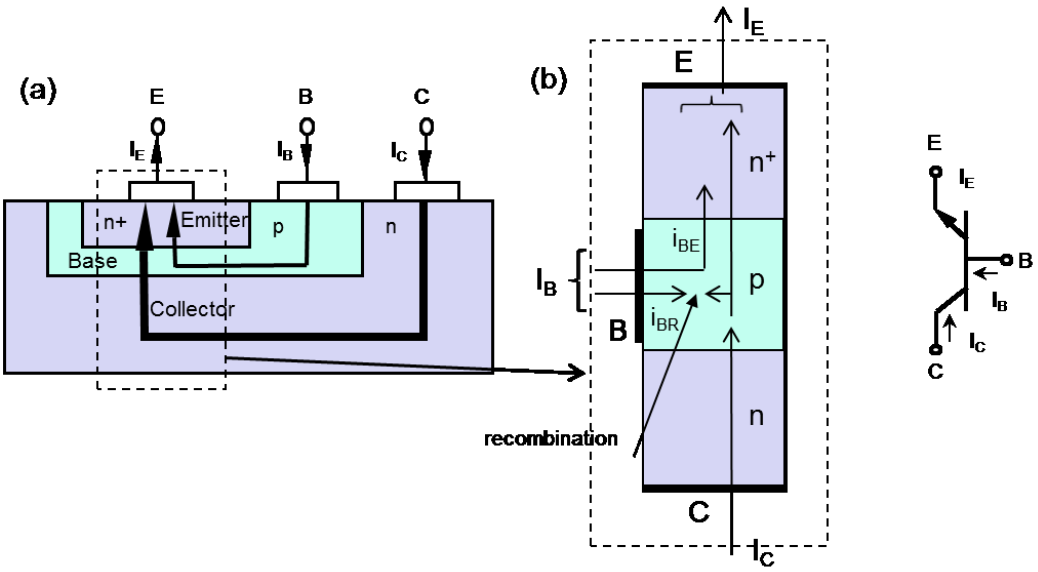


Figure 3.3 - A vertical npn transistor (a) simplified cross-section (b) simplified block model showing the current components

Experimental results demonstrated that the stress-induced changes in Early voltage are very small and negligible [81]. Hence (3.2) can be reduced to the following form:

$$\frac{\Delta I_C}{I_C} = \frac{\Delta I_S}{I_S} \tag{3.3}$$

It shows that the stress act on the relationship in (3.1) through the saturation current. This stress dependence is known as the piezojunction effect, which includes the change in the minority-carrier mobility and the intrinsic carrier concentration. These effects cause variations in the saturation current I_S of bipolar transistors as follows:

$$I_S \propto \mu n_i^2 \quad \text{and} \quad n_i^2 \propto N_C N_V \exp\left(-\frac{E_G}{kT}\right) \tag{3.4}$$

where μ represents the minority-carrier mobility. The intrinsic carrier concentration is related to the densities of states in the conduction and valance bands, N_C and N_V, respectively. The intrinsic carrier concentration is also exponentially dependent upon the bandgap energy E_G. N_C and N_V are dependent upon the effective masses of the carriers and hence in turn dependent on the energy band curvature. In this work, we separately consider the change in mobility and the change in intrinsic carrier concentration as in [56, 68]:

$$\frac{\Delta I_S}{I_S} = \frac{\Delta \mu}{\mu} + \frac{\Delta {n_i}^2}{{n_i}^2} \tag{3.5}$$

This approach provides new insight into the coupling of stress with the physics of the bipolar transistor.

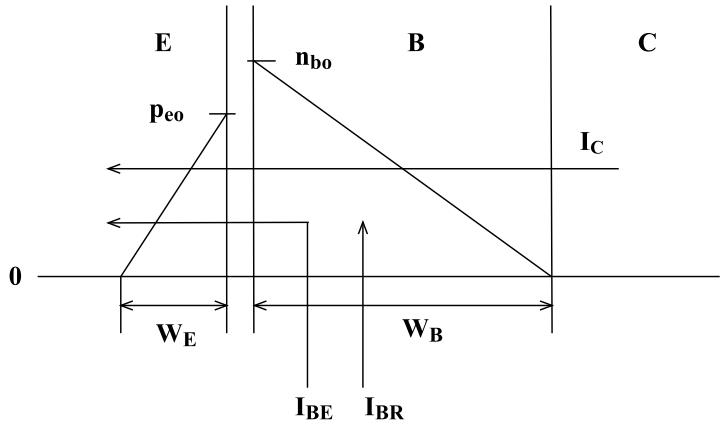


Figure 3.4 - One dimensional npn transistor

One-dimensional transistor model in Figure 3.4 shows the important currents in an npn transistor including collector current I_C and the two important base current terms, I_{BE} representing the back injection into the emitter, and I_{BR} representing recombination in the base. In this work, we are most interested in modeling collector current and current gain, or

equivalently collector current and base current, and to a lesser extent the Early voltage. Note that this is a vertical npn transistor and hence the "horizontal" currents are all actually directed normal to the wafer surface as in the transistor in Figure 3.3.

3.3.1 Vertical npn transistors on (100) silicon

Using the classical bipolar transistor theory, the stress dependence of different current components can be represented as follows in which G_B and G_E represents the Gummel number in the base and emitter and A_E and A_B are the emitter and base area.

Collector current

$$I_C \propto \frac{qA_B}{G_B}\overline{D}_{nB}n_{iB}^2 = V_T\frac{qA_B}{G_B}\overline{\mu}_{nB}n_{iB}^2 \qquad \text{with} \quad G_B = \int_{Base} p(x)dx \cong \int_{Base} N_A(x)dx \tag{3.6}$$

Base current due to back injection

$$I_{BE} \propto qA_E\frac{\overline{D_{pE}}}{G_E}n_{iE}^2 = \frac{qA_EV_T}{G_E}\overline{\mu}_{pE}n_{iE}^2 \quad \text{where} \quad G_E = \int_{Emitter} n(x)dx \cong \int_{Emitter} N_D(x)dx \tag{3.7}$$

Base current due to recombination

$$I_{BR} = qA_B\int\frac{n-n_{BO}}{\tau_{nB}} \propto \frac{n_{iB}^2}{\tau_{nB}} \tag{3.8}$$

Using (3.6-3.8), the normalized changes in the collector and base currents can be written in the form of

$$\frac{\Delta\mu}{\mu} + \frac{\Delta n_i^2}{n_i^2} = \pi\sigma + \frac{\Delta n_i^2}{n_i^2} \tag{3.9}$$

The results from (2.25) are also incorporated to get the following forms:

$$\frac{\Delta I_C}{I_C} = \frac{\Delta I_S}{I_S} = \frac{\Delta \mu_{nB}}{\mu_{\mathbf{nB}}} + \frac{\Delta n_{iB}^2}{n_{iB}^2} = -\pi_{12}^{nB}\left(\sigma'_{11} + \sigma'_{22}\right) - \pi_{11}^{nB}\sigma'_{33} + \frac{\Delta n_{iB}^2}{n_{iB}^2}$$

$$\frac{\Delta \mathrm{I_{BE}}}{\mathrm{I_{BE}}} = \frac{\Delta \mu_{pE}}{\mu_{pE}} + \frac{\Delta n_{iE}^2}{n_{iE}^2} = -\pi_{12}^{pE}\left(\sigma'_{11} + \sigma'_{22}\right) - \pi_{11}^{pE}\sigma'_{33} + \frac{\Delta n_{iE}^2}{n_{iE}^2} \tag{3.10}$$

$$\frac{\Delta I_{BR}}{I_{BR}} = \frac{\Delta n_{iB}^2}{n_{iB}^2} - \frac{\Delta \tau_{nB}}{\tau_{nB}} \cong \frac{\Delta n_{iB}^2}{n_{iB}^2}$$

The values of n_{iE} and n_{iB} may differ due to bandgap narrowing in the emitter, and material differences in the base and emitter. Hence it is possible that the fractional changes in intrinsic carrier concentrations in the base and emitter under stress are not identical.

3.3.2 Vertical pnp transistors on (100) silicon

Similarly the expressions for the collector and base currents of pnp transistors are obtained with appropriate changes in the piezoresistive coefficients for holes and electrons. The intrinsic carrier concentration does not depend on the material type; hence it remains the same.

Collector current

$$\frac{\Delta I_C}{I_C} = \frac{\Delta I_S}{I_S} = \frac{\Delta \mu_{nB}}{\mu_{p\mathbf{B}}} + \frac{\Delta n_{iB}^2}{n_{iB}^2} = -\pi_{12}^{pB}\left(\sigma'_{11} + \sigma'_{22}\right) - \pi_{11}^{pB}\sigma'_{33} + \frac{\Delta n_{iB}^2}{n_{iB}^2} \tag{3.11}$$

Base current due to back injection

$$\frac{\Delta \mathrm{I_{BE}}}{\mathrm{I_{BE}}} = \frac{\Delta \mu_{nE}}{\mu_{nE}} + \frac{\Delta n_{iE}^2}{n_{iE}^2} = -\pi_{12}^{nE}\left(\sigma'_{11} + \sigma'_{22}\right) - \pi_{11}^{nE}\sigma'_{33} + \frac{\Delta n_{iE}^2}{n_{iE}^2} \tag{3.12}$$

Base current due to recombination

$$\frac{\Delta I_{BR}}{I_{BR}} = \frac{\Delta n_{iB}^2}{n_{iB}^2} - \frac{\Delta \tau_{pB}}{\tau_{pB}} \cong \frac{\Delta n_{iB}^2}{n_{iB}^2} \tag{3.13}$$

Current gain expressions for both npn and pnp transistors

The overall current gains for both npn and pnp transistors can now be written as

$$\beta = \frac{I_C}{I_{BE} + I_{BR}} \tag{3.14}$$

and

$$\frac{\Delta\beta}{\beta} = \frac{\Delta I_C}{I_C} - \frac{\Delta I_B}{I_B} = \frac{\Delta I_C}{I_C} - \delta\frac{I_{BE}}{I_{BE}} - (1-\delta)\frac{I_{BR}}{I_{BR}} \tag{3.15}$$

$$\text{where} \quad \delta = \frac{I_{BE}}{I_{BE} + I_{BR}}$$

In another way, the changes in dc current gain can be described as the changes in injection limited and recombination limited terms as:

$$\frac{\Delta\beta}{\beta} = \delta\frac{\Delta\beta_\gamma}{\beta_\gamma} + (1-\delta)\frac{\Delta\beta_{T'}}{\beta_{T'}} \tag{3.16}$$

where β_γ is the injection limited current gain and $\beta_{T'}$ is the transport limited current gain. Parameter δ represents the fraction of current gain that is determined by back injection into the emitter. δ = 1 corresponds to 100% back injection, and δ = 0 corresponds to 100 % recombination.

The injection limited current gain and the transport limited current gain for a vertical npn transistor on (100) plane can be separately written as

Injection limited current gain for an npn transistor

$$\frac{\Delta\beta_\gamma}{\beta_\gamma} = -(\pi_{12}^{nB} - \pi_{12}^{pE})(\sigma'_{11} + \sigma'_{22}) - (\pi_{11}^{nB} - \pi_{11}^{pE})\sigma'_{33} + \left(\frac{\Delta n_{iB}^2}{n_{iB}^2} - \frac{\Delta n_{iE}^2}{n_{iE}^2}\right) \tag{3.17}$$

Transport limited current gain for an npn transistor

$$\frac{\Delta\beta_{T'}}{\beta_{T'}} = -\pi_{12}^{nB}(\sigma'_{11} + \sigma'_{22}) - \pi_{11}^{nB}\sigma'_{33} \tag{3.18}$$

For a pnp transistor it becomes

Injection limited current gain for a pnp transistor

$$\frac{\Delta\beta_\gamma}{\beta_\gamma} = -(\pi_{12}^{pB} - \pi_{12}^{nE})(\sigma'_{11} + \sigma'_{22}) - (\pi_{11}^{pB} - \pi_{11}^{nE})\sigma'_{33} + \left(\frac{\Delta n_{iB}^2}{n_{iB}^2} - \frac{\Delta n_{iE}^2}{n_{iE}^2} \right) \tag{3.19}$$

Transport limited current gain for a pnp transistor

$$\frac{\Delta\beta_{T'}}{\beta_{T'}} = -\pi_{12}^{pB}(\sigma'_{11} + \sigma'_{22}) - \pi_{11}^{pB}\sigma'_{33} \tag{3.20}$$

3.3.3 Vertical npn transistors on (111) silicon

Following similar method and using (2.27) the changes in currents and current gain for an npn transistor on (111) plane can be obtained as

$$\frac{\Delta I_C}{I_C} = \frac{\Delta I_S}{I_S} = -B_3^{nB}\left(\sigma_{11}^{'} + \sigma_{22}^{'}\right) - \left(B_1^{nB} + B_2^{nB} - B_3^{nB}\right)\sigma_{33}^{'} + \frac{\Delta n_{iB}^2}{n_{iB}^2} \tag{3.21}$$

$$\frac{\Delta I_{BE}}{I_{BE}} = -B_3^{pE}\left(\sigma_{11}^{'} + \sigma_{22}^{'}\right) - \left(B_1^{pE} + B_2^{pE} - B_3^{pE}\right)\sigma_{33}^{'} + \frac{\Delta n_{iE}^2}{n_{iE}^2} \tag{3.22}$$

$$\frac{\Delta I_{BR}}{I_{BR}} = \frac{\Delta n_{iB}^2}{n_{iB}^2} - \frac{\Delta \tau_{nB}}{\tau_{nB}} \cong \frac{\Delta n_{iB}^2}{n_{iB}^2} \tag{3.23}$$

$$\frac{\Delta\beta_\gamma}{\beta_\gamma} = -(B_3^{nB} - B_3^{pE})(\sigma'_{11} + \sigma'_{22}) - (B_1^{nb} + B_2^{nb} - B_3^{nb} - B_1^{pE} - B_2^{pE} + B_3^{pE})\sigma'_{33} + \left(\frac{\Delta n_{iB}^2}{n_{iB}^2} - \frac{\Delta n_{iE}^2}{n_{iE}^2} \right) \tag{3.24}$$

$$\frac{\Delta\beta_{T'}}{\beta_{T'}} = -B_3^{nB}\left(\sigma_{11}^{'} + \sigma_{22}^{'}\right) - \left(B_1^{nB} + B_2^{nB} - B_3^{nB}\right)\sigma_{33}^{'} \tag{3.25}$$

3.3.4 Vertical pnp transistors on (111) silicon

Interchanging the doping types the expressions for the currents and current gain for a pnp transistor on (111) plane can be obtained as

$$\frac{\Delta I_C}{I_C} = \frac{\Delta I_S}{I_S} = -B_3^{pB}\left(\sigma_{11}^{'} + \sigma_{22}^{'}\right) - \left(B_1^{pB} + B_2^{pB} - B_3^{pB}\right)\sigma_{33}^{'} + \frac{\Delta n_{iB}^2}{n_{iB}^2} \tag{3.26}$$

$$\frac{\Delta I_{BE}}{I_{BE}} = -B_3^{nE}\left(\sigma_{11}^{'} + \sigma_{22}^{'}\right) - \left(B_1^{nE} + B_2^{nE} - B_3^{nE}\right)\sigma_{33}^{'} + \frac{\Delta n_{iE}^2}{n_{iE}^2} \tag{3.27}$$

$$\frac{\Delta I_{BR}}{I_{BR}} = \frac{\Delta n_{iB}^2}{n_{iB}^2} - \frac{\Delta \tau_{pB}}{\tau_{pB}} \cong \frac{\Delta n_{iB}^2}{n_{iB}^2} \tag{3.28}$$

$$\frac{\Delta \beta_\gamma}{\beta_\gamma} = -(B_3^{pB} - B_3^{nE})(\sigma_{11}' + \sigma_{22}') - (B_1^{pb} + B_2^{pb} - B_3^{pb} - B_1^{nE} - B_2^{nE} + B_3^{nE})\sigma_{33}' + \left(\frac{\Delta n_{iB}^2}{n_{iB}^2} - \frac{\Delta n_{iE}^2}{n_{iE}^2}\right) \tag{3.29}$$

$$\frac{\Delta \beta_{T'}}{\beta_{T'}} = -B_3^{pB}\left(\sigma_{11}^{'} + \sigma_{22}^{'}\right) - \left(B_1^{pB} + B_2^{pB} - B_3^{pB}\right)\sigma_{33}^{'} \tag{3.30}$$

3.4 Characterization

Electrical characterization was performed to determine the stress-induced changes in the current-voltage characteristics of the transistors. The characteristics were measured in forward biased, it covers a current domain of several decades for bipolar transistors. For bipolar transistors, the main characteristics are determined by the saturation current.

The I-V characteristics, Gummel plots and collector and base currents for a fixed base-emitter voltage (one point at Gummel plot) for different stress levels (for both tensile and compressive) were obtained. For the I_C-V_{CE} characteristics V_{CE} was swept from 0 to 1.5 V and

I_B was stepped from 0 μA to 10μA in steps of 2 μA. For Gummel plot I_C and I_B were measured while keeping the V_{CE} constant at 1V and sweeping V_{BE} from 0 to 0.8 V.

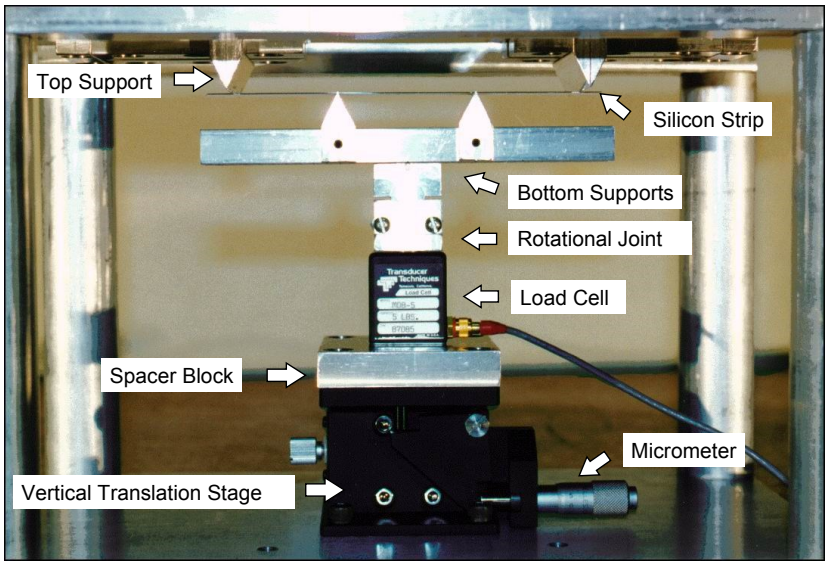
The characterization process employs a four-point-bending fixture (4PB), wafer strips containing the bipolar transistors, flexible connector, an interface box and an HP 4155 semiconductor parameter analyzer or Keithley 4200-SCS.

3.4.1 Conventional experimental set-up

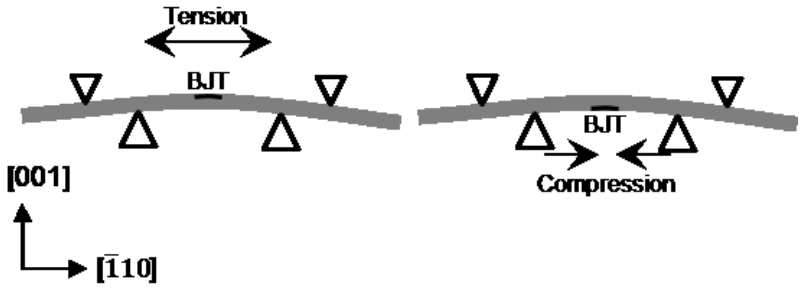
Figure 3.5(a) shows the conventional stress application arrangement consisting of a four-point-bending fixture (4PB) with load cell and probe station. In the 4PB method, a rectangular strip containing a row of chips (transistors) is cut from a wafer and is loaded in a 4PB fixture to generate a uniaxial stress state. By controlling the micrometer, uniaxial stress can be generated. For tensile stress measurements the strip side where the transistors are located faces upwards and for the compressive stress the transistor side faces downwards as shown in Figure 3.5(b). Figure 3.5(c) illustrates a 4PB geometry structure. For this set-up, uniaxial tensile state of stress is induced at the points on the top surface of the beam that are between the bottom supports is given by:

$$\sigma = \frac{3F(L-d)}{t^2 h} \tag{3.31}$$

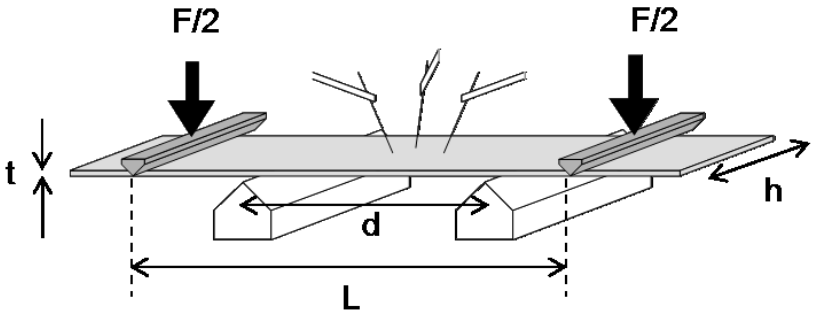
where F is the force applied to the strip on the 4PB fixture, L is the distance between the two outer points, d is the distance between the two inner supports, t is the thickness of the strip, and h is the width of the strip. The direction of the stress application is shown in Figure 3.6. The measurements were taken for uniaxial in-plane normal stress only. Due to the practical difficulties measurements were not taken for other stresses, instead simulations were used for the stress analysis in other directions.



(a)



(b)



(c)

Figure 3.5 - (a) Four-point bending fixture (b) configurations for tensile and compressive stress applications (c) four-point bending geometry

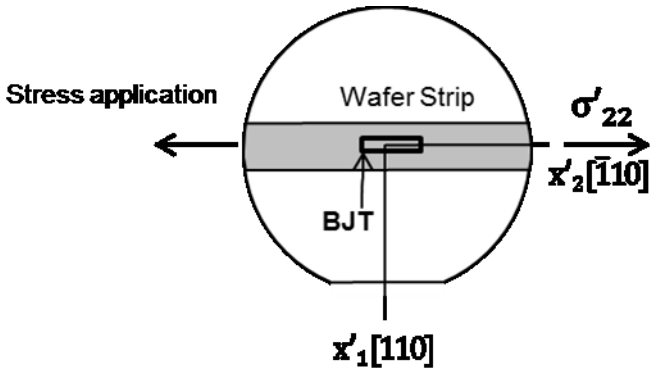


Figure 3.6 - Stress application direction

Measurement results

The load was increased from 0 – 80 MPa in steps of 20 MPa and the measurement was taken by probing. Figure 3.7 and 3.8 show the I_C-V_{CE} characteristics and the Gummel plots resulted from the measurements. During the measurements great care was taken to keep the room temperature constant. The room was kept closed and the lights were kept off to maintain the stability in measurements. Still the results were not uniform and not very accurate as shown in the enlarged plots in Figure 3.7 and 3.8.

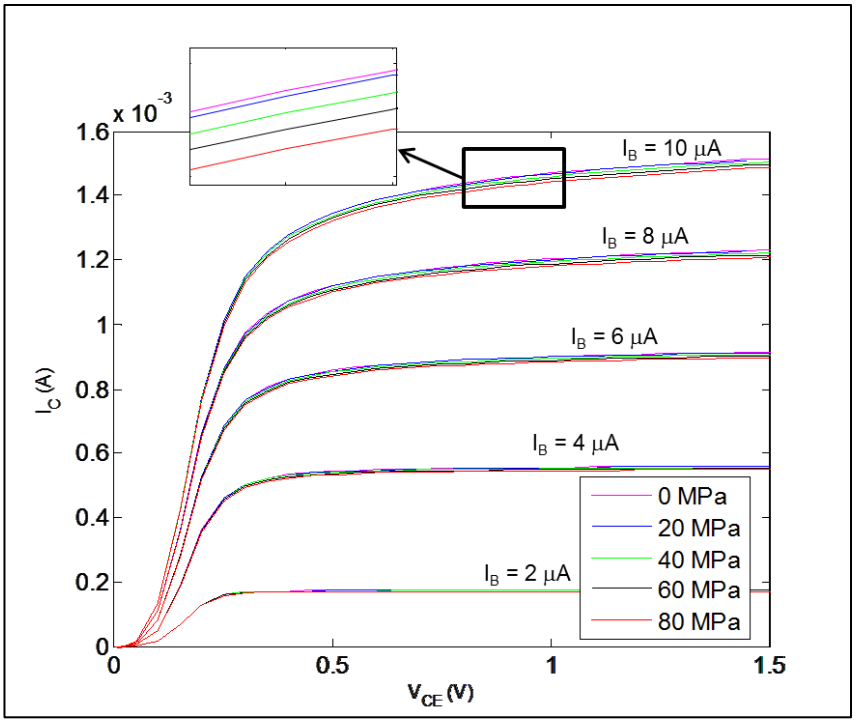


Figure 3.7 - Changes in I_C-V_{CE} Characteristics with stress $\sigma[\bar{1}10]$ for an npn BJT with probing

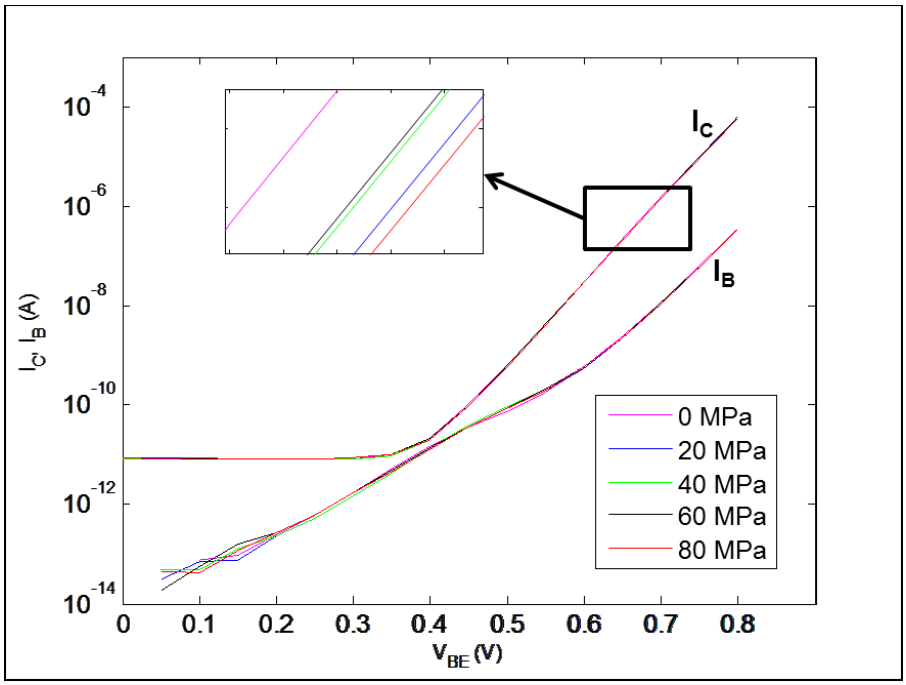


Figure 3.8 - Changes in Gummel plot with stress $\sigma[\bar{1}10]$ for an npn BJT with probing showing non-uniform changes

For dc current gain first the dc current gain was calculated from Gummel plot. Since V_{BE} is much temperature sensitive, sweeping the V_{BE} for Gummel plots affected the temperature of the device and even a small change in room temperature affected the measurements. Hence we tried fixed base-emitter voltage (V_{BE}), and fixed base current (I_B) methods as well to reduce the temperature effects. In addition, the experiments were carried out in sampling mode and the average dc current gain was obtained for 10 fixed sample base-emitter voltages for each different stress levels (Figure 3.9(a)). Similarly Figure 3.9(b) shows the average dc current gain obtained from 10 fixed sample base currents. All above methods considerably reduced the temperature effect in the measurements; however it made the probing effect more visible as shown in Figure 3.9. When making a proper contact with a probe for measurement it usually induce ≈ 10 g load on the strip. In bipolar transistor measurements we usually use a minimum of 3 probes, and all probes together induce ≈ 30 g load on the strip. It corresponds to ~ 30 MPa stress in our measurement set up. Hence probing effect has a significant influence for smaller stress levels.

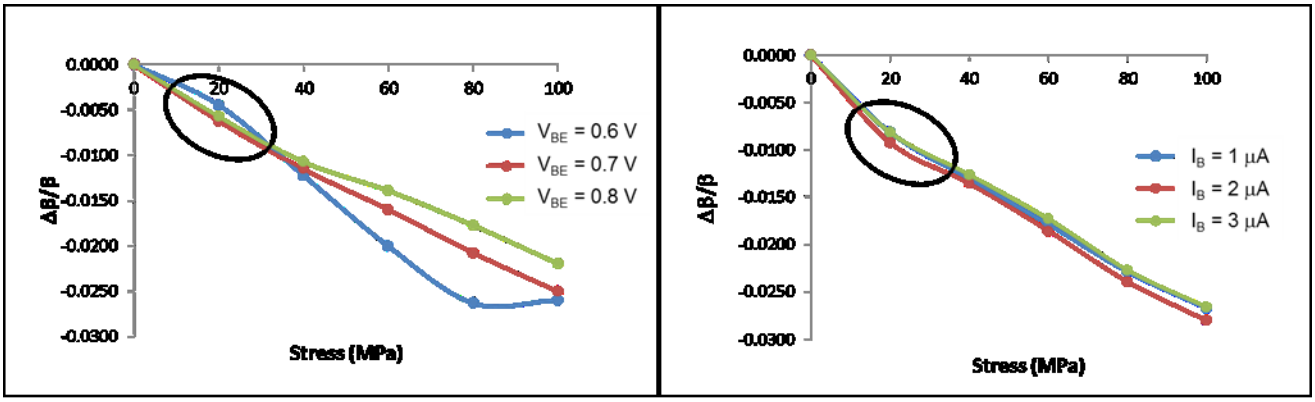


Figure 3.9 - Fractional change in dc current gain with stress $\sigma[\bar{1}10]$ for npn BJT with probing (a) using fixed V_{BE} method (b) using fixed I_B method

As explained above, in this traditional set-up the probing added additional force and gave erroneous results and unrepeatable data. In addition it took long time to set up the probes for each different stresses and get stable measurement.

3.4.2 Improvement with new flex connector

To overcome the issues with probing, a new flex connector was developed by S. Hussain as in [82] and used for the measurements (Figure 3.10 and 3.11). In this experimental set-up, the wafer strip was attached to the polyimide flexible connector at a single point at the center of the strip. Gold wirebonds were used to electrically connect the appropriate bond pads on the wafer strip to the gold plated copper traces on the flex connector. The far end of the flexible connector was configured to connect with a zero insertion force connector attached to an interface board within an interface box. Cables from the interface box were connected to the semiconductor parameter analyzer to obtain the data. With this method we were able to eliminate the additional stiffness associated with traditional manual probing or strip-on-beam method. It also helped making good permanent electrical connection and reducing the measurement time [82].

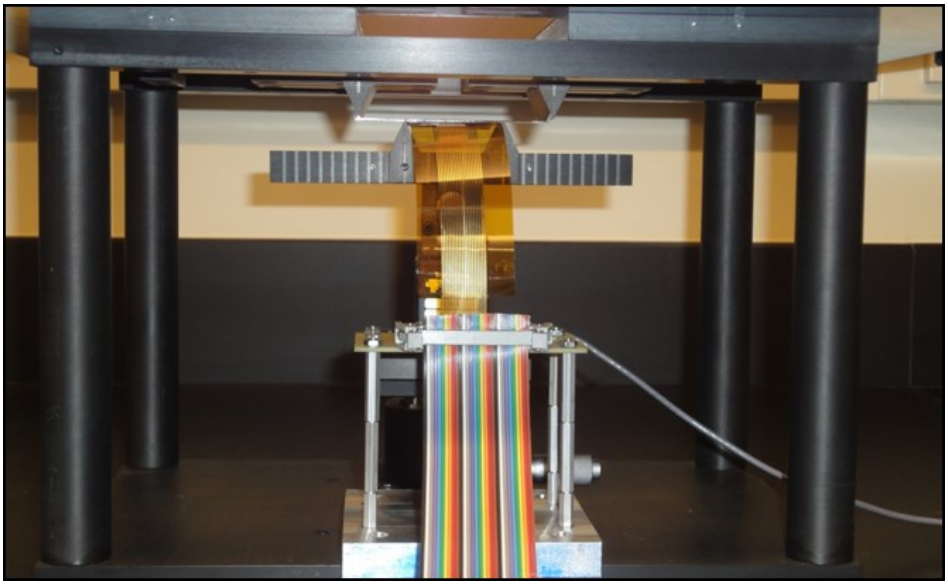


Figure 3.10 - 4 PB set up with new flex connector and a flexible carrier

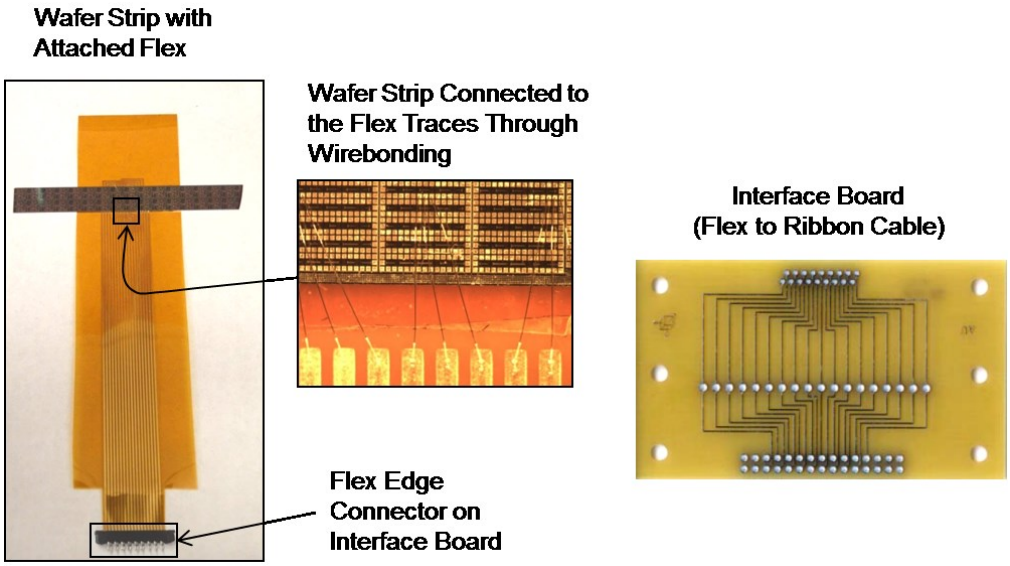


Figure 3.11 - Flex connector and interface board

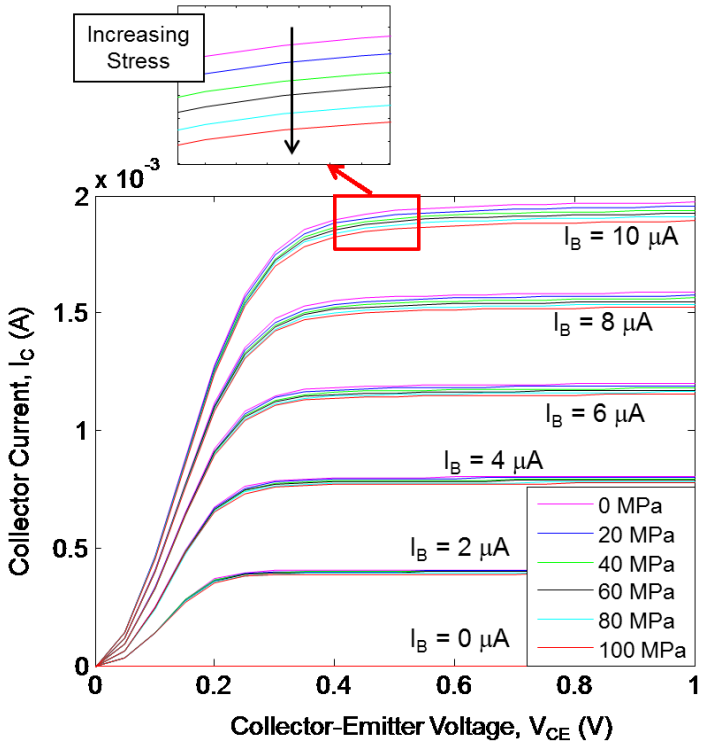


Figure 3.12 - Changes in I_C-V_{CE} Characteristics with stress $\sigma[\bar{1}10]$ for an npn BJT showing uniform changes

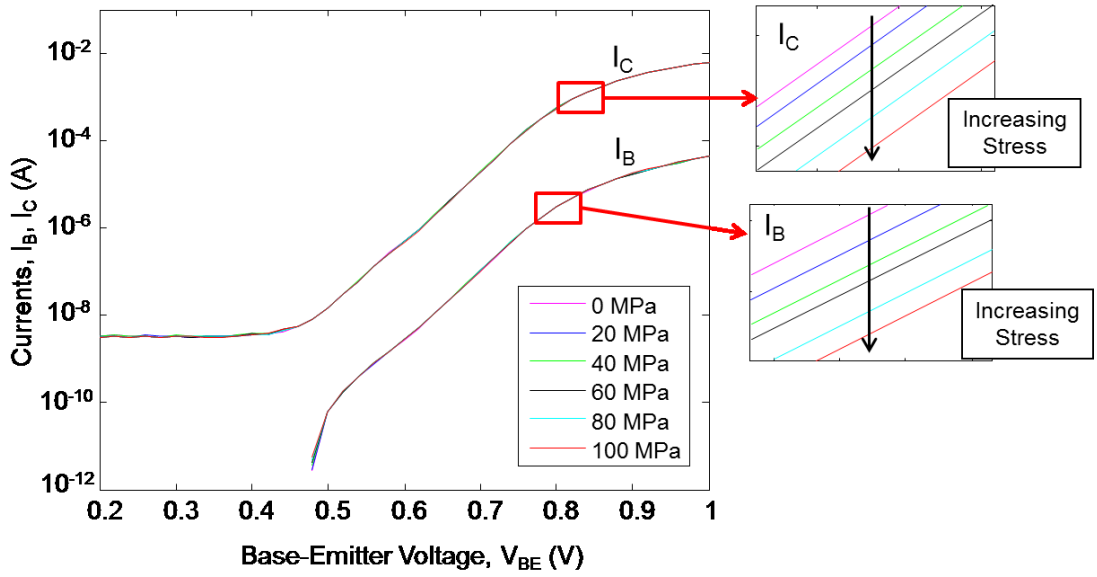


Figure 3.13 - Changes in Gummel plot with stress $\sigma[\bar{1}10]$ for an npn BJT showing uniform changes

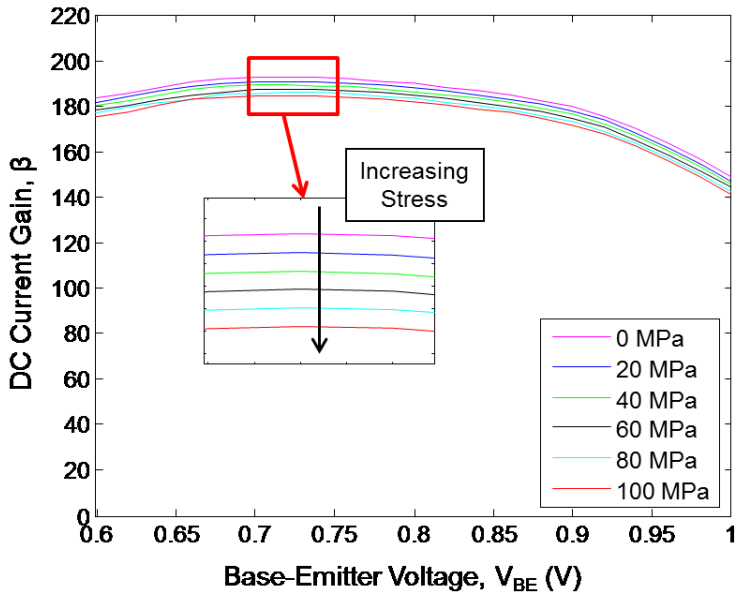


Figure 3.14 - Changes in dc current gain with stress σ[$\bar{1}$10] for an npn BJT showing uniform changes

Figure 3.12-3.14 illustrates the I_C-V_{CE} Characteristics, Gummel plots and the dc current gain plot obtained for an npn bipolar transistor employing the new flex connector. All figures show uniform changes. In I_C-V_{CE} characteristics plot the current I_C reduces with increasing tensile stress. In Gummel plot both collector and base currents reduce with increasing tensile stress, and as a result the current gain reduces (Figure 3.14). These are the typical behavior we expect for an npn transistor with tensile stress.

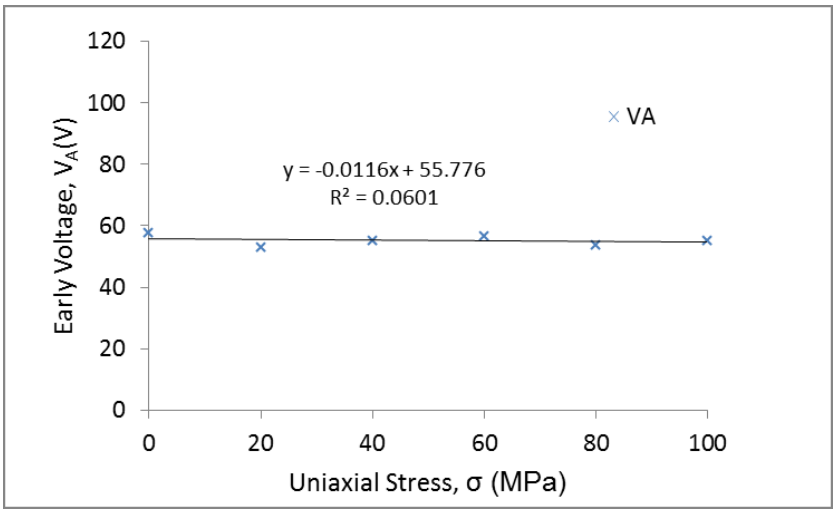


Figure 3.15 - Changes in Early voltage with stress σ[$\bar{1}$10]

Figure 3.15 of Early voltage with stress was obtained from the data in Figure 3.13 (considering for I_B = 2 – 8 μA). This transistor was having an early voltage of 55.8 V when there is no stress applied. The figure also shows that the Early voltage is lightly reduced with stress and almost independent of mechanical stress.

Figure 3.16 depicts the experimental results of fractional changes in currents and current gain for uniaxial stress σ[$\bar{1}$10] for an npn vertical transistor on (100) plane. The measurements have been obtained in the following manner. By changing the stress levels while keeping V_{BE} = 0.7 V and V_{CE} = 1 V, the base and collector currents have been obtained. The experiments were carried out in sampling mode and the average for 10 sample measurements for each different stress levels has been used. The collector and base currents reduce; as a result, the current gain also reduces. This is the typical behaviour theoretically we expect for the currents and current gain of vertical npn bipolar transistors on (100) plane.

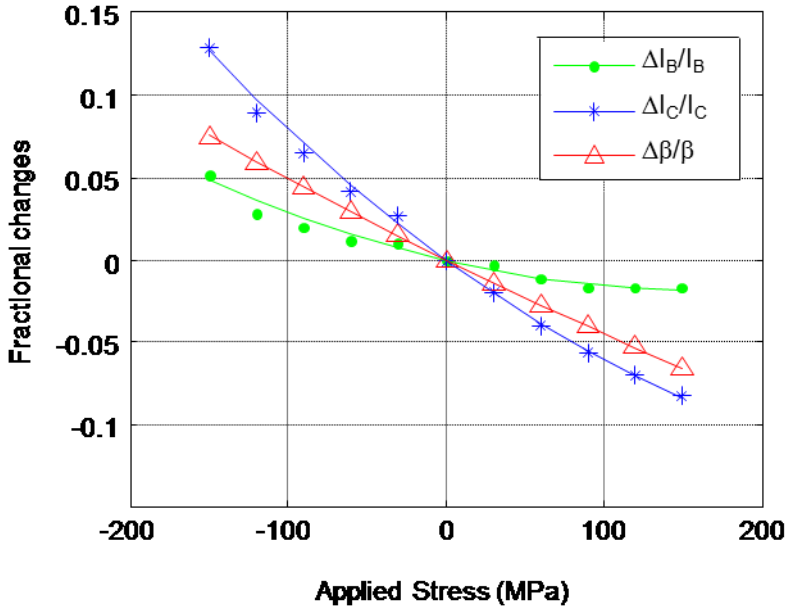


Figure 3.16 - Changes in currents and current gain with stress (npn # 1). Experimental Data provided by S. Hussain.

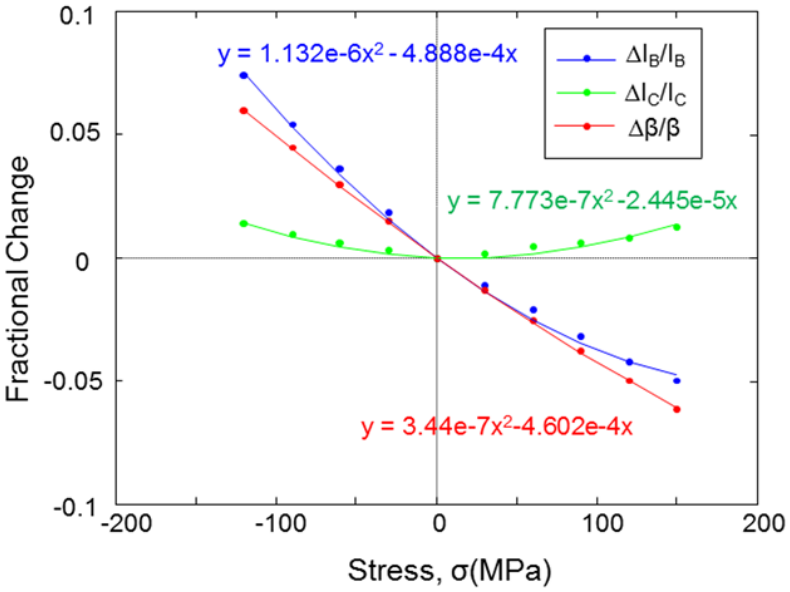


Figure 3.17 - Changes in currents and current gain with stress (npn # 2) Experimental Data provided by S. Hussain.

The fractional changes in currents and current gain of another npn transistor (npn # 2) is shown in Figure 3.17 [83]. In this case, the collector current reduces, the base current increases, and the current gain also reduces. The npn # 1 and npn # 2 transistors have same profiles and from same or similar strips. Experimental results in Figure 3.16 and 3.17 indicate equal slope for the change in dc current gain and slightly different changes for both collector and base currents (an anti-clockwise rotation about the origin in current plots). The residual stresses in the transistors have been identified as the reason for these differences and are explained in detail in chapter 4 and 5.

Various characterization techniques for stress measurement in bipolar transistors minimizing the impact of temperature variations and 1-D theoretical model including the temperature effects are available in [83].

3.5 Summary

The theoretical and the experimental work are presented in this chapter. In the theoretical work, the mechanical stress effect in saturation current is modeled as a combination of stress induced changes in the minority-carrier mobility and the stress induced changes in the intrinsic carrier concentration. 1-D theoretical models for vertical npn and pnp bipolar transistors on (100) plane and (111) plane are presented. A detailed explanation on the investigated transistor structures, experimental methods, the improvement with the flexible connector and the experimental results are also presented.

CHAPTER 4

MODELING OF STRESS EFFECT WITH SENTAURUS TCAD SIMULATOR

4.1 Introduction

Device modelling was performed for further investigation on stress effect on bipolar transistors. BJT structure development and investigation of various vertical npn and pnp bipolar structures on (100) plane is described in this chapter. Fabrication of such devices would require complex lithographic techniques and sophisticated material growth processes. As a result of this high cost and the fabrication challenges, availability of fabricated devices in different types and sizes for measurements was limited. In addition controlled stress application in different orientation for measurement is also not easy. In our measurements we were able to apply uniaxial in-plane tensile and compressive stress using a 4PB structure. There are practical difficulties for controlled stress application in any other directions. However, this device modeling and simulation study helped us to overcome those problems. Device simulation was used for stress analysis in all six stress directions.

4.2 Introduction to Sentaurus TCAD simulator

Numerical simulations have been performed by TCAD simulator Sentaurus from SYNOPSYS Ltd [59]. Sentaurus device is a multidimensional, electro-thermal, mixed-mode device and circuit simulator for 1D, 2D and 3D semiconductor devices. It includes advanced physical models and robust numeric methods for the simulation of most types of semiconductor device ranging from deep submicron devices to large bipolar power structures. It is capable of simulating the electrical, thermal, and optical characteristics of silicon and compound

semiconductor devices. A set of physical device equations that describe the carrier distribution and conduction mechanisms are used to compute terminal voltages, currents, and charges. In Sentaurus, a real semiconductor device is represented as a virtual device whose properties are discretized onto a non-uniform grid of nodes. Continuous properties such as doping profiles are represented on a mesh and, therefore, are only defined at a finite number of discrete points. Each virtual device structure is described in the Synopsys TCAD tool suite by a TDR file containing the following information [59]:

(a) The grid (or geometry) of the device contains a description of various regions, such as, boundaries, material types, locations of any electrical contacts, and the locations of all the discrete nodes and their connectivity.

(b) The data fields contain the properties of the device, such as the doping profiles, in the form of data associated with the discrete nodes.

4.3 Creating and meshing device structures

In Sentaurus device structures can be created by process simulation (Sentaurus Process), process emulation (Sentaurus Structure Editor), or structure editors (Sentaurus Structure Editor). For maximum efficiency of a simulation, a mesh must be created with a minimum number of vertices to achieve the required level of accuracy. For any given device structure, the optimal mesh varies depending on the type of simulation. For a bipolar transistor mesh should be densest in base region (high current density) and depletion regions (high electric fields). Generally, a total node count of 2000 to 4000 is reasonable for most 2D simulations. Large power devices and 3D structures require a considerably larger number of elements.

4.4 Device equations and physical models

Sentaurus device uses TDR file along with various transport equations (see chapter 5 equations 5.1-5.5) and physical models to describe the device electrical characteristics, as well as the device internal parameter variation and distributions, such as electrostatic potential, carrier densities, bandgap, carrier mobilities, carrier velocities, recombination etc. The device equations are solved self-consistently on the discrete mesh in an iterative fashion. Using 'box discretization' method Sentaurus device integrates the partial differential equations (PDEs) over a test volume, applies the Gaussian theorem, and discretizes the resulting terms to a first order approximation. The accuracy of simulation strongly depends upon the appropriate selection of physical models. In order to attain an accurate representation of stress effect in bipolar transistors a large variety of physical models have been tested. In this section the physical models that have been selected and used for the simulations in this study are presented. For details about this models refer [59].

4.4.1 Hydrodynamic transport model

Sentaurus device supports several carrier transport models for semiconductor simulations. They all can be written in the form of continuity equations, which describe charge conservation. Depending on the device under investigation and the level of accuracy required, user can select within four different transport models, the basic drift-diffusion model, thermodynamic model, hydrodynamic model and Monte Carlo model. Monte Carlo model provides more accurate results by solving Boltzmann equation for full band structure, but require high capacity servers and longer run time. Hydrodynamic model accounts for energy transport of the carriers. The bipolar transistors used in this research work are sub-micron devices. High field saturation

effects have to be accounted for such thin base bipolar devices. Hence the hydrodynamic transport model has been selected, which includes the high field saturation effect and is more suitable for devices with small active regions.

4.4.2 Recombination model

Generation–recombination exchanges carriers between the conduction band and the valence band. It plays an important role in bipolar transistors in determining the base current. Shockley–Read–Hall (SRH) recombination and Auger recombination are important for bipolar transistors.

SRH recombination

SRH recombination is the recombination through deep defect levels in the gap. The SRH recombination can be given by:

$$R_{SRH} = \frac{np - n_i^2}{\tau_n(p + p_t) + \tau_p(n + n_t)} \tag{4.1}$$

where τ_n and τ_p are electron and hole carrier lifetime, and n_t is the trap concentration at or near the center of the forbidden gap. The doping dependence of the carrier lifetimes can be modeled with the Scharfetter relation[59]:

$$\tau_{dop}(N_A + N_D) = \tau_{\min} + \frac{\tau_{\max} - \tau_{\min}}{1 + \left(\frac{N_A + N_D}{N_{ref}}\right)^{\gamma}} \tag{4.2}$$

where τ_{dop} is the doping dependence carrier lifetime for electron or hole. The standard parameter values for τ_{max},τ_{min}, N_{ref} and γ are available in Table 4.1.

Table 4.1 – SRH doping and temperature dependent parameters			
Parameter	Electrons	Holes	Unit
τ_{min}	0	0	s
τ_{max}	1×10^{-5}	3×10^{-6}	s
N_{ref}	1×10^{16}	1×10^{16}	cm^{-3}
γ	1	1	1

Auger recombination

Auger recombination is also important in high doping concentrations, as the case in emitter. In Auger recombination an electron recombines with a hole and the excess energy is transferred to another carrier as kinetic energy, which can be expressed as:

$$R_{Auger} = C_n(n^2 p - n n_i^2) + C_p(n p^2 - n_i^2 p) \tag{4.3}$$

The coefficients C_n and C_p can be given as $C_n \approx C_p \approx 1.5 \times 10^{-31}$ $cm^6 sec^{-1}$.

4.4.3 Mobility model

The mobility of electron and holes in semiconductors is influenced by different scattering mechanism. The main scattering mechanisms are lattice or photon scattering and impurity scattering. Each scattering mechanism is associated with a mobility component. If more than one mobility contributions (μ_1, μ_2,….) have to be included, they can be combined by Mathiessen's rule. The net mobility μ depends on various mobilities as

$$\frac{1}{\mu} = \frac{1}{\mu_1} + \frac{1}{\mu_2} + ... \tag{4.4}$$

and the lowest mobility dominates. In our study we assumed that the total mobility is caused by lattice scattering ($\mu_{L)}$ and impurity scattering (μ_{dop}) and the resultant mobility is given by [84]:

$$\frac{1}{\mu} = \frac{1}{\mu_{dop}} + \frac{1}{\mu_L} \tag{4.5}$$

Doping dependent mobility degradation

In doped semiconductors, scattering of the carriers by charged impurity ions leads to degradation of the carrier mobility. In our simulations the Masetti model has been used to describe the mobility dependence on the impurity concentration. The Masetti model reads:

$$\mu_{dop}(N) = \mu_{\min 1} \exp\left(-\frac{P_C}{N_{total}}\right) + \frac{\mu_{const} - \mu_{\min 2}}{1 + \left(\frac{N_{total}}{C_r}\right)^{\alpha}} - + \frac{\mu_1}{1 + \left(\frac{C_S}{N_{total}}\right)^{\beta}} \tag{4.6}$$

$$\text{where } \mu_{const} = \mu_L \left(\frac{T}{300K}\right)^{-\zeta},$$

where $N_{total} = N_A^- + N_D^+$, μ_{min1}, μ_{min2}, and μ_1 are the reference mobilities, P_c, C_r, and C_s are the reference doping concentrations, and α, β are the exponents. Sentaurus default parameters for silicon has been used for this model. These parameter values are presented in Table 4.2 [59].

Table 4.2 – Mobility model parameters at T=300 K

Symbol	Electrons	Holes	Unit
μ_{min1}	52.2	44.9	cm^2/Vs
μ_{min2}	52.2	0	cm^2/Vs
μ_1	43.4	29	cm^2/Vs
P_c	0	9.23×10^{16}	cm^{-3}
C_r	9.68×10^{16}	2.23×10^{17}	cm^{-3}
C_s	3.43×10^{20}	6.10×10^{20}	cm^{-3}
α	0.68	0.719	1
β	2	2	1

(a) High field saturation

In strong electric fields, the carrier drift velocity is no longer proportional to the electric field, rather, the velocity saturates to a finite speed. Canali model is used to model the high field saturation effect:

$$\mu(F) = \frac{\mu_{low}}{\left(1 + \left(\frac{\mu_{low} F_{hfs}}{Vsat}\right)^{\beta}\right)^{1/\beta}} \tag{4.7}$$

where μ_{low} denotes the low field mobility and the exponent β is temperature dependent according to:

$$\beta = \beta_0 \left(\frac{T}{300K}\right)^{\beta \exp} \tag{4.8}$$

Saturation velocity v_{sat} and driving field F_{hfs} are obtained from the velocity saturation model and the driving force model respectively. Model parameters are given in Table 4.3 [59]

Table 4.3 – Canali model parameters for Si at T=300 K [85]

Symbol	Electrons	Holes	Unit
β_0	1.109	1.213	1
β_{exp}	0.66	0.17	1
$\nu_{sat,0}$	1.07 x 10^7	8.37 x 10^6	cm/s
$\nu_{sat,exp}$	0.87	0.52	1

(b) Velocity saturation model

For silicon the velocity saturation model is given by:

$$v_{sat} = v_{sat,0}\left(\frac{300K}{T}\right)^{Vsat,\exp} \tag{4.9}$$

(c) Driving force model

The driving force model requires hydrodynamic simulation. The driving field for electrons is given as

$$F_{hfs,n} = \sqrt{\frac{\max(w_n - w_0, 0)}{\tau_{e,n} q \mu_n}} \tag{4.10}$$

where $w_n = 3kT_n/2$ is the average electron thermal energy, $w_0 = 3kT/2$ is the equilibrium thermal energy, and $\tau_{e,n}$ is the energy relaxation time. The driving fields for holes are analogous.

Mobility due to lattice scattering

The lattice scattering accounts only for phonon scattering and, therefore, it is dependent only on the lattice temperature as follows:

$$\mu_L(T) = \mu_L(T = 300).\left(\frac{T}{300}\right)^{-\eta} \tag{4.11}$$

where μ_L is the mobility due to bulk phonon scattering. The parameter values for μ_L and the exponent η are listed in Table 4.4.

Table 4.4 – Lattice scattering model parameters for silicon at T=300K

Parameter	Electrons	Holes	Unit
μ_L	1417	470.5	cm^2/Vs
η	2.5	2.2	1

4.4.4 Bandgap model

Band structure is the most fundamental property for a semiconductor device simulation. Realistic band structures are more complex and can be fully accounted for only in Monte Carlo simulations. But Monte Carlo simulations need high capacity servers and long time. For any general simulations we consider the most important features such as the temperature and the doping dependencies of the energy bandgap.

Temperature dependence of the energy bandgap

The energy bandgap of semiconductors decreases as the temperature increases. This can be explained as follows: When temperature increases the amplitude of the atomic vibrations increases due to the increase in thermal energy. As a result, interatomic spacing also increases and the average potential seen by the electrons in the material decreases, which in turn reduces the energy bandgap. The lattice temperature dependence of the energy bandgap can be represented as:

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta} \tag{4.12}$$

where $E_g(0)$ is the bandgap energy at 0 K, and α and β are material parameters accessible in Table 4.5. A plot of the resulting bandgap versus temperature for silicon is shown in Figure 4.1.

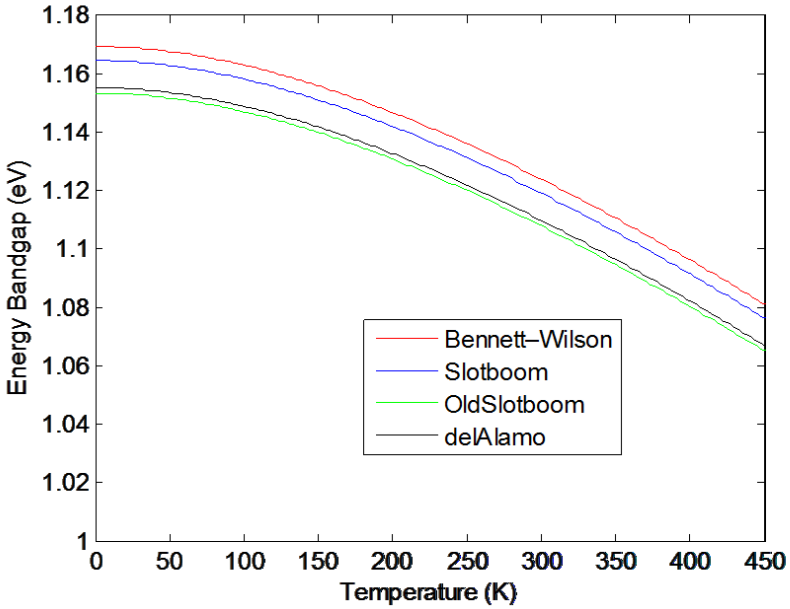


Figure 4.1 - Temperature dependence of the energy bandgap of silicon

Doping dependence of energy bandgap

Bandgap narrowing is one of the important heavy-doping effects to be considered for bipolar devices. At high doping concentrations, the density of states no longer retains a parabolic energy distribution and it becomes dependent on impurity concentrations. It causes a reduction of the bandgap due to broadening of the impurity band along with the formation of bandtails on the conduction band and the valance band. Various bandgap models such as BennettWilson, delAlamo, OldSlotboom, and Slotboom have been tested and the Slotboom bandgap model has been selected for our simulations. The details of different bandgap models and relevant parameters are available in [59]. Slotboom bandgap model [86] is widely used to represent the bandgap narrowing in silicon bipolar transistors. According to Slotboom model, bandgap narrowing is given by

$$\Delta E_g{}^0 = E_{ref}\left[\ln\left(\frac{N_{total}}{N_{ref}}\right) + \sqrt{\ln\left(\frac{N_{total}}{N_{ref}}\right)^2 + 0.5}\right] \tag{4.13}$$

where E_{ref}, N_{ref} are material parameters accessible in Table 4.5.

Accounting for bangap narrowing, the effective bandgap, $E_{g,eff}(T)$, is given as:

$$E_{g,eff}(T) = E_g(T) - \Delta E_g{}^0 \tag{4.14}$$

A plot of the change in bandgap energy with doping density is shown in Figure 4.2. As a result of bandgap narrowing, the effective intrinsic carrier density increases as expressed by

$$n_{i,eff} = n_i \exp\left[\frac{\Delta E_g{}^0}{2kT}\right] \tag{4.15}$$

where $n_{i,eff}$ is the effective intrinsic carrier density.

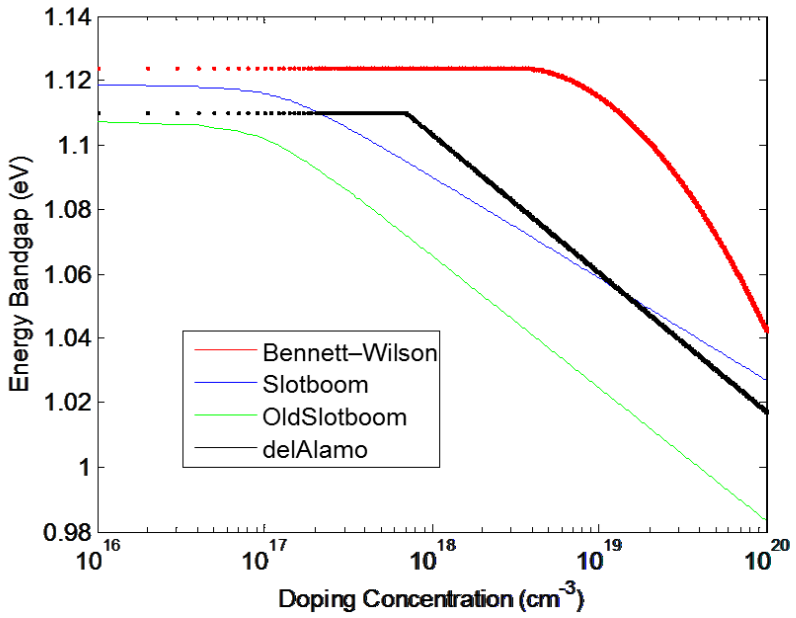


Figure 4.2 - Doping dependence of the energy bandgap of silicon

Table 4.5 – Bangap model parameters for silicon		
Parameter	Value	Unit
$E_g(0)$	1.1648	eV
α	$4.73x10^{-4}$	eV/K
β	636	K
E_{ref}	6.92	mV
N_{ref}	$1.3x10^{17}$	cm^{-3}
n_i	$1.48x10^{10}$	cm^{-3}

4.4.5 Modelling the mechanical stress effect

Mechanical distortion of semiconductor microstructures results in a change in the band structure and carrier mobility. In this work the changes in intrinsic carrier concentration and mobility are modeled separately and described in detail below (equation 3.5). The stress has been assumed constant throughout the transistor in simulations however this is not true in the real case. However considering the smaller size of the transistors this assumption was included.

Stress effects in intrinsic carrier concentration

The basic deformation potential model (default) given in Sentaurus was used to represent the stress effect in bangap/intrinsic carrier concentration. In this model, three two-fold conduction bands sub valleys for electrons and 2 valence bands sub valleys for holes (heavy-hole and light-hole bands) are considered. The shear strain effect for electrons is ignored and the shear strain effect is considered nonlinear for holes. In silicon, strain-induced change for 3 sub valleys in conduction band, and 2 sub valleys in valence bands can be given by [59]:

$$\Delta E_{B,i} = \xi_{i1}^{B2}\varepsilon'_{11} + \xi_{i2}^{B2}\varepsilon'_{22} + \xi_{i3}^{B2}\varepsilon'_{33} + \xi_{i4}^{B2}\sqrt{\frac{\left(\zeta_{i5}^{B2}\right)^2}{2}\left((\varepsilon'_{11}-\varepsilon'_{22})^2 + (\varepsilon'_{22}-\varepsilon'_{33})^2 + (\varepsilon'_{11}-\varepsilon'_{33})^2\right) + \left(\xi_{i6}^{B2}\right)^2\left(\varepsilon'_{12}{}^2 + \varepsilon'_{13}{}^2 + \varepsilon'_{23}{}^2\right)} \quad (4.16)$$

where ξ_{ij}^{B2} are deformation potentials that correspond to the Bir and Pikus model, and ξ_{i4}^{B2} is a unit less constant that defines mainly a sign. i = 1, 2, 3 are for 3 sub valleys in conduction band and i = 4, 5 are for 2 sub valleys in valence band and ε is the strain component. The constants are given in Table 4.6 [59].

Table 4.6- Deformation potential parameters

ξ_{ij}^{B2}	j=1	j=2	j=3	j=4	j=5	j=6
i=1	0.9	-8.6	-8.6	0	0	0
i=2	-8.6	0.9	-8.6	0	0	0
i=3	-8.6	-8.6	0.9	0	0	0
i=4	-2.1	-2.1	-2.1	-1	0.5	4
i=5	-2.1	-2.1	-2.1	1	0.5	4

The strain-induced conduction and valence band-edge shifts are computed using an averaged value of the individual band-edge shifts as follows [59]:

$$\frac{\Delta E_C}{kT} = -\ln\left[\frac{1}{n_C}\sum_{i=1}^{n_C}\exp\left(\frac{-\Delta E_{C,i}}{kT}\right)\right] \quad (4.17)$$

$$\frac{\Delta E_V}{kT} = \ln\left[\frac{1}{n_V}\sum_{i=1}^{n_V}\exp\left(\frac{-\Delta E_{V,i}}{kT}\right)\right] \quad (4.18)$$

where n_c=3 is the number of sub valleys considered in the conduction band and n_v=2 is the number of sub valleys considered in the valence band. Hence the stress-induced change in the bandgap is given by [59],

$$\Delta E_g(\sigma) = \Delta E_C - \Delta E_V \tag{4.19}$$

and stress induced change in intrinsic carrier concentration is given by [59],

$$n_{i,eff}(\sigma) = n_{i,eff} \exp\left[-\frac{\Delta Eg(\sigma)}{2kT}\right] \tag{4.20}$$

where $n_{i,eff}$ is the intrinsic carrier concentration (doping dependent). The change in $\Delta n_i^2/n_i^2$ calculated using the above model is plotted in Figure 4.3.

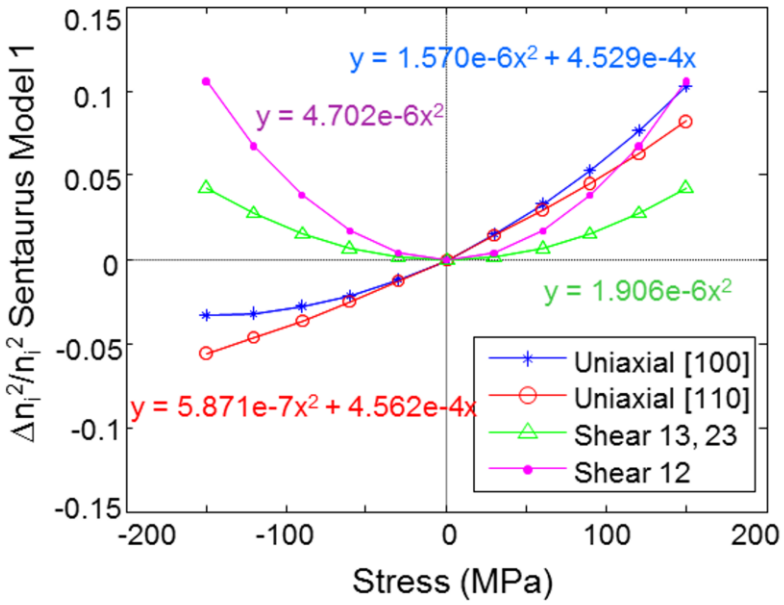


Figure 4.3 - Stress induced change in $\Delta n_i^2/n_i^2$ with stress using deformation potential model (default) in Sentaurus

Piezoresistance mobility model

We have seen in Chapter 2 that the presence of mechanical stress in device structures results in anisotropic carrier mobility that must be described by a mobility tensor. The electron and hole current densities under such conditions are given by:

$$J_\alpha = \left(\frac{\mu_\alpha}{\bar{\mu}_\alpha}\right) J_{\alpha 0}, \quad \alpha = n, p \qquad \text{and} \qquad \frac{\mu_\alpha}{\bar{\mu}_\alpha} = \left(1 + \frac{\Delta\mu_\alpha}{\bar{\mu}_\alpha}\right) \tag{4.21}$$

where $\bar{\mu}_\alpha$ is the mean average doping dependence mobility without applying any stress and $\frac{\Delta\mu_\alpha}{\bar{\mu}_\alpha}$ can be obtained by piezoresistance mobility model. In this study we used moderate stress levels < 200 MPa. For moderate stress levels stress-induced change in mobility is linear. Hence we used the first-order piezoresistance mobility model to represent the stress effect in mobility.

The complete selection of physical models used in Sentaurus simulation is given in Table 4.7.

Table 4.7 – Models selected for Sentaurus simulations

Physical effects	Model selected
Transport	Hydrodynamic transport model
Recombination	SRH (Doping dependence)
Mobility	Doping dependent mobility model
Velocity saturation	High field saturation model
Bandgap	Slotboom model
Mechanical stress effect in bandgap	Deformation potential model (default)
Mechanical stress effect in mobility	Piezoresistance mobility model (first order)

4.5 Stress simulation with 2-D bipolar transistor model

Accurate doping profile is necessary for detailed analysis of semiconductor devices. Unfortunately it is very difficult to determine the actual profile. The two most common methods of measuring doping profiles in semiconductor devices are the spreading resistance profiling (SRP) and secondary ion mass spectrometry (SIMS). Both methods have limitations on accuracy and it is important to consider them carefully while interpreting the results.

An indirect way is to approximate the doping profile by a set of analytical equations [84]. Usually Gaussian equations are used for this purpose. The parameters in these equations can be selected according to the required sheet resistance, epitaxial layer thickness, junction depths etc. It can be further tuned by comparing the electrical characterizations results of the device under test.

4.5.1 npn transistor

Simulation with default parameters in stress models in Sentaurus

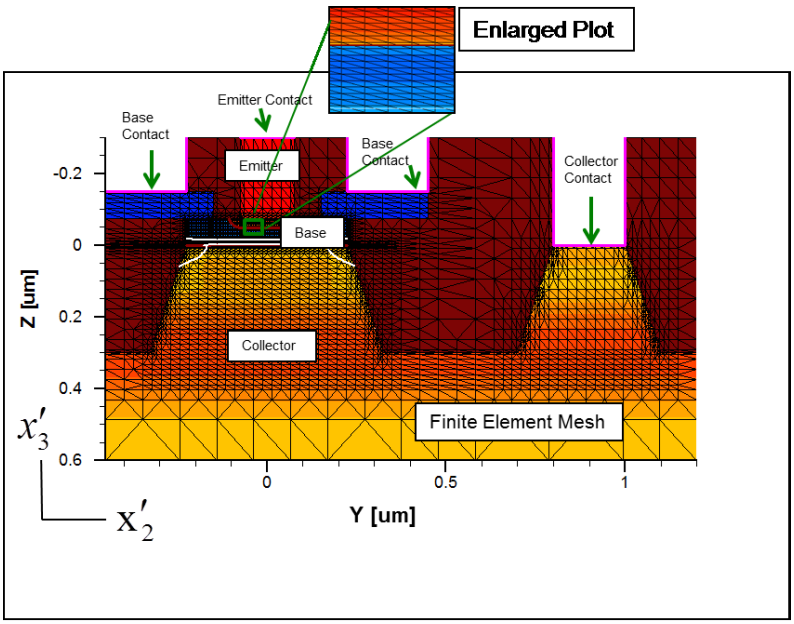


Figure 4.4 - 2-D mesh structure of a vertical npn transistor developed in Sentaurus

A typical 2-D finite element mesh created for vertical npn bipolar transistor using Sentaurus structure editor is shown in Figure 4.4. A high performance vertical npn bipolar transistor on (100) silicon, having a base width of around 75 nm and a heavily doped polysilicon emitter is considered. The doping in the emitter is constant, whereas Gaussian distributions have been assumed for the base and collector as shown in Figure 4.5. Non-uniform mesh was used to increase the efficiency of the simulation. The mesh is fine in the base and the depletion regions to improve the accuracy of the simulation.

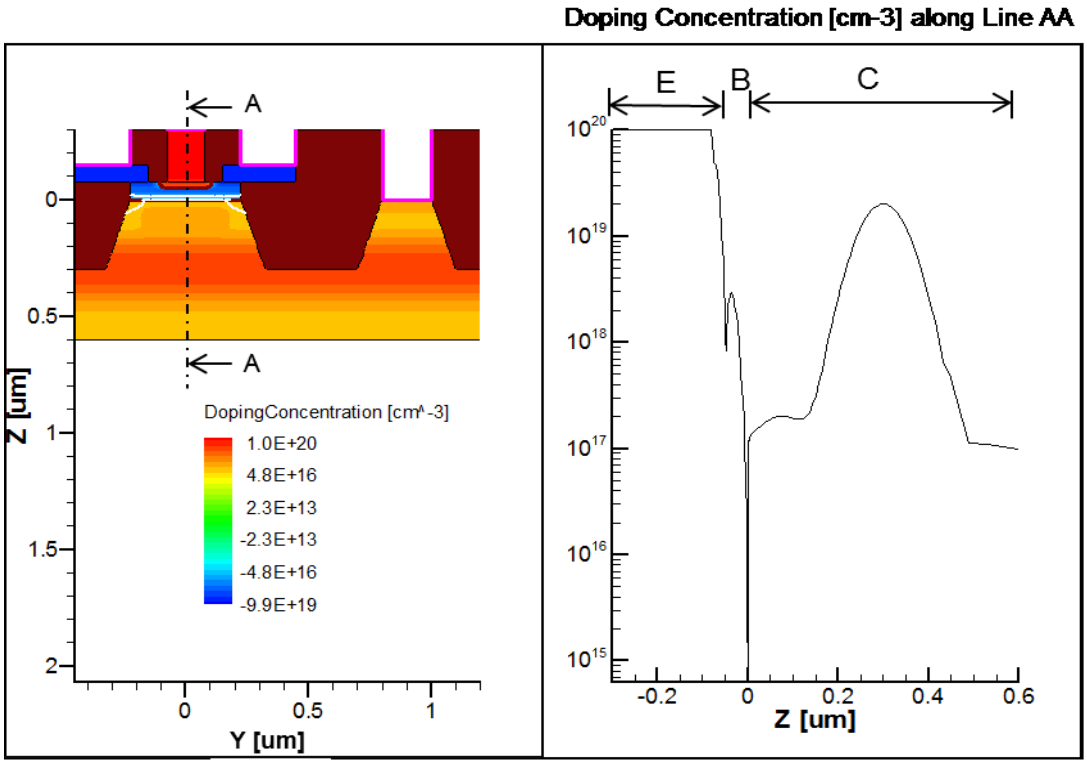


Figure 4.5 - Doping profile along the centerline

The simulations were used to predict how the carrier mobility and the bandgap thereby the intrinsic carrier concentration change with stress and influence the device performance. The piezoresistance mobility model and the deformation potential model (Sentaurus default model) are used together to represent the stress-induced changes in mobility, and the stress induced

changes in the bandgap respectively. The experimental results are used as a guide to decide the most suitable model to predict the stress effects in bipolar transistors.

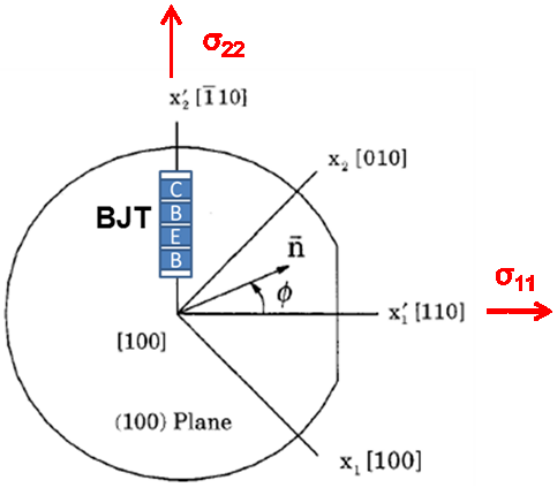


Figure 4.6 - Illustration of transistor arrangement and stress application

Stress simulation was performed for tensile stress $\sigma\,[\bar{1}10]$ for stress levels from 0-150 MPa in step of 30 MPa. Figure 4.6 shows the transistor arrangement and the stress directions. The Gummel plots and the dc current gain plots for different stress levels are shown in Figure 4.7 and 4.8 respectively. It has been observed that the collector current reduces and the base current increases with increasing stress. The simulations have been performed with the default piezoresistive coefficients in Sentaurus (Table 2.3).

Stress induced change in currents ($\Delta I_C/I_C$, $\Delta I_B/I_B$) and current gain ($\Delta\beta/\beta$) have been calculated from the plots in Figures 4.7 and 4.8 at a base-emitter voltage which gives the maximum current gain (V_{BE} =0.71 V), and plotted as in Figure 4.9. The current gain variation with stress is almost linear, similar to the experimental results in Figure 3.17. The slope of the $\Delta\beta/\beta$ vs stress curve is about -600 (1/TPa), correlates with the experimentally obtained value of -

456 (1/TPa) in Figure 3.17. In addition, the simulated collector current and base current variations are slightly nonlinear at higher stress levels, which again correlate with the experimental results shown in Figure 3.17. Qualitatively the results are in agreement with the experimental results. The accurate simulations with matching profile and estimated values of piezoresistamce coefficients are presented in the next section.

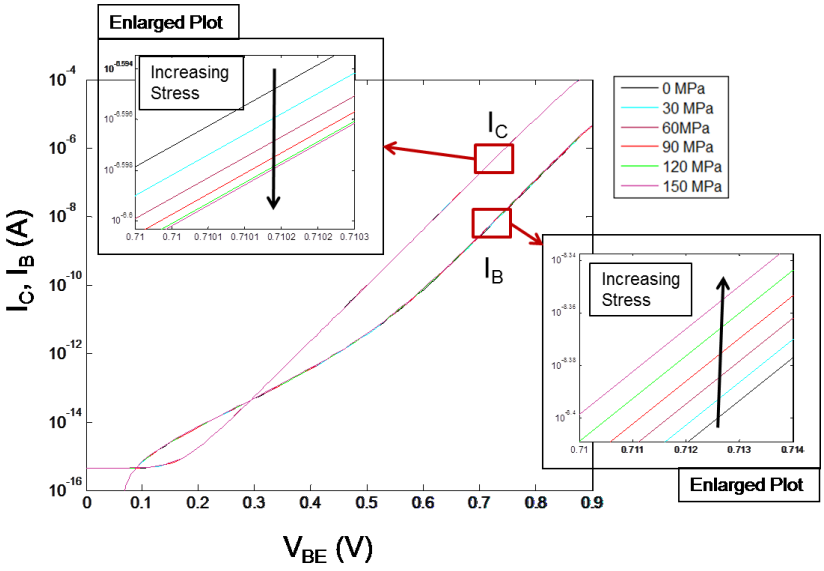


Figure 4.7 - Stress induced change in Gummel plot for an npn vertical transistor in (100) plane

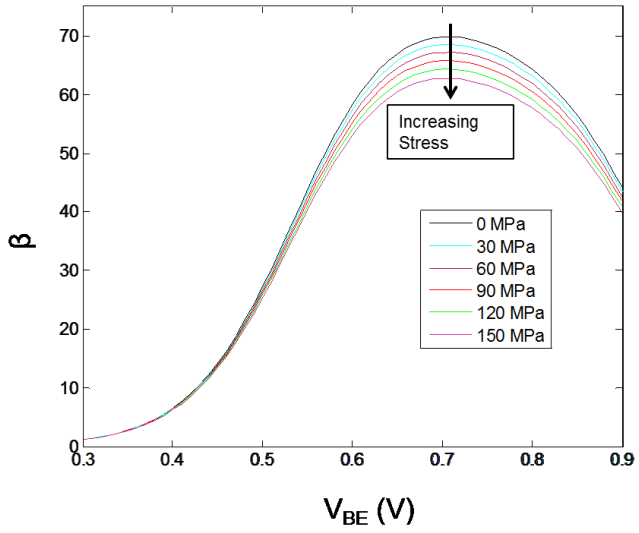
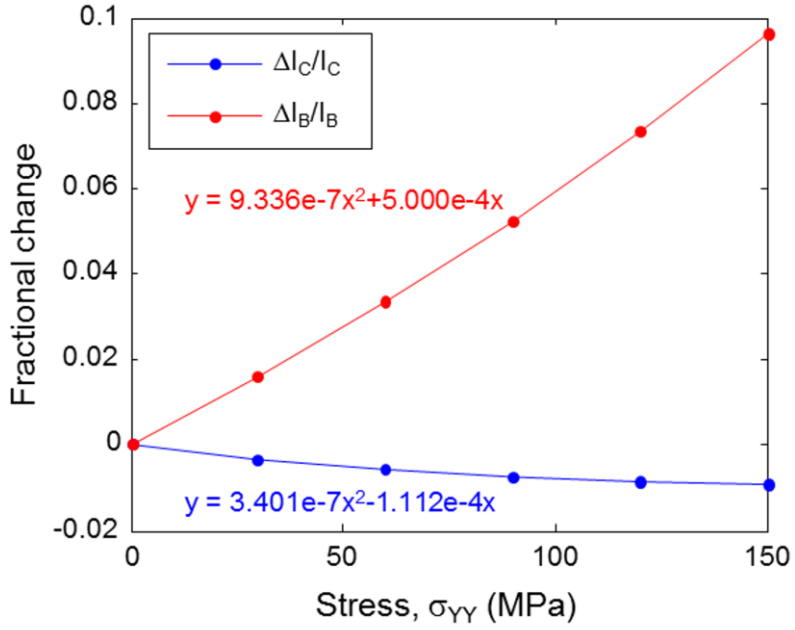
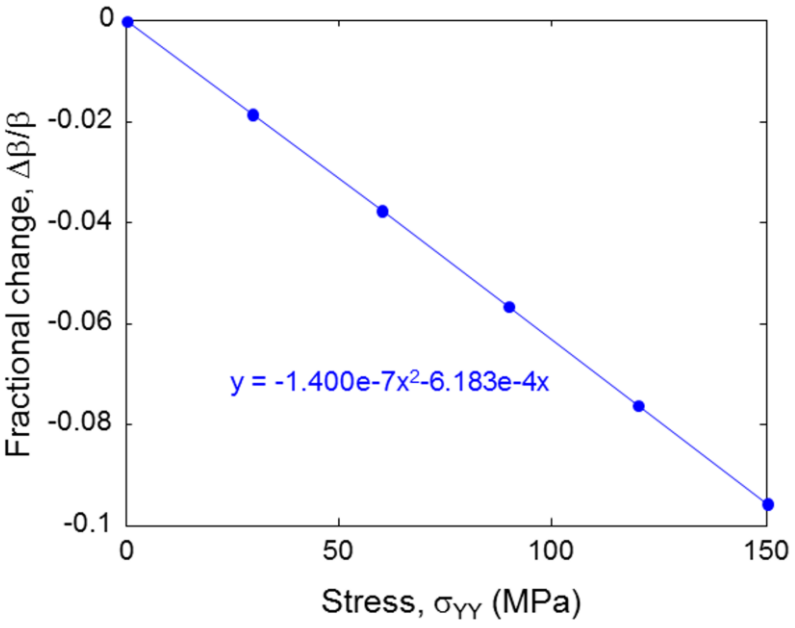


Figure 4.8 - Stress induced change in dc current gain for an npn vertical transistor in (100) plane



(a)

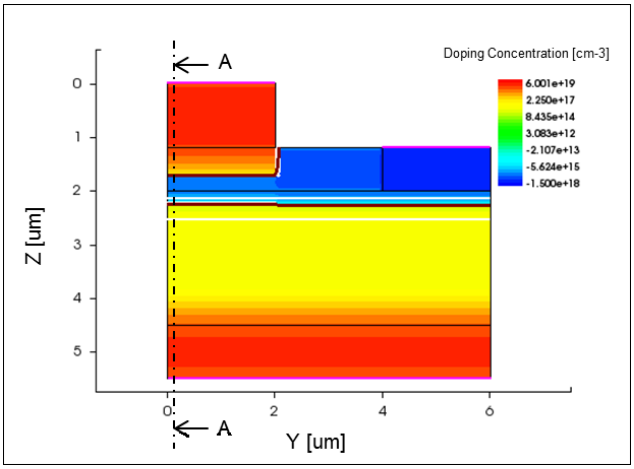


(b)

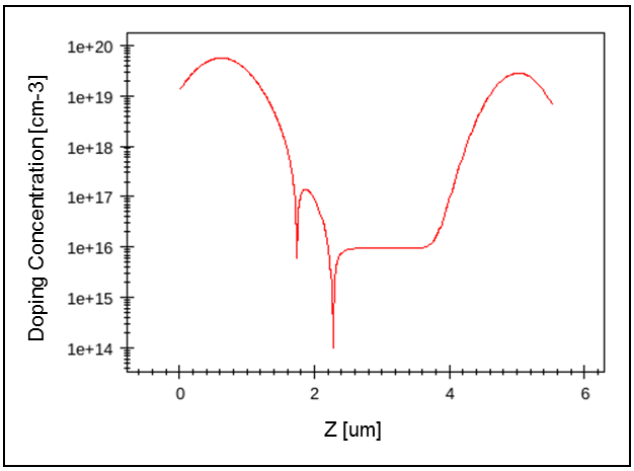
Figure 4.9 - Stress inducted changes of an npn vertical transistor in (100) plane (a) change in currents (b) change in dc current gain

Simulation with matching profile and estimated parameters

In order to further explore the stress effects on transistors, different vertical bipolar structures (different profiles, base and emitter widths, carrier lifetime etc.) were developed and simulations were carried out. The estimated piezoresistance coefficients based on the doping concentration were used for the simulations. All these simulations produced very similar results with a slope ranging from -300 (1/TPa) to -500 (1/TPa) for dc current gain depending on the transport and carrier injection effects in transistors.



(a)



(b)

Figure 4.10 - Another 2-D vertical npn transistor developed in Sentaurus (a) mesh of bipolar structure 2 (b) doping profile along AA

Figure 4.10 shows a vertical npn bipolar transistor (structure 2) with closely matching profile to the tested transistors. The current gain of this transistor is about 200 at V_{BE} = 0.71 V. Doping and temperature dependence of piezoresistance coefficients are given in [77, 79]. Considering the tested transistors are having an average base doping of $2x10^{17}$ cm^{-3} and emitter doping of $3x10^{19}$ cm^{-3}, the piezoresistance coefficients have been estimated and presented in Table 4.8. Piezoresistive coefficients for minority carriers were assumed to be equal to the piezoresistive coefficients of majority carriers [87-89].

Table 4.8 - Piezoresistive coefficient estimates for vertical BJTs on (100) and (111) planes

$N_{Bavg} = 2 \times 10^{17}/cm^3$ $N_{Eavg} = 3 \times 10^{19}/cm^3$

	npn Transistors		pnp transistors	
Coefficient	π^{nB} (x 10^{-12} Pa^{-1})	π^{pE} (x 10^{-12} Pa^{-1})	π^{nE} (x 10^{-12} Pa^{-1})	π^{pE} (x 10^{-12} Pa^{-1})
π_{11}	-900	+25	-400	+30
π_{12}	+455	-8	+200	-15
π_{44}	-150	+700	-70	+1100
B_1	-300	+358	-135	+558
B_2	+250	-119	+112	-191
B_3	+50	-230	+23	-367

Literature studies shows that there will be residual stress developing during the fabrication processes and remains in the devices [90]. Hence residual stresses also added with the applied stress in simulation to get match with the experimental results. Simulation has been performed with two different sets of models. First set consists of the piezoresistance mobility model and the deformation potential model from Sentaurus. For this set the simulation results of current curves and dc current gain showed a good match with the experimental results for a

residual stress of -310 MPa. Next set consists of the piezoresistance mobility model and the deformation potential model from Creemer and French's work (Table 2.3). The later model showed a good match with experimental results for a residual stress of +160 MPa. Figures 4.11(a), (b) and (c) show the experimental results and the matching simulation results with the above models. The current plots are very closely matching and the dc current gain plots are exactly same with both models.

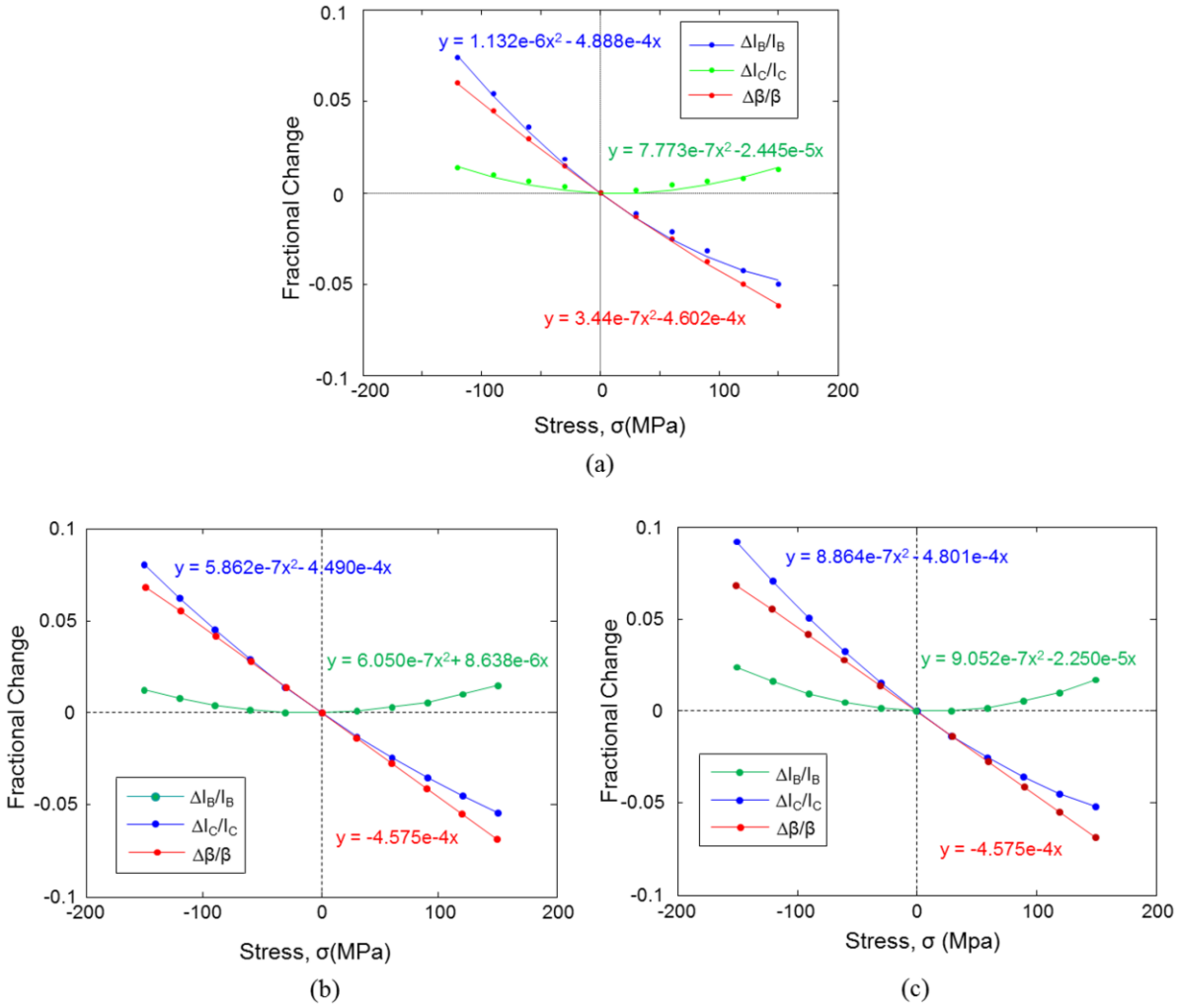


Figure 4.11- Stress induced change in currents and current gain of an npn vertical transistor to match the experimental results (a) experimental results [83] (b) simulated results with estimated piezoresistance values and deformation potential model of Sentaurus with a residual stress of -320 MPa (c) simulated results with estimated piezoresistance values and $(\Delta \mathbf{n_i^2}/\mathbf{n_i^2})$ from Creemer and French's model with a residual stress of +160 MPa.

There can be two possible reasons for these differences. One of the reasons could be that the parameters used in these two deformation potential models may be from two different experimental results with different residual stresses. The other possibility is an error in one of these models. A built-in stress of +480 MPa to the Sentaurus model gives the same results as the Creemer and French model. The original source of the parameters used in Sentaurus deformation potential model are not available. But the model we used from Creemer and French's theoretical model has been verified with their experimental results as well. In addition, our experimental results are also close to the results with this model. Hence, we selected to use the model fits from Creemer and French's research work to represent the change in intrinsic carrier concentration.

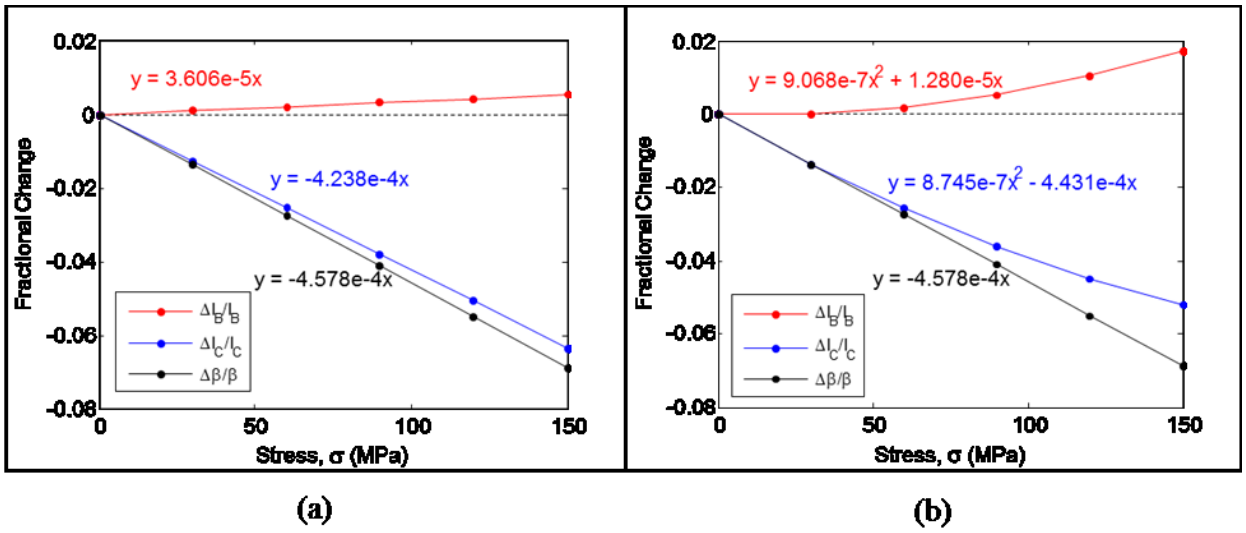


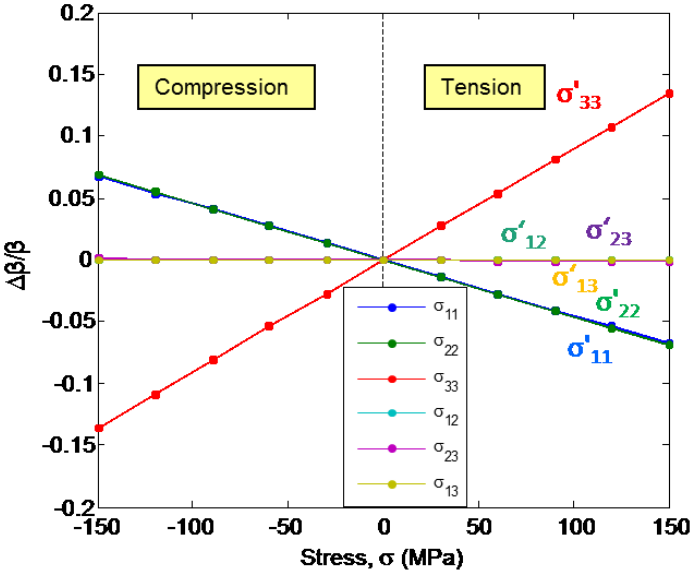
Figure 4.12 - Stress induced change in current and dc current gain for structure 2 (a) accounts for stress induced change in mobility only (b) accounts for change in mobility as well as intrinsic carrier concentration from Creemer and French's model (residual stress = +160 MPa)

In order to separately analyze the changes in characteristics due to the change in mobility and intrinsic carrier concentration the simulation has been performed with the piezoresistance mobility model only and the results were plotted [Figure 4.12 (a)] along with the original results

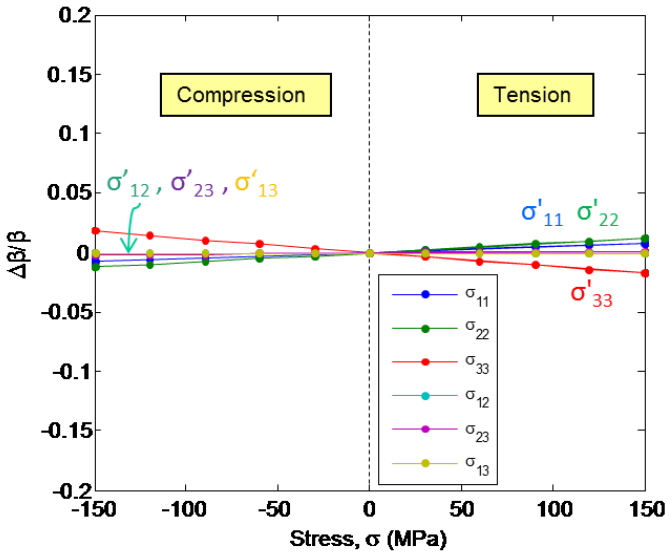
from Figure 4.11(c) which included both mobility and intrinsic carrier concentration together. It is clearly visible that the stress induced mobility changes cause a linear variation in currents and current gains, while the stress-induced bandgap changes cause a nonlinear variation of much smaller magnitude in all these parameters (for the considered stress range). For in-plane tensile stresses in npn transistors on (100) plane, change in mobility reduces the collector current (corresponding to π_{12}^{n}) and thereby reduces the dc current gain. The change in base current is much less (corresponding to π_{12}^{p}) and the change is almost by the change in the bandgap. The change in dc current gain is linear with slight nonlinearity at higher stress levels depending on the differences in compliance coefficients of the emitter and base materials. Bandgap narrowing in the emitter also may cause some differences. In this simulation same compliance values have been assumed for emitter and collector. In practical most of the high performance transistors are fabricated with polysilicon emitter. Polysilicon is an isotropic material whereas the silicon is an anisotropic material. The compliance value of the polysilicon strongly depends on the fabrication facilities and the processing steps. Hence proper compliance values have to be used for the simulations. In addition small temperature variations between the applications of stress levels also may cause variations in the collector and base currents in experiments. However equal temperature terms in base and collector currents will be cancel out in dc current gain.

In Sentaurus, the piezoresistance mobility model gives the expected changes in currents and current gain correctly. But the deformation potential model gives the results for currents shifted along the x-axis/rotated anticlockwise about the origin. However, since the changes in intrinsic carrier concentration cancels out in the dc current gain plot, it comes correct.

4.6 Stress simulation results for all 6 directions for npn and pnp transistors



(a)



(b)

Figure 4.13 – Stress induced change in dc current gain of a pnp transistor for all 6 stress components

A main advantage of simulation is that it is very easy to apply stress in any direction and get the results. Simulated dc current gain results of a vertical npn transistor along with a vertical pnp transistor for all six stress directions are shown in Figure 4.13(a) and 4.13(b) respectively. A pnp vertical mesh structure was created by changing the doping type for the same profile of npn structure (structure 2). The simulation has been performed for both tensile and compressive stresses and the results of both npn and pnp transistors have been compared. In simulations piezoresistance mobility model only included to represent the stress effects. Since the changes in currents due to the stress effects in intrinsic carrier concentration cancels out in the dc current gains, this approach is expected to give reasonably accurate results.

As depicted in Figure 4.13(a) and (b), the stress induced changes in dc current gain are totally opposite to vertical npn and pnp transistors, but sensitivity for normal stress is much less for pnp transistors depending on the corresponding piezoresistive coefficients. The effect of out-of-plane normal stress σ'_{33} is high for vertical transistors comparing to other stresses. For npn transistors, the out-of-plane normal stress σ'_{33} showed high sensitivity of about 897 (1/TPa) corresponding to π^{n}_{11}. The in-plane normal stresses σ'_{11} and σ'_{22} showed almost equal negative slope of -451 (1/TPa) and -457 (1/TPa) similar to the experimental results corresponding to π^{n}_{12}. For pnp transistors, the slope is -158 (1/TPa) for out-of-plane normal stress corresponding to π^{p}_{11}, and +52 (1/TPa) and +98 (1/TPa) corresponding to π^{p}_{12} for in-plane normal stresses. The sensitivity to shear stresses is almost zero for both pnp and npn transistors as we expected from the one dimensional theory.

However in two dimensional simulations the device equations are not solved in the 3rd direction (direction X in these simulations) and the changes in the 3rd direction are not accounted. Hence the stress analysis is not very accurate for shear stresses σ'_{12} and σ'_{13}. In addition, the

current crowding effects and other small amount of lateral current flows in the 3rd direction will not be accounted.

4.7 Stress simulation with 3-D bipolar transistor model

In order to get more accurate results for normal stresses and to simulate the shear stress effect the three dimensional model shown in Figure 4.14 has been developed. This is a thin base vertical npn transistor with a base width of 0.1 μm. The doping profile along the centerline AA is shown in Figure 4.15. The emitter doping is about $2x10^{19}$ cm^{-3} and the average base doping is about $1x10^{17}$ cm^{-3}. Only piezoresistance mobility model was included to represent the stress effects.

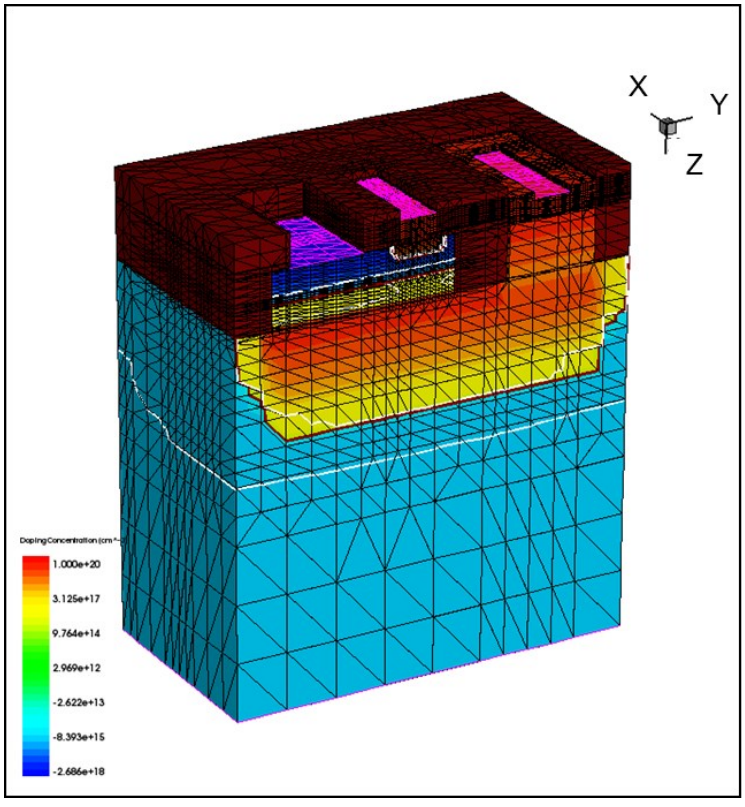


Figure 4.14 - 3-D mesh (structure 3) of a vertical npn transistor developed in Sentaurus

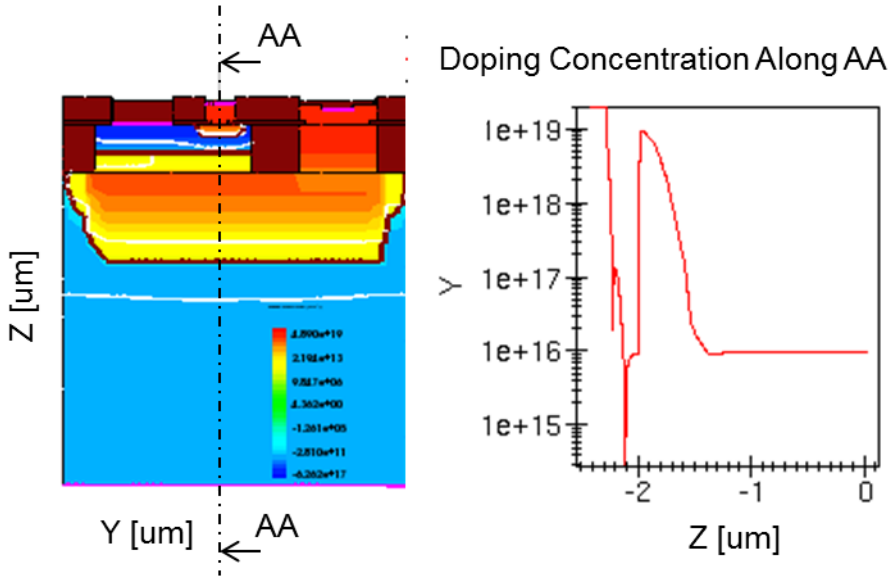
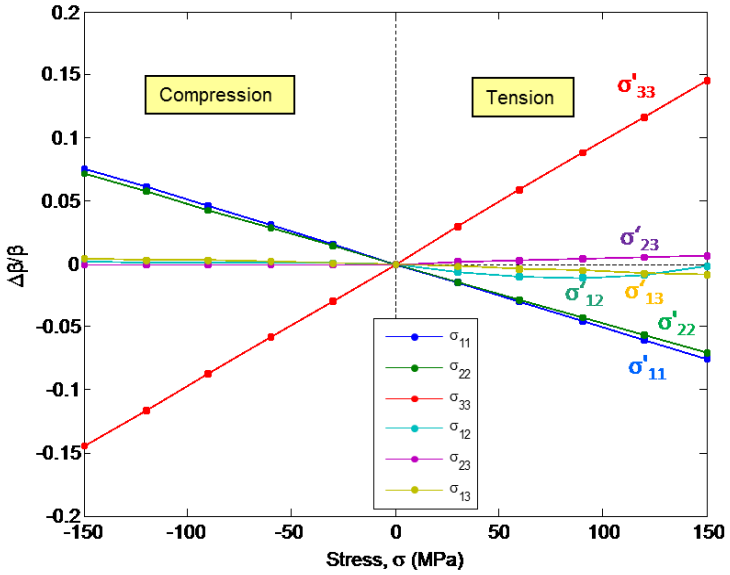
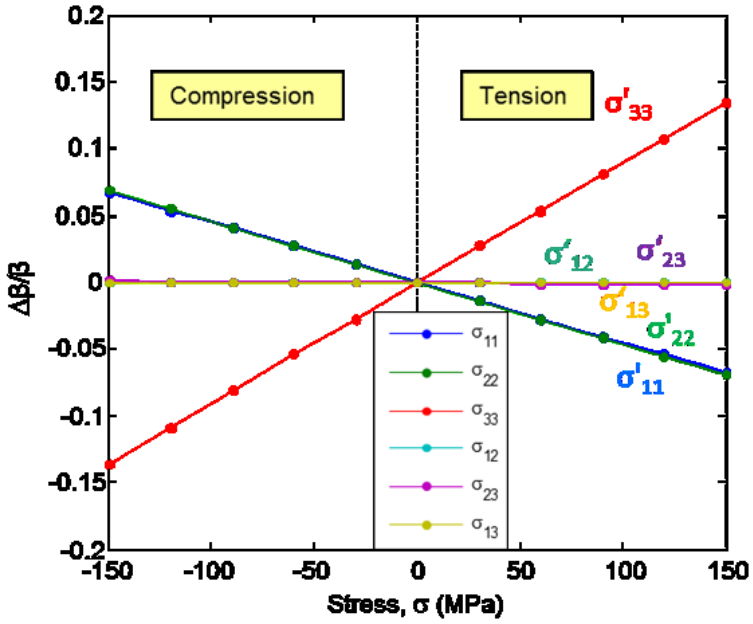


Figure 4.15 - Doping profile of 3-D model (structure 3) along AA

The changes in dc current gain for all six stress components from the 3-D and 2-D simulations are shown in Figure 4.16(a) and (b), respectively. The results are comparable to the results from 2-D simulations. The out-of-plane normal stress σ'_{33} showed high sensitivity of about 974 (1/TPa) and the in-plane normal stresses σ'_{11} and σ'_{22} showed almost equal negative slope of -474 (1/TPa) and -504 (1/TPa). This 3-D model is more injection limited structure with a thin base compared to the 2-D structure we used for the simulations. Hence the slopes of the normal stress plots for this 3-D structure are higher than the results from the 2-D structure as we expected from the theory. In 3-D simulations the shear stresses are also showing some sensitivity for positive shear stresses. This appeared to be due to the current components in other than the normal direction to the wafer surface due to the current crowding effects.



(a)



(b)

Figure 4.16 - Stress induced change in dc current gain of an npn transistor for all 6 stress components (a) with 3-D model (b) with 2-D model

Since this is a vertical bipolar transistor, theoretically we expect the stress sensitivity to σ'_{11} and σ'_{22} to be the same and the sensitivity to σ'_{13} and σ'_{23} to be the same. But there are differences observed in simulation results. These are also due to the slight changes in current distribution directions due to the current crowding effects. The current crowding caused by the lateral voltage drop in the base region has been verified for 2-D and 3-D simulations using Spice simulations (Appendix B).

4.8 Summary

Sentaurus 2-D and 3-D models were developed for stress analysis in vertical bipolar transistors. Simulation results were compared with experimental results. Stress effects were modeled as a combination of piezoresistance mobility model and a deformation potential model. In Sentaurus, the piezoresistance mobility model gives the expected linear changes in currents and current gain correctly. But the deformation potential model gives the results for currents shifted along the x-axis (or rotated anticlockwise about the origin). However, since the changes in intrinsic carrier concentration cancels out in the dc current gain plot, the dc current gain plot comes correct. The changes in dc current gain was obtained for all 6 directions from 2-D and 3-D simulations and compared. The results are comparable. For each stress levels, while 2-D simulation took tens of minutes (depending on the size), 3-D simulations took hours. For high level of accuracy a 3-D analysis is necessary. However 2-D analysis gave reasonably good and comparable results in much lesser time. Since BJTs are highly one dimensional it is possible to get accurate results close to 2-D and 3-D simulations with a 1-D model as well. In order to facilitate fast stress analysis in bipolar transistors a 1-D numerical model was developed and explained in the next chapter.

CHAPTER 5

1-D NUMERICAL MODELLING FOR RAPID STRESS ANALYSIS IN BIPOLAR TRANSISTORS

5.1 Introduction

In this chapter, the development of a new 1-D numerical bipolar transistor model, validating the model and some application of the model for stress analysis are described. Model was developed in Matlab.

Numerical modeling is used as a powerful tool to solve challenging engineering problems in semiconductor devices [91-93] and various new approaches are investigated to speed up the numerical process since high accuracy within a reasonable run time is highly desired [94]. In the case of mechanical stress analysis, numerical modeling and simulation avoid a multitude of practical challenges associated with fabrication, complex lithographic and material growth processes, and application of controlled stress in different orientations for measurement. Modeling may vary depending on the type of semiconductor devices. Since MOSFETs are 2-D/3-D devices either 2-D or 3-D numerical simulation is required for stress analysis. Several commercial TCAD tools such as Sentaurus and Victory are available to analyze the stress effects of semiconductor devices with 2-D or 3-D simulations. However these TCAD tools require high capacity servers to run and the stress simulation process may take hours if high accuracy is required. Since BJTs are highly 1-D devices, a 1-D model can provide comparable results in a very short time and make device analyses much easier. In this work we present a simple and fast 1-D numerical algorithm for stress analysis in BJTs. This algorithm is capable of solving device equations efficiently and accurately and thereby optimizes the run time.

In the commonly used 1-D simulators 5 differential highly nonlinear equations (Poisson equation, transport equations and continuity equations) have to be solved simultaneously for each node [95, 96]. In order to obtain high accuracy in a 1-D model over $N = 1000$ nodes are needed. Therefore, over 5000 highly coupled nonlinear equations have to be solved. With traditional approach these equations are linearized and solved iteratively [96]. Despite the sparsity of these equations, solution of over 5000 equations is very time consuming. In our approach such complex processing is avoided. Each of the five equations is solved independently and analytical solutions are used to make the process even faster. In this model, first we numerically solve the Poisson equation at the junctions to find the depletion regions, electric field, and the electrostatic potential in the depletion regions. Then we iteratively solve the transport equations in the quasi-neutral regions. A new integrated approach is presented to solve the transport equation efficiently. Further reduction in run time was obtained by using a fractional starting point at the junctions when solving the Poisson equation. Furthermore, the transport equations are iteratively solved in the quasi-neutral region for the particular minority-carrier type only. All the above approaches considerably reduce the CPU runtime in our model.

The 1-D simulation results of this model were compared with 2-D simulation results of Sentaurus TCAD tool. This assessment revealed that this 1-D model is much faster and yields comparable results. Then stress models were included in the 1-D BJT model and the validity of the model was verified with experimental results and theoretical expectations for npn and pnp vertical transistors on the (100) plane. Some applications of this model are also illustrated with appropriate parameter selections. Such applications includes predicting the stress induced changes in the saturation current of npn/pnp vertical and lateral bipolar transistors on (100) plane

for various stress orientations, quantifying the residual stress in bipolar transistors and analyzing the stress effects in npn BJTs on (111) plane.

5.2 Device equations

The five basic differential equations describing semiconductor device behavior as a function of doping concentrations, carrier parameters, and applied voltages are as follows [97].

Poisson's Equation
$$\frac{d^2\varphi}{dx^2} = -\frac{q}{\varepsilon}(N_D - N_A + p - n) \tag{5.1}$$

where φ is the electrostatic potential (EP), x is the distance, q is the electric charge, ε is the permittivity of the semiconductor, N_A, N_D are the concentration of acceptors and donors, and p, n are the concentration of holes and electrons respectively.

Continuity equation for electrons
$$\frac{dn}{dt} = \frac{1}{q}\frac{dJ_n}{dx} - R \tag{5.2}$$

Continuity equation for holes
$$\frac{dp}{dt} = -\frac{1}{q}\frac{dJ_p}{dx} - R \tag{5.3}$$

where t is the time, and R is the generation-recombination rate and the electron and hole current densities J_n, J_p are given by the following transport equations:

$$J_n = qD_n\frac{dn}{dx} - q\mu_n n\frac{d\varphi}{dx} \tag{5.4}$$

$$J_p = -qD_p\frac{dp}{dx} - q\mu_p p\frac{d\varphi}{dx} \tag{5.5}$$

where D_n and D_p are electron and hole diffusion constants, and μ_n, μ_p are electron and hole mobilities. The electron and hole concentrations are related to φ, the electrostatic potential (EP) and φ_n, and φ_p, the electron and hole quasi-Fermi potentials (EQFP, HQFP) as follows:

$$n = n_i \exp\left(q \frac{(\varphi - \varphi_n)}{kT} \right) \tag{5.6}$$

$$p = n_i \exp\left(q \frac{(\varphi_p - \varphi)}{kT} \right) \tag{5.7}$$

where k is the Boltzmann constant, T is the temperature, and n_i is the intrinsic carrier concentration. The above two equations represents the Boltzmann approximation to Fermi statics and can be taken as the definitions of the quasi-Fermi potentials. They are valid only as long as $(\varphi_p-\varphi)$ and $(\varphi-\varphi_n)$ do not approach half the bandgap.

5.3 Modeling of an npn transistor with MATLAB

The known quantities in these equations are the concentration of acceptors and donors (N_A, N_D), electron and hole mobilities (μ_n, μ_p), electron and hole diffusion constants (D_n, D_p), electron and hole carrier lifetimes (τ_n,τ_p), and applied emitter and collector voltages (V_{EB}, V_{CB}). The parameters n_t, τ_p and τ_n strongly depend on the processing and vary throughout the device. In this work, the trap concentration in the forbidden gap (n_t) is assumed equal to the intrinsic carrier concentration (n_i) and estimated values based on the doping concentration are used for lifetimes. The five unknown quantities in the equations are the carrier concentrations (n, p), the current densities (J_n, J_p), and the electrostatic potential (φ). All are functions of position (x) and doping profiles as well as applied voltages.

In this proposed model the computation can be further accelerated using the following assumptions:

1) Normal-mode transistor operation was assumed, i.e: the base-emitter (BE) junction is forward-biased and base-collector (BC) junction is reverse-biased.

2) In order to be able to use an iterative process, it was assumed that the minority carrier current in the base is almost constant so that the current change can be computed as a correction.

The next step is to develop the numerical model, which can accurately predict the unknown quantities. This will be done at discrete points in the one-dimensional model of the semiconductor. The discretization is made using standard finite-difference techniques. The entire 1-D BJT is divided into N (N = 1500) equal sections where i is the node number, the emitter contact is at i = 0 and the collector contact is at i = N.

5.3.1 Initialization

Doping concentration, effective intrinsic carrier concentration, Fermi potential, junction locations and equilibrium carrier concentrations are computed in this step. The acceptor and donor concentrations were obtained from Sentaurus since we wanted to compare the simulation results of 1-D model with the Sentaurus 2-D model for the same profiles (Figure 5.1). Obviously, the acceptor and donor concentrations could also be obtained from analytical expressions [84] (see APPENDIX A). The net effective doping concentration (or normalized charge where the normalized quantity is the electric charge q) for the entire region, Q_N, was calculated as $Q_N = N_D - N_A$.

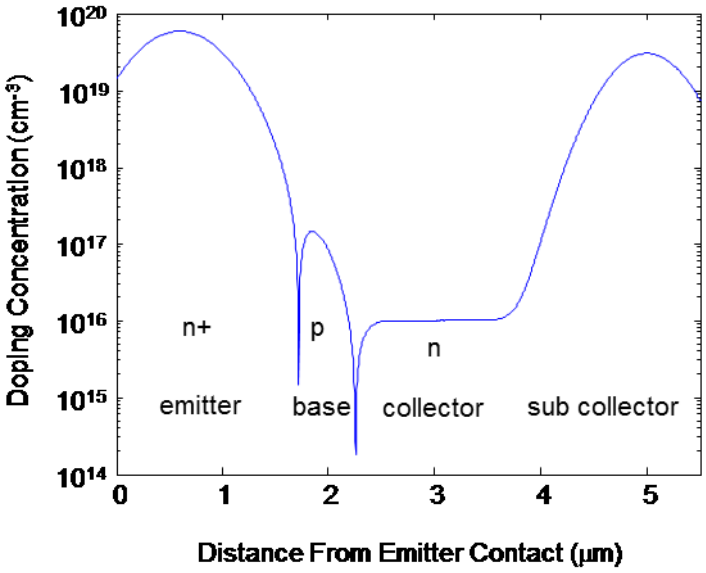


Figure 5.1 - Doping profile of an npn transistor

At high doping concentrations, such as in the case of an emitter, bandgap narrowing and the resultant increase in intrinsic carrier concentration cannot be neglected. According to the widely used Slotboom bandgap model [86], the bandgap narrowing (ΔE_g^0) is given by:

$$\Delta E_g{}^0(N) = E_{ref}\left[\ln\left(\frac{N_{total}}{N_{ref}}\right) + \sqrt{\ln\left(\frac{N_{total}}{N_{ref}}\right)^2 + 0.5}\right] \tag{5.8}$$

where $N_{total} = N_A^- + N_D^+$, E_{ref} = 6.92 mV and N_{ref} = 1.3x10^{17} cm^{-3}. Hence the effective intrinsic carrier concentration, n_i, is given by:

$$n_i = n_{i0}\exp\left[\frac{\Delta E_g{}^0(N)}{2kT}\right] \tag{5.9}$$

where n_{i0}=1.48x10^{10} cm^{-3}, is the intrinsic carrier concentration at 300 K.

The Fermi-potential (V_f) was calculated as:

$$V_f(i) = s(i)\, V_T \ln\left(\frac{|Q_N(i)|}{n_i(i)}\right) \tag{5.10}$$

where V_T = kT/q, is the thermal voltage and s is the sign of the net effective doping concentration. The Fermi potential for the entire region is shown in Figure 5.2.

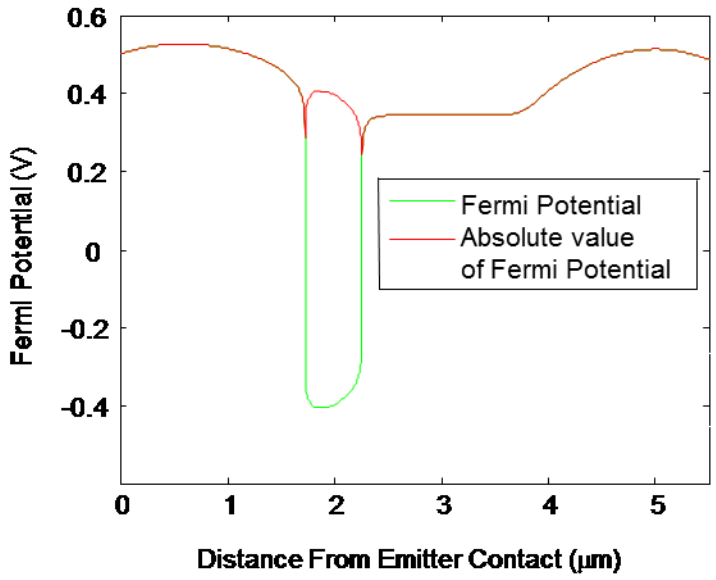


Figure 5.2- Fermi potential of an npn transistor

The built-in potential between a p-n junction can be given by [97]:

$$\varphi_{bi} = V_T \log\left|\frac{Q_N(A)Q_N(B)}{n_i(A)n_i(B)}\right| \tag{5.11}$$

where A and B are two points in p and n type regions, respectively.

For an npn transistor the net charges in the emitter and the collector are positive, and the net charge in the base is negative. Hence the points at which the sign of the charge changes represent the junctions. Based on this, the metallurgical junctions i_{jBE} and i_{jBC} are calculated, where i_{jBE} is the BE junction and i_{jBC} is the BC junction (Figure 5.3).

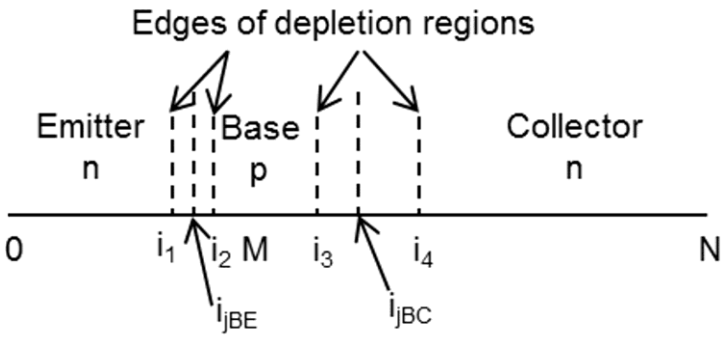


Figure 5.3 - 1-D representation of a BJT illustrating terms and symbols. i_{jBE}, i_{jBC} - metallurgical junctions; i_4, i_3 - start, end points of BC depletion region calculations (used in Figure 5.4, 5.5); i_2, i_1 - start, end points of BE depletion region calculations; i_3, i_2 - start, end points for base transport calculations (used in Figure 5.12).

The equilibrium carrier concentrations for the emitter and collector, where electrons are the majority carriers, are calculated as [97]:

$$n_0 = \frac{\sqrt{Q_N^2 + 4n_i^2} + Q_N}{2}, \qquad p_0 = \frac{n_i^2}{n_0} \tag{5.12}$$

where n_0 and p_0 are the equilibrium electron and hole concentrations respectively. For the base, holes are the majority carriers and the calculations of carrier concentrations are analogous.

5.3.2 Solving Poisson equation for base-collector and base-emitter junctions

Integrating the Poisson equation provides the following equations for electric field and electrostatic potential:

Electric field $$E = \frac{q}{\varepsilon}\int Q_N dx \tag{5.13}$$

Electrostatic potential $$\varphi = -\int E\, dx \tag{5.14}$$

where dx is the distance between adjacent nodes. By iteratively solving Poisson's equation for the BE and BC junctions, the depletion-region edges, electrostatic potential distribution and electric field in the depletion region were calculated.

Traditional numerical solution of Poisson's equation increases computation time as it requires many small sections and iterations for accurate results. Here we have reduced number of sections below 400 ($1/4^{th}$ of the original) and number of iterations below 10 by using fractional sections on junction edges. This way we obtained high accuracy with short time. Further reduction in computation time was also found to be possible by using the analytical model described below to find the initial charge distribution. In the case of the BC junction, the step model was assumed, whereas for the BE junction the linear model was assumed.

For the BC junction, the initial value for the depletion-region starting at a point in the collector was calculated using the following equation [97].

$$w = \sqrt{\frac{2\varepsilon\left(V_{CB} + \varphi_{bi}\right)}{qN_{Col}}} \tag{5.15}$$

where φ_{bi} is the built-in potential and N_{Col} is the collector doping concentration. The depletion width (w) varies as the square root of the total electrostatic potential difference across the junction. Figure 5.4 presents pseudocode describing the method of solving the Poisson equation in detail. Figure 5.5 is used to explain the accurate starting point calculations (lines 3-6 in Figure 5.5(b)), where i_{4f} is the fractional starting point, i_4 is the whole number and δ_1 is the decimal part. In Figure 5.5(b), lines 13 and 14 explain the accurate end point calculations. The changes in potential distribution and the electric field with iteration for the BC junction are shown in Figure 5.6. The solutions with required accuracy were obtained in about 5 iterations.

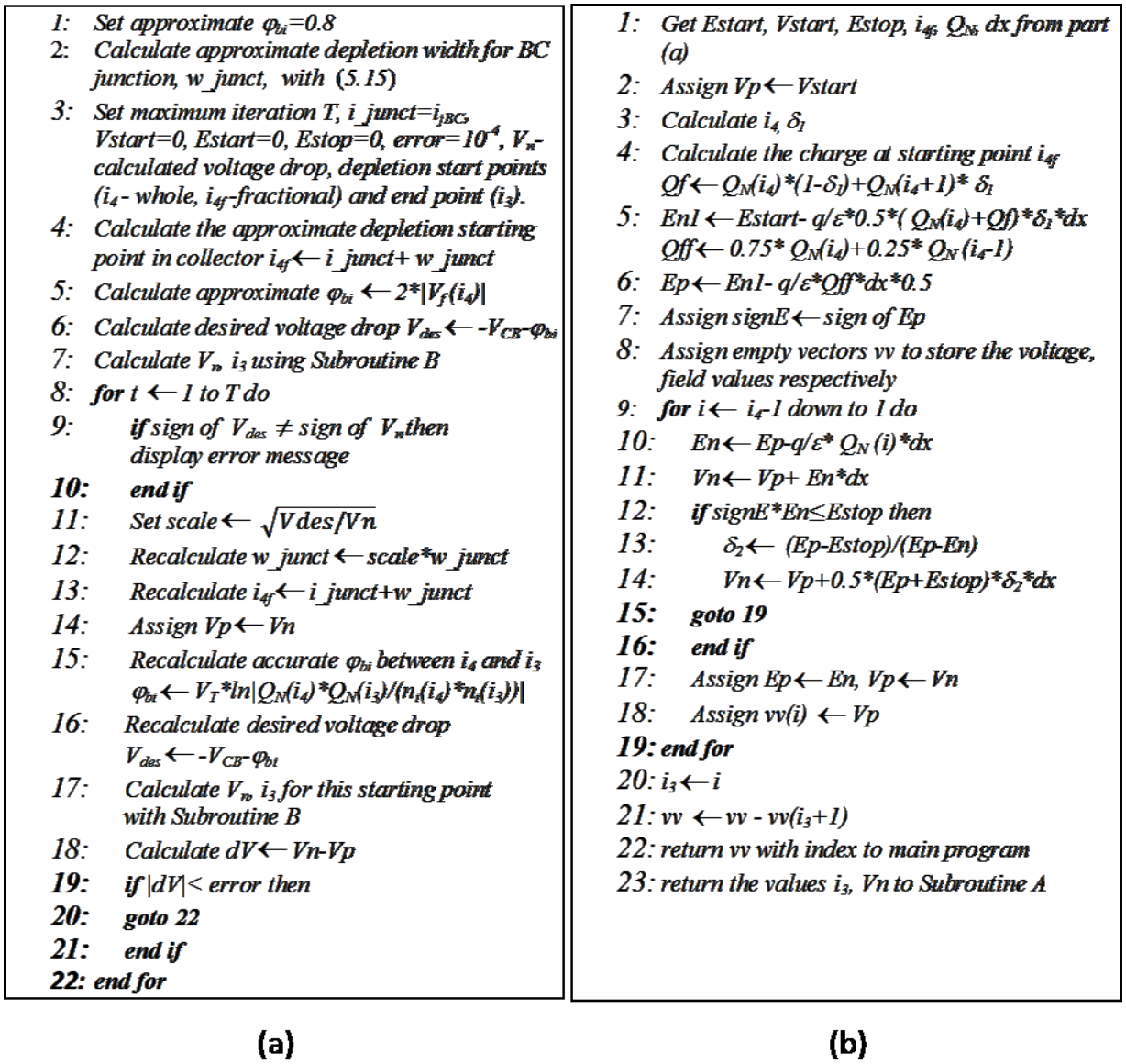


Figure 5.4 - Pseudocodes for BC depletion-region calculations (a) Subroutine A - calculating the depletion start point, built-in potential between the depletion start and end points, desired voltage drop across the junction, and checking whether the accuracy is reached (b) Subroutine B - calculating the potentials, charges and field at and between the fractional start and end points, and returning the end point and the potential at the fractional end point to (a), and also returning the potential between the start and end points to the main program.

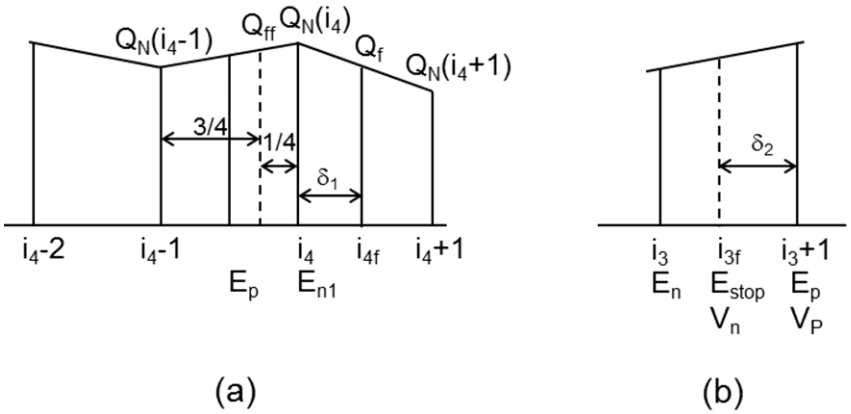
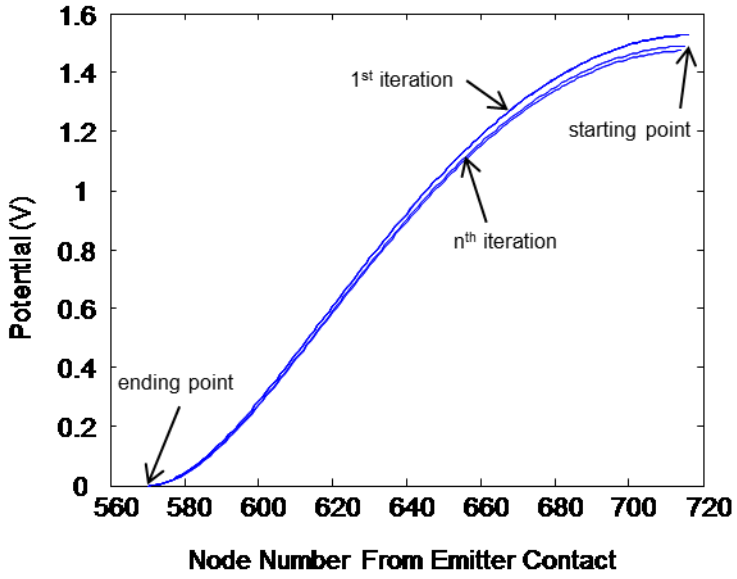
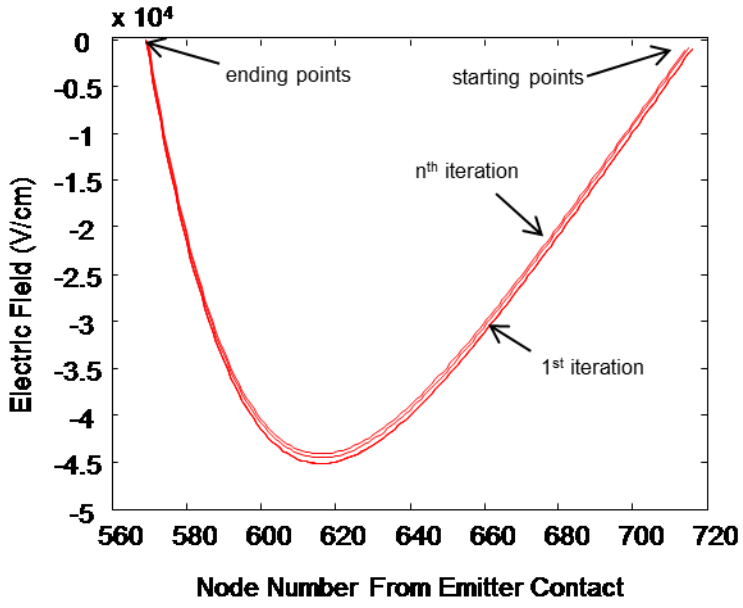


Figure 5.5 - BC depletion-region fractional start and end point illustrations (a) showing the fractional and whole number start points (i_{4f}, $i_{4)}$, decimal part (δ_1) and the charges (Q_N, Q_f, Q_{ff}) (b) showing the fractional and whole number end points (i_{3f}, $i_{3)}$, decimal part (δ_2), potentials (V_n,V_p) and electric fields (E_n, E_{stop}, E_p).

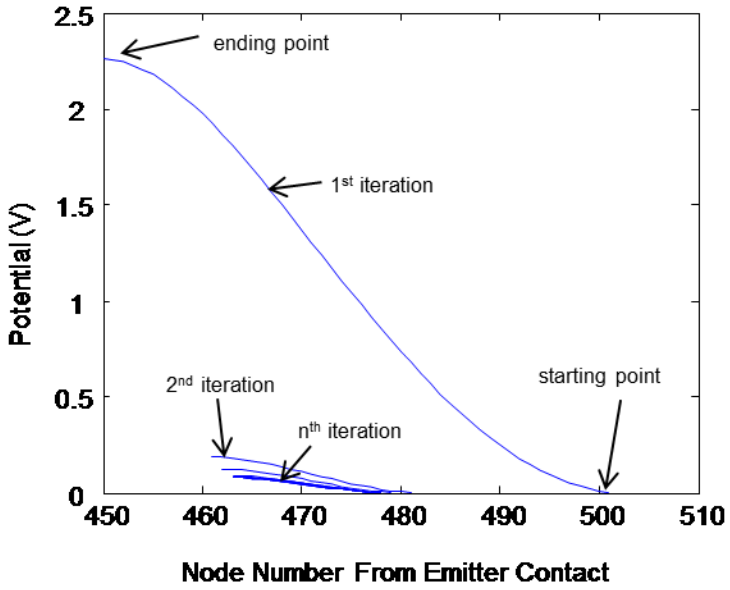


(a)

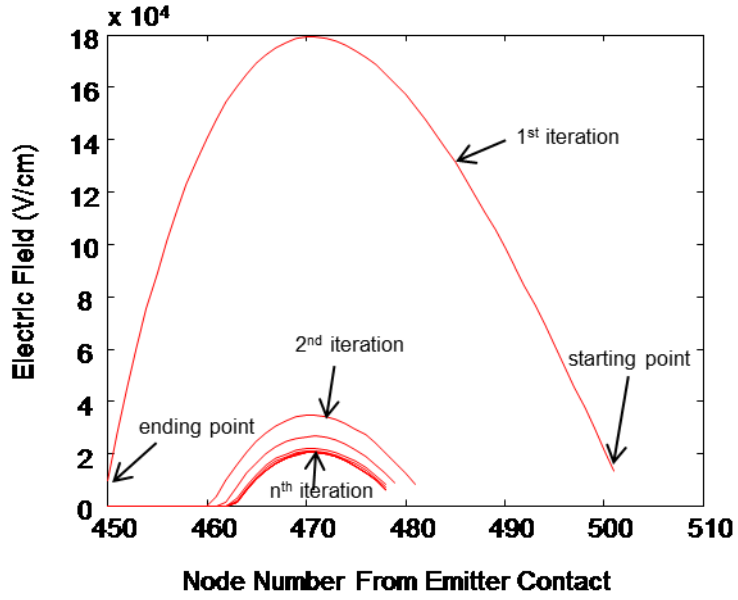


(b)

Figure 5.6 - Base-collector depletion region (a) potential with iteration (b) electric field with iteration



(a)



(b)

Figure 5.7 - Base-emitter depletion region (a) potential with iteration (b) electric field with iteration

A similar procedure is followed for solving the Poisson equation in the BE junction. The BE junction is forward biased and for a linearly-graded forward-biased junction the depletion width can be written as [97]

$$w = \left(\frac{12\varepsilon(\varphi_{bi} - V_{BE})}{qa} \right)^{1/3} \tag{5.16}$$

where a is the impurity gradient, and the depletion layer width varies as $(\varphi_{bi}\text{-}V_{BE})^{1/3}$. The changes in potential distribution and the electric field with iteration are shown in Figure 5.7.

5.3.3 Electrostatic potential and electric field calculations for the entire region

In this 1-D modeling the entire structure is considered as a two-port network between the emitter (node i = 0) and collector contacts (node i = N). Boundary conditions are set similar to Gummel [95] and presented as follows: Carrier equilibrium and charge neutrality are assumed at the end points. According to carrier equilibrium, $\varphi_n = \varphi_p$ at the emitter and collector contacts, where φ_n is the electron quasi-Fermi potential (EQFP) and φ_p is the hole quasi-Fermi potential (HQFP). We set $\varphi_n(0) = \varphi_p(0) = V_{EB}$ at the emitter contact and $\varphi_n(N) = \varphi_p(N) = V_{CB}$ at the collector contact. In the base $\varphi_n \neq \varphi_p$ and an ohmic contact cannot be assumed. In addition, the majority-carrier Fermi-level is nearly constant in the base but the minority-carrier Fermi-level is not. Hence we specify that the quasi-Fermi potential for the majority carriers in the base at a point M, $\varphi_p(M) = V_B = 0$ and take it as the reference level for potential. Since the base is very thin and the majority Fermi-level is nearly constant in the base, the point M can be anywhere in the base quasi-neutral region. As per charge neutrality, the total charge is zero at the emitter and collector contacts ($Q_N = N_D - N_A + p - n = 0$). With the above assumptions and settings the following equations can be obtained for electrostatic potential (EP) at contacts:

Emitter contact $$\varphi(0) = V_{EB} + V_f(0) \tag{5.17}$$

Collector contact $$\varphi(N) = V_{CB} + V_f(N) \tag{5.18}$$

Base contact $$\varphi(M) = V_B + V_f(M) \tag{5.19}$$

Assuming there is no voltage drop due to resistance and all voltage drops will be in the BE and BC depletion regions, a general form of the electrostatic potential equation for emitter, collector and base quasi-neutral regions (including contacts) can be written as:

$$\varphi(i) = V_{Contact} + V_f(i) \tag{5.20}$$

where $V_{contact}$ is V_{EB} (for emitter) or V_{CB} (for collector) or V_B (for base) according to the region considered. By combining with the electrostatic potential calculated in the depletion regions, the electrostatic potential for the entire region is obtained as in the example in Figure 5.8. Spline approximation is used at the connection points. The electric field for the entire region is obtained from

$$E = -\frac{d\varphi}{dx} \tag{5.21}$$

as shown in Figure 5.9.

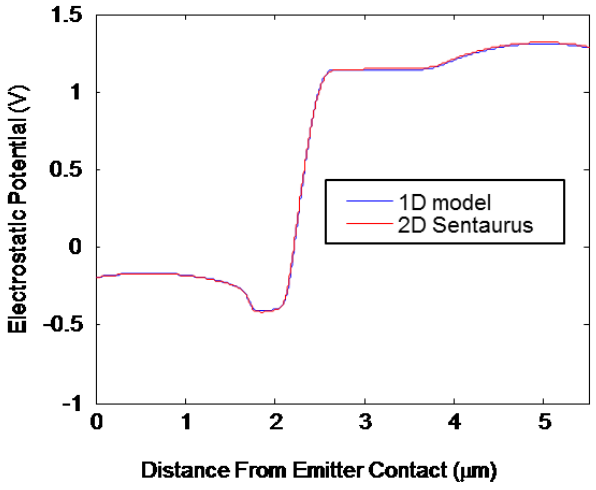


Figure 5.8 - Electrostatic potential for the entire region

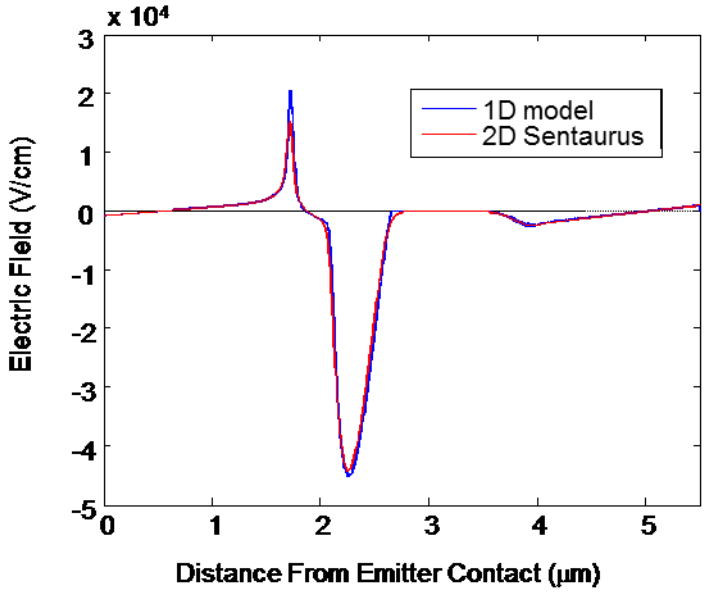


Figure 5.9 - Electric field for the entire region

5.3.4 Field dependent mobility and velocity calculations

The mobility of electrons and holes in semiconductors depends on several scattering mechanisms including doping and temperature. In this work, we adopt the doping dependent mobility model described in [98], which is a slightly modified form of [89] to include phonon scattering. The doping dependent mobility (μ_{dop}) is given by:

$$\mu_{dop} = \mu_{\min 1} \exp\left(-\frac{-P_c}{N_{total}}\right) + \frac{\mu_{const} - \mu_{\min 2}}{1+\left(N_{total}/C_r\right)^{\alpha}} - \frac{\mu_I}{1+\left(C_s/N_{total}\right)^{\beta}} \tag{5.22}$$

$$\text{where } \mu_{const} = \mu_L\left(\frac{T}{300K}\right)^{-\zeta},$$

μ_L is the mobility due to bulk phonon scattering, μ_{min1}, μ_{min2}, $\mu_{I,}$ and μ_{const} are the reference mobilities, P_c, C_r, and C_s are the reference doping concentrations and α, β and ζ are the exponents. These parameter values are presented in Table 4.2.

In high electric fields, the carrier drift velocity is no longer proportional to the electric field, instead the velocity saturates at a finite value. In bipolar transistors, velocity saturation occurs in the BC depletion region. To represent the high field saturation effects we used the Canali model [85], an improved form of Caughey–Thomas formula [99], with the addition of temperature-dependent parameters. The Canali model represents the saturation effects in mobility (μ_{Field}) and velocity (ν_{Field}) as follows [59, 85]:

$$\mu_{Field} = \frac{\mu_{dop}}{\left[1+\left(\frac{\mu_{dop}\,E}{\nu_{sat}}\right)^{\beta_1}\right]^{1/\beta_1}} \quad \text{and} \quad \nu_{Field} = \mu_{Field}\,E \tag{5.23}$$

$$\text{where} \quad \beta_1 = \beta_0\left(\frac{T}{300K}\right)^{\beta_{\exp}}, \quad \nu_{sat} = \nu_{sat,0}\left(\frac{300K}{T}\right)^{\nu_{sat,\exp}},$$

and V_{sat} is the saturation velocity and E is the electric field (Figure 5.9). By substituting parameters from Table 4.3 in (5.23), the carrier mobilities and velocities can be calculated.

5.3.5 Novel Integrated approach for calculating carrier concentration in base

A novel integrated approach was developed in order to speed up the process. This approach gives high accuracy with a much smaller number of sections. First electron concentrations are calculated at the BC and BE junction edges. Then by solving the electron transport equation with an integrated approach, the electron concentration distribution and the currents in the base are computed. Details of this computation process are described as follows:

Assuming the transport is due to drift in the BC depletion region, the electron concentration at the BC depletion region edge can be calculated as:

$$n_{BC\_edge\_i_3} = -\frac{J_n(i_3)}{q\nu_n(i_3)} \tag{5.24}$$

where ν_n is the field dependent velocity calculated in (5.23). Electron concentration at the BE depletion region edge can be calculated as:

$$n_{BE\_edge\_i_2} = n_0(i_2)\exp\left(\frac{qV_{BE}}{kT}\right) \tag{5.25}$$

The following process is performed to calculate the carrier concentration in the base.

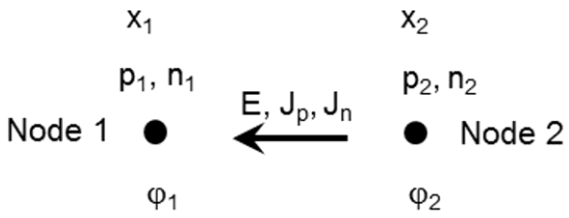


Figure 5.0.10 - Illustration of nodes 1 and 2, positions (x_1, x_2), hole, electron densities (p_1, p_2, n_1, n_2), potentials (φ_1, φ_2), current densities (J_p, J_n) and electric field (E).

Consider a segment in the base between two adjacent nodes as shown in Figure 5.10. Starting from the transport equation for electrons

$$J_n = qD_n\frac{dn}{dx} - q\mu_n n\frac{d\varphi}{dx} \tag{5.26}$$

Using the Einstein relation $D_n = \mu_n V_T$ and multiplying by $\exp\left(\frac{\varphi}{V_T}\right)$ yields

$$J_n\exp\left(\frac{\varphi}{V_T}\right) = q\mu_n V_T\frac{dn}{dx}\exp\left(\frac{\varphi}{V_T}\right) - q\mu_n\frac{d\varphi}{dx}n\exp\left(\frac{\varphi}{V_T}\right) \tag{5.27}$$

Now replace $d\varphi = -d\varphi$ and rearrange,

$$J_n\exp\left(\frac{\varphi}{V_T}\right) = q\mu_n V_T\frac{dn}{dx}\exp\left(\frac{\varphi}{V_T}\right) + q\mu_n\frac{d\varphi}{dx}n\exp\left(\frac{\varphi}{V_T}\right) \tag{5.28}$$

$$J_n \exp\left(\frac{\varphi}{V_T}\right) = q\mu_n V_T \frac{d}{dx}\left[n \exp\left(\frac{\varphi}{V_T}\right)\right] \tag{5.29}$$

Performing integration

$$\int_{x_2}^{x_1} J_n \exp\left(\frac{\varphi}{V_T}\right) dx = \mu_n q V_T \left[n \exp\left(\frac{\varphi}{V_T}\right)\right]_{x_2}^{x_1} \tag{5.30}$$

Substituting $\varphi = -Ex$

$$\left[-\frac{J_n}{\mu_n q V_T}\frac{V_T}{E}\exp\left(\frac{-Ex}{V_T}\right)\right]_{x_2}^{x_1} = \left[\text{n} \exp\left(\frac{-Ex}{V_T}\right)\right]_{x_2}^{x_1} \tag{5.31}$$

$$-\frac{V_T}{E} J_n \left[\exp\left(\frac{-Ex_2}{V_T}\right) - \exp\left(\frac{-Ex_1}{V_T}\right)\right] = \mu_n q V_T \left(n_2 \exp\left(\frac{\varphi_2}{V_T}\right) - n_1 \exp\left(\frac{\varphi_1}{V_T}\right)\right) \tag{5.32}$$

$$-\frac{V_T}{E} J_n \left[\exp\left(\frac{\varphi_2}{V_T}\right) - \exp\left(\frac{\varphi_1}{V_T}\right)\right] = \mu_n q V_T \left(n_2 \exp\left(\frac{\varphi_2}{V_T}\right) - n_1 \exp\left(\frac{\varphi_1}{V_T}\right)\right) \tag{5.33}$$

$$J_n = -q\mu_n E \frac{n_2 \exp\left(\frac{\varphi_2}{V_T}\right) - n_1 \exp\left(\frac{\varphi_1}{V_T}\right)}{\exp\left(\frac{\varphi_2}{V_T}\right) - \exp\left(\frac{\varphi_1}{V_T}\right)} \tag{5.34}$$

by substituting $\varphi_1 = \varphi_2 + \Delta\varphi$ we obtain

$$J_n = -q\mu_n E \frac{n_2 - n_1 \exp\left(\frac{\Delta\varphi}{V_T}\right)}{1 - \exp\left(\frac{\Delta\varphi}{V_T}\right)} \tag{5.35}$$

Replacing $d\varphi = -d\varphi$, substituting E = -Δφ/dx, and rearranging, the formula becomes

$$n_1 = n_2 \exp\left(\frac{\Delta\varphi}{V_T}\right) + \frac{J_n \Delta x}{q\mu_n V_T} \frac{\exp\left(\frac{\Delta\varphi}{V_T}\right) - 1}{\frac{\Delta\varphi}{V_T}} \tag{5.36}$$

Therefore, the electron density between two adjacent nodes can be related as:

$$n(i) = n(i+1)\gamma + n_{diff}\lambda \tag{5.37}$$

where $\Delta\varphi = \varphi(i) - \varphi(i+1)$, $dV = \frac{\Delta\varphi}{V_T}$, $\gamma = \exp(dV)$, $\lambda = \frac{(\gamma - 1)}{dV}$, and $n_{diff} = -\frac{J_n(i+1)\,\Delta x}{q\mu_n(i+1)V_T}$.

The electron current in the BC depletion region is considered as constant with an assumption that there is no recombination in the BC depletion region. Starting from $J_n = 0$ at the BC depletion edge (i_3), and increasing by steps, the transport equation is iteratively solved in the base until attaining the calculated electron concentration at the BE depletion edge (i_2). Recombination is also included in the base, and recombination current density (J_r) is calculated from

$$J_r = q\,R\,\Delta x \tag{5.38}$$

where R is the recombination rate between the adjacent nodes i and i+1. R is calculated with a lifetime of $\tau_n = \tau_p = 10^{-7}$s as follows:

$$R = \frac{n(i+1)p(i+1) - n_i(i+1)n_i(i+1)}{\tau_n\left(p(i+1) + n_i(i+1)\right) + \tau_p\left(n(i+1) + n_i(i+1)\right)} \tag{5.39}$$

With the inclusion of recombination current density, the electron current density is found as:

$$J_n(i) = J_n(i+1) + J_r \tag{5.40}$$

By adding recombination current density along the base (from the BC depletion edge to the BE depletion edge) the total recombination current density (J_{BR}) can be computed as follows:

$$J_{BR} = \sum_{i_3}^{i_2} J_r \tag{5.41}$$

The pseudo code for these calculations is presented in Figure 5.11.

```
1:  Set i2 = BE depletion edge, i3 = BC depletion edge, tp = tn = 10^-7, step = 10, maximum iteration T.
2:  Calculate n at i2 (n_BE_edge_i2) with (5.25)
3:  Initialize Jn=0 in BC depletion region
4:  for t ← 1 to T do
5:      Jn ← Jn+step
6:      Calculate n at i3 with (5.24)
7:      Initialize J_BR ←0
8:      for i←i3 down to i2 do
9:          Calculate dV, ndiff with (5.37)
10:         Calculate R, Jp, Jn with (5.38-5.40)
11:         Update J_BR ← J_BR +J, with (5.41)
12:         Define dVmin=10^-10
13:         if absolute dV < dVmin then
14:             if dV >= 0 then dV ←dVmin
15:             else
16:                 dV←-dVmin
17:             end if
18:         end if
19:         γ←exp(dV)
20:         λ← (γ-1)/dV
21:         Update the following with (5.36)
            n2← n(i+1)
            n1← n2 γ + nAB λ
            n(i) ← n1
22:     end for
23:     error ← n(i2) - n_BE_edge_i2
24:     if |error|<10^2 then
25:         goto 32
26:     elseif error>0 then
27:         Jn ← Jn - step
28:         step ← step/10
29:     elseif error<0 then
30:         goto 4
31:     end if
32: end for
```

Figure 5.11 - Subroutine C - new iterative approach for calculating carrier concentration in base. Starting from electron current density J_n=0 at the BC depletion edge (i_3), and increasing by steps for each iteration, the electron concentration distribution in the base is computed until achieving the required accuracy at the BE depletion edge (i_2).

The electron concentration in the BC depletion-region was also computed using the same integrated approach using (5.39). But an iterative process is not required in this case. Now the current is known at the BC depletion edge (i_3). Assuming no recombination in the BC depletion region the collector current is taken as constant. The electron concentrations in the collector and

emitter quasi-neural regions are already known (5.12). Spline approximation is used to generate the complete electron concentration plot (Figure 5.13).

5.3.6 Calculation of carrier concentrations in emitter and collector

In the next step, carrier concentrations in emitter and collector are calculated to complete our model. We utilized the integrated approach as described in the previous section, however hole transport is considered instead of electron transport, and the hole concentration between two adjacent nodes (Figure 5.11) can be derived as follows:

Transport equation for holes

$$J_p = -qD_p \frac{dp}{dx} - q\mu_p p \frac{d\varphi}{dx} \tag{5.42}$$

multiplying by $\exp(\varphi / V_T)$

$$J_p \exp\left(\frac{\varphi}{V_T}\right) = -qD_p \frac{dp}{dx}\exp\left(\frac{\varphi}{V_T}\right) - q\mu_p \frac{d\varphi}{dx} p \exp\left(\frac{\varphi}{V_T}\right) \tag{5.43}$$

$$J_p \exp\left(\frac{\varphi}{V_T}\right) = -q\mu_p V_T \frac{d}{dx}\left[p \exp\left(\frac{\varphi}{V_T}\right)\right] \tag{5.44}$$

performing integration

$$-\int_{x_1}^{x_2} \frac{J_p}{\mu_p q V_T} \exp\left(\frac{\varphi}{V_T}\right) dx = \left[p \exp\left(\frac{\varphi}{V_T}\right)\right]\Bigg|_{x_1}^{x_2} \tag{5.45}$$

Substituting $\varphi = -Ex$

$$\left[\frac{J_p}{\mu_p q V_T}\frac{V_T}{E}\exp\left(\frac{-Ex}{V_T}\right)\right]\Bigg|_{x_1}^{x_2} = \left[p \exp\left(\frac{-Ex}{V_T}\right)\right]\Bigg|_{x_1}^{x_2} \tag{5.46}$$

And after some arrangements

$$J_p = q\mu_p E \frac{p_2 \exp\left(\frac{\varphi_2}{V_T}\right) - p_1 \exp\left(\frac{\varphi_1}{V_T}\right)}{\exp\left(\frac{\varphi_2}{V_T}\right) - \exp\left(\frac{\varphi_1}{V_T}\right)} \tag{5.47}$$

by substituting $\varphi_1=\varphi_2+\Delta\varphi$ we obtain

$$J_p = q\mu_p E \frac{p_2 - p_1 \exp\left(\frac{\Delta\varphi}{V_T}\right)}{1 - \exp\left(\frac{\Delta\varphi}{V_T}\right)} \tag{5.48}$$

substituting $E = -\frac{\Delta\varphi}{\Delta x}$, and rearranging, the formula becomes

$$p_2 = p_1 \exp\left(\frac{\Delta\varphi}{V_T}\right) + \frac{J_p \Delta x}{q\mu_p V_T} \frac{\exp\left(\frac{\Delta\varphi}{V_T}\right) - 1}{\frac{\Delta\varphi}{V_T}} \tag{5.49}$$

$$p_2 = p_1\gamma + p_{diff}\left(\frac{\gamma - 1}{dV}\right) \tag{5.50}$$

Hence hole concentration between two adjacent nodes can be related as

$$p_2 = p_1\gamma + p_{diff}\lambda \tag{5.51}$$

$$p(i+1) = p(i)\gamma + p_{diff}\lambda \tag{5.52}$$

where, $\Delta\varphi = \varphi(i) - \varphi(i+1)$, $dV = \frac{\Delta\varphi}{V_T}$, $\gamma = \exp(dV)$, $\lambda = \frac{(\gamma - 1)}{dV}$, and $p_{diff} = \frac{J_p(i)\Delta x}{q\mu_p(i)V_T}$

Calculations of hole concentration for the emitter quasi-neutral region and collector quasi-neutral region are described in detail below. The same equation (5.52) is used for both cases. Recombination in the emitter cannot be neglected for the modern transistors with highly-doped

polysilicon emitters. Therefore, recombination is included for the emitter but not the collector.

5.2.6.1 For emitter quasi-neutral region

Hole concentration at the BE junction edge can be written as:

$$p_{BE\_edge\_i_1} = p_0(i_1)\exp\left(\frac{qV_{BE}}{kT}\right) \tag{5.53}$$

The hole concentration at the emitter contact is calculated by the equation below assuming that charge neutrality and equilibrium prevail at the contact, which is assumed to be an ohmic.

$$p(1) = p_0(1) \tag{5.54}$$

Starting from $J_p = 0$ at the emitter contact, and increasing by steps, the transport equation is iteratively solved until it equals the calculated hole concentration at the BE depletion edge. Recombination is also included as

$$R = \frac{n(i)p(i) - n(i)n(i)}{\tau_n\left(p(i) + n_i(i)\right) + \tau_p\left(n(i) + n_i(i)\right)} \tag{5.55}$$

with a lifetime of $\tau_n=\tau_p=10^{-8}$s. Lower values were assumed for lifetimes since the emitter is highly doped. The electron and hole current densities in emitter are written as:

$$J_p(i+1) = J_p(i) + J_r \tag{5.56}$$

$$J_n(i+1) = J_n(i) - J_r \tag{5.57}$$

5.2.6.2 For collector quasi-neutral region

Assuming charge neutrality and equilibrium exist at the collector contact (which is ohmic), the hole concentration at the collector edge can be represented as:

$$p(N) = p_0(N) \tag{5.58}$$

The hole concentration in the quasi-neutral base region and at the BC depletion edge (i_3) are already known (analogous to (5.12)). Starting from $J_p = 0$ at BC depletion edge (i_3), and increasing by steps, the transport equation is iteratively solved until reaching the calculated hole concentration at the collector contact. As discussed above, a method similar to the one used for emitter quasi-neutral region is utilized. We assumed that there is no recombination in the BC depletion region or collector region. This makes the algorithm simpler. Spline approximation is used to generate complete hole density plot (Figure 5.12).

5.3.7 EQFP, HQFP calculations

Since we have calculated the electron and hole concentrations, the EP, the EQFP and HQFP for the entire region can be computed as follows:

$$\varphi_p(i) = V_T \ln \frac{p(i)}{n_i(i)} + \varphi(i) \tag{5.59}$$

$$\varphi_n(i) = \varphi(i) - V_T \ln \frac{n(i)}{n_i(i)} \tag{5.60}$$

The 1-D simulation results for the EQFP, HQFP and electron velocity along with 2-D Sentaurus simulation results are illustrated in Figures 5.13 and 5.14. The minute differences between the 1-D and 2-D curve data may be due to the assumption that the current density is uniform across the width of the transistor in the 1-D model, whereas, the current density is not uniform across the width of the transistor in the 2-D Sentaurus model. Furthermore, in our 1-D model, drift-diffusion equation with velocity saturation is used for carrier transport whereas in Sentaurus the hydrodynamic model was used which is necessary to apply velocity saturation in Sentaurus. Regardless of these minor differences, the data presented in these two figures affirm that these simulation results are in very close agreement with each other.

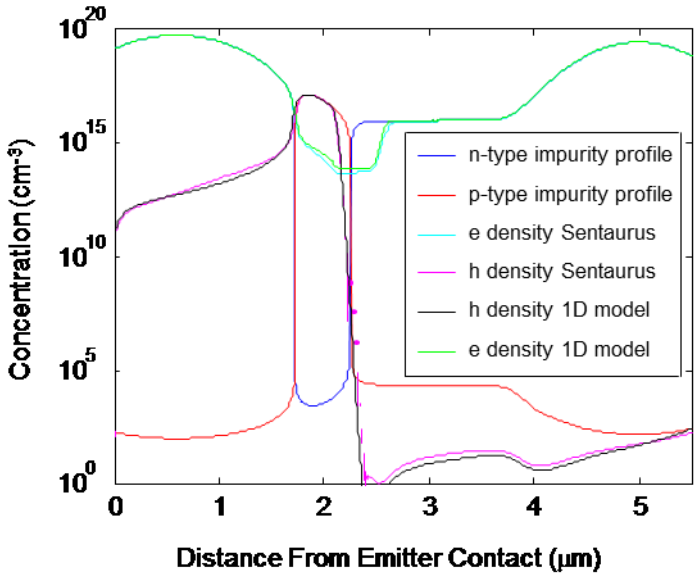


Figure 5.12 - Impurity profiles, electron density and hole density of an npn transistor

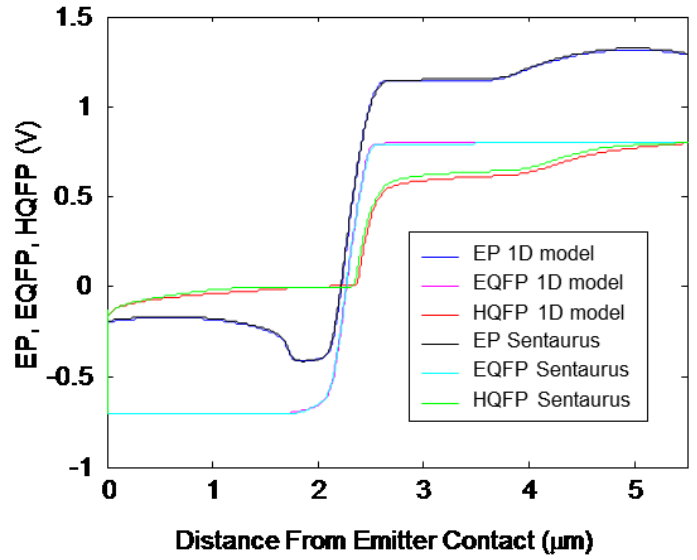


Figure 5.13 - EP, EQFP and HQFP of an npn transistor

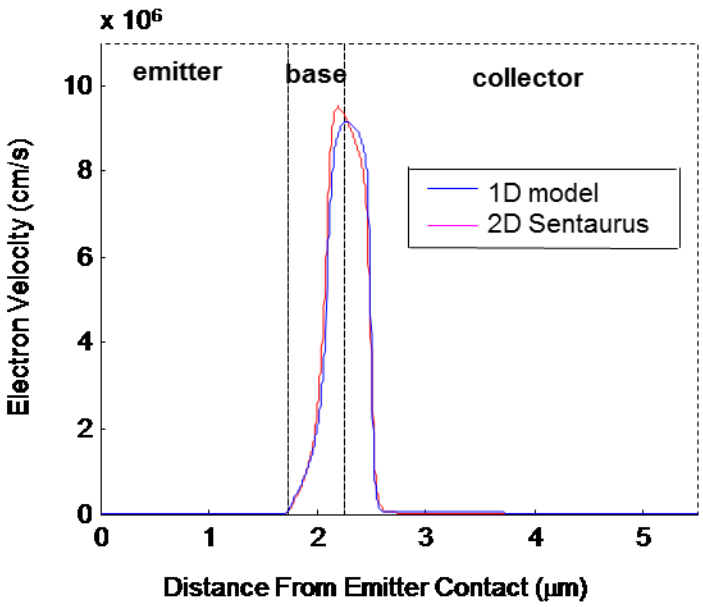


Figure 5.14 - Electron velocity of an npn transistor

5.4 Modeling of a pnp transistor with MATLAB

The pnp BJT model was developed by interchanging the doping type for the same profile and making appropriate sign changes. As shown in the profile in Figure 5.15, for a pnp transistor the emitter and the collector are p-type and the base is n-type. In pnp transistors the collector and the base voltages are negative with respect to the emitter for the normal operation mode (V_{BE} and V_{CE} are negative). Appropriate changes have to be included when solving the Poissons's equations for the junctions. With these changes the electrostatic potential and the electric field were calculated and plotted as shown in Figure 5.16 and 5.17 respectively. The electrostatic potential and the electric field from Sentaurus simulation are also shown in the same figures for comparison. All are showing very good matching.

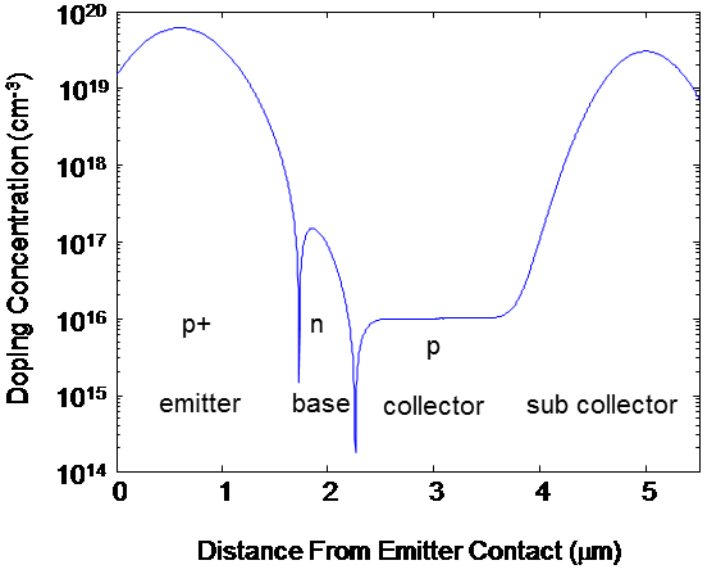


Figure 5.15 - Doping profile of the pnp transistor

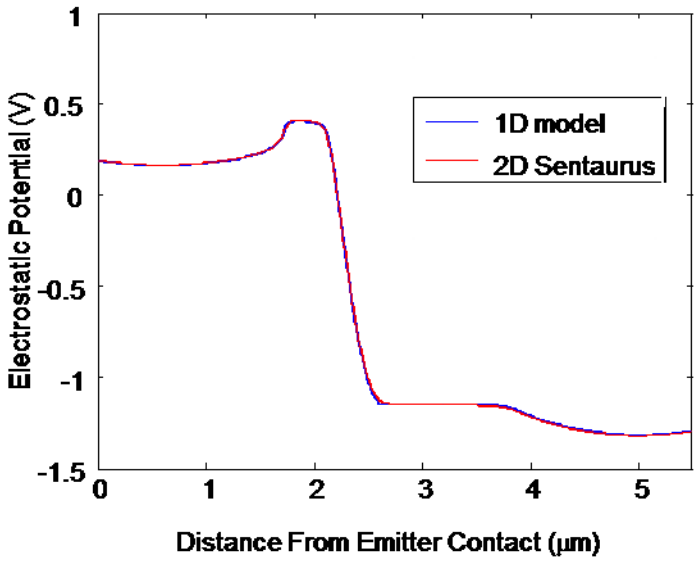


Figure 5.16 - Electrostatic potential of a pnp transistor

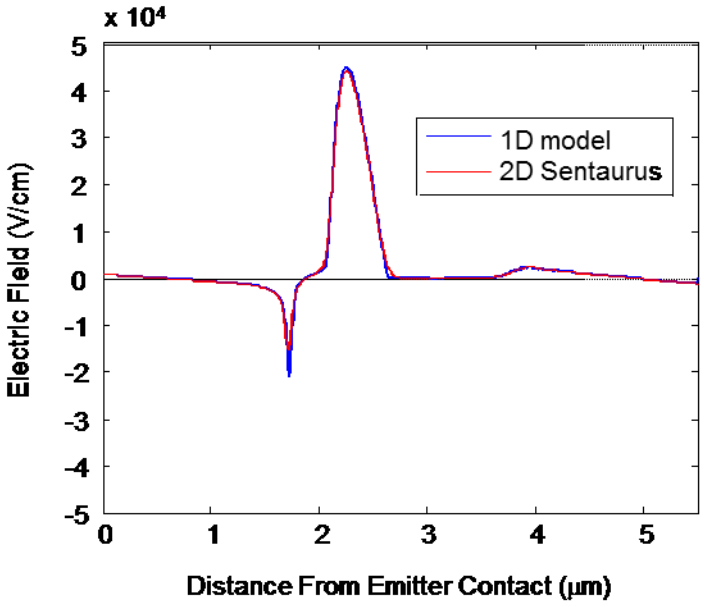


Figure 5.17 - Electric field of a pnp transistor

In the pnp transistor the minority-carriers in the base are holes and the minority-carriers in the emitter and the collector are electrons. Hence, in contrast to the npn transistor, hole transport equations should be solved in the base and the electron transport equations should be solved in the emitter and collector. Calculated minority carrier concentrations from 1-D model along with the minority carrier concentrations from Sentaurus simulation are shown in Figure 5.18.

The mobility of the hole is less than the mobility of electron for the same doping concentration. The saturation velocity is also slightly less for holes. Due to these reasons the carrier velocity is less for pnp transistors than the npn transistors in the base as shown in Figure 5.19.

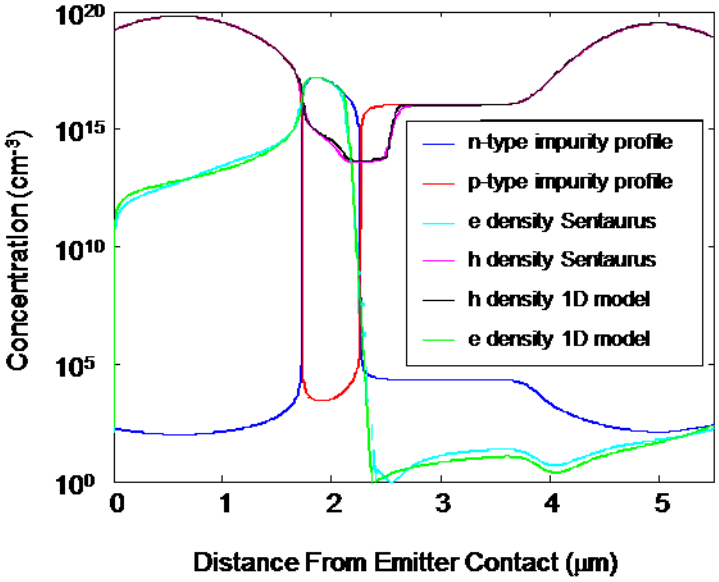


Figure 5.18 - Impurity profiles, electron density and hole density of a pnp transistor

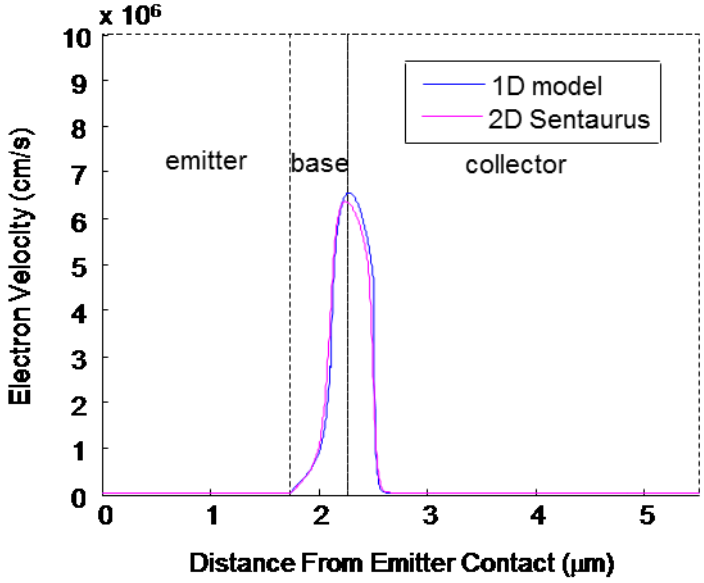


Figure 5.19 - Hole velocity of a pnp transistor

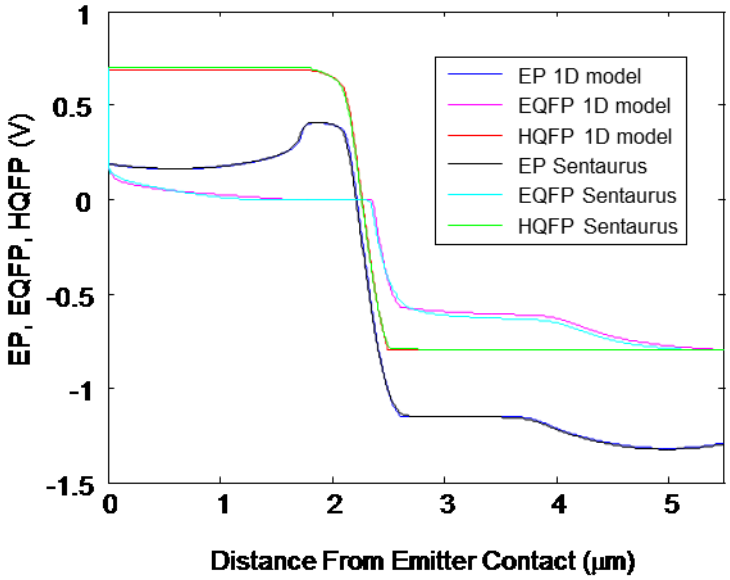


Figure 5.20 - EP, EQFP and HQFP of a pnp transistor

The 1-D simulation results of EP, EQFP and HQFP along with 2-D Sentaurus simulation results are shown in Figure 5.20. Again these are closely matching.

The 1-D model simulations were very fast compared to Sentaurus 2-D and 3-D simulations. It also showed comparable results with Sentaurus 2-D model simulations for both npn and pnp transistors. In the next section this model was used to verify some text book approaches.

5.5 Application of 1-D model to verify text book approaches

I-V Characteristics and Early voltage

Figure 5.21 illustrates the I_C-V_{CE} characteristics of an npn bipolar transistor obtained from the 1-D model developed. An Early voltage of 50.4 V was obtained from the I_C-V_{CE} characteristics, which is very close to the Early voltage obtained from the experiments.

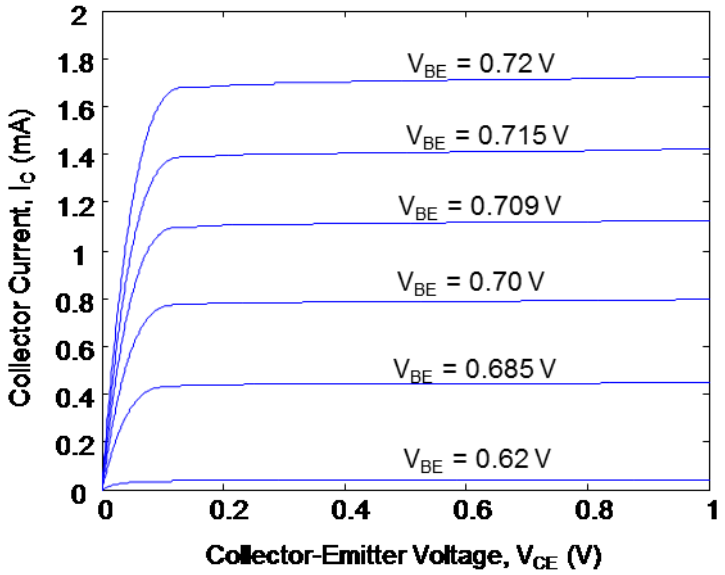


Figure 5.21 - I-V characteristics of an npn transistor

Gummel plot and dc current gain

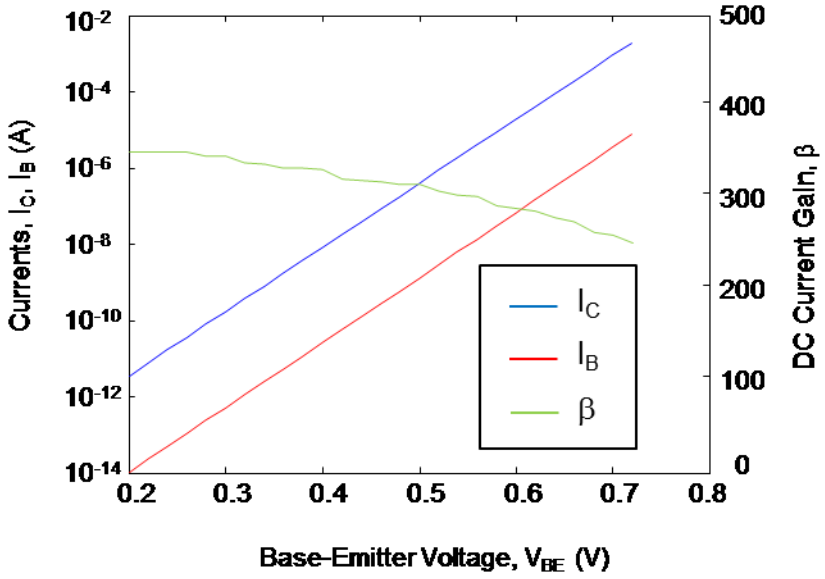


Figure 5.22 - Gummel plot and dc current gain of an npn transistor

Figure 5.22 shows the Gummel plot and current gain plots obtained using the 1-D model. The dc current gain is about 250 for a base-emitter voltage of 0.7 V, again this is close to the value of 200 from experiments.

Verification of drift/diffusion at integration point vs integral formulation

Usually two different methods are used in textbooks to calculate the collector currents in bipolar transistors. One is calculating the drift/diffusion components at the integration point (base-emitter depletion edge in base) and the other one is using the Gummel integral formulation at the same point. The two approaches are verified here using this model.

(a) Collector current calculation by drift/diffusion method

The collector current is given by drift and diffusion current components as

$$J_n = J_n(\text{diffusion}) + J_n(\text{drift}) \tag{5.61}$$

$$J_n = qD_n \frac{dn}{dx} - q\mu_n n \frac{d\varphi}{dx} \tag{5.62}$$

The total collector current density (drift/diffusion components together) at base-emitter injection point can be directly obtained from the numerical model as:

$$J_n(i_2) = 322.58 \text{ A/cm}^2$$

In another way, the drift/diffusion components can be separately calculated as follows:

$$J_n(diffusion) = q\mu_n(i_2)\frac{n(i_2) - n(i_2+1)}{dx} \tag{5.63}$$

$$= 6749.7 \text{ A/cm}^2$$

$$J_n(drift) = -q\mu_n(i_2)\frac{\left(n(i_2) + n(i_2+1)\right)}{2}\frac{\left(\varphi(i_2) - \varphi(i_2+1)\right)}{dx} \tag{5.64}$$

$$= -6425.7 \text{ A/cm}^2$$

As indicated by the different signs the drift and diffusion current components are in opposite directions. The resultant collector current is obtained by adding them together as:

$$J_n = 323.94 \text{ A/cm}^2$$

(b) Collector current by Gummel integral formulation

Collector current density

$$J_n = \frac{q\, n_{i0}^2}{G_B} \exp\left(\frac{qV_{BE}}{kT}\right) \tag{5.65}$$

where G_B is the base Gummel number given by

$$G_B = \int_o^w \frac{n_{i0}^2}{n_{iB}^2} \frac{N_B}{D_B} dx \tag{5.66}$$

The base Gummel number has been calculated by integrating from base-emitter depletion edge to base-collector depletion edge as follows in Figure 5.23.

1: Initialize Gummel number $G_B \leftarrow 0$
2: i_2 is the BE depletion point in the base, and i_3 is the BC depletion point in the base(Figure 5.3)
3: ***for*** *$i \leftarrow i_2$ to i_3 do*
4: $G_B \leftarrow G_B + \frac{n_{i0}^2}{n_i(i)^2} \frac{p(i)dx}{\mu_n(i)V_T}$
5: end for

Figure 5.23 - Gummel plot and dc current gain of an npn transistor

By plugging the value of G_B into (5.65) the collector current density has been calculated as

$$J_n = 269.28 \text{ A/cm}^2$$

The difference between the drift/diffusion method and the Gummel integral formulation is 16.5%. The reason for the difference is the Gummel integral method is an approximation of finding the collector current.

5.6 Modeling the mechanical stress effect

In 1-D modeling also we separately modeled the stress effects in mobility and the intrinsic carrier concentration using the piezoresistance mobility model and the deformation potential model from Creemer and French's work (Table 2.3) respectively. Addition of these stress models are described below.

Modeling the stress-induced changes in mobility

On the wafer planes, the transistor axes are aligned with the wafer axes. Hence, it is common to use the primed wafer coordinate system in which the stress dependent of mobility (μ′) can be expressed as:

$$\mu'(\sigma) = \mu\left(1 - \frac{\Delta\rho'}{\bar{\rho}}\right) \tag{5.67}$$

where μ is the doping and field dependent mobility calculated by (5.22). Using (2.21), the stress dependent mobility for an arbitrarily oriented conductor was estimated as

$$\mu_\sigma = \mu\left(1 - \left(\pi'_{\alpha\beta}\,\sigma^T\right)^T p^T\right) \tag{5.68}$$

where $\sigma = \lfloor \sigma'_1 \quad \sigma'_2 \quad \sigma'_3 \quad \sigma'_4 \quad \sigma'_5 \quad \sigma'_6 \rfloor$ and

$$p = \lfloor l'^2 \quad m'^2 \quad n'^2 \quad 2l'n' \quad 2m'n' \quad 2l'm' \rfloor$$

Modeling the stress-induced changes in intrinsic carrier concentration

The formulas in Table 2.3 were used to model the stress induced change in intrinsic carrier concentration and included to the 1-D BJT model as follows:

$$n_i(\sigma) = \sqrt{n_i^2\left(1 + \frac{\Delta n_i^2}{n_i^2}\right)} \tag{5.69}$$

where n_i is the doping dependent effective intrinsic carrier concentration calculated by (5.9). The developed 1-D numerical model was used to analyze the stress-induced changes in bipolar transistors.

5.7 Verifying the validity of the model with experimental results and theoretical expectations

In this section, the 1-D model was validated by comparing its simulation results with experimental results and theoretical expectations. Stress induced changes in I_C-V_{CE} characteristics, Early voltage, barrier height, collector and base currents, and dc current gain for $\sigma'_{22}[\bar{1}10]$ were analyzed.

5.7.1 Changes in I_C-V_{CE} Characteristics

The simulated and experimental I-V characteristics of a vertical npn transistor on a (100) plane for tensile normal stress σ'_{22} are compared in Figure 5.24(a) and (b). Both plots closely match and clearly show that the collector current (I_C) reduces with increasing stress σ'_{22} for an npn vertical transistor in (100) plane. The rates of change in both plots are almost equal.

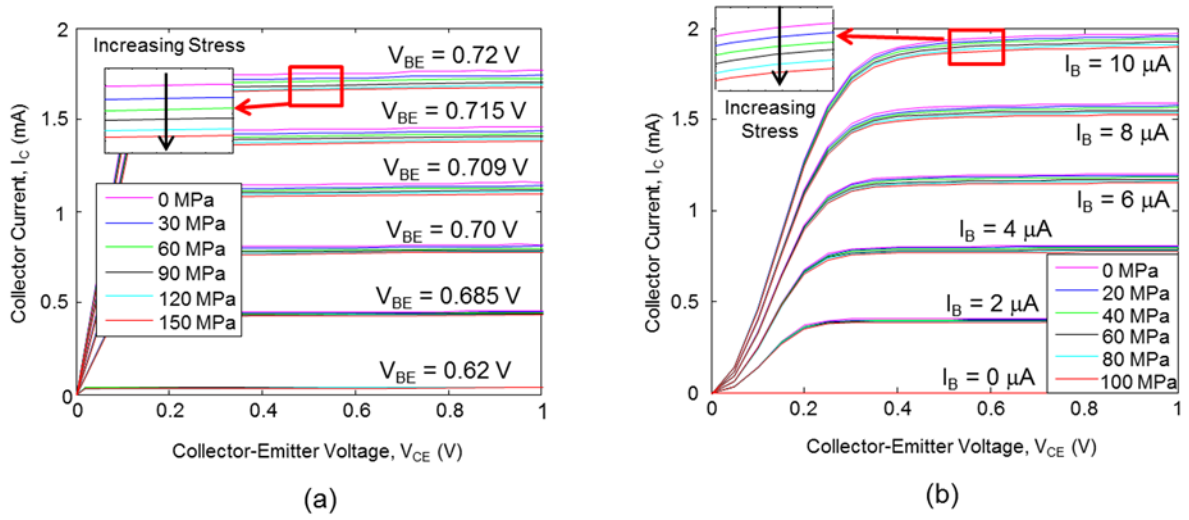


Figure 5.24 - Stress-induced change in I_C-V_{CE} characteristics of an npn bipolar transistor for σ'_{22} (a) 1-D Simulation results (b) Experimental results

5.7.2 Changes in Early voltage

The Early voltages were obtained from the I-V characteristics and plotted as in Figure 5.25(a) and 5.25(b). As per experiments the early voltage is 55.7 V and it slightly reduced with stress (~1.1 V/100MPa). As per simulations the early voltage is 50.4 V and it is also slightly reduced with stress (~0.7V/100 MPa).

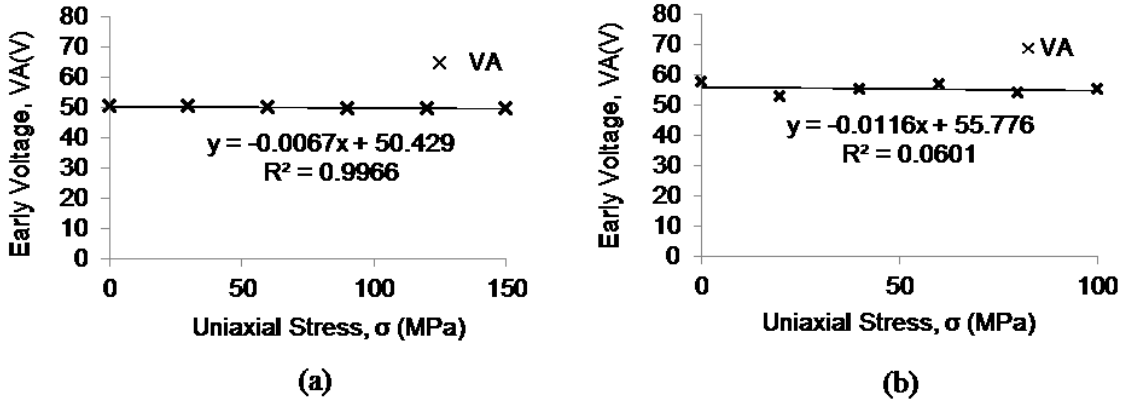


Figure 5.25 - Stress-Induced change in Early voltage of an npn bipolar transistor for σ'_{22} (a) 1-D Simulation results (b) Experimental results

5.7.3 Changes in barrier height at BE junction for npn and pnp BJTs

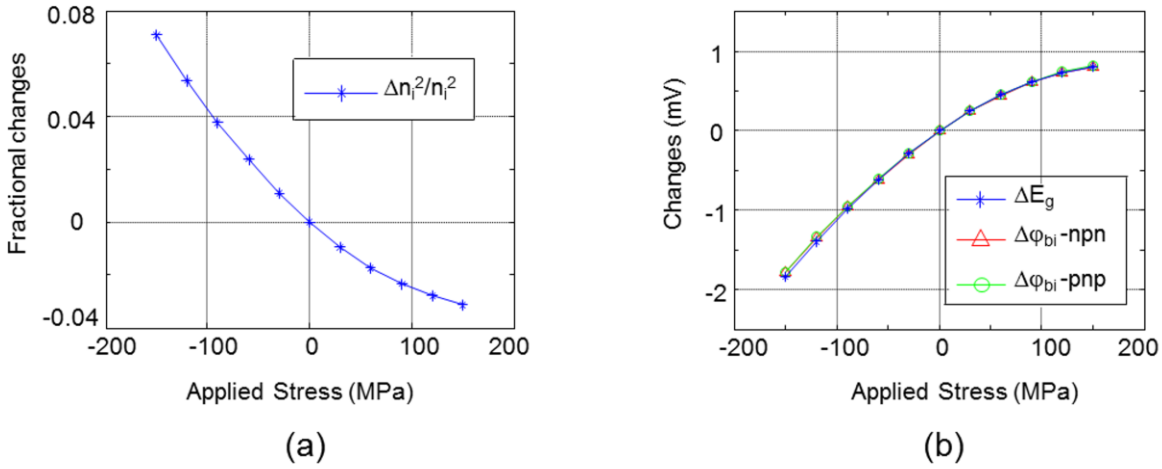


Figure 5.26 - Stress-induced changes for $\sigma'_{22}[\bar{1}10]$ (a) Fractional changes $\boldsymbol{\Delta n_i^2/n_i^2}$ (b) Changes in bandgap (ΔE_g), barrier height of npn BJT ($\Delta\varphi_{bi}$ - npn) and barrier height of pnp BJT ($\Delta\varphi_{bi}$ - pnp).

Figure 5.26(a) illustrates the stress induced changes in intrinsic carrier concentration ($\Delta n_i^2/n_i^2$). The stress induced changes in E_g can be obtained as ΔE_g = -kT ($\Delta n_i^2/n_i^2$) from equation (3.4). Figure 5.26(b) represents the simulated, stress induced changes in barrier heights of an npn and a pnp transistors (for V_{BE} = 0.7 V) along with the changes in bandgap, E_g. For tensile stress, the reduction in intrinsic carrier concentration causes an increase in E_g. For compressive stress increase in intrinsic carrier concentration reduces the barrier height. The changes in barrier heights are equal for both npn and pnp BJTs and are equal to the changes in E_g as depicted in Figure 5.26(b). Hence, the stress induced changes in intrinsic carrier concentration affect both npn and pnp BJTs equally.

5.7.4 Changes in currents and dc current gain

The changes in currents and dc current gain (for V_{BE} = 0.7 V) for an in-plane normal stress σ'_{22} were obtained from experiments and compared with simulation results for both npn and pnp transistors. The stress induced changes in barrier heights are same for npn and pnp transistors as explained in previous section. Tensile stress increases the barrier height and hence makes corresponding reduction in base and collector currents. Compressive stress reduces the barrier height and makes corresponding increase in base and collector currents. But the stress affects the mobility differently for npn and pnp transistors depending on the carrier type and the carrier concentration. Hence the overall changes in currents and current gain are different for npn and pnp BJTs. These changes are discussed in detail below.

<u>npn BJT</u>

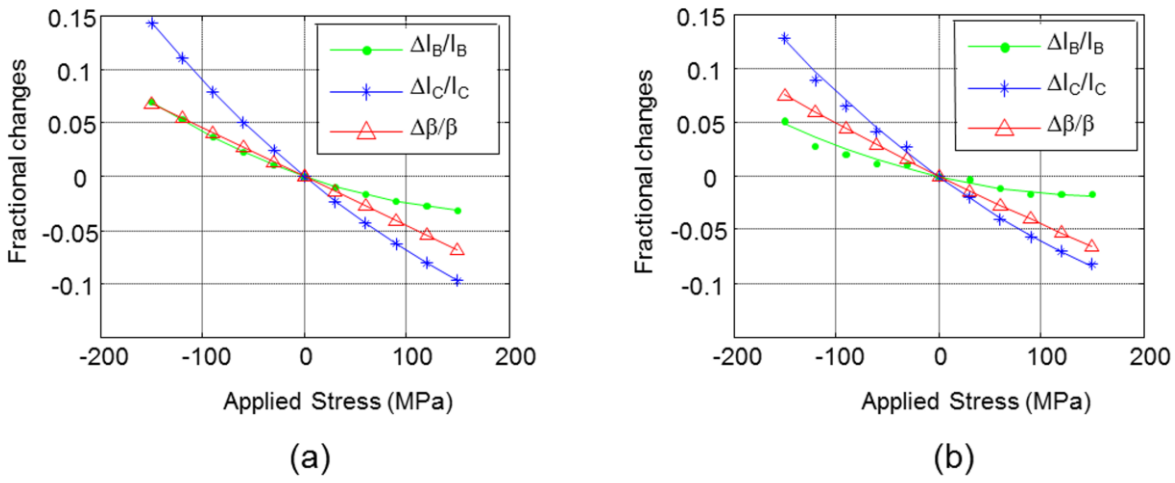


Figure 5.27 - Fractional changes in collector, base currents and current gain of an npn BJT for $\sigma'_{22}[\bar{1}10]$ (a) 1-D simulation results (Simulation was performed without the addition of residual stress, Piezoresistance coefficients are available in Table 4.8) (b) Experimental results (Data provided by S. Hussain).

As illustrated in Figure 5.27(a) and (b), the simulation and the experimental results exhibit a good match in npn transistors. For compressive stress both collector and base currents

as well as the current gain increase with stress. An 8% increase in collector current and a 5% increase in dc current gain were observed for a compressive stress of 100 MPa. As expected the changes are opposite for tensile stress.

Simulation results were compared with the expectations from the theoretical equations. As shown in Figure 5.27(a) and (b) the collector current exhibits a quadratic change in which the slope and the curvature are mainly decided by the changes in electron mobility (π_{12}^{nB}) and base intrinsic carrier concentration ($\Delta n_{iB}^2/n_{iB}^2$) respectively (see equation (3.10)). Base current component I_{BE} depends on the change in hole mobility (π_{12}^{pE}) and the change in intrinsic carrier concentration ($\Delta n_{iE}^2/n_{iE}^2$) in the emitter as in equation (3.10). The piezoresistive coefficient π_{12}^{pE} is very small. In addition, for the modern BJTs with a highly doped polysilicon emitter, a considerable portion of the holes injected into the emitter recombine in the emitter itself. Change in I_{BR} depends on the change in intrinsic carrier concentrations in the base ($\Delta n_{iB}^2/n_{iB}^2$). As a combination of all these effects, the change in base current, which is the weighted average of the change in different base current components, is negative even though the hole mobility increases with tensile stress. The $\Delta n_i^2/n_i^2$ terms in both collector and base currents cancel out in dc current gain plot, and hence almost a linear plot with a slope of -452.6/TPa is obtained in simulation results. A slight curvature observed in the experimental results (Figure 5.27(b)) may be due to a small difference between the base and emitter intrinsic carrier concentration changes under stress and/or the second-order piezoresistive correlations. Overall, these results illustrate that for the dc current gain, simulation results, experimental data and theoretical expectations show excellent match among themselves.

pnp BJT

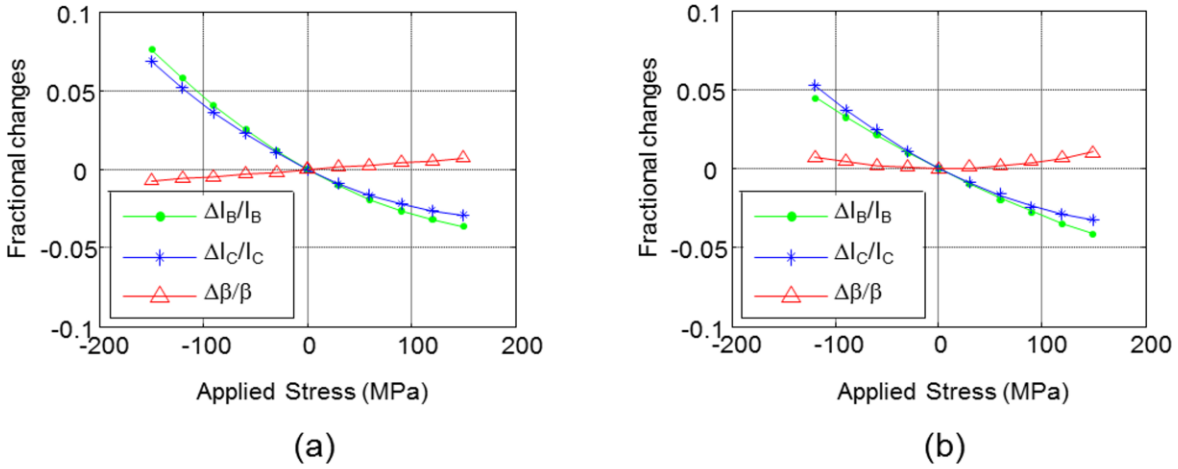


Figure 5.28 - Fractional changes in collector, base currents and current gain of a pnp BJT for $\sigma'_{22}[\bar{1}10]$ (a) 1-D simulation results (Simulation was performed without the addition of residual stress, Piezoresistance coefficients are available in Table 4.8) (b) Experimental results [83].

A similar verification was performed for pnp BJT as well. As illustrated in Figure 5.28(a) and (b), simulation and the experimental results exhibit a good match in pnp transistors. The collector current shows a good match for both tensile and compressive stresses. In addition, for tensile stress, both collector and base currents and dc current gain show matching within themselves. A slight mismatch appears in base current and current gain plots for compressive stress. This could be due to the differences in estimated parameters used in simulations and/or slight temperature changes during experiment. For transport limited pnp transistors the currents and current gain are mainly decided by the $\Delta n_i^2/n_i^2$ terms and corresponding curvature appears in the plots (Figure 5.28(b)). Our simulation result of dc current gain is comparable to that of the experimental results in [56]. These simulation results are compared to theoretical expectations, which are analogous to the theory of npn transistors. For pnp BJT the current gain showed changes for tensile stress, but the stress sensitivity of current gain is much less compared to

vertical npn transistors on (100) plane due to the corresponding low piezoresistive coefficient π_{12}^{pB} (Table 4.8). Only a 0.5% increase in current gain is achieved for a tensile stress of 100 MPa. In contrast, the base and collector currents were increased with compressive stress and showed higher sensitivity of about 4-4.5% for a compressive stress of 100 MPa.

5.8 Residual stresses in bipolar transistors

Residual stress normally develops during the fabrication process and remains in semiconductor devices [90]. Hence addition of residual stress may be essential for accurate modeling of the experimental results [100]. In order to accommodate the residual stress effects, we replaced stress σ in the equations in Table 2.3 with the sum of applied stress σ and residual stress σ_0 and used in our modeling (Table 5.1). Residual stress may vary depending on the details of the fabrication process. In order to study the residual stress in transistors, experimental results of npn and pnp transistors were tested with matching simulation results.

Table 5.1 – Stress induced changes in $\Delta n_i^2/n_i^2$ (including residual stress)

Stress Orientation	$\Delta n_i^2/n_i^2$
<100>	$1.644\text{x}10^{-6}(\sigma+\sigma_0)^2-2.755\text{x}10^{-4}(\sigma+\sigma_0)$
<110>	$8.873\text{x}10^{-7}(\sigma+\sigma_0)^2-3.403\text{x}10^{-4}(\sigma+\sigma_0)$

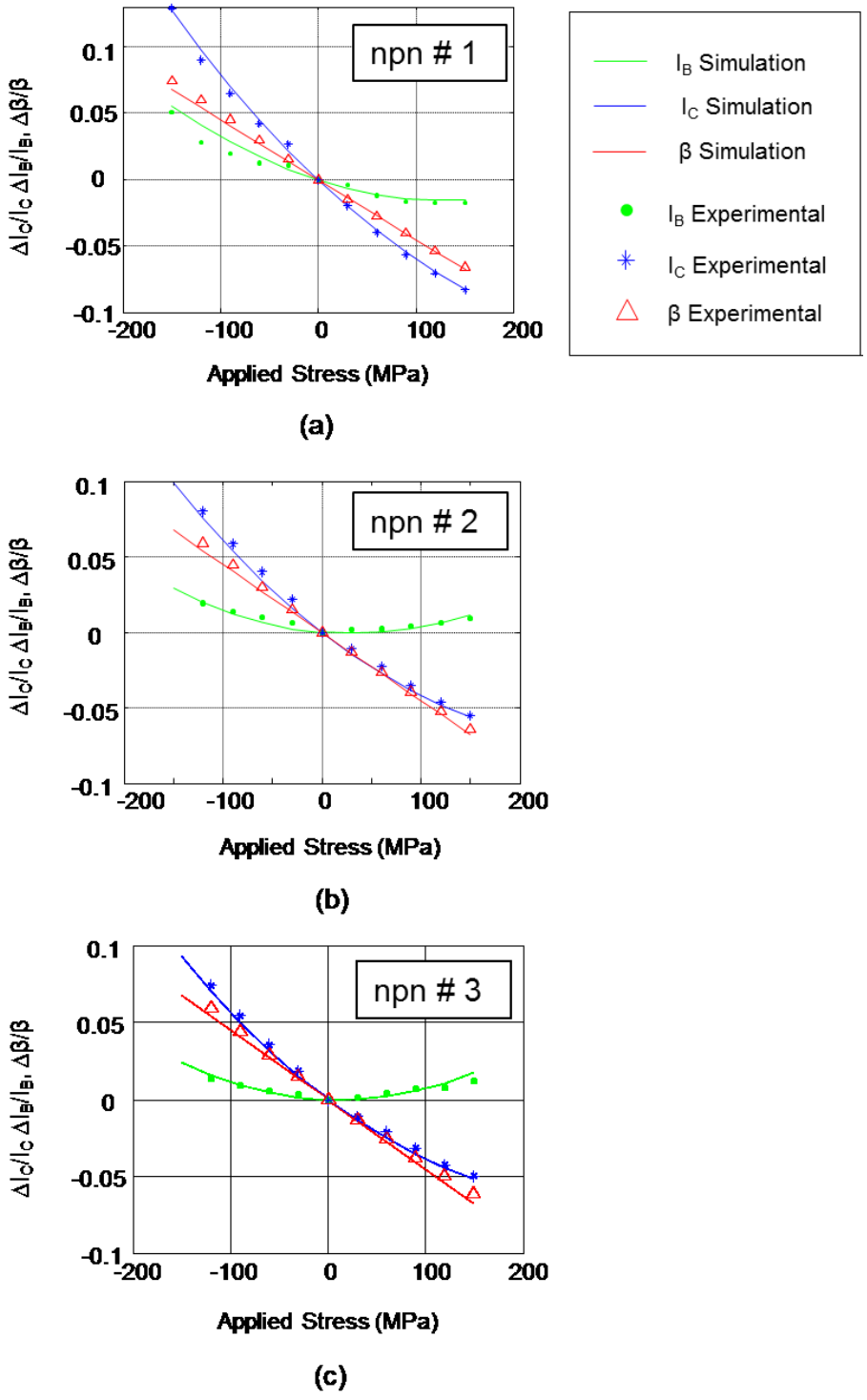


Figure 5.29 - Comparison of experimental and simulation results for different npn BJTs with same profile in similar/same strips (π_{12}^{n} = 455/TPa, π_{12}^{p} = -8/TPa) (a) residual = +70 MPa (b) residual stress = +160 MPa (c) residual stress = +180 MPa. Residual stresses were added in simulation to match the experimental results. Experimental data were provided by S. Hussain [83].

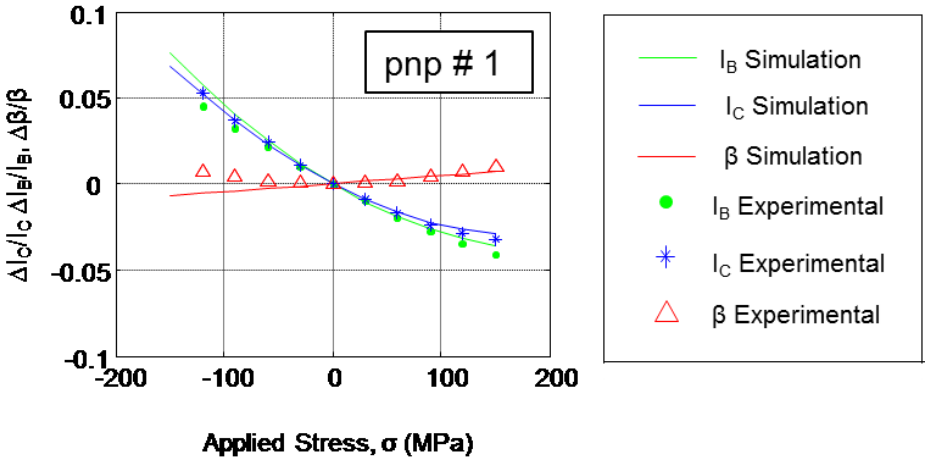


Figure 5.30 - Comparison of experimental and simulation results for pnp BJT in similar/same strips (π_{12}^{n} = 200/TPa, π_{12}^{p} = -15/TPa). Simulation and experimental results matched without adding any residual stress. Experimental data were provided by S. Hussain [83].

The vertical npn and pnp transistors used in this study are from a complementary bipolar technology fabricated using a 0.5 µm BiCMOS process with shallow trench isolation. All transistors are from similar or same wafer strips. The npn transistors incorporate polysilicon emitters while pnp transistors do not. All npn transistors are with same profiles. But the locations of the transistors in the wafer strip are different. Same estimated piezoresistance coefficients were used in simulation (Table 4.8). Figures 5.29 and 5.30 depict the experimental results of three npn transistors and a pnp transistor, respectively, with matching simulation results. As shown in Figure 5.29 the experimental results of 3 different npn transistors (npn #1, npn #2 and npn #3) were matched for different residual stresses of +70 MPa, +160 MPa and +180 MPa, respectively. This indicates the presence of residual stress in the npn transistors. The magnitudes of the residual stresses in different transistors were successfully quantified with this 1-D model. Experiment result of pnp transistor matched with the simulation result without the addition of any residual stress.

Residual stresses observed in the base and emitter regions of the npn transistors may be possibly due to the polysilicon emitter structures. In contrast, zero built-in stress has been found in both emitter and base regions of the pnp transistor. The estimated stress levels correspond to the sum of the two normal stresses ($\sigma_{11} + \sigma_{22}$) on the (100) surface. It appears that the deformation potentials of silicon may be affected by high levels of doping in the emitters of the transistors. Another possibility for the residual stress is due to the shallow trench isolation. Residual stress due to shallow trench isolation is location dependent. Since slightly different residual stresses were observed for the transistors with same profiles in same or similar strips this is also a possibility.

5.9 Stress effects in saturation current for vertical and lateral transistors in (100) plane

The saturation current of a bipolar transistor changes when a mechanical stress is applied. The change can be positive or negative, depending on the minority carrier type, current orientation, stress orientation, type of the stress and the sign of the stress [57]. The simulated results of change in saturation current for npn and pnp transistors for various current and stress orientations are presented in Figure 5.31. The figures shows a strong anisotropic behavior depending on the current and stress orientations. In addition, the responses are much different for npn and pnp transistors. The results are very similar to the change in resistor current where the resistor length is replaced by the base width and the majority carrier concentration is replaced by the minority carrier concentration [57]. In addition a curvature is added to all these plots due to the change in intrinsic carrier concentration. The changes can be fitted with second-order least square fits as shown in the figures. The changes in current are in the same order of magnitude as the piezoresistive effect in the stress range considered.

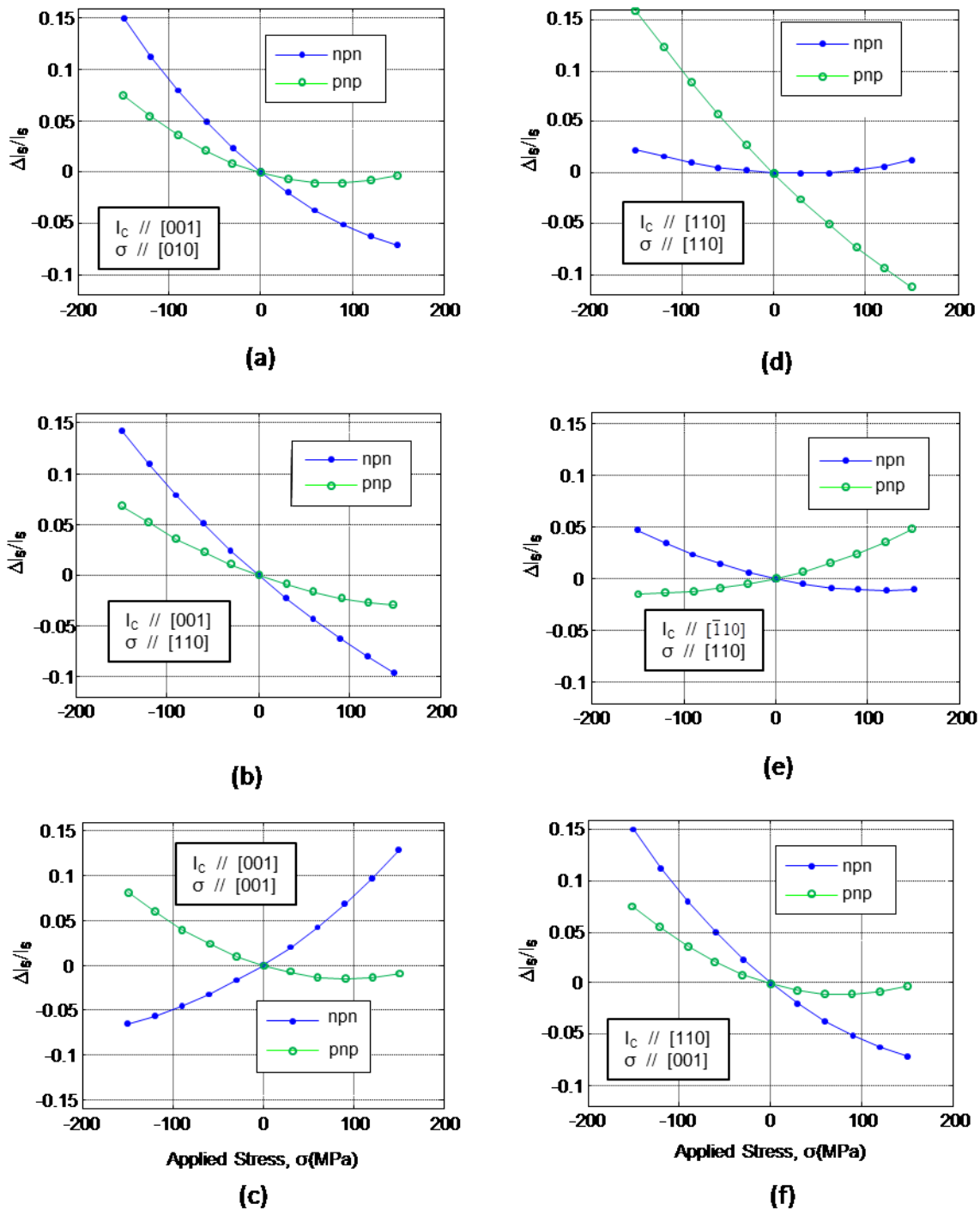


Figure 5.31 - Simulated changes in saturation current for npn and pnp transistors as a function of uniaxial normal stress for various current and stress orientations

Vertical transistors

Figure 5.31(a)-(c) are the stress responses for npn and pnp vertical transistors on (100) plane. Figure 5.31 (a) and (b) are the response for in-plane normal stresses and Figure 5.31(c) is the response for the out-of plane normal stress. It has been reported that the stress sensitivity to vertical transistors is unique when they are fabricated in (100) or (111) planes [57]. That is the first-order stress sensitivity to in-plane normal stress is isotropic for the vertical transistors in these planes. This implies that the sensitivity is independent of the angle of the uniaxial stress in the plane. Our simulation results also confirmed this nature. However there is some anisotropic behavior appears in figures because of the second-order terms due to the change in intrinsic carrier concentration which is slightly anisotropic depending on the stress orientation with respect to the crystal orientation. Vertical pnp transistors are showing much less stress sensitivity compared to vertical npn transistors for in-plane normal stresses and out-of-plane tensile stress for the considered stress range. For pnp transistors, the change in current for both in-plane and out-of-plane normal stresses are much similar for this stress range.

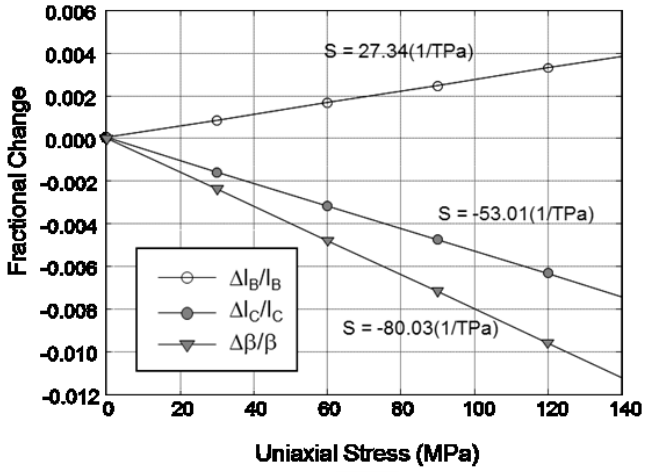
Lateral transistors

The stress sensitivity of lateral transistors on (100) is very anisotropic. This property can be used to select the transistor orientation for specific needs. The graphical representation of piezoresistive coefficients by Kanda [74] is a very good reference for deciding the transistor orientation for lateral transistors. Figures 5.31(d) and (e) show the longitudinal and transverse stress sensitivity of npn and pnp lateral transistors on (100) plane. The stress sensitivities to in-plane longitudinal and transverse stresses are less for npn transistor as shown in figures corresponding to the lateral and transverse piezoresistive coefficients for the transistors in <110>

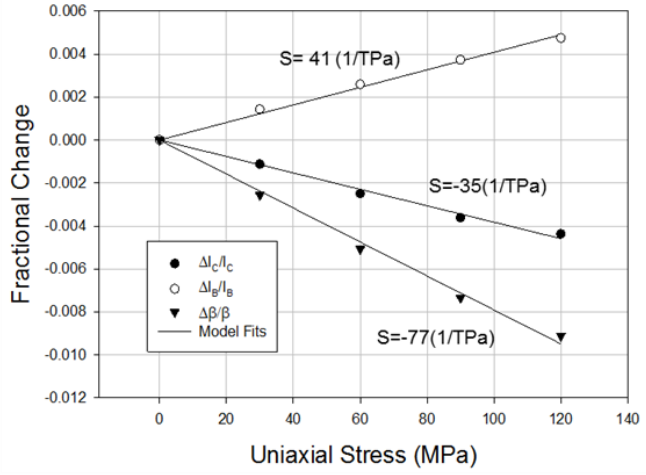
directions in (100) plane (Appendix D Figure D.1). For pnp transistors, longitudinal stress sensitivity is very high for <110> directions (Figure 5.31(d)), whereas the transverse sensitivity is also considerably high (Figure 5.31(e)) and having opposite polarities of changes corresponding to the longitudinal and transverse piezoresistive coefficients. However, the stress sensitivity is zero near the <100> directions (Appendix D Figure D.2). These are similar to the case of p-type resistors.

5.10 Stress effects in bipolar transistors on (111) plane

Fractional changes in currents and dc currents gain for an npn transistor on (111) plane for an in-plane normal stress are illustrated in Figure 5.32(a). Same npn transistor model used for (100) plane in previous section was used changing the current orientation in (111) direction. Simulation was carried out with the piezoresistance mobility model only. (More appropriate simulation should include the changes in intrinsic carrier concentration as well. It is expected to give slight curvature in the current plots while keeping the dc current gain plot same). The simulation results for in-plane normal stress in different orientation gave the same results indicated the isotropic nature for in-plane stresses for vertical transistor in (111) plane. The experimental results of [83] also validating this simulation results presented here for comparison (Figure 5.32(b)). The change rates of collector current (-53.01/TPa) and dc current gain (-80.03/TPa) are much less compared to npn transistor on (100) plane where the corresponding changes were about -450/TPa for both collector current and dc current gain. This indicate that the sensitivity of npn transistors on (111) plane are much less compared to the sensitivity of npn transistors on (100) plane for in-plane normal stress.



(a)



(b)

Figure 5.32 - Fractional changes in currents and current gain of a vertical npn transistor on (111) plane for an in-plane normal stress $\sigma[\bar{1}10]$ (a) simulation results (b) experimental results (Experimental data were provided by S. Hussain [83].

5.11 Summary

A 1-D numerical model was developed for rapid stress analysis in bipolar transistors. The simulation is very fast and results for a given stress orientation are obtained in less than a minute. Importantly, these simulation results are comparable to the results of a 2-D model with Sentaurus TCAD tool, which usually takes hours on a similar CPU when similar accuracy is needed. The

validity of the model was verified for npn and pnp transistors and found to be consistent with the experimental results and the theoretical expectations. With the use of appropriate parameters this model can be used for any npn/pnp vertical or lateral transistor irrespective of the transistor plane or orientation. This model was successfully used to quantify the residual stress in bipolar transistors. The sensitivity of transistors on (100) plane for different current-stress orientations were obtained from simulation and analyzed. Transistors showed different sensitivity for different current-stress orientations. The vertical transistors on (100) and (111) planes showed almost isotropic changes for in-plane normal stress. In vertical transistors, npn transistor on (100) plane showed much higher stress sensitivity than the pnp transistors on (100) plane or npn transistor on (111) plane. Lateral pnp transistors on (100) plane showed much higher anisotropic stress sensitivity with opposite polarities for longitudinal and transverse stresses. Overall, this study indicates an opportunity for performance enhancement or stress mitigation by selecting appropriate combination of current-stress orientation in various transistor structures. A detail analysis on the performance enhancement in vertical and lateral transistors is given the next section.

CHAPTER 6

PERFORMANCE ENHANCEMENT IN BIPOLAR TRANSISTORS ON (100) PLANE USING UNIAXIAL STRESS

6.1 Introduction

In this study the performance enhancement in npn and pnp BJTs on (100) silicon was investigated using uniaxial stress. Experimental results of in-plane normal stress for vertical npn and pnp transistors on (100) plane were analyzed with the help of the 1-D numerical model. Numerical modeling was used to predict and analyze the stress effects for various current-stress orientations in vertical and lateral transistors. By studying the stress induced effects in various parameters of bipolar transistors for different stress-current orientations potential opportunities for strain engineering in npn and pnp bipolar transistors were explored.

6.2 Vertical transistors on (100) plane

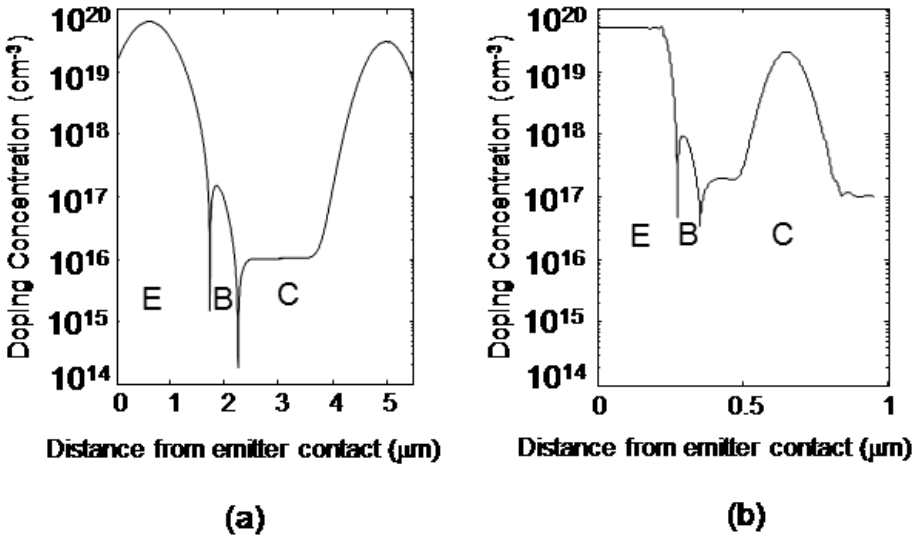


Figure 6.1 - Doping profiles used for simulations (a) profile 1 and (b) profile 2.

Stress induced changes in dc and rf (radio-frequency) characteristics were analyzed. dc analysis was performed on profile 1 using the 1-D numerical model developed in previous chapter and the rf analysis was performed on profiles 1 and 2 with the 2-D Sentaurus model developed in Chapter 4 (Figure 6.1). The piezoresistance coefficients of profiles were calculated based on the average base and emitter doping concentrations of the profiles and provided in Table 6.1.

Table 6.1 - Piezoresistive coefficient estimates for vertical BJTs on (100) plane

Coefficient (10^{-12} Pa^{-1})	npn profile 1 ($N_B = 2x10^{17}/cm^3$, $N_E = 3x10^{19}/cm^3$)		npn profile 2 ($N_B = 8x10^{17}/cm^3$, $N_E = 5x10^{19}/cm^3$)	
	π^{nB}	π^{pE}	π^{nB}	π^{pE}
π_{11}	-900	25	-850	+20
π_{12}	455	-8	420	-8
π_{44}	-150	700	-140	690

6.2.1 dc characteristics

6.2.1.1 Modeling for dc analysis (with Matlab)

Doping profile shown in Figure 6.1(a) was used for dc analysis for which doping types were interchanged for npn and pnp BJTs. Standard models were included to represent the different device physics phenomena such as the carrier transport, doping-dependent mobility, velocity saturation, bandgap narrowing and Shockley–Read–Hall (SRH) recombination. For both

carriers, minority-carrier lifetimes of 10^{-7}s and 10^{-8}s were assumed for the base and emitter respectively.

6.2.1.2 Theoretical expectations (extended theory)

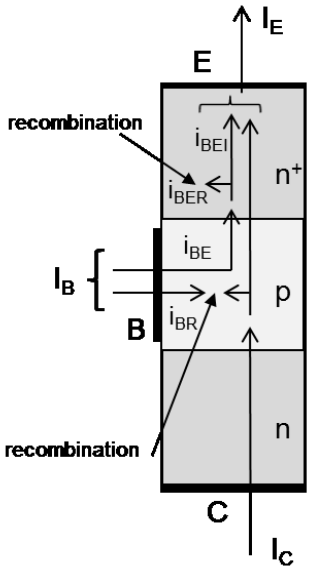


Figure 6.2 - Simplified block model of a vertical npn BJT showing the current components. E-emitter, B-base, C-collector

The theory given in Chapter 3 is slightly extended by dividing the base current component in emitter I_{BE} into two parts to have a more detailed analysis. The 1-D transistor model shown in Figure 6.2 illustrates the main current components in an npn transistor. These include collector current I_C and the two important base current terms: I_{BE} representing the back injection into the emitter, and I_{BR} representing recombination in the base. For modern BJTs with a highly-doped polysilicon emitter, a considerable portion of the holes injected into the emitter recombine in the emitter itself. Hence, the base current component I_{BE} is divided into two parts: the back injected base current component that does not recombine in the emitter I_{BEI} and the back injected base current component that recombines in the emitter I_{BER}.

Changes in current components

Using traditional bipolar transistor theory, the important current components of an npn BJT can be represented as follows:

$$I_C = V_T \frac{qA_B}{G_B} \mu_{nB} n_{iB}^2 \tag{6.1}$$

$$I_{BEI} = V_T \frac{qA_E}{G_E} \mu_{pE} n_{iE}^2 \tag{6.2}$$

$$I_{BER} \propto \frac{n_{iE}^2}{\tau_{pE}} \text{ and} \tag{6.3}$$

$$I_{BR} \propto \frac{n_{iB}^2}{\tau_{nB}} \tag{6.4}$$

where q is the electric charge, V_T is the thermal voltage, τ_{nB} is the minority-carrier lifetime of electrons in the base and τ_{pE} is the minority-carrier lifetime of holes in the emitter. G_B and G_E represent the Gummel numbers in the base and emitter, A_E and A_B are the emitter and base areas, μ_{nB} and μ_{pE} are the effective minority-carrier mobility in the base and emitter and n_{iB} and n_{iE} are the intrinsic carrier concentrations in the base and emitter respectively. Based on equations (6.1-6.4), the normalized changes in the collector current I_C and base current components I_{BEI}, I_{BER} and I_{BR} for an npn BJT on (100) plane can be written as:

$$\frac{\Delta I_C}{I_C} = \frac{\Delta \mu_{nB}}{\mu_{nB}} + \frac{\Delta n_{iB}^2}{n_{iB}^2} \tag{6.5}$$

$$\frac{\Delta I_C}{I_C} = -\pi_{12}^{nB}\left(\sigma'_{11} + \sigma'_{22}\right) - \pi_{11}^{nB}\sigma'_{33} + \frac{\Delta n_{iB}^2}{n_{iB}^2} \tag{6.6}$$

$$\frac{\Delta I_{BEI}}{I_{BEI}} = \frac{\Delta \mu_{pE}}{\mu_{pE}} + \frac{\Delta n_{iE}^2}{n_{iE}^2} \tag{6.7}$$

$$\frac{\Delta I_{BEI}}{I_{BEI}} = -\pi_{12}^{pE}\left(\sigma'_{11}+\sigma'_{22}\right) - \pi_{11}^{pE}\sigma'_{33} + \frac{\Delta n_{iE}^2}{n_{iE}^2} \tag{6.8}$$

$$\frac{\Delta I_{BER}}{I_{BER}} = \frac{\Delta n_{iE}^2}{n_{iE}^2} - \frac{\Delta \tau_{pE}}{\tau_{pE}} \cong \frac{\Delta n_{iE}^2}{n_{iE}^2} \tag{6.9}$$

$$\frac{\Delta I_{BR}}{I_{BR}} = \frac{\Delta n_{iB}^2}{n_{iB}^2} - \frac{\Delta \tau_{nB}}{\tau_{nB}} \cong \frac{\Delta n_{iB}^2}{n_{iB}^2} \tag{6.10}$$

in which the lifetimes are assumed independent of stress. Total base current (I_B) is the sum of above three base current components and given as:

$$I_B = I_{BEI} + I_{BER} + I_{BR} \tag{6.11}$$

The change in base current is the weighted sum of the changes in different base current components:

$$\frac{\Delta I_B}{I_B} = \delta_1 \frac{\Delta I_{BEI}}{I_{BEI}} + \delta_2 \frac{\Delta I_{BER}}{I_{BER}} + \delta_3 \frac{\Delta I_{BR}}{I_{BR}} \tag{6.12}$$

where δ_1, δ_2, δ_3 are the fraction of contributions from different base current components given as:

$$\delta_1 = \frac{I_{BEI}}{I_B}, \quad \delta_2 = \frac{I_{BER}}{I_B}, \quad \delta_3 = \frac{I_{BR}}{I_B} \quad \text{and}$$

$$\delta_1 + \delta_2 + \delta_3 = 1$$

Changes in dc current gain

The stress-induced change in the dc current gain ($\beta = I_C/I_B$) in terms of back injection limited component β_γ and transport limited component $\beta_{T'}$ for both npn and pnp BJTs can be expressed as:

$$\beta = \frac{I_C}{I_{BE} + I_{BR}} = \frac{1}{\frac{I_{BE}}{I_C} + \frac{I_{BR}}{I_C}} = \frac{1}{\frac{1}{\beta_\gamma} + \frac{1}{\beta_{T'}}} \tag{6.13}$$

$$\beta = \frac{\beta_{T'}\beta_{\gamma}}{\beta_{\gamma} + \beta_{T'}} \tag{6.14}$$

$$\frac{\Delta\beta}{\beta} = \left(\frac{\beta_{T'}}{\beta_{\gamma} + \beta_{T'}}\right)\frac{\Delta\beta_{\gamma}}{\beta_{\gamma}} + \left(\frac{\beta_{\gamma}}{\beta_{\gamma} + \beta_{T'}}\right)\frac{\Delta\beta_{T'}}{\beta_{T'}}$$

$$\frac{\Delta\beta}{\beta} = \delta\frac{\Delta\beta_{\gamma}}{\beta_{\gamma}} + (1-\delta)\frac{\Delta\beta_{T'}}{\beta_{T'}} \tag{6.15}$$

$$\text{where } \delta = \frac{\beta_{T'}}{\beta_{\gamma} + \beta_{T'}} \leq 1 \text{ and } \frac{\beta_{\gamma}}{\beta_{\gamma} + \beta_{T'}} \leq 1 \tag{6.16}$$

Parameter $\delta = \delta_1 + \delta_2$ represents the fraction of current gain that is determined by back injection into the emitter. $\delta = 1$ and $\delta = 0$ represent 100% back injection and 100% base recombination, respectively.

6.2.1.3 Understanding the impact of in-plane normal stress on vertical transistors on (100) plane

Figure 6.3 illustrates portions of Gummel plots for an npn and a pnp BJT for tensile stress, σ'_{22}. The tested npn and pnp BJTs had current gains of approximately 200 and 80, respectively. In addition the ideality factors (n) of 1.04 (npn) and 1.07 (pnp) for collector current in the normal operation range of base-emitter voltage ($0.65 \leq V_{BE} \leq 0.8$) indicate that the tested BJTs are injection limited structures. As indicated in Figure 6.3, both I_C and I_B are reduced with in-plane normal tensile stress for both npn and pnp BJTs, whereas β is reduced for the npn BJT but increased for the pnp. These experimental results are discussed in detail in terms of the 1-D model below.

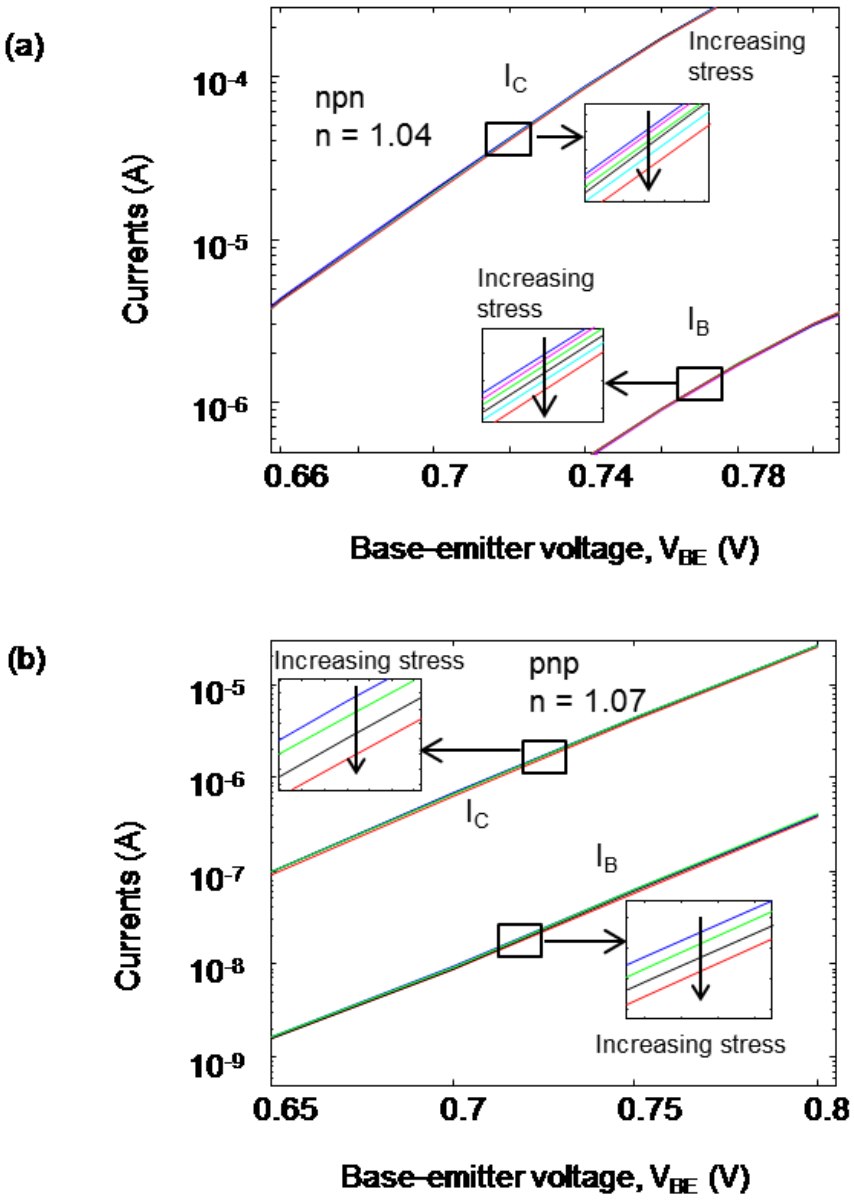


Figure 6.3 - Experimental results of Gummel plots for in-plane tensile stress, $\boldsymbol{\sigma'_{22}}$ $[\bar{\mathbf{1}}\mathbf{10}]$, (a) for an npn BJT and (b) a pnp BJT. The ideality factor (n) of collector current for the plotted V_{BE} range is indicated. $\beta_{npn} \cong 200$, $\beta_{pnp} \cong 80$ corresponding well with the ratio of estimated mobility in the npn and pnp base regions.

npn transistor

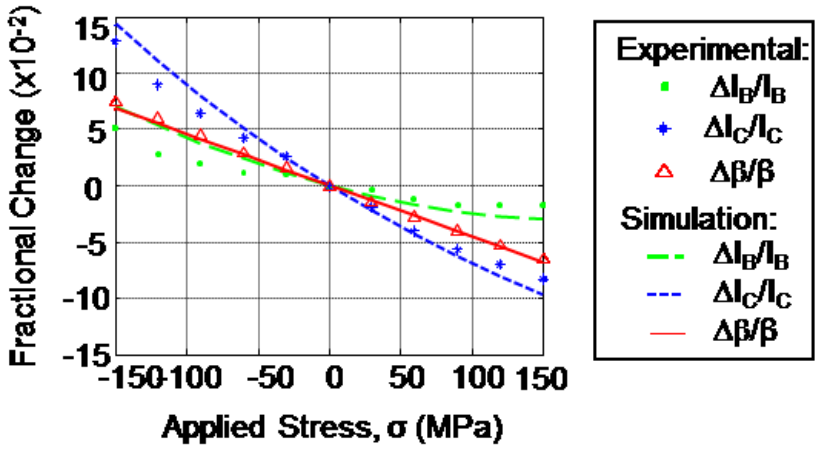


Figure 6.4 - Comparison of experimental and simulated fractional changes in I_C, I_B and β of an npn BJT for σ [$\bar{1}$10]. Simulation was performed without adding any residual stress ($\sigma_0 = 0$). Piezoresistance coefficients are in Table 6.1. Experimental data were provided by S. Hussain.

Figure 6.4 presents experimental results and simulations for changes in I_C, I_B and β without the presence of residual stress ($\sigma_0 = 0$). The agreement for β is excellent whereas clear mismatches exist for the individual current plots. The differences in these plots are attributed to the presence of residual stress.

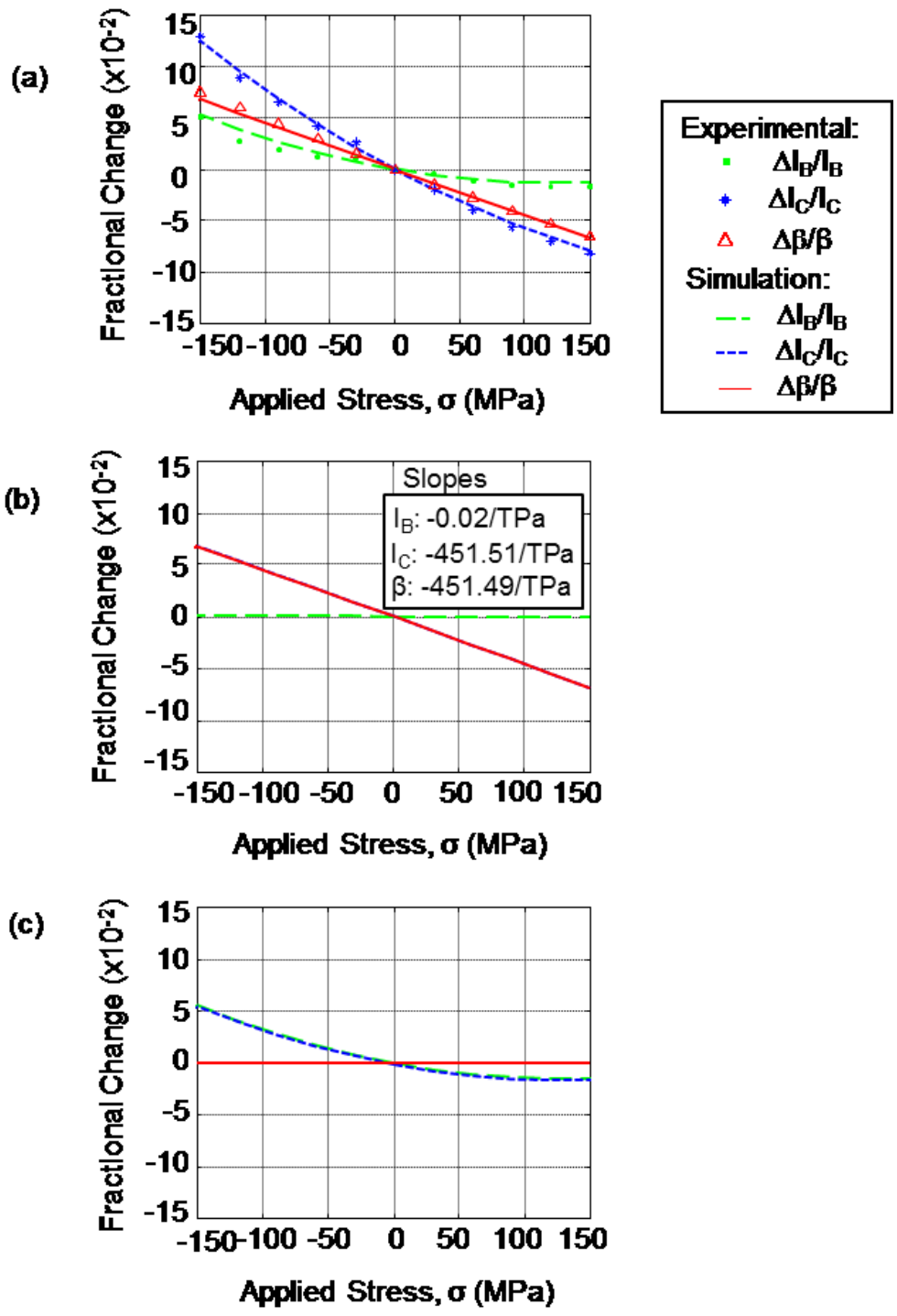


Figure 6.5 - Fractional changes in I_C, I_B and β for an npn BJT for σ'_{22} $[\bar{1}10]$. Residual stress of +70 MPa was added in simulations to match the experimental results (a) comparison with the experimental results (both piezoresistance mobility model and the deformation potential models are included for simulation) (b) simulation with piezoresistance mobility model only (plots of I_C and β overlap) (c) simulation with deformation potential model only (plots of I_C and I_B overlap). Piezoresistance coefficients are in Table 6.1. Experimental data were provided by S. Hussain.

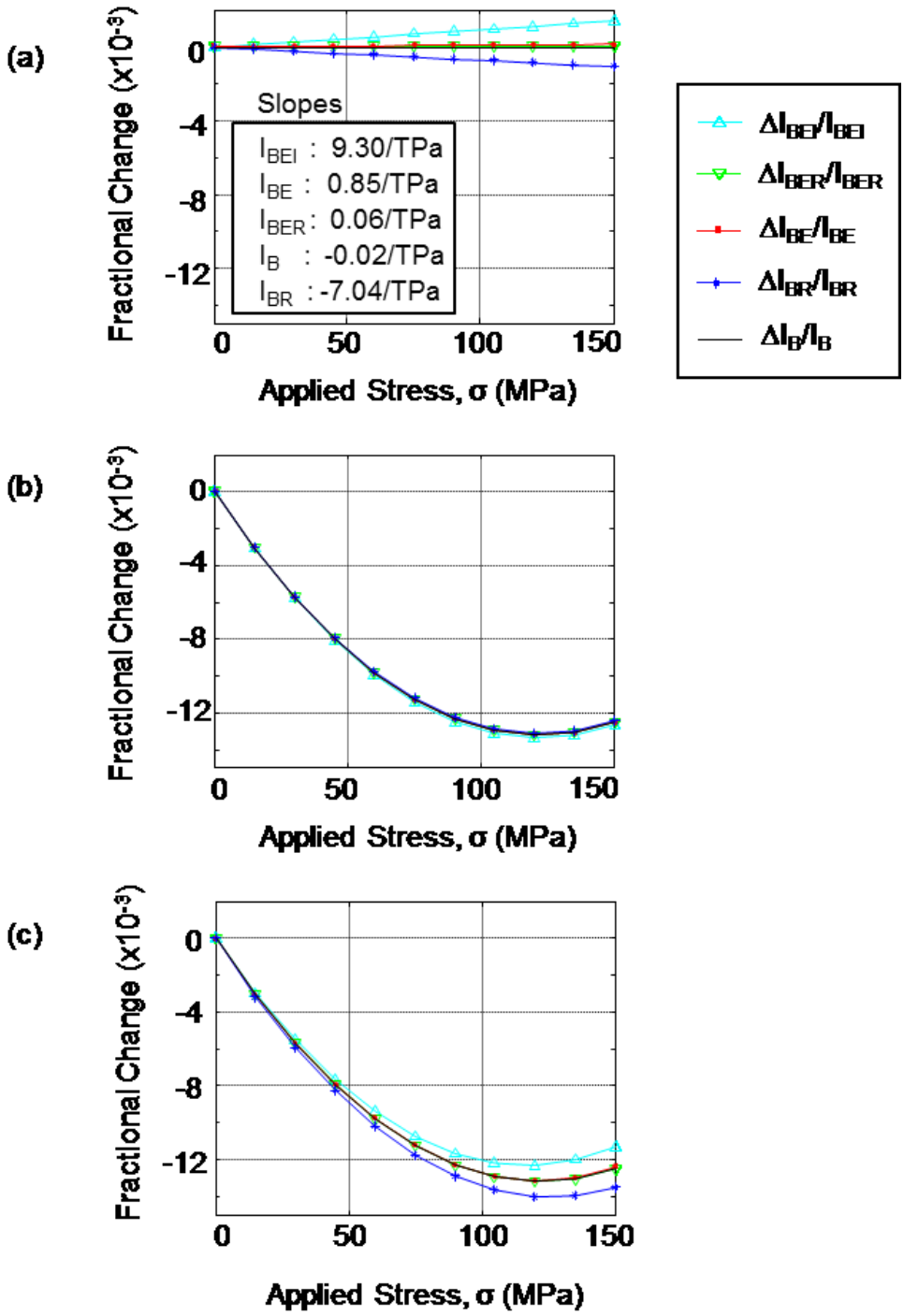


Figure 6.6 - Simulated fractional changes in base current components of an npn BJT for tensile stress. (a) with piezoresistance mobility model only; (b) with deformation potential model only; (c) with both models together. $\delta_1 = 0.08$, $\delta_2 = 0.82$ and $\delta_3 = 0.10$ in simulations.

Figure 6.5(a) presents experimental results and simulations for changes in I_C, I_B and β without the presence of residual stress ($\sigma_0 = 0$ in simulation) of an npn BJT. Both piezoresistance mobility model and the deformation potential models are included for simulation. The agreement for β is excellent whereas clear mismatches exist for the individual current plots. The differences in these plots are attributed to the presence of residual stress. Figure 6.5(a) exhibits the best[1] match obtained by adding a +70 MPa ($\sigma_0 = +70$ MPa) built-in stress to the simulation model including both stress models together. To distinguish the individual contributions of changes in mobility and intrinsic carrier concentration, simulation results were obtained by separately applying the piezoresistance mobility model and the deformation potential model (shown in Figure 6.5(b) and 6.5(c) respectively). As illustrated in Figure 6.5(a), I_C, I_B and β showed the largest changes for compressive stress. A 12.5% increase in I_C and a 7% increase in β were observed for a compressive stress of 150 MPa. As expected the changes were opposite for tensile stress. Figs. 6.5(b) and 4(c) show that I_C is significantly influenced by the change in electron mobility (π_{12}^{nB}) as well as the change in the intrinsic carrier concentration ($\Delta n_{iB}^2/n_{iB}^2$). For compressive stress a strong increase in I_C occurs since the effects of mobility changes and the intrinsic carrier concentration changes are almost the same.

Figures 6.6(a) and (b) show the detailed changes in different base current components due to the stress-induced changes in mobility and changes in intrinsic carrier concentration, respectively. Figures 6.6(c) is the simulation results with both models together. In Figure 6.6(a), I_{BEI} shows a linear increase corresponding to the change in hole mobility (π_{12}^{pE}). I_{BER} partially depends on the hole mobility. However, the change in hole mobility is very low. Hence the change in I_{BER} is almost zero in Figure 6.6(a). I_{BR} depends on the change in electron mobility to a

[1] in the least-square sense

lesser extent. Since the electron mobility decreases with stress the base recombination was also slightly reduced (as the electron supply rate is reduced) as shown by the negative slope for I_{BR} (Figure 6.6(a)). Even though this is a back injection limited structure ($\delta = 0.9$, $\beta_\gamma = 306$, $\beta_{T'} = 2589$ and $\beta = 274$ in simulation) most of the injected holes recombine in the emitter ($\delta_1 = 0.08$, $\delta_2 = 0.82$). Hence, the resultant slope of I_B is mainly decided by the change in I_{BER} and the slope is almost zero as depicted in Figure 6.6(a). Change in intrinsic carrier concentration affects all base current components equally as shown in Figure 6.6(b) and this effect is much higher compared to the changes due to mobility. Thus the total change in base current is mainly determined by the changes in intrinsic carrier concentration as shown in Figure 6.6.

In simulations, the $\Delta n_i^2/n_i^2$ term in both the $\Delta I_C/I_C$ and $\Delta I_B/I_B$ cancel out in the $\Delta\beta/\beta$ plot, and hence almost a linear relationship (Figure 6.5(a)) with a slope of -451.5/TPa was obtained. A slight curvature observed in the experimental results (red triangles in Figure 6.5(a)) may be due to the difference between the base and emitter intrinsic carrier concentrations, slight temperature drift and/or second-order piezoresistive correlations.

pnp transistor

Similar analyses were performed for the pnp BJT. As depicted in Figure 6.7(a) the experimental results and the simulated results (with both models) showed good matches without adding any residual stress. The I_C shows a good match for both tensile and compressive stresses. A slight mismatch appears for compressive stress. This could arise from slight differences in the deformation potentials in the base and emitter or due to a small temperature drift during experiments. Simulation results for β are comparable to that of the experimental results in [56].

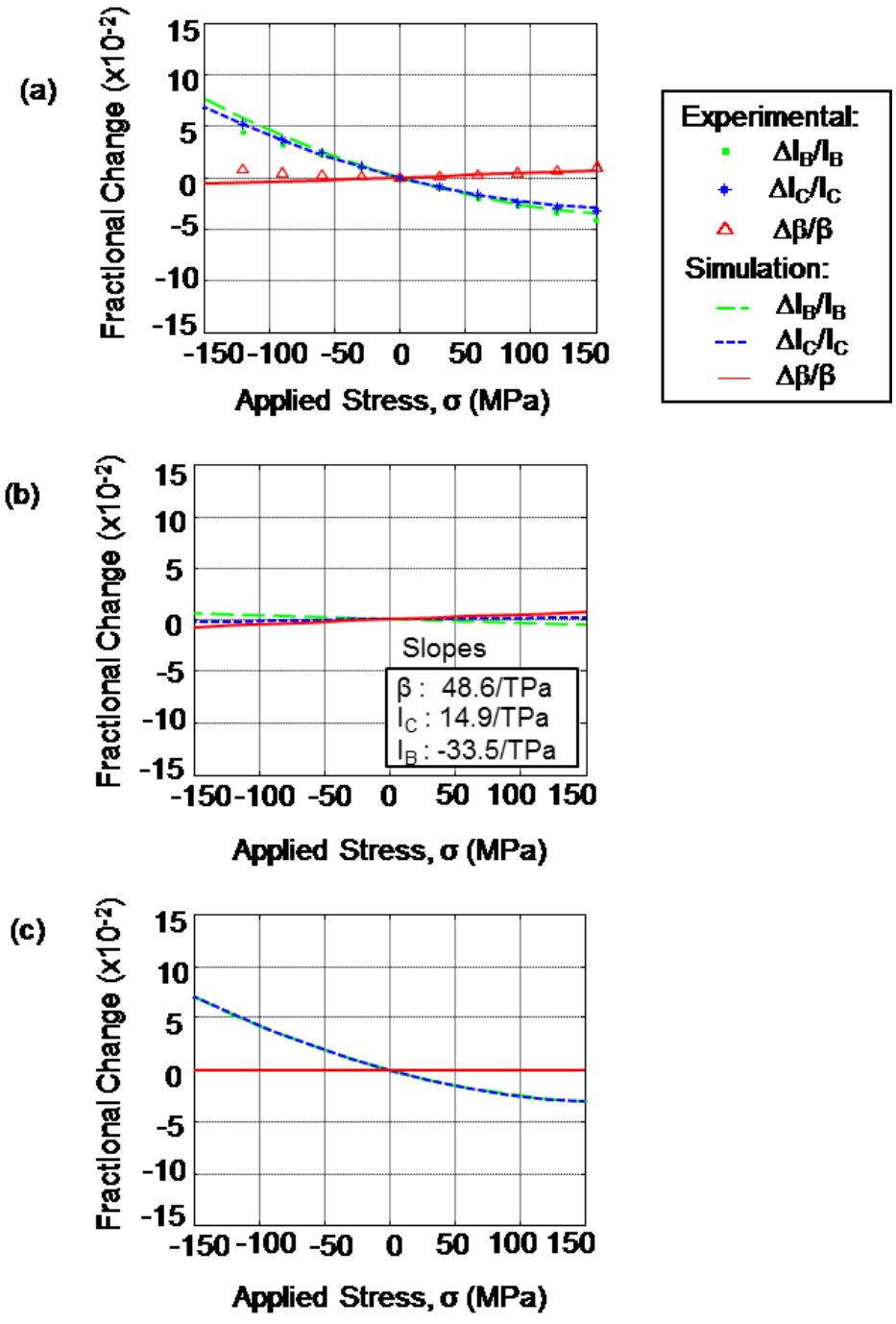


Figure 6.7 - Fractional changes in I_C, I_B and β for a pnp BJT for σ'_{22} [$\bar{1}10$]. No residual stress added (a) comparison with the experimental results (both stress models are included for simulation) (b) simulation with piezoresistance mobility model only (c) simulation with deformation potential model only (plots of I_C and I_B overlap). Piezoresistance coefficients are in Table 6.1. Experimental data were provide by S. Hussain [83].

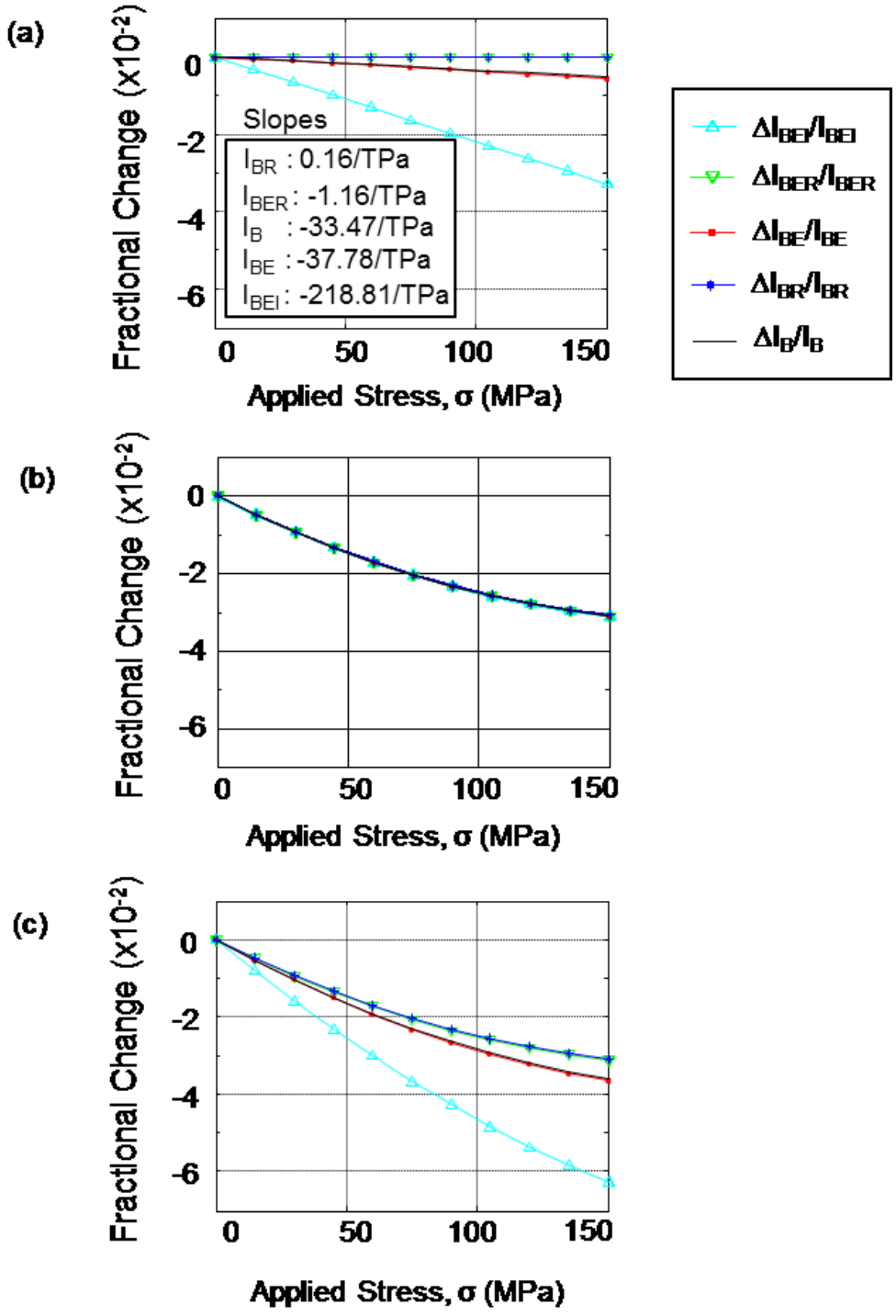


Figure 6.8 - Simulated fractional changes in base current components of a pnp BJT for tensile stress (a) with piezoresistance mobility model only (b) with deformation potential model only (all plots overlap) (c) with both models together. Simulations yields $\delta_1 = 0.15$, $\delta_2 = 0.74$ and $\delta_3 = 0.11$.

Separate simulations were performed with piezoresistance mobility model and with deformation potential model and the results are shown in Figure 6.7(b) and 6.7(c), respectively. In Figure 6.7(b) the collector current shows a slope of +14.9/TPa corresponding to π_{12}^{pB}. However, the change in intrinsic carrier concentration highly influences the changes in collector current as shown in Figure 6.7(c). As a result quadratic change with a negative slope was obtained as depicted in Figure 6.7(a). As mentioned earlier, base current is the weighted average of the injection limited and recombination limited components (δ_1 = 0.15, δ_2 = 0.74 and δ_3 = 0.11 in simulation). For base current, a resultant slope of -33.5/TPa was observed due to the changes in mobility (Figure 6.8(a)). Base current is also greatly influenced by changes in intrinsic carrier concentrations (Figure 6.8(b)). When change in base current is subtracted from the change in collector current a slope with a value of 48.6/TPa is obtained for dc current gain (Figure 6.7(b), δ = 0.89, β_γ = 149, $\beta_{T'}$ = 1168 and β = 132 in simulation). The changes in currents are mainly due to the changes in intrinsic carrier concentrations. Conversely, the $\Delta n_i^2/n_i^2$ terms in both I_C and I_B cancel out in the β plot and give almost a linear variation in simulation (Figure 6.7(a)). However, experimental results showed a slight curvature for β. In transistors, $\Delta n_i^2/n_i^2$ values of emitter and base may vary due to band gap narrowing and deformation potential differences in the emitter. These variations may result in considerable curvature in dc current gain plot as shown in experimental results (Figure 6.7(a)). In addition, small temperature drift or base resistance changes also may be the reason for the curvature in the experimental results.

Differences in stress sensitivity for injection limited and recombination limited structures

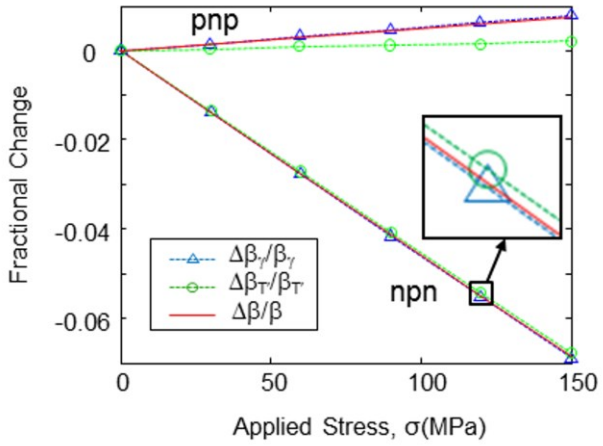


Figure 6.9 - Simulated fractional changes in injection limited and transport limited current gain components of an npn and a pnp BJTs.

Our analysis for different npn and pnp BJT structures indicates that the injection limited BJTs are more sensitive to stress than the transport limited structures. This notion is supported by the larger slope for change in injection limited current gain for both npn and pnp BJTs (Figure 6.9). Further affirmation is provided by the higher slope of I_{BEI} compared to I_{BER} or I_{BR} for both npn and pnp BJTs (Figure 6.6(a) and Figure 6.8(a)). However, since a major portion of minority-carriers injected into the emitter recombines in the emitter itself, the favorable mobility increment using injection limited structures can only be partially achieved.

6.2.1.4 Analysis of impact of in-plane and out-of-plane normal stresses

The stress sensitivity of collector and base currents and dc current gain of vertical transistors are illustrated in Figure 6.10. Response of an npn transistor for in-plane normal stresses in two different orientations are shown in Figure 6.10(a) and 6.10(b). The response for the out-of-plane normal stress is illustrated in Figure 6.10(c). Similarly responses of a pnp

transistor for in-plane normal stresses are shown in Figure 6.10(d) and 6.10(e) and the response of out-of-plane normal stress is illustrated in Figure 6.10(f).

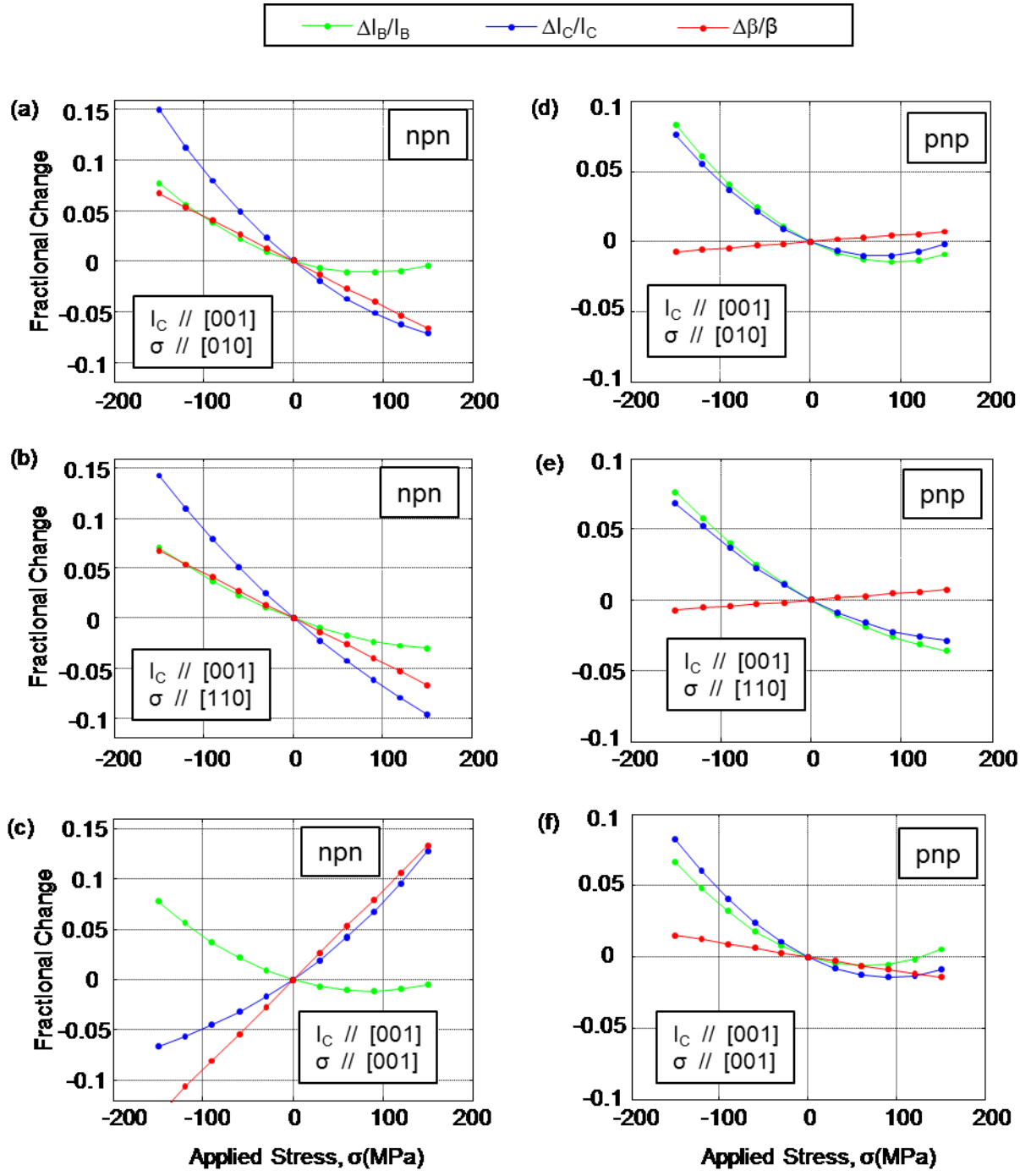


Figure 6.10 - Simulated fractional changes in collector current, base current and dc current gain of vertical transistors on (100) plane as a function of uniaxial stress (a), (b), (c) for npn transistors (d), (e), (f) for pnp transistors

Table 6.2 – Increase in collector current and current gain of a vertical bipolar transistor for 150 MPa				
Stress type	npn transistor		pnp transistor	
	Compressive	Tensile	Compressive	Tensile
In-plane <100>	I_C (15.0%) β(7.0%)	- -	I_C (7.5%) -	- β(1.0%)
In-plane <110>	I_C (14.5%) β(7.0%)	- -	I_C (7.0%) -	- β(1.0%)
Out-of-plane	- -	I_C (12.5%) β(13.0%)	I_C (8.0%) β(1.5%)	- -

For npn transistor the responses for in-plane normal stresses in two different directions are similar (Figure 6.10(a) and (b)). Likewise for pnp transistor the responses for in-plane normal stresses are similar (Figure 6.10(d) and (e)). This similarity is because the current flow direction is perpendicular to the wafer surface in vertical transistors and the sensitivity to in-plane normal stresses is coupled through the piezoresistance coefficients, π_{12}^{n} and π_{12}^{p} for npn and pnp BJTs respectively. Hence the first-order sensitivity to in-plane normal stresses is the same irrespective of the stress orientation in the plane, since $(\sigma'_{11}+\sigma'_{22})$ is invariant under planar stress transformations. However, slight differences can be observed in the second-order sensitivity due to the changes in intrinsic carrier concentration $(\Delta n_i^2/n_i^2)$. This second-order term comes in both I_C and I_B and it ideally cancels out in the β plot. The plots show that the vertical npn transistors are more sensitive to stress-induced changes compared to pnp transistors. Additionally, the changes in dc current gain are opposite for npn and pnp transistors. The dc current gain of both npn and pnp transistors shows higher sensitivity for out-of-plane normal stress compared to in-

plane normal stress. The major differences in the npn plots occur because $\pi_{11} \cong -2\pi_{12}$ in Table 6.1. The percentage increases in collector current and current gain at 150 MPa stress are tabulated in Table 6.2.Out-of-plane tensile normal stress increased both the current and current gain of npn vertical transistors on (100) plane. In addition, in-plane normal compressive stress also increased the I_C, which gave a strong increase of ~15.0% since both the mobility and the intrinsic carrier concentrations terms are added up. In the case of out-of-plane normal stress the changes due to intrinsic carrier concentration is negative in the considered stress levels and reduces the total effect. As a result, the change in I_C is only 12.5% even though the change in mobility is almost double. For pnp transistors, the out-of-plane compressive stress gave some improvement, however the improvement is much less compared to the npn BJT.

6.2.2 rf characteristics

6.2.2.1 Modeling for ac analysis (with Sentaurus)

2-D Sentaurus TCAD simulation was used for rf analysis. Simulations were carried out for two profiles, a lightly doped wide base transistor (Figure 6.1(a)) and a highly doped thin base transistor (Figure 6.1(b)). The hydrodynamic transport model, Philips unified mobility model, piezoresistance mobility model (first order with the piezoresistance coefficients in Table 6.1) and the deformation potential model (default) were selected with all other standard models and parameters.

6.2.2.2 Theoretical expectations

The transit time (τ) cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) of bipolar transistor are related by the following equations [23]:

$$f_T = \frac{1}{2\pi\tau} \tag{6.17}$$

$$f_{\max} = \sqrt{\frac{f_T}{8\pi C_{cb} r_{bb}}} \tag{6.18}$$

where c_{cb} is the base-collector depletion capacitance and r_{bb} is the base resistance. An increase of mobility from stress is expected to decrease transit time, which increases cutoff frequency f_T. The f_T increase and the base resistance r_{bb} decrease from mobility increase both increase f_{max}, maximum oscillation frequency.

6.2.2.3 Analysis of impact of in-plane and out-of-plane normal stresses

Figures 6.11(a) and (b) illustrate the simulated changes in f_T, f_{max} and r_{bb} as a function of I_C for a 1 GHz peak f_T npn BJT (profile 1) and a 34 GHz peak f_T npn BJT (profile 2). The emitter widths are 4.0 μm and 0.18 μm respectively.

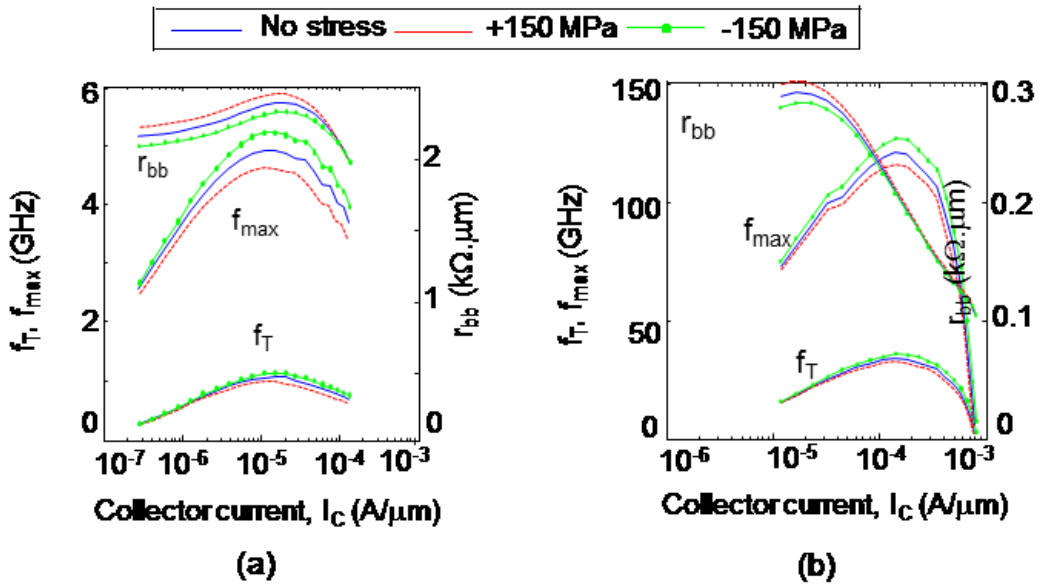


Figure 6.11 - Simulation results of stress induced changes in f_T, f_{max} and r_{bb} of npn BJT for $\sigma'_{22}[\bar{1}10]$ (a) for profile 1 and (b) for profile 2.

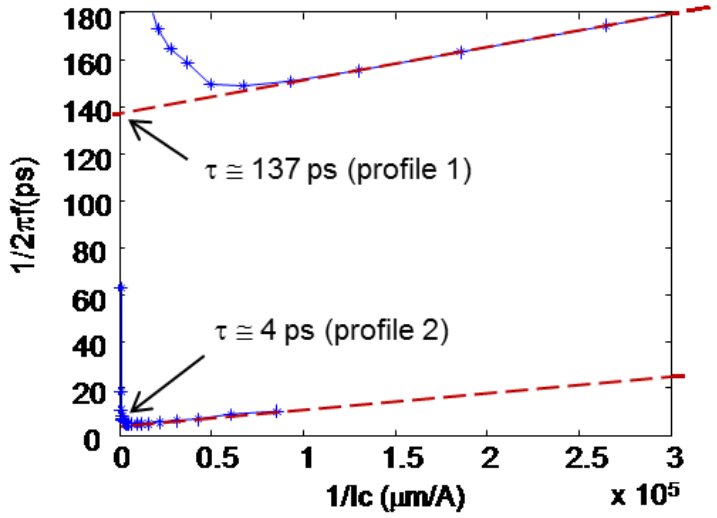


Figure 6.12 - $1/2\pi f_T$ vs $1/I_C$ plots of profile 1 and profile 2 showing the transit time extraction at zero stress.

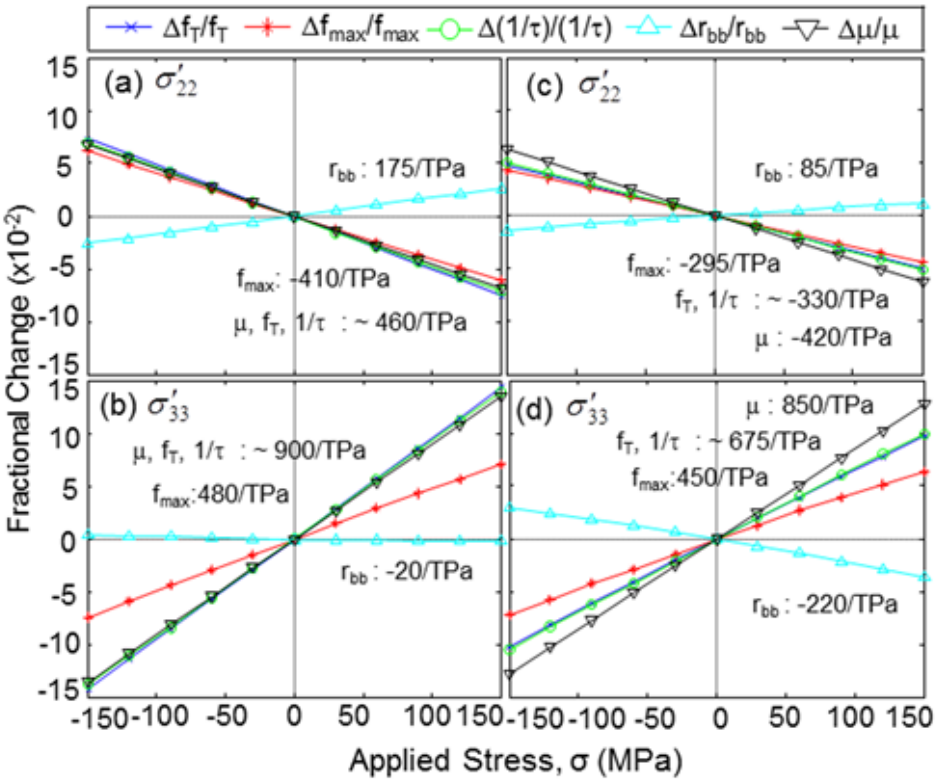


Figure 6.13 - Fractional changes in f_T, f_{max}, $1/\tau$, and r_{bb} along with changes in μ at peak f_T point. (a) & (b) are the results of npn profile 1. (c) & (d) are the results of npn profile 2. Stress directions and the slopes are indicated

Simulations were carried out for both σ'_{22} and σ'_{33} and the changes in f_T, f_{max} and r_{bb} at peak f_T points were calculated. The results are plotted in Figure 6.13 (stress directions are indicated). Transit times for different stress levels were extracted from $1/2\pi f_T$ vs $1/I_C$ plots as described in [23] and changes in $(1/\tau)$ also included. The transit times (at no stress) were obtained as 137 ps for the 1 GHz transistor and 4 ps for 34 GHz transistor respectively (Figure 6.11). Changes in mobility (as per piezoresistance coefficient) are also included for easy comparison. As in Figure 6.12(a), with a 150 MPa in-plane compressive stress, peak f_T and f_{max} increased 7.3% and 6.2%, respectively. These changes are due to enhancement of electron mobility with in-plane compressive stress. The base resistance r_{bb} is reduced due to the enhancement in lateral hole mobility. Changes are opposite for tensile stress. As illustrated in Figure 6.12(b), for an out-of-plane tensile stress, f_T and f_{max} increased and r_{bb} decreased. A 14.1% improvement in peak f_T, and a 7.4% improvement on peak f_{max} were observed.

In all cases the changes in $1/\tau$ and f_T follow the changes in mobility and changes in f_{max} follow the changes in $\sqrt{f_T/r_{bb}}$. However, the changes (magnitude) are less for highly doped low dimensional transistors as depicted in Figures 6.12(c) and (d). In the first transistor, base transit time dominates the total transit time, and therefore mobility has a more direct impact on f_T. In the second transistor, collector transit time is a larger fraction of the total transit time, and velocity saturation plays a bigger role leading to less stress sensitivity of f_T due to the assumption that saturation velocity is unaffected by stress. This assumption however is conservative, as part of the mobility increase from stress is due to effective mass reduction, which should increase saturation velocity [101].

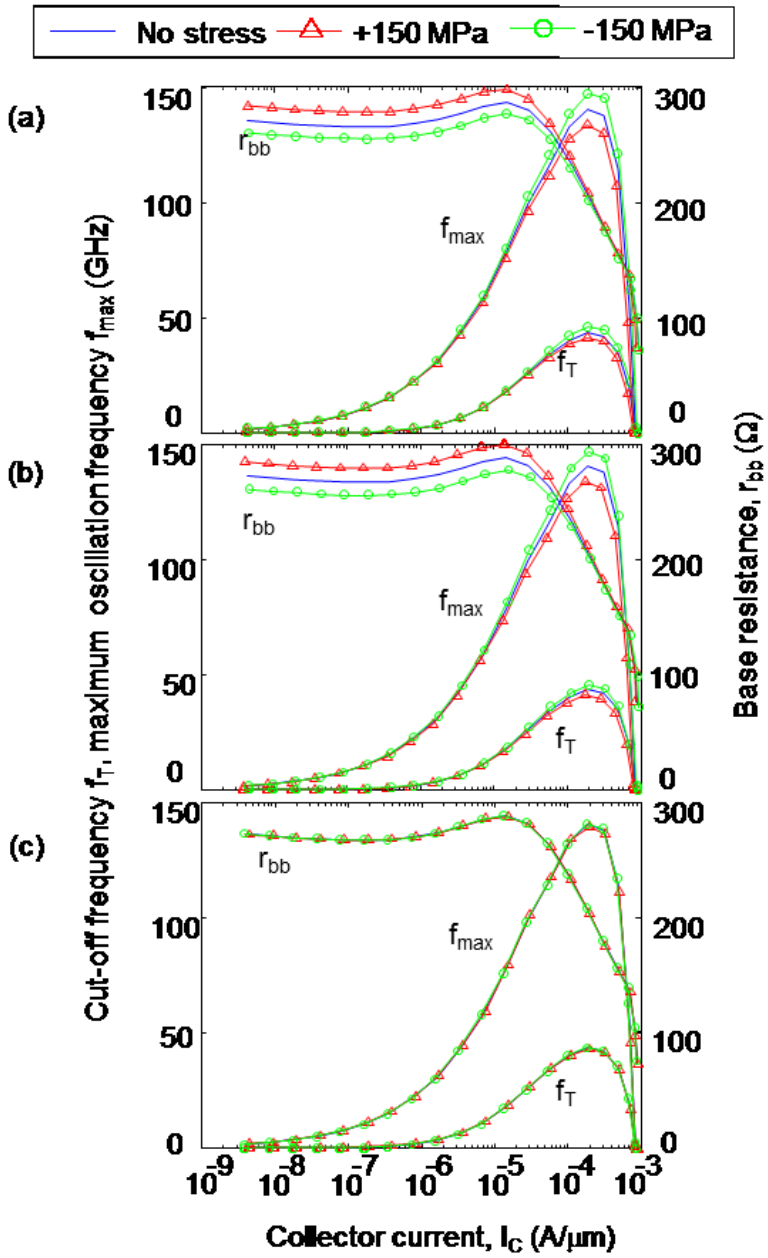


Figure 6.14 - Simulated stress induced changes in f_T, f_{max} and r_{bb} (a) combined effects; (b) with piezoresistance mobility model only; (c) with deformation potential model only.

Simulation results by separately applying each stress model also revealed that the changes were totally due to the variations in mobility and the alterations in n_i produced only minor or no changes in f_T, f_{max} and r_{bb} (Figure 6.14). Hence the rf performance enhancement in

silicon BJT is attributed to mobility improvement and the consequent reductions in transit times in emitter, base and collector regions.

Experimental results for comparable in-plane uniaxial stress (150 MPa) effects in the peak f_T was found to be <1% in SiGe HBT heterostructures while the polarities of changes were similar to the results presented here for silicon BJTs [27]. This less remarkable improvement in SiGe HBTs is probably due to the existing huge strain in the base [24].

6.3 Lateral Transistors on (100) plane

The 1-D model used for dc analysis of vertical transistors was used changing the current in lateral direction.

6.3.1 Theoretical Expectations

Lateral pnp BJT on (100) plane

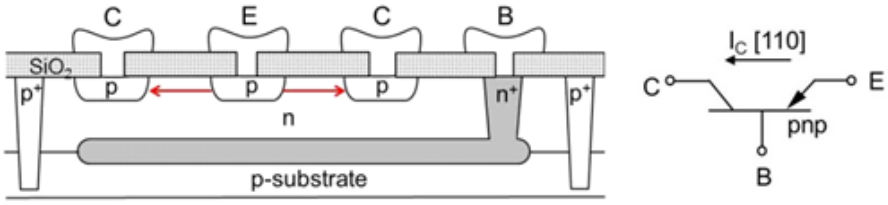


Figure 6.15 - A simplified cross-section of a lateral pnp transistor showing main current direction and notation of the transistor

In lateral transistors the main current direction is parallel to the wafer plane. Usually transistor axes are aligned with the wafer axes and lateral transistors have the current flow direction parallel or perpendicular to the wafer flat. Hence the current direction can be [110] or $[\bar{1}10]$ and both are equivalent. Figure 6.15 shows a lateral pnp BJT on (100) plane, in which the main current flow is in [110] direction. Similar to the vertical transistors, for lateral transistors also the stress-induced changes in different current components can be written as a combination

of changes due to the changes in mobility and the changes in intrinsic carrier concentration. For a lateral BJT, the perpendicular components will be split into two parts: the in-plane components ($\sigma_{\perp in}$, $\pi_{\perp in}$) and the out-of-plane components ($\sigma_{\perp out}$, $\pi_{\perp out}$). Hence the expressions for normalized fractional changes in current components will be as follows:

Normalized change in collector current

$$\begin{aligned}\frac{\Delta I_C}{I_C} &= -\pi_{\perp in}^{pB}\sigma_{\perp in} - \pi_{\perp out}^{pB}\sigma_{\perp out} - \pi_{||}^{pB}\sigma_{||} + \frac{\Delta n_{iB}^2}{n_{iB}^2} \\ &= -\pi_{\perp in}^{pB}\sigma'_{22} - \pi_{12}^{pB}\sigma_{33} - \pi_{||in}^{pB}\sigma'_{11} + \frac{\Delta n_{iB}^2}{n_{iB}^2}\end{aligned} \tag{6.19}$$

Normalized change in injection limited base current component

$$\begin{aligned}\frac{\Delta I_{BE}}{I_{BE}} &= -\pi_{\perp in}^{nE}\sigma_{\perp in} - \pi_{\perp out}^{nE}\sigma_{\perp out} - \pi_{||}^{nE}\sigma_{||} + \frac{\Delta n_{iE}^2}{n_{iE}^2} \\ &= -\pi_{\perp in}^{nE}\sigma'_{22} - \pi_{12}^{nE}\sigma_{33} - \pi_{||in}^{nE}\sigma'_{11} + \frac{\Delta n_{iE}^2}{n_{iE}^2}\end{aligned} \tag{6.20}$$

Normalized change in transport limited base current component

$$\frac{\Delta I_{BR}}{I_{BR}} \cong \frac{\Delta n_{iB}^2}{n_{iB}^2} \tag{6.21}$$

Normalized change in base current

$$\frac{\Delta I_B}{I_B} = \delta\left(-\pi_{\perp in}^{nE}\sigma'_{22} - \pi_{12}^{nE}\sigma_{33} - \pi_{||in}^{nE}\sigma'_{11} + \frac{\Delta n_{iE}^2}{n_{iE}^2}\right) + (1-\delta)\frac{\Delta n_{iB}^2}{n_{iB}^2} \tag{6.22}$$

The $\pi_{\perp in}$, $\pi_{\perp out}$ and $\pi_{||}$ can be expressed in terms of the fundamental piezoresistance coefficients, π_{11}, π_{12}, and π_{44}. The estimated piezoresistance coefficients are in Table 6.3 where $\pi_{||in} = (\pi_{11}+\pi_{12}+\pi_{44})/2$, $\pi_{\perp in} = (\pi_{11}+\pi_{12}-\pi_{44})/2$. The expressions for lateral npn BJTs are analogous.

Table 6.3 - Piezoresistive coefficient estimates for vertical and lateral BJTs on (100) plane					
Current orientation	Coefficient (10^{-12} Pa^{-1})	npn transistors		pnp transistors	
		π^{nB}	π^{pE}	π^{pB}	π^{nE}
	π_{44}	-150	700	1100	-70
Vertical <001>	$\pi_{\parallel} = \pi_{11}$	-900	25	30	-400
	$\pi_{\perp} = \pi_{12}$	455	-8	-15	200
Lateral <110>	$\pi_{\parallel in}$	-297.5	358.5	557.5	-135
	$\pi_{\perp in}$	-147.5	-341.5	-542.5	-65
	$\pi_{\perp out} = \pi_{12}$	455	-8	-15	200

6.3.2 Analysis of impact of in-plane and out-of-plane normal stresses

The 1-D model used for dc analysis of vertical transistors was used changing the current in lateral direction. A similar analysis was carried out for lateral transistors as well. In contrast to the vertical transistors, the stress sensitivity varies for in-plane stresses also in lateral transistors depending on the current and stress orientations. Hence, the stress sensitivity to longitudinal (current and the stress are in same direction) and transverse (stress direction is perpendicular to the current direction) stresses were also analyzed. For npn transistors the simulation results for the in-plane longitudinal normal stress, in-plane transverse normal stresses and out-of-plane normal stress are shown in Figure 6.16(a-c), respectively. Likewise simulation results for pnp transistors are illustrated in the same order in Figure 6.16(d-f). As evident in the plots, the stress sensitivity of npn lateral transistors are much less for in-plane normal stresses. However, for an out-of-plane compressive stress of 150 MPa, npn lateral transistors showed an increase of 15.0% in collector current and an increase of 7% in dc current gain. The stress sensitivity of lateral pnp transistors for in-plane normal stress vary widely depending on the current and stress orientations (Figure 6.16(d) and (e)).

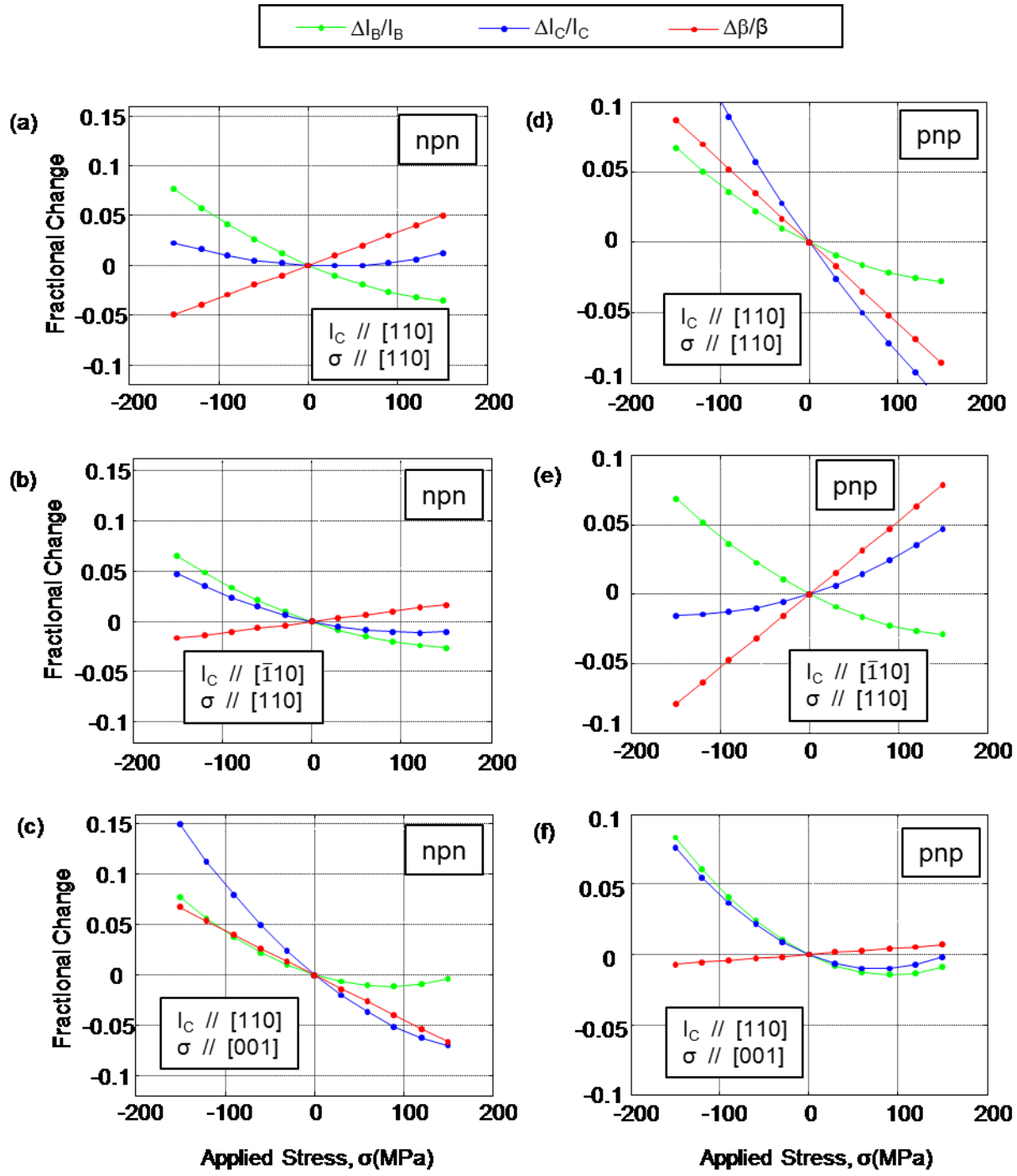


Figure 6.16 - Simulated fractional changes in collector current, base current and dc current gain of lateral transistors on (100) plane as a function of uniaxial stress (a), (b), (c) for npn transistors (d), (e), (f) for pnp transistors

Table 6.4 - Increase in collector current and current gain of a lateral transistor for 150 MPa				
Stress type	npn transistor		pnp transistor	
	Compressive	Tensile	Compressive	Tensile
In-plane longitudinal	Ic (2.0%) -	Ic (1.5%) β (5.0%)	Ic (20.0%) β (8.5%)	- -
In-plane transverse	Ic (5.0%) -	- β (2.0%)	- -	Ic (5.0%) β (8.0%)
Out-of-plane	Ic (15.0%) β (7.0%)	- -	Ic (7.5%) -	- β (1.0%)

The highest increase of about 20% in the collector current and about 8.5% increase in the dc current gain were achieved for longitudinal in-plane compressive stress. Changes in dc current gain for out-of-plane normal stress is very small. However, change in collector current is moderately high for compressive stresses (Table 6.4).

In the previous section we found that f_T and f_{max} improve with mobility. Hence the same stresses whichever give improvement in dc current gain also give improvement in f_T and f_{max} as well. Based on these analyses we suggest that out-of-plane compressive stress can be utilized to maximize the I_C, β, f_T and f_{max} for npn lateral transistors on (100) plane. In addition, the longitudinal in-plane compressive stress can be utilized to maximize the I_C, β, f_T and f_{max} for pnp lateral transistors on (100) plane.

6.3 Summary

In this work the analysis of stress induced effects in vertical and lateral bipolar transistors on (100) plane is presented with a combined mobility-deformation potential model approach. For the considered stress range (< 200 MPa), the collector and base currents of npn and pnp transistors showed a non-linear change which consists of a linear portion due to the mobility variations and a non-linear portion due to the variations in intrinsic carrier concentration. The variation due to the changes in intrinsic carrier concentration nearly cancels out and the changes are almost linear in dc current gain. However, a small nonlinearity is also possible in the dc current gains when there is a mismatch in the intrinsic carrier concentrations of the base and emitter. Vertical pnp transistors exhibits low stress sensitivity over vertical npn and lateral npn and pnp transistors on (100) plane.

The possibility for potential strain engineering was explored. Analyses revealed that in vertical transistors significantly higher enhancement in I_C, β, f_T and f_{max} can be achieved for npn BJTs compared to pnp BJTs. Out-of-plane normal stress showed higher increments compared to in-plane normal stresses for both npn and pnp BJTs. Also the injection limited structures were found to be more sensitive to stress in both npn and pnp BJTs. Similar results were observed for various transistor geometries. In lateral transistors, pnp transistors showed higher enhancement compared to npn transistors. In-plane longitudinal compressive stress give higher improvement in pnp transistors and out-of-plane compressive stress gives higher improvement in npn transistors. This model can be extended for stress analysis in transistors in any plane. Such analysis, when performed for different current and stress orientations, is likely to identify the current-stress orientation combinations in which the stress-induced changes in important bipolar parameters will be optimized.

CHAPTER 7

MITIGATION OF STRESS EFFECTS IN PRECISION ANALOG CIRCUITS

7.1 Introduction

In previous chapters the stress effects in various npn and pnp bipolar transistor structures were studied. In the last chapter it has been shown that by selecting appropriate stress orientation with respect to the current orientation the performance of bipolar transistors can be improved. This chapter presents methods to minimize the inaccuracy caused by the stress effects in precision analog circuits. With the outcome of previous chapters the stress induced changes in some basic analog building blocks on (100) plane were predicted and methods were suggested to minimize these effects. Spice simulation was used to demonstrate these effects for number of important analog circuits including differential pairs, PTAT (Proportional To Absolute Temperature) circuits, operational amplifiers (op-amps) and bandgap references.

7.2 Magnitudes of stress and stress gradients in integrated circuits

The more complete expressions for the transistor current variations include the sum of the in-plane normal stresses ($\sigma'_{11}+\sigma'_{22}$), which is invariant under planar stress transformations. This sum can be very large in the center of large die in certain packaging configurations. Stress gradients across a small die was reported from measurements using a CMOS sensor array chip containing 256 sensor cells in each of the PMOS and NMOS sensor arrays. The measured stress variations for $\sigma'_{11,}$ σ'_{22} and σ'_{12} across sample rows in the array showed the significant stress gradients that occur across these die (2.2 mm x 2.2 mm), 65 MPa/mm and 12 MPa/mm respectively [102]. Such variations of stress in individual stress terms across the die surface may

cause issues in precision analog circuits which work upon the precise matching of the transistors. Typical values of the shear stress as well as the out-of-plane normal stress are expected to be much smaller (in the 10's of MPa) and less important to BJT current variations. In-plane normal stress effects in some analog circuits are investigated in the next section.

7.3 Impact of stress on analog integrated circuit building blocks

In this section the Spice simulation results are presented for some basic analog building blocks on (100) plane such as differential pairs, PTAT circuits, op-amps and voltage reference circuits and compared with the theoretical expectations. In Spice simulation the stress effect in transistors was included by incorporating the 1-D theoretical model illustrated in chapter 3 for stress effects in I_S and β. When resistors are in the circuits, stress effects in resistors are also modeled by the piezoresistance model. Spice Netlists are included in Appendix E. Refer [103] for details about adding models for various parameters.

Stress response of offset voltage of differential pairs

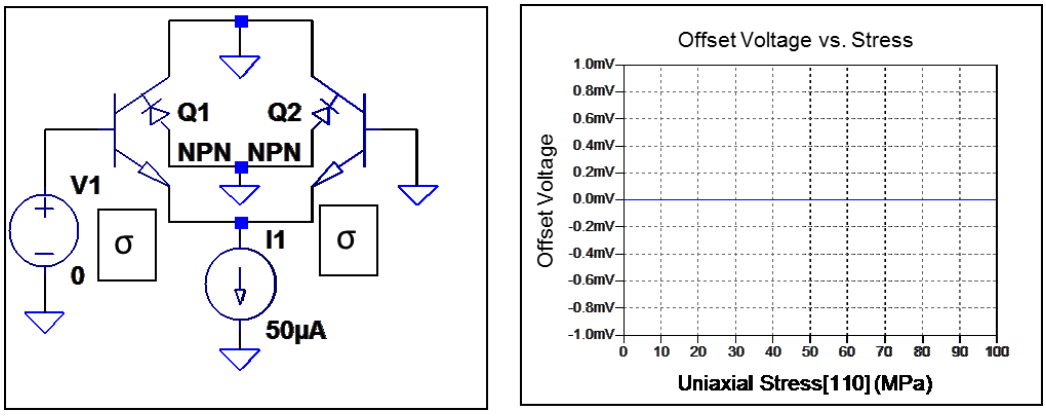


Figure 7.1 - A differential pair circuit (a); and simulated offset voltage versus uniaxial [110] Stress (b).

Figure 7.1 presents a differential pair circuit and the simulated offset voltage of the circuit for a uniaxial stress [110]. Q_1 and Q_2 are matching npn transistors with base-emitter voltages and saturation currents of (V_{BE1}, V_{BE2}) and (I_{S1}, I_{S2}), respectively. An initial mismatch is assumed in saturation currents. The offset voltage (V_{OS}) expression for this simple differential pair can be derived as follows:

$$V_{OS} = V_1 = V_{BE1} - V_{BE2} \tag{7.1}$$

$$I_{C1} = I_{S1} \exp\left(\frac{\mathrm{V_{BE1}}}{\mathrm{V_T}}\right) \quad \Rightarrow \quad V_{BE1} = V_T \ln\left(\frac{I_{C1}}{I_{S1}}\right) \tag{7.2}$$

Similarly, for Q_2

$$V_{BE2} = V_T \ln\left(\frac{I_{C2}}{I_{S2}}\right) \tag{7.3}$$

Substituting (7.2) and (7.3) in (7.1) yields:

$$V_{OS} = V_T \ln\left(\frac{I_{C1}}{I_{S1}}\right) - V_T \ln\left(\frac{I_{C2}}{I_{S2}}\right) \tag{7.4}$$

$$V_{OS} = V_T \ln\left(\frac{I_{C1}}{I_{C2}}\frac{I_{S2}}{I_{S1}}\right) \tag{7.5}$$

Applying $I_{C1}=I_{C2}$

$$V_{OS} = V_T \ln\left(\frac{I_{S2}}{I_{S1}}\right) \tag{7.6}$$

Including stress effects in saturation current the theoretical expression for V_{OS} becomes

$$V_{OS} = V_T \ln\frac{I_{S2}(1+\pi\sigma)}{I_{S1}(1+\pi\sigma)} \tag{7.7}$$

If stress is maintained as a common-mode effect V_{OS} will be independent of stress and the expression becomes

$$V_{OS} = V_T \ln \frac{I_{S2}}{I_{S1}} \tag{7.8}$$

The simulated results agree with this theoretical expectation. However, the output will change if there are stress gradients across the transistor causing different rate of changes in I_{S1} and I_{S2}.

Stress response of PTAT Circuit

In a similar way the PTAT voltage can be derived for the circuit in Figure 7.2. V_{PTAT} is equal to the difference in the two base-emitter voltages of the transistors can be given as

$$V_{PTAT} = V_{BE2} - V_{BE1} \tag{7.9}$$

$$V_{PTAT} = V_T \ln\left(\frac{I_{C2}}{I_{C1}} \frac{I_{S1}}{I_{S2}}\right) \tag{7.10}$$

$$V_{PTAT} = V_T \ln \frac{I_2}{I_1} \frac{I_{S1}(1+\pi\sigma_1)}{I_{S2}(1+\pi\sigma_2)} \tag{7.11}$$

where σ_1 and σ_2 are the stresses experienced by the transistors Q_1 and Q_2, respectively.

Assuming $I_{S1} = I_{S2,}$ for $I_2 = 5\ I_1$ and $\sigma_1 = \sigma_2$

$$V_{PTAT} = V_T \ln(5) = 0.0259 \text{ V } (1.609) = 41.7 \text{ mV}$$

This theoretical calculation indicates the output voltage should be independent of stress as long as the stress state is the same in both transistors. But the output voltage may change if any stress gradient appears across these two transistors. The simulation results with the common-mode stress effect and with different mode stress effect are also shown in Figure 7.2. Both agree well with the theoretical calculations. Stress induced changes in I_S and β were included in the spice simulation (Appendix B)

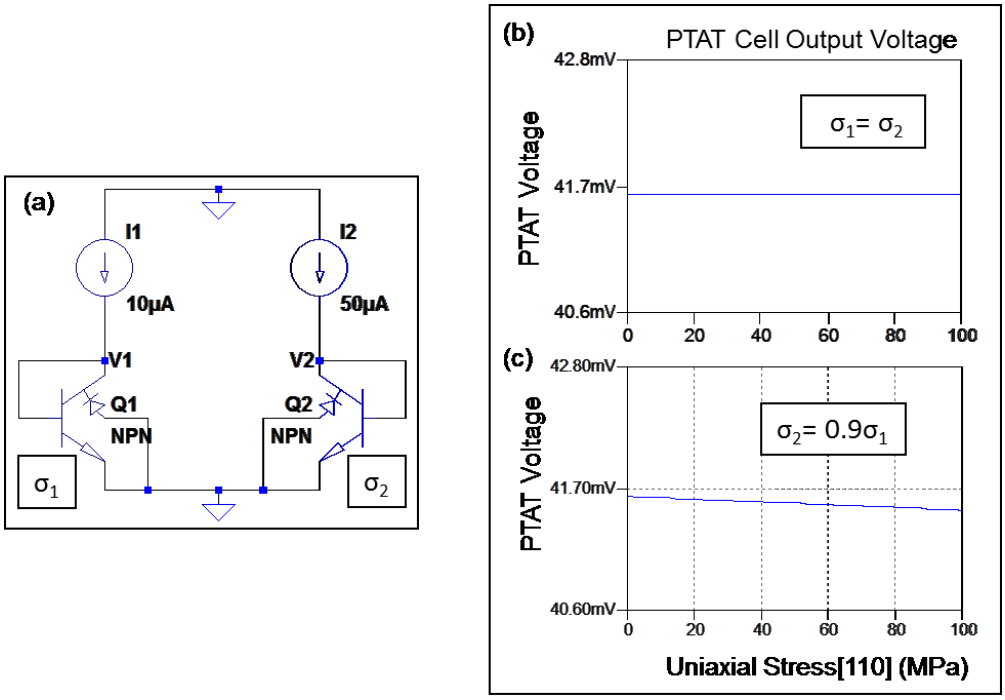


Figure 7.2 - Simulated output voltage of a PTAT circuit versus uniaxial [110] Stress (a) circuit (b) output when both transistors experience equal stress ($\sigma_1 = \sigma_2$) (c) output when transistors experience different stress ($\sigma_2 = 0.9\ \sigma_1$).

Stress response of op-amp offset voltage

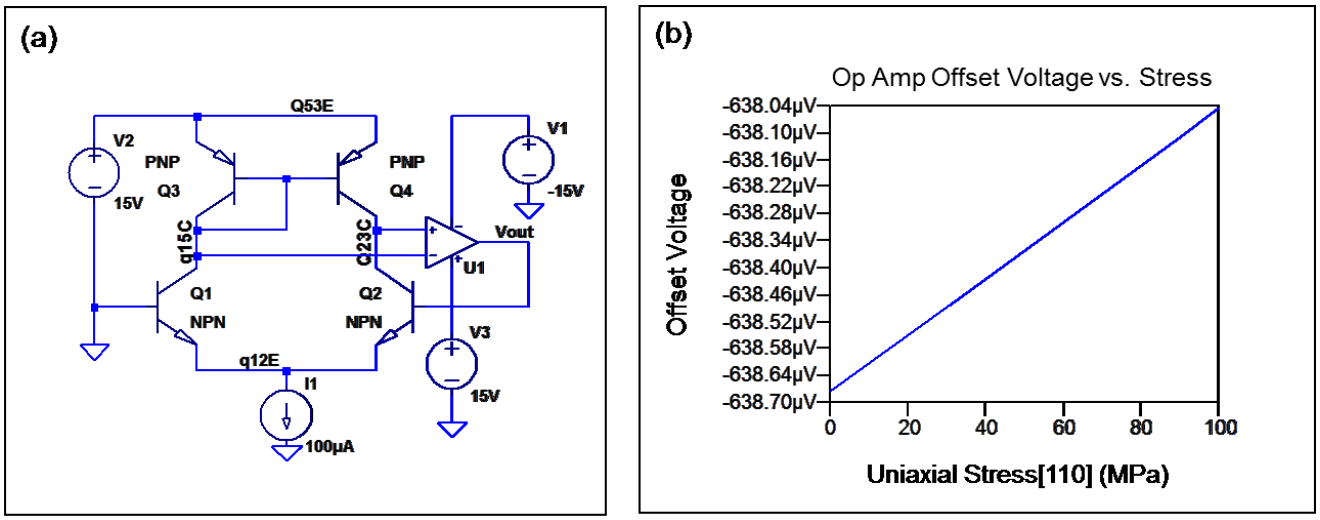


Figure 7.3 - A simple op-amp circuit (a); and simulated offset voltage versus uniaxial [110] stress (b).

The offset voltage of the op-amp in Figure 7.3 can be given by

$$\frac{\Delta V_{OS}}{\Delta \sigma} = -\frac{2\pi_\beta V_T}{\beta_{pnp}} \tag{7.12}$$

$$\text{where } \pi_\beta = -10/TPa \quad and \quad \beta_{pnp} = 80(1-\pi_\beta \sigma) = 80(1+10x10^{-12}\sigma)$$

From the above theoretical expression change in offset voltage can be calculated as

$$\frac{\Delta V_{OS}}{\Delta \sigma} = \frac{2(10x10^{-12})(0.0258)}{80}$$
$$\frac{\Delta V_{OS}}{\Delta \sigma} = 6.45 \ nV/MPa \tag{7.13}$$

Equation (7.12) indicates that the stress-induced changes in the dc current gain of the pnp transistors make changes in the offset voltage while the changes in the current gain of npn transistors do not affect the offset voltage in this op-amp circuit.

As per spice simulation results in Figure 7.3, the change in offset voltage is calculated as

$$\frac{\Delta V_{OS}}{\Delta \sigma} = 6.29 \ nV/MPa \tag{7.14}$$

This also agrees with the theoretical expectations.

Stress response of bandgap reference circuit

Bandgap reference circuits are used to generate a very stable voltage reference with respect to both temperature and the power supply variations in analog circuits. The basic idea of the bandgap voltage reference is to balance the negative temperature efficient of a pn junction with the positive temperature coefficient of the thermal voltage. The circuit components are precisely designed to balance any unintentional effects of temperature variations and power changes. However if mechanical stresses make any variations in the circuit parameters, it may

cause the reference circuits to work out of specifications. Hence, it is very important to mitigate these stress effects.

Figure 7.4(a) and 7(b) presents a bandgap reference circuit and the simulation results of the circuit for the stress-induced changes in the output reference voltage (for R and σ in [110] direction). In the simulation stress induced changes in the transistors and the resistors are included. In addition common-mode stress effect is assumed for all transistors and resistors. The op-amp element is assumed ideal.

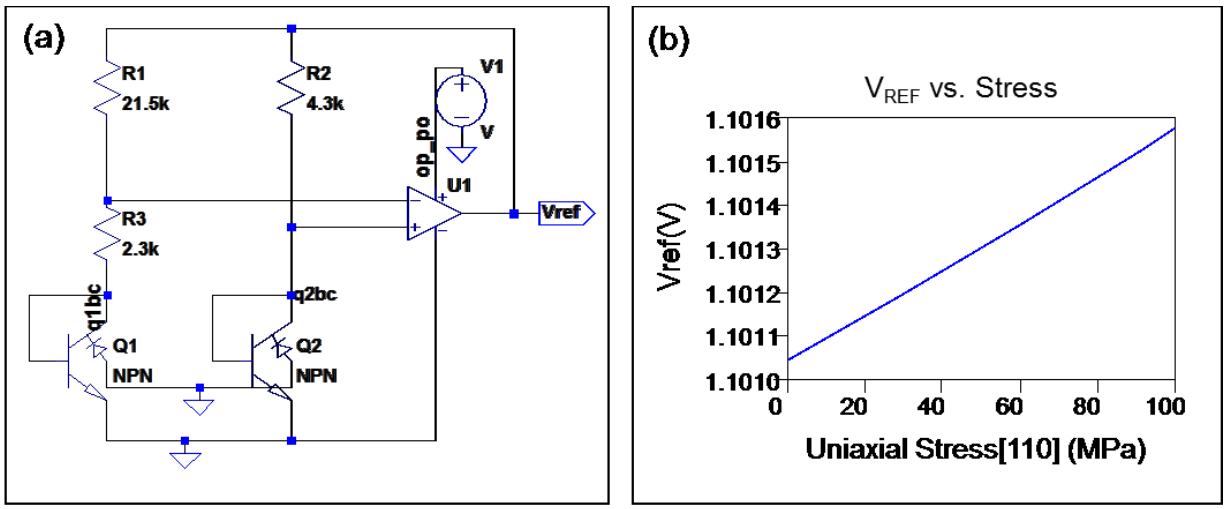


Figure 7.4 - Simulated output voltage of a bandgap reference circuit versus uniaxial [110] Stress (a) circuit diagram (b) SPICE simulation output for resistors in [110] and stress in [110] directions.

Considering the circuit in Figure 7.4, the theoretical expression for the stress-induced changes in V_{REF} can be derived as follows:

The voltage across the resistances R_1 and R_2 are equal since the voltages at two input points are equal in an ideal op-amp.

$$R_1 I_1 = R_2 I_2 \tag{7.15}$$

$$\frac{I_2}{I_1} = \frac{R_1}{R_2} \tag{7.16}$$

Since voltages at two inputs of the op-amp are equal the following expressions also can be written.

$$VBE_2 = VBE_1 + I_1 R_3 \tag{7.17}$$

$$V_T \ln\left(\frac{I_2}{I_S}\right) = V_T \ln\left(\frac{I_1}{I_S}\right) + I_1 R_3 \tag{7.18}$$

$$I_1 = \frac{V_T}{R_3} \ln\left(\frac{I_2}{I_1}\right) \tag{7.19}$$

$$I_1 = \frac{V_T}{R_3} \ln\left(\frac{R_1}{R_2}\right) \tag{7.20}$$

$$V_{REF} = VBE_2 + R_2 I_2 = VBE_1 + (R_1 + R_3) I_1 \tag{7.21}$$

$$V_{REF} = V_T \ln\left(\frac{I_1}{I_S}\right) + (R_1 + R_3) I_1 \tag{7.22}$$

$$V_{REF} = V_T \ln\left(\frac{V_T}{R_3 I_S} \ln\left(\frac{R_1}{R_2}\right)\right) + (R_1 + R_3) \frac{V_T}{R_3} \ln\left(\frac{R_1}{R_2}\right) \tag{7.23}$$

$$V_{REF} = V_T \ln\left(\frac{V_T}{R_3 I_S} \ln\left(\frac{R_1}{R_2}\right)\right) + \left(1 + \frac{R_1}{R_3}\right) V_T \ln\left(\frac{R_1}{R_2}\right) \tag{7.24}$$

$$V_{REF} = V_T \ln\left(\frac{V_T}{R_3 I_S} \ln\left(\frac{R_1}{R_2}\right)\right) + \left(1 + \frac{R_1}{R_3}\right) V_T \ln\left(\frac{R_1}{R_2}\right) \tag{7.25}$$

In equation (7.25) stress dependent quantities are I_S, R_1, R_2 and R_3. Stress induced changes associated with $\frac{R_1}{R_2}$ and $\frac{R_1}{R_3}$ terms will be cancelled out if R_1, R_2 and R_3 are in same orientation. However, still the stress effects in R_3 and I_S affect the resultant V_{REF}. The transistors are vertical

npn on (100) plane. The stress sensitivity is isotropic for in-plane normal stress irrespective to the stress direction in the plane. For resistors, selecting p-type resistors and keeping at ±45^o or using 0^o/90^o compensation (making the resistances into two equal parts and keeping them at right angle along [110] and [$\bar{1}$10] directions) is expected to reduce the changes in V_{REF} due to resistor changes. Some simulation results and analysis verifying the theoretical expectations for in-plane normal stress in different orientation are presented below.

In this analysis we keep the resistances R_1, R_2 and R_3 at the same orientations. Hence the second term in (7.25) is cancelled out and the expression for stress-induced changes in V_{REF} reduces as:

$$\frac{\Delta V_{ref}}{\Delta \sigma} = -V_T \left[\frac{1}{I_S} \frac{\Delta I_S}{\Delta \sigma} + \frac{1}{R_3} \frac{\Delta R_3}{\Delta \sigma} \right] \tag{7.26}$$

In this analysis, the sress effects in saturation current is modeled using piezoresistance mobility model (assuming linear variation for small stress levels).

$$I_S = 10^{-16} \left(1 - \pi_{12}^{nB} \sigma \right) \tag{7.27}$$

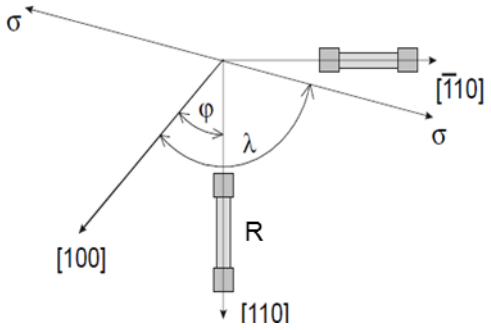


Figure 7.5 - Resistor (R) and stress (σ) orientations in a (100) plane [56]

Stress effects in each resistor in the voltage reference circuit is modeled by the following equation (Figure 7.5) in [56]:

$$R(\sigma) = R\left[1+\sigma\left(\pi_{11}^{p}\left(\frac{1}{2}+\frac{1}{2}\cos 2\phi\cos 2\lambda\right)+\pi_{12}^{p}\left(\frac{1}{2}-\frac{1}{2}\cos 2\phi\cos 2\lambda+\pi_{44}^{p}\left(\frac{1}{2}\sin 2\phi\sin 2\lambda\right)\right)\right)\right] \tag{7.28}$$

where R is replaced by R_1, R_2 or R_3. Simulation results and the results from the analytical calculations for some different configurations are presented in Table 7.1. As illustrated both theoretical and simulation results agree well. Stress effects in transistor alone give a variation of 11.8 μV/MPa in V_{REF}, which is independent of in-plane stress orientation. The resistor-stress orientation combination in the plane increase or reduce this change depending on the orientations.

Table 7.1 – $\frac{\Delta V_{REF}}{\Delta\sigma}$ for an in-plane stress in different orientations with respect to R

Elements considered	theoretical	simulation	Unit
BJT, no stress in R	$V_T\,\pi_{12}^{nB} = 11.61$	11.8	μV/MPa
BJT, R[110], σ [110]	$-V_T\left[-\pi_{12}^{nB}+\frac{\left(\pi_{11}^{p}+\pi_{12}^{p}+\pi_{44}^{p}\right)}{2}\right] = 4.992$	5	μV/MPa
BJT, R[110], σ[$\bar{1}$10]	$-V_T\left[-\pi_{12}^{nB}+\frac{\left(\pi_{11}^{p}+\pi_{12}^{p}-\pi_{44}^{p}\right)}{2}\right] = 17.792$	18	μV/MPa
BJT, $\frac{R}{2}$[100], $\frac{R}{2}$ [$\bar{1}$10], σ[110]	$-V_T\left[-\pi_{12}^{nB}+\frac{\left(\pi_{11}^{p}+\pi_{12}^{p}\right)}{2}\right] = 11.392$	11.7	μV/MPa

In the wafer resistors are normally aligned with wafer axis [110] or [$\bar{1}$10]. However, in some cases they aligned with [100], [010] axes as well. Hence resistors are fixed aligned with one of these axes. But the stress orientation changes. Figure 7.6 demonstrates the changes in V_{ref} with different stress orientations. Simulation was performed keeping the resistors R_1, R_2 and R_3 aligned with these axes and changing the stress orientation and the results are presented in Figure 7.6.

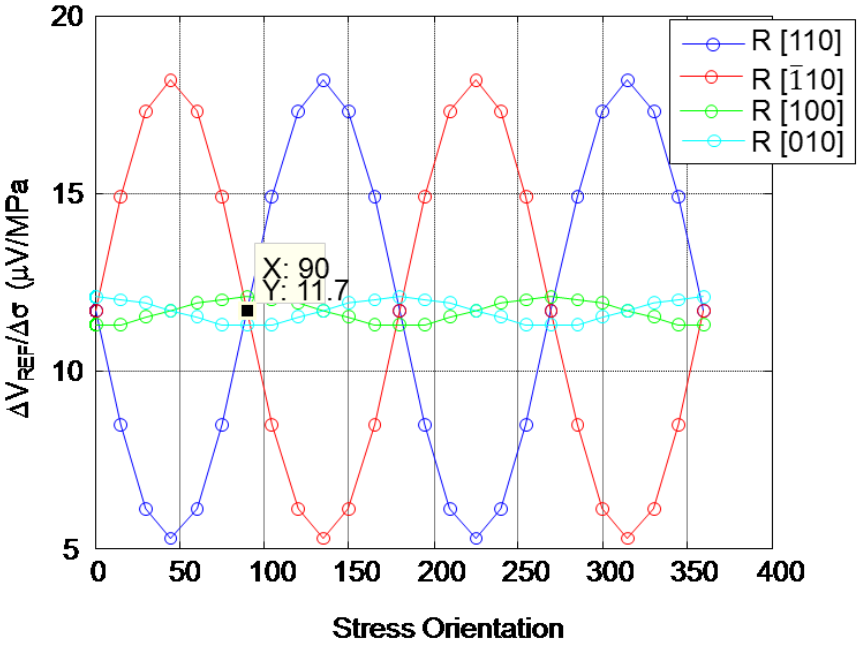


Figure 7.6 - Relative stress induced change V_{REF} for different resistor orientations

For this circuit, change in saturation current and the changes in resistances due to stress highly influence the resultant V_{REF}. The change in resistance depends on the resistance type and the orientation. The changes due to resistance variation can be reduced by keeping the resistor at [100] or [010] orientations. $0^o/90^o$ compensation also minimized the changes in resistances and hence the changes in V_{REF} as indicated in Table 7.1. However, for in-plane stresses the changes

in saturation current of a vertical transistor on (100) plane is isotropic. Employing npn transistors on (111) plane could help in keeping the changes in saturation current small.

7.4 Approaches for minimizing the impact of stress on bipolar integrated circuits

The following methods are suggested for minimizing the stress effects in bipolar analog circuits.

- Using $\pm 45^{o}$ p-type resistors or $0^{o}/90^{o}$ p-type resistor compensation whenever possible for resistors in precision analog circuits.
- Replacing resistors with transistors whenever possible to reduce the area and thereby the stress gradient.
- Using standard differential circuit techniques to make the stress a common-mode effect. This includes
  - Match transistors as closely as possible
  - Differential circuits minimize impact of $\Delta I_S/Is$
  - Place matched devices close together to avoid stress gradients
  - Avoid chip regions of high stress and high gradient using finite element method (FEM) simulations
- Enclosed lateral devices provide stress compensation.
- Using pnp transistors than npn transistors reduce the stress dependence effects in current mirrors on (100) plane.
- Circuits on (100) plane sensitive to current gain values should employ pnp transistors than npn transistors whenever possible.
- Circuits on (111) plane sensitive to current gain values should employ npn transistors than pnp transistors whenever possible.

7.5 Summary

In this chapter, methods are provided to mitigate the unfavorable stress effects is bipolar transistors and analog circuits. Spice simulations were carried out in some basic precision analog circuits. With incorporating the 1-D theoretical models developed in chapter 3 the stress induced changes in analog circuits were successfully predicted. The predicted results match well with the theoretical expectations. Some methods for stress mitigation also provided.

CHAPTER 8

CONCLUSION

In this dissertation a comprehensive study on mechanical stress effects on bipolar transistor characteristics is presented using experimental and numerical modeling approaches. A new 1-D numerical model was developed for stress analysis in which stress-induced changes in bipolar transistors were modeled with a combined mobility-deformation potential modeling approach. This approach provided clear insight into the dominant effects of stress on different bipolar transistor parameters. The validity of the model was verified for npn and pnp transistors on (100) plane and found to be consistent with the experimental results and the theoretical expectations. With the 1-D numerical model the simulation was very fast and results for a given stress orientation were obtained in less than a minute. Importantly, these 1-D simulation results are comparable to the results of a 2-D model with Sentaurus TCAD tool, which usually takes about an hour on a similar CPU when similar accuracy is needed. With the use of appropriate parameters this model can be extended for any npn/pnp vertical or lateral transistor irrespective of the transistor plane or orientation.

The stress induced changes in various parameters of vertical and lateral npn/pnp BJTs on (100) plane were analyzed to determine the best stress orientation with the overall goal of improving/maximizing the mobility and/or intrinsic carrier concentration. Analyses for vertical BJTs on (100) plane revealed that significantly higher enhancement in I_C, β, f_T and f_{max} can be achieved for npn BJTs compared to pnp BJTs. Out-of-plane normal stress showed higher increments compared to in-plane normal stresses for both npn and pnp vertical BJTs. In lateral pnp transistors, in-plane longitudinal compressive stress and in lateral npn transistors out-of-

plane compressive stress showed significant improvement in Ic, β, f_T and f_{max}. Overall results indicated a promising opportunity for strain engineering in both vertical and lateral Si BJTs.

This study facilitated ideas for stress mitigation as well. The bipolar transistors showed different stress sensitivity for different stress-current orientations. The injection limited structures were found to be more sensitive to stress in both npn and pnp BJTs. Vertical npn transistors on (100) plane showed high stress sensitivity over vertical npn on (111) plane. The stress sensitivity of vertical pnp transistors on (100) planes were much less than the stress sensitivity of the vertical npn transistors on (100) planes or (111) planes. However, the lateral pnp transistors on (100) plane also showed high stress sensitivity for in-plane longitudinal and transverse stresses. Using the less stress sensitive BJTs is one method for stress mitigation in precision analog circuits. Spice simulation was used to model the stress effects in analog circuits. With the use of the theoretical 1-D models we were able to successfully model the stress effects in analog circuits and provided some stress mitigation techniques. These information will help in mitigating the unfavorable stress effects in analog circuits.

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Appendix A - Doping profile

Following is an example of the profile of a bipolar transistor used in this research study. The impurity distribution in the emitter (N_E), base (N_B) and the sub-collector (N_{SC}) are approximately given by Gaussian distribution and the collector impurity profile (N_{Col}) is taken as constant as follows:

Emitter profile

$$N_e(i) = 3\text{x}10^{19}\exp\left(\frac{\text{i - 320}}{320}\right)^2 \quad \text{(A.1)}$$

Base profile

$$N_b(i) = 5\text{x}10^{17}\exp\left(\frac{\text{i - 1000}}{300}\right)^2 \quad \text{(A.2)}$$

Collector profile

$$N_{Col}(i) = 1\text{x}10^{16} \quad \text{(A.3)}$$

Sub-collector profile

$$N_{sc}(i) = 5\text{x}10^{19}\exp\left(\frac{\text{i - 3000}}{100}\right)^2 \quad \text{(A.4)}$$

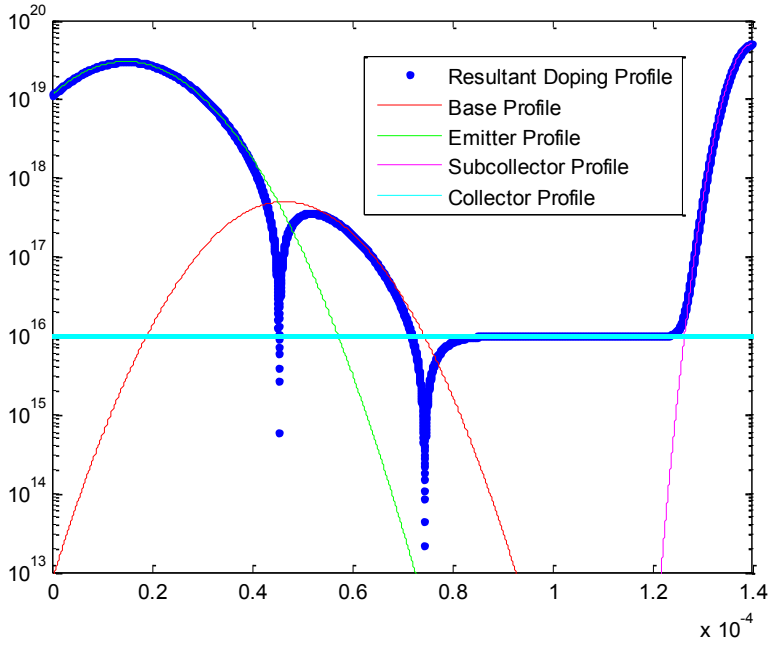

Figure A.1 – Impurity profile of a bipolar transistor using analytical equations

where the entire 1-D bipolar transistor is divided into N sections and i is the node. N_e, N_b, N_{sc}, N_c are the doping profile of emitter, base, collector and sub-collector respectively. The resultant doping profile have been calculated using the equation $N= N_e-N_b+N_c+N_{bc}$. Figure A.1 shows the impurity profiles obtained from above equations.

Appendix B - Current crowding effects in 2-D and 3-D simulations

The sheet resistance of the base underneath the emitter R_S is given by:

$$R_S = \frac{1}{\int_{x_e}^{x_c} q\mu_p N dx} \cong \frac{1}{qp\mu_p t} \tag{B.1}$$

Refer the front view of a 2-D bipolar transistor used for simulations is shown in Figure B.1. The following approximate values have been assumed for the calculation of sheet resistance.

base width	t	=	75 nm
average base doping	N	=	1e17
hole mobility	μ_p	=	250 $cm^2/(V.s)$

Plugging these values in the sheet resistance equation the approximate sheet resistance of the transistor has been calculated as 33.33 kΩ. This is considerably high value for sheet resistance as what we would expect in modern submicron transistors since the base width is very thin. Due to high sheet resistance, lateral voltage drop and the resultant current crowding effect cannot be neglected. It can be modeled as follows:

Current crowding effects in 2-D analysis

In 2D analysis current crowding can be approximated by putting number of 1-D transistors in parallel coupled through bias-dependent base resistances. In this study the 2-D transistor was modelled with 10 bipolar transistors in parallel as shown in Figure B.1. R is the resistance between the base of two adjacent transistors and R_1 is the resistance between the contact and the first transistor. The resistance R and R_1 have been calculated using

$$R = R_S \frac{L}{W} \tag{B.2}$$

where L=0.2 μm and w=1 μm. The resistance R and R_1 have been obtained as R = 666.67Ω, R1 = 333.33Ω.

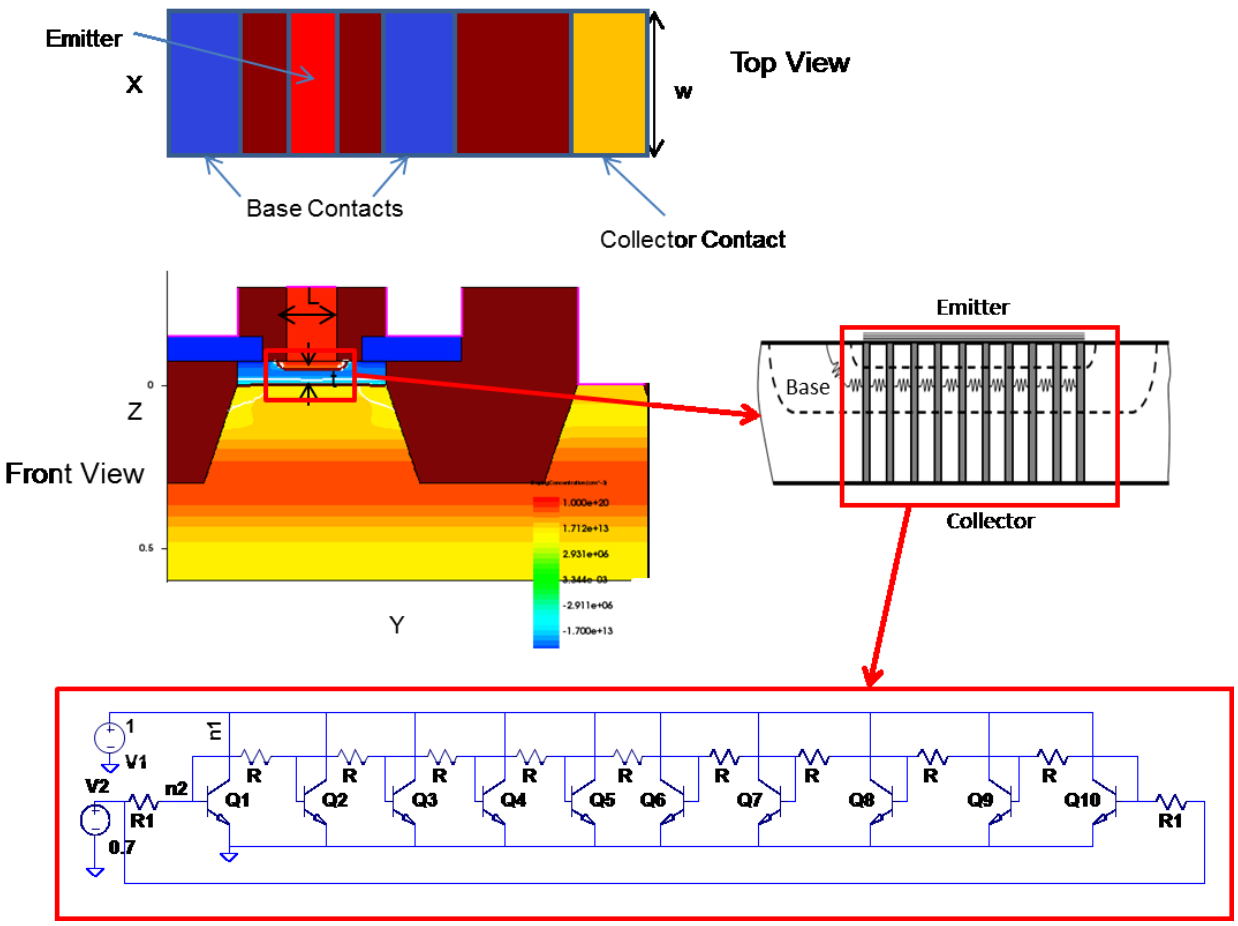

Figure B.1 – Modeling the 2-D npn transistor with 10 parallel 1-D transistors

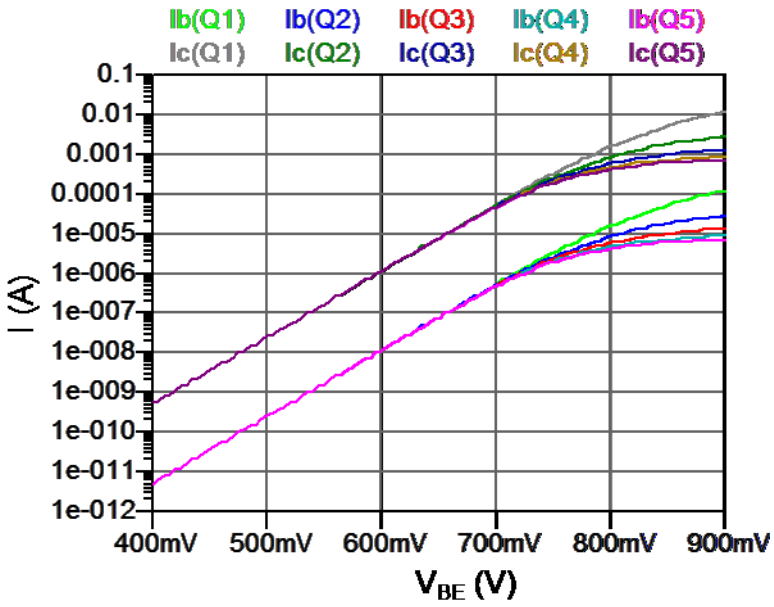

Figure B.2 – I_B, I_C Vs. V_{BE} showing current crowding effect of 2-D analysis

The spice simulation results in Figure B.2 show the current crowding effect for higher voltages. At high base-emitter voltages the base current increases in transistors Q_5 to Q_1 and Q_6 to Q_{10} (from center to the edge in both sides). This is also illustrated with the contour plots in Figure B.3. The figures clearly show the internal lateral distribution of current in the base. At high voltages the current is flowing close to the contact and the effective base resistance is reduced. It also shows that there is no change in current along Y direction. These differences in current distribution are the reason for the slight difference in stress response for σ'_{11} and σ'_{22} for the vertical transistors in npn (100) plane.

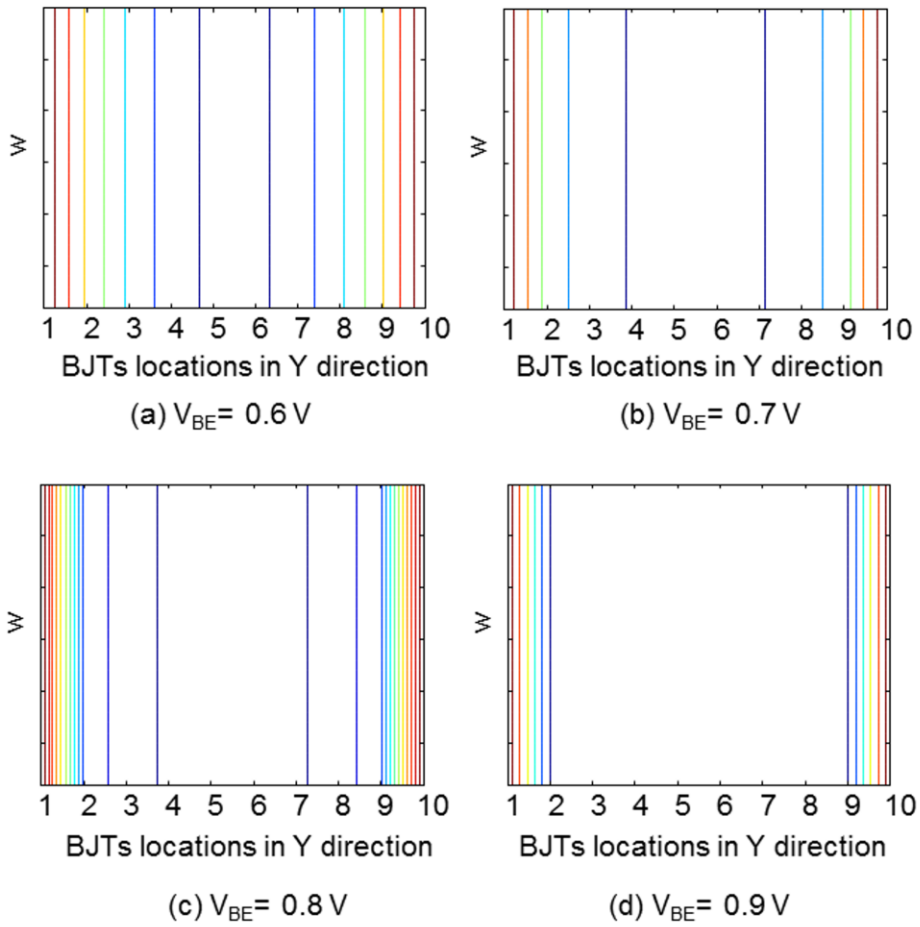

Figure B.3 – Contour plots of I_B showing the current crowding effect at high current (Top view) (a) at V_{BE}= 0.6 V current is distributed to all transistors and current crowding effect is slightly observed (b) at V_{BE}= 0.7 V current distribution is moving towards the contacts (c) at V_{BE}= 0.8 V current distribution is further moving towards the contacts, and (d) at V_{BE}= 0.9 V almost all the current is distributed to the transistors close to the contact.

Current crowding effects in 3D analysis

For 3-D analysis assuming L = 0.2 μm and w = 0.5 μm (half), an array of 50x10 transistors have been used to approximate the current crowding effect as shown in Figure B.4 where R = 33.33 kΩ, R1 = 16.67 kΩ.

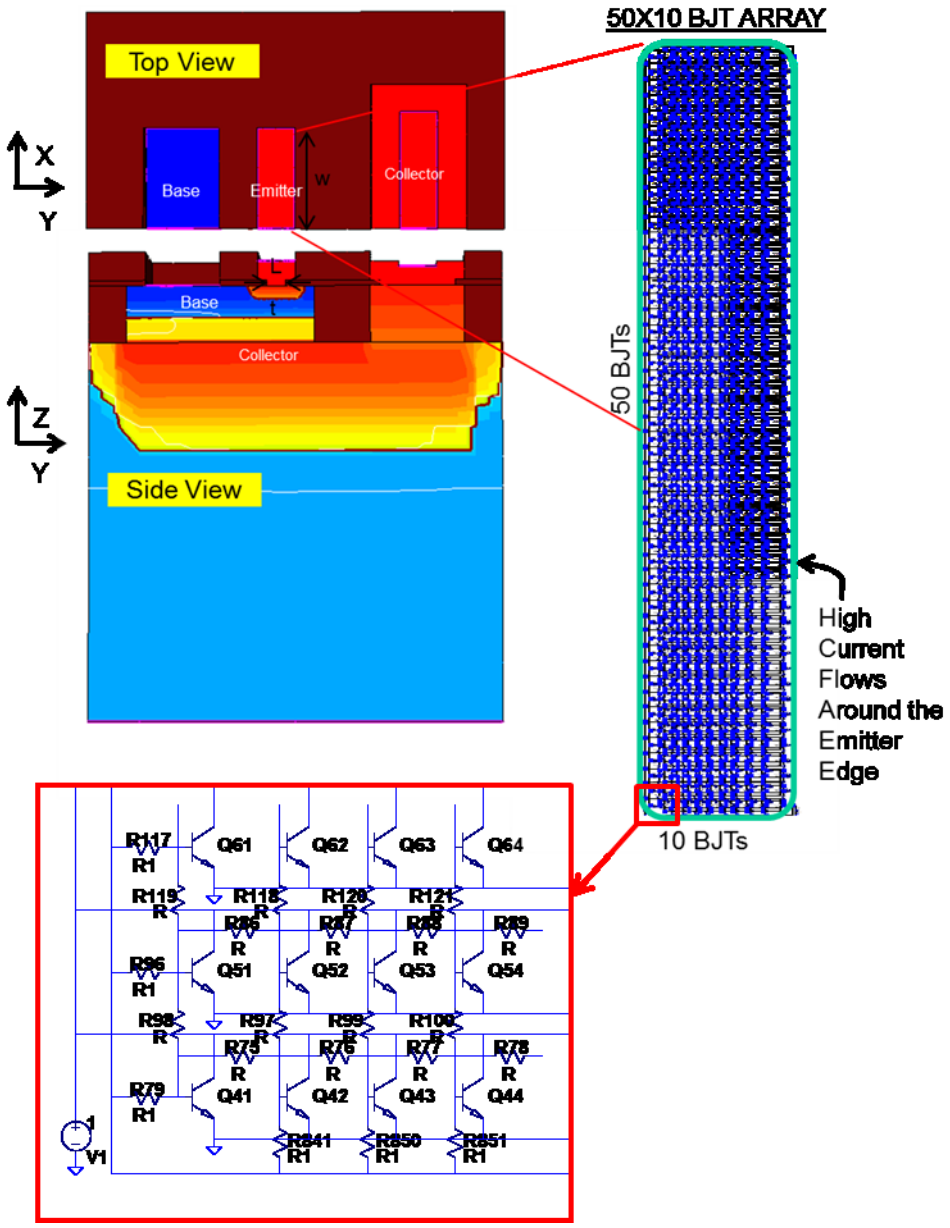

Figure B.4 – Modeling the 3-D npn transistor with several parallel 1-D transistors

As shown in the spice simulation results in Figure B.5 the current crowding is even more in 3-D analysis since the non-uniform distribution occurs in X, Y both directions. The current crowding is visible from 0.7 V in Figure B.2 (2-D analysis) whereas it is visible from 0.6 V in Figure B.5 (3-D analysis).

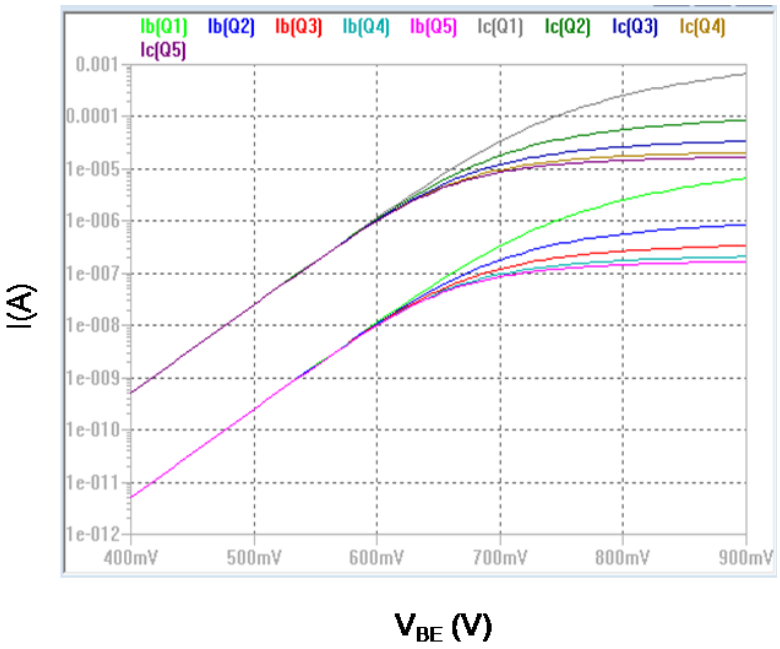

Figure B.5 – I_B, I_C Vs. V_{BE} showing current crowding effect of 3D analysis

The contour plot (Figure B.6) and the mesh plots (Figure B.7) show the non-uniform current distribution under the emitter. High current flow observed at the corner of the emitter-base junction around the emitter. Effective internal lateral current distribution in X, Y direction is also slightly different due to the current crowding effect.

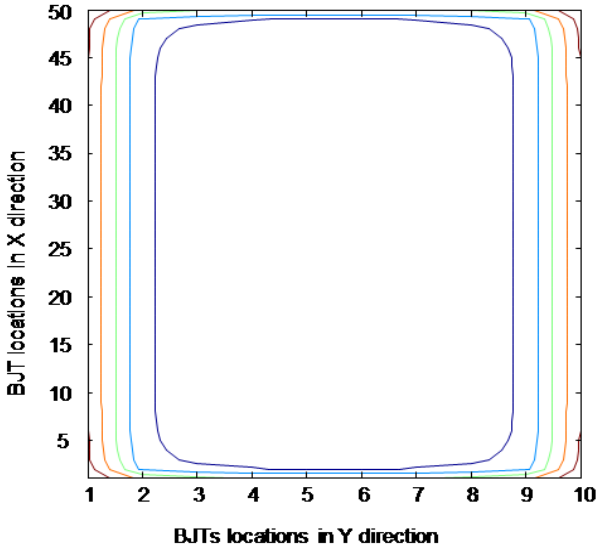

Figure B.6 – Contour Plot of I_B for V_{BE} = 0.8 V showing the current crowding effect (not to scale)

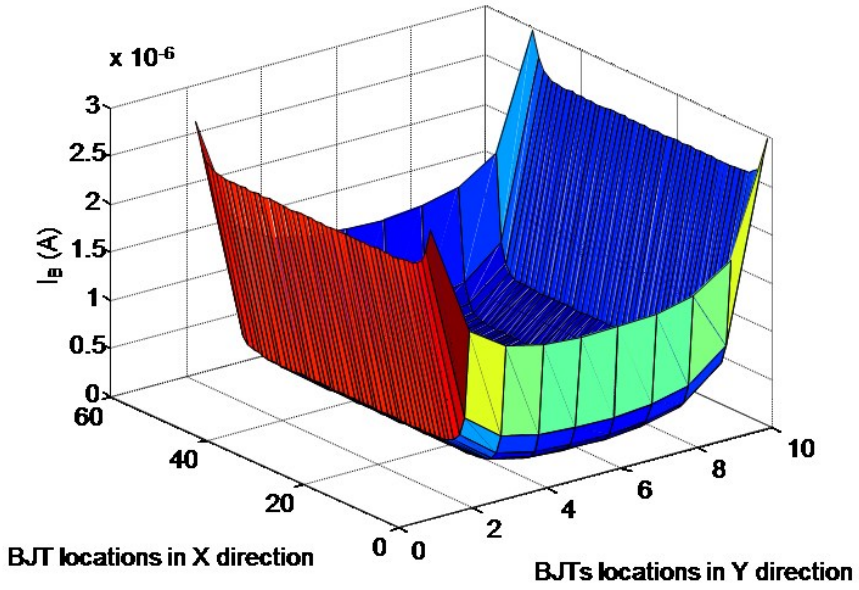

Figure B.7 – Mesh plot of I_B for V_{BE} = 0.8 V showing current crowding effect (not to scale)

Appendix C - MATLAB Code of 1-D npn bipolar transistor model

```
clear all; format compact;format short g; warning off;
ni0 = 1.48e10; VT = 0.0258; q = 1.59e-19; eps = 1.04e-12;  %eo*eSi F/cm
q_eps=q/eps; N=1500; %L=5.5e-4; %[54] Sentaurus profile
L=1.4e-4; %[54]
x=linspace(0,L,N); %
dx=L/N; maxite=1000;
betae=1.109;  betap=1.213; vsate=1.07e7; vsatp=8.37e6;    % velocity model
mumaxn=1417; zeta_n=2.5; T=300; mumaxp=470.5; zeta_p=2.2;   %mobility model

settingImpurityProfiles; %from analytical equations
% if input profile is from other source
% BJT=xlsread('profile_gain180.xlsx');
% x=BJT(:,1); ND=BJT(:,2); QQ=BJT(:,3); Ntotal=BJT(:,4);

V=zeros(1,N); VV=zeros(1,N);   %potential
EE=zeros(1,N);
Ne=zeros(1,N); Nb=zeros(1,N); Nc=zeros(1,N);  % impurity profiles
nvel=zeros(1,N); pvel=zeros(1,N);  % velocity
veff=zeros(1,N); veffp=zeros(1,N); veffp2=zeros(1,N);
Jn=0;
Jn=Jn*ones(1,N); %electron current density
Jp=zeros(1,N);   %hole current density
%Jrr=zeros(1,N);
RR=zeros(1,N);
%tt=zeros(1,N); dtt=zeros(1,N); %lifetime
nn=zeros(1,N); dnn=zeros(1,N);
znn=zeros(1,N); zpp=zeros(1,N); zpp1=zeros(1,N); zn=zeros(1,N); zp=zeros(1,N);
HQFP=zeros(1,N); EQFP=zeros(1,N);
%mobility model parameters
mumin1_n=52.2; mumin2_n=52.2; mu1_n=43.4; Pc_n=0; Cr_n=9.68e16; Cs_n=3.43e20; alpha_n=0.68; beta_n=2;
mumin1_p=44.9; mumin2_p=0; mu1_p=29.0; Pc_p=9.23e16; Cr_p=2.23e17; Cs_p=6.10e20; alpha_p=0.719;
beta_p=2;
muconst_n=mumaxn*(T/300)^zeta_n;
muconst_p=mumaxp*(T/300)^zeta_p;
%piezoconductance values
pi11_n=900e-12; pi12_n=-455e-12; pi44_n=150e-12; pi11_p=-25e-12; pi12_p=8e-12; pi44_p=-700e-12;

f1=figure(1); clf; f2=figure(2); clf; f5=figure(5); clf; f8=figure(8); clf; f10=figure(10); clf;
f14=figure(14); clf; f19=figure(19); clf; f21=figure(21); f22=figure(22); clf;

VBC=0.80; VB=0; Vbe=0.695;
Stress=11; nos=6; ss=30e6; plane=100; sdir=110; % nos-no of steps ss-step size

for a=1:nos
   nth=a;
   %stress dependant mobility
   [mu_n] = mobility(plane,nth,Stress,nos,ss,pi11_n,pi12_n,pi44_n);
   [mu_p] = mobility(plane,nth,Stress,nos,ss,pi11_p,pi12_p,pi44_p);
    % mu_n=1
    % mu_p=1
    %stress dependant intrinsic carrier concentration
```

```
[ni] = bandgap1(plane,nth,Stress,nos,ss,ni0);
%ni=ni0;

%bandgap narrowing
i=1:N;
Eref=6.92e-3; Nref=1.3e17; DEgFermi=0;
DEg0(i)=Eref*(log(Ntotal(i)./Nref)+sqrt((log(Ntotal(i)./Nref)).^2+0.5));
Ebgn(i)=DEg0(i)+DEgFermi;
ni(i)=ni*exp(Ebgn(i)./(2*VT));

%canali model & stress dependant
for i=1:N
   munn(i)=mumin1_n*exp(-Pc_n./Ntotal(i))+(muconst_n-mumin2_n)./(1+(Ntotal(i)/Cr_n).^alpha_n)+
mu1_n./(1+(Cs_n./Ntotal(i)).^beta_n);
   mun1(i)=munn(i)*mu_n;
   mupp(i)=mumin1_p*exp(-Pc_p./Ntotal(i))+(muconst_p-mumin2_p)./(1+(Ntotal(i)/Cr_p).^alpha_p)+
mu1_p./(1+(Cs_p./Ntotal(i)).^beta_p);
   mup1(i)=mupp(i)*mu_p;
end;

aQQ=abs(QQ); sQQ=sign(QQ);
%fermi potential calculations
for i=1:N
   Vf(i)=sQQ(i)*VT*log(aQQ(i)/ni(i));
   Vdf(i)=Vf(i);  if sQQ(i)<0,  Vdf(i)=-Vf(i); end;
end;
V=Vf;
figure(f1); semilogy(x,aQQ, 'b'); hold on; axis([0 L 1e14 1e20]);
figure(f2); plot(x,Vf,'g'); hold on; plot(x,Vdf,'r'); hold on; title('Fermi potential');axis([0 L -0.6 0.6]);
legend('Fermi Potential', 'Absolute Value of Fermi Potential'); grid on;

%junction location calculation
JunLoc = LocJunction(QQ);
JunLocx1=x(round(JunLoc(1))); JunLocx2=x(round(JunLoc(2)));

% equilibrium carrier concentration calculations
for i=1:N
   sr=sqrt(aQQ(i).^2+4*ni(i)^2);
   znn(i)=0.5*(sr+aQQ(i)); zpp(i)=ni(i)^2/znn(i);
   if i> JunLoc(1)  && i< JunLoc(2), zpp(i)=0.5*(sr+aQQ(i)); znn(i)=ni(i)^2/zpp(i); end;
end;
figure(f8); axis([0 L 1e0 1e20]); semilogy(x,znn, 'b'); hold on; semilogy(x,zpp, 'r'); hold on;

%Poisson eqn for BC junction
i_junct2=JunLoc(2);
junction_bc=round(i_junct2);
Vbi_bc=0.80;
w_junct2=sqrt(2*eps*(VBC+Vbi_bc)/(q*1e16))/dx;
Estart=0; Estop=0; Vstart=0; Vdesired=VBC; maxiter=10;
[Vn,i_end2,En] = VoltIter2(maxiter, Vdesired, q_eps,dx,Vdf, QQ, w_junct2, i_junct2, Estart,  Vstart, Estop, ni,
VT);

%Poisson eqn for BE junction
i_junct1=JunLoc(1);
Vbi_be=0.80;
w_junct1=sqrt(2*eps*(Vbi_be-Vbe)/(q*1e16))/dx;
```

```
   Estart=0; Estop=0; Vstart=0; Vdesired=-Vbe; maxiter=50;
  [Vexternal,i_start1,i_end1, Vbi] = VoltIter3(maxiter, Vdesired, q_eps,dx, Vdf, QQ, w_junct1, i_junct1, Estart,
Vstart, Estop, ni,VT);

  %load calculated potential & electric field
   load vvee
   v2 = v2 + Vf(idx2(length(idx2)));
   VV(idx2)=v2;
   i_start2=idx2(1); i_end2=idx2(length(idx2));
   v3 = v3 + Vf(idx3(1));
   VV(idx3)=v3;
   i_start1=idx3(1); i_end1=idx3(length(idx3));

   %calculate entire Electrostatic potential
   id1=1:i_end1; id2=i_start1:i_end2; id3=i_start2:N;
   VE=VB-Vbe;
   for i=1:i_end1-1
      VV(i)=Vf(i)+VE;
   end;
   ii=i_start1:i_end2;
   VV(ii)=Vf(ii);
   for i=i_start2:N,
      VV(i)=Vf(i)+VBC;
   end;
   r=5;
   xx1=linspace(1,N,N);
   ii1=(1:i_end1-r*2); ii2=(i_end1+r*2:i_start1-r); ii3=(i_start1+r:i_end2-r*2); ii4=i_end2+r*4:i_start2-r*7;
ii5=i_start2+r*3:N;
   C2=reshape([ii1 ii2 ii3 ii4 ii5],1,[]);
   VVV=VV(C2);
   VVV=spline(C2,VVV,xx1);

   %calculate entire E field
   for i=1:N-1
      EE(i)=(VVV(i)-VVV(i+1))/dx;
   end;
   figure(13); plot(x(1:end),EE,'b'); hold on; title('Electric Field'); grid on; legend('1D model'); %axis([0 L -5e4
3e4]);

   %calculate field dependant velocity
   for j=1:N
      v1=abs(-mun1(j)*EE(j));
      v2=vsate;
      mun(j)=mun1(j)/(1+(v1/v2)^betae)^(1/betae);
      veff(j)=abs(-mun(j)*EE(j));

      v1p=abs(mup1(j)*EE(j));
      v2p=vsatp;
      mup(j)=mup1(j)/(1+(v1p/v2p)^betap)^(1/betap);
   end;

   % solving e transport for base
   no=znn(i_start1);
   znn(i_start1)=no*exp(Vbe/VT);
   znn_o=znn(i_start1);
   istart=i_end2; A=1;  step = 10; Jn(istart:i_start2)=0;
```

```
tpb=1e-7; tnb=tpb;
%vol=dx*A;

for ite5=1:maxite
    Jn(istart:i_start2) = Jn(istart:i_start2)+step;
    znn(i_end2:i_start2)=(1/q)*(Jn(istart)./veff(i_end2:i_start2));
    Jrr=0;
    for i=istart:-1:i_start1
        dV=-(VVV(i+1)-VVV(i))/VT;
        vdifn= mun(i+1)*VT/dx;
        ndif=Jn(i+1)/(q*vdifn);
        R=((znn(i+1)*zpp(i+1)-ni(i+1)^2)/(tpb*(znn(i+1)+ni(i+1))+tnb*(zpp(i+1)+ni(i+1))));
        Jr=q*R*A*dx;
        %fprintf('znn=%10e, zpp=%10e, R=%10e \n',znn(i+1),zpp(i+1),R);
        Jn(i)=Jn(i+1)+Jr;
        Jp(i)=Jr;
        Jrr=Jrr+Jr;
        %fprintf('i=%4d R=%10e, Jr=%15.8f Jn=%15.8f\n',i,R,Jr,Jn(i+1));
        dVmin=1e-10;
        if abs(dV)<dVmin,  if dV>=0, dV=dVmin;  else dV=-dVmin; end; end;
        gamma=exp(dV);
        delta=(gamma-1)/dV;
        nn2= znn(i+1);
        nn1=nn2*gamma+ndif*delta;
        %fprintf('gamma=%8.4f, delta=%8.4f, ndif=%9e, nn2=%9e, nn1=%9e\n',gamma,delta,ndif, nn2, nn1);
        znn(i)= nn1;
        RR(i)=R;
    end;
    if abs(znn(i_start1)-znn_o)<1e2
        break;
    elseif znn(i_start1)>znn_o
        Jn(istart:i_start2) = Jn(istart:i_start2) - step;
        step = step/10;
    elseif znn(i_start1)<znn_o
        continue
    end;
end;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% e transport for BC depletion
Jnn=Jn(i_end2);
    for i=i_start2:-1:i_end2
        dV=-(VVV(i+1)-VVV(i))/VT;
        vdifn= mun(i)*VT/dx;
        ndif=Jnn/(q*vdifn);
        dVmin=1e-10;
        if abs(dV)<dVmin,  if dV>=0, dV=dVmin;  else dV=-dVmin; end; end;
        gamma=exp(dV);
        delta=(gamma-1)/dV;
        nn2= znn(i+1);
        nn1=nn2*gamma+ndif*delta;
        znn(i)= nn1;
    end;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Irb(a)=Jrr;
```

```
% h transport for emitter
Jn(i_end1:i_start1)=Jn(i_start1);
Jn(i_end2:N)=Jn(i_end2);
Jn(1:i_end1-1)= Jn(i_end1);
for i=i_start1:i_start2
   nvel(i)=Jn(i)/(q*znn(i));
end;

po=ni(i_end1).^2/aQQ(i_end1);
zpp_o=po*exp(Vbe/VT);
zpp(1)=ni(1).^2/aQQ(1);

Jp(1)=0; step = 0.1; tne=1e-8; tpe=tne;
for ite3=1:maxite
   Jp(1) = Jp(1)+step;
   for i=1:i_end1
      dV=(-VVV(i+1)+VVV(i))/VT;
      R1=((znn(i)*zpp(i)-ni(i)^2)/(tpe*(znn(i)+ni(i))+tne*(zpp(i)+ni(i))));
      Jr=q*R1*A*dx;
      Jp(i+1)=Jp(i)+Jr;
      %Jr(i)=Jr;
      Jn(i+1)=Jn(i)-Jr;
      %fprintf('i=%4d R1=%10e, Jr=%15.8f Jp=%15.8f\n',i,R1,Jr,Jp(i+1));
      dVmin=1e-10;
      if abs(dV)<dVmin,  if dV>=0, dV=dVmin;  else dV=-dVmin; end; end;
      gamma=exp(dV);
      delta=(gamma-1)/dV;
      pp1= zpp(i);
      vdifp= ((mup(i)+mup(i+1))/2)*VT/dx;
      pdif=((Jp(i)+Jp(i+1))/2)/(q*vdifp);
      pp2=pp1*gamma+pdif*delta;
      %fprintf('gamma=%8.4f, delta=%8.4f, pdif=%9e, pp2=%9e, pp1=%9e\n',gamma,delta,pdif, pp2, pp1);
      zpp(i+1)= pp2;
   end;
   err=zpp(i_end1)-zpp_o;

   if abs(err)<1e2
      break;
   elseif zpp(i_end1)-zpp_o>0;
      Jp(1) = Jp(1) - step;
      step = step/10;
   elseif zpp(i_end1)-zpp_o<0;
      continue;
   end;
   ite3;
end;

for i=1:i_end1;
   Jn(i)=Jn(i)+Jp(i_end1)-Jp(1);
end;

Jpemitter=Jp(i_end1);
Ipe(a)=Jp(i_end1);
Ipei(a)=Jp(1);
Iper(a)=Jp(i_end1)-Jp(1);
```

```
% h transport for collector
zpp_N=zpp(N);
Jpend2=0; Jp(i_end2:N)=Jpend2; step = 0.1;

for ite6=1:maxite
   Jp(i_end2:N) = Jp(i_end2:N)+step;
   for i=i_end2:N-1
      dV=(-VVV(i+1)+VVV(i))/VT;
      dVmin=1e-10;
      if abs(dV)<dVmin,  if dV>=0, dV=dVmin;  else dV=-dVmin; end; end;
      gamma=exp(dV);
      delta=(gamma-1)/dV;
      pp1= zpp(i);
      vdifp= mup(i+1)*VT/dx;
      pdif=Jp(i+1)/(q*vdifp);
      pp2=pp1*gamma+pdif*delta;
      %fprintf('gamma=%8.4f, delta=%8.4f, pdif=%9e, pp2=%9e, pp1=%9e\n',gamma,delta,pdif, pp2, pp1);
      zpp(i+1)= pp2;
   end;
   if abs(zpp(N)-zpp_N)<1e2   %2
      break;
   elseif zpp(N)>zpp_N
      Jp(i_end2:N) = Jp(i_end2:N) - step;
      step = step/10;
   elseif zpp(N)<zpp_N
      Jp(i_end2:N) = Jp(i_end2:N) + step;
      continue;
   end;
   ite6;
end;

i1=(1:i_end1-5); i2=(i_start1+5:i_end2-5); i3=(i_end2+5:N); i4=(round(JunLoc(2))+5:N); i5=i_start1+5:N;
C1=reshape([i1 i5],1,[]);
znn1=znn(C1);
znn=spline(C1,znn1,xx1);
zpp1=zpp(C1);
zpp=spline(C1,zpp1,xx1);

figure(f14); plot(x,Jn,'b'); hold on; plot(x,Jp,'r'); hold on; title('Electron Current Density, Hole Current Density')
legend('electron current density','hole current density');

for i=1:N
   HQFP(i)=VT*log(zpp(i)/ni(i))+VVV(i);
   EQFP(i)=VVV(i)-VT*log(znn(i)/ni(i));
end;

C3=reshape([i1 i2 i4],1,[]);
AP=HQFP(C3);
AE=EQFP(C1);
yp=spline(C3,AP,xx1);
ye=spline(C1,AE,xx1);

figure(f10); axis([0 L -1 1.5]); plot(x,VVV,'b'); hold on;
plot(x,ye,'m'); hold on; plot(x,yp,'r'); hold on;
axis([0 L -1 1.5]);
legend('EP 1D model', 'EQFP 1D model', 'HQFP 1D model');
```

```
    xlabel('Distance from emitter contact (cm)');
    ylabel('EP, EQFP, HQFP (V)');

    for i=1:N
       p(i)=ni(i)*exp((yp(i)-VVV(i))/VT);
       n(i)=ni(i)*exp((VVV(i)-ye(i))/VT);
    end;
    for i=1:N
       peff(i)=Jp(i)/(q*zpp(i));
       if peff(i)>1e7 peff(i)=vsatp; end;
    end;
    for i=1:N
       neff(i)=Jn(i)/(q*n(i));
    end;
    figure(f5); axis([0 L 0 1.1e7]); plot(x,neff, 'b'); hold on; axis tight;
    figure(f19); axis([0 L 0 1.1e7]); plot(x, peff,'b'); hold on;
    title('Hole Velocity'); legend('emitter', 'base', 'collector','h velocity 1D Model');
    figure(f8); axis([0 L 1e0 1e20]); semilogy(x, zpp, 'k'); hold on; semilogy(x, znn, 'g'); hold on;
    legend('n-type impurity profile','p-type impurity profile','h concen 1D model', 'e concen 1D model');
    xlabel('Distance from emitter contact (cm)');
    ylabel('Concentration (cm^-^3)');

    Jpe=Jp(i_end1);
    Jrr;
    JB=Jrr+Jpe;
    JC=Jn(i_end2);
    Ib(a)=JB;
    Ic(a)=JC;
    beta(a)=JC/JB
    dIper_o_Iper(a)=(Iper(a)-Iper(1))/Iper(1);
    dIpei_o_Ipei(a)=(Ipei(a)-Ipei(1))/Ipei(1);
    dIpe_o_Ipe(a)=(Ipe(a)-Ipe(1))/Ipe(1);
    dIrb_o_Irb(a)=(Irb(a)-Irb(1))/Irb(1);
    db_o_b(a)=(beta(a)-beta(1))/beta(1);
    dIb_o_Ib(a)=(Ib(a)-Ib(1))/Ib(1);
    dIc_o_Ic(a)=(Ic(a)-Ic(1))/Ic(1);
end;

j=1:nos;
xx=((j-1)*ss);
n1=2;
n2=2;

pIper=polyfit(xx/1e6,dIper_o_Iper,n2);
pIpei=polyfit(xx/1e6,dIpei_o_Ipei,n2);
pIpe=polyfit(xx/1e6,dIpe_o_Ipe,n2);
pIrb=polyfit(xx/1e6,dIrb_o_Irb,n2);
p=polyfit(xx/1e6,db_o_b,n2);
pIb=polyfit(xx/1e6,dIb_o_Ib,n2);
pIc=polyfit(xx/1e6,dIc_o_Ic,n2);
xfit=xx/1e6;

yIperfit=polyval(pIper,xfit);
yIpeifit=polyval(pIpei,xfit);
yIpefit=polyval(pIpe,xfit);
yIrbfit=polyval(pIrb,xfit);
```

```
yfit=polyval(p,xfit);
yIbfit=polyval(pIb,xfit);
yIcfit=polyval(pIc,xfit);

figure(f21);
plot(xfit,yIbfit,'-g'); hold on; plot(xfit,yIcfit,'-b'); hold on; plot(xfit,yfit,'-r'); grid on; hold on;
axis([-200 200 -0.15 0.15]);
legend('I_B Simulation','I_C Simulation','\beta Simulation');
xlabel('Applied Stress, \sigma[110](MPa)');
ylabel('\Delta\beta/\beta, \DeltaI_C/I_C, \DeltaI_B/I_B');

figure(f22); plot(xfit,yIbfit,'*-g'); hold on; plot(xfit,yIrbfit,'.-m'); hold on; plot(xfit,yIpefit,'.-k'); hold on;
plot(xfit,yIpeifit,'*-c'); hold on; plot(xfit,yIperfit,'-r'); hold on;
xlabel('Stress, \sigma (MPa)');
ylabel('Change in Base Current Components');
legend('\DeltaI_B/I_B','\DeltaI_B_R_/I_B_R','\DeltaI_B_E_I/I_B_E_I','\DeltaI_B_E_R/I_B_E_R');
axis([0 150 -0.020 0.005]); grid on;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% settingImpurityProfiles;
scale=N/3000;
for i=1:N    % setting imputity profile and initial conditions
    ix=i/scale;
            Ne(i)= 3e19* exp(- ((ix-320)/320)^2);     %gaussian profile
            Nb(i)= 5e17* exp(- ((ix-1000)/300)^2);    %gaussian profile
            Nbc(i)= 5e19* exp(- ((ix-3000)/100)^2);    %gaussian profile
            Nc=1e16;
    QQ=Nc+Ne+Nbc-Nb;
    Ntotal=Nc+Ne+Nb+Nbc;
    aQQ=abs(QQ); sQQ=sign(QQ);
    Vf(i)=sQQ(i)*VT*log(aQQ(i)/ni0);
    Vdf(i)=Vf(i);  if sQQ(i)<0,  Vdf(i)=-Vf(i); end;
end;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%functions
function JunLoc = LocJunction(QQ)
% locate the junctions
[m,n]=size(QQ);
j=0;
for i=1:n-1,
    if sign(QQ(i))*sign(QQ(i+1)) <=0,
        j=j+1;
        Q1=QQ(i);
        Q2=QQ(i+1);
        JunLoc(j)=i+abs(Q1/(Q1-Q2));
    end
end;
return;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function [26] = mobility(plane,nth,Stress,nos,ss,pi11,pi12,pi44)
switch(plane)
    case 100
        l1=cosd(45); m1=cosd(45); n1=cosd(90); l2=cosd(135); m2=cosd(45); n2=cosd(90); l3=cosd(90);
m3=cosd(90); n3=cosd(0);
    case 111
        l1=-1/sqrt(2); m1=1/sqrt(2); n1=0; l2=-1/sqrt(6); m2=-1/sqrt(6); n2=2/sqrt(6); l3=1/sqrt(3); m3=1/sqrt(3);
n3=1/sqrt(3);
```

```
end;
pi=[pi11 pi12 pi12 0 0 0;
   pi12 pi11 pi12 0 0 0;
   pi12 pi12 pi11 0 0 0;
   0 0 0 pi44 0 0;
   0 0 0 0 pi44 0;
   0 0 0 0 0 pi44];
sigma11b=zeros(1,nos)'; sigma22b=zeros(1,nos)'; sigma33b=zeros(1,nos)'; sigma12b=zeros(1,nos)';
sigma23b=zeros(1,nos)'; sigma13b=zeros(1,nos)';
j=1:nos;
d=((j-1)*ss)';
if Stress==11
   sigma11b=d;
   elseif Stress==22
   sigma22b=d;
   elseif Stress==33
   sigma33b=d;
   elseif Stress==13
   sigma12b=d;
   elseif Stress==23
   sigma23b=d;
   elseif Stress==12
   sigma13b=d;
end;
sigmab=[sigma11b sigma22b sigma33b sigma12b sigma23b sigma13b];
T=[l1^2 m1^2 n1^2 2*l1*n1 2*m1*n1 2*l1*m1;
   l2^2 m2^2 n2^2 2*l2*n2 2*m2*n2 2*l2*m2;
   l3^2 m3^2 n3^2 2*l3*n3 2*m3*n3 2*l3*m3;
   l1*l3 m1*m3 n1*n3 (l1*n3+l3*n1) (m1*n3+m3*n1) (l1*m3+l3*m1);
   l2*l3 m2*m3 n2*n3 (l2*n3+l3*n2) (m2*n3+m3*n2) (l2*m3+l3*m2);
   l1*l2 m1*m2 n1*n2 (l1*n2+l2*n1) (m1*n2+m2*n1) (l1*m2+l2*m1)];
Tinv=inv(T);
pi_b=T*pi*Tinv;
l=0; m=0; n=1;   %plane 100 ok
%l=1; m=0; n=0;
%l=0; m=1; n=0;
%l=cosd(0); m=cosd(90); n=0; %plane 100 ok
%l=0; m=0; n=1;   %plane 111 ok
%l=0; m=0; n=1;   %plane 111 ok
p=[l^2 m^2 n^2 l*n m*n l*m];
a=nth;
   b=sigmab(a,:)';
   mu(a)=(1+(pi_b*b)'*p');
mu=mu(a);
return;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function [nis] = bandgap1(plane,nth,Stress,nos,ss,ni)
ss=((nth-1)*ss/1e6);
b=70; % 180 npn 1  % 60 npn 2
nis=sqrt(ni*ni*(1-3.403e-4*(ss+b)+8.873e-7*(ss+b)^2));  % 110
%     nib=sqrt(ni*ni*(1-3.403e-4*(b)+8.873e-7*(b)^2));
%     nis=sqrt(nib*nib*(1-3.403e-4*(ss+b)+8.873e-7*(ss+b)^2 -(-3.403e-4*(b)+8.873e-7*(b)^2 ) ));  % 110
%nis=sqrt(ni*ni*(1-2.755e-4*(ss+b)+1.644e-6*(ss+b)^2));  % 010
%nis=sqrt(ni*ni*(1-3.387e-4*(ss+b)+5.285e-7*(ss+b)^2));  % 111
return;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
function [Vn,i_start, iend,En] = VoltIter2(maxiter, Vdesired, q_eps,dx,Vdf, QQ, w_junct, i_junct, Estart,  Vstart,
Estop,ni, VT);
i_start=i_junct+w_junct;
Vbif=2*Vdf(round(i_start));
Vdes=-Vdesired-Vbif;
[Vn,iend,En] = poissBMW2(q_eps,dx,QQ, i_start, Estart,  Vstart, Estop);
for iter=1:maxiter
   if sign(Vdes)~=sign(Vn), disp('ERROR Voltiter ==> voltages have different signs'); end;
   scal= sqrt(Vdes/Vn);
   w_junct=scal*w_junct;
   i_start=i_junct+w_junct;
   Vp=Vn;
   Vbif=VT*log(abs(QQ(round(i_start))*QQ(iend))/(ni(iend)*ni(round(i_start))));
   Vdes=-Vdesired-Vbif;
   [Vn,iend,En] = poissBMW2(q_eps,dx,QQ, i_start, Estart,  Vstart, Estop);
   dV=Vn-Vp;
   Vn;
   iter;
   Vexternal=Vn+Vbif;
   if abs(dV)< 0.0001,
%        iter, dV,
      break;
   end;
end;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function [Vexternal,i_start,iend, Vbif] = VoltIter3(maxiter, Vdesired, q_eps,dx,Vdf, QQ, w_junct, i_junct, Estart,
Vstart, Estop, ni, VT);
i_start=i_junct+w_junct;
Vbif=2*Vdf(round(i_start));
Vdes=Vdesired+Vbif;
[Vn,iend] = poissBMW3(q_eps,dx,QQ, i_start, Estart,  Vstart, Estop);
for iter=1:maxiter
   if sign(Vdes)~=sign(Vn), disp('ERROR Voltiter ==> voltages have different signs');end;
   %scal= sqrt(Vdes/Vn);
   scal= (Vdes/Vn)^(1/3);
   w_junct=scal*w_junct;
   i_start=i_junct+w_junct;
   Vp=Vn;
   Qstart=QQ(round(i_start));
   Vbif=VT*log(abs(QQ(round(i_start))*QQ(iend))/ (ni(iend)*ni(round(i_start))));
   test1=ni(iend);
   test2=ni(round(i_start));
   Vdes=Vdesired+Vbif;
   [Vn,iend] = poissBMW3(q_eps,dx,QQ, i_start, Estart,  Vstart, Estop);
   dV=Vn-Vp;
   Vn;
   iter;
   Vexternal=-Vn+Vbif;
   Vbif;
   if abs(dV)< 1e-4,
   %fprintf('iter=%8.0f, Vexternal=%8.4f, dV=%8.4f\n',iter,Vexternal, dV);
      break;
   end;
end;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function [Vn,iend,En] = poissBMW2(q_eps,dx,QQ, istart, Estart,  Vstart, Estop)
```

```
%fast without storing values
% allowes for fractional ivalues of istart and iend
Vp=Vstart;
iround=floor(istart); del = istart - iround;
Qf=QQ(iround)*(1-del)+QQ(iround+1)*del;
En1=Estart-q_eps*0.5*(QQ(iround)+Qf)*del*dx;  % trapezoid
Qff=0.75*QQ(iround)+0.25*QQ(iround-1);
Ep=En1-q_eps*Qff*dx*0.5; %En = Enext  Ep = Eprevious
sigE=sign(Ep);vv=[];ee=[];
for i=iround-1:-1:1     %poisson equation for depletion region  from right to lelt
    En=Ep-q_eps*QQ(i)*dx;    %   En=Ei  Ep=Ei-1      Vn=Vi  Vp=Vi-1
    Vn=Vp+ En*dx;
   if sigE*En<=Estop,  %this is correct
%        if En>Estop,
       del2=(Ep-Estop)/(Ep-En);
       Vn=Vp+ 0.5*(Ep+Estop)*del2*dx;
%        res=[istart, Vstart, Estart,Ep, En, Estop,Vn, Vp, del2];
       break;
    end;
    Ep=En; Vp=Vn;
    ee(i)=Ep;
    vv(i)=Vp;
end;
iend=i;
vv = vv - vv(iend+1);
%ee=ee+ee(iround-1);
%figure(6); plot(iround-1:-1:iend+1,vv(iround-1:-1:iend+1),'b');  title('Potential');
%figure(7);  plot(ee,'r');  title('Electric Field');hold on;
 load vvee
 idx2 = iround-1:-1:iend+1;
 v2 = vv(iround-1:-1:iend+1);
 e2 = ee(iround-1:-1:iend+1);
 save('vvee','idx2','v2','e2');
return;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function [Vn,iend] = poissBMW3(q_eps,dx,QQ, istart, Estart,  Vstart, Estop)
%fast without storing values
% allowes for fractional ivalues of istart and iend
Vp=Vstart;
iround=floor(istart); del = istart - iround;
Qf=QQ(iround)*(1-del)+QQ(iround+1)*del;
En1=Estart-q_eps*0.5*(QQ(iround)+Qf)*del*dx;  % trapezoid
Qff=0.75*QQ(iround)+0.25*QQ(iround-1);
Ep=En1-q_eps*Qff*dx*0.5; %En = Enext  Ep = Eprevious
sigE=sign(Ep);vv=[];ee=[];
for i=iround-1:-1:1     %poisson equation for depletion region  from right to lelt
    En=Ep-q_eps*QQ(i)*dx;    %   En=Ei  Ep=Ei-1      Vn=Vi  Vp=Vi-1
    Vn=Vp+ En*dx;
    if sigE*En<=Estop,
%        if En>Estop,
       del2=(Ep-Estop)/(Ep-En);
       Vn=Vp+ 0.5*(Ep+Estop)*del2*dx;
%        res=[istart, Vstart, Estart,Ep, En, Estop,Vn, Vp, del2];
       break;
    end;
    Ep=En; Vp=Vn;
```

```
    ee(i)=Ep;
    vv(i)=Vp;
end;
iend=i;
%vv = vv - vv(iround-1)
%ee=ee+Ef(iround);
%figure(6); plot(iround-1:-1:iend+1,vv(iround-1:-1:iend+1),'b');  title('Potential');
%figure(7);   plot(ee,'r');  hold on; title('Electric Field');
 load vvee
 %idx3 = (iround-1:-1:iend+1); % original
 idx3 = (iround-1:-1:iend+3);
 v3 = vv(idx3);
 e3 = ee(idx3);
 save('vvee','idx2','v2','e2','idx3','v3','e3');
return;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

Appendix D - Piezoresistive coefficients in Si

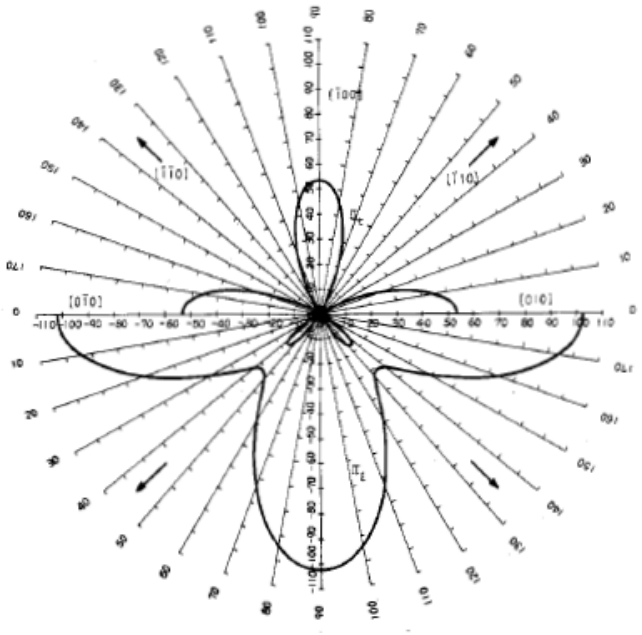

Figure D.1 – Room temperature piezoresistance coefficients in the (001) plane of n-Si (10^{-12} cm^2/dyne) [D.1].

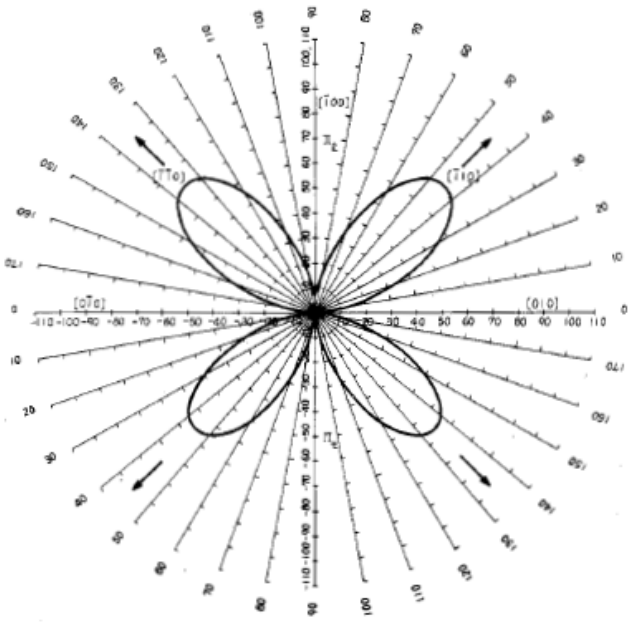

Figure D.2 – Room temperature piezoresistance coefficients in the (001) plane of p-Si (10^{-12} cm^2/dyne). [D.1]

Reference

D.1 Y. Kanda, "A graphical representation of the piezoresistance coefficients in silicon," *IEEE Transactions on electron devices,* vol. 29, pp. 64-70, 1982.

Appendix E - Spice Netlists for simulation of stress effects in analog circuits

1. Differential pairs

```
* I:\spice models\differential pair\differential pair.asc
.param BF=200 sxx=0 syy=0 szz=0 syz=0 sxz=0 sxy=0 pi_11nb=-900e-12 pi_12nb=450e-12 pi_11pe=20e-12
pi_12pe=-10e-12 npnb=200
Q1 0 N001 N002 [NC_01] NPN
Q2 0 0 N002 [NC_02] NPN
I1 N002 0 50uA
V1 N001 0 0
.model NPN NPN(IS={1e-14*(1-pi_12nb*sxx*1E6)} BF={npnb*(1-(pi_12nb-pi_12pe)*sxx*1E6)})
.model PNP PNP
.step param sxx 0 100 30
.op
.lib C:\PROGRA~2\LTC\LTSPIC~1\lib\cmp\standard.bjt
.backanno
.probe
.end
```

2. PTAT circuit

```
* I:\spice models\PTAT\PTAT.asc
.param N=0.9 pi_11nb=-900e-12 pi_12nb=450e-12 pi_11pe=20e-12 pi_12pe=-10e-12 npn_BF0=200
Q1 V1 V1 0 0 NPN1
Q2 V2 V2 0 0 NPN2
I1 0 V1 10µA
I2 0 V2 50µA
.model NPN1 NPN(IS={1e-14*(1-pi_12nb*sxx*1E6)} BF={npn_BF0*(1-(pi_12nb-pi_12pe)*sxx*1E6)})
.model NPN2 NPN(IS={1e-14*(1-pi_12nb*N*sxx*1E6)} BF={npn_BF0*(1-(pi_12nb-pi_12pe)*N*sxx*1E6)})
.model PNP PNP
.step param sxx 0 100 20
.op
.lib C:\PROGRA~2\LTC\LTSPIC~1\lib\cmp\standard.bjt
.backanno
.probe
.end
```

3. Op-amp circuit

```
* F:\bjt\spice models\simple oppamp.asc

.param BF=60 sxx=0 syy=0 szz=0 syz=0 sxz=0 sxy=0 x=1 pi_11nb=-1022e-12 pi_12nb=534e-12 pi_11pe=66e-12
pi_12pe=-11e-12 npnb=200 pi_11pb=66e-12 pi_12pb=-11e-12 pi_11ne=-1022e-12 pi_12ne=534e-12 pnpb=80
I1 q12E 0 100µA
V1 Q53E 0 15V
*XU1 q15C Q23C N001 0 Vout LT1001
XOP1    q15C Q23C       vout    OPAMP1

Q4 q15C 0 q12E 0 QNOMN
Q1 Q23C Vout q12E 0 QNOMN
Q2 q15C q15C Q53E 0 QNOMP
Q3 Q23C q15C Q53E 0 QNOMP
```

```
.model QNOMN NPN(BF={npnb*(1-(pi_12nb-pi_12pe)*(sxx+syy)*1E6-(pi_11nb-pi_11pe)*szz*1E6)})
.model QNOMP PNP(BF={pnpb*(1-(pi_12pb-pi_12ne)*(sxx+syy)*1E6-(pi_11pb-pi_11ne)*szz*1E6)} IS=1e-8)
.SUBCKT OPAMP1      1   2   6
* INPUT IMPEDANCE
RIN       1          2          10MEG
* GAIN BANDWIDTH PRODUCT = 10MHZ
* DC GAIN (100K) AND POLE 1 (100HZ)
EGAIN  3 0        1 2        100K
RP1       3          4          1K
CP1       4          0          1.5915UF
* OUTPUT BUFFER AND RESISTANCE
EBUFFER          5 0        4 0        1
ROUT   5          6          10
.ENDS

.step param sxx 0 120 30
.op
.lib LTC.lib
.backanno
.probe
.end
```

4. Bangap reference circuit

```
* I:\spice models\bandgap_ref_type_C.asc
.param BF=200 szz=0 syz=0 sxz=0 sxy=0 x=0.5 pi_11nb=-900e-12 pi_12nb=450e-12 pi_11pe=20e-12 pi_12pe=-
10e-12 npnb=200
.param pi11_p=20e-12 pi12_p=-10e-12 pi44_p=500e-12 pi=3.14159 fi=pi/4 lamda=1*pi/4

Q1 q1bc q1bc 0 0 NPN
Q2 q2bc q2bc 0 0 NPN
*R1 Vref r13 21.5k
*R2 Vref q2bc 4.3k
*R3 r13 q1bc 2.3k
R1 Vref r13 {21.5k*(1+s*1e6*(pi11_p*(0.5+0.5*cos(2*fi)*cos(2*lamda))+pi12_p*(0.5-
0.5*cos(2*fi)*cos(2*lamda))+pi44_p*(0.5*sin(2*fi)*sin(2*lamda))))}
R2 Vref q2bc {4.3k*(1+s*1e6*(pi11_p*(0.5+0.5*cos(2*fi)*cos(2*lamda))+pi12_p*(0.5-
0.5*cos(2*fi)*cos(2*lamda))+pi44_p*(0.5*sin(2*fi)*sin(2*lamda))))}
R3 r13 q1bc {2.3k*(1+s*1e6*(pi11_p*(0.5+0.5*cos(2*fi)*cos(2*lamda))+pi12_p*(0.5-
0.5*cos(2*fi)*cos(2*lamda))+pi44_p*(0.5*sin(2*fi)*sin(2*lamda))))}
XU1 q2bc r13 op_po 0 Vref level.2 Avol=1Meg GBW=10Meg Slew=10Meg ilimit=25m rail=0 Vos=0
phimargin=45 en=0 enk=0 in=0 ink=0 Rin=500Meg
V1 op_po 0 3
.model NPN NPN(IS={1e-16*(1-pi_12nb*s*1E6-pi_11nb*szz*1E6)} BF={npnb*(1-x*((pi_12nb-pi_12pe)*s*1E6-
(pi_11nb-pi_11pe)*szz*1E6) -(1-x)*(pi_12nb*s*1e6-pi_11nb*szz*1e6))})
.model PNP PNP

.lib C:\PROGRA~2\LTC\LTSPIC~1\lib\cmp\standard.bjt
.step param s 0  100 30
.op
.lib UniversalOpamps2.sub
.backanno
.probe
.end
```

Appendix F - Publications of the Author

- P. Gnanachchelvi, R. C. Jaeger, B. M. Wilamowski, G. Niu, S. Hussain, J. C. Suhling, and M. C. Hamilton, "Performance Enhancement in Bipolar Junction Transistors Using Uniaxial Stress on (100) Silicon," IEEE Trans. Electron Devices, accepted for publication on April 22nd 2016.

- P. Gnanachchelvi, B. M. Wilamowski, R C. Jaeger, S. Hussain, J. C. Suhling and M. C. Hamilton, "A 1-D numerical model for rapid stress analysis in bipolar junction transistors," International Journal of Numerical Modelling: Electronic Networks, Devices and Field, accepted for publication on April 26th 2016.

- R. Nana, P. Gnanachchelvi, M. A. Awaah, M. H. Gowda, A. M. Kamto, Y. Wang, M. Park, and K. Das, "Effect of deep-level states on current-voltage characteristics and electroluminescence of blue and UV light emitting diodes", Phys. Status Solidi A 207, No. 6, 1489–1496 (2010).

- R. Jaeger, S. Hussain, G. Niu, P. Gnanachchelvi, J. Suhling, B. Wilamowski, and M. Hamilton, "Characterization of residual stress levels in complementary bipolar junction transistors on (100) silicon," IEEE BCTM 2015, pp. 60-63.

- S. Hussain, R. C. Jaeger, J. C. Suhling, B. M. Wilamowski, M. C. Hamilton, and P. Gnanachchelvi, "Understanding the impact of temperature variations on measurement of stress dependent parameters of bipolar junction transistors," ITherm 2014, pp. 1244-1250.

- R. Jaeger, S. Hussain, J. Suhling, P. Gnanachchelvi, B. Wilamowski, and M. Hamilton, "Impact of mechanical stress on bipolar transistor current gain and Early voltage," in Sensors, 2013 IEEE, 2013, pp. 1-4.

- S. Hussain, P. Gnanachchelvi, J. C. Suhling, R. C. Jaeger, M. C. Hamilton, B. M. Wilamowski, "The Influence of Uniaxial Normal Stress on the Performance of Vertical Bipolar Transistors", InterPACK 2013.

- P. Gananchchelvi, J. Yu, Michael S. Pukish "Current trends in in-vehicle electrical engineering applications," IECON 2012, pp. 6268-6273, 25-28 Oct. 2012.

- M. S. Pukish, P. Gnanachchelvi, X. Wu, "Recent Developments in Wireless Hardware Design, Modeling, and Analysis for Industrial Applications", IECON 2012, October 25-28, 2012.

- J. Yu, P. Gnanachchelvi, B. M. Wilamowski, “Performance Analysis of IES Journals using Internet and Text Processing Robots” IEEE 37-th Annual Industrial Electronics Conference IECON 2011, Nov 7-10, 2011, pp. 4612-4618.