Phospho-silicate glass as gate dielectric in 4H-SiC metal-oxide-semiconductor devices

by

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Abstract

Silicon carbide (SiC) based MOS devices are well suited to meet the need for energy efficient power electronics. For 4H-SiC MOSFET technology, one of the crucial challenges is to improve the quality of SiO_2/SiC interface, which is plagued by high interface trap density (D_{it}) and low inversion layer mobility. Till date, nitric oxide (NO) post oxidation annealing of the gate oxide has become the standard process to produce commercial quality devices with acceptable channel mobility($\sim$35$cm^2V^{-1}s^{-1}$, only 4% of the theoretical limit). However, due to the competing nitridation and oxidation reactions during NO annealing, there is a limit to the nitrogen coverage at the SiO_2/SiC interface, which can reduce the trap density near the 4H-SiC conduction band edge. On the other hand, according to the recently proposed C-ψ_s method which avoids the probing frequency limitation in the conventional characterization methods, nitridation treatment generates certain amount of fast interface states. Because of the increase of the fast interface state density, NO annealing at a temperature higher than 1250 °C is not effective.

Meanwhile, a dielectric/SiC interface that results in higher channel mobility, steeper sub-threshold slope and stable positive threshold voltage is still extremely desired for next-generation devices. Conversion of SiO_2 into phospho-silicate glass (PSG) reduces the interface trap density more efficiently and improves the channel mobility by a factor of 3 compared to nitridation. In addition to trap passivation, both nitrogen and phosphorus atoms at the interface can dope the channel region of the MOSFET. This counter-doping effect in PSG is more prominent than nitridation, which contributes more to the mobility improvement. However, as PSG is an intrinsical polar material, undesirable polarization induces threshold-voltage instability, making this gate dielectric impractical.

In this research, we have investigated the phospho-silicate glass (PSG) as gate dielectric in SiC metal-oxie-semiconductor (MOS) devices. With several characterization techniques, we demonstrate that PSG formed by phosphoryl chloride ($POCl_3$) annealing has more efficient role in passivating the interface traps (D_{it}) than NO annealing, both in 4H and 6H polytypes. As nitridation method, there exist "fast states" at the PSG/SiC interface, which are undetectable by conventional characterization methods. C-ψ_s method was used to extract the accurate D_{it} profiles, including those "fast states". Through the D_{it} profiles extracted by C-ψ_s method, a universal relationship between the total interface traps N_{it} (the D_{it} integration) and the peak channel mobility for both 4H and 6H polytypes has been identified, through which the mobility improvement of PSG dielectric on 6H-SiC devices is suggested.

We have explored the correlation between the phosphorus uptake in PSG dielectric and its effect on the electrical properties of 4H-SiC MOS devices. Based on the P_2O_5-SiO_2 phase diagram, different phosphorus uptake is achieved by varying the $POCl_3$ annealing temperature in the range 900 °C - 1100 °C. The interface trap density is closely related to the interfacial phosphorus coverage, and more interfacial phosphorus incorporation leads to more reduction of D_{it}. In general, the mobility in 4H-SiC MOSFETs can be improved by a larger phosphorus uptake. However, due to the difference of counter-doping effect at various $POCl_3$ annealing temperatures, the P passivation and surface counter-doping reach an optimum at 1000 °C $POCl_3$ annealing, resulting in the highest mobility $\sim$105$cm^2V^{-1}s^{-1}$. At high oxide field E_{ox}, we observe two mobility behaviors in temperature dependency for different PSG dielectrics. In 1000 °C PSG dielectric, possibly due to a minimal interface roughness, the surface phonon scattering is limiting the high field mobility; in other PSG dielectrics, the mobility limiting factor is surface roughness scattering.

In addition, two competing mechanisms in PSG dielectric instability are identified, polarization and electron trapping. Through a modulation of thin PSG structure and phosphorus uptake, we have suggested that it is possible to achieve stable PSG-gated 4H-SiC devices.

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Chapter 1

Introduction

1.1 Power electronics and wide band gap semiconductors

Modern society is very much defined by its access to electricity, and the world today is extremely hungry for energy. Power electronics is the application of solid-state electronics to the control and conversion of electric power. It is estimated that at least 50% of the electricity used worldwide is controlled by power devices[1]. With the widespread use of power electronics in automobiles, industry, electricity transmission, transportation and communication sectors, power devices have a major impact in economy because they determine the cost and efficiency of systems.

In power electronics, devices based upon silicon technology are rapidly approaching their theoretical limits of performance. Consequently, it is necessary to develop devices from other materials in order to reduce power losses in high-frequency systems and achieve high efficiencies. With different theoretical considerations, several analyses of the impact of material parameters on the performance of semiconductor devices have been performed [2].

To define the power-frequency product for a low-voltage transistor, E. Johnson derived a figure of merit (JFOM) in 1965 [3],

$$JFOM = \frac{E_c \cdot v_s}{2\pi} \tag{1.1}$$

Here, E_c is the critical electric field for breakdown in the semiconductor and v_s is the saturated drift velocity.

To provide a thermal limitation to the switching behavior of transistors used in integrated circuits, R. Keyes derived another figure of merit (KFOM) in 1972 [4],

$$KFOM = \lambda \left[\frac{c \cdot v_s}{4\pi\epsilon_s} \right]^{1/2} \tag{1.2}$$

Here, λ is the thermal conductivity of the material, c is the velocity of light, and ϵ_s is the dielectric constant of the semiconductor.

In 1982, B. Baliga [5] derived the well-known figure of merit (BFOM) to define material parameters to minimize the conduction losses in power field-effect transistors (FETs).

$$BFOM = \epsilon_s \cdot \mu \cdot E_G^3 \tag{1.3}$$

Here, μ is the mobility and E_G is the band gap of the semiconductor.

The BFOM is based upon the assumption that the power losses are solely due to the power dissipation in the on-state by current flow through the on-resistance of the power FET. Thus, the BFOM applies to systems operating at lower frequencies where the conduction losses are dominant. The derivation of BFOM is shown as follows.

For all power devices, a useful figure of merit is the product of the blocking voltage and the on-state current, since an "ideal" power switch would maximize both. Thus,

$$FOM \equiv I_{ON}V_B = AJ_{ON}V_B \tag{1.4}$$

where A is the area of the device, J_{ON} is the on-state current density, and V_B is the blocking voltage. The maximum allowable power dissipation P_{MAX} is determined by the thermal capability of the package, the heat sink temperature, and the maximum allowable junction temperature of the device. In a unipolar power device, we can attribute the majority of

power dissipation to the on-state power P_{ON}, thus $J_{ON} = \sqrt{P_{MAX}/R_{ON,SP}}$, and the Eq(1.4) can be written

$$FOM = A\sqrt{P_{MAX}(V_B^2/R_{ON,SP})} \tag{1.5}$$

In Eq(1.5), the factor, $V_B^2/R_{ON,SP}$, represents the *unipolar device FOM*, and it is the goal of the designer to maximize this ratio.

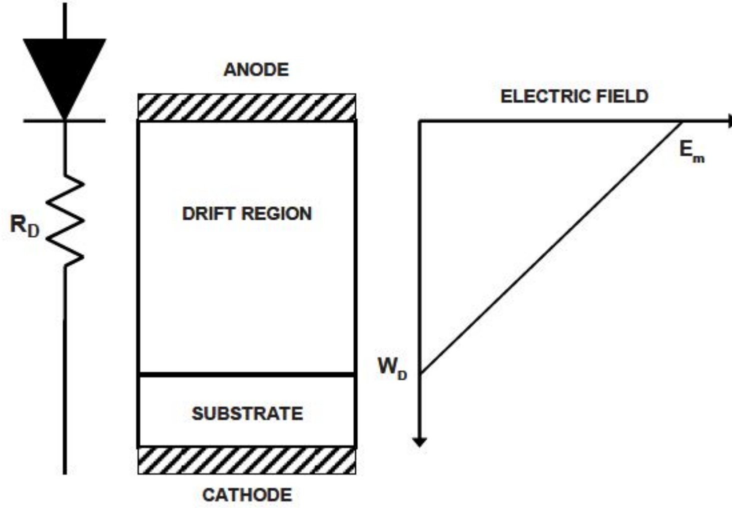


Figure 1.1: The ideal drift region and its electric field distribution

Consider a p+/n- one-sided junction under reverse bias, as shown in the Figure. 1.1, the n- drift region thickness W_D can be written as

$$W_D = 2V_B/E_C \tag{1.6}$$

Meanwhile, the depletion width of one-sided step junction at breakdown can be written

$$W_D = \sqrt{2\epsilon_s V_B/(qN_D)} \tag{1.7}$$

where N_D is the doping concentration.

Thus, to eliminate W_D and solve the breakdown voltage V_B from Eq(1.6) and Eq(1.7), we get

$$V_B = (\epsilon_s E_C^2)/(2qN_D) \tag{1.8}$$

The on-resistance arises primarily from the resistance of the lightly-doped n- drift region,

$$R_{ON,SP} = W_D/(q\mu N_D)$$

Substituting W_D and N_D,

$$R_{ON,SP} = \frac{2V_B/E_C}{\mu\epsilon_s E_C^2/2V_B} = \frac{4V_B^2}{\mu\epsilon_s E_C^3} \tag{1.9}$$

Equation (1.9) indicates that the specific on-resistance of a non-punch-through unipolar device is inversely proportional to the cube of the critical field. After rearranging Eq(1.9), we yield the BFOM here

$$V_B^2/R_{ON,SP} = \frac{2V_B/E_C}{\mu\epsilon_s E_C^2/2V_B} = \frac{4V_B^2}{\mu\epsilon_s E_C^3} \tag{1.10}$$

Equation (1.10) represents the maximum possible FOM for an optimally designed non-punch-through unipolar device. Real devices can only approach this theoretical limit. Note that there is slight difference in the form of BFOM, instead of E_G, it is E_C in equation (1.10). In any case, this theoretical BFOM depends on fundamental material constants, and not on specific device parameters. Figure 1.2 [6] shows the comparison of $R_{ON,SP}$ for Si, SiC and GaN based FET devices.

Most importantly, this figure of merit demonstrates that instead of silicon (Si, $E_G = 1.12eV$), the wide-band gap semiconductors, gallium nitride (GaN, $E_G = 3.4eV$), silicon carbide (SiC, 4H-type, $E_G = 3.26eV$), and semiconducting diamond ($E_G = 5.5eV$) offer significant potential for improving power FET performance.

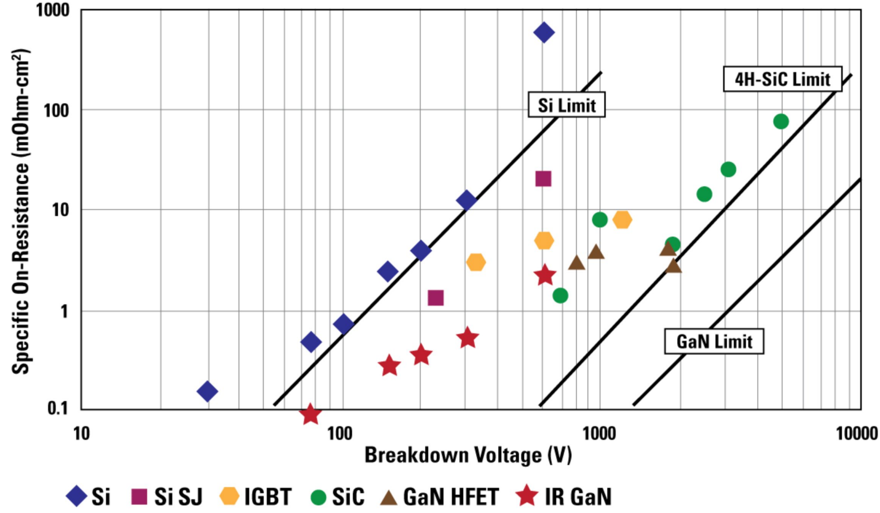


Figure 1.2: comparison of the theoretical $R_{ON,SP}$ limit for Si, SiC and GaN.[6]

1.2 Physical properties of SiC

SiC is a compound semiconductor, with 50% of silicon (Si) and 50% of carbon (C). Both Si and C atoms are tetravalent elements and have four valence electrons in their outermost shells. Si and C atoms are tetrahedrally bonded with covalent bonds by sharing electron pairs in sp^3- hybrid orbitals to form a SiC crystal, and the Si-C bond energy is 4.6 eV [7], which makes this material very stable.

SiC crystallizes in a wide variety of structures (more than 200 polytypes), divided into three basic crystallographic categories: cubic (C), hexagonal (H), and rhombohedral (R). In Ramsdell's notation, polytypes are represented by the number of Si-C bilayers in the unit cell and the crystal system. The stacking sequences for 2H-, 4H-, 6H-, 15R- and 3C-SiC polytypes are shown in Fig. 1.3[8].

Each polytype of SiC exhibits unique electrical, optical, thermal, and mechanical properties. For instance, compared to 3C-SiC ($E_G = 2.36eV$), 4H-SiC has a larger band gap ($E_G = 3.26eV$). In the past three decades, extensive research has been devoted to the development of SiC-based electronics technology. 3C-SiC, due to its lower band gap than 4H-

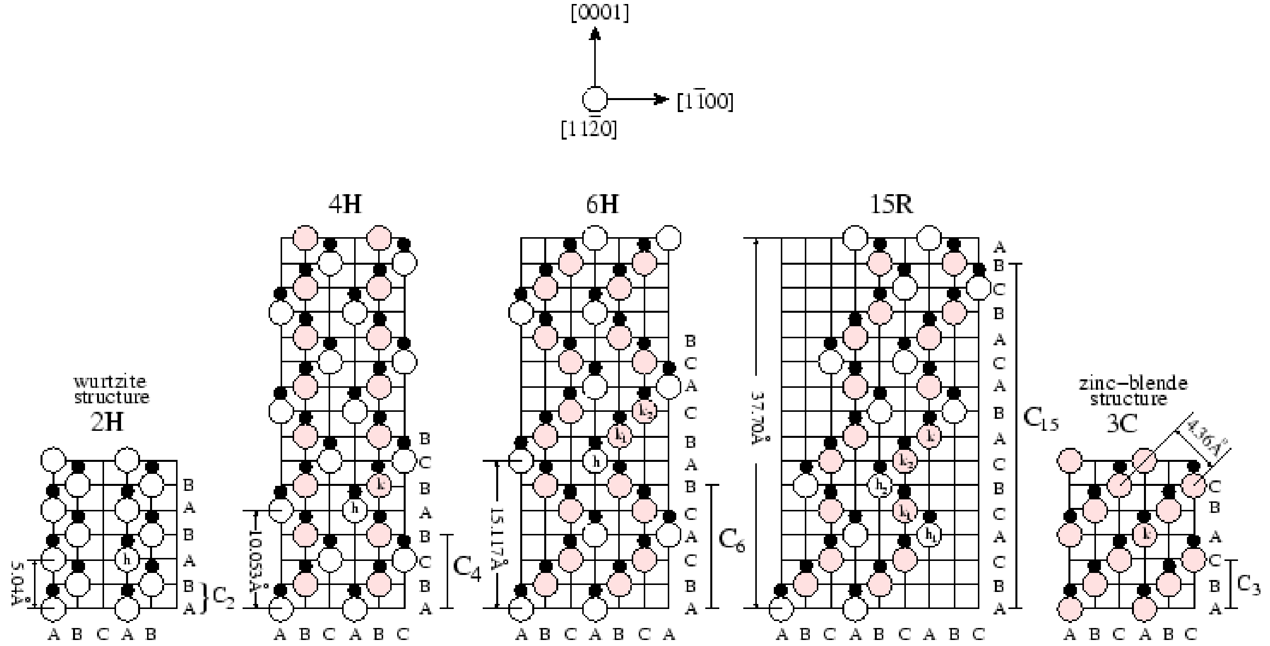


Figure 1.3: The stacking sequences for 2H-, 4H-, 6H-, 15R- and 3C-SiC polytypes.[8]

and 6H-SiC, instead of power applications, has been researched for non electronic applications, such as micro-electro-mechanical systems (MEMS) and biosensors [9]. 4H-SiC and 6H-SiC both have advances in physical properties, such as high electric breakdown field, high thermal conductivity and high saturation velocity. Provided that all other device processing, performance, and cost-related issues are roughly equal between the 4H- and 6H-polytypes, 4H-SiC's substantially higher carrier mobility and shallower dopant ionization energies compared to 6H-SiC make it the polytype of choice for most SiC electronic devices [10]. In addition, the inherent mobility anisotropy that degrades conduction parallel to the crystallographic c-axis in 6H-SiC (the electron mobility parallel to *c*-axis is 100 $cm^2V^{-1}s^{-1}$, perpendicular to *c*-axis 450 $cm^2V^{-1}s^{-1}$) particularly favors 4H-SiC for vertical power device configurations [11]. Besides, 4H-SiC crystal growth and epitaxy technologies have matured rapidly, and large diameter wafers (6 in.) are currently commercially available. All these make the mass production of 4H-SiC power devices possible with high energy and cost efficiency.

Table 1.1: The band gap (E_g), dielectric constant (ϵ_s), electron mobility (μ_n) [12], critical electric field (E_C) and relative-to-Si BFOM for various materials. The electron mobility and BFOM values for 4H-SiC, 6H-SiC and 3C-SiC are in [0001] direction.

Material	Si	GaAs	4H-SiC	6H-SiC	3C-SiC	GaN	β-Ga_2O_3	Diamond
E_g(eV)	1.12	1.42	3.26	3.02	2.36	3.4	4.7–4.9	5.5
ϵ_s	11.8	13.1	9.76	9.66	9.72	9.0	10	5.5
μ_n(cm^2/Vs)	1430	8500	900	100	1000	900	300	1900
E_C(MV/cm)	0.3	0.4	2.8	3.0	1.4	3.3	8	10
Relative BFOM	1	16	626	63	61	852	3371	22937

Taking account of the Baliga figure of merit (BFOM), which is discussed above, Table.1.1 compares the BFOMs of Si, 4H-SiC, 6H-SiC and other wide band gap semiconductors to illustrate the viability of 4H-SiC power electronics technology.

Compared to other wide band gap semiconductors, one of the great advantages in silicon carbide (SiC) is its nature that thermal oxide grows on SiC surface similarly to silicon. From the technological standpoint, this feature enables the fabrication of SiC-based power metal-oxide-semiconductor (MOS) transistors. Moreover, from the commercial manufacturing standpoint, many silicon foundries can perform the SiC device processing task easily.

In the rest of this thesis, most of our discussion will be restricted to 4H-SiC (or 6H-SiC). Therefore, here it is necessary to point out multiple different faces in the hexagonal lattice structure. As shown in Fig.1.4, (0001) is referred as Si-face, $(000\bar{1})$ C-face, $(11\bar{2}0)$ a-face, and $(1\bar{1}00)$ m-face.

1.3 MOS interface challenges

A SiC power MOSFET is regarded as one of the most promising power switching devices for 600V, 1200V, 1700V and 3300V applications. For higher voltage application with low switching frequencies, the IGBT would be good choice. The ability to form a layer of native SiO_2 on SiC by thermal oxidation in a way similar to Si provides a good basis for the fabrication of SiC MOS-based electronic devices. Although M. Nawaz [13] evaluated other high-κ materials (such as Si_3N_4, Al_2O_3, AlN, and HfO_2) for 4H-SiC MOSFETs with better

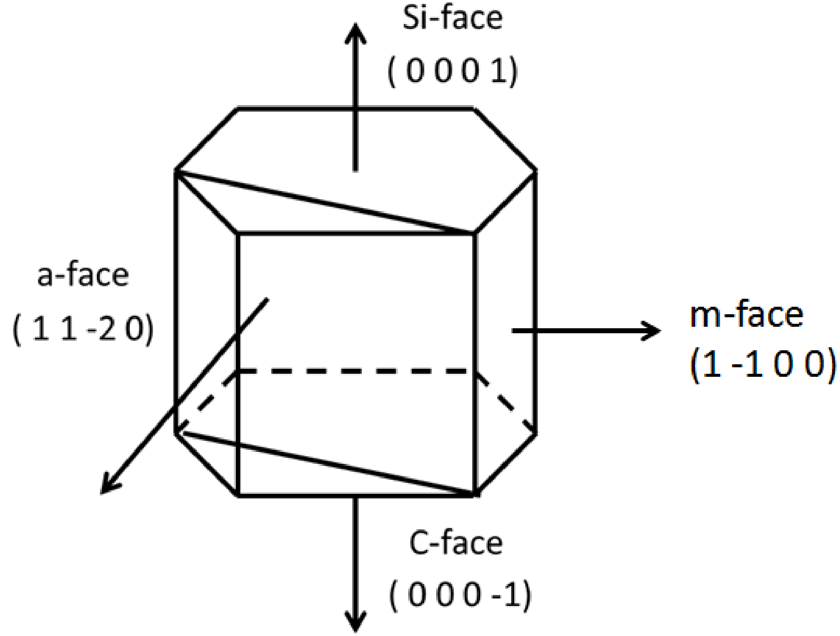


Figure 1.4: The hexagonal crystal lattice structure, and Si-, C-, a- and m- faces

potential to reduce the amount of electric field in the gate dielectric with equal gate dielectric thickness and reduce the threshold voltage shift, thermal oxides are still the most commonly utilized gate dielectrics in SiC MOS technology.

Despite the similarity of the oxides grown on Si and SiC, the oxidation process of SiC is different due to the presence of carbon. The overall reaction is expressed as

$$\mathrm{SiC} + \frac{3}{2}\mathrm{O_2} \longrightarrow \mathrm{SiO_2} + \mathrm{CO} \tag{1.11}$$

Thermal oxidation kinetics of SiC has been discussed by the modified *Deal-Grove* model[14], which was developed for Si technology. The modified *Deal-Grove* model takes the generation and transport of CO during oxidation into consideration, in addition to the transport and consumption of O_2 at the interface of SiO_2/SiC.

The oxidation of a new layer of SiC at an abrupt SiC/oxide interface broadly consists of three steps, as shown in Fig.1.5: (a) an O_2 molecule approaches the interface through the growing oxide, (b) at the interface, O-O bonds readily break apart to form the stronger

Si-O-C bonds, (c) carbon is removed from SiC as a CO molecule leaving behind an oxygen passivated carbon vacancy (V_CO_2) with only Si-O-Si bonds[15;16].

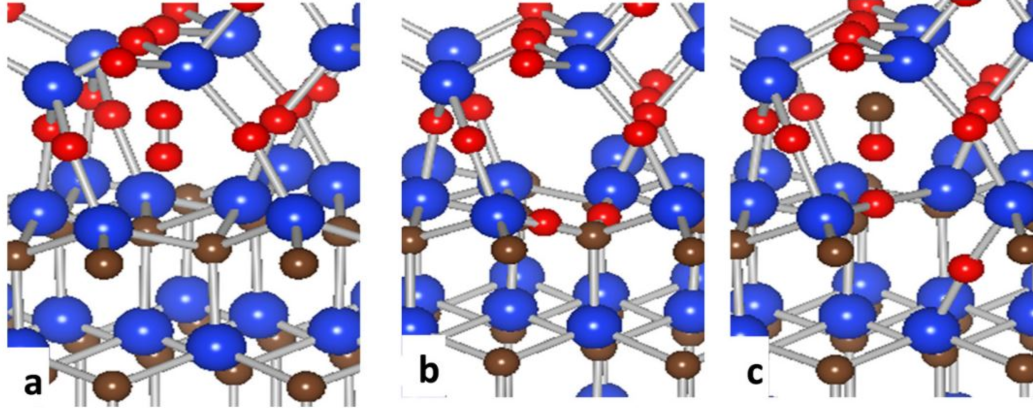


Figure 1.5: The schematic of SiC oxidation process in three steps. Blue balls are silicon atoms, brown balls are carbon atoms, and red balls are oxygen.[15]

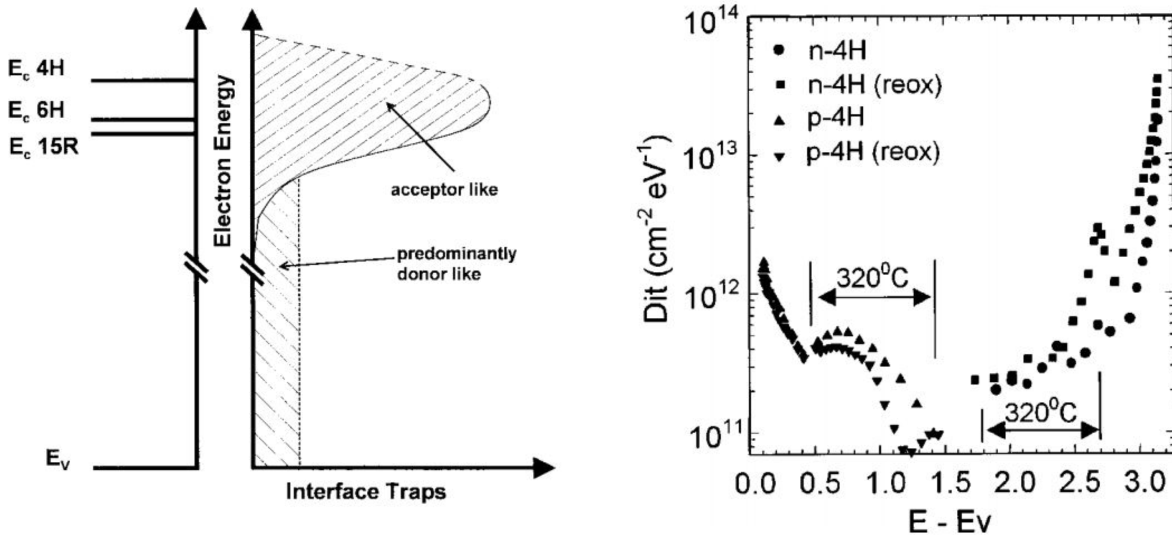
During thermal oxidation, most of the carbon atoms in SiC are removed and diffuse out as CO molecules. Researches suggest that a small portion of carbon atoms diffuses into the SiC bulk region, leading to the reduction of carbon-vacancy-related deep-level defects [17] while forming split interstitial defects [18]. However, the thermal oxide is not free of carbon, and it is believed that the incomplete CO ejection causes several types of defects near the oxide/SiC interface, such as carbon cluster, and carbon interstitials. In addition to carbon-related defects, at the interface, there exists oxygen-vacancy, Si dangling bonds and Si interstitials.

Those defects, energetically, behave as interface traps in the band gap (Ideally, no electron states are allowed within the band gap, therefore it is also referred as forbidden gap). In modern CMOS technology, the density of interface traps (D_{it}) does not exceed 10^{10} cm^{-2}/eV at the Si/SiO_2 interface[19]. In contrast, at the SiC/SiO_2 interface, this value is about $\sim 10^{11}$ cm^{-2}/eV in the middle of the band gap and 10^{13} cm^{-2}/eV or even more at the band edges of 4H-SiC.

Several reports [20–22] have investigated the distribution of interface trap density, and pointed out that above the mid gap, D_{it} profile follows the empirical relation:

$$D_{it}(E) = D_{it}^{mid} + D_{it}^{edge}\exp\Big(\frac{E - E_C}{\sigma}\Big) \tag{1.12}$$

where D_{it}^{mid} is a constant representative of D_{it} in the midgap region, D_{it}^{edge} is the band-edge interface trap density, and σ is a parameter in eV that dictates the sharpness of the profile. R. Schörner postulated the distribution of interface traps at the SiO_2/SiC interface for 4H-SiC, 6H-SiC, and 15R-SiC [23], as shown in Fig.1.6a. G.Y. Chung *et al.* [24] charted the interface state densities profile across the whole band gap for 4H-SiC/SiO_2 interface, by characterizing both *n*-type and *p*-type substrates, as shown in Fig.1.6b.



(a) Scheme of the postulated distribution of interface defects at the SiO_2/SiC interface for 4H-SiC, 6H-SiC, and 15R-SiC.[23]

(b) Interface state densities for p- and n- type as-oxidized 4H-SiC/SiO_2 interface.[24]

Figure 1.6: Postulated and measured distribution of interface trap density in SiC

The quality of the SiC/SiO_2 interface is highly jeopardized by the existence of high interface trap density. It is a critical factor for the device performance of MOSFETs with a surface channel. The existence of defects form during the thermal oxidation dramatically affect the current transport in the device. For example, lateral 4H-SiC MOSFETs with

thermally grown oxide as gate dielectric have field-effect mobility less than 10 $cm^2V^{-1}s^{-1}$, two orders lower than its theoretical value. This is usually explained by the high density of interface traps that lead to the reduction of carrier concentration and strong Coulomb scattering at the interface, and thus significantly reduce the channel mobility.

To fully realize the potential of SiC MOSFET technology and give full scope to all its attractive advantages over other materials, three critical challenges must be met: increasing the channel mobility, improving the device stability, and establishing a better defined threshold voltage. All these challenges inevitably point to the requirement of a better SiC/SiO_2 interface with lower interface trap density.

1.4 Progress

So far, extensive research work has been done in improving the quality of SiC/SiO_2 interface on (0001) Si-face. At this point, nitridation of the thermally grown oxide with nitric oxide (NO) gas or nitrous oxide (N_2O) gas has become the standard process to produce commercial quality devices with acceptable channel mobility, but still lacks optimum performance. Before we discuss about the nitrogen or other Group V elements incorporation at the SiC/SiO_2 interface, here we first introduce the recent progress in the interface issue by other methods.

1.4.1 High temperature oxidation

As discussed above, the presence of C atoms in SiC causes more deficiencies than Si after the thermal oxidation. It has long been a goal to directly grow a defect-free interface without post-oxidation treatments. Typically, to grow thermal oxides on SiC, a standard quartz oxidation furnace which is limited to a maximum operating temperature of 1100 °C - 1200 °C is used. In 2006, Kurimoto *et al.*[25] reported that the interface trap density has a dependence on the thermal oxidation temperature. Based on this dependence, dry oxidation at temperatures above 1200 °C requires more attention and research.

Recently, Naik and Chow[26] obtained a noticeable lowering in D_{it} by oxidizing at 1400 °C. Kikuchi and Kita [27;28], by employing a rapid thermal annealing (RTA) furnace, which can operate at 1300 °C, obtained good SiC/SiO_2 interface with low interface trap density $<10^{11}$ cm^{-2}/eV for the energy range of 0.1-0.4 eV below the conduction band of SiC. Taking the thermodynamical and kinetic into consideration, raising the oxidation temperature enhances the emission of CO [29] during the oxidation process. Besides, for a shorter emission path, a thinner oxide is conducive to the carbon emission as well. The capacitors fabricated with high temperature thin oxide have nearly ideal capacitance-voltage characteristics, as shown in Fig.1.7. The CV curves taken with different applied frequencies are mostly overlapped with the ideal CV curve, indicating very small amount of interface traps.

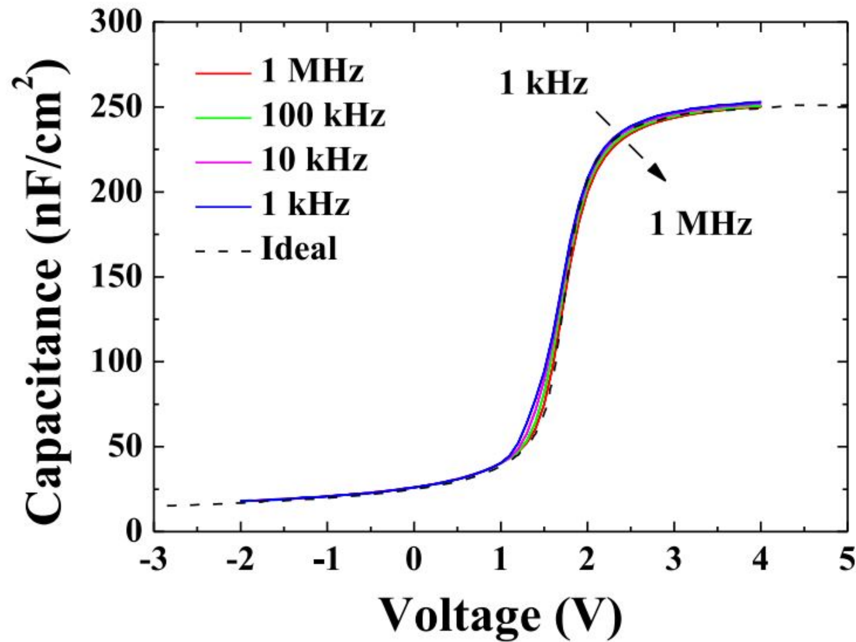


Figure 1.7: C-V characteristics of the MOS capacitor fabricated by 1300 °C oxidation.[29]

In another study, Thomas *et al.* [30] obtained a channel mobility of 40 $cm^2V^{-1}s^{-1}$ using an oxidation temperature of 1500 °C, but the device was normally on. The improvement in mobility is speculated due to the reduction of carbon precipitation at high temperature.

High temperature oxidation provides some new prospect in solving the interface challenge. However, more investigations are needed to establish the underlying mechanisms of mobility improvement in this method.

1.4.2 Metals

In 2007, E. Sveinbjörnsson *et al.*[31] reported exceptionally high peak field-effect mobility of about 150 $cm^2V^{-1}s^{-1}$ with the addition of sodium (Na) in the gate oxide. The mechanism of the mobility enhancement can be explained by that the presence of sodium during oxidation increases the oxidation rate and suppresses the formation of near interface traps. While the mobility is impressive, the devices suffer from the mobile ion effect, i.e., the sodium ions move within the gate oxide at typical operating temperatures and gate biases. The poor device stability dramatically negates the benefits of mobility enhancement by sodium incorporation. Fig.1.8 [32] shows the change of device's mobility before and after bias-temperature stressing (BTS). The shift of threshold voltage and the shape change of the mobility curve indicate very poor stability of the device.

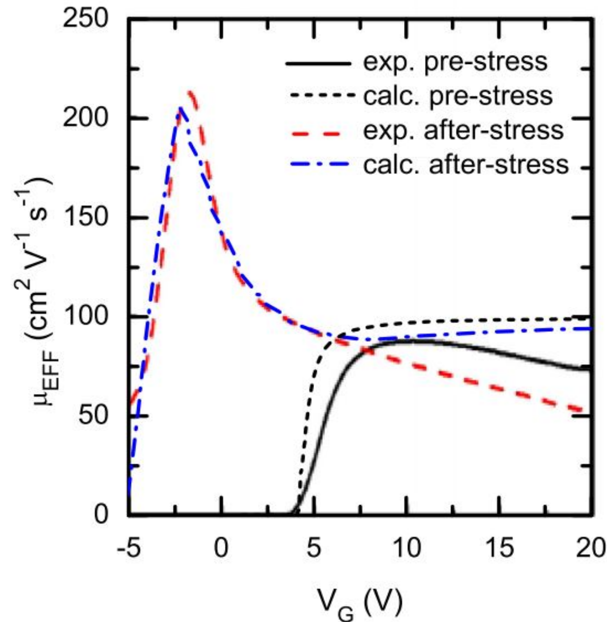


Figure 1.8: The shift of mobility curves of the device with sodium incorporation pre- and after stress. After stressing, the device shows very poor stability.[32]

Recently, D. Lichtenwalner *et al.*[33] investigated atoms in group I (alkali elements Rb and Cs) and group II (alkaline earth elements Ca, Sr, and Ba). In an ultra-high vacuum molecular beam epitaxy (MBE) system, they evaporate a very thin interface layer (∼0.6 - 0.8 nm) of these metal materials at first, and then stack with ∼ 30 nm SiO_2 dielectric cap layer, followed by a post-deposition anneal. The alkali elements Rb and Cs raise the field-effect mobility > 25 $cm^2V^{-1}s^{-1}$, and the alkaline earth elements Sr and Ba yield even higher peak mobility values of 40 and 85 $cm^2V^{-1}s^{-1}$, respectively (shown in Fig.1.9). With the *n*-type capacitors, they find that barium (Ba) interface layer substantially reduces D_{it} near E_C. Furthermore, Ba-modified MOSFETs show stable threshold voltage under 2 MV/cm gate bias stress at 175°C, which demonstrates that Ba, as a larger ionic radii element, is less mobile and more strongly bonded. It is also likely that Ba atoms in the interface layer act in a donor-like way.

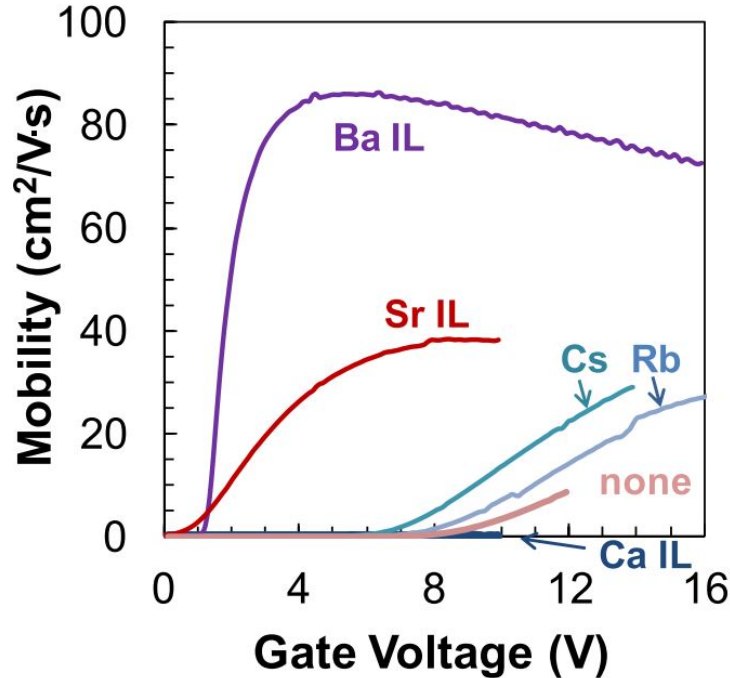


Figure 1.9: Field-effect mobility from I_D-V_G characteristics for MOSFETs processed with Rb, Cs, Ca, Sr, or Ba interface layers, compared to an unpassivated thermal oxide (labeled "none").[33]

In another study, Yang *et al.*[34;35] demonstrated a novel interface engineering technique to achieve high mobility and maintain a sufficiently positive threshold voltage. In this technique, an ultra thin (< 2.5nm) lanthanum oxide (La_2O_3) is deposited on the surface of SiC, then a thick stack of SiO_2 is deposited by atomic layer deposition (ALD). This method is free of thermal oxidation and aforementioned carbon related defects from oxidation, however, post deposition treatment is required to improve the interface properties. Post deposition annealing (PDA) the La_2O_3/SiO_2 stack at high temperatures (>800 °C), La_2O_3 reacts with SiO_2 and forms stable lanthanum silicate $LaSiO_x$ due to the scavenging effect of La_2O_3. A thin layer of lanthanum silicate $LaSiO_x$, which is a high-κ dielectric, is sandwiched in between SiC and high quality SiO_2 deposited by atomic layer deposition (ALD). The thin $LaSiO_x$ layer is introduced to improve the interface properties, and the thick ALD SiO_2 layer suppresses the gate leakage. The authors also researched the effect of the variation in the thickness of the initial deposited lanthanum oxide (La_2O_3). They found that, MOSFET with initial 1 nm La_2O_3 thin layer deposition and 900 °C PDA in nitrous oxide (N_2O) gas can yield a peak mobility of 133 $cm^2V^{-1}s^{-1}$ at room temperature and relatively stable threshold voltage, as seen in Fig.1.10.

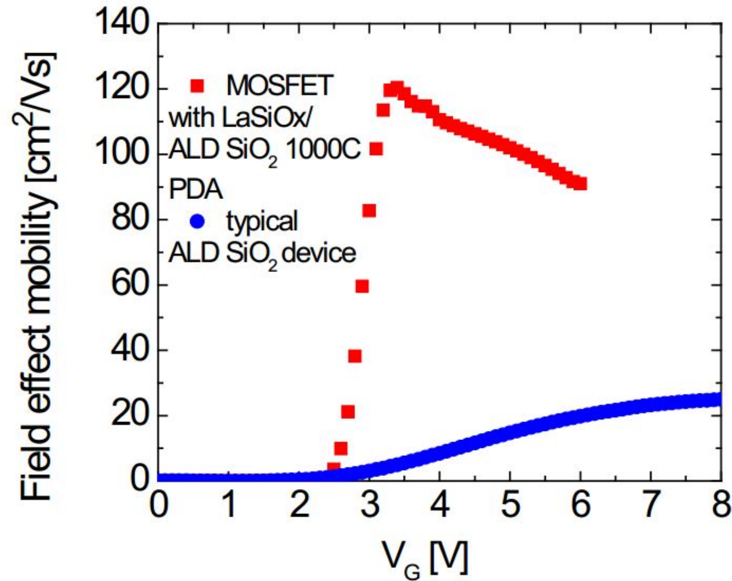


Figure 1.10: Field effect mobility of MOSFETs with lanthanum incorporation. [34]

1.4.3 Group III element - Boron

Okamoto *et al.*[36] introduced group III element boron (B) atoms into SiO_2/4H-SiC interface by thermal annealing with a boron nitride (BN) planar diffusion source. This treatment resulted in a significantly reduced D_{it} and a peak field-effect mobility of 102 $cm^2V^{-1}s^{-1}$, as shown in Fig.1.11. The B concentration was found to be 3×10^{20} cm^{-3} in the oxide and 7×10^{20} cm^{-3} at the interface, while the N concentration was two orders of magnitude lower than B. Therefore, this achievement is mainly due to B effect. The enhancement in mobility is attributed to the reduction of interface states near the conduction band-edge of 4H-SiC, while the authors suggest that instead of the trap passivation or the termination of the dangling bonds, the structural change in SiO_2 near the interface due to the stress relaxation could be responsible for the reduced D_{it}, because B_2O_3 is a network former that reduces the network connectivity of SiO_2 [37] and the interface stress.

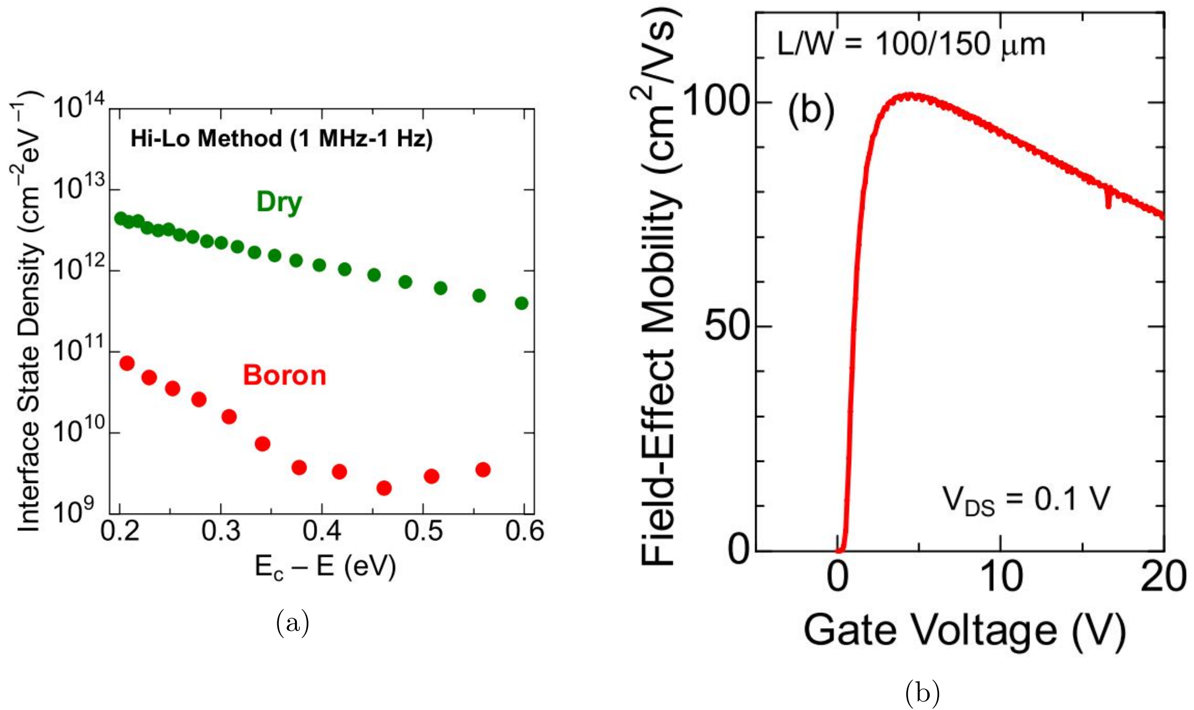


Figure 1.11: (a) Distribution of interface state density near the conduction band edge from Hi-Lo method for dry and B-doped oxides. (b) Field-effect mobility of 4H-SiC MOSFETs fabricated with the B diffusion process.[36]

1.4.4 Group IV element - Germanium

The group IV element germanium (Ge) is an isoelectronic impurity in SiC, since Ge, Si and C are in the same group. The incorporation of Ge does not contribute to the doping of SiC. Therefore, it is not expected to contribute to the conductivity.

However, G. Katulka *et al.*[38] reported that Ge incorporation in SiC by ion implantation and subsequent annealing improves the conductivity of ohmic contacts. T. Sledziewski *et al.* [39] introduced Ge into SiC during epitaxial growth with chemical vapor deposition (CVD) method to avoid the ion implantation damage to the crystal lattice, and found that the Ge-doped SiC sample overall has higher Hall-effect mobility than the sample without Ge incorporation while keeping the free carrier concentration the same. At $T \approx 55K$, the enhancement factor in Hall mobility is ~ 2, as seen in Fig.1.12.

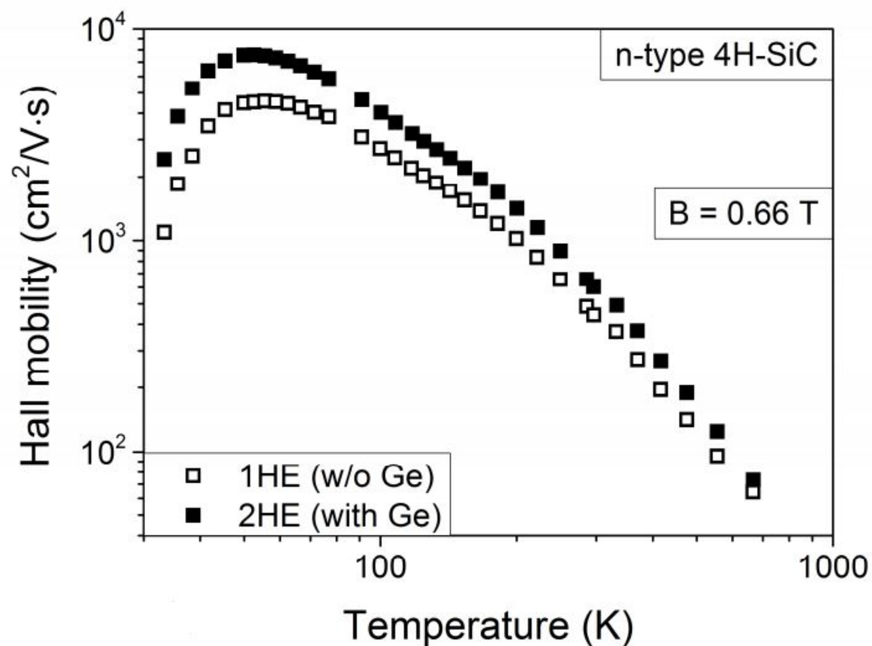


Figure 1.12: Hall mobility as a function of temperature in the samples with and without Ge incorporation. Two samples have the same free electron concentration, while the mobility in the Ge-doped sample is higher than the one without Ge.[39]

The mechanisms of the Hall mobility enhancement by Ge-doping have not been identified yet, most likely due to the lattice strain generated by the large Ge atoms. Up to now, no field-effect mobility enhancement by Ge-doping in SiC has been reported. In MOS structure, the increase of the local Hall mobility by germanium is likely to improve the channel transport mobility.

1.4.5 Alternative crystal faces

Currently most of the effort is devoted to (0001) orientated wafers since the epitaxial growth technology on Si-face has matured rapidly. Meanwhile, research on other faces (C-face, a-face, m-face, etc.) [40;41;41–44] gains more and more attention in that they usually exhibit higher transport mobility and a higher threshold voltage, compared to Si-face. As a very desirable design for next-generation SiC power MOSFETs, trench MOSFET (also referred as UMOSFET) utilizes various non-polar faces. More work is needed with the combined effort from material development, epitaxial growth, oxide reliability, and stability, to make the devices derived from alternative faces competitive with the Si-face devices. For the progress on those alternative crystal faces, please refer to G. Liu *et al.'s*[15] review "Silicon Carbide: A unique platform for metal-oxide-semiconductor physics", section IV E.

1.5 Group V elements

Group V elements, namely nitrogen (N), phosphorus (P), arsenic (As) and antimony (Sb), have been studied intensively in the past decade, especially nitrogen and phosphorus[24;45–48]. Theoretically, N and P can terminate the dangling bonds thus reduce the trap density at the interface effectively. Here, it is worth mentioning that, nitridation of the gate oxide by nitric oxide (NO) gas, patented by Auburn University and Vanderbilt University [Publication number: US6939756 B1], has enabled the fabrication of high-quality oxide-based SiC power devices and the commercial release of SiC MOSFETs.

1.5.1 Nitridation

In 1997, H. Li *et al.*[49] demonstrated that high temperature (1100 °C) NO annealing reduces the D_{it} at SiO_2/6H-SiC interfaces. In 2000, G.Y. Chung *et al.*[24] reported the effects of NO annealing on SiO_2/4H-SiC interface, and found that nitrogen is incorporated only at the interface during NO annealing. The interface nitrogen coverage is very efficient to reduce the density of states (by a factor of ≈ 10). With this annealing, the field-effect mobility of Si-face 4H-SiC MOSFETs can be increased to 30∼35 $cm^2V^{-1}s^{-1}$. These pioneering works have triggered a lot of interest in this field, and a variety of nitridation techniques have been intensively investigated.

In 2004, T. Kimoto *et al.*[44] investigated the N_2O annealing on SiO_2/4H-SiC interface, and found that it also greatly improves the interface properties and reduces interface states significantly. With lightly doped *p*-body, the Si-face MOSFET device can yield 26 $cm^2V^{-1}s^{-1}$. However, the N_2O treatment is not as efficient as NO because at high temperature, N_2O decomposes into a small fragment of NO and a large percent of N_2 and O_2. The undesired byproducts lead to competing reactions and hinder the incorporation process of N into the interface.

Nitridation by ammonia (NH_3) annealing and its effect in MOS capacitors with deposited SiO_2 films was reported by G.Y. Chung *et al.*[50] and E. Pitthan *et al.*[51]. G.Y. Chung *et al.* found that unlike NO annealing, nitrogen is incorporated throughout the oxide layer (bulk and interface) during NH_3 annealing. NH_3 annealing is demonstrated to be effective for the reduction of the effective oxide charge and the interface state density near the conduction band edge in *n*-4H-SiC/SiO_2 MOS capacitors, however, it has little improvement on *p*-type 4H-SiC/SiO_2 interfaces. E. Pitthan *et al.*'s study shows that the nitrogen incorporation by NH_3 annealing is in the form of nitrogen bonded only to silicon, or in the form of silicon oxynitrides. The authors also point out that NH_3 annealing deteriorates the dielectric strength of the dielectric films and thus causes high leakage current.

In 2014, A. Modic *et al.*[52] investigated another nitridation method with nitrogen plasma based annealing process. This process results in substantially greater interfacial N coverage at the SiO_2/4H-SiC interface and lower interface trap densities than the standard NO annealing process. However, with regard to the field-effect mobility, this process does not provide any improvement compared to that of NO-annealed MOSFETs.

Recently, A. Chanthaphan *et al.*[53] found that the high temperature post-oxidation annealing (POA) in N_2 gas can also incorporate a sufficient amount of nitrogen atoms directly into thermal SiO_2/SiC interfaces. This nitridation method requires high annealing temperatures ($> 1350\,^{\circ}$C) and is effective for thin SiO_2 layers (< 15 nm).

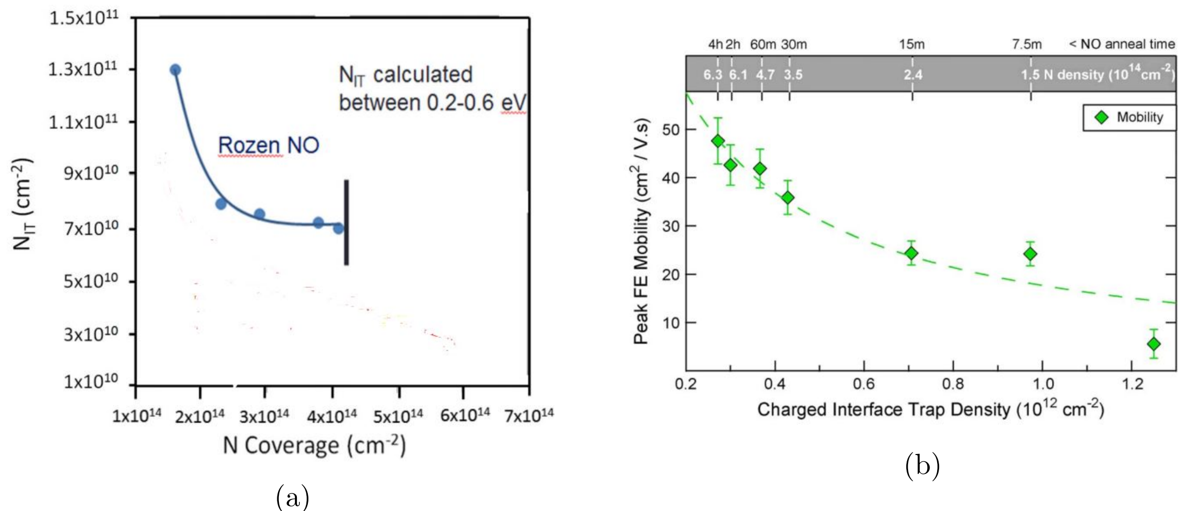


Figure 1.13: (a) As nitrogen coverage at the interface increases, the total number of the interface traps in the device decreases [54], (b) The maximum mobility of the device increases as total number of the interface traps decreases[55].

Behind all different ways of nitridation, it is interesting to see some relationship which connects the nitrogen coverage at the SiO_2/SiC interface and the electrical properties. J. Rozen *et al.*[45;55] proposed a “scaling” relationship between the nitrogen coverage, the number of interface traps (N_{it}), and the peak mobility of the device. For the same substrate doping, as nitrogen coverage at the interface increases, the N_{it} of the device decreases, as seen in Fig.1.13a, here N_{it} was derived by integrating the density of interface traps (D_{it}) from E_C - 0.2 eV to E_C - 0.6 eV. Competing nitridation and oxidation reactions limit the

maximum nitrogen coverage obtainable from standard NO passivation. This limit is represented by the vertical line. On the other hand, the second scaling relationship is that as N_{it} decreases, maximum mobility increases (Fig.1.13b). Combining these two relationships, one can agree to the following conclusion: for the same substrate doping, larger nitrogen coverage would be beneficial in that it further decreases the N_{it} and increases the channel mobility.

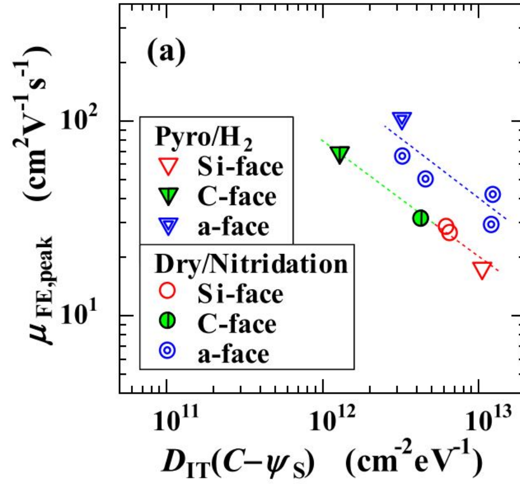


Figure 1.14: H. Yoshioka scaling: correlation between peak field-effect mobility ($\mu_{FE,peak}$) and D_{it}(C-ψ_s) at E_C - 0.2 eV.[56]

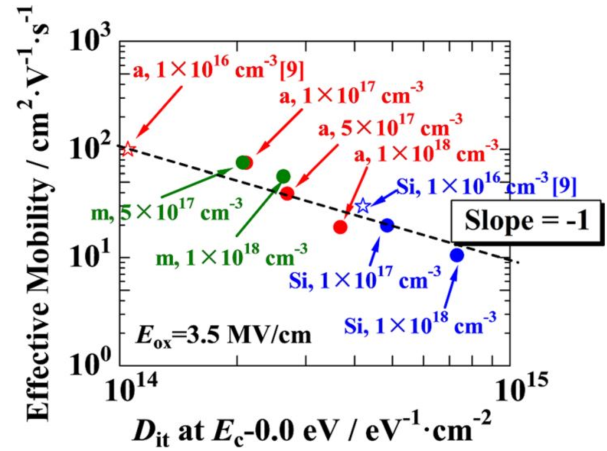


Figure 1.15: Kobayashi scaling: Linear correlation between the channel mobility of 4H-SiC MOSFETs at room temperature and the estimated D_{it} at E_C - 0.0 eV.[43]

Taking account of different crystal faces and p-body dopings, H. Yoshioka *et al.*[56] (Fig.1.14) and T. Kobayashi *et al.*[43] (Fig.1.15) proposed similar scaling relationships. Both exhibit a linear correlation between peak mobility and the D_{it} close to the conduction band of 4H-SiC. Interestingly, T. Kobayashi *et al.* observed that the scaling is valid regardless of crystal face (Si-, a-, m-face) or acceptor density of p-body. This fact suggests that at low field range where Coulomb scattering competes with the surface phonon scattering mechanism, the peak value of mobility is governed by the interface trap density D_{it} (or N_{it} the integrated D_{it}). D_{it} affects the transconductance, which is the increasing rate of the mobility curve. The position of peak mobility is where the rising of Coulomb scattering mobility becomes suppressed by the surface phonon scattering mechanism. Note that D_{it} is in log scale, and

the linear slope is -1. In fact, this slope -1 correlation was reported by S. Nakazawa *et al.*[42] as well.

In their quantification of interface traps, the C-ψ_s method[57] and subthreshold slope method[58] were used respectively. These two methods will be discussed in the following chapters of this thesis.

1.5.2 Phosphorus incorporation

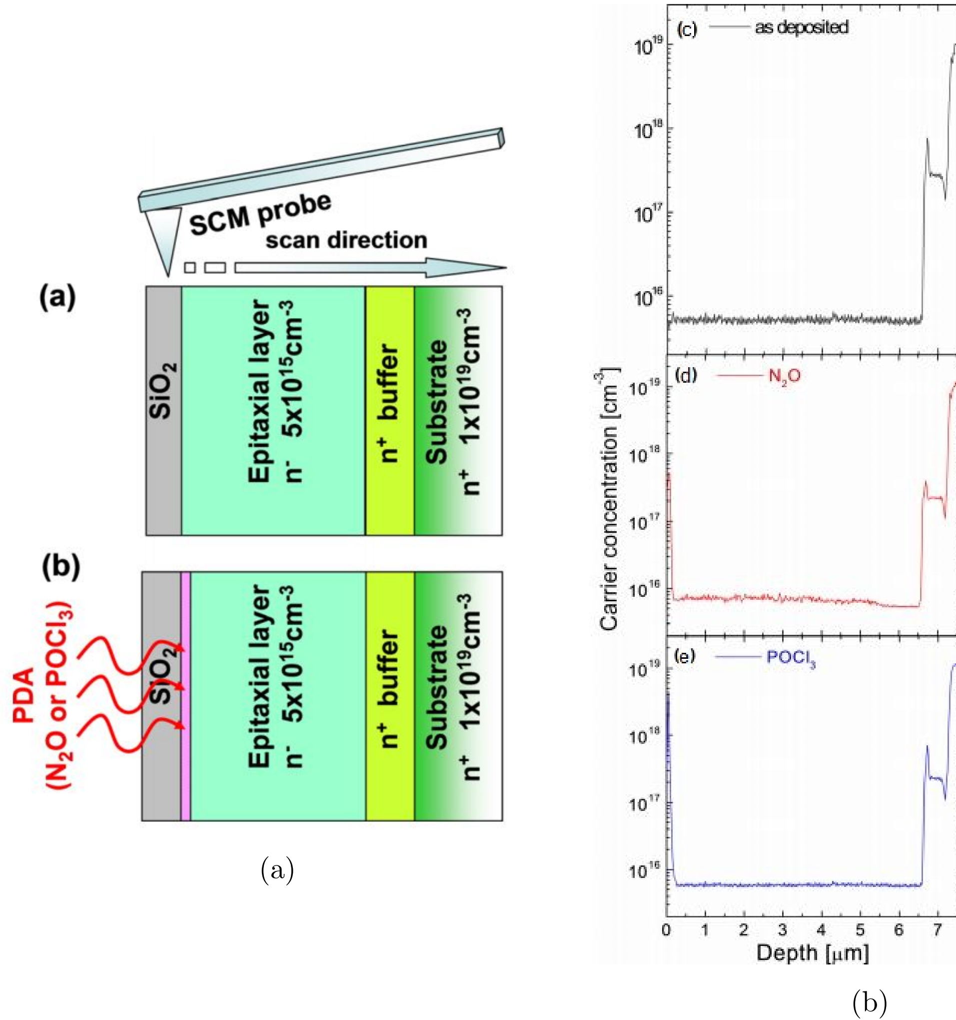
Phosphorus incorporation converts SiO_2 into phospho-silicate glass (PSG). In Si filed-effect transistors, a very thin PSG film is used outside of the thermally grown SiO_2 layer to improve the device behavior, in that the PSG film acts as a Na^+ ion getter and a barrier against Na^+ ion drift, thereby lessening the mobile ion effect in the SiO_2 dielectric and stabilizing the device characteristics[59;60].

In SiC technology, PSG is used not as a mobile ion getter but the dielectric itself. High inversion layer mobility of 89 $cm^2V^{-1}s^{-1}$ on Si-face of 4H-SiC and lower D_{it} compared to NO annealing were achieved by D. Okamoto *et al.*[47] via annealing thermal SiO_2 in phosphoryl chloride ($POCl_3$). Afterwards, Y. Sharma *et al.*[61] reported similar results in PSG annealing using a SiP_2O_7 planar diffusion source (PDS). Unfortunately, PSG is a polarizable material and can therefore lead to threshold voltage instability. H. Yano *et al.*[62] studied the threshold voltage instability in PSG gate dielectric and compared it to nitrided gate dielectric, and found that the oxide traps in phosphorus-doped oxides are the main origin of the threshold voltage instability via the capture of electrons.

In order to reduce the PSG polarization effect, a stacked gate oxide structure consisting of a thin PSG interfacial layer ($\sim$ 10 nm) and a deposited oxide ($\sim$ 35 nm) was proposed[63]. This led to a significant improvement in threshold voltage stability while maintaining high peak field effect mobilities, up to 70 $cm^2V^{-1}s^{-1}$. A similar structure with good stability in MOS capacitor was also reported by T. Akagi *et al.*[64].

Besides PSG post-oxidation annealing, T. Sledziewski *et al.* [65;66] investigated the effect of pre-oxidation phosphorus implantation, and observed the reduction of trap density and flat-band voltage shift to the left in MOS capacitors.

1.5.3 Interfacial counter-doping



(a)

(b)

Figure 1.16: (a) Schematic of scanning capacitance microscopy measurement on the side cross section of samples prepared with P or N treatments and on reference sample. (b) Measured carrier concentration profiles of reference, with N and P treatments are shown in (c)- (e), respectively.[67]

In addition to the passivation effect, group V elements, with 5 electrons in the outmost electronic shell, in SiC can serve as donors, since they are able to free one extra electron

after they are bonded with Si or C atoms. Therefore, once these atoms accumulate at the SiO_2/SiC interface and substitute the Si or C atoms, they can dope the surface of SiC. This doping effect is confirmed by the scanning capacitance microscopy (SCM) profiling of the interfacial charges caused by N or P incorporation[67]. Compared to a reference sample, Fig.1.16 shows the SCM measured carrier concentration profiles of samples with N and P treatments. The profiles indicate that both N and P are distributed within a very thin layer at the interface. Compared to the reference sample as dry-oxidized, the interfacial activated nitrogen concentration is 5×10^{17} cm^{-3}, and for phosphorus 4.5×10^{18} cm^{-3}. This fact indicates that phosphorus activation energy level in SiC is shallower than nitrogen, hence it is easier to activate and the concentration of one order higher in magnitude is detected.

In n-channel MOSFET, the substrate is p-type doped. Therefore, the doping effect of group V elements is referred as counter-doping effect. A very thin counter-doping in MOSFET can be easily depleted by the adjacent p-well without gate bias, resulting in normally off devices. The counter-doping effect benefits the channel field-effect mobility for these reasons: (i) In inversion mode, the positive ion cores introduced by counter-doping reduce the electrical field at the interface, making the slope of band less bending, thereby raising the surface potential, as depicted in Fig.1.17[68]. At the same gate bias, the effective channel depth shall be widened, which results in the free carriers located further away from the Coulomb scattering sites at the interface. (ii) At lower transverse fields regime, the additional supply of electrons from counter-doping can bring more effective screening from Coulomb scattering.

Note that the counter doping mainly affects the mobility at low field regime where the free electron density is low and Coulomb scattering is the dominant limiting factor, while it has little effect on surface roughness scattering at high field regime. Since the surface roughness scattering is associated with the transverse electrical field, the inversion electron density greatly overwhelms the counter doping carrier density at high field regime, minimizing the counter doping effect thereby.

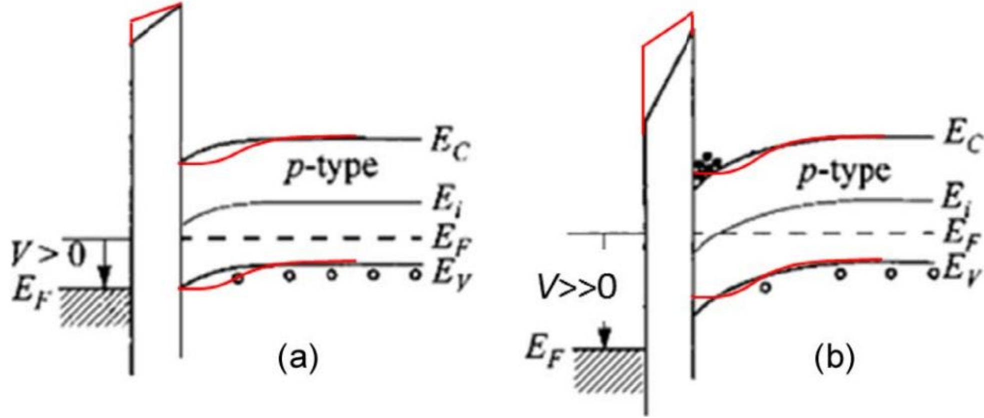


Figure 1.17: Energy-band diagrams of an n-channel MOSFET, in (a) depletion and (b) strong inversion, where the standard enhancement mode structure is illustrated in black and the n-type counter-doping effect is highlighted in red.[68]

Counter-doping effect via ion implantation of nitrogen in the SiC channel was first discussed by K. Ueno *et al.*[70], and two consequences associated with this effect were identified. As the interfacial nitrogen density increases, the observed channel mobility increases, while the threshold voltage decreases.

1.5.4 Combination of different group V elements

In 2013, H. Yano *et al.*[69] investigated the effect of the combination of NO and $POCl_3$ annealing on the electrical properties and stability of 4H-SiC MOS capacitors and MOSFETs. This combination suppresses more interface trap density than NO or $POCl_3$ only. While the MOSFET mobility exceeds that of NO annealing but is still lower than $POCl_3$ annealing, as shown in Fig.1.18a. In addition, the combination of NO and $POCl_3$ annealing results in much smaller threshold voltage shift under high electrical field stress (6 MV/cm), as seen in Fig.1.18b. The authors ascribed the stable characteristics to the strong Si-N bonds and relaxation effect of phosphorus at the interface.

In 2014, A. Modic *et al.*[48] combined pre-oxidation antimony (Sb) implantation and NO annealing, and obtained a channel mobility of > 100 cm^{2}V^{-1}s^{-1} while maintaining a positive threshold voltage, as shown in Fig.1.19. Sb is not expected to passivate interface

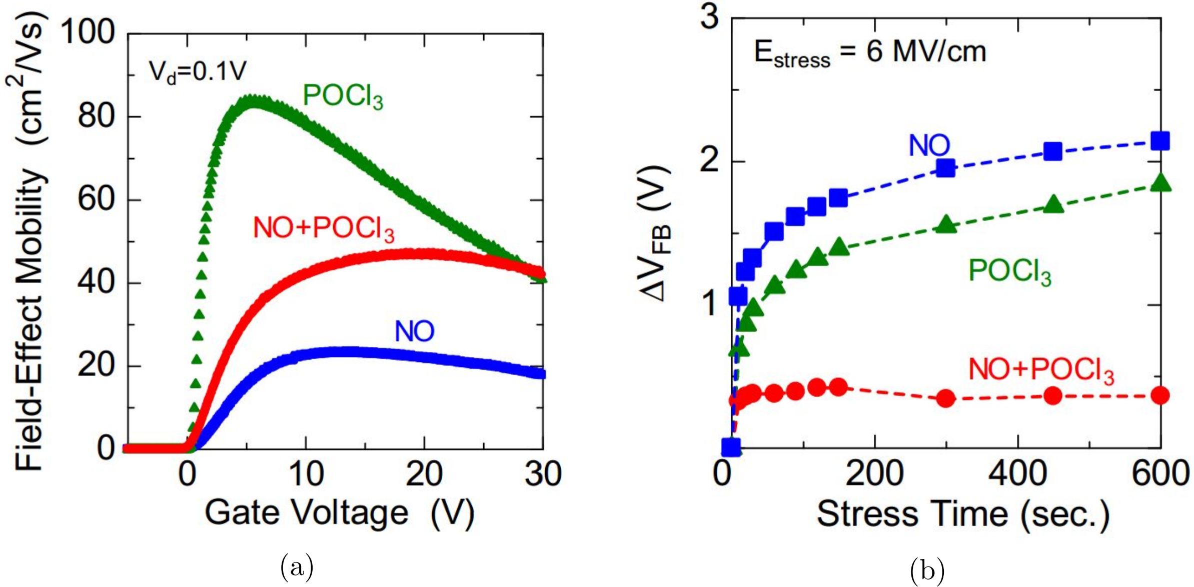


Figure 1.18: (a) Field-effect mobility of MOSFETs comparison for NO annealing, $POCl_3$ annealing and the combined annealing.[69] (b) Variation of flat-band voltage shift with constant field stress of 6 MV/cm.

traps due to its large atomic size, therefore only serves as *n*-type dopants in the surface channel. The authors attributed the mobility enhancement to the counter-doping effect from Sb in conjunction with NO passivation of the interface states. From the low temperature measurement measurement, they clearly separated these two mechanisms.

1.5.5 Universal behavior in NO-treated devices

We fabricated 4H-SiC MOSFET devices with arsenic (As) and antimony (Sb) incorporation plus NO annealing. As and Sb were introduced from pre-oxidation ion implantation. During the device processing, 30 min NO annealing was followed by the gate oxidation, which consumed certain thickness of As or Sb layer, only leaving a thin counter-doping layer. The mobility results[71](Fig.1.20b) indicate a universality at high electrical field for those NO-treated devices.

The figure shows that the mobility curves of four devices merge at high field region, which is similar to the universal mobility behavior in Si MOSFETs[72–74] (shown in Fig.1.20a). Arsenic plus NO device has more counter-dopants in the inversion channel layer, which

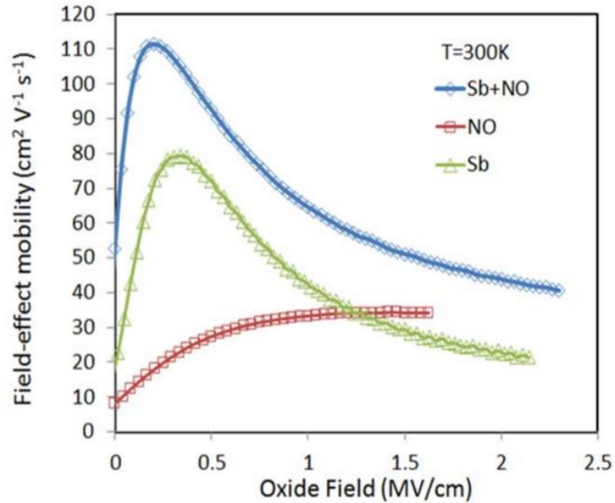


Figure 1.19: Room temperature field-effect mobility of 4H-SiC MOSFETs fabricated with the combination of Sb implantation and NO annealing.[48].

causes higher mobility than the antimony plus NO device and a smaller threshold voltage. The authors suggest that the universal behavior results from the same roughness scattering mechanism of NO annealing. In the figure, we notice that poly-silicon gate results in a more positive threshold voltage, which is beneficial in practice.

1.6 Motivation of phosphorus incorporation variation

As discussed above, J. Rozen *et al.* proposed the scaling correlation between the nitrogen interfacial coverage and the electrical properties. For post-oxidation annealing in NO, a common nitridation method, it has been reported that the N concentration at the interface varies with NO annealing time and temperature [46]. The interface state density is reduced with increasing N interfacial coverage. And this effect almost saturates at a concentration 6×10^{14} cm^{-2} of interfacial N atoms [45;75]. This saturation value is thought to originate from the competition between N binding at host sites and N removal during the slow re-oxidation occurring in parallel.

Y. Xu *et al.*[76] investigated the the concentration, chemical bonding, and etching behavior of P and N at the SiO_2/4H-SiC (0001) interface using photoemission, X-ray photoelectron

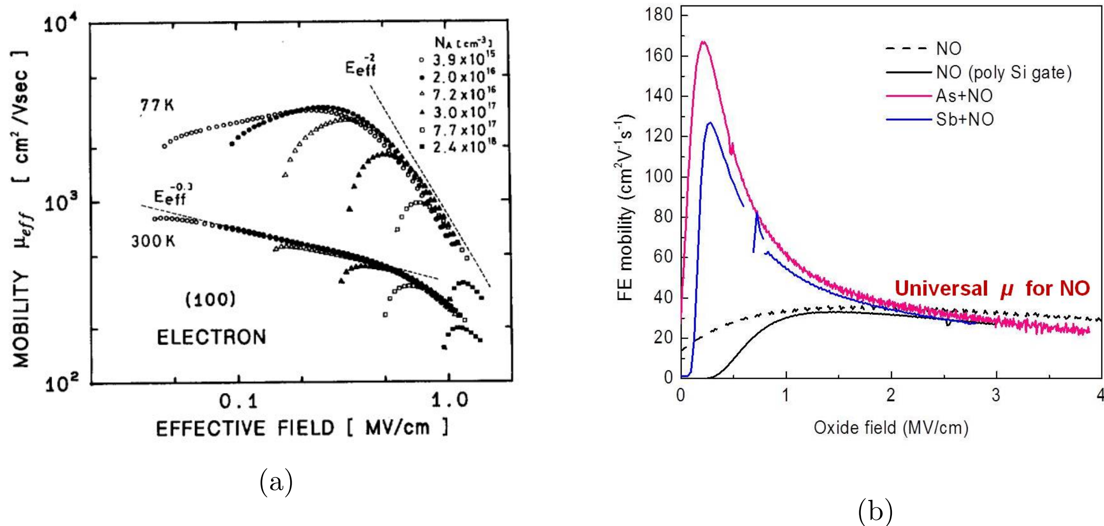


Figure 1.20: (a)Electron mobility in inversion layer at 300 K and 77 K versus effective field E_{eff}, as a parameter of substrate acceptor concentration N_A. (b) Room temperature field-effect mobility for devices with varying doping channel concentration (by counter doping of As or Sb), exemplifying a universal mobility curve related to NO annealing.

spectroscopy (XPS), ion scattering and secondary ion mass spectrometry (SIMS). Fig.1.21 is the SIMS profile of PSG and NO annealed dielectric/SiC structure. As we pointed out above, phosphorus incorporation converts the thermal SiO_2 into phospho-silicate glass, while NO annealing does not change the composition of SiO_2 in the bulk. SIMS profile shows that the PSG chemical composition is approximately uniform throughout the PSG layer, while N is accumulated exclusively at the interface for a standard NO annealed SiO_2/4H-SiC sample.

Both interfacial P and N are found to be strongly bonded to the interface and resistant to buffered HF solution etching. The medium energy ion scattering spectroscopy (MEIS) on the samples after etching reveals that both the passivating nitrogen and phosphorus are confined within 0.5 nm of the interface. Angle resolved photoemission spectroscopy (ARPES) shows that P and N are likely situated in different chemical environments at the interface.

The N atoms are primarily bound to Si atoms at the interface in NO annealing, while the interface phosphorus atoms are primarily bound to oxygen atoms, same as in the PSG bulk. Fig.1.22 shows the P 2p XPS spectrum from 4H-SiC before (black) and after (red) an etch in buffered HF etchant. The P 2p peak position of the residual P (after total etching)

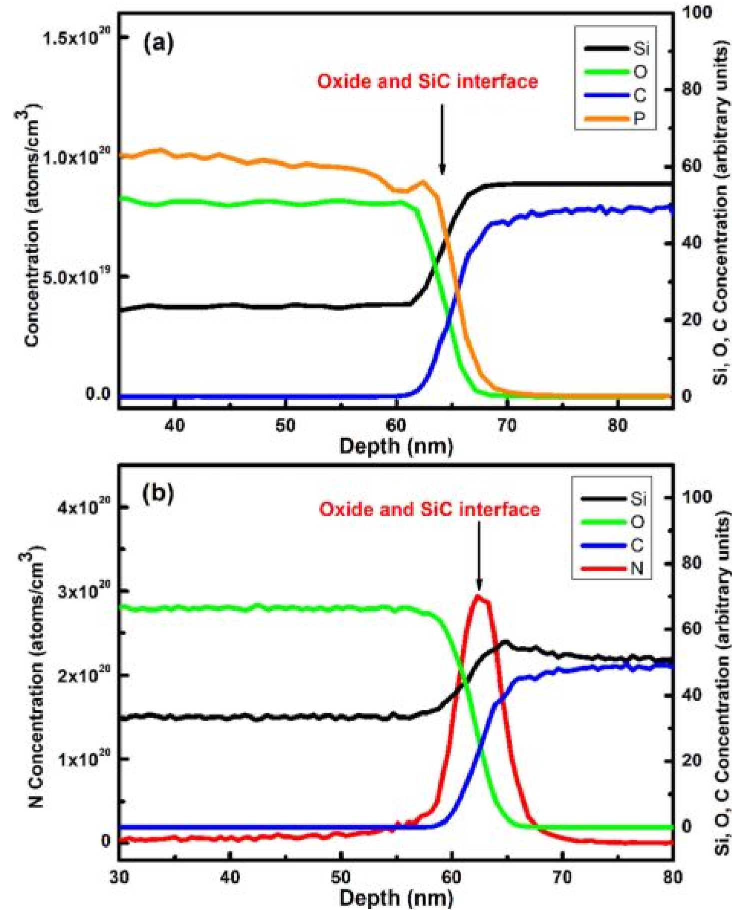


Figure 1.21: SIMS profile of (a) PSG/SiC structure and (b) an NO annealed SiO_2/SiC structure.[76]

at the interface is shifted 0.6 eV from the PSG bulk towards a lower binding energy. This implies that phosphorous atoms at the interface are still primarily bound to oxygen atoms, not silicon. This binding energy shift reflects a slightly different chemical environment for P at the PSG/SiC interface than in the bulk of the PSG.

The main motivation of this thesis work is to investigate the possible correlations between the phosphorus uptake (both at the interface and in the bulk of PSG) and the electrical properties of MOS devices. For phosphorus, as a passivation agent from the same group, it is highly likely that a similar correlation exists between the interfacial phosphorus coverage and the device electrical properties. However, some basic differences lie in the way nitrogen and phosphorus incorporate in the dielectric or at the interface.

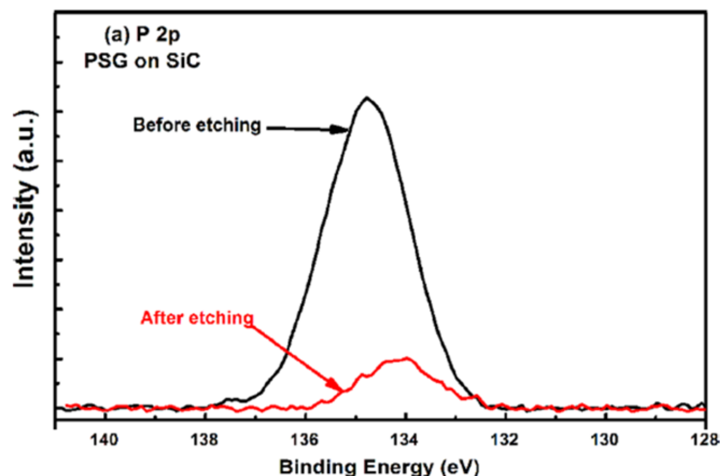


Figure 1.22: XPS spectrum of P 2p electron before and after etching at the PSG/SiC interface.

1.7 Thesis outline

In chapter 2, we are going to introduce the fundamentals of MOS devices, the interface traps, and several characterization methods.

In chapter 3, the properties of phospho-silicate glass (PSG) dielectric will be discussed. We are going to introduce two PSG formation methods and their difference. $POCl_3$ annealing is used for this research. Based on the P_2O_5-SiO_2 phase diagram for PSG dielectric, we are going to discuss the P uptake variations obtained in the PSG dielectrics by changing the annealing temperature.

In chapter 4, the correlation between the different P uptake and the electrical properties of MOS devices will be studied. Using multiple characterization techniques, we will compare the interface trap density between nitrogen and phosphorus incorporations. The effect of PSG dielectric on 6H-SiC will also be investigated.

In chapter 5, the mechanisms in PSG-gate dielectric instability will be discussed. Aiming to have a better control in the device stability, we are going to show the preliminary results using the thin PSG structure.

Chapter 6 will be the conclusion and some suggestions about future work.

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Chapter 2

Electrical characterization of MOS interface

2.1 MOS fundamentals

The basic concepts of metal-oxide-semiconductor (MOS) devices were proposed by J. E. Lilienfeld in his patent (patent number: US1900018 A) in the early 1930s. Laboratory studies were performed in the late 1940s but the device remained in the laboratory for over a decade following that. In 1959, Kahng and Atalla demonstrated a working MOS transistor [1]. After that, the development of techniques reliably growing oxides and the establishment of basic theories of operation started to take off.

Based on MOS structure, two kinds of useful devices are well-studied, two-terminal MOS capacitor, and three-terminal MOS field-effect transistor (MOSFET). Here we will discuss the basic concepts and theories for n-type MOS capacitors and (p-substrate) n-channel MOSFETs operation.

2.1.1 Capacitance of the N-type MOS capacitor

The MOS capacitor is the simplest form of two-terminal MOS device. The schematic structure of an MOS capacitor is shown in Fig.2.1. In ideal case, the capacitance of the MOS system is associated with a series connection of the oxide capacitance C_{ox} and the semiconductor capacitance C_s across the surface region, as sketched in Fig.2.2. Here, the ideal condition means that the oxide/semiconductor interface is nearly perfect, the interface trapped charge Q_{it} is negligible.

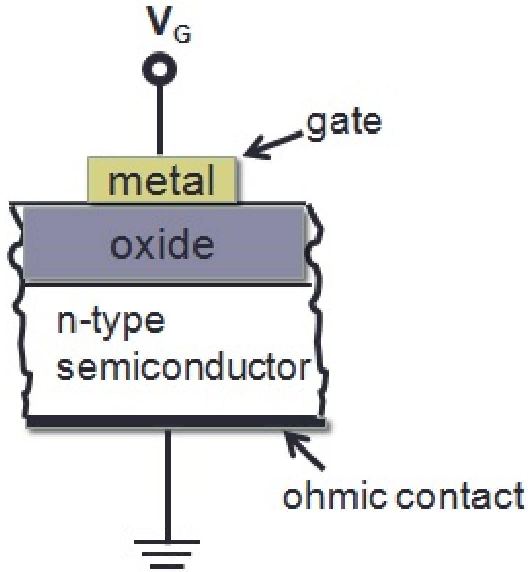


Figure 2.1: The schematic of n-type MOS capacitor structure.

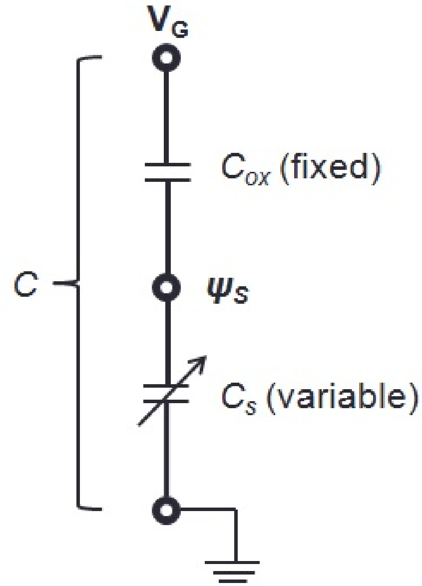


Figure 2.2: The equivalent circuit for the overall capacitance C with voltage V_G, ψ_s, and 0 (grounded) at the gate, interface and substrate, respectively.

According to Fig.2.2, the total applied gate voltage V_G is divided into the potential ψ_s in the semiconductor and the voltage drop in the oxide V_{ox}. When no flat-band voltage is considered, the gate voltage V_G can be written as

$$V_G = V_{ox} + \psi_s \tag{2.1}$$

And the overall capacitance

$$C = \frac{1}{1/C_{ox} + 1/C_s} \tag{2.2}$$

For the ideal case, the surface potential $\phi(x)$ as a function of position x is given by the Poisson equation,

$$\frac{d^2\phi(x)}{dx^2} = -\frac{\rho(x)}{\epsilon_s} \tag{2.3}$$

where $\rho(x)$ is the charge density composed of immobile ionized donors and acceptors and mobile holes and electrons, ϵ_s is the dielectric permittivity of semiconductor.

The surface potential at the interface ψ_s is defined as

$$\psi_s \equiv \frac{1}{q}(E_i(\infty) - E_i(0)) \tag{2.4}$$

By solving the Poisson equation, the charge per unit area in the n-type semiconductor Q_s can be obtained[2]:

$$Q_s = \mp\sqrt{2q\epsilon_s N_D}\sqrt{\phi_t e^{\psi_s/\phi_t} - \psi_s - \phi_t + e^{-2\phi_B/\phi_t}(\phi_t e^{-\psi_s/\phi_t} + \psi_s - \phi_t)} \tag{2.5}$$

where N_D is the n-type doping concentration, $\phi_t = k_B T/q$, $q\phi_B = k_B T \ln\left(\frac{\mathrm{N_D}}{\mathrm{n_i}}\right)$ is the bulk potential, k_B is the Boltzmann constant. The + sign in front of the right side of the equation must be used with $\psi_s < 0$ (depletion or inversion), and the − sign with $\psi_s > 0$ (accumulation).

Then the surface capacitance per unit area[2] is

$$C_s = -\frac{dQ_s}{d\psi_s} = \pm\sqrt{2q\epsilon_s N_D}\left\{\frac{1 - e^{\psi_s/\phi_t} + e^{-2\phi_B/\phi_t}(e^{-\psi_s/\phi_t} - 1)}{2\sqrt{\phi_t e^{\psi_s/\phi_t} - \psi_s - \phi_t + e^{-2\phi_B/\phi_t}(\phi_t e^{-\psi_s/\phi_t} + \psi_s - \phi_t)}}\right\} \tag{2.6}$$

For p-type semiconductor, Eq(2.5) and Eq(2.6) are with the similar forms, only substituting N_D with N_A and ψ_s with $-\psi_s$. Fig.2.3 shows the surface charge density $|Q_s|$ as a function of surface potential for p-type silicon having $N_A = 4 \times 10^{15} cm^{-3}$, $T = 300K$ [3].

Usually the doping concentration in wide band gap semiconductor is several orders higher than the intrinsic carrier density n_i, therefore, $\phi_B = \frac{kT}{q}\ln(\frac{\mathrm{N_D}}{\mathrm{n_i}})$ is several times of ϕ_t.

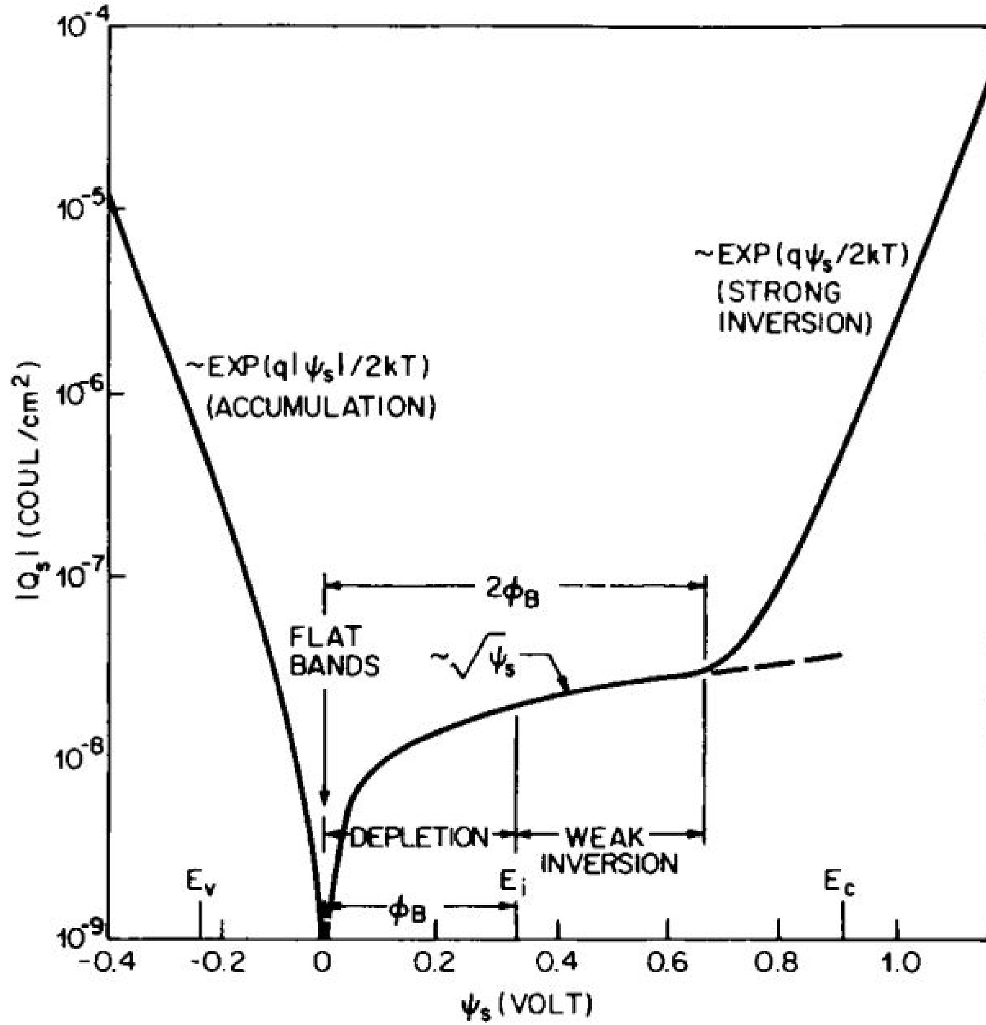


Figure 2.3: The surface charge density $|Q_s|$ as a function of surface potential ψ_s for ***p*-type** silicon in different operation mode.[3]

Taking this into consideration, in Eq.2.6, $e^{-2\phi_B/\phi_t} \sim 0$ would be a good approximation, and the equation itself can be reduced to

$$C_{s,\text{theory}}(\psi_s) = \frac{qN_D \left|\exp\left(\frac{\psi_\text{s}}{\phi_\text{t}}\right) - 1\right|}{\sqrt{\frac{2kTN_D}{\epsilon_S}\left\{\exp\left(\frac{\psi_\text{s}}{\phi_\text{t}}\right) - \frac{\psi_\text{s}}{\phi_\text{t}} - 1\right\}}} \tag{2.7}$$

For an ideal MOS system, as the bias voltage is changed, the surface potential ψ_s changes correspondingly and the MOS capacitor (n-type) experiences different operation modes. Here, for the convenience in our following study, we only discuss flat-band, accumulation,

and depletion mode for n-type MOS capacitor, and later the inversion mode for n-channel (p-type substrate) MOSFET.

Flat-band

Energy band diagram of an ideal n-type MOS capacitor at flat-band is shown in Fig.2.3. Under this mode, there is zero charge stored at the gate and the interface. Due to no electrical field across the device, the band diagram shows no bending. Most of the cases, the metal

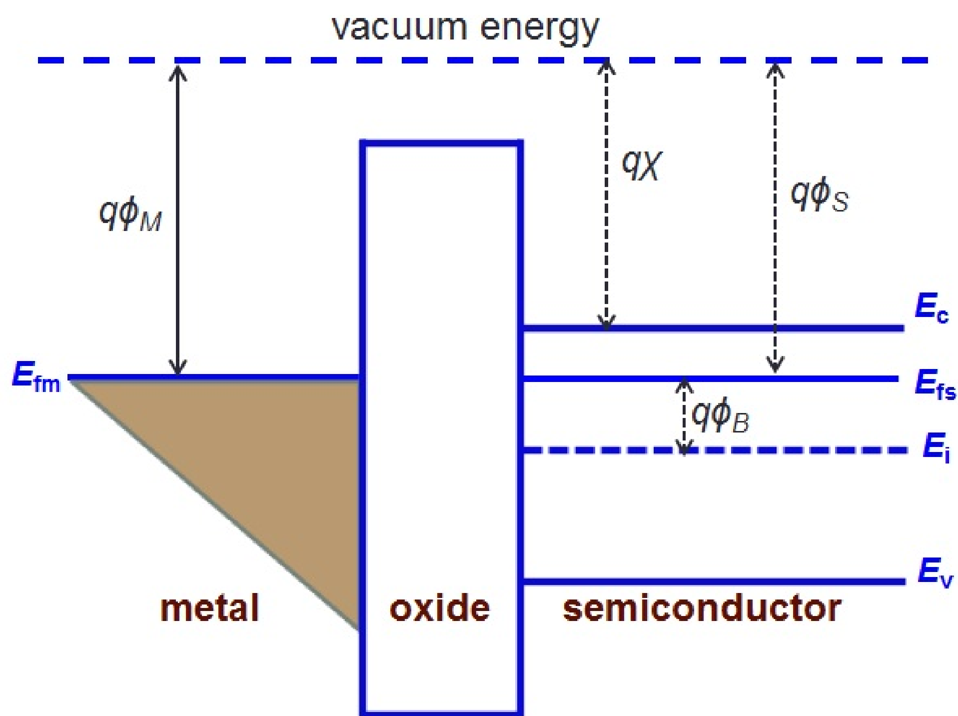


Figure 2.4: Energy band diagram of an ideal ***n*-type** MOS capacitor at flat-band mode.

work function (ψ_m) is not equal to the semiconductor work function (ψ_s). Once the metal makes contact with the oxide/semiconductor, the system would automatically form a built-in potential and store charges on the MOS capacitor due to the thermal equilibrium. To achieve the flat-band diagram, the applied voltage must be set to a value that exactly compensates the difference in the work functions. Hence this voltage is called *flat-band voltage*, and given

by

$$V_{FB}^0 = \Phi_M - \Phi_S \equiv \Phi_{MS} \tag{2.8}$$

where V_{FB}^0 is the flat band voltage, Φ_M is the metal work function, and Φ_S is the semiconductor work function. The work function is the minimum amount of energy required to remove an electron from the material. And in the figure, the difference between the vacuum level and the conduction band edge is χ, called the *electron affinity*.

Typically in a MOS system, there are additional charges intrinsically distributed in the bulk of silicon dioxide and at the oxide-SiC interface. Moreover, the processing also can induce some charged defects. These charges can be broadly classified into the following types for SiC MOS: ① oxide fixed charge Q_f and ② oxide trapped charge Q_{ot}, ③ mobile ionic charge Q_m, ④ the deep level traps whose emission and capture times are long enough, thereby behaving similarly as fixed charge. The effective interfacial charge Q_{eff} is the sum of all those types, whose number density exhibits high level (10^{11} - 10^{12} cm^{-2}) in SiC devices. Considering the existence of Q_{eff}, Eq.(2.8) should be modified as

$$V_{FB} = \Phi_{MS} - \frac{Q_{\text{eff}}}{C_{ox}} \tag{2.9}$$

The flat band voltage is an important characterization for two reasons: (1) it influences the threshold voltage for a MOSFET, as discussed later; (2) the difference between the ideal and the experimental flat-band voltages is a measure of defects and trap-related fixed charges located in the oxide as well as near the oxide-semiconductor interface.

At flat-band, $V_G = V_{FB}$, surface potential $\psi_s = 0$, the semiconductor capacitance in Eq.2.6 can be expressed as

$$C_{s,FB} \equiv C_s(\psi_s = 0) = \epsilon_s / L_D = \sqrt{\frac{q^2 \epsilon_s N_D}{kT}} \tag{2.10}$$

where $L_D \equiv \sqrt{\frac{\epsilon_s kT}{q^2 N_D}}$ is known as the *Debye length*.

The total capacitance of the MOS system C_{FB} is

$$C_{FB} = \frac{1}{1/C_{ox} + L_D/\epsilon_s} \tag{2.11}$$

Experimentally, the flat-band voltage is typically extracted from capacitance-voltage (C-V) measurements by determining the gate voltage at which the device capacitance is equal to flat-band capacitance (C_{FB}) in Eq.(2.11).

When applied bias is different from V_{FB}, the electric field will be induced in the oxide and the semiconductor, and the excess voltage results in a potential drop in the oxide V_{ox} and the oxide-semiconductor surface potential at ψ_s. Hence, Eq.(2.1) should be rewritten as

$$V_G - V_{FB} = V_{ox} + \psi_s \tag{2.12}$$

Accumulation

When a greater bias than V_{FB} is applied to the gate, holes (+Q) collect at the metal-oxide interface and electrons (-Q) collect at the oxide-semiconductor interface (Fig.2.5b). The holes build up at the metal-oxide interface, which lowers the metal Fermi level. Since the oxide prevents current from flowing in the semiconductor, the semiconductor Fermi level does not change at deep distances in the semiconductor. However, near the oxide-semiconductor interface, the semiconductor energy bands bend downward because the Fermi level must be continuous across the entire MOS system. The energy levels of the oxide are also bent due to the electric field in the oxide so that the oxide Fermi level connects the metal Fermi level and the semiconductor Fermi level, as shown in Fig.2.5a. From another point of view, the oxide and semiconductor are voltage dividers in one circuit, and the electric fields in them should have the same direction. And this causes downward bending of semiconductor energy bands.

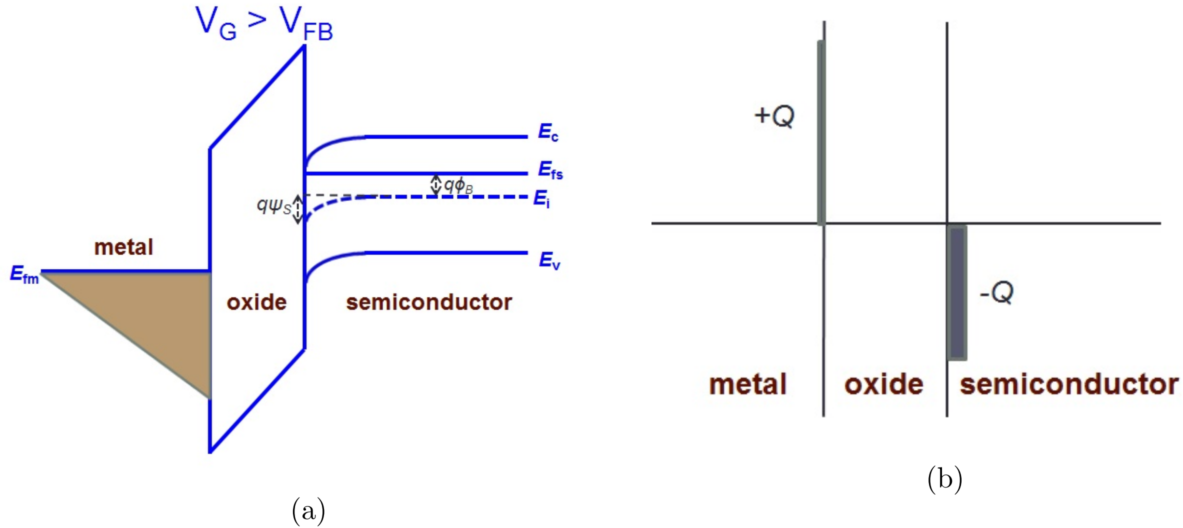


Figure 2.5: (a) Energy band diagram, (B) Space-charge diagram for an ideal ***n*-type** MOS capacitor in accumulation mode.

The buildup of majority carriers at the oxide-semiconductor interface is called accumulation. For n-type semiconductor, $\psi_s > 0$ is the accumulation condition.

Depletion

When the gate voltage is decreased below the flat band voltage, negative charges build up at the metal-oxide interface. These negative charges cause electrons to move away from the oxide-semiconductor interface, leaving behind the positive-charged donor ion cores (Fig.2.6b). The negative charges at the metal-oxide interface raise the metal Fermi level above the semiconductor Fermi level. The difference between the metal Fermi level and the semiconductor Fermi level causes the semiconductor bands to bend near the oxide-semiconductor interface, and the electric field in the oxide causes the oxide bands to bend, similar to what occurs in the accumulation regime. However, because the electric field and charge build up are opposite to what occurs in the accumulation regime, the bands bend in the opposite direction. The band diagram is shown in Fig.2.6a.

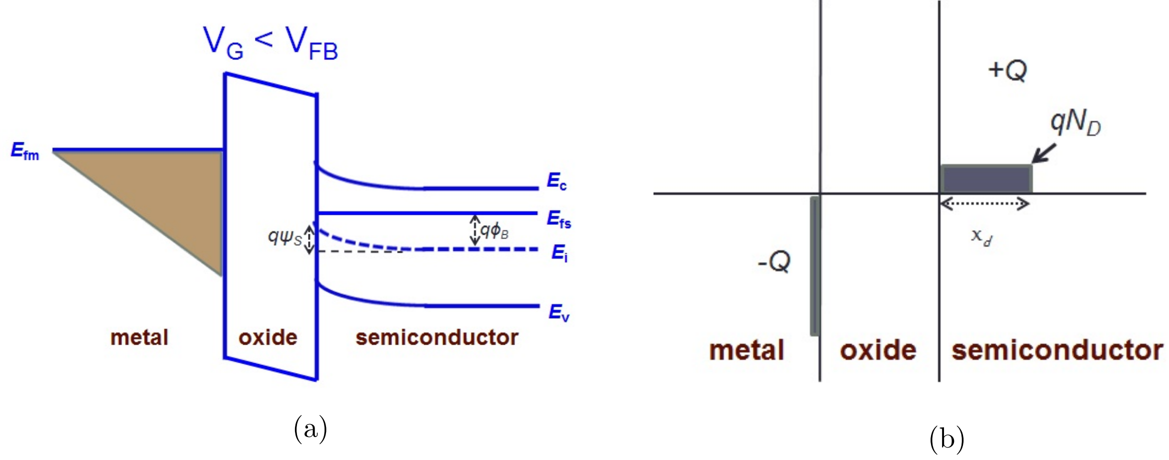


Figure 2.6: (a) Energy band diagram, (B) Space-charge diagram for an ideal ***n*-type** MOS capacitor in depletion mode.

The moving away of the majority carriers is called depletion. The depletion region is also referred as space charge region, since in this region only the ion cores (space charge) are left behind. In depletion mode, the surface potential $\psi_s < 0$.

In Fig.2.6b, we have made several assumptions about the semiconductor charge. First, the free-hole population is assumed to be everywhere so small that it needs not be considered; second, the electron density is much less than the donor density from the interface to a plane at $x = x_d$. Beyond x_d, the donor density N_D is taken to be equal to n. These assumptions make up what is usually called the ***depletion approximation***. Although they are not precisely true, they are generally sufficiently valid to permit the development of very useful relationships.

According to ***depletion approximation***, the depletion width in the semiconductor is given by

$$x_d = \sqrt{2\epsilon_s q|\psi_s|/qN_D} \tag{2.13}$$

and the space charge Q_s (per unit area) in the semiconductor is

$$Q_s = qN_D x_d = \sqrt{2q\epsilon_s N_D|\psi_s|} \tag{2.14}$$

Correspondingly, in depletion mode, the surface capacitance C_s can be expressed as

$$C_d = \frac{\epsilon_s}{x_d} = \sqrt{\frac{q\epsilon_s N_D}{2|\psi_s|}} \tag{2.15}$$

In deep depletion mode, ψ_s has a large negative value compared to ϕ_t (which at room temperature is $\sim$ 0.025V), then $e^{-2\phi_B/\phi_t}$ and e^{ψ_s/ϕ_t} terms in Eq.(2.6) are so small that can be omitted, thus Eq.(2.15) can be deduced from Eq.(2.6).

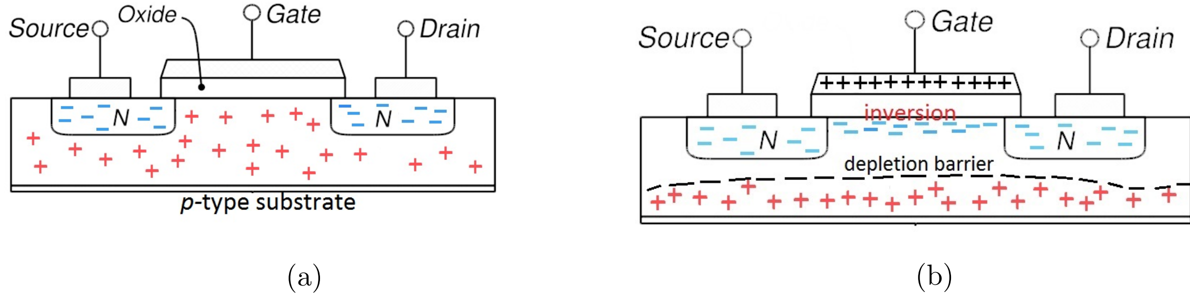
Note that the relation for one-sided abrupt junctions,

$$\frac{d(1/C_d^2)}{dV} = \frac{2}{q\epsilon_s N_D} \tag{2.16}$$

provides an experimental way to determine the semiconductor doping concentration.

2.1.2 *N*-channel MOSFET

N-channel lateral MOS field-effect transistors (MOSFETs) are three-terminal switches on p-doped substrate with highly n-doped ($\sim 1 \times 10^{20} cm^{-3}$) regions for the source and drain. When the applied gate voltage is below the threshold voltage V_T, little leakage current occurs and the device is considered to be "off" (Fig.2.7a). The n-p-n junction between the source and drain blocks current as long as the gate voltage is below threshold. If the gate voltage is positive, the applied electric field moves the majority carriers – holes – in p-doped substrate away from the oxide/semiconductor interface, and therefore forms a depletion region. Once the applied gate voltage surpasses the threshold voltage, carrier 'inversion' occurs at the interface (the surface electron concentration n_s becomes dominant and greater than surface hole concentration). The current flows along the inversion channel, and the device is considered to be "on" (Fig.2.7b). The inversion process is discussed below in more details.



(a) (b)

Figure 2.7: (a) Lateral MOSFET diagram in off state, (b) Lateral MOSFET diagram in on state: channel forms under gate oxide during inversion.

Inversion

For ***p*-type** substrate MOSFET, the condition for the surface potential is opposite to that on n-type as discussed above. As shown in the table list, the following regions of surface petential can be distinguished on p-substrate MOS system. n_s is the electron concentration at the interface.

$\psi_s < 0$	accumulation of holes (bands bend upward)
$\psi_s = 0$	flat-band condition
$\phi_B > \psi_s > 0$	depletion of holes (bands bend downward)
$\phi_B = \psi_s$	midgap with $n_s = p_s = n_i$ (intrinsic concentration)
$2\phi_B > \psi_s > \phi_B$	weak inversion ($n_i < n_s < N_A$)
$\psi_s = 2\phi_B$	onset of strong inversion ($n_s = N_A$)
$\psi_s > 2\phi_B$	strong inversion ($n_s > N_A$)

Same as n-type, $\psi_s = 0$ is the flat-band condition. After flat-band, the semiconductor depletes holes away from the interface and bands begin to bend downward. As the gate voltage increases, the depletion region continues to expand.

When $\psi_s = \phi_B$, the intrinsic Fermi level (E_i) is at the semiconductor Fermi level (E_{fs}), bringing the conduction band edge (E_c) to the Fermi level the same as to the valance band edge (E_v) at the interface. Hence, the interface becomes intrinsic $n_s = p_s = n_i$.

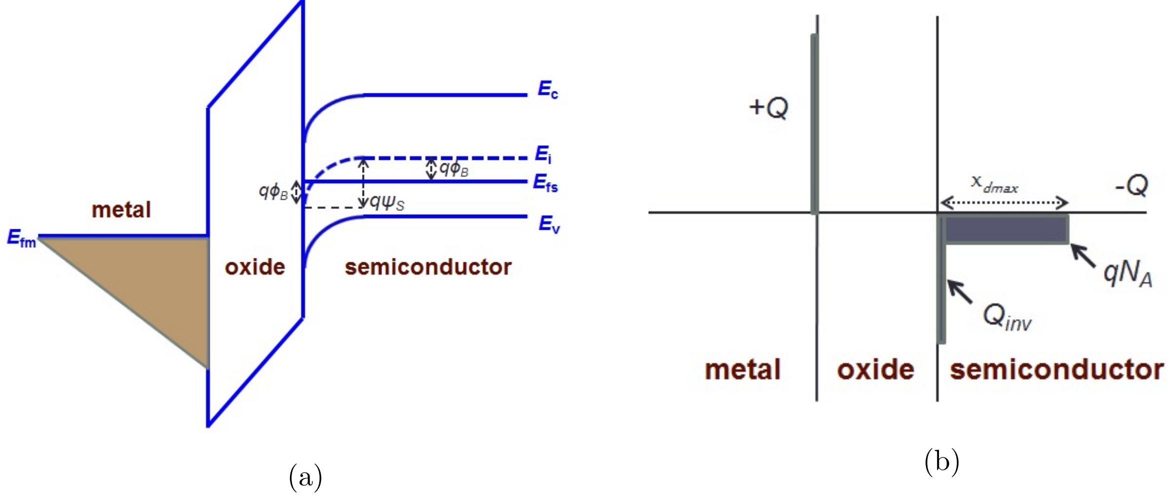


Figure 2.8: (a) Energy band diagram under strong inversion mode, (b) Space-charge diagram for an ideal ***p*-type** MOS system at strong inversion mode.

As the gate voltage increases, $\psi_s > \phi_B$, $n_s > p_s$. These negative charges "invert" the p-type material at the surface, causing the formation of a minority-carrier (electrons in this case) conducting channel, commonly known as the inversion channel.

When $\psi_s = 2\phi_B$, the surface free electron concentration n_s equals to the immobile acceptor core ion concentration N_A. This is considered to be the onset of strong inversion. Once strong inversion is reached, the surface potential remains relatively constant at $2\phi_B$ (the increase is within several ϕ_t), because n_s is increased such a sensitive function of surface potential ψ_s (exponential function, as pointed out in Fig.2.3).

At strong inversion, the maximum depletion width is reached (x_{dmax}).

$$x_{dmax} = \sqrt{\frac{4\epsilon_s \phi_B}{qN_A}} \tag{2.17}$$

Fig.2.8 shows the energy band diagram and the space-charge diagram for an ideal ***p*-type** MOS system at strong inversion.

Note that, the inversion layer can be formed in silicon under gate bias. While due to wide band gap, the net rate of Shockley-Hall-Read recombination is very small. Generally, under normal gate bias, the minority carrier generation in SiC is not enough to form an

inverted layer. However, with the free-electrons supplied from the source and drain region, the inversion layer can be formed in SiC.

2.1.3 MOSFET mobility

The carrier mobility influences the device performance through its frequency or time response in two ways. First, at low electric fields the carrier velocity is proportional to the mobility with higher mobility material leading to higher frequency response, because carriers take less time to travel through the device. Second, higher mobility devices have higher currents that charge capacitances more rapidly resulting in a higher frequency response. And more importantly, the channel resistance is reversely proportional to the carrier mobility, thus higher carrier mobility results in a lower power loss.

There are several ways to define carrier mobility in a MOSFET channel, listed as below.

Effective mobility μ_{eff}

We consider an n-channel MOSFET of gate length L and width W. The drain current I_D can be expressed as a combination of drift and diffusion currents

$$I_D = \frac{W \mu_{\text{eff}} Q_n V_{DS}}{L} - W \mu_{\text{eff}} \frac{kT}{q} \frac{dQ_n}{dx} \tag{2.18}$$

where Q_n is the mobile channel charge density, and μ_{eff} the *effective mobility*, usually measured at small drain voltages of typically 25-100 mV. The first term is the drift current when an external electrical field is applied, second term the diffusion current when there is a spatial variation of carrier densities within the material. Smaller V_{DS} is better, because then the channel charge is more uniform from source to drain, allowing the diffusive second term in Eq.(2.18) to be dropped. Solving for the *effective mobility* μ_{eff} gives

$$\mu_{\text{eff}} = \frac{g_d L}{W Q_n} \tag{2.19}$$

where the drain conductance g_d is defined as

$$g_d \equiv \frac{\partial I_D}{\partial V_{DS}}|_{V_{GS}} \tag{2.20}$$

The mobile channel charge density Q_n can be directly determined from the measurement of gate-to-channel capacitance/unit area, C_{GC}, according to

$$Q_n = \int_{-\infty}^{V_{GS}} C_{GC} dV_{GS} \tag{2.21}$$

Usually, effective electric field E_{eff} is used to characterize μ_{eff} dependence,

$$E_{\text{eff}} = \frac{1}{\epsilon_s}(Q_{dpl} + \eta Q_n) \tag{2.22}$$

where Q_{dpl} is the depletion charge per area, η a fitting parameter ($\frac{1}{2}$ is used mostly).

Field-effect mobility μ_{fe}

While the effective mobility is derived from the drain conductance, the *field-effect mobility* is determined from the transconductance g_d, defined by

$$g_m \equiv \frac{\partial I_D}{\partial V_{GS}}|_{V_{DS}} \tag{2.23}$$

The drift component of the drain current with $Q_n = C_{ox}(V_{GS} - V_T)$ is

$$I_D = \frac{W}{L}\mu_{\text{eff}} C_{ox}(V_{GS} - V_T) V_{DS} \tag{2.24}$$

Therefore,

$$g_m = \frac{W}{L}\mu_{\text{eff}} C_{ox} V_{DS} \tag{2.25}$$

When this expression is solved for the mobility, it is known as the *field-effect mobility*

$$\mu_{\text{fe}} = \frac{Lg_m}{WC_{ox}V_{DS}} \tag{2.26}$$

The discrepancy between μ_{eff} and μ_{fe} is due to the neglect of the electric field dependence of the mobility in the derivation of transconductance. Considering the μ_{eff} dependence on gate voltage,

$$\mu_{\text{fe}} = \frac{Lg_m}{WC_{ox}V_{DS}\left(1 + \frac{(V_{GS}-V_T)}{\mu_{\text{eff}}}\frac{d\mu_{\text{eff}}}{dV_{GS}}\right)} \tag{2.27}$$

Hall mobility μ_H

The Hall effect describes the behavior of the free carriers in a semiconductor when applying an electric as well as a magnetic field. The experimental setup shown in Fig.2.9a, depicts a semiconductor bar with a rectangular cross section. A voltage is applied between the two contacts, resulting in a field along the y-direction. The magnetic field is applied in the z-direction. Fig.2.9b depicts the top view of a Hall-bar MOSFET with its contacts for Hall effect measurement.

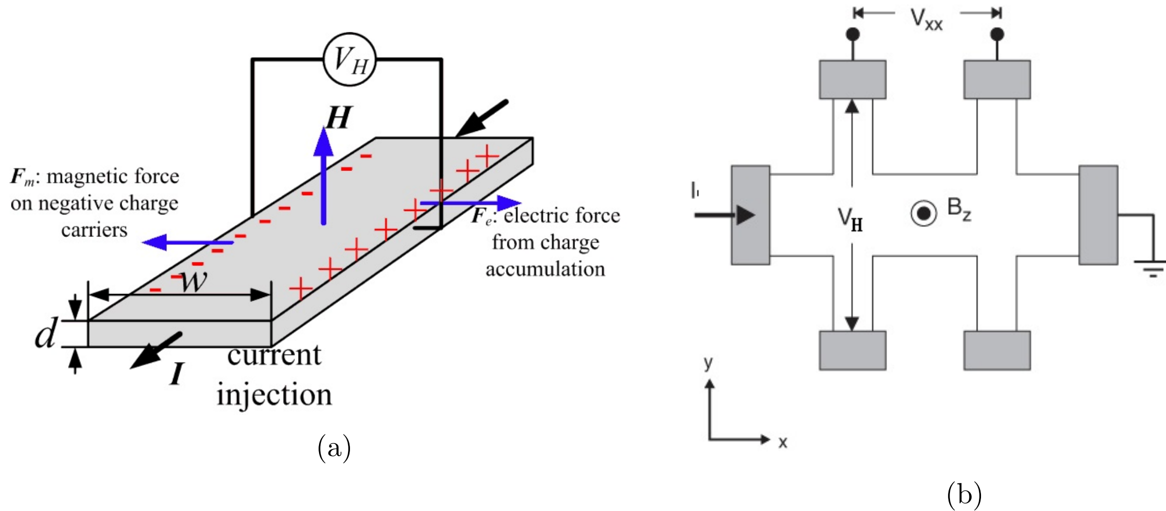


Figure 2.9: (a) Schematic illustrating the Hall effect measurement setup (b) Top view of Hall-bar MOSFET.

Hall coefficient R_H is defined as

$$R_H = \frac{dV_H}{BI} \tag{2.28}$$

where V_H is the Hall voltage.

The advantage in Hall effect measurement is that it can separate the carrier concentration and Hall mobility.

Hall mobility μ_H, defined by

$$\mu_H = \frac{|R_H|}{\rho} = |R_H| \cdot \sigma \tag{2.29}$$

and the carrier concentration is given by

$$p = \frac{1}{qR_H}; n = -\frac{1}{qR_H} \tag{2.30}$$

2.2 Interface traps

2.2.1 Chemical nature of interface traps

Interface traps or states are located at the oxide-semiconductor interface and have energy levels that exist within the forbidden band gap of the semiconductor. In silicon MOS systems, these traps can be produced by excess silicon or oxygen, dangling silicon bonds, or impurities. The presence of these traps at the Si/SiO_2 interface can be greatly reduced by forming gas anneal. In the case of SiC, due to the presence of C during thermal oxidation, the SiC/SiO_2 interface is highly disordered and several types of defects are formed with density $\sim 10^{11}$ cm^{-2}/eV in the middle of the band gap and 10^{13} cm^{-2}/eV or even more at the band edges of 4H-SiC.

Interface traps interact with the semiconductor conduction band by capturing or emitting electrons. Capture or emission occurs when interface traps change occupancy. The

changes in occupancy can be produced by changes in gate bias, light illumination, heating/-cooling, and etc.

Interface traps can be either acceptor-like or donor-like. The donor-like trap energy levels are located in the lower half of the band-gap. Those trap levels are positively charged when empty and electrically neutral when occupied by an electron. The acceptor-like energy levels are located in the upper half of the band-gap. Those trap levels are electrically neutral when empty and negatively charged when occupied by an electron.

Through theoretical and experimental study, some types of interface defects have been identified. The emission of C into SiC substrate during oxidation can generate single carbon interstitial defect (configuration: Si-C-C) and carbon dimer interstitial defect. The calculations indicate that the single carbon interstitial introduces three trap states in the bandgap at 2.5, 0.45 and 0.15 eV below the conduction band, while the carbon dimer interstitial defects (configuration: SiC-C=C-SiC) are energetically located in the midgap and at 0.1 eV below the conduction band[4–6]. Deep-level transient spectroscopy (DLTS) revealed two types of oxide defects with broad trap distribution, O1 and O2, which are energetically centered at 0.15 and 0.39 eV below the conduction band, respectively[7].

High density of interface traps in SiC MOS devices can dramatically undermine the current transport in the channel. To characterize the interface traps, several methods can be applied, including capacitance-voltage (C-V), conductance, Gray-Brown technique, deep-level transient spectroscopy (DLTS) and sub-threshold slope (SS).

2.2.2 Simultaneous high-low frequency capacitance voltage method

The low-frequency or quasi-static method is a common interface trapped charge measurement method[8]. Considering the contribution from interface traps, in depletion mode the equivalent circuit can be illustrated as Fig.2.10, where C_D is the depletion capacitance, C_{it} the interface trap capacitance which is a function of ac probe frequencies ω.

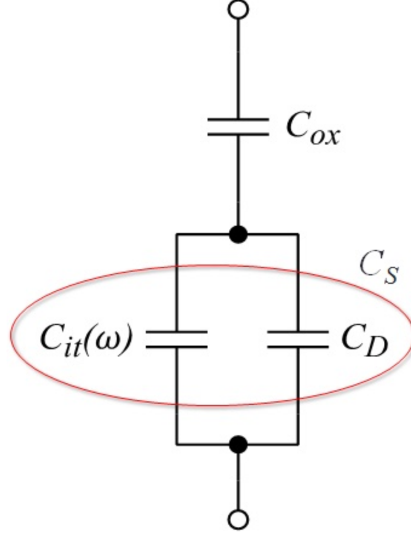


Figure 2.10: The equivalent circuit for the overall capacitance taking interface traps into account.

As the gate voltage (dc bias) is swept from accumulation to depletion, the gate charge $Q_G = -(Q_s + Q_{it})$ assuming no oxide charges. The interface traps can respond to the additional small ac signals. In simultaneous high-low frequencies capacitance voltage, "low frequency" means that all the interface traps are able to respond to the measurement ac probe frequency. In depletion mode (for n-type MOS capacitor, gate voltage $V_G < 0$), the applied "low frequency" ac signal causes two processes in one ac cycle, as depicted in Fig.2.11. When the ac signal is at the peak, it is leading to less depletion while moving the Fermi energy level slightly upward. Interface traps below the Fermi energy level can be filled, and this process is called trapping. When the ac signal is at the valley, the depletion effect becomes stronger while moving the Fermi energy level downward. This stage would cause filled trap states to emit, hence it is de-trapping process.

The charge difference Q_{it} through trapping and de-trapping introduces a capacitance C_{it} at the Fermi energy level, which is determined by the applied dc bias (since the ac signal is small). The capacitance C_{it} cannot be directly monitored, its information is included in the *low frequency* capacitance.

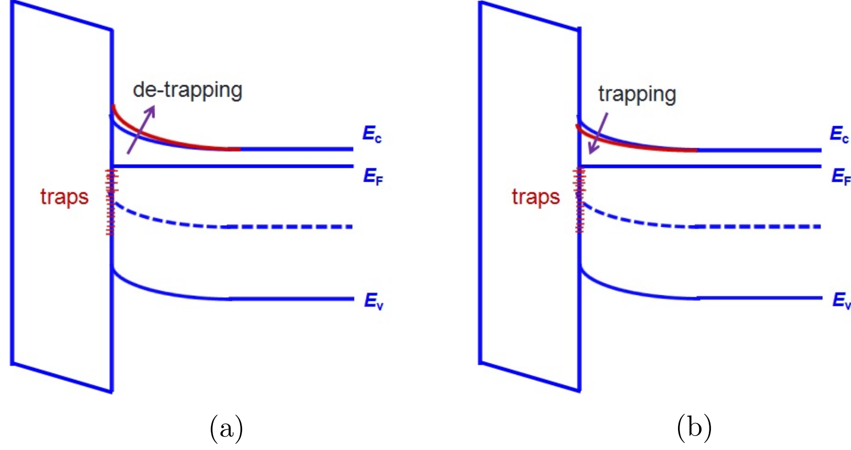


Figure 2.11: (a) Energy band diagram, (B) Space-charge diagram for an ideal ***n*-type** MOS capacitor in depletion mode.

The *low frequency* capacitance is given by

$$C_{lf} = (\frac{1}{C_{ox}} + \frac{1}{C_D + C_{it}})^{-1} \tag{2.31}$$

and C_{it} is associated to the interface trap density D_{it} by

$$C_{it} = \frac{dQ_{it}}{dE(\text{in V})} = q\frac{dN_{it}}{dE(\text{in V})} = q^2\frac{dN_{it}}{dE(\text{in eV})} = q^2 D_{it} \tag{2.32}$$

where dE is the slight change of Fermi energy level within a ac cycle.

In contrast, "high frequency" means that interface traps are not able to respond to the measurement ac probe frequency. Under this condition, $C_{it} = 0$, Fig.2.10 can be reduced to Fig.2.2. And high frequency capacitance is given by the series connection of C_D and C_{ox},

$$C_{hf} = (\frac{1}{C_{ox}} + \frac{1}{C_D})^{-1} \tag{2.33}$$

Therefore,

$$D_{it}(high - low) = \frac{C_{ox}}{q^2}\left(\frac{C_{lf}/C_{ox}}{1 - C_{lf}/C_{ox}} - \frac{C_{hf}/C_{ox}}{1 - C_{hf}/C_{ox}}\right) \tag{2.34}$$

This formula can be used to determine D_{it} as a function of gate voltage, while it is more relevant to determine D_{it} as a function of surface potential ψ_S or the energy level in the semiconductor. Hence, Berglund formula is used to determine the surface potential in high-low C-V method,

$$\psi_S(V_G) = \int (1 - \frac{C_{QS}}{C_{OX}}) dV_G + A \tag{2.35}$$

where A is an integration constant.

Integration from $V_G = V_{fb}$ makes $A = 0$, because band bending is zero at flat-band. As we mentioned above, the flat-band voltage is experimentally extracted from capacitance-voltage (C-V) measurements by determining the gate voltage at which the device capacitance is equal to flat-band capacitance (C_{FB}) in Eq.(2.11).

2.2.3 C$-\psi_s$ method

In high-low method, it is assumed that the "high frequency" is so high that no interface traps are able to respond to the measurement ac probe frequency, therefore, only measuring the ideal capacitance C_s free of the contribution from interface traps.

However, in practice, usually the probe frequency used in high-low is limited to 0.1 $\sim$ 1 MHz. The maximum probe frequency turns out to be not high enough, especially in SiO_2/SiC case. For those traps that are fast enough to respond to the "high frequency", the measured capacitance by "high frequency" apparently contains their contribution ($C_{\mathrm{it}} \neq 0$). As a result, by subtracting the "high frequency" capacitance from low frequency capacitance, the high-low D_{it} fails to include those fast states and underestimates the density of traps.

To solve this problem, H. Yoshioka *et al.*[9;10] proposed to replace the high frequency capacitance with a theoretical capacitance $C_{\mathrm{D,theory}}$. The capacitance $C_{\mathrm{D,theory}}$ can be directly calculated from the MOS physics[11] where the ideal interface is assumed. Therefore, $C_{\mathrm{D,theory}}$ does not carry any interface states information ($C_{\mathrm{it}} = 0$). By comparing the *low frequency* capacitance and $C_{\mathrm{D,theory}}$, the information of all interface traps can be extracted. Note

that C-ψ_s technique can monitor the very fast interface states that are undetectable in the conventional methods.

$$C_{\mathrm{D,theory}}(\psi_s) = \frac{qN_D \left|\exp\left(\frac{\mathrm{q}\psi_\mathrm{s}}{\mathrm{kT}}\right) - 1\right|}{\sqrt{\frac{2kTN_D}{\epsilon_S}\left\{\exp\left(\frac{\mathrm{q}\psi_\mathrm{s}}{\mathrm{kT}}\right) - \frac{\mathrm{q}\psi_\mathrm{s}}{\mathrm{kT}} - 1\right\}}},$$

$$D_{\mathrm{it}}(C - \psi_s) = \frac{(C_\mathrm{D} + C_\mathrm{it})_{LF} - C_{\mathrm{D,theory}}}{q^2}.$$

A comparison between high-low method and C-ψ_s method is shown in Fig.2.12. It clearly indicates that the high-low method underestimate the interface trap density. The corresponding Matlab code for C-ψ_s method is attached in Appendix. A.

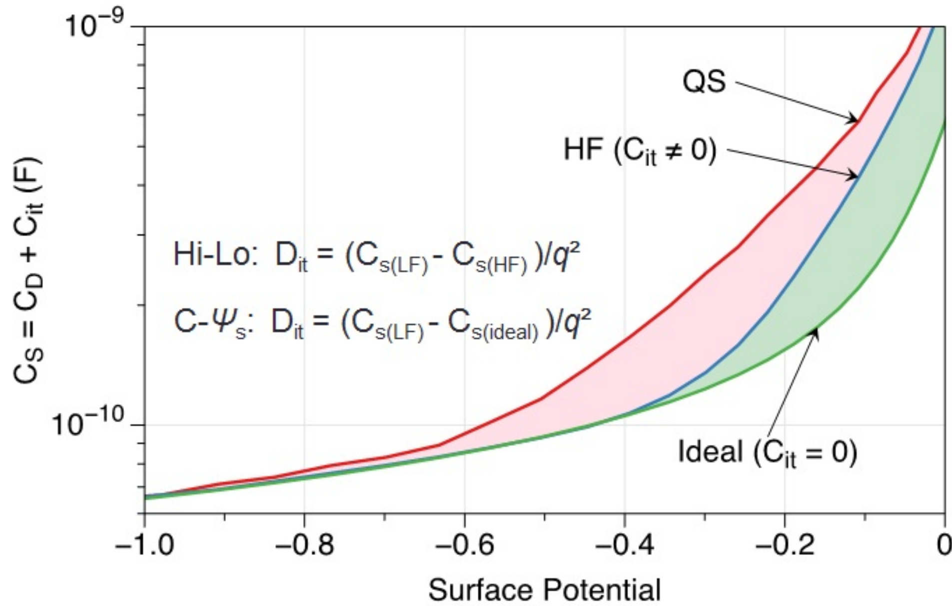


Figure 2.12: The illustration of the difference between high-low method and C-ψ_s method. Conventional high-low method underestimates the density of traps.

2.3 Summary

In this chapter, we discussed different working modes for MOS devices, and introduced the fundamental mobilities of MOSFETs. The presence of interface traps in SiC MOS devices

dramatically undermines the current transport in the channel. Among several interface trap density characterization methods, we introduced the simultaneous high-low frequency C-V method and C-ψ_s method, and discussed the difference between these two methods.

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Chapter 3

Phospho-silicate glass formation and P uptake variation

3.1 The structure of phospho-silicate glass

As mentioned in chapter 1, nitrogen incorporation into SiO_2/SiC interface does not change the chemical composition of the SiO_2 bulk. In contrast, phosphorus incorporation through diffusion method transforms the silicon dioxide into phospho-silicate glass (PSG).

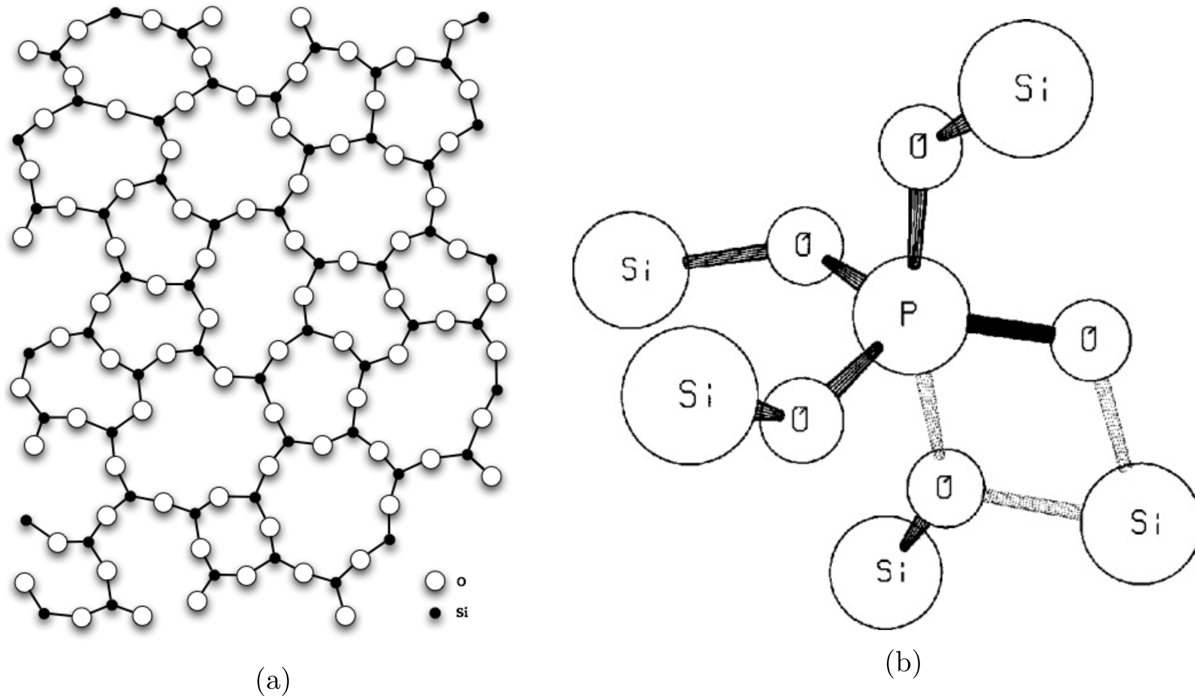


Figure 3.1: (a) Schematic diagram of SiO_2 structure. (b) Schematic three-dimensional structure of phospho-silicate glass. The proposed mechanism for the polarization process in the glass is indicated by the arrows[1].

PSG is a composite with chemical formula $(P_2O_5)_x(SiO_2)_{1-x}$, where x is the mole fraction of P_2O_5. The schematic diagram of SiO_2 is shown in Fig.3.1a; while, after alloying with P_2O_5, this structure is transformed to PSG, whose three-dimensional structure is shown in

Fig.3.1b three-dimensional. PSG material is internally polarizable, which means that polarization can be induced under external electrical field. In addition, it has successfully served the industry because of its mobile ion gettering effect[2;3], for it has the ability to capture the mobile Na^+ and K^+ ions and keep them from migrating.

Elemental phosphorus oxidizes in trivalent or pentavalent forms (P_2O_3 and P_2O_5). The pentavalent form is commonly encountered when excess oxygen is present. At low concentrations, oxidized phosphorus is incorporated substitutionally into the silicon dioxide lattice, which consists of tetrahedra of Si-O_4[4], with each oxygen bridging to a neighboring silicon. Thus the local stoichiometry of the phosphorus atoms in the lattice is PO_2 rather than $PO_{2.5}$. In other words, half of phosphorus atoms form P-O_4 tetrahedra that are connected to the oxygen sites. On the average, every other phosphorus site has an "extra" non-bridging oxygen atom associated with it. Thermally grown SiO_2 consists of Si-O_4 tetrahedra (with Si at the center) that are connected at the corners (the oxygen sites) to form a three-dimensional network of multi-membered rings comprised of Si and O ions. To form phospho-silicate glass by alloying SiO_2 with P_2O_5, the P-O_4 tetrahedra incorporates into the silicate network, as shown in the two-dimensional representation of this structure in Fig.3.2a.

The polarization of PSG has two origins. First, since a non-bridging oxygen ion should be associated with every other phosphorus ion, two oppositely charged phosphorus centers will form for each P_2O_5 molecule added to the glass. The arrows in Fig.3.2a indicate that this loosely bound oxygen ion can be transferred between neighboring P-O_4 tetrahedra under the influence of an applied field. This transfer would constitute a fast polarization process. Second, a slow polarization phenomenon is also expected caused by long range drifting of the same non-bridging oxygen ions.

The gettering effect of PSG originates from the presence of the "extra" non-bridging oxygen atoms as well. These atoms have a significant local negative charge, and thus represent favorable sites (similar to trapping sites) for a positive ion such as sodium drifting through the lattice. The mechanism of mobile ion gettering in PSG is depicted in Fig.3.2b.

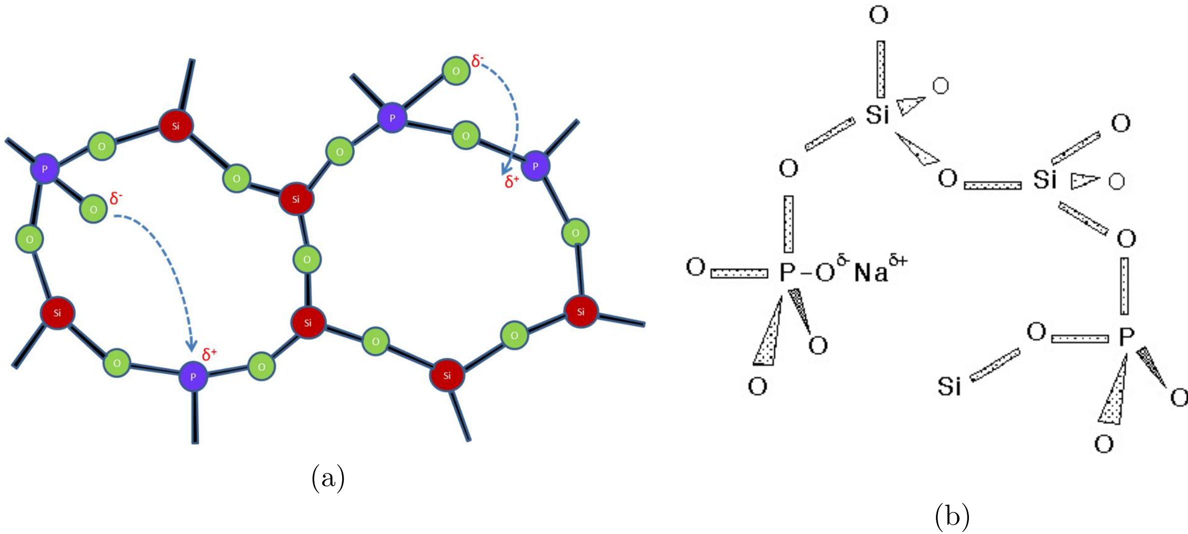


Figure 3.2: (a) Schematic diagram of phospho-silicate glass two-dimensional structure. The proposed mechanism for the polarization process in the glass is indicated by the arrows.[5] (b) Position of trapped sodium ion in phospho-silicate glass network. [6]

Note that the figure shows two adjacent P sites with and without an additional O atom for clarity here, but in fact the occupied and unoccupied sites are distributed randomly through the lattice.

3.2 PSG formation methods

Since PSG is generally prepared by doping thermally grown SiO_2 with gaseous P_2O_5, a detailed understanding of the kinetics of glass formation and the conditions which govern its phosphorus concentration is needed.

For doping P_2O_5 into silicon dioxide, usually diffusion is a common way which requires a region of high phosphorus concentration to act as a diffusion source. According to the phospho-silicate glass phase diagram, the addition of phosphorus to silicon dioxide causes large reductions in the glass transition temperature and melting temperature. The higher phosphorus concentration in a region, the lower is the melting temperature. If the diffusion temperature is over the melting temperature for the high-concentration region, it will liquify. Subsequently, the neighboring undoped oxide will dissolve the phosphorus rapidly to dilute the liquid region. As the dilution of the liquid region reduces the concentration of phosphorus,

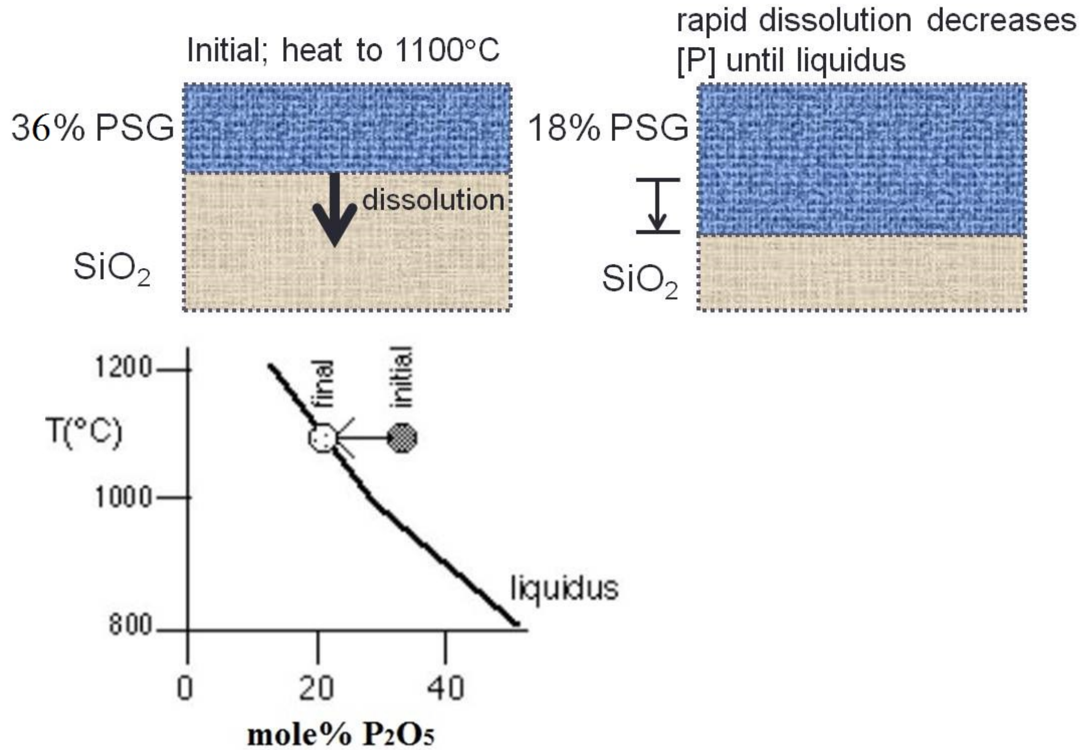


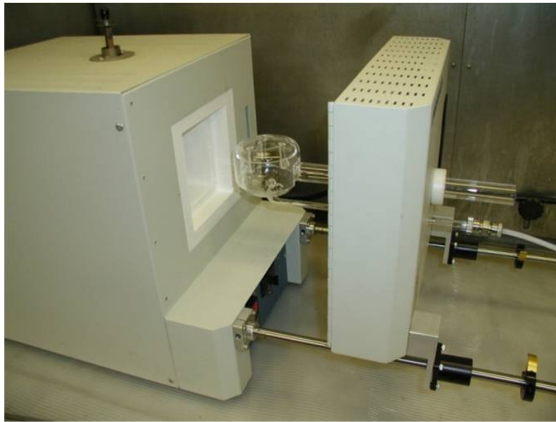
Figure 3.3: The kinetics of dissolution in the liquid/solid mixture of PSG/oxide, accompanied by the transport of P_2O_5. The mole fraction of P_2O_5 in PSG is capped by the liquidus line. [7]

the melting temperature increases and the molten region begins to solidify. This dissolution proceeds much more rapidly than solid-phase diffusion of phosphorus through thick oxides, and thus is the primary means of phosphorus transport and PSG formation. This process occurs very rapidly, and the steps described above can repeat multiple times from the high concentration region to the low concentration region, leading to a uniform phosphorus concentration in the PSG layer. The dissolution process is depicted schematically in Fig.3.3, which shows the formation of thick PSG layer (18% P_2O_5) from the original PSG source (36% P_2O_5), while the thickness doubles, the phosphorus concentration becomes half. The figure also shows part of the liquidus line of PSG material, with the arrow indicating the mechanism at 1100 °C.

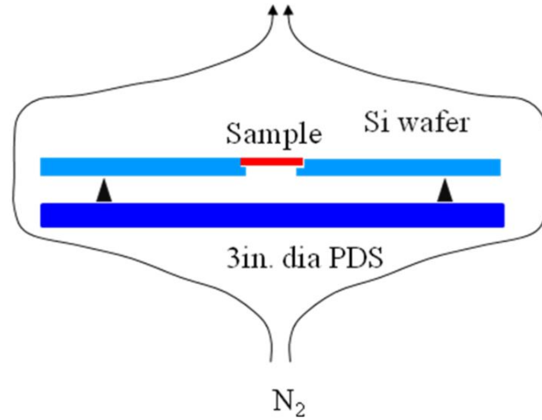
In the work, we used two methods to form PSG dielectric: P_2O_5 from planar diffusion source (PDS) and pyrolysis of phosphoryl chloride ($POCl_3$)-O_2 mixtures[8–11].

3.2.1 Planar diffusion source (PDS)

A silicon pyrophosphate-containing (SiP_2O_7) solid planar diffusion source (PDS) has been evaluated for phosphorus doping of silicon in modern manufacturing technology [12–14]. PDS products allow semiconductor fabricators to replace hazardous chemical dopants such as phosphoryl chloride ($POCl_3$), phosphine(PH_3), therefore they are preferred for use in applications requiring a high concentration of dopant, to dope large diameter silicon, particularly 150 mm diameter, and in high volume production. Usually, PDS products are made in the form of thin wafers or disks, perhaps 2, 3 and up to 6 inches in diameter.



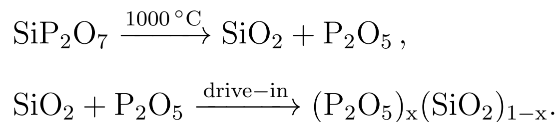
(a)



(b)

Figure 3.4: (a) The picture of the diffusion annealing furnace. (b) Schematic of the layout of the PDS furnace chamber.

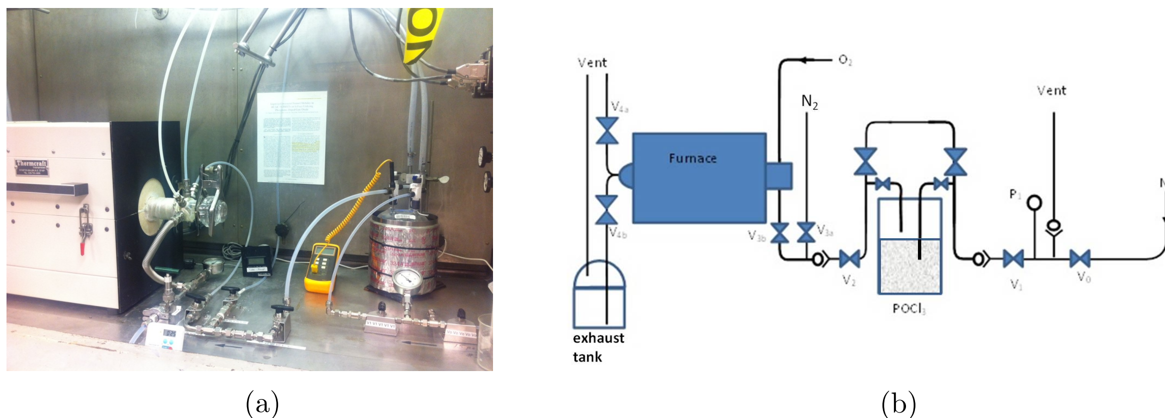
Fig.3.4a shows the picture of the diffusion annealing furnace in our lab. In the annealing furnace chamber, the PDS source is sitting on a support structure below the sample with ∼1cm spacing, as shown in Fig.3.4b. During the annealing, the furnace is heated to 1000 °C. Under this condition, the reaction leads to the formation of phosphorus pentoxide. Meanwhile, nitrogen gas is flowing at 500 sccm to assist the gaseous P_2O_5 diffusion into the sample.



$$\mathrm{SiP_2O_7} \xrightarrow{1000\,^{\circ}\mathrm{C}} \mathrm{SiO_2} + \mathrm{P_2O_5}\,,$$
$$\mathrm{SiO_2} + \mathrm{P_2O_5} \xrightarrow{\mathrm{drive-in}} (\mathrm{P_2O_5})_{\mathrm{x}}(\mathrm{SiO_2})_{1-\mathrm{x}}.$$

3.2.2 Phosphoryl chloride ($POCl_3$)

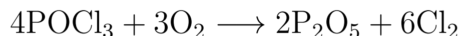
Phosphoryl chloride ($POCl_3$) is a colorless hazardous liquid with a pungent odor. It is kept in a glass bubbler tank with extreme care since it is very toxic by inhalation and corrosive to metals and tissue. Fig.3.5a is the picture of the annealing furnace and $POCl_3$ tank, while Fig.3.5b shows the schematic of the whole system with the gas pipes and the exhaust tank.



(a) (b)

Figure 3.5: (a) The picture of the $POCl_3$ annealing furnace. (b) Schematic of the $POCl_3$ annealing system.

With $POCl_3$ as the phosphorus source, when the furnace is heated to desired temperature, we flow nitrogen gas (flow rate at 100 sccm) through the $POCl_3$ liquid in the bubbler tank to carry out $POCl_3$ vapor. And meanwhile, oxygen gas flows (flow rate at 133 sccm) into the furnace chamber. The gas mixture can have the following reaction at high temperature to generate phosphorus pentoxide:



$$4POCl_3 + 3O_2 \longrightarrow 2P_2O_5 + 6Cl_2$$

The bubbler containing $POCl_3$ is maintained at 15 °C. When the furnace is ramped up to the pre-set temperature, pure N_2 is flowing through the bubbler to carry $POCl_3$ vapor into the furnace tube, while a mixture of pure O_2 and additional N_2 is flowing directly into the tube. The ratio of flow rates between carrier N_2, pure O_2 and additional N_2 is 3:4:9. We

limit the flow of $POCl_3$ and O_2 mixture to 15 minutes during the annealing. Subsequently, while maintaining the same furnace temperature, we stop the flow of the carrier N_2 and pure O_2, leaving only the additional nitrogen gas flow to rid of the remaining $POCl_3$ vapor and chlorine or any other dangerous chemicals for 30 minutes. This part is called additional N_2 drive-in annealing. Afterwards, we ramp the furnace temperature down to 750 °C, and get the sample out of furnace. For consideration of safety, the additional nitrogen gas (flow rate at 300 sccm) is on throughout the whole annealing process.

3.2.3 Comparison of two annealing methods

Due to the poor reproducibility of the results from PDS annealing, we sent a piece of PDS-annealed PSG sample for Inductively coupled plasma mass spectrometry (ICP-MS) analysis, and found out that it contains a lot of contaminations, among which the concentrations of aluminum (Al), boron (B), iron (Fe), magnesium (Mg), nickel (Ni), zinc (Zn) are over $2\times10^{12}\text{cm}^{-2}$. In the list, we also see a high concentration of sodium (Na) contamination, as shown in Fig.3.6.

These contaminations affect the device performance severely, especially the stability under electrical stress. They cause a higher leakage current and early breakdown. Fig.3.7a shows the breakdown test at room temperature for a circular capacitor device (radius $\sim$ $300\mu m$) which is annealed with PDS source. If we consider 1×10^{-6}A as the breakdown current, the breakdown field is $\sim$ 6.5 MV/cm.

Phosphoryl chloride ($POCl_3$) liquid is a relatively cleaner phosphorus source, which results in a higher breakdown field $\sim$ 9MV/cm, as shown in Fig.3.7b. At low field, the leakage current is smaller than PDS case, e.g., below 6MV/cm, the current is lower than 1×10^{-10}A.

From the BTS (bias-temperature stress) shift, we can also see the difference of two PSGs. The presence of mobile ions causes a negative shift of flat-band voltage in CV curve, as shown in Fig.3.7c.

Impurity	Atoms/cm2
Aluminum (Al)	2.20E+13
Barium (Ba)	1.30E+10
Boron (B)	8.60E+12
Cerium (Ce)	9.20E+10
Cobalt (Co)	4.40E+10
Copper (Cu)	1.40E+12
Gold (Au)	2.50E+11
Iron (Fe)	2.90E+13
Lead (Pb)	2.50E+10
Magnesium (Mg)	6.00E+12
Manganese (Mn)	3.30E+11
Molybdenum (Mo)	8.10E+10
Neodymium (Nd)	2.00E+11
Nickel (Ni)	3.20E+12
Niobium (Nb)	3.70E+11
Silver (Ag)	2.40E+10
Sodium (Na)	9.40E+11
Strontium (Sr)	9.80E+09
Tantalum (Ta)	9.50E+09
Titanium (Ti)	1.50E+12
Tungsten (W)	3.70E+10
Vanadium (V)	3.40E+10
Zinc (Zn)	2.50E+12
Zirconium (Zr)	8.50E+10

Figure 3.6: The results of chemical element analysis for PDS source. It contains many contaminations, including aluminum (Al), boron (B), iron (Fe), magnesium (Mg), nickel (Ni), zinc (Zn), sodium (Na), etc.

3.3 Phosphorus uptake variation

PSG annealing with $POCl_3$ results in reproducible and more reliable devices, therefore we chose this as the main annealing method in our research. The detailed annealing process has been discussed above.

For MOS capacitors, ~60nm-thick oxides were formed by dry oxidation at 1150 °C on n-type 4H-SiC (0001) epitaxial layers. Two kinds of SiC epi-layers were used, doped with N to concentrations of 5×10^{15}cm^{-3} and 1×10^{16}cm^{-3}, respectively. After oxidation, the samples were annealed at 900 °C, 950 °C, 1000 °C, 1050 °C and 1100 °C in $POCl_3$ annealing

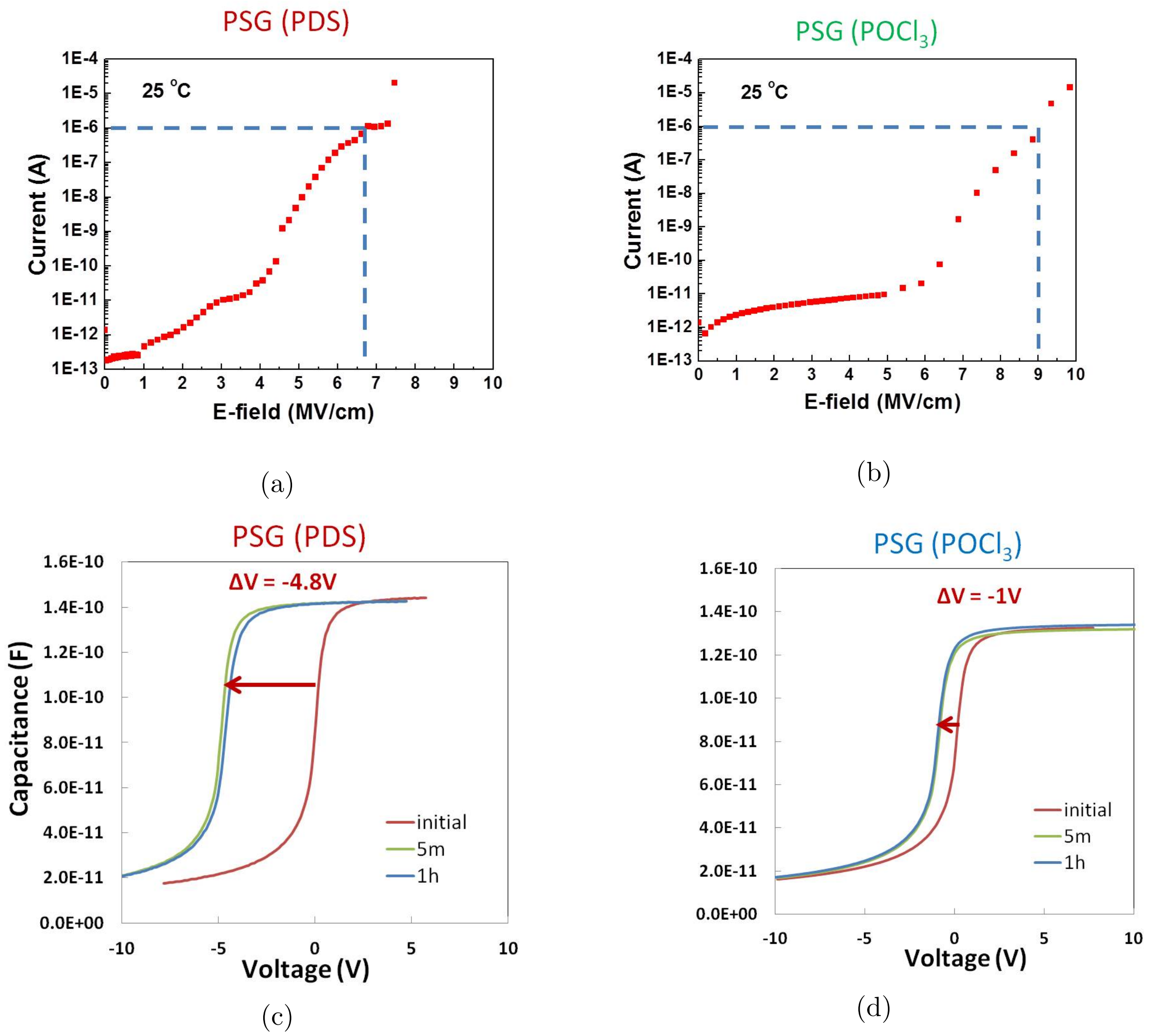


Figure 3.7: The breakdown test at room temperature on (a) a PDS-annealed capacitor device; (b) a $POCl_3$-annealed capacitor device. And the bias-temperature stressing test on (c) a PDS-annealed capacitor device, showing -4.8V shift; (d) a $POCl_3$-annealed capacitor device, , showing -1V shift.

and additional N_2 drive-in annealing. After the PSG formation, molybdenum (Mo) was deposited by DC sputtering, and a photolithography/lift-off process was used to define the gate electrode, while broad area nickel (Ni) contact was used as the backside electrode. The schematic of a MOS capacitor device with PSG dielectric is shown in Fig.3.8a.

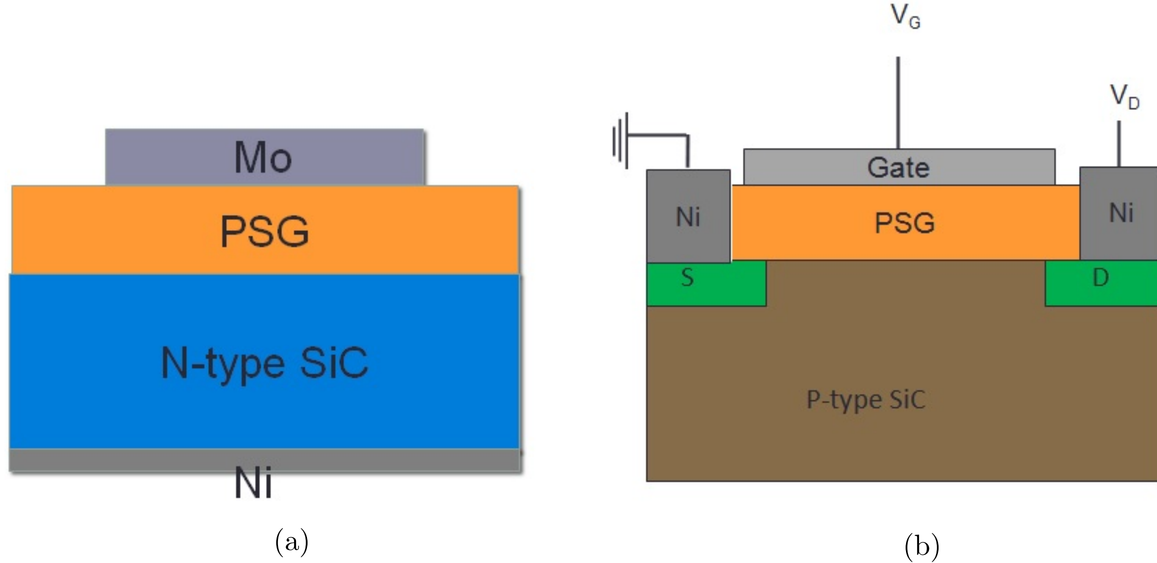


Figure 3.8: Schematic of (a) a MOS capacitor device , (b) a MOSFET device with PSG dielectric.

Accordingly, the lateral n-channel MOSFETs were fabricated on p-type epitaxial layers on n-type 4H-SiC substrates (4°-off; Si face). The net acceptor concentration of the p-type epi-layer was 1×10^{16}cm^{-3}. The gate oxide was formed by dry oxidation at 1150 °C, followed by $POCl_3$ annealing at 900 °C, 1000 °C, 1050 °C and 1100 °C using the same conditions described above for the fabrication of MOS capacitors. Mo and Ni were used as the gate and the source/drain electrodes, respectively. The channel length (L) and width (W) of the FETs were 150 and 290 μm, respectively.

After the CV measurements on MOS capacitors, the gate metal was removed and the PSG layer was partially etched by buffered oxide etch (BOE). X-ray photoelectron spectroscopy (XPS) was then performed to analyze the chemical composition, from which the average atomic percentage in the bulk of PSG was quantified. Next, the PSG layer was completely etched. As we discussed in chapter 1, the remnant unetchable P atoms at the

interface are primarily bonded to O atoms[15]. The interface P areal concentration were also quantified using XPS. All the XPS analyses were performed by Prof. L. C. Feldman's group at Rutgers University.

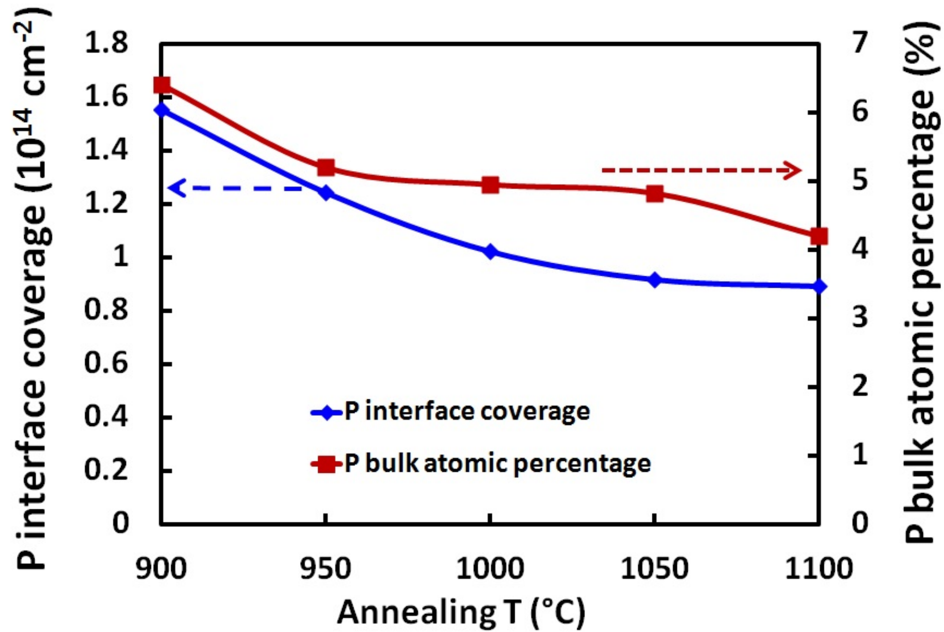


Figure 3.9: Phosphorus coverage at the interface of SiC (left-axis) and the atomic percentage of P in PSG bulk (right-axis) as a function of $POCl_3$ annealing temperature [performed at Rutgers University].

The results of phosphorus uptake in the PSG bulk and at the interface are shown in Fig.3.9. It indicates that the P incorporation, both at the PSG/SiC interface and in the bulk of PSG, is reduced with increasing the annealing temperature in the range 900-1100 °C. The interface P concentration is varied from 0.89 to 1.55×10^{14}cm^{-2} in these experiments. As is known in SiC, the monolayer atomic density is 1.25×10^{15}cm^{-2}. Thus, converting the interface P concentration into the monolayer coverage, we obtain a monolayer coverage variation from 7.1% to 12.4%. In the bulk, the phosphorus atomic percentage is varied from 4.2% to 6.7%. After converting into the P_2O_5 mole fraction in the formula $(P_2O_5)_x(SiO_2)_{1-x}$, x values vary from 0.069 to 0.115, as listed in Table.3.1.

The tendency of phosphorus uptake, lower P with higher annealing temperature, can be explained by the P_2O_5-SiO_2 phase diagram, which is shown in Fig.3.10. The liquidus

Table 3.1: The phosphorus atomic percentage in the PSG bulk and corresponding P_2O_5 mole fraction x.

$POCl_3$ annealing temp	Bulk P percent (%)	P_2O_5 mole fraction x
900 °C	6.7	0.115
950 °C	5.2	0.087
1000 °C	4.6	0.076
1050 °C	4.6	0.076
1100 °C	4.2	0.069

curve (curve ①) represents the maximum solubility of P_2O_5 in the composition of PSG. The maximum solubility decreases as the temperature increases. Note that in 900-1100 °C region, the tendency of our data is consistent with the phase diagram, marked by the red part. However, the mole fraction values obtained in our experiment (marked by the blue star-like dots) are about half of the maximum solubility. This is most likely due to the additional N_2 post annealing right after the $POCl_3$ annealing, where some P_2O_5 is lost to the gas phase by evaporation.

We investigated the role of the additional N_2 drive-in annealing by comparing two samples, with and without N_2 drive-in annealing, the other with. P depth profile was analyzed by XPS depth profiling technique using argon ion sputtering. Fig.3.11 indicates that the additional N_2 post annealing helps homogenize the phosphorus distribution in PSG dielectric, while losing part of P_2O_5 into the gas phase. In the figure, the horizontal axis is the etch level, and the etched thickness of PSG between every two etches is very close.

The PSG dielectric thickness is obtained from the CV measurement and calculated by the following equation

$$C_{ox} = \frac{\epsilon_{\mathrm{PSG}}}{t_{ox}} \tag{3.1}$$

where C_{ox} is the oxide capacitance per unit area, assuming the dielectric constant of PSG ϵ_{PSG} is 3.9 [9;16], the same as the dielectric constant for SiO_2.

An increase of the dielectric thickness after $POCl_3$ annealing is observed, which hints an additional oxidation. R. Chen *et al.*[17] investigated the PSG growth on silicon (Si) via

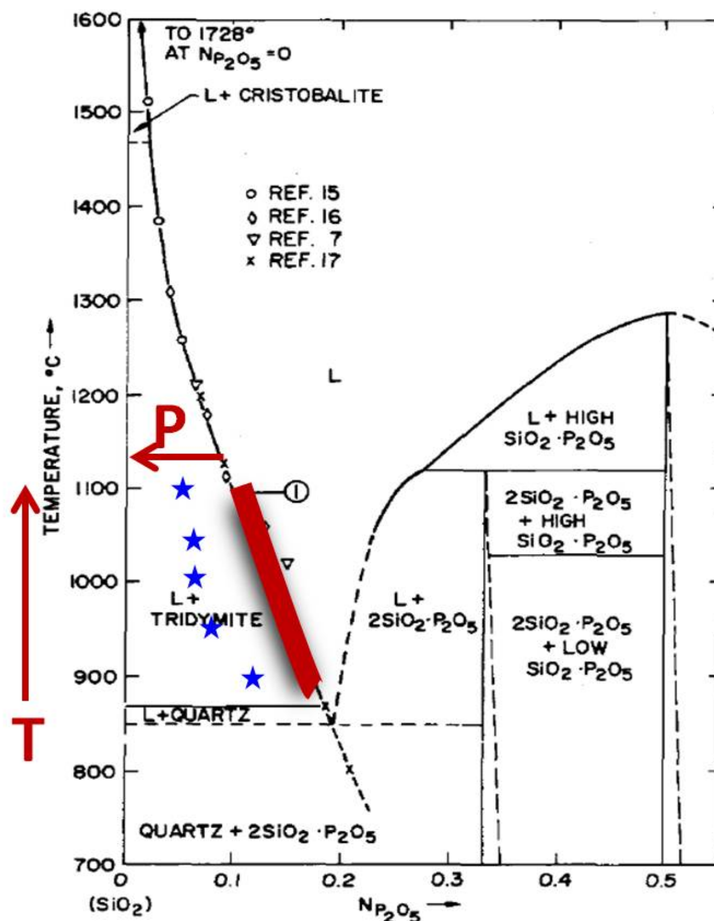


Figure 3.10: Correspondence of PSG composition with the maximum solubility of crystalline SiO_2 in phosphosilicate liquid (curve 1), shown on SiO_2-P_2O_5 phase diagram[5].

$POCl_3$ annealing and suggested that PSG formation during $POCl_3$ annealing is the result of P diffusion into SiO_2 from high concentration regions in conjunction with the inward oxidation (due to high temperature and the presence of oxygen gas). In the case of Si, a pile-up of P occurs at the interface, while substantial amount of P atoms diffuse into Si across the growing interface. In the case of SiC, the PSG formation mechanism is likely to be similar albeit kinetically slower for SiC due to the low oxide growth rate, which can explain the increase of the dielectric thickness. Only a small amount of P atoms are expected to enter into SiC because of the small P diffusivity or diffusion coefficient into SiC[18–20]. Those P atoms could be the activated as n-type dopants, which is likely the origin of counter-doping effect in n-channel MOSFETs.

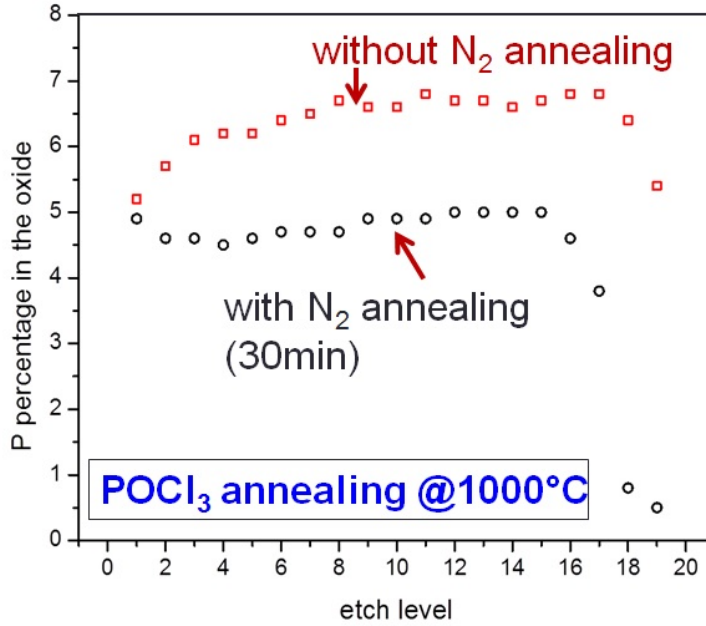


Figure 3.11: XPS depth profiles for phosphorus in the PSG dielectrics w/ and w/o the additional N_2 post annealing.

The PSG formation model for SiC is schematically depicted in Fig.3.12. In this model, two parallel processes, one for phosphorus and the other for oxygen, are assumed with a steady-state flux. Arrows denote the net flows of P (orange) and O (blue). J_D, J_S, and J_R denote fluxes of diffusion, segregation, and reaction, respectively. Also shown in the schematic are critical interface concentrations, in which atom species (P and O) are denoted by subscripts, and the associated regions are denoted by superscripts (G stands for PSG and X stands for oxide). The oxygen flux diffuses through the PSG layer J_D and splits into two portions, the reaction flux J_R (the reaction between $POCl_3$ and O_2), and the segregation flux J_S (this flux passes into the oxide layer, and terminates at SiC interface due to the inward oxidation reaction with SiC). The diffusion process of phosphorus is similar as oxygen, expect that some phosphorus atoms can enter SiC bulk due to small phosphorus diffusivity in SiC[18]. This PSG formation model is slightly different from the fixed source diffusion mechanism introduced in Section.3.2, because the ambient gaseous P_2O_5 in the furnace tube can supply

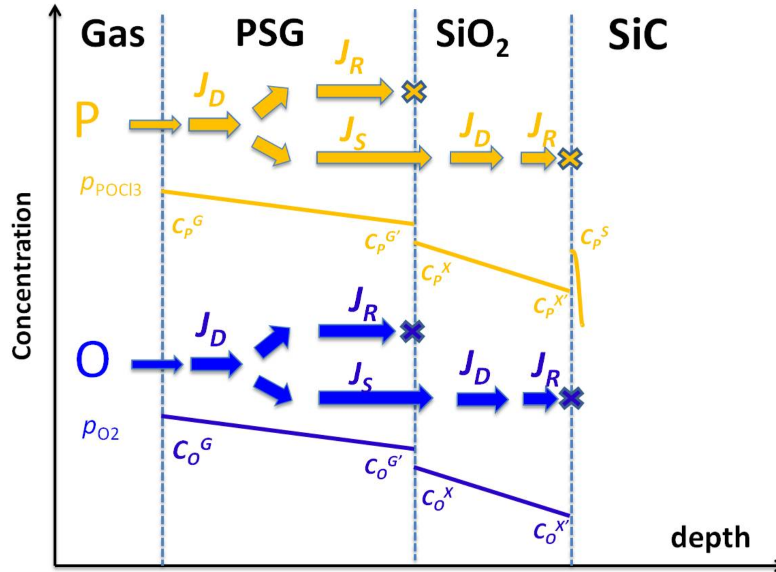


Figure 3.12: PSG formation model schematic with critical concentrations at interfaces. Subscripts denote atom species, and superscripts denote the associated regions(G stands for PSG and X stands for oxide). Arrows denote the net flows of P (orange) and O (blue). J_D, J_S, and J_R denote fluxes of diffusion, segregation, and reaction, respectively.

as an unlimited diffusion source for the small sample. The samples annealed with sufficient P_2O_5 source and post N_2 treatment are more likely to reach uniform P profiles in the PSG bulk.

3.4 Summary

Phospho-silicate glass (PSG) material is formed by alloying P_2O_5 and silicon dioxide. Compared to nitrogen incorporation, using PSG as gate dielectric in 4H-SiC MOS can reduce more interface traps. However, the drawback to this dielectric is its intrinsic polarization. In the lab, there are two ways to form PSG dielectric, planar diffusion source (PDS) diffusion and $POCl_3$ annealing. $POCl_3$ annealing results in a better dielectric quality and less contamination, hence it is chosen for this research. Based on the P_2O_5-SiO_2 phase diagram, we obtain P uptake variations in the PSG dielectrics by changing the annealing temperature.

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Chapter 4

Electrical properties of PSG-gated MOS devices

4.1 NO and PSG

For post-oxidation annealing in NO, it has been reported that the N concentration at the interface varies with NO annealing time and temperature [1;2]. The interface state density, is reduced with increasing N interfacial coverage, and this effect almost saturates at a concentration $5 \sim 6{\times}10^{14}$cm^{-2} of interfacial N atoms [3]. This nitrogen coverage saturation is limited by the competing nitridation and oxidation reactions in NO passivation, which leads to the maximum reduction of interface state density to $4.5 \sim 5{\times}10^{11}$cm^{-2}eV^{-1} at E_C - 0.2eV level (detected by hi-lo method at room temperature) and the highest mobility $\sim$ 35 cm^{2}V^{-1}s^{-1}.

At room temperature, E_C - 0.2eV is very close to the position of flat-band level ($\approx E_g/2 - k_B T \ln\left(\frac{\mathrm{N_D}}{\mathrm{n_i}}\right)$). As discussed in the interface trap characterization, capacitance-voltage techniques are valid in the depletion region, hence 0.2eV is the up limit of the detection range at RT. To get closer to the conduction band edge, lower temperature is needed.

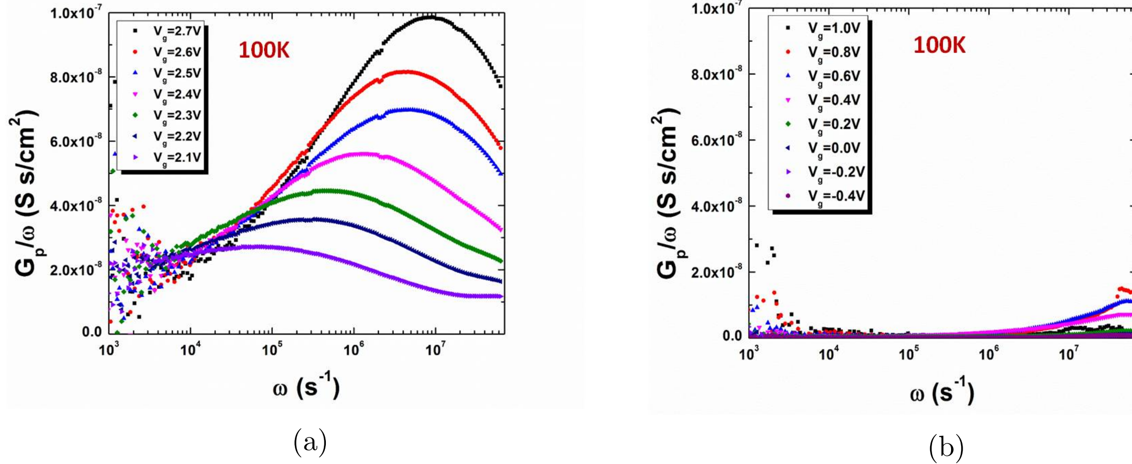
Comparatively, PSG post-oxidation annealing reduces the interface trap density more efficiently. According to previous reports, even the phosphorus interface coverage (the highest value in our experiment is $1.55{\times}10^{14}$cm^{-2}) is 25% of nitrogen coverage, the interface state density is much lower, and the channel mobility in PSG is $\sim$ 3 times of that in NO-treated device.

Before the further investigation in PSG-gated devices, it is necessary to gain some insight by looking into the difference of the electrical properties with NO-treated and PSG gate dielectric. Here, we first compare NO devices with PSG (annealed in PDS or $POCl_3$ at 1000 °C) with several techniques.

Fig.4.1 shows the low temperature (100K) conductance measurements, which were taken at Arizona State University. An approximate expression giving the interface trap density in terms of the measured maximum conductance is

$$D_{it} \approx \frac{2.5}{q}\left(\frac{G_P}{\omega}\right)_{max} \tag{4.1}$$

The density of interface states is proportional to the peak value. Contrary to the PSG passivated sample, high G_p/ω peaks were observed for NO sample at frequencies in 10^6 - 10^7 Hz range. For the PSG sample, small G_p/ω peaks were detected above 10^7 Hz. These results imply that close to the conduction band edge, both NO and PSG samples have interface states with high frequencies, and overall the density of interface traps in NO is higher than that in PSG sample.



(a) (b)

Figure 4.1: The conductance $G_p\ /\omega$ versus ω at 100 K measured on (a) NO annealed sample and (b) PSG sample (PDS annealed at 1000 °C).

From another perspective, Gray-Brown technique[4] provides a qualitative way to compare the interface traps. Lower temperature causes the Fermi energy level to move closer to the conduction band, if $T_1 > T_2$, then $E_F(T_1) < E_F(T_2)$, where $E_F(T)$ is the Fermi energy level at temperature T. As a result, the interface traps below the Fermi energy level will be occupied. In the upper half of the band gap, the trap levels are electrically neutral when

empty and negatively charged when occupied by an electron. Therefore, it brings additional negative charge to the effective charge Q_{eff} at low temperature, which causes a right shift in the CV curve, and the amount of shift can be written as

$$V_G(T_2) - V_G(T_1) = \frac{q \int_{E_F(T_1)}^{E_F(T_2)} D_{it}(E)dE}{C_{ox}} = \frac{qN_{it}^*}{C_{ox}} \tag{4.2}$$

Here $V_G(T_1)$ and $V_G(T_2)$ are the gate bias to maintain the same band-bending at different temperatures. N_{it}^* is the total number of interface traps in the range from $E_F(T_1)$ to $E_F(T_2)$.

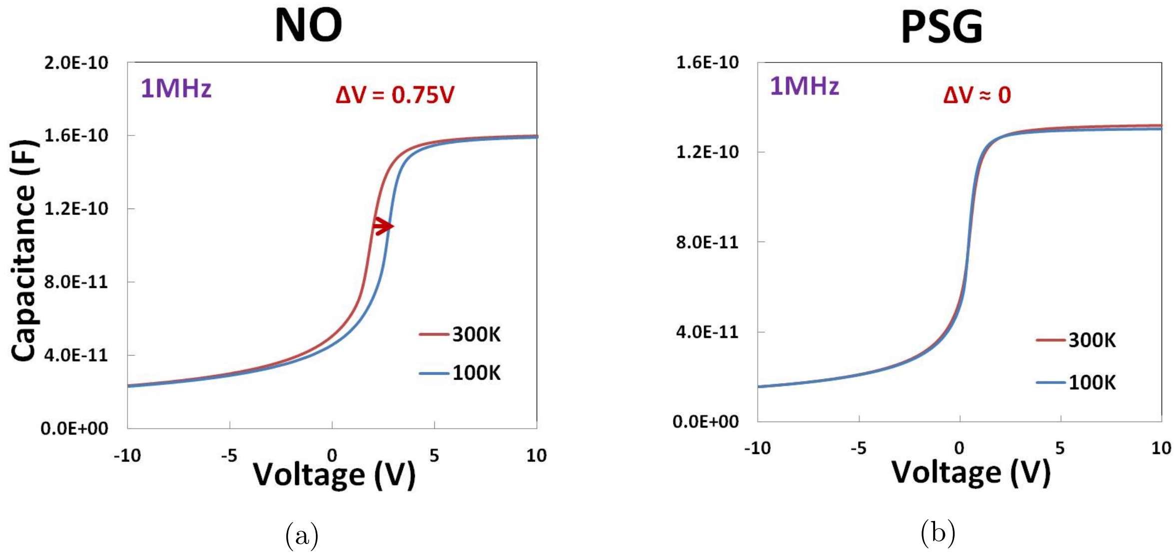


Figure 4.2: Gray-Brown technique: the capacitance-voltage curves measured at 100K and 300K on (a) NO sample and (b) PSG sample (PDS annealed at 1000 °C).

In Gray-Brown method, the simple band-bending case is flat-band. The freeze-out of traps at low temperature causes right shift of the flat-band voltage (ΔV_{FB}) compared to room temperature, and the amount of ΔV_{FB} indicates the amount of interface traps located within the two Fermi levels at T_1 and T_2. Fig.4.2 shows the CV curves at 100K and 300K for NO and PSG case respectively. The CV curves were taken with 1MHz high frequency. NO-treated 4H-SiC MOS capacitor has a ΔV_{FB} of 0.75V, while the PSG exhibits nearly zero shift. This is another implication of higher N_{it} in NO than PSG sample.

Deep-level-transient spectroscopy (DLTS) is a commonly employed method to characterize defects in semiconductors because of its higher signal-to-noise ratio and greater energy resolution compared to other measurement techniques. With a constant-capacitance feedback loop, this method, known as CCDLTS, is used to measure the energy distribution and capture cross sections of interface states in 4H-SiC/SiO_2 capacitors. With this technique, two types of near-interface oxide traps, O1 and O2, are observed in 4H-SiC/SiO_2 as-oxidized and NO-treated capacitors [5;6]. Fig.4.3a shows the CCDLTS spectrum of a NO sample (annealed at 1175 °C for 30 minutes). Two broad peaks are displayed at peak temperatures of approximately 100 K and 200 K, respectively, which are energetically aligned at 0.15 eV and 0.39 eV below E_C of 4H-SiC.

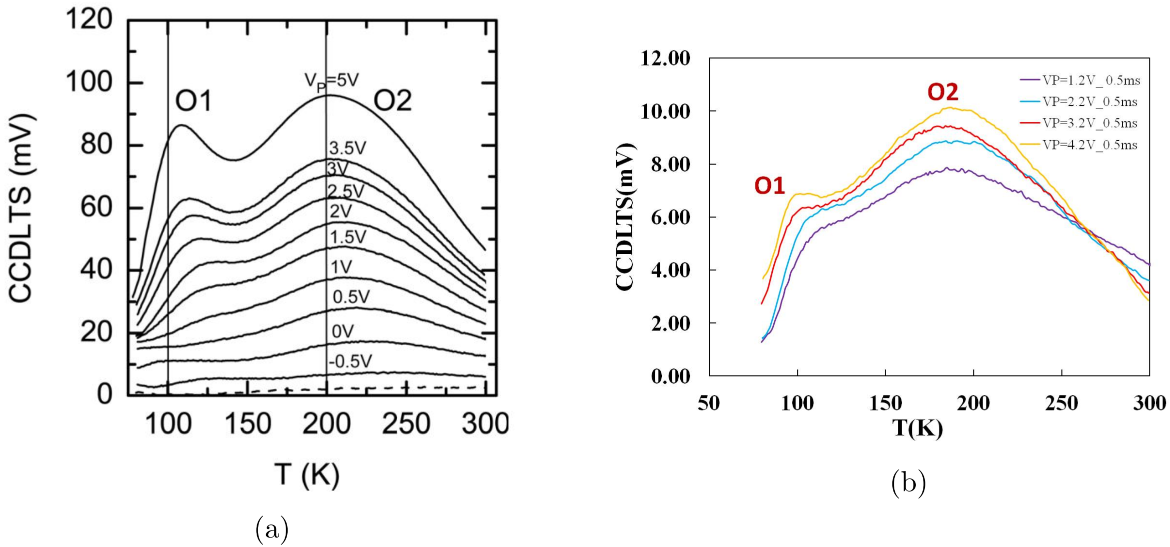


Figure 4.3: Energy-resolved CCDLTS spectra for (a) NO sample (1175 °C annealed for 30 min) (b) PSG sample (1000 °C annealed with $POCl_3$) taken at the filling voltages indicated.

Recently, we employed CCDLTS to investigate the PSG-gated 4H-SiC MOS capacitor. The CCDLTS spectrum in Fig.4.3b suggests the existence of O1 and O2 type traps in PSG as well. However, at similar filling voltages, the CCDLTS signals of O1, O2 traps in PSG are about 1 order lower than that in Fig.4.3a for NO. The extracted trap densities are summarized in Table.4.1, which shows that PSG annealing plays a remarkable role in reducing the interface trap density.

Table 4.1: The extracted data of near-interface oxide trap (O1 and O2) densities,and their sum, N_{IT}(CCDLTS) in 4H-SiC as-oxidized, NO and PSG samples.

sample	O1 trap(CCDLTS) $\times 10^{11}cm^{-2}$	O2 trap(CCDLTS) $\times 10^{11}cm^{-2}$	N_{IT}(CCDLTS) $10^{11}cm^{-2}$
As-oxidized	26	45	71
NO (1000 °C, 30min)	4.8	7.8	13.6
NO (1000 °C, 120min)	3.0	3.5	6.5
PSG (1000 °C)	0.20	0.44	0.64

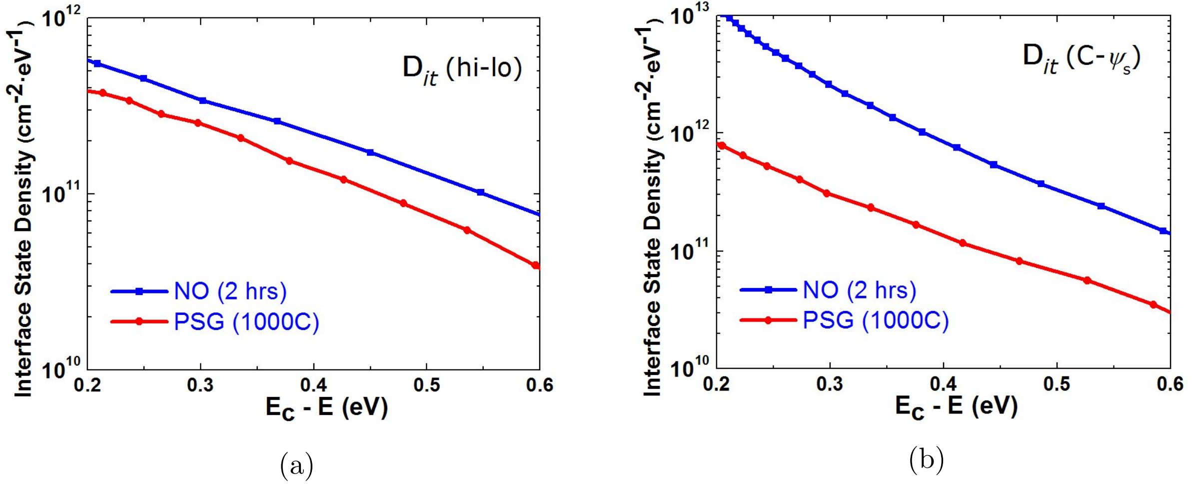


Figure 4.4: The comparison of interface trap density between NO sample (1175 °C annealed for 30 min) sample and PSG sample (1000 °C annealed with $POCl_3$) sample through (a) hi-lo method (b) C-ψ_s method. Both of the measurements are taken at room temperature.

Finally, with the aid of hi-lo method and C-ψ_s method, we can directly compare the interface trap density through capacitance-voltage measurements, as shown in Fig.4.4. The high frequency used in Fig.4.4a is 100kHz. Consistent with the discussions above, the interface trap density of NO annealing (blue curve), quantitatively, detected by hi-lo method, is overall higher than that of PSG annealing (red curve). Because of the limitation of applied high frequency, some fast states with responding frequencies higher than 100kHz are underestimated by hi-lo method. Fig.4.4b shows the comparison of interface trap densities detected by C-ψ_s method, which takes account of those "fast states". As reported by H. Yoshioka *et al.*[7], the generation of very fast states by nitridation is observed in our measurement. At E_C - 0.2eV level, the total interface trap density is about 16 times of hi-lo

D_{it}, while for PSG annealing, the ratio is about twice. The subtraction of these two sets of data is considered as the "fast states" density. Hence, we can conclude that PSG annealing also generates some amount of "fast states". For 1000 °C annealing case, the generation is not as prominent as nitridation. Moreover, the generation of "fast states" in terms of the phosphorus uptake variation will be discussed below.

4.2 4H-SiC and 6H-SiC comparison

4.2.1 Intrinsic carrier density and energy band

As seen in chapter 1 (Fig.1.3), both 4H- and 6H-SiC belong to hexagonal polytype, but with different number of Si-C bilayers. The stacking sequence of 4H-SiC is ABCB, while 4H-SiC has stacking sequence ABCACB. Hence, distinct physical properties arise from the difference in crystal structure of each polytype (seen some basic physical parameters in Table.1.1). Here we first compare some physical parameters for these two semiconductors.

The bandgaps of 4H-SiC and 6H-SiC at room temperature are $E_g^{T_0} = 3.265$eV for 4H-SiC, 3.023eV for 6H-SiC. Their temperature dependence can be modeled by

$$E_g(T) = E_g^{T_0} - \alpha^{E_g} \cdot \frac{T^2}{\beta^{E_g} + T} \tag{4.3}$$

where the parameters $\alpha^{E_g} = 0.033eV/K$, $\beta^{E_g} = 1.0 \times 10^5 K$.

The wide band gap results in a very low intrinsic electron concentration:

$$n_i = \sqrt{N_c \cdot N_v} \cdot \exp\left(- \frac{\mathrm{E_g}}{\mathrm{2k_B T}} \right) \tag{4.4}$$

The quantities N_c and N_v, called the effective densities of states at the conduction- and valence-band edges, respectively, are given by the expressions

$$N_c = 2\left(\frac{2\pi m_n^* k_B T}{h^2} \right)^{3/2} \tag{4.5}$$

and

$$N_v = 2\left(\frac{2\pi m_p^* k_B T}{h^2}\right)^{3/2} \tag{4.6}$$

where m_n^* and m_p^* denote the effective masses of electrons and holes. For 4H-SiC, $m_n^* = 0.39m_0$, $m_p^* = 0.82m_0$; for 6H-SiC, $m_n^* = 0.71m_0$, $m_p^* = 0.90m_0$[8], where m_0 is the free electron mass.

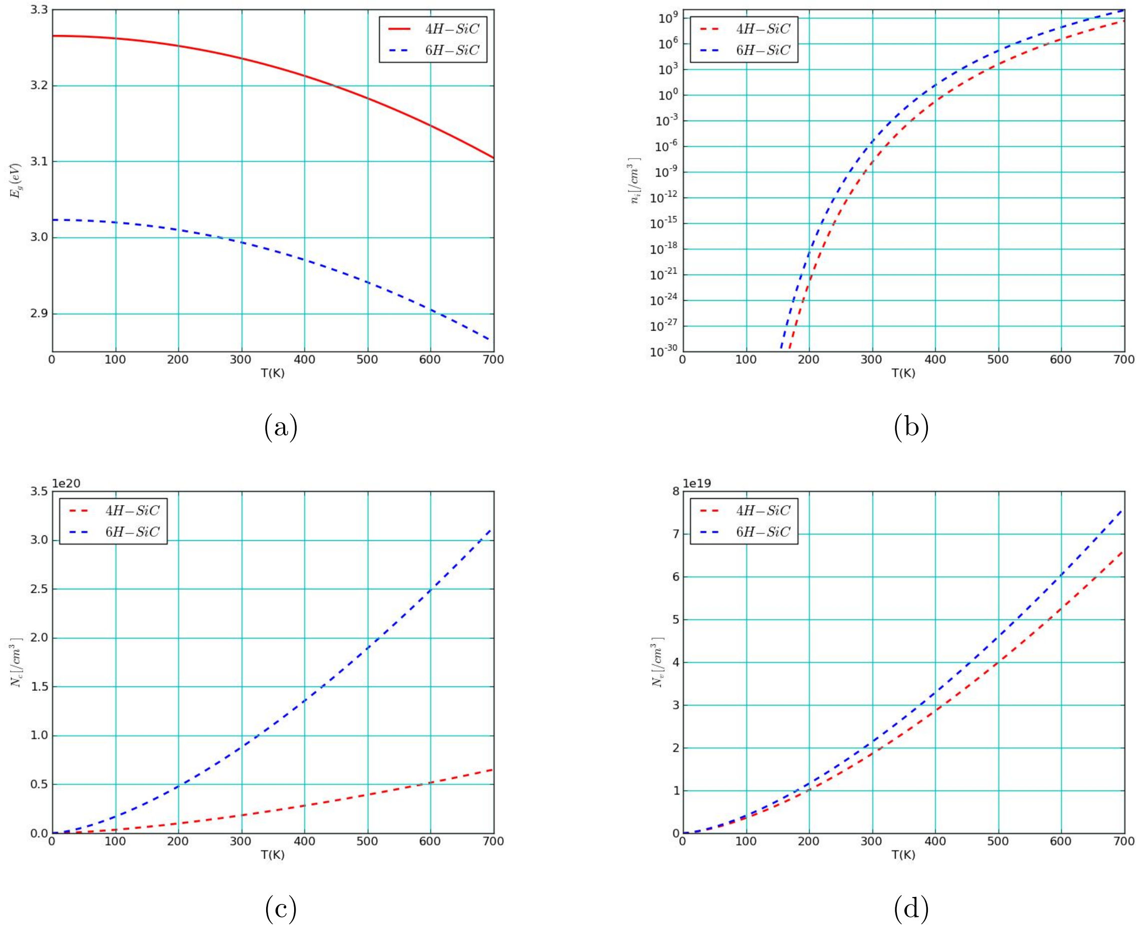


Figure 4.5: (a)-(d) The temperature dependence of the band gap energy, intrinsic carrier density, effective densities of states at the conduction and valence-band edges, respectively, in 4H- and 6H-SiC.

Figs.4.5 (a)-(d) depict the fitting of temperature dependence of the physics parameters E_g, n_i, N_c and N_v. The intrinsic carrier density of 4H/6H-SiC is smaller by the order of 16-18 compared to Si due to the wide band gap. Furthermore, the exponential dependence

of n_i on E_g introduces a rather large uncertainty, so that the overall error range can hardly be estimated.

4.2.2 Interface trap profiles in 4H and 6H-SiC MOS

In previous work by other authors, 6H-SiC MOS has been reported with lower interface trap density than 4H-SiC from various methods, including temperature dependent CV, constant capacitance deep-level transient spectroscopy (CCDLTS) technique, and simultaneous high-low frequency CV. None of these methods can take traps into account that respond with a rate higher than the highest measurement frequency, which is usually around 1-10 MHz in practice.

In section.3.2, we see that the NO or PSG post-oxidation treatment can greatly suppress the interface trap density (D_{it}) near the conduction band in 4H-SiC MOS. In this section, we investigate the effect of NO and PSG annealing on 6H-SiC MOS with the C-ψ_s method, which can take account of the "fast states", and make a cross comparison of D_{it} profiles with 4H- polytype. The motivation of this work is to expand the understanding of the effect of fast traps on SiC inversion channel transport by answering two questions: (1) Do 6H-SiC interfaces also contain fast traps? (2) What role may the fast traps have in the channel transport?

In our experiment, we fabricated two sets of capacitors in parallel for controlled comparison. For each polytype, there were four MOS samples: as-oxidized, NO annealing, 900 °C $POCl_3$ annealing and 1000 °C $POCl_3$ annealing. The 6H-SiC substrate has a lightly n-doped epitaxial layer with a thickness about 8 μm, and the doping concentration is $4{\sim}5\times10^{15}$cm^{-3}. The 4H-SiC epitaxial samples were commercially obtained, and had a donor concentration $\sim1\times10^{16}$cm^{-3}. After RCA cleaning, thermal oxidation was carried out at 1150 °C $POCl_3$ on (0001) Si-face of 4H- and 6H-SiC samples at the same time. One sample from each polytype was treated by post-oxidation annealing (POA) at 1175 °C $POCl_3$ in NO for 2 hours. Another two samples experienced $POCl_3$ annealing at 900 °C and 1000 °C, respectively (the

annealing procedure was the same as described in section.3.2.2). After formation of these different gate dielectrics, Ni was sputtered as back contacts for the MOS capacitors, and Al by thermal evaporation through a shadow mask was used as the gate metal.

Simultaneous high-low frequency capacitance-voltage (C-V) characteristics were measured at room temperature, using 100kHz as the high frequency. Based on the quasi-static CV measurement (low frequency), C-ψ_s analysis was applied to get the interface trap profiles.

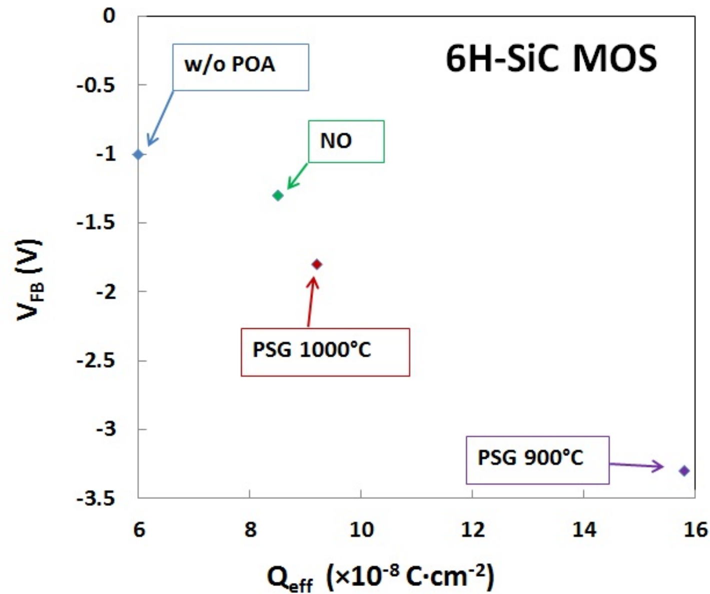


Figure 4.6: Flat-band voltage (V_{FB}) for 6H-SiC MOS capacitors with different annealing conditions vs. effective charge (Q_{eff}).

Fig.4.6 shows the flat-band voltage (V_{FB}) for 6H-SiC MOS capacitors with different annealing conditions and the corresponding effective charge (Q_{eff}). Compared to the as-oxidized interface, NO and $POCl_3$ annealing decrease the flat-band voltage by adding positive effective charge into the interface or oxide layer. As discussed above, nitrogen and phosphorus atoms, which substitute Si or C atoms at the interface, can serve as n-type dopants, and the fixed ion cores bring the positive effective charge to the interface.

Another fact from Fig.4.6 is that $POCl_3$ annealing at 900 °C introduces significantly more positive effective charge than that at 1000 °C, resulting in a shift of V_{FB} from -1.8V to -3.3V. The difference indicates that more phosphorus atoms enter the SiO_2/SiC interface

in $POCl_3$ annealing at 900 °C. This is consistent with the SiO_2-P_2O_5 phase diagram about PSG composition (seen Fig.3.10 in chapter 3), and consistent with the phosphorus uptake trend in 4H-SiC case as well.

For both high-low CV and C-ψ_s method, trap profiles below flat-band potential $E_g/2$-$k_B T \ln(\frac{\mathrm{N_D}}{\mathrm{n_i}})$ (for 6H-SiC, 0.25eV; for 4H-SiC, 0.20eV) is most accurate, and were extracted.

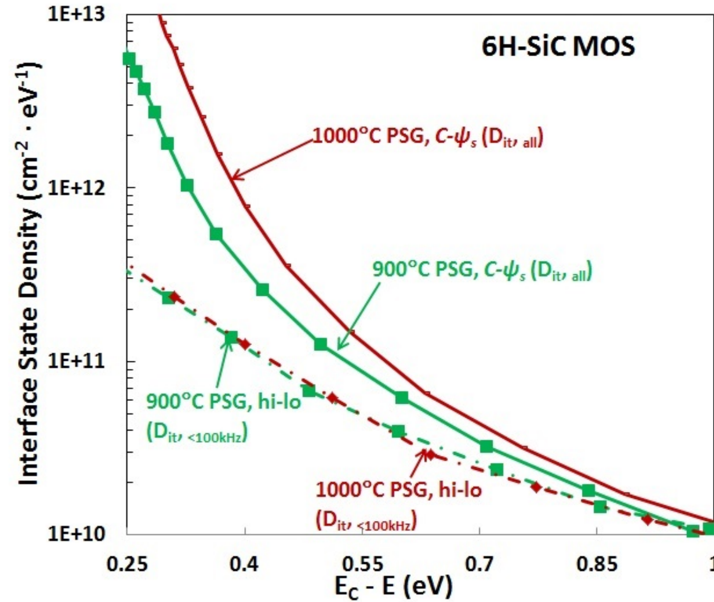


Figure 4.7: Interface trap density profiles for 6H-SiC MOS samples annealed in $POCl_3$ at 900 °C and 1000 °C, obtained by high-low method and C-ψ_s method.

Fig.4.7 shows the interface trap profiles determined by the two methods for 900 °C and 1000 °C annealed PSG on 6H-SiC. It is evident from the figure that, the C-ψ_s method exhibits much larger interface trap density (labeled as $D_{it,all}$) than the high-low CV method (labeled as $D_{it,<100kHz}$), especially when approaching the conduction band-edge. This figure indicates that "fast states" do exist in 6H-SiC MOS as well. For instance, at $E_c - E = 0.25$eV, $D_{it,all}$ is $5.4{\times}10^{12}$cm^{-2}eV^{-1} for 900 °C PSG, while the high-low method only detected a small portion of the total $D_{it,<100kHz} = 3.2{\times}10^{11}$cm^{-2}eV^{-1}. This comparison proves that high-low method severely underestimates the interface state density by not evaluating the fast states, consistent with previous reports.

Furthermore, the extracted $D_{it,<100kHz}$ profiles for the two different PSG devices are almost the same, while $D_{it,all}$ profiles indicate a remarkable discrepancy. This is linked to the phosphorus uptake difference, similar as the trend in 4H-SiC/PSG system which will be discussed in next section. 900 °C PSG has more interfacial phosphorus incorporation, and it leads to more interface trap passivation.

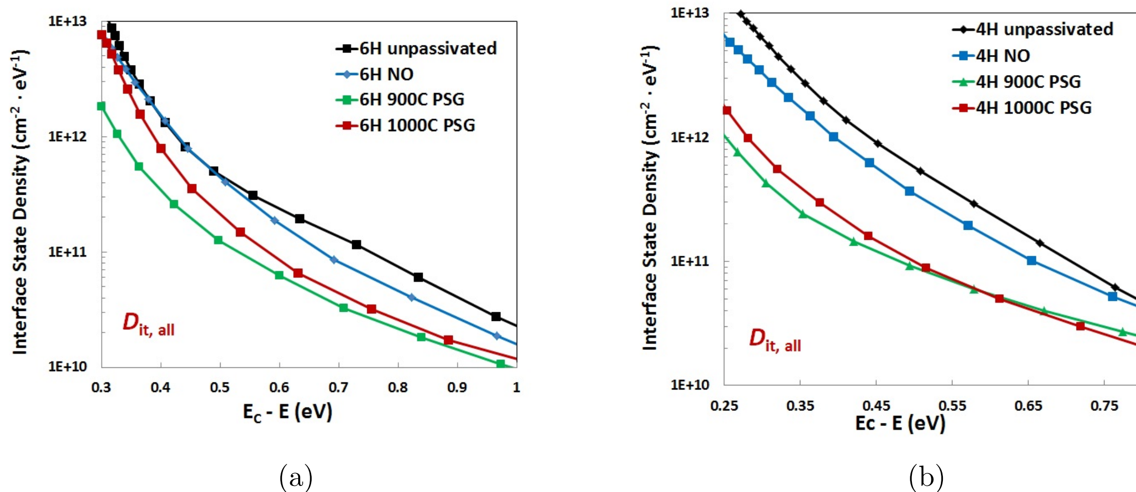


Figure 4.8: The breakdown test at room temperature on (a) a PDS-annealed capacitor device; (b) a $POCl_3$-annealed capacitor device.

Next, Fig.4.8 shows the $D_{it,all}$ profile comparison of different gate oxides on 4H and 6H MOS, separately. We notice that the as-oxidized gate dielectric has very high trap density. In general, both N and P incorporation reduce the interface traps, and the trap passivation by P incorporation is more efficient. In the 4H-SiC case, NO treatment reduces the traps located close to the conduction band-edge and deep level in the band-gap. In contrast, for 6H-SiC, nitrogen incorporation mainly reduces D_{it} located deep in the band-gap, with small improvement close to the conduction band-edge, consistent with reports in the literature.

Fig.4.9 shows the 4H- and 6H-SiC cross comparison of interface trap density profiles for gate oxide as oxidized, NO annealed and PSG annealed, respectively. Since the top of the valence energy bands in 4H- and 6H-SiC line up, the comparisons of these two polytypes have been made with respect to E_v. In every case, the interface trap density ($D_{it,all}$) profiles near the conduction band-edge for two polytypes are comparable.

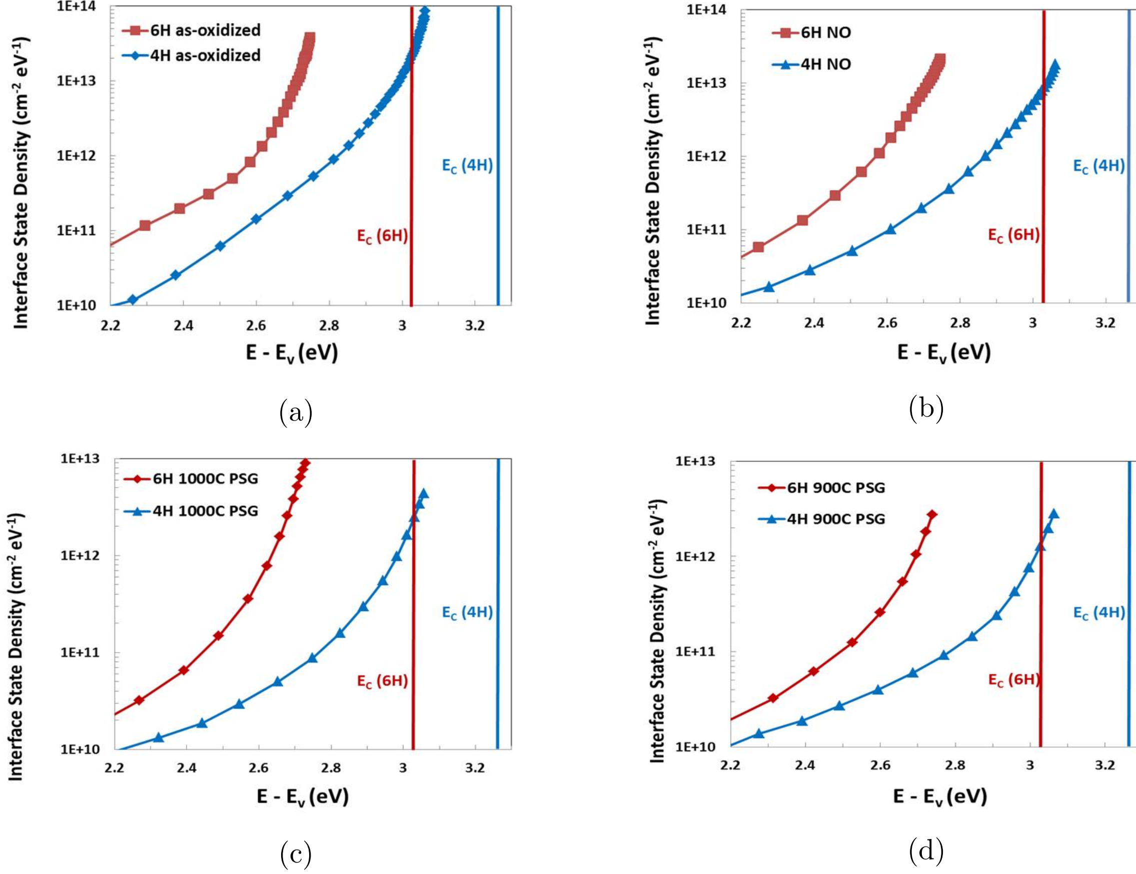


Figure 4.9: Interface trap density profile comparison between 4H- and 6H-SiC MOS capacitors. (a) gate oxide without POA annealing; (b) gate oxide with NO annealing; (c) gate oxide with 1000 °C $POCl_3$ annealing; (d) with 900 °C $POCl_3$ annealing. The vertical lines are corresponding to the band gap of 4H-SiC (blue) and 6H-SiC (red).

In literature, NO annealing improved channel mobility in 4H-SiC from $\sim$5 $cm^2V^{-1}s^{-1}$ to 30$\sim$40 $cm^2V^{-1}s^{-1}$. Y. Deng *et al.*[9] reported that NO annealing in 6H-SiC improves the peak mobility from 30 $cm^2V^{-1}s^{-1}$ to a slightly higher value 40 $cm^2V^{-1}s^{-1}$. This increase of mobility was ascribed to the passivation of deep traps, as shown in Fig.4.10. From the $I_d - V_g$ characteristic of MOSFETs in the subthreshold region, they extracted the total interface trap density N_{it} with subthreshold slope method. The marginal improvement of NO annealing in 6H-SiC can be explained by the deep trap passivation and small reduction of N_{it}.

From the interface trap density profiles by C-ψ_s method (in Fig.4.9), N_{it} was calculated by integrating $D_{it,all}$ for each case. The integration range is from flat-band level to E_c - 1.0eV, below which the $D_{it,all}$ values are relatively small that add little to the total N_{it}. As discussed above, the flat-band level for 6H-SiC is ∼0.25eV, for 4H-SiC, ∼0.20eV, as shown in Fig.4.11.

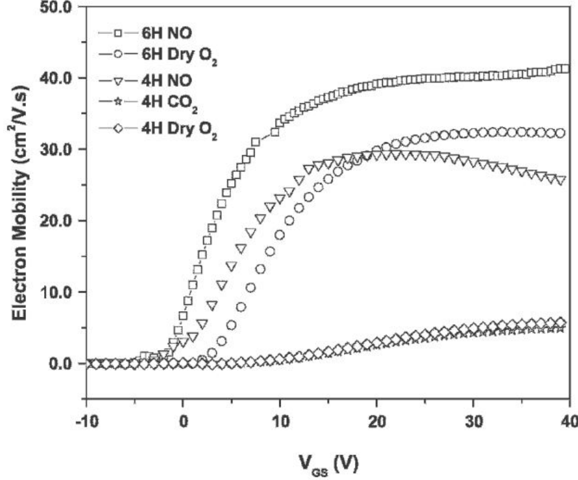


Figure 4.10: Field-effect mobility of 4H and 6H-SiC MOSFETs under various annealing processes.[9]

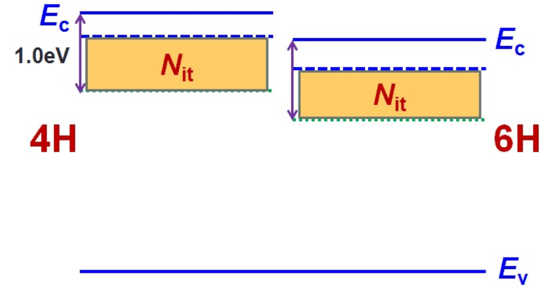


Figure 4.11: The schematic of N_{it} integration range in 4H- and 6H-SiC.

Table 4.2: N_{it} values from C-ψ_s and subthreshold slope method for 4H-SiC and 6H-SiC MOS under various annealing processes. The mobility improvements by NO annealing in both polytypes are listed as reference.

Material	process	N_{it} from C-ψ_s $\times 10^{11}\mathrm{cm}^{-2}$	N_{it} from SS[9] $\times 10^{11}\mathrm{cm}^{-2}$	peak mobility $\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$
4H-SiC	as-oxidized	29.36	34	5
	NO	10.42	9.5	30
	1000 °C PSG	3.07		105 [10]
	900 °C PSG	1.79		100 [10]
6H-SiC	as-oxidized	10.40	10	30 [9]
	NO	6.95	7.8	40 [9]
	1000 °C PSG	5.16		
	900 °C PSG	1.81		

Previously, Yoshioka *et al.*[11] reported that in 4H-SiC MOS, D_{it} at E_c - 0.2eV values evaluated from SS method and C-ψ_s method show very good agreement. In our comparison,

Table.4.2 lists the N_{it} values extracted by both C-ψ_s (sum of slow and fast traps) and subthreshold slope method, and the corresponding mobility values in as-oxidized and NO annealed MOSFETs. We notice that not only in 4H-SiC MOS, also in 6H-SiC MOS, the N_{it} values are consistent by these two methods. Note that NO annealed 4H-SiC MOS and as-oxidized 6H-SiC MOS have almost same N_{it} values and peak mobilities.

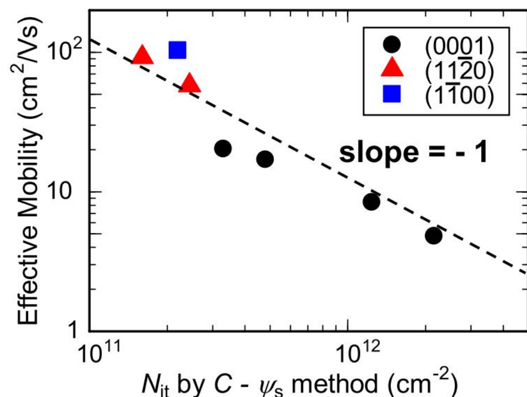


Figure 4.12: Correlation between the effective mobility and the integrated interface state density N_{it} for 4H-SiC (0001), (11$\bar{2}$0), and (1$\bar{1}$00) MOSFETs with nitrided gate oxides. N_{it} was calculated from the D_{it} distribution determined by C-ψ_s method.[12]

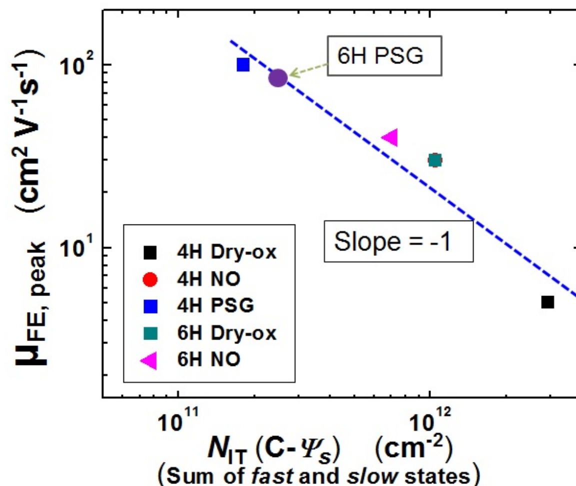


Figure 4.13: Correlation between the peak field-effect mobility and the integrated interface state density N_{it} for both 4H- and 6H-SiC MOS with different gate dielectric. N_{it} was calculated from the D_{it} distribution determined by C-ψ_s method.

Another observation is that regardless of polytypes, N_{it} is an important factor in limiting the channel mobility. Fig.4.13 shows the correlation between the peak field-effect mobility and the integrated interface state density N_{it} for both 4H- and 6H-SiC MOS with different gate dielectric. The $POCl_3$ annealing at 1000 °C possibly activates a lot more phosphorus atoms[10], hence the mobility improvement is greatly enhanced by the surface counter-dopants, so we didn't include the data from 1000 °C PSG dielectric in Fig.4.13.

In the figure, both $\mu_{\text{fe,peak}}$ and N_{it} are in log scale. The linear fitting shows slope=-1, meaning the $\mu_{\text{fe,peak}}$ and N_{it} are numerically in inverse proportion. This correlation is consistent with that reported by S. Nakazawa *et al.*[12], as seen in Fig.4.12. Instead of N_{it},

with regard to D_{it} at certain level, similar correlations were reported by Kobayashi *et al.*[13] and Yoshioka *et al.*[11].

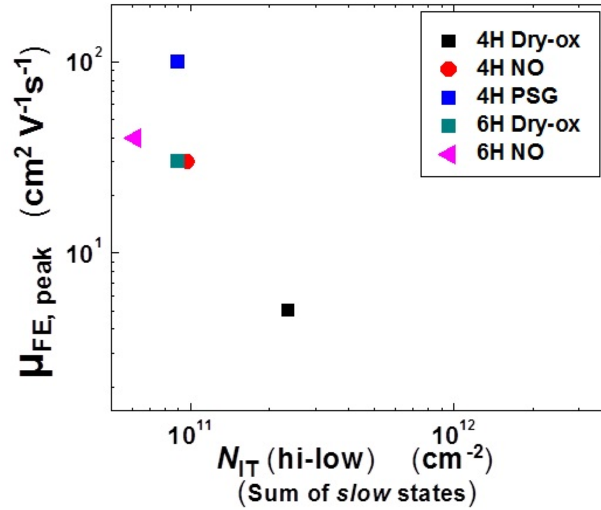


Figure 4.14: Correlation between the peak field-effect mobility and interface state density N_{it}. N_{it} was calculated from the D_{it} distribution determined by high-low method.

On the other hand, the N_{it} integrated from the hi-low method (only slow traps) and the peak field-effect mobility show very poor correlation (Fig.4.14). For example, a large difference in channel mobility between 4H-SiC NO and 4H-SiC PSG exists at similar N_{it}. The figures suggest that the correlation can be extended to different polytypes and that fast states do negatively affect the channel transport. Based on this correlation, we expect that $POCl_3$ annealing can raise the channel mobility in 6H-SiC MOSFET to $\sim$90 $cm^2V^{-1}s^{-1}$, as pointed out in Fig.4.13.

4.3 Trend of 4H-SiC/PSG electrical properties in terms of P uptake

4.3.1 Flat-band voltage and effective charge

On MOS capacitors with different PSG dielectrics mentioned in chapter 3, high-frequency (100 kHz) and quasi-static capacitance-voltage characteristic was performed at room temperature in a dark box using a CV Meter (Keithley model 595).

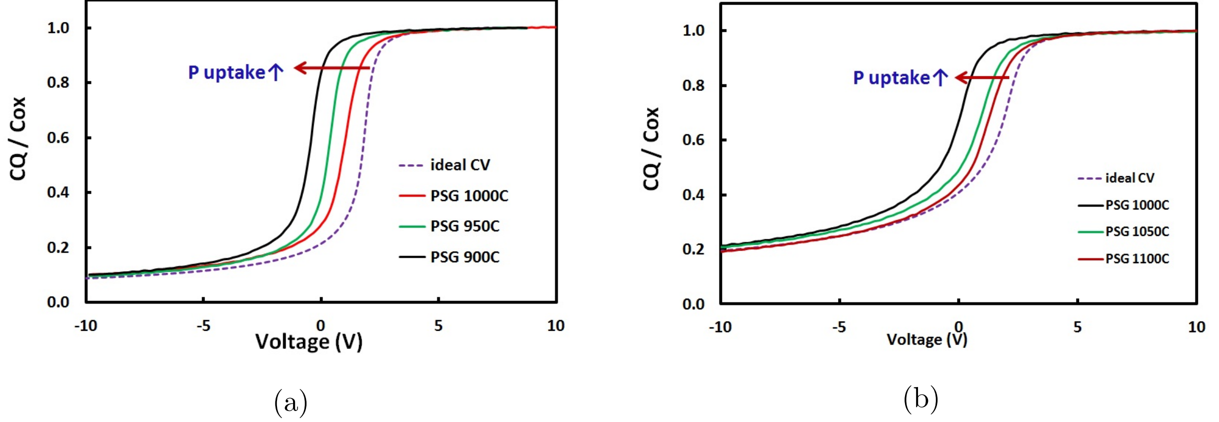


Figure 4.15: The breakdown test at room temperature on (a) a PDS-annealed capacitor device; (b) a $POCl_3$-annealed capacitor device.

From the CV measurements, the first observation is the position shift of CV curves. Fig.4.15a shows the dielectric thickness normalized CV curves of three MOS capacitors fabricated on 5×10^{15}cm^{-3} n-type doped SiC epi-layers, with $POCl_3$ annealing temperatures, 900 °C, 950 °C and 1000 °C, (and therefore different P concentrations). In this figure, the ideal CV curve (the dashed line), simulated from MOS physics [14], is added as reference. The flat-band voltage of the ideal CV curve is modified by the additional fixed charge introduced during the molybdenum gate sputtering process in our lab. Similarly, Fig.4.15b shows the normalized CV curves of MOS capacitors fabricated on 1×10^{16}cm^{-3} n-type doped SiC epi-layers, with annealing temperatures, 1000 °C, 1050 °C and 1100 °C. Note that the depletion capacitance in deep depletion region is higher in 1×10^{16}cm^{-3} doped epi-layer, since the depletion capacitance C_d is proportional to $\sqrt{N_D}$ in Eq.(2.15).

The figures clearly indicate the increase of effective positive charge with the decreasing $POCl_3$ annealing temperature (increasing phosphorus concentration), resulting in an decreasing flat-band voltage (V_{FB}). Hence, the shift of CV curves is consistent with the P uptake trend with regard to the annealing temperature.

Near the PSG/SiC interface, some P atoms, which occupy Si sites, act as donors and contribute to the total effective charge (Q_{eff}). From Eq.(2.9), we can calculate the corresponding effective charge. Fig.4.16 shows the number of effective charge N_{eff} ($=Q_{\text{eff}}/q$) vs.

the $POCl_3$ annealing temperature. Here, we can see the noticeable trend: as annealing temperature decreases, more and more phosphorus atoms incorporate at the PSG/SiC interface, hence more positive effective charge are generated.

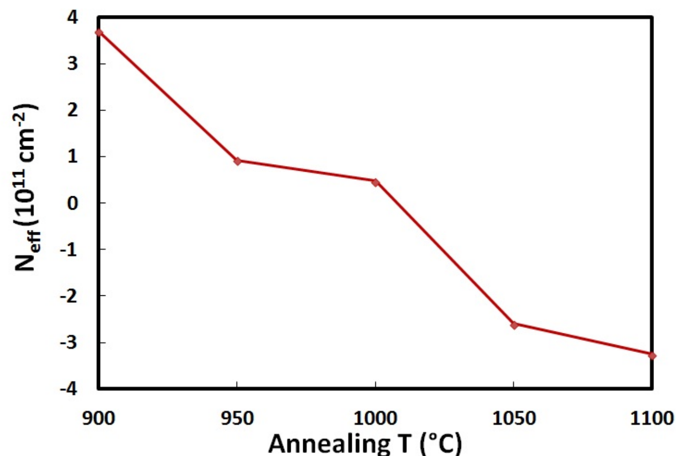


Figure 4.16: Phosphorus coverage at the interface of SiC (left-axis) and the atomic percentage of P in PSG bulk (right-axis) as a function of $POCl_3$ annealing temperature.

4.3.2 Interface trap density

Fig.4.17 shows the interface trap density extracted from the conventional simultaneous high (100kHz)-low frequency C-V method. As previously reported, 100kHz is not high enough to detect very "fast traps" that exist at SiO_2/SiC interfaces. A large amount of traps close to the conduction band can respond to the 100kHz signal, which makes them undetectable by the principle of high-low technique. Therefore in this measurement, D_{it} is denoted as $D_{it,<100kHz}$.

The correlation between the interface P coverage and interface trap density can be inferred from this figure. Overall, higher P coverage leads to a lower interface trap density. The $D_{it,<100kHz}$ curves of 1000 °C and 950 °C annealed PSG are very close above 0.5eV, while showing obvious difference below that energy level. Compared to devices annealed at 1000 °C, the additional P atoms incorporated from the lower annealing temperature dramatically eliminates the deep level traps.

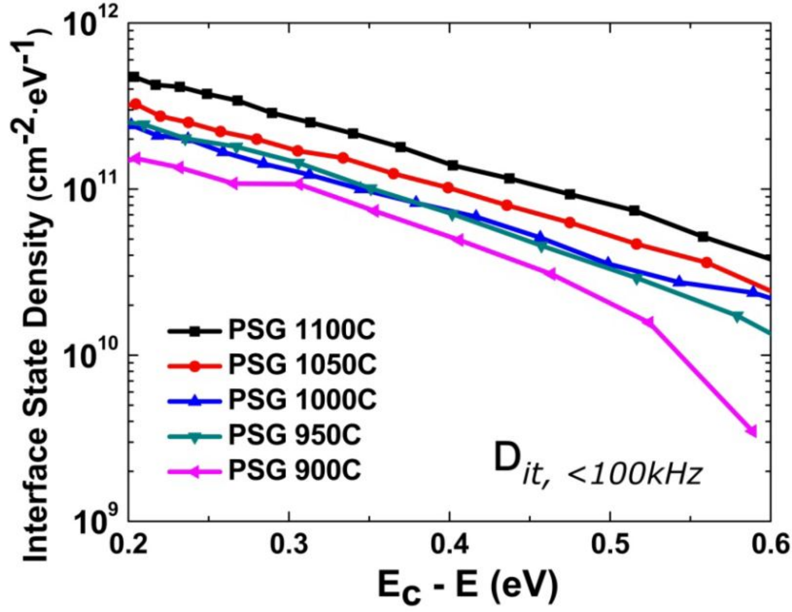


Figure 4.17: Interface trap density (slower than 100kHz) of five MOS capacitors with different interface phosphorus coverage.

Using the quasi-static capacitance (C_{QS}), the C-ψ_s method was applied according to the procedure described in chapter 2. C-ψ_s method uses the deviation of the measured quasi-static C-V with the theoretically calculated C-V to estimate D$_{it}$. This allows the detection of very fast states with emission times shorter than practical measurement frequencies (1MHz or 10^{-6} s), which cannot be detected by the high-low method. The extracted interface trap density is denoted as D$_{it,all}$, shown in Fig.4.18.

The same correlation between the interface P coverage and interface trap density is observed using C-ψ_s method, although the D$_{it}$ values are higher here due to inclusion of the fast states. The subtraction of D$_{it,<100kHz}$ from D$_{it,all}$ can be deemed as the fast states densities that are not counted by high-low method. For the 1050 °C and 1100 °C annealed PSG, D$_{it,all}$ is an order of magnitude higher than D$_{it,<100kHz}$ at 0.2eV, therefore the fast state density is almost ten times that of the slow state density(<100kHz) in low P coverage cases. As P incorporation increases, in 1000 °C and 950 °C annealed PSGs, the values of D$_{it,all}$ and D$_{it,<100kHz}$ become close, indicating more fast traps reduction. In this comparison, we lack the total interface state density distribution for the 900 °C-annealed device because of

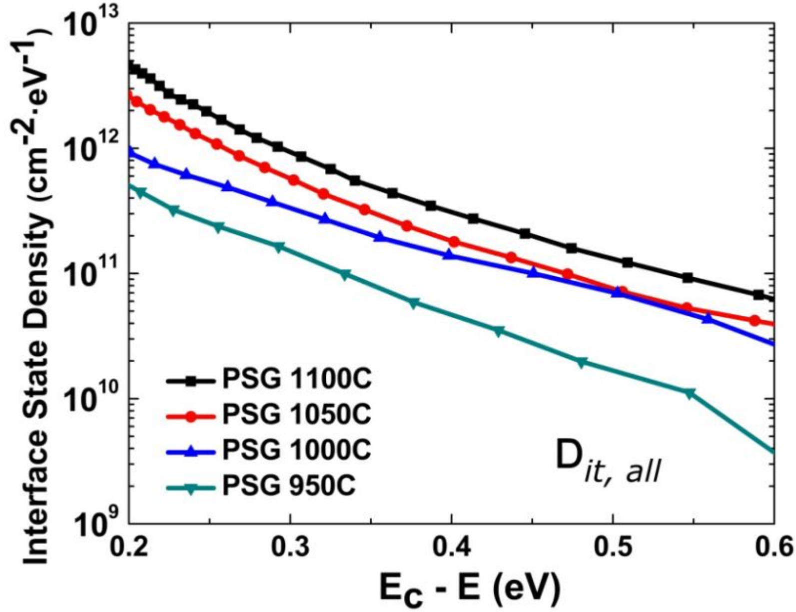


Figure 4.18: Phosphorus coverage at the interface of SiC (left-axis) and the atomic percentage of P in PSG bulk (right-axis) as a function of $POCl_3$ annealing temperature.

the non-physical nature of extracted data (negative density). The calculation of theoretical capacitance-voltage curve is based on the assumption of constant substrate doping. However, large amount of P atoms acquired at 900 °C possibly alters the surface potential so significantly as to affect the calculation of the theoretical capacitance. We believe that the true $D_{it,all}$ for this PSG device should be very close to $D_{it,<100kHz}$, which is shown in Fig.4.17.

4.3.3 Field-effect mobility in PSG

On MOSFETs with different PSG dielectrics, drain current-voltage ($I_D - V_G$) characteristic was performed at room temperature under dark condition using Keithley 2400 Source Meter. Field-effect mobility (μ_{eff}) is extracted by

$$\mu_{fe} = \frac{Lg_m}{WC_{ox}V_{DS}}$$

where transconductance $g_m \equiv \frac{\partial I_D}{\partial V_{GS}}|_{V_{DS}}$, C_{ox} is the oxide capacitance per unit area, L channel length 150 μm, W channel width 290 μm, and drain voltage V_D is set as 0.025V.

Fig.4.19 shows the room temperature channel field-effect mobility characteristics of 4H-SiC MOSFETs fabricated using different PSG gate dielectrics formed by annealing at 900 °C, 1000 °C, 1050 °C and 1100 °C, respectively.

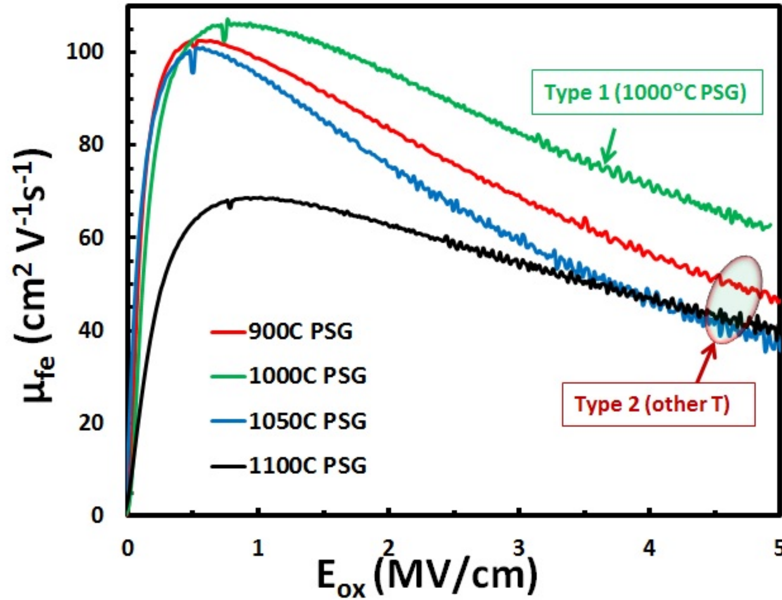


Figure 4.19: Field-effect mobility of 4H-SiC MOSFETs fabricated on Si face by dry oxidation and $POCl_3$ annealing at 900 °C, 1000 °C, 1050 °C and 1100 °C.

All devices show a small threshold voltage (V_T) close to 0 V, which is acceptable considering the low p-well doping of the samples. The results can be categorized into two types of mobility behavior. Type-1(PSG 1000 °C) with peak mobility 105 cm^{2}V^{-1}s^{-1}, gradually decreases as the oxide field ($E_{ox} = V_G/t_{ox}$) increases; but even at fields as high as 5MV/cm, the mobility is still high, about 62 cm^{2}V^{-1}s^{-1}. Type-2 (PSG annealed at temperatures other than 1000 °C) behavior corresponds to lower peak mobility values and a more rapid decrease of mobility as the oxide field increases. The lowest peak mobility, observed from PSG formed at 1100 °C, is 68 cm^{2}V^{-1}s^{-1}, still about twice that of the typical peak channel mobility of standard NO-annealed MOSFETs.

The type-2 behavior shows a trend which demonstrates well the effect of P incorporation variation on the transport properties in MOS devices. With increasing $POCl_3$ annealing temperature, the transconductance becomes smaller, consistent with the lower P coverage

and corresponding higher D_{it}. Even though lower P incorporation leads to lower mobility, it should be noted that it is still significantly superior compared to conventional NO annealing. Therefore, the optimum trade-off between P incorporation, mobility and device instability should be further investigated. The two types of mobility behavior infer that other than the amount of P incorporation at different annealing temperature, there is also difference in the way P atoms are incorporated in the bulk or at the interface of PSG/SiC.

N. Murphy *et al.*[15] pointed out that:

$$\mu_{\mathrm{fe}} = (1 - \gamma)\left[n \cdot \frac{d\mu_{con}}{dn} + \mu_{con}\right] \tag{4.7}$$

where γ stands for the proportion of the induced charge which is trapped in the interface states, μ_{con} the conduction mobility, and n the carrier concentration.

The conduction mobility μ_{con} usually varies with the carrier concentration n, therefore the carrier concentration plays a role in the field-effect mobilty. Even though 900 °C PSG has a greater P uptake than 1000 °C PSG, the higher field-effect mobility in 1000 °C PSG (type-1) at high field, where nearly all the traps are filled, probably results from a higher carrier concentration. One explanation could be that $POCl_3$ annealing at 1000 °C is accompanied by prominent surface counter-doping effect. Those P atoms which enter SiC side would occupy Si or C sites to become substitutional dopants, and this dopant activation happens most significantly at 1000 °C. However, this hypothesis needs to be experimentally confirmed by means of charge profile measurement, such as scanning-capacitance microscopy (SCM).

The difference in these two types of mobility behavior also gives rise to some other aspects of channel transport. Next, we have analyzed the temperature dependence to reveal the mobility-limiting mechanisms in these two types.

4.3.4 Mobility limiting mechanisms

Mobility follows Matthiessen's rule: the inverse of the total amount is equal to the sum of the inverse of each contributing part. Therefore, the total amount will always be less than the smallest contributor. The net mobility of the inversion channel depends on various mobilities as

$$\frac{1}{\mu} = \frac{1}{\mu_c} + \frac{1}{\mu_{sp}} + \frac{1}{\mu_{sr}} + ... \tag{4.8}$$

where μ_c is the Coulomb scattering mobility, μ_{sr} the surface roughness scattering mobility, and μ_{sp} the surface phonon scattering mobility. These three mobilities are each limited by a separate scattering mechanism, and the lowest mobility dominates the net mobility.

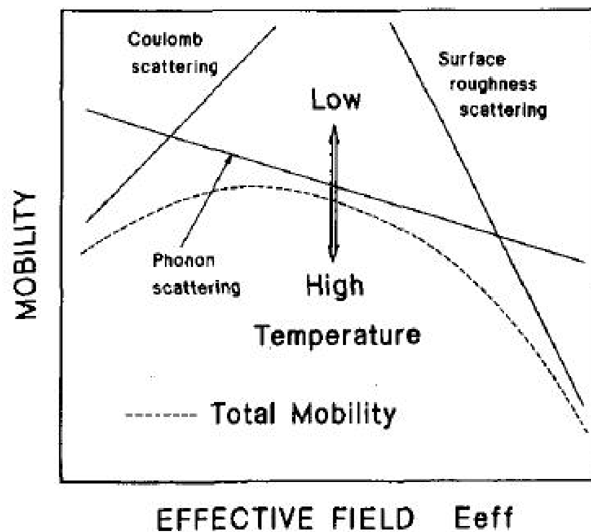


Figure 4.20: The three scattering mechanisms and their effect on the total mobility in the inversion channel.[16]

In Si MOSFETs, S. Tagaki *et al.*[16] reported the universality of inversion layer mobility. Fig.4.20 shows a schematic diagram of the E_{eff} (or n_s) dependence on the basis of a general understanding of the inversion layer mobility. According to this diagram, the universal curve can be divided into Coulomb scattering term, phonon scattering term and surface roughness scattering term. In different region, one mechanism dominates.

In SiC MOSFETs, as investigated by several authors[17;18], the mobility can be similarly separated into the scattering mechanisms as in Si MOSFETs. Each mobility component has different dependence on the temperature. For Coulomb scattering, as temperature goes up, the Fermi energy level of the semiconductor becomes lower, therefore the released electrons from the interface trap (whose levels are below the low temperature Fermi energy) reduce the number of scattering centers, and on the other hand the increase of the inversion layer electrons contributes to the screening of the Coulomb scattering centers effectively. As a result, μ_c increases at a higher temperature. For the surface phonon scattering, when temperature goes up, the crystal lattice vibration becomes stronger, which leads to an increase in the number of surface phonons. Hence, μ_{sp} decreases at a higher temperature[19–21]. For the surface roughness scattering, it is weakly dependent on the temperature, but mainly affected by the transverse electric fields.

S.Potbhare *et al.*[18] simulated the surface phonon mobility component as

$$\mu_{sp} = \frac{A}{E_{\text{eff}}} + \frac{B}{TE_{\text{eff}}^{1/3}} \tag{4.9}$$

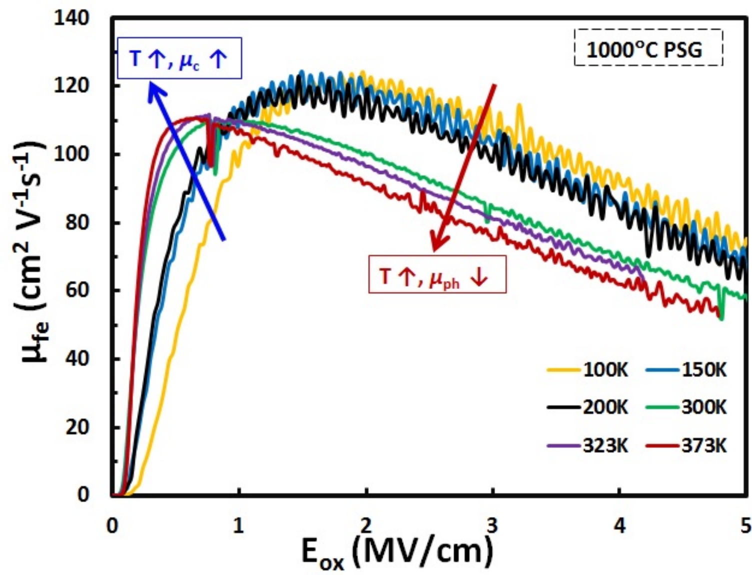
where A and B are parameters evaluated using theory and experiment.

Surface roughness mobility component as

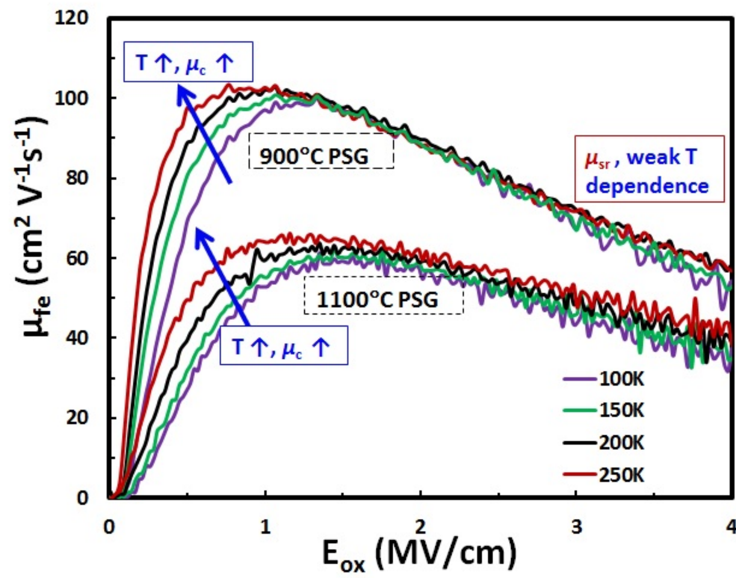
$$\mu_{sr} = \frac{\Gamma_{sr}}{E_{\text{eff}}^2} \tag{4.10}$$

where Γ_{sr} is a parameter that depends on the roughness of the SiO_2/SiC interface.

To examine the scattering mechanisms in PSG gated 4H-SiC MOSFETs, the temperature dependence of the mobility was performed under dark conditions in a wide temperature range of 20K-300K. The temperature dependence of the mobility reveals different mobility limiting mechanisms at different transverse electric fields[17;22;23]. Note that the field-effect mobility used in this study is not identical to the actual conduction mobility of electrons in the inversion layer because the number of free electrons in the inversion layer is decreased



(a)



(b)

Figure 4.21: The temperature dependence of field-effect mobility on the MOSFETs (a) with PSG dielectric annealed at 1000 °C (type-1), (b)with PSG dielectric annealed at 900 °C and 1100 °C (type-2).

by the interface traps. However, the results of this study provide a qualitative analysis of the mobility limiting mechanisms in PSG devices.

Fig.4.21a shows the temperature dependence (100K - 373K) of the 1000 °C PSG MOSFET. At low E_{ox}, mobility is mainly limited by Coulomb scattering, indicated by the increasing field-effect mobility with rising ambient temperature. When the temperature increases, for a given gate bias, the trapped charge is reduced in light of lowering of Fermi energy level. On the other hand, the number of free carriers in the inversion layer significantly increases with increasing temperature, thus collecting more electrons in the drain of the device. This effect is similar to NO devices[24], but significantly weaker for PSG, consistent with a lower trap density. At high E_{ox}, the mobility decreases as ambient temperature increases, indicating it is limited by phonon-scattering (μ_{sp}). The number of surface acoustic phonon increases with the rising in temperature, and this leads to a more remarkable phonon scattering and therefore the reduction in electron mobility.

Fig.4.21b shows the temperature dependence (100K - 250K) of PSG 900 °C and 1100 °C MOSFETs. At high E_{ox}, the mobility weakly changes with the ambient temperature, indicating the mobility is limited by surface roughness scattering (μ_{sr}). Interestingly, the surface roughness mobility for PSG devices is significantly higher than that of NO-annealed devices.

Therefore, two types of mobility behavior are dominated by different scattering mechanisms at high oxide fields. As discussed above, 1000 °C annealed PSG (type-1) seems to represent an optimum of P passivation, surface counter-doping, and possibly a minimal interface roughness, such that the expected surface phonon-related temperature dependence is observed. Again, this explanation needs to be verified by futher detailed investigation.

4.4 Summary

In summary, the interface trap density profiles for 4H-SiC and 6H-SiC MOS structures have been investigated by employing the C-ψ_s method. The D_{it} comparison between hi-low CV method and C-ψ_s method indicates that in 6H-SiC MOS there also exists "fast states".

Besides, the phosphorus incorporation (PSG dielectric) passivates the interface traps both near conduction band edge and deep level. The total interface trap density N_{it} calculated from C-ψ_s is consistent with that from SS method. The total interface trap density N_{it} is limiting the mobility for both 4H-SiC and 6H-SiC MOS, and the correlation suggests that the "fast states" also have a detrimental effect on the MOSFET channel transport.

For 4H-SiC MOS devices with PSG gate dielectrics, the correlation between the phosphorus uptake and the electrical properties has been investigated. Higher interfacial phosphorus coverage leads to lower interface trap density. In general, there is a trend between phosphorus incorporation and the channel mobility, namely, phosphorus incorporation significantly improves the channel mobility. However, there is an anomaly in the mobility enhancement in $POCl_3$ annealing at 1000 °C. It possibly can be attributed to an enhanced counter-doping effect, which needs further investigation. $POCl_3$ annealing at different temperatures results in two types of mobility behavior, one identified as surface roughness scattering limited, the other limited by surface phonon scattering at high transverse field.

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Chapter 5

PSG-based MOS device stability

5.1 Bias temperature instability

In both Si and SiC MOSFETs, the applied gate voltages and an elevated temperature during the device operation can cause a shift of threshold voltage V_{th}. This degradation phenomenon is called bias temperature instability (BTI), and this degradation typically exhibits logarithmic dependence on time. BTI is a key reliability issue in devices before large scale production in industry. It is of immediate concern in MOS devices, since they almost always operate with applied gate-to-source voltage. Except changing the threshold voltage V_{th}, other important transistor parameters which degrade because of BTI are: decreasing transconductance g_m, decreasing linear drain current $I_{\mathrm{d,lin}}$ and saturation current $I_{\mathrm{d,sat}}$, decreasing channel mobility μ_{eff}, decreasing subthreshold slope SS, increasing off current I_{off}.

Currently, NO annealing is a primary process for commercial power SiC MOSFETs. In addition to reducing the interface state density and improving mobility, nitridation of the SiO_2/SiC interface also yields immunity to electron injection but increases hole trapping[1]. In early 2013, Cree Inc. commercially introduced its 2nd Generation $25m\Omega$ and $80m\Omega$, 1200V planar SiC MOSFETs. Innovation on SiC MOSFET device design and manufacturing processes continues to drive reliability and performance improvements and cost reductions. These ongoing refinements are being implemented into current- and next-generation SiC MOSFETs and have lead to a significant improvement in long-term stability and reliability, as well as a reduction in the specific on-resistance ($R_{\mathrm{on,sp}}$) of 40% in a 1200 V device compared to Cree's C2M product family. On this basis, it is particularly important to understand the instability mechanisms for SiC MOS structures.

Several factors may contribute to BTI in SiC at higher temperatures, including temperature induced barrier lowering and trap-creation [2], hole trapping, hot-carrier injection, and etc. To test the bias temperature instability, the stress conditions typically lie below 6MV/cm for the gate oxide electric field and temperatures ranging between 100-300 °C. Higher electric fields can cause additional degradation due to hot carriers and should be avoided for the evaluation of BTI. Particularly, with PSG dielectric, the intrinsic polarization is another essential factor leading to the bias temperature instability.

5.2 Two competing mechanisms in PSG dielectric instability

The stability of the various PSG devices was investigated by bias-temperature-stress (BTS) test on MOS capacitors. The stressing condition was +1.5MV/cm at 150 °C for 5 minutes or 1 hour. Immediately after the stressing, the capacitance (flat-band voltage $=V_{FB1}$) at room temperature was measured, and compared with the pre-stressed CV curve (flat-band voltage$=V_{FB0}$). It was found that for devices annealed at temperature equal to or lower than 1000 °C, the flat-band voltage shift $\Delta V_{FB} = V_{FB1} - V_{FB0}$ was always negative indicating positive polarization charge. For the 1100 °C annealed PSG, ΔV_{FB} was positive, indicating accumulation of negative charge in the dielectric as a result of electron trapping. Interestingly, both kinds of V_{FB} shift were observed on the PSG 1050 °C devices, but with significantly smaller net magnitudes. This instability combined with the P uptake and D_{it} trend, suggests that the V_{FB} shift is determined by two competing mechanisms, namely polarization charge in PSG and electron trapping in the PSG. Therefore, the flat-band voltage shift can be expressed as:

$$q \cdot (N_{trp} - N_{pol}) = C_{ox} \cdot (V_{FB1} - V_{FB0}) \tag{5.1}$$

where N_{trp} is the areal density of trapped electrons, N_{pol} the areal density of polarization charge, C_{ox} the oxide capacitance per unit area, V_{FB1} and V_{FB0} are as mentioned above.

After depolarization under zero bias and room temperature for several weeks, the CV curves were measured again (flat-band voltage = V_{FB2}). Assuming that within the long period of time, most of the polarization relaxed, and the electron de-trapping process was much slower than depolarization, from Eq.(5.1):

$$q \cdot N_{trp} = C_{ox} \cdot (V_{FB2} - V_{FB0}) \tag{5.2}$$

Solving for N_{pol}, we can get

$$q \cdot N_{pol} = C_{ox} \cdot (V_{FB2} - V_{FB1}) \tag{5.3}$$

Using these equations, the polarization charge and electron trapped charge for PSG annealed at 1000 °C, 1050 °C and 1100 °C was extracted from 5 minutes and 1 hour BTS tests, as shown in Table.5.1.

Table 5.1: Polarization and electron trapping charge densities for different PSG dielectrics extracted from 5 minutes and 1 hour BTS tests.

Gate oxide	N_{pol} ($\times 10^{12}$cm^{-2}) [5min BTS]	N_{trp} ($\times 10^{12}$cm^{-2})	N_{pol} ($\times 10^{12}$cm^{-2}) [1h BTS]	N_{trp} ($\times 10^{12}$cm^{-2})
PSG 1000 °C	**1.39**	0.56	**1.23**	0.77
PSG 1050 °C	**0.44∼0.83**	0.39∼0.70	**0.40∼0.66**	0.60∼1.45
PSG 1000 °C	**0.17**	0.34	**0.32**	0.88

Fig.5.1 shows the data extracted from two stressing time spans. The polarization charge density N_{pol} exhibits trends with regard to the annealing temperatures, indicating that polarization charge scales with the P uptake. Meanwhile, as we can notice, the electron trapping charge density shows relatively steady characteristic and longer stressing time causes more electron trapping effect. Usually, it exhibits logarithmic dependence on time.

From BTS tests on MOS capacitors, we can conclude that higher P incorporation in the gate dielectric causes higher device instability. This conclusion is supported by BTS tests (stressing condition: +1.5MV/cm @150 °C for 5 minutes and 1 hour) on MOSFETs as well.

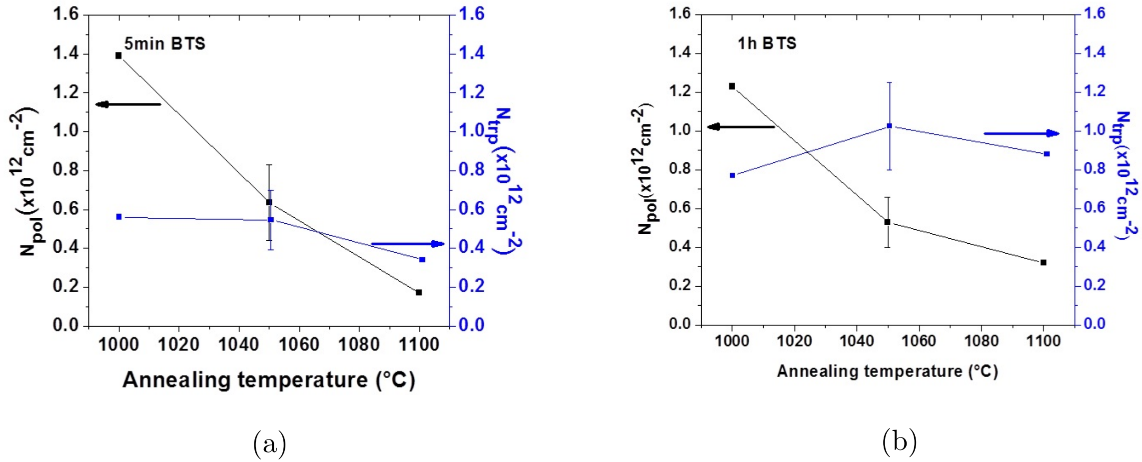


Figure 5.1: (a) Polarization and electron trapping charge densities extracted from 5 minutes BTS (b) Polarization and electron trapping charge densities extracted from 1 hour BTS.

As an example, the pre and post-stress $I_D - V_G$ and μ_{fe} results for the 1050 °C annealed PSG and 1100 °C annealed PSG MOSFET with 5 minutes stressing are shown in Fig.5.2.

It is evident from the figures that the stressing results in a lateral shift of the transfer characteristics, and overall maintains the same field-effect mobility shape. Table.5.2 summarizes the threshold voltage shift (ΔV_T) for each device after stressing (+1.5MV/cm @150 °C) for 5 minutes and 1 hour. The data for 900 °C PSG after 1h BTS is missing as the device degraded after stressing.

Table 5.2: Threshold voltage shift after BTS on MOSFETs.

Gate oxide	ΔV_{T} (V) [5min BTS]	ΔV_{T} (V) [1h BTS]
PSG 900 °C	-7.2	–
PSG 1000 °C	-3.8	-4.4
PSG 1050 °C	-1.3	-0.7
PSG 1000 °C	0.3	1.2

From Table.5.2, we can see that the PSG device stability depends on the trade-off between polarization and electron trapping. It has been demonstrated that employing stacked PSG structures can minimize the negative effect of PSG polarization and obtain good device stability [3]. These results further affirm the observation that with precise control of the phosphorus uptake, good device stability and reliability can be obtained.

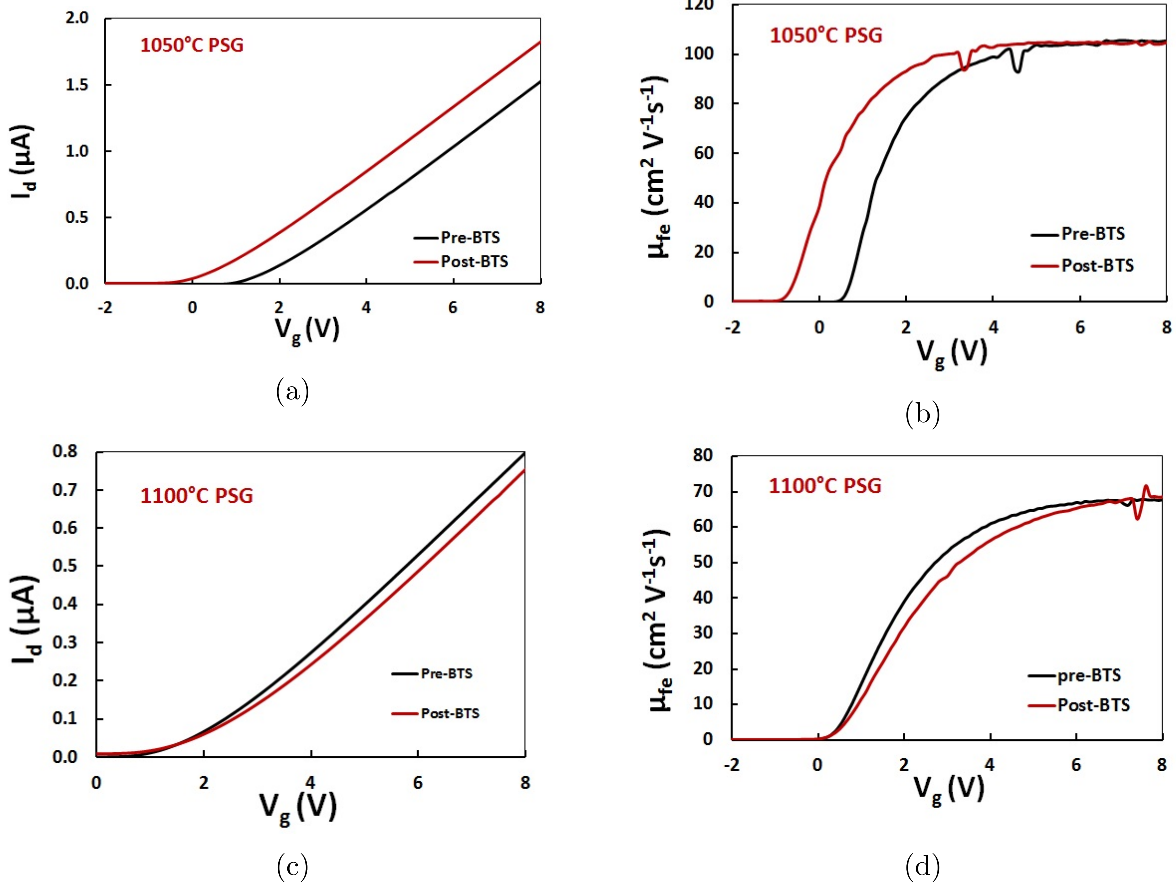


Figure 5.2: On 1050 °C PSG MOSFET, the comparison of (a) $I_D - V_G$ and (b) μ_{fe} before and after stressing with 5 minutes stressing; on 1100 °C PSG MOSFET, comparison of (c) $I_D - V_G$ and (d) μ_{fe} before and after stressing with 5 minutes stressing.

5.3 Thin PSG structure

As discussed above, the slow polarization in phospho-silicate glass jeopardizes the stability of SiC MOS devices. This polarization can be described by polarizability χ_p. Under an applied voltage, the polarizability will give rise to the slow build-up of a uniform volume polarization $\mathbf{P} = \epsilon_0 \chi_p \mathbf{E}_g$ where ϵ_0 is the permittivity of free space and $\mathbf{E}_g$ is the field in the glass layer. This slow polarization is in addition to the instantaneous polarization which is related to the dielectric constant ϵ_g. Such a volume polarization is equivalent to a surface charge on the PSG/SiC interface.

In Si MOS devices, thin PSG film is used as an upper level passivation layer to improve device behavior for it acts as a cation impurities (notably Na^+ ions) getter and a barrier against Na^+ ion drift, thereby stabilizing the device characteristics. However, due to the intrinsic polarization, the drawback to utilizing PSG films in the gate dielectric stack for stabilization is that they contribute to the shift in flat-band voltage (ΔV_{FB}) or threshold voltage (ΔV_T). For a metal/PSG/SiO_2/Si structure, the glass layer is polarized by applying a polarizing voltage V_p across the structure for a given length of time at an elevated temperature. In the C-V method, application of a dc field causes a charge-displacement in the glass. This displacement alters the surface potential of the semiconductor and the resulting flat-band voltage shift (ΔV_{FB}) can be observed in C-V characteristic after quenching to room temperature. As increasing the stressing time, the build up of polarization eventually reaches equilibrium, and leads to a voltage shift saturation ΔV_{SAT}.

E. H. Snow and B. E. Deal[4] detailedly investigated the polarization effect in the metal/PSG/SiO_2/Si structure, and derived a model to describe the saturation ΔV_{SAT}.

$$\Delta V_{SAT} = \frac{-\epsilon_{ox} t_g \chi_p V_p}{\epsilon_g[(\epsilon_g + \chi_p)t_{ox} + \epsilon_{ox} t_g]} \tag{5.4}$$

where ϵ_{ox} and t_{ox} are the dielectric constant and thickness of the SiO_2, respectively, ϵ_g and t_g the dielectric constant and thickness of glass layer. In their investigation, the dielectric constant values obtained were in the range 4.0 to 4.1 for the phosphosilicate glass, slightly higher than the SiO_2 dielectric constant values 3.75 to 3.9.

By rearranging the terms, Eq.(5.4) can be rewritten as

$$\frac{\Delta V_{SAT}}{V_p} = -\frac{t_g}{t_{ox}} \cdot \frac{\epsilon_{ox}\chi_p}{\epsilon_g[\epsilon_g + \chi_p + \epsilon_{ox}\frac{t_g}{t_{ox}}]} \tag{5.5}$$

Note that $\frac{\Delta V_{SAT}}{V_p}$ is determined by two variables, the glass layer and oxide ratio $\frac{t_g}{t_{ox}}$ and the polarizability χ_p. J. M. Eldridge *et al.*[5;6] found that χ_p is proportional to the PSG composition $N_{P_2O_5}$, $\chi_p \propto N_{P_2O_5}$ within the uncertainty of the data (in Fig.5.3). The effect

of the glass polarization on the surface potential of silicon can be virtually eliminated by reducing the P_2O_5 concentration. Fig.5.4 shows the dependence of ΔV_{SAT} per unit of applied voltage on PSG composition and relative thickness. For several compositions under 10%, the observed values of ΔV_{SAT} (normalized with respect to V_p) are seen to saturate with increasing $\frac{t_g}{t_{ox}}$. The derivation for polarization charge in metal/SiO_2/PSG/SiC structure

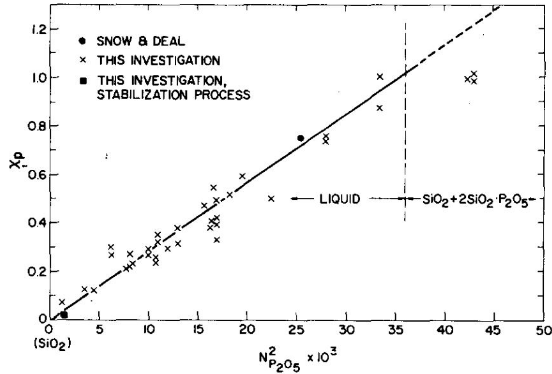


Figure 5.3: Dependence of χ_p on PSG composition.[5]

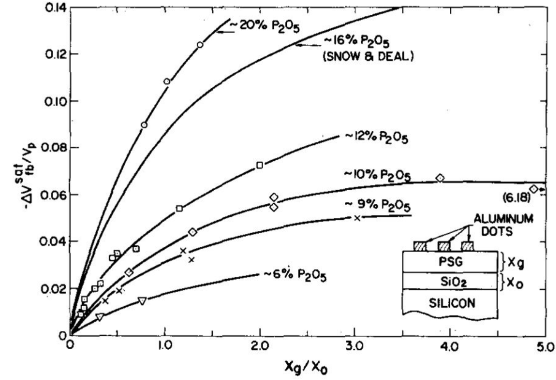
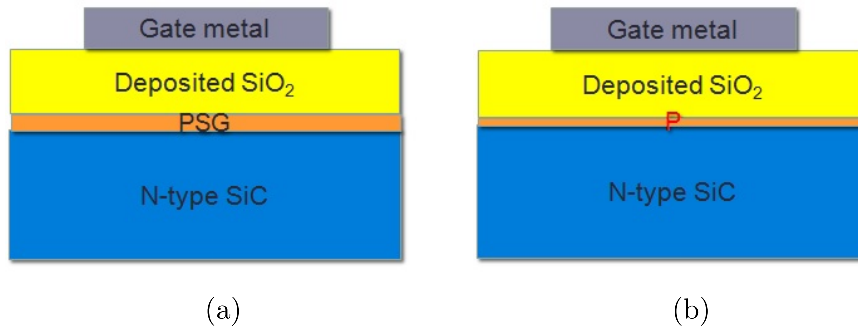


Figure 5.4: Dependence of ΔV_{SAT} per unit of applied voltage on PSG composition and relative thickness.[5]



(a) (b)

Figure 5.5: (a) Thin PSG structure. (b) PSG structure with only the unetchable ultrathin phosphorus layer.

(thin PSG structure, Fig.5.5a) is the same as Snow and Deal's model Eq.(5.4), hence it can be extended for application in SiC case. By stacking a thin PSG layer (∼10nm) and a deposited oxide (∼35nm), Y. K. Sharma *et al.*[3] demonstrated high mobility (∼70$cm^2V^{-1}s^{-1}$) with a significant improvement in threshold voltage stability.

Unlike the good quality of SiO_2/Si interface, the existence of high trap density at PSG/SiC interface gives rise to the electron trapping effect during stressing, which causes a shift of ΔV_{FB} or ΔV_T to the positive direction. The balance between polarization effect and electron trapping effect is important, as discussed above. Therefore, three factors must be considered in the device instability:

- the ratio $\frac{t_g}{t_{ox}}$
- the mole fraction $N_{P_2O_5}$ (or the polarizability χ_p)
- electron trapping

In Chapter 3 and 4, we demonstrated that different mole fraction of $N_{P_2O_5}$ in the bulk of PSG can be achieved by varying the $POCl_3$ annealing temperature, and meanwhile the interface trap density is closely related to the interfacial phosphorus incorporation. It is reasonable to assume that the electron trapping effect scales with interface trap density. Due to the intricate role of phosphorus in PSG, it is essential to investigate the stability issue of thin PSG structure with the consideration of varying the amount of phosphorus incorporation.

For this purpose, three 4H-SiC MOS capacitors were fabricated by utilizing the thin PSG structure. The dielectric stack was prepared in the steps: (1) the initial thermal oxidation for a short time, limited within 1 hour; (2) $POCl_3$ annealing at various temperature; (3) tetraethyl orthosilicate (TEOS) oxide by low pressure chemical vapor deposition (LPCVD) at 650 °C; (4) densification in N_2 ambient at 850 °C.

Because of high temperature processes after the initial oxidation, the thickness of PSG layer is likely affected by the extra oxidation during $POCl_3$ annealing, and the diffusion of P_2O_5 from PSG into SiO_2, resulting an expanded PSG layer with non-uniform phosphorus profile. Hence, to some degree the device fabrication has uncertainties hard to control. For example, consider sample#1 (1050 °C $POCl_3$ annealing), t_{ox}=50nm, t_g=20nm; sample#2 (1000 °C $POCl_3$ annealing), t_{ox}=50nm, t_g=12nm, the initial oxidation time was the same for

two samples. The difference in PSG layer thickness arises from the faster extra oxidation rate at higher $POCl_3$ annealing temperature. Moreover, following a LPCVD tube maintenance, TEOS oxide deposited on sample#3 by LPCVD was close to 100nm, even under the same operation conditions. These factors are adverse to a fine control in thin PSG structure, however, we can reach some inferences from our preliminary results.

Table 5.3: Specifications and Flat-band voltage shift (ΔV_{FB}) after certain time of bias-temperature stressing for three thin PSG samples.

sample ID	sample #1	sample #2	sample #3
PSG layer thickness (t_g)	20 nm	12 nm	-
LPCVD oxide thickness (t_{ox})	50 nm	50 nm	∼100 nm
BTS time	ΔV_{FB}(V) in sample #1	sample #2	sample #3
5m	-0.7	-0.2	2.5
1h	-3	-0.84	1.7
2h	–	-1.3	–
3h	–	–	1.22
6h	–	–	1.35
8h	–	-3.02	–

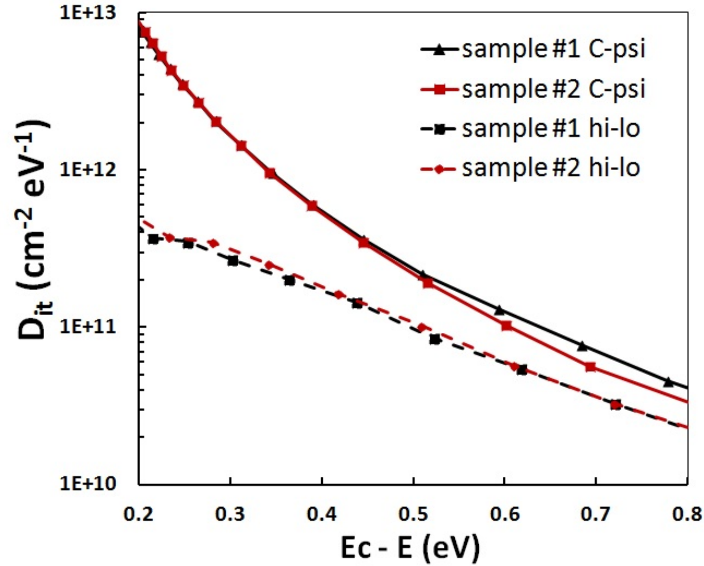
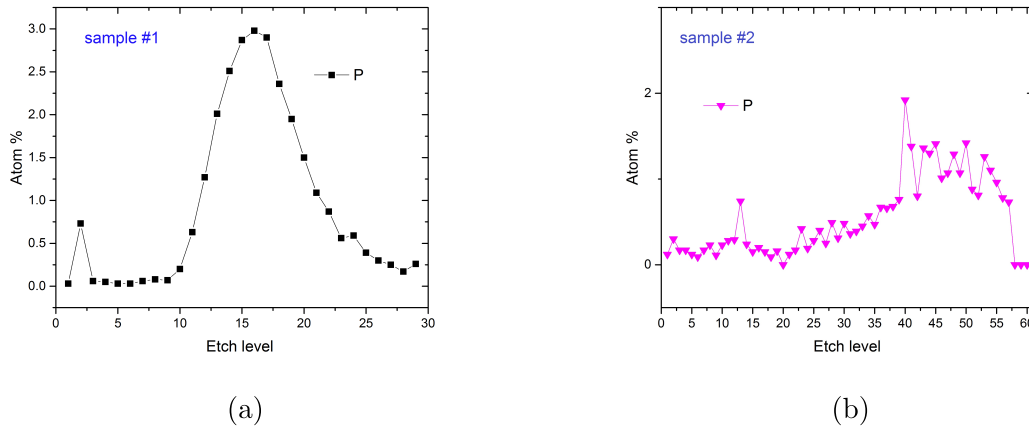


Figure 5.6: The interface trap distributions for thin PSG sample#1 and sample#2, detected by both hi-low method and C-ψ_s method.

The preliminary results of BTS instability (+1.5MV/cm @150 °C) are summarized in Table.5.3. Both sample#1 and #2 have negative flat-band voltage shifts after a certain length of time stressing. Compared to sample#1, sample#2 is relatively more stable, for instance, 1 hour stressing caused the same ΔV_{FB} in sample#1 as 8 hours stressing in sample#2, -3V. The C-V characterization (including hi-low method and C-ψ_s method) shows that these two samples have the same interface trap distribution, as shown in Fig.5.6, from which the same electron trapping effect can be assumed. The smaller polarization effect originates from a lower P_2O_5 composition in sample#2. This is confirmed by the phosphorus atomic profiles measured by XPS depth profiling with argon ion sputtering (at Rutgers Univ.). As seen in Fig.5.7, sample#2 has a P atomic peak value <2%, sample#1 peak value ∼3%.



(a) (b)

Figure 5.7: The phosphorus atomic percentage analyzed by XPS Depth Profiling with Argon Ion Sputtering for (a) sample #1 , (b) sample #2.

For sample#3, to reduce the polarization effect, before the LPCVD oxide deposition, we intentionally did additional high temperature (1000 °C) annealing in N_2 ambient for 1 hour to lose some P_2O_5 into gas phase. It turned out that more electron trapping effect (due to less interfacial phosphorus incorporation) caused the flat-band voltage shift to the right, opposite to sample#1 and #2.

Through the preliminary analysis, we can infer that the intricate control of phosphorus incorporation at the interface and in the PSG bulk is the key to a better stability. The thin PSG structure can help minimize the negative effect of the intrinsic PSG polarization.

5.4 Summary

In PSG dielectric, two competing mechanisms are identified to affect the SiC MOS devices' stability, namely polarization and electron trapping effect. The thin PSG structure is proposed to minimize the polarization effect, considering two factors, the glass/oxide thickness ratio and the polarizability χ_p which is determined by the phosphorus uptake in the PSG bulk. Preliminary results show that good device stability can be achieved by a fine control of the phosphorus incorporation in the PSG layer. To fully utilize the benefit of thin PSG structure, the ideal scenario is to etch the PSG bulk totally, only leaving an ultrathin unetchable phosphorus layer, as shown in Fig.5.5b. This ideal scenario does not introduce unnecessary polarization effect, while in the ultrathin layer, phosphorus atoms passivate the interface traps, eliminating the electron trapping effect. This way of phosphorus incorporation is in analogy with nitrogen incorporation by NO annealing. In the practical fabrication, low temperature processing methods are needed to maintain the phosphorus layer, for high temperature processes can destroy the phosphorus bonding and diffuse away the ultrathin layer. This deserves more attention in further investigations.

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Chapter 6

Conclusion and future work

6.1 Conclusion

Silicon carbide (SiC) has been recognized as a promising material for high-power devices because of its wide bandgap, high breakdown electric field and large thermal conductivity. However, the channel mobility of 4H-SiC metal-oxide-semiconductor field effect transistors (MOSFETs) fabricated by standard dry oxidation is extremely low, thus hindering the development of SiC power MOSFETs. In particular, the channel mobility of the MOSFETs on the (0001) Si-face of 4H-SiC is extremely low, and typically below $10\text{cm}^2\text{V}^{-1}\text{s}^{-1}$. The low channel mobility is attributed to the high interface trap density (D_{it}) near the conduction band edge of 4H-SiC. Although the standard NO post oxidation annealing process has commercialized the SiC power MOSFETs with mobility $\sim 35\text{cm}^2\text{V}^{-1}\text{s}^{-1}$, further improvement in channel mobility on the (0001) Si-face is required for the development of next-generation low-loss SiC MOS devices.

In this work, phosphorus diffusion into the gate oxide through $POCl_3$ annealing has been demonstrated to passivate the interface trap density more efficiently than NO annealing, resulting in a much higher mobility $>90\text{cm}^2\text{V}^{-1}\text{s}^{-1}$. A comparison of D_{it} between nitrogen and phosphorus passivated interfaces was shown through multiple electrical characterization methods. In addition to a higher D_{it} reduction by phosphorus, the mobility improvement can also be attributed to a greater counter-doping effect at the interface. The drawback to this approach is phosphorus incorporation converts the gate oxide into phospho-silicate glass (PSG), an intrinsic polar material. The polarization induced during the device operation under an applied bias and an elevated temperature endangers the device long-term reliability.

This dissertation explores the correlation between the phosphorus uptake in PSG dielectric and its effect on the electrical properties of 4H-SiC MOS devices. Based on the P_2O_5-SiO_2 phase diagram, different phosphorus uptake is achieved by varying the $POCl_3$ annealing temperature in the range of 900 °C - 1100 °C. The major findings from this study can be summarized into several points,

- The interface trap density (D_{it}), extracted from simultaneous high-low frequency CV method and C-ψ_s method, is closely related to the interfacial phosphorus coverage. As the interfacial phosphorus coverage increases, more reduction of D_{it} can be realized.

- Difference between the D_{it} measured from C-ψ_s method and high-low method shows that PSG/SiC interfaces contain "fast states" also.

- High phosphorus uptake (including interfacial coverage, the mole fraction of P_2O_5 in PSG bulk or even phosphorus diffused into SiC) leads to a larger effective positive charge, thus a smaller flat-band voltage V_{FB}.

- In general, phosphorus uptake is conducive to the improvement of mobility in MOSFETs. However, due to the difference of counter-doping effect at various $POCl_3$ annealing temperatures, the P passivation and surface counter-doping reach an optimum at 1000 °C $POCl_3$ annealing, resulting in the highest mobility $\sim$105cm^{2}V^{-1}s^{-1}.

- At high oxide field E_{ox}, two mobility limiting behaviors in temperature dependency are observed for different PSG dielectrics. In 1000 °C PSG dielectric, possibly due to a minimal interface roughness, the surface phonon scattering is limiting the high field mobility; in PSG dielectrics annealed in other temperatures, the mobility limiting factor is surface roughness scattering.

- Two competing mechanisms in PSG dielectric instability are identified, polarization and electron trapping. The mole fraction of P_2O_5 in PSG bulk scales with the polarization effect, likely due to polarizability $\chi_p \propto N_{P_2O_5}$.

In this dissertation, 6H-SiC MOS system is also investigated as it offers a way to analyze electronic properties of structure with similar chemistry but different bandgap. In 6H-SiC MOS structure, nitridation has little effect in passivating the traps near the conduction band, only eliminating the deep level traps. This study deepens our understandings by identifying that: (1) Phosphorus incorporation in 6H-SiC MOS passivates the traps both near the conduction band and in deep level; (2) "Fast states" exist in 6H-SiC MOS structure as well; (3) The total interface trap density N_{it} extracted from the C-ψ_s method is consistent with that from subthreshold slope method; (4) The correlation between N_{it} and peak mobility $\mu_{\mathrm{fe,peak}}$ is valid for both 4H-SiC and 6H-SiC.

In addition, we have suggested that by modulating three factors in thin PSG structure, a better device stability is likely to be achieved. Those three factors are the ratio $\frac{t_g}{t_{ox}}$, the mole fraction $N_{P_2O_5}$ (or the polarizability χ_p) and the electron trapping. During the device fabrication, high temperature processes induce undesired phosphorus diffusion and reduce the controllability. Preliminary results indicate that an optimal phosphorus incorporation can balance the competing polarization and electron trapping effects.

6.2 Future work

Based on the discussion in the thesis, in order to further understand the surface counter-doping role of phosphorus and make the PSG-dielectric practical, more work should be carried out, including

- Characterize the interfacial phosphorus dopants with techniques, such as scanning capacitance microscopy (SCM), for different temperature $POCl_3$ annealed PSG dielectrics
- Fabricate Hall-bar MOSFETs with PSG dielectrics and study the Hall effect. Characterize the temperature dependency for the carrier concentration and Hall mobility
- Adopt low temperature processes to make the dielectric stack for thin PSG structure, such as ALD SiO_2, ALD Al_2O_3

- The ultrathin PSG structure: Totally etch the PSG bulk, only leaving the unetchable P layer, use low temperature processes to deposit dielectric, maintaining the P interfacial atoms

- In last two suggestions, add a thin Si_3N_4 diffusion barrier layer on top of PSG to avoid the diffusion of phosphorus

- Study the combination of phosphorus and other passivating agents, such as Boron, Nitrogen, Arsenic, Antimony, etc. in 4H-SiC MOS

- Study the effect of phosphorus passivation on the carbon face of 4H-SiC.

Appendices

Appendix A

MATLAB code for C-ψ_s method

```
1 function d_out = hilo(d, varargin)
2 % HILO  Process high-low C-V data into interface trap density vs. energy
3 %
4 % Notes:
5 %   * Has not yet been tested on p-type data; should work but...
6 %
7 % Syntax
8 %
9 %   d = HILO('-v')   prints version string
10 %   d = HILO(d)      processes the given CV data with default parameters
11 %   d = HILO(d, 'param1', value1, 'param2', value2, ...)
12 %                    allows additional parameters to be specified.
13 %
14 %   d is a struct containing all the data required to perform HiLo CV
15 %   analysis. The minimum set of fields is:
16 %
17 %       d.Vg    vector   Gate voltage (V)
18 %       d.Cqs   vector   Quasi-static capacitance (F)
19 %       d.Chf   vector   HF capacitance (F)
20 %
21 %   Optional fields:
22 %
23 %       d.f     scalar   Frequency for HF capacitance measurement (Hz)
24 %       d.G     vector   Parallel model measured conductance
25 %
26 %   Other fields are ignored. All vector fields must have the same length.
27 %
28 %
29 % Allowable parameters are:
30 %
31 %   'Temperature' (default: 21 C)
32 %       Specifies the temperature at which the measurent was performed.
33 %       If specified, any existing value is overwritten. If not specified
34 %       and no existing value is present, the default value is used.
```

```
35 %
36 %    'Substrate' (default: 'SiC')
37 %        Name of the material used for the substrate. One of 'Si' or 'SiC'
38 %
39 %    'Oxide' (default: 'SiO2')
40 %        Name of the material used for the gate insulator.
41 %        One of 'SiO2' or 'Al2O3'
42 %
43 %    'Area' (default: 1.59e-3 cm^2)
44 %        The area of the measured device. Default is area of 450 um circle
45 %        If specified, any existing value is overwritten. If not specified
46 %        and no existing value is present, the default value is used.
47 %
48 %    'Frequency' (default: 100 kHz)
49 %        The frequency at which the HF capacitance data was taken.
50 %        If specified, any existing value is overwritten. If not specified
51 %        and no existing value is present, the default value is used.
52 %
53 %    'Cox'
54 %        The oxide capacitance. (default: calculated by averaging 5 data
55 %        points near the maximum in the quasi-static capacitance)
56 %        If specified, any existing value is overwritten. If not specified
57 %        and no existing value is present, the default value is used.
58 %
59 %    'Offset' (default: 0)
60 %        The offset applied to the calculated surface potential. Used to
61 %        explore the effect of arbitrary shifts in the surface potential.
62 %
63 %    'Range' (default: [])
64 %        A list of indices of the data that will be retained for analysis.
65 %        All other data in the vectors supplied in 'd' will be discarded.
66 %        An empty array [] indicates all data should be used.
67 %
68 %    'RsCorrect' (default: true)
69 %        Use the (optionally) provided conductance data (d.G) to correct
70 %        both Chf and G data for series resistance. Original data is moved
71 %        to d.Chf_raw and d.G_raw
72 %
73 %    'AdjRange' (default: [])
74 %        A list of indices of the data to use to calculate gain and offset
75 %        correction parameters. If the list is empty no offset correciton is
```

```
 76 %        performed. The listed data points should be in strong accumulation
 77 %        and/or strong depletion where Cqs and Chf should be equal. The
 78 %        adjusted Chf overwrites the existing Chf data;
 79 %        The corrected d.Chf' = A * d.Chf + B. The coeffients A and B are
 80 %        found to minimize the error term Cqs-Chf in a least-squared sense.
 81 %        If 'Range' is used in conjunction with 'AdjRange' the latter is
 82 %        corrected as needed.
 83 %
 84 %    'Debug' (default: true)
 85 %        The debug mode generates diagnostic plots and prints diagnostic
 86 %        information to the command line.
 87 %
 88 %    'Method' (default: 'Intercept')
 89 %        Selects the method that will be used to calculate the surface
 90 %        potential. Options are:
 91 %
 92 %        'FullFit'   Fits the entire 1/Cs_hf^2 dataset to the exact
 93 %                    MOS-CV model
 94 %        'Intercept' Fits the linear section of the 1/Cs_hf^2 data to a
 95 %                    linear model and forces the x-intercept to -1 kT/q
 96 %
 97 % Data added to structure by HILO:
 98 %
 99 %    The following are added only if not already present:
100 %
101 %        d.T         Measurement temperature (C)
102 %        d.area      Device area (cm^2)
103 %        d.f         Frequency used during HF capacitance measurement (Hz)
104 %
105 %    The following are added from the parameters given on the command line:
106 %
107 %        d.offset    The arbitrary offset added to the internally determined
108 %                    surface potential (in normalized units: kT/q)
109 %
110 %    The following are added during the analysis
111 %
112 %        d.Rs        Series resistance
113 %        d.Cox       Oxide capacitance (if not specified on command line)
114 %        d.invCsq    1/Chf^2 normalized to area (cm^4/F^2)
115 %        d.Nd        Donor concentration as extracted from 1/Chf^2 vs Vg
116 %        d.Na        Acceptor concentration as extracted from 1/Chf^2 vs Vg
```

```
117 %         d.w          Depth associated with extracted doping profile (cm)
118 %         d.doping     Doping profile (- for n-type, + for p-type) (cm^-3)
119 %         d.Ef_Ei      Bulk Ef-Ei (eV) i.e. doping parameter (-kT/q * Uf)
120 %         d.Lde        Extrinsic Debye length (cm)
121 %         d.Cs_fb      Semiconductor capacitance at flatband (F)
122 %         d.Cs_hf      HF semiconductor capacitance (F)
123 %         d.Cs_qs      QS semiconductor capacitance (F)
124 %         d.phi_s      Surface potential (V)
125 %         d.Ec_Ef      Ec-Ef at surface (trap position relative to Ec) (eV)
126 %         d.Vfb        Flatband voltage (V)
127 %         d.Cfb        Flatband capacitance (V)
128 %         d.Ecb_Ef     Flatband energy (on Ec-Ef scale used for Dit)
129 %         d.Cs_ideal   Ideal semiconductor depletion capacitance (F)
130 %         d.Chf_ideal  Ideal HF capacitance (F)
131 %         d.Cfb_ideal  Ideal flatband capacitance (F)
132 %         d.Dit_hilo   Dit by traditional Hi-Lo technique (cm^-2 eV^-1)
133 %         d.Dit_Cpsi   Dit by C-psi technique (cm^-2 eV^-1)
134 %         d.Nit_hilo   Nit (Hi-Lo Dit integrated over Ec-Ef) midgap to flatband
135 %         d.Nit_Cpsi   Nit (C-psi Dit integrated over Ec-Ef) midgap to flatband
136 %
137 % References:
138 %
139 %   C. N. Berglund, ?Surface states at steam-grown silicon-silicon dioxide
140 %         interfaces,? Electron Devices, IEEE Transactions on, vol. 13,
141 %         no. 10, pp. 701?705, 1966.
142 %
143 %         J. R. Brews, ?Correcting interface-state errors in MOS doping profile
144 %         determinations,? Journal of Applied Physics, vol. 44, no. 7,
145 %         pp. 3228?3231, 1973.
146 %
147 %   H. Yoshioka, T. Nakamura, and T. Kimoto, ?Accurate evaluation of
148 %         interface state density in SiC metal-oxide-semiconductor structures
149 %         using surface potential based on depletion capacitance,?
150 %         Journal of Applied Physics, vol. 111, no. 1, pp. 014502 1?5, 2012.
151 %
152 % Copyright (c) 2013 Dallas T. Morisette (morisett@purdue.edu).
153 % Released under the terms of the FreeBSD License.
154 % See LICENSE file for details.
155 %
156
157     version = 'hilo: v1.1.0; common: v1.2.0';
```

```
158
159     ip = inputParser;
160     ip.addRequired('d', @(x)isstruct(x) || ischar(x));
161     ip.addParamValue('Temperature',     -1, @isscalar);
162     ip.addParamValue('Substrate',    'SiC'           );
163     ip.addParamValue('Oxide',        'SiO2'          );
164     ip.addParamValue('Area',            -1, @isscalar);
165     ip.addParamValue('Frequency',       -1, @isscalar);
166     ip.addParamValue('Cox',             -1, @isscalar);
167     ip.addParamValue('Offset',           0, @isscalar);
168     ip.addParamValue('Range',           [], @isvector);
169     ip.addParamValue('RsCorrect',     true           );
170     ip.addParamValue('AdjRange',        [], @isvector);
171     ip.addParamValue('Debug',         true           );
172     ip.addParamValue('Method','Intercept'            );
173
174     ip.parse(d, varargin{:});
175
176     if ischar(d)
177         switch d
178             case {'-v', '--version'}
179                 disp(version);
180             otherwise
181                 disp(['Unknown option: ' d]);
182         end
183         return;
184     end
185
186     debug = ip.Results.Debug;
187     method = lower(ip.Results.Method);
188
189     VerifyLengths(d);
190     nFig = 1;
191
192     % If the 'Temperature' parameter is specified, override any existing
193     % value in d.T. If not specified, and if d.T does not exist, set
194     % to default of 21 C
195
196     if ip.Results.Temperature ~= -1
197         d.T = ip.Results.Temperature;
198     elseif ~isfield(d, 'T')
```

```
199         d.T = 21;
200     end
201 
202     % Get fundamental physical constants and material properties
203     c  = GetConstants(d.T);
204     s  = GetMaterial(ip.Results.Substrate, d.T);
205 
206     % If the 'Area' parameter is specified, override any existing
207     % value in d.area. If not specified, and if d.area does not exist, set
208     % to default of 1.59e-3 cm^2 (area of 450um diameter circle)
209 
210     if ip.Results.Area ~= -1
211         d.area = ip.Results.Area;
212     elseif ~isfield(d, 'area');
213         d.area = ((450e-4)^2)*pi/4;
214     end
215 
216     % If the 'Frequency' parameter is specified, override any existing
217     % value in d.f. If not specified, and if d.f does not exist, set
218     % to default of 100e3 (100 kHz)
219 
220     if ip.Results.Frequency ~= -1
221         d.f = ip.Results.Frequency;
222     elseif ~isfield(d, 'f');
223         d.f = 100e3;
224     end
225 
226     d.offset = ip.Results.Offset;
227 
228     cropRange = ip.Results.Range;
229     adjustRange = ip.Results.AdjRange;
230 
231     % If a range is supplied, crop data to range
232     if ~isempty(cropRange)
233         n = length(d.Vg);
234         mask1 = ismember(1:n,cropRange);
235         d = CropRange(d, cropRange);
236         if ~isempty(adjustRange)
237             mask2 = ismember(1:n,adjustRange);
238             mask = mask1 & mask2;
239             adjustRange = find(mask(cropRange));
```

```
240         end
241     end
242
243     % If the 'Cox' parameter is specified, override any existing value in
244     % d.Cox. If not specified, and if d.Cox does not exist, calculate based
245     % on the average of 5 points in strong accumulation.
246
247     if ip.Results.Cox > 0
248         d.Cox = ip.Results.Cox;
249     elseif ~isfield(d, 'Cox');
250         d.Cox = FindCox(d.Cqs, 5);
251     end
252     if debug
253         fprintf('Cox = %.3f pF\n', d.Cox*1e12);
254     end
255
256     % If RsCorrect was requested, extract Rs and correct d.Chf and d.G
257     % Saves old Chf and G data in d.Chf_raw and d.G_raw, respectively
258     % Will only be performed if d.Chf_raw does not exist, since running
259     % the correction more than once would corrupt the raw data and would
260     % not improve the correction (extracted Rs should be close to zero if
261     % the correction has already been performed).
262
263     if ip.Results.RsCorrect && ~isfield(d, 'Chf_raw')
264         d.Chf_raw = d.Chf;
265         d.G_raw    = d.G;
266
267         d.Rs = FindRs(d.Chf, d.G, d.f, 5);
268
269         den = (d.G*d.Rs - 1).^2 + (2*pi*d.f*d.Chf*d.Rs).^2;
270         d.Chf = d.Chf./den;
271         d.G = (d.G - d.Rs*d.G.^2 - d.Rs*(2*pi*d.f*d.Chf).^2)./den;
272         if (debug)
273             fprintf('Rs = %.2f ohms\n', d.Rs);
274         end
275     end
276
277     % Perform gain/offset correction
278     % Chf' = A * Chf + B
279     if ~isempty(adjustRange)
280         pf = [d.Chf(adjustRange) ones(length(d.Chf(adjustRange)),1)]\d.Cqs(adjustRange);
```

```
281         d.Chf = d.Chf*pf(1)+pf(2);
282     end
283
284     % Extract doping using slope of linear fit of 1/Chf^2 vs Vg plot
285     d.invCsq = 1./(d.Chf/d.area).^2;
286     [pf, rng] = FindLinearFit(d.Vg, d.invCsq, 5);
287     doping = 2/(c.q*c.eps0*s.k*pf(1));
288     if doping < 0
289         d.Nd = -doping;
290         d.Na = 0;
291         d.type = 'n';
292     else
293         d.Na = doping;
294         d.Nd = 0;
295         d.type = 'p';
296     end
297
298
299     % Calculate doping profile
300     % J. R. Brews, J. of Appl. Phys., vol. 44, no. 7, pp. 3228-3231, 1973.
301     d.w = s.k*c.eps0*d.area*(1./d.Chf - 1/d.Cox);
302     d.doping = 2/(c.q*s.k*c.eps0)*(1-d.Cqs/d.Cox)./(1-d.Chf/d.Cox) ./ ...
303                 dydx(d.Vg,d.invCsq,11);
304
305     if debug
306         figure(nFig);
307         nFig = nFig + 1;
308         if d.type == 'n'
309             x = linspace(min(d.Vg),-pf(2)/pf(1));
310         else
311             x = linspace(-pf(2)/pf(1), max(d.Vg));
312         end
313         plot(d.Vg, d.invCsq, 'ob', ...
314              d.Vg(rng), d.invCsq(rng), 'og', ...
315              x, polyval(pf,x), 'r');
316         xlabel('Gate Voltage (V)');
317         ylabel('1/C_{HF}^2 (cm^4/F^2)');
318         grid on;
319
320         if d.type == 'n'
321             str = 'Nd';
```

```
322         else
323             str = 'Na';
324         end
325         fprintf('%s = %.3e cm^-3\n', str, abs(doping));
326
327         figure(nFig);
328         nFig = nFig + 1;
329         semilogy(d.w*1e7, abs(d.doping));
330         xlabel('Depth (nm)');
331         if d.type == 'n'
332             str = 'Donor';
333         else
334             str = 'Acceptor';
335         end
336         ylabel(sprintf('%s Concentration (cm^{-3})', str));
337         grid on;
338     end
339
340     % Flatband capacitance and voltage
341     Uf = -fzero(@(u)exp(-u) - exp(u) + (d.Nd - d.Na)/s.ni, 0);
342     d.Ef_Ei = -c.kT*Uf;
343     nb = s.ni*exp( d.Ef_Ei/c.kT);
344     pb = s.ni*exp(-d.Ef_Ei/c.kT);
345     d.Lde = sqrt(s.k*c.eps0*c.kTq/(c.q*(pb+nb)));
346     d.Cs_fb = s.k*c.eps0/d.Lde*d.area;
347
348     % Surface potential
349     d.Cs_hf = d.Chf*d.Cox./(d.Cox-d.Chf);
350     d.Cs_qs = d.Cqs*d.Cox./(d.Cox-d.Cqs);
351     d.phi_s = cumtrapz(d.Vg,1-d.Cqs/d.Cox);
352
353     switch method
354         case 'fullfit'
355             Us = d.phi_s/c.kTq;
356             options = optimset('Display', 'off', 'TolX',1e-7);
357             dU = fminbnd(@(dU)rms((d.Cs_fb./d.Cs_hf).^2 - 1./(CdNorm(Us-dU,Uf)).^2), ...
358                          -5,5, options);
359         case 'intercept'
360             [pf, ~] = FindLinearFit(d.phi_s/c.kTq, 1./(d.Cs_hf).^2, 5);
361             dU = -pf(2)/pf(1) + 1;
362
```

```
363         otherwise
364             dU = 0;
365     end
366     d.phi_s = d.phi_s - dU*c.kTq + d.offset*c.kTq;
367     d.Ec_Ef = s.Ec_Ei - d.Ef_Ei - d.phi_s;
368
369     if debug
370         invCssq = 1./(d.Cs_hf).^2;
371         [pf, rng] = FindLinearFit(d.phi_s, invCssq, 5);
372         figure(nFig);
373         nFig = nFig + 1;
374         if d.type == 'n'
375             x = linspace(min(d.phi_s), -pf(2)/pf(1));
376         else
377             x = linspace(-pf(2)/pf(1), max(d.phi_s));
378         end
379         plot(d.phi_s/c.kTq, invCssq, 'ob', ...
380              d.phi_s(rng)/c.kTq, invCssq(rng), 'og', ...
381              x/c.kTq, polyval(pf,x), 'r');
382         xlabel('Surface Potential (kT/q)');
383         ylabel('1/C_{SHF}^2 (cm^4/F^2)');
384         grid on;
385     end
386
387     try
388         % Flatband voltage interpolation
389         index = find(abs(diff(sign(d.phi_s)))==2);
390         rng = index-5:index+5;
391         d.Vfb = interp1(d.phi_s(rng),d.Vg(rng), 0);
392
393         % Flatband capacitance interpolation
394         index = find(abs(diff(sign(d.Vg-d.Vfb)))==2);
395         rng = index-5:index+5;
396         d.Cfb = interp1(d.Vg(rng),d.Chf(rng),d.Vfb);
397
398         if debug
399             fprintf('Vfb = %.2f V\n', d.Vfb);
400         end
401     catch err
402     end
403
```

```
404    % Flatband location on energy scale
405    d.Ecb_Ef = s.Ec_Ei-d.Ef_Ei;
406    if debug
407        fprintf('Ec-Ef (flatband) = %.3f eV\n', d.Ecb_Ef);
408    end
409
410    % Ideal capacitances (Cs, Chf, Cfb)
411    d.Cs_ideal = d.Cs_fb*CdNorm(d.phi_s/c.kTq,Uf);
412    d.Chf_ideal = d.Cox*d.Cs_ideal./(d.Cox+d.Cs_ideal);
413    d.Cfb_ideal = d.Cox*d.Cs_fb/(d.Cox + d.Cs_fb);
414
415    % Calculate Dit by Hi-Lo and C-psi
416    d.Dit_hilo = (d.Cs_qs - d.Cs_hf    )/d.area/c.q;
417    d.Dit_Cpsi = (d.Cs_qs - d.Cs_ideal)/d.area/c.q;
418
419    % Calculate Nit. Ignores data from flatband to majority band edge.
420    % Data in the near band edge region is likely unreliable, but as a
421    % result the calculated Nit is underestimated.
422
423    if (d.type == 'n')
424        rng = find(d.Ec_Ef >= d.Ecb_Ef & d.Ec_Ef < s.Eg/2);
425    else
426        rng = find(d.Ec_Ef <= s.Eg - d.Ecb_Ef & d.Ec_Ef > s.Eg/2);
427    end
428    d.Nit_hilo = trapz(d.Ec_Ef(rng),d.Dit_hilo(rng));
429    d.Nit_Cpsi = trapz(d.Ec_Ef(rng),d.Dit_Cpsi(rng));
430
431    if debug
432        figure(nFig);
433        nFig = nFig + 1;
434        semilogy(d.Ec_Ef, [d.Dit_hilo d.Dit_Cpsi],'.');
435        xlabel('Trap Energy (E_c - E_t, eV)');
436        ylabel('Interface Trap Density (cm^{-2} eV^{-1})');
437        ylim([1e10 10^(ceil(log10(max([d.Dit_hilo; d.Dit_Cpsi]))))]);
438        grid on;
439        hold on;
440        semilogy(d.Ecb_Ef*[1 1],ylim,'r--');
441        hold off;
442
443        figure(nFig);
444        nFig = nFig + 1;
```

```
445         semilogy(d.phi_s/c.kTq, [d.Cs_qs d.Cs_hf d.Cs_ideal]);
446         xlabel('Surface Potential (kTq)')
447         ylabel('Semiconductor Capacitance (F)');
448         if d.type == 'n'
449             xlim([-s.Eg*0.4 d.Ecb_Ef]/c.kT);
450         else
451             xlim([d.Ecb_Ef -s.Eg*0.4]/c.kT);
452         end
453         grid on;
454 
455         figure(nFig);
456         nFig = nFig + 1;
457         plot(d.Vg, [d.Cqs d.Chf d.Chf_ideal]*1e12, ...
458              d.Vg, d.Cox*ones(size(d.Vg))*1e12,'k--');
459         if isfield(d,'Vfb')
460              hold on;
461              plot(d.Vfb, d.Cfb*1e12, '.g');
462              hold off;
463         end
464         xlabel('Gate Voltage (V)');
465         ylabel('Capacitance (pF)');
466         grid on;
467 
468         fprintf('Nit (HiLo) = %.2e cm^-2\n', d.Nit_hilo);
469         fprintf('Nit (Cpsi) = %.2e cm^-2\n', d.Nit_Cpsi);
470     end
471 
472     d_out = d;
473 end
474 
475 function rng = FindAccumulation(C,n)
476 % FINDACCUMULATION(C,n)  Finds n points around the maximum of a smoothed
477 %   version of the given capacitance data. Selected points are biased
478 %   towards the nearest end of the data set. Used to locate the area of
479 %   strong accumulation to extract Rs and Cox
480 
481     % Idiot check - make sure n is not greater than length of data set
482     if length(C) < n
483         n = length(C);
484     end
485 
```

```
486     % Smooth given data and locate maximum
487     C = smooth(C);
488     i = find(C == max(C));
489     i = i(1);
490
491     % Select data points to average
492     m = length(C);
493     if i < m/2           % max in low end of data set
494         if i <= n
495             rng = 1:n;
496         else
497             rng = (i-n+1):i;
498         end
499     else                         % max in high end of data set
500         if i > m-n
501             rng = (m-n+1):m;
502         else
503             rng = i:(i+n-1);
504         end
505     end
506 end
507
508 function Cox = FindCox(C,n)
509     rng = FindAccumulation(C,n);
510     Cox = mean(C(rng))*1.001; % Add 0.1% to eliminate NaN errors
511 end
512
513 function Rs = FindRs(C,G,f,n)
514     rng = FindAccumulation(C,n);
515     w2 = (2*pi*f)^2;
516     Rs = G./(w2*C.^2 + G.^2);
517     Rs = mean(Rs(rng));
518 end
519
520 function d = CropRange(d,rng)
521 % CROPRANGE(d,rng) Crop all vectors in the struct d to the given range rng
522 %
523     fields = fieldnames(d);
524     for i = 1:length(fields)
525         field = fields{i};
526         tmp = d.(field);
```

```
527             if isvector(tmp) && ~isscalar(tmp) && isnumeric(tmp)
528                 d.(field) = tmp(rng);
529             end
530         end
531 end
532 
533 function VerifyLengths(d)
534 % VERIFYLENGTHS(d)  Ensure that all numeric vectors are the same length
535 % in the given structure d
536 %
537     n = 0;
538     fields = fieldnames(d);
539     for i = 1:length(fields);
540         tmp = d.(fields{i});
541         if isvector(tmp) && ~isscalar(tmp) && isnumeric(tmp)
542             if n == 0
543                 n = length(tmp);
544             else
545                 assert(n == length(tmp), 'All vectors must be the same length');
546             end
547         end
548     end
549 end
550 
551 function C = CdNorm(Us,Uf)
552 % CDNORM  Calculate the normalized depletion capacitance from
553 % the surface potential Us and doping parameter Uf.
554 % The normalization constant is the flatband semiconductor capacitance
555 %
556 % Uf = (Ei(bulk) - Ef)/kT = { ln(ni/ND) n-type or ln(NA/ni) p-type }
557 % Us = (Ei(bulk) - Ei(surface))/kT
558 %
559     if Uf < 0   % n-type
560         C =  sign(Us).*(exp( Us)-1)./sqrt(2*(exp( Us)-Us-1));
561     else        % p-type
562         C = -sign(Us).*(exp(-Us)-1)./sqrt(2*(exp(-Us)+Us-1));
563     end
564 end
```

Appendix B

Device processing

B.1 Sample cleaning process

1. Use a cotton swab and acetone to remove the glue on SiC sample surface. The next set of steps removes organic compounds on sample surface.

2. After surface appears clean by inspection with microscope, place sample in a beaker of acetone and place in the ultrasonic system for 5 min.

3. Remove sample and place in trichloroethylene (TCE) beaker in ultrasonic cleaner for 5 min.

4. Remove sample and place in acetone beaker in ultrasonic cleaner for 5 min.

5. Remove sample and place in methanol beaker in ultrasonic cleaner for 5 min.

6. Remove sample and place in a second methanol beaker in ultrasonic cleaner for 5min.

7. Remove sample and place in deionized water (DI water) beaker in ultrasonic cleaner for 5min.

8. Remove sample and place in buffered oxide etch (BOE) for 5min.

9. Rinse sample in DI water.

The next set of steps removes inorganic compounds on sample surface.

10. Mix a solution of 1:1 H_2SO_4:H_2O_2 and place sample in solution for 15min.

11. Rinse sample in DI water, then place sample in BOE for 2min.

12. Mix a solution of 3.5:1:1 DI water:H_2O_2:NH_4OH and heat to 100-115 °C.

13. Rinse sample in DI water and place in solution for 15 min.

14. Rinse sample in DI water and place in BOE for 2 min.

15. Mix a solution of 3.5:1:1 DI water:H_2O_2:HCl and heat to 100-115 °C.

16. Rinse sample in DI water and place in solution for 15 min.
17. Rinse sample in DI water and place in BOE for 2 min.
18. Rinse sample and dry with N_2 air gun.

B.2 Sample oxidation

1. Vacuum oxidation furnace tube until base pressure is less than 1 torr.
2. Prepare argon tank and fill oxidation furnace tube to atmospheric pressure.
3. Flush oxidation furnace tube with argon for 10-15 min to remove residual gases.
4. Load samples into oxidation furnace tube.
5. Vacuum oxidation furnace tube for 10-15 min.
6. When pressure is less than 1 torr, fill and flush with argon for 10-15 min.
7. Set oxidation furnace temperature to 1150 °C and the ramp rate to 5 °C/min.
8. When temperature is at 1150 °C, stop argon flow and begin oxygen flow at 750 sccm.
9. Record the start time.
10. Let oxidation run for the desired time.
11. Record finish time.
12. Stop oxygen flow and begin argon flow.
13. Let sample anneal in argon for 30 min post oxidation.

Steps 14-22 are for NO passivation. If no NO passivation necessary, skip to step 23.

14. Increase temperature to 1175 °C.
15. Flow argon through NO lines.
16. Begin NO flow and turn off argon flow.
17. Set NO regulator to 30 psi.
18. Flow NO at 575 sccm and anneal for 2h.
19. After anneal is finished, stop NO.
20. Let NO pressure drop to zero, and then flush NO lines with argon.
21. Stop argon flow in NO lines and vacuum NO lines until pressure is zero.

22. Stop vacuum of NO lines.

23. Set oxidation furnace temperature ramp rate to 10 °C/min and ramp temperature down to oxidation furnace base temperature.

24. Remove samples from oxidation furnace tube.

B.3 $POCl_3$ annealing

1. Turn on the chiller, cool down the $POCl_3$ to 15 °C.

2. Flow the additional N_2, open the exhaust valve.

3. Load the sample.

4. Close the exhaust valve and the all gas inlets.

5. Turn on the mechanical pump.

6. Refill N_2 gas into the furnace tube; once the inner pressure reaches 1 atm, open the exhaust valve.

7. Set the furnace program and start ramping temperature.

8. When the temperature ramps to the targeted number, open the O_2 tank and O_2 inlet, open carrier N_2 through $POCl_3$ tank.

9. Timing 15 min.

10. After 15 min, close the carrier N_2 and O_2 inlet.

11. Flow the additional N_2 inlet for another 30 min.

12. Wait the program to cool down the furnace to 750 °C.

13. Take out the sample, and close the exhaust valve, vacuum, then refill the gas to 1 atm.

14. Close all gas valves and gas tanks.

B.4 Mask aligner and spinner procedure

1. Place a drop of 5214E photoresist glue on the silicon wafer.

2. Attach sample to the wafer and put it in a 105 °C oven. Do not let the oven temperature exceed 110 °C.

3. Cook sample for 10 min in oven.

4. Begin mask aligner start-up procedure.

5. Remove wafer from oven.

6. Start spinner.

7. Put water in center of spinner.

8. Use a pipet with a disposable tip to cover sample with 5214E photoresist.

9. Run spinner for 30 sec at 4000 RPM.

10. Place wafer in oven for 1min. Do not exceed 1min or 105 °C.

11. Remove wafer.

12. Place wafer in mask aligner and adjust mask for appropriate pattern.

13. Expose sample to UV lamp for 30 sec.

14. Remove wafer and place in a 1:4 ratio of AZ 400:H_2O for 10 sec and then quickly put it under running DI water.

15. The pattern should be visible when viewed under a microscope. If it is not, repeat step 14 for a few seconds.

16. When the pattern is clearly visible, check it under the microscope. If all of the lines are sharp, the pattern has been properly set.

B.5 Sputter system procedure

1. Load samples into sputter system.

2. Put correct metal targets on sputter guns.

3. Close sputter system and vacuum pressure to 10-7 torr or less.

4. Flow Ultra High Pure Argon through sputter system, adjusting pressure to 18 mtorr.

5. Flow Ar gas for 3 min.

6. Adjust voltage and current to appropriate settings for the selected metal target.

7. Pre-sputter for 2 min on dummy sample.

8. Sputter metal onto sample for appropriate length of time.

9. Stop argon flow.

10. Allow vacuum pump to empty chamber.

11. Stop vacuum pump and fill chamber to atmospheric pressure with nitrogen.

12. Remove samples.

13. Complete any necessary steps to return sputter system to stand-by mode.

B.6 Reactive ion etch procedure

1. Open glass window of etcher.

2. Remove blank Si wafer.

3. Place and center sample on electrode.

4. Use large tweezers to press down on wafer to ensure it is securely in place.

5. Close the glass window and tighten until snug.

6. Vacuum system for 20-30 min or until system reaches base pressure (9-10 mtorr).

7. Open all valves to etch gas line and turn on the appropriate switch on the flow controller.

8. Turn on cooling water and open all water valves to system.

9. Turn on RF power supply.

10. Adjust power setting to about three (3) watts higher than the desired power.

11. Once the pressure has stabilized, turn on power supply.

12. If necessary, adjust power to appropriate level and adjust matching network to obtain the lowest possible reflected power.

13. After desired etch time, turn off the RF power.

14. Turn off the etchant gas and allow system to vacuum to base pressure.

15. If no other etching is required, close all valves and turn off system.

16. Fill etchant chamber to atmospheric pressure with nitrogen.

17. Remove the wafer with the sample and replace it with the blank Si wafer.

B.7 Ohmic anneal furnace procedure

1. Flow argon through Ohmic anneal furnace tube until atmospheric pressure is reached.
2. Adjust argon flow rate to 8 L/min.
3. Open loading area and load samples.
4. Close loading area.
5. Flush Ohmic anneal system with argon for 5min.
6. Stop argon flow and vacuum Ohmic anneal furnace tube until 10-7 torr.
7. Stop vacuuming and flush system with argon for 5min at 12 L/min.
8. Insert samples into furnace and start 30 sec timer once sample temperature reaches 850 °C.
9. After 30 sec annealing is finished, transfer samples from furnace to loading area.
10. Remove samples from system.
11. Complete any necessary steps to return Ohmic anneal system to stand-by mode.