Reconfigurable Software-Defined Radio
—System Analyses, Architecture Designs, and Circuit Implementations

by

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Abstract

Researchers have assessed the uses of Software-defined radio (SDR) for more than thirty years. They have specifically investigated its advantages in ultimate reconfigurability and programmability to support multi-standard, multi-mode, multi-channel and multi-user applications. In recent decades, there has been renewed interest in SDR, with many new developments and breakthroughs on key enabling technologies used with SDR. Moreover, the demand for a practical SDR implementation has increased greatly due to heightened demand for multi-standard, multi-mode, multi-channel and multi-user applications. We are now witnessing a revolution in the transformation from traditional radio architecture to SDR-based radio designs.

This dissertation investigates the systematic challenges and overall development of the enabling technologies for SDR. First, a practical SDR architecture is derived from the classic SDR architecture. Then, the research focuses on important aspects of SDR systems, including (i) system level performance analyses on the impact of local oscillator (LO) imperfections; (ii) data converter designs and challenges for SDR with an exemplary DAC design; (iii) a novel SDR reconfigurable analog filter design; and (iv) a complete SDR digital front-end design with few key building block designs. This dissertation ultimately seeks to develop detailed theoretical analyses as well as practical circuit designs. Simulation results and test results are presented and discussed with detail.

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Lastly, this dissertation is dedicated to my family, including my wife Jiang Yu, my father ZhaoWu Chen, my mother YuanQiu Liao, my grandfather BoYa Liao, my late grandmother ZeYu Tang, and my two lovely children. I could not have achieved this without their love.

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List of Abbreviations and Acronyms

3G	Third-generation
ASIC	Application-specific integrated circuit
ADC	Analog to digital converter
AGC	Automatic gain control
AWGN	Additive white Gaussian noise
BAW	Bulk acoustic wave
BiCMOS	BJT and the CMOS transistor
BPF	Band pass filter
BJT	Bipolar junction transistor
BOM	Bill of material
CDC	Clock domain crossing
CDMA	Code division multiple access
CIC	Cascaded integrator–comb (filter)
CMOS	Complementary metal–oxide–semiconductor
CPU	Central processing unit
DAC	Digital to analog converter
DC	Direct current
DNL	Differential non-linearity
DPD	Digital pre-distortion
DSP	Digital signal processor/processing

DVB	Digital video broadcasting
EVM	Error vector magnitude
ENOB	Effective number of bit
FIR	Finite-duration impulse response (filter)
FOM	Figure-of-merit
GPS	Global Positioning System
GSM	Global System for Mobile
HBT	Heterojunction bipolar transistor
HPF	High pass filter
IF	Intermediate frequency
INL	Integral non-linearity
IoT/E	Internet of things/everything
LIF	Low intermediate frequency
LO	Local oscillator
LPF	Low pass filter
LSB	Least significant bit
LTE	Long term evolution (3GPP 4G technology)
IEEE	Institute of Electrical and Electronics Engineers
MIMO	Multiple-input and multiple-output
MSB	Most significant bit
NASA	National Aeronautics and Space Administration
NCO	Numerically controlled oscillator
NFET	Negative channel field effect transistor

NMOS	Negative-channel metal oxide semiconductor
NPN	Negative-positive-negative (transistor)
OFDM	Orthogonal frequency division multiplexing
PDF	Probability density function
PLL	Phase lock loop
PFET	Positive channel field effect transistor
PMOS	Positive-channel metal oxide semiconductor
PNP	Positive-negative-positive (transistor)
PSD	power spectrum density
QAM	Quadrature amplitude modulation
QPSK	Quadrature phase-shift keying
RC	Resistor-capacitor
RF	Radio frequency
RFIC	Radio frequency integrated circuit
RHBD	Radiation hardening by design
Rx	Receiver
SDR	Software-defined radio
SER	Symbol error rate
SFDR	Spurious Free Dynamic Range
SNR	Signal-to-noise ratio
SoC	System-on-chip
SiGe	Silicon Germanium
SAW	Surface acoustic wave

Tx	Transmitter
TR	Transceiver
UMTS	Universal Mobile Telecommunications System
UWB	Ultra-wideband
UWT	Ultra-wide temperature
VCO	Voltage controlled oscillator
WiFi	Wireless Fidelity
WLAN	Wireless local area network
WPAN	Wireless personal area network
ZIF	Zero intermediate frequency

Chapter 1 Introduction

1.1 Background and Motivation

The concept of software-defined radio (SDR, software radio) was first conceived in the 1970s during the research of cognitive radio systems. The term "software radio" was coined by E-Systems Corporation in 1984. In the 1990s, Mitola [14] published a groundbreaking paper that redefined the concept of SDR and discussed the architecture and the key design challenges for an SDR system. Researchers have conducted further inquiry on this topic [15]. Today, SDR represents the next stage of the revolutionary development of radio systems following the heretofore migration from analog to digital that started in the 1980s and continued into the 1990s.

In recent years, SDR has evolved from a theoretical research topic with only conceptual development and prototype designs, to an idea with more tangible commercial applications. The development of multiple technologies has enabled this transition. Among the most important enabling technologies for SDR are the digital signal processors (DSP) and general-purpose central processing units (CPU), which have significantly reduced the cost and exponentially improved performance in accordance with Moore's Law since the 1960s. During the last decade, the DSP/CPU development crossed a major threshold. The baseband signal processing and modulation of many commercial applications can now be fully implemented into software run by either DSP or CPU. A system with this implementation is considered to be SDR.

Data converters, which have improved steadily in recent decades [16], are another key enabling SDR technology. The performance figure-of-merit (FOM) of ADCs has also improved exponentially in recent couple of decades [21]. Consequently, the boundary between analog and digital domains in a radio system is pushed increasingly closer to the antenna. Progressively, more functions that used to be implemented in the analog intermediate frequency (IF) domain, or even in radio frequency (RF) domain, can now be realized using digital circuitries with software programmability.

Since the 1990s, most radio systems, especially mobile, WLAN, WPAN and satellite positioning systems, have rapidly increased in quality, capacity, functional versatility, and number of users. Multiple standards are defined for mobile systems. The second generation's cellular standards include GSM and CDMA1x. The third generation cellular standards include WCDMA, CDMA2000 and TDSCDMA. In addition, the fourth generation's cellular standards include FDD-LTE, Mobile WiMax and TDD-LTE. Multiple standards are currently under development for the fifth generation's cellular system. Similarly, there are many different standards for WLAN, WPAN and satellite positioning systems.

Also since the 1990s, the cell phone has become by far the world's most frequently used and deployed radio system. Premier smartphones accommodate most standards for mobile, WLAN, WPAN and satellite positioning systems. Consequently, SDR has been increasingly implemented in smartphones due to its reconfigurability and programmability for multi-standard, multi-mode, multi-channel and multi-user applications.

Key technologies for SDR will keep improving and evolving. Besides the steadily growing mobile phone industry, many new systems are being developed, including internet of

things/everything (IoT/E), smart cars, autonomous-driving vehicles, virtual reality and augmented reality systems. All of these new systems require multi-standard, multi-mode connectivity characteristic to SDR. Consequently, SDR has the potential to be applied to a much wider variety of systems that affect our daily lives.

1.2 Organization of Dissertation

In this dissertation, the system requirements and the design challenges for SDR are analyzed. Additionally, some innovative designs for key building blocks in SDR systems are proposed.

Chapter 2 gives the overview of software-defined architectures, design challenges and future development trends. SDR is in a transition from an idealized concept to a practical system implementation. Based on currently available technologies, a practical SDR architecture is presented with multiple key building design blocks addressed and discussed.

Chapter 3 presents a rigorous analytical model for analyzing the effects of local oscillator output imperfections such as phase/amplitude imbalances and phase noise on M-ary quadrature amplitude modulation (M-QAM) transceiver performance. This model analyzes key system performance parameters for SDR systems.

Chapter 4 discusses the data converter design requirements and challenges for an SDR system. Both ADC and DAC are the most important design blocks for an SDR system. With high performance data converters, the boundary between the digital and analog domains has moved toward the antenna with many analog components being replaced with digital and software designs. A DAC design is then shown as an example.

Chapter 5 proposes a novel, fully reconfigurable, switched capacitor filter design. This filter is another key enabling design block used for the anti-aliasing filter on the receiver signal path before the ADC and is important for achieving a high performance and low cost SDR transceiver. This filter is a discrete time FIR filter implemented with analog circuitry that can be reconfigured to many different filter architectures with different FIR coefficients for different high pass, low pass, or band pass filtering requirements.

Chapter 6 discusses the design challenges to the digital front-end in an SDR transceiver. A multi-mode multi-channel SDR digital front-end design is presented. The design is implemented in a femtocell base station that supports a flexible multi-channel combination of most 2G, 3G and 4G cellular standards. As one of the key blocks, an innovative reconfigurable resampler design with arbitrary fractional resampling ratio is then presented.

Chapter 7 summarizes and concludes the research work and discusses future work on SDR.

Chapter 2 Overview of Software-Defined Radio

2.1 Classic Software-Defined Radio Architecture and Design Challenges

Software-defined radio (SDR) has been addressed and defined in many ways. One of the most commonly cited definitions is from Buracchini [17]

"*Software radio is an emerging technology, thought to build flexible radio systems, multi-service, multi-standard, multi-band, reconfigurable and reprogrammable by software."*

The core idea of this definition is to have most of the signal processing in a radio system be defined, controlled, and implemented in software. Compared with conventional hardware implementations, which support one dedicated application, an SDR system with reconfigurability and programmability from the software is capable of receiving different signals in a wide frequency range, with different signal bandwidths, different power/sensitivities, different modulations, different codecs, and different clock domains, not only for existing standards but also for future ones.

The term "software" is defined as the programs and other operating information run by a general purpose computation unit. It is naturally in the digital signal domain and bonded with digital circuitry. Therefore, one hallmark for SDR is to place data converters, and by extending the digital to analog boundary, as close as possible to the antenna [14]. The classic and most ideal SDR architecture [18][19] has been illustrated as in Figure 2-1, in which ADC and DAC run at a clock frequency more than twice the signal RF frequency to provide the integrity of RF

signal in the digital to/from analog conversions based on the Nyquist-Shannon sampling theorem. All signal processing and conversions including those for RF, IF, and baseband are implemented in software by a powerful DSP. The extremely high performance ADC and DAC convert the digital signal in RF frequency domain to and from analog RF signals which directly interface with the antenna with a duplexer block in the middle to separate the transmit and receive signals. In this ideal conceptual SDR system, the full signal spectrum within the bandwidth of both ADC and DAC crosses the digital to analog boundary to become the digital signal without any process or conversion in the analog domain. The software operated in the DSP will process, convert, modulate/demodulate and code/decode the full bandwidth signal for any current or future standard, any mode in any frequency band, and with any bandwidth within the bandwidth of both ADC and DAC.

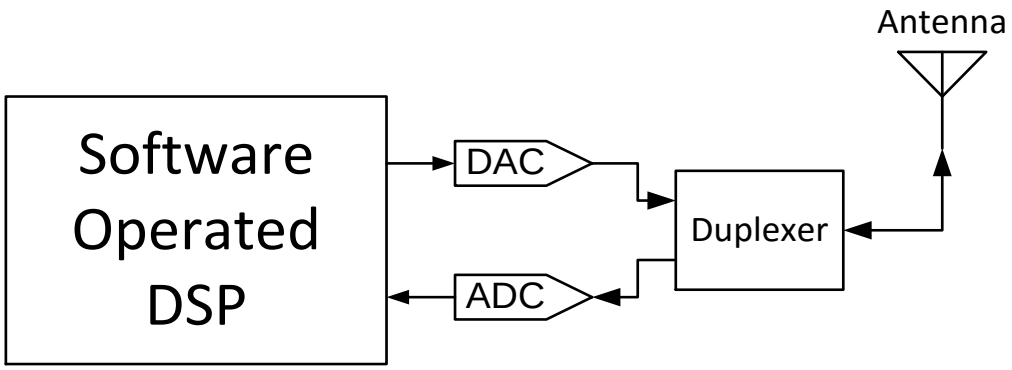


Figure 2-1 Conceptual drawing of an ideal SDR architecture

However, this ideal SDR architecture is not practical or applicable for most radio systems. Among all practical limitations, there is no feasible ADC or DAC design yet for this ideal SDR architecture. Of these two, the ADC is more challenging to design for matched bandwidth and dynamic range. Even considering the bandpass sampling case, the data converter bandwidth is

relaxed to cover only the bandwidth of the combined multi-standard multi-channel signal. For a typical 3G/4G cell phone, it means to cover a very wide 2GHz bandwidth from 700MHz to 2.7GHz, which is a still very challenging objective for any cutting-edge ADC design.

Another key ADC performance is the dynamic range, which is measured as either the effective number of bit (ENOB) or spurious free dynamic range (SFDR). In any traditional single-channel radio system, the ADC needs to provide enough ENOB to receive a signal with different power levels. However, especially for an SDR system, ADC needs to convert a combined multi-standard, multi-channel signal with quite different power levels for each channel. Thus, a higher dynamic range is required to convert the analog RF signal to the digital signal with integrity, without desensitizing any signal channel in a lower power level.

Even though ADC technology has improved steadily over the past decades, the latest state-of-the-art ADC designs still far from meeting the required performance as used in the ideal SDR architecture [20]. Other than the performance shortage, power consumption, cost and transition power are other practical considerations for a data converter to be used in a practical SDR system. High speed and dynamic range ADC means high power consumption and high cost. Additionally, ADC power efficiency is dropping with the increase of the bandwidth for any bandwidth more than 1GHz [20][21]. Consequently, a feasible choice of ADC in practical SDR system should not ask for a state-of-the-art ADC with highest available bandwidth. On the transmission side of the system, even though some of latest DAC designs can provide enough both conversion bandwidth and dynamic range for a practical SDR system, they cannot provide enough radiating RF power to meet most radio system requirements. To resolve the above shortcomings of ADCs and DACs used in the ideal SDR architecture, RF conversion circuitries-

including power amplifier, LNA, band select filter and anti-aliasing filter- have to be added in to the system for a more practical SDR system.

2.2 SDR System Architectures

A practical SDR architecture considering the current development level of SDR key enabling technologies, system cost, and power efficiency, is illustrated in Figure 2-2. On the left side, one SDR system-on-chip (SoC) is composed of a software operated baseband block, an SDR digital front-end block, a software operated system controller and data converters. On the Tx side, the signal output from SDR SoC is mixed with the RF carrier from the digital PLL, then passes through the BPF before going to the duplexer and the antenna. On the Rx side, the received signal from the antenna goes through the duplexer and is then amplified by the LNA. After that, the Rx signal is mixed down with the RF carrier from the digital PLL and passes through the LBF before being input into the SDR SoC.

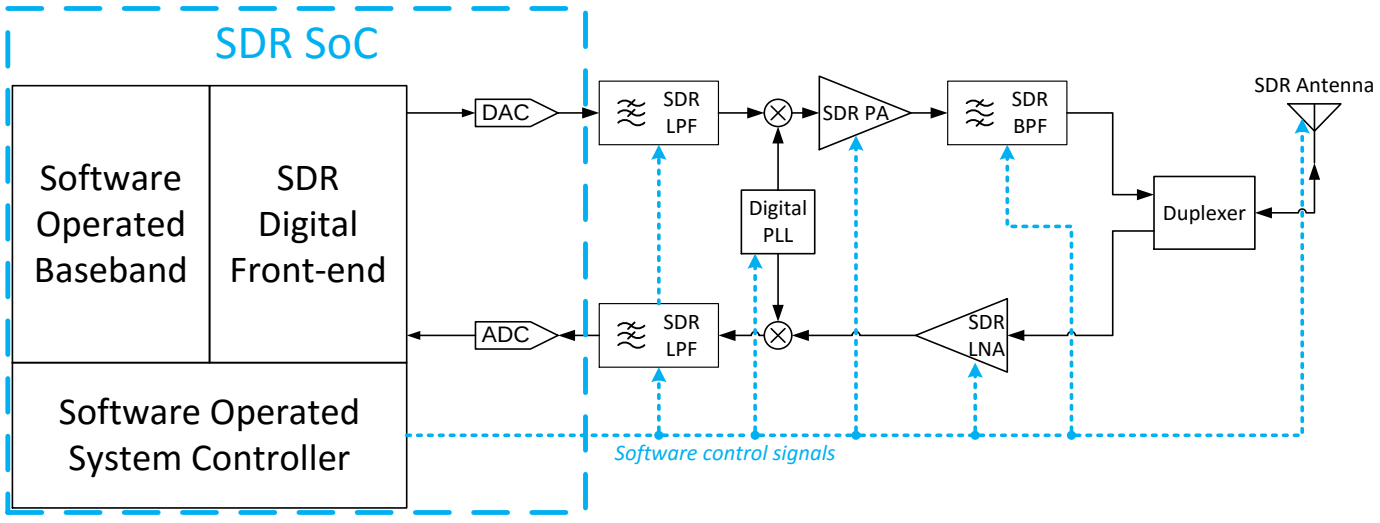


Figure 2-2 A more practical SDR architecture

For a multi-standard, multi-channel radio application, the bandwidth of the practical data converter designs should only cover the combined bandwidth of multi-channel signals but not the whole bandwidth from DC to the highest signal RF frequency. Therefore, a low intermediate frequency (LIF) architecture is chosen for this SDR architecture. On the Tx path, multiple signals for different standards or bands are mixed to one of several very low intermediate frequencies and then combined together. On the Rx path, the combined multi-standard, multi-channel RF signal is first converted from RF to a close to baseband very low IF, then converted to digital signal by the DAC. In the SDR digital front-end block, the band selectivity for different channels is implemented using digital filters. The signal is first split, then filtered into multiple signals for different standards and bandwidths, and finally mixed digitally into the baseband.

Even though the digital IF conversion is all implemented on the SDR SoC digital domain, the sample rate for the signal is still very high. For example, the sample rate of a cellular system during the IF conversion can be hundreds of mega samples per second. Any process, even a simplest one such as digital mixing or a 3-tap equalizing, runs at this very high sample rate. Therefore, the computational complexity and the power consumption would be very high if using a pure software processing with a general purpose DSP or CPU. To optimize the system cost and power efficiency, a highly reconfigurable and programmable digital application-specific integrated circuit (ASIC) front-end design controlled by software is chosen for the proposed practical SDR architecture instead. Chapter 6 will present a multi-standard, multi-mode, multi-channel digital front-end design. Advanced and novel designs for two key blocks, a time interleave reconfiguration FIR filter, and a reconfiguration fractional ratio resampler will be discussed in more detail.

With currently available and very powerful DSP and CPU technology, the baseband conversion and source processes can mostly be done in software. There have been commercialized software-defined baseband products on marking in recent years. As far as the digital front-end block and the software operated baseband block are concerned, a software-operated controller provides all system level synchronized control signals for all other blocks in the SDR system.

Compared with the classic SDR architecture shown in Figure 2-1, this proposed practical SDR architecture has moved the data converters, and thus digital to analog boundary, farer from the antenna with practical considerations. The RF conversion is still implemented by analog/RF circuitries unlike the case for the ideal SDR architecture where there is no analog/RF circuitry for the RF conversion. However, for those analog/RF circuitries used in the SDR system, each of them needs to be improved and evolved from having a dedicated function for a single band and a single mode to having both reconfigurability and programmability.

The antenna was not envisioned to be a block with any reconfigurability and programmability in the classic SDR architecture. However, with a dedicated antenna design, the reconfigurability and the programmability provided from all other design blocks in the SDR system would be much diminished since a dedicated antenna design has a fixed radiation frequency with a fixed optimal radiation bandwidth. Especially for an antenna designed with very limited physical space for a cell phone, the antenna bandwidth would be too limited to effectively cover the whole multi-band signal bandwidth. Recent developments have provided SDR system required reconfigurability and programmability to the antenna designs with dynamic impedance tuning [22][23][24][25] or dynamic aperture tuning [26][27][28]. With these

developments, the newly designed SDR antennas can be controlled by the software to be reconfigured or adaptively tuned to different radiation frequencies with different bandwidths for different multi-mode and multi-channel signals. Moreover, adaptive tuned antenna can compensate dynamically for the channel drifting or the electrical environment changing. The reconfigurable and adaptively tunable antenna has become a newly added enabling technology for an SDR system, which has been commercialized by several companies in the industry [30].

The power amplifier (PA) in the Tx path is a necessary RF design to provide sufficient RF radiation power which no current DAC design can do as used in the classic SDR architecture. Traditionally, the PA for most radio systems is designed on high power technologies, LDMOS, GaN and GaAs, for a dedicated band and power objective without any programmability. In recent decades, there have been more and more PA design developments in CMOS or hybrid technologies. Reconfigurability and programmability have been added to the PA design by having software-controlled tunabilities on the load line, the active size of PA, the biases, and the supply voltages and other circuitries around the PA. Utilizing the latest technology developments on PA, an SDR PA can have software controlled reconfigurability and programmability and can be used for a multi-standard, multi-channel SDR system.

On the Rx path, a low noise amplifier (LNA) is required to amplify the received signal to a good power level for being processed later without adding too much noise. Similar to the PA design on the Tx path, the latest developments on LNA designs also adds reconfigurability and programmability for SDR systems.

For both Tx and Rx paths, the signal needs to be mixed up or down with the RF carrier frequency. Evolved from classic phase locked loop (PLL) circuitry, digital PLLs [29][31][32][33] have been developed in recent decades for reconfigurability and programmability.

For the proposed practical SDR architecture, most frequency selectivities are implemented in the digital domain. However, in the RF/analog domain, it is still necessary to have a tunable band pass filter after the Tx PA to reject sideband interference generated by PA nonlinearity. It is also necessary to have a tunable low pass filter before the ADC on Rx path for rejecting aliasing and for relaxing the dynamic range challenge of the ADC design. Chapter 5 will discuss the SDR tunable filer design in detail.

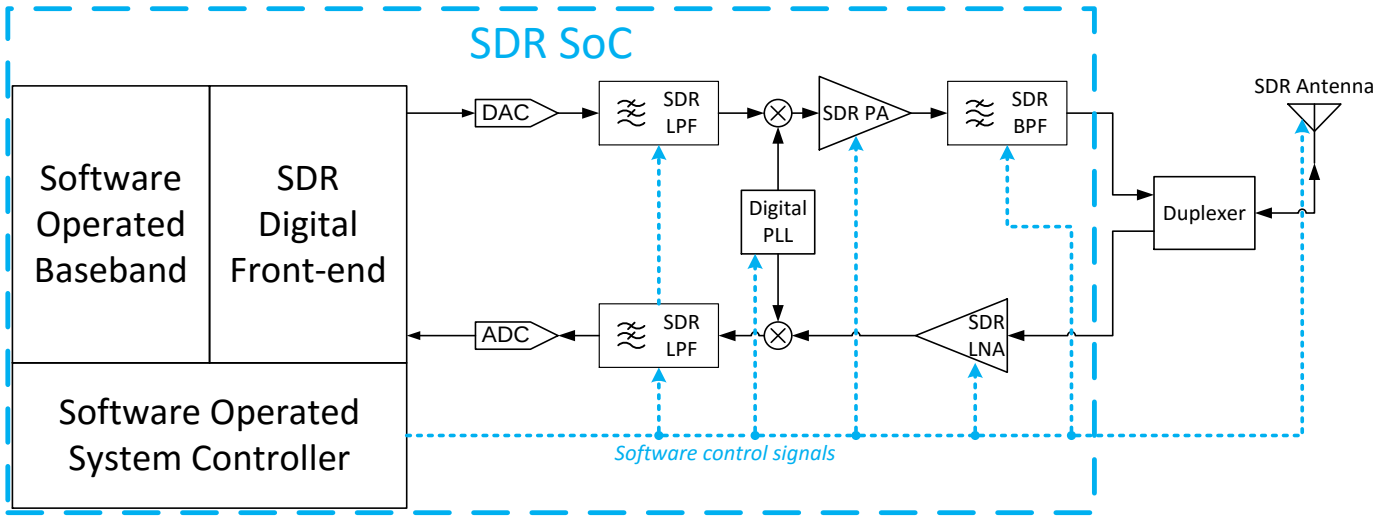


Figure 2-3 A integrated SDR architecture

With the advance of semiconductor technologies, all RF/analog circuitries for the RF conversion part of the proposed SDR architecture shown in Figure 2-2 will be implemented on the same die using advanced CMOS technology. Therefore, as shown in Figure 2-3, an SDR SoC

will be implemented to include every part of the SDR system except the duplexer and the SDR antenna. This would be one big step toward the ideal SDR architecture as shown in Figure 2-1.

Chapter 3 Effects of LO Phase and Amplitude Imbalances and Phase Noise on M-QAM Transceiver Performance

This chapter presents a rigorous analytical model for analyzing the effects of local oscillator output imperfections such as phase/amplitude imbalances and the phase noise on M-ary quadrature amplitude modulation (M-QAM) transceiver performance. A closed-form expression of the error vector magnitude (EVM) and an analytic expression of the symbol error rate (SER) are derived considering a single carrier, linear transceiver linked with additive white Gaussian noise (AWGN) channel. The proposed analytical model can calculate system EVM and SER performance thousands of times faster than Monte-Carlo method and giving higher number precision for the results. The proposed QAM imperfection analysis model provides an efficient method for system and circuit designers to analyze the wireless transceiver performances and properly trade-off and specify the transceiver block specifications.

3.1 Introduction

With the ever-increasing demand for high data rate in emerging communication systems, such as fourth-generation (4G) wireless systems, wireless local area network (WLAN) systems, and digital video broadcasting (DVB), high bandwidth efficiency is highly required. An M-ary quadrature amplitude modulation (QAM) with large M value, such as 32, 64, 128 or higher, has received increasing interest from many wireless communications systems. However, there is a significant cost for the high bandwidth efficiency. The M-ary QAM systems with a large M value has more stringent requirements than the slow data-rate 4-ary or 8-ary modulations on

many wireless transceiver specifications such as the signal-to-noise ratio (SNR), linearity, local oscillation (LO) phase and amplitude accuracy, LO synchronizations, and LO phase noise.

In addition to the complicated modulation schemes, the emerging high data-rate wireless systems are required to operate at higher and higher frequency bands, e. g., 2GHz for 3G systems, 2.4GHz/5.2GHz for WLAN networks, and 3GHz~10.6GHz for ultra-wideband (UWB) applications and so on. Therefore, high data-rate wireless transceiver designs are facing more challenges to provide clean and balanced LO quadrature signals. For a typical voltage controlled oscillator (VCO), the phase noise increases with the square of the center frequency [34][35]. Therefore, at higher frequency bands, the phase noise effect is rather significant for the M-ary QAM systems with large M value. Furthermore, the quadrature synthesizer will introduce non-negligible phase and amplitude imbalances for the LO frequency in the GHz range. Those imbalances will further degrade the QAM system performance [45]. Because the free space propagation loss is proportional to the square of the frequency [36], higher transmission power is needed for increased range and receiver sensibility. The modern multi-wireless standard co-existence also generates more complicated wireless environment. The resultant degraded wireless spectrum with large jamming signals and interferences has placed more demanding linearity requirements on the receiver front-end designs.

The link budget and system parameters have to be carefully considered and budgeted into the transceiver block specifications. The M-QAM stringent requirements on the wireless system increasingly challenges the transceiver RFIC designs. It is thus desirable for both the system and the circuit level designs to have a rigorous analytical model for the imperfections of the transceiver, such as phase and amplitude imbalances, phase noise, non-ideal synchronization,

and nonlinearity. These imperfections directly affect the QAM system performance. There have been some investigations related to this topic. Several theoretical models of the VCO phase noise have been derived in [37][38][39][40]. In addition, from a practical point of view, the contributions from different noise sources in a phase lock loop (PLL) frequency synthesizer design for WLAN applications have been modeled in [41], which can be used to simulate the overall PLL synthesizer phase noise performance. A model of the phase and amplitude imbalances and DC offset in quadrature modulators and demodulators has been reported in [42]. The M-QAM-OFDM system performance with the presence of a nonlinear amplifier and phase noise is analyzed in [43]. The error vector magnitude (EVM) is normally used as a major system specification to quantify the QAM modulation accuracy. The work presented in [44] derives the effects of imbalances and phase noise of the LO signals on the EVM. The work given in [45] discussed an approach to apply EVM to RF system design. However, it is the symbol error rate (SER) that is directly related to the system performance of a transceiver data link, and the relationship between SER and EVM is not straightforward. So far, the effects of the imbalances and imperfections on the SER have not been discussed and analytically modeled in previous publications.

In this chapter, a system model of a transceiver data link for an M-QAM system is developed, which includes the phase and amplitude imbalances and the phase noise in both transmitter and receiver LOs. With this model, a closed-form analytic expression of the EVM is derived, which is more complete compared to the model given in [44] by taking into account phase and amplitude imbalances. Moreover, an analytical expression of the SER is obtained with the presence of the imbalances and the phase noise. This integration expression of the SER has no closed-form solution and can only be numerically calculated by the finite element method,

which is still more efficient compared to the commonly used Monte-Carlo based simulation approaches. Thus, the proposed QAM imperfection analysis model provides an efficient method for system engineers to analyze wireless transceiver performance and specify the transceiver requirements. It can also assist circuit designers by providing guidance for proper trade-offs in transceiver RFIC designs.

3.2 System Model

This chapter focuses on a one-directional physical link between the coder in the transmitter (Tx) and the decoder in the receiver (Rx). As shown in Figure 3-1, a full system model is comprised of a QAM modulator and demodulator, a quadrature modulator and demodulator, RF amplifier, low noise amplifier (LNA), automatic gain control (AGC), low pass filter (LPF) and antennas. The input and output of this system model are data streams to and from the coder-decoder (codec). The SER will be derived analytically and used as the major parameter to assess the performance of this system model.

In a QAM modulator, the transmitted symbols are mapped to a constellation with M signal points in a lattice, which are different in both the phase and the amplitude. Then, those discrete signal points excite a shaping filter to generate the baseband signals in two channels that are called in-phase channel (I-channel) and quadrature-phase channel (Q-channel). The QAM demodulator performs the reversed function, i.e., the received two-channel baseband signals are filtered by a matching filter and sampled to get the received signal points, which then mapped into symbols.

The quadrature modulator up-converts the two-channel baseband signals to an RF band. The carriers for both channels are generated by a transmitter's (Tx) LO generator, which is

normally a PLL with quadrature outputs. The baseband I-Q signals are up-converted using an image-rejection mixer with the single side band output. The quadrature demodulator down-converts the received RF signals to I-Q baseband signals by mixing the quadrature RF carriers generated by an Rx LO generator. The Tx and Rx LOs can be generated from the same PLL synthesizer if the up-link and the down-link operate at the same frequency. The two LPFs in the receiver path provide the baseband filtering. The RF amplifier, LNA and AGCs are used to adjust the received and transmitted signal power.

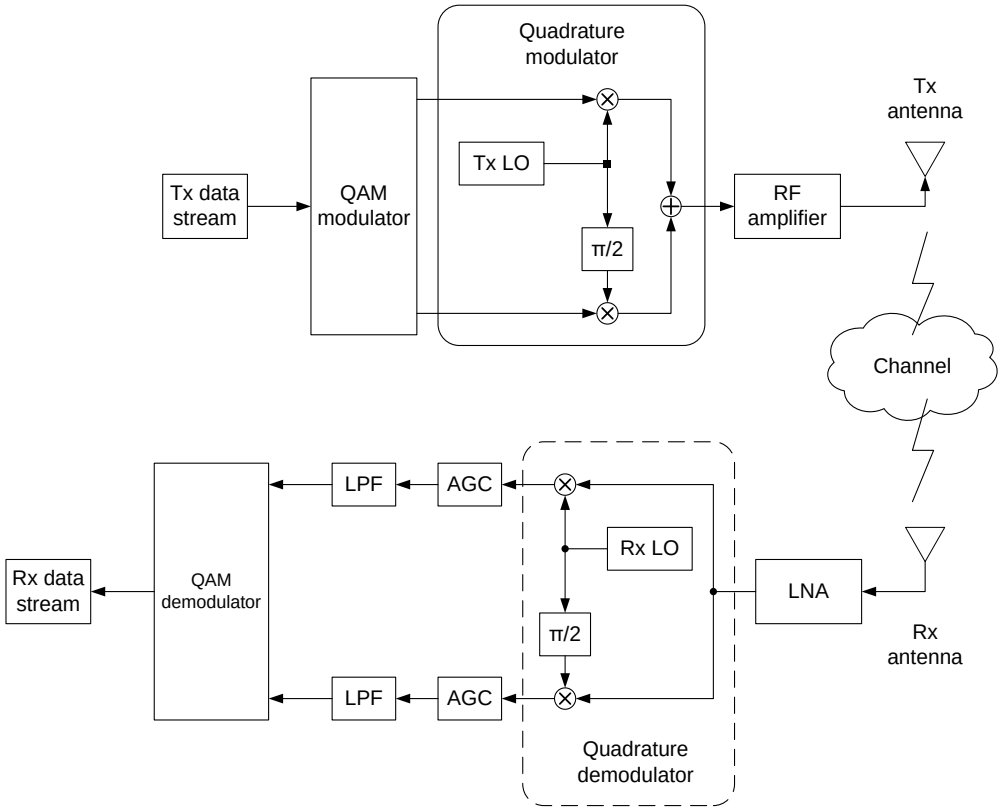


Figure 3-1 System model for an M-QAM transceiver

When implementing this system, several imperfections are introduced by the different components. Transceiver building blocks such as the LNA, AGC and RF amplifier can produce

noise and non-linearity. The amplitude imbalance, phase imbalance, DC offset and phase noise are present in the local oscillators (LO) in quadrature modulator and demodulator. In wireless transceiver RFIC designs, the commonly used techniques for quadrature signal generation can be summarized as follows: (i) a divided-by-2 by frequency divider following the VCO running at the double the frequency. This approach generally shows poor quadrature accuracy, as it requires 50% duty cycle VCO output. Therefore, there will be non-negligible phase imbalance at the divider-by-2 output. (ii) A VCO followed by a passive poly-phase RC complex filter. An integrated RC-CR network will suffer from process spread of the RC time constant resulting in amplitude imbalance between the quadrature outputs. Furthermore, the typical RC phase shift network will also load the RF oscillator. A buffer after the oscillator to relieve this loading will be power hungry and may attenuate this signal. The poly-phase network is normally a narrow band with poor quadrature amplitude and phase accuracy. (iii) Two VCOs are forced to run in quadrature by using transformer coupling, which provides wide-band quadrature accuracy with tradeoff in large silicon area for transformer designs. Two VCOs are forced to run in quadrature by using coupling transistors, which provides wide-band quadrature accuracy with a tradeoff in phase noise. The above two quadrature VCO designs suffer from large power consumption necessary to operate two VCOs, non-negligible phase noise and phase/amplitude imbalances. Therefore, phase and amplitude imbalances have to be considered in transceiver RFIC designs for QAM applications. At the receiver the non-ideal synchronizations= of the frequency and phase of the carrier and the sample timing will also degrade the system performance. LO synchronization is a critical requirement for MIMO transceiver RFIC designs [46]. For a real system, the channel may have the features of frequency selective, time varying, doubly selective and fading for different application environments.

This chapter will discuss the imperfections that degrade performance, including amplitude imbalance, phase imbalance, dc offset and phase noise. Other imperfections are neglected but also shown here to give a full picture of the system considerations. To simplify the problem, an additive white Gaussian noise (AWGN) channel is used as the channel model in the analysis.

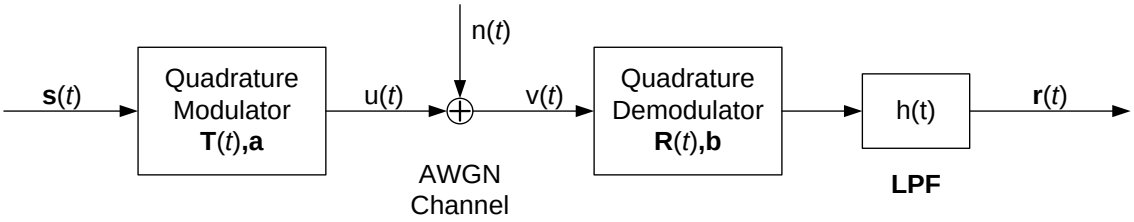


Figure 3-2 Equivalent system model.

Under those considerations, the equivalent system model in vector presentation is shown in Figure 3-2. The $\mathbf{s}(t) = \left[s_i(t), s_q(t)\right]^{\mathrm{T}}$ presents the shaped QAM output, where the superscript T denotes the transpose operation. The quadrature modulator imperfection is modeled by a vector $\mathbf{a} = \left[a_i, a_q\right]^{\mathrm{T}}$, which represents the DC offset and a 1-by-2 matrix $\mathbf{T}(t)$ as

$$\mathbf{T}(t) = 2[k\cos(\omega t)\,, \sin(\omega t + \phi)\,] \tag{3.1}$$

where ω is carrier angular frequency, k presents the amplitude imbalance which has a value around 1, ϕ presents the phase imbalance with its magnitude much smaller than $\pi/2$. The constant, 2, is inserted to keep the gain of the transceiver link to be one. Therefore, the output signal from the quadrature modulator is a time-varying scalar expressed as

$$u(t) = \mathbf{T}(t)\left[\mathbf{s}(t) + \mathbf{a}\right]. \tag{3.2}$$

Similar to the modulator, the imperfection of the quadrature demodulator is modeled by a vector $\mathbf{b} = \left[b_i,\ b_q\right]^{\mathrm{T}}$ and a 2-by-1 matrix $\mathbf{R}(t)$ as

$$\mathbf{R}(t) = \left[l\cos\left(\omega t + \alpha\right),\ \sin\left(\omega t + \alpha + \gamma\right)\right]^{\mathrm{T}}, \tag{3.3}$$

where α presents a constant phase difference between the transmitter LO and the receiver LO, which is introduced by the non-ideal synchronization of carrier, l presents the amplitude imbalance, γ presents the phase imbalance. Let n(t) denote AWGN with power single-side spectrum density (PSD) of N_0. Using all above expressions, the output signal $\mathbf{r}(t)$ can be expressed as

$$\begin{aligned}\mathbf{r}(t) &= LPF\left\langle \mathbf{R}(t)\left\{\mathbf{T}(t)\left[\mathbf{s}(t) + \mathbf{a}\right] + n(t)\right\} + \mathbf{b}\right\rangle \\ &= LPF\left\langle \mathbf{R}(t)\mathbf{T}(t)\mathbf{s}(t) + \mathbf{R}(t)\mathbf{T}(t)\mathbf{a} + \mathbf{b} + \mathbf{R}(t)n(t)\right\rangle,\end{aligned} \tag{3.4}$$

where $LPF\left\langle\ \right\rangle$ represents the function of LPF. Considering that the signal bandwidth is smaller than the bandwidth of the LPF and the RF carrier frequency is out of the passband of the baseband LPF, equation (3.4) can be rewritten as

$$\mathbf{r}(t) = \mathbf{H}\mathbf{s}(t) + \mathbf{d} + \mathbf{n}_r(t), \tag{3.5}$$

with the output constant offset given as

$$\mathbf{d} = \mathbf{H}\mathbf{a} + \mathbf{b}, \tag{3.6}$$

the channel matrix given as

$$\begin{aligned}\mathbf{H} &= LPF\left\langle \mathbf{R}(t)\mathbf{T}(t)\right\rangle \\ &= LPF\left\langle 2\left[l\cos(\omega t+\alpha),\ \sin(\omega t+\alpha+\gamma)\right]^{\mathrm{T}}\left[k\cos(\omega t),\ \sin(\omega t+\phi)\right]\right\rangle \\ &= LPF\left\langle 2\begin{bmatrix} kl\cos(\omega t+\alpha)\cos(\omega t) & l\cos(\omega t+\alpha)\sin(\omega t+\phi) \\ k\sin(\omega t+\alpha+\gamma)\cos(\omega t) & \sin(\omega t+\alpha+\gamma)\sin(\omega t+\phi)\end{bmatrix}\right\rangle \\ &= \begin{bmatrix} kl\cos(\alpha) & l\sin(\phi-\alpha) \\ k\sin(\alpha+\gamma) & \cos(\alpha+\gamma-\phi)\end{bmatrix},\end{aligned} \tag{3.7}$$

and the received channel noise given as

$$\mathbf{n}_r(t) = LPF\left\langle \mathbf{R}(t)n(t)\right\rangle. \tag{3.8}$$

In equation (3.7), it is observed that the channel matrix **H** is no longer dependent on time, because the high frequency components are suppressed by the LPF. The received noise, $\mathbf{n}_r(t)$, is still a Gaussian noise, because it comes from a linear transform of the Gaussian channel noise. It has zero mean, and its covariance matrix is given by (as detailed in sector 3.8)

$$\mathbf{C}_{\mathbf{n}_r\mathbf{n}_r} = \frac{N_0 B}{4}\begin{bmatrix} l^2 & l\sin(\gamma) \\ l\sin(\gamma) & 1\end{bmatrix}, \tag{3.9}$$

where B presents the bandwidth of LPF. Thus, the presence of the receiver phase imbalance results in a correlated noise in I and Q channels.

Assuming an ideal synchronization of the sampling time, the received signal samples then are expressed as

$$\mathbf{r}(n) = \mathbf{H}\mathbf{s}(n) + \mathbf{d} + \mathbf{n}_r(n), \tag{3.10}$$

where the channel matrix **H** is the same as what expressed in (3.7), the noise $\mathbf{n}_r(n)$ has the same covariance matrix as given in (3.9), and $\mathbf{r}(n) = \mathbf{r}(nT_s)$, $\mathbf{s}(n) = \mathbf{s}(nT_s)$, $\mathbf{n}_r(n) = \mathbf{n}_r(nT_s)$, are sampled signals with the symbol period of T_s.

3.3 Error Vector Magnitude Calculation

In the communication system, the modulation accuracy is quantified by error vector magnitude (EVM), which is defined as the root mean square error between the sent and the received signal vectors. For the system model discussed in this chapter, EVM can be obtained from (3.10).

First, the error vector is the difference between the transmitted and the received signal vectors expressed as

$$\mathbf{e}(n) = \mathbf{r}(n) - \mathbf{s}(n) = \left(\mathbf{H} - \mathbf{I}\right)\mathbf{s}(n) + \mathbf{d} + \mathbf{n}_r(n) = \mathbf{e}_s(n) + \mathbf{e}_n(n). \tag{3.11}$$

The above error vector consists of two components: one, denoted by $\mathbf{e}_s(n)=(\mathbf{H}-\mathbf{I})\mathbf{s}(n)+\mathbf{d}$, is related to the signal vector and is determined by a given symbol; the other, denoted by $\mathbf{e}_n(n)=\mathbf{n}_r(n)$, comes from the channel random noise with Gaussian distribution. Figure 3-3 illustrates the definition of the error vector and its two components.

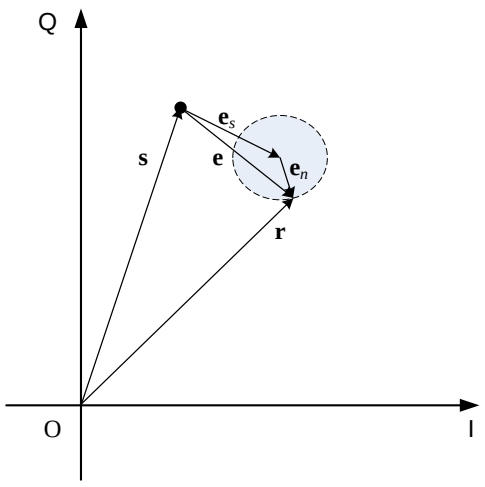


Figure 3-3 Error vector.

From the error vector expressed in (3.11), the EVM can be found out as

$$\begin{aligned} EVM^2 = \sigma_{\mathbf{e}}^2 &= E\left[\mathbf{e}^{\mathrm{H}}(n)\mathbf{e}(n)\right] = E\left[\mathbf{e}^{\mathrm{T}}(n)\mathbf{e}(n)\right] \\ &= E\left[\left(\left(\mathbf{H}-\mathbf{I}\right)\mathbf{s}(n)+\mathbf{d}+\mathbf{n}_r(n)\right)^{\mathrm{T}}\left(\left(\mathbf{H}-\mathbf{I}\right)\mathbf{s}(n)+\mathbf{d}+\mathbf{n}_r(n)\right)\right], \end{aligned} \tag{3.12}$$

where the superscript H denotes Hermitian operator. Because all vectors and matrices in the approach are real, the Hermitian operator is then equivalent to the transpose operator which will be used in the following derivations. With the assumptions that the transmitted signal vectors have zero mean and are independent from the noise, and that I and Q components of the signal vectors are independent, equation (3.12) can be simplified as

$$EVM^2 = E\left[\mathbf{s}^{\mathrm{T}}(n)\left(\mathbf{H}-\mathbf{I}\right)^{\mathrm{T}}\left(\mathbf{H}-\mathbf{I}\right)\mathbf{s}(n)\right]+\mathbf{d}^{\mathrm{T}}\mathbf{d}+E\left[\mathbf{n}_r(n)^{\mathrm{T}}\mathbf{n}_r(n)\right]. \tag{3.13}$$

Based on the above mentioned assumptions, the covariance matrix of the signal is obtained as

$$\mathbf{C}_{\mathbf{s}(n)\mathbf{s}(n)} = \frac{E_s R}{2}\mathbf{I}, \tag{3.14}$$

where E_s represents average symbol energy, R represents symbol rate, and $\mathbf{I}$ represents a unit matrix. Therefore, with equation (3.7), the first term in the right hand of (3.13) can be expressed as

$$\begin{aligned}
&E\left[\mathbf{s}^{\mathrm{T}}(n)\left(\mathbf{H}-\mathbf{I}\right)^{\mathrm{T}}\left(\mathbf{H}-\mathbf{I}\right)\mathbf{s}(n)\right] \\
&= \frac{E_s R}{2}\mathrm{Tr}\left(\left(\mathbf{H}-\mathbf{I}\right)^{\mathrm{T}}\left(\mathbf{H}-\mathbf{I}\right)\right) \\
&= \frac{E_s R}{2}\left[\mathrm{Tr}\left(\mathbf{H}^{\mathrm{T}}\mathbf{H}\right)-2\mathrm{Tr}\left(\mathbf{H}\right)+2\right] \\
&= \frac{E_s R}{2}\left[\left(k^2 l^2\cos^2\left(\alpha\right)+k^2\sin^2\left(\phi-\alpha\right)+l^2\sin^2\left(\alpha+\gamma\right)+\cos^2\left(\alpha+\gamma-\phi\right)\right)-\right. \\
&\quad \left.2\left(kl\cos\left(\alpha\right)+\cos\left(\alpha+\gamma-\phi\right)\right)+2\right].
\end{aligned} \tag{3.15}$$

From equation (3.9), it can be obtained that

$$E\left[\mathbf{n}_r(n)^{\mathrm{T}}\mathbf{n}_r(n)\right] = \frac{N_0 B\left(l^2+1\right)}{4}. \tag{3.16}$$

And from (3.6)

$$\mathbf{d}^{\mathrm{T}}\mathbf{d} = \mathbf{a}^{\mathrm{T}}\mathbf{H}^{\mathrm{T}}\mathbf{H}\mathbf{a}+\mathbf{a}^{\mathrm{T}}\mathbf{H}^{\mathrm{T}}\mathbf{b}+\mathbf{b}^{\mathrm{T}}\mathbf{H}\mathbf{a}+\mathbf{b}^{\mathrm{T}}\mathbf{b}. \tag{3.17}$$

By substituting (3.15), (3.16) and (3.17) into (3.13), a detailed expression of EVM is obtained but will not be listed here for conciseness.

In practice, the EVM is usually normalized by signal power, $P=RE_s$. And by assuming that the symbol rate is equal to the pass bandwidth of the LPF, $R=B$, the normalized EVM is thus obtained as

$$EVM_{normalized} = \sqrt{\frac{1}{2}\mathrm{Tr}\left(\mathbf{H}^{\mathrm{T}}\mathbf{H}\right)-\mathrm{Tr}\left(\mathbf{H}\right)+1+\frac{\left(l^2+1\right)}{4E_s/N_0}+\frac{\mathbf{d}^{\mathrm{T}}\mathbf{d}}{P}}. \tag{3.18}$$

In the radical sign, $\frac{1}{2}\mathrm{Tr}\left(\mathbf{H}^{\mathrm{T}}\mathbf{H}\right)-\mathrm{Tr}\left(\mathbf{H}\right)+1$ represents the contribution of the phase and amplitude imbalances to EVM; $\frac{\left(l^2+1\right)}{4E_s/N_0}$ represents the contribution of the channel noise; and $\frac{\mathbf{d}^{\mathrm{T}}\mathbf{d}}{P}$ represents the contribution of the constant offsets. By using (3.18), the effects of the transceiver imbalances, channel noise and modulation offsets on EVM can be analyzed in further.

3.4 Symbol Error Rate Calculation

Considering an M-QAM system, all possible symbols are defined as an alphabet of $\mathbb{S}=\left\{s_1,\ s_2,\ \ldots\ s_N\right\}$. And the corresponding modulated vectors are defined as a vector alphabet of $\mathbb{V}=\left\{\mathbf{v}_1,\ \mathbf{v}_2,\ \ldots\ \mathbf{v}_N\right\}$. Recalling (3.10) and (3.11), for a given transmitted signal vector $\mathbf{s}(n)\in\mathbb{V}$, the received vector is expressed as

$$\mathbf{r}\left(n\right)=\mathbf{s}\left(n\right)+\mathbf{e}_s\left(n\right)+\mathbf{e}_n\left(n\right). \tag{3.19}$$

As illustrated in (3.19), the received vector has a deterministic component, $\mathbf{s}(n)+\mathbf{e}_s(n)$, and a random component, $\mathbf{e}_n(n)$. With the covariance matrix obtained in (3.9), the Gaussian noise, $\mathbf{e}_n(n)$, has a joint normal probability density function (PDF) that is expressed as

$$\begin{aligned} f_{\mathbf{e}_n}(x,y) &= N_2\left(0,0,N_0Bl^2/4,N_0B/4,\sin(\gamma)\right) \\ &= A\exp\left\{-\frac{2}{N_0B\left(1-\sin^2(\gamma)\right)}\left[\frac{x^2}{l^2}-2\sin(\gamma)\frac{xy}{l}+y^2\right]\right\}, \end{aligned} \tag{3.20}$$

$$\text{and } A=\frac{2}{\pi N_0Bl\sqrt{1-\sin^2(\gamma)}}, \tag{3.21}$$

where $N_2(\ )$ denotes a 2-dimensional joint normal distribution PDF; *x* and *y* denote the I and Q components of the received noise vector that are zero-mean random variables with their variances and correlation given by the covariance matrix in (3.9). As shown in Figure 3-4, the concentric ellipses in different gray colors illustrate the PDF of the noise. Because the two channels of the noise are correlated to each other, the contours of the PDF are not circles but tilted ellipses. Moreover, because this noise term is independent of the signal, the received noise components have identical PDF and do not relate to different transmitted signal vectors.

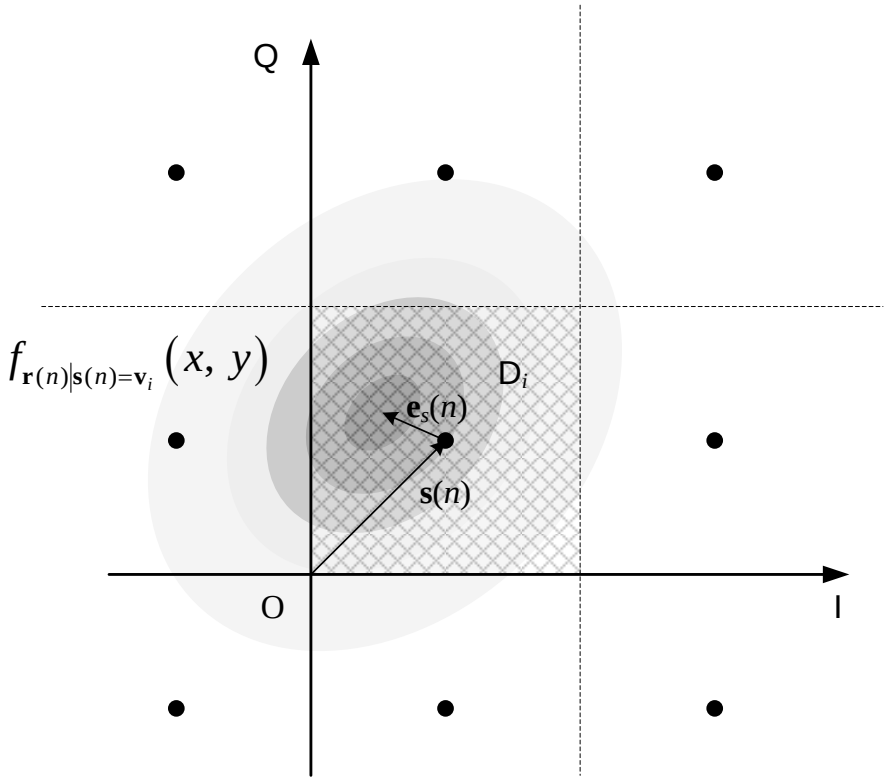


Figure 3-4 PDF of the received vector and the decision zone.

From (3.19) and (3.20), the conditional probability density function (PDF) of the received vector can be obtained as

$$\begin{aligned} f_{\mathbf{r}(n)|\mathbf{s}(n)}(x, y) &= f_{\mathbf{e}_n}\left(x-\bar{r}_x(n),\, y-\bar{r}_y(n)\right) \\ &= N_2\left(\bar{r}_x(n),\, \bar{r}_y(n), N_0Bl^2/4, N_0B/4,\, \sin(\gamma)\right) \\ &= A\exp\left\{-\frac{4}{N_0B\left(1-\sin^2(\gamma)\right)}\left[\frac{\left(x-\bar{r}_x(n)\right)^2}{l^2}-2\sin(\gamma)\frac{\left(x-\bar{r}_x(n)\right)\left(y-\bar{r}_y(n)\right)}{l}+\left(y-\bar{r}_y(n)\right)^2\right]\right\}, \end{aligned} \tag{3.22}$$

and

$$\begin{aligned} \bar{r}_x(n) &= I\left\langle \mathbf{s}(n) + \mathbf{e}_s(n) \right\rangle \\ \bar{r}_y(n) &= Q\left\langle \mathbf{s}(n) + \mathbf{e}_s(n) \right\rangle \end{aligned}, \tag{3.23}$$

where $I\langle\ \rangle$ and $Q\langle\ \rangle$ are the functions for the I component and the Q components of a vector, respectively, $\bar{r}_x(i)$ and $\bar{r}_y(i)$ are the mean values of the I and the Q components of the received vector.

For the system model considered in this chapter, under the assumption that the channel and all devices are linear and memoryless, the received QAM modulated vectors are demodulated by hard decision criteria. Thus, the decision of a received QAM symbol is made by choosing the symbol that minimizes geometric distance from the received signal vector to the assumed transmitted signal vector in the signal vector alphabet $\mathbb{V}$. Each inner constellation point has four nearest neighbors and a square decision zone. The square area shaded by crossed lines in 0, $\mathbf{D}_i$, shows a decision zone of the transmitted signal vector, $\mathbf{v}_i$. Therefore, the conditional detection probability is the integral of the conditional PDF of the received sample vector in the decision zone, $\mathbf{D}_i$, namely,

$$P_{D_i} = \iint_{\mathbf{D}_i} f_{\mathbf{r}(n)|\mathbf{s}(n)=\mathbf{v}_i}(x, y)\, dxdy. \tag{3.24}$$

And the conditional error probability is the integration of the conditional PDF of the received sample vector in the area other than decision domain, $\mathbf{D}_i$, which is the complement of the conditional detection probability expressed as

$$P_{e_i} = 1 - P_{D_i}. \tag{3.25}$$

In the constellation, the edge points and the corner points have two or three nearest neighbors, respectively. Then, the decision zone becomes a one-end-open strip or a quarter plane. The decision zone of the above three situations can be expressed in the same form as $D_i = \{x,\ y \mid x \in (a_i,\ b_i)\ \mathrm{y} \in (c_i,\ d_i)\}$ where the boundaries can be either finite or infinite. By substituting the expression of the decision zone and (3.20) into (3.22), the detection probability is expressed as

$$P_{D_i} = \int_{c_i}^{d_i}\int_{a_i}^{b_i} A\exp\left\{-\frac{4}{N_0 B\left(1-\sin^2(\gamma)\right)}\left[\frac{\left(x-\bar{r}_x(n)\right)^2}{l^2} - 2\sin(\gamma)\frac{\left(x-\bar{r}_x(n)\right)\left(y-\bar{r}_y(n)\right)}{l} + \left(y-\bar{r}_y(n)\right)^2\right]\right\}dxdy. \tag{3.26}$$

Because there is a mixture of terms of x and y in the integrand, the above integral does not have a closed form solution and can only be calculated by numerical integral methods. To calculate the total detection probability for all possible transmitted symbols, this integral needs to be calculated for each symbol. An efficient method to do the numerical integral is derived by converting (3.26) to

$$P_{D_i} = \int_{c_i-\bar{r}_y(n)}^{d_i-\bar{r}_y(n)}\int_{a_i-\bar{r}_x(n)}^{b_i-\bar{r}_x(n)} N_2\left(0,0,N_0Bl^2/4,N_0B/4,\sin(\gamma)\right)dxdy. \tag{3.27}$$

Therefore, the integrand is no longer related to the symbols. The numerical integral then can be estimated by a finite element method, i.e., calculating the integrand values in grids and accumulating grids in different integral fields.

For 32-QAM and 128-QAM, the decision zone of corner points will have a sloped boundary which makes the calculation of the SER more complicated. The SER calculation for 32-QAM and 128-QAM is not given here, yet the results can be obtained by slightly extending the work of this chapter.

Based on the assumption that each symbol in $\mathbb{S}$ has the same probability to be sent, the total symbol error rate (SER) is obtained by averaging the conditional detection error probability of each symbol as

$$P_e = \frac{1}{N}\sum_{i=0}^{N-1} P_{e_i}. \tag{3.28}$$

Equation (3.28) gives an analytical expression of the SER for an M-QAM system with the presence of transceiver imbalances and channel noise.

3.5 Phase Noise Consideration

In the above sections, the phase noise has not been taken into account, and all phase variables presented in the equations are deterministic. For a more realistic consideration of the transceiver system discussed in this chapter, the LO signals in both the transmitter and the receiver are not ideal tones, but each is a carrier with the phase noise when represented in the frequency domain or a jittered signal when represented in time domain. The phase noise then results in both random phase imbalances in quadrature modulators and random phase differences between two LOs.

A detailed phase analysis is beyond the scope of this chapter. Instead, we will simply approximate the phase noise as a zero-mean Gaussian noise in phase representation whose

variance is defined as the LO mean square phase error which can be obtained from other works [14][41].

3.5.1 EVM Calculation

All approaches presented in the above sections are valid formally except that the phase variables should be understood as random variables. Therefore, the phase difference, α, is updated as

$$\alpha = \alpha_d + \alpha_r, \quad \alpha_r \sim N\left(0,\ \alpha_{rms}^2\right) \tag{3.29}$$

where α_d denotes a constant phase difference and α_r is a Gaussian random variable which represents the phase noise.

Substituting (3.29) to (3.7),

$$\mathbf{H} = \begin{bmatrix} kl\cos\left(\alpha_d + \alpha_r\right) & l\sin\left(\phi - \alpha_d - \alpha_r\right) \\ k\sin\left(\alpha_d + \alpha_r + \gamma\right) & \cos\left(\alpha_d + \alpha_r + \gamma - \phi\right) \end{bmatrix}. \tag{3.30}$$

Under the assumption that $\alpha_{rms} << 1$, the above equation can be simplified as

$$\begin{aligned} \mathbf{H} &= \begin{bmatrix} kl\cos\left(\alpha_d\right) - kl\alpha_r\sin\left(\alpha_d\right) & l\sin\left(\phi - \alpha_d\right) - l\alpha_r\cos\left(\phi - \alpha_d\right) \\ k\sin\left(\alpha_d + \gamma\right) + k\alpha_r\cos\left(\alpha_d + \gamma\right) & \cos\left(\alpha_d + \gamma - \phi\right) - \alpha_r\sin\left(\alpha_d + \gamma - \phi\right) \end{bmatrix} \\ &= \begin{bmatrix} kl\cos\left(\alpha_d\right) & l\sin\left(\phi - \alpha_d\right) \\ k\sin\left(\alpha_d + \gamma\right) & \cos\left(\alpha_d + \gamma - \phi\right) \end{bmatrix} + \alpha_r \begin{bmatrix} -kl\sin\left(\alpha_d\right) & -l\cos\left(\phi - \alpha_d\right) \\ k\cos\left(\alpha_d + \gamma\right) & -\sin\left(\alpha_d + \gamma - \phi\right) \end{bmatrix} \\ &\triangleq \mathbf{H}_d + \alpha_r \mathbf{H}_r, \end{aligned} \tag{3.31}$$

where $\mathbf{H}_d$ has the same form as $\mathbf{H}$ in (3.7), and α_r is factored out of the matrix and multiplied by a deterministic matrix $\mathbf{H}_r$. Then, (3.10) becomes

$$\mathbf{r}(n) = \mathbf{H}_d \mathbf{s}(n) + \alpha_r \mathbf{H}_r \left(\mathbf{s}(n) + \mathbf{a}\right) + \mathbf{d} + \mathbf{n}_r(n), \tag{3.32}$$

where $\mathbf{d} = \mathbf{H}_d \mathbf{a} + \mathbf{b}$. Comparing (3.32) with (3.10), a new term, $\mathbf{n}_p(n) \equiv \alpha_r \mathbf{H}_r \left(\mathbf{s}(n) + \mathbf{a}\right)$, appears which represents the effect of the LO phase noise on the received signal. Unlike the channel noise which is additive, the phase noise is multiplied with signal. Moreover, observing the matrix, $\mathbf{H}_r$, if the phase imbalances and the phase difference are small, it approximates to an anti-identity matrix. Then, the phase noise term, $\mathbf{n}_p(n)$, is approximately perpendicular to the signal vector, which means the error due to the phase noise is mostly on the phase and not on the amplitude. Figure 3-1 illustrates the PDF of the received signal vector with the presence of phase noise with $\alpha_{rms} \approx 7^\circ$ which intuitively shows that a constellation point with a larger amplitude is influenced more by the phase noise.

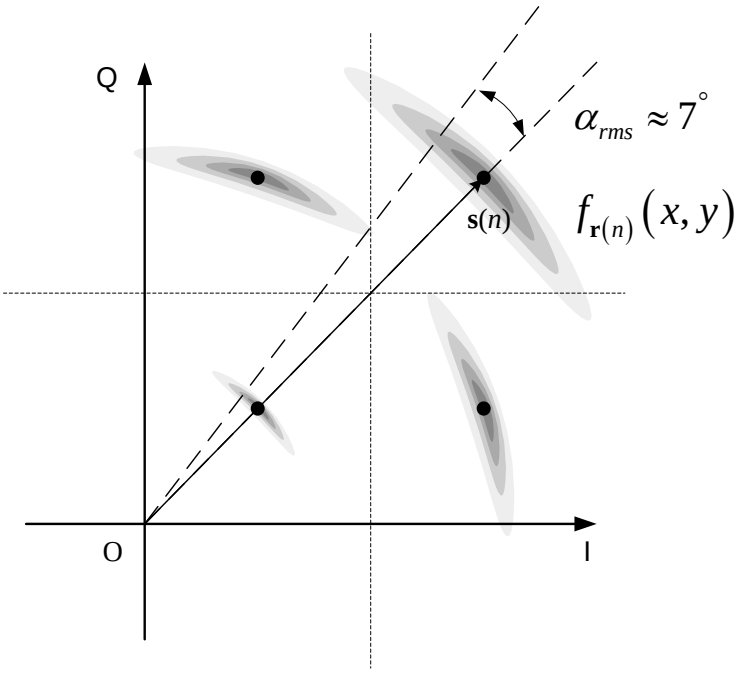


Figure 3-5 PDF of the phase noise for different constellation points.

Considering that the phase noise is independent of the signal, the covariance matrix of the $\mathbf{n}_p(n)$ is obtained as

$$\begin{aligned}\mathbf{C}_{\mathbf{n}_p\mathbf{n}_p} &= E\left[\alpha_r\mathbf{H}_r\left(\mathbf{s}(n)+\mathbf{a}\right)\left(\alpha_r\mathbf{H}_r\left(\mathbf{s}(n)+\mathbf{a}\right)\right)^{\mathrm{T}}\right] \\ &= E\left[\alpha_r^2\right]\mathbf{H}_r E\left[\mathbf{s}(n)\mathbf{s}^{\mathrm{T}}(n)\right]\mathbf{H}_r^{\mathrm{T}} + E\left[\alpha_r^2\right]\mathbf{H}_r\mathbf{a}\mathbf{a}^{\mathrm{T}}\mathbf{H}_r^{\mathrm{T}} \\ &= \frac{E_s R\alpha_{rms}^2}{2}\mathbf{H}_r\mathbf{H}_r^{T} + \alpha_{rms}^2\mathbf{H}_r\mathbf{a}\mathbf{a}^{\mathrm{T}}\mathbf{H}_r^{\mathrm{T}}.\end{aligned} \tag{3.33}$$

Note that the phase noise term in (3.32), $\mathbf{s}(n)$, α_r and $\mathbf{n}_r(n)$ are zero-mean and independent from each other, the EVM in (3.13) becomes

$$EVM^2 = E\left[\mathbf{s}^{\mathrm{T}}(n)\left(\mathbf{H}_d+\alpha_r\mathbf{H}_r-\mathbf{I}\right)^{\mathrm{T}}\left(\mathbf{H}_d+\alpha_r\mathbf{H}_r-\mathbf{I}\right)\mathbf{s}(n)\right]+\alpha_{rms}^2\mathbf{a}^{\mathrm{T}}\mathbf{H}_r^{\mathrm{T}}\mathbf{H}_r\mathbf{a}+\mathbf{d}^{\mathrm{T}}\mathbf{d}+\frac{1}{4}N_0B\left(l^2+1\right). \tag{3.34}$$

Since the phase noise is zero-mean and independent of the signal, substituting (3.31) in the first term in the right hand of (3.34) leads to the following expression:

$$\begin{aligned}&E\left[\mathbf{s}^{\mathrm{T}}(n)\left(\mathbf{H}_d+\alpha_r\mathbf{H}_r-\mathbf{I}\right)^{\mathrm{T}}\left(\mathbf{H}_d+\alpha_r\mathbf{H}_r-\mathbf{I}\right)\mathbf{s}(n)\right] \\ &= E\left[\mathbf{s}^{\mathrm{T}}(n)\left(\mathbf{H}_d-\mathbf{I}\right)^{\mathrm{T}}\left(\mathbf{H}_d-\mathbf{I}\right)\mathbf{s}(n)\right]+E\left[\mathbf{s}^{\mathrm{T}}(n)\alpha_r\mathbf{H}_r{}^{\mathrm{T}}\left(\mathbf{H}_d-\mathbf{I}\right)\mathbf{s}(n)\right] \\ &\quad + E\left[\mathbf{s}^{\mathrm{T}}(n)\alpha_r\left(\mathbf{H}_d-\mathbf{I}\right)^{\mathrm{T}}\mathbf{H}_r\mathbf{s}(n)\right]+E\left[\mathbf{s}^{\mathrm{T}}(n)\alpha_r^2\mathbf{H}_r{}^{\mathrm{T}}\mathbf{H}_r\mathbf{s}(n)\right] \\ &= E\left[\mathbf{s}^{\mathrm{T}}(n)\left(\mathbf{H}_d-\mathbf{I}\right)^{\mathrm{T}}\left(\mathbf{H}_d-\mathbf{I}\right)\mathbf{s}(n)\right]+E\left[\alpha_r^2\right]E\left[\mathbf{s}^{\mathrm{T}}(n)\mathbf{H}_r{}^{\mathrm{T}}\mathbf{H}_r\mathbf{s}(n)\right] \\ &= \frac{E_s R}{2}\left[\mathrm{Tr}\left(\mathbf{H}_d{}^{\mathrm{T}}\mathbf{H}_d\right)-2\mathrm{Tr}\left(\mathbf{H}_d\right)+2\right]+\frac{E_s R\alpha_{rms}^2}{2}\mathrm{Tr}\left(\mathbf{H}_r{}^{\mathrm{T}}\mathbf{H}_r\right)\end{aligned} \tag{3.35}$$

Therefore, the normalized EVM in (3.18) becomes

$$EVM_{normalized} = \sqrt{\frac{1}{2}\mathrm{Tr}\left(\mathbf{H}_d^{\mathrm{T}}\mathbf{H}_d\right)\text{-}\mathrm{Tr}\left(\mathbf{H}_d\right)+1+\frac{\alpha_{rms}^2}{2}\mathrm{Tr}\left(\mathbf{H}_r{}^{\mathrm{T}}\mathbf{H}_r\right)+\frac{\left(l^2+1\right)}{4E_s/N_0}+\frac{\alpha_{rms}^2\mathbf{a}^{\mathrm{T}}\mathbf{H}_r^{\mathrm{T}}\mathbf{H}_r\mathbf{a}+\mathbf{d}^{\mathrm{T}}\mathbf{d}}{P}}. \tag{3.36}$$

Comparing with (3.18), in the radical sign, $\mathrm{Tr}\left(\mathbf{H}_d^{\mathrm{T}}\mathbf{H}_d\right)/2$-$\mathrm{Tr}\left(\mathbf{H}_d\right)+1$ represents the contribution of the phase and amplitude imbalances to EVM and keeps the same form; $\left(l^2+1\right)/\left(4E_s/N_0\right)$ represents the contribution of the channel noise and also keeps the form; $\left(\alpha_{rms}^2\mathbf{a}^{\mathrm{T}}\mathbf{H}_r^{\mathrm{T}}\mathbf{H}_r\mathbf{a}+\mathbf{d}^{\mathrm{T}}\mathbf{d}\right)/P$ represents the contribution of the constant offsets which increased by a term related to phase noise; and a new component, $\alpha_{rms}^2\mathrm{Tr}\left(\mathbf{H}_r{}^{\mathrm{T}}\mathbf{H}_r\right)/2$, appears to represent the increased contribution from the phase noise to EVM.

3.5.2 SER Calculation

With the presence of phase noise, the expression of the error from the received signal becomes

$$\mathbf{r}(n)=\mathbf{s}(n)+\mathbf{e}_s(n)+\mathbf{e}_p(n)+\mathbf{e}_n(n). \tag{3.37}$$

where $\mathbf{e}_s(n)$ becomes $\left(\mathbf{H}_d\text{-}\mathbf{I}\right)\mathbf{s}(n)+\mathbf{d}$, and $\mathbf{e}_p(n)=\alpha_r\mathbf{H}_r\left(\mathbf{s}(n)+\mathbf{a}\right)$ represents the phase noise effect. Since both the channel noise and the phase noise are Gaussian, the sum of them, $\mathbf{e}(n)=\mathbf{e}_p(n)+\mathbf{e}_n(n)$, is still Gaussian. As shown in Figure 3-5, unlike the channel noise, $\mathbf{e}_n(i)$, which is independent of the signal and has an identical PDF for different symbols, the phase noise term, $\mathbf{e}_p(i)$, is dependent on the signal. Thus, it has different PDFs for different symbols. Therefore, given a transmitted symbol, the conditional covariance matrix of $\mathbf{e}_p(i)+\mathbf{e}_n(i)$ is obtained as

$$\begin{aligned}\mathbf{C}_{\mathbf{ee}|\mathbf{s}(n)} &= E\left[\alpha_r \mathbf{H}_r\left(\mathbf{s}(n)+\mathbf{a}\right)\left(\alpha_r \mathbf{H}_r\left(\mathbf{s}(n)+\mathbf{a}\right)\right)^{\mathrm{T}}\right]+\mathbf{C}_{\mathbf{n}_r\mathbf{n}_r} \\ &= \alpha_{rms}^2 \mathbf{H}_r\left(\mathbf{s}(n)+\mathbf{a}\right)\left(\mathbf{s}(n)+\mathbf{a}\right)^{\mathrm{T}}\mathbf{H}_r^T+\mathbf{C}_{\mathbf{n}_r\mathbf{n}_r} \\ &\square \begin{bmatrix} c_{11} & c_{12} \\ c_{12} & c_{22} \end{bmatrix}.\end{aligned} \tag{3.38}$$

Then the PDF of the received signal is expressed as

$$f_{\mathbf{r}(n)|\mathbf{s}(n)}(x,\, y) = N_2\left(\bar{r}_x(n),\, \bar{r}_y(n),\, c_{11},\, c_{22},\, c_{12}/\sqrt{c_{11}c_{22}}\right). \tag{3.39}$$

Following the similar approach used for (3.24), (3.25), and (3.28) in Section 3.4, the SER can be calculated with the presence of the phase noise as

$$P_e = \frac{1}{N}\sum_{i=0}^{N-1}\left(1-\iint_{\mathbf{D}_i} f_{\mathbf{r}(n)|\mathbf{s}(n)=\mathbf{v}_i}(x,\, y)\,dxdy\right). \tag{3.40}$$

It should be noticed that the simplified approach in (3.27) is no longer valid. Although the above integral has to be numerically calculated for each individual constellation point, this theoretical calculation is still much more efficient than a Monte-Carlo simulation based method. Moreover, the proposed SER model provides an accurate calculation for a SER less than 10^{-5}, which is difficult to achieve using Monte-Carlo simulations.

3.5.3 Phase Noise Presented in Phase Imbalance

As mentioned in the above section, the phase noise can also yield the randomization of the phase imbalance. Similar to (3.29), the phase imbalances in the transmitter and the receiver can be decomposed to a deterministic part and a random part as

$$\phi = \phi_d + \phi_r, \quad \phi_r \sim N\left(0,\ \phi_{rms}^2\right) \tag{3.41}$$

$$\gamma = \gamma_d + \gamma_r, \quad \gamma_r \sim N\left(0,\ \gamma_{rms}^2\right) \tag{3.42}$$

Substituting (3.41) and (3.42) to (3.7) respectively, and assuming that φ_{rms}<<1 and γ_{rms}<<1, the channel matrix becomes

$$\begin{aligned}\mathbf{H} &= \begin{bmatrix} kl\cos(\alpha) & l\sin(\phi_d + \phi_r - \alpha) \\ k\sin(\alpha+\gamma) & \cos(\alpha+\gamma-\phi_d-\phi_r)\end{bmatrix} \\ &= \mathbf{H}_d + \phi_r \begin{bmatrix} 0 & l\cos(\phi_d - \alpha) \\ 0 & \sin(\alpha+\gamma-\phi_d)\end{bmatrix} \\ &\approx \mathbf{H}_d + \phi_r \mathbf{H}_\phi,\end{aligned} \tag{3.43}$$

and

$$\begin{aligned}\mathbf{H} &= \frac{A_r A_t}{2}\begin{bmatrix} kl\cos(\alpha) & l\sin(\phi-\alpha) \\ k\sin(\alpha+\gamma_d+\gamma_r) & \cos(\alpha+\gamma_d+\gamma_r-\phi)\end{bmatrix} \\ &= \mathbf{H}_d + \gamma_r \begin{bmatrix} 0 & 0 \\ k\cos(\alpha+\gamma_d) & -\sin(\alpha+\gamma_d-\phi)\end{bmatrix} \\ &\approx \mathbf{H}_d + \gamma_r \mathbf{H}_\phi.\end{aligned} \tag{3.44}$$

If all phase noise effects on phase imbalances and phase difference are taken into account, a more sophisticated channel matrix is expressed as

$$\mathbf{H} = \mathbf{H}_d + \alpha_r \mathbf{H}_r + \phi_r \mathbf{H}_\phi + \gamma_r \mathbf{H}_\phi \tag{3.45}$$

Using the channel matrices in (3.43), (3.44) and (3.45), following the approach above, the calculation of EVM and SER can be obtained with the presence of random phase imbalance in

the transmitter or the receiver or both. It should be noticed that the random phase imbalance in the receiver would affect the received channel noise and change the expression of the covariance matrix in (3.9). The details of this part of work are very similar to what have been shown in above sections and will not be presented in this chapter.

3.6 Simulations and Calculations

In section 3.5, the expressions of EVM, (3.36), and SER, (3.40) are shown which include all the parameters from Tx phase and amplitude imbalance, Tx offset, Rx phase and amplitude imbalance, Rx offset, carrier synchronization phase offset and phase noise. A program to calculate EVM and to numerically calculate SER has been built. We have also developed a Monte-Carlo simulation program to provide the comparison and the verification for the analytically calculated results. All results shown below are normalized to signal power, thus $B = R = 1$ and $E_s = 1$.

In the model used in this section, many parameters are taken into account, including the transmitter amplitude imbalance, k, phase imbalance, φ, transmitter offset, **a**, receiver amplitude imbalance, l, phase imbalance, γ, receiver offset, **b**, phase difference, α_d, and phase noise quantified by α_{rms}, and E_s/N_0. Each parameter affects the received signal respectively. In Figure 3-6, the simulated received signals with different imperfections are shown. Only four points in 64-QAM constellations are shown to illustrate the result clearly.

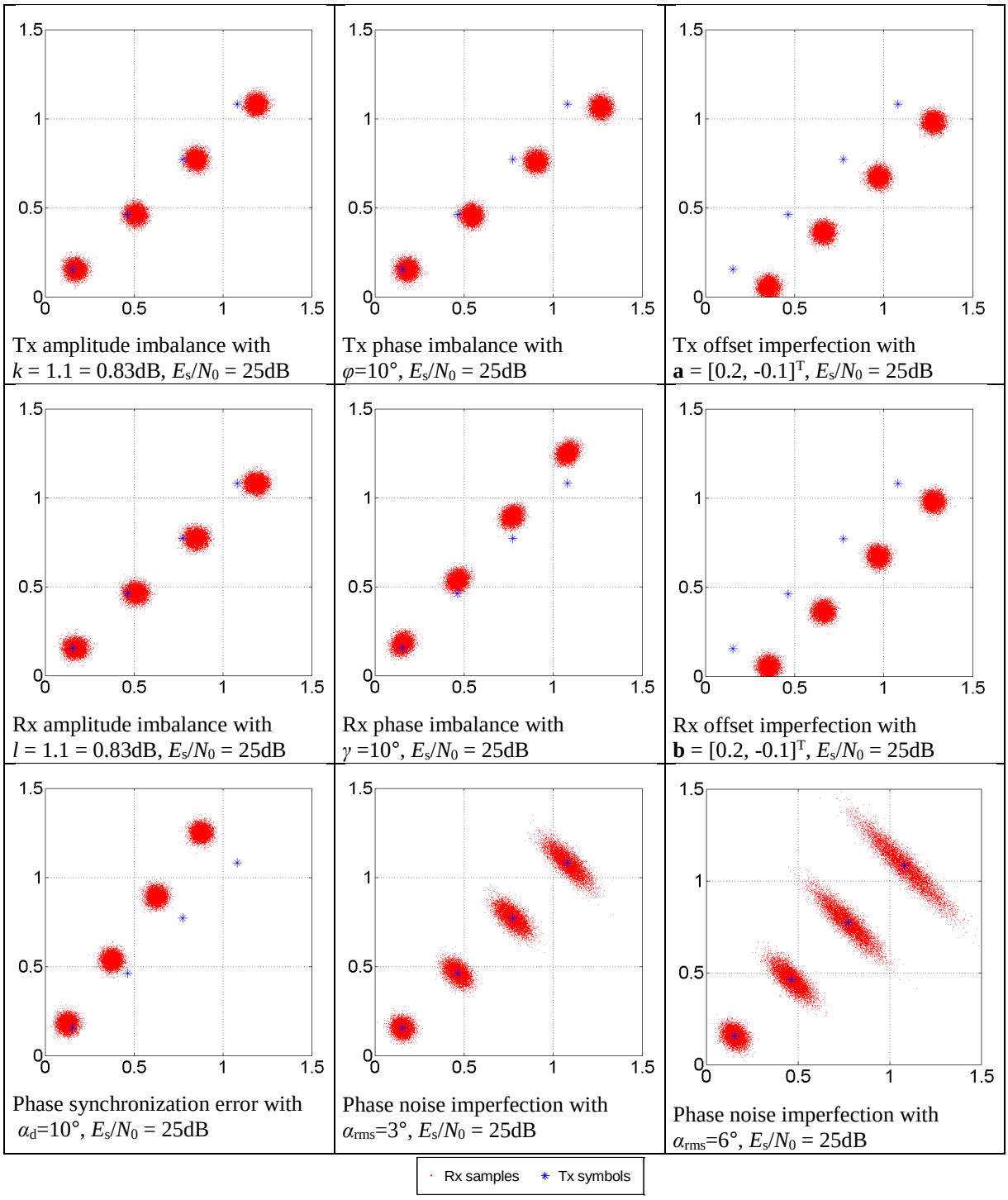
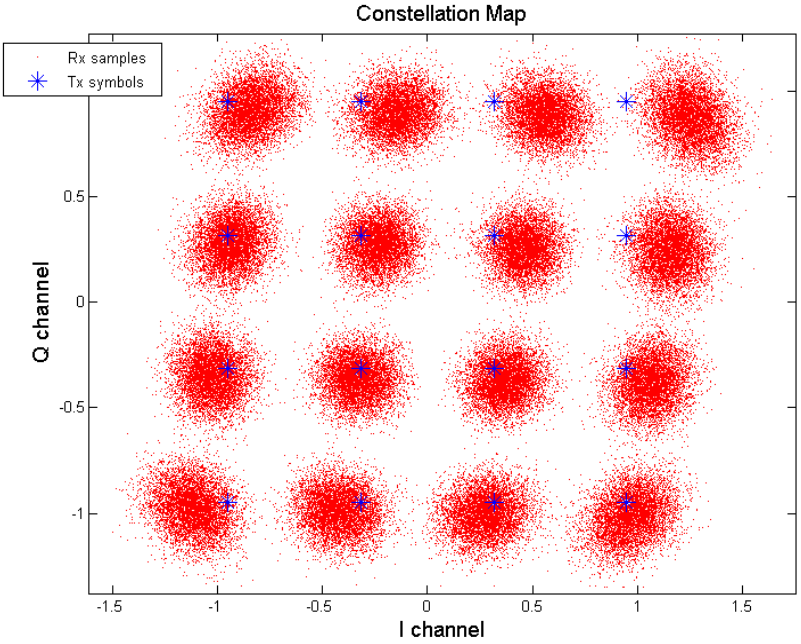


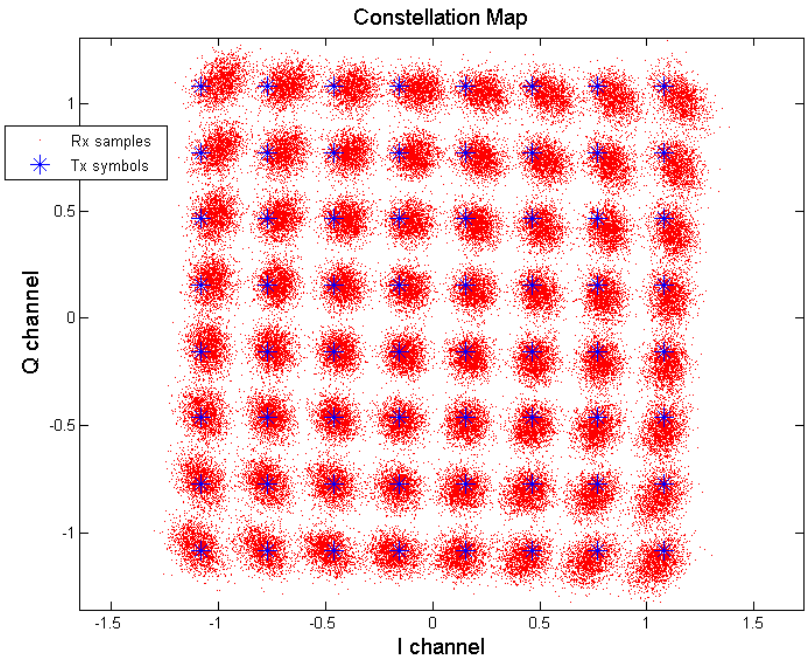
Figure 3-6 64 QAM constellations affected by different imperfections.

Figure 3-7 and Figure 3-8 demonstrate two typical situations for 16-QAM and 64-QAM, respectively. As shown in the figures, the results from the analytical calculation are well matched with the results from Monte-Carlo simulation. An observation of the received samples is that the constellation is distorted in a complicated way, which combines the shift, rotation, and shear transformations coming from many effective parameters mentioned above. In addition, the shift and shape of the clouds of received samples are different for different transmitted constellation points. Intuitively, the points with larger amplitude are affected more by imbalances and the phase noise and thus contribute more to the average SER and EVM than the points closer to the origin.



Calculated EVM = 0.2067	Simulated EVM = 0.2063
Calculated SER = 2.963e-2	Simulated SER = 2.977e-2

Figure 3-7 16-QAM sample situation: k = 1.05 = 0.42dB, φ=5°, $\mathbf{a} = [0.06,0]^T$, l = 1.05= 0.42dB, γ=2°, $\mathbf{b} = [0, -0.05]^T$, α_d=-3°, α_{rms}=3°, and N_0= -15dB with 1e5 symbols simulated.



Calculated EVM = 0.09679	Simulated EVM = 0.09668
Calculated SER = 4.615e-2	Simulated SER = 4.587e-2

Figure 3-8 64-QAM sample situation: k = 1.02 = 0.17dB, φ=2°, $\mathbf{a} = [0.03,0]^T$, l = 0.97 = -0.26dB, γ=-1°, $\mathbf{b} = [0, -0.02]^T$, α_d=-1°, α_{rms}=2°, and N_0= -20dB with 1e5 symbols simulated.

Figure 3-9 shows the EVM variation for 16-QAM with the transmitter gain and the phase imbalance in the case without channel noise, phase noise and receiver imbalances. Because the symmetric characteristic between the transmitter imbalances and the receiver imbalances in channel matrix in (3.7), the EVM variation with the receiver gain and the phase imbalance results in the identical figure. However, the presence of channel noise will break the symmetry and make the receiver imbalances contribute a little more to the EVM than the transmitter imbalances. The EVM calculation in (3.18) and (3.36) also shows that the EVM is not related to

the number of the modulation points, *N*. Thus, the EVM calculation will give the same results for QPSK, 16-QAM and 64-QAM.

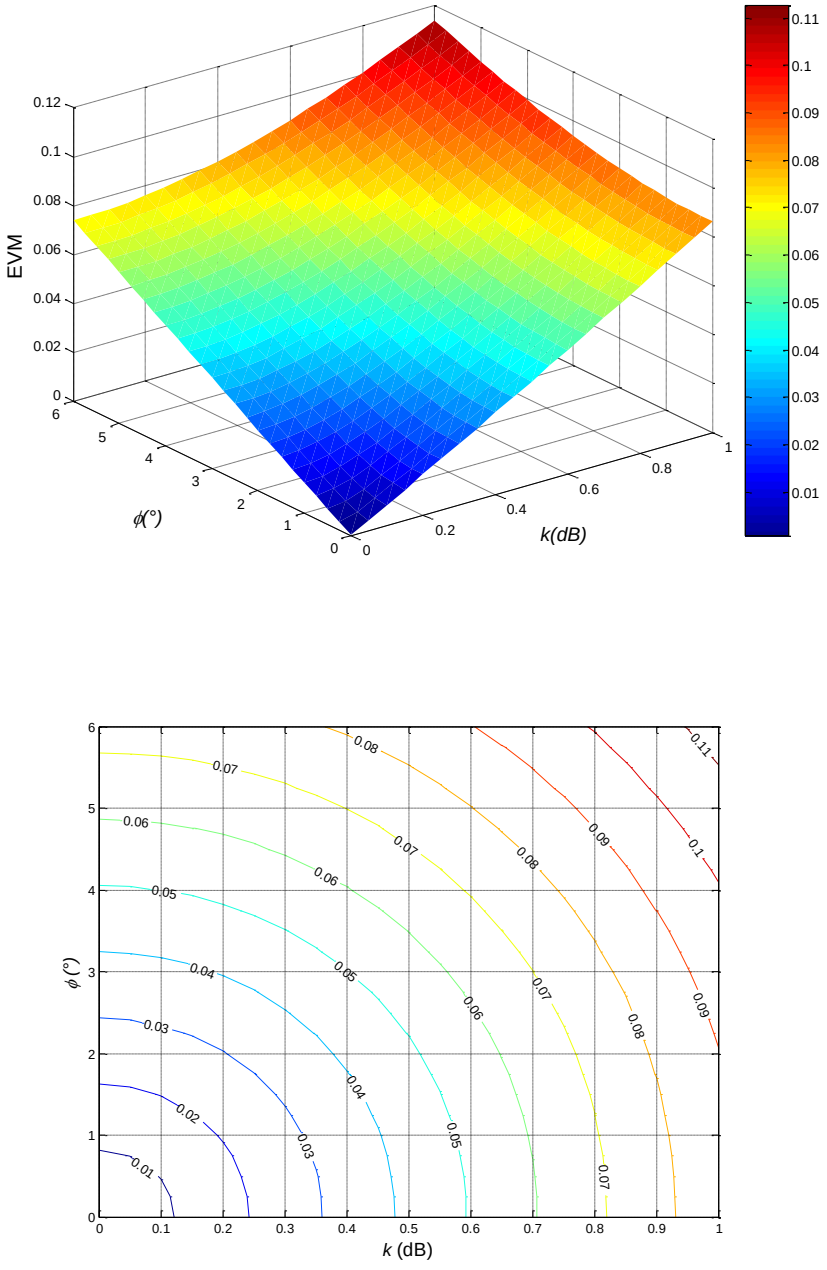


Figure 3-9 EVM variation with the transmitter amplitude and phase imbalance for M-QAM. Left: 3-D diagram, right: 2-D contour.

Although the EVM calculation is not related to different modulations and gives the same result for different modulations, the SER calculation presents quite different results for different modulations. Because 64-QAM has much more points in constellation than QPSK, which means the decision zones of 64-QAM are much smaller than those of QPSK. Intuitively, if the same sample cloud is received for a certain point, more samples drop out of the decision zone and yield more error symbols for 64-QAM. Therefore, the SER of 64-QAM is more sensitive to each imperfection.

Figure 3-10 shows the SER variation with E_s/N_0 in which only the transmitter phase imbalance is considered. For SER of 10^{-4}, the 3° phase imbalance yields about 3dB degradation for 64-QAM, and about 1dB degradation for 16-QAM, but ignorable degradation for QPSK. The figure also shows that, if the phase imbalance is increased to a certain value, such as 44° for QPSK, 15° for 16-QAM and 7° for 64-QAM, the SER curve become almost flat in the low E_s/N_0 area. Those angles agree with half of the smallest angle difference between the points with the same amplitude in each modulation scheme , i.e., 45° for QPSK, 18.4° for 16-QAM and 8.1° for 64-QAM. Several data points obtained from the simulation are shown to verify the theoretical results.

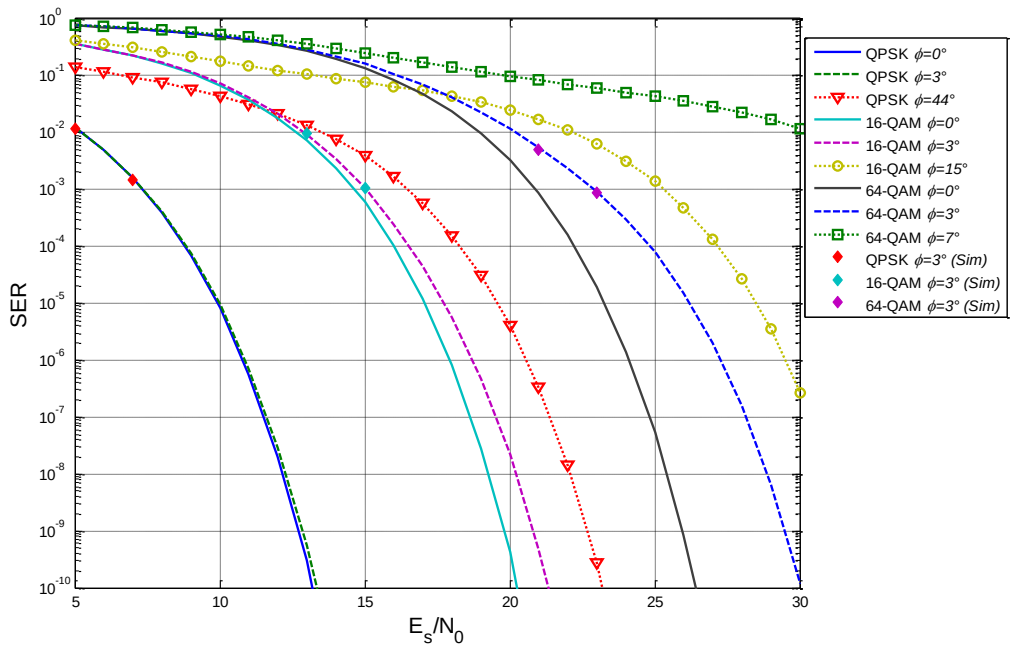


Figure 3-10 SER~E_s/N_0 with different transmitter phase imbalance for QPSK, 16-QAM and 64-QAM.

Figure 3-11 shows the SER variation with E_s/N_0 in which only the deterministic phase synchronization error, α_d, is considered. This figure gives similar curves with those from Figure 3-10. However, the angle in the phase synchronization error degrades the SER a little bit more than the same angle in transmitter phase imbalance.

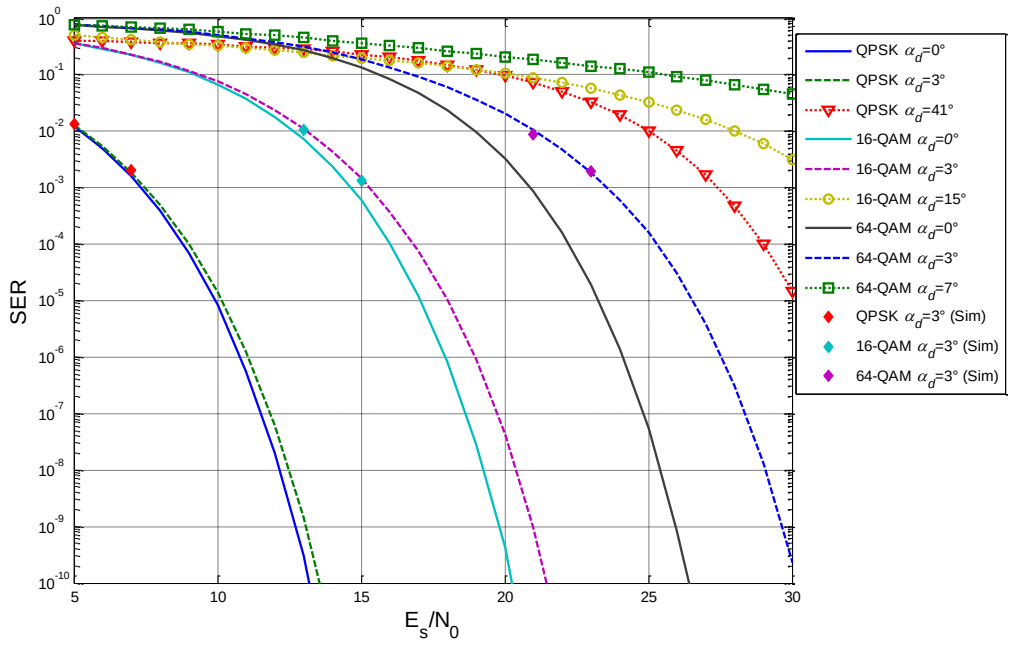


Figure 3-11 SER~E_s/N_0 with different phase synchronization error for QPSK, 16-QAM and 64-QAM.

Figure 3-12 considers only the phase noise contribution. It shows that the phase noise degrades the SER more than the phase imbalance and the deterministic phase synchronization error. The curves also show the noise floors which are related not only to the variance, α_{rms}, but also to the different modulation schemes. For the 64-QAM, the phase noise with 3° variance will yield a noise floor above 10^{-3} which is unacceptable for most systems. Therefore, the phase noise is the primary design consideration among the parameters discussed in this section for a system using 64-QAM. The last curve in the legend list is for 64-QAM with α_{rms}=0.5° which is typical phase noise coming from a WLAN synthesizer [41]. The result shows that this phase noise degrades the system performance less than 1dB.

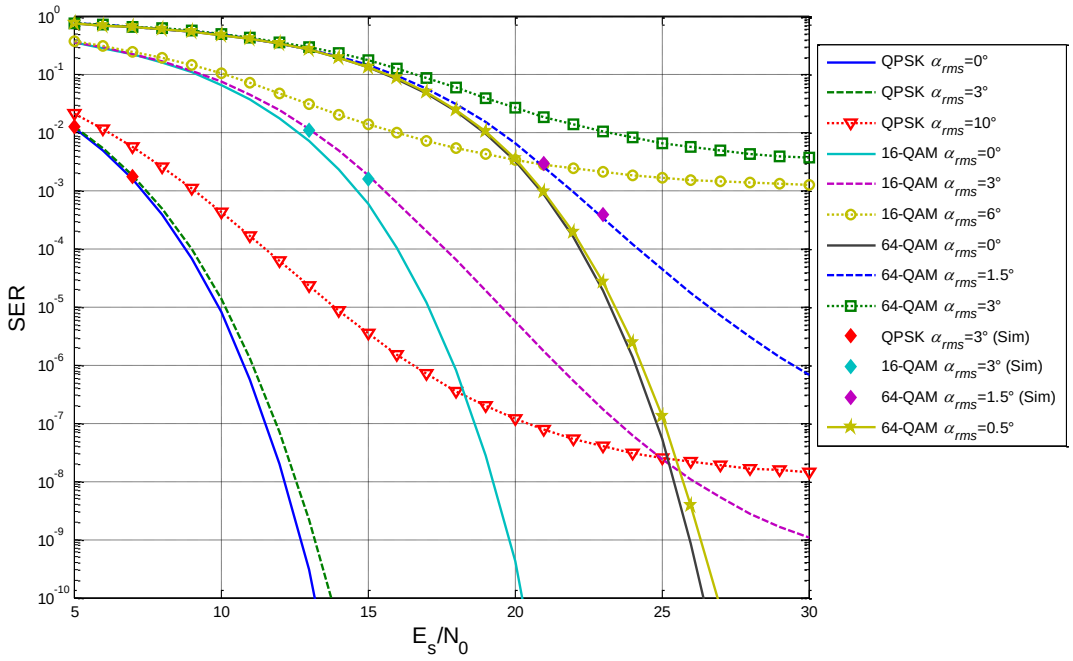


Figure 3-12 SER~E_s/N_0 with phase noise for QPSK, 16-QAM and 64-QAM.

If more than one parameter is considered, the results will be much more complicated and can hardly be shown in one plot. For a real system design, usually, a specific system performance is required. And under this system requirements the contribution of each component in the system is investigated and the link budget is calculated and distributed to each component. In Figure 3-13, a simple example is shown for a system using 64-QAM and requiring SER performance of 10^{-4}, which is a typical requirement for a wireless communication system. The 3-dimensional surface shows the minimum E_s/N_0 to achieve the SER requirement with the presence of phase noise and phase synchronization error.

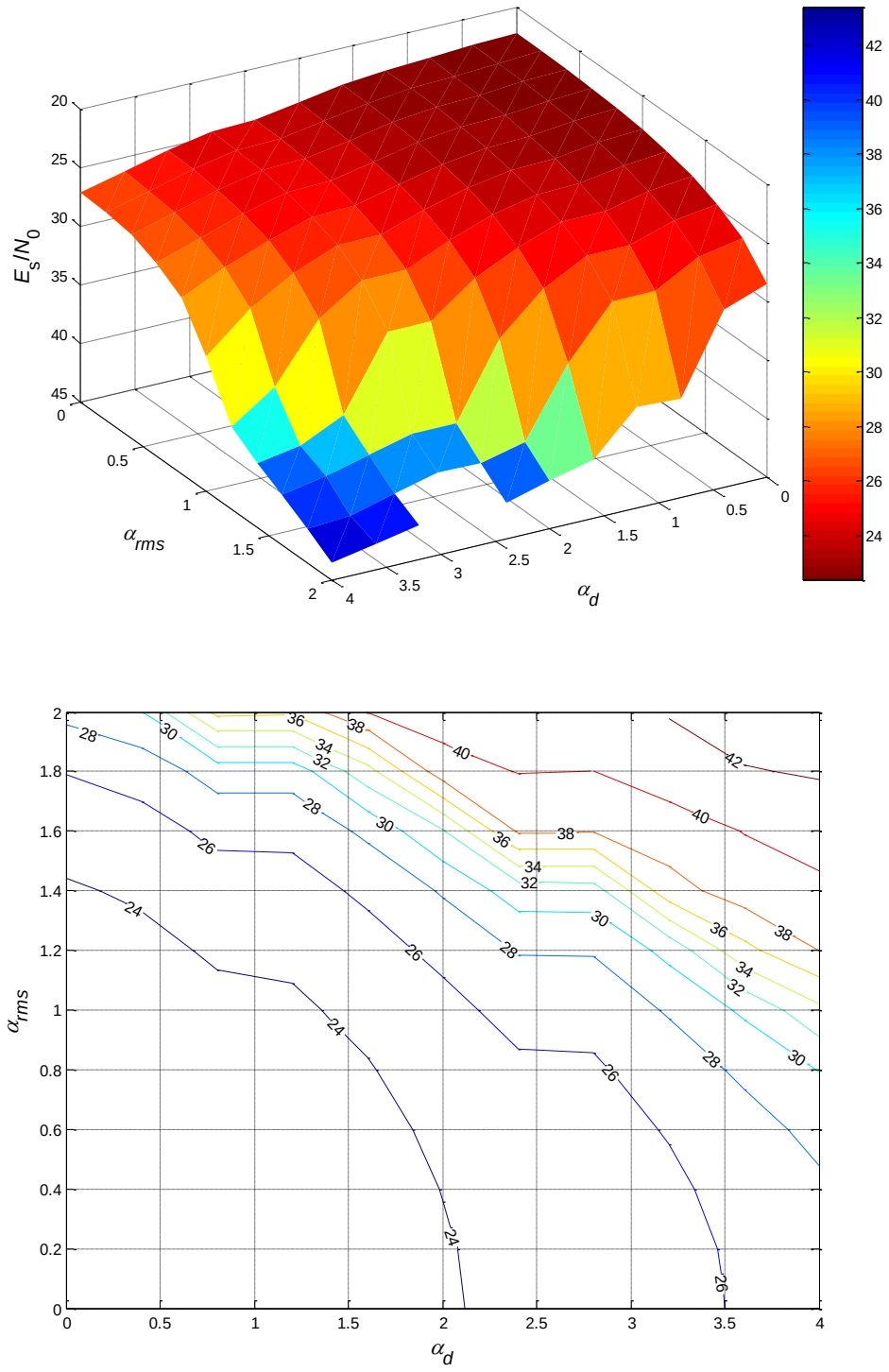


Figure 3-13 E_s/N_0 requirement for 10^{-4} SER with phase noise and phase synchronization error.

Left: 3-D diagram, right: 2-D contour.

In another case, for a WLAN system using 64-QAM, assuming that channel noise can be neglected, synchronization is ideal, and the transmitter and the receiver have the same imbalances, the proposed theoretical model can be used to find the maximum tolerable phase and amplitude imbalance and LO phase noise for a typical system requirement of SER=10^{-4}. The results are shown in Figure 3-14, which provide an efficient means for system and circuit designers to find a proper tradeoff between the imbalances and the phase noise requirements.

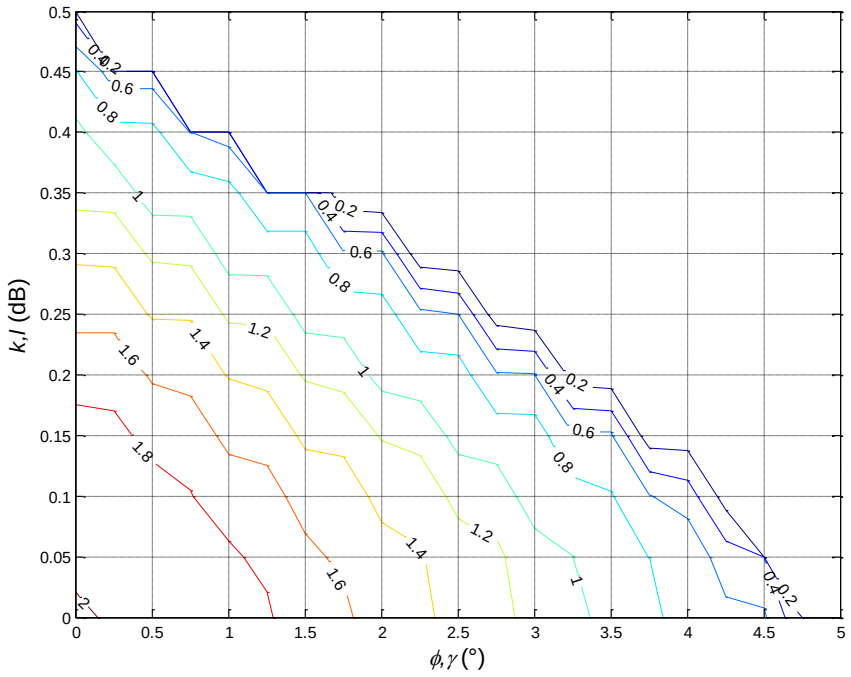


Figure 3-14 Tolerable phase and amplitude imbalance and LO phase noise for SER=10^{-4} in a 64-QAM WLAN system.

3.7 Conclusions

In the chapter, a theoretical analysis of the joint effects of the transmitter and the receiver phase and amplitude imbalance, phase noise and channel noise on M-QAM systems has been

presented. An analytic expression for EVM and an integral expression for SER have been derived in (3.36) and (3.40), which provides an efficient means to specify the wireless system and block requirements considering the effects of those imperfections on the system performance. The analysis shows that the 64-QAM is very sensitive to the phase noise and other system imperfections. Therefore, the link budget should be carefully considered and distributed to each component for a 64-QAM system. The analytical results are also compared with time-consuming Monte-Carlo simulation results and show a good agreement. For a more complete system analysis, the nonlinearity of the RF amplifier and multi-path fading channel should be considered. This could be the subject for the future work.

3.8 Calculation Approach for Channel Noise Covariance Matrix

Assuming an ideal low pass filter (LPF) which has the pass bandwidth of B and the impulse response of $h(t)$, the received noise in two channels then can be expressed as

$$\begin{aligned} n_i(t) &= l\left[n(t)\cos(\omega t+\alpha)\right]\otimes h(t) \\ &= l\int_{\tau=0}^{+\infty} n(t-\tau)\cos(\omega t-\omega\tau+\alpha)h(\tau)\,d\tau, \\ n_q(t) &= \left[n(t)\sin(\omega t+\alpha+\gamma)\right]\otimes h(t) \\ &= \int_{\tau=0}^{+\infty} n(t-\tau)\sin(\omega t-\omega\tau+\alpha+\gamma)h(\tau)\,d\tau, \end{aligned} \tag{3.46}$$

where $\mathbf{n}_r(t) \square \left[n_i(t),\ n_q(t)\right]^{\mathrm{T}}$, $\otimes$ denotes convolution, $n(t)$ is the white Gaussian noise in channel which has the double side PSD of $N_0/2$. Then each element in the covariance matrix is obtained as following

$$
\begin{aligned}
E\left[n_i^2(t)\right] &= l^2 E\left[\int_{\tau=-\infty}^{+\infty} n(t-\tau)\cos(\omega t-\omega\tau+\alpha)h(\tau)d\tau \int_{\xi=-\infty}^{+\infty} n(t-\xi)\cos(\omega t-\omega\xi+\alpha)h(\xi)d\xi\right] \\
&= l^2 \int_{\tau=-\infty}^{+\infty}\int_{\xi=-\infty}^{+\infty} E\left[n(t-\xi)n(t-\tau)\right]\cos(\omega t-\omega\xi+\alpha)\cos(\omega t-\omega\tau+\alpha)h(\xi)h(\tau)d\xi d\tau \\
&= l^2 \int_{\tau=-\infty}^{+\infty}\int_{\xi=-\infty}^{+\infty} \frac{N_0}{2}\delta(\xi-\tau)\cos(\omega t-\omega\xi+\alpha)\cos(\omega t-\omega\tau+\alpha)h(\xi)h(\tau)d\xi d\tau \\
&= l^2 \frac{N_0}{2}\int_{\tau=-\infty}^{+\infty}\left[\frac{1}{2}+\frac{1}{2}\cos(2\omega t-2\omega\tau+2\alpha)\right]h^2(\tau)d\tau \\
&= l^2 \frac{N_0}{4}\int_{\tau=-\infty}^{+\infty} h^2(\tau)d\tau + A_r^2 l^2 \frac{N_0}{4}\int_{\tau=-\infty}^{+\infty}\cos(2\omega t-2\omega\tau+2\alpha)h^2(\tau)d\tau \\
&= l^2 N_0 B/4
\end{aligned}
\tag{3.47}
$$

From the Plancherel's Theorem,

$$
\int_{\tau=-\infty}^{+\infty} h^2(\tau)d\tau = \int_{f=-\infty}^{+\infty}\left|H(f)\right|^2 df = B, \quad H(f)=\begin{cases}1, & |f|<B/2\\ 0, & \text{otherwise}\end{cases}
\tag{3.48}
$$

where $H(f)$ is the frequency response of the ideal LPF. And assuming the carrier frequency is much larger than the pass band of the LPF, $\omega \gg \pi B$, the integral $\int_{\tau=-\infty}^{+\infty}\cos(2\omega t-2\omega\tau+2\alpha)h^2(\tau)d\tau$ approximately equals to zero.

Similarly,

$$
\begin{aligned}
E\left[n_q^2(t)\right] &= E\left[\int_{\tau=0}^{+\infty} n(t-\tau)\sin(\omega t-\omega\tau+\alpha+\gamma)h(\tau)d\tau \int_{\xi=0}^{+\infty} n(t-\xi)\sin(\omega t-\omega\xi+\alpha+\gamma)h(\xi)d\xi\right] \\
&= N_0 B/4.
\end{aligned}
\tag{3.49}
$$

And,

$$
\begin{aligned}
E\left[n_i(t)n_q(t)\right] &= lE\left[\int_{\tau=0}^{+\infty} n(t-\tau)\cos(\omega t-\omega\tau+\alpha)h(\tau)d\tau \int_{\xi=0}^{+\infty} n(t-\xi)\sin(\omega t-\omega\xi+\alpha+\gamma)h(\xi)d\xi\right] \\
&= \frac{lN_0}{2}\int_{\tau=0}^{+\infty}\left[\frac{1}{2}\sin(2\omega t-2\omega\tau+2\alpha+\gamma)+\frac{1}{2}\sin(\gamma)\right]h^2(\tau)d\tau \\
&= \frac{lN_0B}{4}\sin(\gamma)
\end{aligned}
\tag{3.50}
$$

From (3.47), (3.49) and (3.50), the covariance matrix is expressed as

$$
\mathbf{C}_{\mathbf{n}_i\mathbf{n}_r} = \frac{N_0B}{4}\begin{bmatrix} l^2 & l\sin(\gamma) \\ l\sin(\gamma) & 1 \end{bmatrix}, \tag{3.51}
$$

Chapter 4 Data Converters for SDR

4.1 Design Challenge of Data Converters for SDR

SDR intends to use software/firmware code or reconfigurable digital design blocks to replace analog and RF blocks in a transceiver system. Therefore, high-speed, high-resolution data converters are one of the most important enabling technologies to realize an SDR system and push the boundary between digital and analog towards the antenna. An SDR transceiver presents design challenges to data converters such as high conversion rate and high dynamic range. Other practical considerations for using high-speed high-resolution data converters in a SDR system are the power consumption and the cost.

4.2 A 3mW 8-Bit Low-Power RHBD DAC for Cryogenic Applications from -180°C to 120°C

As an example, this section presents an 8-bit low power digital to analog converter (DAC) with radiation-hardened-by-design (RHBD) for cryogenic applications. It is not an ideal high-speed high-resolution DAC design for SDR. However, as a part of a NASA funded project, this design is a showcase for the design of high performance data converters.

This cryogenic DAC design has been implemented using the CMOS part of a 0.5μm SiGe BiCMOS technology. It is capable of operating over an ultra-wide temperature (UWT) range from -180 °C to +120 °C and under the high-energy particle radiation environment of the lunar surface.

A segmented R-2R binary code with a thermometer code architecture is used for the DAC core. A sophisticated quadrature symmetric layout for the DAC core is implemented to improve the matching. The DAC achieves a measured differential nonlinearity by integral nonlinearity (DNL/INL) of ±0.2/0.3 least significant bit (LSB) at 27^{o}C and ±0.6/0.9 LSB at -180 ^{o}C. Power consumption is highly optimized to be 3mW. The whole DAC design takes 0.25mm^{2} die area.

4.2.1 Introduction

With the development of aerospace exploration, the considerations for extreme environments have been included more comprehensively into most designs related to aerospace engineering. The extreme environment elements, such as temperature, radiation, pressure, vibration, etc, will easily preclude the use of conventional terrestrial engineering designs for operation, actuation and movement under ambient conditions. Although the moon is relatively close to the earth and the radiation level there is not too high, the extreme temperature conditions on the lunar surface can still invalidate conventional electronic components and systems for control, sensing, and communications. This would be a problem, since the development of modular, expandable, and reconfigurable human and robotics systems for the lunar missions clearly requires electronic components and integrated packaged electronics modules that can operate robustly without external thermal control.

For the use on the NASA Lunar-Mars series of missions, a data acquisition system is being developed. The unit will accept inputs from multiple types of sensors, employing three types of input channels that each incorporates programmable elements to accommodate a wider variety of input signals. The extreme space environment of those projects gives tough challenges

to even aging circuit technologies. This section presents an 8-bit DAC, which is a key part of the NASA data acquisition system for a sense-and-control circuit. To save the precious energy and weight in space equipment, this DAC is required to be optimized for low power and small size. Although the speed of this DAC is not a big concern, linearity and power consumption are crucial for the NASA application. Moreover, this design has to operate in extreme temperature and the radiation environments.

The chosen SiGe BiCMOS technology for this design inherently provides both novel bipolar devices (SiGe HBTs) and Si CMOS. Unlike conventional Si transistors, SiGe HBTs are very well suited for operation in the lunar environment [47]. The addition of Ge allows tailoring of the device bandgap, which can be used to optimize the device behavior as a function of temperature. SiGe BiCMOS offers unparalleled low temperature performance, wide temperature capability, and optimal mixed-signal design flexibility at the monolithic level by offering power efficient, high speed SiGe HBTs and high density Si CMOS [47][48].

4.2.2 Circuit Design

This cryogenic DAC comprises a segmented R-2R 8-bit DAC core, a digital logic part, an ultra-wide temperature (UWT) band-gap reference and a differential to single output convertor.

By considering the low power requirement and the extreme application environment, an R-2R resistor ladder structure is selected for the design. This structure is more robust than other DAC structures because of its simplicity and fewer active components. It also consumes less current then the current-steering DAC structure by using only one current source and by having smaller current for the LSB branch. The design's coding approach is a hybrid of a binary code and a thermometer code. When a binary code is used for all 8 bits, the switching of the MSB will

introduce a large glitch and therefore excessive DNL error on the output signal during the transition time. Using a thermometer code can reduce the output glitch and also relax the matching but a thermometer code occupies more area. To balance the tradeoffs, this DAC is segmented to represent the 5 LSBs with R-2R binary codes and to represent the 3 most significant-bits (MSBs) with a thermometer code, as shown in Figure 4-1.

On one side, to achieve the low power design requirement, only 400μA total is designed to be supplied to the R-2R resistor ladder. The divided current drawn on the LSB branch is less than 2μA, which is a big challenge for design mismatch and balance. On the other side, the value of the resistors used in the R-2R resistor ladder is limited for small area requirement. Therefore, the matching issue is a significant challenge for this design. To improve the matching and the linearity, all the resistors and most transistors used in the ladder are divided to the same size, and those resistors and transistors are then divided again into four parts to allow a quadrature layout style as shown in Figure 4-2. This technique compensates for the effects of gradients or other systematic mismatches [49][50].The measurement results in Sector 4.2.4 show good linearity achieved by these design considerations.

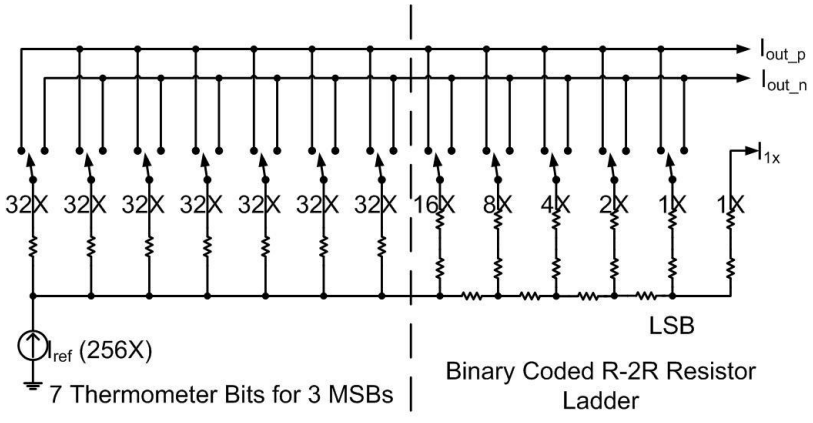


Figure 4-1 8-bit segmented architecture for the DAC core.

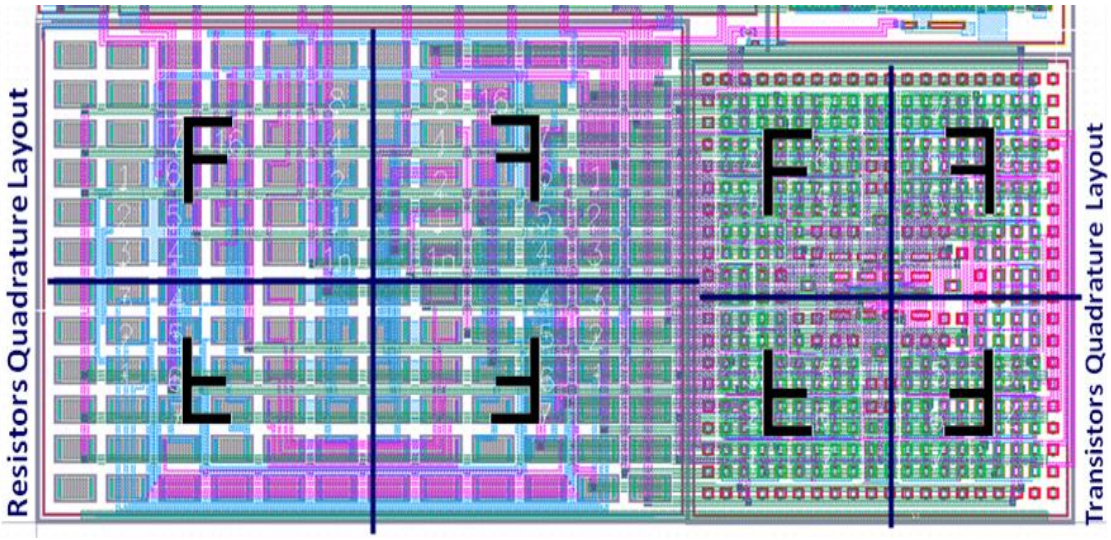
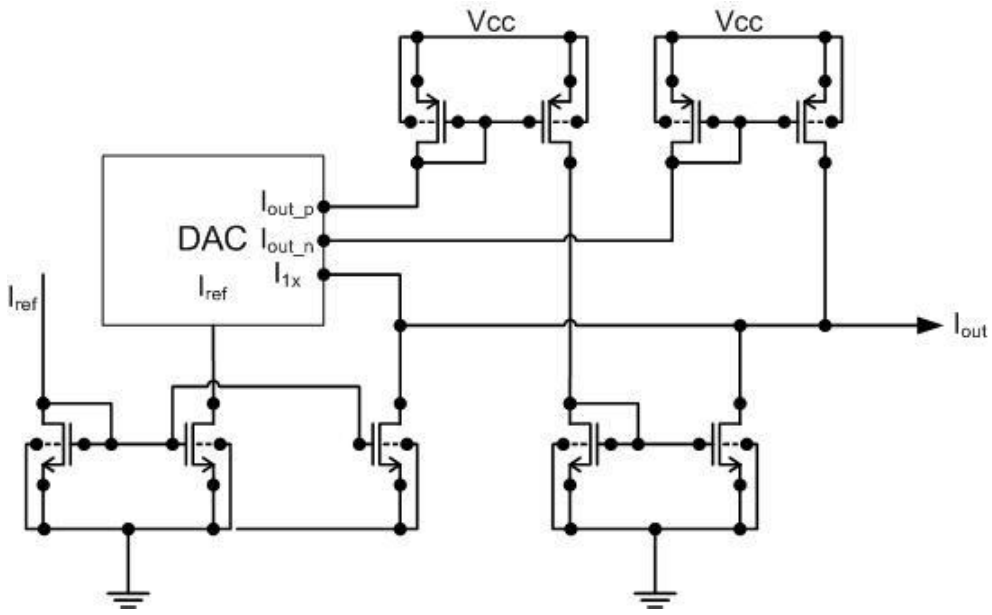


Figure 4-2 Quadrature layout for resistors and transistors.

The digital logic part of the DAC includes a thermometer decoder, which converts 3 binary MSBs to 7 thermometer code and clocked input buffers for the input bits of the DAC.

As shown in Figure 4-3, by using several accurate cascode current mirrors to realize the current addition and subtraction, the output convertor converts the differential current output from the DAC to a single current output with full swing from 0μmA to 32μmA, which is required by the NASA project architecture. The output current signal is centered on the DC current of Iref. As shown in Figure 4-1, the reference current source for the DAC provides 256 times LSB current while the full swing output of both positive and negative differential outputs are 255 times LSB current. Therefore, to reach 0μA as the lower bound of the single output swing, the amount of the current on one LSB branch is output from the DAC and subtracted from the output current.



$$I_{out} = I_{ref} + I_{out\_p} - I_{out\_n} - I_{1x}$$

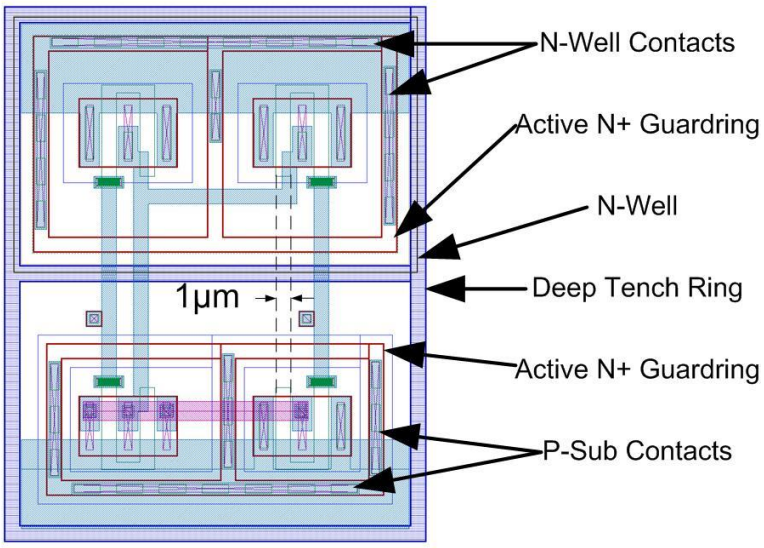
Figure 4-3 Current differential to single output convertor. (cascode transistors are not shown in figure for simplification)

A UWT band gap reference is used and tuned to give a constant current output in the UWT range [51]. In the post-simulation, the temperature coefficient is less than 40ppm from -180 °C to 120 °C with full swing output.

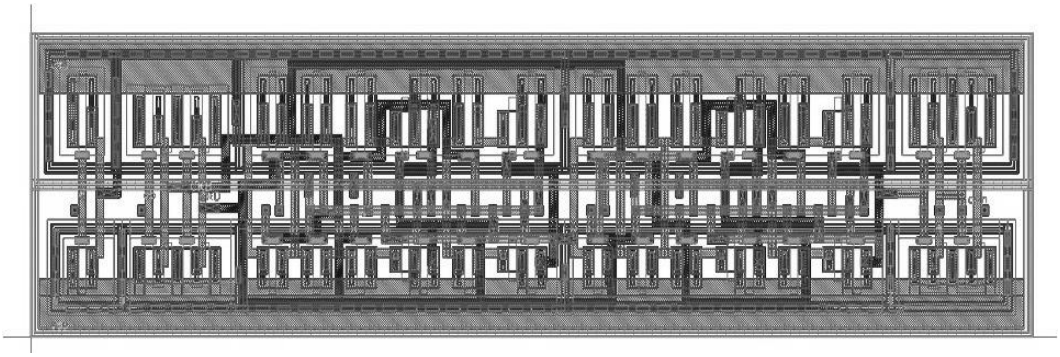
4.2.3 Radiation Hardened by Design

To improve the robustness in high radiation environments: the minimal transistor width is chosen as 1μm other than the default 0.5μm. In addition, to prevent a single event latch-up caused by the positive feedback formed in the parasitic transistors, special RHBD layout rules are applied in this design to reduce the well/substrate parasitic resistance and reduce the gain product of the parasitic NPN/PNP pairs. The RHBD rules include: active N+ (P+) guard rings are added around PMOS (NMOS); n-well and p-sub contacts are generously and frequently used;

deep trench rings are added for isolation between PMOSs and NMOSs; keep n-well and n+ source/drain father apart if possible [52].



(a)



(b)

Figure 4-4 (a) NAND gate by RHBD layout rules; (b) D-flip-flop by RHBD layout rules

Two example cells of RHBD layout in this design is shown in Figure 4-4. As shown in Figure 4-4 (a), by using those RHBD layout rules, the die size of this design is enlarged by

several times compared with the normal layout without the RHBD consideration. As shown in Figure 4-4 (b), NFETs and PFETs are grouped by function with active N+(P+) guard rings which reduce the area punishment by applying RHBD layout rules. This design still results in relatively small area compared with similar works by choosing the suitable circuit architecture and a good layout floor plan.

4.2.4 Measured Results

The die photo of this DAC design is shown in Figure 4-5. The active area is 0.55×0.45mm2 and the DAC core takes 0.55×0.25mm2.

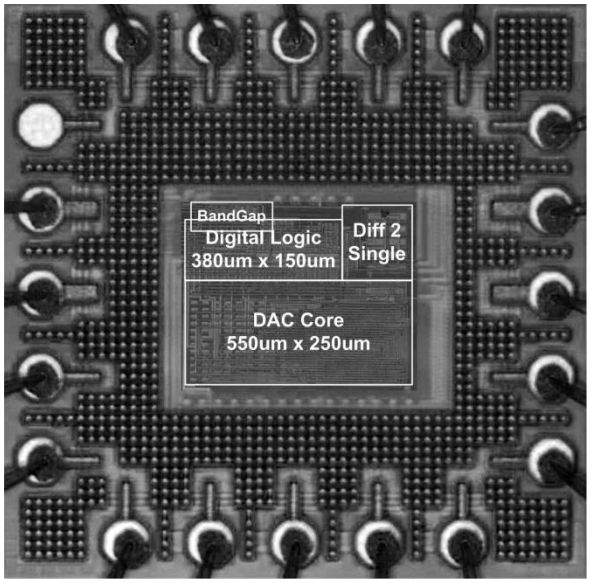


Figure 4-5 Die photo of the 8-bit cryogenic DAC.

Figure 4-6 shows the measured DNL/INL performance. With the matching considerations in the circuit design and layout, especially the effort of quadrature layout, this design achieves the DNL/INL of ±0.2/0.3 at room temperature which is a good result for a low-

power DAC without any calibration method compared with others work. Expecting the one big spike in the DNL figure, the DNL for other codes is around ±0.1.

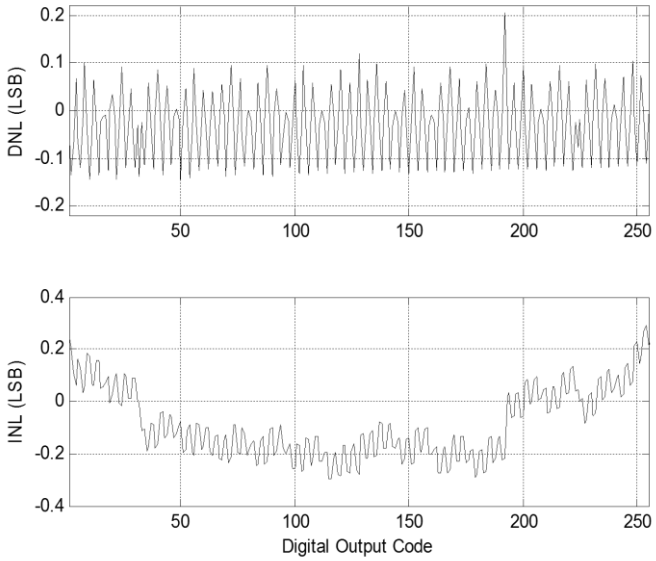


Figure 4-6 Measured INL and DNL at 27 ^{o}C temperature.

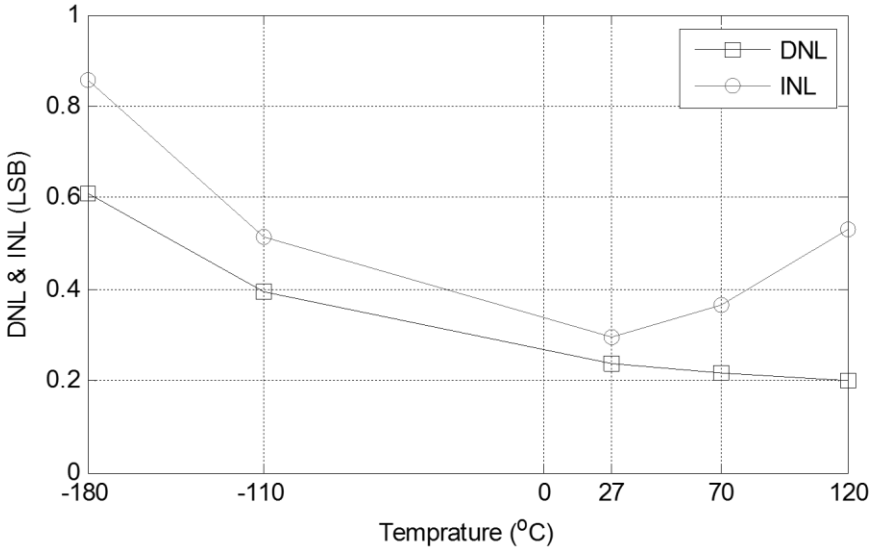


Figure 4-7 Measured DNL and INL at from -180 ^{o}C to 120 ^{o}C temperature.

The DAC is tested in UWT environment with the temperature from -180 ºC to 120 ºC. Figure 4-7 shows the measured DNL/INL performance over the UWT range. At -180ºC, the DNL/INL gets to ±0.6/0.85 LSB, still less than ±1 LSB, which is in the acceptable range. At 120 ºC, the DNL/INL gets to ±0.2/0.53 LSB, slightly degraded from the room temperature performance. The INL curve shows the best performance at room temperature for the matching of the design being tuned best at 27 ºC.

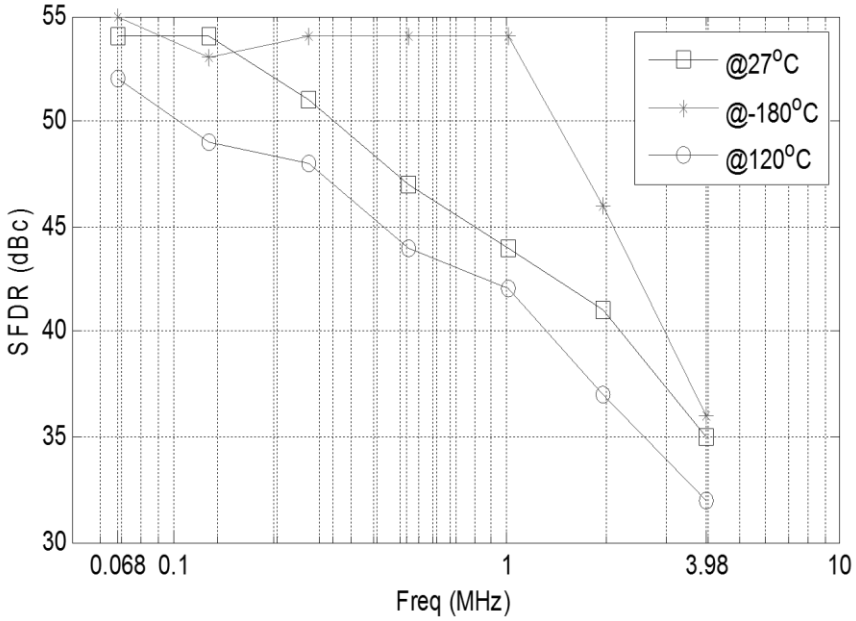


Figure 4-8 Measured SFDR at -180 ºC to 120 ºC temperature.

Figure 4-8 shows the measured SFDR performance over the UWT range. The SFDR performance is given up to Nyquist frequency in three curves representing -180 ºC, 27 ºC and 120 ºC respectively. As shown in the figure, SFDR is improved at a low temperature of -180 ºC for around 4dB compared with room temperature. In addition, it is degraded at a high temperature of 120 ºC. However, at both -180 ºC and 120 ºC, the SFDR can get comparable

performance as the maximum performance of 55dB as achieved at room temperature. A summary of measured performance is listed in the Table 4-1.

Table 4-1 Summary of Measured DAC Performance

Parameter	Performance
Technology	0.5μm SiGe BiCMOS
Temperature	-180°C ~ 120°C
Resolution	8
Conversion Type	Segmented R-2R and Thermometer
Maximal	10 MS/s
Full-scale output	Differential 200uA; Single 32uA
SFDR	55dBc@63k,10MS/s 27°C
DNL/INL	±0.22/0.3 at 27°C
Power Supply	3.3 V
Power dissipation	3 mW @ 10 MS/s
Die Size	0.55×0.45 mm2

4.2.5 Conclusion

A low power 8-bit DAC for cryogenic applications was developed with the improvements on matching, low power dissipation and die size optimization. Special design considerations were given for the radiation and cryogenic environment. The measured results show that the DAC achieves DNL/INL of ±0.6/0.85 LSB over the UWT temperature range that meets the NASA requirements.

Chapter 5 Fully Reconfigurable Switch Capacitor Filter Design for SDR

5.1 Motivations and Challenges on Frequency Selectivity for SDR

Nowadays, typical smartphones need to support multiple communication standards, e.g. GSM, cdma1x, CDMA, UMTS, LTE, WiFi, Bluetooth and GPS. Additionally, smartphones need to support many different bands. Just for the mobile 4G-LTE standard, there are more than 40 different frequency bands defined within the frequency range from 700MHz to 2.7GHz with bandwidths ranging from 5MHz to 200MHz. Furthermore, RF frequency resources have been reallocated from other application fields to emerging mobile standards. Consequently, frequency selectivity has become the hardest challenge in the RF front-end design for smartphones. Traditionally, surface acoustic wave (SAW) or bulk acoustic wave (BAW) filters are chose for the frequency selectivities in a smartphone radio system for their high quality, high linearity, low noise and good low cost. However, for a premier smartphone to support multi-standard and multi-band, there are normally from 40 to up to 100 different SAW/BAW filters, diplexers, and quadplexer, which cost more than half of the total bill of material (BOM) of the entire RF front-end system. Multi-standard, multi-mode and multi-band mobile system also results in very sophisticated RF design, which has to overcome high RF path loss and are facing many design challenges including isolation and interference tolerance.

An SDR system is an ideal solution for multi-standard, multi-mode and multi-band system, which enables a much simpler, more flexible and reconfigurable design. Ideally, if the

data converters in the SDR system have very high, close to the RF frequency, bandwidth, the RF signal can be fully converted to digital signal and the most required frequency selectivities can be realized with several reconfigurable and programmable digital filters in the digital domain. Several SDR analog filters and SDR digital filters can then replace big amount of SAW/BAW filters. Latest research and development have realized data converters [53][54][55] working at clock frequencies beyond 10G sample per second. Nevertheless, those state-of-the-art high-speed data converters consume very high power, leading to shortened talk-time in a battery-powered mobile system, and take large die area, i.e. the cost. Consequently, they are currently not feasible choices for any commercial system. Moreover, the latest standard development for both WiFi and 5G cellular is pushing the carrier frequency high as 28GHz, 60GHz or even higher with much wider signal bandwidth. With this continuing trend, there will not be a data converter with bandwidth comparable to RF bandwidth, which also has competitive power consumption and cost in a foreseeable future.

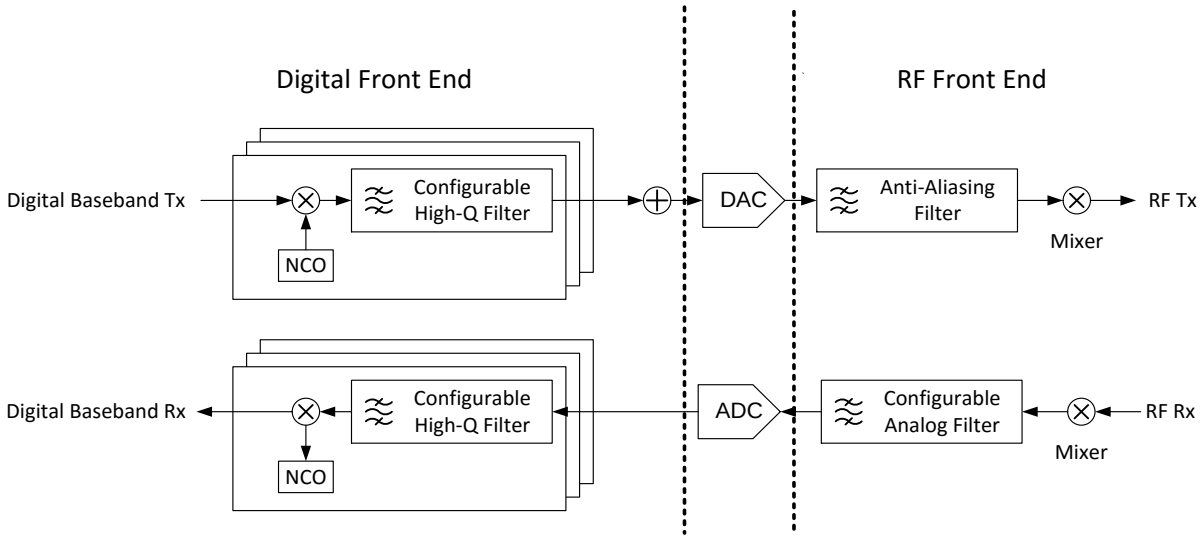


Figure 5-1 SDR Tx signal chain with reconfigurable analog/RF filter

From the proposed practical SDR architecture in Chapter 2, a detailed diagram of the signal filtering is shown in Figure 5-1. On the Tx side, the frequency selectivity can be implemented separately with narrow band, high-Q digital filters before the data converters and simple low-Q analog anti-aliasing filter after data converter. Therefore, multi-mode multi-channel Tx signals have be mixed to different intermediate carrier frequencies and merged together after digital high-Q filter before the DAC. Since the required high-Q frequency selectivities are implemented in digital circuitries, the Tx RF front-end design will be greatly simplified with much fewer number of SAW filters compared to the conventional design.

On the Rx side, the ADC design is one of the most challenge blocks, which dictates the signal bandwidth and dynamic range of the signal that converted from the analog domain to the digital domain. The figure of merit (FOM) for an ADC is defined as $FOM = P/(f_s \times 2^{ENOB})$[56]. For a multi-mode multi-channel SDR receiver, a very high sample rate is normally required from the ADC to cover a wide bandwidth for a multi-mode multi-channel signal. Therefore, the effective number of bits for the ADC will be limited. To relax the ADC design requirements, a reconfigurable analog filter working for both anti-aliasing and band selectivity is a key design block on the Rx path before the ADC.

This section presents a finite-impulse-response (FIR) filter implemented in the analog domain with fully reconfigurable 15 taps programmed by 5-bit filter coefficients. This design is implemented in a 0.18μm CMOS technology. Binary coded capacitor banks and digitally controlled switches are used to realize the arithmetic functions of the FIR filter. As a prototype design, the filter coefficients' control bits are directly input from the input pins, which can be later implemented with software controlled internal memory or a register cluster. With the fully

arbitrary programmable filter coefficients, this FIR filter can realize different filter characteristics such as low pass filter (LPF), band pass filter (BPF) or high pass filter (HPF) with different bandwidths and center frequencies. This design can also be reconfigured to different FIR architectures or different combined N-path filters.

5.2 Fully-Reconfigurable Switch Capacitor FIR Filter for SDR

5.2.1 Introduction

For SDR transceivers, the filters are one of the key components. A reconfigurable analog filter enables the possibility to implement an SDR transceiver without using an ultra-high speed ADC, which reduces power consumption and die area cost. For the selectivity after the LNA on the Rx chain, an analog SDR low pass filter has been proposed with stacked blocks of a sampler, a Sinc FIR filter, couple of RC stages and a tunable decimator [18]. Recently, reconfigurable N-path band pass filters have been developed to replace the fixed band SAW filters [57][58][59]. All those reconfigurable filters proposed for SDR have focused on select one signal channel with tunable bandwidth. A SDR system, however, normally being required support multi-mode applications, needs to receive a signal with coexisted multiple signal bands. Consequently, the reconfigurability for a SDR filter need to be further enhanced those existed to support multi-band band pass filtering or equalizing signal powers among coexisted different signal bands. This section proposes a novel analog FIR filter with fully software reconfigurable filter coefficients, which can support wideband filtering with flexible low-pass, high-pass or band-pass frequency responses.

5.2.2 Circuit Design

The most basic design block for this software reconfigurable analog filter is a capacitor voltage sampler as shown in Figure 5-2. A pair of high speed CMOS switches is connected to the top node of the sampling capacitor. One serves as the input switch while another is used for the output. The switch transistor size is optimized and the sample capacitor size is minimized for fast response and high sample rate.

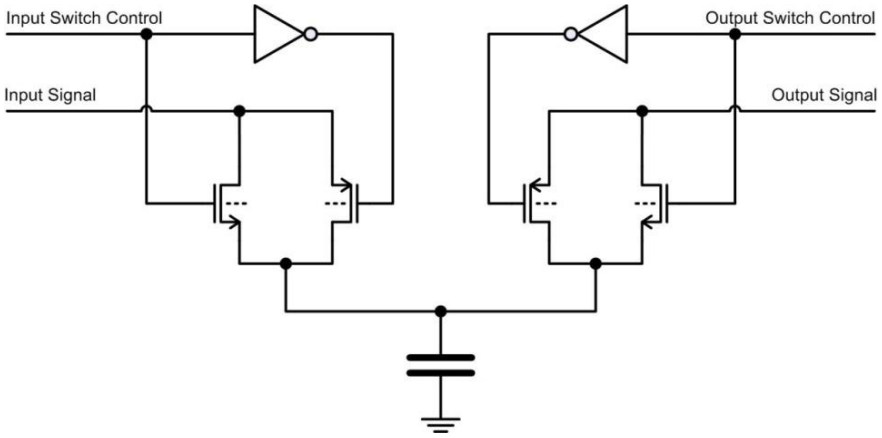


Figure 5-2 Basic switch capacitor voltage sampler cell

Each filter coefficient has 5 bits with one MSB for sign. So a coefficient can have any integer value in the range from -16 to 15. Five basic sampler cells with binary coded size compose a 5-bit binary coded capacitor sampler as shown in Figure 5-3. This 5-bit sampler is charged at the same time as the sampled voltage level. Differential input signals are required. MSB sampling capacitor is charged from the negative signal and 4 LBS sample capacitors are charged from positive signal. They will also be discharged at the same time but gated by the filter coefficient control bits.

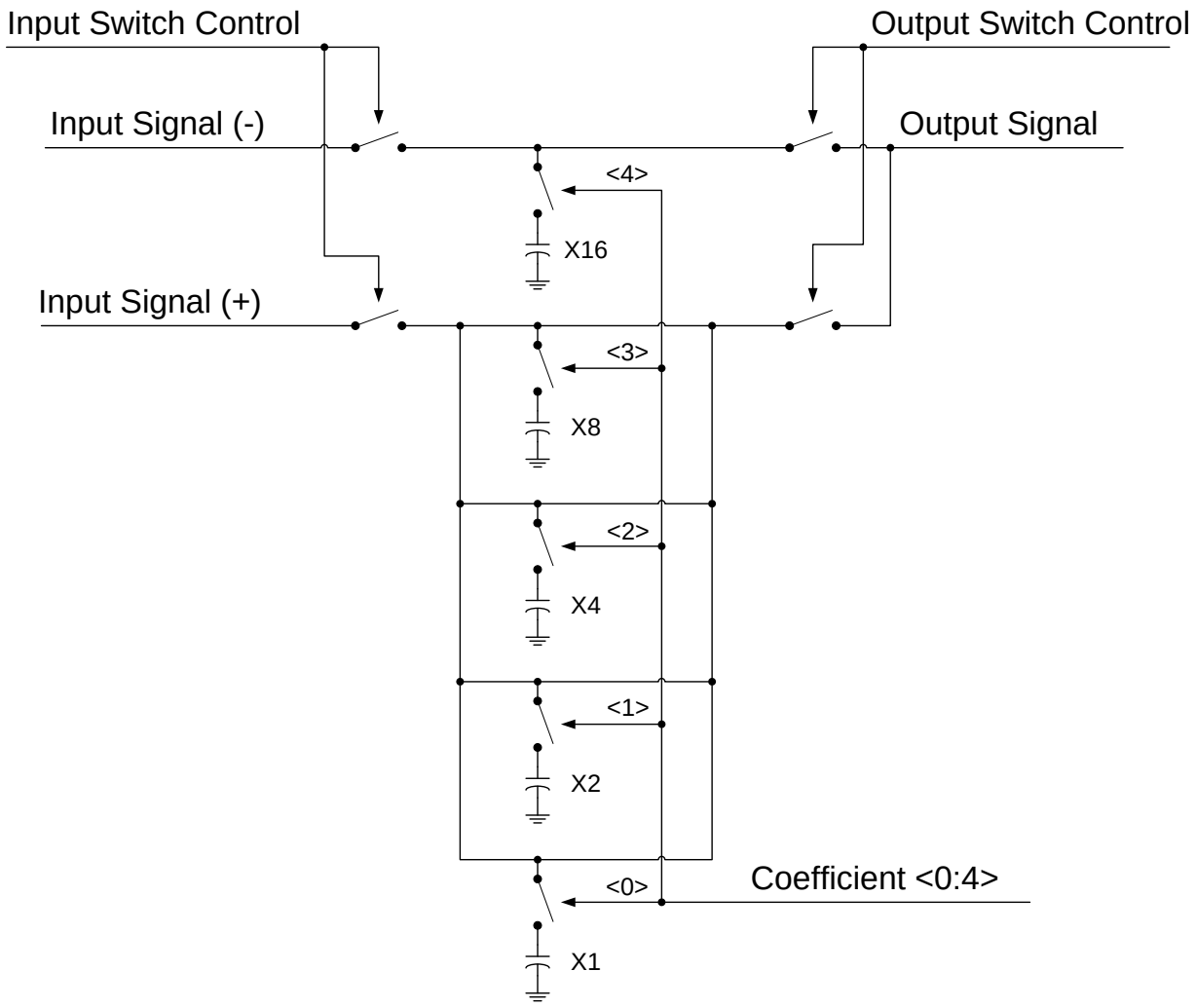


Figure 5-3 5-bit binary coded capacitor sampler schematic

Figure 5-4 shows the layout for the 5-bit binary coded capacitor sampler. All the switches and capacitors are divided to the same size as the LSB and then placed with quadrature symmetry. Two dummy cells are inserted in the middle to make it fully symmetric. By doing this special layout, mismatches between different bits are much reduced. Therefore, the filter quantization error is minimized.

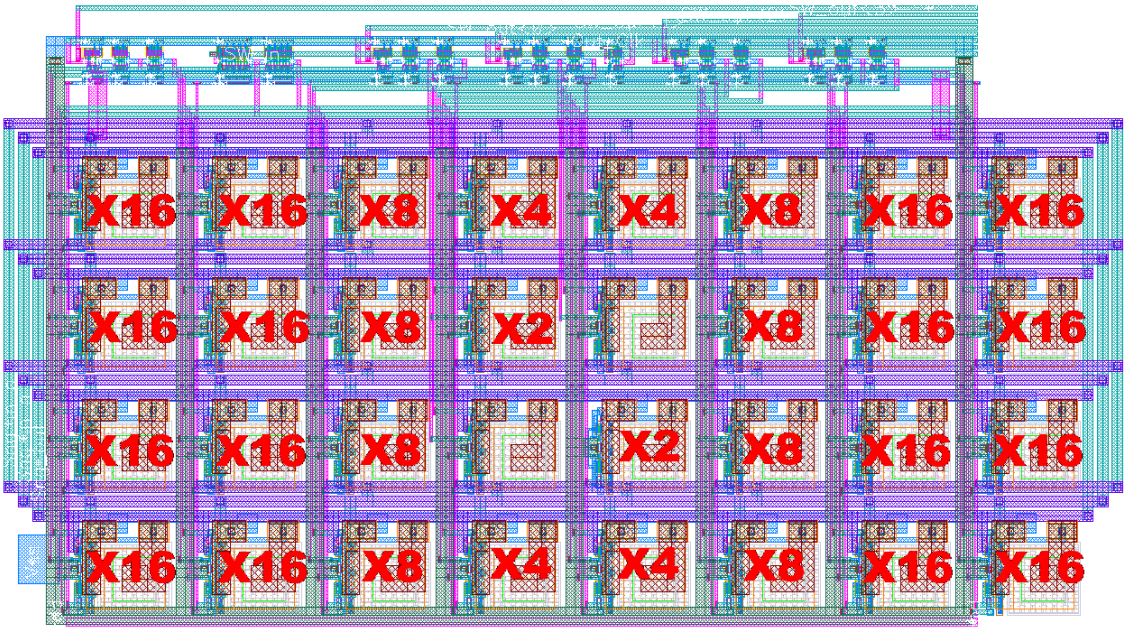


Figure 5-4 5-bit binary coded capacitor sampler layout

For most applications, linear phase is required for the filter. Therefore, 15 FIR coefficients are symmetric and noted as [h_1, h_2, h_3, h_4, h_5, h_6, h_7, h_8, h_7, h_6, h_5, h_4, h_3, h_2, h_1]. The 14^{th} order FIR filter transfer function in Z domain is defined as

$$H(Z) = \sum_{n=1}^{8} h_n Z^{-n} + \sum_{n=9}^{15} h_{16-n} Z^{-n} \tag{5.1}$$

Figure 5-5 shows 3 different example filter designs for low pass, high pass and band pass filter respectively with different 14^{th} order 5-bit integer FIR coefficients. As shown, this filter design is fully reconfigurable and can be software controlled to change the frequency selectivity on fly to be used in multi-mode, multi-channel receivers.

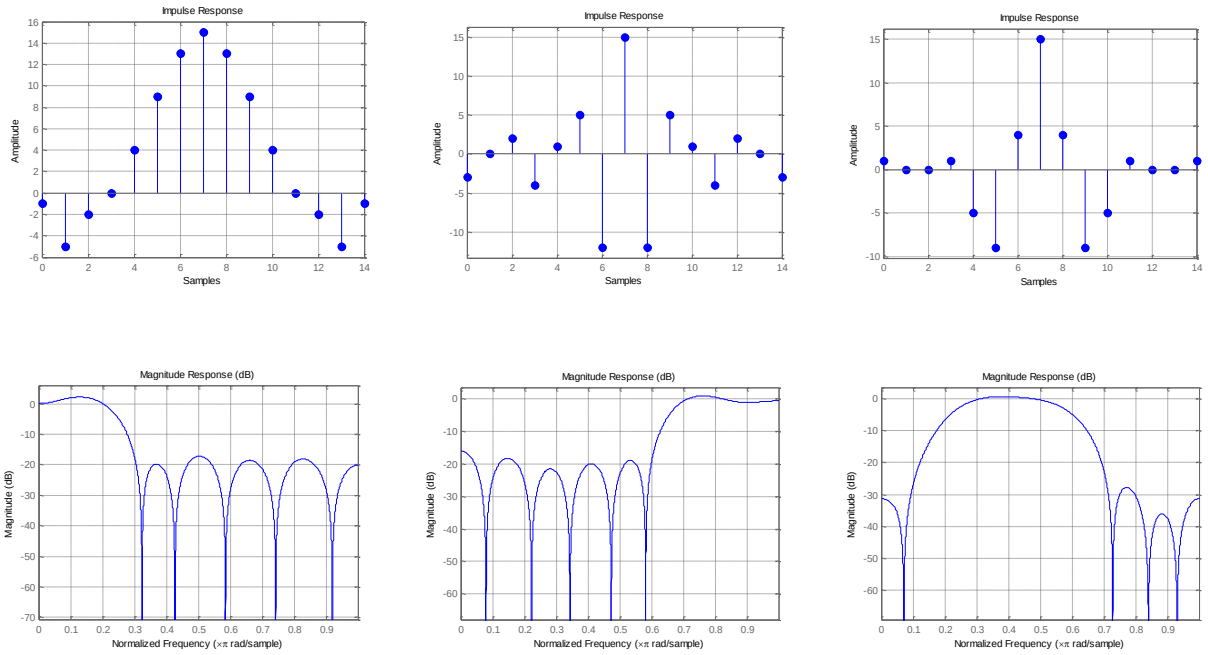


Figure 5-5 14th order 5-bit integer coefficient FIR filter impulse responses and frequency response

Figure 5-6 shows the architecture of the FIR filter design. There are total 20 delay blocks on the circle perimeter. After each delay block, there are 4 small blocks connected together with different filter coefficients labeled on. They will sample the input signal voltage simultaneously with a control clock pulse. Each block is a 5-bit binary coded capacitor sampler as shown in Figure 5-3. There are total 80 sampler blocks in the filter design.

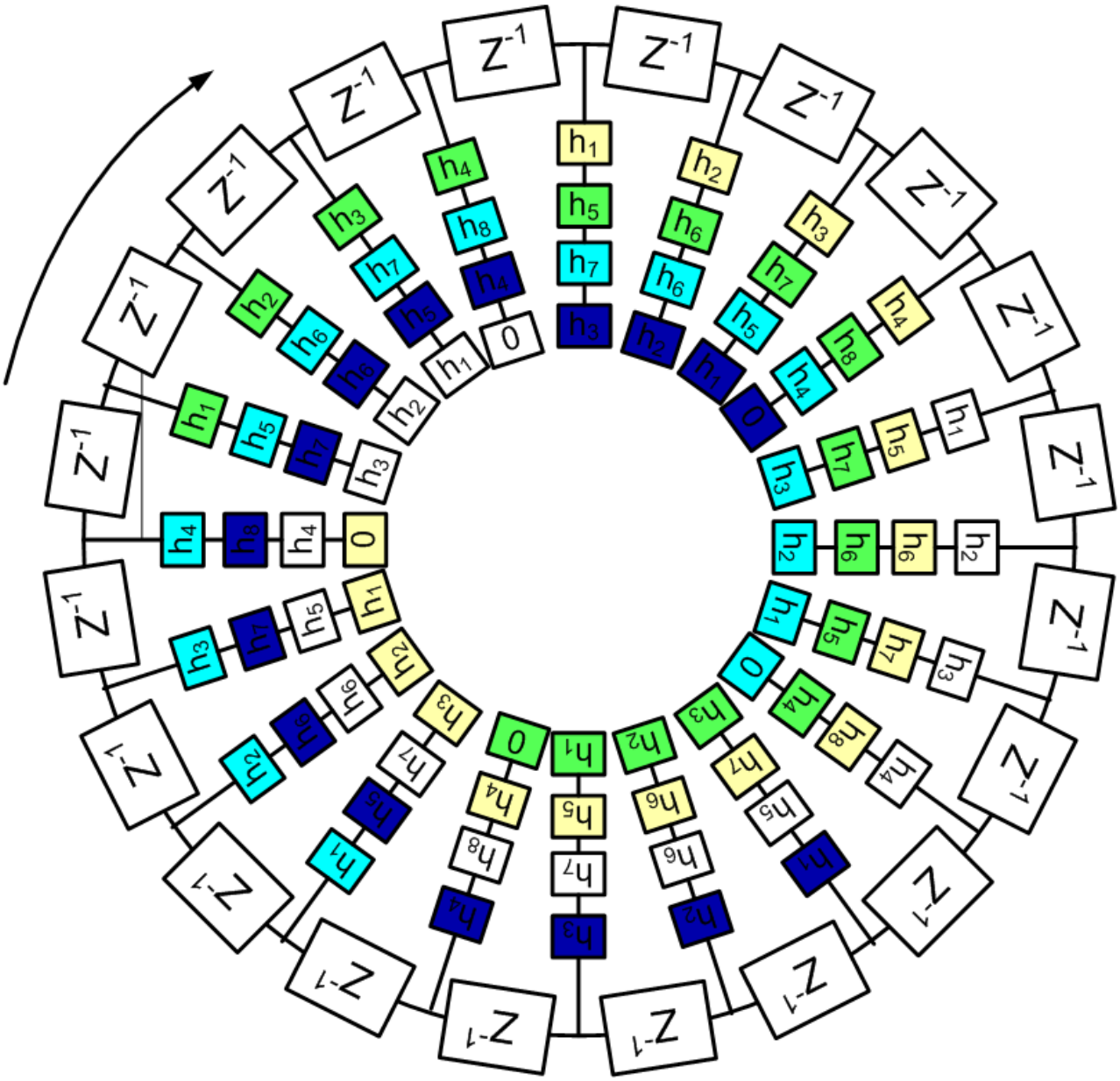


Figure 5-6 FIR circuit architecture

In the design circuit, there is no real analog delay cell. Instead, 20-phase multi-phase clocks are generated from a higher rate clock and used as the sampler clock as shown as in Figure 5-7. Each group of 4 samplers will sample the input voltage signal controlled by the corresponding poly-phase clock pulse. For controlling the sampler output, 5-phase multi-phase

clocks are generated from the same higher rate clock. However, the output clock is 4 times slower than the input clock. Therefore, this FIR filter is inherent with a downsample ratio of 4. 5 different output clock phases are labeled in different colors correspondingly in both Figure 5-6 and Figure 5-7.

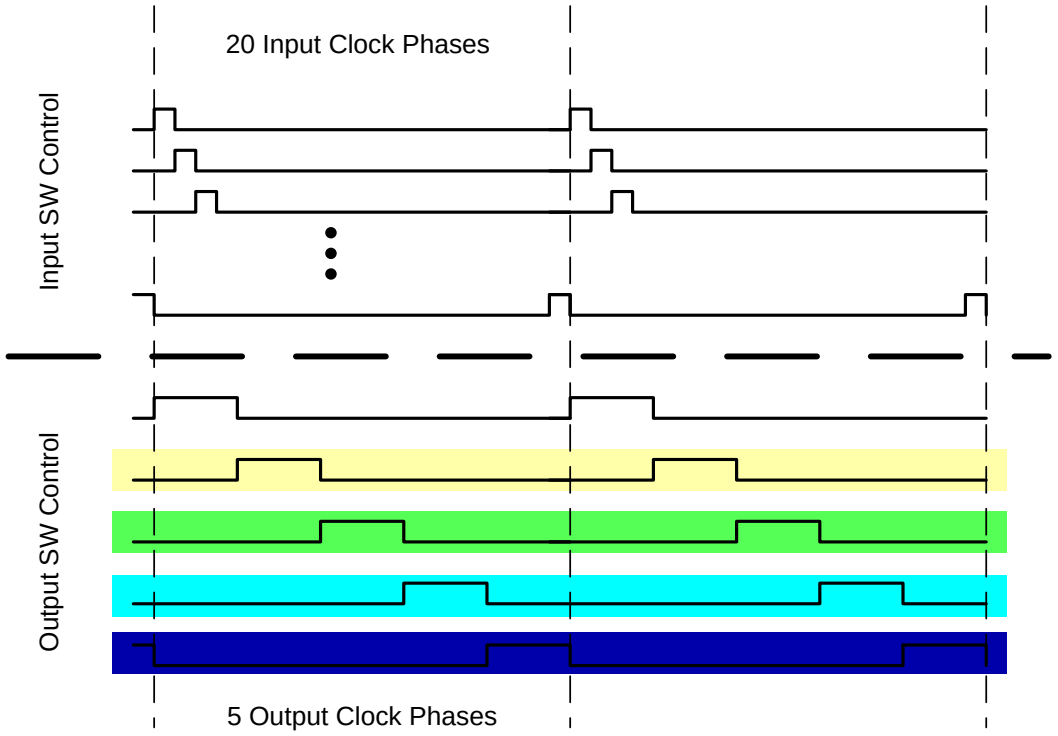
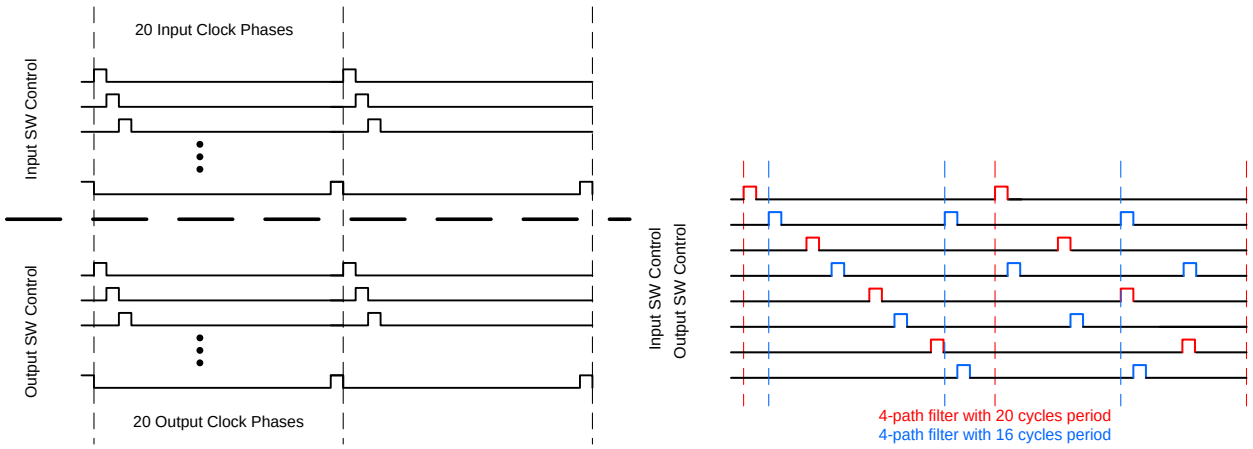


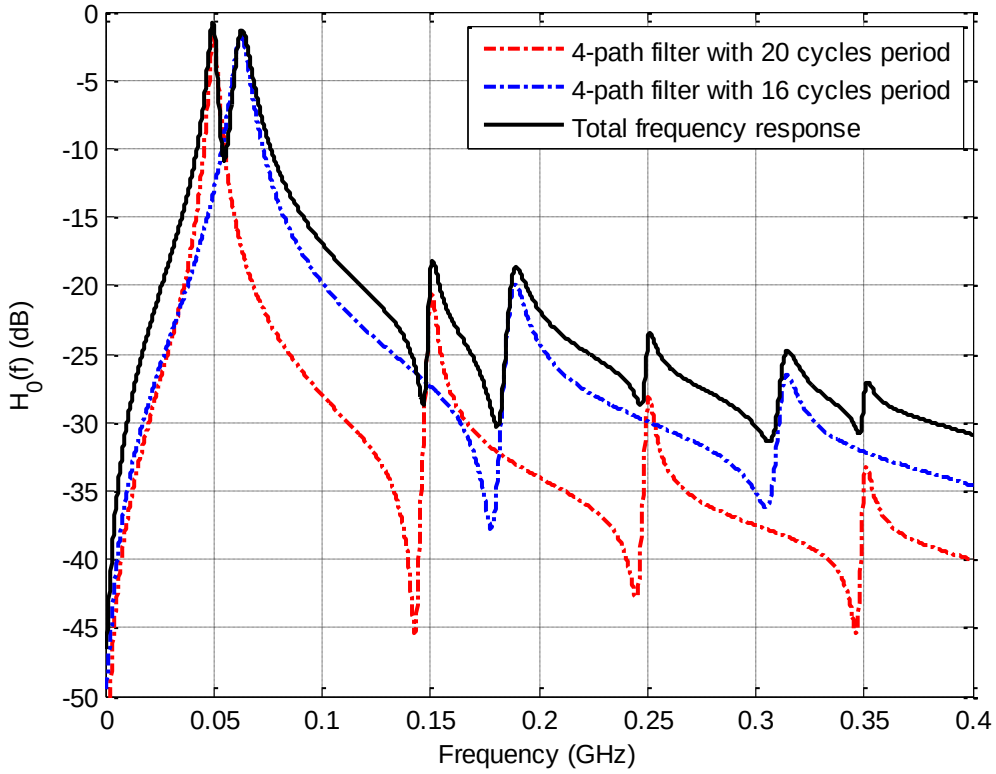
Figure 5-7 Multi-phase clocks Timing diagram for sampler input controls and output controls

As illustrated, the input voltage signal will be sampled in 20 different clock phases. Within each of 5 different output clock phases, 15 samplers will output together with different control coefficients. Therefore, the output voltage will be the weighted sum of the sampled input signal in 15 different input clock phases and thus the 14^{th} order analog FIR filter is realized by this design.

With different input/output clock phase sequences and a different number of taps for the filter coefficients, this filter can be easily reconfigured to different filter architectures. One such simplified case is to has the output clock phases be the same as the input clock phases as shown in Figure 5-8 (a) and have all the filter coefficients to be set as 15, then the filter is reconfigured to be a N-path filter with N=20. Alternatively, using less clock phases and combining multiple switched capacitor samplers together for each of the clock phases, this filter can also be reconfigured to be a N-path filter with any number N<20. Furthermore, this filter design can be reconfigured to a multi-band bandpass filter as a combination of 2, 3 or more N-path filters. Figure 5-8 (b) shows an example for a combined two 4-path filters with different periods. Those clock phases in red color are for a 4-path filter with a period of total 20 clock pulses. Those clock phases in blue color are for a 4-path filter with a period of 16 clock pulses. The sampler capacitor coefficient for red colored 4-path filter is 7 while the sampler capacitor coefficient for the blue colored 4-path filter is 14. Consequently, the 4-path filter with red colored clock phases has lower passband frequency and narrower bandwidth compared to the 4-path filter with blue colored clock phases. Figure 5-8 (c) shows the frequency responses for each of 2 4-path filters and also the total frequency response respectively. This feature is a major improvement from the original N-path filter, which can only have one narrow bandwidth band pass frequency response, and significantly increasing the reconfigurability and flexibility necessary for a multi-band SDR system.



(a) (b)



(c)

Figure 5-8 Alternative multi-phase clocks Timing diagram for sampler input controls and output controls for different N-path filters

This filter can also be reconfigured to be different FIR filters. For example, Figure 5-8 shows 4 alternative input/output multi-phase clocks. With corresponding coefficient setup, this reconfigurable filter can be reconfigured to be an 8-tap FIR filter with decimation ratio as 2, a 20-tap FIR filter with decimation ratio as 4, a 12-tap FIR filter with decimation ratio as 6 and a 24-tap FIR filter with decimation ratio as 3 respectively.

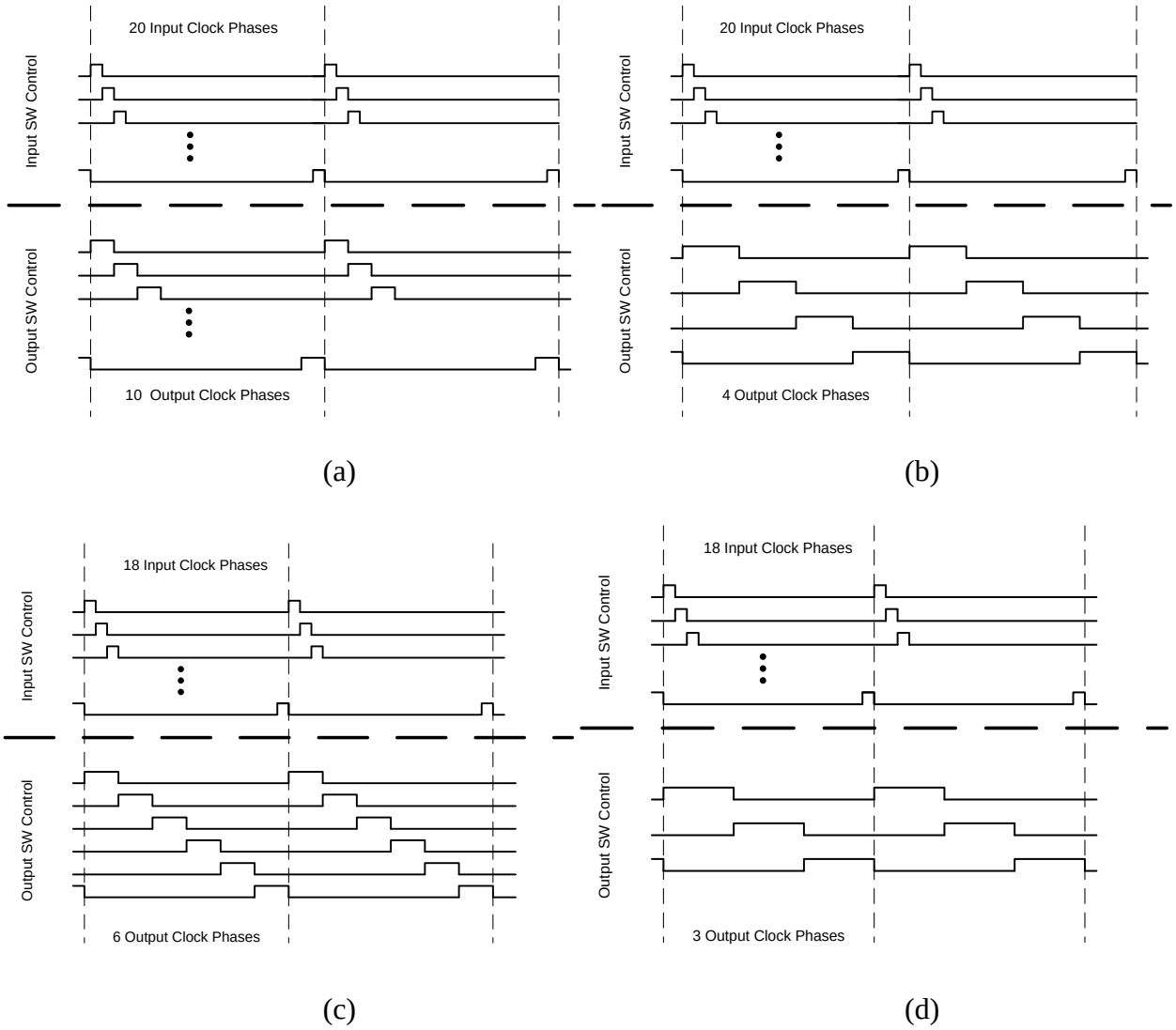


Figure 5-9 Alternative multi-phase clocks Timing diagram for sampler input controls and output controls for different FIR filters

Figure 5-10 shows the layout of this design. The active core takes 1.8x2.6mm^2 die area on a 0.18µm SiGe BiCMOS technology. Quadrature layout is used to improve the matching. As a prototype design, there is no build-in microcontroller or memory yet. For 8 independent 5-bit coefficients, there are a total 40 control bits, all from the external input pins on the top, left and the bottom edges of the design. The total 80 5-bit capacitor sampler takes most of the design area. One group of 15 samplers is labelled in the filter coefficient order. On the right edge are the signal input, output and power supplies.

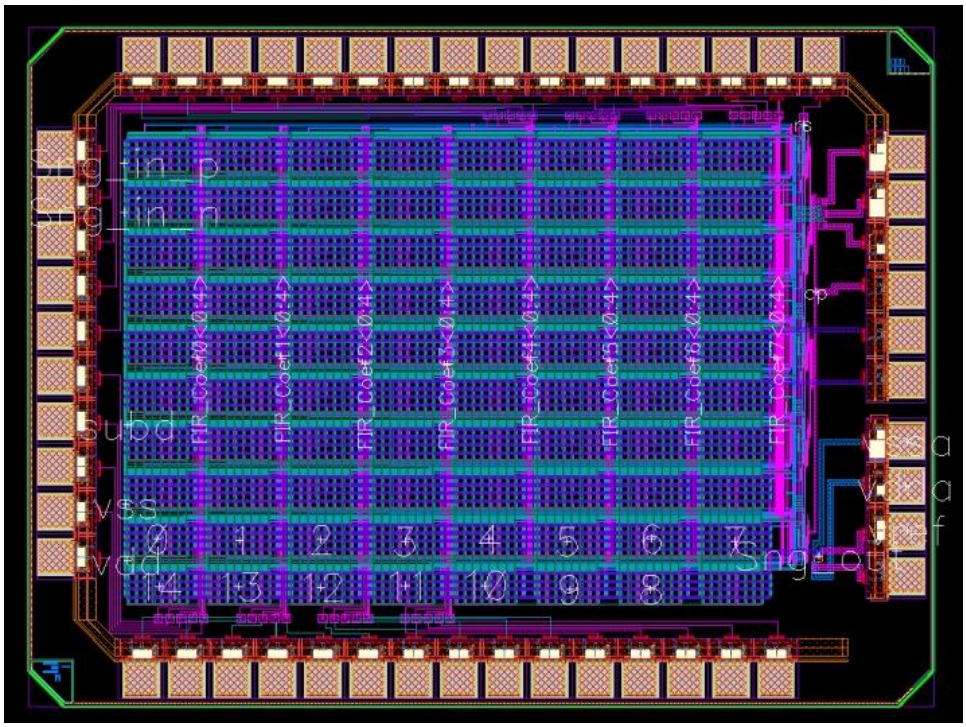


Figure 5-10 Fully Reconfigurable switch capacitor filter design layout

This filter is designed to take differential input with up to 400mV$_{P-P}$ amplitude and output filtered signal with up to 300mV$_{P-P}$ amplitude. The sampling rate of this filter is up to 1 Gsps. If configured with decimation ratio of 4, the output signal has sampling rate up to 250MHz which is a comfortable sampling rate for an ADC to convert the filtered signal to digital domain.

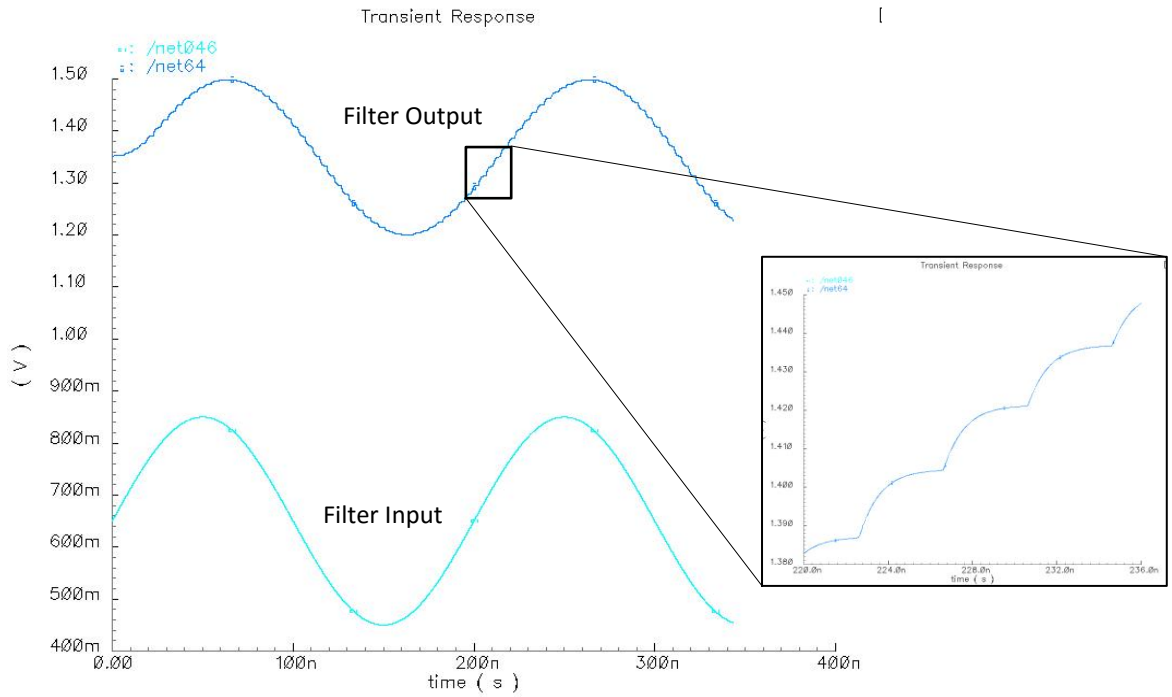


Figure 5-11 Post-layout transient simulation

Figure 5-11 shows the transient simulation results for the design. The sampling clock is set for 1Gsps. The input signal is a 5MHz single tone with 400mV_{P-P} full swing. The filter coefficient is set to be a LPF with pass bandwidth as 50MHz. Therefore, the 5MHz single tone is well within the passband and goes through the filter without addition loss. The zoomed in part shows the smooth and uniform steps on the output signal curve from each of the output clock phases.

5.2.3 Conclusion

This section proposed a novel design for a fully reconfigurable switch capacitor FIR filter to be used as a key building block for the multi-mode multi-channel SDR receiver. By changing 8 independent 5-bit filter coefficients, any 14^{th} order linear phase FIR design can be realized with this design. It can also be fully reconfigured to be various combined multiple N-path filters or

different FIR filters with different number of taps and decimation ratio. The microcontroller can be added in the future to change the filter response on fly to provide the frequency selectivity for different input signal modes and frequency bands.

Chapter 6 Digital Front-end Design for SDR

6.1 Challenges on Reconfigurability and Flexibility for SDR

A decade ago, a practical SDR system still needed to have a quite complicated filter chain designed in the analog circuitry to provide a sufficient band selectivity for the baseband signal after the mixer [60]. With recent technology developments, both ADC and DAC designs can have much better bandwidth and dynamic range than a decade ago. Therefore, as proposed in Chapter 2, a practical SDR system in modern times has chosen a low intermediate frequency architecture. The functions of those analog filters proposed in [60] are now mostly moved to the digital domain and implemented in the digital front-end block.

Traditionally, a digital front-end design dedicates to single channel, fixed bandwidth, and fixed input/output sample rates for a single communications standard. Therefore, the conventional digital front-end design is optimized with fixed digital filters, fixed ratio upsampler and downsampler along with other design blocks with little flexibility. However, current mobile systems need to support multiple standards, i.e. GSM, cdma1x, CDMA2000, UMTS, 4G-LTE, WiFi, Bluetooth and GPS. Similarly, as for a RF front-end design, there is a strong n for an SDR digital front-end design, which can be reconfigured to support multiple standards and multi-mode multi-channel communications.

Compared to conventional signal communication systems with dedicated digital front-end designs, an SDR digital front-end design takes flexible and reconfigurable. Therefore, one SDR digital front-end design can fulfill the functions of multiple conventional digital front-ends

in supporting different standards for multiple channels simultaneously. Thus, the die area, the bill of material (BOM) cost and the power consumption are significantly optimized by having one SDR digital front-end design to replace multiple conventional single functional digital front-ends. However, there are also many new design challenges for a SDR digital front-end design. Unlike for the traditional dedicated system, in which all design blocks are optimized to complete one fixed function, most of the building blocks for an SDR digital front-end design need to be redesigned or optimized differently to have wide flexibility and reconfigurability. For each functional block, for both area efficiency and power efficiency, the comparison needs to be addressed between a new multi-mode configurable design and multiple parallel traditional single mode designs that can be switched on/off.

In this chapter, an SDR multi-mode multi-channel MIMO digital front-end design will be presented. It has far more functionality than existing multi-mode digital front-end designs [61][62][63][64][65][66]. One of the key functional blocks, a novel resampler design with flexible fractional resampling ratio, will be discussed thereafter.

6.2 SDR Multi-Mode Multi-Channel MIMO Digital Front-End Design

6.2.1 Introduction

In this section, a software defined multi-mode multi-channel MIMO digital front-end design is presented. This design is implemented for a 4G mobile femtocell base station transceiver system. A femtocell base station is a small scale, low power cellular base station normally deployed for home or small business use. Although it only needs to support a limited number of connections, which is reduced from what a normal cellular base station does, for each connection, it is still required to support all existing cellular standards. Since the whole system is

targeted for a very compact, low cost and low power femtocell base station system, it cannot afford a dedicated signal path for each different standard as in the normal cellular base station system. Therefore, the SDR design is ideal for this application to provide a much smaller but highly flexible design.

This designed MIMO system has 2 input antennas and 2 output antennas. Each antenna can transmit or receive up to 7 signal channels with different modes and different frequency bandwidths. The combined frequency bandwidth is up to 20MHz. Different cellular standards can co-exist. Supported standards are CDMA2K, UMTS, LTE-1.4MHz, LTE-3MHz, LTR-5MHz, LTE-10MHz, LTE-15MHz and LTE-20MHz. Figure 6-1 shows different scenarios for the total 20MHz bandwidth split to up to 7 co-exist signal channels. Compared to existing multi-mode digital front-end designs [61][62][63][64][65][66], this required function set is more capable and more ambitious by far.

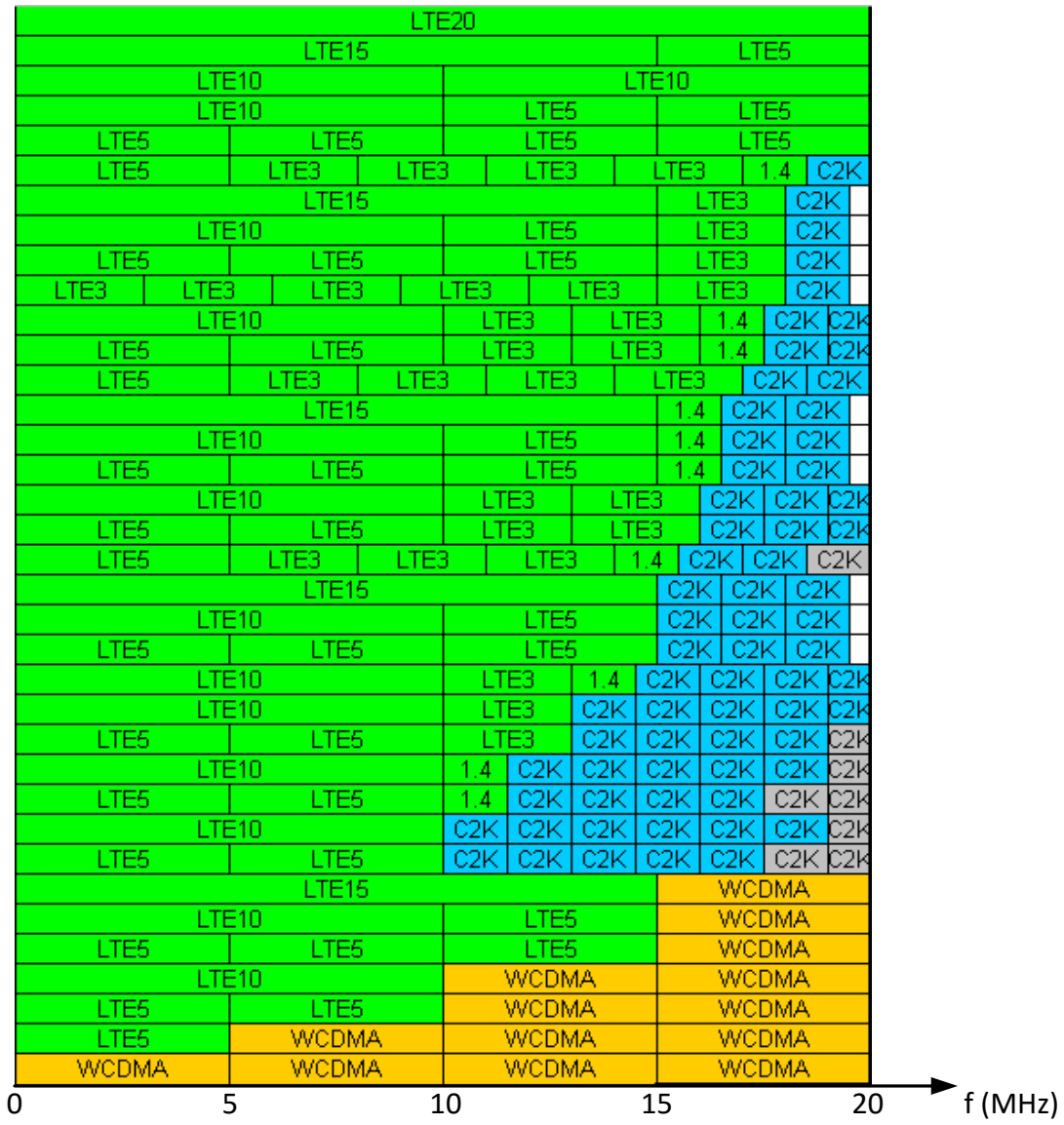


Figure 6-1 Multi-channel multi-mode scenarios for 20MHz total bandwidth

As shown as in Table 6-1, each mode has a different signal bandwidth, a different sample rate, an in-band ripple spec, and an out-band rejection spec. A highly flexible design is required to be configured to meet all different specs and switch from one mode to another quickly and on fly.

Table 6-1 Multi-standard design objectives

Modes	Channel Filter f_p (MHz)	Channel Filter f_s (MHz)	Tx Rejection (dB)	Tx In-band Ripple (dB)	Tx Input Rate (Msps)	Rx Rejection (dB)	Rx In-band Ripple (dB)	Rx Output Rate (Msps)
CDMA2k	0.59	0.74	90	0.2	1.2288	90	1	2.4576
UMTS	1.92	2.5	90	0.2	3.84	70	1	7.68
LTE-1.4	0.54	0.7	90	0.2	1.92	80	1	1.92
LTE-3	1.35	1.5	90	0.2	3.84	80	1	3.84
LTE-5	2.25	2.5	90	0.2	7.68	80	1	7.68
LTE-10	4.5	5	90	0.2	15.36	80	1	15.36
LTE-15	6.75	7.5	90	0.2	23.04	80	1	23.04
LTE-20	9	10	90	0.2	30.72	80	1	30.72

6.2.2 System Architecture

Figure 6-2 shows the functional diagram for the digital front-end transmitter chains. There are 2 identical paths, one for each output antenna. For each path the following process steps are performed. First, the serialized source signal stream from baseband module is de-serialized and split into up to 7 source signals with I and Q channel pair. The 7 identical Tx signal processing blocks take the 7 source signals separately. In each Tx signal processing block, the source signal will pass through several processes including gain adjustment, rounding, crest factor reduction and delay adjustment. Then, it will be up-sampled to the same sample rate. The signal will then be digitally mixed with NCO to different sub carrier frequencies. At this point, the signals from up to 7 sources would have the same sample rate, comparable power and different carrier frequencies. The outputs from 7 signal process blocks are summed together to become a single signal stream with up to 20MHz of signal bandwidth. The merged signal will then go through similar data processes again as in the separated blocks, i.e. rounding, clipping and up-sampling. Before getting to DAC, the digital signal stream goes through a digital pre-

distortion (DPD) block to be distorted to compensate for the nonlinearity of the RF power-amplifier, which is placed later in the Tx RF front-end chain. Another RF calibration and correction cell processes the digital signal to compensate for DC offsets, and amplitude and phase imperfections from the analog mixer as discussed in Chapter 3. Multiple digital filters needed after each up-sampler and digital mixer are not shown in the diagram. There are also 2 signal sensing paths to receive and feedback the transmitted signal back from the Tx RF front-end to provide the information for DPD and RF calibration and correction.

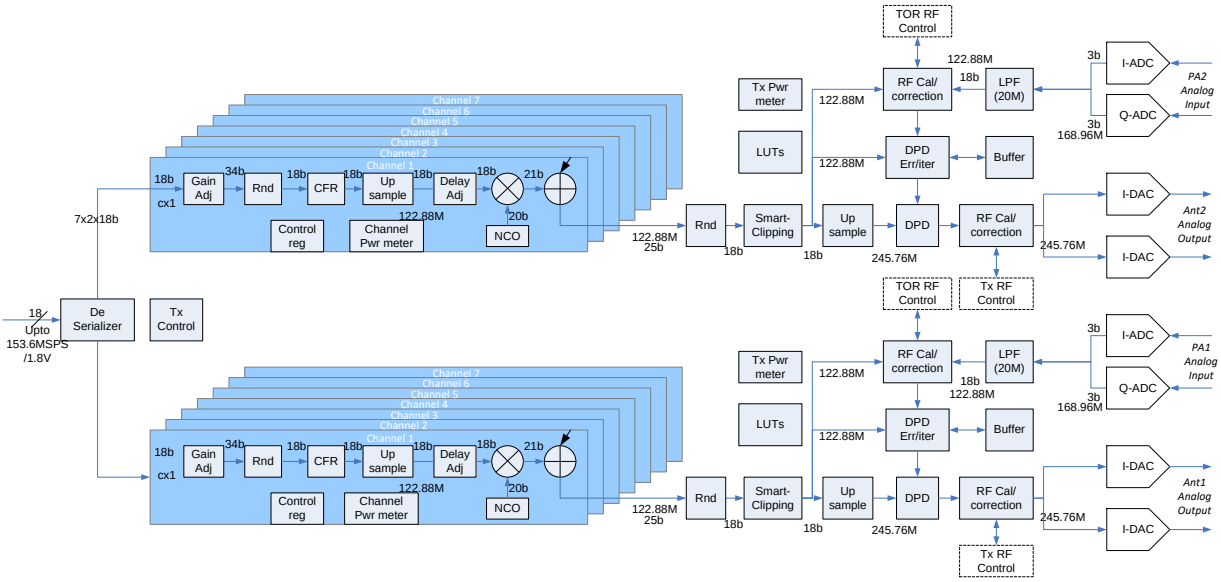


Figure 6-2 SDR digital front-end transmitter functional diagram

Figure 6-3 shows the functional diagram for the digital front-end receiver chains. As same as for transmitter chains, there are 2 identical paths from 2 receiver antennas respectively. For each path the high rate digital signal output from ADC will first pass through 2 high-Q digital low pass filters with 20MHz passband. After that, a RF calibration and correction cell processes the filtered digital signal to compensate for amplitude and phase imperfection from the analog mixer in the RF front-end receiver path. 7 identical Rx signal processing blocks then

separately take the signal, mixing with NCO to down convert each signal channel to the baseband. Each signal channel goes through delay adjustment, another high-Q digital low pass filter and a gain adjustment before being serialized and merged to be sent to baseband module.

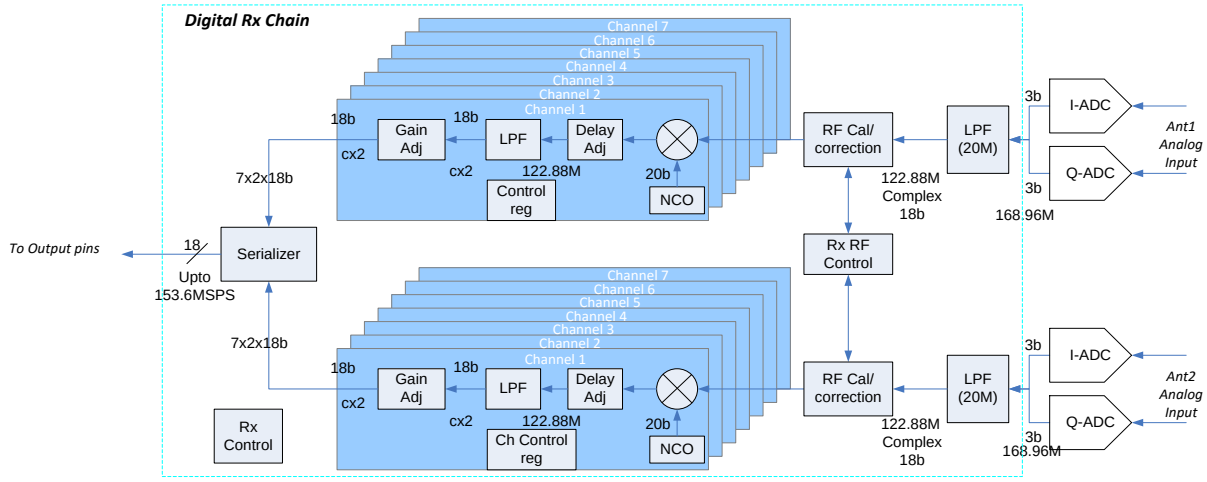
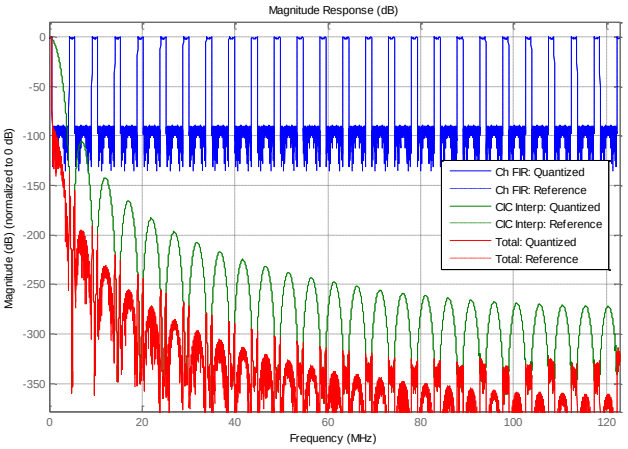


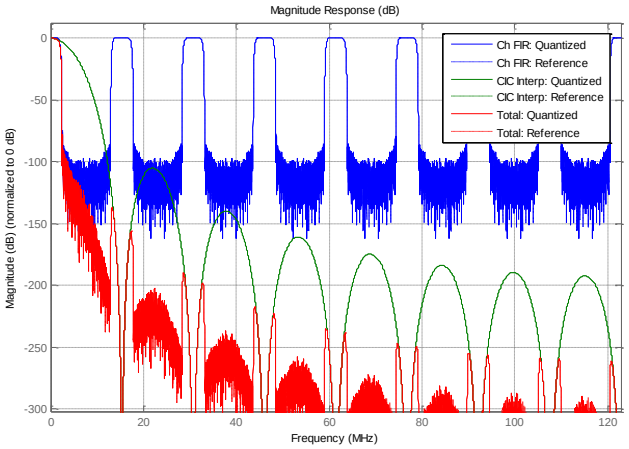
Figure 6-3 SDR digital front-end Receiver functional diagram

6.2.1 Design Challenges for Filter and Resampler

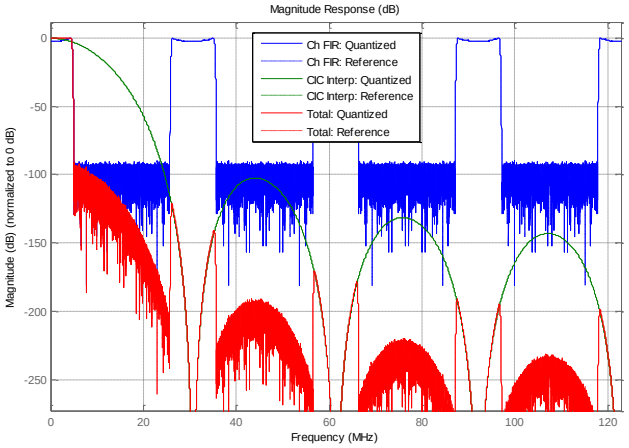
For both Tx and Rx designs, one challenge is to provide different filtering for different modes and also to satisfy the different design objectives for in band flatness and out band rejection. Multiple Cascaded integrator–comb (CIC) filters and one big 16-bit 80-tap FIR filter are implemented in the Tx chain to realize the filtering functions. The order for the CIC filters are configured differently and the FIR filter coefficients are from the memory and different for each mode respectively. Figure 6-4 shows the Tx filtered spectrum for different standards.



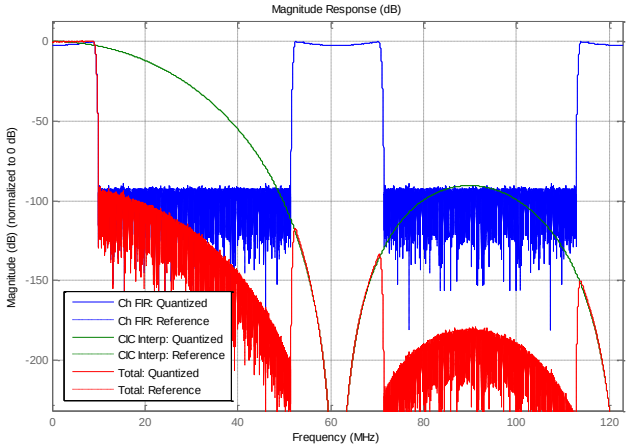
(a) CDMA2000



(b) WCDMA



(c) LTE-10MHz



(d) LTE-20MHz

Figure 6-4 Tx filtered spectrum for different standards

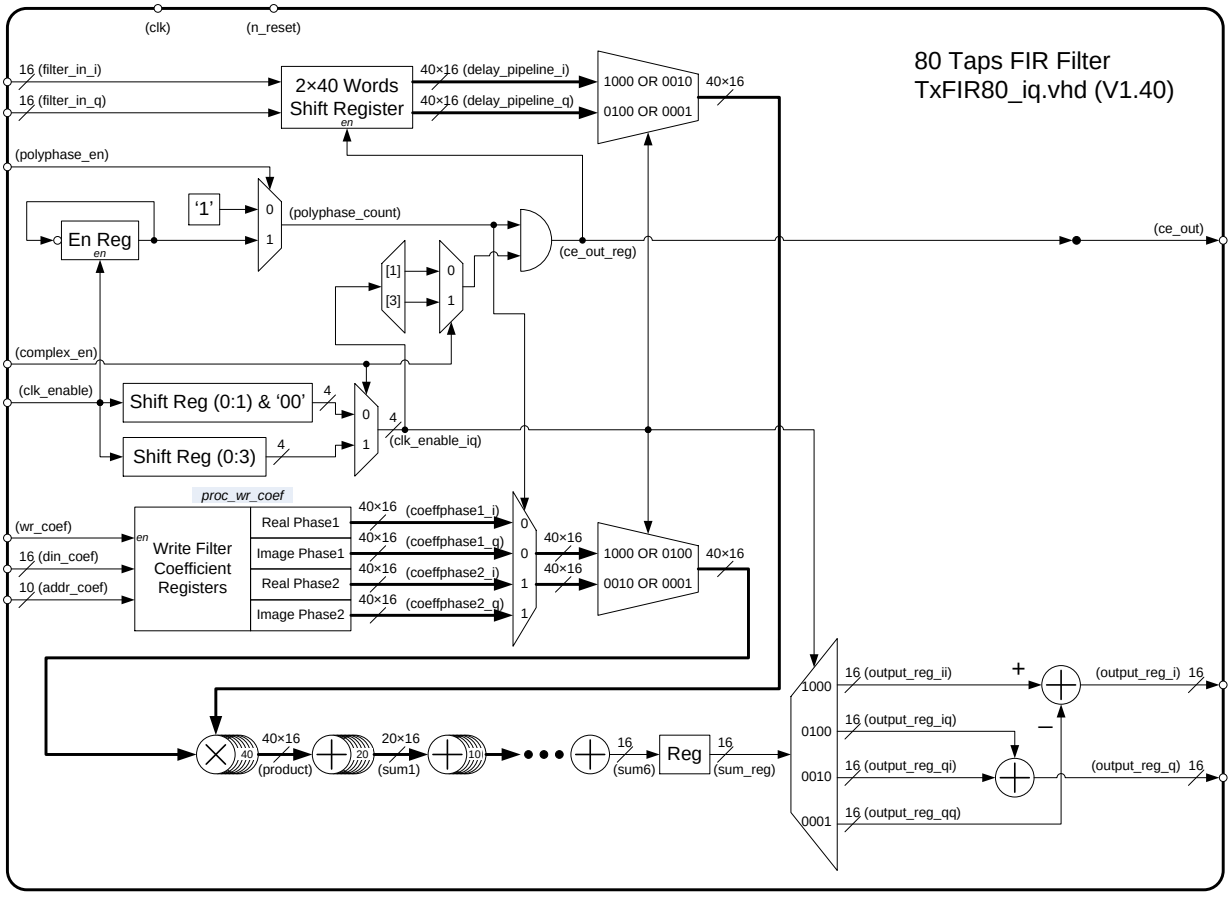


Figure 6-5 80-tap polyphase FIR filter functional diagram

For the FIR filter design, the 16-bit input depth multiplier cell takes a big area along with the adders and other associated logics. Besides all other functional blocks, the FIR filter is dictating the total design area. The area for the FIR filter would be multiplied by 14 if two such filters are implemented for each of 7 channels for both I and Q signals. To optimize the die area, a polyphase FIR filter is used as shown in Figure 6-5. Each I or Q signal takes 2 phases. The number of multipliers is reduced by half to be 40. Both I and Q signals are filtered together within this single FIR filter block. Moreover, the highest clock rate for the FIR is 245.76MHz, which is the same as the DAC clock rate. Therefore, this FIR filter can be time interleaved for all 7 channels. Through all of the above, instead of having 14 separated FIR filters with 80

multipliers in each, one polyphase time interleaved FIR filter with only 40 multipliers is in place to provide the same filtering for all 7 channels. The total die area and the design cost are greatly reduced. Similarly, one 4-phase polyphase time interleaved FIR filter with 55 multipliers is implemented in the Rx chain to provide 110-tap FIR filter functions for all 7 Rx channels with both I and Q signals.

Comparing the ADC and DAC design, the DAC design is a relatively easier one to achieve higher sampling rate and/or effective number of bit (ENOB). On the Tx side, the least common multiple of the baseband source signal sample rates from all possible modes is chosen, 245.76MHz. So the up-sample ratios for different modes are all integers which are realized by the combination of the inherent up-sampling ratios in both the polyphase FIR filter and the CIC up-convert filter. On the Rx side, the ADC cannot run as fast as the DAC with required the ENOB. With a slower sample rate from the ADC and a more inherent down-sampling ratio from the CIC filter on the Rx chain, an arbitrary fractional ratio resampler is required for the design. The next section will give a detailed design for a novel resampler with arbitrary fractional resampling ratios.

Along with resolved design challenges for the FIR filter and the resampler blocks, many other design improvements have been achieved in the other design blocks, such as smart adaptive clipping, low-spur low-noise NCO, 2-step fast response power estimation and digital AGC. The design details for those blocks are omitted here.

This SDR digital front-end design is taped out in a 45nm CMOS technology as a part of a major function block in a SoC cellular femtocell modem chip. Figure 6-6 shows the place and route map of the SDR digital front-end with functional blocks color coded. The total area is

1350µm×3300µm = 4.46mm^2. The total flop count is 156K. The silicon area is mostly taken by the FIR filters and the resamplers in both Tx and Rx chains. All Tx chains is in blue color while the Rx chains is in green color. The total area for all Rx chains is about as twice big as the area for all Tx chains because each Rx chain has a resampler block which is not needed in any of the Tx chains, and also because the FIR filter in the Rx chains has longer taps compared with the FIR filter in the Tx chains. Other blocks labeled in red, grey and cyan take less than 5% of total area. This design has multiple clocks from data converter interface and baseband interface. The Tx part closed timing at 250MHz and the Rx part is closed timing at 200MHz.

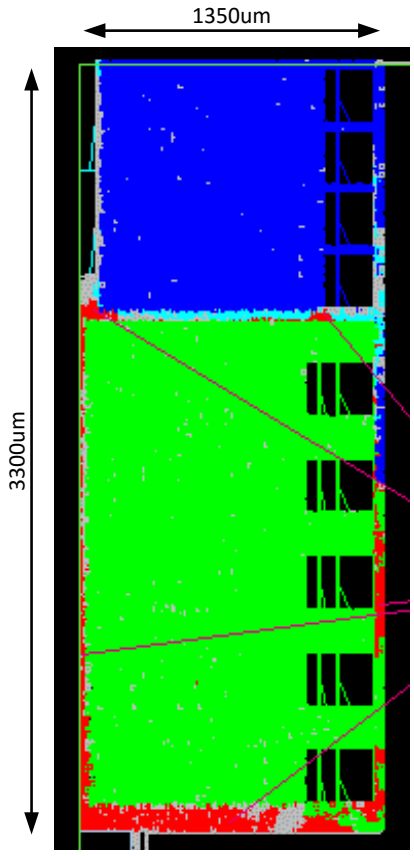


Figure 6-6 SDR digital front-end place and route map

6.2.2 Conclusion

This SDR multi-mode multi-channel digital front-end design has been taped out in a 45nm CMOS process as a major functional block for a system-on-chip (SOC) femtocell base station modem chip. This SDR digital front-end design provides much more functionality and flexibility than previous designs, supporting 2 Tx antennas and 2 Rx antennas MIMO, up to 7 channels for each antenna, multiple users, and flexible combinations of multiple cellular standards from 2G, 3G to 4G. The whole chip becomes a successful product in the emerging market for femtocells because of its compact size, low-power consumption and support for most existing cellular standards with great flexibility and capability.

6.3 An Innovative Resampler Design with Arbitrary Fractional Resampling Ratios

6.3.1 Introduction

As addressed in previous section, the resampler block is a necessary functional block for the Rx chain of an SDR digital front-end and presents multiple design challenges. For each different signal channel and each mode, the total downsample ratio for the Rx chain is defined by the ratio of the input data rate to the output data rate.

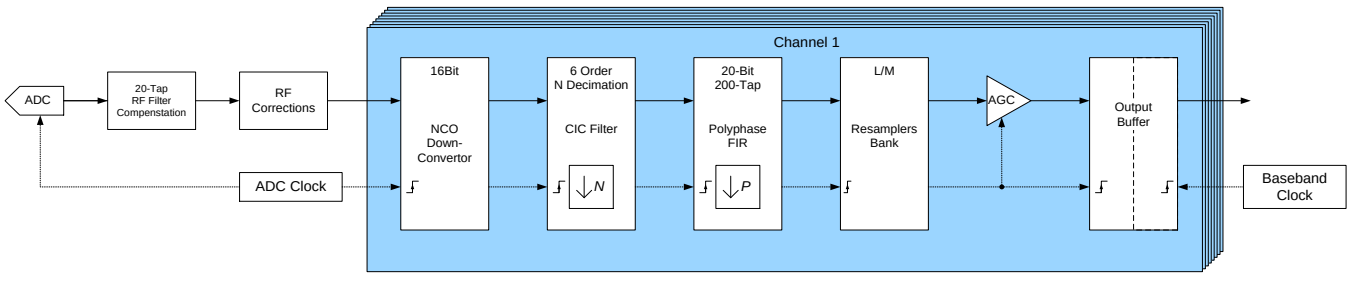


Figure 6-7 Rx Chain functional diagram

Figure 6-7 shows a simplified functional diagram for the Rx chains. The input data rate for the Rx chain is decided by the data converter rate. For an ADC design to cover wideband, high dynamic range required for multi-mode multi-channel communications, the conversion rate cannot be pushed very high. The Rx chain output sample rate is defined and fixed to different rates for different modes as from 2.4576MHz for CDMA2000 to 30.72MHz for LTE-20MHz. Moreover, to achieve good filter functionality while considering area and power efficiencies, a CIC filter and a FIR filter are implemented in the Rx chain, which needs to have some inherent down-sample ratio. With all of the above constraints, the resampler in the Rx chain for this multi-mode multi-channel digital front-end needs to support different fractional down-sampling ratios such as 3/5, 4/5, 3/4 and 96/125 etc.

Another design constraint for a downsample resampler is noise and alias rejection. For a downsample resampler, a wider signal spectrum, as from the input's higher sampling rate will be folded into a narrower signal spectrum as defined by the output's lower sampling rate. Therefore, similar to the use of an ADC, to not degrade the SNR for the signal, a filter function is needed to be placed before or inside the downsample resampler.

6.3.2 Convectional Resampler Design

Figure 6-8 shows the functional diagram for a conventional resampler design. The input signal sample rate is F_1 while the output signal sample rate is F_2. For an upsample resampler, $F_1 < F_2$. For a downsample resampler, $F_1 > F_2$. Normally, we define the resampler ratio as $F_2/F_1 = L/M$, where M and L are the smallest integers to get the ratio. As for the application in the Rx chain, only the downsampler resampler will be discussed in the section.

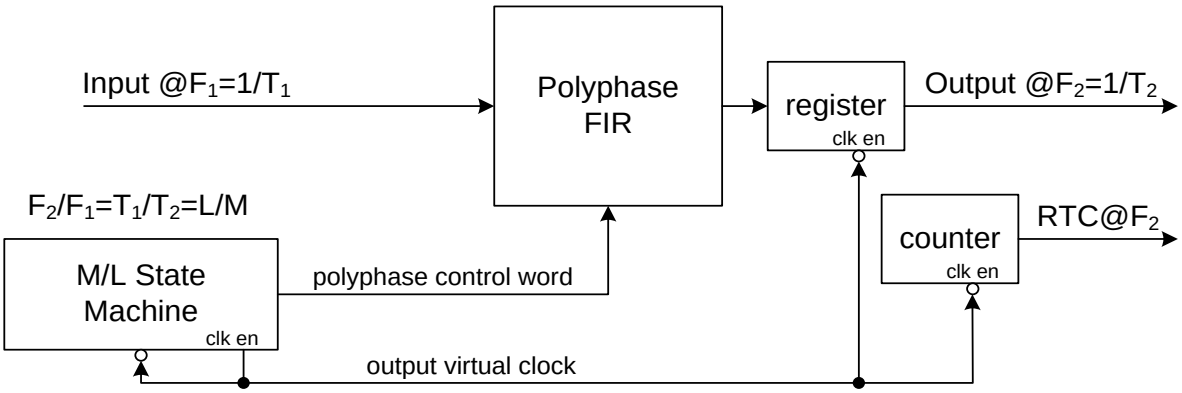


Figure 6-8 Conventional resampler functional diagram

Although a resampler is converting the input signal from one clock frequency to a different clock, in the common practice, resamplers are designed in one clock domain, normally, the higher one between F_1 and F_2. As illustrated in Figure 6-9, for a downsample resampler with ratio, L/M =2/5, a virtual clock, F_{2i} is created in F_1 clock domain. The virtual clock has the same clock frequency as F_2, however, with imbalanced duration from one clock cycle to another. Using this virtual clock makes the resampler design much simpler without any clock domain crossing (CDC) design complications. The CDC will be handled later in the Rx chain as an output buffer block as shown in Figure 6-7.

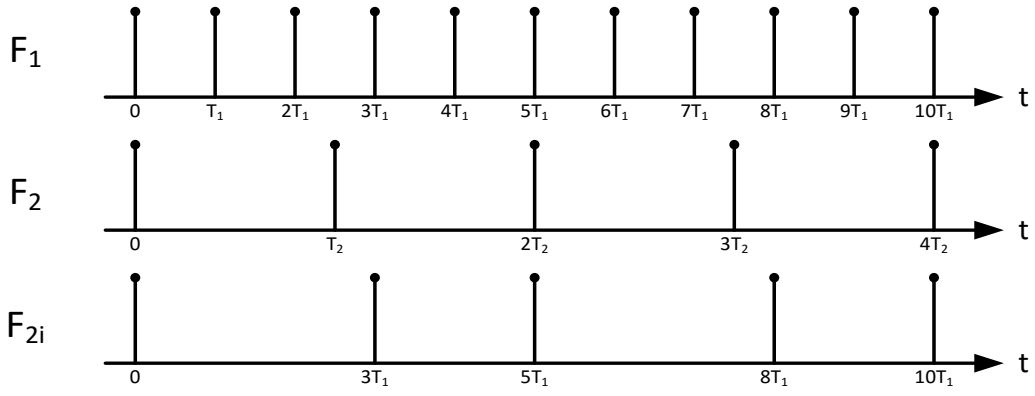


Figure 6-9 Virtual clock converter timing diagram

For alias and noise rejection purposes, a FIR filter is needed within the resampler block. Considering the same example for designing a downsample resampler with ratio, L/M = 2/5, the whole block is running on the F_1 clock. However, to get the right filter output values right at the F_2 clock timing ticks, the FIR filter needs to be designed a for high rate virtual clock of $2\times F_1$, which is the least common multiple of F_1 and F_2. As in Figure 6-10, the FIR input signal at F_1 clock will be first padded with zeroes to form a signal on F_V virtual clock. This signal then passes through the FIR filter with the F_V virtual clock. The filter output signal samples at the F_2 clock ticks will be then output and shifted to F_{2i} clock ticks as the resampler output.

Since only signal points on the F_2 clock ticks are for the output, all other signal points, as grayed out in the figure will be omitted on the output. They do not need to be calculated at all. A polyphase FIR filter working with the virtual clock control block then takes advantage of this to run the design at the F_1 clock and to calculate only those output data points on the F_2 clock. Compared with a full phase FIR filter running on F_V, the running clock is reduce by L times and the computation complexity is reduced by M times. Both power consumption and the design area/cost are therefore optimized. After the polyphase FIR filter, a register and a counter are for the resampler output in F_{2i} clock.

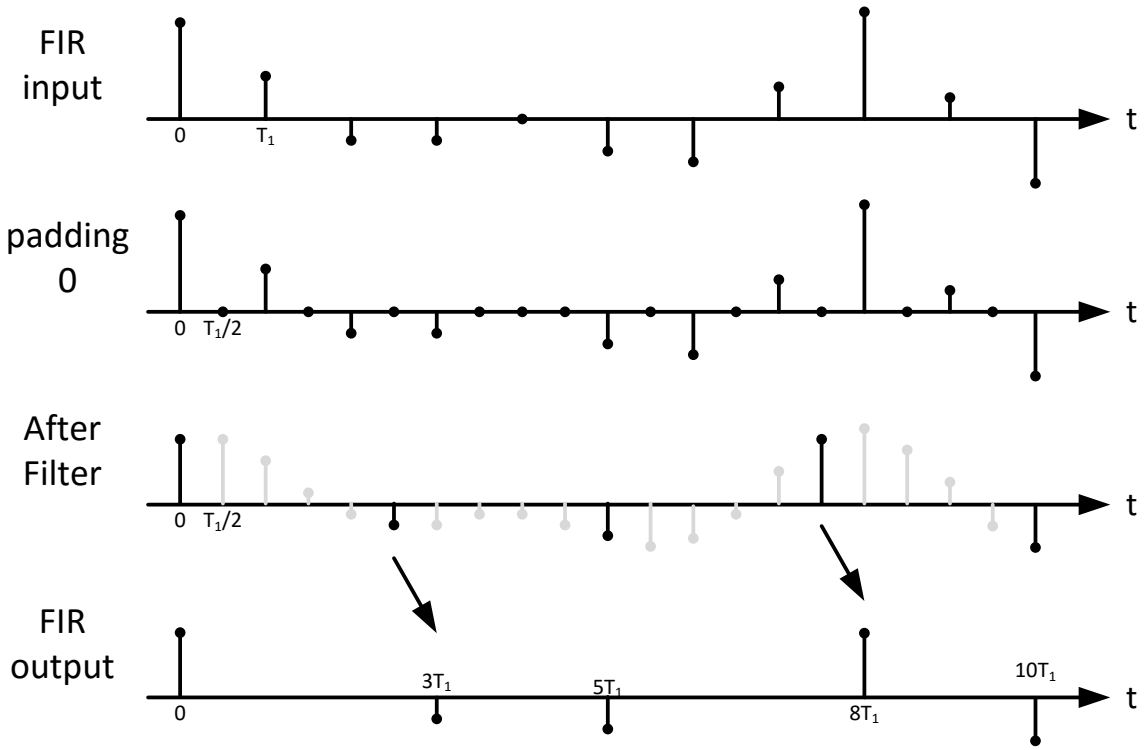


Figure 6-10 Polyphase FIR filter input and output signals

6.3.3 Challenges for SDR Resampler Design

Optimized for the die area and the cost, the polyphase FIR filter still dominates the total design area by having multiple multipliers and memory to save the filter coefficients. To get required noise and alias rejection, an N-tap FIR filter is designed in the F_1 clock domain. However, the FIR filter in the resampler is running at the virtual clock domain in $F_V=LF_1$. Therefore, to have the same filter effect, it becomes an N×L-tap FIR filter. Much more memory is needed to save the N×L filter coefficients.

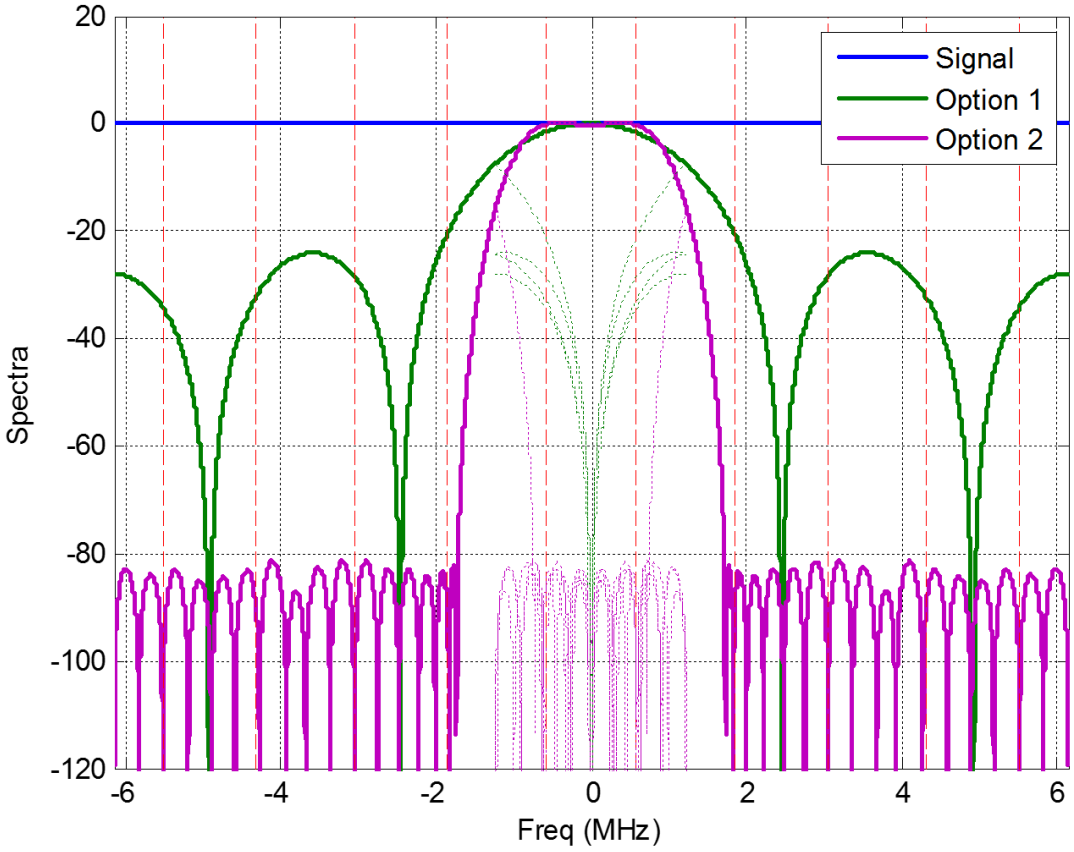


Figure 6-11 Downsample resampler noise and alias rejection by different filters

Considering the Rx chain design from the previous section, a required resampler design for CDMA2000 mode has specifications as F1 = 3.072MHz, F2 = 2.4576MHz and downsample ratio L/M = 4/5. As shown in Figure 6-11, we compared the filter effect for two different FIR options. For Option 1, a very simple 8-tap FIR filter is used which is equivalent to a 2-tap FIR filter in F_1 clock domain with the behavior of a linear interpolator. There are only 2 multipliers and memory for 10 16-bit coefficients. However, the filter performance is poor for having 1.6dB in-band ripple and 26.9dB SNR which is far short of design objectives. Option 2 has a 40-tap FIR filter, which is equivalent to a 10-tap FIR low-pass filter in F_1 clock domain. It provides

good performance of 0.4dB in-band ripple and 80dB SNR, which meets design objectives. 10 multipliers and memory for 40 16-bit coefficients are required for Option 2 resampler. For a resampler with larger ratio numbers like 96/125, it will require much more memory to achieve a 10-tap equivalent FIR low pass filter in the F_1 clock domain.

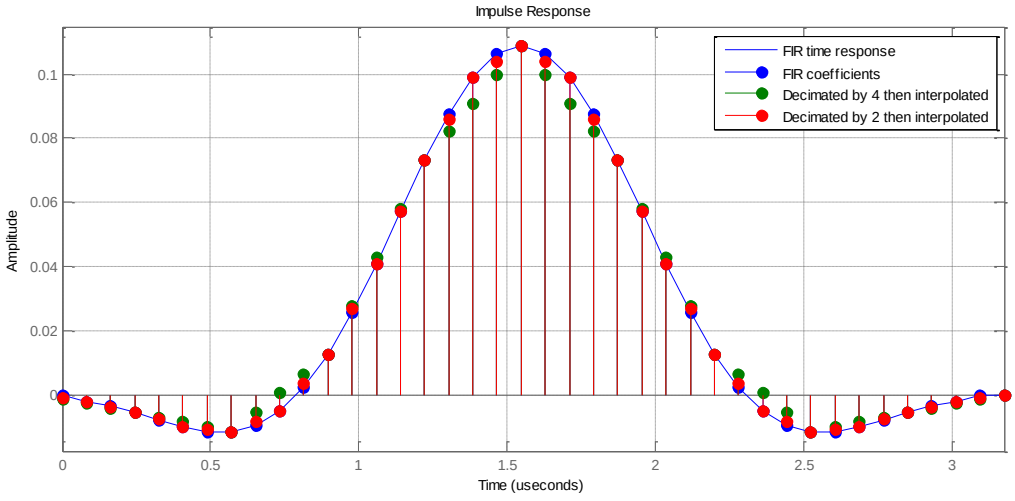
Another limitation of the conventional resampler design is that it is a big challenge for one resample design to have multiple reconfigurable downsample ratios. For the Rx chain design from the previous section, if different downsample ratios as $L_1/M_1=3/4$, $L_2/M_2=3/5$ and $L_3/M_3=4/5$ are required for different modes, one solution is to design the resampler with M=20 which is the least common multiple of all M_1, M_2 and M_3 from different ratios. The virtual clock to input clock ratio is $F_V/F_1=12$ which is the least common multiple of all M_1, M_2 and M_3 from different ratios. To achieve an equivalent to a 10-tap FIR low-pass filter in F_1 clock domain, a total of 50 multipliers and memory for 240 16-bit filter coefficients are required for this resampler design. It actually costs more area than designing 3 resamplers separately for each ratio as 3/4, 3/5 and 4/5.

6.3.4 An Innovative Resampler Design for SDR Digital Front-ends

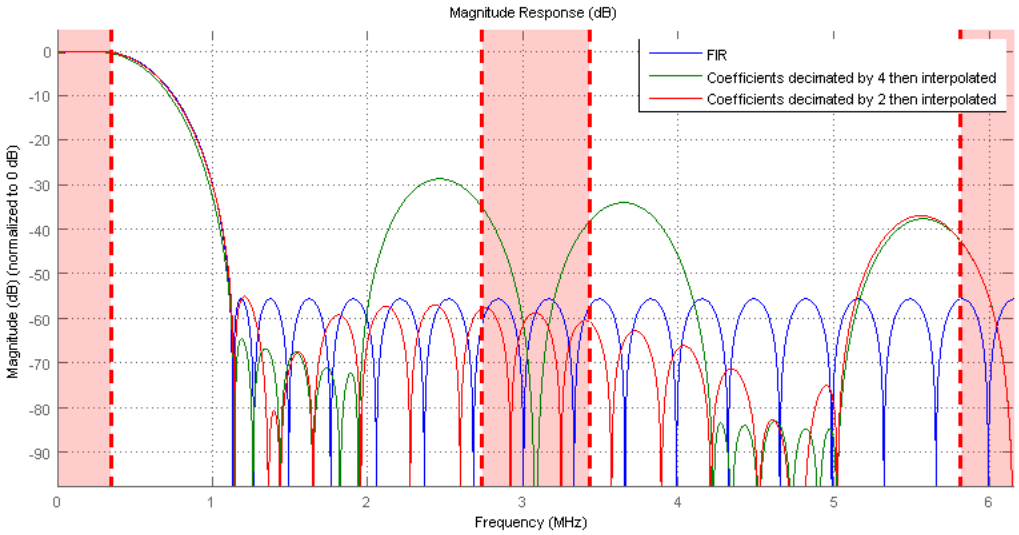
As discussed above, conventional resampler designs have shortcomings when used in an SDR digital front-end. For an N-tap FIR filter designed in F_1 clock domain, N×L filter coefficients are required for the resampler FIR filter running in F_V virtual clock domain. For a big number L such as for the ratio as L/M = 96/125, a big memory area is needed to save 96N FIR filter coefficients. To reduce the memory area, filter coefficients can be decimated. As shown in Figure 6-12, blue curves represent the impulse response and the frequency response for a designed 40-tap FIR low pass filter for resample use. Green curves are for the situation if we

only save one coefficient out of each 4 and calculate 3 not saved coefficients in the middle by linear interpolation. Red curves are for the situation if filter coefficients are decimated by two than linear interpolated by 2. Comparing the frequency response of these 3 FIR filters, the in-band responses are almost identical while the out-band rejection are similar. Since the filter block in resampler is for rejecting the alias spectrum, comparisons among 3 FIR filters are drawn only for those shaded areas in Figure 6-12(b) as for alias spectrum.

Other than reducing memory area, there is a much more important advantage by using linear interpolation to calculate filter coefficients. As shown in Figure 6-13, if interpolating 4 times more for the filter coefficients in red color from Figure 6-12, the frequency response is the same for the original bandwidth but extended to 4 times wider frequency range. The interpolation ratio can be much higher for any big number R to get the sampler frequency response with a much larger extended frequency range. So instead of a virtual clock domain of $F_V=LF_1$, the resampler filter is running at a much higher virtual clock domain as $F_V = RF_1$ where R>>L.



(a)



(b)

Figure 6-12 Decimated resampler filter coefficients and frequency responses

Choosing a big enough R, 8192 for example, for all different required resampler ratios, 3/4, 3/5, 4/5, 96/125 and any other ratio, a close enough ratio can be found with a common numerator R=8192 as 3/4~8192/10932, 3/5~8192/13655, 4/5~8192/10240 and 96/125~8192/10667. Therefore, we can design one resampler with the filter running at a very high virtual clock domain, that is easily reconfigured for any given resampler ratio.

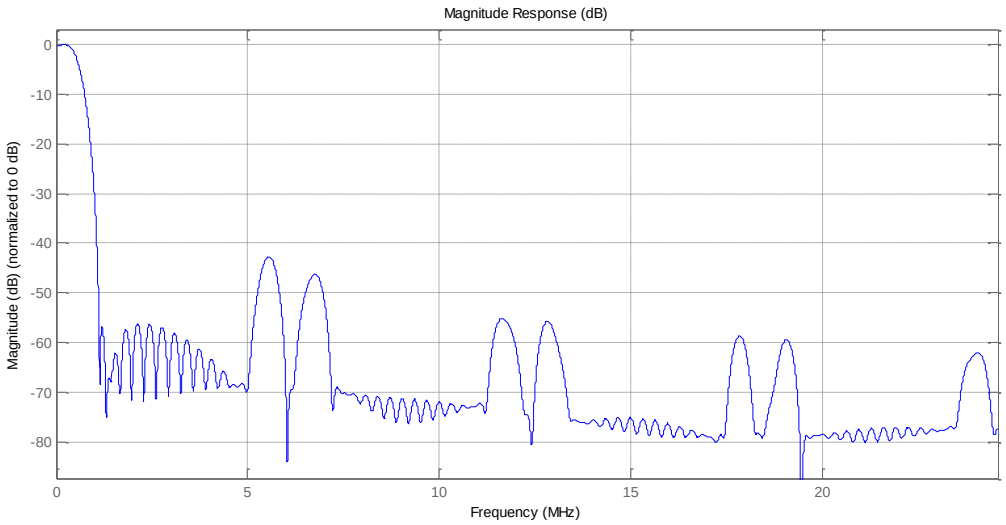


Figure 6-13 Resampler filter frequency responses with higher ratio linear interpolated coefficients

No extra die area (cost) or computation complexity (power) is needed to be paid for by having this resampler FIR filter running at a very high virtual clock domain. To design the low pass filter for the resampler, a low pass filter should be first designed with a much lower frequency domain, i.e. $4F_1$. Only minimal memory is needed to save the much fewer number of coefficients. All other coefficients in the middle are calculated from the linear interpolation. Only 2 extra multipliers are required for the interpolation for any given higher virtual clock. The 2 interpolation coefficients for the linear interpolation are directly from the binary counters in the polyphase filter control block as shown in Figure 6-8. Since only the filter output at the F_2 clock domain is calculated, and the filter input signal is a zero padded signal with nonzero values only at the F_1 clock ticks, for any given higher virtual clock domain, it is the same number of multiply computations for each output in the F_2 clock domain.

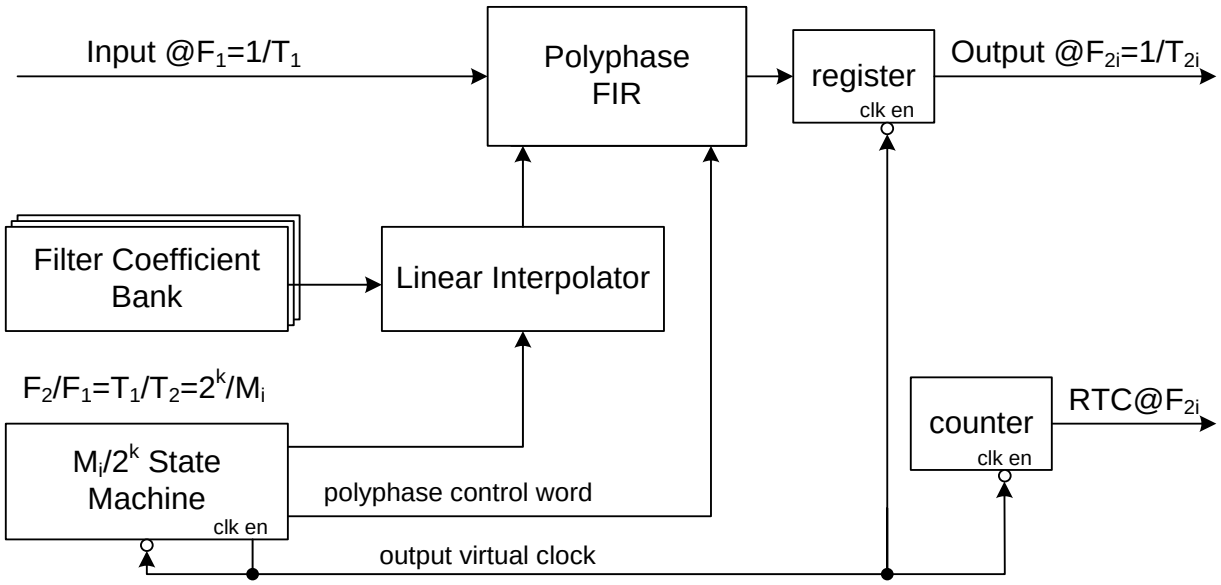
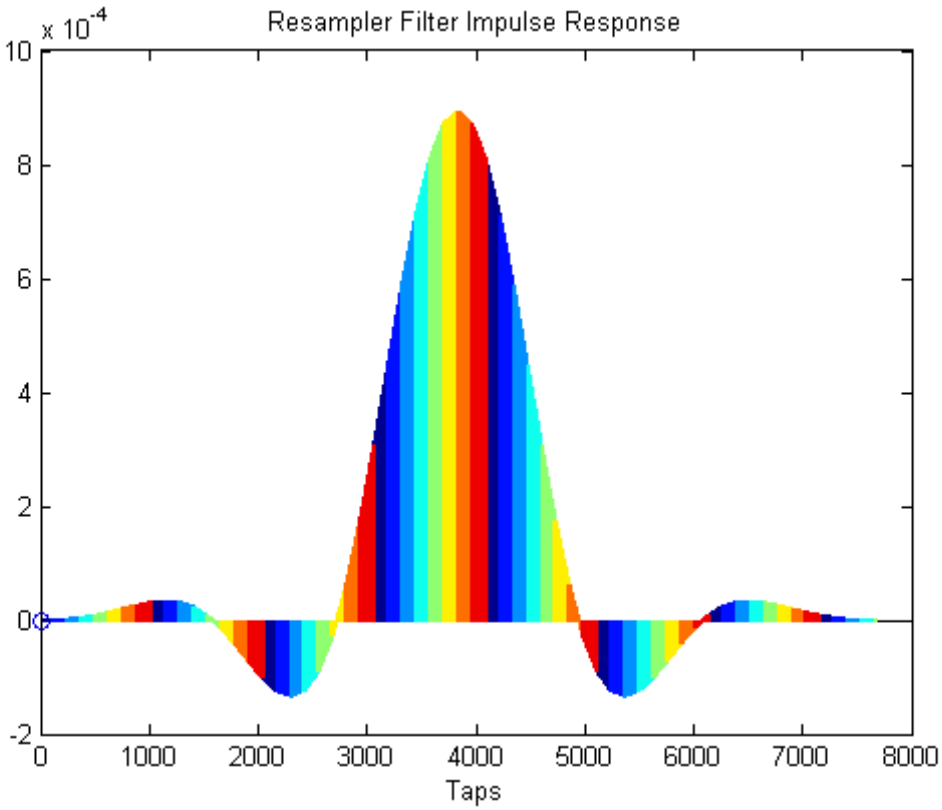
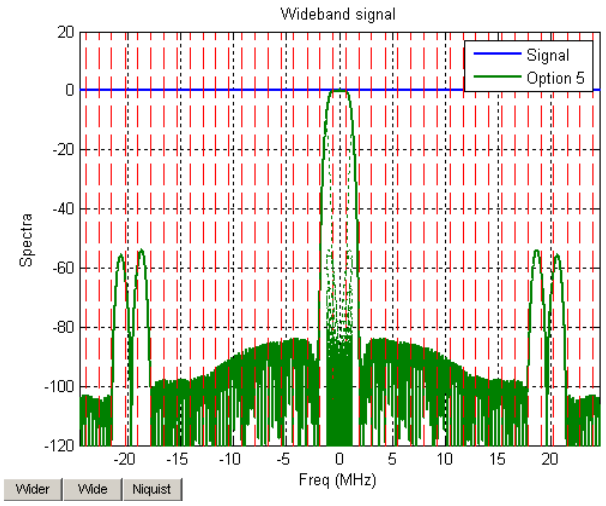


Figure 6-14 Proposed innovative SDR resampler functional diagram

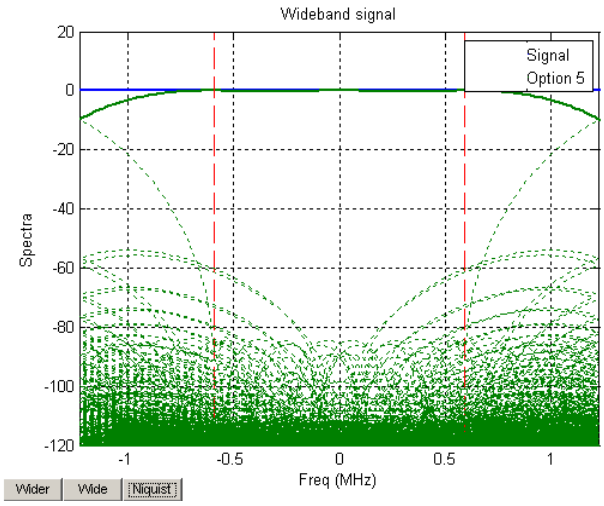
Figure 6-14 shows the functional diagram of the proposed innovative resampler for SDR system. Every block running at the F_1 clock is the same as for conventional resampler designs. The polyphase FIR filter virtually runs at much higher clock as 2^kF_1. The resampler can be reconfigured for multiple down sampler ratios, $2^k/M_i$ where i = 1, 2, 3... The filter coefficient bank saves all filter coefficients for different resampler ratios and different modes. The $M_i/2^k$ state machine not only gives the polyphase FIR filter control ticks but also gives the 2 interpolation coefficients for the linear interpolator block.



(a)



(b)



(c)

Figure 6-15 Resampler coefficients and filter spectrum with interpolation

Figure 6-15 shows one of the actual designed resampler filters for CDMA2000 mode, which is used in the SDR digital front-end design discussed in the previous section. The low pass filter is designed in $8F_1$ clock domain with 64 coefficients. Therefore, the impulse response for this filter is $8T_1$ long and the polyphase filter needs 8 multipliers. The 64 filter coefficients are then interpolated 128 times to form a total 8192-tap filter as shown as in Figure 6-15 (a). Different colors represent 8 different polyphases in $8F_1$ clock domain and show the group of 63 interpolated coefficients. Figure 6-15 (b) shows the partial, close to baseband part of the frequency response of this filter. Figure 6-15 (c) shows the folded frequency response of this filter in F2 clock domain as for the resampler output signal.

The SDR resampler has 8 multipliers for the FIR filter plus 2 multipliers for linear interpolator. Compared to a design multiple with fixed ratio resamplers for different modes, this die area (cost) and computational complexity (power) are significantly optimized for the SDR system.

6.3.5 Conclusion

For an SDR digital front-end, an innovative resampler is designed to provide reconfigurability for arbitrary resampling ratios. Design area (cost) and computational complexity (power) are also optimized compared with existing conventional resampler designs. This is one of the most important building blocks for the multi-mode multi-channel SDR digital front-end design.

Chapter 7 Conclusions

Due to a variety of developments and breakthroughs for the enabling technologies, the software-defined radio (SDR) has become a practical application for the mobile system as well as other emerging systems. Derived from the conceptual and ideal SDR architecture, this dissertation proposes a practical SDR architecture. Each of the building blocks has been discussed in the context of available technologies and potential design challenges. Altogether, a realistic SDR system is achieved with rich flexibility from software controlled reconfigurability and programmability for multi-standard, multi-mode, multi-user and multi-channel applications.

This dissertation presents novel contributions for a practical SDR system across a full spectrum. For an SDR system, all system performance requirements need to be re-analyzed and re-evaluated accordingly. As an example, the dissertation thoroughly analyzed the system EVM for the impact from the local oscillator imperfections. As the most important enabling technology, the design requirements and challenges for the data converters of an SDR system have been discussed in extensive detail with one exemplary design shown. A novel reconfigurable switched-capacitor FIR filter design has been mathematically modelled with design details and simulation results presented. This filter can enable the SDR system for many practical applications for its full flexibility to be reconfigured to different FIR filter structures or different combined N-path filters to have filter characters as LPFs, HPFs, BPFs, BSFs, multi-band BPFs and frequency equalizers. As another major part of the SDR system, a fully designed SDR digital front-end was presented and discussed. This SDR digital front-end has been designed to support

multi-standard, multi-user, multi-mode and multi-channel application for a cellphone system with optimized design area/cost and power efficiency. Within this SDR digital front-end design, the most challenging designs for being an SDR have been resolved by a highly optimized, time interleaved, polyphase digital FIR design and an innovative arbitrary fractional ratio resampler design. These are accompanied by architecture, design detail, and simulation results.

Due to the rapid improvement of all enabling technologies, we are now witnessing the revolution from the traditional dedicated radio to the SDR. Future works will focus on making every functional block in the system fully software-defined and making the whole system integrated altogether. Among all building blocks for the SDR, further developments and improvements need to be done for the reconfigurable RF/analog filter to have a higher quality factor, better flexibility, lower power consumption and lower cost. Moreover, the PA and LNA designs for the SDR would also need to be improved for more reconfigurability and programmability.

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