Superconducting Flexible Cables For Cryogenic Applications

by

George A. Hernandez

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Approved by

Michael C. Hamilton, Chair, Associate Professor of Electrical and Computer Engineering
Fa Foster Dai, Professor of Electrical and Computer Engineering
Michael E. Baginski, Associate Professor of Electrical and Computer Engineering
Lloyd S. Riggs, Professor of Electrical and Computer Engineering
Minseo Park, Professor of Physics

Abstract

In systems for cryogenic electronics experiments and applications containing multiple temperature stages down to the milliKelvin temperature range, such as in quantum computing research performed in dilution refrigerators, significant effort is undertaken to limit thermal leakage between the various temperature stages. In order to route many RF/microwave/high-speed signals, a large number of semi-rigid coaxial cables are generally used. From a practical perspective the number of microwave connections is limited; due to the thermal load imposed on the cryogenic system, as well as space and volume constraints within the refrigerator. As advances in cryogenic electronics are made, the number of connections that can be achieved could potentially limit its scalability. Consequently, there is a need for high-density, low-loss, low thermal leakage cables. Polyimide has been shown to have exceptional mechanical and thermal properties at cryogenic temperatures. Polyimide as a substrate material with Nb traces has been commonly used in relatively low-frequency ($<$ MHz) applications such as superconducting focal plane arrays. This work addresses the need for even lower loss microwave interconnects by using thin-film processing methods to fabricate controlled-impedance superconducting microstrip cables on 20 μm thick PI-2611 polyimide and on 50 μm thick E-series Kapton films with 250 nm thick Nb traces and ground planes. In this work, we also studied embedded microstrip transmission lines and Nb cladded with Cu and Al microstrip transmission lines. We also implemented distributed element models to match measurements that took into account the kinetic inductance effects on the microwave performance. The fabricated microstrip flex cables were measured at 4.2 K, in liquid He, and up to a frequency of 14 GHz.

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List of Abbreviations

ϵ_r	Dielectric constant
λ_L	London penetration depth
ξ	coherence length
L_k	Kinetic Inductance
Z_0	Characteristic impedance
ADS	Keysight Advanced Design Systems
ALN	Aluminum nitride
CBCPW	Conductor Backed Coplanar Waveguide
CPW	Coplanar Waveguide
DC	Direct Current
DI	Deionized
DUT	Device Under Test
EBPVD	Electron Beam Physical Vapor Deposition
FEM	Finite Element Model
HMDS	Hexamethyldisilizane
IC	Integrated Circuit
LHe	Liquid Helium

LN_2	Liquid Nitrogen
M	Molar
M0	Ground plane
M1	Signal metallizaton
M2	Top ground plane
MLIN	Microstrip Line Element
NaCl	Sodium Chloride
NiCr	Nichrome
PT	Pulse Tube Cryostat
R_{sh}	Sheet Resistance
RRR	Residual Resistivity Ratio
SOL	Short-Open-Load
SOLR	Short Open Reciprocal Thru
SOLT	Short Open Load Thru
STS AOE	Advanced Oxide Etcher
T_c	Transition Temperature
TRL	Thru-Reflect-Line
UBM	Under Bump Metallurgy
Via01	First via contact to the ground plane
Via12	Via contact to the underlying signal and ground layer

YBCO Yttrium Barium Copper Oxide

YSZ Yttria-Stabilized Zirconia

Chapter 1

Introduction

1.1 Scientific motivation

There has been a limited amount of research in addressing the need for low-loss, small cross-sectional area microwave flex cables for cryogenic applications. Previously published work has shown the potential of 1/2 oz. (∼18 μm) thick copper conductors on 5 mil (∼127 μm) thick Kapton films for microstrip and stripline microwave flex cables [1, 2]. Bai et al., demonstrated superconducting Nb microstrip resonators on 2 mil (∼50 μm) Kapton with metallization that was only 250 nm thick [3]. Microwave loss measurements of the Kapton dielectric at 1.2 K by [3] suggests that Kapton might be a suitable substrate for superconducting Nb microstrip flex cables.

Current microwave cables used at deep cryogenic temperatures consist of coaxial cables whose signal conductor is comprised of a superconducting metal that exhibits zero DC loss, with no joule heating and minimal attenuation at these temperatures [4]. Superconducting coaxial cables that can be used up to 65 GHz can be readily purchased from vendors, such as Keycom[1] and Coax Corporation[2]. These types of RF cables would be used at a 4 K temperature stage and below where the superconductor is sufficiently below its critical transition temperature. For temperatures above 4 K, there are coax cables whose signal conductor is comprised of a poor electrical conductor, such as stainless steel or copper nickel (CuNi). The poor electrical conductivity limits the thermal conductivity, by the Wiedemann–Franz law, which relates the thermal conductivity to the electrical conductivity by a constant of proportionality, known as the *Lorenz number*, that is dependent on the metal. For multiple

[1] `http://www.keycom.co.jp/eproducts/upj/upj6/page.htm`
[2] `http://www.coax.co.jp/en/pdf/superconducting_cable.pdf`

DC connections, there are wire looms that consist of NbTi that can be used at deep cryogenic temperatures (mK range) [5, 6]. For 4 K and above, wire looms and multi-conductor wires of phosphor bronze are also readily available[3,4]. The purpose of using poor-thermal conductors is to reduce the thermal leakage from the "hot" side to the "cold" side. For RF measurements, making multiple connections requires the use of multiple-coax and/or the use of microwave switches to reduce the number of coax connections that are routed in the refrigerator [7, 8].

Consequently, as the complexity of the devices tested at cryogenic temperatures increases, the physical volume constraints of the refrigerator may impose limitations. Therefore, in this work, we attempt to leverage Integrated Circuit (IC) thin-film processes to build superconducting microstrip flex cables that at most have a dielectric thickness of 50 μm with a conductor metallization thickness of 250 nm. In one flex cable, we can include multiple controlled impedance microstrip that can be interfaced with commercial end launch connectors. Therefore, we can reduce the cross-sectional area of the flex cables by using thin-film dielectrics, have significantly more connections per cable than a single coax and by using superconducting metals, we decrease the microwave loss.

This work is focused on the simulation, fabrication, and measurement of thin-film superconducting Nb microstrip cables designed to be interface with edge launch connectors. Microstrip and embedded microstrip are demonstrated, with discussion of alternative transmission line flex cables that were attempted early in this project.

1.2 Superconducting materials selection

There are several elemental superconductors that range in transition temperature (T_c) from 9.3 K for Nb to Rh with a T_c of 0.325 mK. A graphical view of the table of elements with the superconductors highlighted in either green (superconducting under high pressure) or blue (superconducting at ambient pressure) is shown in Figure 1.1. The only pure metals

[3] http://www.cryoconnect.com/markets/science/

[4] http://www.lakeshore.com/products/cryogenic-accessories/wire/pages/overview.aspx

that do not exhibit superconducting properties are copper, gold, and silver. The criteria for selecting the superconducting metallization for this work was based on the T_c and the deposition method. From Figure 1.1, materials such as lead, indium, aluminum and niobium were suitable material choices; these metals can be deposited by either sputter deposition or electron beam physical vapor deposition (EBPVD). Lead has a T_c of 7.2 K and can be sputter deposited, but is toxic and an environmental hazard. Indium can be either deposited by sputter or by EBPVD methods, but has a transition temperature of ∼3.4 K and a melting temperature of 160 °C, which is not compatible with the cure temperature (225 °C and above) of the spin-on dielectrics we used in this work. Aluminum has a T_c of 1.2 K and can be deposited by EBPVD or by sputter deposition, but has a significantly lower T_c than Nb. In addition, measuring the superconducting properties of Al would be difficult in our pulse-tube based cryostat with the lowest operating temperature achievable is ∼1.3 K, which cannot be continuously maintained.

Nb has a bulk T_c of 9.3 K [9] and can be sputtered deposited with a controlled film morphology [10, 11]. The relationship between the room temperature sheet resistance (R_{sh}) and T_c are well correlated. Typically, a low sheet resistance yields a T_c closer to bulk [10]. From Figure 1.2, we can see the trend towards a higher T_c, as the sheet resistance of the Nb film on SiO_2 decreases. Moreover, the deposition parameters are important, in order to limit oxygen diffusion through the Nb film [10]. Therefore the deposition conditions for Nb need to be optimized to produce high quality (low R_{sh} and high T_c) films. It is also possible to use EBPVD method to deposit Nb [12], but this method was not attempted in this work. We chose to DC sputter Nb films, as it led to consistent film quality.

1.3 Microwave properties of superconductors

The microwave properties of superconductors can be described by a two-fluid phenomenological model [14]. We assume that in the superconductor there are two types of fluids, normal electrons (quasi-particles) and superconducting electrons (Cooper pairs). The

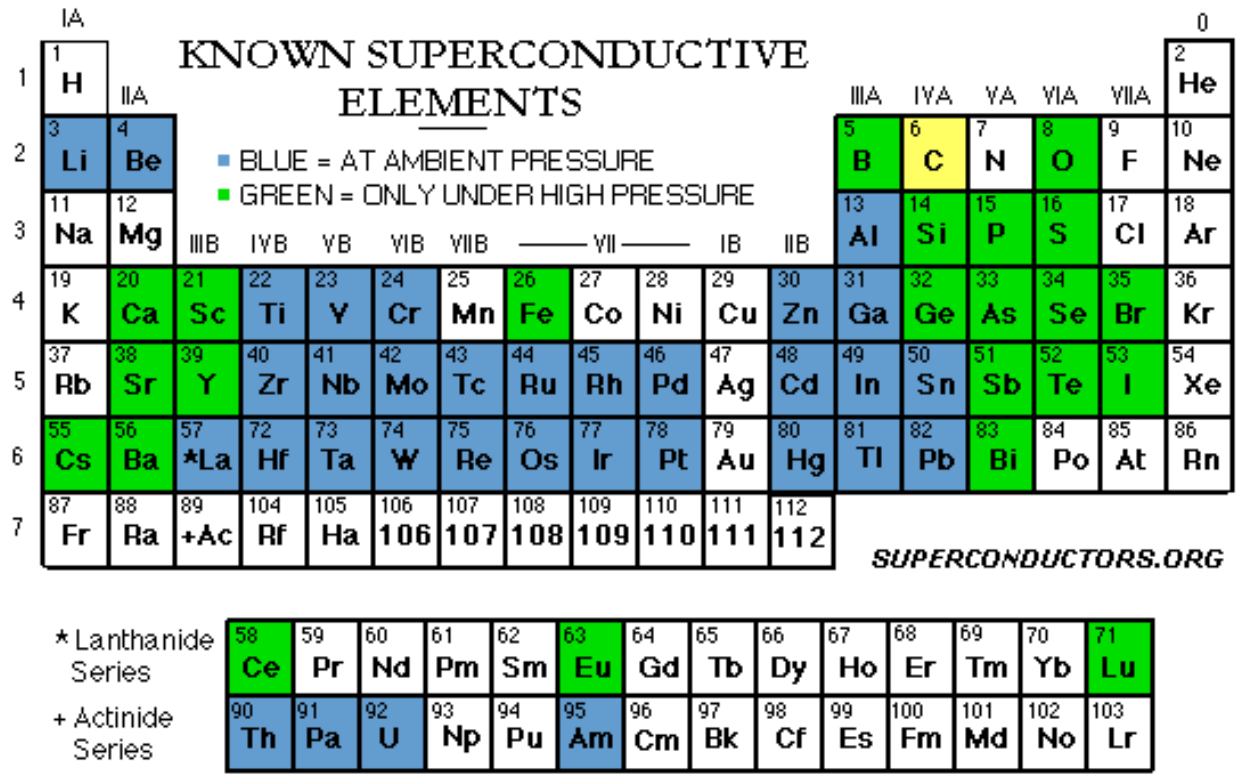

Figure 1.1: Periodic table of elements with known superconductors at ambient pressure and under high pressure highlighted in blue and green, respectively. Adapted from [13].

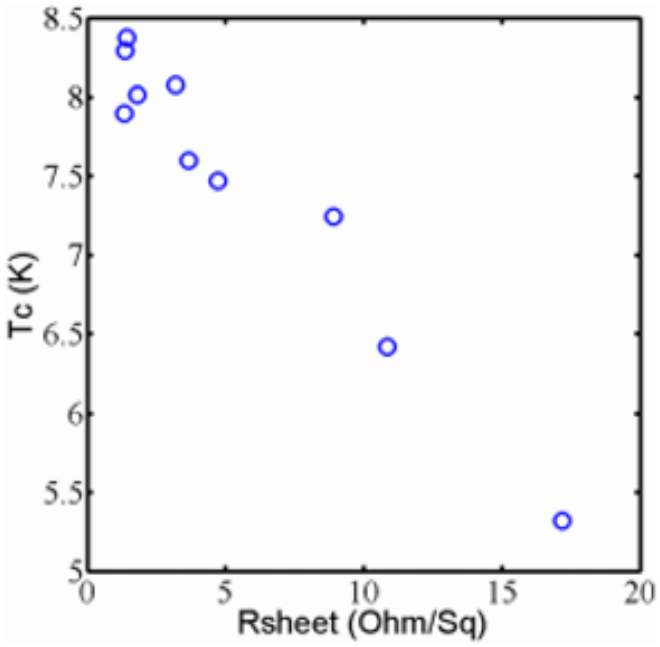

Figure 1.2: Relationship between sheet resistance and transition temperature for sputter deposited Nb films on SiO_2. Adapted from [10].

normal electrons travel in the lattice, as they do in any normal metal (i.e. experience scattering), when an electric field is applied, the quasi-particles lose some energy due to scattering, which is measured as an electrical resistance. The normal electrons also have a mass, therefore when an alternating field is applied, there is a time delay for the electrons to react, which is represented as an inductance. This inductance is significant when the frequency of the oscillations is significantly higher than the scattering rate, otherwise this phenomenon is not observed.

Superconducting electrons (Cooper pairs) do not experience scattering, they travel through the lattice by a phonon-electron interaction and therefore exhibit zero resistance [15]. Superconducting electrons also have a mass and therefore also exhibit an inductance. Both the quasi-particles and Cooper pairs can be thought of as fluids in a superconductor, which interact by screening the applied field.

To describe these fluids and their interaction to an applied field, we consider their number density. The density of normal (N_n) and superconducting electrons (N_s) is constant in the metal (conservation of mass and charge). Therefore, the total density of electrons is defined as $N = N_s + N_n$; when the temperature is decreased, the density of superconducting electrons increases and consequently the density of quasi-particles decreases. The temperature dependence is described to have a power dependence: $N_n/N = t^4$, where $t = T/T_c$ is the normalized temperature [14]. The temperature dependence is shown in Figure 1.3. For example, Nb with a bulk T_c of 9.3 K, when measured at a temperature of 4.2 K, we calculate the normalized temperature ratio to be $(0.45)^4$ or ~ 0.041. Therefore, approximately 4 % of the electrons would be normal, while 96 % would be superconducting electrons. At DC, superconductors exhibit zero resistance, this is because the superconducting electrons short the sample, although the normal electrons are present [14]. At higher frequencies, the superconducting electrons lag in response to alternating field and therefore do not completely short the circuit, consequently some of the normal electrons will carry the current with an increase loss. The circuit model that depicts this phenomenon is shown in Figure 1.4.

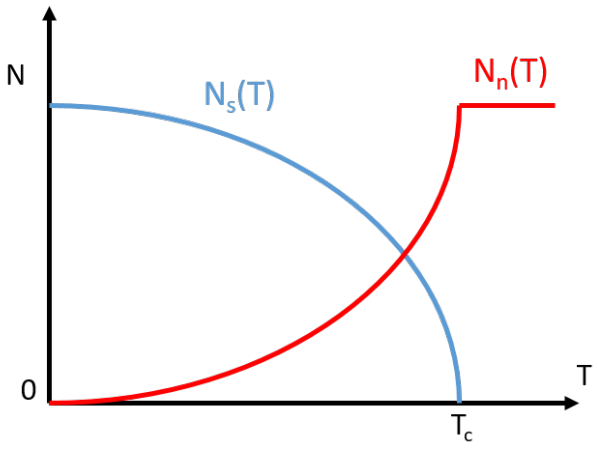

Figure 1.3: Temperature dependence of the normal electrons (N_n) and superconducting electrons (N_s). Adapted from [16].

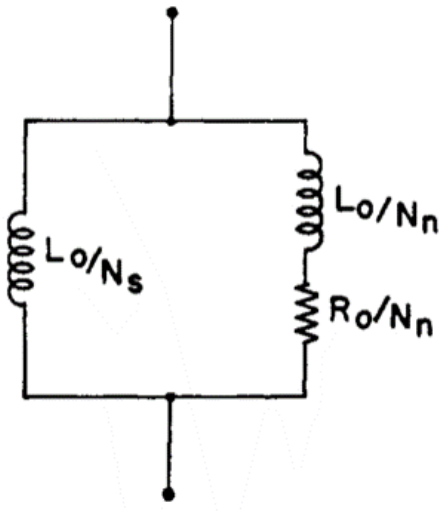

Figure 1.4: Two-fluid circuit model for a superconductor. N_s is the number density of superconducting electrons and N_n is the number density of the normal electrons. Adapted from [14].

We define a complex conductivity of the superconductor as a function of current carried by the normal electrons and the superconducting electrons. By using ohm's law J=σE and assuming a local relationship with an applied time dependent electric field, $E = E_0 e^{i\omega t}$ we can solve for Equations 1.1 and 1.2 to obtain the relationship shown in Equation 1.3 [14]. In these equations, m is the mass of an electron, e is the charge of a single electron, τ is the scattering time for the normal electrons, and ω is angular frequency [14].

$$m\frac{dj_n}{dt} + \frac{m}{\tau}j_n = N_n e^2 E, \quad j_n = N_n e v_n \tag{1.1}$$

$$m\frac{dj_s}{dt} + N_s\omega^2 E, \quad j_s = N_s e v_s \tag{1.2}$$

$$j_0 = j_{n0} + j_{s0} = \sigma E_0 = [\sigma_1 - i\sigma_2]E_0 \tag{1.3}$$

$$\sigma_1 = N_n e^2 \tau/m, \quad \sigma_2 = \frac{e^2}{m\omega}[N_s + N_n\omega\tau] \tag{1.4}$$

Equations 1.3 and 1.4 essentially state that the conductivity is comprised of normal-state (σ_1) conductivity and a mix of normal and superconducting conductivity (σ_2), in both cases, τ is the scattering time of the normal electrons. At low temperatures, sufficiently far away from T_c, σ_2 dominates and the normal-state (N_n) electron density can be assumed to be zero. Therefore Equation 1.4, can be re-written as the expression shown in Equation 1.5

$$\sigma_2 = \frac{e^2}{m\omega}N_s \tag{1.5}$$

Two material properties that define the quality of the superconductor are the coherence length denoted as ξ and the London penetration depth (λ_L). The coherence length can be thought of as the extent of the superconducting electrons (Cooper pairs) [14], while the

London penetration depth is related to the depth a magnetic field can penetrate into a superconductor [17]. For high-quality Nb, the London penetration depth has been measured to be approximately 39 nm [18]. The mean free path can be determined through the relationship shown in Equation 1.6, where l is the mean-free path. The mean-free path l of the superconductor can be estimated by measuring the grain-size of the deposited film [19]. In an ideal superconductor, ξ would be equal to ξ_0 ($l = \infty$), this would imply a perfect superconductor. For a thin-film, that is sputter deposited, with the condition that the penetration depth (λ_L) is greater than the mean-free path (l), we have a local J=σE relationship. This implies that the superconductor has a uniform current distribution throughout. We can then define the impedance of the film as described in Equation 1.7.

$$\frac{1}{\xi} \simeq \frac{1}{\xi_0} + \frac{1}{l} \tag{1.6}$$

$$Z = R + iX \tag{1.7}$$

The real (R) and reactive (X) components are related to the conductivity, σ_1 and σ_2 by the relationships shown in Equation 1.8. b is defined as the cross-sectional area of the film.

$$R = \frac{\sigma_1}{b(\sigma_1^2 + \sigma_2^2)} \quad X = \frac{\sigma_2}{b(\sigma_1^2 + \sigma_2^2)} \tag{1.8}$$

Equation 1.8 implies a few things that are worth noting. Primarily, if the temperature is low enough ($T \ll T_c$), the real term, R $\sim$ is 0 and $Z = iX$. Which implies that the impedance is purely due to the superconducting electrons responding to the applied field. Explicitly, the reactive term can be defined as shown in Equation 1.9. We then define the kinetic inductance as shown in Equation 1.10. L_k is dependant on the density of superconducting electrons, the number density, the cross-sectional area, electron charge and mass.

$$X = \frac{1}{b\sigma_2} \quad X = (\frac{m}{e^2 N_s})(\frac{1}{b})\omega \tag{1.9}$$

$$L_k = \frac{m}{e^2 N_s}\frac{1}{b} \tag{1.10}$$

The reactive term is referred to as a kinetic inductance (L_k). In the case that that the temperature is not far away from T_c, the superconductor will have a small but non-negligible resistance due to the quasi-particles (normal electrons) which is known as BCS resistance [20].

1.3.1 Kinetic inductance

Kinetic inductance is related to the motion of charge-carriers in a metal. The kinetic inductance is a property of all metals. In normal metals, the mean scattering time τ, is in the order of 10^{-14} seconds [21], which implies that the applied signal should be greater than $f{=}\frac{1}{\tau}$, which would require a signal to be changing in the THz frequency range, these collisions dominate the loss mechanism, and therefore the kinetic inductance is not observed. In superconductors, τ is infinity for the Cooper pairs (no collisions), and the kinetic inductance plays an important role in the microwave performance. For example, in a microstrip structure, such as the one shown in Figure 1.5a, the kinetic inductance is included as an additional series element in a circuit element model. In Figure 1.5b, a representative simplified circuit model of a microstrip is shown, we note that L_k is the kinetic inductance and L_m is the magnetic inductance. Therefore the total inductance in the microstrip structure is $L_k + L_m$. We can think of the kinetic inductance and magnetic inductance as two forms of stored energy. This relationship is shown in Equation 1.11 [22].

A diagram of a superconducting film is shown in Figure 1.6 that is used to derive the relationship between magnetic and kinetic energy of the charge carrier motion. The relationship shown in Equation 1.11 states that the total energy of a structure is the sum of the magnetic energy and the charge carrier motion over the volume of the conductor.

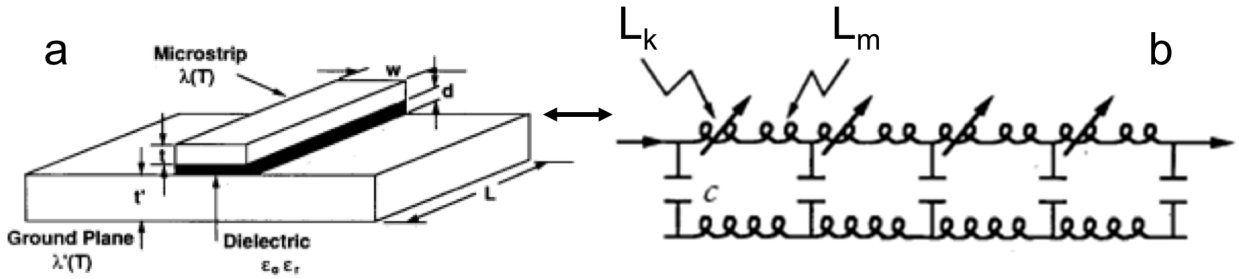

Figure 1.5: (a) Cross-sectional image of a microstrip (b) equivalent circuit model with the kinetic inductance (L_k) included as a series element. Adapted from [23].

Equation 1.11 reduces to Equation 1.12, after integration [22]. In this equation, l is the length, A is the cross-sectional area, e is electronic charge, and I is the current. This relationship describes the contribution of the Cooper pairs to the kinetic inductance.

$$E = \int_{all\ space} \frac{1}{2}\mu H^2 d\tau + \int_{conductor} \frac{1}{2} m v^2 N_s d\tau \tag{1.11}$$

$$E = \frac{1}{2} L_M I^2 + \frac{1}{2}[(m/N_s e^2) \cdot (l/A)] I^2 \tag{1.12}$$

The kinetic inductance L_k is related to London penetration depth by the relationship shown in Equation 1.13. The l term is the length and a and b are the half-width and half-height, λ is the magnetic penetration depth [22].

$$L_k = (\mu_0 l \lambda / 4a)[2/\pi^2) ln(4a/b)] \quad b \gg \lambda \tag{1.13}$$

1.4 Flexible cables

The focus of this section is to review the previous work undertaken by other research groups in the area of cryogenic flexible cables. Although commercial flex cables with copper

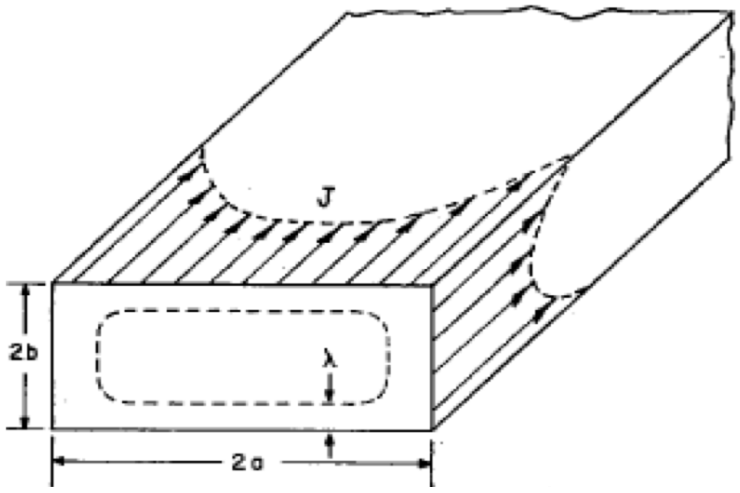

Figure 1.6: Cross-sectional diagram of a rectangular superconducting film. J is the surface current and λ is the London penetration depth. a and b are the half width and height, respectively. Adapted from [22].

metallization for the signal and ground is common, very limited work has been undertaken in using superconducting metallization on flexible substrates.

In the work by van Weers et al., embedded Nb DC flexible cables were fabricated on Pyralin PI-2611 that had a dielectric thickness of 19 μm and a length of 130 mm, with 10 DC traces that were comprised of superconducting Nb encapsulated in Pyralin PI-2611 [24]. These flex cables were fabricated on a temporary glass carrier that was removed at the end of the fabrication process. A cross-sectional diagram of the flex cable is shown in Figure 1.7a.

The DC lines ranged in line widths from 15 to 25 μm that were lithographically defined on a 12 μm thick PI-2611 layer and sputtered with a 15-20 nm thick Ti layer for adhesion, followed by DC sputtering of Nb that was 250 nm thick. These traces were protected by a second Pyralin coating that was 7 μm thick. Contact holes were dry etched in the pyralin to make contact to the Nb and an under bump metallurgy (UBM) consisting of Ti/Cu/Ni/Au was deposited onto the exposed Nb signal traces. Following the deposition of the UBM layer, a solder paste (Ecorel easy 803s) was applied locally with a syringe. The flex was then

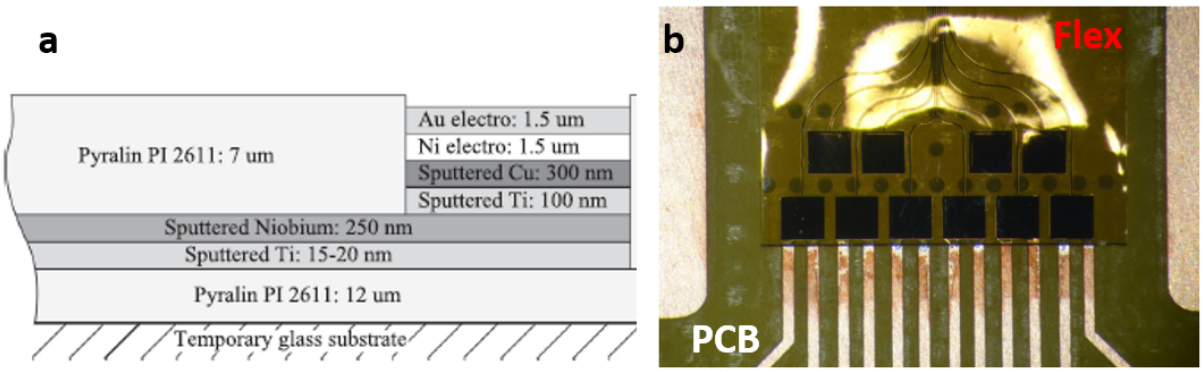

Figure 1.7: (a) Cross-section of a Nb DC flex cable (b) top-view of the Nb flex cable mounted onto a PCB. Adapted from [24].

aligned and clamped to a printed circuit board (PCB) and the assembly was reflowed. The Nb flex cable after assembly onto a PCB is shown in Figure 1.7b.

DC measurement of the T_c for a 25 μm wide line is shown in Figure 1.8. The two distinctive drops in resistance at ~9 and 7.8 K are representative of the Nb and SnPb solder transitioning to the superconducting state. Measurements of critical current of these lines indicated a current range between 7 mA to over 60 mA, based on the different line widths that were measured [24].

This same group also studied a Nb flex cable that was fabricated in-situ with a silicon detector chip, as shown in Figure 1.9. This flex cable consisted of Nb traces that were embedded in polyimide with UBM that was compatible with the transition edge sensor array [25]. The Nb traces varied in line widths, from 14 to 10 μm and were embedded in polyimide that was cured at 350°C. A thin Ta layer that was 10 nm thick coated the Nb traces to prevent oxidation and in some locations a 400 nm thick SiO_2 was also used on top of the Ta to protect the Nb from the handling stresses and the high temperature cure of the polyimide. A cross-sectional schematic of the flex cable is shown in Figure 1.9a. The flex was attached onto two different Si substrates that had traces that matched the profile of the flex cable. Figure 1.9b is a top-view of the flex attached to the LC and detector chip. We

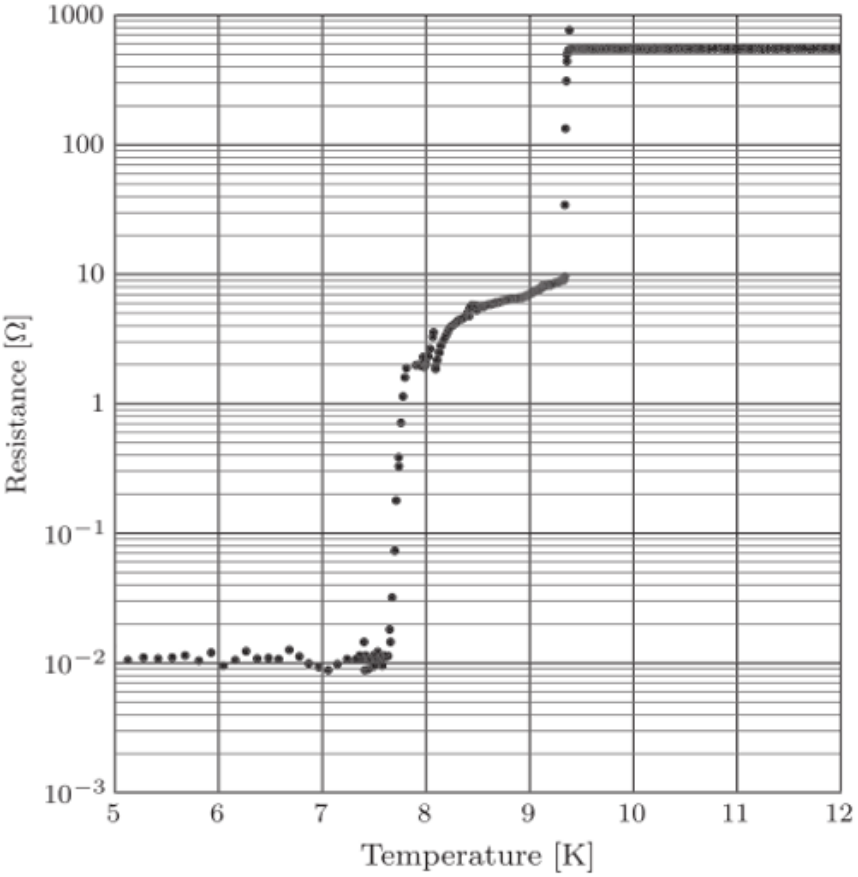

Figure 1.8: Resistance vs. temperature measurement of a DC flex cable with a Ti/Nb/Ti signal trace with a line width of 25 μm. Adapted from [24].

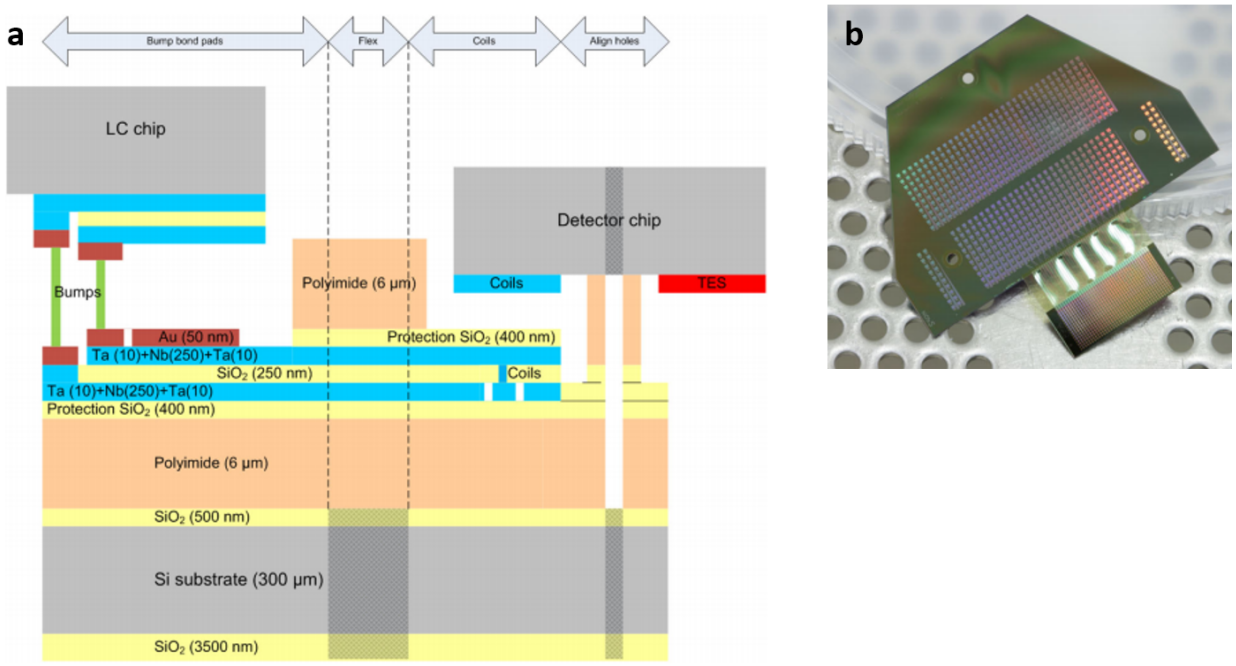

Figure 1.9: (a) Schematic cross-section of a Nb DC flex cable attached to a LC filter and detector (b) LC filter attached to the flex cable by a bump array. Adapted from [25].

note in this work that their smaller line widths had a lower transition temperature of ∼7 K compared to the 14 μm track width that had a T_c of ∼7.5 K. Correspondingly, the 10 μm wide line had a lower residual resistivity ratio (RRR) of 3.6, meanwhile for the 14 μm wide line, the RRR was determined to be 5.6. The measurement results of these two traces is shown in Figure 1.10. The authors' noted that for smaller line widths, the Nb traces did not fully transition. At present, the experimental reason the superconductivity was suppressed in the Nb is currently not well understood.

In the work by Yung et al., they fabricated MgB_2 flex cables on flexible Yttria-stabilized zirconia (YSZ) substrates with 33 DC signal traces per cable [26]. The flex cable was 50 μm thick and 10 cm long. Connections were made to flex cable through a PCB and flat flexible connector (FFC) interface. The flex cable assembly is shown in Figure 1.11. The DC critical current of this flex cable was measured through the FFC/PCB interface. The critical current density at 30 K was measured to be $10^5 A/cm^2$. Measurements of the critical current, as a

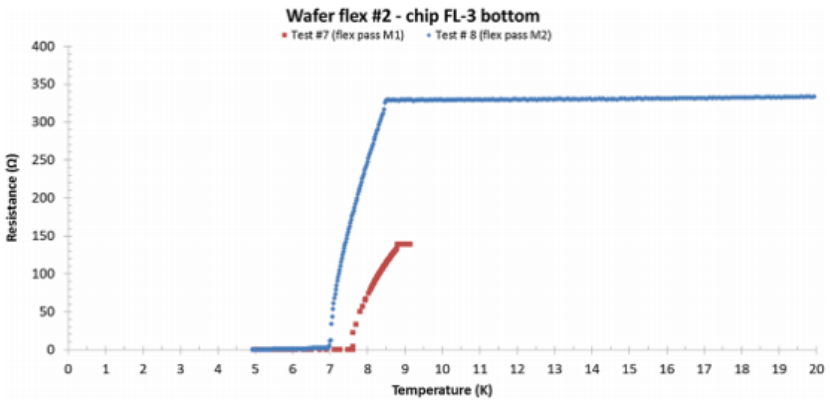

Figure 1.10: Resistance vs. temperature measurement of 12 μm (shown in blue) and 14 μm (shown in red) wide Nb traces embedded in polyimide. Adapted from [25].

function of temperature are shown in Figure 1.12b on two different substrate materials. The resistance vs. temperature measurements were taken on a 1 cm $\times$ 1 cm witness samples, the measurement results are shown in Figure 1.12a. From Figure 1.12a, we note the T_c was approximately 37 K, which is particularly high compared to pure elemental superconductors (e.g. Nb with a T_c of 9.3 K).

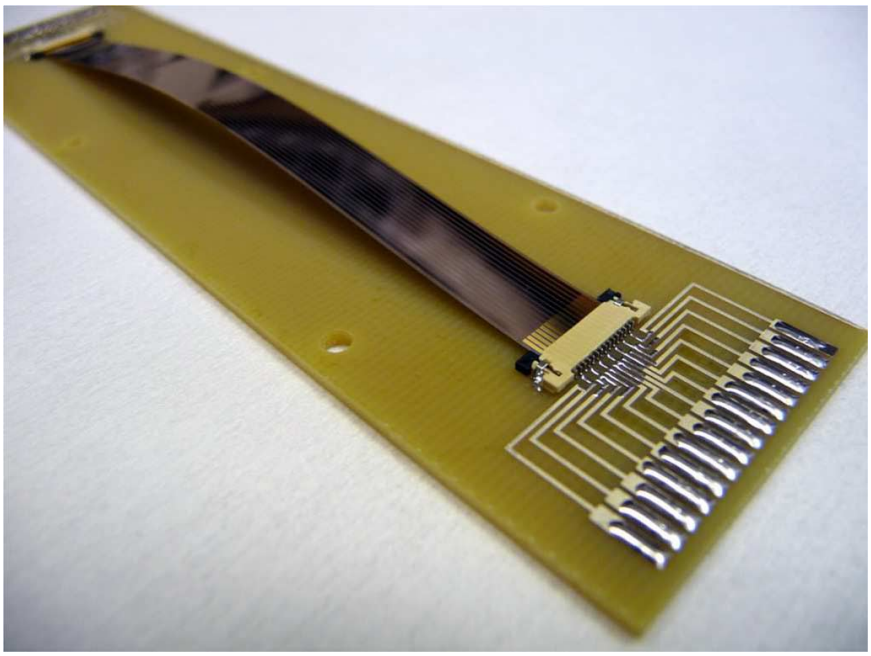

Figure 1.11: MgB_2 flex cable with 350 μm wide traces interfaced to a PCB through an FFC. Adapted from [26].

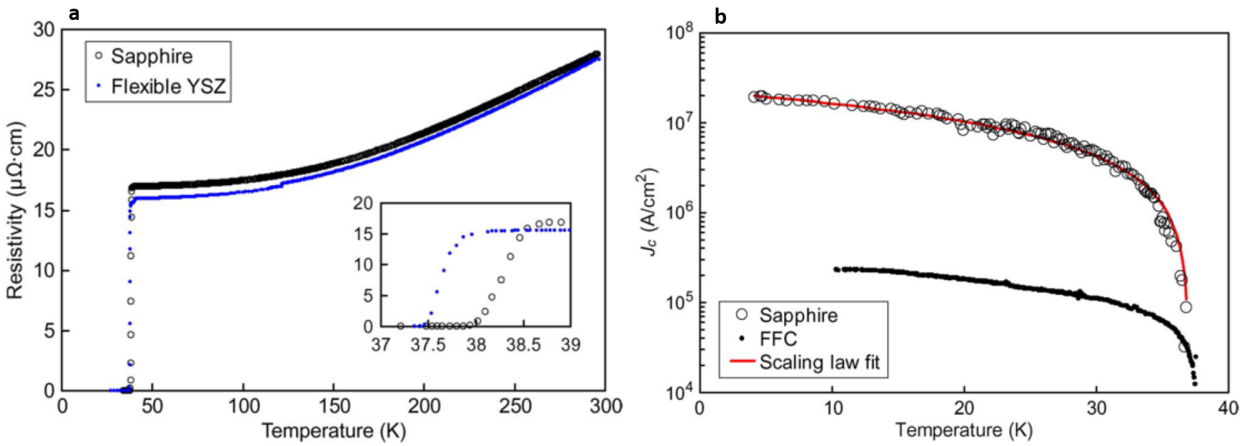

Figure 1.12: (a) Resistance vs. temperature measurement of a MgB_2 trace on sapphire and on a YSZ flexible substrate (b) critical current measurement as a function of temperature of MgB_2 on sapphire for a 2 μm wide trace and measurement through the flex of a 350 μm wide trace, interfaced with an FFC connector. Adapted from [26].

Although the MgB_2 flexible cable exhibited notable electrical properties, the authors highlighted a few problems related to the reliability of these cables. For example, the MgB_2 delaminated from the substrate when exposed to water at 20 °C (room temperature). Therefore, two different types of passivisation materials were studied, Parylene-C and aluminum oxide (Al_2O_3). Parylene was deposited by vapor-phase to a thickness of ∼500 nm, while the Al_2O_3 was deposited by atomic layer deposition (ALD) to a thickness of 10 nm. These two coatings prevented the MgB_2 from delaminating from the substrate in a period of 24 hours when exposed to DI water. If the water was heated to 90 °C, the films began to degrade in less than an hour [26].

Webber et al., fabricated DC flex cables based on a high temperature superconducting metal consisting of Yttrium barium copper oxide (YBCO) on a flexible haste alloy tape [27]. Haste alloy is a conductive material and therefore this group isolated the YBCO traces from the underlying substrate by depositing an insulating MgO layer, prior to the deposition of the YBCO traces. These flex cables were 100 mm long and 50 μm thick with a YBCO thickness of 1 μm and protected from the environment by coating of Teflon film. The author's note

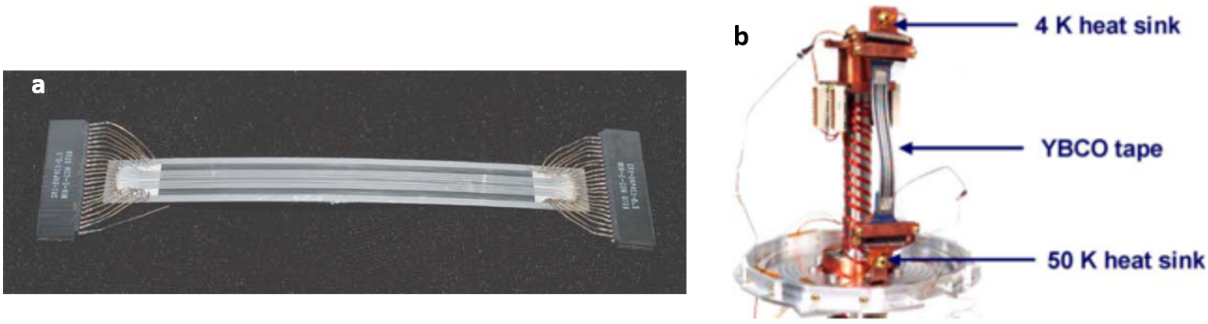

Figure 1.13: (a) YBCO flex cable connected to a *Min-E-con* DC adapter and (b) flex cable mounted onto a cryocooler. Adapted from [27].

that Teflon coating was necessary to prevent moisture from degrading the YBCO film. Each cable consisted of 22 lines with a maximum critical current of 200 mA. These flex cables were interfaced with a *Min-E con* connector via a Cerrobend mixed alloy to 3 μm thick silver pads. The Cerrobend metal alloy was important because it has a melting temperature of 70 °C, which prevented the scavenging of silver from the contact pads [27]. A stand alone YBCO flex cable is shown in Figure 1.13a. The flex cable was mounted onto a cryocooler for testing is shown in Figure 1.13b. The critical currents were measured in liquid nitrogen (LN_2) which showed critical currents as high as 3.0 A on line width of 300 μm. Critical current measurements at LN_2 temperatures as a function of line width are shown in Figure 1.14.

An Al DC superconducting flex cable for interfacing to a transition edge sensor focal plane array was fabricated by Pappas for the Atacama Cosmology Telescope (ACTPol) [28]. The aluminum traces and wire bonds were measured to transition at 1.2 K $\pm$ 0.1 K [28]. The critical current was measured to be 5.7 mA at 1.0 K. In this particular flex cable, they integrated the DC lines in PI-2611 polyimide from HD microsystems. This flex cable had a Si underside beneath the wire bond regions in order to improve the wire bond strength. A cross-section of the flex cable with Si underside support is shown in Figure 1.16.

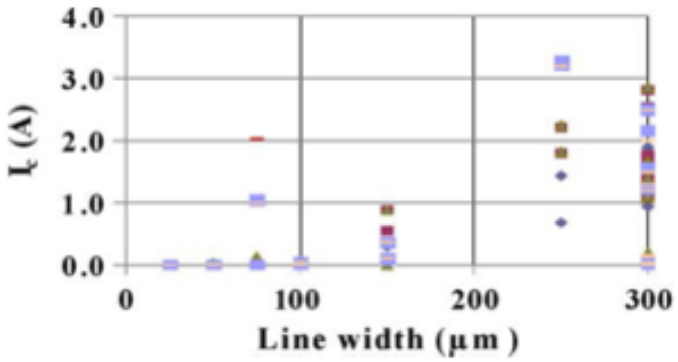

Figure 1.14: Critical current measurements of a YBCO flex cable as a function of line width. Adapted from [27].

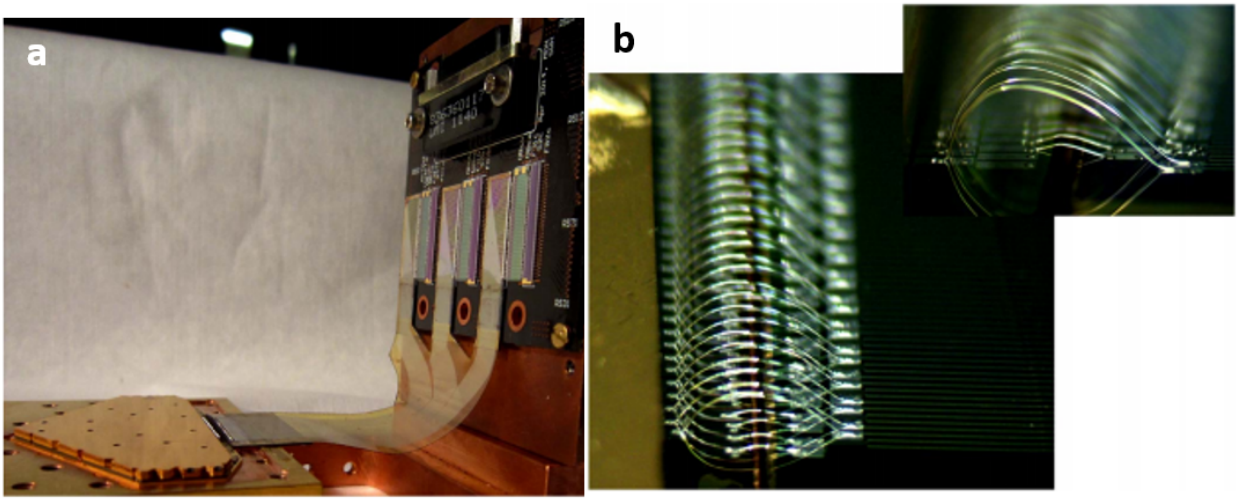

Figure 1.15: (a) High-density superconducting Al flex cable for ATCPol (b) close-up view of the wire bonds attached onto the flex cable and to the support substrate. Adapted from [28].

For RF applications at cryogenic temperatures there has been some progress in integrating multiple signal conductors on thin Kapton films, similar to DC ribbon cables that can be commercially found. A non-superconducting RF flex cable for cryogenic applications was studied by Harris et al., which consisted of a set of microstrip transmission lines on Kapton that used 1/2 Oz.($\sim$18 μm) thick copper as the signal and ground metallization on 5 mil ($\sim$127 μm) Kapton AP-855R [1]. The flex cable was 1.5 inch (3.81 cm) by 4.1 inch (10.4 cm) long. SMA connectors were directly soldered onto the Kapton flex, due to the thickness of the film, no additional support was needed under the SMA connector to make

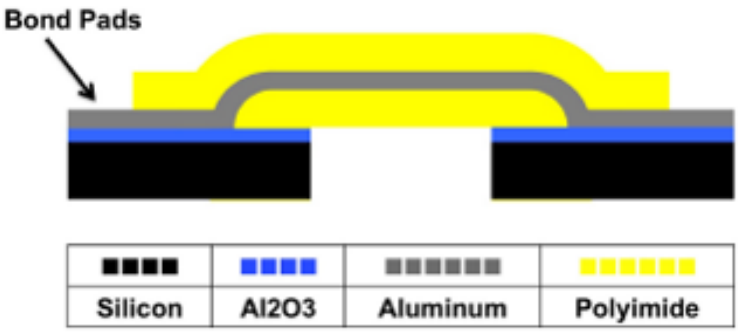

Figure 1.16: Cross-section diagram of Al traces embedded in polyimide with a Si support substrate. Adapted from [29].

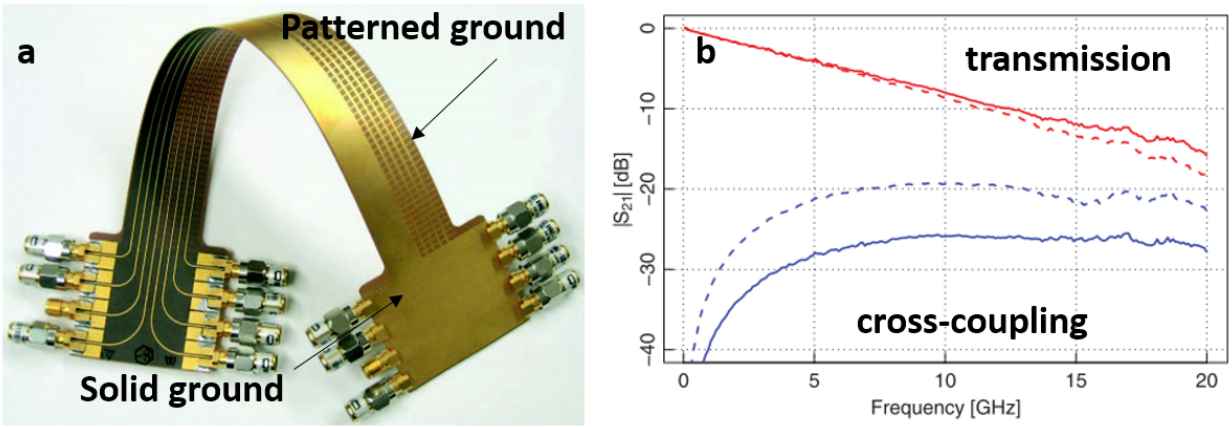

Figure 1.17: (a) Microstrip on Kapton Dupont Pyralux AP-855R with 8 signal traces (b) S_{21} measurement comparison of the flex cable with a solid ground plane (solid line) and patterned ground plane (dashed line). Adapted from [1].

contact. In Figure 1.17a, the Kapton microstrip with 8 signal lines is shown with a slight bend to highlight the solid and patterned ground plane. The patterned ground plane was studied to reduce the thermal heat leakage, which showed slight degradation in performance at the higher frequencies. The microwave performance of this Cu based microstrip flex is shown in Figure 1.17b. The coupling between adjacent signal lines indicates more coupling occurs when the ground plane is patterned when compared to a solid ground plane. These measurements were performed at room temperature.

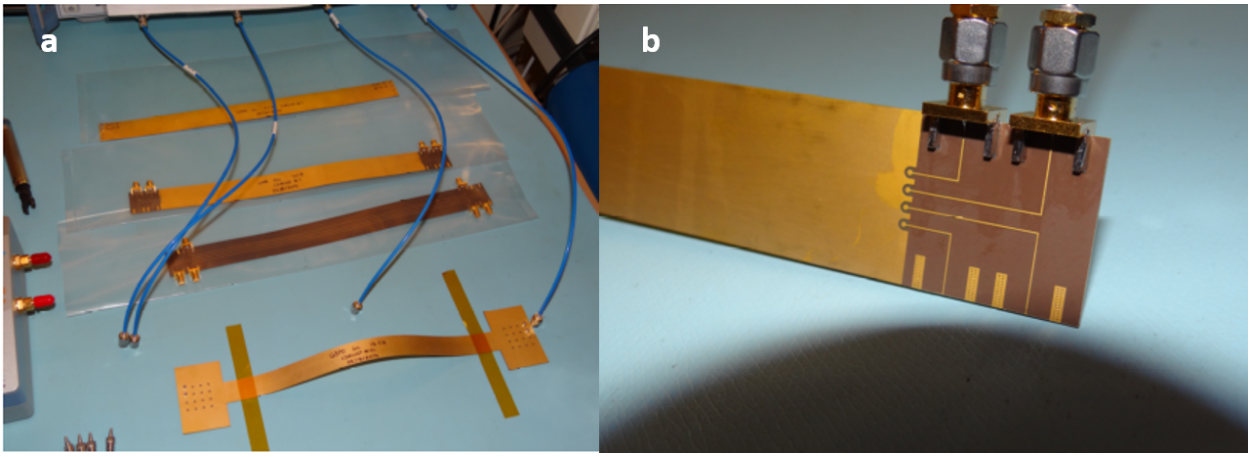

Figure 1.18: (a) Stripline flex cables interfaced with G3PO connectors (b) close-up of the G3PO connectors interfaced to flex signal line and ground. Adapted from [2].

In the work by McGarey et al., they fabricated and measured Cu stripline flex cables for use in a focal plane array [2]. This flex cable had 16 signal lines that were interfaced with G3PO connectors. The flex cables are shown in Figure 1.18a with a close-up view of the underside with the close-up of the backside of the flex shown in Figure 1.18b. The substrate material was Dupont Kapton Pyralux AP with a thickness of 4 mil ($\sim$102 μm) with 1/2 oz. Cu ($\sim$18 μm). To provide mechanical support to the G3PO connectors, they sandwiched a 20 mil ($\sim$508 μm) thick FR4 board between the flex cable and the connector. The microwave performance of the flex cable is shown in Figure 1.19. Transmission shows about -10 dB at 8 GHz and a match that stays below -10 dB up to 10 GHz. The stripline Cu flex cable was also measured at room temperature.

In summary, significant strides have been made in the fabrication and measurement of superconducting and normal-metal flex cables. Many groups have focused on the fabrication of superconducting DC flex cables with multiple conductors on a single ribbon. Some work in addressing the need for multi-conductor cryogenic microwave flex cables has been undertaken by [1] and [2] using Cu-based conductors. The work reviewed demonstrates the potential of flexible DC and microwave interconnects for cryogenic-based systems.

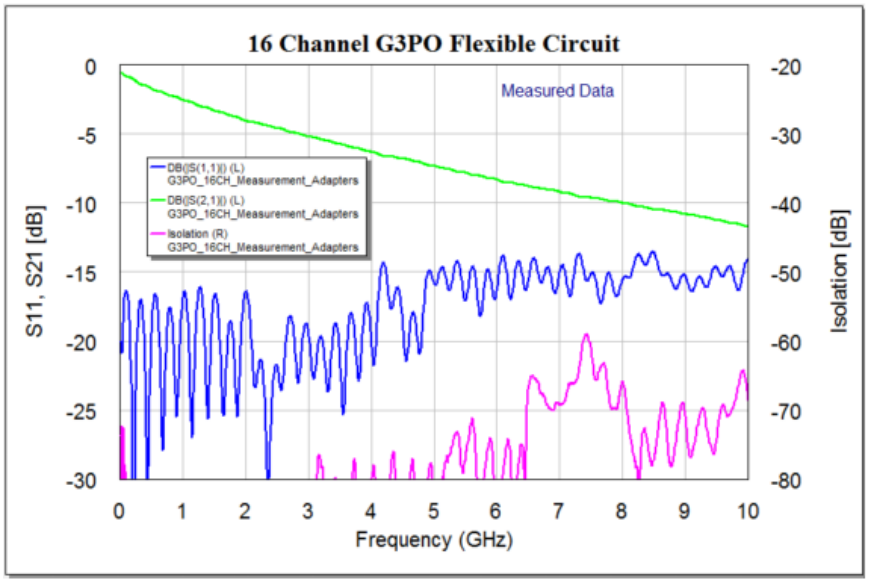

Figure 1.19: Microwave measurements at room temperature of a 16 channel flex cable interfaced with G3PO connectors. Adapted from [2].

1.5 Outline of this dissertation

In this dissertation, we discuss the several microwave flex cable technologies that were attempted and measurement results for the microstrip flex cables that were successfully fabricated. The goal of this dissertation is to provide a foundation for future work in the area of superconducting microwave flex cables. This dissertation is organized as follows:

- The design details such as the dielectric types, thicknesses, and signal line widths for the different dielectrics and transmission lines (coplanar waveguide, stripline, and microstrip) are discussed in Chapter 2.

- The fabrication processes for the various flex cables, which include dielectric spin-on and metal deposition parameters is presented in Chapter 3.

- A description of the measurement equipment and LabVIEW software that was written to automate DC and RF measurements is presented in Chapter 4. We also present the calibration process that was required to correct for measurement errors. We discuss the

calibration standards that were assembled and used to perform a Short-Open-Load-Reciprocal-Thru (SOLR) calibration in liquid Helium (4.2 K).

- Measurement and simulation results for the fabricated microstrip flex cables on Kapton and spin-on polyimide is presented in Chapter 5.

- Concluding remarks and discussion of next-steps for this work is presented in Chapters 6 and 7.

Chapter 2

Design and Layout of Flex Cables

In this chapter we discuss the design, layout, and simulation results of the various RF flex cables and interface methods that were attempted in this work. We studied two types of spin-on dielectrics, AL-X [30] and PI-2611 [31], which are commonly used as interlayer dielectrics. Kapton which is a form of polyimide that can be purchased as a free-standing film was also used. The physical length of these flex cables ranged from several millimeters to up to one meter. We modeled coplanar waveguide, microstrip, and stripline flex cables with Keysight's advanced design software (ADS)[1].

In the work by Tighe et al., they demonstrated stripline Cu flex cables flip chip attached to break out boards [32]; we attempted to use the same attachment method on AlN substrates for some of the flex cables we fabricated. Due to constraints in the size of the Dewar opening and sample holder, our substrate size was limited to ∼25 mm in width and ∼18 mm in length. We designed short (∼4 mm in length) Nb-based conductor backed coplanar waveguide (CBCPW) structures on both ends of an AlN substrate. At the ends of each trace, there was metallization deposited that was compatible with indium soldering. These pads served as attachment points for the flex cables. The CPW traces on the edges of AlN would be soldered with GPPO connectors at each end. The assembled parts would then be attached to a copper holder.

The initial flex cables used for flip-chip attachment were AL-X and Kapton samples. These flex cables were ∼11 mm in length and due to the fabrication and assembly challenges, we did not pursue this assembly method much further. Although, we discuss the RF performance and design of these methods as background to what eventually was established. We

[1] Advanced Design Systems 2015.01

therefore sought an alternative assembly method to make reliable RF connections to the flex cables without the need for flip-chip bonding. A 3D model depicting the holder with GPPO connectors is shown in Figure 2.1.

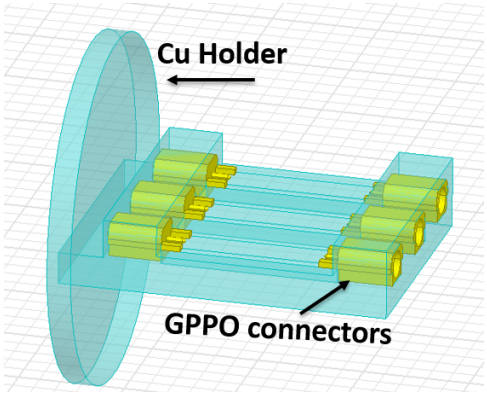

Figure 2.1: A 3D model of the copper holder and the GPPO connectors that would be used to interface to the AlN substrate.

Based on commercially available edge-launch connectors, we determined Southwest Microwave SMA connectors[2] were the most suitable. The edge launch connector has an adjustable grounding plate and a signal pin diameter of only 0.005 inch, which facilitated soldering directly onto our thin flex cables. After working with these connectors, we decided that longer flex cables would allow us to obtain more meaningful measurements. We therefore decided to move towards flex cables with lengths of 5 cm and greater.

The next iteration of flex cables consisted of microstrip and stripline transmission lines that used edge launch connectors. We designed 5 cm and up to one meter microstrip transmission lines on a PI-2611 dielectric. The stripline fabrication process was undertaken on PI-2611, but was inherently more complex, which did not yield fully functional flex cables. We present the layout for a 5 cm and one meter long stripline stripline flex cables for reference. On Kapton, we moved away from the CBCPW structures and focused on microstrip transmission lines only.

[2]Connector information: `http://mpd.southwestmicrowave.com/products/endLaunch.php`

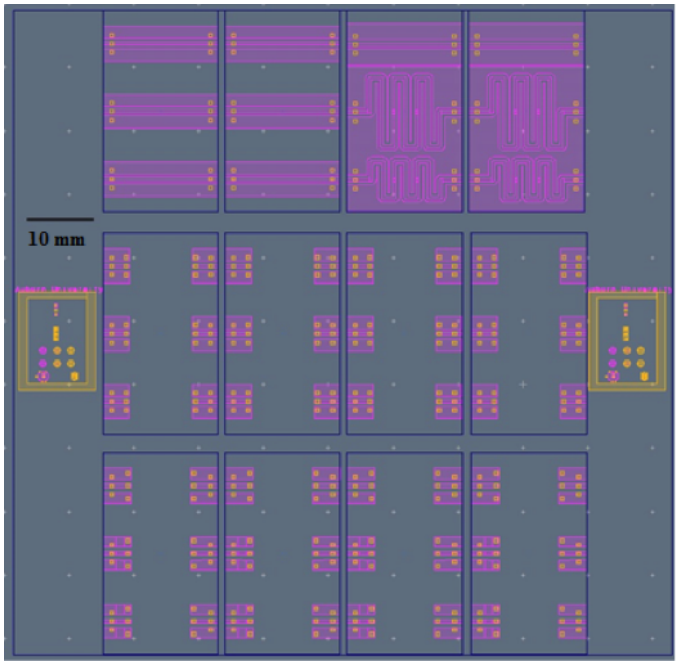

Figure 2.2: ADS layout of CBCPW transmission lines on AlN for flip-chip bonding flex cables.

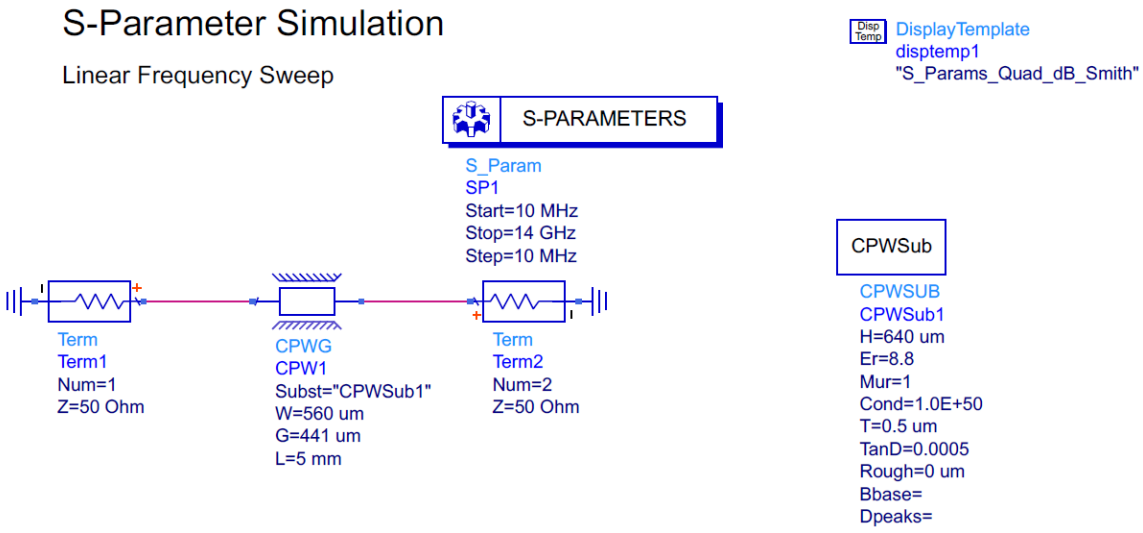

Figure 2.3: Simulation model for one end of a 5 mm long CBCPW on AlN.

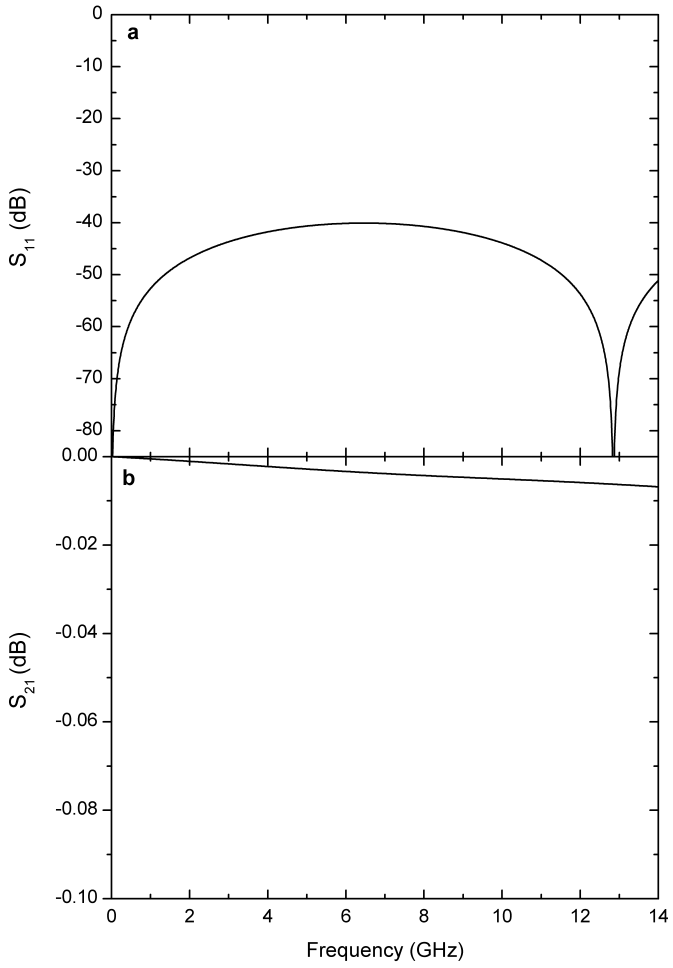

Figure 2.4: (a) S_{11} and (b) S_{21} simulations of a 5 mm long CBCPW on an AlN substrate.

2.1 AlN flip-chip board

Aluminum nitride (AlN)[3] substrates were used as the host board for flip-chip attachment of flex cables. The AlN was designed to have up to six GPPO connectors soldered at each end of the substrate, therefore three flex cables could be measured during one temperature cool-down cycle. We designed a Conductor Backed Coplanar Waveguide (CBCPW) on a 640 μm thick AlN substrate with a signal line width of 560 μm and a gap between the signal and ground of 441 μm. In Figure 2.2, the CBCPW design for the AlN substrate is shown. The design included a straight CBCPW, a meandered version, and short CBCPW structures for flip-chip bonding. The straight and meandered CBCPW designs were included to measure the T_c of the sputtered deposited Nb on the AlN substrate. The UBM is shown as pads on the signal and ground traces on the topside metallization, which were used for soldering connectors and flip-chip attachment. The simulation setup for the short CBCPW used for flip-chip bonding is shown in Figure 2.3. The RF performance of these short CPW structures is shown in Figure 2.4. Our simulations indicate a return loss (S_{11}) below -40 dB and an insertion loss (S_{21}) less than -0.02 dB from 10 MHz to 14 GHz. In the proceeding section, we introduce the design parameters for the AL-X and Kapton CPW and CBCPW flex cable designs that utilized this substrate.

[3]AlN from Stellar Industries

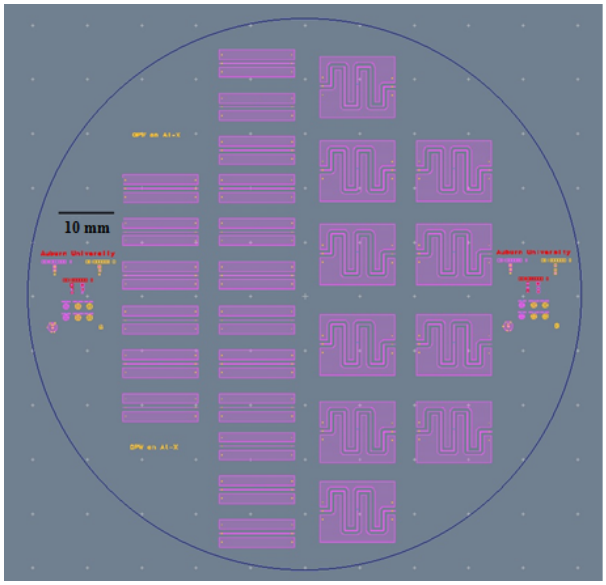

Figure 2.5: ADS layout of a CBCPW design for a 50 μm thick AL-X cable. The layout was designed to fit on a 100 mm diameter Si wafer.

2.2 AL-X flex cables

AL-X is a spin-on photoimageable dielectric that is commonly used as a packaging material [33,34]. We studied this dielectric as a possible substrate material for the fabrication of RF flex cables. We designed CBCPW flex cables based on the dielectric constant of 2.6 [30].

2.2.1 CBCPW

CBCPW transmission lines were designed on AL-X for a dielectric thickness of 50 μm. Two CBCPW structures were developed, a straight signal line design that was 11.2 mm in length and a meandered CBCPW with a total length of 42.7 mm. The gap between the signal and ground trace was 641 μm in both of these designs. The CBCPW designs included UBM pads for flip-chip bonding onto an AlN substrate. The layout of this design was for a 100 mm diameter Si wafer and is shown in Figure 2.5. The simulation model and RF performance are shown in Figure 2.6 and Figure 2.7. S_{11} simulation results show a return loss (S_{11}) below -60 dB up to 14 GHz and with an insertion loss (S_{21}) less than -0.01 dB.

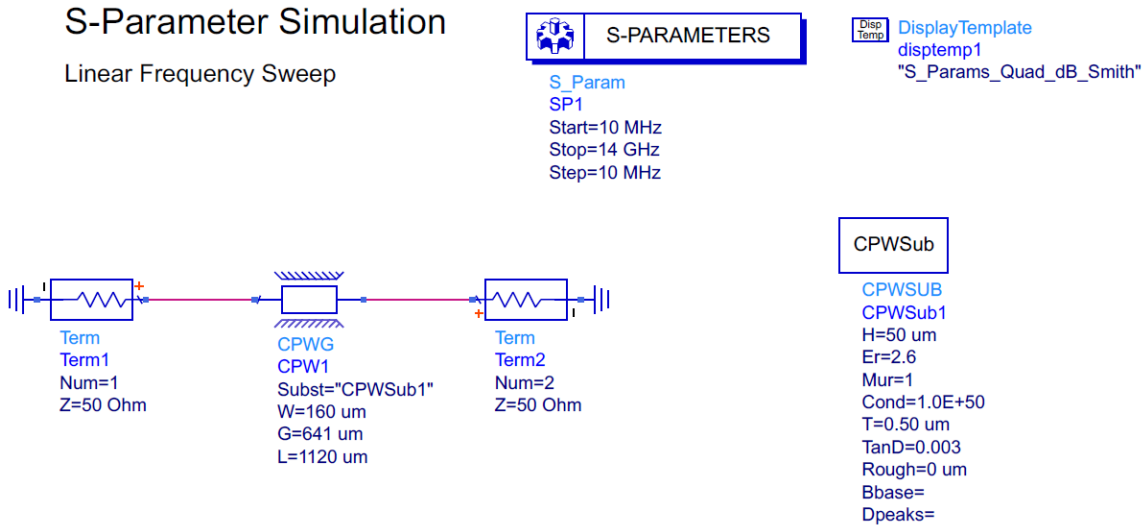

Figure 2.6: Simulation model for a 1.2 mm long CBCPW on AL-X.

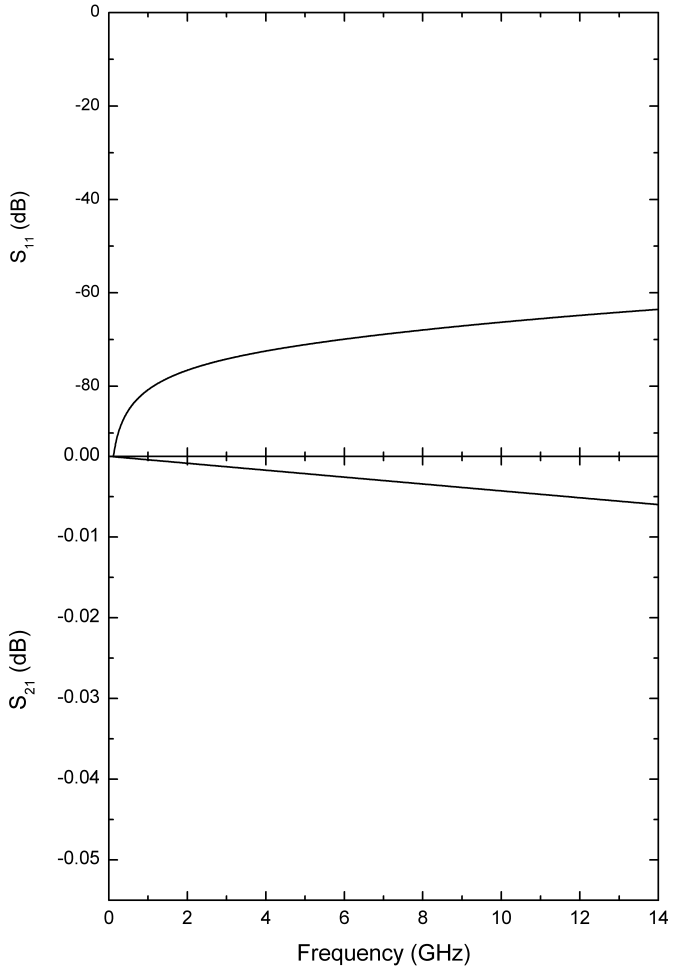

Figure 2.7: (a) S_{11} and (b) S_{21} simulations of a CBCPW on AL-X.

2.3 Kapton flex cables

E-series Kapton films were used in this work were 2 mils (50.8 μm) thick. We designed CBCPW, CPW, and microstrip transmission lines. The CPW and CBCPW designs were based on a dielectric constant of 3.4 [35]. The next iteration of designs, consisted of microstrip transmission lines. Based on the work by Bai et al., the dielectric constant of Kapton was measured as 3.2 at cryogenic temperatures in the 2-10 GHz frequency range [3]. This measured dielectric constant was then used for the design of the 5 cm and longer microstrip transmission lines.

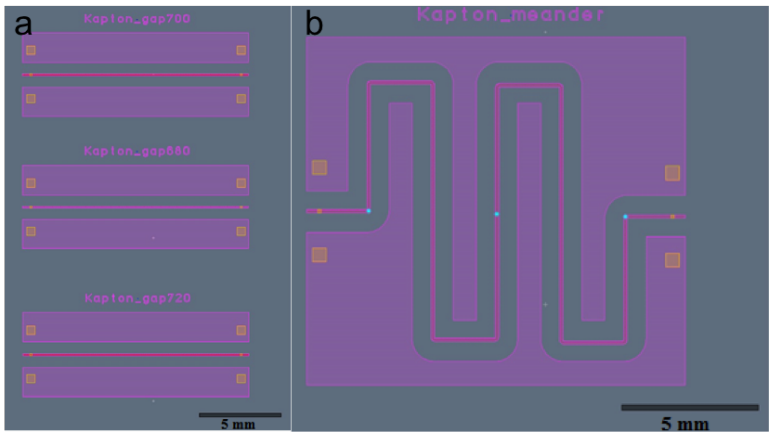

Figure 2.8: (a) ADS layout of a CBCPW for a ∼50 μm thick Kapton film with a signal line width of 121 μm and 11.2 mm in length (b) meander version of a CBCPW with a direct length of 42.6 mm.

2.3.1 CBCPW

CBCPW structures on free-standing Kapton were studied as possible transmission lines for the fabrication of flex cables. The signal line was 121 μm wide and 11.2 mm long for the straight CBCPW and 42.6 mm long for the meandered version. Both types of CBCPW designs are shown in Figure 2.8. The simulation model is shown in Figure 2.9. The RF performance of these flex cable is shown in Figure 2.10. The simulation indicateds a return loss (S_{11}) below -20 dB up to 14 GHz and an insertion loss (S_{21}) of less than -0.02 dB.

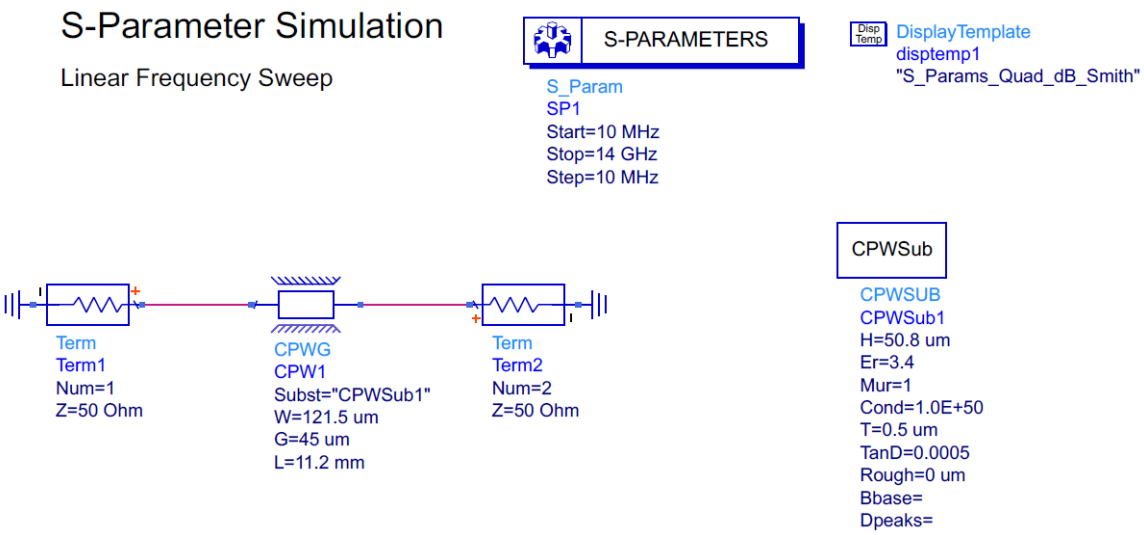

Figure 2.9: Simulation model for a 11.2 mm long CBCPW on Kapton.

2.3.2 CPW

A CPW design on Kapton without a backside ground plane was also studied as an alternative to CBCPW flex cables. This design reduced the number of processing steps. The CPW was designed with a signal line width of 1070 μm and length of 11.2 mm for the straight signal and 43.35 mm for the meandered signal version. The gap for both the CPW transmission lines was 40 μm. The layout of the two CPW designs is shown in Figure 2.11. The simulation model and RF performance is shown in Figures 2.12 and 2.13. The return loss (S_{11}) was less -30 dB with an insertion loss (S_{21}) below -0.01 dB up to 14 GHz.

2.3.3 Microstrip

Microstrip transmission lines were studied as an alternative to CPW and CBCPW flex cables. We designed a 5 cm long microstrip transmission lines with a line width of 120 μm. The mask design for a 100 mm wide Kapton film is shown in Figure 2.14. We used the mathematical relationship discussed by Pozar for a microstrip based on a thickness of 2 mils (50.8 μm) and dielectric constant of 3.2 to design these transmission lines [36]. The relationships between dielectric constant and line width are shown in Equations 2.1-2.2.

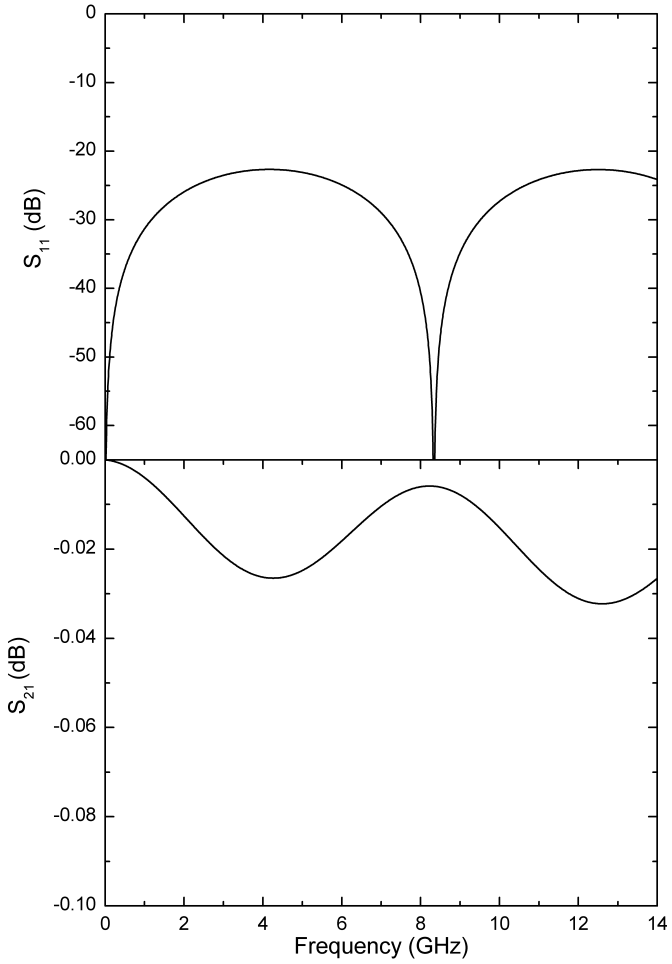

Figure 2.10: ADS simulation of (a) S_{11} and (b) S_{21} of a CBCPW on Kapton.

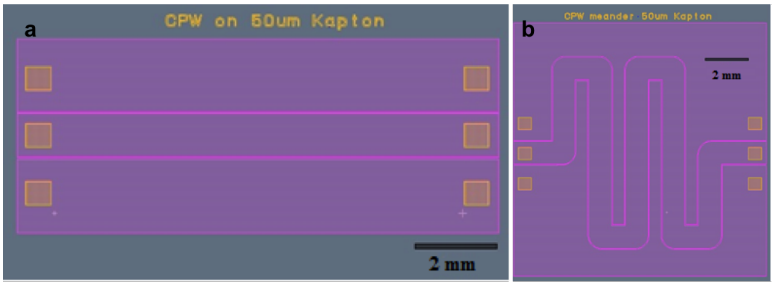

Figure 2.11: ADS layout of (a) a straight CPW on Kapton with a signal line width of 1070 μm and gap of 40 μm (b) a meandered version with a direct length of 43.6 mm.

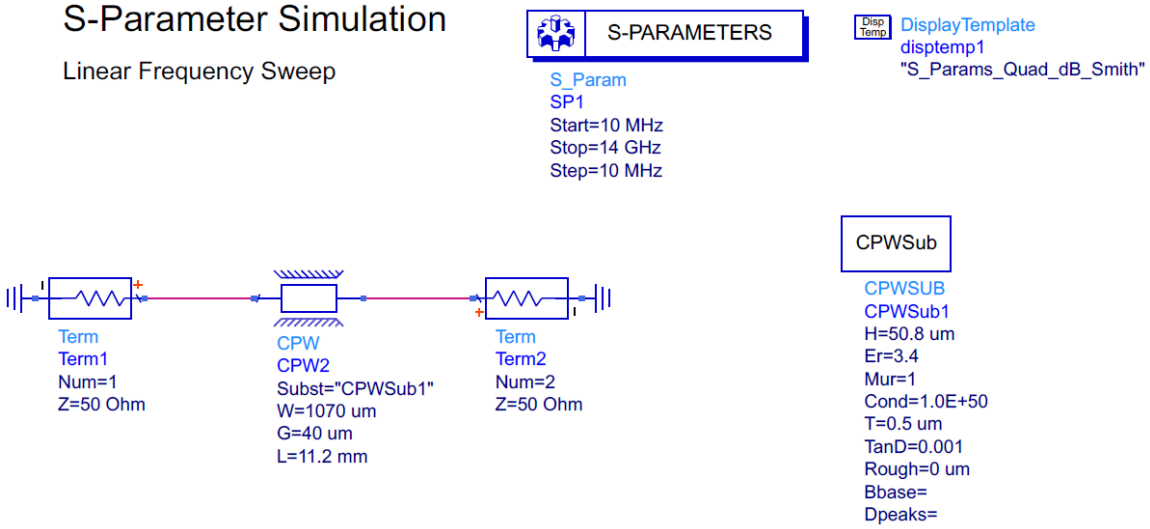

Figure 2.12: Simulation model for a 11.22 mm long CPW on Kapton.

$$W = \frac{2d}{\pi}[B - 1 - ln(2B - 1) + \frac{\epsilon_r - 1}{2\epsilon_r}\{ln(B - 1) + 0.39 - \frac{0.61}{\epsilon_r}\} \tag{2.1}$$

where B is defined as,

$$B = \frac{377\pi}{2Z_0\sqrt{\epsilon_r}} \tag{2.2}$$

We determined the line width to be 124 μm and was adjusted to 120 μm after simulation. The results of the simulation are shown in Figure 2.15. The results indicate a slight improvement in match with a width change, but can conclude that the microstrip was not sensitive to the line width.

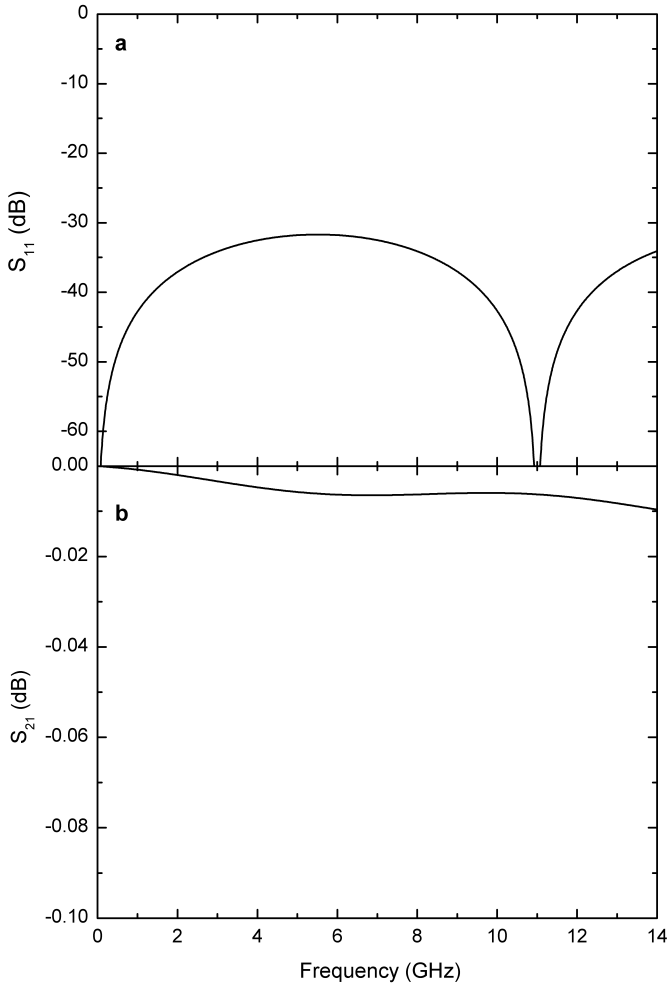

Figure 2.13: ADS simulation of (a) S_{11} and (b) S_{21} of a CPW on Kapton.

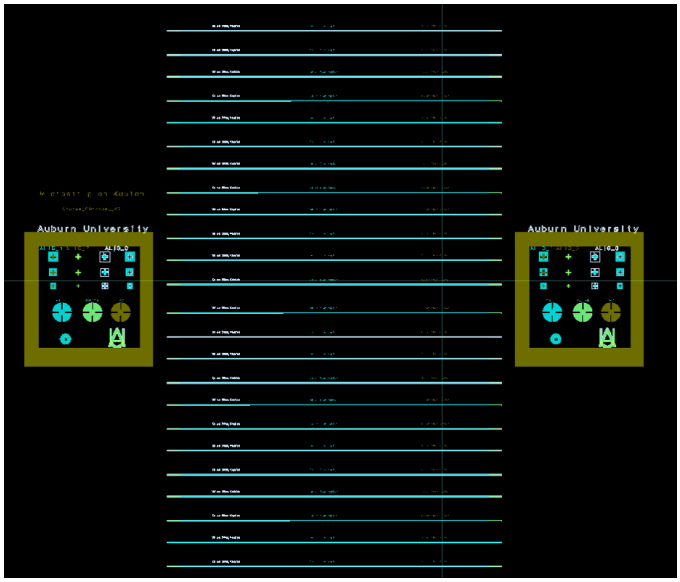

Figure 2.14: ADS layout of a microstrip designed for a ∼50 μm thick Kapton substrate.

2.4 PI-2611 polyimide flex cables

HD MicroSystems PI-2611 is a spin-on dielectric that was used to fabricate transmission lines on a 100 and 125 mm diameter Si wafers. PI-2611 polyimide has been commonly used in IC packaging [37, 38] as an interlayer dielectric. The dielectric properties of PI-2611 have also been measured at cryogenic temperatures as having a dielectric constant of 3.2 and a loss tangent as low as 8.21E-5 at 1.2 K [39].

2.4.1 A 5 cm long microstrip

The mask design for a 5 cm long microstrip on PI-2611 is shown in Figure 2.16. This design included transmission lines and resonators; the transmission lines were used to measure the T_c, I_c, as well as the RF properties of the microstrip lines. The resonators were used in a separate work to measure the dielectric properties of the PI-2611 at cryogenic temperatures. The microstrip had a line width of 46 μm with solder pads at each end that were 120 μm wide by 1200 μm long. These solder pad dimensions were designed for the Southwest Microwave edge launch connectors.

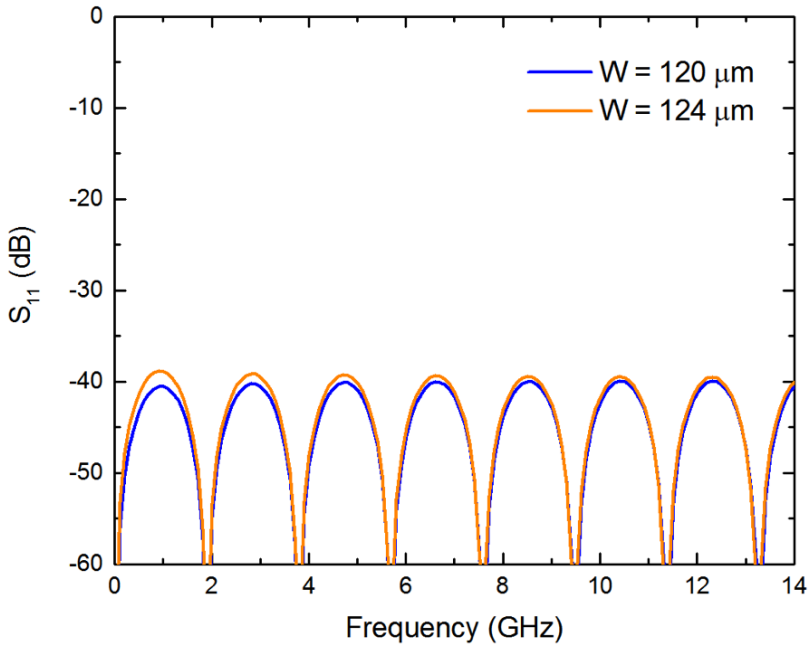

Figure 2.15: S_{11} simulation for a line width of 124 μm and after adjustment to a line width of 120 μm, after simulation.

In Figure 2.17, we demonstrate through simulation the impact the solder pads have on the RF performance of the transmission line. As we decreased the pad length from 1200 μm to 720 μm, we noticeably obtained a 5 dB improvement in match (S_{11}). A future redesign would involve reducing the pad length to reduce the impedance mismatch introduced by the pads.

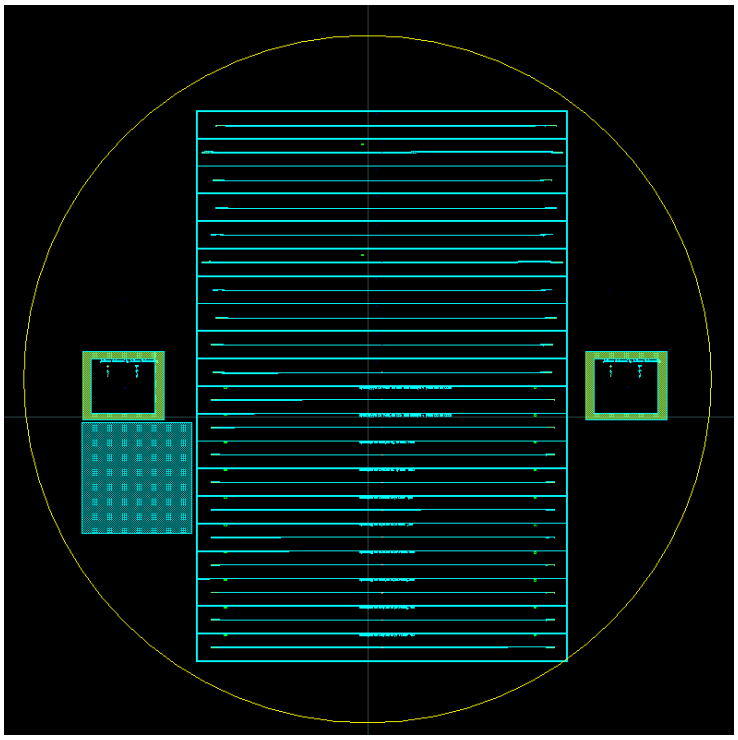

Figure 2.16: ADS layout for 5 cm long microstrip lines and resonators on PI-2611 with varying line widths. The solid square on the left of the design is a process monitoring area used for measuring the sheet resistance of the sputter deposited Nb.

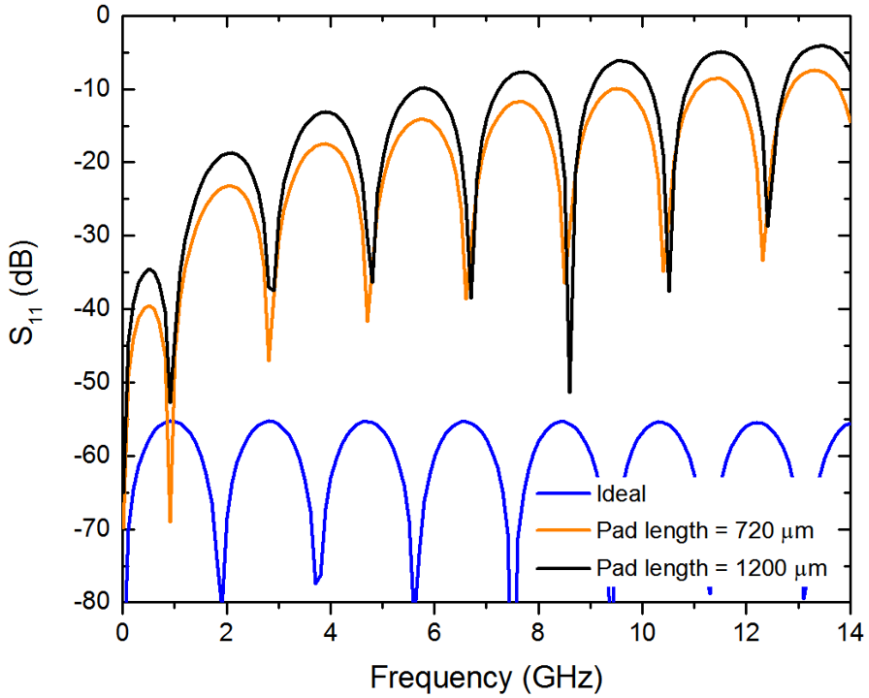

Figure 2.17: S_{11} simulations of a 5 cm long microstrip with varying solder pad lengths on PI-2611.

2.4.2 A 1 meter long microstrip

A meter long microstrip on 10 μm thick PI-2611 with a line width of $\sim$26 μm was designed to fit on a 100 mm diameter Si wafer. The layout is shown in Figure 2.18. This design included two signal lines in parallel with four edge launch connectors. The simulation model and RF performance is shown in Figures 2.18 and 2.19. From Figure 2.20b, we note we have a predicted insertion loss (S_{21}) less than $\sim$2 dB up to 14 GHz.

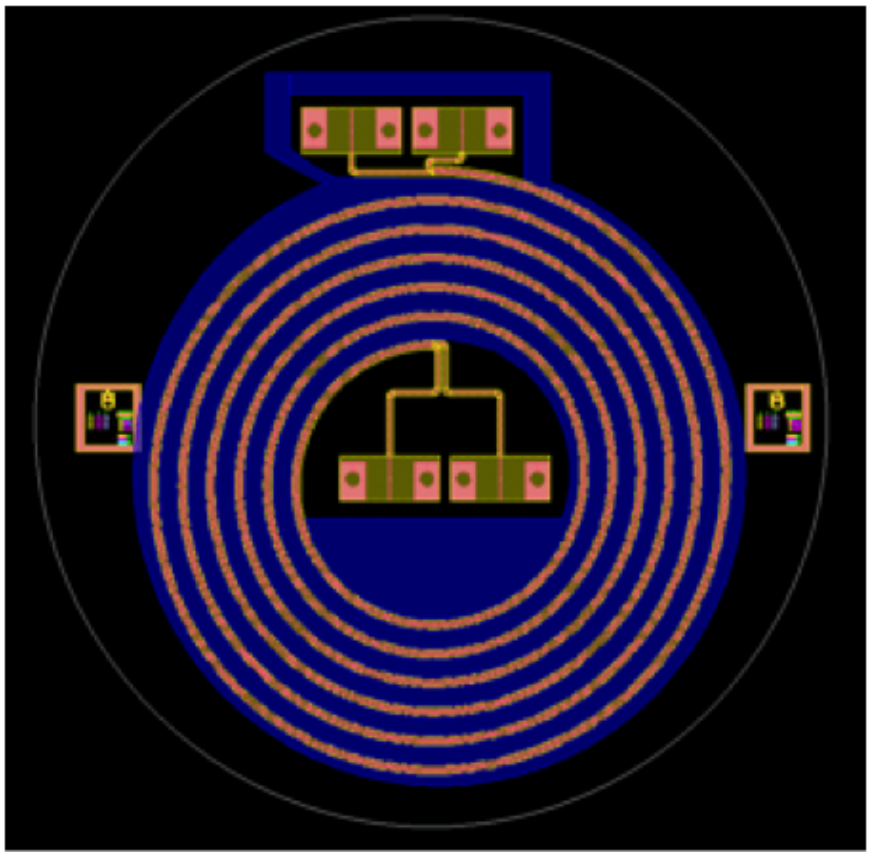

Figure 2.18: Layout for a one meter long microstrip with two signal conductors on a 100 mm diameter Si wafer.

2.4.3 A 5 cm long stripline

A 5 cm long stripline was designed based on the dielectric constant of 2.9 [31] and a dielectric thickness of 20 μm. We calculated the line width based on Pozar's derivation [36], as shown in Equation 2.3. Z_0 is the characteristic impedance, ϵ_r is the dielectric constant of

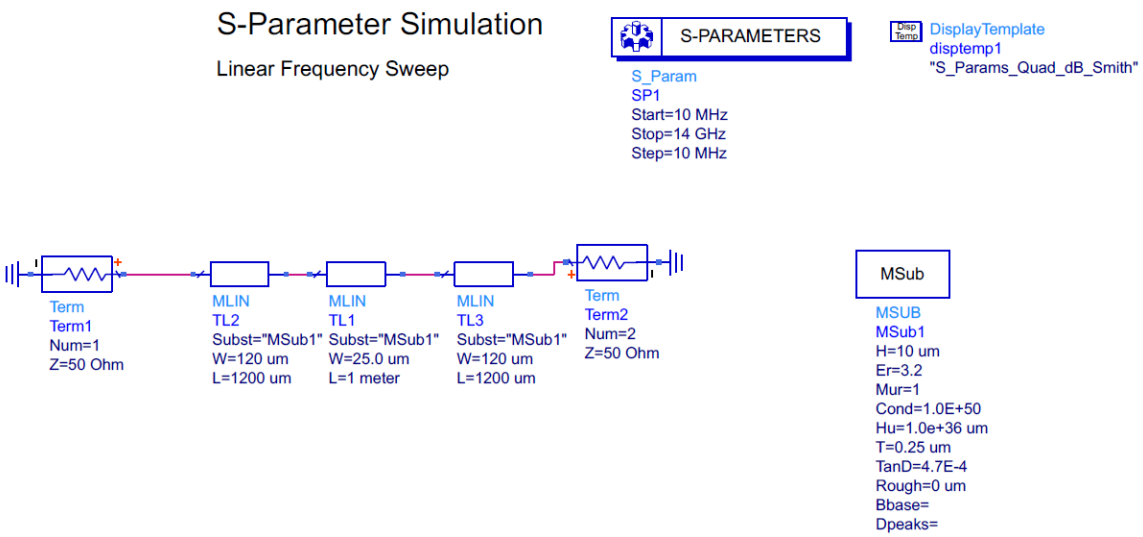

Figure 2.19: Simulation model for a one meter long microstrip on PI-2611.

the material and t is the dielectric thickness.

$$W = t \cdot (\frac{30\pi}{\sqrt{\epsilon_r} Z_0} - 0.441) \tag{2.3}$$

Based on Equation 2.3, we determined the line width to be ∼13.3 μm. After simulation, we adjusted the line width to 12 μm. The design for the 5 cm stripline is shown in Figure 2.21. A single stripline cable is shown in Figure 2.22. The stripline had a CPW launch on both ends that were used to interface to the edge launch connectors. Due to complexity of the structure, we performed a finite element model (FEM) simulation on a 2 mm long structure. The simulation results are shown in Figure 2.24. We note below -20 dB match and less than -0.01 dB in loss.

2.4.4 A 1 meter long stripline

A meter long stripline was designed to study the feasibility of fabricating multi-layer transmission lines that were significantly longer than 5 cm. The design was for a 125 mm diameter Si wafer. There are two stripline cables with each cable having two signal lines that were 12 μm wide. The design is shown in Figure 2.25. A closer view of the two signal

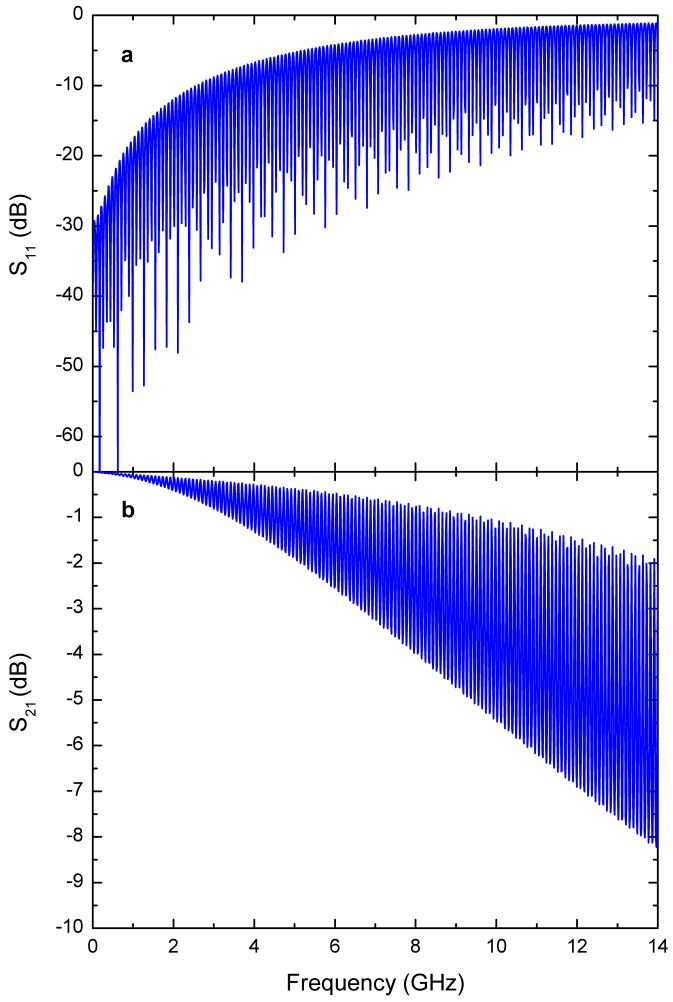

Figure 2.20: ADS simulation of (a) S_{11} and (b) S_{21} of a 1 meter long microstrip.

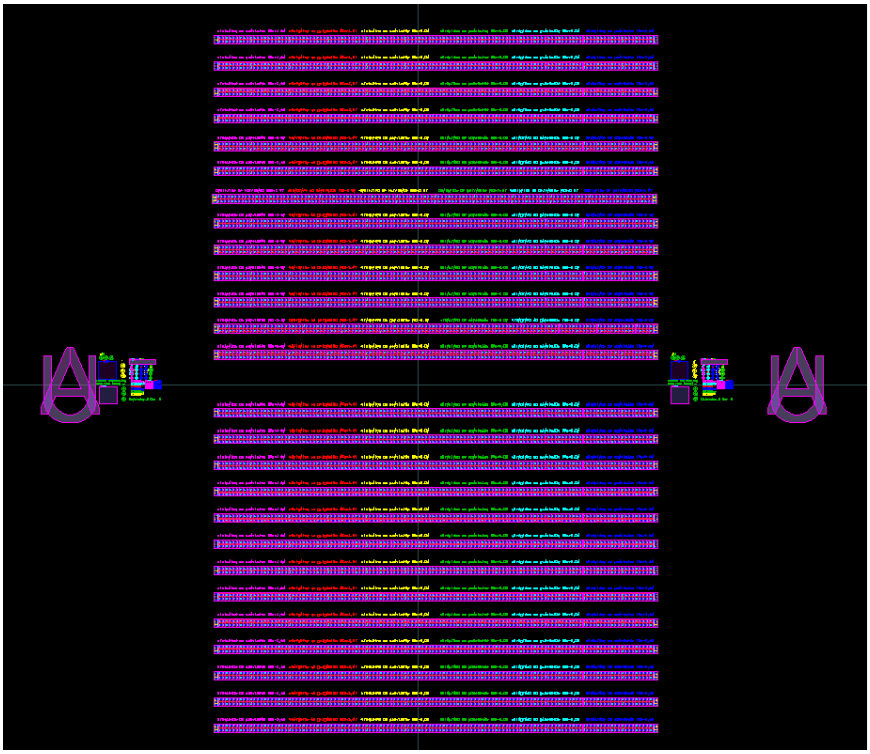

Figure 2.21: Layout for a 5 cm long stripline on a 100 mm diameter Si wafer.

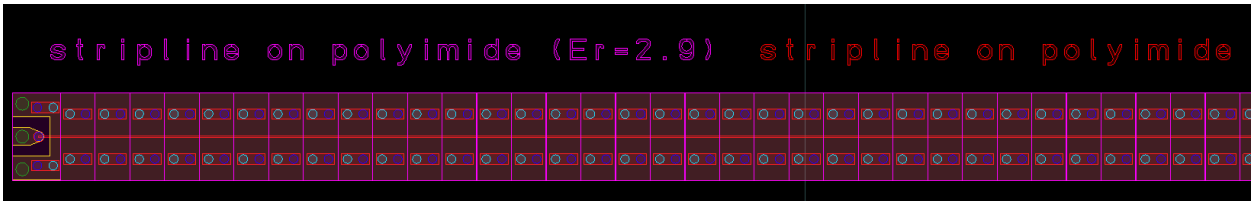

Figure 2.22: A single 5 cm long stripline is shown with vias to ground.

lines with a via fence between the two signal lines is shown in Figure 2.26. The pink narrow lines are the signal lines. The rectangular pads are catch pads for the vias.

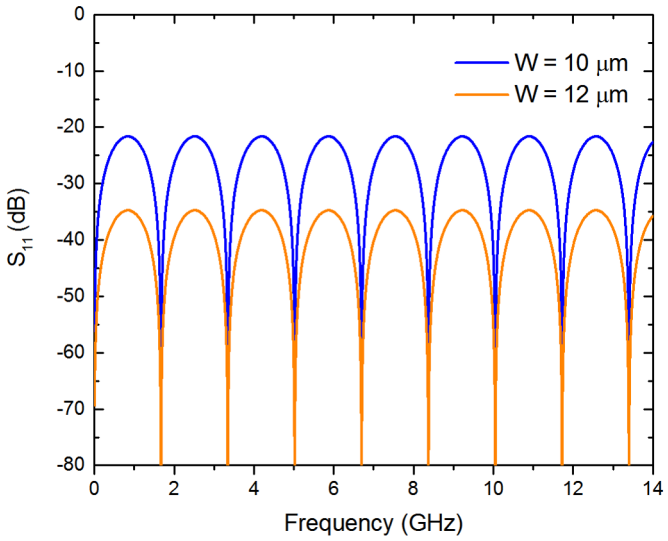

Figure 2.23: S_{11} simulation of a stripline for two different line widths, showing an improvement in match with a 12 μm line width.

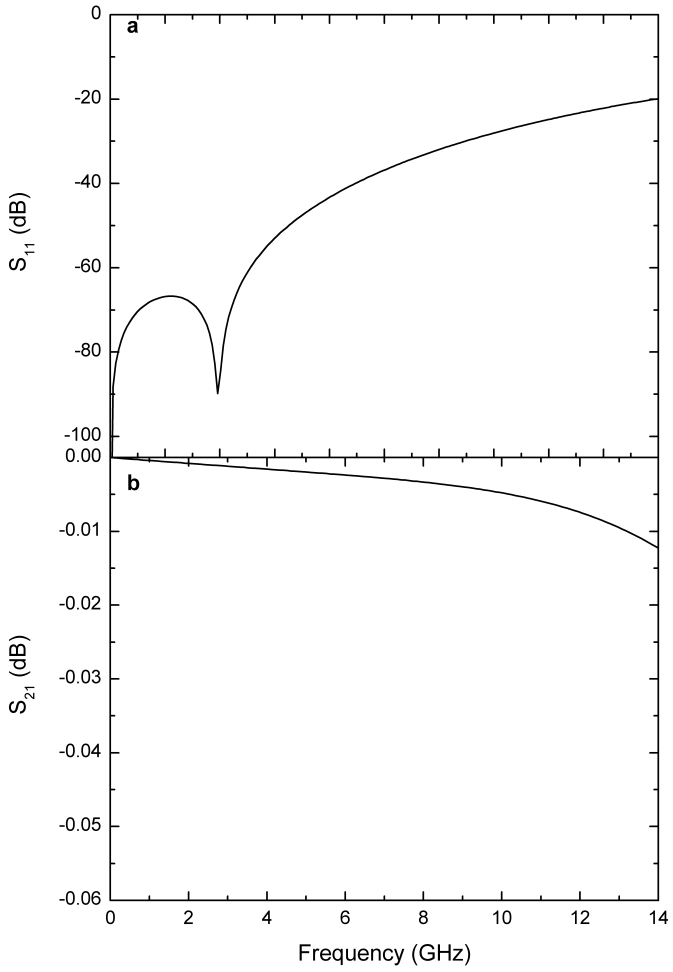

Figure 2.24: ADS FEM simulation of (a) S_{11} and (b) S_{21} of a 2 mm long stripline with a CPW launch on both ends.

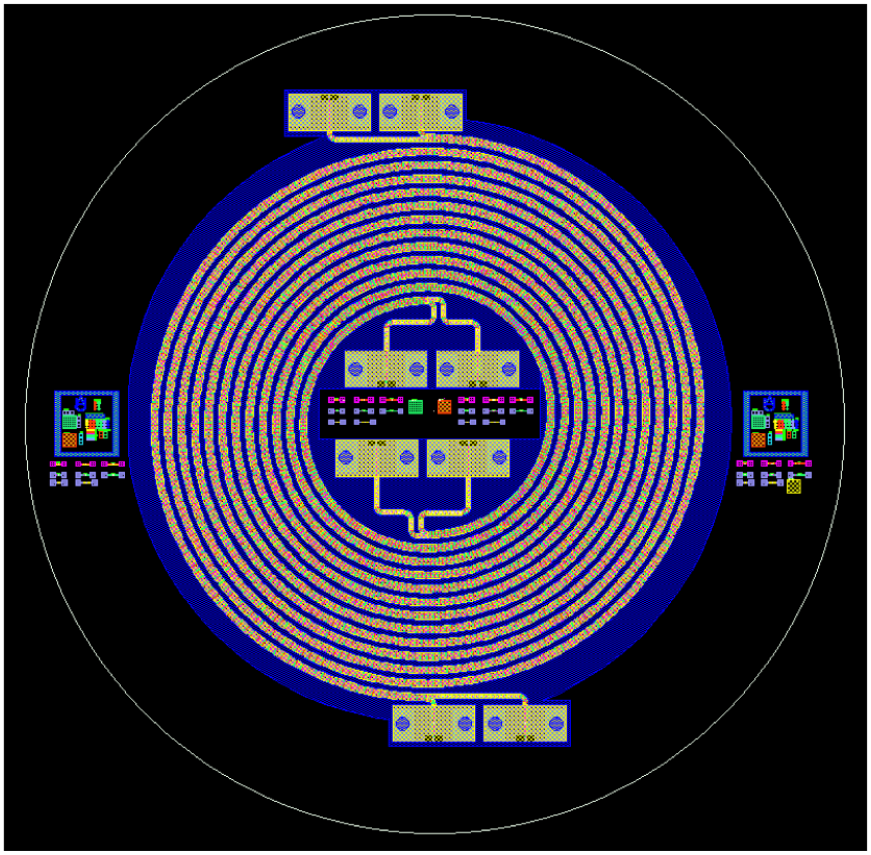

Figure 2.25: Layout of a one meter long stripline flex cable with all the layers shown. Two cables with two signal lines on each cable on a 125 mm Si diameter wafer is shown.

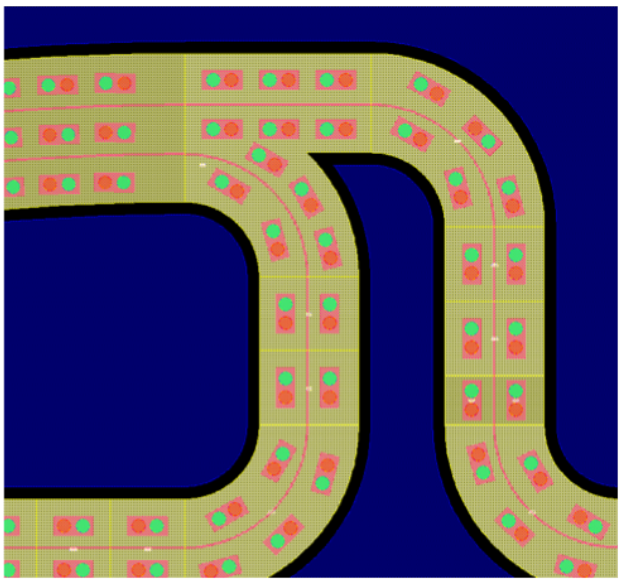

Figure 2.26: A close-up view of the two signal lines that are in parallel is shown in pink. The yellow wide regions is the patterned ground plane.

2.4.5 Meandered microstrip

Microstrip transmission lines that were one meter in length was determined to be an aggressive design that resulted in low yield. On a 100 mm diameter Si wafer, only one microstrip transmission line could be fabricated. We therefore decided to design transmission lines whose signal lines were meandered to yield lengths between 15 to 55 cm that could provide measurement results on the performance of these longer structures. The design for these meandered microstrip transmission lines and resonators is shown in Figure 2.27.

The simulation models and results for the 55, 25, and 15 cm long microstrip transmission lines are shown in Figures 2.29-2.33. The simulation model for a ∼55 cm long microstrip is shown in Figure 2.28. The simulation results are shown in Figure 2.29. We note from Figure 2.29a that our match is below -10 dB up to ∼6 GHz with intrinsic insertion loss of less than -1 dB up to 14 GHz, as shown in Figure 2.29b. The simulation model for the ∼25 cm long microstrip is shown in Figure 2.30. The model is similar to the ∼55 cm long line. We make note that the match, shown in Figure 2.31a, stays below -10 dB up to ∼6 GHz, as well. The intrinsic insertion loss stayed below -0.5 dB, as shown in Figure 2.31b. The ∼15 cm long microstrip model is shown in Figure 2.32. Similar to the other microstrip models, we show the simulation results for the return and insertion loss in Figures 2.33a and 2.33b. The intrinsic insertion loss stays below -0.25 dB up to 14 GHz. We conclude from these simulations is that even at lengths of 55 cm, the intrinsic microstrip performance is very low.

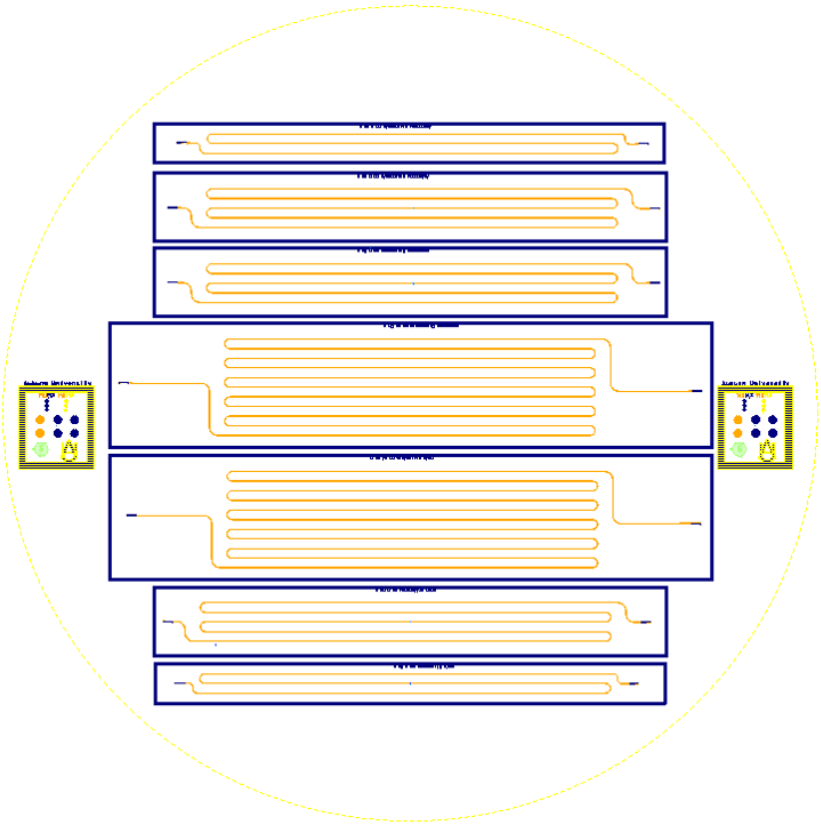

Figure 2.27: Mask design for meandered microstrip transmission lines and resonators with lengths ranging from ∼15 to 55 cm.

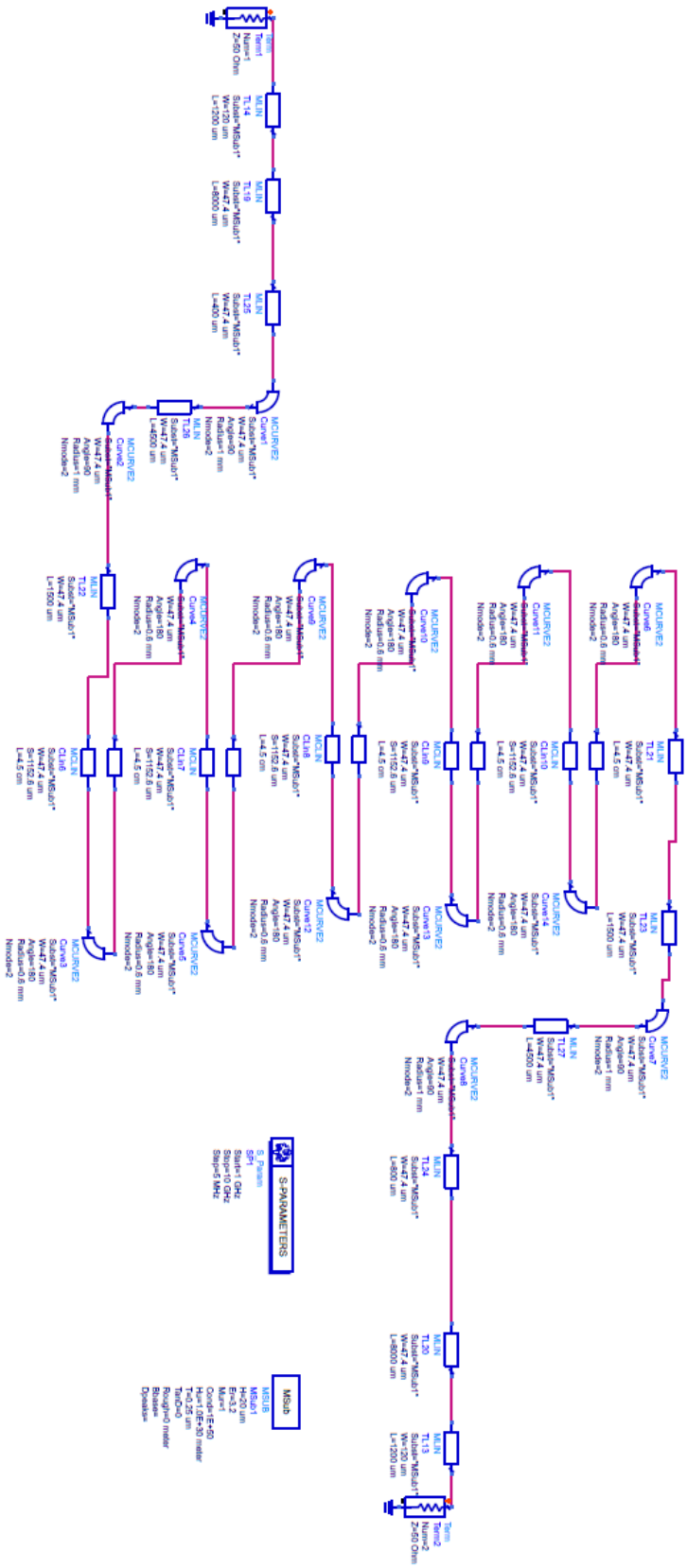

Figure 2.28: Simulation model for a ∼55 cm long microstrip.

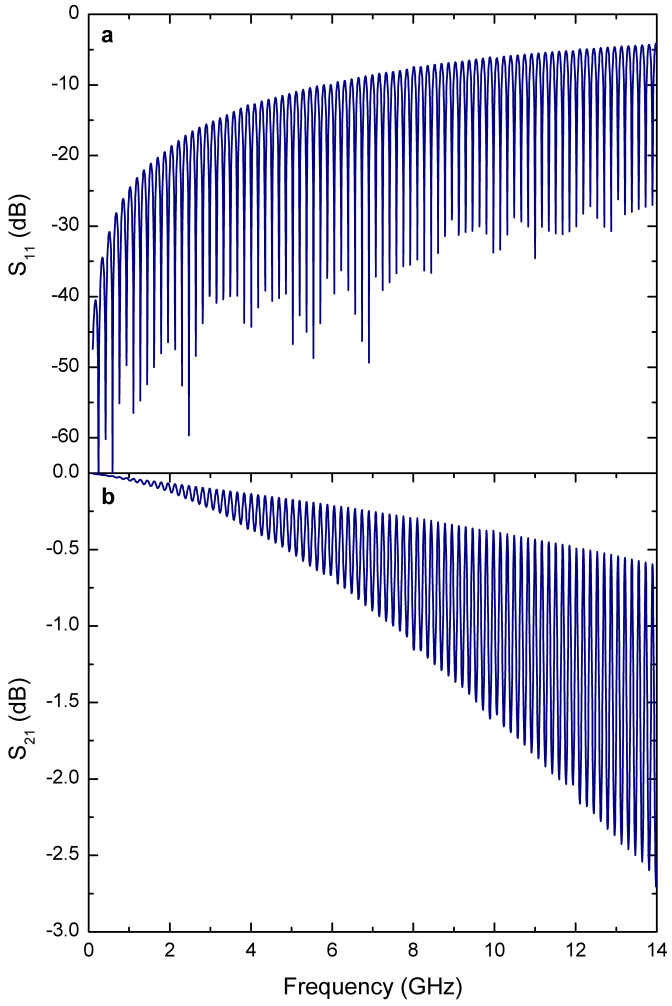

Figure 2.29: ADS simulation of (a) S_{11} and (b) S_{21} simulations of a $\sim$55 cm long microstrip design.

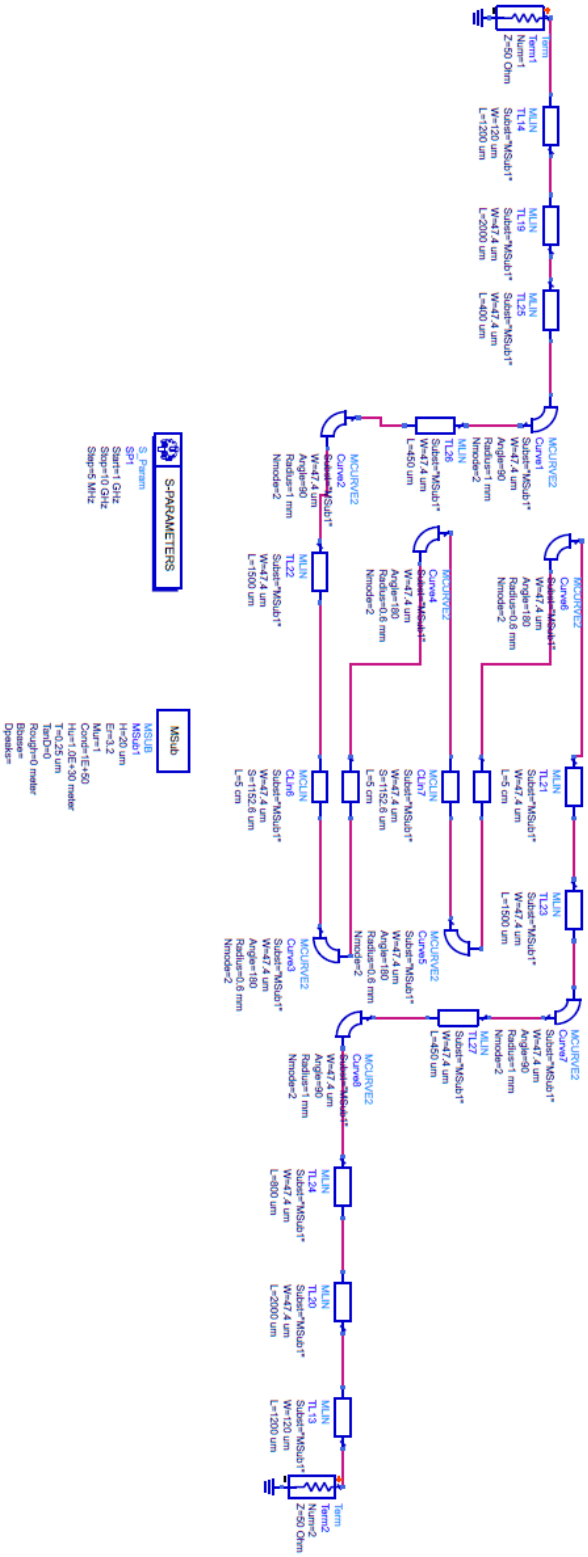

Figure 2.30: Simulation model for a ∼25 cm long microstrip.

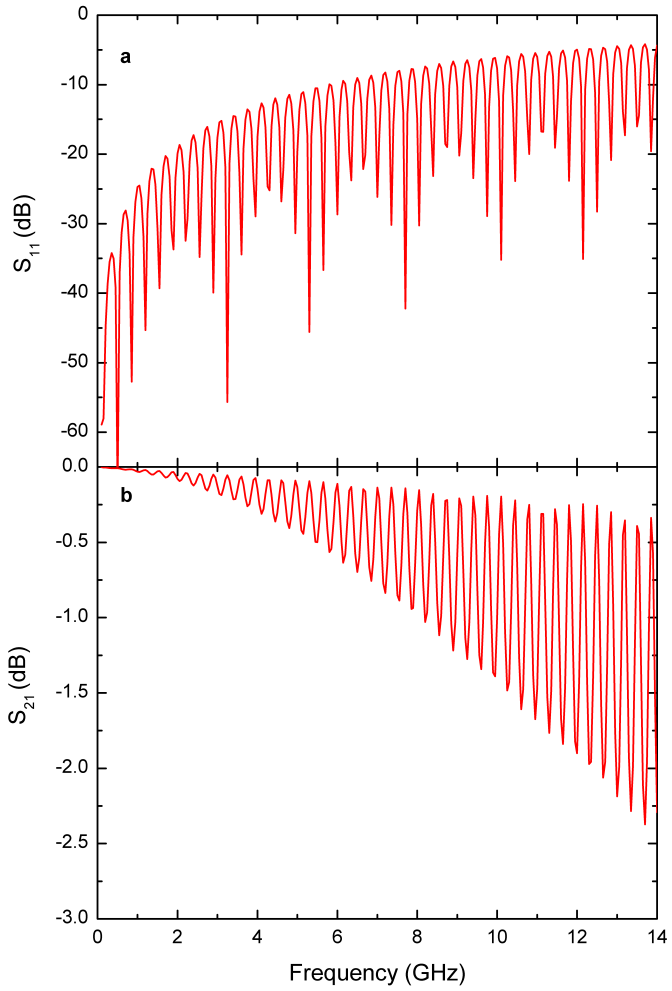

Figure 2.31: ADS simulation of (a) S_{11} and (b) S_{21} of a ∼25 cm long microstrip on PI-2611.

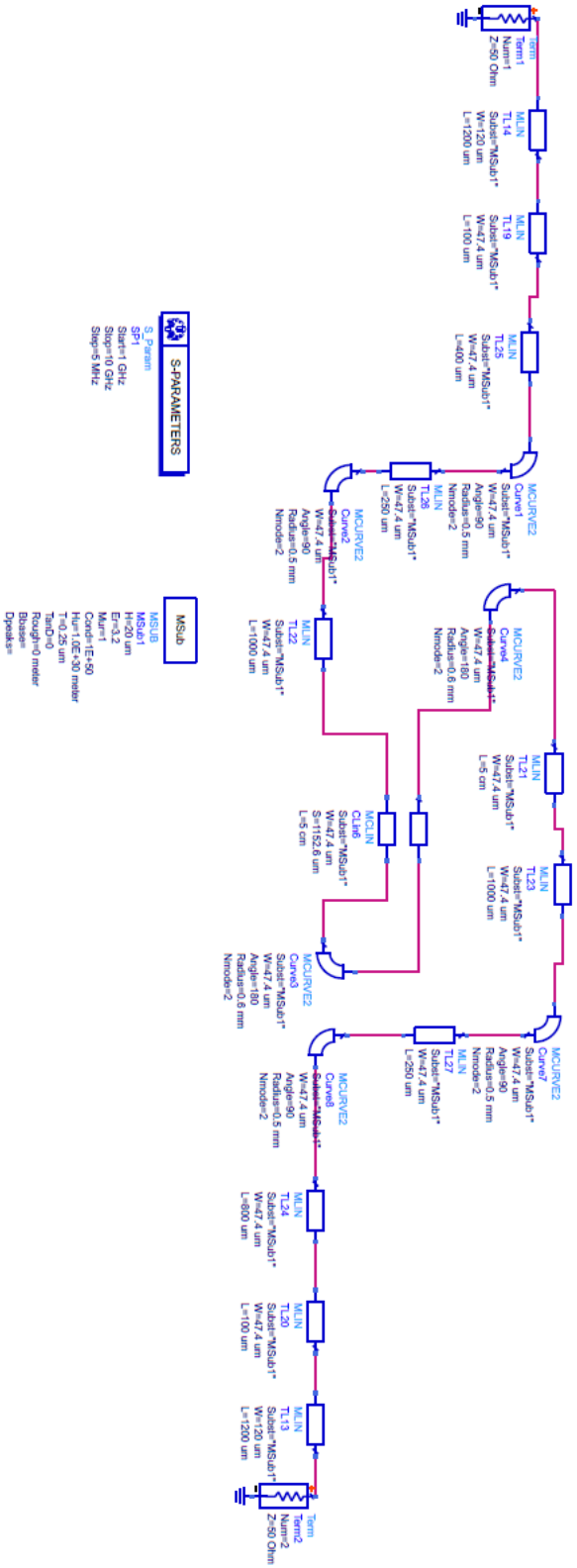

Figure 2.32: Mask design for meandered microstrip transmission lines and resonators with lengths ranging from ∼15 to 55 cm.

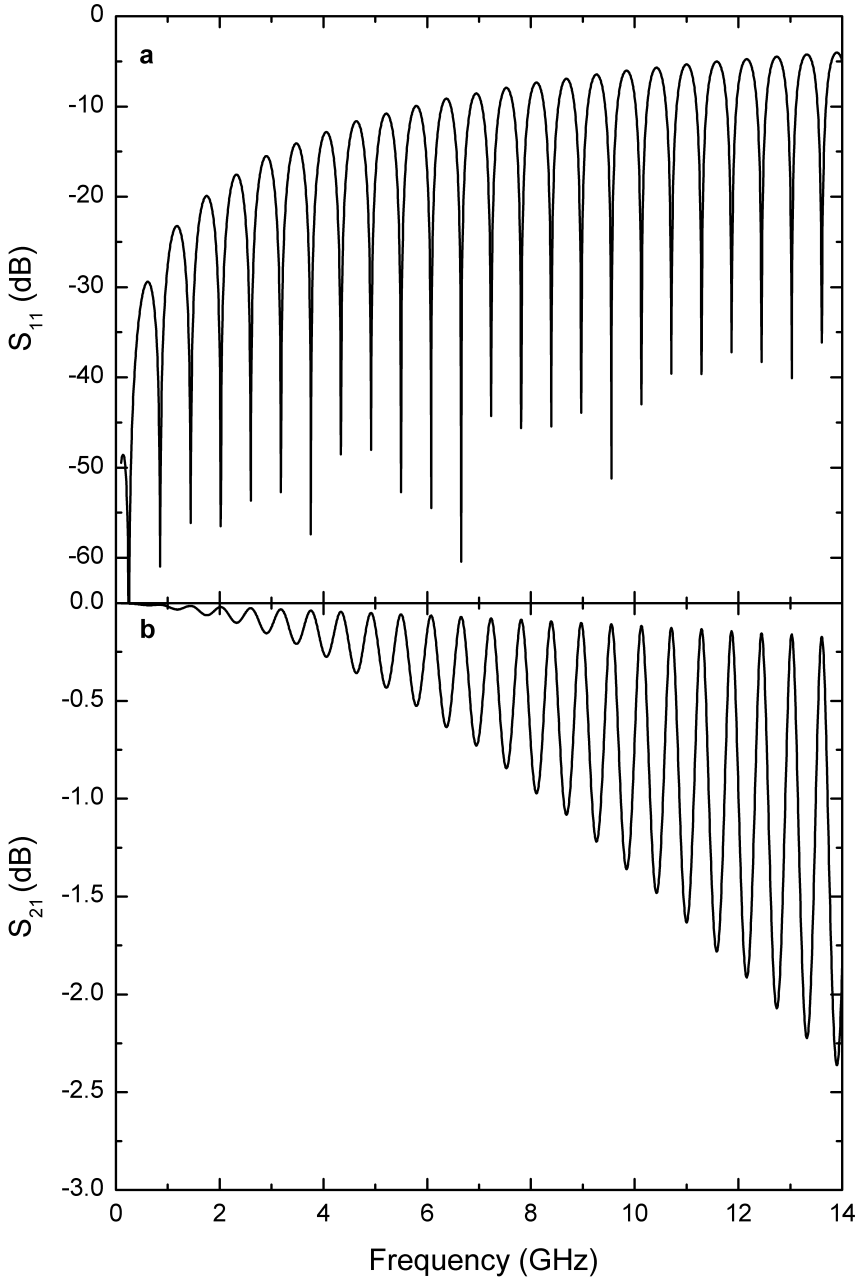

Figure 2.33: ADS simulation of (a) S_{11} and (b) S_{21} of a ∼15 cm long microstrip on PI-2611.

Chapter 3

Fabrication Processes

In this chapter we discuss the fabrication processes that were developed for AlN, Kapton, and spin-on dielectrics such as AL-X 2025 and PI-2611. We built several types of transmission lines, which included CPW, CBCPW, microstrip, embedded microstrip, and stripline. The initial prototypes consisted of CBCW and CPW on AL-X, and Kapton and were ∼4 mm in length. These samples were path-finders, they helped us define the fabrication steps that were needed, such as photoresist, and dielectric bake times, spin-on speeds for photoresist and dielectrics to achieve the desired thicknesses, etc.

This chapter begins with the discussion of AlN substrates and the fabrication steps that were undertaken. We then continue with discussion of CBCPW flex cables on AL-X and the surface treatment that was required to yield low-stress Nb metallization on AL-X. Fabrication and attachment methods that were undertaken on Kapton films are also discussed. In the next section, we discuss the fabrication process on polyimide PI-2611 for microstrip, stripline, and embedded microstrip transmission lines. We discuss in great detail the fabrication and associated challenges that were encountered. In the last section, we discuss the release process used to create free-standing RF flex cables from the spin-on dielectrics. More specifically, we discuss the anodic dissolution of Al in a salt bath. Step-by-step fabrication travelers are provided in the Appendix for all the processes discussed in this chapter.

3.1 AlN

The as-received AlN substrates were oxidized at 800 °C for 30 minutes in an oxygen ambient furnace. The substrates were then baked in a vacuum oven at 120 °C and primed

with hexamethyldisilizane (HMDS)[1] for 10 minutes. A positive-tone photoresist was then applied and exposed with a CPW pattern. The substrates where then loaded into a metal deposition chamber for sputtering. A Nb film was then sputtered at 1 kW with a rate of ∼0.14 nm/s to yield a 250 nm thick film. These samples were then patterned with a design that overlaid UBM onto designed points on the CPW traces. An EBPVD process was used to deposit the UBM consisting of Ti/Cu/Au with a thickness of 500/2000/500 Å, respectively. The substrates were then mounted onto a Si handle wafer with the backside exposed (signal side down). Nb was then sputter deposited onto the backside with the same parameters as the signal-side metallization. A CBCPW on an AlN substrate for flip-chip bonding an individual flex cable is shown in Figure 3.1.

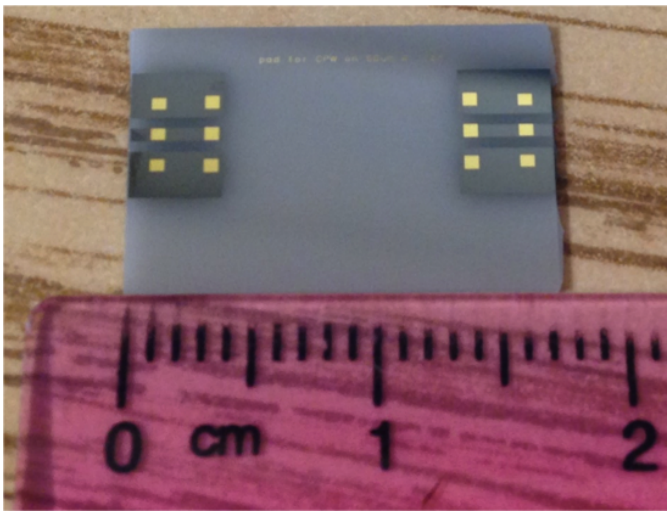

Figure 3.1: AlN substrate with CPW patterns and UBM metallization for flip-chip attachment of an individual flex cable.

3.2 AL-X CBCPW

As-received Si handle wafers were deposited with Cr/Al by EBPVD to a thickness of 500 Å/2000 Å, respectively. The handle wafers were then baked in vacuum oven at 110 °C for 30 minutes and an adhesion promoter (AP903) was applied and baked at 100 °C for 90 seconds. AL-X was then spin-coated to a thickness of 50 μm and cured in a nitrogen ambient oven

[1] http://www.imicromaterials.com/technical/hmds

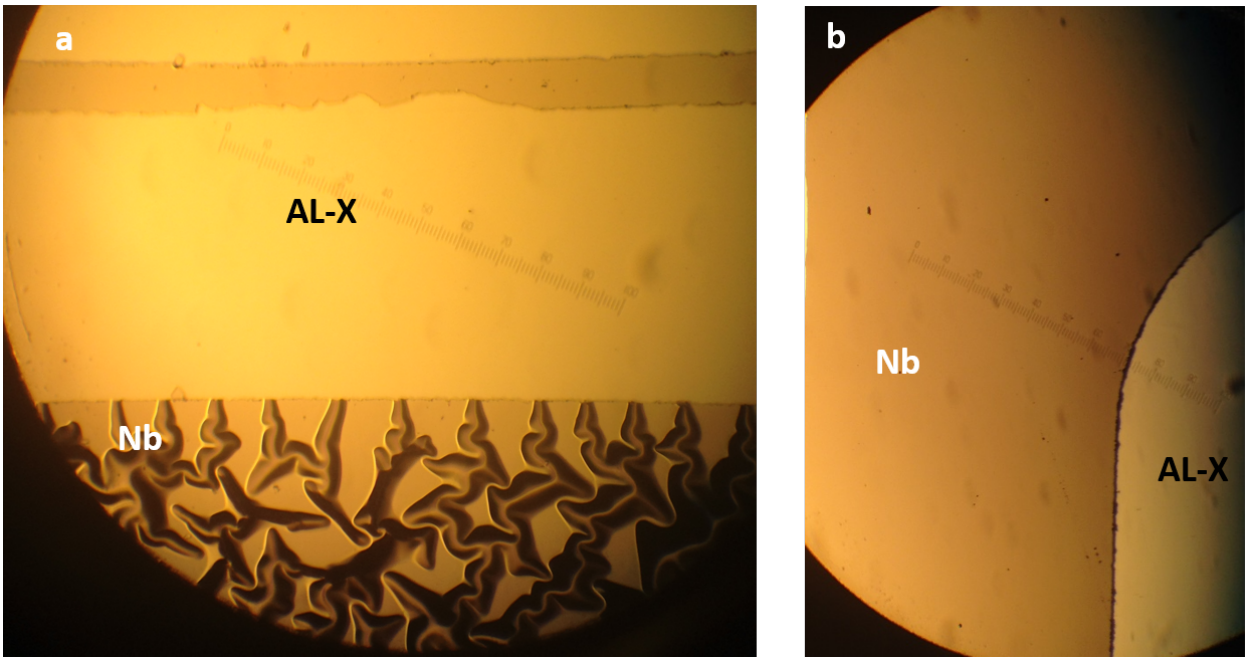

Figure 3.2: Nb on AL-X (a) without ion milling (b) with 2 minutes of ion milling treatment.

following the guidelines of the manufacturer [30]. Positive-tone photoresist was then applied and exposed with CPW traces. These substrates were then loaded into a metal deposition system for Nb sputtering. A 2 minute ion milling with Ar at 1 kV was performed prior to the sputter deposition. We experimentally determined the ion milling step was necessary to avoid buckling of the Nb film on this dielectric. Representative microscopy images of the Nb film on AL-X are shown in Figure 3.2. We note that the as-deposited Nb without ion milling (Figure 3.2a) appeared wrinkled, while the ion milling treatment resulted in a smoother Nb film, as shown in Figure 3.2b.

A CBCPW flex cable on AL-X after removal from the Si handle wafer is shown in Figure 3.3a. A representative sample mounted on the AlN is shown in Figure 3.3b. We note that after removing the dielectric from the substrate, it became very brittle. We therefore did not use this material after these initial prototypes were made.

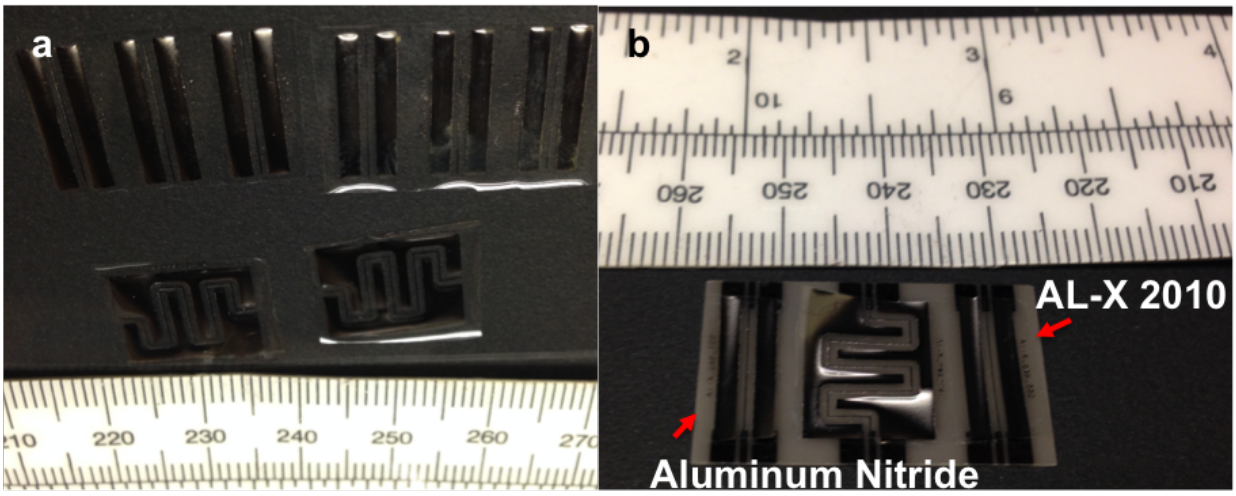

Figure 3.3: (a) CBCPW on a 30 μm thick AL-X (b) a representative AL-X flex sample mounted onto a AlN substrate.

3.3 Free-standing Kapton

E-series Kapton films received from the vendor were inspected and cut to fit onto Si handle wafers. The surface of the Kapton was cleaned in methanol and rinsed in DI water to remove surface contamination.

3.3.1 CPW and CBCPW

Kapton films were baked in an oven at 110 °C for 30 minutes and primed with HMDS while still warm. The Kapton films were then mounted onto Si handle wafers and coated with positive tone photoresist and baked at 110 °C on a hot plate. The Kapton samples were then exposed and developed with either a CPW or CBCPW pattern. Great care was then undertaken to dry the film, to avoid cracking the photoresist on the Kapton. The samples were then loaded into a metal deposition system and sputter deposited with Nb at 1 kW at a rate of ∼0.14 nm/s to yield a 250 nm thick film. A lift-off process was performed and the photolithography process was repeated to define UBM pads on the Nb traces. These samples were loaded into the metal deposition chamber and EBPVD was used to deposit a

Ti/Cu/Au with a thickness of 500/2000/500 Å, respectively. Following a lift-off step, the CPW samples were cut into individual flex cables; for the CBCPW Kapton samples, they were mounted onto a new Si handle wafer with the backside exposed and sputtered with the same Nb deposition parameters as the signal metallization. A Kapton film with CPW patterns before UBM deposition is shown in Figure 3.4.

A CPW sample with Nb metallization and In bumps on Kapton is shown in Figure 3.5a. An In solder paste was applied to the UBM pads with a syringe and a heat gun was used to reflow the In. Samples were then flip-chip bonded to AlN substrate that had corresponding UBM pads using an FC150 flip-chip bonder. A CPW sample flip-chip bonded onto an AlN substrate is shown in Figure 3.5b. Unfortunately, controlling the solder volume through this method proved to be difficult. Samples would routinely short due to excess solder after the flip-bonding step. If this method were to be pursued further, indium plating would have been a potential alternative [40].

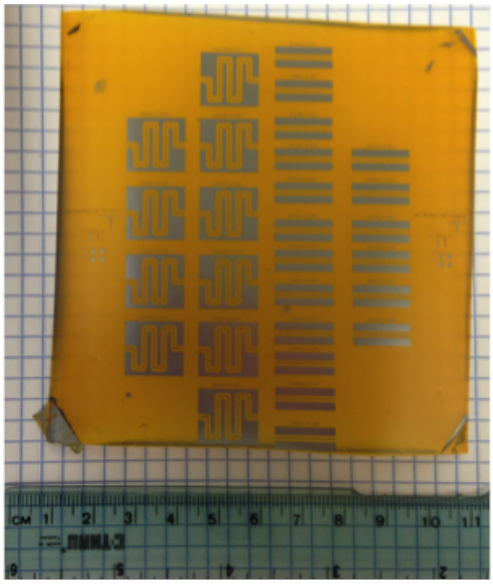

Figure 3.4: CPW with topside Nb metallization on free-standing Kapton before UBM deposition.

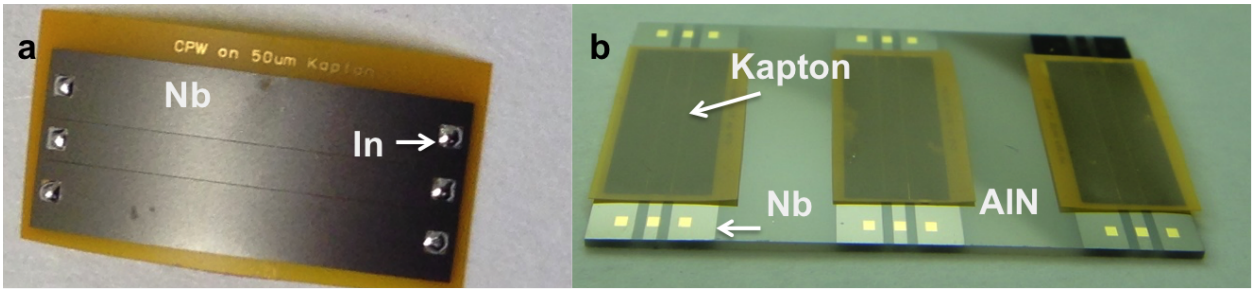

Figure 3.5: (a) CPW on a Kapton film with In bumps (b) a CPW flip-chip bonded onto a AlN substrate.

3.3.2 Microstrip

Kapton samples were optically inspected for surface defects (e.g. scratches) and those with a minimal amount of imperfections were cut to fit onto 100 mm diameter Si wafers. The Kapton films were then cleaned in methanol and DI water to remove any surface contamination. These Kapton films were then mounted onto a Si handle wafers with an adhesive tape and baked in a vacuum oven at 110 °C for 20 minutes. These samples were then primed with HMDS for 10 minutes and coated with positive-tone photoresist and baked on a hot plate at 110 °C for 2 minutes. These samples were then patterned with the microstrip signal design and loaded into the metal deposition chamber (as shown in Figures 3.6a and 3.6b) and sputter deposited with Nb. A typical lift-off step was performed on the Kapton films (Figure 3.6c) to complete the signal metallization. A Kapton film with signal and UBM metallization removed from the Si Handle wafer is shown in Figure 3.7.

The Kapton samples underwent a second lithography step to define UBM pads on the signal lines following the same lithography procedure outlined previously. After patterning, the samples were transferred to the metal deposition system for deposition of a Ti/Cu solder base (UBM) consisting of a thickness of 500 Å and 5000 Å, respectively (Figure 3.6d). After the UBM deposition, a typical lift-off process was performed leaving behind a solder base on both ends of the transmission line (Figure 3.6e).

The Kapton samples were then mounted with the signal side down onto a polished Si handle wafer for backside metallizaton. The ground plane was then deposited with the same parameters as the signal side metallization (shown in Figure 3.6f). Individual microstrip samples where then cut from the Kapton film.

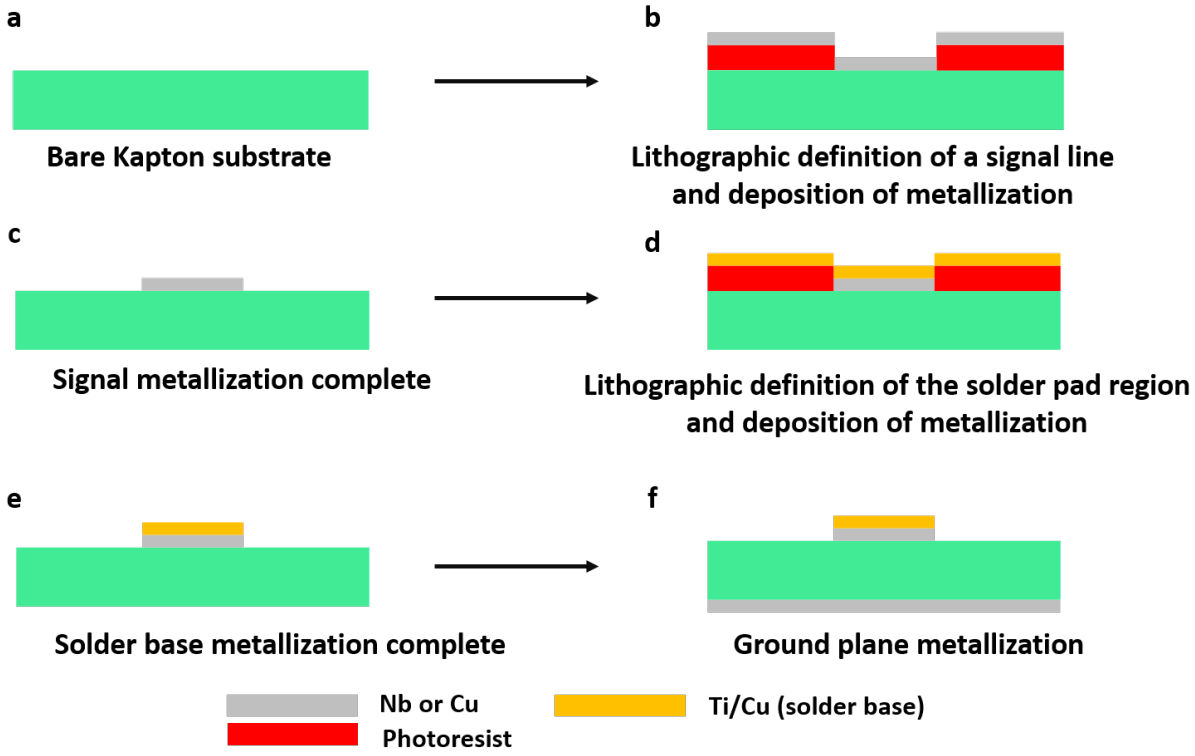

Figure 3.6: Microstrip fabrication process on Kapton (a) bare Kapton film (b) photoresist was applied and patterned with microstrip design and metal is deposited (c) a lift-off process is performed (d) photoresist is applied and solder based is defined on the signal trace (e) lift-off process is repeated to leave the solder base on the signal line and (f) the ground plane of the microstrip is deposited.

3.4 Polyimide PI-2611

Several transmission lines were fabricated using HD MicroSystems PI-2611, a spin-on dielectric. We fabricated stripline and microstrip flex cables of varying lengths. What follows in this section is a discussion of the processing steps required to fabricate each type

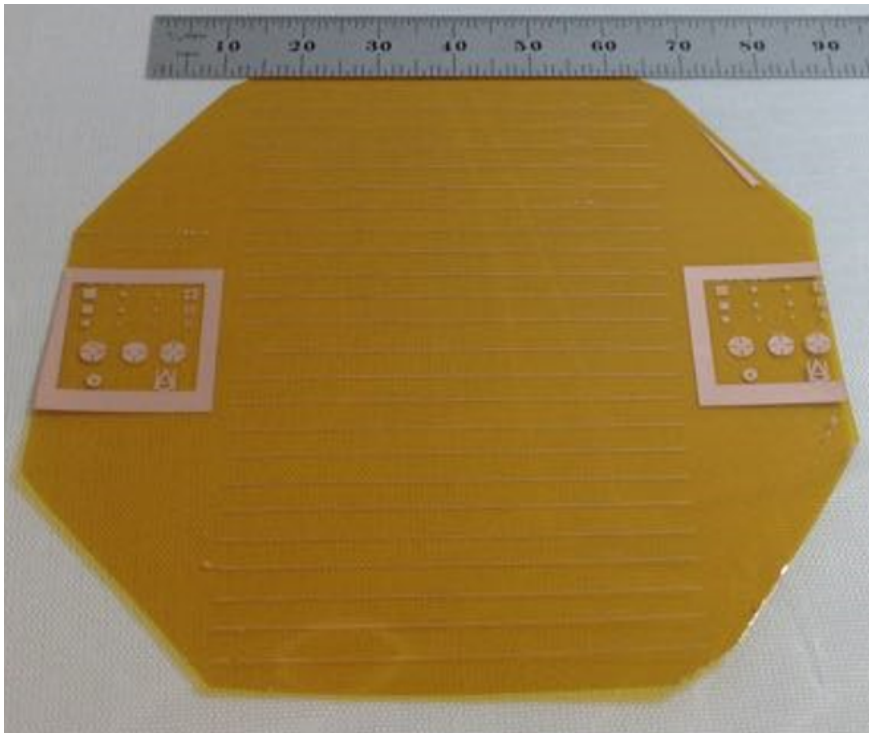

Figure 3.7: Microstrip transmission lines on E-series Kapton before the ground plane metallization.

of transmission line on PI-2611. We begin our discussion with stripline, which is the most complex and ends with embedded microstrip transmission lines that required fewer processing steps.

3.4.1 Stripline

The stripline fabrication process began with deposition of a Cr/Al release layer with a thickness of 500 Å/2000 Å, respectively on a 125 mm diameter Si wafers (Figure 3.8a). Wafers were then transferred into a metal deposition chamber and the surface was ion milled for 2 minutes at 1 kV to remove the surface oxidation from the Al. After the ion milling process, the wafers were sputter deposited with Nb at 1 kW with a rate of ∼0.14 nm/s to yield a 250 nm thick film (Figure 3.8b). This solid Nb film was the ground plane (M0) for the stripline. Wafers were then transferred to an oven and baked at 110 °C for 20 minutes. Wafers were then coated with VM652 adhesion promoter and baked at 120 °C for 1 minute.

Polyimide was then spin-coated to a thickness of ∼10 μm and baked on a hot plate for 5 minutes at 120 °C. The wafers were then transferred to an nitrogen ambient oven and cured at 350 °C (Figure 3.8c) based on the manufacturers data sheet [31].

After the dielectric was cured, we etched vias in the dielectric to make contact to the underlying ground plane, following the process outlined by Mimoun et al. [41]. An Al hard mask was required to define the via regions in the dielectric. Therefore, the wafers were baked in vacuum oven at 110 °C for 20 minutes. While the wafers were still warm, they were loaded into the metal deposition system and ion milled for 2 minutes at 1 kV followed by an Al deposition by EBPVD at a rate of 2 Å/s to yield a 2000 Å thick film (Figure 3.8d). The Al was then patterned with a positive-tone photoresist with the via pattern and wet etched with aluminum etch 80-15-3-2 from J.T. Baker (Figure 3.8e). Wafers where then loaded into a Branson IPC asher and exposed to an oxygen plasma at a power of 1 kW for 60 minutes, which etched ∼3 μm into the polyimide. The wafers were then transferred to an STS advanced oxide etcher (AOE) to be etched anisotropically. The etch process concluded when contact to the ground plane was made (Figure 3.8f). After the etch process was complete, we rinsed the wafers in acetone, methanol, followed by a DI water rinse to remove any residual photoresist and solvent (Figure 3.9g). Wafers were then exposed to a short 30 second plasma at 150 W.

Wafers were then transferred into a vacuum oven and baked at 110 °C for 30 minutes and primed with HMDS. The signal and via metallization layer was then patterned (Figure 3.9h). Wafers were loaded into the metal deposition system and sputtered with Nb with the same parameters as the ground plane (Figure 3.9i). We then performed a lift-off process, which defined the signal line (M1) and contact to the underlying ground plane through the via (Via01), as shown in Figure 3.9j.

A second, encapsulating dielectric layer was then spun-on to a thickness of 10 μm and cured at 350 °C (Figure 3.9k). The via etch process was then repeated as the first via layer. Wafers were baked at 110 °C for 20 minutes in a vacuum oven. While the wafers were still

warm, they were loaded into the metal deposition system and ion milled for 2 minutes at 1 kV followed by an Al deposition by EBPVD at a rate of 2 Å/s to yield a 2000 Å thick film (Figure 3.9l). The Al was then patterned with a positive-tone photoresist with the second via pattern (Via12) and wet etched in aluminum etchant (Figure 3.9m). Wafers were then transferred to a Branson IPC asher and exposed to an oxygen plasma at 1 kW for 60 minutes, which etched $\sim$3 μm into the polyimide. Wafers were then transferred to an STS avanced oxide etch to be etched aniostropically. The etch process was stopped when contact was made to the ground plane (Figure 3.10n). After the etch process was complete, we rinsed the wafers in acetone, methanol, followed by a DI water rinse to remove any residual photoresist and solvent, as shown in Figure 3.10o.

After the dielectric etch steps were completed, the top ground plane (M2) following the same lithography steps previously discussed. We deposited the top ground plane with the same deposition parameters as before, shown in Figures 3.10p and 3.10q. We then performed a lift-off process to complete the Nb metallization process (Figure 3.11r). Wafers were then transferred to a dehydration bake oven at 110 °C and primed with HMDS and coated with positive-tone photoresist for the next lithography step. Wafers were then patterned with the solder pad mask (Figure 3.11s) and loaded into the metal deposition system. The solder pad metallization was deposited by EBPVD and consisted of a Ti/Cu layer with a thickness of 500 Å/5000 Å, respectively (Figure 3.11t). A lift-off process was performed and then samples were released from the wafer in a salt bath (Figures 3.11u-3.11v). A 5 cm long flex cable and a one meter long flex cable after release from the Si handle wafer are shown in Figure 3.12 and in Figure 3.13.

SEM images of the stripline before being released from the Si handle were taken to study the via profiles. In Figure 3.14, we note Via01 with a dielectric encassing the opening and in Figure 3.15, we can see the hollow via (Via12). In Figure 3.16, the launch structure without UBM is shown.

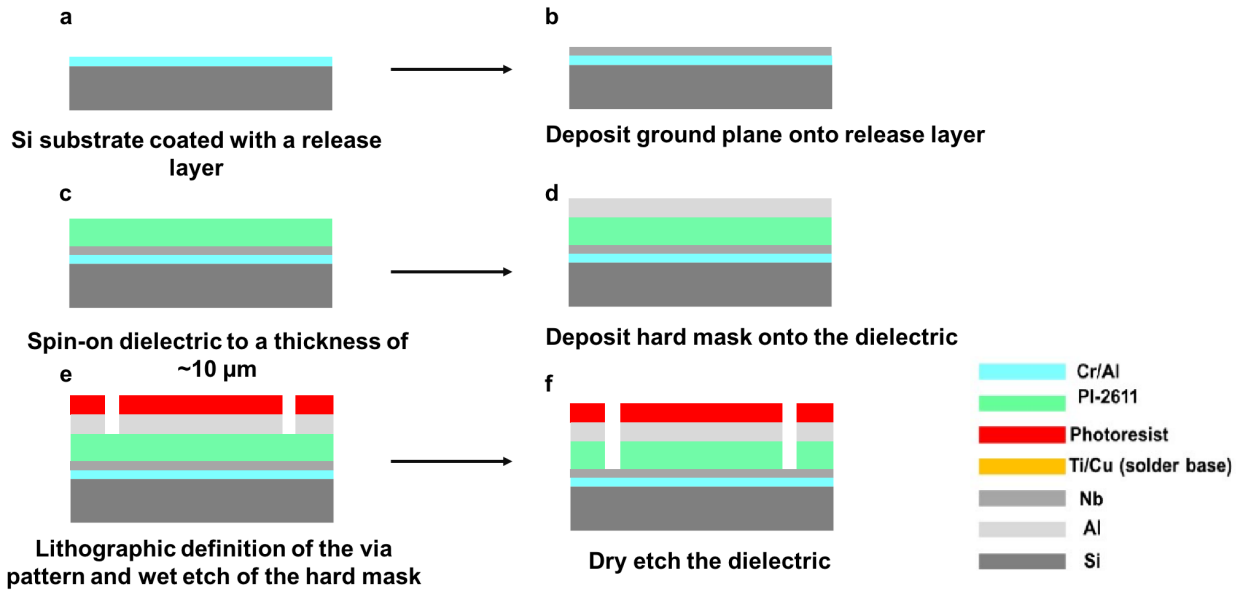

Figure 3.8: Stripline fabrication process flow (a) Si substrate is deposited with Cr/Al release layer (b) Nb ground plane is sputter deposited (c) spin-on PI-2611 to a 10 μm thick film (d) deposit Al (e) pattern and wet etch the Al (f) dry etch the polyimide to make contact to the ground plane.

At the present time, the Nb metallization on these flex cables did exhibit superconductivity. We suspected the curing temperature was suppressing the superconductivity of the Nb films. We therefore shifted our focus to the fabrication of microstrip flex cables that did not subject the Nb metallization to a high temperature cure of 350 °C. Once we obtained superconducting Nb microstrip flex cables, we began to fabricate embedded microstrip flex cables, which were cured with a lower temperature of 225 °C.

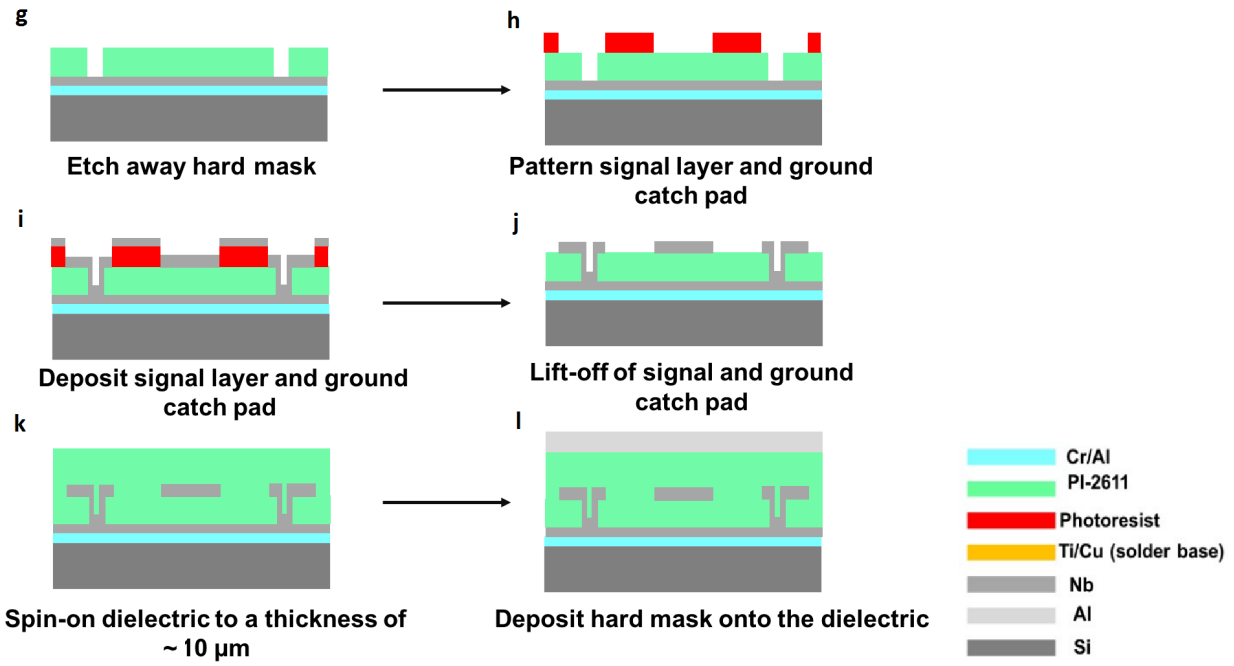

Figure 3.9: Stripline fabrication process flow continued (g) Etch the Al hard mask (h) pattern the signal and via ground contact pads (i) sputter deposit Nb (j) lift-off signal and ground contact pads (k) spin-on PI-2611 to a 10 μm thickness (l) deposit Al hard mask to etch second via.

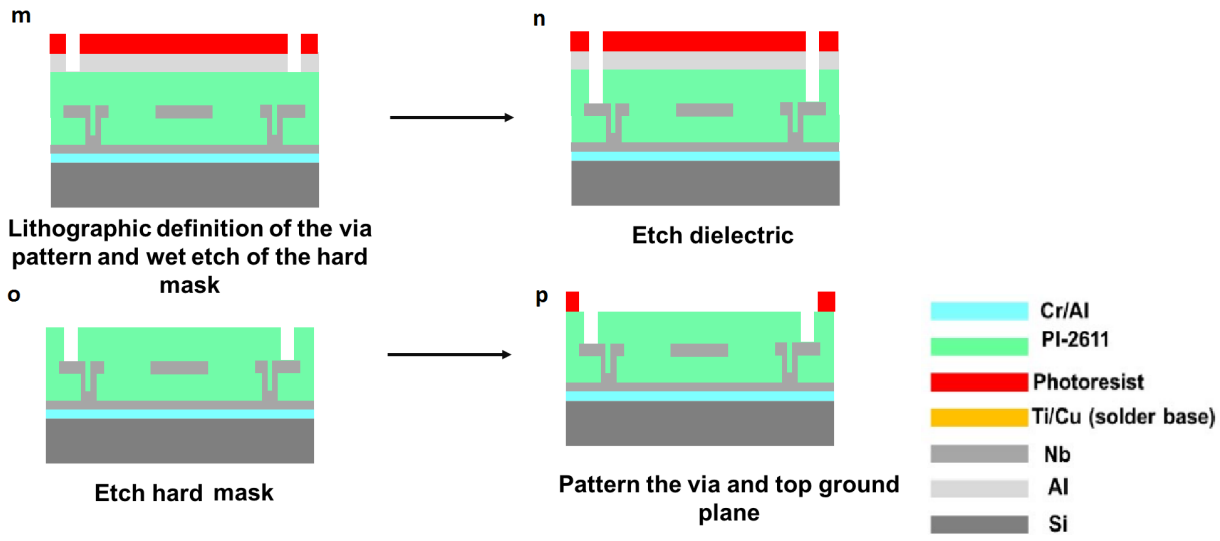

Figure 3.10: Stripline fabrication continued (n) photoresist is applied to to define the second via and the Al hard mask is etched (o) second polyimide layer is etched to make contact to the via contact pad (p) Al hard mask is wet etched (q) pattern the top ground ground plane and via contact to the underlying ground plane

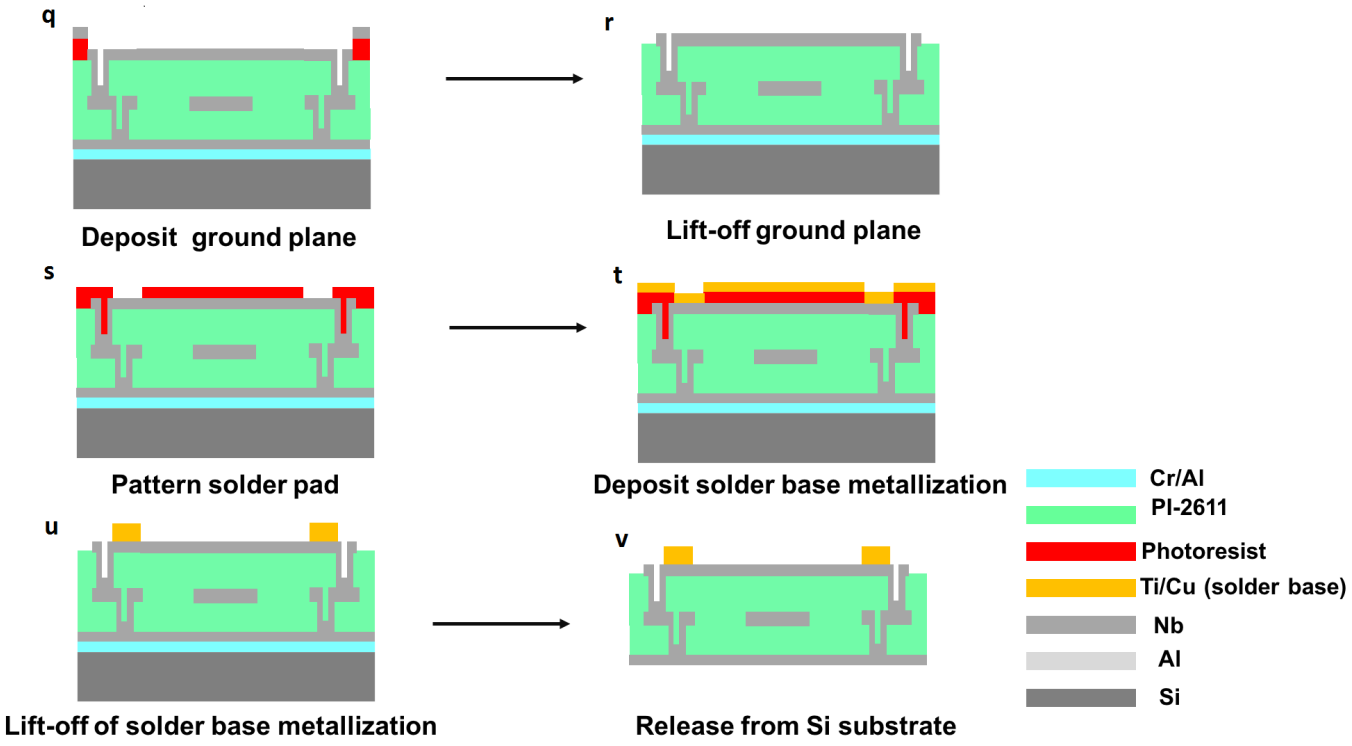

Figure 3.11: Stripline fabrication continued (r) ground plane is deposited (s) groundplane is sputter deposited and contact to via is made (t) photoresist is patterned for solder base metallization (u) solder base is deposited (v) lift-off of the solder base is performed (w) stripline sample is released from the underlying substrate in a salt bath

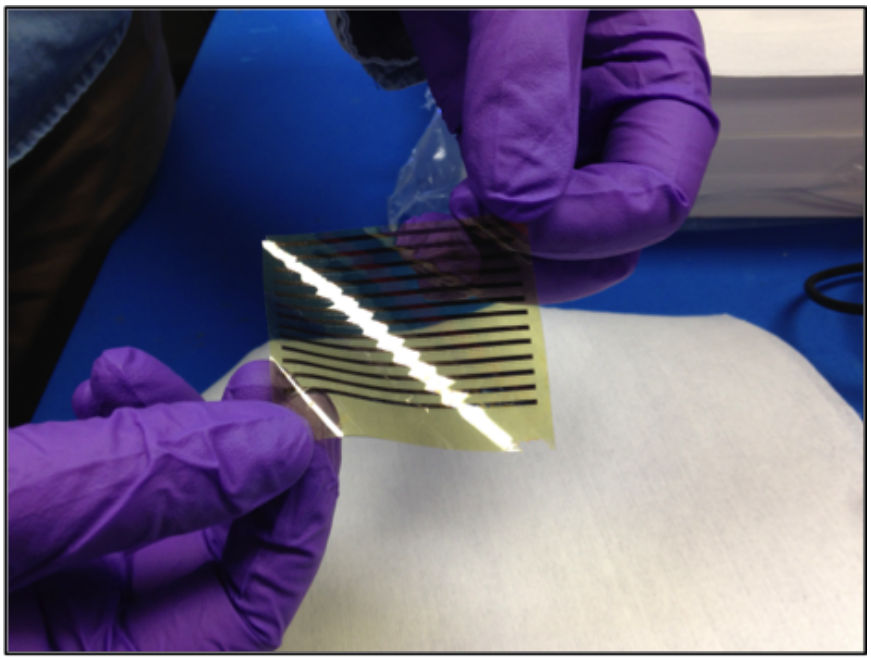

Figure 3.12: A set of 5 cm stripline flex cables released from a 125 mm diameter Si wafer.

Figure 3.13: A set of 1 meter long stripline flex cables released from a 125 mm diameter Si wafer.

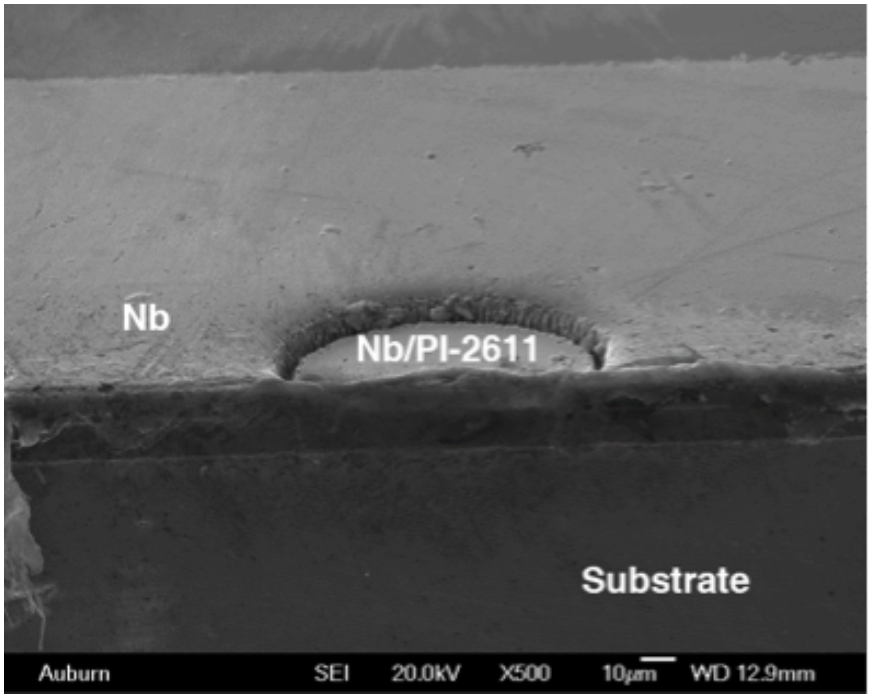

Figure 3.14: SEM image of via01 (ground to the first dielectric layer) covered in polyimide.

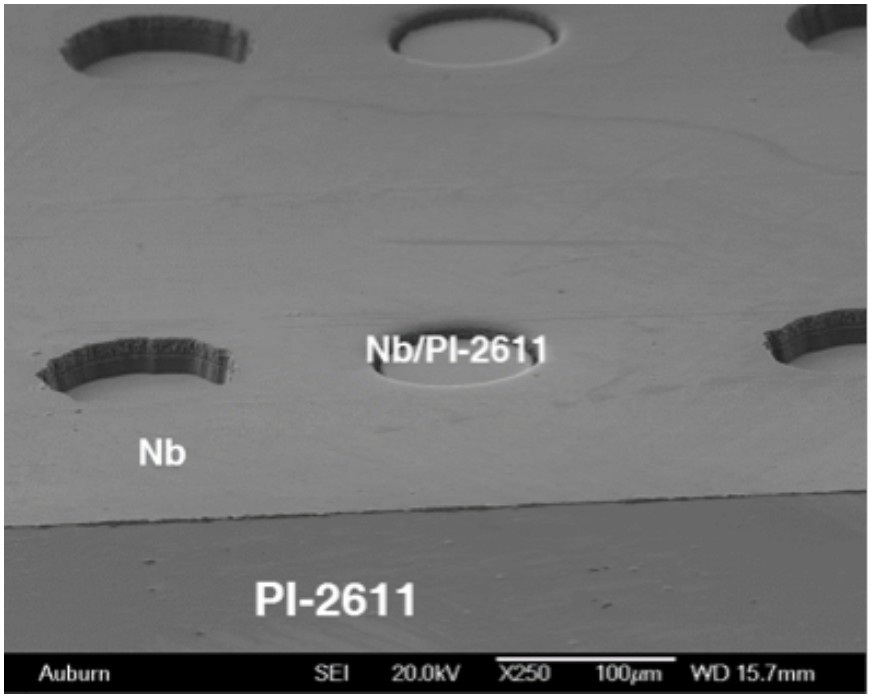

Figure 3.15: SEM image of via01 and via12 shown with via12 (unfilled).

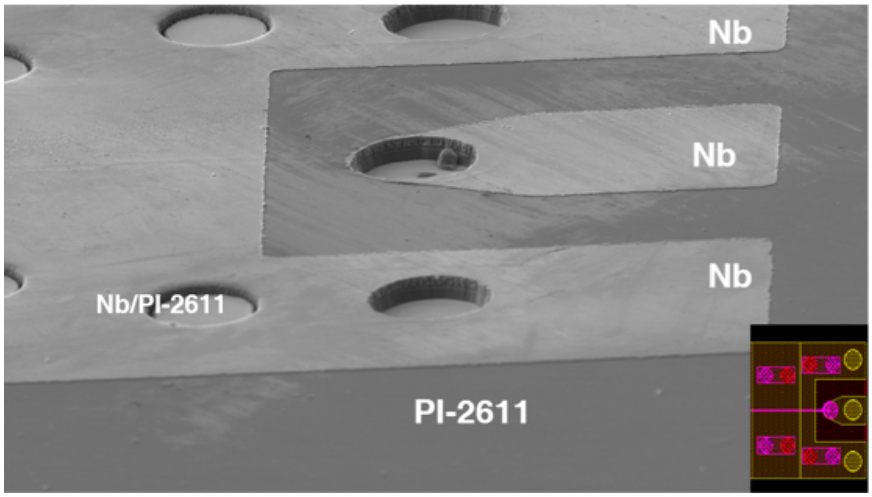

Figure 3.16: SEM of the launch region showing the vias and the top signal/ground metallization.

3.4.2 Microstrip

Microstrip samples were fabricated on 100 mm diameter Si handle wafers following a fabrication process very similar to the stripline. As-received Si wafers were coated with a Cr/Al release layer through EBPVD with a thickness of 500 Å/2000 Å, respectively (Figure 3.17a). An adhesion promoter, VM652, was then spun onto the release layer and baked on a hot plate at 120 °C for 1 minute. The dielectric was then spin coated onto the wafer to a thickness of ∼10 μm and baked on a hotplate at 120 °C for 5 minutes. The wafers were then transferred to a nitrogen ambient oven for curing at 350 °C. Wafers where then exposed to an O_2 plasma at a power of 150 Watts for 20 seconds to improve the adhesion of the next polyimide layer. Wafers were then baked in a vacuum oven at 110 °C for 20 minutes. A second PI-2611 layer was spin-coated following the same steps as the previous layer, to yield a total dielectric thickness of ∼20 μm (Figure 3.17b).

After the dielectric spin-on steps were complete, the signal lines were patterned using a positive-tone photoresist. A two minute ion mill was performed at 1 kV, prior to the Nb sputter deposition. A lift-off process was then undertaken to define the signal lines of the microstrip (Figure 3.17c). After the lift-off process, wafers were patterned for UBM, consisting of Ti/Cu, 500/5000 Å, respectively. Following the UBM deposition and lift-off (Figure 3.17d), wafers were coated with positive-tone photoresist and baked at 110 °C and diced into individual samples. Samples were then loaded into a salt bath solution and released from the Si handle wafer (Figure 3.17e). After the release process was complete, samples were free-standing films that had their surface cleaned from the photoresist using acetone, methanol, and DI water. These samples were then mounted onto a 100 mm Si wafer with the signal side facing the Si polished surface and the backside of the film was exposed. These samples were then loaded into the metal deposition chamber and sputtered with the same parameters as the signal line (Figure 3.17f). A 5 cm long microstrip sample after the backside metallization was completed is shown in Figure 3.18.

Microstrip samples of longer lengths were also fabricated. Meandered microstrip lines that had lengths up to 55 cm were made with the same process outlined above with a different signal mask design. All other processing steps remained the same. A one meter microstrip was also fabricated, but had poor yield. A one meter microstrip, after release from the Si handle wafer is shown in Figure 3.19. the fabrication process was slightly different. The thickness of the dielectric was only $\sim$10 μm thick, requiring only one spin-on and cure step. In addition, this microstrip had a patterned Nb ground plane that was directly deposited onto the release layer. Therefore, the Nb ground plane underwent a 350 °C curing process that appeared to have degraded the Nb quality. We therefore began studying embedded microstrip flex cables, discussed in the next-section with a lower dielectric curing of 225 °C temperature.

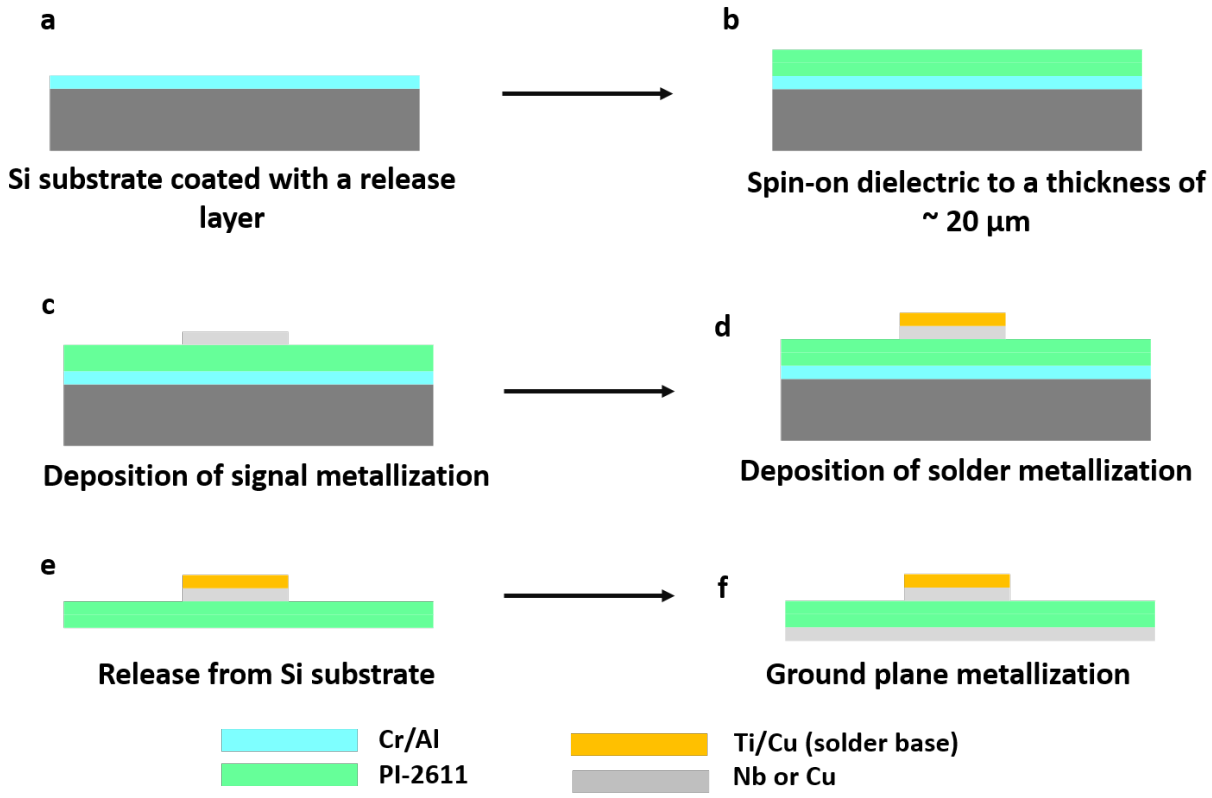

Figure 3.17: Microstrip fabrication process on PI-2611 (a) release layer is deposited onto a Si wafer (b) PI-2611 is applied and cured in two steps to achieve a 20 μm thick dielectric (c) signal layer is sputter deposited (d) solder base is deposited by EBPVD (e) samples are released from the wafer (f) ground plane of the microstrip is sputter deposited.

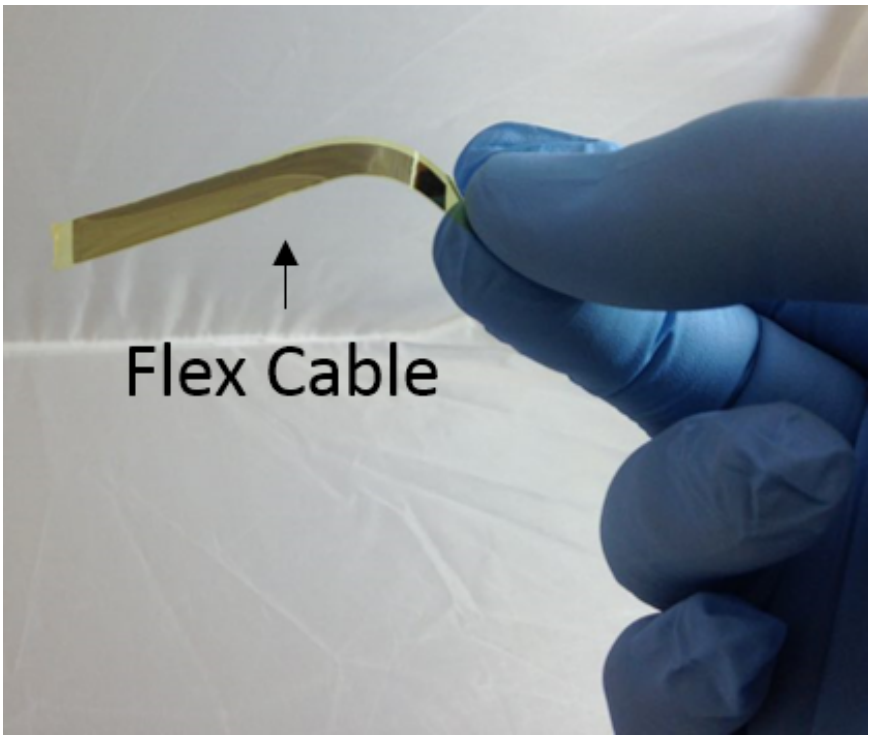

Figure 3.18: A 5 cm flex cable fabricated on PI-2611 after backside Nb metallization.

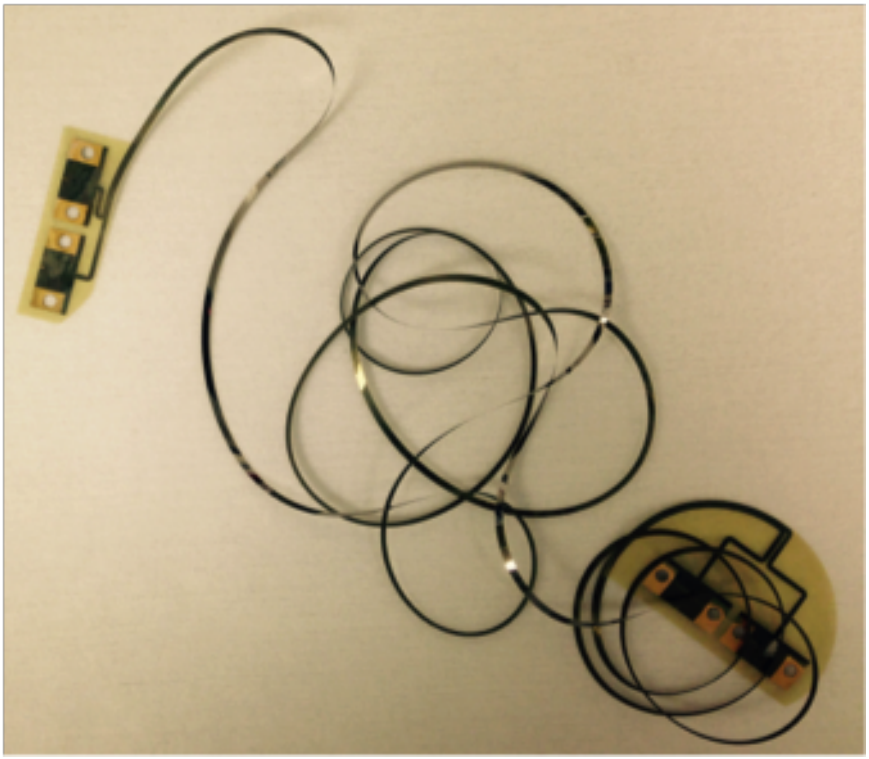

Figure 3.19: A one meter microstrip after release from a 100 mm diameter Si wafer.

3.4.3 Embedded microstrip

The fabrication process of an embedded microstrip follows the same fabrication steps as the 5 cm long microstrip. After the signal layer was deposited and lift-off process was preformed, Kapton tape was then placed onto each end of the solder pad regions of the microstrip to prevent the polyimide from encasing these connection points. The polyimide was then applied to a thickness of $\sim$10 μm and cured in a nitrogen ambient oven at 225 °C. This temperature was experimentally determined to be sufficient to cure the dielectric and not significantly degrade the superconducting properties of the Nb. After the top dielectric layer was cured on the signal line, we removed the Kapton tape from the solder pads and the samples were patterned for UBM metallization. We deposited a UBM of Ti/Cu consisted of a thickness of 500/5000 Å, respectively. After a lift-off, these samples were diced and released from the Si handle wafer in a salt bath solution. The free-standing films where then mounted onto a new Si handle wafer, with the signal side facing the wafer and the backside was sputter deposited Nb.

3.5 Flex cable release process

At the end of the front-side fabrication process (signal and UBM metallization), the samples were diced and removed from the Si handle wafer through the anodic dissolution of Al in a salt bath. The release process of these flex cables was not limited by the design or substrate size, although larger substrates required a longer time to release. Due to our equipment capabilities and processing steps required, we either used a 100 or 125 mm diameter Si handle wafers. The release layer consisted of a chromium and aluminum layers that were 500 Å and 2000 Å thick, respectively.

The flex cables were released from the underlying substrate by anodically etching the Al seed layer in a NaCl water bath. The samples were submerged into a 2 M solution and biased at 0.5 V. From Figure 3.20, we note that at potentials that are higher than -0.5 V, the aluminum begins to be etched away in the water bath. This implies that even without

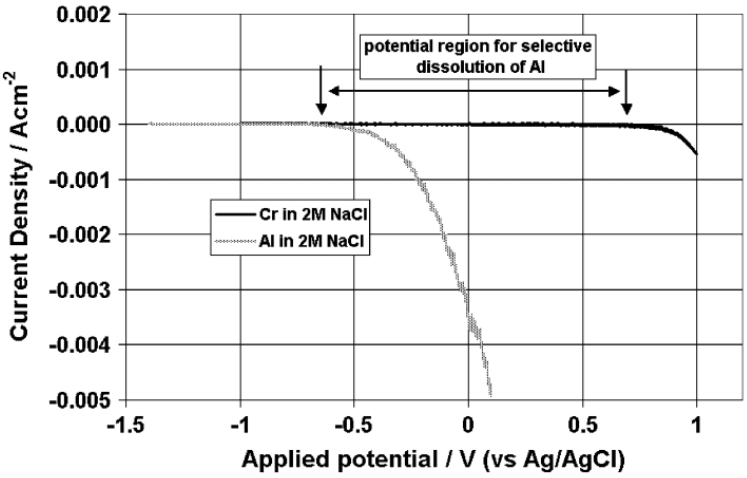

Figure 3.20: Current density versus applied potential. The regions for aluminum dissolution are shown as a light grey line and as a dark line for chromium. Adapted from [42].

a potential applied to the wafer, the Al will be etched away in the presence of a NaCl bath. The process is described in greater detail by Metz et al., in their work they measured the release rate of polyimide and SU-8 with a set of controlled areas [42].

The salt water bath consisted of laboratory grade sodium chloride (NaCl)[2] that was mixed with deionized (DI) water to create a solution that was 2 Molar (M) in concentration. The calculations are shown in Equation 3.1. In the most general case for any volume (V) to produce a 2M concentration solution of NaCl in DI water. Therefore a 1.5 L solution of 2 M solution would require 175.2 g of NaCl. The release process was undertaken at room temperature. Typical release times varied from several hours to over 24 hours.

$$m_{NaCl} = V_{H_2O} \times \frac{116.8g \cdot NaCl}{1L \cdot H_2O}[g] \tag{3.1}$$

[2]Sigma-Aldrich CAS # 647-14-5

Chapter 4

Measurement Setup and Calibration

In this chapter we present the equipment in our laboratory that was used for DC and RF measurements, which include the storage Dewars for liquid nitrogen and helium and a pulse tube based cryostat. We also present the measurement holders that were custom designed to be interfaced with our different systems. In addition, we also discuss the LabVIEW software that was written to automate routine DC and RF measurements. We review in-depth the RF calibration process and introduce RF standards that were built on edge launch connectors.

This chapter begins with a discussion of the LabVIEW software that was written for automating resistance vs. temperature measurements (for determining T_c) and controlling a set of RF switches for calibration. We then discuss in great detail the calibration process that was required to reduce the systematic errors of the network analyzer and cabling. We then discuss the calibration method and standards that we built to calibrate the measurement equipment in liquid helium. We then conclude this chapter with a comparison of these standards to commercially available calibration kit at room temperature to asses any major differences.

4.1 Measurement equipment and automation

The cryogenic systems in our laboratory consist of a Cryo Industries of America pulse tube (PT) based cryostat with a base temperature of $\sim$3 K (Figure 4.1) and liquid nitrogen and helium Dewars from CryoFab, as shown in Figure 4.2. The temperature of the cryostat was monitored with a Lakeshore 335 temperature controller. We have the capabilities to perform 2-wire or 4-wire DC resistance measurements of samples through the use of an

Agilent 34420a micro-ohm meter. For RF measurements, we used a Agilent PNA N5227A 4-port network analyzer, shown in Figure 4.3.

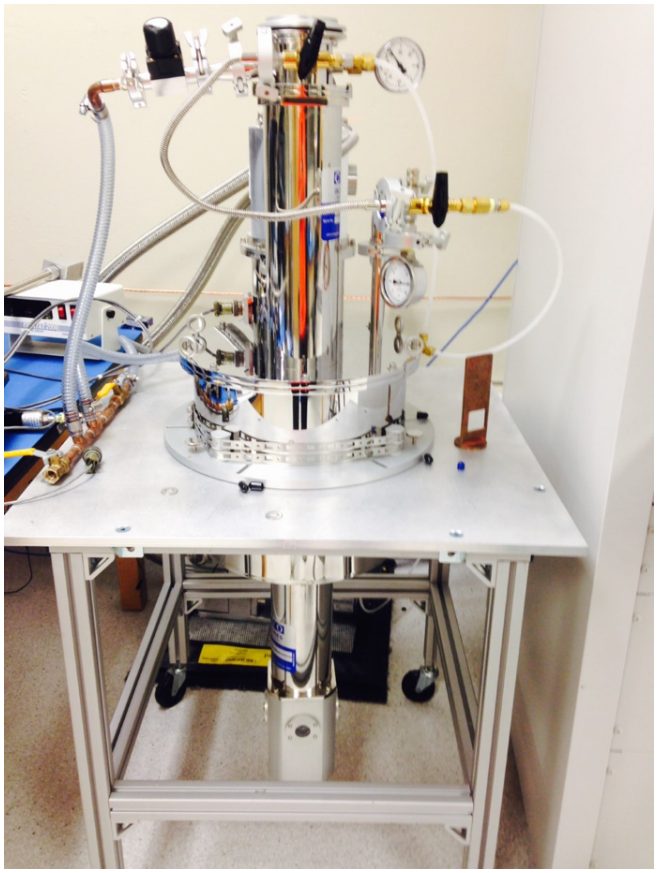

Figure 4.1: Cryo Industries of America pulse tube based cryostat.

4.1.1 T_c measurements

Two LabVIEW programs were developed to allow the users in our laboratory record temperature and resistance data to lowest temperature in the PT, which is ~3 K. The first program shown in Figure 4.4, allows the user to measure the resistance of the sample as it cools down in the PT. In Figure 4.5, the block diagram is shown. A while-loop monitors the current temperature and compares it to the given set-point, if the temperature is less than or equal to the given set-point, the program stops. Basic error handling was also implemented in the program; if the software loses connectivity to the measurement equipment,the

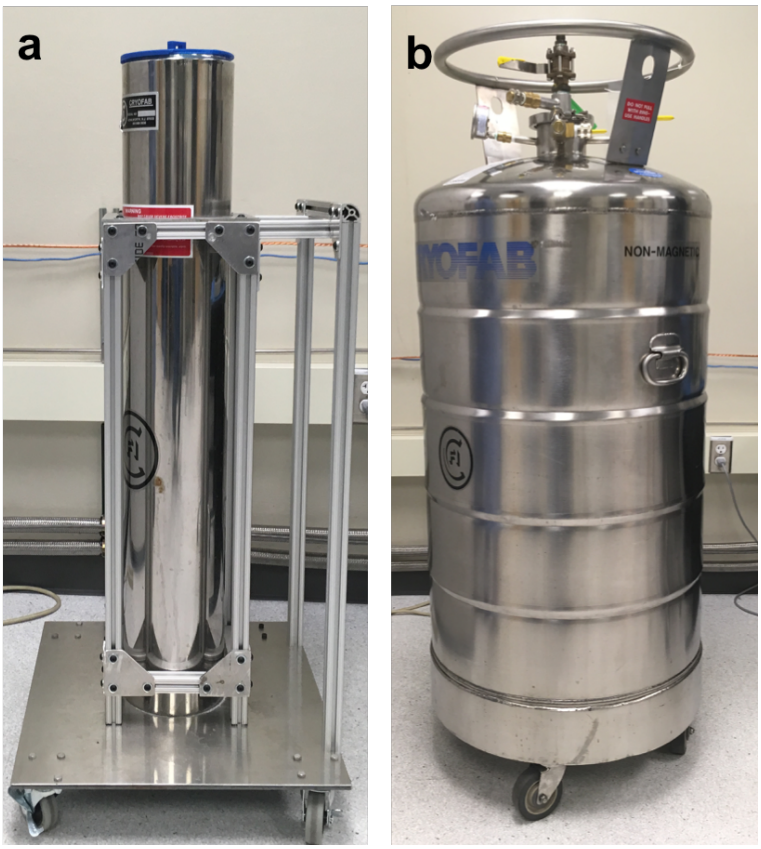

Figure 4.2: Dewars in our laboratory for (a) liquid nitrogen (b) liquid helium.

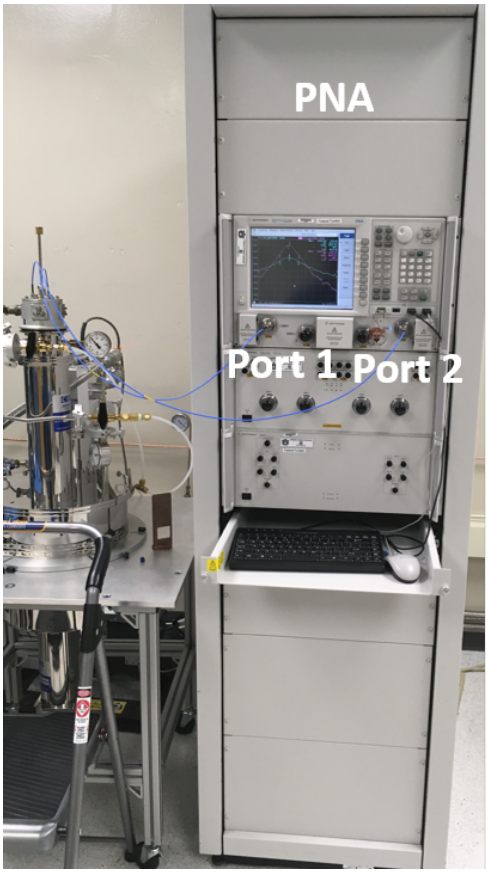

Figure 4.3: Agilent PNA N5227A 4-port network analyzer connected to the pulse tube cryostat with ports 1 and 2 labeled.

measurements are stopped. The software reads the temperature from a Lakeshore 335 temperature controller and queries a Keysight 34420A micro-ohm meter every second. The data is stored in two individuals arrays, one for the temperature and another for the resistance values. Once the program finishes gathering data, it prompts the operator to save the data. The arrays of information are then written to a tab-delimited file. The file contains header information with the sample id, temperature, and resistance.

The second resistance measurement program, is a bit more complex, the front panel of the program is shown in Figure 4.6. This program allows the operator to set a starting temperature, a final temperature, a temperature step size, a wait time before going onto the next set-point, and a heater controller. The program verifies the set-point temperature is higher than the current temperature, it then sets the temperature on the Lakeshore controller

to the given start temperature and heats the sample holder, the program waits until it is within 0.5% of the given temperature set point. Once the set point temperature has been reached, the program dwells for a user-given amount of time (default: one minute), before it takes a set of three resistance measurements and averages the values. The program then proceeds to the next temperature set point by increasing the current set-point by the given step size. The "middle_setpoint" in the program, allows the user to increase to take coarser step sizes after it reaches the "middle_setpoint". The "coarse_step size" and by default set to increment at 5 K intervals, it is used to reduce the measurement time at the higher temperature ranges, where the resistance does not changing significantly. The "heater range" controls how much power is provided to the resistive heater to raise the temperature of the sample sensor to the given set point.

A custom PCB was made that used pogo[1] pins to interface to samples that were $\sim$ 2.1 $\times$ 2.1 cm^2 in area. Pogo pins were used for making resistance measurements with minimal damage caused to the samples. The PCB is shown in Figure 4.7, two pogo pins force and sink the current, and the two other pogo pins measure the voltage. By using a 4-wire measurement setup, we eliminated the resistance from the cabling. The sample holder used in these measurements is shown in Figure 4.8.

4.1.2 Microwave switches

LabVIEW code was written to control the RF outputs of two microwave switches at room temperature and in liquid He. We used a BK Precision 1697 DC power supply and a Measurement Computing USB-ERB24 DC relay to pulse a voltage to two radiall[2] microwave switches. Therefore, by using one relay, we used a single power supply to actuate the two switches independently. Each position on the relay was addressed by writing a bit-string to the DC relay. A table that summarizes the bit-strings for the different positions that were

[1]Everett Charles Technologies: HPA-0J
[2]Model: R573 423 600

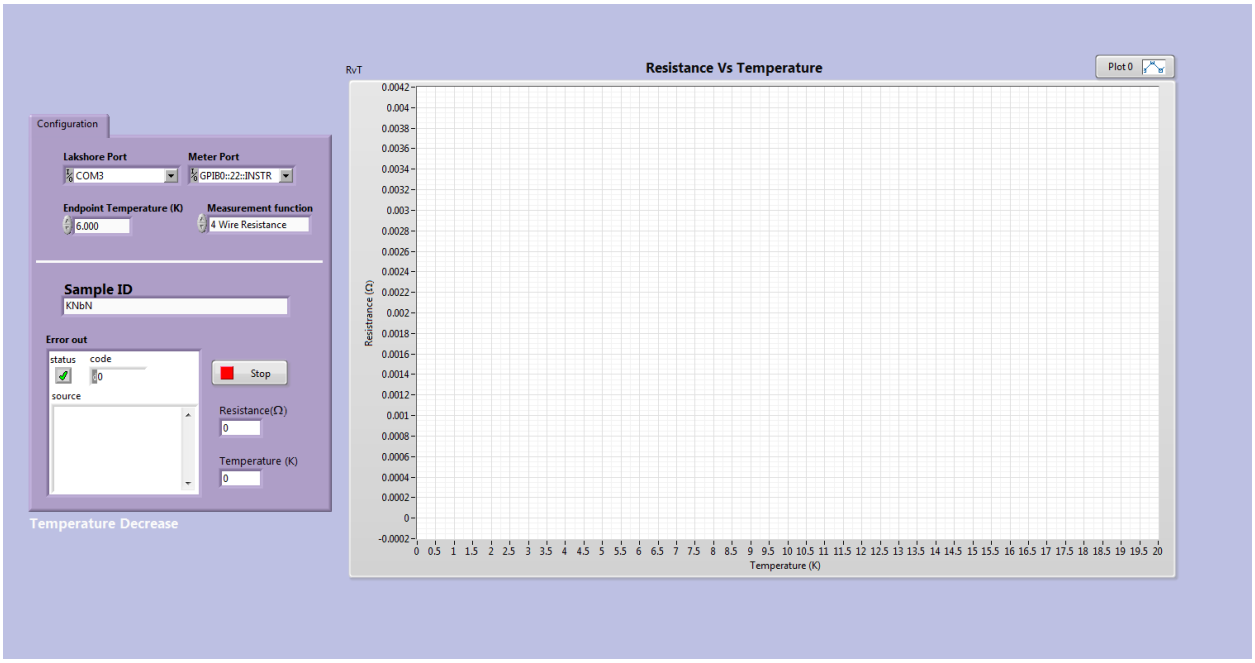

Figure 4.4: LabVIEW front panel for the acquisition of resistance data. Software stops logging data at a given setpoint temperature.

used to control the switches is shown in Table 4.1. The equipment that used to interface and operate the switches is shown in Figure 4.9.

The front panel diagram of the Labview code is shown in Figure 4.10. The program interfaces to a BK power supply and sets the voltage, based on the test environment: "Testing at 4.2 K" or "room temperature", sets the voltage to either 28 Volts or 10 Volts. The power supply leads are wired to the connected (C) position, and the output lines are connected to the normally open position (NO). We latch to the given position by writing a bit-string to the relay, which latches from the C to the NO. We reset the latch, by addressing the position and writing a bit string of "0", which forces the relay to unlatch. When a position is latched, it sends either a 28 Volt or 10 Volt signal to the given position, which forces the microwave switch to latch to the given position. The bit strings to address a position on the switch is shown in Table 4.1. Relay positions 1-8 were used for switch 1 and positions 9 through 16 were used for switch 2. Some modifications to the switch were made to have the switch

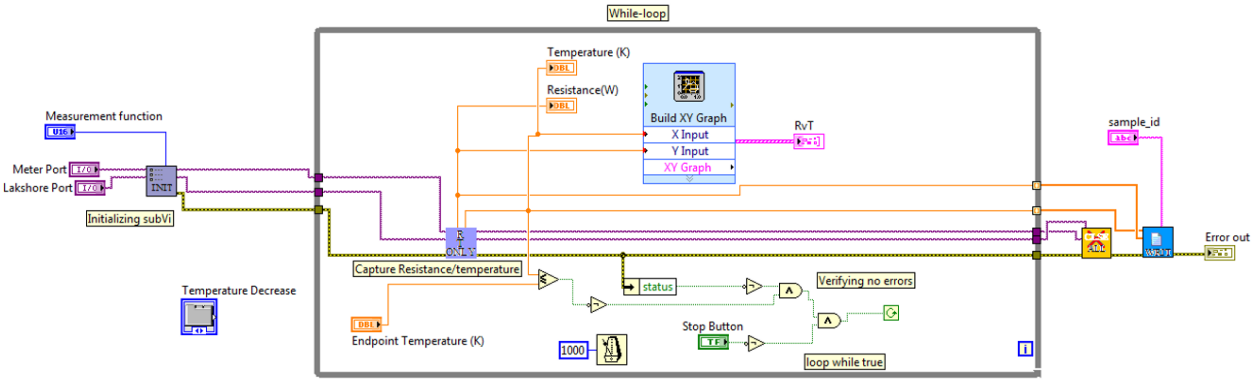

Figure 4.5: LabVIEW block diagram for the acquisition of resistance data.

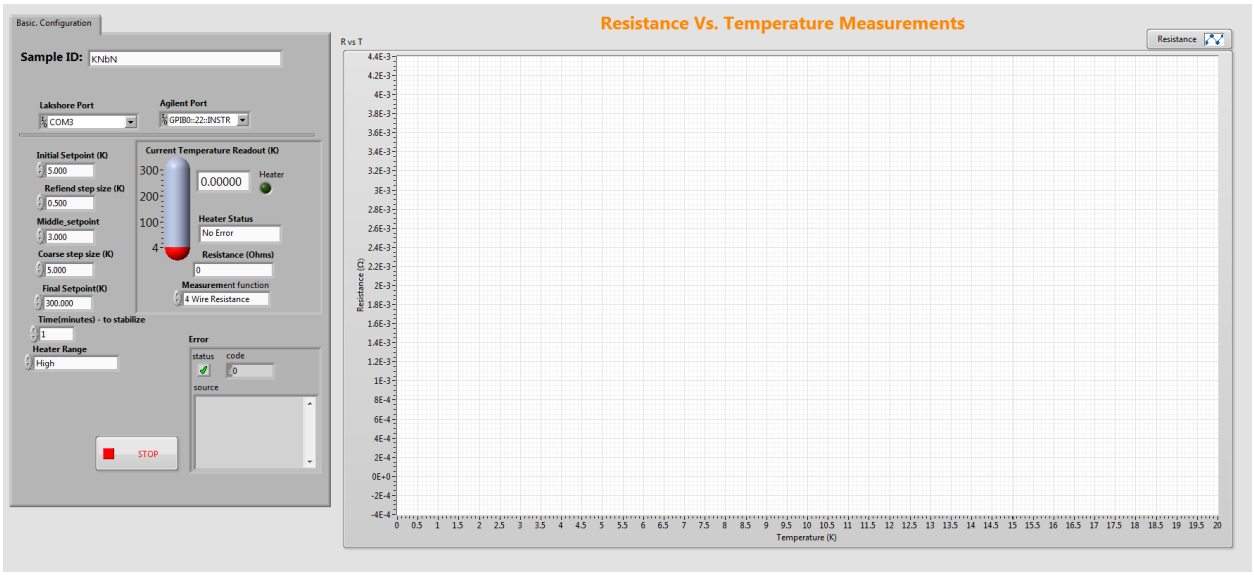

Figure 4.6: Front panel for a LabVIEW program that allows the user to ramp the temperature to a given set point and acquire resistance data as a function of increasing temperature.

work in liquid He. A schematic diagram of how the different equipment is wired is shown in Figure 4.11.

An as-received RF switch, is shown in Figure 4.12, has a protective metal enclosure and inside are two PCBs that are vertically stacked that route the DC signal, ground, and reset traces to a set of nine pins. Based on the dissertation by Kurtis [43], we removed the enclosure on one switch, removed the two PCBs and directly soldered DC lines to the

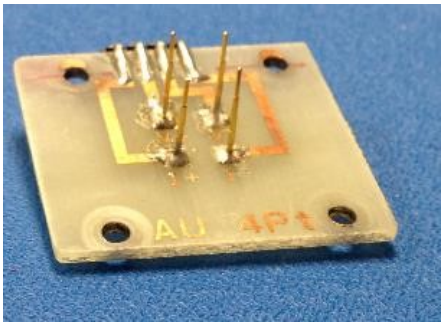

Figure 4.7: PCB for four-wire resistance measurements.

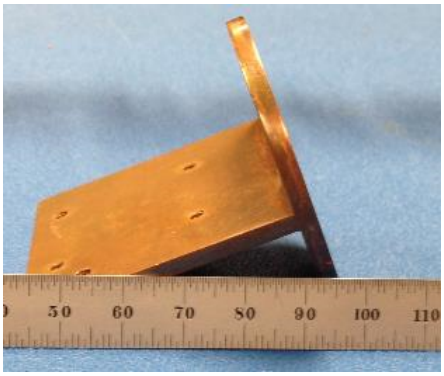

Figure 4.8: Sample holder for 2.1 cm $\times$ 2.1 cm sized samples.

pins on the switch. Prior to making direct connections to the fragile pins, we used a non-conductive cryogenic epoxy[3] to keep these pins in-place. As shown in Figure 4.13, the ground connections to each solenoid are connected together, the reset locations are also wired to a common reset wire. Each switch was modified the same with the connections following the same color scheme, in order to track the wiring.

[3]Stycast 2850-FT, Catalyst 9

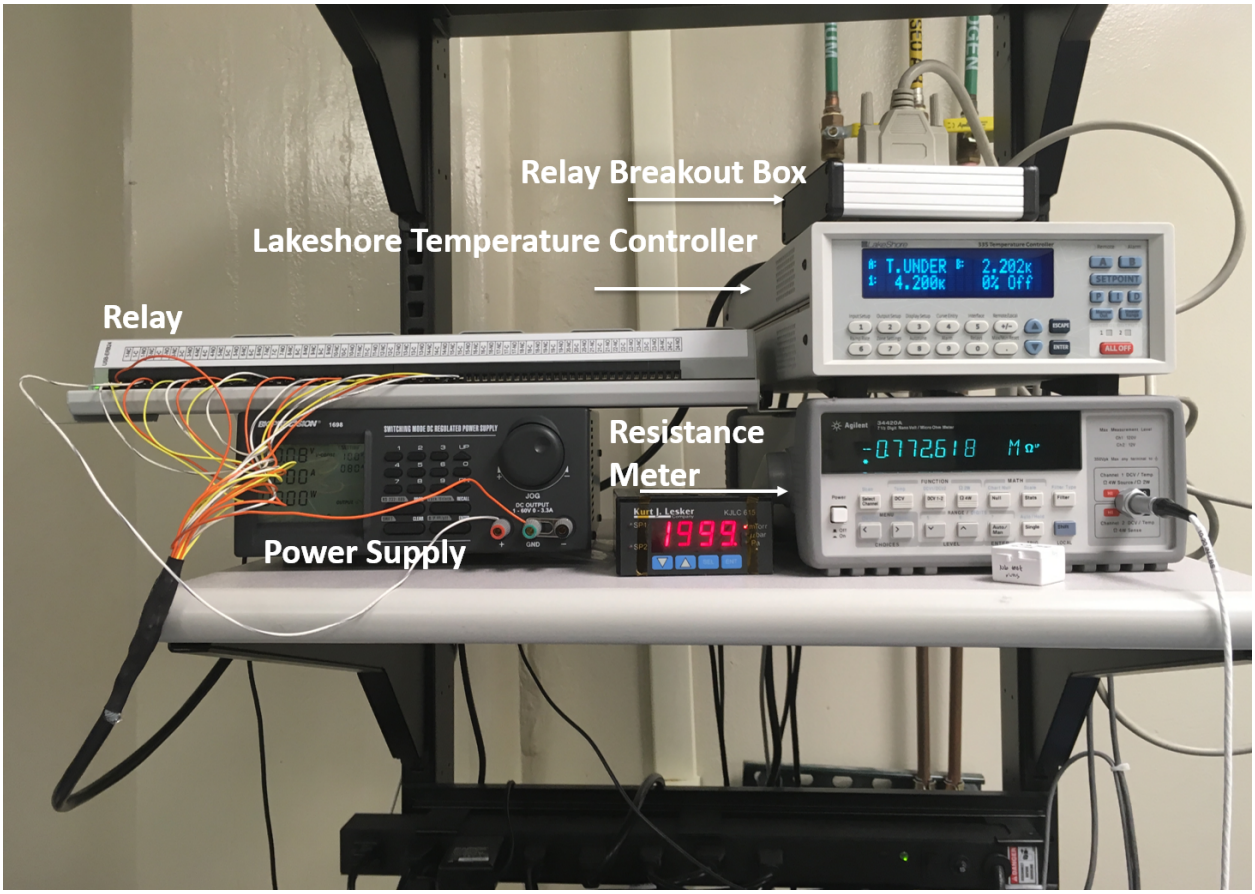

Figure 4.9: Equipment used for controlling microwave switches and ancillary hardware used to measure the resistance of samples.

Table 4.1: Relay positions and bit address string for two RF switches.

Relay Position	Bit string	Switch Position	Note
1	-	GND	Negative Common
2	0000 0010 ($0x2_{16}$)	1	Open
3	0000 0100 ($0x4_{16}$)	2	Short
7	0100 0000 ($0x40_{16}$)	6	Load
8	1000 0000 ($0x80_{16}$)	Reset	Reset
9	0001 0000 0000 ($0x100_{16}$)	1	Open
10	0010 0000 0000 ($0x200_{16}$)	2	Short
11	0100 0000 0000 ($0x400_{16}$)	3	Load
15	0100 0000 0000 0000 ($0x4000_{16}$)	Reset	Reset
6 & 14	0010 0000 0010 0000 ($0x2020_{16}$)	5, 4	Thru

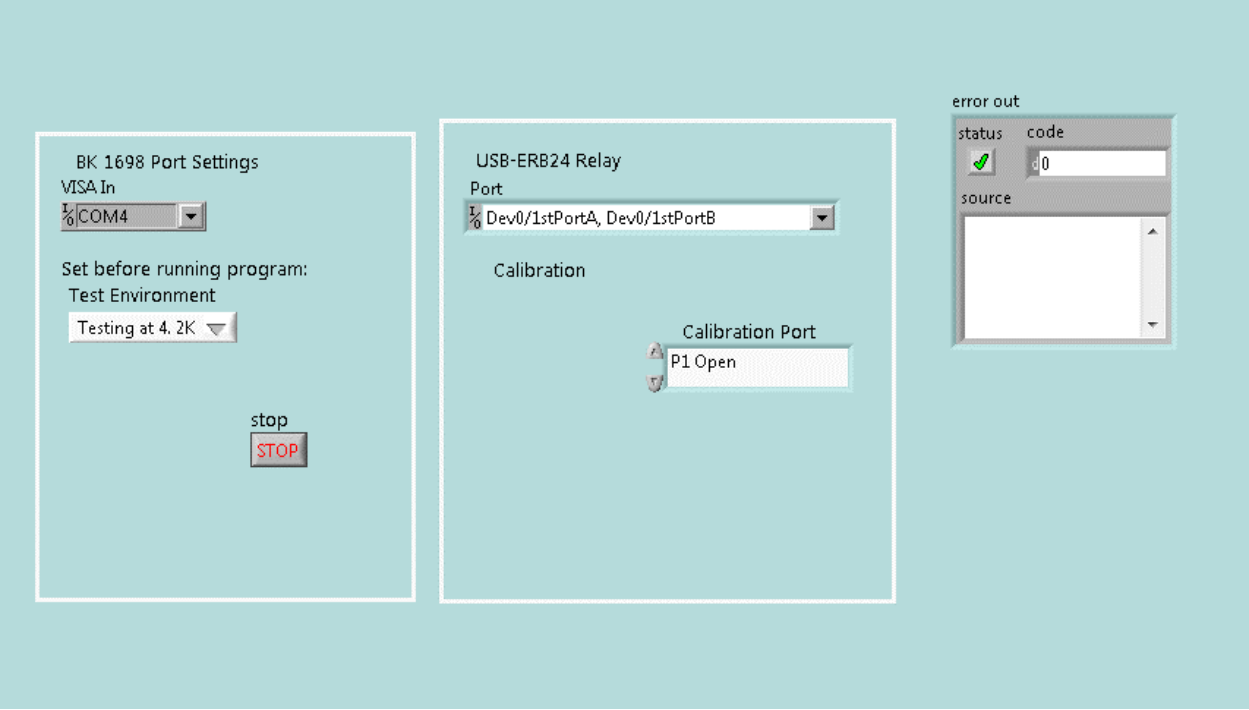

Figure 4.10: LabVIEW front panel for controlling two radiall RF switches.

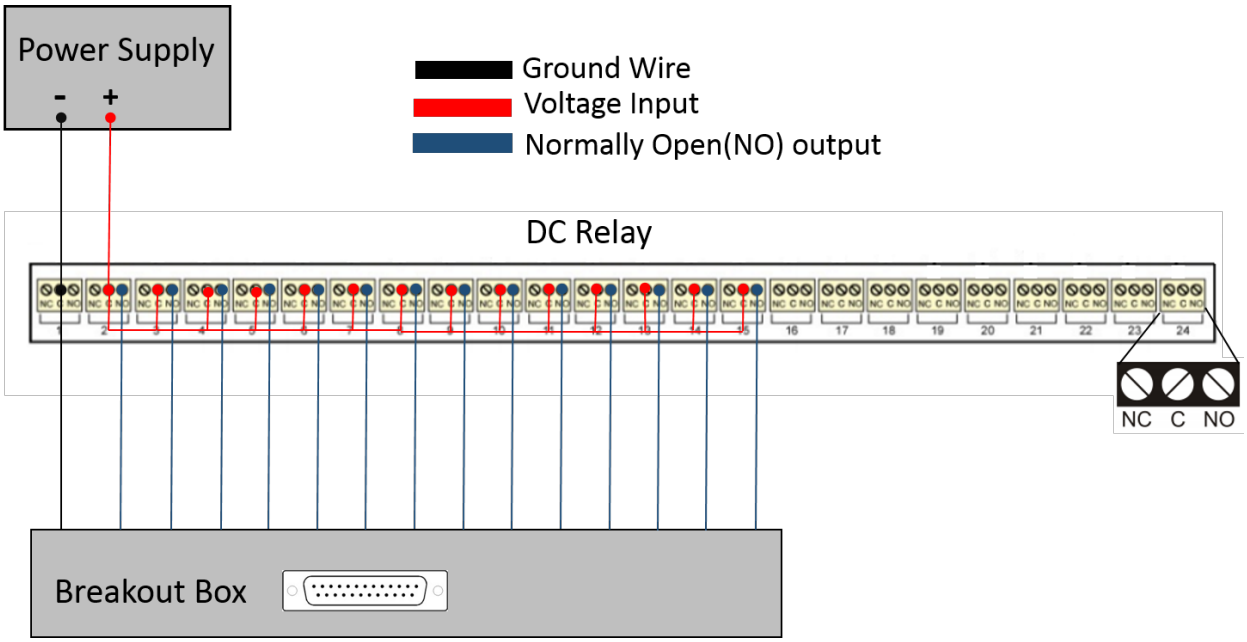

Figure 4.11: Schematic diagram of the equipment used to control radiall switches. Ground wire is connected to (C) on pin 1, the voltage outputs on the relay are connected to the normally open (NO), and the voltage input is connected on (C) of pin 2 on the relay.

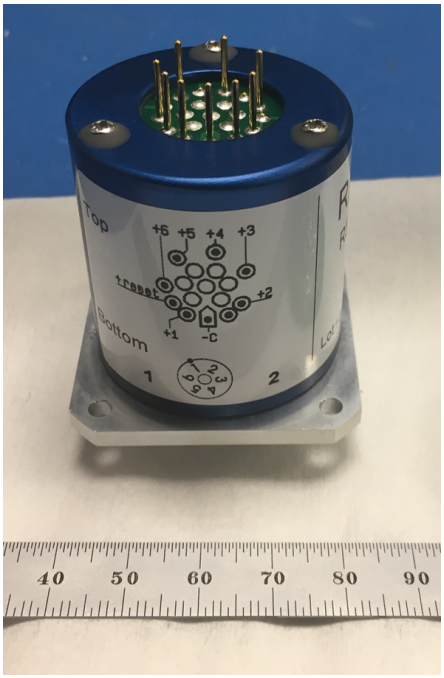

Figure 4.12: An as-received radiall six-position RF switch.

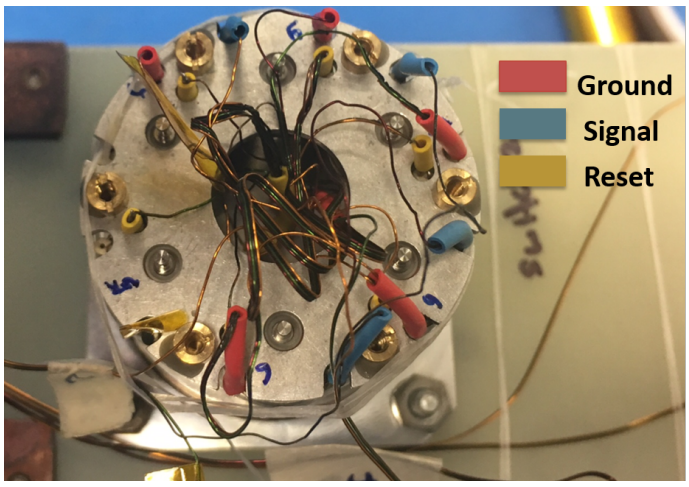

Figure 4.13: Radiall switch with the PCB removed and connections soldered directly. Red is the common ground, blue is signal, and yellow is the reset.

4.2 Calibration overview

The purpose of an RF calibration is to reduce system errors introduced by the internals of the measurement equipment, cabling, and adapters that are used to interface to the device under test (DUT). What follows is a discussion of the calibration process for a short-open-load-Thru (SOLT) calibration that is very similar to a short-open-load-reciprocal thru calibration to discuss some of the errors that are mathematically corrected for in the network analyzer. The error correction process would be similar with other types of calibration methods such as thru-reflect-line (TRL) method.

A simplified block diagram of the internals of a network analyzer is shown in Figure 4.14. The source generates the signals that are sent to an incident receiver R and to the DUT. The purpose of the incident receiver is to track the source signal magnitude and phase. The reflected and transmitted receivers are used to measure the signal that was either reflected by the DUT or transmitted through it.

Error correction is applied internally in the network analyzer to correct for signal leakage in the couplers and internal circuitry. The errors that are calibrated for are outlined in Figure 4.15. There are four main error corrections that are performed during an SOLT calibration. The first error correction is shown in Figure 4.15a, a 50 Ω load would be connected on port 1, a signal would be transmitted and receiver R would track the magnitude and phase of the signal sourced. Receiver A is expecting no reflections, therefore no signal should be measured on A. Due to the couplers and the different paths that the signal takes inside the network analyzer, some signal reaches receiver A, this would be considered a directivity error.

The second error correction is shown in Figure 4.15b, with the load connected to the input port. A signal is generated and incident on the load, since this is a one port measurement, receiver B should not measure any signal. Due the internal circuity, a signal is measured on receiver B. This is considered an isolation error. Ports 1 and 2 should be completely isolated from each other.

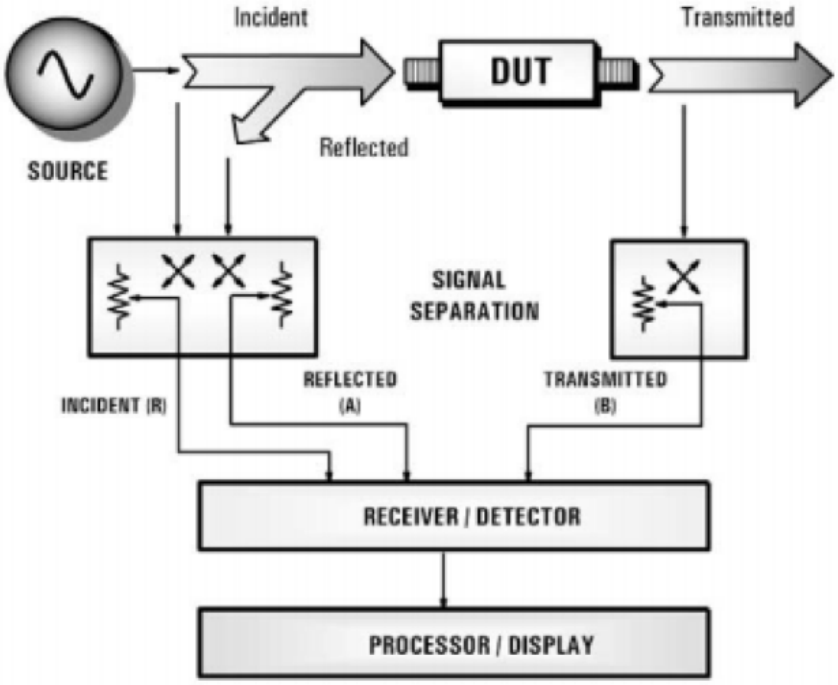

Figure 4.14: A simplified block diagram of a network analyzer. Adapted from [44].

After the load has been measured, the third correction is applied by connecting a short or an open standard (a reflection standard is needed) on port 1. When the signal is sourced and reaches the short or the open, the signal should be completely reflected back to receiver A, but due to internal reflections from the connections, some of the signal does not reach receiver A. This is called a source match error and is illustrated in Figure 4.15c.

The fourth correction is applied by measuring a thru standard. As shown in Figure 4.15d, a signal would be sent to the thru standard and receiver B would measure the output through the DUT. Some of the signal is reflected on port 2 and is measured on receiver A, this is termed a load match error. This error is removed from transmission and reflection measurements [45]. There are two other errors that are also calibrated for by the network analyzer, they are termed frequency response reflection and frequency response transmission tracking errors [45]. Frequency response reflection tracking uses the short and open to analyze the amplitude of the signal that reached receiver A and compares it to the reference receiver

R. The amplitudes of the signal should be the same, but due to cabling and adapters, they are not. Therefore complex math is used to calculate the difference and mathematically corrected for to reduce the difference. The same process is used for transmission tracking error, except a thru is used, and the magnitude of the signal transmitted to receiver B is compared to the reference receiver R. A diagram of this process is shown in Figure 4.16.

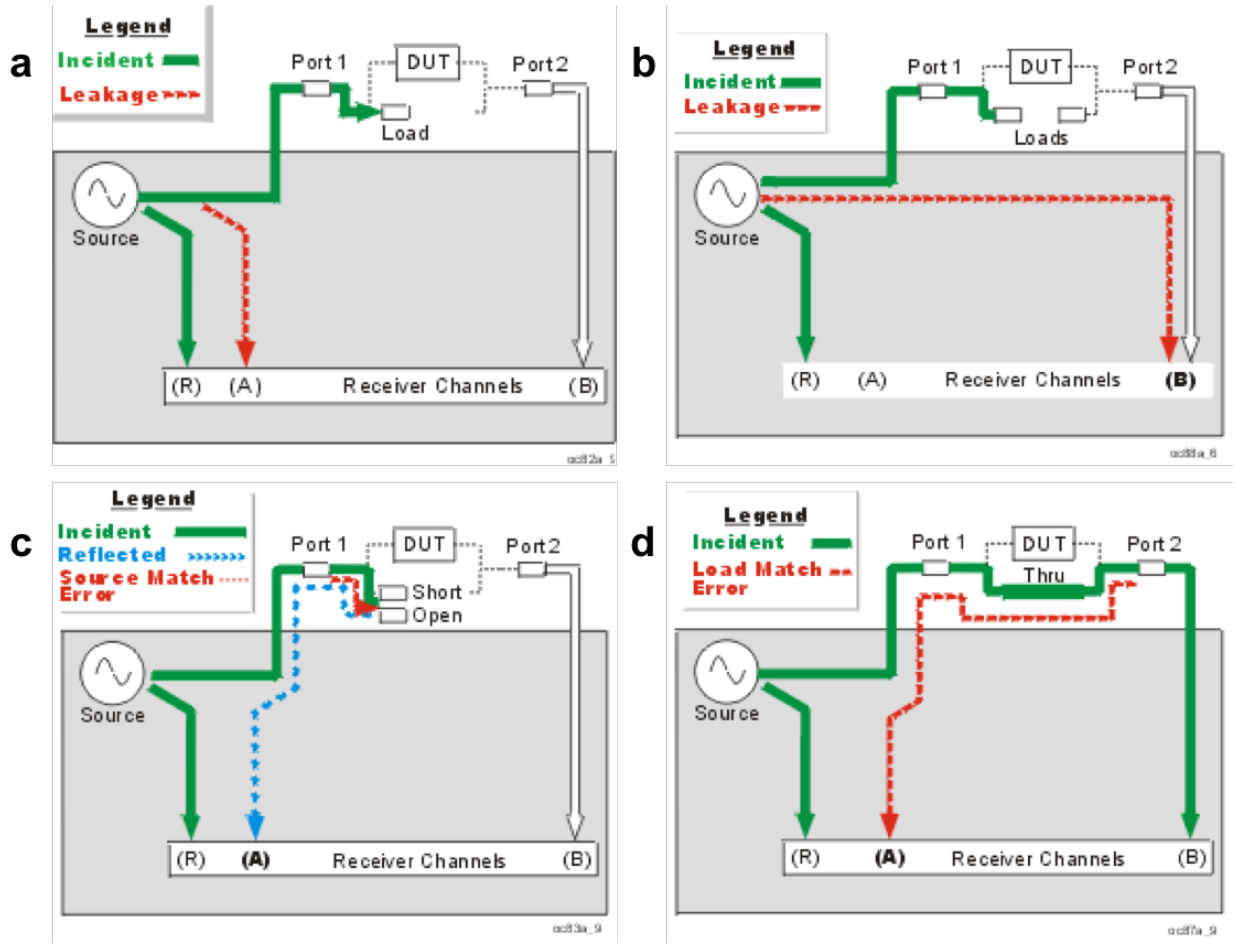

Figure 4.15: Calibration process for reducing systematic measurement (a) directivity (b) isolation (c) source and (d) load errors. Adapted from [45].

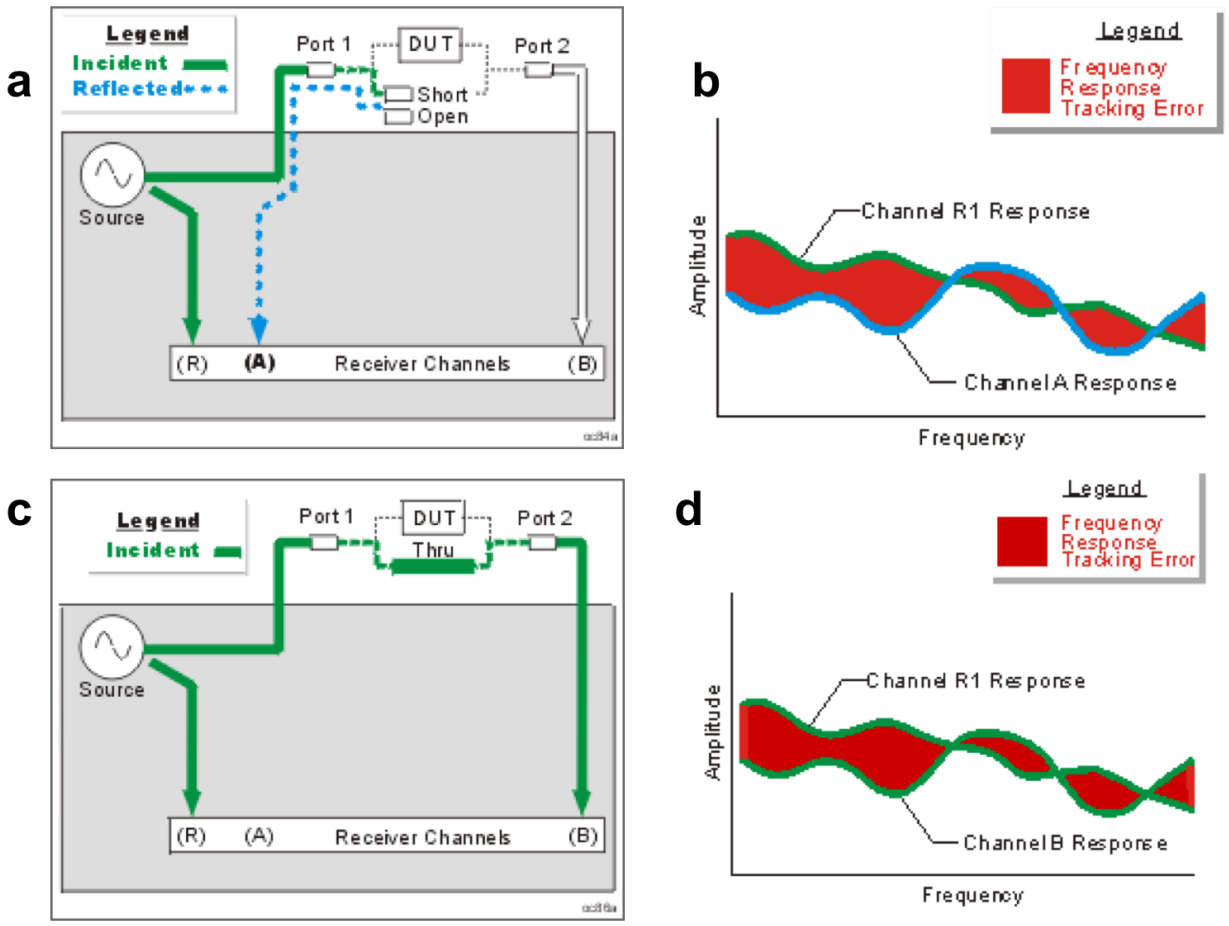

Figure 4.16: Frequency response and reflection and transmission tracking errors (a) short or open connected (b) amplitude of signal compared to reference receiver A (c) thru measurement for transmission tracking error and (d) amplitude of signal comparison to receiver B. Adapted from [45].

4.3 Cryogenic calibration

Mechanical and electronic calibration standards that are commonly used for room temperature calibration are generally not usable at cryogenic temperatures. For example, the Keysight (Agilent) 85052D calibration kit used in this work for room temperature calibration has a rated temperature range between 20 °C (293.2 K) to 26 °C (299.15 K) [46]. Therefore, for calibration at cryogenic temperatures, it is necessary to make or assemble standards that that can be used from temperature of 77 K and below. At cryogenic temperatures, TRL calibration [47] is one of the most commonly used methods at low temperatures to set the reference plane at the Device Under Test (DUT) [7, 48]. For ultra-low temperatures (mK range), microwave switches with TRL standards are used for calibration. For most applications, TRL is the most suitable calibration method when the DUT is interfaced through a PCB or a custom-made holder [7, 49], especially when the DUT is the only changing component.

An alternative, albeit less accurate calibration method, using a single port is a Short-Open-Load (SOL) calibration. SOL has been previously shown to be a suitable calibration method at low temperatures to calibrate the network analyzer and to set the reference plane at the DUT [50, 51]. A one port calibration does not remove the errors associated with transmission or load match. Therefore this calibration is limited in accuracy. What is of interest in their work was the use Nichrome films that were made into 50 ohm resistors. These resistors were shown to be stable at temperatures as low as 4.2 K.

A two-port calibration method such as SOLT (Short-Open-Load-Thru) requires a known electrical length for the thru standard and requires four standards, not including the DUT. Meanwhile, SOLR (Short-Open-Load-Reciprocal thru) calibration only requires three standards with the DUT serving as the uknown-thru [52]. The calibration is similar to the SOLT, with the exception of the thru standard. In the SOLR calibration, there are no assumptions made on the electrical length of the thru sample, the network analyzer determines this electrical length. In order for the network analyzer to determine this electrical length, the thru

has to be reciprocal ($S_{21} = S_{12}$) and there has to be less than 40 dB loss to the DUT, otherwise there is not enough signal coming back to the network analyzer to accurately determine the length [53].

For our research purposes, where the material sets were changing including the metallization, the TRL calibration method would have been impractical. If we were to have used a TRL calibration, we would have needed to build set of standards for every variation of metallization and dielectric of interest. Therefore, the SOLR calibration method was the most suitable; it reduced the calibration time, the DUT was used as a calibration standard, and it reduced the calibration error by limiting the cable movements and adapters needed to interface to the DUT. Therefore, we developed a set of calibration standards (Short-Open-Load) on Southwest Microwave edge launch connectors for the SOLR calibration method. Based on the work reported by [51] that showed the stability of NiCr metallization, we sought out commercial NiCr resistors that could be used as load standards in this type of calibration.

We present the SOLR calibration standards that were used to measure microstrip flex cables. In the next section, we discuss the different standards that were implemented on edge launch connectors, compare their performance to Keysight standards at room temperature and compare two sets of standards to each other, in order to study the variation between each standard.

4.3.1 Calibration standards and procedures

A set of four calibration standards were assembled on Southwest Microwave edge launch connectors (short, open, and load). The set of standards are shown in Figure 4.17 and a representative thru is shown in Figure 4.18. A close-up microscopy image of the nichrome (NiCr) resistor shown in Figure 4.19. Southwest Microwave SMA connectors were chosen for this work because they have an adjustable grounding plate and the smallest signal pin diameter (0.005 inch) commercially available that we are aware of. These two properties made interfacing to thin (50 μm and less) microwave flex cables possible.

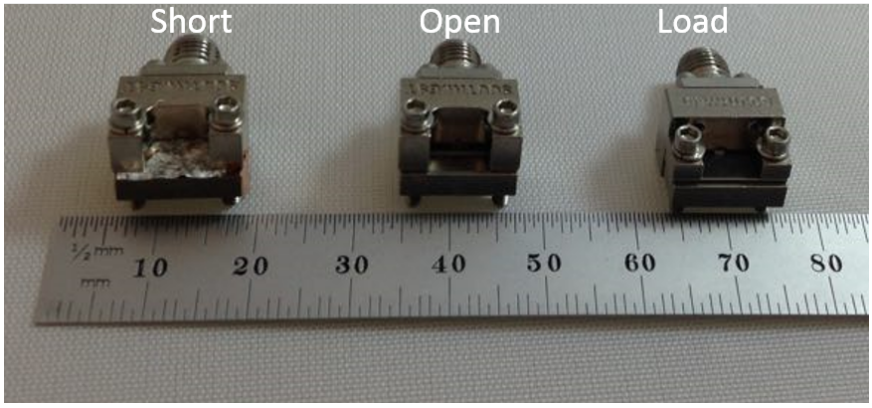

Figure 4.17: A representative set of calibration standards assembled on Southwest Microwave edge launch connectors.

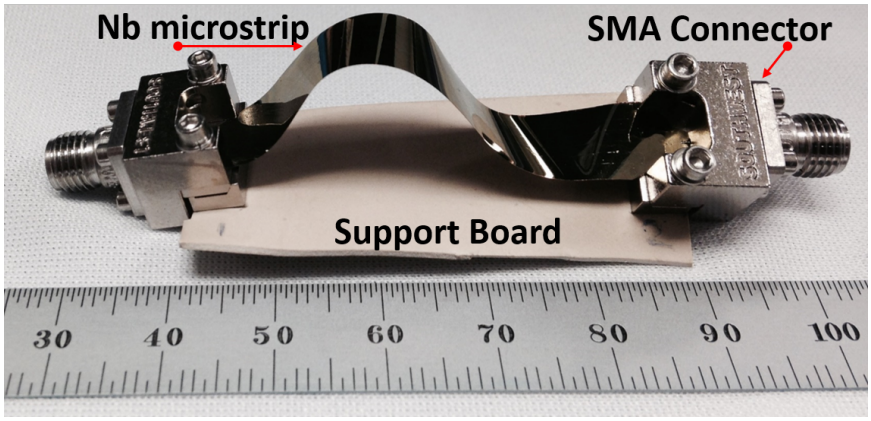

Figure 4.18: A representative ∼25 cm long microstrip line as a thru standard.

4.3.2 Measurement of calibration standards at room temperature

An 85052D calibration kit was used to perform a one-port calibration to set the calibration plane at the end of a short SMA cable, standards were then connected to the SMA cable and their response was measured. The purpose was to determine how two of the same standards assembled at different times would vary. The open standard is shown in Figure 4.20, with a variation of 0.2 db near 8-10 GHz band, but for the most part, symmetric across every other frequency range. The short standard was measured in the same method and the measurement results are shown in Figure 4.21. We note a difference in the short standard of ∼0.1 db above 6 GHz, but we believe this deviation was acceptable. The load standard measurements are shown in Figure 4.22, we note a deviation of ∼5 dB, but both standards

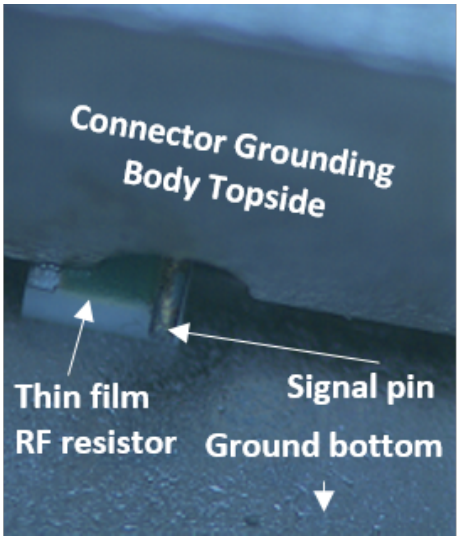

Figure 4.19: Close-up view of a thin-film NiCr chip resistor.

are significantly below -20 dB across the frequency range. We can conclude from these measurements that standards are fairly consistent across the frequency range of interest (10 MHz to 14 GHz).

For comparison, we also measured the 85052D calibration standards without performing a calibration to compare the RF performance in the same frequency range to our in-house assembled standard. Although this method is less accurate since it includes the cable losses and internal network analyzer errors, we can state the instrument and cable errors are fairly constant and therefore the standards are close. From the uncalibrated measurements, shown in Figures 4.23-4.25, we can conclude the standards are comparable to the 85052D calibration standards at room temperature.

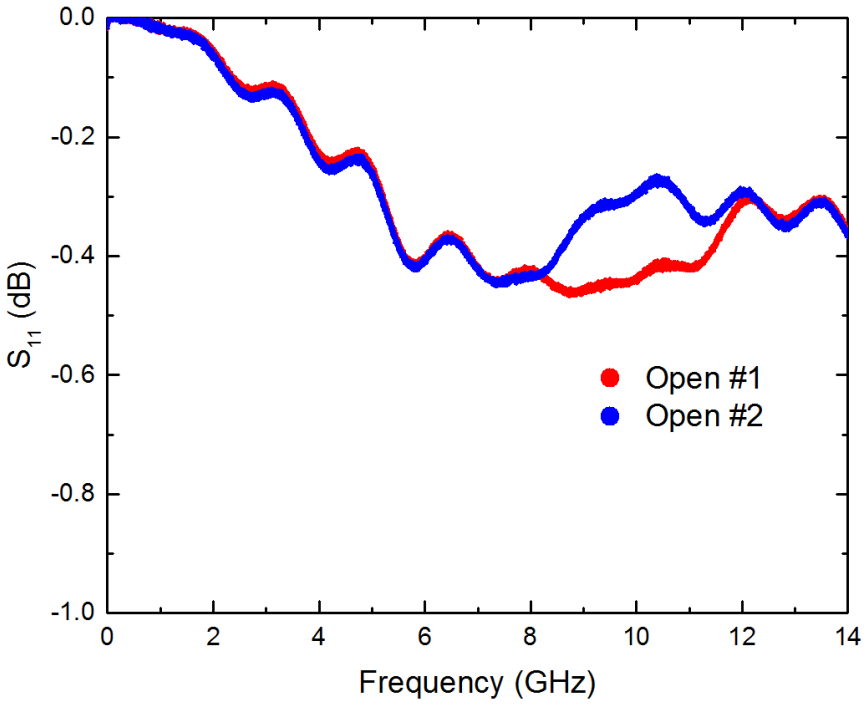

Figure 4.20: S_{11} measurement for two open standards assembled on edge launch connectors.

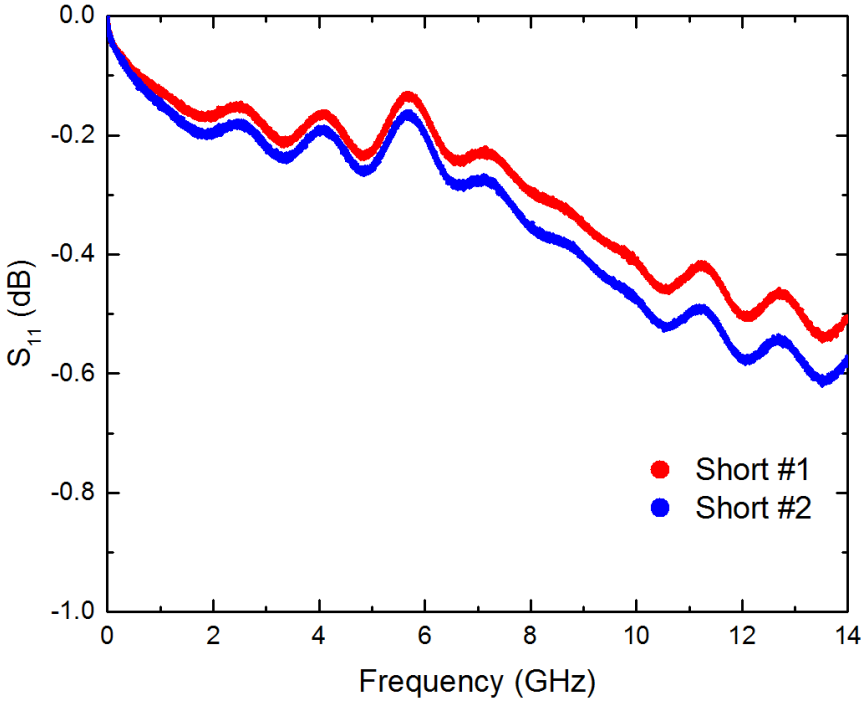

Figure 4.21: S_{11} measurement for two short standards assembled on edge launch connectors.

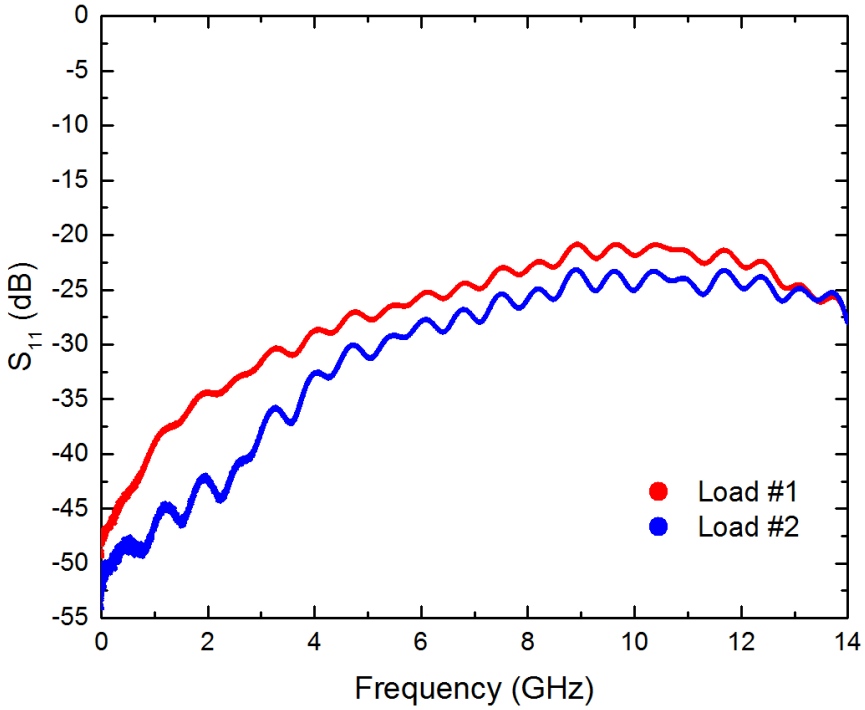

Figure 4.22: S_{11} measurement for two load standards assembled on edge launch connectors.

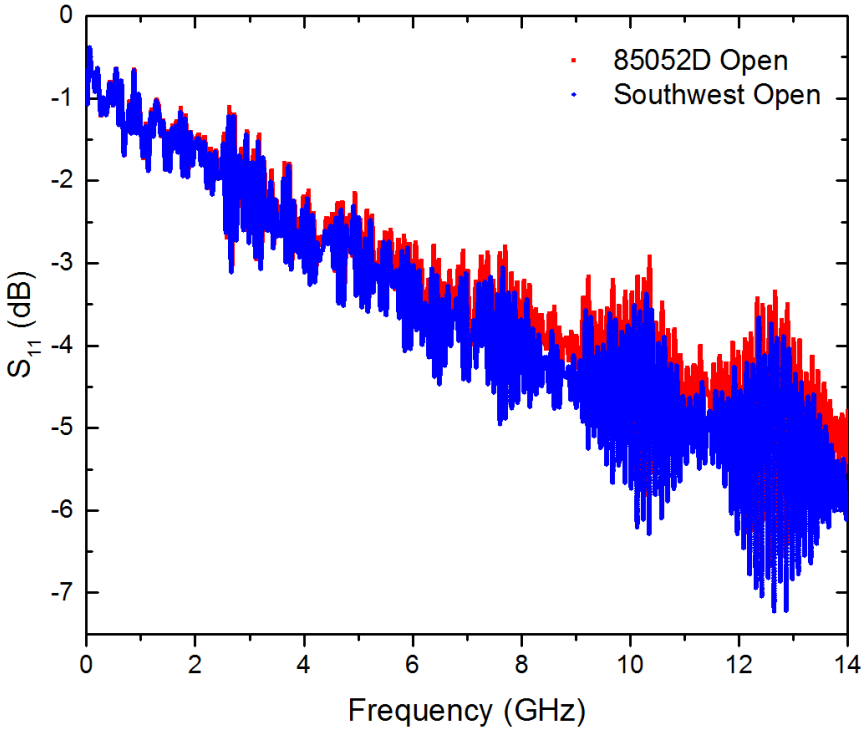

Figure 4.23: S_{11} measurement of a open standard assembled on an edge launch connector and a 85052D open standard for comparison.

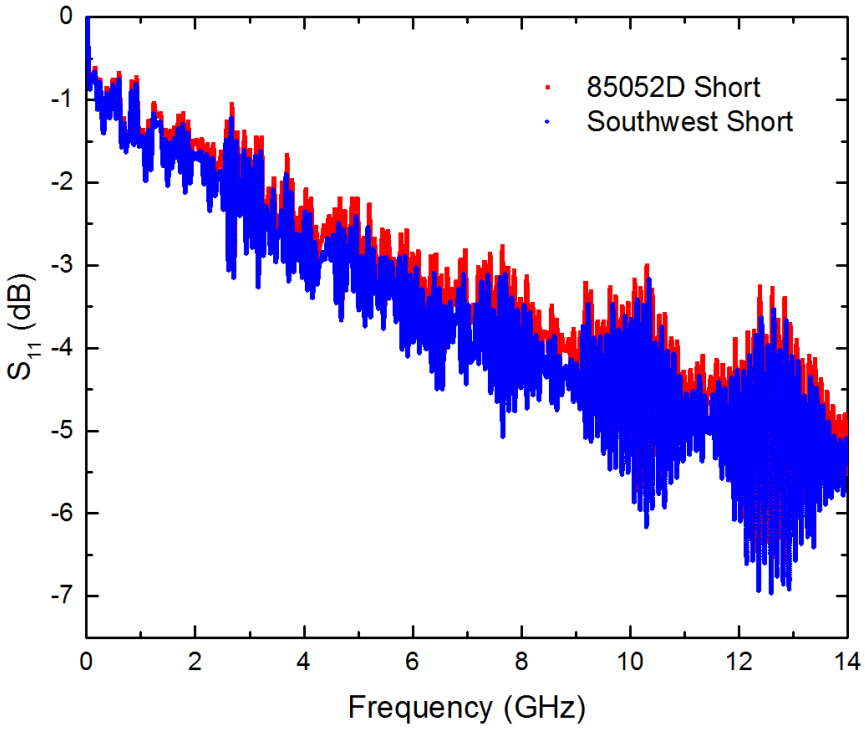

Figure 4.24: S_{11} measurement of a short standard assembled on an edge launch connector and a 85052D short standard for comparison.

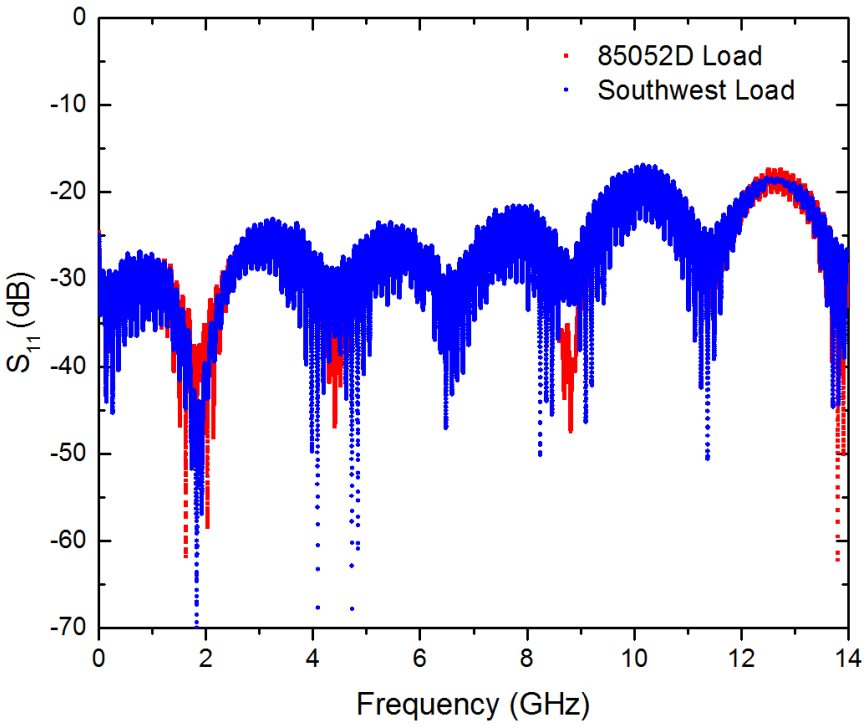

Figure 4.25: S_{11} measurement of a load standard assembled on an edge launch connectors and a 85052D load standard for comparison.

4.3.3 Cryogenic calibration process in liquid He

The cryogenic calibration process in liquid He (LHe) consists of a test fixture that minimized the cable and sample movement. The rod used for calibration in the Dewar is shown in Figure 4.26 with a microstrip sample connected to the end of each SMA cable. The top of the rod is shown in Figure 4.27, which highlights the SMA connectors with 90 degree bend adapters and a Teflon Dewar cap. The Teflon cap isolates each of the SMA connectors, which allows us to measure the signal and ground resistance. The calibration process consisted of loading the appropriate standard onto the end of the SMA cables and cooling the standard in liquid nitrogen (LN_2) Dewar. After the rod, SMA cables and the standards were themallized, we transferred the rod into a liquid He Dewar. After the standard was measured in liquid He, the fixture was heated and brought up to room temperature, before the next standard was connected.

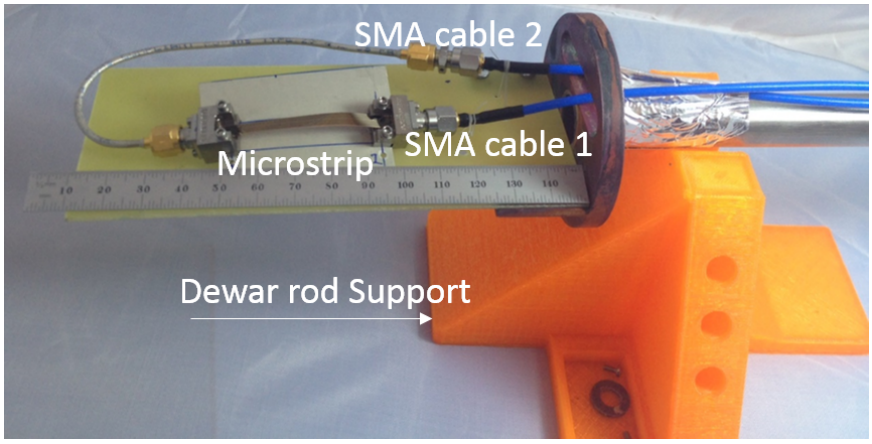

Figure 4.26: A rod for mounting samples in a Dewar with a microstrip sample mounted for testing.

4.3.4 Assembly of calibration standards

For the SOLR calibration, we require an open, a short, a load and the sample as the thru. A short standard was made by soldering with Indium a thin copper foil directly onto the SMA connector signal pin. The two wire resistance measurement of the short was measured

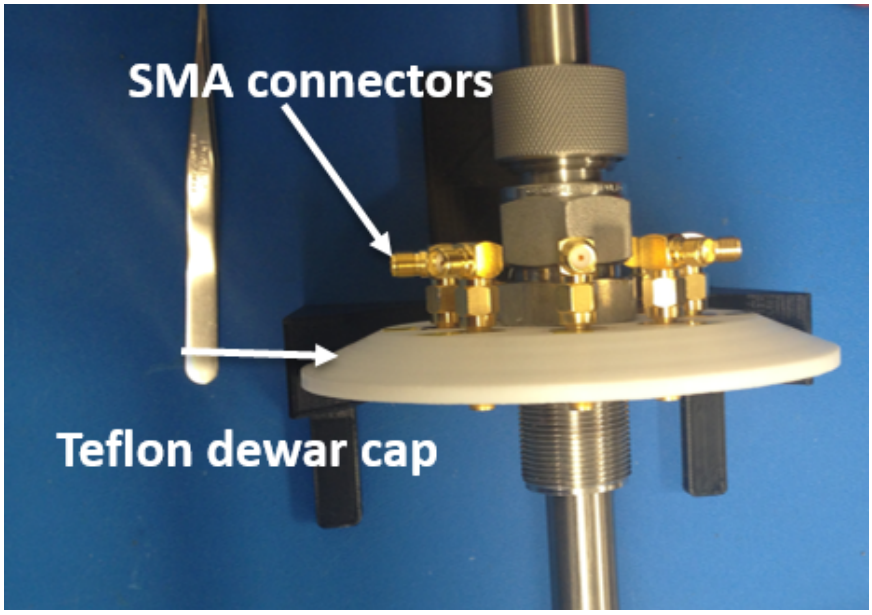

Figure 4.27: Topside of the rod with SMA connectors shown.

to be ∼0.5 Ω at room temperature and ∼0.2 Ω at 4.2 K. For the open standard, we removed the adjustable grounding plate of the SMA connector to prevent shorting the signal pin to grounding wall. For the load standard, we used a 50 Ω NiCr resistor from Vishay[4]. The NiCr resistor that was ordered had two contact pads that were pre-tinned with solder, one pad of the resistor was aligned to the signal pin of the connector and the other pad made contact to the grounding wall. The assembly was reflowed in a oven to ensure a good solder contact. We verified the resistance of the NiCr did not deviate more than 1 percent from room temperature at DC to 4.2 K in a pulse-tube cryostat by a two-wire measurement. The two-wire resistance measurement results are shown in Figure 4.28.

[4]Part # FC0402E50R0BTBT1

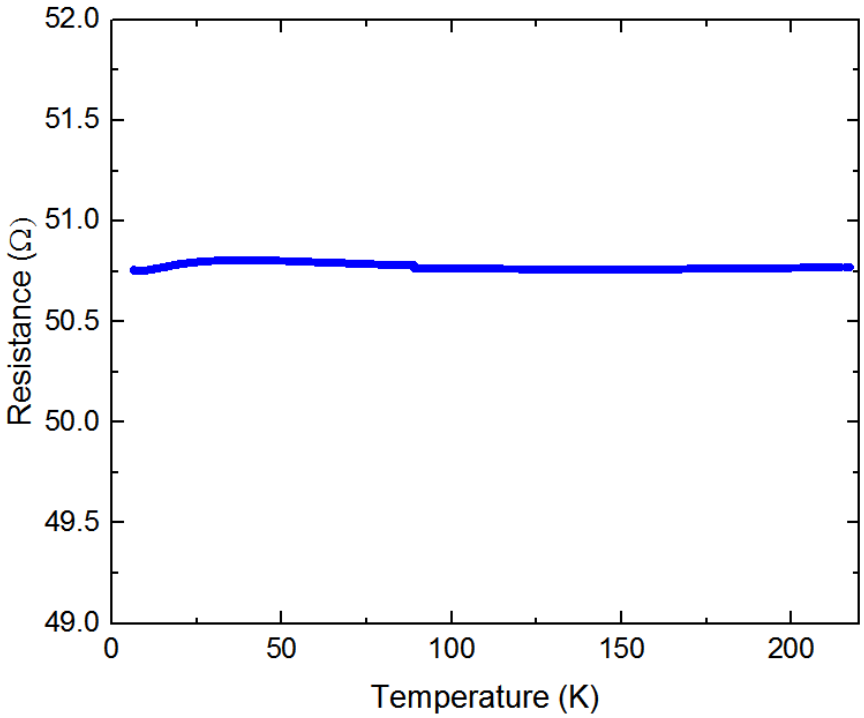

Figure 4.28: Representative resistance vs. temperature measurement of the thin film NiCr resistor using a two wire measurement setup.

Chapter 5

Results and Discussion

In this chapter we present the RF measurements and modeling results of microstrip transmission lines on Kapton and PI-2611. This chapter begins with an introduction to the simulation models that were implemented in Keysight ADS using the circuit model toolkit. A discussion of the impact of kinetic inductance on the RF performance of these transmission lines. is then presented. We then present the measurement results for a Ti/Nb and Ti/Cu microstrip lines on Kapton [54]. Due to concerns that the Ti under layer might have introduced additional RF loss, we also fabricated, measured, and fit a model to a Nb microstrip transmission line that omitted the Ti under layer.

The measurement results of microstrip transmission lines on PI-2611 are presented. This spin-on dielectric was used to fabricate transmission lines of various lengths. With this dielectric we studied metallizations that included Ti/Nb, Nb-only, Nb/Cu, and Nb/Al microstrip lines. Metallization such as Nb/Cu and Nb/Al were of interest as previous research has shown these metals can improve the mechanical reliability of Nb [55–58]. DC measurements in our research group of Nb with various cladded meallization have indicated a minimal impact on the T_c of Nb [59], while resonator measurements indicated that the addition of a normal metal introduce additional RF loss, until this metal was proximitized with the Nb [60] at $\sim$1.2 K. Although the extent of the proximity into the normal metal was dependant on the thickness.

Based on the T_c measurements results of Nb with a dielectric cover from [59], we were able to experimentally determine a dielectric curing temperature that was compatible with our Nb metallization. We therefore present preliminary measurements of an embedded Nb microstrip transmission lines that had a $\sim$10 μm dielectric cover.

This chapter concludes with a discussion of the impact of excess solder on the RF performance of these transmission lines. All of the RF measurements that are presented in this chapter were performed in liquid helium after performing an SOLR calibration [52]. We interfaced directly to these flex cables by end launch SMA connectors from Southwest Microwave. Two-wire DC resistance measurements of the transmission lines were undertaken in a pulse tube cryostat to confirm that the signal line and ground plane had fully transitioned to the superconducting state.

5.1 Simulation models

Microstrip transmission lines were modeled in Keysight ADS design tool using the built in circuit tool kit. A representative distributed element model for a Kapton microstrip implemented in ADS is shown in Figure 5.1. A transmission line can be divided into smaller subsections, as long as the length of the subsection is less than $\lambda/10$ at the highest simulation frequency [61]. In a microstrip, we used the effective dielectric constant (ϵ_{eff}) to calculate the guide wavelength (λ_g) at 14 GHz. The guide wavelength calculation is shown in Equation 5.1. The λ_g has to be used in the calculation because the fields are not completely enclosed in the dielectric. The effective dielectric constant in a microstrip was calculated from [36]. MLIN is a built-in microstrip element in ADS with a width (W_L) that was designed to give a 50 Ω characteristic impedance and with a length (L_L) that was less than $\lambda/10$. C_p was the parasitic capacitance due to excess solder. L_k was the kinetic inductance, which was incorporated as a series inductor. The kinetic inductance included both the signal and ground was lumped together and was iteratively fit through simulation.

$$\lambda_g = \frac{c}{f\sqrt{(\epsilon_{eff})}} \tag{5.1}$$

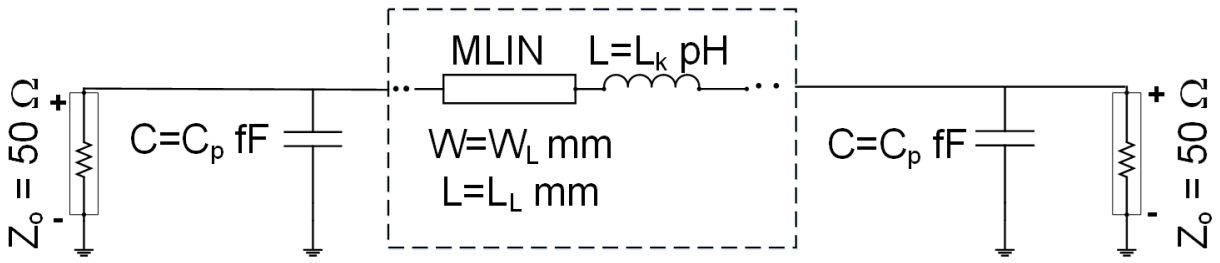

Figure 5.1: Distributed element model used in Keysight ADS schematic tool.

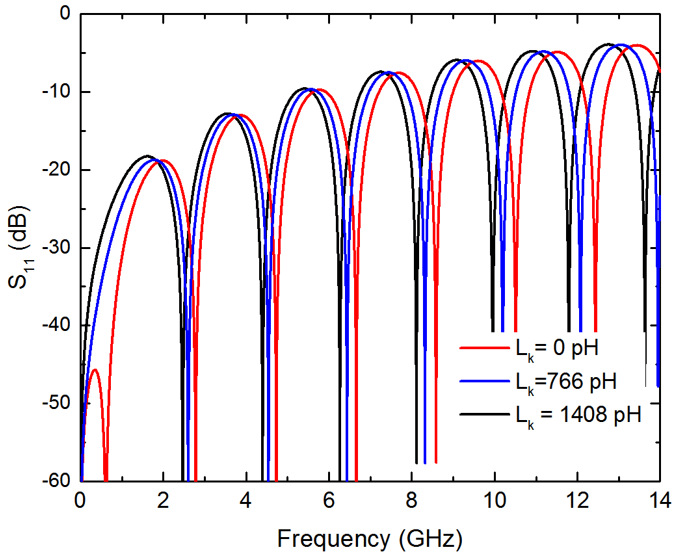

Figure 5.2: Simulation of a 5 cm long microstrip in ADS demonstrating the impact of kinetic inductance on S_{11}.

5.2 Kinetic inductance impact on the microwave performance

In the simulation models, we included an inductive element to account for the kinetic inductance of the Nb signal and ground. To obtain a better understanding of how the kinetic inductance impacted the S-parameter measurements, we simulated a 5 cm long microstrip on PI-2611 with the solder pads present. We swept the kinetic inductance from the ideal-case ($L_k = 0$) to a high kinetic inductance film ($L_k = 1408$ pH). Therefore, the impact on the reflection coefficient (S_{11}) was seen as a slightly longer transmission line, as shown in Figure 5.2. From the insertion loss (S_{21}) simulations shown in Figure 5.3, we note that as the kinetic inductance was increased, the peak loss was shifted to a lower frequency.

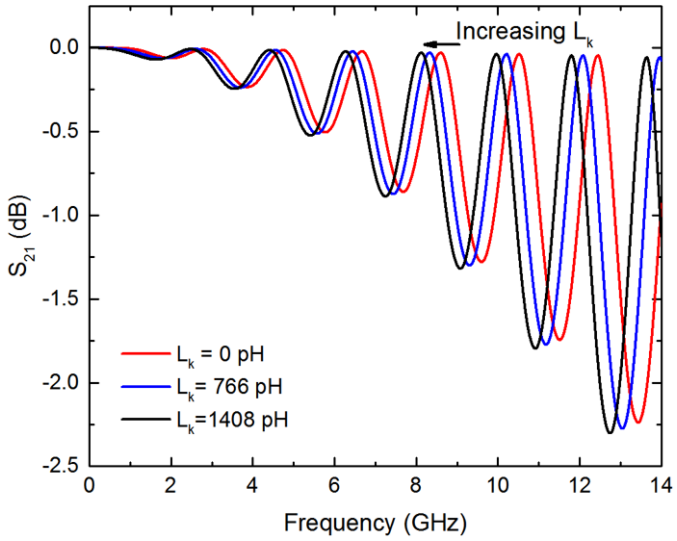

Figure 5.3: Simulation of a 5 cm long microstrip in ADS demonstrating the impact of kinetic inductance on S_{21}.

5.3 A 5 cm long Nb and Cu microstrip with a Ti adhesion layer on Kapton

We measured Nb and Cu microstrip lines with a 500 Å thick Ti adhesion layer on Kapton. We designed these transmission lines to have a 50 Ω characteristic impedance. Therefore a signal line width of 121 μm was determined to meet these requirements. We demonstrated less than 0.1 dB of intrinsic loss up to 14 GHz for the Ti/Nb microstrip. The copper transmission line exhibited ∼4.5 dB of loss.

DC measurements of both the signal and ground of the Ti/Nb microstrip were performed in a pulse tube (PT) cryostat to verify transition to the superconducting state by a two wire measurement setup. From the measurement results shown in Figure 5.4, we determined the transition temperature of both the signal and ground to be ∼7.0 K and ∼8.0 K, respectively. These T_c values were lower than bulk value of Nb, we attribute the decrease in T_c to surface imperfections in the Kapton film.

The simulation model used to match measurement is shown in Figure 5.5, for clarity only a portion of the circuit is shown. The RF measurement results and simulation results are shown in Figures 5.6 and 5.7. The measurement results indicate less than 1.0 dB of intrinsic loss on E-series Kapton up to 14 GHz with a reasonable match (S_{11}). A parasitic

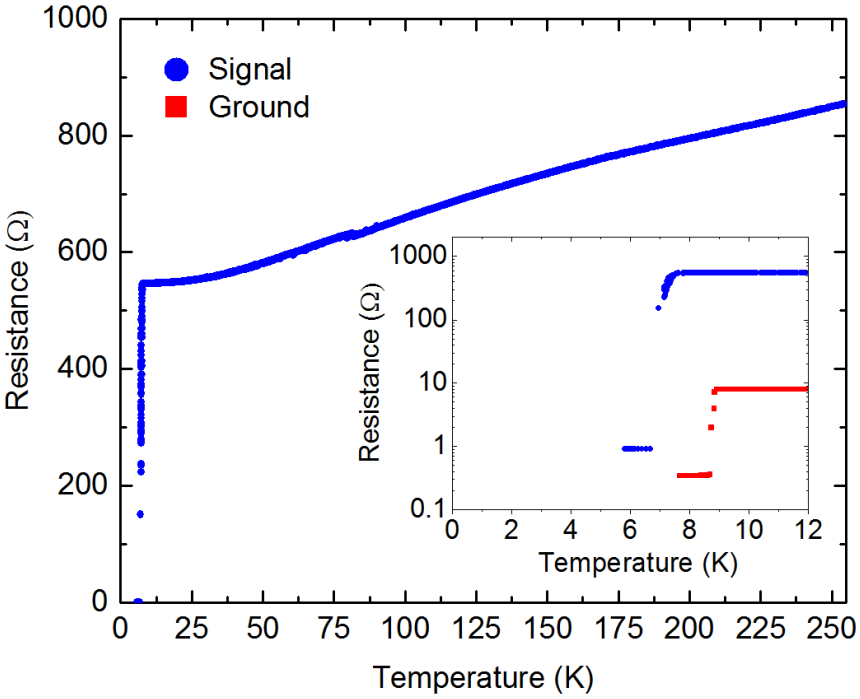

Figure 5.4: Temperature vs. resistance measurement of the signal trace and ground plane of a Ti/Nb microstrip on Kapton.

capacitance of 90 fF was added to the model in order to account for the depth of the dips in S_{21} and S_{12} in the measurement. We note that without the capacitors at each end, the peak loss matches measurement, as expected. The kinetic inductance was accounted for as a series of 366 inductive elements with each inductive element having a value of 0.130 pH (L_k) and each transmission line segment had a length of 0.136 mm (L_L) with 367 segments.

The dielectric properties incorporated into the simulation were obtained from Cu and Nb resonators that were fabricated on the same E-series Kapton film. The dielectric properties of the Kapton film was reported by [3] at 4.2 K to have a dielectric constant(ϵ_r) of 3.126 and a loss tangent ($\tan\,\delta$) of $1.167\times\ 10^{-3}$ at 14 GHz.

In Figure 5.8, we compared the insertion loss for Ti/Nb and Ti/Cu microstrip transmission lines. We conclude that there was a significant improvement in RF performance when using a Nb microstrip transmission when compared to normal-metal metallization under the same measurement conditions.

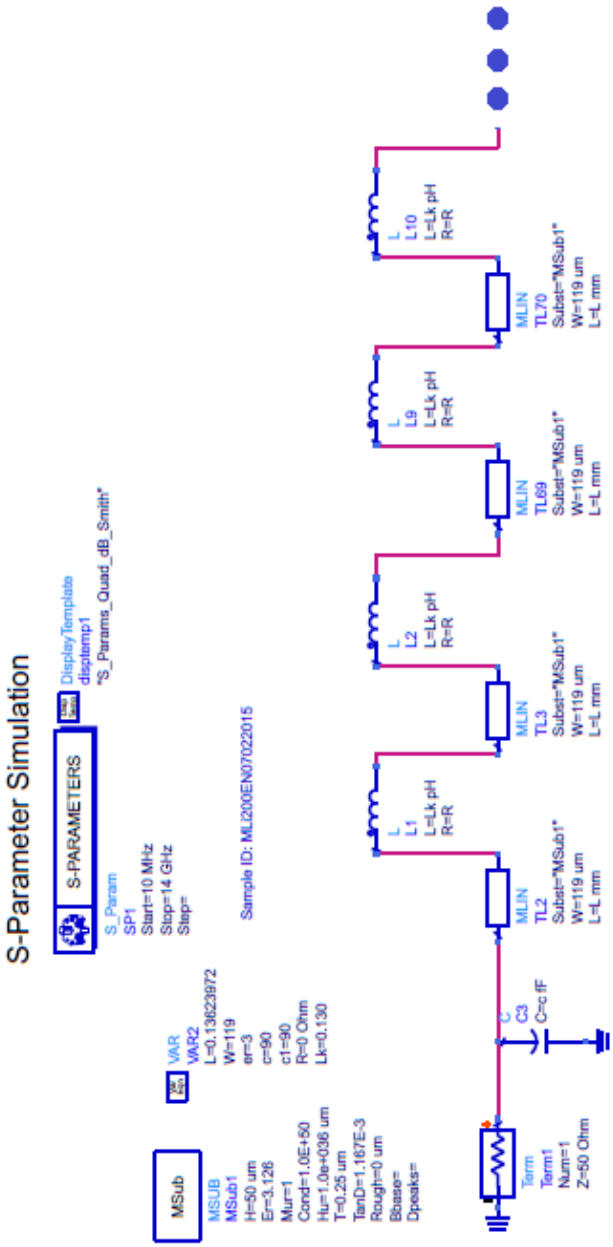

Figure 5.5: A Ti/Nb microstrip model on Tab-E Kapton implemented in ADS.

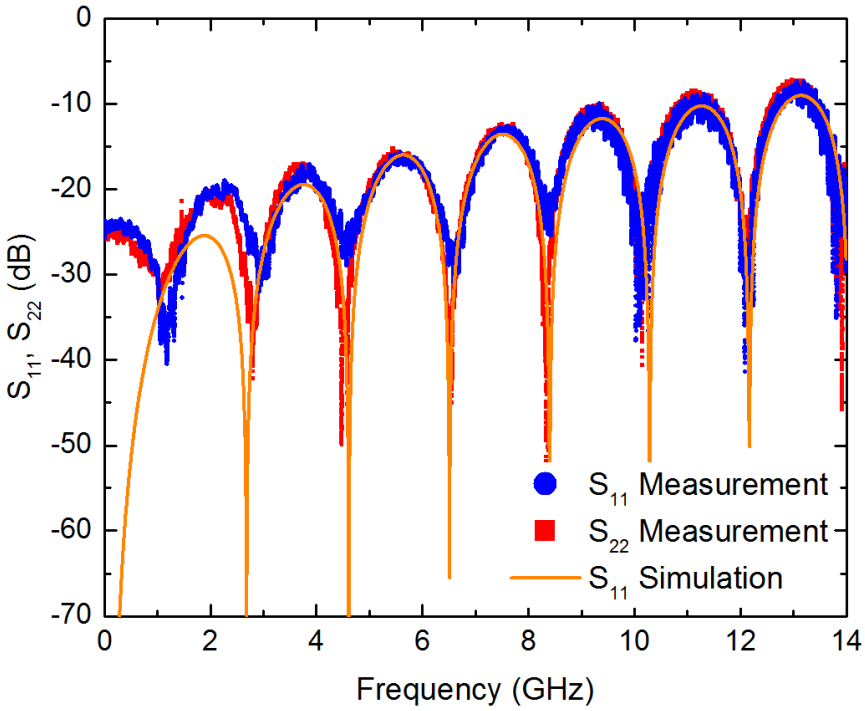

Figure 5.6: S_{11}, S_{22} measurements and simulation of a Ti/Nb microstrip on Kapton at 4.2 K.

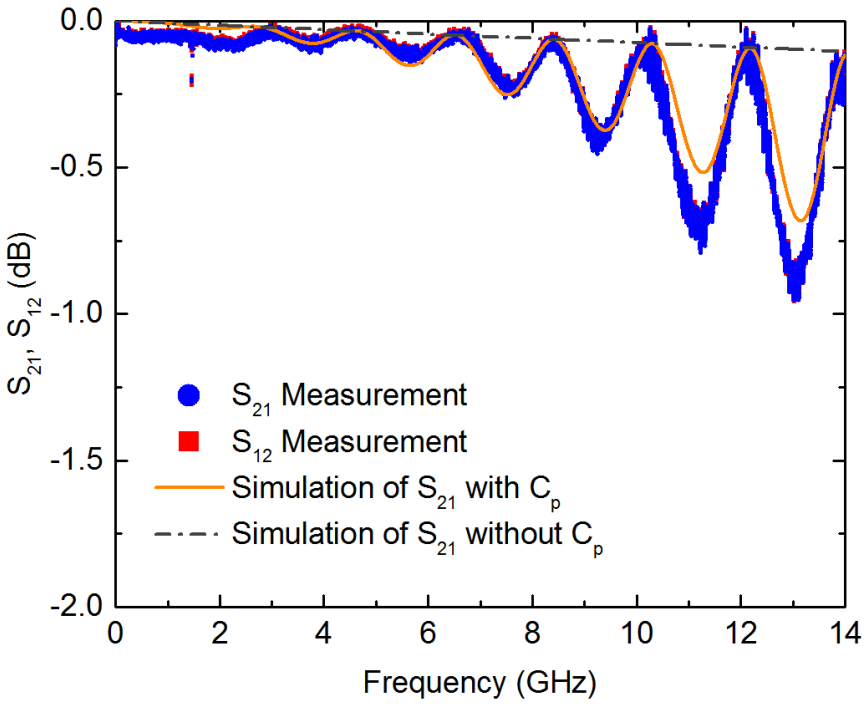

Figure 5.7: S_{12}, S_{21} measurements of a Ti/Nb microstrip on Kapton at 4.2 K.

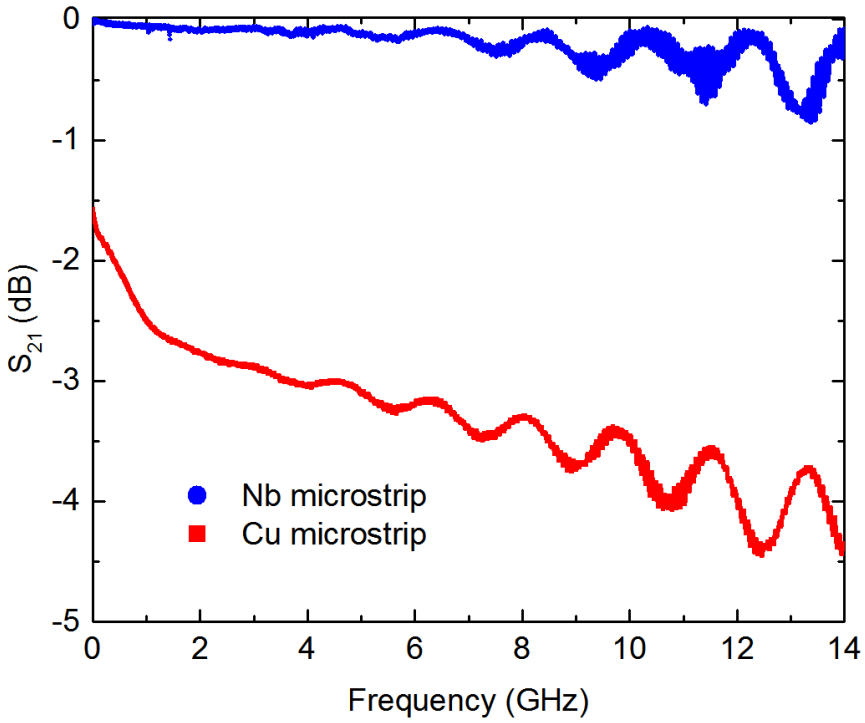

Figure 5.8: S_{21} measurement comparison of a Ti/Nb and Ti/Cu microstrip on Kapton.

5.4 A 5 cm long Nb microstrip on Kapton

Early in this work, we suspected that the 500 Å thick Ti layer might introduce additional RF loss in the microstrip transmission line. We therefore fabricated Nb only microstrip transmission lines on Kapton that omitted the Ti metallization. Process modifications were made to ensure adhesion of the Nb metallization onto the Kapton film. The simulation model that was used to fit to the measurement results is shown in Figure 5.9. The measurement results with simulation of the Nb microstrip are shown in Figures 5.10 and 5.11. We note that the Nb microstrip had less than -0.02 db intrinsic loss at the highest measurement frequency. We note that a 110 fF of capacitance was added to the model, due to excess solder. Overall, we saw an improvement in the intrinsic loss, although the excess solder had a larger negative impact on the RF performance.

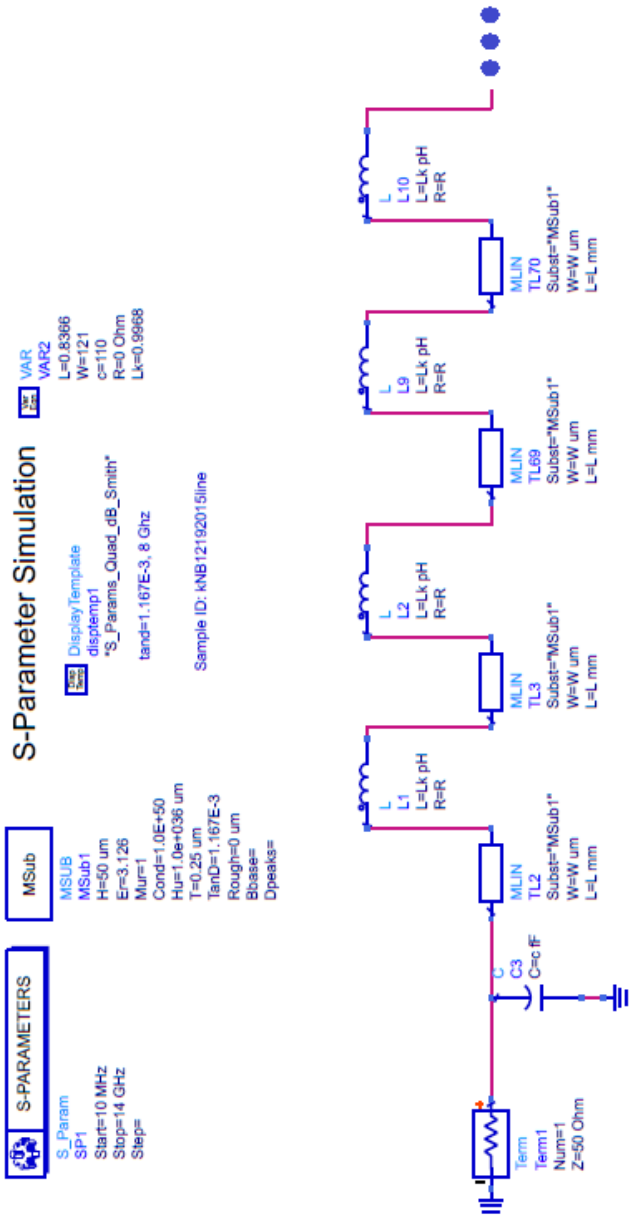

Figure 5.9: A 5 cm long Nb microstrip model on Kapton implemented in ADS.

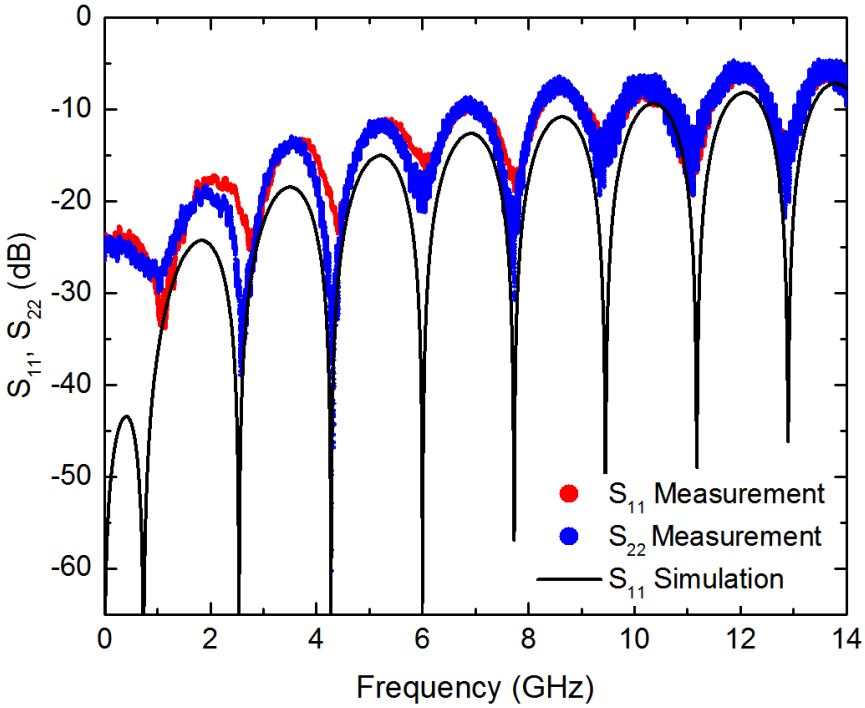

Figure 5.10: S_{11} and S_{22} measurement and simulation of a 5 cm long Nb microstrip on Kapton.

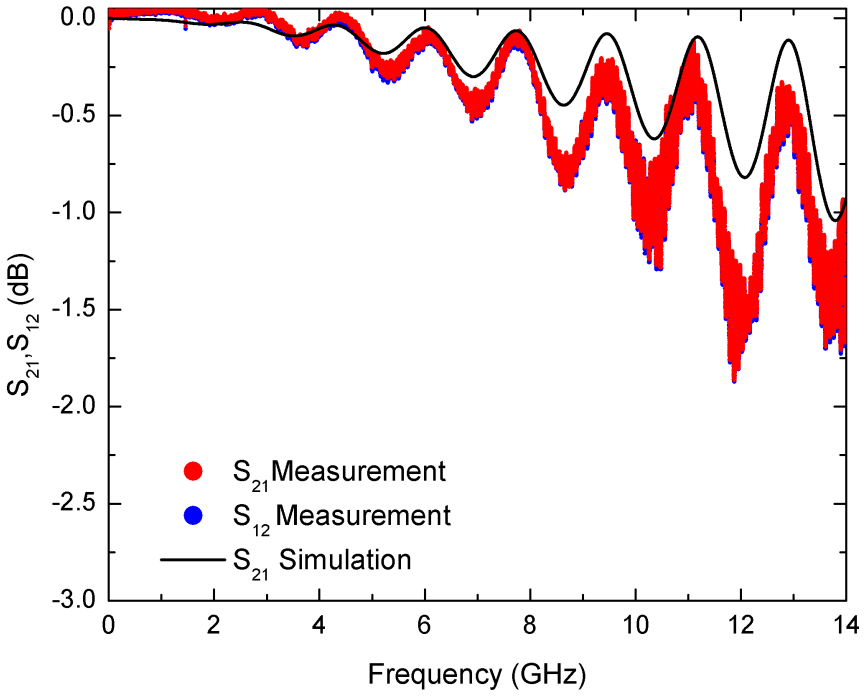

Figure 5.11: S_{21} and S_{12} measurement and simulation of a 5 cm long Nb microstrip on Kapton.

5.5 A 5 cm long Nb and Cu microstrip with a Ti adhesion layer on PI-2611

We present superconducting Ti/Nb microstrip and for comparison, a non-superconducting Ti/Cu microstrip, each with only 100 Å of Ti for adhesion, fabricated on HD MicroSystems PI-2611 film that was ∼20 μm thick. These samples were 2.5× thinner than the Kapton film and therefore the signal lines were significantly more narrow (∼46 μm) to match a 50 Ω impedance. Solder pads were included to be able to interface to the microstrip. What follows are the DC and RF measurement results of these transmission lines.

We studied the critical temperature (T_c) and current (I_c) of a Ti/Nb signal line with a width of 46 μm. Two wire DC measurements were performed using SMA cables that were interfaced with the Ti/Nb microstrip cable. To measure the T_c of the Ti/Nb line, we used a closed cycle pulse tube (PT) based cryostat with cryogenic cables that can reach temperatures down to ∼1.2 K. This measurement setup allowed us to determine the T_c of both the signal and ground plane. Resistance vs. temperature measurements for both the signal line and ground plane are shown in Figure 5.12. The T_c of the signal line and ground plane were measured as ∼7.0 K and 8.0 K, respectively. These DC measurements clearly indicate both the signal and ground plane became superconducting. Critical current measurements of the signal line were measured as a function of temperature and are shown in Figure 5.13. We note the critical current decreased as the temperature increased, this is general trend that is consistent with theory. As the temperature increases, there are less Cooper pairs to carry this current, if enough current is applied, the Cooper pairs are broken and a resistance is observed. At the lowest measurement of temperature of 3.5 K, we observed a critical current of ∼2.8 mA.

The RF circuit model implemented in ADS is shown in Figure 5.14. The transmission line was modeled as a series of transmission line elements (MLIN) with lengths of 0.732 mm. The kinetic inductance that was present in the Nb was fit in the simulation model with 65 inductive elements and the value of the kinetic inductance was iteratively found to be 779 pH by matching the location of the peaks in S_{21}. The kinetic inductance caused the location

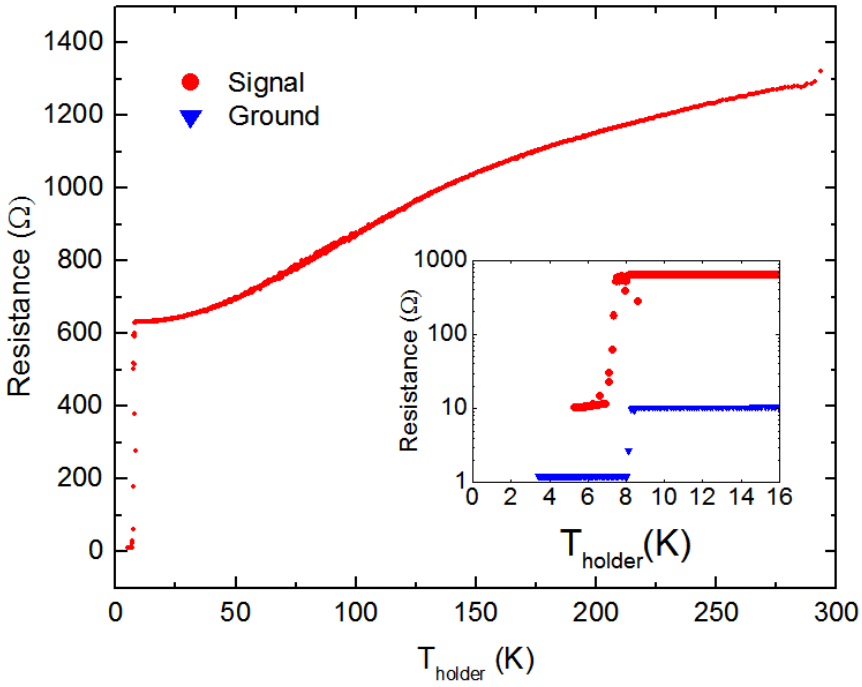

Figure 5.12: Representative two wire resistance vs. temperature measurement of the signal (red) and ground (blue) as the Ti/Nb microstrip cools down in the pulse tube based cryostat.

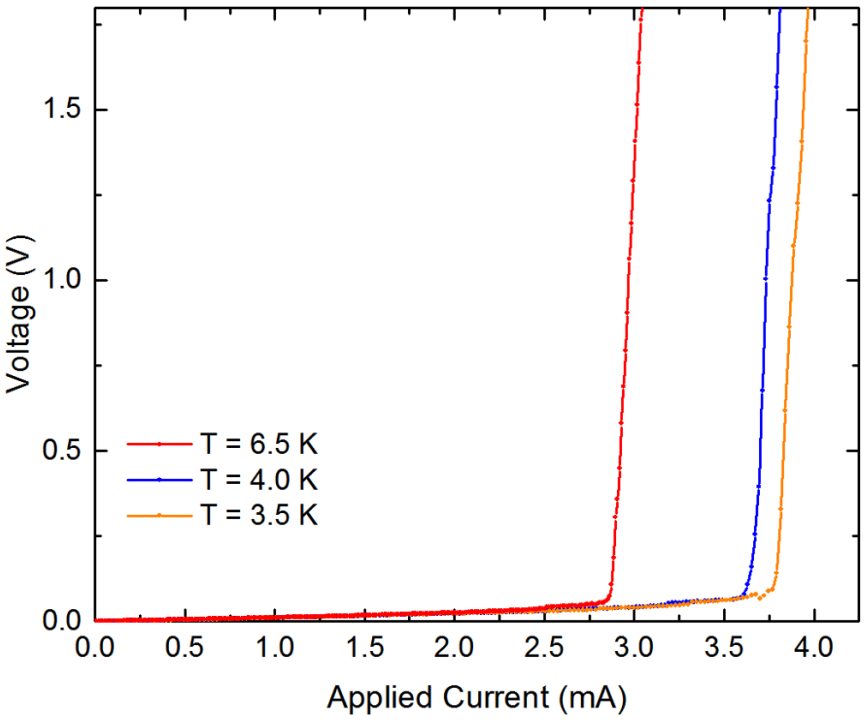

Figure 5.13: Critical current measurement of a Ti/Nb microstrip with a 46 μm wide signal line on PI-2611 as a function of temperature.

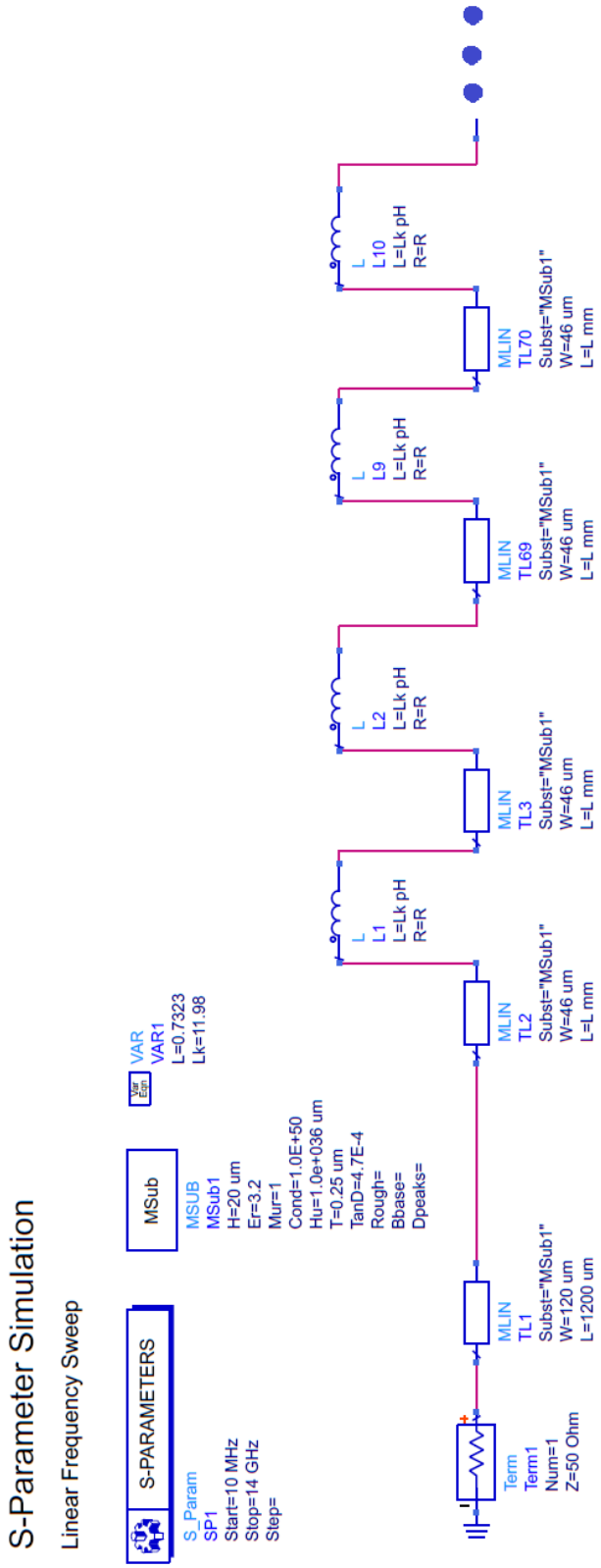

Figure 5.14: A 5 cm long Ti/Nb microstrip model on PI-2611 implemented in ADS.

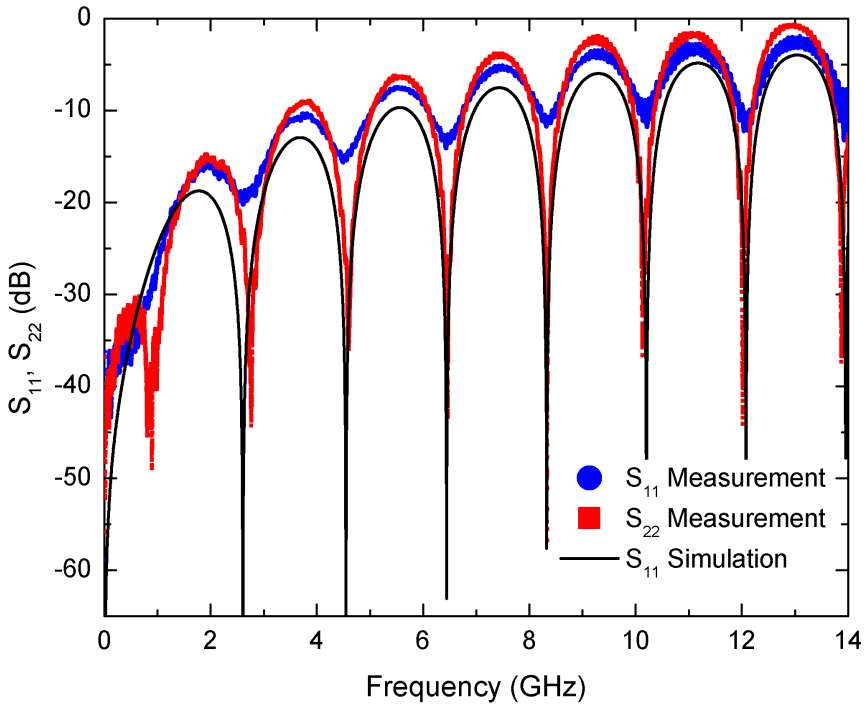

Figure 5.15: Measurement and simulation of S_{11} and S_{22} of a 5 cm long Ti/Nb microstrip on PI-2611 at 4.2 K.

of the peaks in S_{21} to be shifted towards a lower frequency. The dielectric properties of the PI-2611 that were included in the model, such as the loss tangent ($\tan\delta$) was measured by a Ti/Nb resonator that was in the same deposition run as the microstrip and the $\tan\delta$ was determined to be 4.7×10^{-4} at 14 GHz in liquid He [39]. The dielectric constant was measured with a Cu resonator in the frequency range of 2-14 GHz and a broadband fit was used to determine a dielectric constant of 3.2 in ADS schematic tool to avoid the influence of the kinetic inductance.

The measurement results and simulation are shown in Figures 5.15 and 5.16. From the S_{11} measurements, below 5 GHz, we see a fairly good match (S_{11}) that is below -10 dB. At higher frequencies, we attribute this mismatch to the solder pads and excess solder. The excess solder was modeled as an additional parasitic capacitance. Simulations that show a match to the insertion loss (S_{21}) measurement is shown in Figure 5.16.

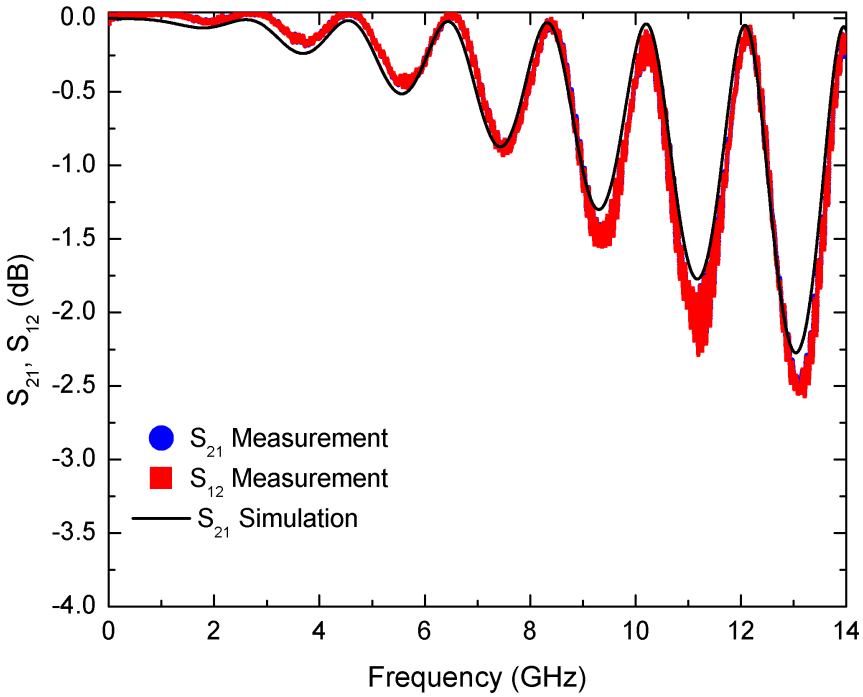

Figure 5.16: Measurement and simulation of S_{21} and S_{12} of a 5 cm long Ti/Nb microstrip at 4.2 K on PI-2611.

To demonstrate the advantage of using superconducting metal on a thin-film dielectric, we compared a similarly construed microstrip transmission line comprised of Ti/Cu on PI-2611 with the same dimensions. The microstrip sample was measured in liquid He at 4.2 K. The simulation model is shown in Figure 5.17. The excess solder was modeled as a solder pad with a width of 260 μm (compared to 120 μm), which was an increase of 140 μm (not unreasonable for a hand soldered connection). The measurement results and simulation fit are shown in Figure 5.18 and 5.19. We see a fairly good agreement to measurement. We then compared the insertion loss measurement (S_{21}) of the Cu microstrip to the Nb microstrip, as shown in Figure 5.20. We note a significant improvement in loss when using Nb. From the S_{21} measurements of the microstrip lines, we note significantly higher loss for the Ti/Cu lines with same metal thickness and line width as the Ti/Nb microstrip.

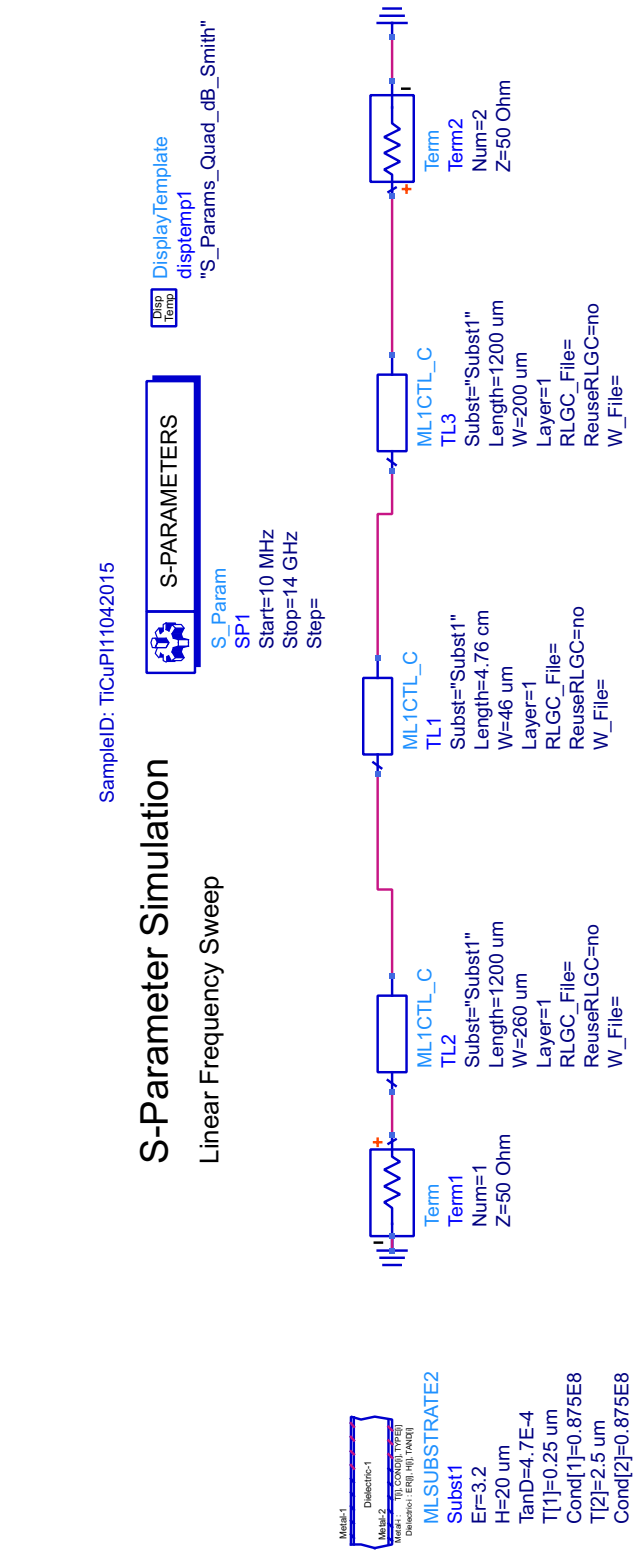

Figure 5.17: A 5 cm long Ti/Cu microstrip model on PI-2611 implemented in ADS.

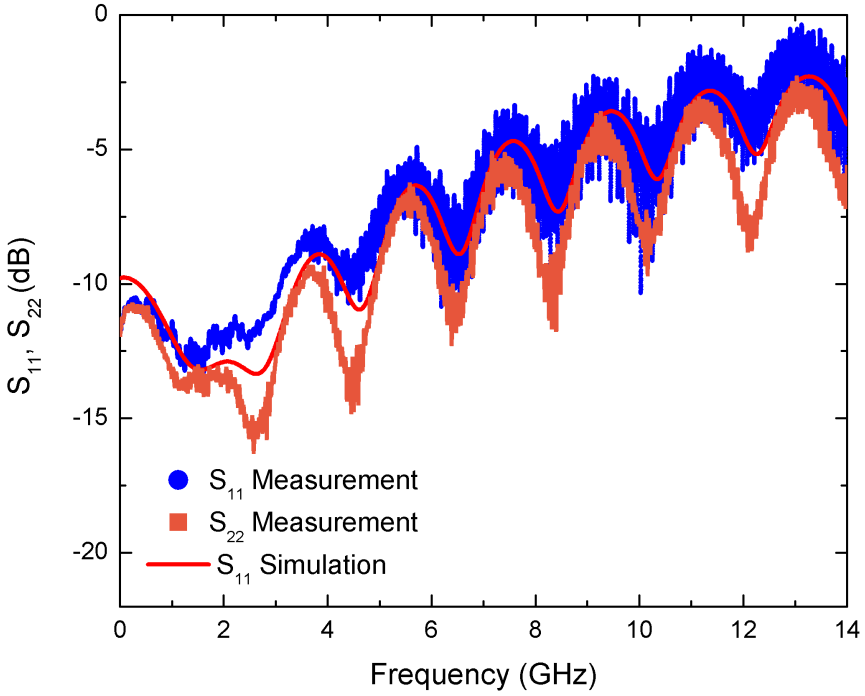

Figure 5.18: S_{11}, S_{22} measurement of a 5 cm long Ti/Cu microstrip on PI-2611 with simulation fit to S_{11}.

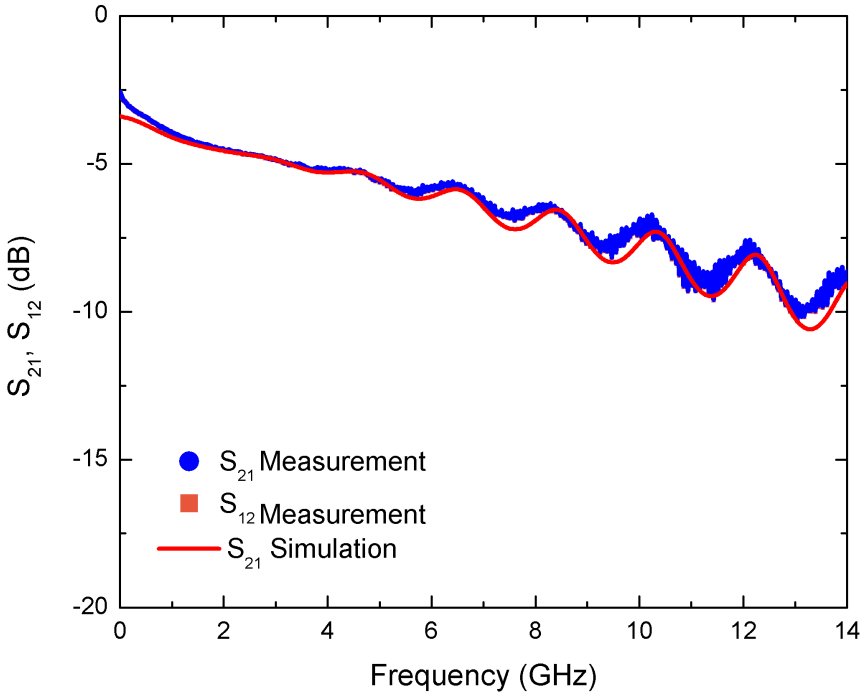

Figure 5.19: S_{21}, S_{12} measurement of a 5 cm long Ti/Cu microstrip on PI-2611 at 4.2 K with simulation fit to S_{21}.

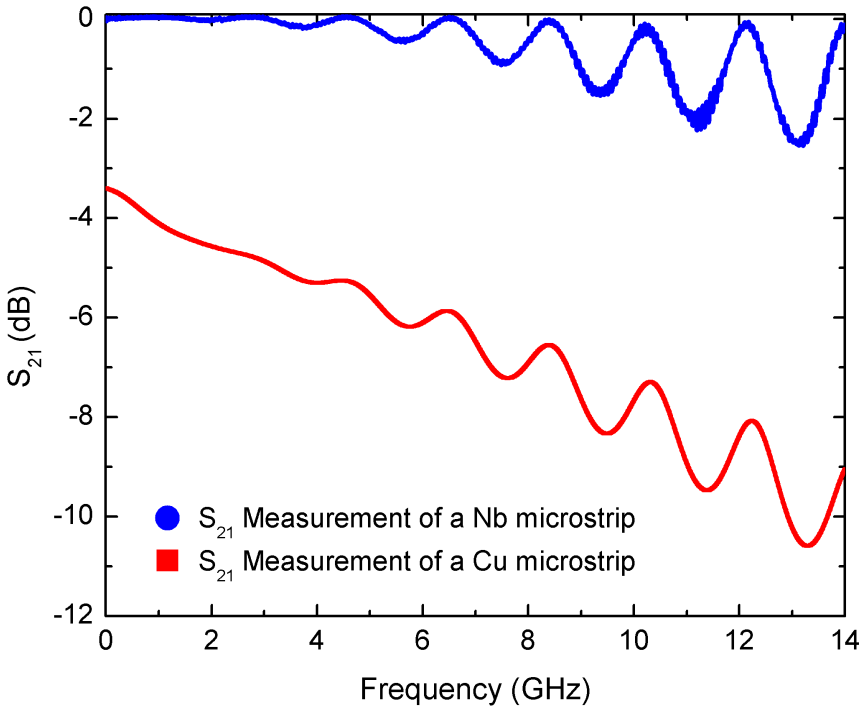

Figure 5.20: S_{21} measurement comparison of a Ti/Cu and Ti/Nb microstrip at 4.2 K.

5.6 A 25 cm long Nb microstrip on PI-2611

A meandered 25 cm long Nb microstrip line was fabricated on PI-2611 and measured in liquid He. The simulation model is shown in Figure 5.21. The measurement results and simulation are shown in the Figures 5.22 and 5.23. We note a few interesting results of this measurement. Foremost, the match is less than -10 dB below 4 GHz and at higher frequencies, we see the mismatches due to the solder pads and excess solder. The peak-loss of the transmission line (from simulation) is significantly less even at these lengths. The dominate loss mechanism was due to excess solder used to make contact to the edge launch connectors.

5.7 A 55 cm long Nb/Cu microstrip on PI-2611

Cladded Nb/Cu microstrip transmission lines were studied to protect the Nb signal trace. For this work, we studied a 200 nm thick Cu layer on a 250 nm Nb signal transmission

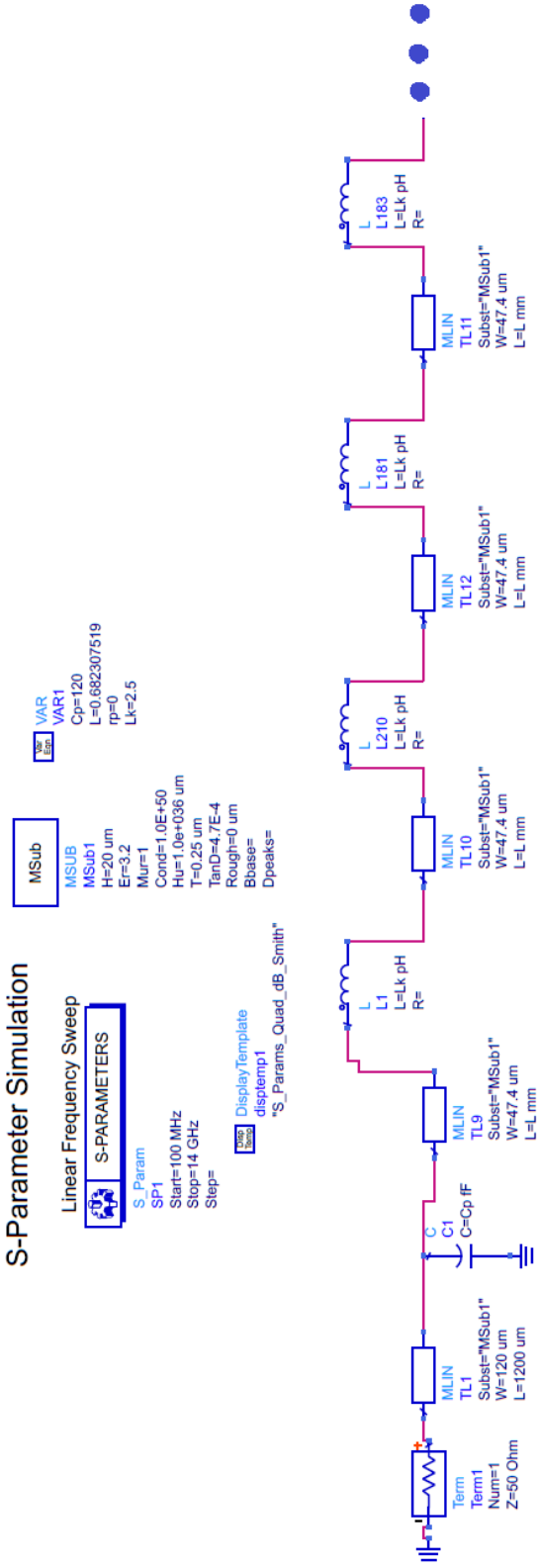

Figure 5.21: A 25 cm long Nb microstrip model on PI-2611 implemented in ADS.

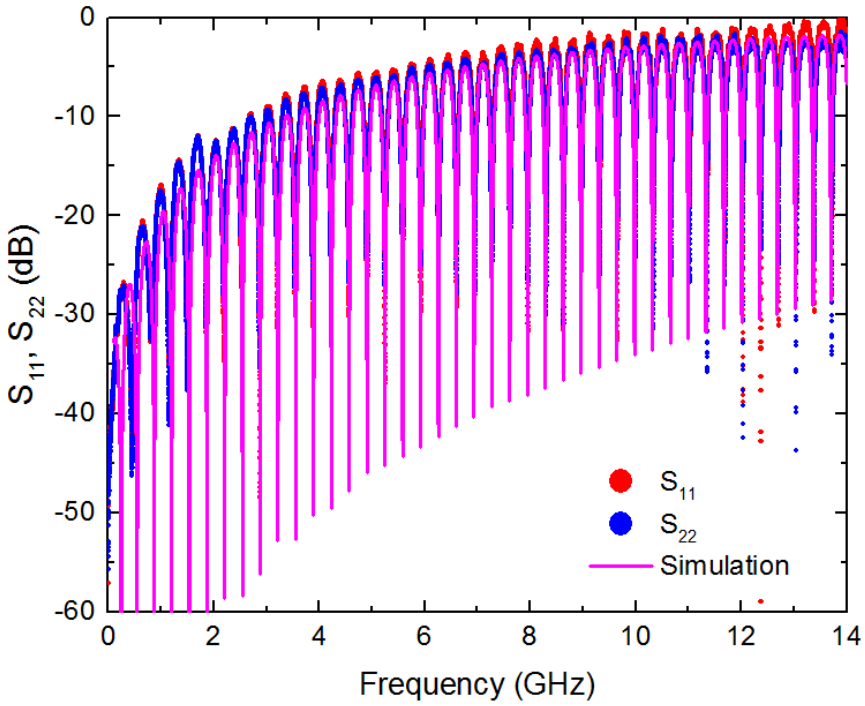

Figure 5.22: S_{11} and S_{22} measurements and simulation of a ∼25 cm long Nb microstrip on PI-2611 at 4.2 K.

line. Meanwhile, the ground plane was deposited with Nb only. This was done purposefully to ensure the loss contribution was primarily from the signal line. The results are shown in Figures 5.24 and 5.25. Superconductors with a normal metal layer is not a fundamentally new idea. Significant research at what occurs at this interface has been previously under taken by many researchers [62–64]. To our knowledge, cladded Nb microstrip transmission lines have not been previously reported. At present, simulation models to fit the data have not been developed and are the focus of future work. None the less, we report early measurement results of a 200 nm Cu cladded Nb microstrip. We note the S-parameter measurements of S_{11} and S_{22} have a significant mismatch between the two ends. We attribute this to uneven solder at each end of the microstrip transmission line. The insertion loss measurements (S_{21}) clearly show an additional loss with oscillations of the solder capacitance shadowed by the loss of the Cu. More experimental work would need to be studied in order to correlate the copper thickness to the impact on loss of the transmission line samples.

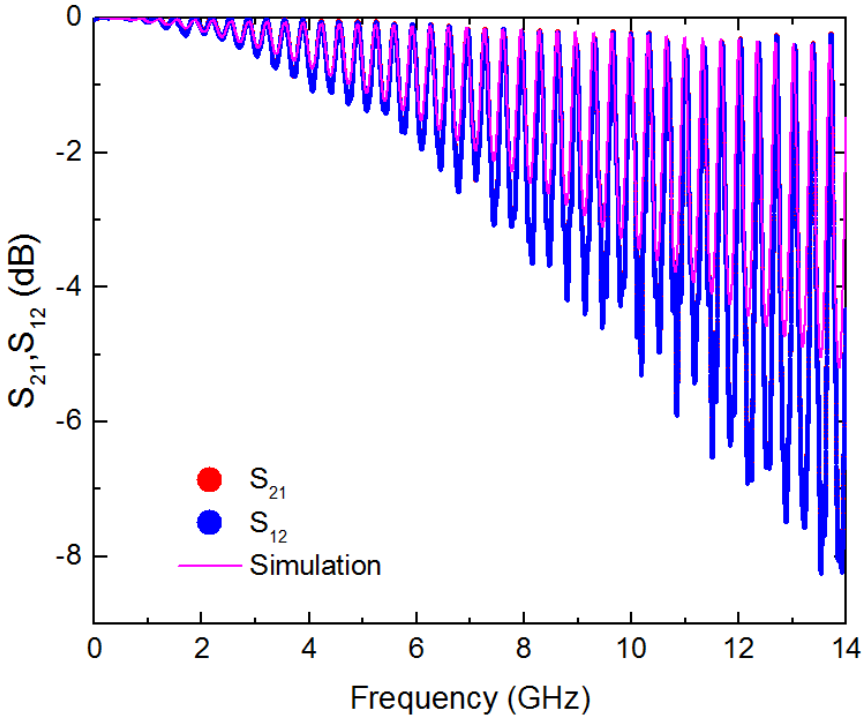

Figure 5.23: Measurement and simulation of S_{12} and S_{21} of a ~25 cm long Nb microstrip on PI-2611 4.2 K.

5.8 A 15 cm long Nb/Al microstrip on PI-2611

Nb with a 20 nm thick Al metallization was also studied. Like the Cu metallization, the Al layer was used to protect the underlying Nb from mechanical fatigue and from surface oxidation. Unlike Cu, Al can become superconducting at temperatures below 1.2 K. Therefore, the aluminum can help the Nb thermalize at higher temperatures (above 1.2 K). At temperatures below 1.2 K, the Al would become superconducting and the flex cable would be dominated by the losses in the excess solder and interface pad. The measurement results at 4.2 K are shown in Figures 5.26 and 5.27. We note the 15 cm long line, the peak loss is nearly lossless at the lowest frequency range of 10 MHz to ~4 GHz, above that we note the decrease in S_{21} with a peak loss at 14 GHz of ~2.0 dB. More work would be required to correlate the additional loss introduced by Al metallization.

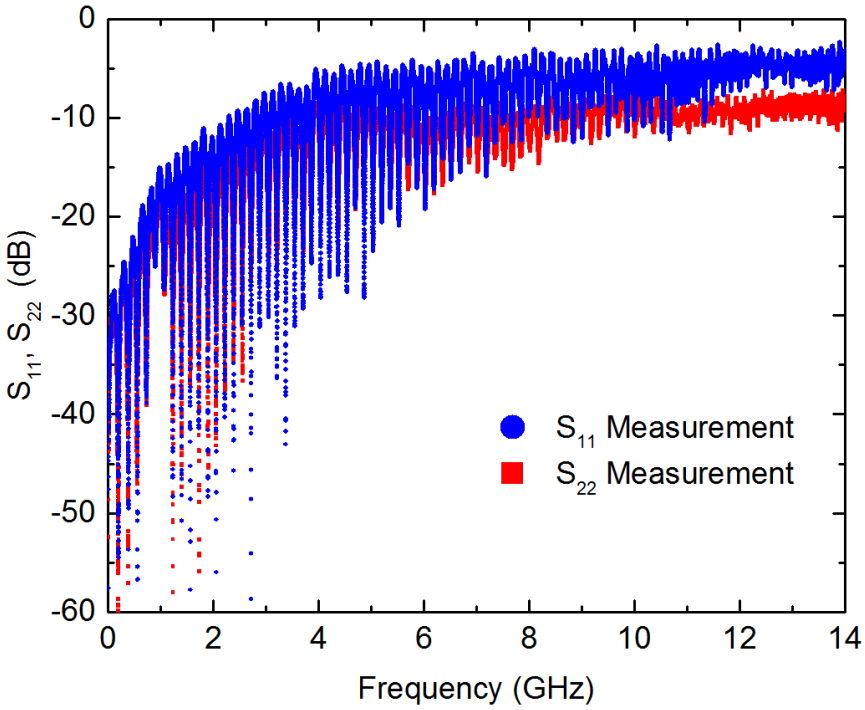

Figure 5.24: S_{11} and S_{22} measurement of a Nb/Cu microstrip transmission line measured at 4.2 K.

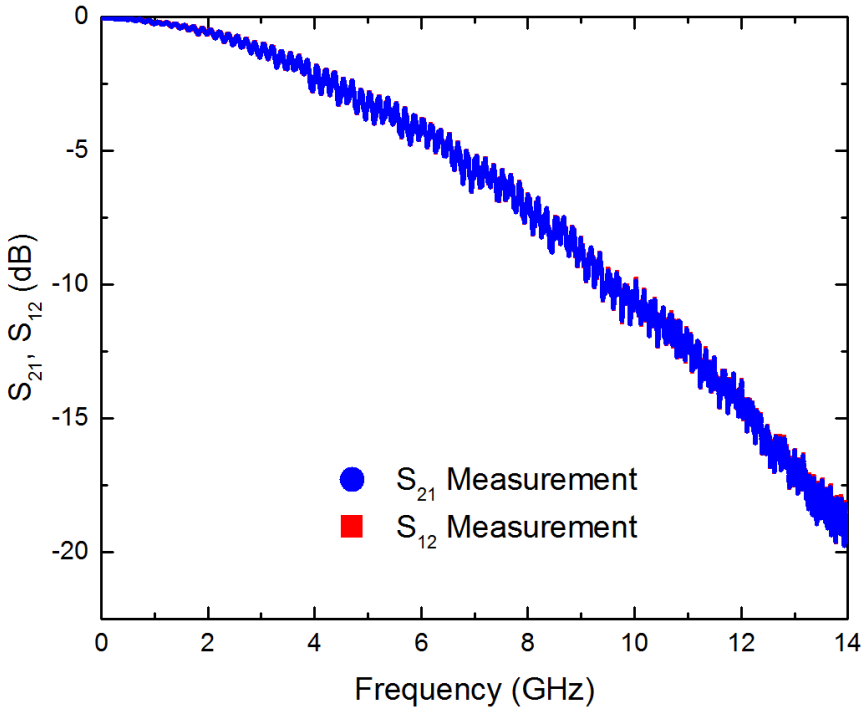

Figure 5.25: S_{21} and S_{12} measurement of a Nb/Cu microstrip transmission line measured at 4.2 K.

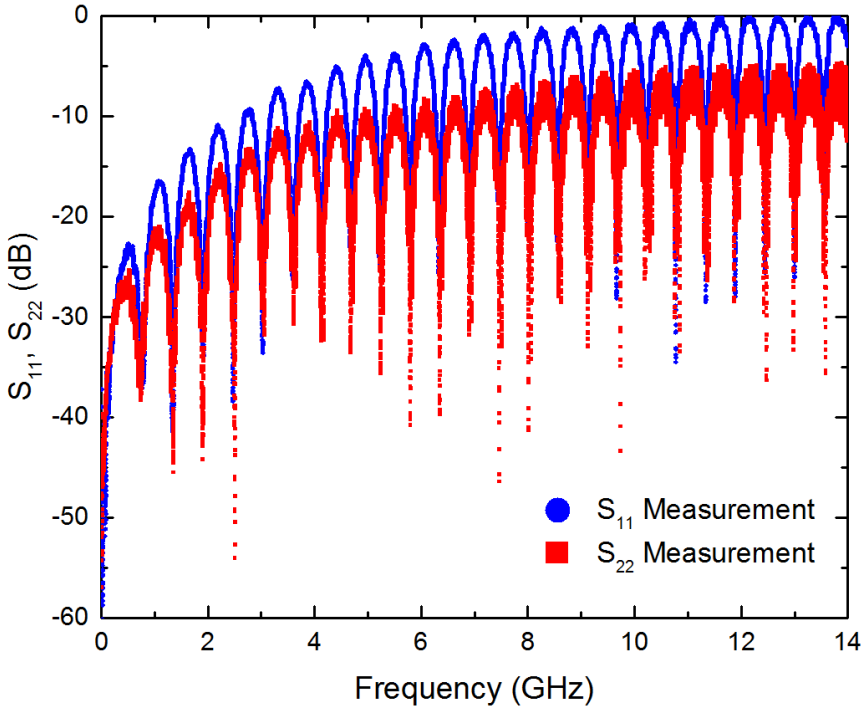

Figure 5.26: S_{11} and S_{22} measurement of a ∼15 cm long Nb/Al microstrip transmission line at 4.2 K.

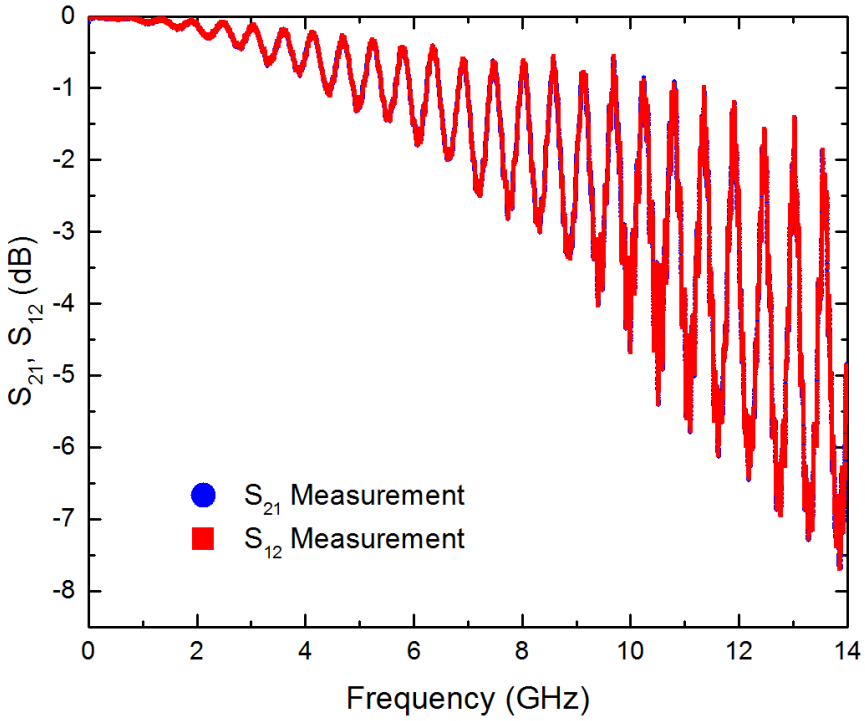

Figure 5.27: S_{21} and S_{12} measurement of a ∼15 cm long Nb/Al microstrip transmission line at 4.2 K.

5.9 A 25 cm long embedded Nb microstrip on PI-2611

An embedded Nb microstrip that was 25 cm in length was fabricated with a dielectric cover of ∼11 μm thick was measured in liquid He. The top embedding dielectric layer that contacted the Nb signal line was cured at a temperature of 225 °C to reduce the degradation of the Nb film quality. This temperature was experimentally determined to have the least impact on the Nb metallization. Measurements of S_{11} and S_{22} show a significant disparity between the two ends of the transmission lines. We suspect the difference is due to solder non-uniformity. The simulation model implemented to model the embedded microstrip is shown in Figure 5.28. The measurement results fitted to S_{11} and S_{21} fit are shown in Figures 5.29 and 5.30. Although the measurements suggest we have a higher loss with a low-cure dielectric, we cannot conclusively rule out Nb variation and/or changes in the quality of the Nb after curing. More work is required in this area to understand the impact of the dielectric curing on the RF performance of these transmission lines

5.10 Impact of excess solder on the microwave performance

Connections to microstrip samples were made through the use of high purity In solder applied to pads that had metallization that was compatible with the solder. At present, the In was applied manually and heated with a soldering iron, which introduced solder volume variability and degradation of the microwave performance with the excess solder. In our simulation models, we have included a parasitic capacitance (C_p) that we stated was due to excess solder. We verified the excess solder can be modeled as a parallel capacitance by removing the excess solder on a 15 cm long Nb only microstrip. Microscopy images of the microstrip sample under study are shown in Figure 5.31. We carefully removed the excess solder with a heated soldering iron and tweezers. After the excess solder was removed is shown in Figure 5.31b. Measurements before and after removing the excess solder are shown in Figure 5.32 and 5.33. The simulation models match the measurement, which indicated a

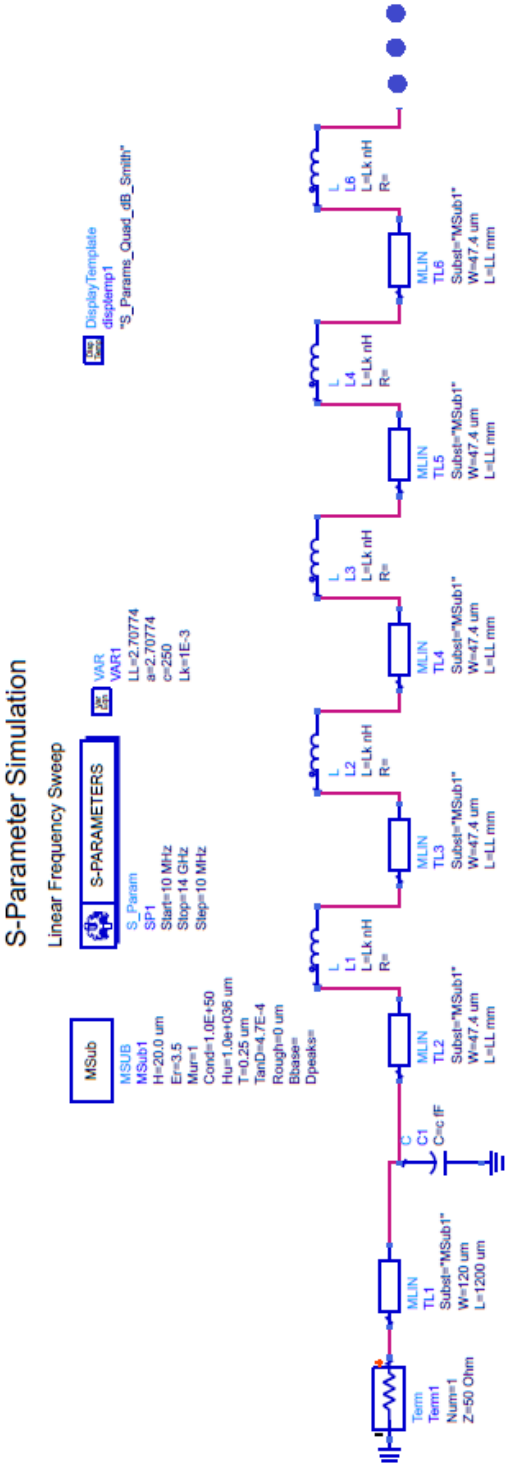

Figure 5.28: A ∼25 cm long embedded Nb microstrip model on PI-2611 implemented in ADS.

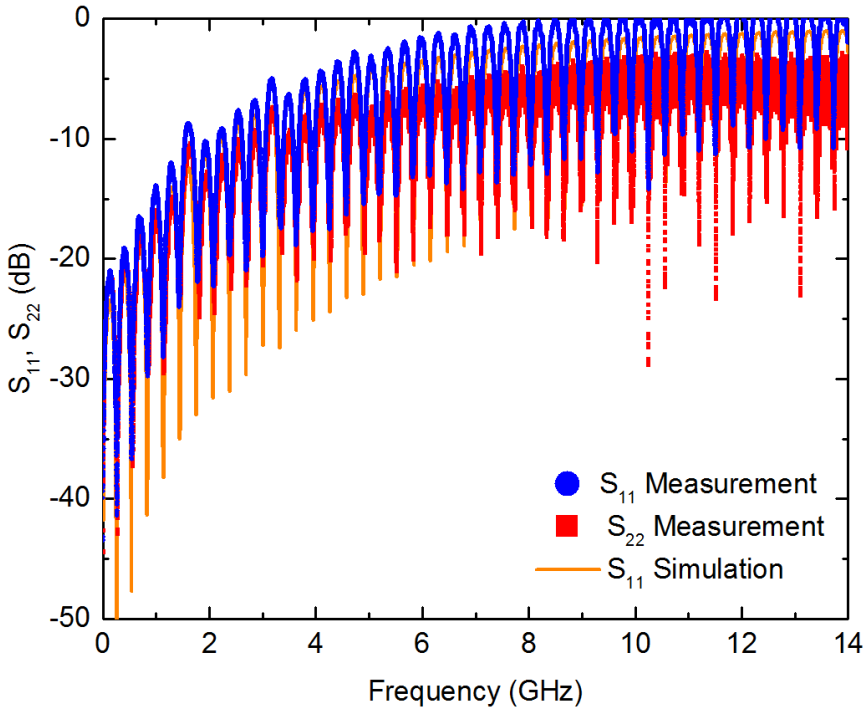

Figure 5.29: S_{11} and S_{22} measurement and simulation of a ~25 cm long embedded Nb microstrip transmission line 4.2 K.

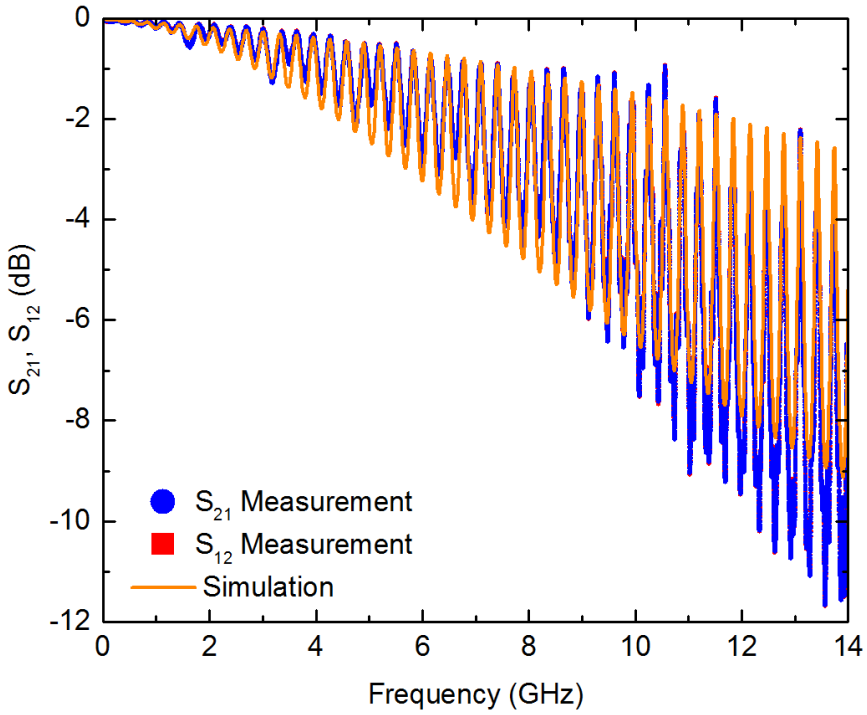

Figure 5.30: S_{21} and S_{12} measurement and simulation of a ~25 cm long embedded Nb microstrip transmission line 4.2 K.

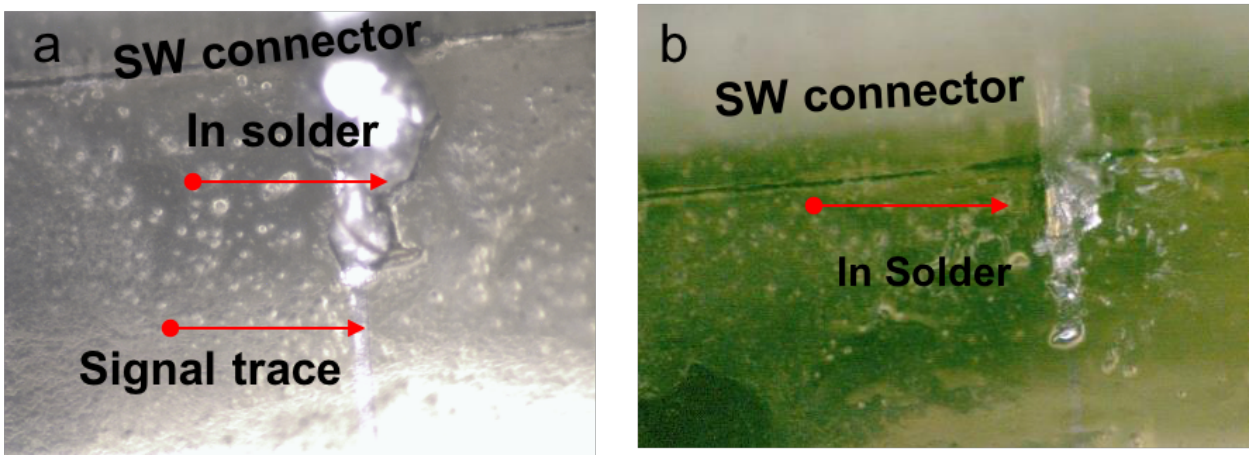

Figure 5.31: Microscopy images of the excess solder on a ∼15 cm long Nb microstrip cable (a) as assembled and (b) after excess solder removal

decrease in capacitance from an initial 250 fF to 124fF. Therefore we confirmed that including this additional capacitance did accurately represent the excess solder.

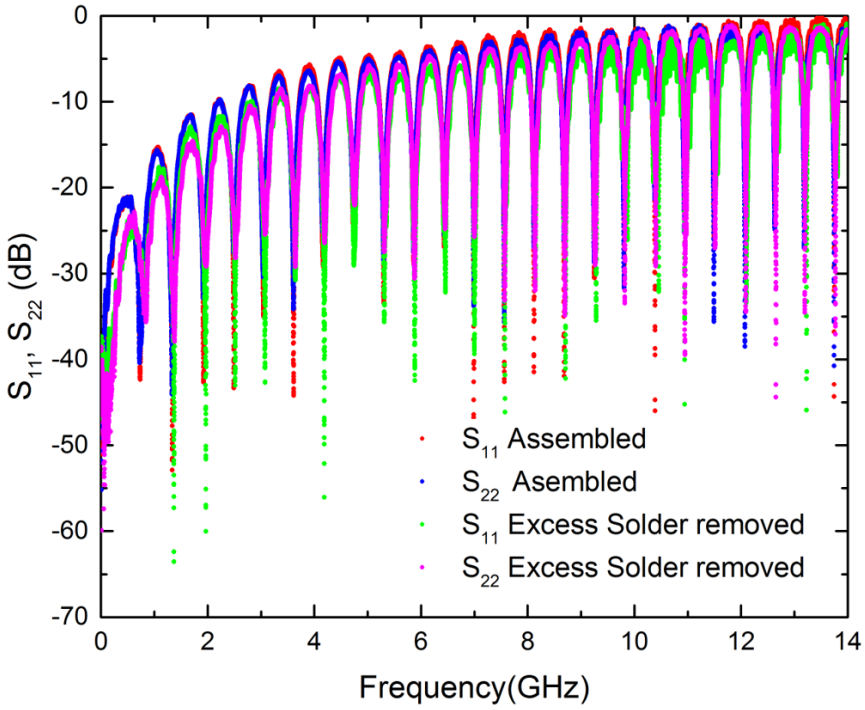

Figure 5.32: S_{11} and S_{22} measurement of a ∼15 cm long Nb microstrip transmission line at 4.2 K

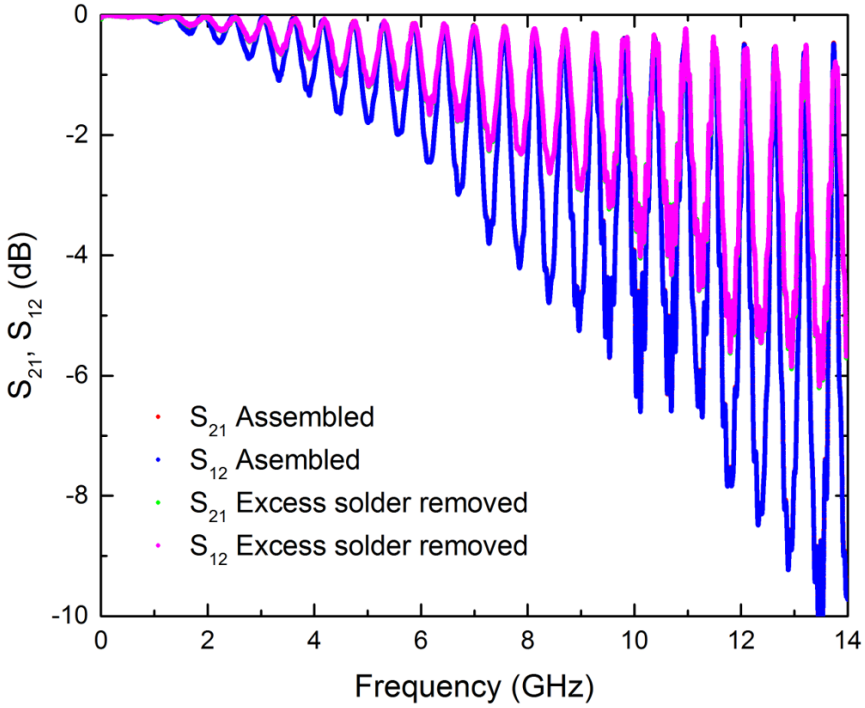

Figure 5.33: S_{21} and S_{12} measurement of a ∼15 cm long Nb microstrip transmission line at 4.2 K

Chapter 6

Conclusion

We presented superconducting Nb microstrip flex cables on Kapton and spin-on polyimide for use in cryogenic systems. We successfully implemented simulation models that predicted the RF performance of these microstrip flex cables at 4.2 K in liquid He. RF measurement results of these transmission lines was made possible through the implementation of RF standards (open, short, load, and thru) assembled on SMA edge launch connectors. We used an SOLR calibration performed in liquid He with the standards that we assembled to reduce the errors associated with the network analyzer, SMA cables and connectors. Without proper calibration standards that would work in liquid helium, the RF performance of the fabricated flex cables could not have been reported.

We measured 5 cm long Ti/Nb and Nb microstrip transmission lines on E-series Kapton that showed less than -0.1 dB of intrinsic loss up to 14 GHz. The main observable difference between the two samples ere the dips (valleys) in S_{21} that were caused by excess solder. We also fabricated Ti/Cu microstrip transmission lines that exhibited less than -3.5 dB of loss. From these measurements, it is apparent the benefit of using superconducting metallization for transmission lines on Kapton.

We also built microstrip transmission lines on spin-on polyimide, PI-2611, that was 20 μm thick. We fabricated and measured microstrip samples that were up to 55 cm in length. We meandered the signal line in a serpentine pattern to study longer transmission lines that were spaced closely together on a 100 mm diameter Si wafer. We studied Ti/Nb, Nb, and embedded Nb microstrip transmission lines of varying lengths. We were unable to observe a performance difference between Ti/Nb and Nb microstrip transmission lines due to the solder pad and excess solder that introduced a mismatch that shadowed any minute differences.

Despite these non-idealities present in the sample, measurements of these microstrip flex cables indicated less than -0.1 dB of intrinsic loss up to 14 GHz at 4.2 K. Measurements of a ∼25 cm long Nb microstrip samples also indicated similar intrinsic loss in the same frequency range. For comparison, we measured a 5 cm long Ti/Cu microstrip transmission line that exhibited less than -9.0 dB of intrinsic loss up to 14 GHz in liquid He. Meanwhile, a 25 cm long embedded microstrip samples exhibited less than -3 dB of intrinsic loss up to 14 GHz. Therefore, embedded and non-embedded microstrip transmission lines exhibited less loss at 4.2 K than similarly construed Ti/Cu transmission lines.

We also presented measurement results of cladded, Nb/Cu and Nb/Al microstrip samples at 4.2 K. RF measurement results of these samples indicated an increase in RF loss. A ∼55 cm long Nb with 200 nm of Cu microstrip measured at 4.2 K exhibited less than -20 dB of loss up to 14 GHz. While a 20 nm Al metallization on Nb that was ∼15 cm long exhibited less than -0.2 dB of loss in the same frequency range. Although more extensive work in this area needs to be undertaken to fully understand the impact the cladded metallization has on the RF performance

To our knowledge, we were the first to report RF measurements of a superconducting Nb microstrip on free-standing Kapton and PI-2611 polyimide at liquid He temperatures. This work is also first to report RF measurements of embedded microstrip and cladded Nb microstrip structures. The initial measurements show promising results with significant room for improvement. Our fabrication processes were based on traditional clean room methods, which naturally lends it self to creating microwave structures on larger size substrates to increase yield. The possibility of several transmission lines on a single flex cable is also realizable with the current methods outlined in this work.

Chapter 7

Future Work

The continuation of this work can branch into several different directions that would demonstrate even further the potential of these RF flex cables. Future work would involve the fabrication of multiple RF signal lines on a single flex cable. Therefore, cross-talk measurements would provide insight into the isolation between adjacent signal lines. Microstrip transmission flex cables could easily be made with multiple signal lines that are spaced at least 240 μm or 120 μm (2$\times$ the line width) for Kapton and PI-2611, respectively, which would reduce the far-end cross-talk [65]. First attempts should involve only two signal lines; the edge-launch connectors have a significant footprint which would limit the number of signal lines that could fit onto a single 100 mm diameter Si wafer.

An alternative method that could also be implemented would involve the use of a PCB with the flex cable flip-chip bonded onto designated pads, similar to the work by Tighe et al. [32]. Contact to the microstrip ground plane could be made with a clamp, that would be machined out of a bulk metal such as aluminum. Reduced size RF connectors can also be employed on the PCB to increase the signal line density with 0.9 mm connectors from Southwest Microwave that can be operated from DC to 67 GHz[1].

Stripline flex cables on PI-2611 could also be attempted again by curing the dielectric at a temperature of 225 °C, which was shown to work in an embedded microstrip structure. A few key processing steps would have to be revisited, specifically the dry etching of conformal vias in the dielectric. Dry etching with just an O_2 plasma has been shown to create a residue layer that is difficult to remove without the addition of a fluorinated gas, such as CF_4 during the etch process [41]. This CF_4 gas also can etch the Nb, if it is not protected with an

[1] `http://mpd.southwestmicrowave.com/products/family.php?family=297`

etch-stop layer [66]. Therefore, a protective metal, such as chromium (of a thickness that would need to be determined) on selected regions would need to be used [66] to protect the Nb during the etching of the dielectric. Since there would significant processing involved to make a stripline with vias in PI-2611, an alternative spin-on dielectric such as HD-4100 [67] could be used. HD-4100 is a spin-on photo-imageable dielectric that could be used to define vias without the need to dry-etch. Via chain structures could then be used to verify the via profile (i.e. conformal) and step coverage of the sputter deposited Nb.

A significant effort should also be made to focus on the application of a controlled solder volume on the fabricated flex cables. Methods for uniform indium plating on a Ti/Cu seed layer has been shown on 3 inch wafers [40], which could be applied to our own fabrication processes. We would need to verify what impact, if any, the plating seed layer would have on a niobium film. A simple test would involve plating Cu to the desired thickness and pattern, plating indium on this pattern and etching away the seed layer, this would help verify that these steps did not impact Nb superconductivity.

In this work, we briefly studied cladded metallization consisting of a normal metal on superconducting Nb. There was a proximity effect between the Nb and normal metal due to Andreev reflections [64] that could be studied in greater detail. Our RF measurements on Nb/Cu and Nb/Al films suggest an increase microwave loss, but more work is required to study these metallization (e.g. thinner metallization and lower temperatures). Measurements of the kinetic inductance by Claassen [63] suggest that there are changes in the kinetic inductance by cladding the Nb with a normal conductor. Therefore, creating microstrip transmission lines with varying thickness of the normal metallization and correlating it to RF measurements would provide useful information for bimetallic RF structures. Modeling efforts could then follow from measurement data.

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Appendices

Material type	Company	Model/Product	Notes
Dielectric	Asahi Glass	AL-X2030/2025	Material name change to 2030 from 2025
Dielectric	HD MicroSystems	PI-2611	not photoimageable
Kapton	Dupont	EN	American DuraFilm
AlN	Stellar		Double side polished
Metals	Kamis Incorporated	Cu, Ti, Nb target	
Wafers	SiWafers	www.Siwafers.com	
Chemicals	Sigma-Aldrich/VWR	Sodium Chloride	
Al Etch	Transene Type-A		
Pogo Pins	Everett Charles Technologies	HPA-0J	

Table 1: List of Suppliers

Material type	Company	Model/Product	Notes
Dielectric	Asahi Glass	AL-X2030/2025	Material name change to 2030 from 2025
Dielectric	HD MicroSystems	PI-2611	not photoimageable
Kapton	Dupont	EN	American DuraFilm
AlN	Stellar		Double side polished
Metals	Kamis Incorporated	Cu, Ti, Nb target	
Wafers	SiWafers	www.Siwafers.com	
Chemicals	Sigma-Aldrich/VWR	Sodium Chloride	
Al Etch	Transene Type-A		
Pogo Pins	Everett Charles Technologies	HPA-0J	

Table 2: List of Equipment Used

Appendix A

Microwave switches

In this chapter, we provide detailed information of how the microwave switches that are at the end of the rod (cold side) are interfaced to a computer running LabVIEW. We used a DB25 (25 pin) female connector to interface to the DC lines that control the microwave switches. Pins 1 through 16 are the only pins that are currently being used. The pin out profile of the DB25 connector is shown in Figures A.1.

The top of the rod has a female DB25 connector which is interfaced to a breakout box that has the same connector type with a male-male DB25 cable. The breakout box is then connected to a relay that allows us to select a specific output. The wiring map of the DB25 to the relay and switch is detailed in Table A.1. We used lakeshore quadwire phosphor bronze wires that have 4 wires bundled together. Each switch has 8 different connections, therefore two wires (8 leads total) per switch. Switch 1 has two wires and were labeled (1_1) and (1_2) for switch 1 cable 1, the same nomenclature was followed for switch 2.

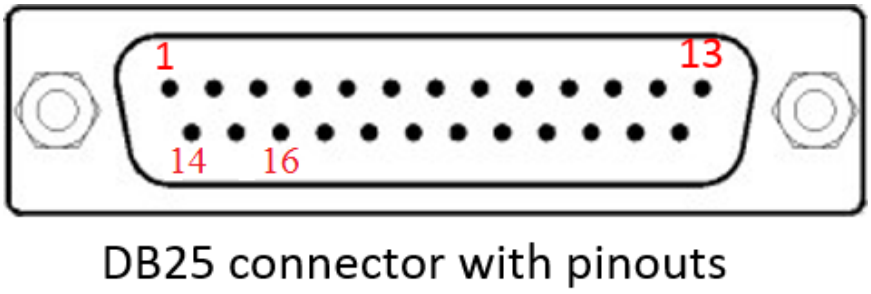

Figure A.1: DB25 connector with pin 1 labeled for reference. The breakout box uses a total of 16 inputs. Inputs are numbered for clarity.

Table A.1: Pin outs and wiring for two radiall switches.

DB25	Relay	Switch	wire_number (color)
1	1	GND	1_1 (green)
2	2	1	1_1 (red)
3	3	2	1_1 (black)
4	4	3	1_1 (brown)
5	5	4	1_2 (red)
6	6	5	1_2 (green)
7	7	6	1_2 (black)
8	8	RESET	1_2 (brown)
		Switch 2	
9	1	GND	2_1 (green)
10	9	1	2_1 (red)
11	10	2	2_1 (black)
12	11	3	2_1 (brown)
13	12	4	2_2 (red)
14	13	5	2_2 (green)
15	14	6	2_2 (black)
16	15	RESET	2_2 (brown)

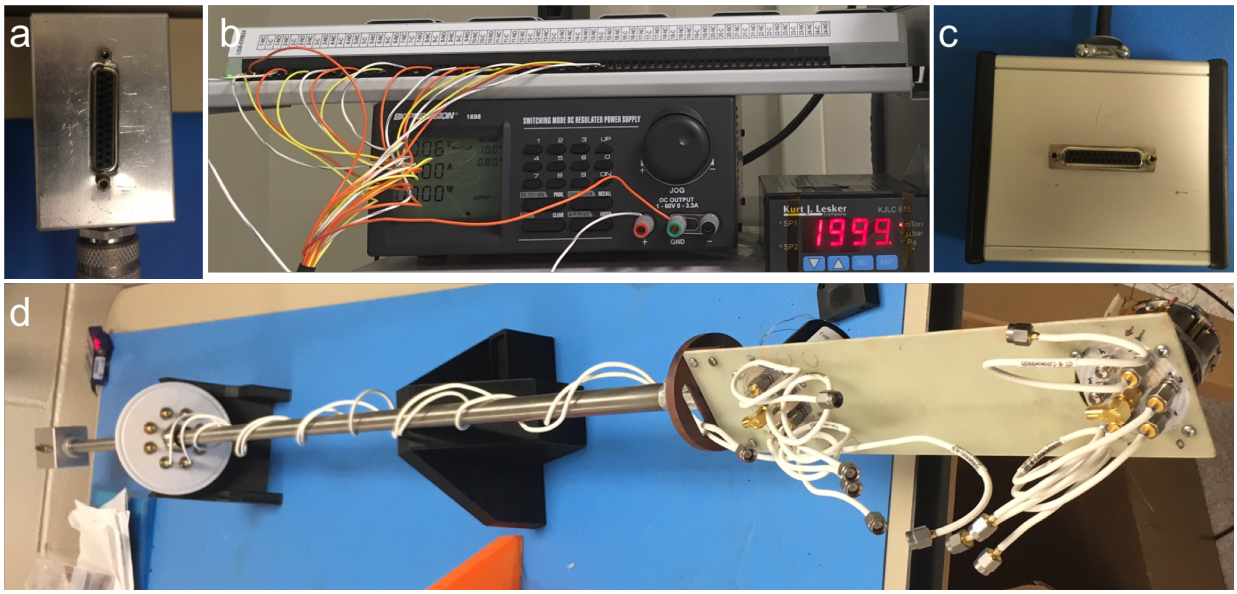

Figure A.2: Microwave switch interface equipment (a) breakout box on the rod (b) relay and power supply (c) breakout box that interfaces with the relay (d) rod with the SMA cables and microwave switches is shown.

Appendix B

Fabrication travelers

In this chapter, the fabrication processes are described in greater detail. Each step is outlined with the appropriate step (e.g. bake, spin-on, etc.).

Step No.	Process	Parameters	Remarks
		Dielectric spin-on steps to achieve 20 μm	
1	Release Layer	a. 2 minutes of ion milling at 1 kV b. 250 Å Cr, 500 Å Al	
2	Dehydration Bake	Vacuum oven at 110°C for 20 minutes	
3	Adhesion Promoter	VM652. Spin speed 1. 500 RPM a=500 rpm/s 2. 3000 RPM a=1000 rpm/s t=30s	
4	Soft Bake	hotplate bake at 120°C t=60s	
5	PI Spin	1. 500 rpm a=500 rpm/s t=5s, 2. 1600 RPM a=1000 RPMs/s t=30s	
6	Bake	hotplate bake at 120°C t=5 mins.	
7	Cure	Profile 2 (350°C Cure)	
8	Plasma	150 W for 25 seconds	
9	Dehydration Bake	Vacuum oven at 110°C for 20 minutes	
10	Adhesion Promoter	VM652. Spin speed 1. 500 RPM a=500 rpm/s 2. 3000 RPM a=1000 rpm/s t=30s	
11	Soft Bake	hotplate bake at 120°C t=60s	
12	PI Spin	1. 500 rpm a=500 rpm/s t=5s, 2. 1600 RPM a=1000 RPMs/s t=30s	
13	Bake	hotplate bake at 120°C t=5 mins.	
14	Cure	Profile 2 (350°C Cure)	
		Signal Line Definition	
15	Dehydration Bake	Vacuum Oven at 110°C for 20 minutes	
13	HMDS Coat	Place in HMDS beaker for 10 minutes	HMDS is found in an amber bottle
14	PR	AZ-9245: spin speed 1. 1700 RPM t=5s, a=500 RPM/s 2. 2200 RPM t=25s a= 1000 RPM/s	
15	Soft Bake	hotplate bake at 110°C t=90s	
16	Mask Alignment	Exposure time: 25 seconds Alignment gap: 25μm	Mask:M1
17	Development	3:1 DI Water: AZ 400k. Agitate solution prior to placing wafer in solution. Rinse in DI water and N_2 blow dry Ratio: 150 mL of DI water, 50 mL Developer	2 minute development time
18	Nb Deposition	a. 2 minutes of ion milling at 1 kV. b. P= 1 kW/6.1 mTorr/30 minutes	
19	Lift-off	Rinse in acetone/methanol/IPA	

Table B.1: Microstrip Traveler 1/2

Step No.	Process	Parameters	Remarks
		Under Bump Metallization	
20	Dehydration Bake	Vacuum oven at 110°C for 20 minutes	
21	HMDS Coat	Place in HMDS beaker for 10 minutes	HMDS is found in an amber bottle
22	PR	AZ-9245: spin speed 1. 1700 RPM t=5s, a=500 RPM/s 2. 2200 RPM t=25s a= 1000 RPM/s	
23	Soft Bake	hotplate bake at 110°C t=90s	
24	Mask Alignment	Exposure time: 25 seconds Alignment gap: 25μm	Mask:UBM
25	Development	3:1 DI Water: AZ 400k. Agitate solution prior to placing wafer in solution. Rinse in DI water and N_2 blow dry Ratio: 150 mL of DI water, 50 mL Developer	2 minute development time
26	UBM	a. 2 minutes of ion milling at 1 kV. b. Ti: 500 Å(2Å/s), Cu: 5000Å(2Å/s)	
27	Lift-off	Rinse in acetone/methanol/IPA	
		Release Sample & Ground Plane Metallization	
28	PR	AZ-9245: spin speed 1. 1700 RPM t=5s, a=500 RPM/s 2. 2200 RPM t=25s a= 1000 RPM/s	
29	Soft Bake	hotplate bake at 110°C t=90s	
30	Dice samples	Use profile ANG/5inch profile	
31	Salt Solution	2M (Moles/L) solution of NaCl based on 1L of H20. (a) Pour 500 mL of DI water into beaker (b) 117 gramsof NaCl. Pour into beaker and fill with water until 1L	
32	Sample Release	Connect ground to the metal mesh, and apply 0.6 V to the sample	
33	Surface clean	rinse in acetone/methanol/IPA, followed by DI water	
34	Backside Sample	Mount sample onto a wafer with the backside exposed	
35	Nb Deposition	a. 2 minutes of ion milling at 1 kV. b. P= 1 kW/6.1 mTorr/30 minutes	

Table B.2: Microstrip Traveler 2/2

Step No.	Process	Parameters	Remarks
		Dielectric spin-on steps to achieve 20 μm	
1	Release Layer	a. 2 minutes of ion milling at 1 kV b. 250 Å Cr, 500 Å Al	
2	Dehydration Bake	Vacuum oven at 110°C for 20 minutes	
3	Adhesion Promoter	VM652. Spin speed 1. 500 RPM a=500 rpm/s 2. 3000 RPM a=1000 rpm/s t=30s	
4	Soft Bake	hotplate bake at 120°C t=60s	
5	PI Spin	1. 500 rpm a=500 rpm/s t=5s, 2. 1600 RPM a=1000 RPMs/s t=30s	
6	Bake	hotplate bake at 120°C t=5 mins.	
7	Cure	Profile 2 (350°C Cure)	
8	Plasma	150 W for 25 seconds	
9	Dehydration Bake	Vacuum oven at 110°C for 20 minutes	
10	Adhesion Promoter	VM652. Spin speed 1. 500 RPM a=500 rpm/s 2. 3000 RPM a=1000 rpm/s t=30s	
11	Soft Bake	hotplate bake at 120°C t=60s	
12	PI Spin	1. 500 rpm a=500 rpm/s t=5s, 2. 1600 RPM a=1000 RPMs/s t=30s	
13	Bake	hotplate bake at 120°C t=5 mins.	
14	Cure	Profile 2 (350°C Cure)	
		Signal Line Definition	
15	Dehydration Bake	Vacuum Oven at 110°C for 20 minutes	
13	HMDS Coat	Place in HMDS beaker for 10 minutes	HMDS is found in an amber bottle
14	PR	AZ-9245: spin speed 1. 1700 RPM t=5s, a=500 RPM/s 2. 2200 RPM t=25s a= 1000 RPM/s	
15	Soft Bake	hotplate bake at 110°C t=90s	
16	Mask Alignment	Exposure time: 25 seconds Alignment gap: 25μm	Mask:M1
17	Development	3:1 DI Water: AZ 400k. Agitate solution prior to placing wafer in solution. Rinse in DI water and N_2 blow dry Ratio: 150 mL of DI water, 50 mL Developer	2 minute development time
18	Nb Deposition	a. 2 minutes of ion milling at 1 kV. b. P= 1 kW/6.1 mTorr/30 minutes	
19	Lift-off	Rinse in acetone/methanol/IPA	

Table B.3: Embedded Microstrip Traveler 1/3

Step No.	Process	Parameters	Remarks
		Dielectric Encapsulation layer	
20	Signal	Kapton tape the signal line	
21	Dehydration Bake	Vacuum oven at 110°C for 20 minutes	
22	Adhesion Promoter	VM652. Spin speed 1. 500 RPM a=500 rpm/s 2. 3000 RPM a=1000 rpm/s t=30s	
23	Soft Bake	hotplate bake at 120°C t=60s	
24	PI Spin	1. 500 rpm a=500 rpm/s t=5s, 2. 1600 RPM a=1000 RPMs/s t=30s	
25	Bake	hotplate bake at 120°C t=5 mins.	
26	Signal	Remove Kapton tape	
27	Cure	Profile 5 (225°C Cure)	
		Under Bump Metallization	
20	Dehydration Bake	Vacuum oven at 110°C for 20 minutes	
21	HMDS Coat	Place in HMDS beaker for 10 minutes	HMDS is found in an amber bottle
22	PR	AZ-9245: spin speed 1. 1700 RPM t=5s, a=500 RPM/s 2. 2200 RPM t=25s a= 1000 RPM/s	
23	Soft Bake	hotplate bake at 110°C t=90s	
24	Mask Alignment	Exposure time: 25 seconds Alignment gap: 25μm	Mask:UBM
25	Development	3:1 DI Water: AZ 400k. Agitate solution prior to placing wafer in solution. Rinse in DI water and N_2 blow dry Ratio: 150 mL of DI water, 50 mL Developer	2 minute development time
26	UBM	a. 2 minutes of ion milling at 1 kV. b. Ti: 500 Å(2Å/s), Cu: 5000Å(2Å/s)	
27	Lift-off	Rinse in acetone/methanol/IPA	

Table B.4: Embedded Microstrip Traveler 2/2

Step No.	Process	Parameters	Remarks
		Release Sample & Ground Plane Metallization	
28	PR	AZ-9245: spin speed 1. 1700 RPM t=5s, a=500 RPM/s 2. 2200 RPM t=25s a= 1000 RPM/s	
29	Soft Bake	hotplate bake at 110°C t=90s	
30	Dice samples	Use profile ANG/5inch profile	
31	Salt Solution	2M (Moles/L) solution of NaCl based on 1L of H20. (a) Pour 500 mL of DI water into beaker (b) 117 gramsof NaCl. Pour into beaker and fill with water until 1L	
32	Sample Release	Connect ground to the metal mesh, and apply 0.6 V to the sample	
33	Surface clean	rinse in acetone/methanol/IPA, followed by DI water	
34	Backside Sample	Mount sample onto a wafer with the backside exposed	
35	Nb Deposition	a. 2 minutes of ion milling at 1 kV. b. P= 1 kW/6.1 mTorr/30 minutes	

Table B.5: Embedded Microstrip Traveler 3/3

Step No.	Process	Parameters	Remarks
		Ground Plane Metallization and via etch	
1	Release Layer	a. 2 minutes of ion milling at 1 kV b. 250 Å Cr, 500 Å Al	
2	Dehydration Bake	Vacuum oven at 110°C for 20 minutes	
3	HMDS Coat	Place in HMDS beaker for 10 minutes	HMDS is found in an amber bottle
4	PR	AZ-9245: spin speed 1. 1700 RPM t=5s, a=500 RPM/s 2. 2200 RPM t=25s a= 1000 RPM/s	
5	Soft Bake	hotplate bake at 110°C t=90s	
6	Mask Alignment	Exposure time: 25 seconds Alignment gap: 25μm	Mask:M0
7	Development	3:1 DI Water: AZ 400k. Agitate solution prior to placing wafer in solution. Rinse in DI water and N_2 blow dry Ratio: 150 mL of DI water, 50 mL Developer	2 minute development time
8	Nb Deposition	a. 2 minutes of ion milling at 1 kV. b. P= 1 kW/6.1 mTorr/30 minutes	
9	Lift-off	Rinse in acetone/methanol/IPA	
		Dielectric spin-on and via01 etch	
10	Dehydration Bake	Vacuum oven at 110°C for 20 minutes	
11	Adhesion Promoter	VM652. Spin speed 1. 500 RPM a=500 rpm/s 2. 3000 RPM a=1000 rpm/s t=30s	
12	Soft Bake	hotplate bake at 120°C t=60s	
13	PI Spin	1. 500 rpm a=500 rpm/s t=5s, 2. 1600 RPM a=1000 RPMs/s t=30s	
14	Bake	hotplate bake at 120°C t=5 mins.	
15	Cure	Profile 2 (350°C Cure)	
16	Bake	hotplate bake at 110°C t=20 mins.	
17	Al hard mask	a. 2 minutes of ion milling at 1 kV a. 2000 Å Al	
18	Bake	hotplate bake at 110°C t=20 mins.	
19	HMDS Coat	Place in HMDS beaker for 10 minutes	HMDS is found in an amber bottle
20	PR	AZ-9245: spin speed 1. 1700 RPM t=5s, a=500 RPM/s 2. 2200 RPM t=25s a= 1000 RPM/s	
21	Mask Alignment	Exposure time: 25 seconds Alignment gap: 25μm	Mask:via01
22	Development	3:1 DI Water: AZ 400k. Agitate solution prior to placing	
23	Isotropic via etch	Load into Branson IPC asher, P=1000W for t=60 minutes	
24	Anisotropic via etch	Load into AOE etcher,PBrad profile	verify etch
24	Aluminum etch	load wafers into J.T. Baker 80-15-3-2 solution	

Table B.6: Stripline Traveler 1/4

Step No.	Process	Parameters	Remarks
		Signal Deposition and via01 contact	
25	Plasma exposure	150 W for 25 seconds	
26	Dehydration Bake	Vacuum oven at 110°C for 20 minutes	
27	HMDS Coat	Place in HMDS beaker for 10 minutes	HMDS is found in an amber bottle
28	PR	AZ-9245: spin speed 1. 1700 RPM t=5s, a=500 RPM/s 2. 2200 RPM t=25s a= 1000 RPM/s	
29	Soft Bake	hotplate bake at 110°C t=90s	
30	Mask Alignment	Exposure time: 25 seconds Alignment gap: 25μm	Mask:UBM
31	Development	3:1 DI Water: AZ 400k. Agitate solution prior to placing wafer in solution. Rinse in DI water and N_2 blow dry Ratio: 150 mL of DI water, 50 mL Developer	2 minute development time
32	Nb Deposition	a. 2 minutes of ion milling at 1 kV. b. P= 1 kW/6.1 mTorr/30 minutes	
33	Lift-off	Rinse in acetone/methanol/IPA	
		Dielectric spin-on and via12 etch	
34	Dehydration Bake	Vacuum oven at 110°C for 20 minutes	
35	Adhesion Promoter	VM652. Spin speed 1. 500 RPM a=500 rpm/s 2. 3000 RPM a=1000 rpm/s t=30s	
36	Soft Bake	hotplate bake at 120°C t=60s	
37	PI Spin	1. 500 rpm a=500 rpm/s t=5s, 2. 1600 RPM a=1000 RPMs/s t=30s	
38	Bake	hotplate bake at 120°C t=5 mins.	
39	Cure	Profile 2 (350°C Cure)	
40	Bake	hotplate bake at 110°C t=20 mins.	
41	Al hard mask	a. 2 minutes of ion milling at 1 kV a. 2000 Å Al	
42	Bake	hotplate bake at 110°C t=20 mins.	
43	HMDS Coat	Place in HMDS beaker for 10 minutes	HMDS is found in an amber bottle
44	PR	AZ-9245: spin speed 1. 1700 RPM t=5s, a=500 RPM/s 2. 2200 RPM t=25s a= 1000 RPM/s	
45	Mask Alignment	Exposure time: 25 seconds Alignment gap: 25μm	Mask:via12
46	Development	3:1 DI Water: AZ 400k. Agitate solution prior to placing	
47	Isotropic via etch	Load into Branson IPC asher, P=1000W for t=60 minutes	
48	Anisotropic via etch	Load into AOE etcher,PBrad profile	verify etch
49	Aluminum etch	load wafers into J.T. Baker 80-15-3-2 solution	

Table B.7: Stripline Traveler 2/4

Step No.	Process	Parameters	Remarks
		Top ground plane deposition	
50	Plasma exposure	150 W for 25 seconds	
51	Dehydration Bake	Vacuum oven at 110°C for 20 minutes	
52	HMDS Coat	Place in HMDS beaker for 10 minutes	HMDS is found in an amber bottle
53	PR	AZ-9245: spin speed 1. 1700 RPM t=5s, a=500 RPM/s 2. 2200 RPM t=25s a= 1000 RPM/s	
54	Soft Bake	hotplate bake at 110°C t=90s	
55	Mask Alignment	Exposure time: 25 seconds Alignment gap: 25μm	Mask:M2
56	Development	3:1 DI Water: AZ 400k. Agitate solution prior to placing wafer in solution. Rinse in DI water and N_2 blow dry Ratio: 150 mL of DI water, 50 mL Developer	2 minute development time
57	Nb Deposition	a. 2 minutes of ion milling at 1 kV. b. P= 1 kW/6.1 mTorr/30 minutes	
58	Lift-off	Rinse in acetone/methanol/IPA	
		UBM deposition	
59	Dehydration Bake	Vacuum Oven at 110°C for 20 minutes	
60	HMDS Coat	Place in HMDS beaker for 10 minutes	HMDS is found in an amber bottle
61	Soft Bake	hotplate bake at 110°C t=90s	
62	Mask Alignment	Exposure time: 25 seconds Alignment gap: 25μm	Mask:M2
63	Development	3:1 DI Water: AZ 400k. Agitate solution prior to placing wafer in solution. Rinse in DI water and N_2 blow dry Ratio: 150 mL of DI water, 50 mL Developer	2 minute development time
64	UBM	a. 2 minutes of ion milling at 1 kV. b. Ti: 500 Å(2Å/s), Cu: 5000Å(2Å/s)	
65	Lift-off	Rinse in acetone/methanol/IPA	

Table B.8: Stripline Traveler 3/4

Step No.	Process	Parameters	Remarks
		Release Sample	
66	PR	AZ-9245: spin speed 1. 1700 RPM t=5s, a=500 RPM/s 2. 2200 RPM t=25s a= 1000 RPM/s	
67	Soft Bake	hotplate bake at 110°C t=90s	
68	Dice samples	Use profile ANG/5inch profile	
69	Salt Solution	2M (Moles/L) solution of NaCl based on 1L of H20. (a) Pour 500 mL of DI water into beaker (b) 117 gramsof NaCl. Pour into beaker and fill with water until 1L	
70	Sample Release	Connect ground to the metal mesh, and apply 0.6 V to the sample	
71	Surface clean	rinse in acetone/methanol/IPA, followed by DI water	

Table B.9: Stripline Traveler 4/4