Evaluation of thick film materials for high temperature electronics packaging

by

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Abstract

Geothermal well logging requires electronics and packaging working reliably at 300°C. Thick film technology has many advantages and has been widely investigated for high temperature applications. Previous studies showed that a commonly used thick film conductor and dielectric with capability of operating at 300°C had a leakage current increase and adhesion loss after aging with bias voltage due to the glass modifier, Na, migrating in the dielectric and accumulating on the negative electrode. This dissertation presents the electrical and mechanical reliability testing of alternative thick film materials. Test vehicles were fabricated with thick film materials as capacitor and interdigitated finger structures. For the vehicles with PtPdAu thick film paste, the leakage current with thin multilayer dielectrics increased significantly in a short time after 300°C aging with 100 V bias with the positive bias on the top electrode and the negative electrode on the bottom. The leakage current of test vehicles with thick dielectrics remained relatively constant during 300°C aging in both capacitor and all interdigitated finger structures. Cross section and EDS analysis showed that Bi, in the PtPdAu paste as the binder, diffused into the dielectrics from both the top and bottom conductors during the firing process in fabrication. The Bi from both sides met in the center of the dielectric and resulting in the increase of leakage current during aging with bias. By using UV-vis spectroscopy analysis, electron traps were found to be 3.2 - 3.5 eV in dielectric with diffused Bi.

The adhesion of the thick film capacitor decreased from 100 hours for test vehicles with thin multilayer dielectrics or from 500 hours for vehicles with thick multilayer dielectrics. The multilayer dielectrics lifted off from the bottom conductor if the conductor was PtPdAu and the 100 V positive bias was applied on the top electrode. With Au conductor or if the

100 V positive bias was applied on the bottom electrode, the adhesion remained relatively constant before and after aging.

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Chapter 1

Introduction

Consumer electronics, which are the majority of electronics manufactured today, are typically used in an environment ranging from -40°C to +85°C, such as home appliances, smart phones and laptops[1]. However, some applications may be in environments at +300°C or even greater, such as automotive engines, the surface of Venus, oil and gas exploration, and geothermal wells. These harsh environment applications challenge the ability of the electronics to operate in high temperature environments. This chapter briefly introduces high temperature electronics and challenges in packaging for high temperature applications.

1.1 High temperature electronics

While there is no precise definition of high temperature electronics, generally, electronics operating at 175°C or greater can be considered as high temperature [1]. The temperature can either be due to power dissipation within the device or due to the operating environment. Table 1.1 lists the applications and requirements for high temperature electronics[2, 3]. These high temperature applications require the materials, devices and packaging to be compatible with the environment.

Table 1.1: Applications and requirements for high temperature applications[2, 3].

Application	Temperature (°C)	Minimum Duration	Duty
Nuclear waste storage	25 - 150	Months-years	Continuous
Automobiles	150 - 250	10 years	Intermittent/cyclical
Gas & oil well logging instrumentation	150 - 300	Few hours-years	Intermittent/cyclical, or continuous
Geothermal well logging instrumentation	150 - 400	Few-100 hours	Intermittent/cyclical
Space Exploration	125 - 485	Months-years	Intermittent/cyclical, or continuous
Fossil-fuel energy plants	400 - 500	Months-years	Continuous
Aircraft systems-on engines & smart transducers	300 - 500	1000 hours	Intermittent/cyclical
Aircraft engine R & D	500 - 600	1000 hours	Intermittent/cyclical (one-shot acceptable)
Nuclear reactors	25 - 1000	Months-years	Continuous

1.1.1 Automotive applications

In automotive applications, integration of power transistors and smart power devices will require power devices to operate at 175°C to 200°C[4]. Hybrid electric vehicles and fuel cell vehicles will also drive the demand for higher temperature power electronics. In the case of hybrid electric and fuel cell vehicles, the high temperature will be due to power dissipation. The alternatives to high-temperature devices are thermal management systems, which add weight and cost. Finally, the number of sensors in vehicles is increasing as more electrically controlled systems are added. Many of these sensors must work in high temperature environments. The harshest applications are exhaust gas sensors and cylinder pressure or combustion sensors.

1.1.2 Space application

Venus has a surface temperature of 485°C and a pressure of 90 bars[5]. Increasing the operating temperature capability of the electronics will increase the operating life of the surface landing probes and/or reduce the size and weight of the probes by reducing the complexity of the thermal protection system[6].

1.1.3 Geothermal energy application

Geothermal energy is the thermal energy stored at accessible depth in the earth's crust. Thermal energy in the earth is distributed between the constituent host rock and the natural fluid that is contained in its fractures and pores. These fluids are mostly water with various dissolved gases and salts. Most geothermal resources, which are usable for electrical power generation, result from the intrusion of magma (molten rock) from great depth (>20 km) into the earths crust[7]. These intrusions typically reach depths of 0 - 10 km.

The growth of geothermal energy development is limited by inadequate technology, instead of resource availability. Only the very highest grade geothermal resources can be economically used today for the generation of electricity. Figure 1.1 gives an illustration of a geothermal energy plant[8]. Mock, et al suggested the use of advanced drilling and improved heat mining methods as approaches to increase the worldwide use of geothermal energy by reducing field development costs[7]. Researchers have demonstrated that conventional drilling methods can be adapted for the harsh environments ranging from 250 to 350°C, which are hot enough to generate commercial power production[7, 9].

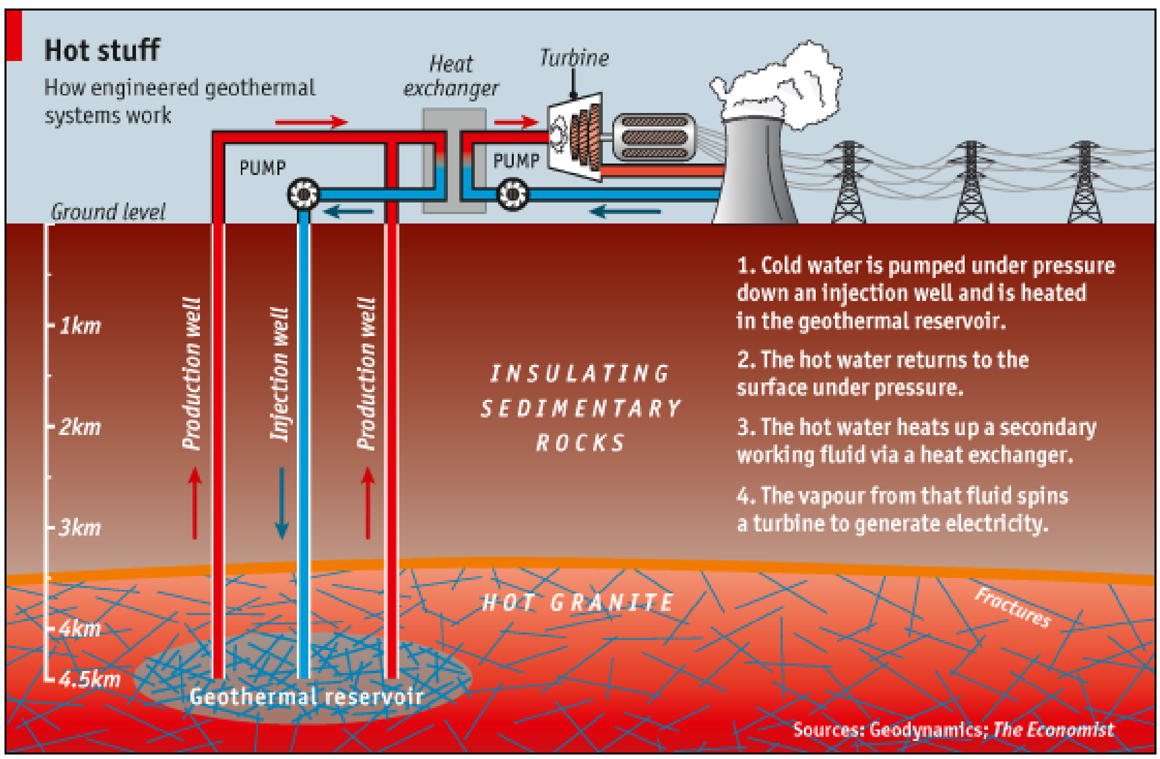

Figure 1.1: Illustration of geothermal energy plant[8].

Most geothermal instruments use conventional oil patch electronics operating in a heat shield. These instruments have electronics that are generally limited to 150°C. The highly specialized and relatively expensive heat shields are limited to 400°C[10]. The geothermal instruments are expected to work between 4 and 12 hours at 300°C in a geothermal well, until the shielded electronics reach their limit in temperature[10].

Only a limited number of instruments are designed to operate at 300°C. A televiewer with a stackable spectral gamma tool has been demonstrated at 300°C and a 238°C tolerant vertical seismic profiling instrument is available[10]. Both of these tools are useful in the analysis of induced fracturing and microseismicity studies. In addition, a dual laterolog resistivity tool has been designed for 300°C operation [10]. Figures 1.2 - 1.3 give examples of the high temperature tools operating up to 300°C in geothermal wells[11]. The development of these devices shows that there is a demand to develop electronic devices, which are durable and reliable when operating at 300°C or greater temperature.

Figure 1.2: A demonstration for multisensor in use[11].

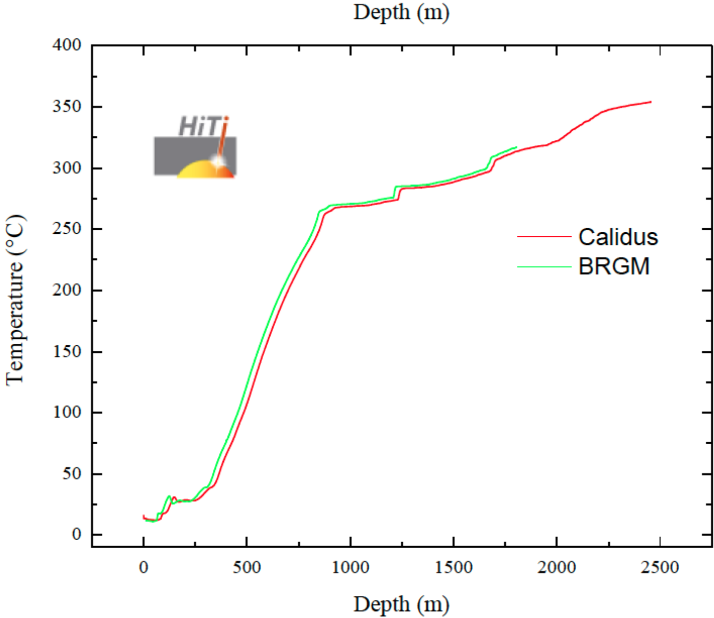

Figure 1.3: Temperature readings up to 300°C from two high temperature borehole instruments[11].

1.2 High temperature packaging

Most materials used in consumer electronics packaging, such as conductive adhesives or low melting point solders for die attach and epoxy molding compounds, melt or decompose in high temperature environments[1]. New developments in packaging to interconnect devices and build modules operating at high temperatures are required[12, 13].

Thick film technology based on metals, glasses, and ceramics has many advantages for high temperature applications, for example, the ability to produce hybrid integrated circuits in a robust and miniaturized package. Figures 1.4 - 1.6 show examples of thick film circuits for high temperature operation. An amplifier test board, shown in figure 1.4, was based on thick film technology and tested as functional at 300°C[14]. The substrate was fabricated with thick film technology and amplifiers and resistors were assembled on the substrate. Figure 1.5 shows a pressure to frequency circuit test board using a thick film metalized substrate[15]. The pressure to frequency test board was capable of converting pressure data to a frequency signal at 300°C. Figure 1.6 shows a DIP socket test fixture with inserted DIP package, which provides reliable conductivity at 300°C[15].

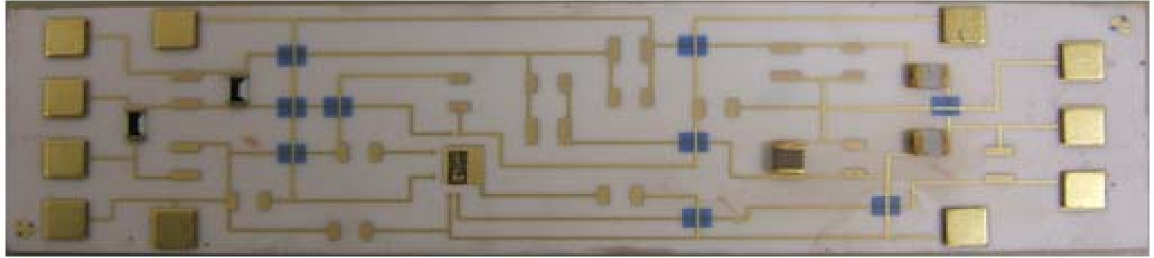

Figure 1.4: An amplifier test board for 300°C operation[14].

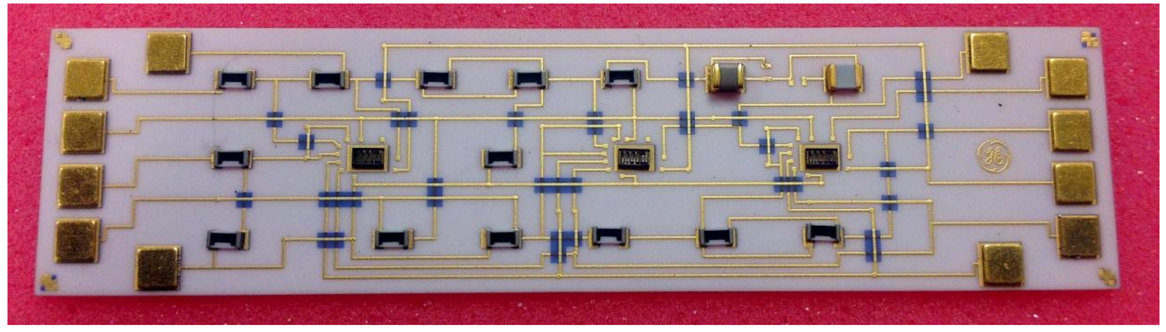

Figure 1.5: An pressure to frequency circuit test board for 300°C operation[15].

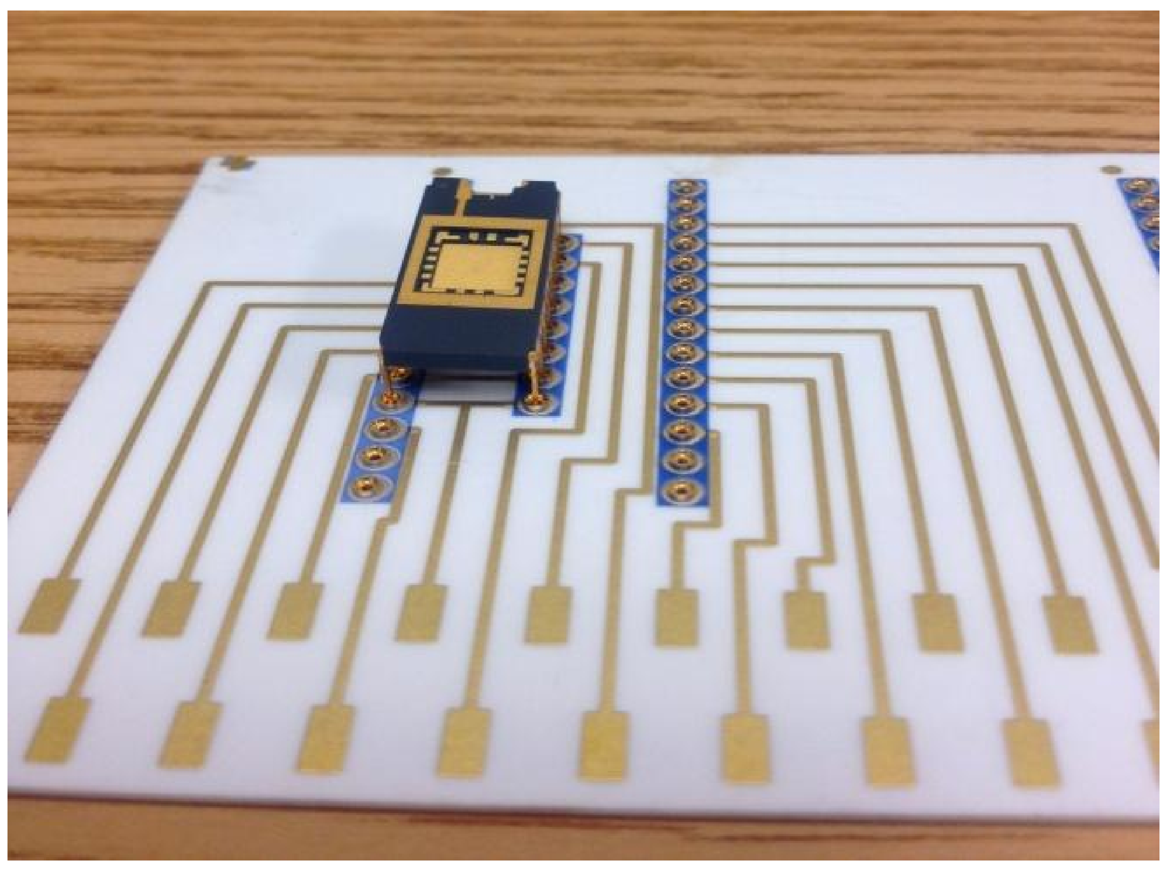

Figure 1.6: An DIP test board for 300°C operation[15].

In Chapter 2 thick film technology is reviewed. Chapter 3 examines the electrical reliability of thick film materials. Leakage current mechanisms in thick film dielectrics are examined in Chapter 4. The adhesive reliability of thick films is detailed in Chapter 5. The conclusions from this research are presented in Chapter 6 along with recommendations for future research.

Chapter 2

Literature Review

Hybrid microelectronics is a packaging and interconnecting technology in which two or more electrical components or devices are combined on a common interconnected substrate to create a specific function. The devices may include unpackaged die or miniature packages mounted on the interconnected substrate surface. The substrate interconnection patterns include conductors, dielectrics, and/or resistors[16, 17, 18]. Figure 2.1 illustrates hybrid microelectronics technology and figure 2.2 is a photo of a hybrid microelectronics circuit. Common hybrid microelectronic substrate techniques are thin film and thick film technology. The development of hybrid microelectronics has demanding requirements for technology, including increased device densities, miniaturization, increased reliability, and reduced cost. These requirements result in challenges in materials and processes[19, 20]. Thick film technology serves an important role in hybrid circuits development with multiple advantages, such as, low product cost, low design cost, reliability in applications with high power, high voltage, and suitable to produce low volume custom circuits and complex arrays[21].

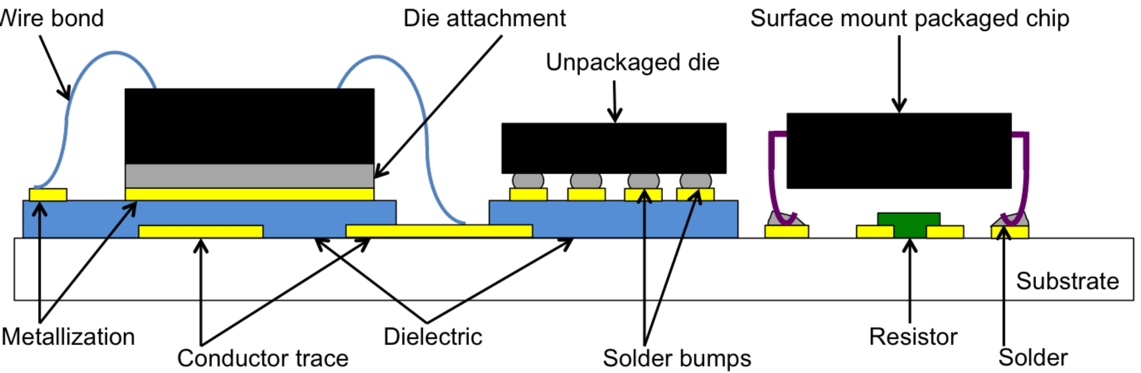

Figure 2.1: Illustration of hybrid microelectronic technology.

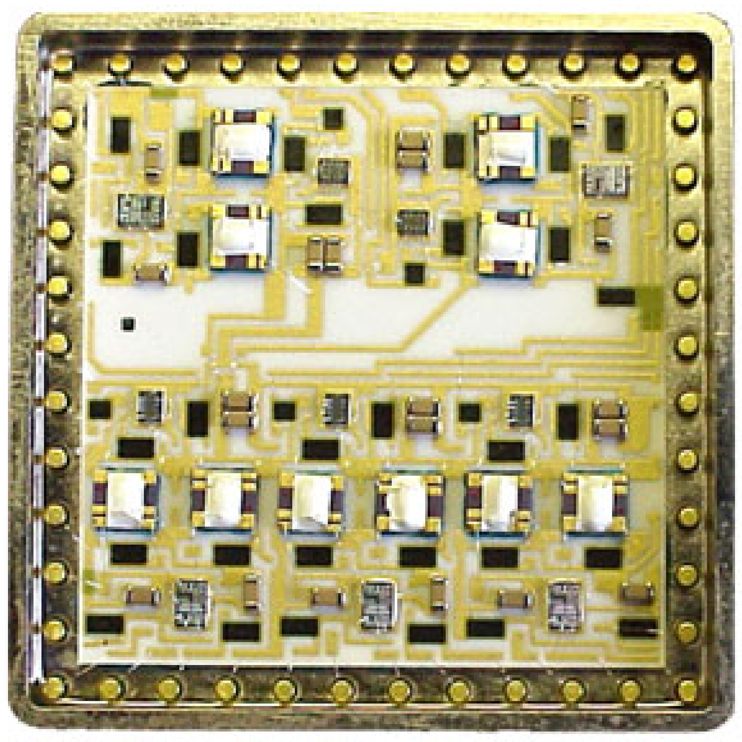

Figure 2.2: A photo of hybrid microelectronics[22].

2.1 Thick film technology

Thick film technology is a method in which specially formulated pastes are screen printed, dried and fired onto substrates to form a film ranging from 8 - 16 μm thick with designed patterns. Based on the differences in formulation and application, thick film pastes are commonly regarded as three different types: conductor, dielectric, and resistor. In hybrid microelectronics, thick film technology is used to produce individual passive components (resistors, capacitors and inductors), interconnections such as conductive circuit traces, metallization for die attachment or wire bonding, and insulation between two conductive traces. Figure 2.3 shows a hybrid circuit based on thick film technology. These applications require that the thick film conductors must be compatible with insulation dielectrics and other adjacent materials. This section introduces the thick film conductor and dielectric with an emphasis on material composition, process, and properties.

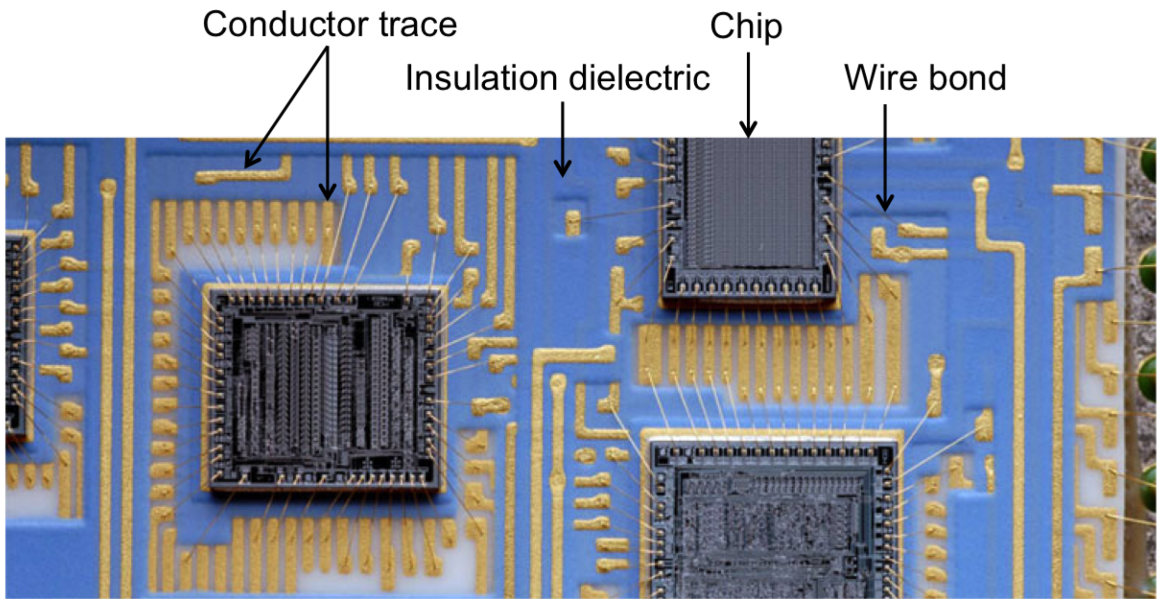

Figure 2.3: Hybrid circuits based on thick film technology. [23].

2.1.1 Conductor

Thick film conductors are used in electronic packaging, primarily, as an electrically conducting material to provide conducting paths, such as signal traces and crossover connections, provide interconnections to the devices and connections to the next level assembly[19].

Compositions

The basic constituents of a thick film conductor typically consists of three phases: functional phase, binder, and organic medium[24]. The functional phase is generally finely divided metal powders, such as gold (Au), platinum (Pt), palladium (Pd), aluminum (Al), silver (Ag), copper (Cu), and nickel (Ni). The permanent binder phase is inorganic and consists of a mixture of glass powders and/or oxides. An organic medium acts as the carrier agent for the functional phase and the binder components, and provides the rheology appropriate for screen printing on the substrates.

a. Functional phase

The functional phases in thick film conductors include noble and base metals, as shown in Table 2.1[25, 26, 27, 28]. These metals are used as powders with particle size ranging from hundreds of nanometers to several micrometers[21]. Table 2.2 compares sheet resistivity, initial and aged adhesion of various conductor types[19].

Table 2.1: Functional phases used in thick film conductors[25, 26, 27, 28].

Element	D	R_e	R_s	T_m	CTE	ρ	C
Noble							
Ag	10.5	1.6	0.64	961	19.7	429	1
Au	19.3	2.3	0.92	1063	14.2	317	70
Pt	21.4	10.5	4.2	1769	9.0	72	100
Pd	12	10.8	4.3	15521	11.7	72	30
Base							
Cu	8.96	1.7	0.68	1083	16.5	401	0.02
Mo	10.2	5.2	2.04	2610	5.1	138	0.07
W	19.3	5.6	2.24	3410	4.6	174	0.06
Ni	8.9	6.8	2.72	1453	13.3	91	0.03

D is density(g/cm);

R_e is electrical resistance($\mu\Omega$*cm at 25°C);

R_s is sheet resistivity(mΩ/sq/25 μm);

T_m is melting point(°C);

CTE is linear thermal expansion coefficient(ppm/°C);

ρ is thermal conductivity(W/m*°K);

C is relative cost.

Table 2.2: Typical properties of various thick film conductors[19].

Conductor	Sheet resistivity(mΩ/sq/12.7 μm)	Initial adhesion	Aged adhesion
Au	3-5	Fair	Fair
AuPt	30-50	Good	Fair
AuPd	5-7	Fair	Fair
Au via fill	20-40	Poor	Poor
Ag	3-5	Good	Good
AgPt	4-6	Excellent	Good
25Ag-1Pd	4-7	Good	Good
6Ag-1Pd	12-16	Good	Good
4Ag-1Pd	15-20	Good	Good
Cu	2-4	Good	Fair
Ni (air fired)	40-70	Fair	Fair

b. Inorganic binders

Thick film binder systems are typically composed of glass and oxide additives[29]. The bonding mechanisms are commonly three types: frit bonding mechanism based on glass binder, reactive bonding mechanism using oxide additives, and flux bonding mechanism resulting from a mixture of glass and oxide additives.

Glasses utilized in thick film perform two primary functions: one is to enhance adhesion and the other is to adjust the sintering kinetics and mechanisms[30]. General requirements of the glasses binders include mechanical strength, corrosion resistance particularly with moisture and acids, and thermal shock resistance. Additionally, the physical properties of glass are related to the requirements of the specific application and substrate type, including thermal expansion coefficient, viscosity as a function of temperature, glass transition temperature, surface-tension/temperature relationship, and compatibility with each material[27].

A variety of borosilicate compositions are added into the glasses, such as Pb and Bi borosilicate, and alkaline earth (Ba, Ca, Mg) borosilicate. The glass composition typically ranges from 1 to 10% in weight in the paste formulation[31, 32, 33, 34]. During the sintering process, the viscosity of the glass changes with temperature, controlling the sintering kinetics of the functional phase. The firing process should produce a densified film without bubble

entrapment, blister formation, exaggerated grain growth, and excessive amounts of glass capillary movement to the fired film surface. Besides, the glass will wet the substrate and produce an enhanced adhesion as ions diffused into the substrate surface grains, forming mechanical and chemical bonds to a certain surface depth. Serving as a binder, it requires that the glass penetrate the functional phase networking, reaching the substrate surface to form mechanical interlockings.

As the viscosity of glass is relevant to the temperature, the firing temperature profile is crucial in the process to prevent a continuous glass film from forming between the functional metal and the substrate. This kind of glass film is undesirable as it will result in brittle fracture and crack propagation at the interface in thermal cycling, power cycling, and low mechanical stresses.

Oxide additives, known as the second class of inorganic binder is also called reactive binder or chemical binder. These types of binders are typically present in concentration of less than 2 wt% of the paste formulation and promote adhesion by forming spinal compounds with the substrate[19]. For example, copper oxide, known as one of the most commonly used oxide binders, enhances the adhesion by forming copper aluminate on the alumina substrate. Reactive binders provide the best bond between noble metals and the substrate by forming oxygen-metal bonds[35].

Flux binders, for example, Bi_2O_3, are typically utilised in thick film paste in less than 5 wt%. Flux bonding mechanism is a mixture of glass bonding and reactive bonding[36].

c. Organic vehicles

Organic vehicles are the medium carrying the functional metal phase and the inorganic binders in thick film. Organic vehicles mainly consist of high molecular weight polymer, low vapor pressure solvent, and usually rheology modifiers. A specific organic vehicle formulation needs to match multiple requirements, such as the compatibility with other thick film composition, the paste manufacturing method, and the application process (deposition method, subsequent processing atmosphere and temperature profile)[19].

Sintering

Sintering is a process in which increased temperature results in the densification of particles from the initially point-contact microstructure to the final neck microstructure. Thick film conductor sintering happens during the firing process and is very complex. It involves several mechanisms, such as solid-state sintering, vitrification, and reactive liquid sintering.

The sintering process can be divided into three stages: initial, intermediate, and final stages. The major focus is on the initial stage, where transfer of material, driven by vapor pressure differences between the neck area and particle surface, results in neck formation.

For solid-state sintering, isothermal neck growth between two spheres can be expressed by a general equation (2.1) and figure 2.4 [37] illustrates the neck formation during initial stage of sintering. The small radius of curvature ρ at the neck indicates a significantly lower vapor pressure than that of the particle. Besides the vapor pressure transfer, numerous mechanisms could occur in the initial solid-state sintering. These mechanisms are summered in table 2.3. Intermediate and final stage sintering are controlled by volume or grain boundary diffusion mechanisms.

$$(\frac{x}{r})^N = Bt \tag{2.1}$$

where:

x is neck radius;

r is particle radius;

N is constant dependent on the sintering mechanism;

B is constant;

t is time.

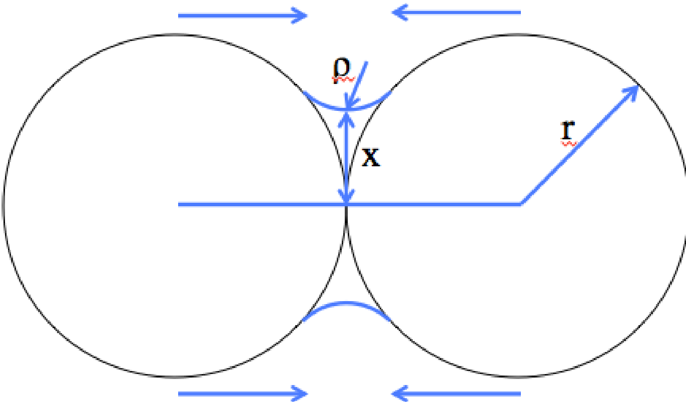

Figure 2.4: Neck formation during initial stage of sintering[37].

Table 2.3: Mechanism for material transport during the initial stage of sintering[19].

Mechanism	Source of material	Sink of material
Vapor pressure transfer	Surface	Neck
Surface diffusion	Surface	Neck
Lattice diffusion	Surface	Neck
Boundary diffusion	Grain boundary	Neck
Lattice diffusion	Grain boundary	Neck

The low temperature glass binders and flux in thick film conductors lead to additional mechanisms that aid in densification at relatively modest time and temperature profile, which are referred to as vitrification and reactive liquid sintering[19]. Vitrification of the glass binders is densification with the aid of a viscous liquid phase. The material is rearanged by viscous flow into the pore region. Reactive sintering is a process in which solid phase dissolves in the glass at high energy region and reprecipitates as solid phase at the low energy region, resulting in increased grain size and densification[38, 39, 40].

Properties

The properties of the fired conductor are determined by the combination of several factors, such as, bulk material properties, conductor formulation, substrate, and the various

processing steps. Common considerations are electrical and mechanical properties, including fired film thickness, conductivity and adhesion.

a. Thickness

The fired film thickness can be measured by numerous instruments, such as light section microscope and surface profilometer. Thickness uniformity can affect properties such as resistivity, adhesion, and solder leach resistance[41].

b. Conductivity

The conductivity is determined by the combination of paste formulation, fired density and thickness[42]. It is important for applications involving rapid signal speed. The electrical conductivity σ is defined in equation 2.2.

$$\sigma = \frac{j}{E} \tag{2.2}$$

where:

j is the electric current density (charge transported through unit area in unit time).

E is the electrical field strength.

In practice, the resistivity, which is the inverse of conductivity, is usually measured. Resistivity is the ability of a material to resist the passage of current. Although surface resistance or line resistance for bulk material is expressed in ohms (Ω), the common expression for thick film conductors is sheet resistivity, which is electrical resistance measured across opposing sides of a square for a normalized thickness, and expressed in milliohms per square (mΩ/sq).

c. Adhesion

Adhesion measures the conductor bonding strength to the substrate. This property is affected by the combination of factors, including but not limited to, specific conductor formulation, substrate, test vehicle, adhesion test preparation, and test method[43]. Commonly used test methods are shear test, peel test and pull test.

2.1.2 Insulator dielectric

Thick film dielectrics are used to provide electrical insulation, mechanical environmental protection, and electrical charge storage[44]. Based on the functional differences, dielectric formulations are categorized as either insulator dielectrics with dielectric constant lower than 15, or capacitor dielectrics with dielectric constant greater than 20[45]. This section focuses on the insulation dielectric materials.

Insulator dielectric materials are commonly regarded as sealing glasses, crossover dielectrics, and multilayer dielectrics.

Sealing glasses, used for environmental, chemical, and mechanical protection, need to meet the application requirements of coefficient of thermal expansion, sealing temperature, hermeticity, chemical resistance, compatibility with other materials, stability at high temperature and humidity, and electrical insulation resistance.

Crossover dielectrics, used as electrical insulation layers between two crossing or overlapping conductor traces, require not only the fundamental properties of a sealing dielectric, but also additional properties, including dielectric strength and minimized interactions with the conductor materials when fired at the same temperature.

Besides the properties of crossover dielectric materials, multilayer dielectric materials, used to build three dimensional interconnect structures, complicate the design by requiring minimum chemical interaction between the dielectric and conductor materials through multiple firings, closely matched coefficient of thermal expansion (CTE) between the dielectric and the substrate materials to prevent warpage on re-firings, and optimum printability not only to retain small via holes (for example, 8 mils in diameter), but also fill in the pinholes created by the printing process[46].

Compositions

Typically, an insulator dielectric formulation consists of insulator glass as the major component and refractory oxides as additives.

Glasses have numerous excellent properties, including high insulation resistance, high dielectric strength, and resistance in humid environments, but not enough mechanical strength at high temperature during firing. The oxide additives, such as Al_2O_3, ZnO_2, SiO_2, and TiO_2 are added into the glasses to enhance high temperature strength, and also modify the CTE of the insulating glass. These thick film dielectrics are referred to as ceramic-filled glasses. During firing of these materials, the glasses melt and the ceramic oxides dissolve in the glass, forming a hermetic structure.

Property and measurement

Commonly measured dielectric properties are dielectric constant, capacitance, dissipation factor, insulation resistance, and dielectric strength.

a. Dielectric constant

The dielectric constant, K, of a material is the ratio of dielectric permittivity, ϵ, of the material to the permittivity, ϵ_o, of a vacuum, as shown in equation 2.3. As insulators, thick film dielectrics are multiphase materials, and the electronic, ionic, and interfacial polarization mechanisms all contribute to the dielectric constant K.

$$K = \frac{\epsilon}{\epsilon_o} \tag{2.3}$$

The K of a material is usually obtained from capacitance measurement of a parallel plate capacitor made from thick film dielectric and conductor materials, as shown in equation 2.4.

$$K = \frac{dC}{\epsilon_o A} \tag{2.4}$$

where:

d is the distance between two electrodes;

C is the capacitance;

A is the area of the electrodes.

b. Dissipation factor

Ideally, electrical energy stored in dielectric materials is not lost, however, in reality, part of the electrical energy supplied in the dielectric materials dissipates in the form of heat. The lost energy is indicated by the dielectric loss factor, which is know as dissipation factor, or tanδ. Equation 2.5 expresses the common measurement of dissipation factor.

$$tan\delta = \frac{\epsilon'}{\epsilon} \tag{2.5}$$

where:

ϵ' is absolute dielectric loss;

ϵ is dielectric permittivity.

The movement of ions, which generates heat, is the main cause of dielectric loss at low frequencies. Mobile ions and free charge carriers in the material can drift when a direct current (DC) electric field is applied. At frequencies greater than 1 KHz, the dielectric loss from mobile ions can be negligible[19].

Glass modifiers, which usually are monovalent or bivalent ions, are randomly distributed in the glass network as open structures[19]. These monovalent or bivalent ions can jump from site to site in the open structure under an electrical field lower than 1 MHz, causing dielectric loss. These ions are not able to follow the electrical field at frequencies greater than 1 MHz.

The porosity in dielectric materials also lead to dielectric loss, since the surfaces of the pores contain large number of crystalline defects, which provide sites for the hopping of ions. The absorption of moisture in the pores can also contributes to the dielectric loss.

c. Insulation resistance

In ceramic materials, electrical charge carriers could be electrons, electron holes, or ions. Dielectrics containing high amounts of alkali metal oxide or semiconducting oxide show low insulation resistance, since alkali metal ions, free electrons and holes have high electronic mobility. Dielectric containing CaO, BaO, PbO and MgO show higher resistivity. Insulation

resistance can be indicated by the ratio of DC voltage and leakage current across a capacitor structure.

d. Dielectric strength

Although the intrinsic dielectric strength of insulator dielectric materials could be very high, the observed dielectric strength of thick film dielectric is usually 10 - 60 V/μm. Intrinsic dielectric breakdown occurs when the electric field levels are sufficient to cause a field emission of electrons in the dielectric. These electrons, accelerated by the electrical field, possess enough energy to generate additional electrons on collision with material, initiating electron avalanches. In thick film manufacturing, mesh marks, pinholes from printing, porosity and nonuniformity of the electrode intensify the local electric field concentration. When the intensified local electric field increases to a level as high as the intrinsic breakdown strength, thick film dielectric breakdown occurs. As the largest defect determines the breakdown strength of the material, increasing electrode area usually indicates higher probability of finding a critical defect and lower dielectric breakdown strength[19].

Dielectric strength is measured by applying an incrementally increasing AC or DC voltage across a capacitor structure until dielectric breakdown occurs. This measurement is affected by multiple factors, including sample preparation, the rate of increase of electric field, and the environment surrounding the sample.

2.1.3 Manufacturing process

Thick film used in hybrid circuits are manufactured by screen printing, followed by drying and firing steps.

Screen printing

Screen printing is used to deposit thick film paste on substrates with a specific pattern. The important process variables in screen printing include screen printer setup parameters (snap off distance, speed, pressure), squeegee hardness, and screen details (wire diameter,

mesh opening size, emulsion thickness, and screen tension)[47]. Figure 2.5 illustrates the screen printing process.

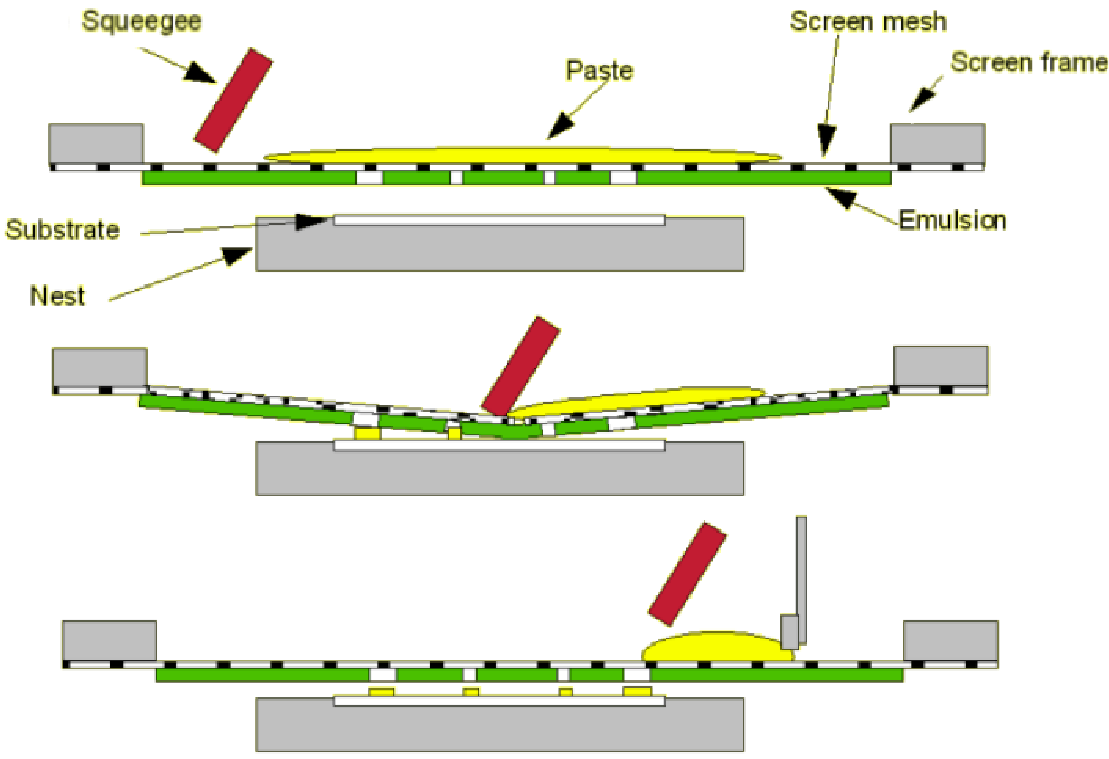

Figure 2.5: Illustration of screen printing in thick film technology[48].

Drying

After screen printing, thick film pastes are dried to evaporate the solvents from the printed film. The drying process is influence by air flow rate, drying temperature and time. Due to the high ratio of surface area to volume of deposited films and the boiling points ranging from 180°C to 250°C for most commonly used solvents, typical drying profiles are 80°C to 160°C for 10-30 minutes, which removes most of the solvent from the wet films.

There are two types of dryers: box furnaces with convection heating, used for batch processing with small to medium production volumes, and belt furnaces, providing ease of process automation and enabling the utilization of a common belt for both drier and firing furnace in some automated production lines.

Firing

In the firing process, the organic removal requirements help to determined the temperature profile. The organic material must be removed from the paste, typically by pyrolysis prior to the melting of the glass phase. The peak temperature and time depended on the thick film compositions. Typical firing profiles have 10 minutes peak at temperatures ranging from 500°C to 980°C[49, 50]. The required time-temperature profile depends on the specifics of the glass melting and metal sintering for the particular paste formulation.

Belt furnaces with several zones are commonly used to fire thick films. The zone temperature can be controlled independently and the belt moves through these heating zones at a constant speed. The air flow rates control the atmosphere inside the belt furnace for most thick films while special designs are utilized in special circumstances. For example, copper conductors are fired in a N_2 atmosphere. Figure 2.6 illustrates the paste morphology during the process.

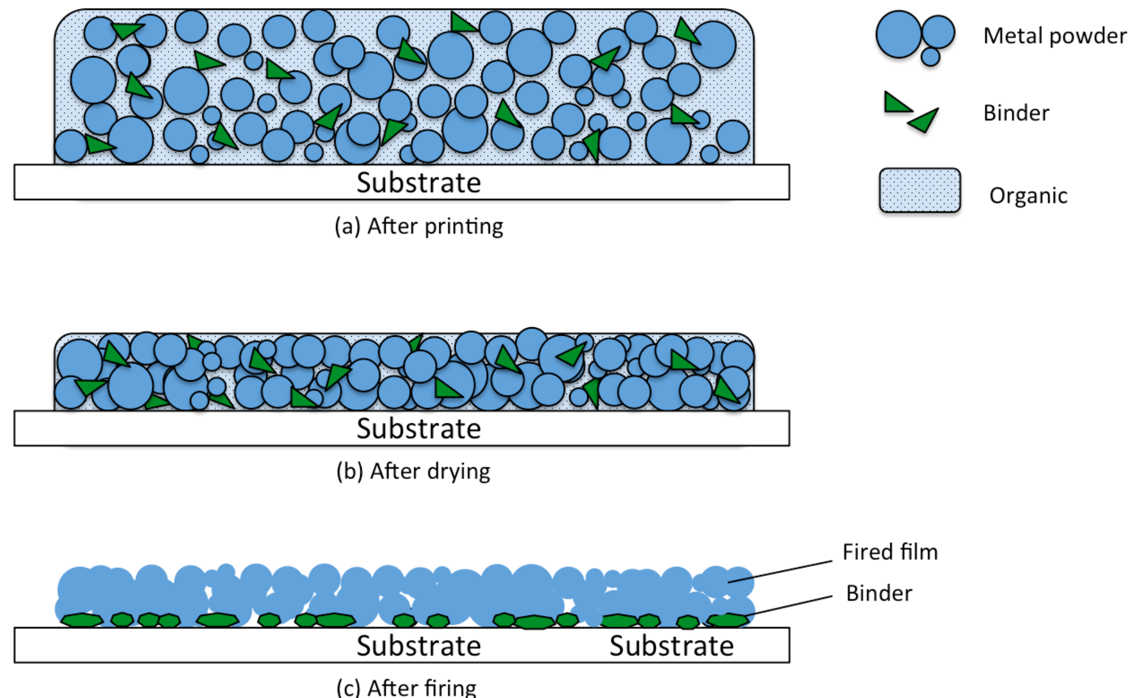

Figure 2.6: Illustration of thick film morphology during process.

2.2 Gold thick film

With the growth of microelectronics industry over the past decades[51, 52, 53, 54, 55], gold based thick film have been firmly established in commercial use. Table 2.4 lists the properties of various commercial gold based thick film conductors.

Table 2.4: Properties of gold based thick film conductors[56, 57, 58].
("R_s" is Sheet resistivity. "Res" is Line resolution.)

Ink	R_s (mΩ/squ)	Res (μm)	Solids (%)	Au wire bondability
Heraeus C5729	≤ 5.5	150	86.5	2 mil wire, initial: $\geq 20g$
Heraeus C6029	≤ 9.5	200	84.0	-
DuPont 5771	≤ 7.0	150	84.0	2 mil wire, initial: $\geq 35g$
Dupont 5715R	≤ 6.5	175	-	2 mil wire, initial: $\geq 40.5g$

Pure Au conductor formulations are chemically inert, and exhibit high conductivity, excellent resistance to corrosion or migration, and excellent wire bondability with Al and Au. Therefore, Au thick films are selected for applications in military, space, and extreme environments. These applications require highly reliable interconnections, resistor terminations, high frequency stripline configurations and pads for wire bonding or die attachment. On the other hand, Au thick film application is limited by its high cost and incompatibility with commonly used Sn-Pb solders[24, 59].

Since Pt is more costly and has 5 times higher resistivity than Au, it is usually used in the pure form only for high temperature applications. Adding Pt into Au increases the resistivity but improves Sn/Pb solderability[60]. When discrete components are attached with solder or components need to be replaced frequently, Au-Pt thick film conductors are suitable for the applications[61]. Adding Pd to Au can obtain properties similar to those of Au-Pt while reducing cost. These Au-Pd formulations provide alternative solutions to situations where Ag cannot be used due to Ag migration[62, 63] and Au-Pt pastes are beyond the budget. In addition to binary Au alloy, ternary alloy are utilized to optimize properties of interest. For example, Au-Pt conductors do not typically fire to high densities and tend to crack[19].

Adding small amounts of Pd increases the density of the fired film by forming a Au-Pt-Pd alloy, which is suitable for high temperature process and application.

The fired Au thick film morphology is affected by multiple factors, including firing temperature and particle size. Individual Au particles could be observed after films were fired below 600°C, but these metal particles sintered and formed uniform films when fired at 800°C.(Figure 2.7)[50]. Smaller particles (0.5 μm in diameter) are less stable and trend to sinter at relatively lower temperature (600°C) during firing (Figure 2.8)[50].

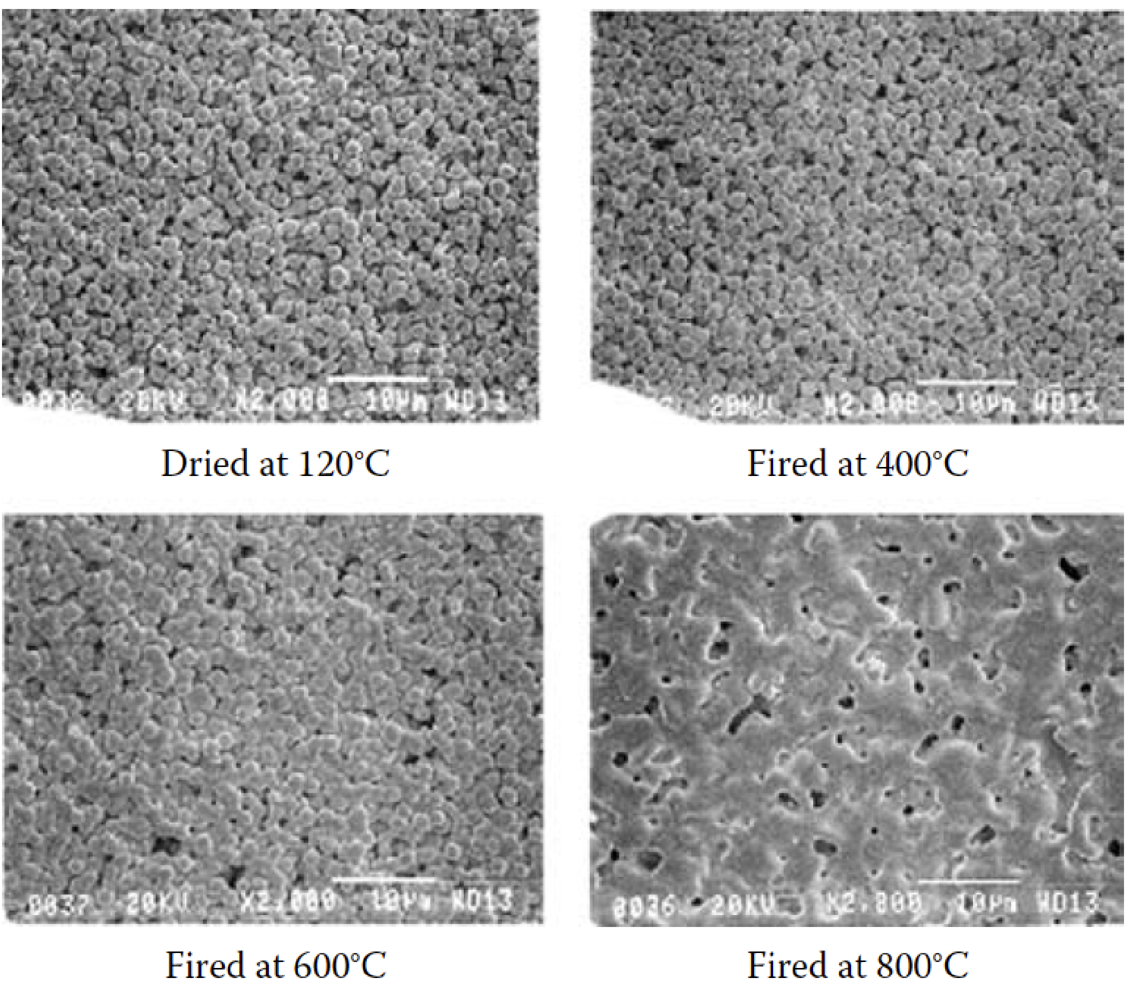

Figure 2.7: Gold film morphology after firing at various temperature[50].

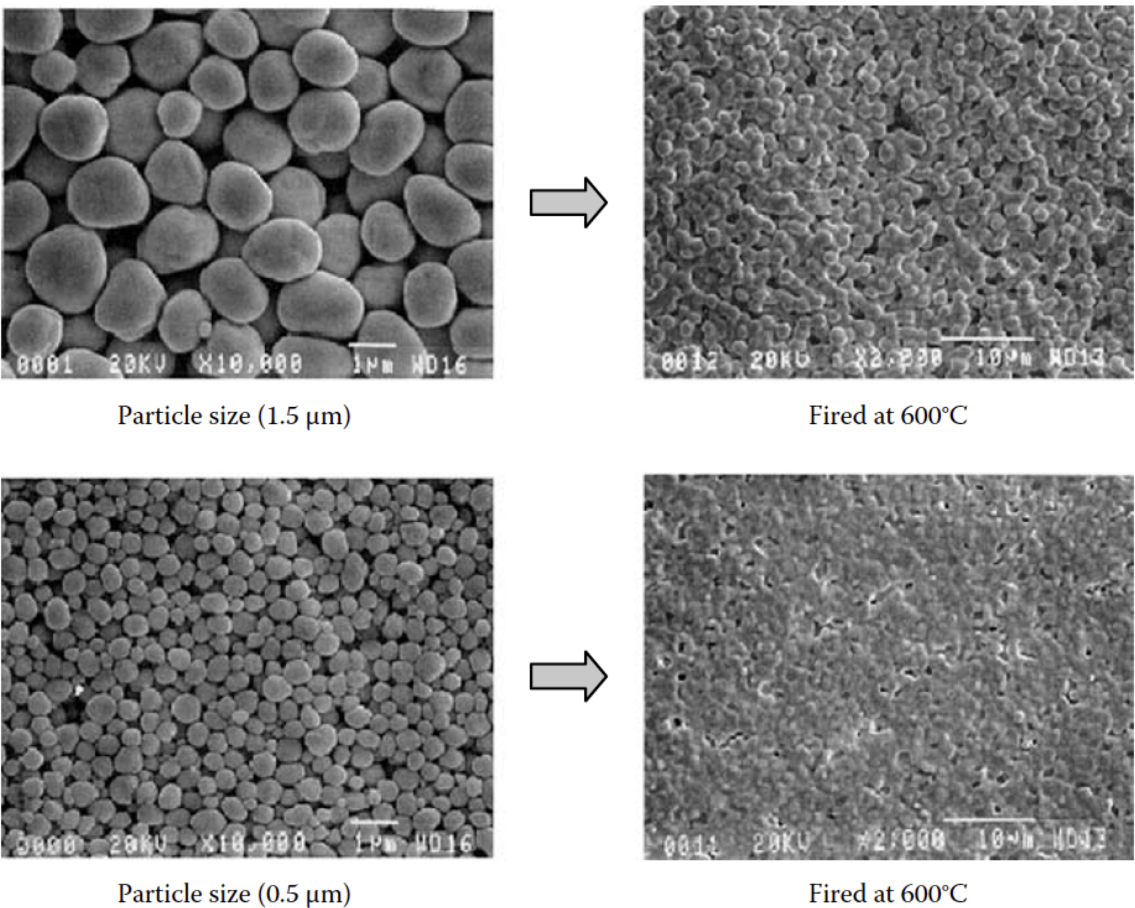

Figure 2.8: Fired gold film morphology affected by particle sizes[50].

2.3 Thick film gold in high temperature application

Gold based thick films on Al_2O_3, AlN, Si_3N_4 have been examined by a number of researchers[64]. Salmon, et al. had previously demonstrated thick film paste, DuPont 5771, was capable of operation at a temperature of 500°C[65]. Riches, et al. studied the reliability of wire bond interconnections of Au and Al-1%Si wire when bonded to Au and Ag-Pd thick film on Al_2O_3 respectively[66]. The results showed that the Au wire system was stable after storage for 1300 and 2500 hours at temperatures of 200, 225 and 250°C. Figure 2.9 shows SOI devices assembled on ceramic substrates for assessment of electrical performance at 250°C. Chen, et al. had electrically characterized ceramic substrates and Au thick-film metallization based packages at temperatures up to 550C[67, 68].

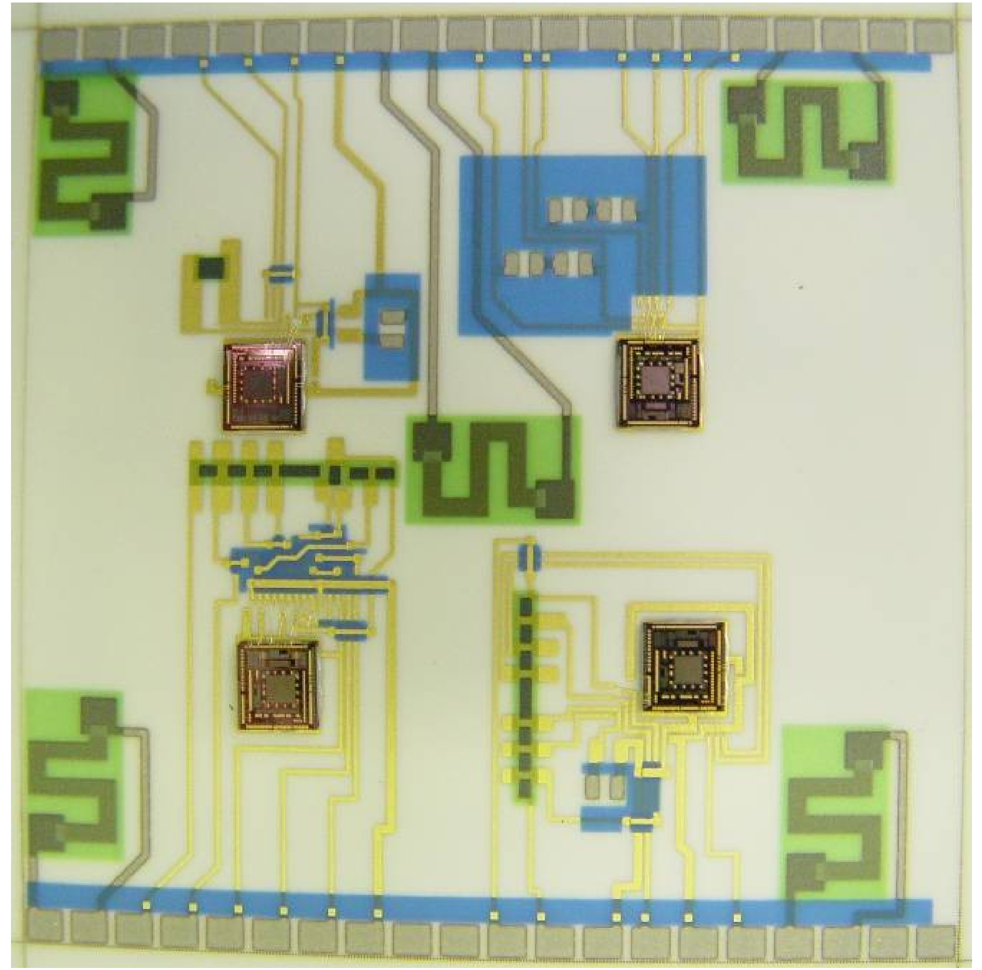

Figure 2.9: SOI devices assembled on ceramic substrates for assessment of electrical performance at 250°C.[66].

Palmer, et al. had examined Au thick film metallization on Al_2O_3 and Si_3N_4 ceramic substrates[69]. AuGe die attach was successfully demonstrated using Cr/Pt/Au backside die metallization and 5771 Au on Al_2O_3 in 300°C storage tests for 2000 hours. AlN71 thick film Au was evaluated for use on Si_3N_4. While Si_3N_4 had desirable mechanical properties, no compatible thick film conductor inks had been identified (2006). Hagler, et al. evaluated the first generation thick film Au (2010) for Si_3N_4 substrates, including Au paste chemistry control and surface engineering[70]. Figure 2.10 shows the Au thick film metalization on a Si_3N_4 substrate.

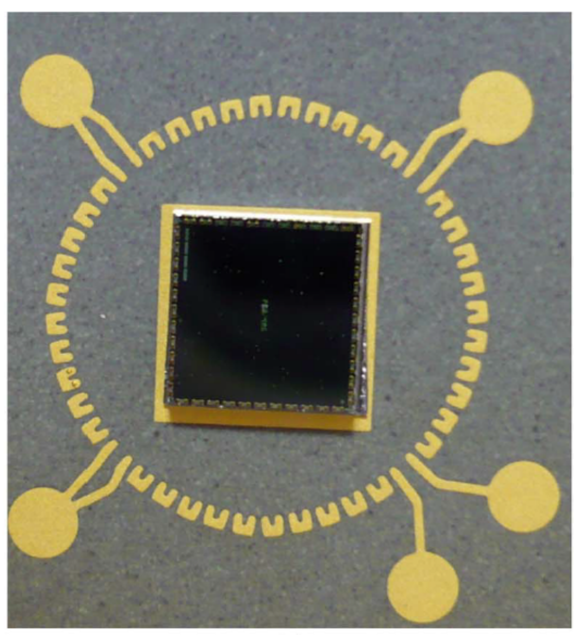

Figure 2.10: Au thick film on the Si_3N_4 substrate[70].

Zhang, et al. characterized the electrical properties of thick film Au DuPont 5771 and dielectric DuPont 5951 by measuring test vehicles shown in Figure 2.11[49]. The capacitance and dissipation factor can be measured by numerous instruments, for example, an Agilent 4129A LF impedance analyzer. Figure 2.12 illustrates the testing fixture designed to measure the capacitance and dissipation factor. The test sample was held by an aluminum substrate. Four 1-meter (electrical length) coax cables were connected to the capacitor via spring and screw, through a glass ceramic. When placed inside a heating oven, the testing fixture can measure the capacitance and dissipation factors as a function of temperatures. Tests included the leakage current, capacitance, and dissipation factor, each as a function of temperature in the range of 25-300°C, as shown in figures 2.13-2.18.

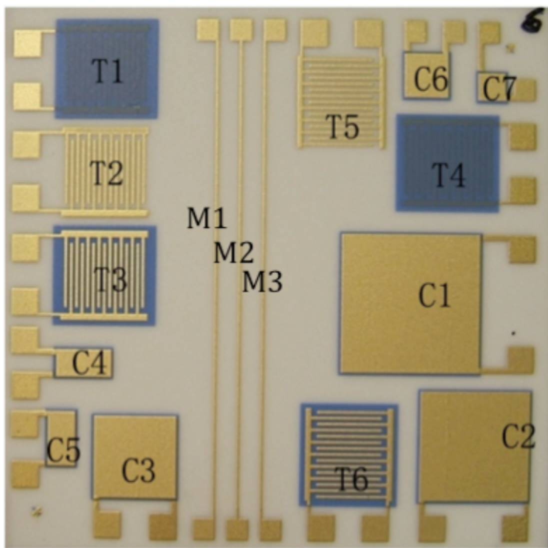

Figure 2.11: Electrical test vehicle[49].

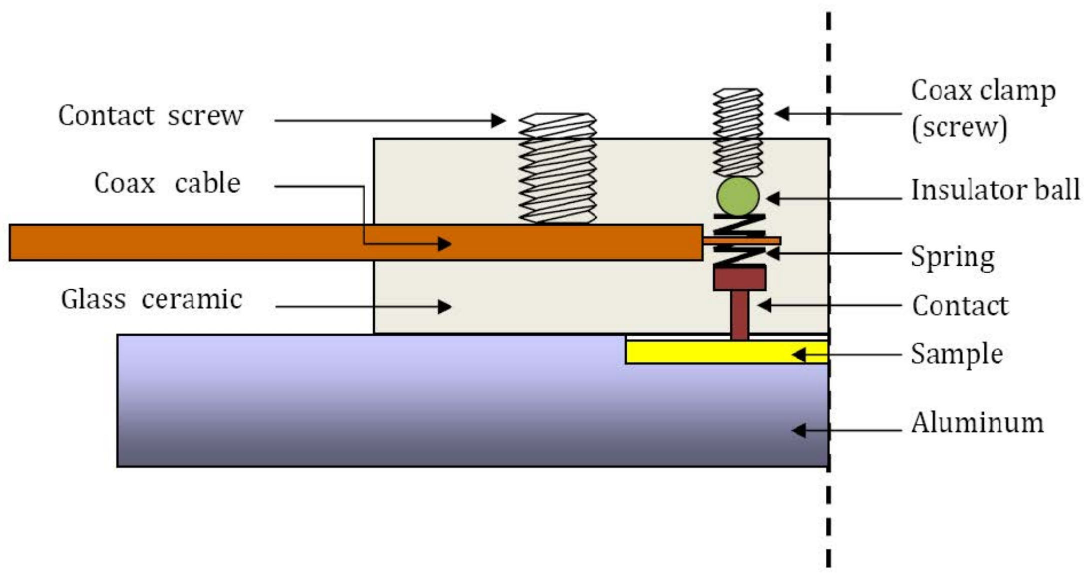

Figure 2.12: Illustration of testing fixture for capacitance and dissipation factor measurements[49].

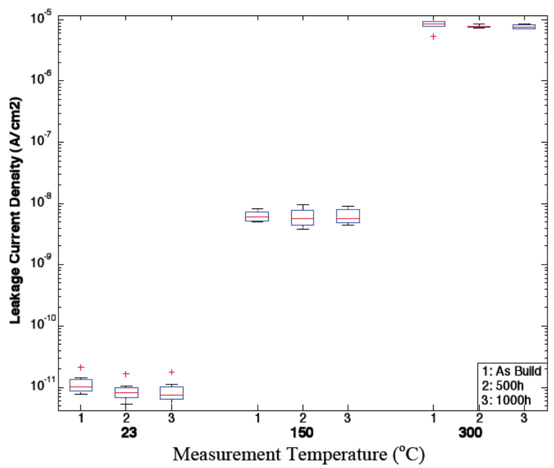

Figure 2.13: Leakage current at 100 V bias as a function of storage time at 320°C[49].

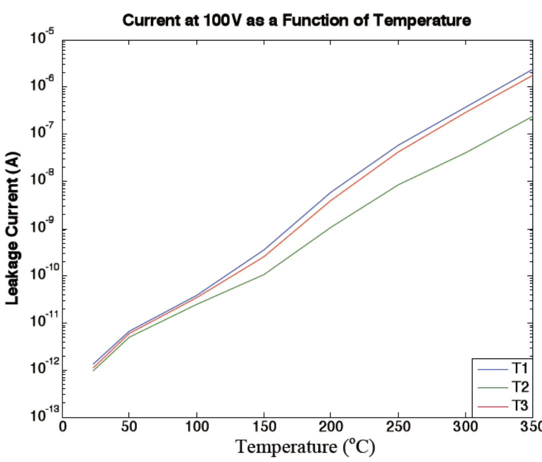

Figure 2.14: Initial leakage current at 100V bias as a function of temperature.[49].

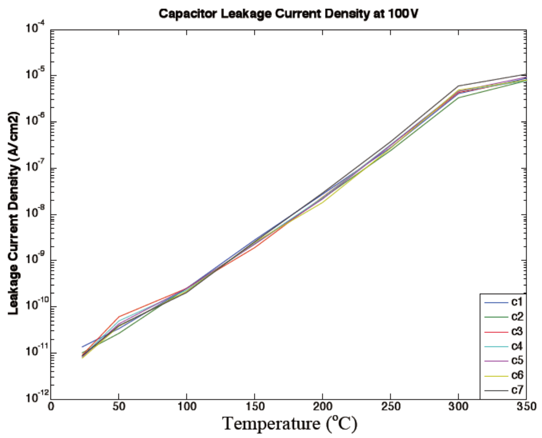

Figure 2.15: Initial leakage current as a function of temperature (patterns T1, T2, and T3)[49].

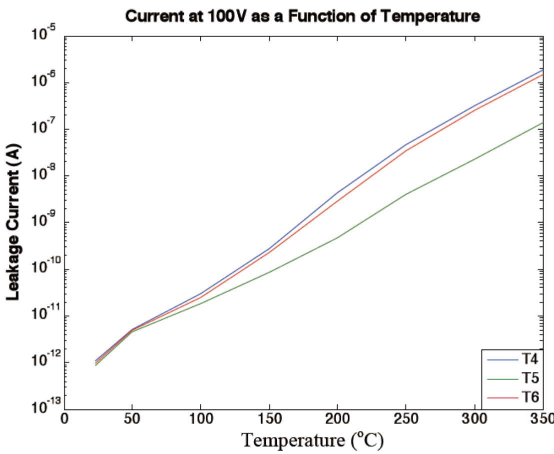

Figure 2.16: Initial leakage current as a function of temperature (patterns T4, T5, and T6)[49].

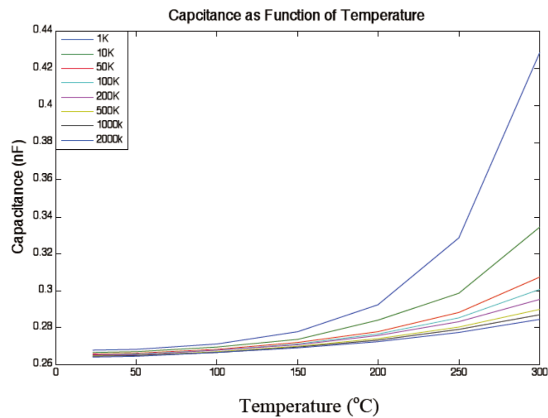

Figure 2.17: Initial capacitance as a function of frequency and temperature[49].

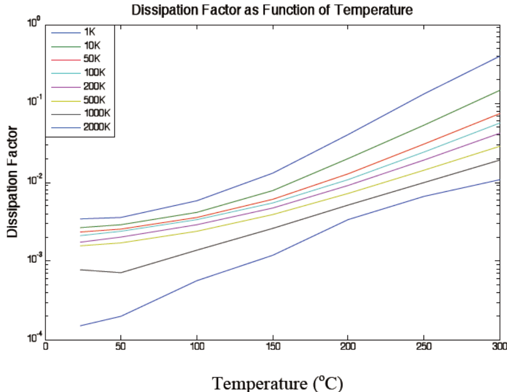

Figure 2.18: Initial dissipation factor as a function of frequency and temperature[49].

Zhang, et al. also studied the effect of 300°C storage on the adhesion of two different thick film Au conductors (DuPont 5771 and 5725) with a multilayer dielectric (DuPont 5951) on Al_2O_3 substrates by pull test. The test vehicles are fabricated in capacitor structures show in figure 2.19)[49].

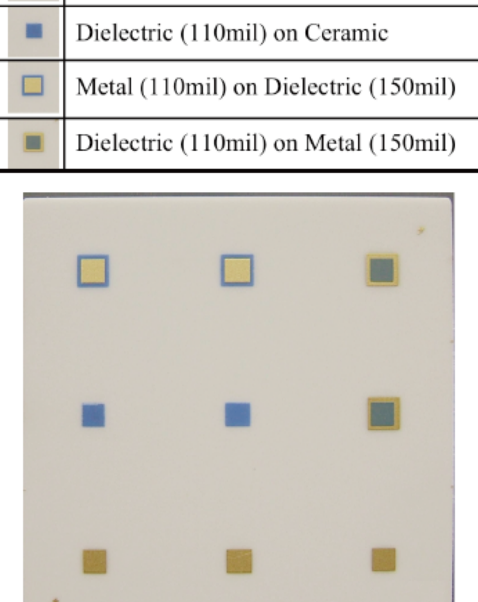

Figure 2.19: Adhesion test vehicle[49].

In pull testing used in this research, the substrate was diced into individual pads. A ceramic plate with epoxy coating was attached to the backside of the sample to strengthen the substrate. An aluminum stud with an epoxy coated head was aligned and cured to the surface of thick film test pad. A mounting clip was used to hold the assembly during epoxy cure. After curing, the test was conducted by a pull test machine, where a perpendicular force with controlled increasing rate was applied to the stud end until sample failure. Figure 2.20 illustrates the process of pull testing.

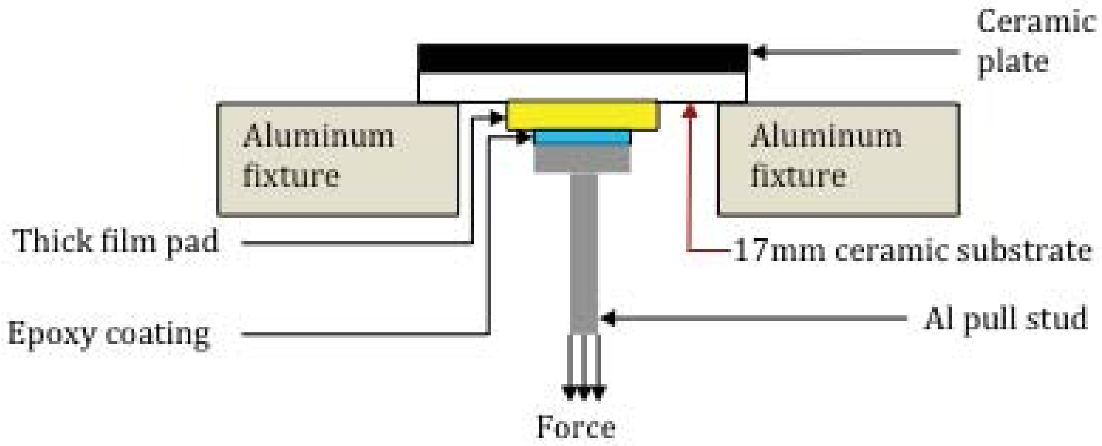

Figure 2.20: Illustration of pull testing.[71].

When fabricated based on the manufacturer's recommendations, Au conductor 5771 and dielectric 5951 presented relatively stable adhesion in 320°C storage up to 2000 hours, as shown in figure 2.21[49]. However, the Au conductor 5725 had a significant decrease in adhesion from the earliest test interval (500 hours), as shown in figure 2.22, and all of the metal was pulled off from the ceramic and from the dielectric with low strength[49].

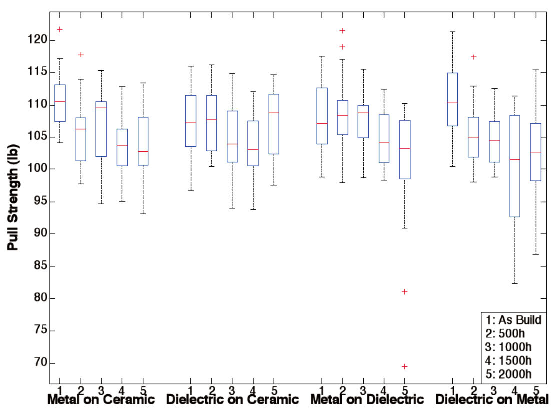

Figure 2.21: Pull strength as a function of aging (320°C) for DuPont conductor 5771 and dielectric 5951 fired at 980°C[49].

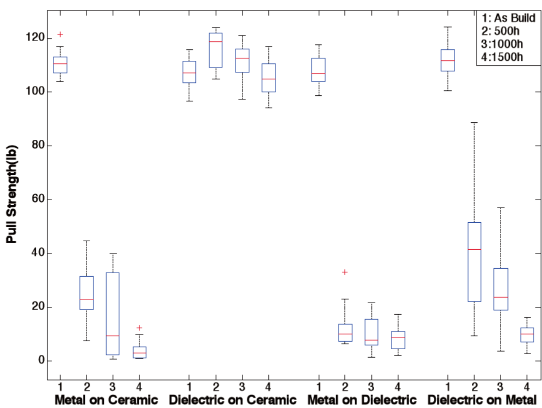

Figure 2.22: Pull Strength as a Function of Aging (320°C) for DuPont Conductor 5725 and Dielectric 5951 fired at 850°C[49].

Zhang, et al. also studied the failure mechanism in the thick film materials for 300°C operation[71]. They fabricated capacitor structures with two thick film conductors (Au and PtPdAu) and a dielectric, and applied bias voltage with alternative directions to the electrodes during 300°C aging. Figure 2.23 shows the electrical test vehicle. As shown in figures 2.24-2.25, the leakage current increased during the first few minutes after voltage was applied to the electrode, and gradually decreased, indicating mobile ion in the materials.

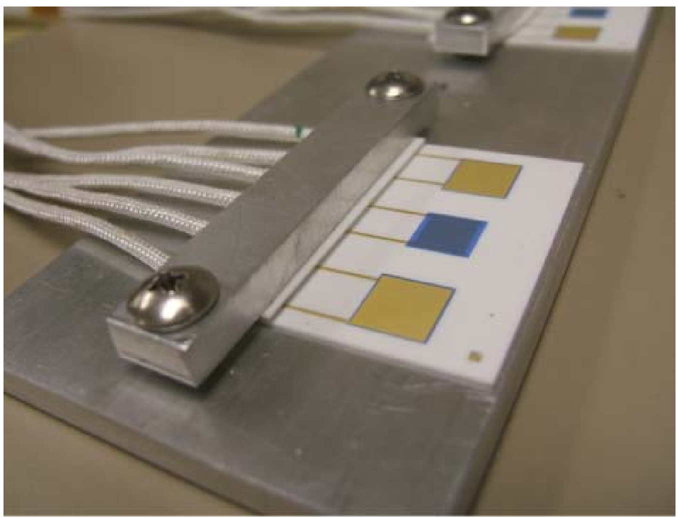

Figure 2.23: Wires held on test vehicle.[71].

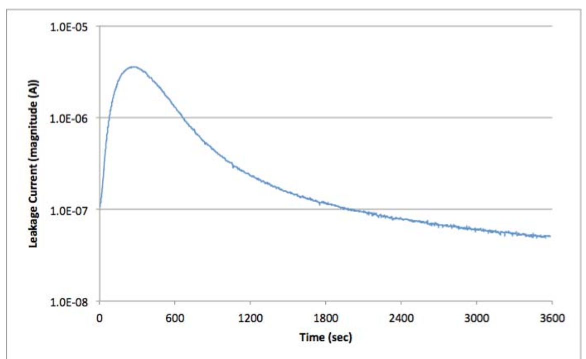

Figure 2.24: Leakage current at 300°C and 100 V as a function of time. The top electrode was positive biased for an hour and reversed at 0 second. [71].

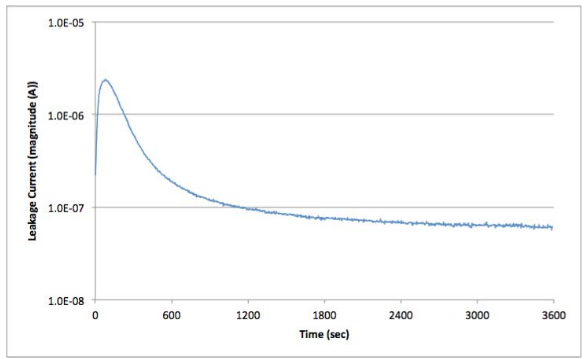

Figure 2.25: Leakage current at 300°C and 100 V as a function of time. The bottom electrode was positive biased for an hour and reversed at 0 second.[71].

Zhang et. al, also measured the adhesion of the capacitors before and after 320°C aging, with or without biased voltage. The pull strength of all test vehicles shown in figure 2.19 remained relatively constant during all test intervals from 0-2000 hours without bias. Figure 2.26 shows pull strength of test vehicles fabricated with Au and dielectric (fired at 980°C) during aging at 320°C, without bias. Figure 2.27 pull strength of test vehicles fabricated with PtPdAu and dielectric (fired at 850°C) during aging at 320°C, without bias.

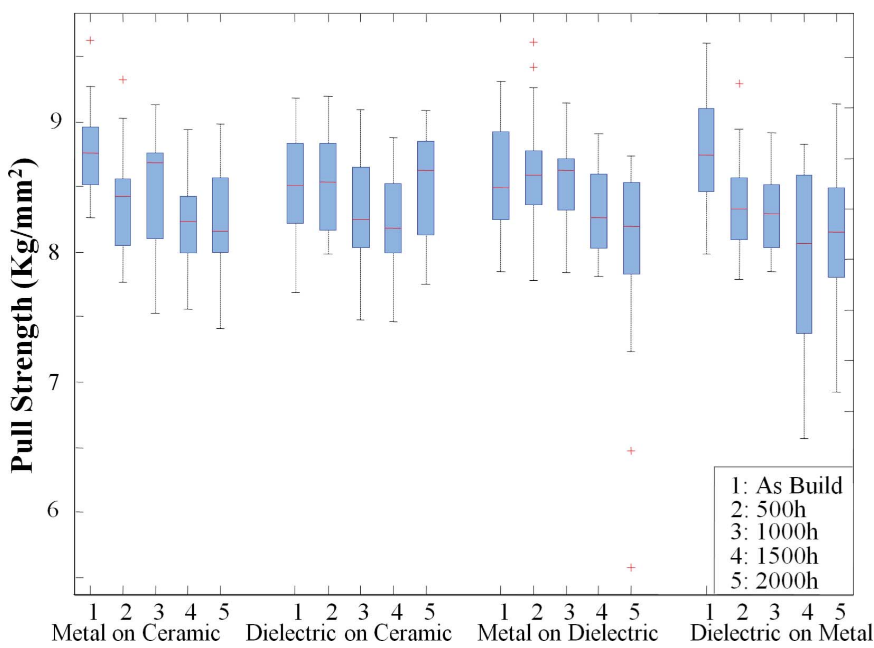

Figure 2.26: Pull strength as a function of aging (320°C) for Au conductor and dielectric (fired at 980°C), without bias[71].

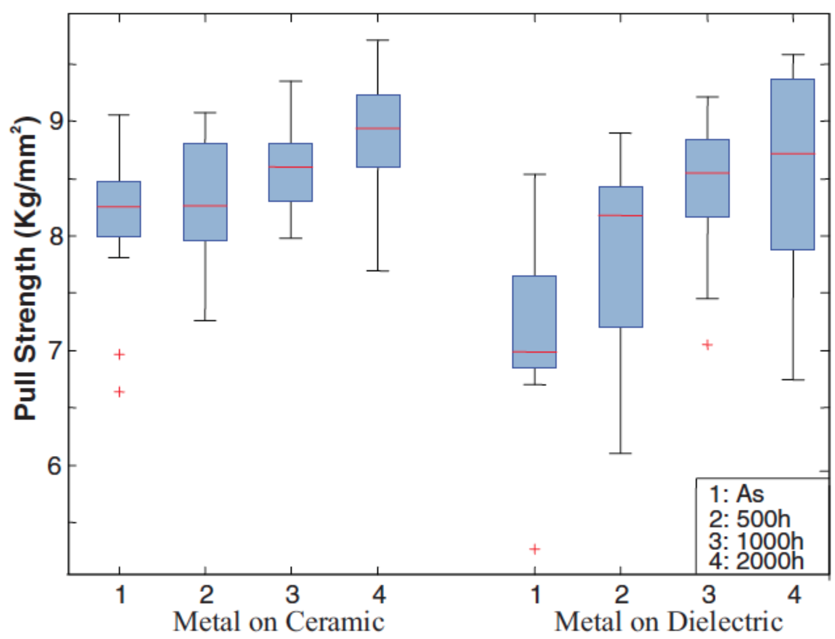

Figure 2.27: Pull strength as a function of aging (320°C) for PtPdAu conductor and dielectric (fired at 850°C), without bias[71].

However, after the biased voltage was applied on the test vehicles shown in figure 2.28, failure occurred. For test vehicles built with Au conductor, all of the initial (t = 0) failures were within the epoxy and the average pull strength was 8.7 kg/mm^2. This was consistent with the previous results. After 250 hours biased aging at 300°C, there was significant adhesion degradation for test vehicles built with the Au conductor. For vehicles with the positive bias voltage applied to the top conductor, the average pull strength was 0.51 kg/mm^2, with the dielectric and the top conductor pulled off, exposing the bottom conductor, as shown in figure 2.29 (a). The bottom conductor was also lifted, indicating adhesion loss at the bottom conductor-to-ceramic interface. For samples with positive bias voltage applied to the bottom conductor, the average pull strength was 1.12 kg/mm^2, with the top conductor pulled off from the dielectric, as shown in figure 2.29 (b). Discoloration of the dielectric was also observed as shown in figure 2.29 (b).

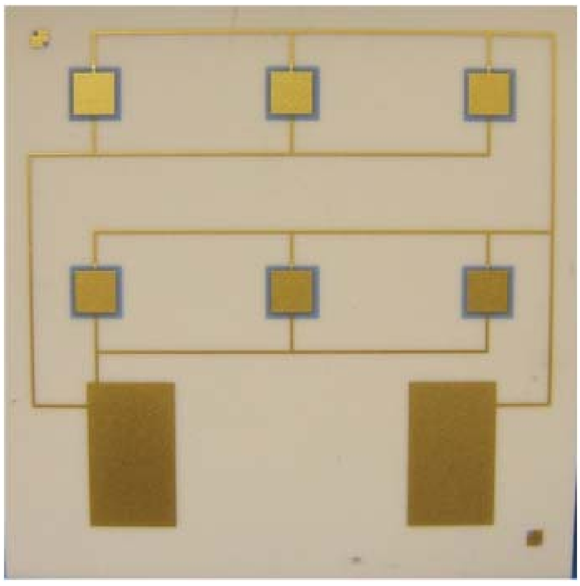

Figure 2.28: Biased adhesion test vehicle[71].

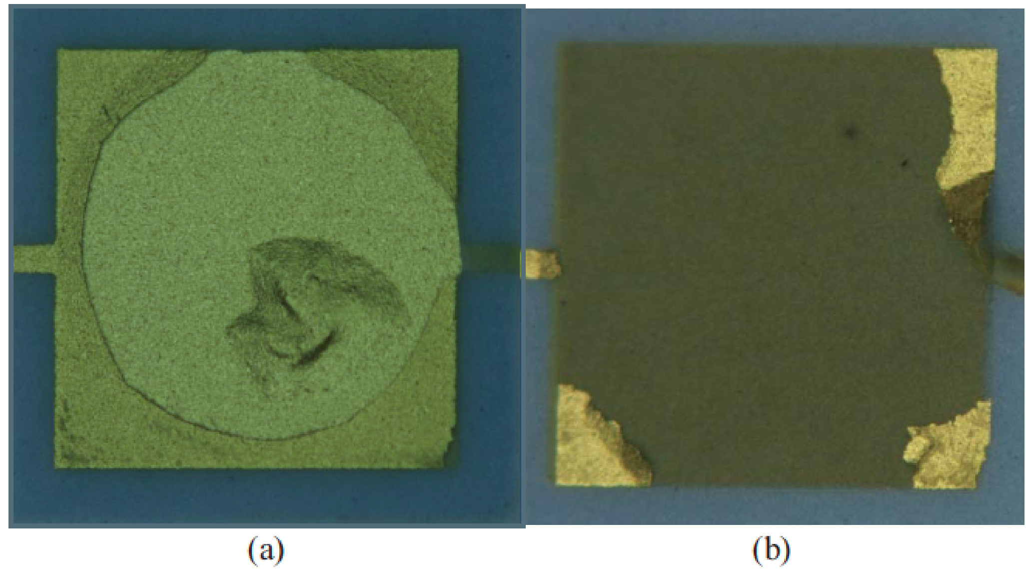

Figure 2.29: Pull test failure mode for bias aging with Au conductor. (a) Positive bias voltage applied to the top conductor. (b) Positive bias voltage applied to the bottom conductor.[71].

For PtPdAu conductor samples with positive bias voltage applied to the top conductor, the top conductor and dielectric pulled off from the bottom conductor for most of the samples. No significant lifting of the bottom metal was observed. For samples with positive bias voltage applied to the bottom conductor, the top conductor pulled off from the dielectric on most samples. In both cases, there were some samples that had small areas with all three layers pulled off, the same as was observed in the pull testing of as-built samples. For both bias polarities, the average pull strength was 7.7 kg/mm^2 after 250 hours of biased aging, significantly higher than the aged Au test vehicles. The decrease in aged PtPdAu adhesion and change in the failure mode compared to time zero indicates some adhesion degradation.

Failure analysis identified that Na in the glass binder of the Au conductor and in the dielectric resulted in leakage current and adhesion loss with high temperature biased aging.

Na was used in both the thick film Au conductor glass binder and in the dielectric as a glass network modifier to alter the network structure. At conventional temperatures ($\leq 125°C$), Na migration would be substantially reduced due to the decreased mobility. In

high temperature applications, Na in the thick films as the modified glass binder would result in issues in electrical and mechanical reliability.

Based on the previous studies, thick film gold for high temperature application must be evaluated in aging with bias.

Chapter 3

Electrical Reliability of Thick Film Materials

The electrical reliability of thick film materials was evaluated by measuring the leakage currents of capacitor and interdigitated finger structures in high temperature aging. The leakage current test vehicles, which were fabricated with two thick film conductors and two dielectrics with various thicknesses, were aged at 300°C for 2000 hours with 100 V bias applied in each polarity. The leakage current increased significantly after a short time aging, only when the conductor layer was printed with PtPdAu and thin dielectric (D1: 20 μm, D2: 30 μm). Cross sections and EDS analysis showed that Bi in the PtPdAu paste diffused into dielectrics, D1 and D2, during the firing process and resulted in an significant increase in leakage current. The maximum leakage current increase was directly correlated to the electrical polarity. With positive bias voltage on the top electrode, test vehicles showed a higher increase in leakage current compared to the ones with positive bias voltage on the bottom electrode. When the electrical polarity was alternated during aging, the leakage current decreased immediately, then increased again.

3.1 Experiment method

Two conductive thick film pastes (PtPdAu, Au) and two thick film dielectric pastes (D1, D2) were selected to fabricate capacitor and interdigited finger structures.

The leakage current test vehicle included two capacitor patterns (10.2 mm square) and one interdigitated finger pattern (254 μm line and space) on a 50 mm x 50 mm alumina substrate. Figure 3.1 shows the test vehicle design of the leakage current test vehicle. Figure 3.2 illustrates the cross section schematic of the thick film capacitor pattern.

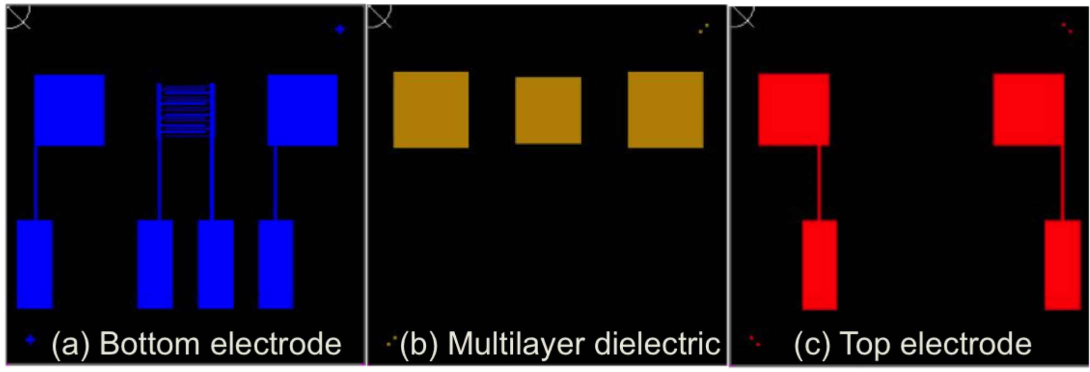

Figure 3.1: Design of the leakage current test vehicle. (a) Pattern for bottom electrode. (b) Pattern for multilayer dielectric. (c) Pattern for top electrode.

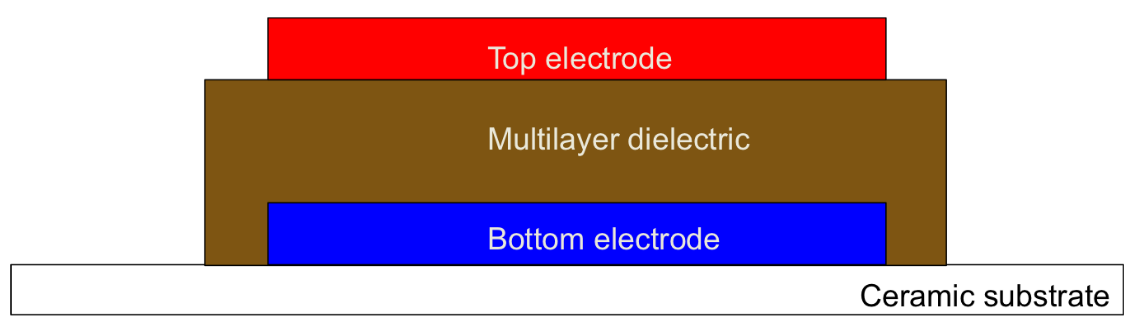

Figure 3.2: The cross section of the thick film capacitor

Two screens with different parameters (listed in table 3.1) were used to produce various dielectric thicknesses. The thickness of the wet, dried, and fired films are listed in tables 3.2. All thick film conductors and dielectrics were screen printed at room temperature, dried at 150°C for 10 minutes, and fired at 850°C for 10 minutes. After the bottom capacitor electrodes and interdigitated finger patterns were printed on 96% Al_2O_3 ceramic substrates, dried (150°C) and fired (850°C), two layers of thick film dielectric D1 or three layers of thick film D2 were printed over the capacitor bottom electrode and the interdigitaged finger patterns. Each dielectric layer was sequentially printed, dried (150°C) and fired (850°C). Finally, the top capacitor electrode conductor was printed, dried (150°C) and fired (850°C).

Table 3.1: Parameters of screens applied in test.

Screen type	Wire mesh	Wire diameter	Emulsion
325	325	0.9	0.5
250	250	1.6	0.5

Table 3.2: Film thickness of conductor and dielectric materials per layer, printed with different screens.

Materials	Wet thickness (μm)	Dried thickness (μm)	Fired thickness (μm)
Screen 325			
PtPdAu	23 - 27	15 - 19	8 - 11
Au	21 - 25	12 - 16	5 - 8
D1	—	14	10
D2	—	14	10
Screen 250			
PtPdAu	35 - 39	21 - 25	12 - 16
Au	33 - 37	20 - 22	8 - 11
D1	—	21	15
D2	—	21	15

In this research, the conductors were fabricated with the thicknesses recommended in the manufacturer's instructions. Dielectric thicknesses were fabricated at two thicknesses: the "thick dielectric" corresponded to the recommended dielectric thickness on the paste manufacturer's instructions, and the "thin dielectric" was 10 μm less than recommended value. Table 3.3 lists the conductor and dielectric thicknesses.

Table 3.3: Fired conductor and dielectric thicknesses.

Conductor	Thickness (μm)	
PtPdAu	12 - 16	
Au	8-11	
Dielectric	Thin (μm)	Thick (μm)
D1	20	30
D2	30	40

The leakage current samples were fabricated with various material combinations and dielectric thicknesses. The test groups, Thin 1-Thin 12, were fabricated with two conductors

(PtPdAu, Au) and two thin dielectrics (D1: 20 μm, D2: 30 μm). The test groups, Thick 1-Thick 12, were fabricated with two conductors (PtPdAu, Au) and thick dielectrics (D1: 30 μm, D2: 40 μm). All test vehicles were aged at 300°C with 100 V bias voltage in two polarities. Tables 3.4-3.5 list all the test groups with materials, dielectric thicknesses, and bias polarities.

Table 3.4: Thin dielectric test groups with various materials, dielectric thicknesses T_d, and polarities.

No.	Materials	T_d (μm)	Polarity
Thin 1	PtPdAu/D1/PtPdAu	20	Positive bias on the top electrode
Thin 2	PtPdAu/D2/PtPdAu	30	Positive bias on the top electrode
Thin 3	Au/D1/Au	20	Positive bias on the top electrode
Thin 4	Au/D2/Au	30	Positive bias on the top electrode
Thin 5	PtPdAu/D1/PtPdAu	20	Positive bias on the bottom electrode
Thin 6	PtPdAu/D2/PtPdAu	30	Positive bias on the bottom electrode
Thin 7	Au/D1/Au	20	Positive bias on the bottom electrode
Thin 8	Au/D2/Au	30	Positive bias on the bottom electrode
Thin 9	PtPdAu/D1/PtPdAu	20	Interdigitated finger structure
Thin 10	PtPdAu/D2/PtPdAu	30	Interdigitated finger structure
Thin 11	Au/D1/Au	20	Interdigitated finger structure
Thin 12	Au/D2/Au	30	Interdigitated finger structure

Table 3.5: Thick dielectric test groups with various materials, dielectric thicknesses T_d, and polarities.

No.	Materials	T_d (μm)	Polarity
Thick 1	PtPdAu/D1/PtPdAu	30	Positive bias on the top electrode
Thick 2	PtPdAu/D2/PtPdAu	40	Positive bias on the top electrode
Thick 3	Au/D1/Au	30	Positive bias on the top electrode
Thick 4	Au/D2/Au	40	Positive bias on the top electrode
Thick 5	PtPdAu/D1/PtPdAu	30	Positive bias on the bottom electrode
Thick 6	PtPdAu/D2/PtPdAu	40	Positive bias on the bottom electrode
Thick 7	Au/D1/Au	30	Positive bias on the bottom electrode
Thick 8	Au/D2/Au	40	Positive bias on the bottom electrode
Thick 9	PtPdAu/D1/PtPdAu	30	Interdigitated finger structure
Thick 10	PtPdAu/D2/PtPdAu	40	Interdigitated finger structure
Thick 11	Au/D1/Au	30	Interdigitated finger structure
Thick 12	Au/D2/Au	40	Interdigitated finger structure

A clamping fixture was used to compress high temperature compatible wire to the conductive pads on the substrate to apply biased voltage on the capacitor electrode at high temperature. Figure 3.3 shows the test fixture with the thick film substrate. The other end of the high temperature wires were soldered to a printed circuit board (PCB) located external to the test oven. Current limiting resistors (150k ohms) were used on the PCB between the positive voltage supply and the wire leading to one terminal of each test structure. The leakage current for each structure was calculated from the measured voltage across the resistor in that structure's electrical path.

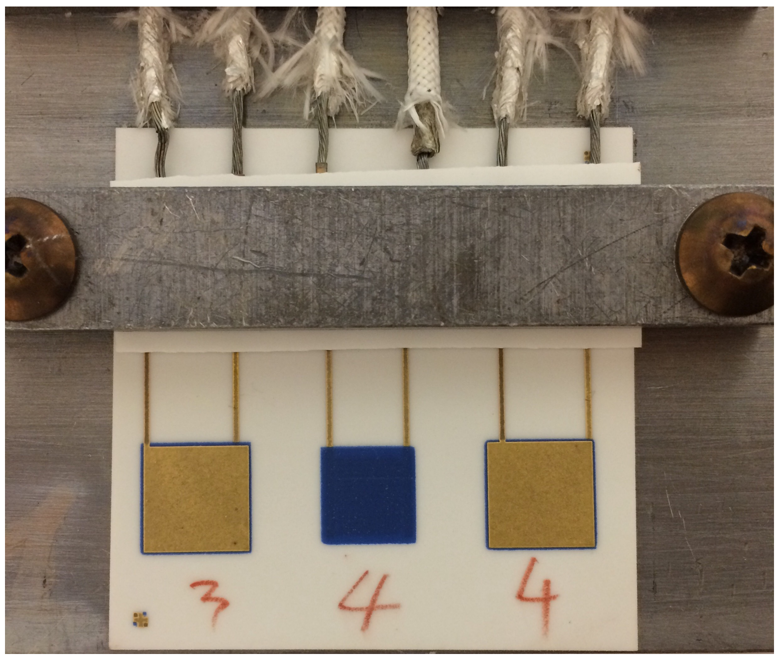

Figure 3.3: A leakage current test vehicle on fixture.

3.2 Leakage current results

3.2.1 Thin dielectrics

Figures 3.4-3.15 present the leakage current results with bias voltage (100V), at 300°C for thin dielectric groups (D1: 20 μm, D2: 30 μm). Figures 3.4-3.7 show the leakage current results with the top electrode biased positive with respect to the bottom electrode. As seen

in figures 3.4-3.5, all eight PtPdAu/D1/PtPdAu and eight PtPdAu/D2/PtPdAu capacitors had a significant increase in leakage current after a short aging time. Figures 3.6-3.7 plot the results for the eight Au/D1/Au and eight Au/D2/Au capacitors, which had nominally constant leakage current with time at 300°C.

Figures 3.8-3.11 show the leakage current results with the bottom electrode biased positive with respect to the top electrode. As seen in Figures 3.8-3.9, all eight PtPdAu/D1/PtPdAu and eight PtPdAu/D2/PtPdAu capacitors had a significant increase in leakage current after a short aging time. The maximum leakage current was lower for these vehicles than the ones with the top electrode biased positive. Figures 3.10-3.11 plot the result for the eight Au/D1/Au and eight Au/D2/Au capacitors, which had nominally constant leakage current with time at 300°C.

Figures 3.12-3.15 show the leakage current results of the interdigitated finger structures. All eight PtPdAu/D1/PtPdAu, eight PtPdAu/D2/PtPdAu, eight Au/D1/Au and eight Au/D2/Au interdigitated finger structures had nominally constant leakage current with time at 300°C.

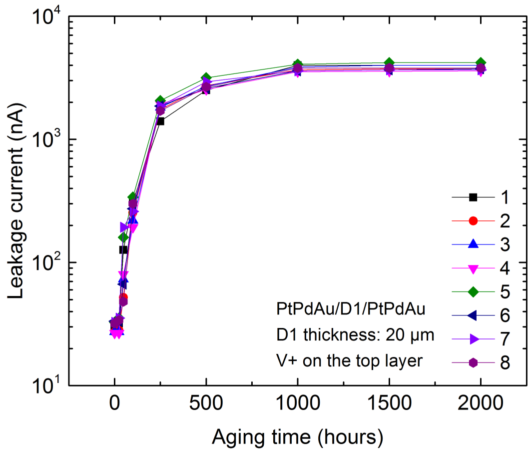

Figure 3.4: The leakage current of eight PtPdAu/D1/PtPdAu capacitors increased significantly with aging at 300°C.

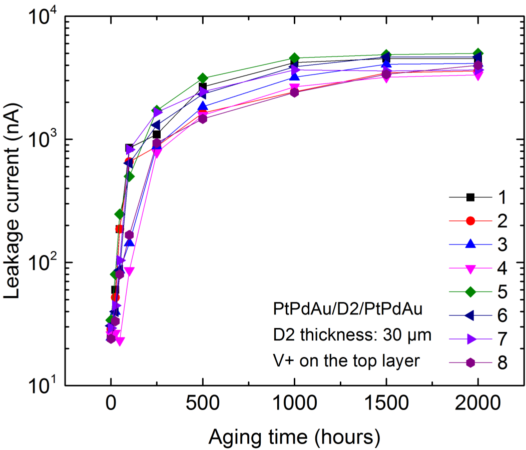

Figure 3.5: The leakage current of eight PtPdAu/D2/PtPdAu capacitors increased significantly with aging at 300°C.

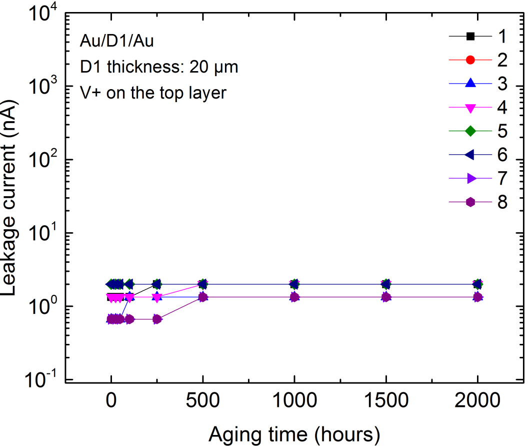

Figure 3.6: The leakage current of eight Au/D1/Au capacitors remained constant with aging at 300°C.

Figure 3.7: The leakage current of eight Au/D2/Au capacitors remained constant with aging at 300°C.

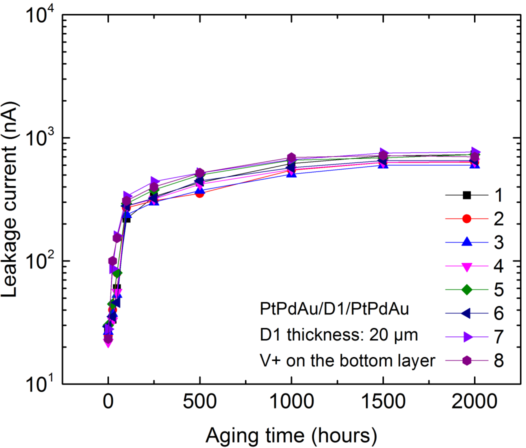

Figure 3.8: The leakage current of eight PtPdAu/D1/PtPdAu capacitors increased significantly with aging at 300°C.

Figure 3.9: The leakage current of eight PtPdAu/D2/PtPdAu capacitors increased significantly with aging at 300°C.

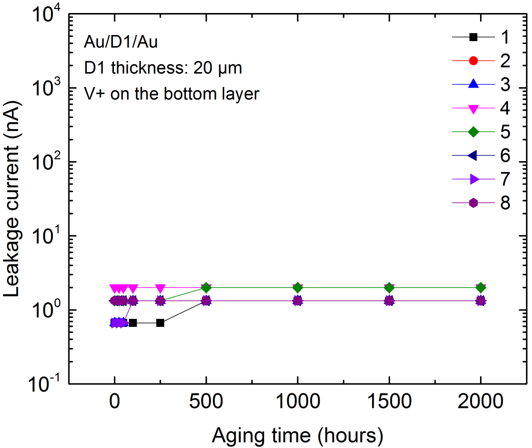

Figure 3.10: The leakage current of eight Au/D1/Au capacitors remained constant with aging at 300°C.

Figure 3.11: The leakage current of eight Au/D2/Au capacitors remained constant with aging at 300°C.

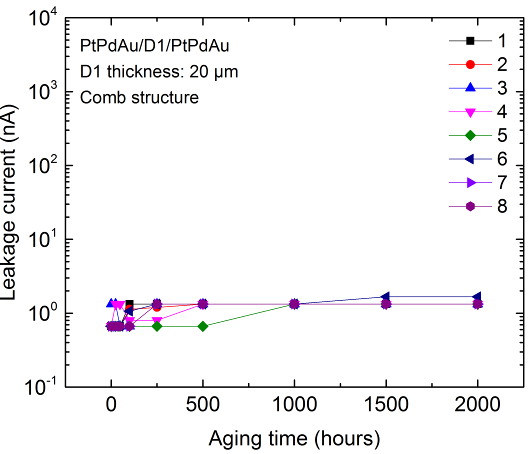

Figure 3.12: The leakage current of eight PtPdAu/D1/PtPdAu interdigitated finger structures remained constant with aging at 300°C.

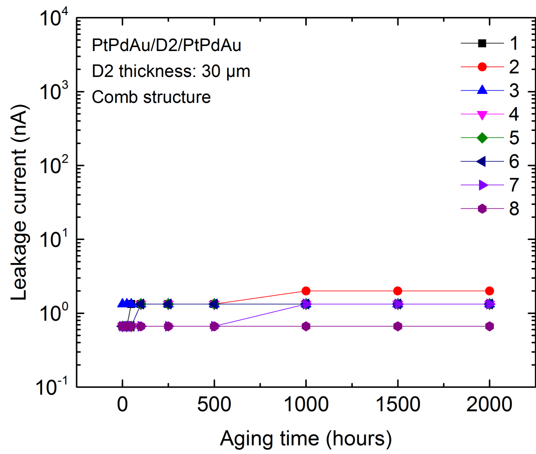

Figure 3.13: The leakage current of eight PtPdAu/D2/PtPdAu interdigitated finger structures remained constant with aging at 300°C.

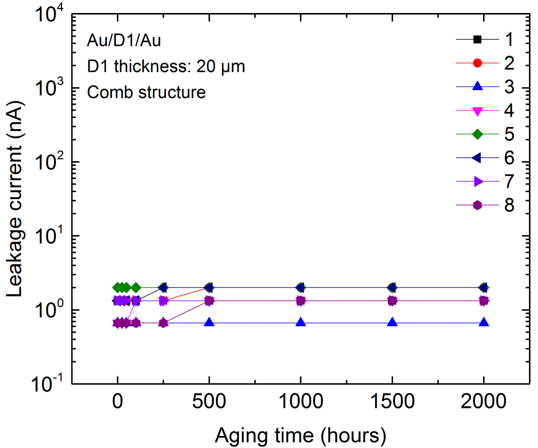

Figure 3.14: The leakage current of eight Au/D1/Au interdigitated finger structures remained constant with aging at 300°C.

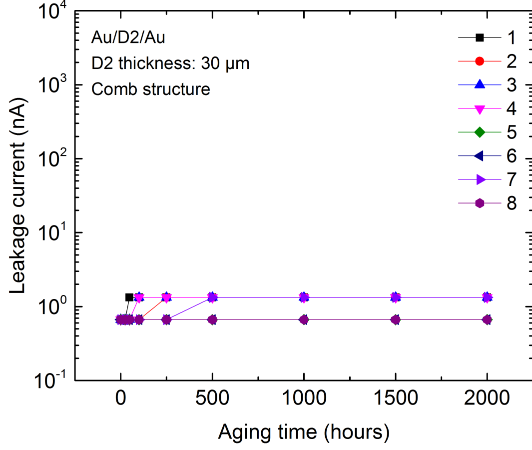

Figure 3.15: The leakage current of eight Au/D2/Au interdigitated finger structures remained constant with aging at 300°C.

3.2.2 Thick dielectrics

Figures 3.16-3.27 present the leakage current results with bias voltage (100V), at 300°C for thick dielectric groups, D1: 30 μm, and D2: 40 μm. All eight PtPdAu/D1/PtPdAu, eight PtPdAu/D2/PtPdAu, eight Au/D1/Au and eight Au/D2/Au capacitors had nominally constant leakage current with time at 300°C, regardless of polarity. All eight PtPdAu/D1/PtPdAu, eight PtPdAu/D2/PtPdAu, eight Au/D1/Au and eight Au/D2/Au interdigitated finger structures had nominally constant leakage current with time at 300°C.

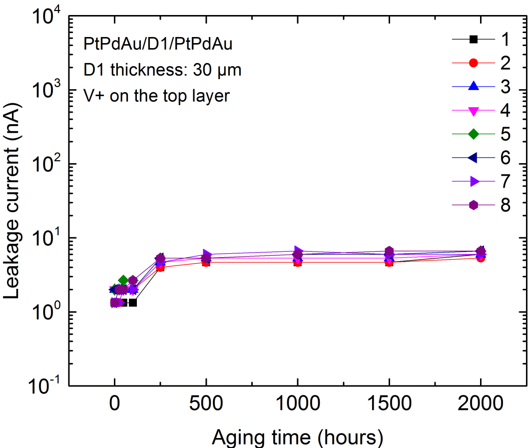

Figure 3.16: The leakage current of eight PtPdAu/D1/PtPdAu capacitors increased slightly with aging at 300°C.

Figure 3.17: The leakage current of eight PtPdAu/D2/PtPdAu capacitors increased slightly with aging at 300°C.

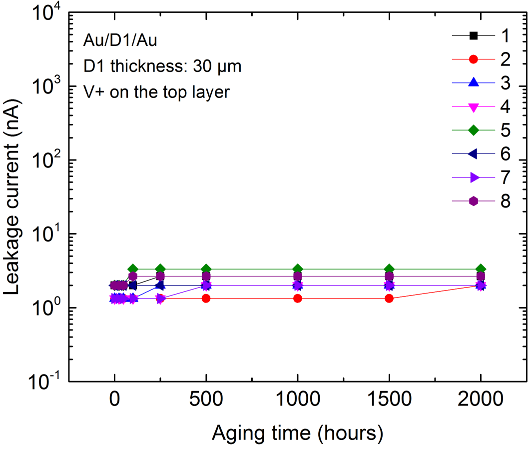

Figure 3.18: The leakage current of eight Au/D1/Au capacitors remained constant with aging at 300°C.

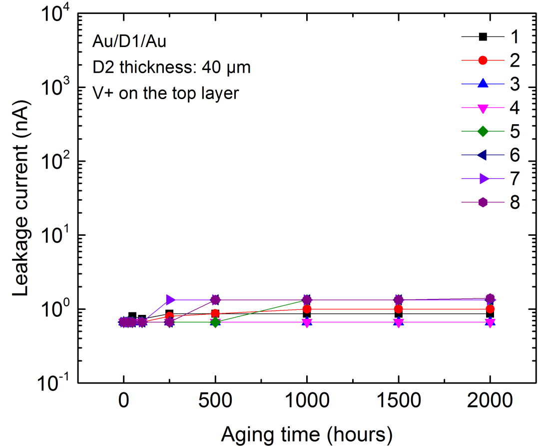

Figure 3.19: The leakage current of eight Au/D2/Au capacitors remained constant with aging at 300°C.

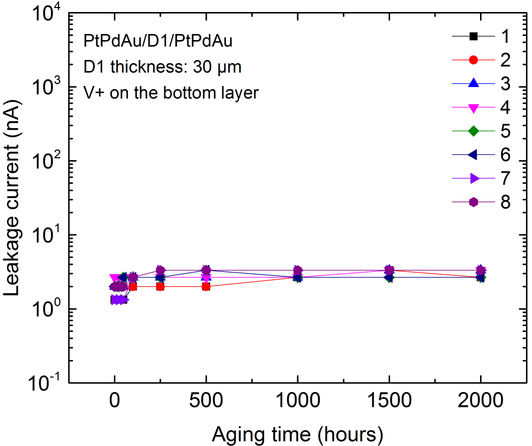

Figure 3.20: The leakage current of eight PtPdAu/D1/PtPdAu capacitors remained constant with aging at 300°C.

Figure 3.21: The leakage current of eight PtPdAu/D2/PtPdAu capacitors remained constant with aging at 300°C.

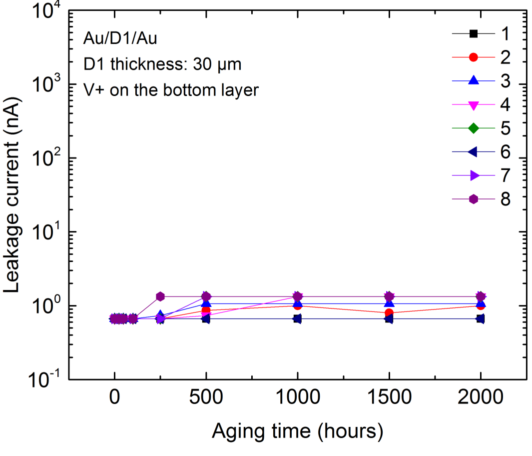

Figure 3.22: The leakage current of eight Au/D1/Au capacitors remained constant with aging at 300°C.

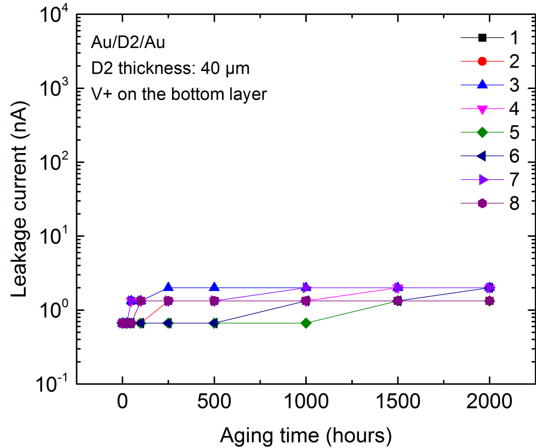

Figure 3.23: The leakage current of eight Au/D2/Au capacitors remained constant with aging at 300°C.

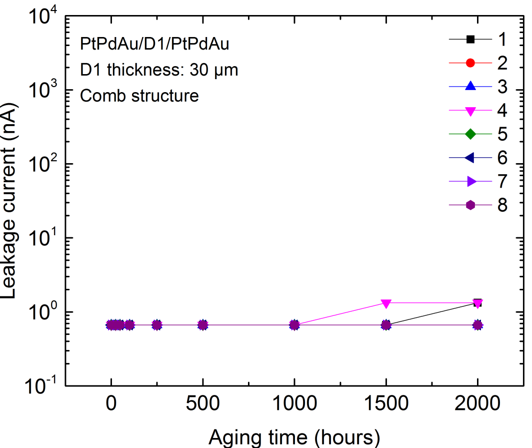

Figure 3.24: The leakage current of eight PtPdAu/D1/PtPdAu interdigitated finger structures remained constant with aging at 300°C.

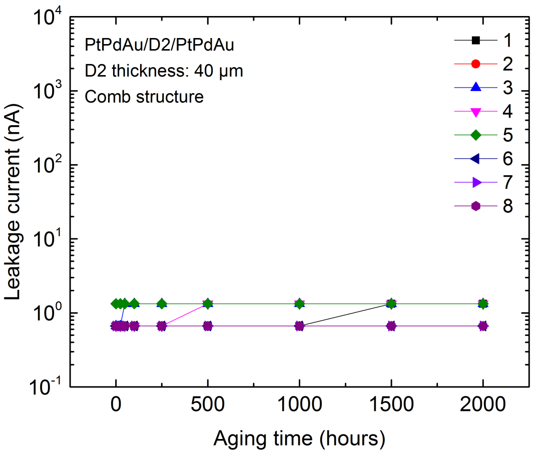

Figure 3.25: The leakage current of eight PtPdAu/D2/PtPdAu interdigitated finger structures remained constant with aging at 300°C.

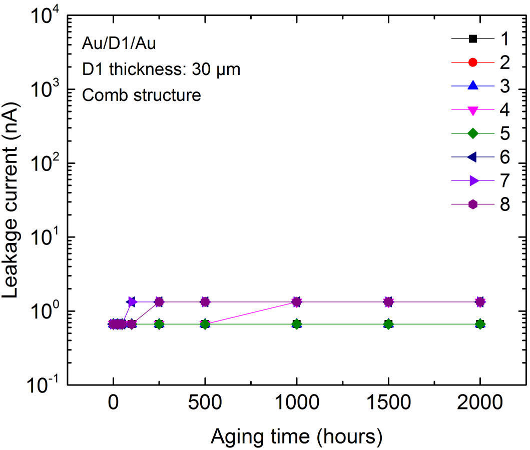

Figure 3.26: The leakage current of eight Au/D1/Au interdigitated finger structures remained constant with aging at 300°C.

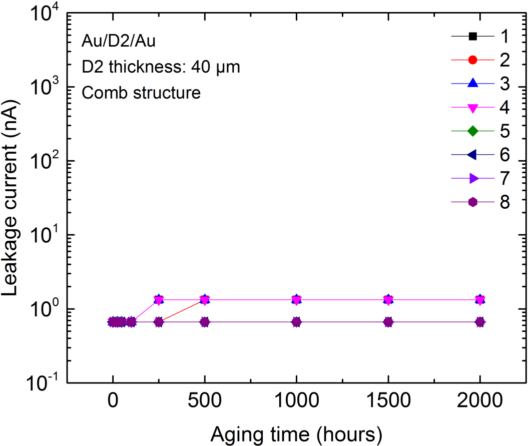

Figure 3.27: The leakage current of eight Au/D2/Au interdigitated finger structures remained constant with aging at 300°C.

3.3 Analysis

3.3.1 Material analysis

Thin dielectric

Cross sections of six leakage current test vehicles with thin dielectrics were analyzed by energy dispersive spectroscopy (EDS). Table 3.6 lists the information for each pattern with dielectric type, thicknesses (T_d), aging time and polarities. Figures 3.28 - 3.33 and tables 3.7 - 3.12 present the cross sections and EDS results of PtPdAu/D1/PtPdAu and PtPdAu/D2/PtPdAu capacitors with thin dielectrics at 0 and 2000 hours aging with each polarity. Bi was found in both thin D1 and thin D2, decreasing away from both top and bottom PtPdAu conductors, but still present in the center of the dielectric. The concentration of Bi in the dielectric layer remained relatively constant during aging. Figures 3.34 - 3.35 show the Bi distribution in the thin D1 (as built and after 2000 hours aging with both polarities) and thin D2 (as built and after 2000 hours aging with both polarities), respectively. Other elemental concentrations also remained relatively constant in both thin D1 and thin D2 during 2000 hours aging with both polarities (Figures 3.36 - 3.41), which means there is no elemental movement or diffusion.

Table 3.6: The leakage current test vehicles with thin dielectrics analyzed by EDS.

Pattern	Dielectric	T_d (μm)	Aging time (hours)	Polarity
D1-0	D1	20	0	None
D1-t	D1	20	2000	Positive bias on the top electrode
D1-b	D1	20	2000	Positive bias on the bottom electrode
D2-0	D2	30	0	None
D2-t	D2	30	2000	Positive bias on the top electrode
D2-b	D2	30	2000	Positive bias on the bottom electrode

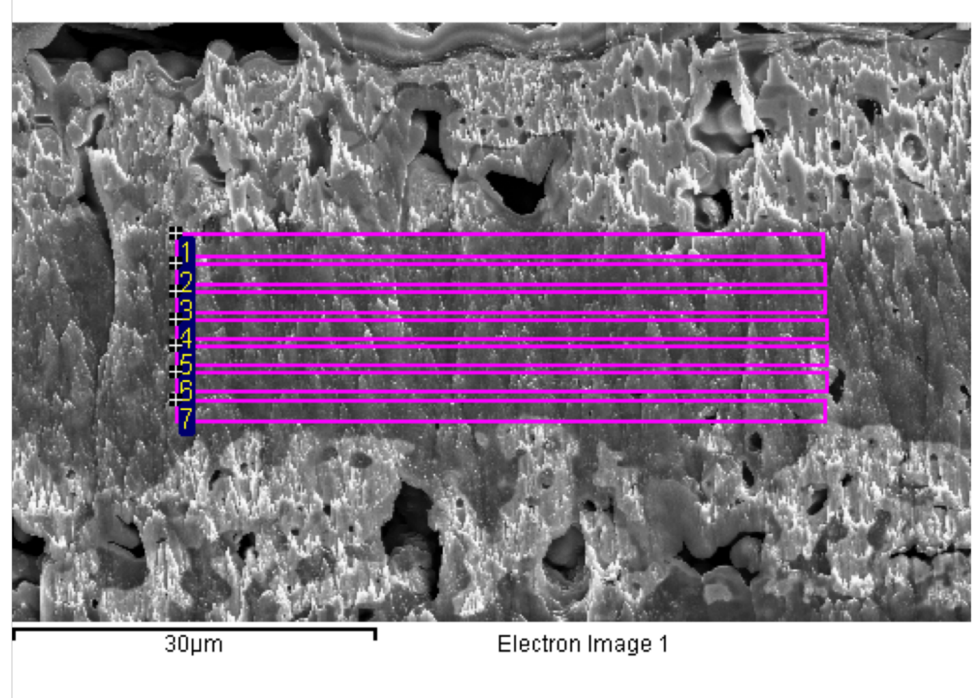

Figure 3.28: The cross section of pattern D1-0 (PtPdAu/D1/PtPdAu, D1 thickness: 20 μm, as build).

Table 3.7: Elemental distribution in wt% of D1-0 (PtPdAu/D1/PtPdAu, D1 thickness: 20 μm, as build), areas identified in figure 3.28.

Area	O	Al	Si	K	Ca	Zn	Ba	Bi
1	35.7	11.7	7.4	0.0	4.3	12.5	4.7	23.5
2	35.9	13.6	10.7	0.0	5.0	12.3	9.3	13.1
3	33.2	15.6	11.5	0.0	6.1	17.1	10.0	6.6
4	35.4	15.9	12.3	0.0	4.9	18.8	8.2	4.4
5	34.2	16.6	12.2	0.0	3.9	22.0	7.5	3.7
6	38.1	13.9	12.2	0.0	5.5	14.0	7.0	9.3
7	38.9	15.9	11.7	0.0	5.7	9.5	9.1	9.2

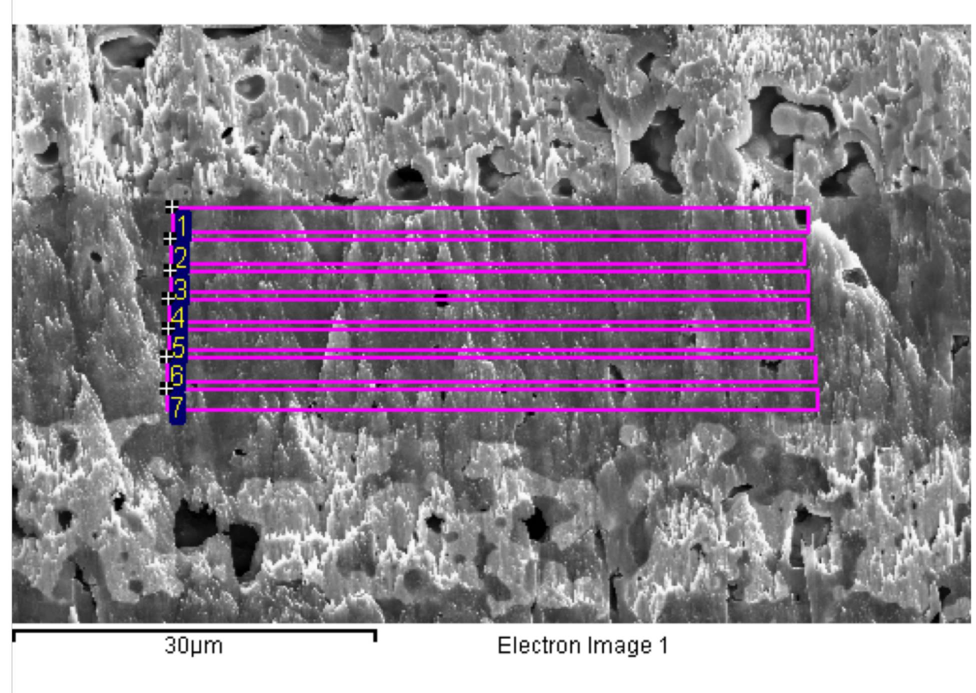

Figure 3.29: The cross section for pattern D1-t (PtPdAu/D1/PtPdAu, D1 thickness: 20 μm, after 2000 hours aging at 300°C with positive bias on the top electrode).

Table 3.8: Elemental distribution in wt% of D1-t (PtPdAu/D1/PtPdAu, D1 thickness: 20 μm, after 2000 hours aging at 300°C with positive bias on the top electrode), areas identified in figure 3.29.

Area	O	Al	Si	K	Ca	Zn	Ba	Bi
1	35.8	13.4	9.6	0.0	3.8	11.2	7.1	19.3
2	38.8	14.7	12.7	0.0	5.8	10.1	7.6	10.4
3	37.9	15.8	11.6	0.0	5.2	14.4	7.3	7.8
4	38.3	17.8	11.6	0.0	4.2	16.3	7.1	4.8
5	36.8	16.7	12.4	0.0	5.7	14.9	8.7	4.8
6	37.8	15.4	11.7	0.0	5.1	12.5	7.7	9.8
7	36.9	16.0	11.9	0.0	5.8	10.5	8.1	10.8

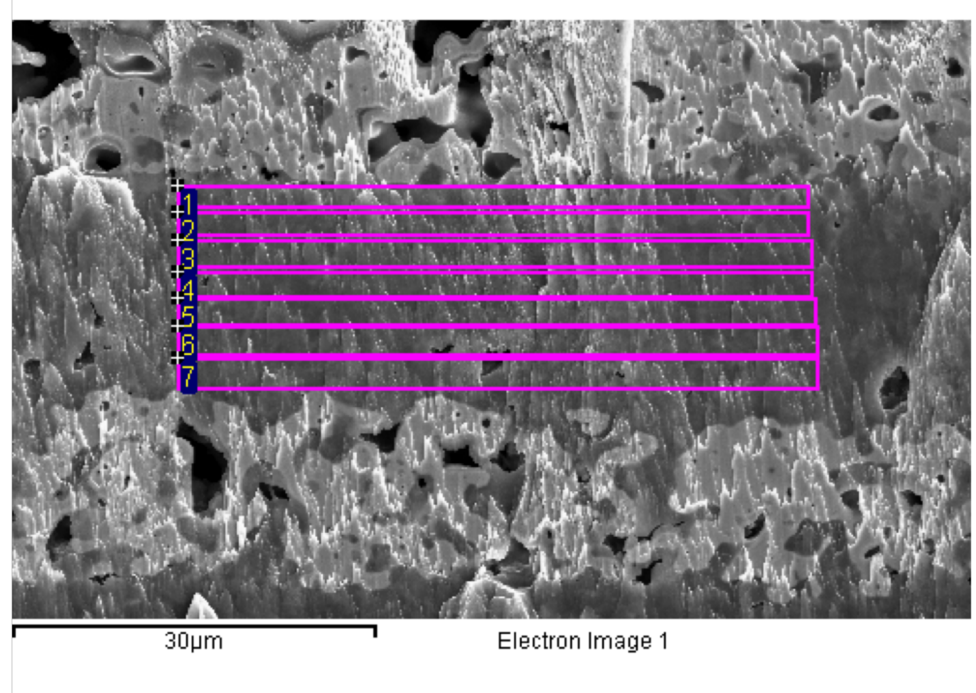

Figure 3.30: The cross section of pattern D1-b (PtPdAu/D1/PtPdAu, D1 thickness: 20 μm, after 2000 hours aging at 300°C with positive bias on the bottom electrode).

Table 3.9: Elemental distribution in wt% of D1-b (PtPdAu/D1/PtPdAu, D1 thickness: 20 μm, after 2000 hours aging at 300°C with positive bias on the bottom electrode), areas identified in figure 3.30.

Area	O	Al	Si	K	Ca	Zn	Ba	Bi
1	35.9	13.3	7.8	0.0	4.2	12.8	3.5	22.5
2	36.1	15.7	11.9	0.0	5.3	11.0	8.3	11.8
3	38.4	16.0	11.7	0.0	6.0	12.2	7.0	8.8
4	37.5	18.3	11.3	0.0	4.5	16.9	6.9	4.6
5	38.1	17.6	11.6	0.0	5.8	15.2	7.5	4.2
6	36.4	15.9	10.7	0.0	5.2	14.1	7.9	9.9
7	36.7	15.5	12.2	0.0	5.0	11.6	7.6	11.4

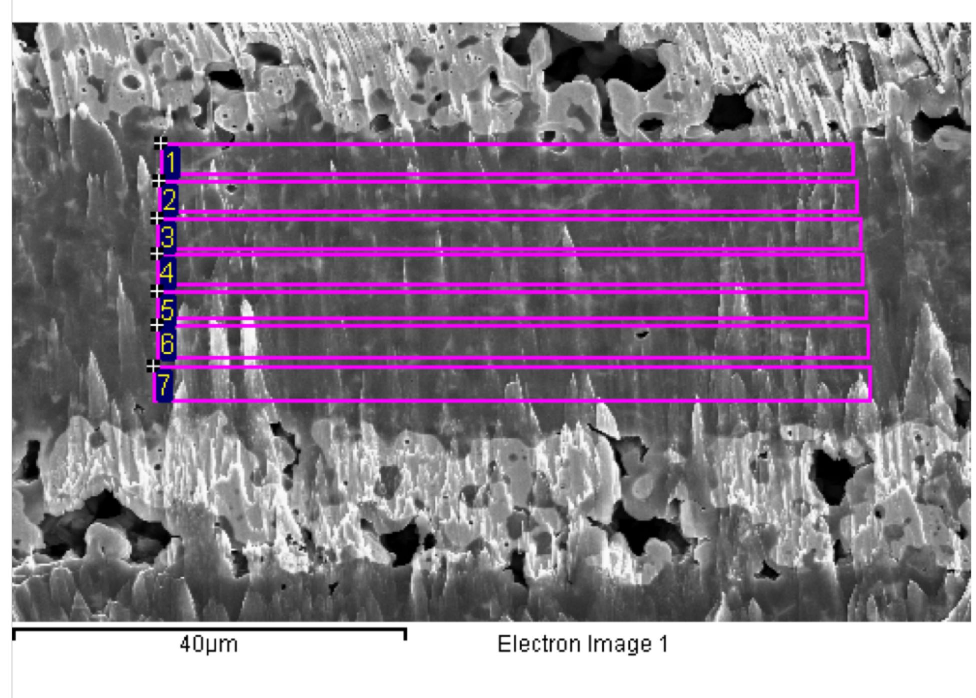

Figure 3.31: The cross section of pattern D2-0 (PtPdAu/D2/PtPdAu, D2 thickness: 30 μm, as build).

Table 3.10: Elemental distribution in wt% of D2-0 (PtPdAu/D2/PtPdAu, D2 thickness: 30 μm, as build), areas identified in figure 3.31.

Area	O	Al	Si	K	Ca	Zn	Ba	Bi
1	35.7	15.2	16.8	1.5	2.2	0.0	16.0	12.6
2	35.0	14.5	17.0	1.7	2.3	0.0	16.3	13.2
3	37.1	17.1	16.4	1.0	1.4	0.0	17.2	9.7
4	37.7	14.5	19.0	2.0	1.9	0.0	18.3	6.7
5	41.0	14.5	18.9	2.0	3.3	0.0	15.4	5.0
6	38.9	15.9	16.6	1.3	2.1	0.0	15.7	9.6
7	36.1	15.3	18.4	1.4	2.3	0.0	16.2	10.5

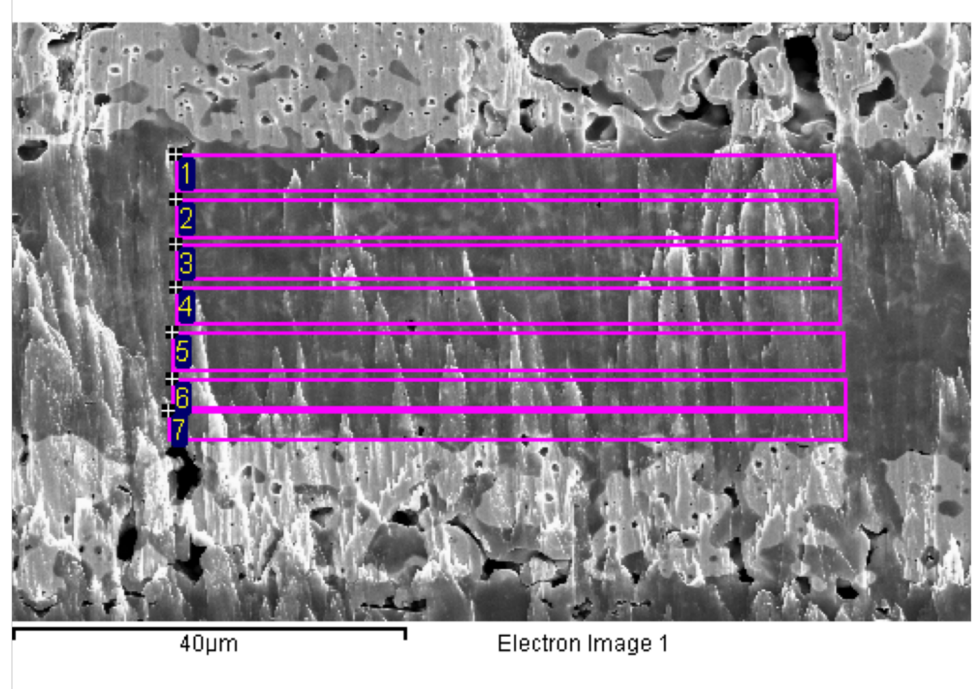

Figure 3.32: The cross section of pattern D2-t (PtPdAu/D2/PtPdAu, D2 thickness: 40 μm, after 2000 hours aging at 300°C with positive bias on the top electrode).

Table 3.11: Elemental distribution in wt% of D2-t (PtPdAu/D2/PtPdAu, D2 thickness: 40 μm, after 2000 hours aging at 300°C with positive bias on the top electrode), areas identified in figure 3.32.

Area	O	Al	Si	K	Ca	Zn	Ba	Bi
1	30.2	15.1	20.7	1.8	3.2	0.0	19.3	9.7
2	33.1	11.2	21.0	1.7	2.8	0.0	18.5	11.6
3	33.8	17.3	20.7	1.6	1.6	0.0	18.0	7.0
4	34.4	16.3	21.2	1.4	2.4	0.0	18.1	6.2
5	33.2	14.8	22.2	2.1	2.5	0.0	20.7	4.5
6	32.3	15.6	21.5	1.8	3.2	0.0	19.8	5.8
7	31.5	13.6	20.2	1.5	2.5	0.0	20.2	10.4

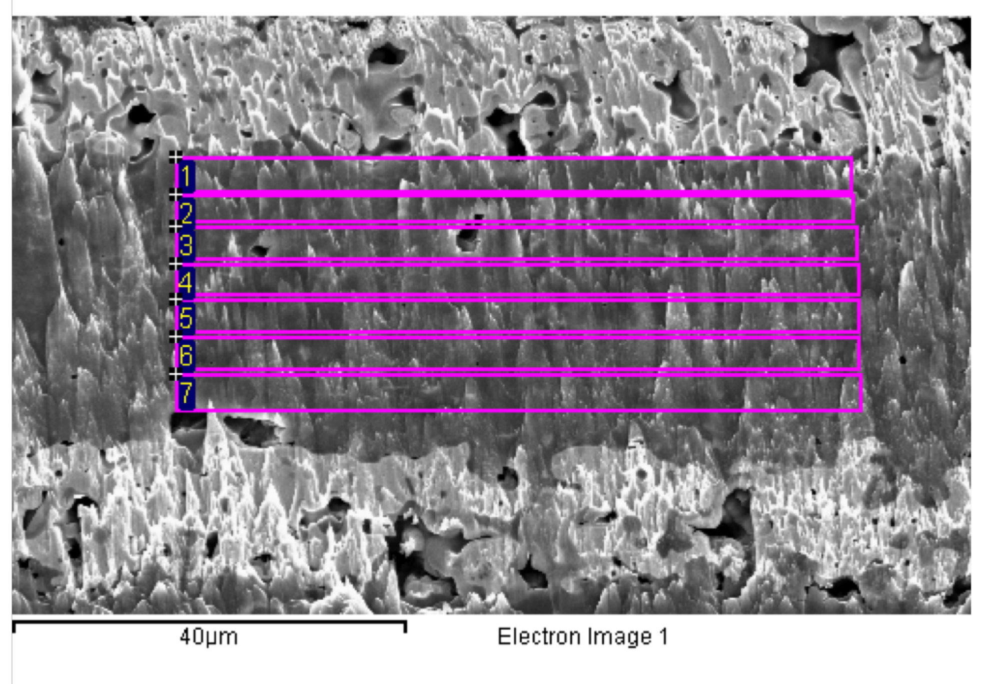

Figure 3.33: The cross section of pattern D2-b (PtPdAu/D2/PtPdAu, D2 thickness: 30 μm, after 2000 hours aging at 300°C with positive bias on the bottom electrode).

Table 3.12: Elemental distribution in wt% of D2-b (PtPdAu/D2/PtPdAu, D2 thickness: 30 μm, after 2000 hours aging at 300°C with positive bias on the bottom electrode), areas identified in figure 3.33.

Area	O	Al	Si	K	Ca	Zn	Ba	Bi
1	36.3	14.3	16.9	1.5	2.1	0.0	19.6	9.3
2	37.3	17.7	14.7	1.4	1.6	0.0	15.9	11.4
3	38.9	14.2	15.3	1.7	1.9	0.0	16.4	11.6
4	37.9	20.4	15.3	0.9	2.0	0.0	16.3	7.3
5	40.5	19.0	16.5	1.0	2.2	0.0	16.3	4.5
6	39.1	17.8	15.5	1.7	2.1	0.0	17.7	6.0
7	36.2	15.3	16.5	1.8	1.8	0.0	19.2	9.2

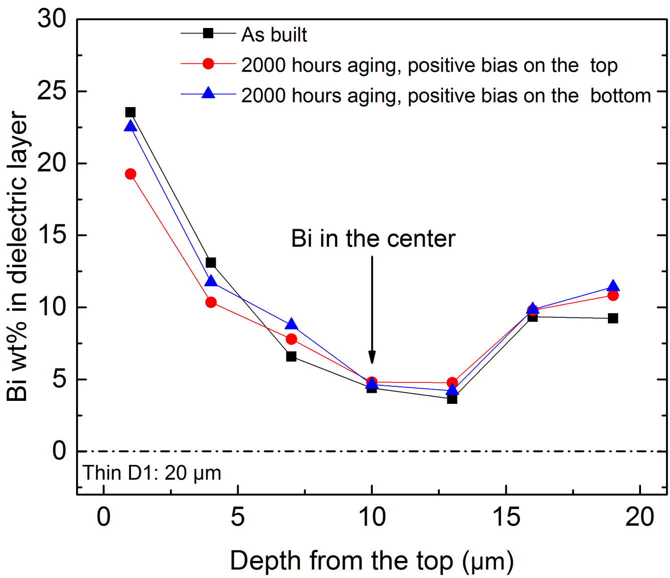

Figure 3.34: Bi distribution (wt%) in thin D1 (PtPdAu/D1/PtPdAu, D1 thickness: 20 μm).

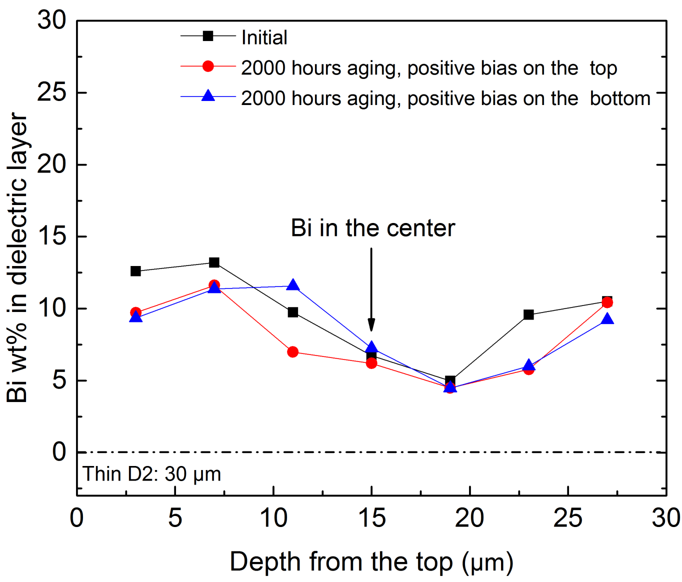

Figure 3.35: Bi distribution (wt%) in thin D2 (PtPdAu/D2/PtPdAu, D3 thickness: 10 μm).

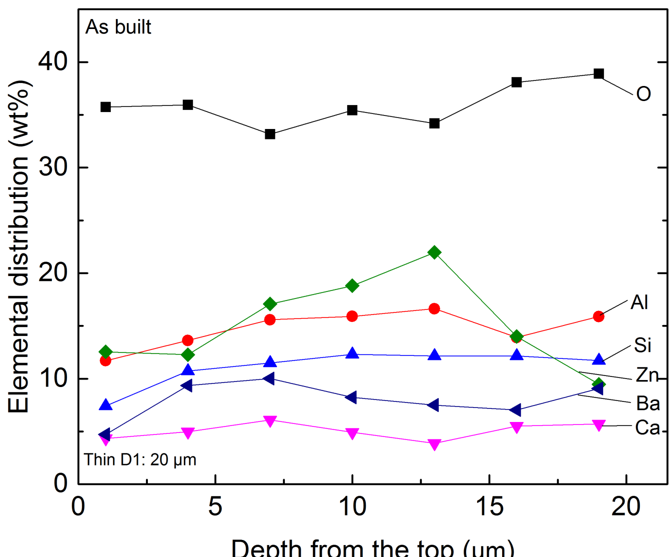

Figure 3.36: Elemental distribution (wt%) in thin D1 (PtPdAu/D1/PtPdAu, D1 thickness: 20 μm), as built.

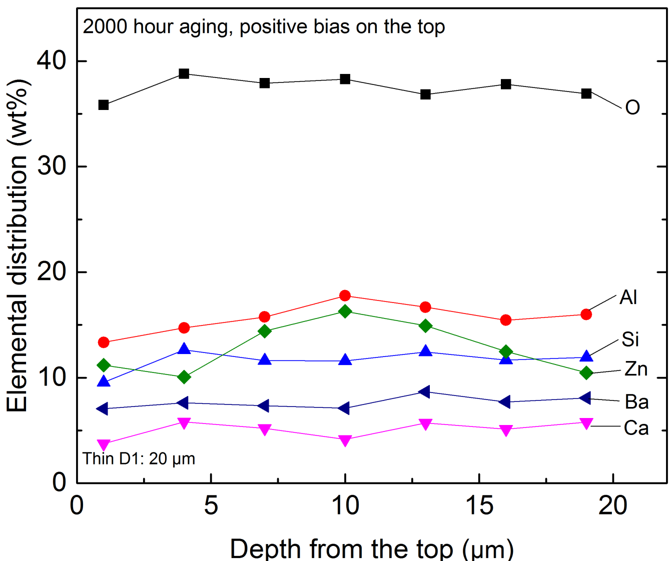

Figure 3.37: Elemental distribution (wt%) in thin D1 (PtPdAu/D1/PtPdAu, D1 thickness: 20 μm, after 2000 hours aging with positive bias on the top electrode).

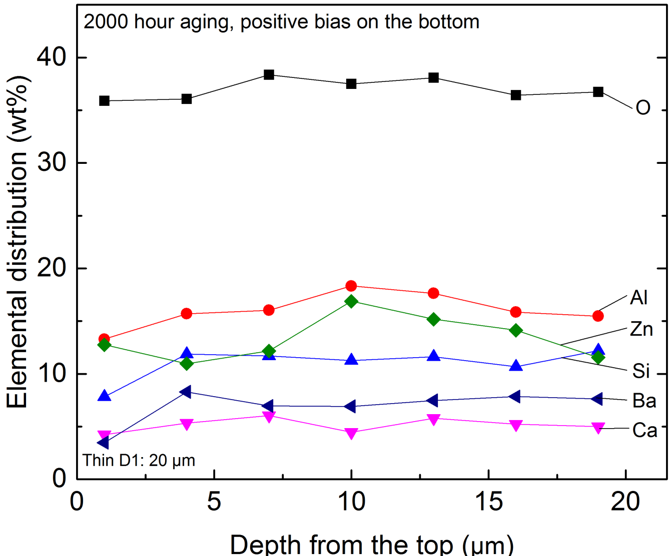

Figure 3.38: Elemental distribution (wt%) in thin D1 (PtPdAu/D1/PtPdAu, D1 thickness: 20 μm, after 2000 hours aging with positive bias on the bottom electrode).

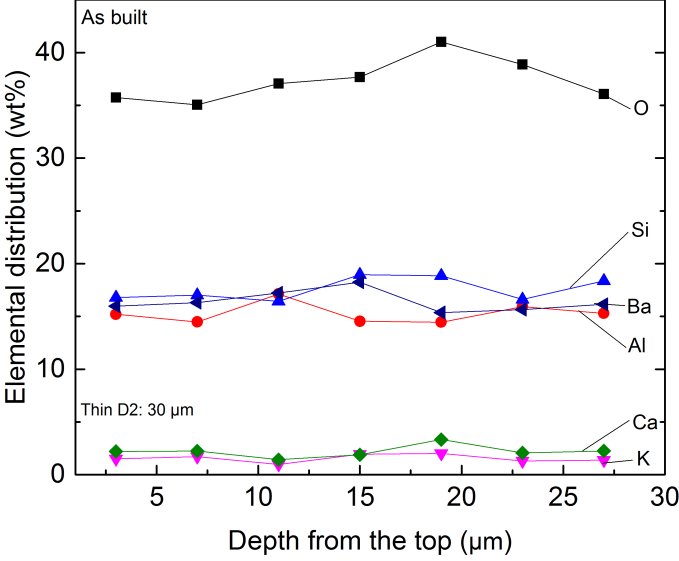

Figure 3.39: Elemental distribution (wt%) in thin D2 (PtPdAu/D2/PtPdAu, D2 thickness: 30 μm, as build).

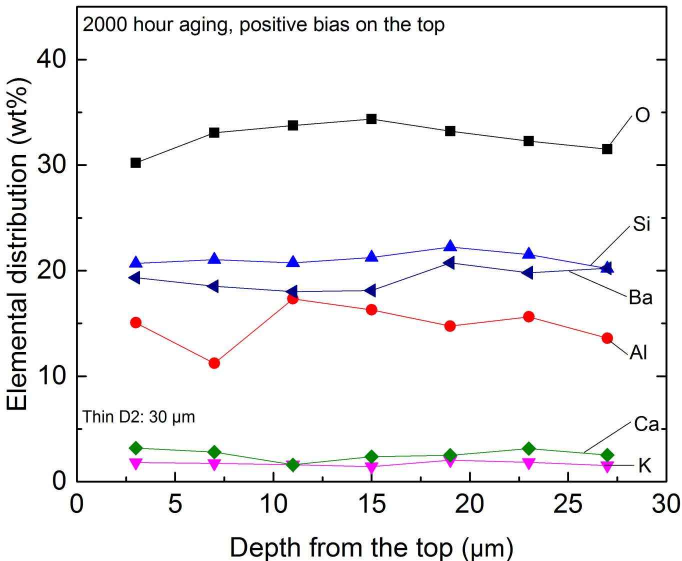

Figure 3.40: Elemental distribution (wt%) in thin D2 (PtPdAu/D2/PtPdAu, D2 thickness: 30 μm, after 2000 hours aging with positive bias on the top electrode).

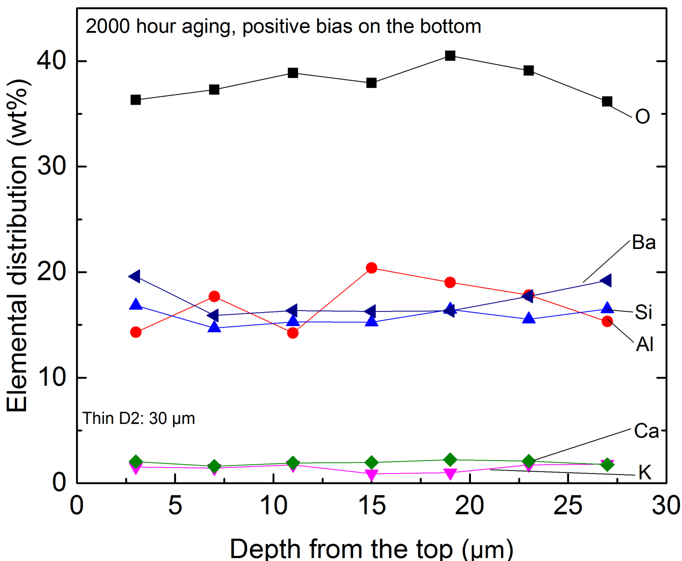

Figure 3.41: Elemental distribution (wt%) in thin D2 (PtPdAu/D2/PtPdAu, D2 thickness: 30 μm, after 2000 hours aging with positive bias on the bottom electrode).

Thick dielectric

Cross sections of six leakage current test vehicles with thick dielectrics were analyzed by EDS. Table 3.13 lists the materials, dielectric thicknesses, aging time and polarities of six leakage current test vehicles with thick dielectrics. Cross sections and elemental analysis results were shown in figures 3.42 - 3.47 and tables 3.14 - 3.19. Bi was found in both thick D1 and thick D2, decreasing away from both top and bottom PtPdAu conductors, but Bi did not reach to the center of the dielectric. Figures 3.48 - 3.49 shows Bi distribution in thick D1 (as built and after 2000 hours aging with both polarities) and thick D2 (as built and after 2000 hours aging with both polarities), respectively. Other elemental concentrations also remained relatively constant during 2000 hours aging with both polarities, which means there was no elemental movement.

Table 3.13: The leakage current test vehicles with thick dielectrics analyzed by EDS.

Pattern	Dielectric	T_d (μm)	Aging time (hours)	Polarity
D1t-0	D1	30	0	None
D1t-t	D1	30	2000	Positive bias on the top electrode
D1t-b	D1	30	2000	Positive bias on the bottom electrode
D2t-0	D2	40	0	None
D2t-t	D2	40	2000	Positive bias on the top electrode
D2t-b	D2	40	2000	Positive bias on the bottom electrode

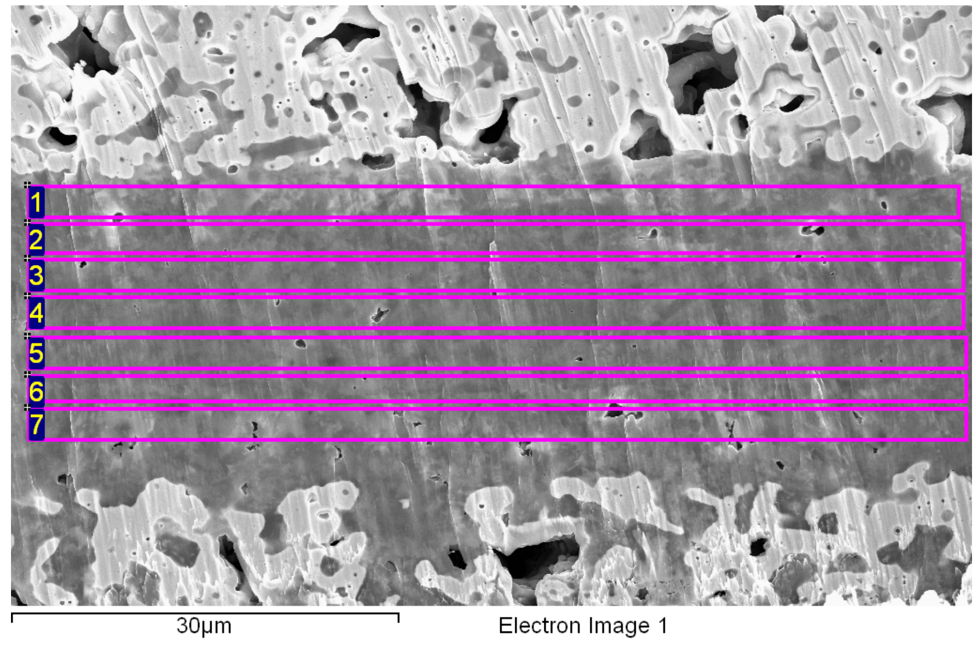

Figure 3.42: The cross section of pattern D1t-0 (PtPdAu/D1/PtPdAu, D1 thickness: 30 μm, as build).

Table 3.14: Elemental distribution in wt% of D1t-0 (PtPdAu/D1/PtPdAu, D1 thickness: 30 μm, as build), areas identified in figure 3.42.

Area	O	Al	Si	K	Ca	Zn	Ba	Bi
1	46.3	13.9	10.0	0.0	5.3	7.9	7.6	9.1
2	46.8	15.1	10.8	0.0	5.8	10.1	6.5	4.9
3	49.3	15.1	10.8	0.0	6.4	9.8	6.9	1.7
4	48.6	15.0	10.9	0.0	5.4	13.8	6.3	0.0
5	48.5	15.2	10.9	0.0	6.1	13.4	5.9	0.0
6	47.7	14.9	9.7	0.0	6.0	12.3	6.9	2.5
7	47.2	14.8	9.9	0.0	4.6	8.9	6.5	8.0

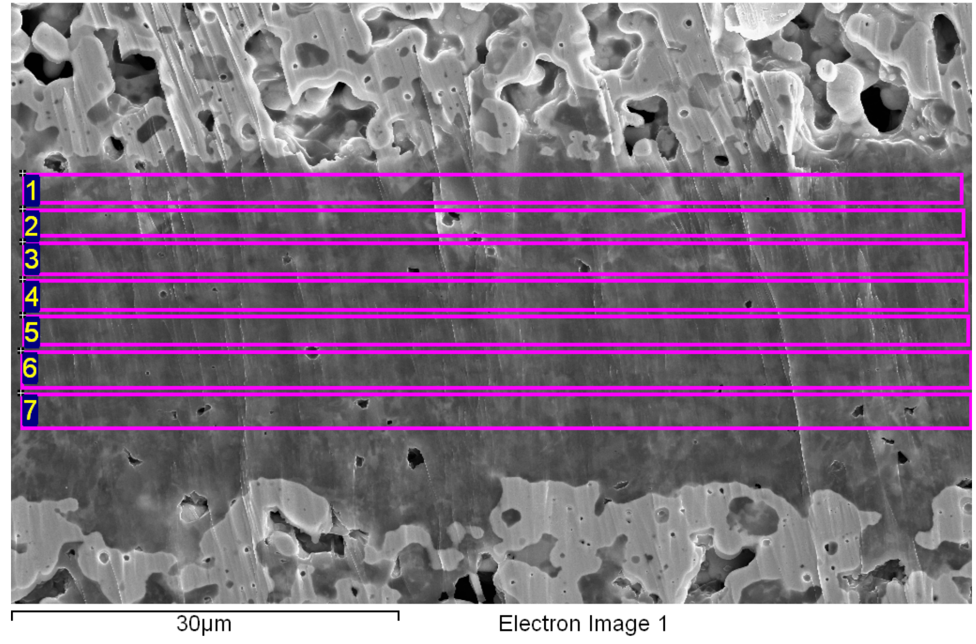

Figure 3.43: The cross section for pattern D1t-t (PtPdAu/D1/PtPdAu, D1 thickness: 30 μm, after 2000 hours aging at 300°C with positive bias on the top electrode).

Table 3.15: Elemental distribution in wt% of D1t-t (PtPdAu/D1/PtPdAu, D1 thickness: 30 μm, after 2000 hours aging at 300°C with positive bias on the top electrode), areas identified in figure 3.43.

Area	O	Al	Si	K	Ca	Zn	Ba	Bi
1	45.1	13.2	10.6	0.0	5.6	11.9	7.0	6.7
2	47.8	15.2	11.2	0.0	5.4	9.3	7.2	4.0
3	48.4	16.5	10.6	0.0	5.8	10.9	6.6	1.2
4	47.5	17.2	11.5	0.0	6.2	10.9	6.8	0.0
5	46.9	17.0	10.9	0.0	5.4	13.0	5.8	1.1
6	48.2	14.7	9.9	0.0	4.9	11.7	5.6	4.9
7	46.7	14.7	11.4	0.0	4.8	9.3	6.1	7.0

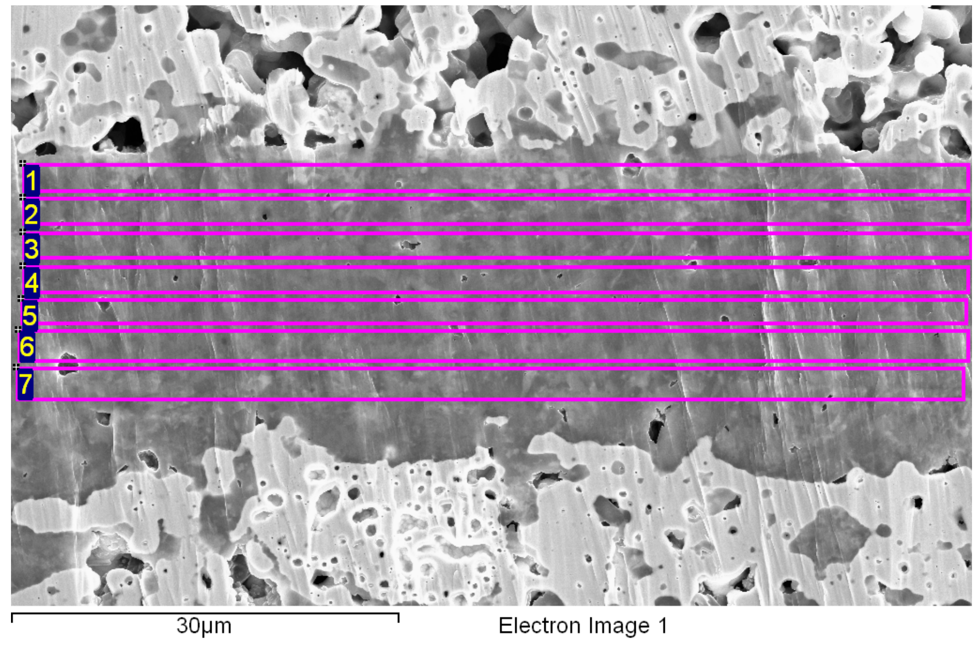

Figure 3.44: The cross section of pattern D1t-b (PtPdAu/D1/PtPdAu, D1 thickness: 30 μm, after 2000 hours aging at 300°C with positive bias on the bottom electrode).

Table 3.16: Elemental distribution in wt% of D1t-b (PtPdAu/D1/PtPdAu, D1 thickness: 30 μm, after 2000 hours aging at 300°C with positive bias on the bottom electrode), areas identified in figure 3.44.

Area	O	Al	Si	K	Ca	Zn	Ba	Bi
1	44.9	13.5	10.8	0.0	5.4	8.8	7.0	9.7
2	46.4	13.9	10.5	0.0	6.0	11.1	7.0	5.1
3	47.8	15.6	10.7	0.0	5.7	10.8	6.6	2.7
4	46.9	17.3	10.9	0.0	5.8	11.4	7.6	0.0
5	46.8	15.6	9.9	0.0	5.1	14.3	6.4	1.9
6	45.8	16.9	11.1	0.0	5.2	11.7	6.3	3.2
7	46.8	15.2	10.6	0.0	4.5	9.8	6.5	6.5

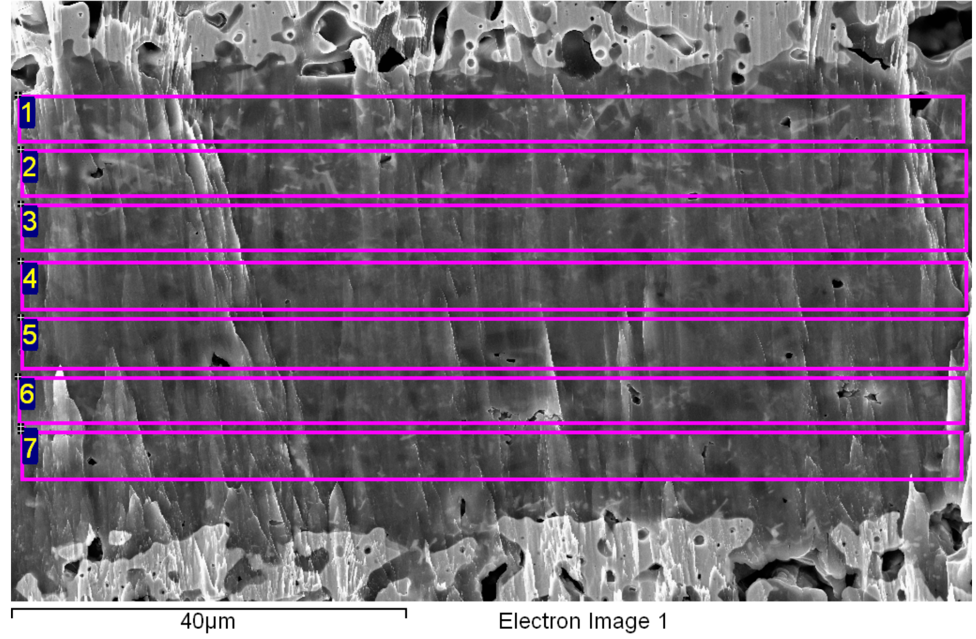

Figure 3.45: The cross section of pattern D2t-0 (PtPdAu/D2/PtPdAu, D2 thickness: 40 μm, as build).

Table 3.17: Elemental distribution in wt% of D2t-0 (PtPdAu/D2/PtPdAu, D2 thickness: 40 μm, as build), areas identified in figure 3.45.

Area	O	Al	Si	K	Ca	Zn	Ba	Bi
1	47.2	10.7	13.3	1.0	0.0	2.0	13.4	12.4
2	48.6	13.3	13.4	1.4	0.0	1.6	13.9	7.8
3	49.8	14.4	15.6	1.2	0.0	1.9	15.4	1.8
4	50.0	14.7	15.5	1.3	0.0	2.2	16.3	0.0
5	50.2	15.8	15.2	1.3	0.0	2.1	15.3	0.0
6	50.3	16.5	14.4	1.3	0.0	2.3	12.6	2.6
7	49.0	14.6	13.2	1.0	0.0	2.1	12.2	7.9

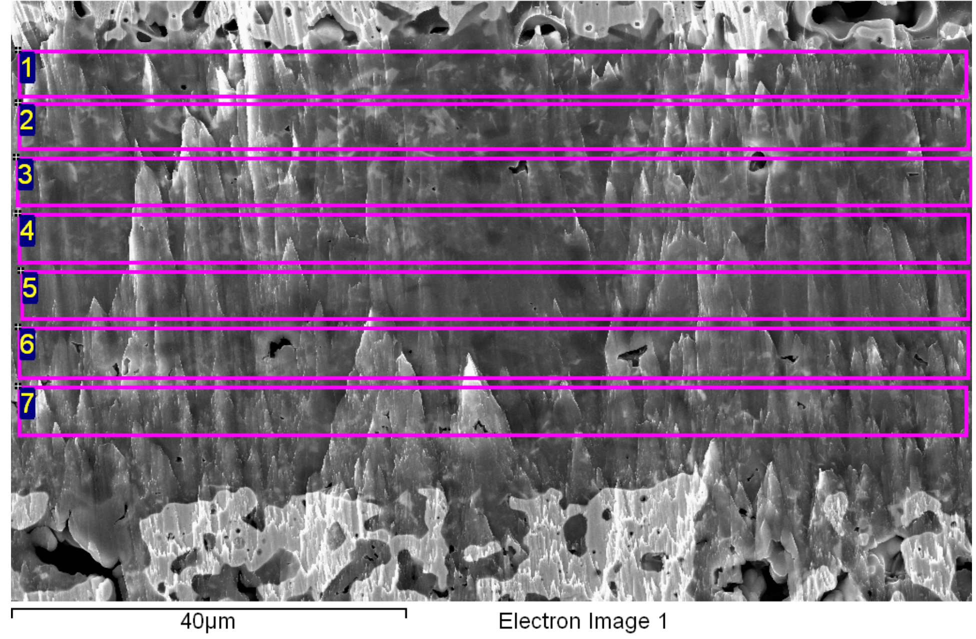

Figure 3.46: The cross section of pattern D2t-t (PtPdAu/D2/PtPdAu, D2 thickness: 40 μm, after 2000 hours aging at 300°C with positive bias on the top electrode).

Table 3.18: Elemental distribution in wt% of D2t-t (PtPdAu/D2/PtPdAu, D2 thickness: 40 μm, after 2000 hours aging at 300°C with positive bias on the top electrode), areas identified in figure 3.46.

Area	O	Al	Si	K	Ca	Zn	Ba	Bi
1	47.2	13.0	12.9	1.2	0.0	1.5	14.8	9.4
2	48.9	12.0	16.0	1.3	0.0	2.3	15.3	4.3
3	49.6	14.4	15.7	1.4	0.0	2.0	15.0	1.9
4	49.0	16.5	15.4	1.5	0.0	2.0	15.7	0.0
5	50.2	16.8	15.4	1.5	0.0	1.8	14.4	0.0
6	46.7	12.3	15.9	1.7	0.0	1.5	18.7	3.3
7	49.5	14.5	13.6	1.2	0.0	2.0	13.2	6.0

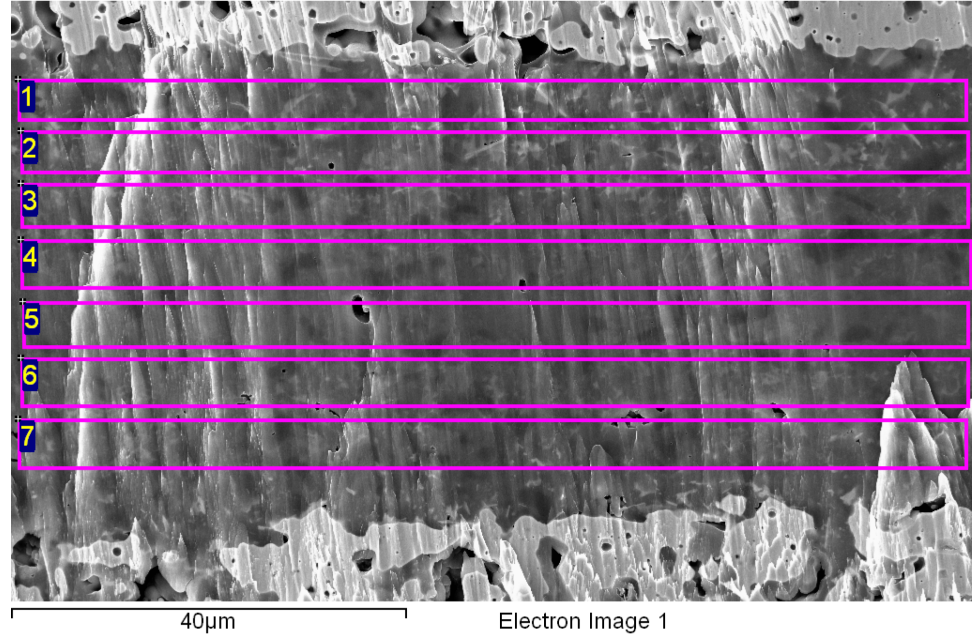

Figure 3.47: The cross section of pattern D2t-b (PtPdAu/D2/PtPdAu, D2 thickness: 40 μm, after 2000 hours aging at 300°C with positive bias on the bottom electrode).

Table 3.19: Elemental distribution in wt% of D2t-b (PtPdAu/D2/PtPdAu, D2 thickness: 40 μm, after 2000 hours aging at 300°C with positive bias on the bottom electrode), areas identified in figure 3.47.

Area	O	Al	Si	K	Ca	Zn	Ba	Bi
1	44.0	13.2	14.5	1.5	0.0	2.4	15.1	9.3
2	44.8	13.5	14.1	1.6	0.0	2.3	18.2	5.4
3	45.2	14.5	16.1	1.5	0.0	2.4	17.9	2.3
4	45.8	14.0	16.6	1.6	0.0	2.3	19.7	0.0
5	44.3	14.8	17.4	1.8	0.0	2.4	19.4	0.0
6	43.6	12.8	17.1	1.7	0.0	2.4	20.1	2.4
7	47.0	15.0	15.0	1.3	0.0	2.8	15.4	3.5

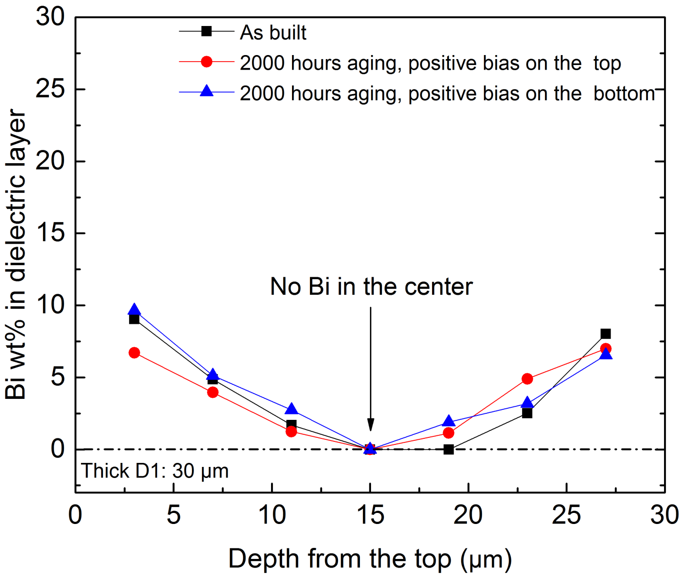

Figure 3.48: Bi distribution (wt%) in thick D1 (PtPdAu/D1/PtPdAu, D1 thickness: 30 μm).

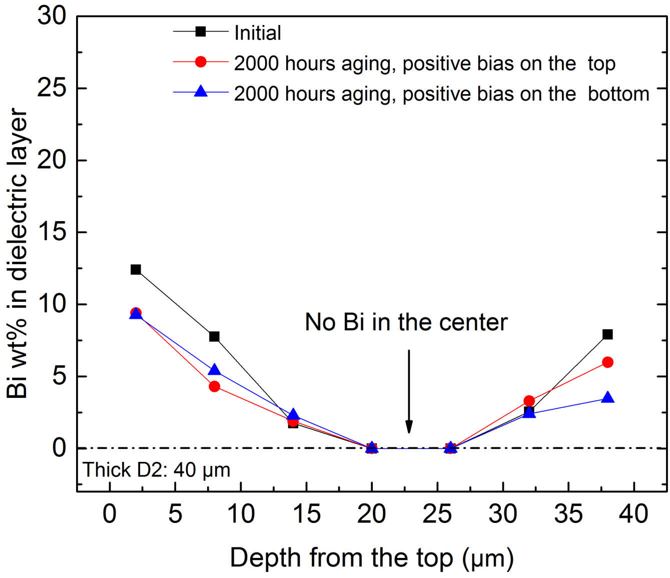

Figure 3.49: Bi distribution (wt%) in thick D2 (PtPdAu/D2/PtPdAu, D2 thickness: 40 μm).

Source of Bi

According to the material supplier, the dielectric does not contain Bi, but the PtPdAu conductor does. To confirm the dielectric paste did not contain Bi, two layers of D1 were sequentially printed, dried and fired on an alumina substrate. The elemental analysis of D1 is shown in table 3.20. A single layer of the PtPdAu conductor was printed, dried and fired on an alumina substrate without conductor. The elemental analysis of PtPdAu conductor is shown in figure 3.50 and table 3.21.The analysis confirms no Bi in D1, and the PtPdAu conductor does contain Bi.

Table 3.20: Elemental distribution in wt% of undoped dielectric D1.

Area	O	Al	Si	K	Ca	Zn	Ba	Bi
1	44.7	16.5	11.4	0.0	6.0	13.9	7.6	0.0
2	46.7	16.7	11.7	0.0	6.8	12.3	5.8	0.0
3	42.7	17.1	12.3	0.0	6.1	13.3	8.5	0.0
4	43.1	16.6	12.1	0.0	6.2	13.8	8.2	0.0

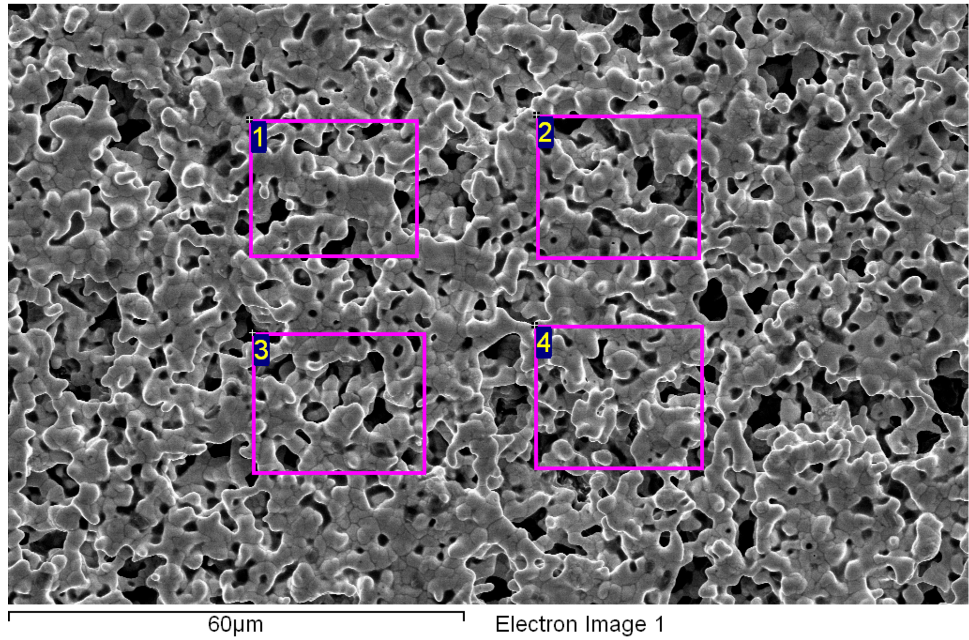

Figure 3.50: The surface of bare PtPdAu conductor.

Table 3.21: Elemental distribution in wt% of bare PtPdAu conductor, areas identified in figure 3.50.

Area	O	Al	Si	Ba	Pt	Pd	Au	Bi
1	6.7	0.0	0.0	0.0	8.5	6.5	72.3	6.0
2	8.3	0.0	0.0	0.0	10.4	5.7	69.1	6.5
3	6.2	0.0	0.0	0.0	9.3	7.7	70.5	6.3
4	6.9	0.0	0.0	0.0	8.6	7.0	71.9	5.7

As the only source of Bi was the PtPdAu, two samples were fabricated to evaluate the diffusion of Bi into the dielectric. Sample 1 was two layers of dielectric D1 sequentially printed, dried and fired on a previously fired layer of PtPdAu. Sample 2 was a single layer of PtPdAu printed, dried and fired on two previously fired layers of D1. The cross section and elemental analysis results are shown in figures 3.51 - 3.52 and tables 3.22 - 3.23. In both samples, Bi was found in the dielectric, decreasing away from the PtPdAu. The analysis proves that Bi diffuses into the dielectric from the PtPdAu conductor during both dielectric firing and on top of PtPdAu, and PtPdAu firing on top of dielectrics.

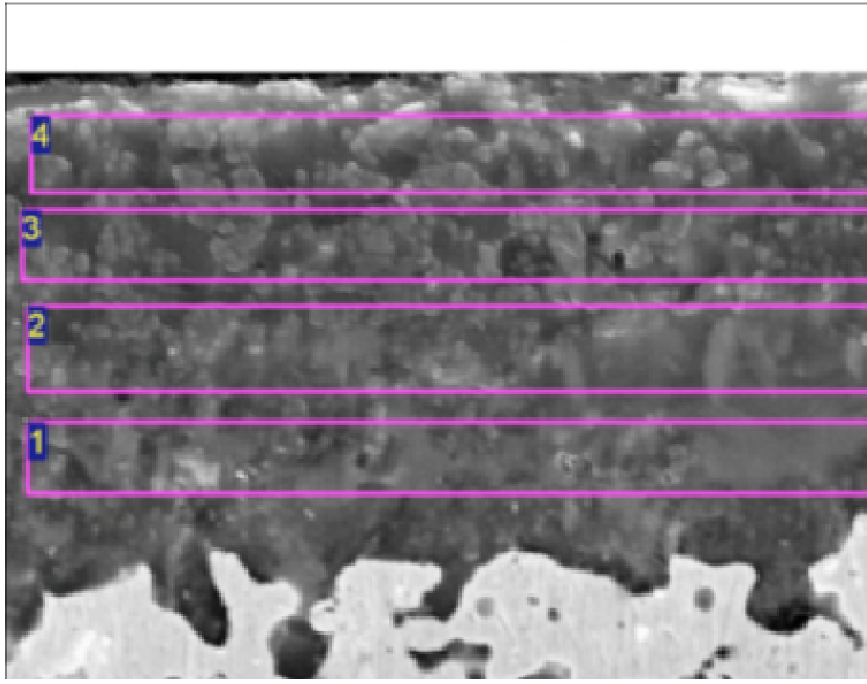

Figure 3.51: The cross section of two layers of D1 on PtPdAu, as build.

Table 3.22: Elemental distribution in wt% of two layers of D1 on PtPdAu, as build, areas identified in figure 3.51.

Area	Al	Si	Ca	Zn	Ba	Bi
1	23.16	23.93	8.91	26.91	4.41	12.68
2	26.46	25.23	14.14	24.51	5.45	4.21
3	31.64	26.01	12.76	25.32	4.27	0
4	33.42	27.15	11.58	23.46	4.4	0

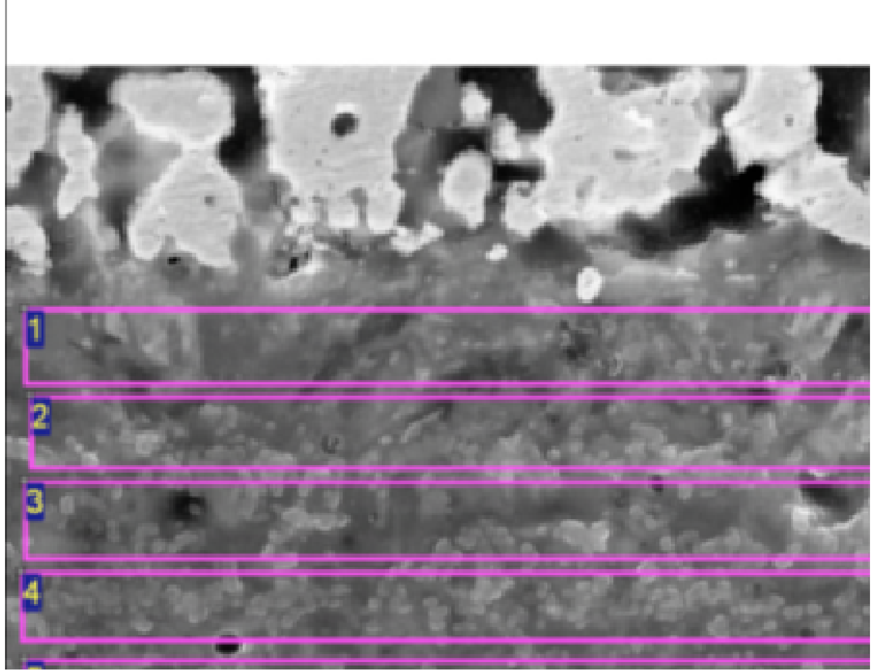

Figure 3.52: The cross section of PtPdAu on two layers of D1, as build).

Table 3.23: Elemental distribution in wt% of PtPdAu on two layers of D1, as build, areas identified in figure 3.52.

Area	Al	Si	Ca	Zn	Ba	Bi
1	23.28	22.39	11.02	21.24	4	18.07
2	28.84	24.32	12.57	17.78	4.18	12.32
3	29.44	26.8	13.53	23.85	3.69	2.69
4	36.46	24.59	11.09	23.79	4.07	0
5	31.96	27.49	11.64	24.85	4.06	0

3.3.2 PtPdAu-low Bi

To confirm that Bi diffused into the dielectric, the manufacturer reduced the Bi concentration in the PtPdAu paste to the lowest practical level and this conductor (PtPdAu-low Bi) was used to fabricate test vehicles for leakage current and adhesion measurement. The test groups Low 1-Low 6 were capacitor and interdigitated finger structures fabricated with PtPdAu-low Bi (12-16 μm thick) and two thin dielectrics (D1: 20 μm, D2: 30 μm), as shown in table 3.24. When the top electrode was applied with positive bias, there was a small increase in the leakage current initially, for all eight vehicles in group Low 1 (Figure 3.53) and Low 2 (Figure 3.54). The leakage current in all other groups remained relatively constant during 300°C aging with each polarity up to 2000 hours, as shown in figures 3.55 - 3.58.

Table 3.24: PtPdAu-low Bi test groups, thin dielectric thickness T_d, and polarities.

No.	Materials	T_d (μm)	Polarity
Low 1	PtPdAu-low Bi/D1/PtPdAu-low Bi	20	Positive bias on the top electrode
Low 2	PtPdAu-low Bi/D2/PtPdAu-low Bi	30	Positive bias on the top electrode
Low 3	PtPdAu-low Bi/D1/PtPdAu-low Bi	20	Positive bias on the bottom electrode
Low 4	PtPdAu-low Bi/D2/PtPdAu-low Bi	30	Positive bias on the bottom electrode
Low 5	PtPdAu-low Bi/D1/PtPdAu-low Bi	20	Interdigitated finger structure
Low 6	PtPdAu-low Bi/D2/PtPdAu-low Bi	30	Interdigitated finger structure

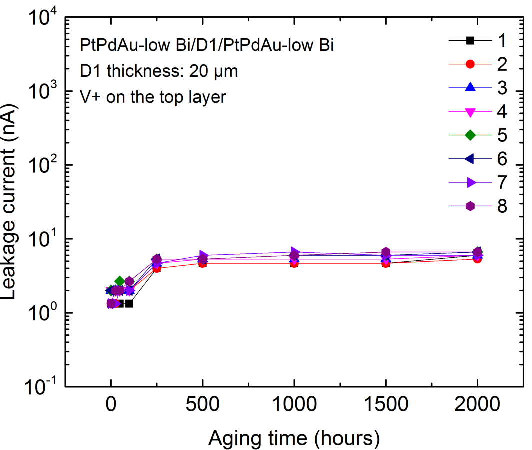

Figure 3.53: The leakage current of eight PtPdAu-low Bi/D1/PtPdAu-low Bi capacitor structures increased slightly after a short time in aging at 300°C.

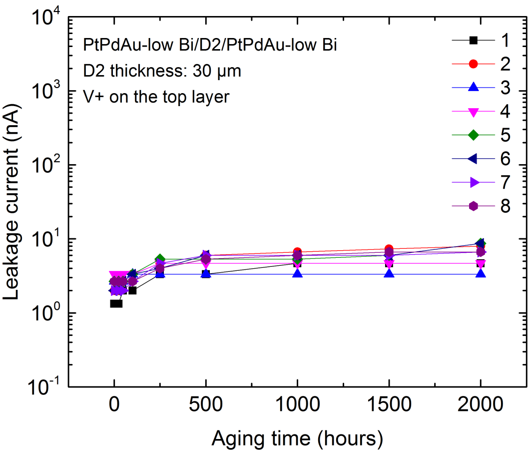

Figure 3.54: The leakage current of eight PtPdAu-low Bi/D1/PtPdAu-low Bi capacitor structures increased slightly after a short time in aging at 300°C.

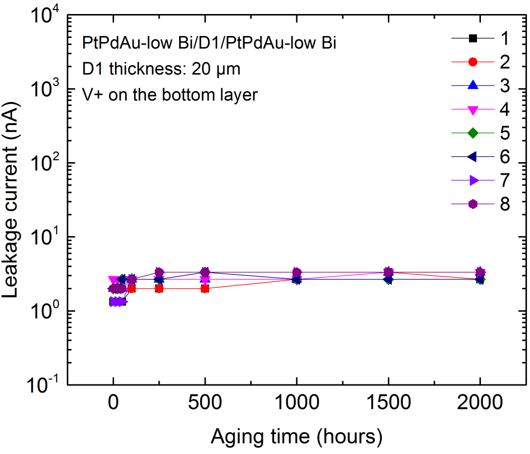

Figure 3.55: The leakage current of eight PtPdAu-low Bi/D2/PtPdAu-low Bi capacitor structures remained constant with aging at 300°C.

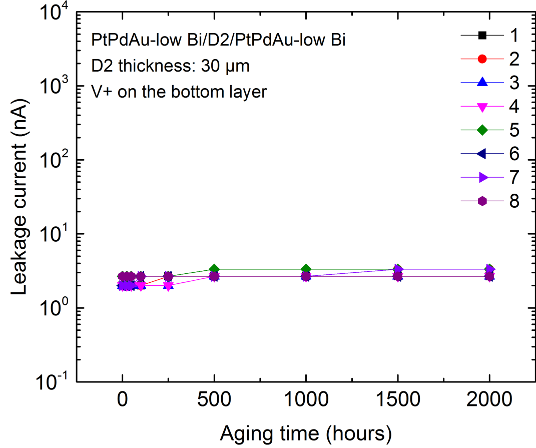

Figure 3.56: The leakage current of eight PtPdAu-low Bi/D2/PtPdAu-low Bi capacitor structures remained constant with aging at 300°C.

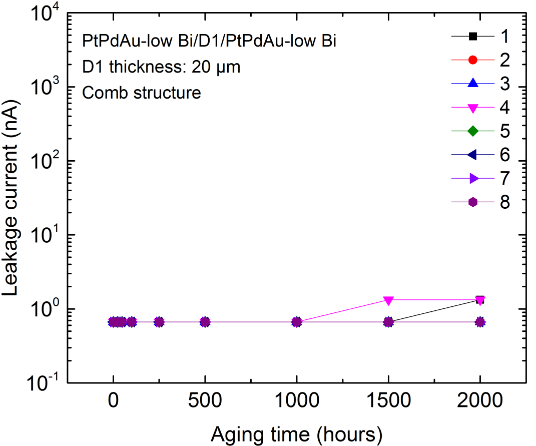

Figure 3.57: The leakage current of eight PtPdAu-low Bi/D1/PtPdAu-low Bi interdigitated finger structures remained constant with aging at 300°C.

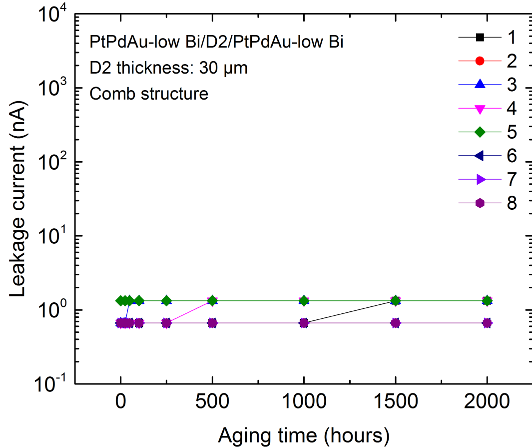

Figure 3.58: The leakage current of eight PtPdAu-low Bi/D2/PtPdAu-low Bi interdigitated finger structures remained constant with aging at 300°C.

3.3.3 Leakage current with alternating biased polarity

Based on the leakage current results at 300°C, additional experiments were designed for the PtPdAu capacitors with thin dielectric (D1: 20 μm, D2: 30 μm). Aging was at 350°C and the bias voltage was either 100 V or 200 V. During the 4000 hours test, the voltage bias direction was reversed every 1000 hours. Table 3.25 lists the test groups.

All eight PtPdAu/D1/PtPdAu and PtPdAu/D2/PtPdAu test vehicles were aged with the top electrode biased 100 V or 200 V positive with respect to the bottom electrode during the 0-1000 hours and 2000-3000 hours intervals. During the 1000-2000 hours and 3000-4000 hours intervals, all test vehicles were aged with the bottom electrode biased 100 V or 200 V positive with respect to the top electrode.

All eight PtPdAu/D1/PtPdAu and PtPdAu/D2/PtPdAu capacitors had a significant increase in leakage current after a short aging time regardless of the polarity. With the reversed polarity, the leakage current immediately decreased to a level that was still higher

Table 3.25: Alternating bias test groups with various dielectric materials, thicknesses T_d, bias voltages and polarities aging at 350 ° C.

No.	Materials	T_d (μm)	Bias (V)	Initial polarities
R1	PtPdAu/D1/ PtPdAu	20	100	Positive bias on the top electrode
R2	PtPdAu/D1/ PtPdAu	20	200	Positive bias on the top electrode
R3	PtPdAu/D2/ PtPdAu	30	100	Positive bias on the top electrode
R4	PtPdAu/D2/ PtPdAu	30	200	Positive bias on the top electrode
R5	PtPdAu/D1/ PtPdAu	20	100	Positive bias on the bottom electrode
R6	PtPdAu/D1/ PtPdAu	20	200	Positive bias on the bottom electrode
R7	PtPdAu/D2/ PtPdAu	30	100	Positive bias on the bottom electrode
R8	PtPdAu/D2/ PtPdAu	30	200	Positive bias on the bottom electrode

than the initial value and then increased again. The maximum leakage currents with positive polarity on the top conductor were higher than the values with reversed polarity. Figures 3.59-3.66 present the leakage current results of thin dielectric patterns at 350°C aging, with the periodically reversed polarity (100 V, 200 V) at each 1000 hours interval.

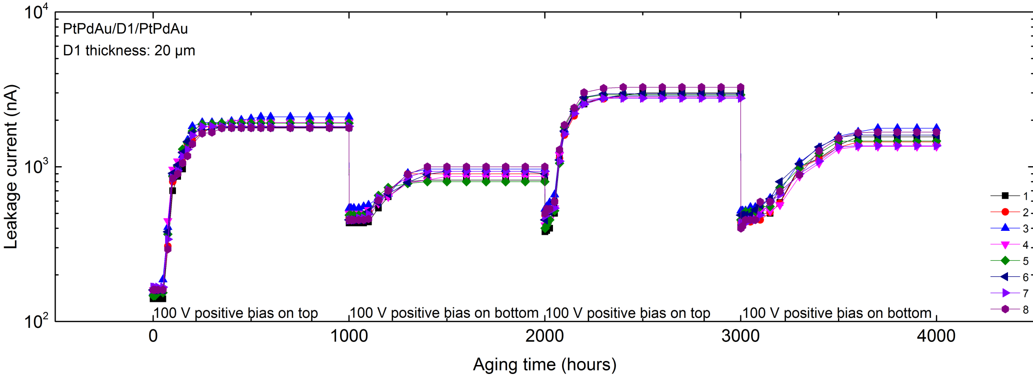

Figure 3.59: The leakage current of eight PtPdAu/D1/PtPdAu capacitors with periodically alternating polarity (100 V biased positive on the top electrode initially), aging at 350°C.

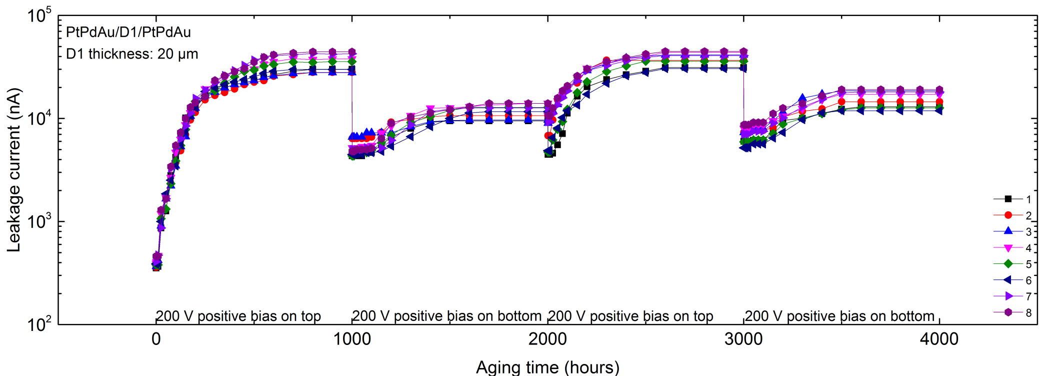

Figure 3.60: The leakage current of eight PtPdAu/D1/PtPdAu capacitors with periodically alternating polarity (200 V biased positive on the top electrode initially), aging at 350°C.

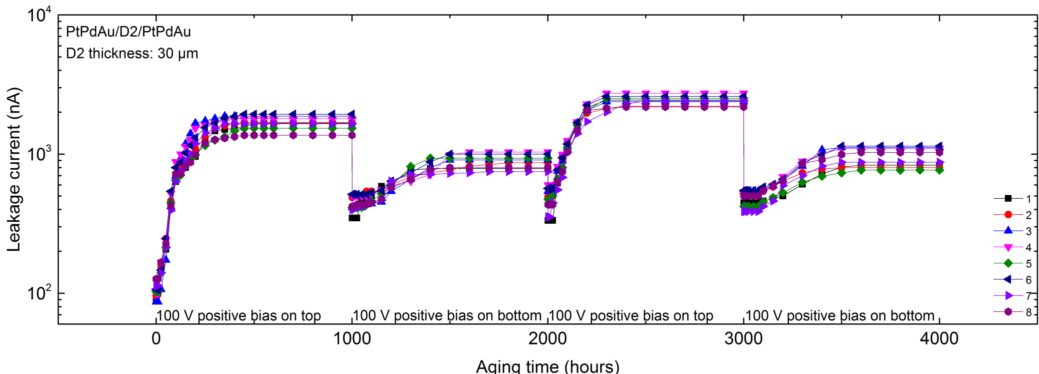

Figure 3.61: The leakage current of eight PtPdAu/D2/PtPdAu capacitors with periodically alternating polarity (100 V biased positive on the top electrode initially), aging at 350°C.

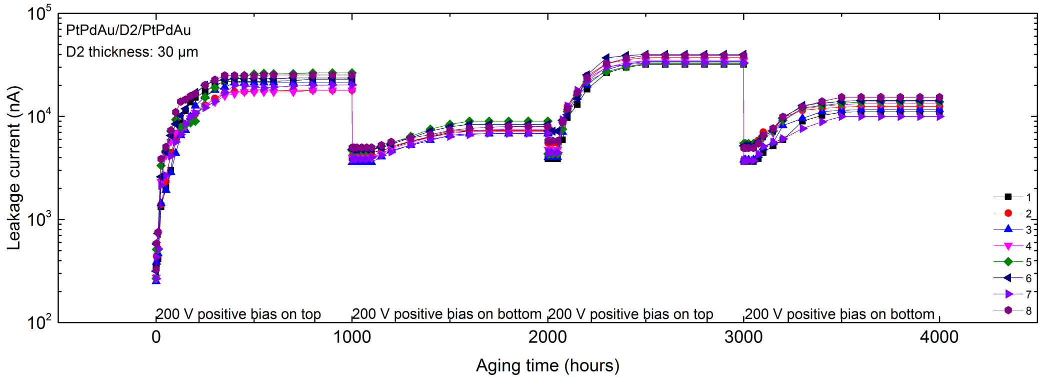

Figure 3.62: The leakage current of eight PtPdAu/D2/PtPdAu capacitors with periodically alternating polarity (200 V biased positive on the top electrode initially), aging at 350°C.

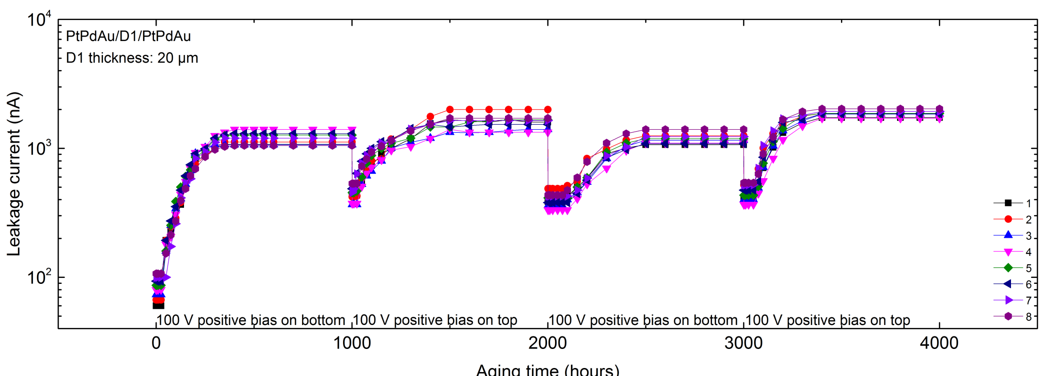

Figure 3.63: The leakage current of eight PtPdAu/D1/PtPdAu capacitors with periodically alternating polarity (100 V biased positive on the bottom electrode initially), aging at 350°C.

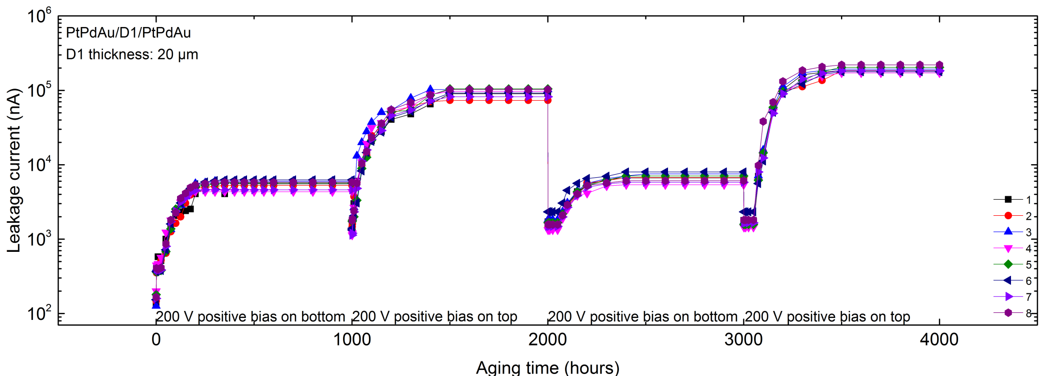

Figure 3.64: The leakage current of eight PtPdAu/D1/PtPdAu capacitors with periodically alternating polarity (200 V biased positive on the bottom electrode initially), aging at 350°C.

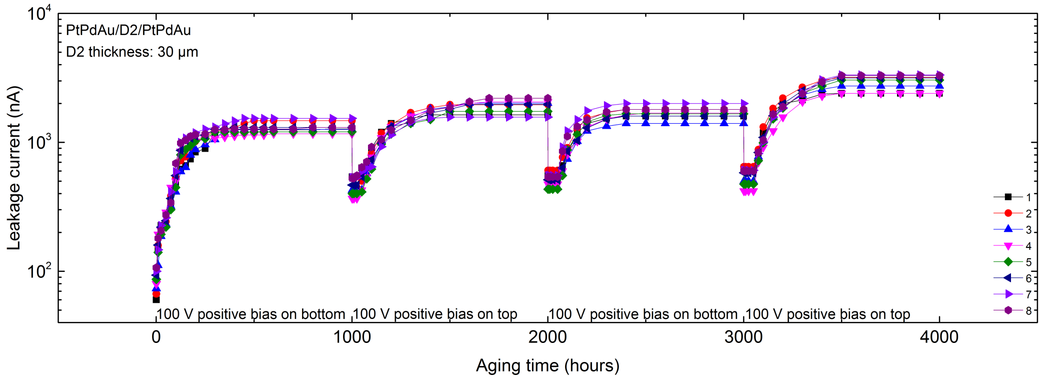

Figure 3.65: The leakage current of eight PtPdAu/D2/PtPdAu capacitors with periodically alternating polarity (100 V biased positive on the bottom electrode initially), aging at 350°C.

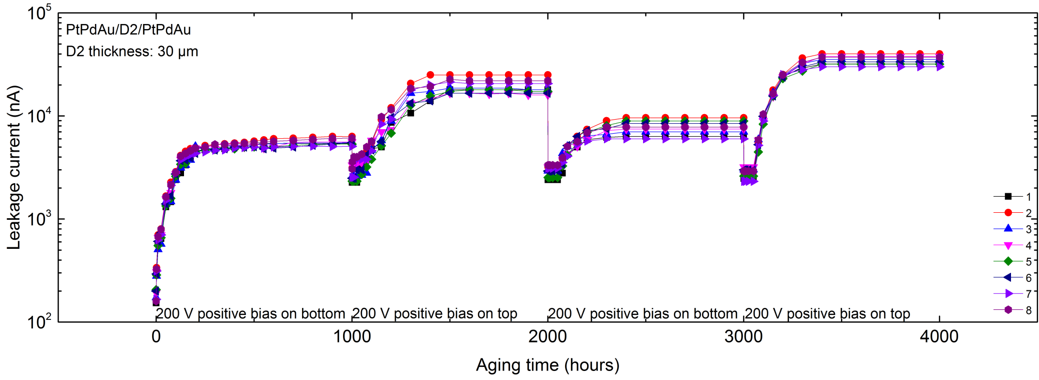

Figure 3.66: The leakage current of eight PtPdAu/D2/PtPdAu capacitors with periodically alternating polarity (100 V biased positive on the bottom electrode initially), aging at 350°C.

3.4 Summary

In summary, four thick film pastes, conductor PtPdAu, Au, dielectric D1 and D2 were evaluated. test vehicles were designed as capacitor and interdigitated finger structures. The leakage currents of these structures were measured during aging at 300°C for 2000 hours with 100 V biased on each polarity.

The leakage current increased significantly only when the conductor layer was printed with PtPdAu and thin dielectric (D1: 20 μm, D2: 30 μm). The leakage current was constant with time at 300°C if the conductor layer was fabricated with pure Au or if the dielectric was thick (D1: 30 μm, D2: 40 μm). The leakage currents of the interdigitated finger structures were constant with time at 300°C in all test group.

Bi in the PtPdAu paste diffused into dielectrics D1 and D2 during the firing process and resulted in an significant increase in leakage current after a short time aging if the dielectric was thin. The leakage current increase could be avoided by increasing the dielectric thickness to prevent Bi from diffusing through the entire thickness of the dielectric. The maximum leakage current increase was directly correlated to the electrical polarity. With positive bias voltage on the top electrode, test vehicles showed a higher increase in leakage

current compared to the ones with positive bias voltage on the bottom electrode. When the electrical polarity was alternating during aging, the leakage current decreased immediately, then increased again.

Chapter 4

Leakage Current Mechanism in Thick Film Dielectric with Bi

To study the effect of Bi on the leakage current of the dielectrics, we mixed Bi_2O_3 nano particles with the undoped dielectrics, D1 and D2, to produce dielectrics with various Bi concentration (D1mix and D2mix).

4.1 Dielectrics with Bi_2O_3

Bi_2O_3 nano particles were purchased from the Inframat Advanced Material company. Since the nano particles aggregated and the thick film dielectric paste didn't wet the Bi_2O_3 particle, the Bi_2O_3 nano particles were mixed into thick film vehicle solvent with ultrasonic vibration to deagregate the particles and improve the wetting, aiding in the mixing process. The mixture was dispersed by ultrasonic horn for 1 hour to disperse the aggregation of Bi_2O_3 nano particles. After dispersion, the mixture stood for 30 minutes at room temperature to allow the Bi_2O_3 particles to settle, separating the solid Bi_2O_3 particles and excessive vehicle solvent. The excessive vehicle was removed with a syringe and the Bi_2O_3 particles wetted with vehicle were mixed into D1 and D1 respectively. By controlling the additive of Bi_2O_3 into the dielectrics, the Bi concentration (wt%) in the fired dielectric layers was designed to be 3 wt%, 6 wt%, and 9 wt%. The cross sections of the fire dielectrics were analyzed by EDS to confirm the Bi concentration. Results showed that the Bi was distributed in the dielectric uniformly in weight concentration of 3.5%, 6.2% and 9.3%, respectively.

The vehicles for the leakage current test with Bi doped dielectrics (Au/D1mix/Au and Au/D2mix/Au), were fabricated via the same process in Chapter 3. The bottom electrodes were screen printed with thick film Au on 96% Al_2O_3 ceramic substrates, dried (150°C) and fired (850°C). Then two layers of D1mix and three layers of D2mix were printed over the

bottom electrodes. Each dielectric layer was sequentially printed, dried (150°C) and fired (850°C). Finally, the top electrode conductor was printed, dried (150°C) and fired (850°C).

The vehicles for the leakage current test, Au/D1mix/Au and Au/D2mix/Au, were printed with the mixed dielectric by thick film screen printing. The dielectric thickness was thin (D1mix: 20 μm, D2mix: 30 μm). All layers were dried at 150°C for 10 minutes and fired at 850°C for 10 minutes. All test vehicles were aged at 300°C with 100 V bias voltage with both polarities. Table 4.1 lists the materials, Bi wt% and biased polarities for the leakage current test vehicles.

Table 4.1: Materials and Bi wt% in dielectrics for leakage current test.

Group	Materials	Polarities
M1	Au/D1 with 3 wt% Bi/Au	Positive biased on the top electrode
M2	Au/D2 with 3 wt% Bi/Au	Positive biased on the top electrode
M3	Au/D1 with 6 wt% Bi/Au	Positive biased on the top electrode
M4	Au/D2 with 6 wt% Bi/Au	Positive biased on the top electrode
M5	Au/D1 with 9 wt% Bi/Au	Positive biased on the top electrode
M6	Au/D2 with 9 wt% Bi/Au	Positive biased on the top electrode
M7	Au/D1 with 3 wt% Bi/Au	Positive biased on the bottom electrode
M8	Au/D2 with 3 wt% Bi/Au	Positive biased on the bottom electrode
M9	Au/D1 with 6 wt% Bi/Au	Positive biased on the bottom electrode
M10	Au/D2 with 6 wt% Bi/Au	Positive biased on the bottom electrode
M11	Au/D1 with 9 wt% Bi/Au	Positive biased on the bottom electrode
M12	Au/D2 with 9 wt% Bi/Au	Positive biased on the bottom electrode

Figures 4.1-4.4 show the leakage current for the groups M1-M12. The leakage current in all 12 groups increased significantly after a short time at 300°C. The initial and after bias leakage current were directly correlated to the bismuth concentration mixed in the dielectric. The 9% vehicle was more conductive initially and after bias, compared to the 3% and 6% vehicles. Positive bias on the top electrode resulted in a slightly higher leakage current than positive bias on the bottom electrode. D1mix and D2mix were comparable.

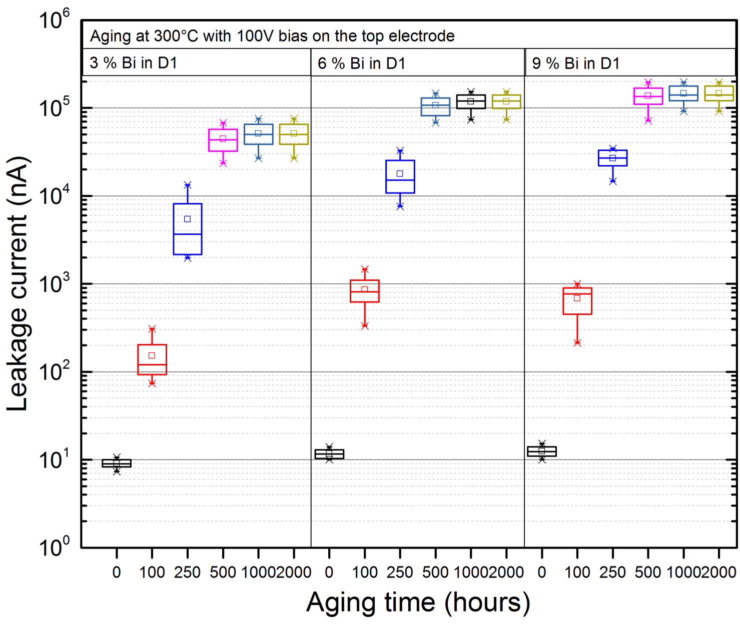

Figure 4.1: Leakage current of test groups M1, M3 and M5.

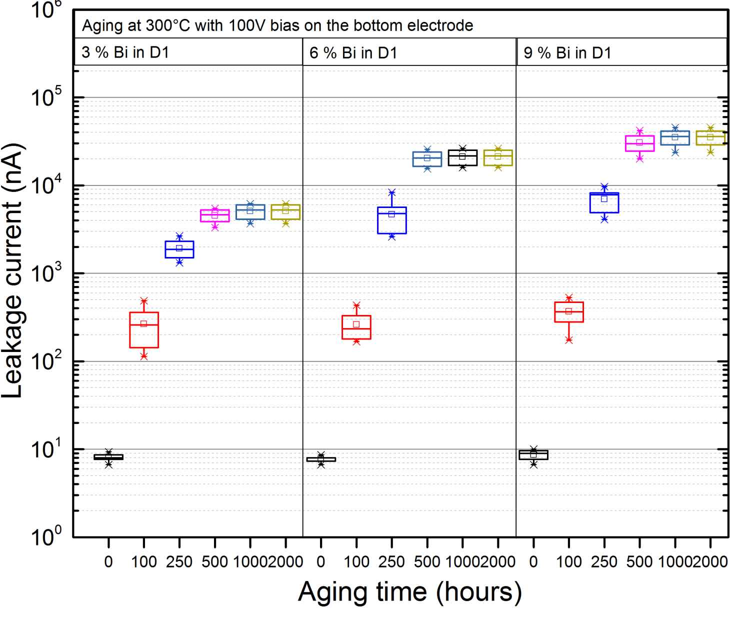

Figure 4.2: Leakage current of test groups M2, M4 and M6.

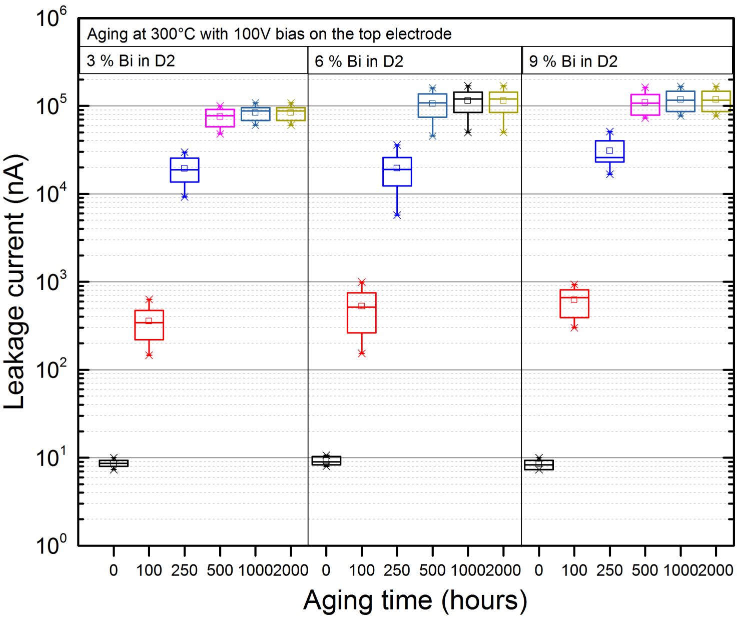

Figure 4.3: Leakage current of test groups M7, M9 and M11.

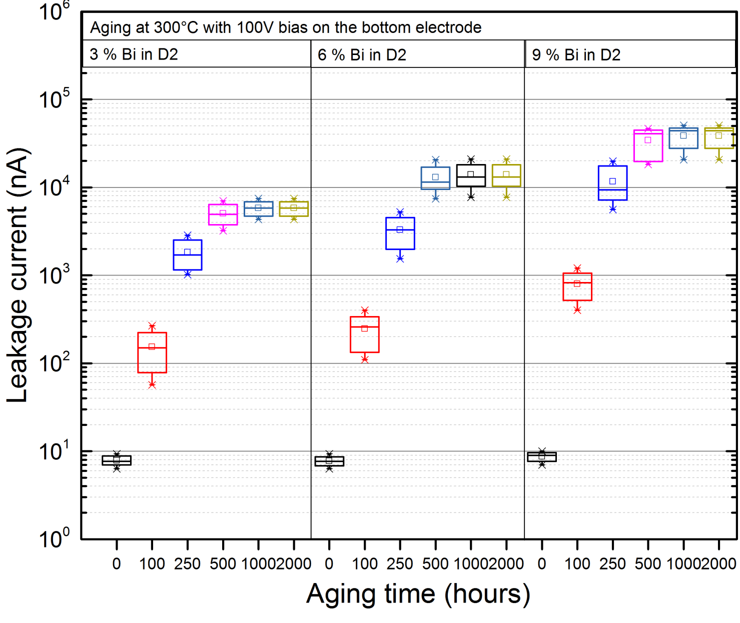

Figure 4.4: Leakage current of test groups M8, M10 and M12.

4.2 Electron traps in thick film dielectrics with Bi

In the aging of capacitors with thin dielectrics, there were two factors to be considered. Did the increase in leakage current result from the applied electric field or the flow of leakage current? In this section, experiments were designed to separate the influences of leakage current and bias voltage (electric field).

4.2.1 Experiment design

Insulating substrate

Sapphire substrates were selected to replace the 96% ceramic substrates because sapphire was transparent to UV-vis spectroscopy analysis and the coefficient of thermal expansion (CTE) of sapphire was compatible with the thick film dielectric. The CTE of Al_2O_3 substrate was compatible with the thick film dielectric but could not be used for UV-vis spectroscopy analysis. SiO_2 substrates were transparent but the thick film dielectric cracked after firing due to the CTE mismatch. Table 4.2 lists the coefficient of thermal expansion of 96% Al_2O_3, SiO_2, and sapphire, in the range of 20°C-1000°C[72].

Table 4.2: The CTE of 96% Al_2O_3, SiO_2, and sapphire, (20°C-1000°C)[72].

Substrate	96% Al_2O_3	SiO_2	Sapphire
CTE (10^{-6}/°C)	7.8-9.0	0.55	7.9-8.8

Table 4.3 lists the test vehicles with different dielectrics on sapphire substrates and aging time. A single layer of dielectric was printed, dried (150°C) and fired (850°C) on the sapphire substrates. A 10 μm aluminum layer was deposited via e-beam on both the dielectric layer and on the back of the substrates, as the top and bottom electrodes. After aging, the aluminum was removed by chemical etching, and all samples were analyzed by UV-vis spectroscopy.

Table 4.3: Vehicles with different dielectrics on sapphire substrate for UV-vis analysis.

No.	Dielectric	Aging time (hours)
S1	Undoped D1	0
S2	D1 doped with 3% Bi	0
S3	D1 doped with 3% Bi	500 (without bias)
S4	D1 doped with 3% Bi	500 (with positive bias on the top electrode)

The sapphire substrate is a dielectric and adds a series capacitor dielectric between the two Al electrodes. The electric field distribution between the sapphire and the thin D1mix must be considered to determine the appropriate bias voltage between the two Al electrodes to achieve the desired voltage (electric field) across the thin D1mix. Figures 4.5-4.6 show the cross section schematic of Al/D1/sapphire and the equivalent capacitor model. The sapphire substrate and dielectric were considered as an equivalent dielectric. The positive bias voltage was applied to the top Al layer with the respective electrode on the probe station. Table 4.4 lists the parameter symbols and definitions in the equations. Equations 4.1-4.7 illustrate the calculation of the adjusted bias voltage. The adjusted bias voltage was set to 1700 V to provide 100 V across the dielectric.

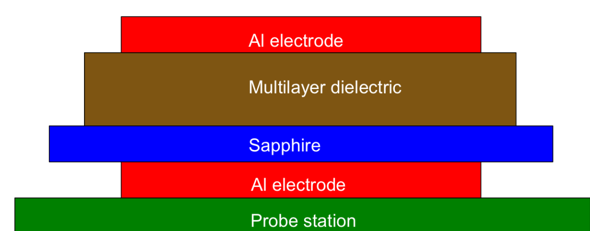

Figure 4.5: The cross section of the Al/D1 with Bi_2O_3 on sapphire substrate placed on probe station during aging

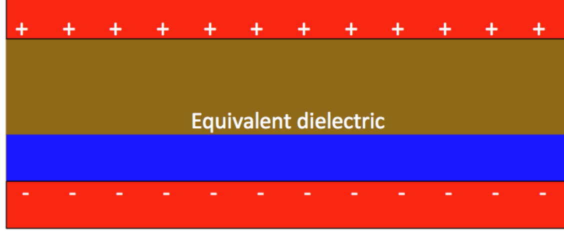

Figure 4.6: The cross section of the equivalent capacitor model during aging.

Table 4.4: Parameter symbols and definitions in equations

Symbol	Definition
E_e	Equivalent electrical field in capacitor model with sapphire substrate
Q_e	Equivalent charges in capacitor model with sapphire substrate
ϵ_e	Equivalent permittivity in capacitor model with sapphire substrate
V_{adj}	Adjusted bias voltage in capacitor model with sapphire substrate
C_e	Equivalent capacitance in capacitor model with sapphire substrate
d_e	Total distance between parallel plates in capacitor model with sapphire substrate: 340 μm
A_e	Equivalent parallel plate area in capacitor model with sapphire substrate
E_o	Original electrical field in PtPdAu/D1/PtPdAu capacitor with 20 μm D1
Q_o	Original charges in PtPdAu/D1/PtPdAu capacitor with 20 μm D1
ϵ_o	Original permittivity in PtPdAu/D1/PtPdAu capacitor with 20 μm D1
V_o	100 V bias voltage on PtPdAu/D1/PtPdAu capacitor
C_o	Original capacitance in PtPdAu/D1/PtPdAu capacitor with 20 μm D1
d_o	20 μm D1
A_o	Original parallel plate area in PtPdAu/D1/PtPdAu capacitor

According to the parallel capacitor properties, we know:

$$E = \frac{Q}{\epsilon A} \tag{4.1}$$

$$Q = CV \tag{4.2}$$

$$C = \frac{\epsilon A}{d} \tag{4.3}$$

From equation 4.3, then:

$$\epsilon = \frac{dC}{A} \tag{4.4}$$

To ensure $E_e = E_o$, then:

$$\frac{E_e}{E_o} = \frac{Q_e}{Q_0} \times \frac{\epsilon_o A_o}{\epsilon_e A_e} = 1 \tag{4.5}$$

As A_o=A_s, according to equition 4.2, we know:

$$\frac{E_e}{E_o} = \frac{C_e V_{adj}}{C_o V_o} \times \frac{C_o d_0}{C_e d_e} = 1 \tag{4.6}$$

Thus:

$$V_{adj} = \frac{d_e}{d_o} \times V_o = 17 \times 100V = 1700V \tag{4.7}$$

Conductive substrate

Platinum foil was used to replace the 96% ceramic substrates. Two layers of dielectric D1mix were sequentially printed, dried, and fired on the platinum foil and a 10 μm aluminum layer was deposited as the top electrode via e-beam or sputtering. Figure 4.7 shows the cross section schematic of the Al/D1/Pt. Table 4.5 lists the test vehicles with different dielectrics on Pt foil substrates and aging time. The P2 vehicle was aged at 300°C without bias. The P3 vehicle was aged at 300°C with a 100 V positive bias voltage on the top aluminum layer and the negative on the bottom platinum foil. Additionally, test vehicles P5 - P13 (as listed in table 4.5) were fabricated to study how the Bi concentration in the dielectric influenced the dielectric conductivity. The dielectric layers were sequentially printed, dried, and fired on the platinum foil and a 5 μm aluminum layer was sputtering on top of the dielectric as the electrode. Test vehicles P6, P9, and P12 were aged at 300°C, without bias. P7, P10, and P13 were aged at 300°C with a 100 V positive bias voltage on the top aluminum layer and the negative on the bottom platinum foil.

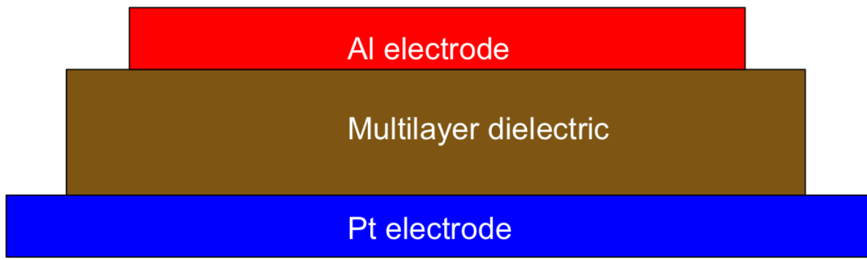

Figure 4.7: The cross section of Al/D1/Pt, D1 thickness: 20 μm.

Table 4.5: Patterns with Bi doped and undoped dielectric D1 on platinum foil substrates for UV-vis analysis.

No.	Dielectric	Aging time (hours)
Ebeam Al		
P1	Undoped D1	0
P2	D1 doped with 3% Bi	0
P3	D1 doped with 3% Bi	500 (without bias voltage)
P4	D1 doped with 3% Bi	500 (with 100V positive bias on the top electrode)
Sputtering Al		
P5	D1 doped with 3% Bi	0
P6	D1 doped with 3% Bi	500 (without bias voltage)
P7	D1 doped with 3% Bi	500 (with 100V positive bias on the top electrode)
P8	D1 doped with 6% Bi	0
P9	D1 doped with 6% Bi	500 (without bias voltage)
P10	D1 doped with 6% Bi	500 (with 100V positive bias on the top electrode)
P11	D1 doped with 9% Bi	0
P12	D1 doped with 9% Bi	500 (without bias voltage)
P13	D1 doped with 9% Bi	500 (with 100V positive bias on the top electrode)

After aging, the aluminum was removed by chemical etching. All dielectric layers on Pt were lifted off from the platinum foil for UV-vis analysis. Although the Al etching for all samples followed the same process, it was noticed that the Al on test vehicles P9, P10, P12, and P13 did not etch properly. Al residuals on the dielectrics of these test vehicles were visually identified. These Al residuals affected the UV-vis analysis of these patterns. Further experiments are required to eliminate the Al residual on the P9, P10, P12 and P13 vehicles by polishing before UV-vis analysis.

4.2.2 Results

Figure 4.8 plots the leakage current of P4 (Al/D1 with 3% Bi/Pt) and S4 (Al/D1 with 3% Bi/sapphire) with 100 V positive bias on the top aluminum layer and the negative on the bottom platinum foil or bottom Al electrode respectively, aged at 300°C. The leakage current of P4 increased significantly after a short time in aging. The leakage current of

S4 was relatively constant during aging as expected due to the insulation properties of the sapphire.

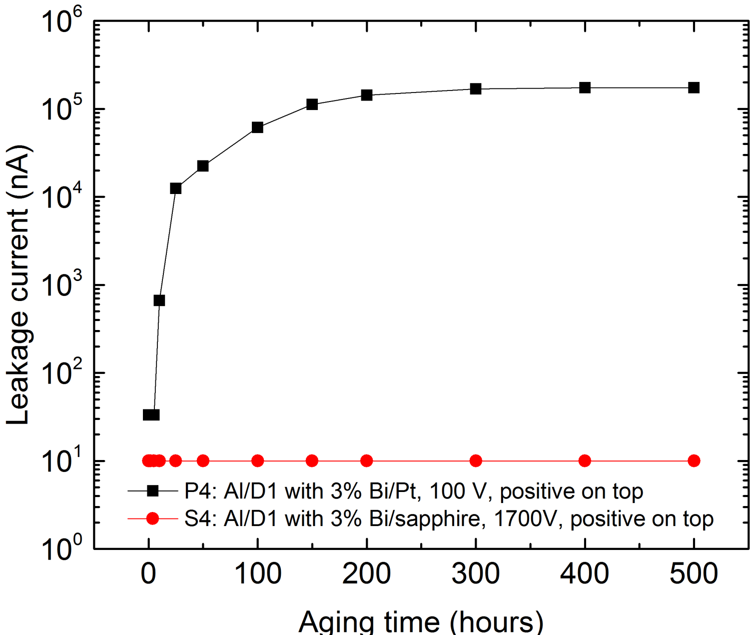

Figure 4.8: The leakage current of P4 (Al/D1 with 3% Bi/Pt biased with 100 V on the top electrode) and S4 (Al/D1 with 3% Bi/sapphire with 1700 V on the top electrode), aging at 300°C, D1 thickness: 20 μm.

Figure 4.9 plots the leakage current of P7 (Al/D1 with 3% Bi/Pt), P10 (Al/D1 with 6% Bi/Pt) and P13 (Al/D1 with 9% Bi/Pt) with a 100 V positive bias on the top aluminum layer and the negative on the bottom platinum foil or bottom Al electrode respectively, aged at 300°C. The leakage current of P7, P10 and P13 increased significantly after a short time in aging. The leakage current tended to be slightly higher in the test vehicles with higher Bi concentration in the dielectrics, corresponding to the previous results.

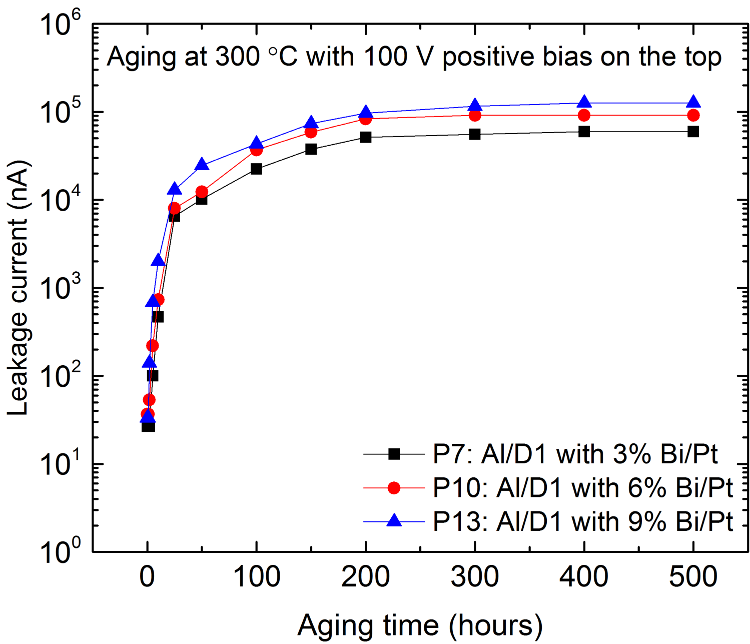

Figure 4.9: The leakage current of P7, P10 and P13, aging at 300°C, D1 thickness: 20 μm.

4.2.3 Analysis

Figure 4.10 shows the UV-vis analysis results for the bare sapphire substrates and vehicles S1 - S4. Bare sapphire substrates did not absorb light between 200 - 800 nm. S2 - S4 have absorption peaks in the same range between 520 - 650 nm, meaning the peaks were contributed by the base dielectric, instead of doped Bi. There were significant absorption peaks between 200 - 310 nm for the patterns S2 -S4. The absorbance for S2, S3, and S4 were higher compared to S1 with undoped D1, which means adding Bi_2O_3 resulted in a UV-vis absorption increase between 200 - 310 nm. Aging at 300°C with or without bias voltage did not influence the absorption.

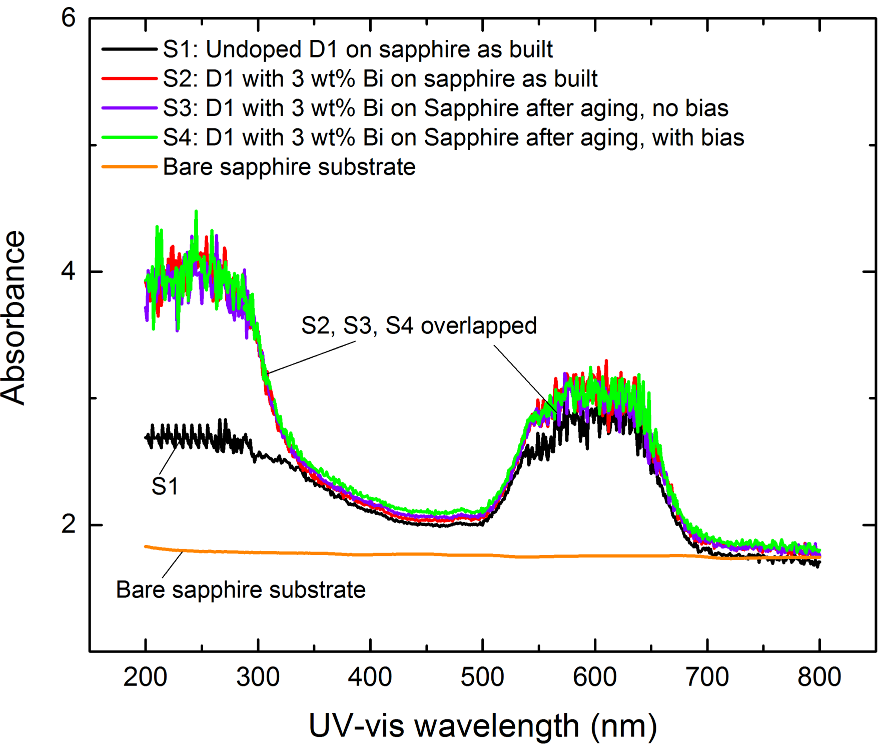

Figure 4.10: The UV-vis spectrums of bare sapphire substrate, Al/bare D1/sapphire, Al/D1 with 3% Bi/sapphire as build, and after 500 hours aging with or without bias voltage.

Figure 4.11 shows the UV-vis analysis results for the patterns P1 - P4. Compared to P1 plot, P2, P3 and P4 had significant absorption peaks between 200 - 310 nm, which means adding Bi_2O_3 resulted in a UV-vis absorbance increase between 200 - 310 nm. The absorbance of P4 was higher compared to P2 and P3, which means the leakage current flow activated the dielectric with Bi with aging at 300°C. Aging without bias voltage did not influence the absorption due to the lack of leakage current. To determine the energy level of the electron traps, a Tauc plot was used. Figure 4.12 shows the Tauc plot of spectrums of P2 - P4. The plot calculated that the electron traps were at 3.5 eV.

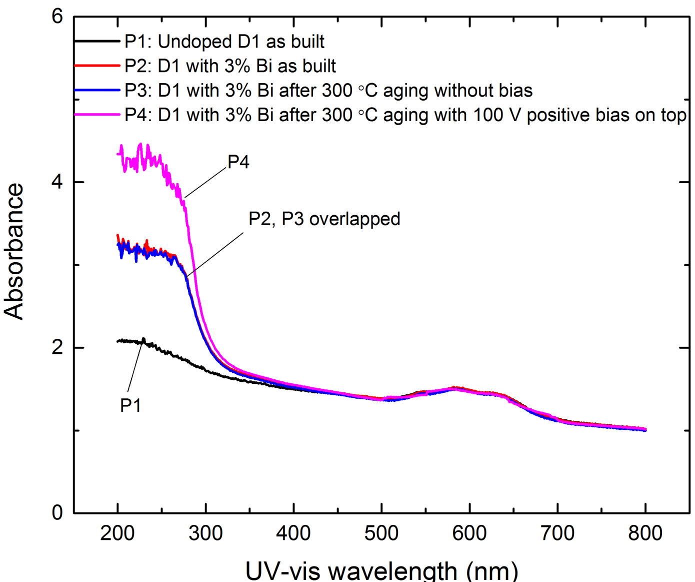

Figure 4.11: The UV-vis spectrums of P1 - P4.

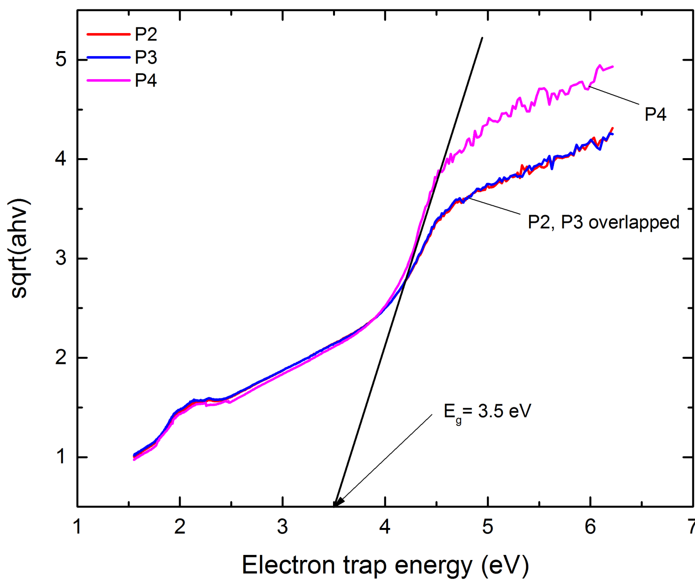

Figure 4.12: The Tauc plots of UV-vis spectrums in figure 4.11. The electron traps were 3.5 eV.

Figure 4.13 shows the UV-vis analysis results for the patterns P5 - P7. The spectrum of P7 showed a significant absorption peak between 200 - 310 nm, corresponding to the spectrum of P4 in figure 4.11. The absorbance of P7 confirmed that the leakage current flow activated the dielectric with Bi with aging at 300°C. To determine the energy level of the electron traps from the UV-vis spectrums of P5 - P7, a Tauc plot was used, as shown in figure 4.14. The plot calculated that the electron traps were at 3.2 eV.

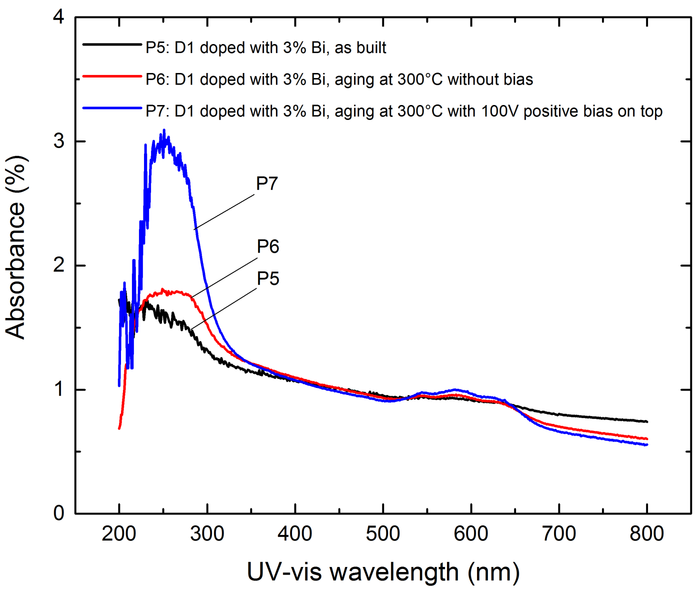

Figure 4.13: The UV-vis spectrums of P5 - P7.

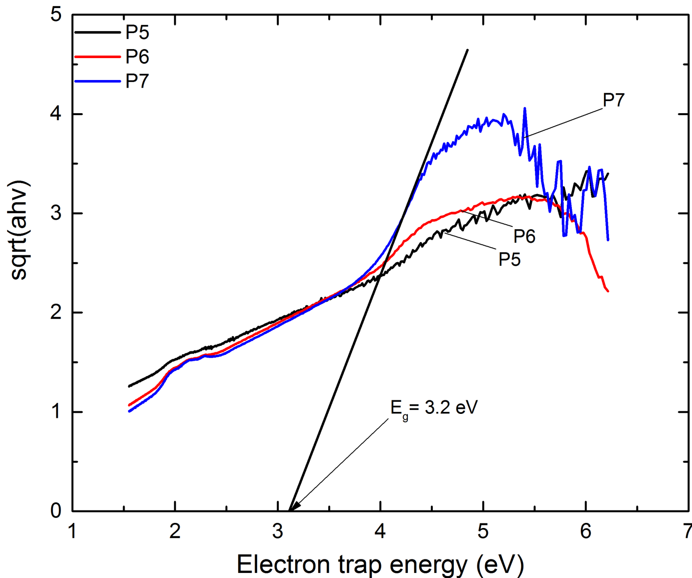

Figure 4.14: The Tauc plots of UV-vis spectrums in figure 4.13. The electron traps energy were 3.2 eV.

4.3 Summary

By adding bismuth oxide nano particles into dielectric, D1, we could use UV-vis spectroscopy to measure the electron traps created by doped Bi in the thick film dielectric. Calculated from the Tauc plot, the electron traps were at 3.2-3.5 eV in the dielectric with 3wt% Bi.

Chapter 5

Mechanical Reliability of Thick Film Materials

Multilayer thick film circuits built with conductors and dielectrics are widely used in high temperature applications. To keep the electronics functioning properly, the mechanical reliability requires good adhesion between the substrate and the thick film and between each thick film layer after high temperature exposure. In this chapter, the adhesion of multilayer thick films by pull testing is discussed.

5.1 Experiment method

Two conductive thick film pastes (PtPdAu, Au) and two thick film dielectric pastes (D1, D2) were selected to fabricate capacitor structures.

The test vehicle design is shown in figure 5.1. Each test vehicle contained 6 identical capacitors. The bottom capacitor electrodes were printed on 96% Al_2O_3 ceramic substrates, dried (150°C) and fired (850°C). Then two layers of thick film dielectric D1 or three layers of thick film D2 were printed over the capacitor bottom electrodes. Each dielectric layer was sequentially printed, dried (150°C) and fired (850°C). Finally, the top capacitor electrode conductor was printed, dried (150°C) and fired (850°C). Figure 5.2 is a photograph of the test vehicle as built.

In this research, the conductors were fabricated with the thicknesses recommended in the manufacturer's instructions. Dielectric thicknesses were fabricated at two thicknesses: the "thick dielectric" corresponded to the recommended dielectric thickness on the paste manufacturer's instructions, and the "thin dielectric" was 10 μm less than recommended value.

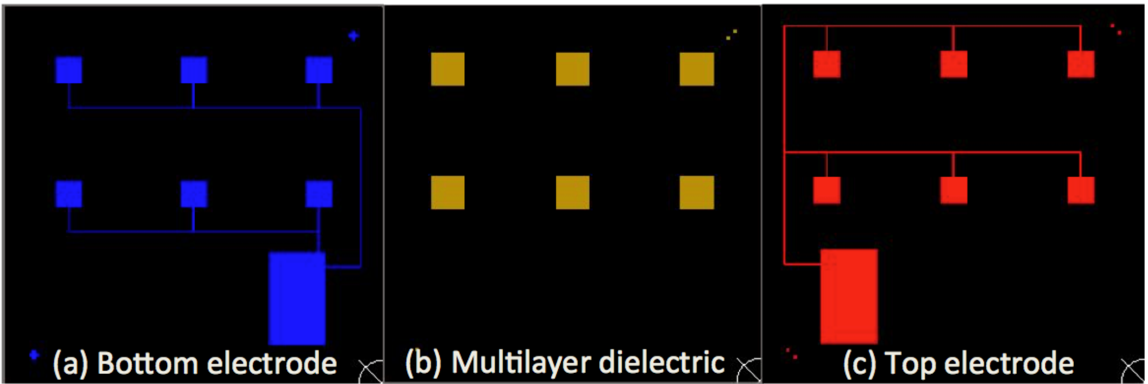

Figure 5.1: Design of the adhesion test vehicle. (a) Pattern for bottom electrode. (b) Pattern for multilayer dielectric. (c) Pattern for top electrode.

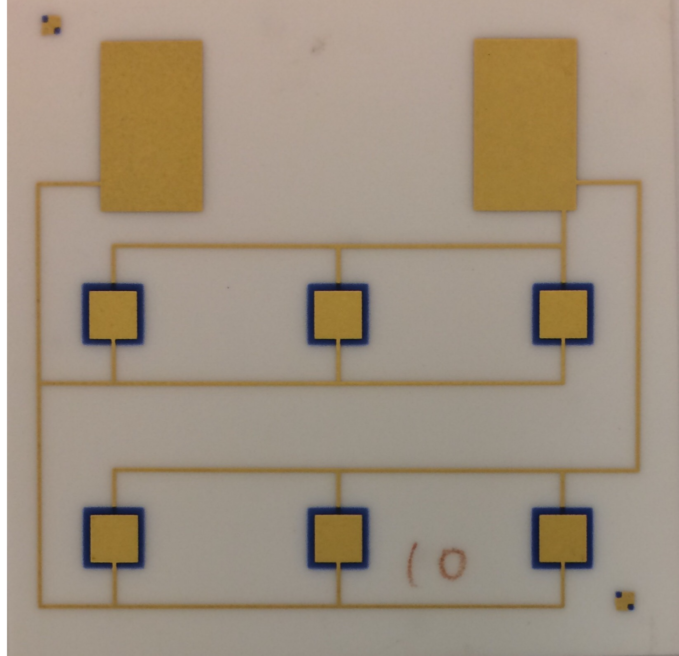

Figure 5.2: Photograph of the test vehicle. The pattern was printed by thick film gold and dielectric (D1), on a 2 inch by 2 inch ceramic substrate.

The test vehicles were fabricated and aged at 300°C with bias. The 100 V bias was applied on either the top or bottom conductor in different test groups. Table 5.1 lists the test groups 1-16 with the materials, dielectric thicknesses, and polarities.

Table 5.1: The test groups with materials, dielectric thicknesses (T_d), and polarities in aging.

No.	Materials	T_d (μm)	Polarity
1	PtPdAu/D1/ PtPdAu	20	Positive bias on top conductor
2	PtPdAu/D1/ PtPdAu	20	Positive bias on bottom conductor
3	Au/D1/ Au	20	Positive bias on top conductor
4	Au/D1/ Au	20	Positive bias on bottom conductor
5	PtPdAu/D2/ PtPdAu	30	Positive bias on top conductor
6	PtPdAu/D2/ PtPdAu	30	Positive bias on bottom conductor
7	Au/D2/ Au	30	Positive bias on top conductor
8	Au/D2/ Au	30	Positive bias on bottom conductor
9	PtPdAu/D1/ PtPdAu	30	Positive bias on top conductor
10	PtPdAu/D1/ PtPdAu	30	Positive bias on bottom conductor
11	Au/D1/ Au	30	Positive bias on top conductor
12	Au/D1/ Au	30	Positive bias on bottom conductor
13	PtPdAu/D2/ PtPdAu	40	Positive bias on top conductor
14	PtPdAu/D2/ PtPdAu	40	Positive bias on bottom conductor
15	Au/D2/ Au	40	Positive bias on top conductor
16	Au/D2/ Au	40	Positive bias on bottom conductor

A 2000 hours, 300°C, 100 V biased adhesion test was performed on each group. Twelve patterns were tested as-built, and after 100 hours, 250 hours, 500 hours, 1000 hours, and 2000 hours at 300°C with 100 V bias.

In the pull test, each test vehicle was diced into 6 identical patterns. A ceramic plate was glued to the substrate backside to reinforce the substrate strength and prevent the substrate from cracking during the test. One side of the ceramic plate was coated with epoxy and held in contact with the substrate backside with an aluminum fixture. After being pre-cured at 150°C for 10 minutes and cooled down, an aluminum stud with epoxy coated on the head was attached to the top layer of thick film on the pattern. The entire assembly test structure was cured at 150°C for 60 minutes to harden the epoxy. The pattern was placed on the test platform with the thick film layers facing down. A chuck was use to clamp the end of the aluminum stud, the stud was pulled vertically down with gradually increasing force. Figure 5.3 illustrates the pull test configuration.

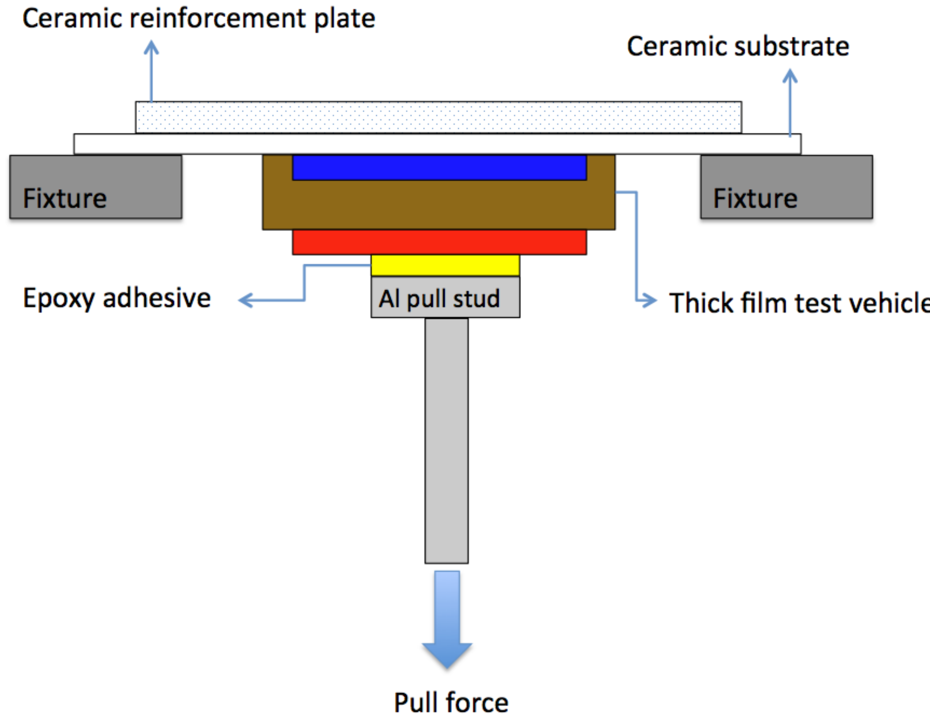

Figure 5.3: Illustration of pull test.

5.2 Adhesion test result

5.2.1 Thin dielectrics

The failure interface for the as-built PtPdAu/D1/PtPdAu (dielectric thickness: 20 μm) patterns was in the epoxy. For the patterns in group 1 with the positive bias applied to the top electrode with respect to the bottom electrode, the failure interface was between the dielectric and the bottom conductor layer for the patterns aged 100 hours through 2000 hours (Figure 5.4). There was a significant decrease in the pull strength during the first 500 hours. For the patterns with the reverse bias in group 2, the failure interface remained in the epoxy at all the test intervals through 2000 hours and the adhesion remained high (Figure 5.4).

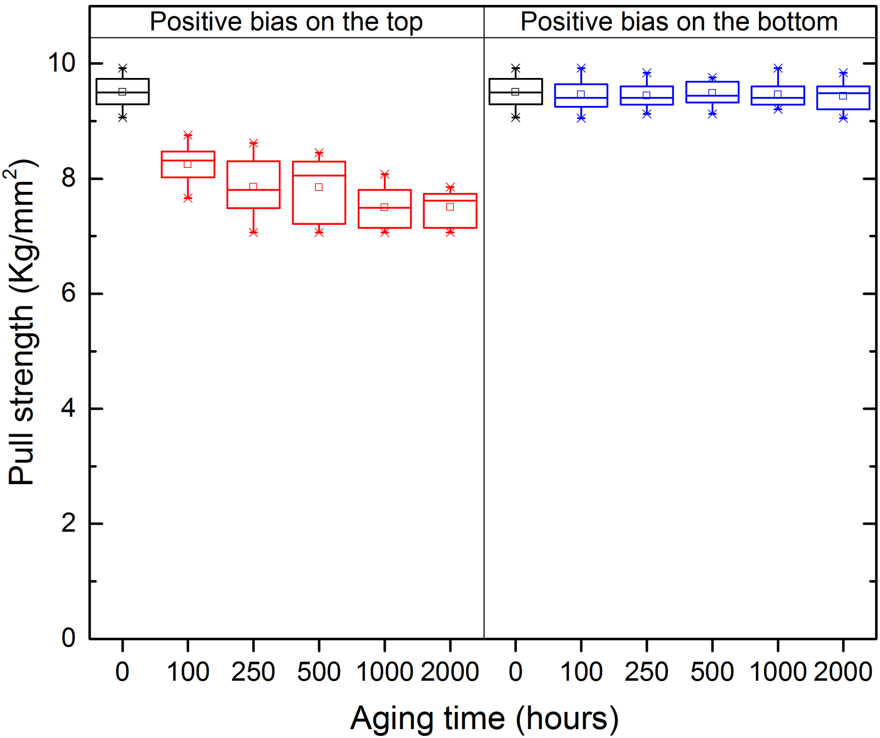

Figure 5.4: The pull strength of the PtPdAu/D1/PtPdAu patterns with 20 μm dielectric thickness. The pull strength decreased after the 100 hours aging with the positive bias applied on the top conductor. The pull test failure surface was at the interface of the bottom electrode and the dielectric layer.

The failure interface for the Au/D1/Au (dielectric thickness: 20 μm) patterns (groups 3 and 4) was in the epoxy for both bias polarities and at all time intervals. The pull strength was relatively constant at all the test intervals through 2000 hours (Figure 5.5).

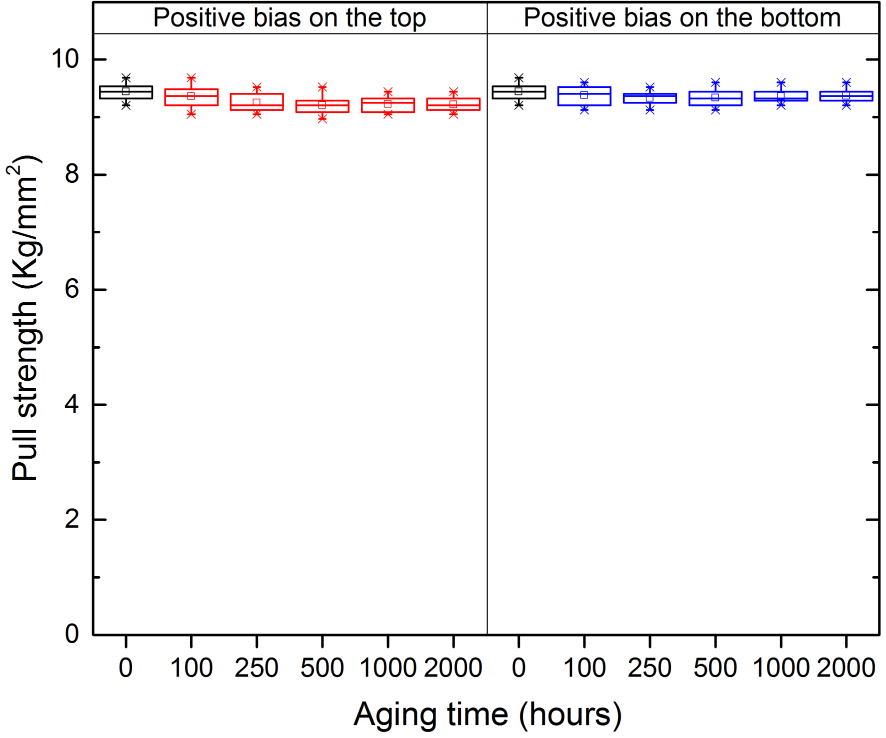

Figure 5.5: The pull strength of the Au/D1/Au patterns with 20 μm dielectric thickness. The pull strength was relatively constant at all the test intervals through 2000 hours.

The failure interface for the initial PtPdAu/D2/PtPdAu (dielectric thickness: was 30 μm) patterns was in the epoxy. With positive bias applied to the top electrode in group 5, the failure was at the interface of the dielectric and the bottom electrode at all time intervals from 100 to 2000 hours. There was a significant decrease in the pull strength at the 100 hours aging interval (Figure 5.6). For the patterns with the reverse bias in group 6, the failure interface remained in the epoxy at all the test intervals through 2000 hours and the pull strength remained high (Figure 5.6)

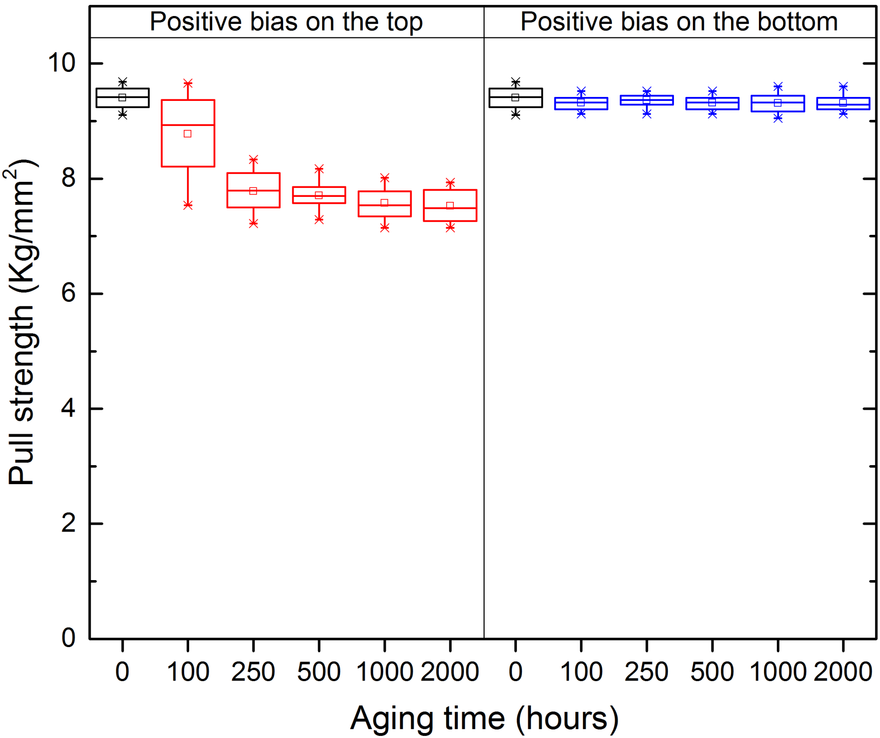

Figure 5.6: The pull strength of the PtPdAu/D2/PtPdAu pattern with 30 μm dielectric thickness. The pull strength decreased after the 100 hours aging with the positive bias applied on the top conductor. The pull test failure surface was at the interface of the bottom electrode and the dielectric layer.

The failure interface for the Au/D2/Au (dielectric thickness: 30 μm) patterns (groups 7 and 8) was in the epoxy for both polarities at each test interval. The pull strength remained relatively constant at all the test intervals through 2000 hours (Figure 5.7).

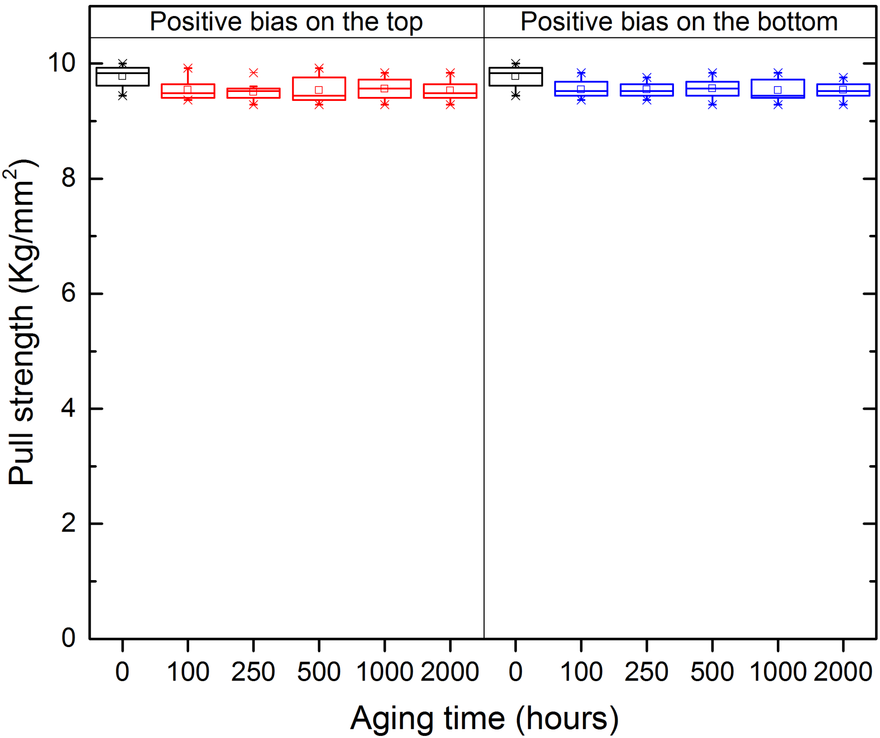

Figure 5.7: The pull strength of the Au/D2/Au patterns with 30 μm dielectric thickness. The pull strength was relatively constant at all the test intervals through 2000 hours..

Based on all the pull strength results from groups 1-8, the PtPdAu thick film paste contributed to the adhesion decreases during aging. The adhesion decreases only occurred when the positive bias was applied on the top electrode.

5.2.2 Thick dielectrics

The pull test results for groups 9-16 were plotted in figures 5.8 - 5.11. In these groups, the dielectric thickness was increased by 10 μm in the adhesion test vehicles and corresponds to the dielectric manufactures recommended thickness.

The failure interface for the initial, 100 hours, and 250 hours aged PtPdAu/D1/PtPdAu (dielectric thickness: 30 μm) patterns was in the epoxy. For the patterns in group 9 with

the positive bias applied to the top electrode and with respect to the bottom electrode, the failure interface was between the dielectric and the bottom conductor layer for the patterns aged 500 hours through 2000 hours. There was a significant decrease in the pull strength beginning at the 500 hours aging interval (Figure 5.8). With the reversed biased patterns (group 10), the failure interface remained in the epoxy at all the test intervals through 2000 hours and the pull strength remained high (Figure 5.8).

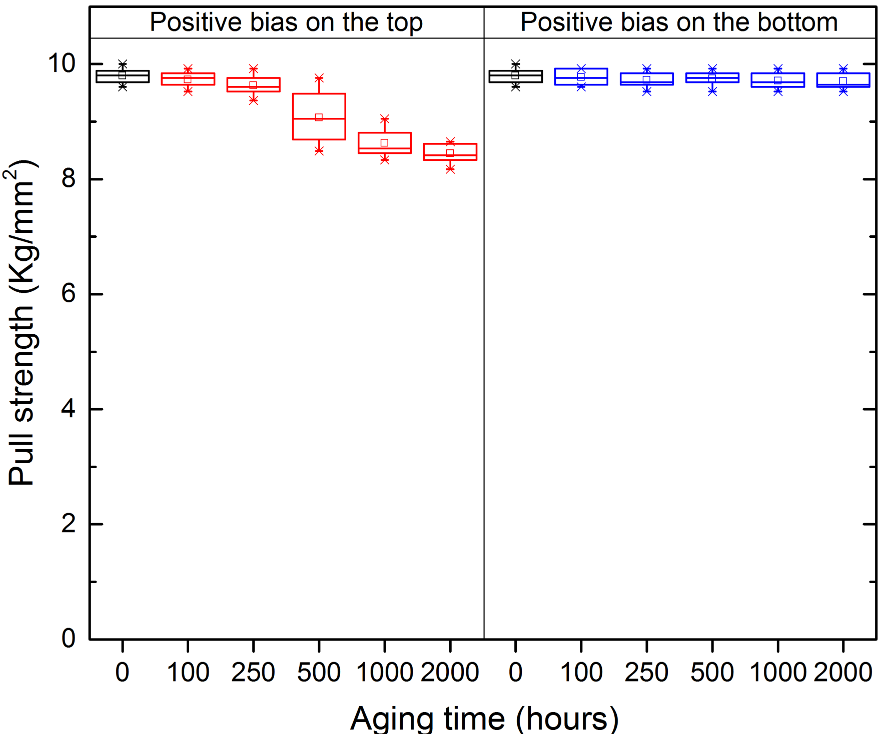

Figure 5.8: The pull strength of the PtPdAu/D1/PtPdAu patterns with 30 μm dielectric thickness. The pull strength decreased after the 500 hours aging with the positive bias applied on the top electrode. The pull test failure surface was at the interface of the bottom PtPdAu and the dielectric layer.

The failure interface for the Au/D1/Au (dielectric thickness: 30 μm) patterns (group 11 and 12) was in the epoxy for both polarities and at all the test intervals. The pull strength remained high at all the test intervals through 2000 hours (Figure 5.9).

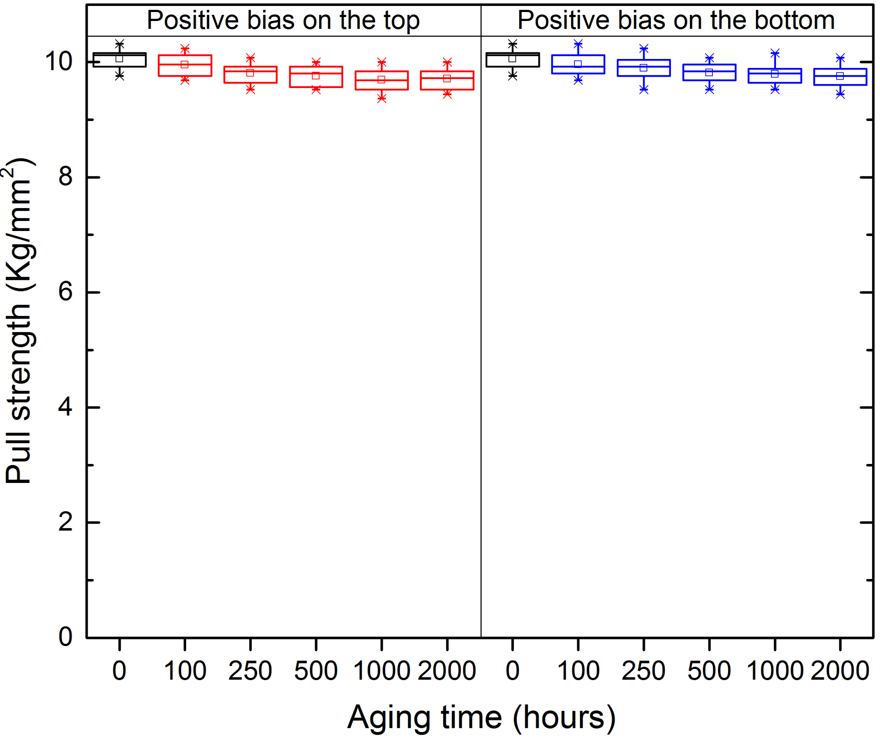

Figure 5.9: The pull strength of the Au/D1/Au patterns with 30 μm dielectric thickness. The pull strength was relatively constant at all the test intervals through 2000 hours.

The failure interface for the as-built, 100 hours, and 250 hours aged PtPdAu/D2/PtPdAu (dielectric thickness: 40 μm) patterns was in the epoxy. With the positive bias applied to the top electrode of patterns in group 13, the failure was at the interface of the dielectric and the bottom electrode at all the test intervals from 500 to 2000 hours. There was a significant decrease in the pull strength from the 500 hours aging interval (Figure 5.10). With the reversed biased patterns in group 14, the failure interface remained in the epoxy at all the test intervals through 2000 hours and the pull strength remained high (Figure 5.10).

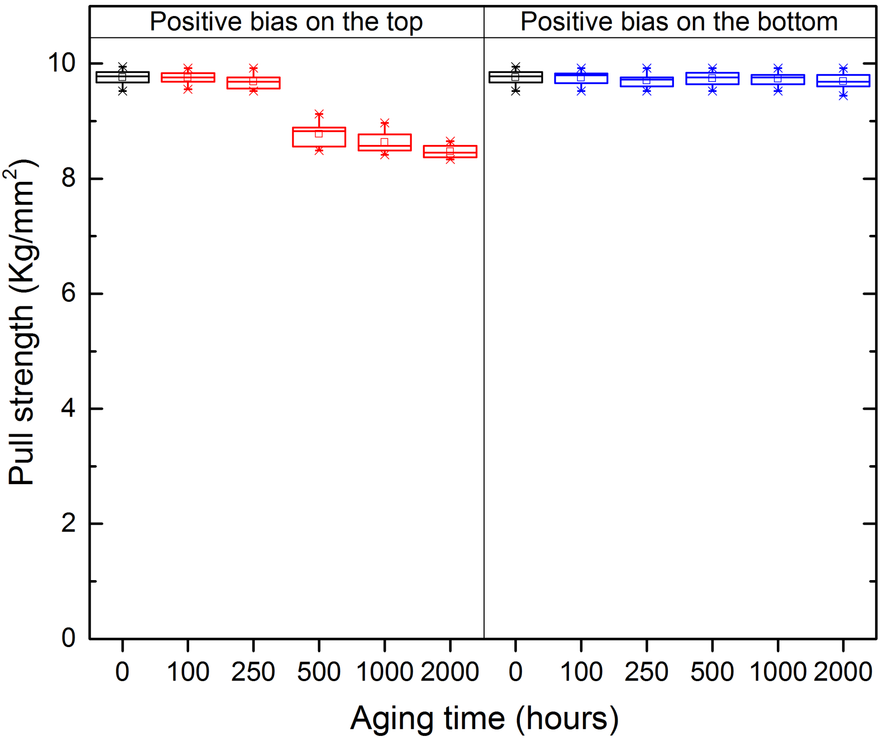

Figure 5.10: The pull strength of the PtPdAu/D2/PtPdAu patterns with 40 μm dielectric thickness. The pull strength decreased after the 500 hours aging with the positive bias applied on the top electrode. The pull test failure surface was at the interface of the bottom electrode and the dielectric layer.

With both bias polarities applied on the Au/D2/Au patterns in the groups 15 and 16, the failure interface was in the epoxy and the pull strength remained high at all the test intervals through 2000 hours (Figure 5.11).

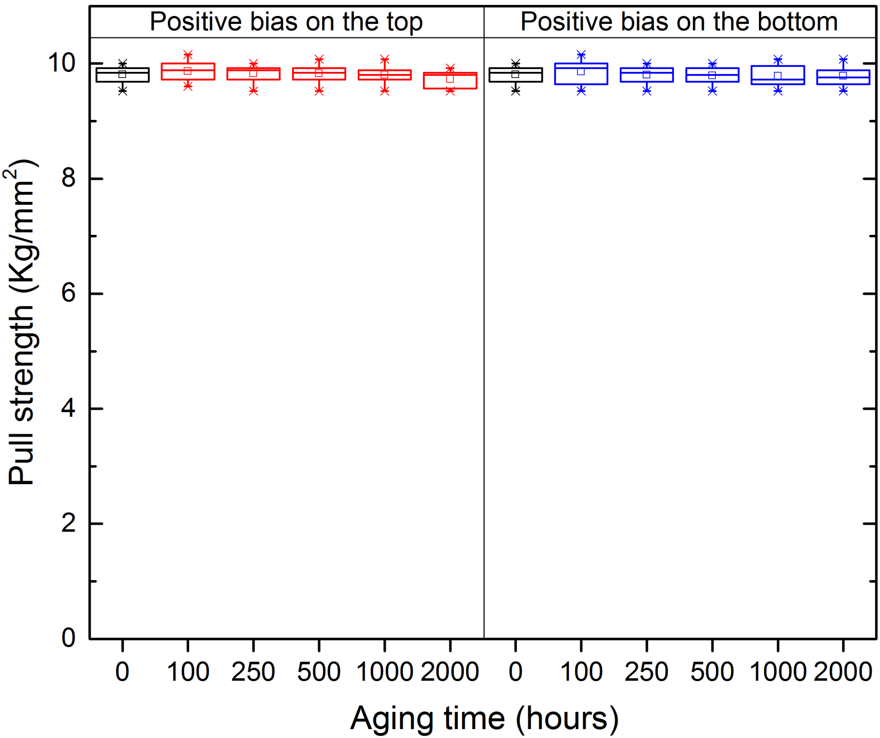

Figure 5.11: The pull strength of the Au/D2/Au patterns with 40 μm dielectric thickness. The pull strength was relatively constant at all the test intervals through 2000 hours.

Based on all the adhesion results from the groups 1-16, the PtPdAu thick film conductor exhibited a decrease in adhesion during aging when a positive bias was applied to the top electrode. Increasing the dielectric thickness extended the time period in which the pull strength remained at the initial level. The first observed adhesion decrease was delayed from the 100 hours aging to the 500 hours aging. The adhesion decrease only occurred when the positive bias applied to the top electrode.

5.2.3 PtPdAu-low Bi conductor

The manufacturer reduced the Bi concentration in the PtPdAu paste to the lowest practical level and this conductor (PtPdAu-low Bi) was used to fabricate adhesion test

vehicles. Table 5.2 lists the materials and dielectric thickness applied in the test. In these groups, the dielectric thickness was thin (D1 thickness: 20 μm, D2 thickness: was 30 μm).

Table 5.2: The test groups with materials, dielectric thicknesses (T_d), and polarities.

No.	Materials	T_d (μm)	Polarity
La1	PtPdAu-low Bi/D1/ PtPdAu-low Bi	20	Positive bias on top electrode
La2	PtPdAu-low Bi/D1/ PtPdAu-low Bi	20	Positive bias on bottom electrode
La3	PtPdAu-low Bi/D2/ PtPdAu-low Bi	30	Positive bias on top electrode
La4	PtPdAu-low Bi/D2/ PtPdAu-low Bi	30	Positive bias on bottom electrode

The pull test results for the groups La1-La4 were plotted in figures 5.12 - 5.13. The failure interface for the initial, 100 hours, and 250 hours aged PtPdAu/D1/PtPdAu (dielectric thickness: 20 μm) patterns was in the epoxy. For the patterns in group La1 with the positive bias applied to the top electrode and with respect to the bottom electrode, the failure interface was between the dielectric and the bottom conductor layer for the patterns aged 500 hours through 2000 hours. There was a significant decrease in the pull strength starting at the 500 hours aging interval (Figure 5.12). With the reversed biased patterns in the group 18, the failure interface remained in the epoxy at all the test intervals through 2000 hours and the pull strength remained high (Figure 5.12).

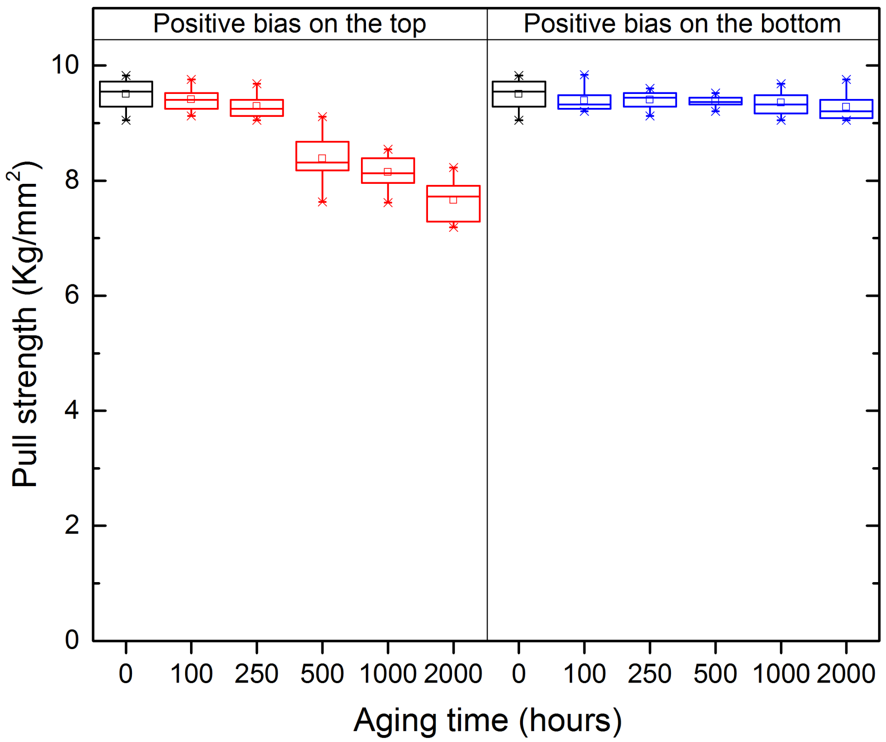

Figure 5.12: Figure 4.12 The pull strength of the PtPdAu low Bi/D1/PtPdAu low Bi pattern with 30 μm dielectric thickness. The pull strength decreased after the 500 hours aging with the positive bias applied on the top electrode. The pull test failure was at the interface of the bottom electrode and the dielectric layer.

The failure interface for the initial, 100 hours, and 250 hours aged PtPdAu/D2/PtPdAu (dielectric thickness: 30 um) patterns was in the epoxy. With the positive bias applied to the top electrode in the group 19, the failure was at the interface of the dielectric and the bottom electrode at all the test intervals from 500 to 2000 hours. There was a significant decrease in the pull strength starting at the 500 hours aging interval (Figure 5.13). With the reversed biased patterns in the group 20, the failure interface remained in the epoxy at all the test intervals through 2000 hours and the pull strength remained high (Figure 5.13).

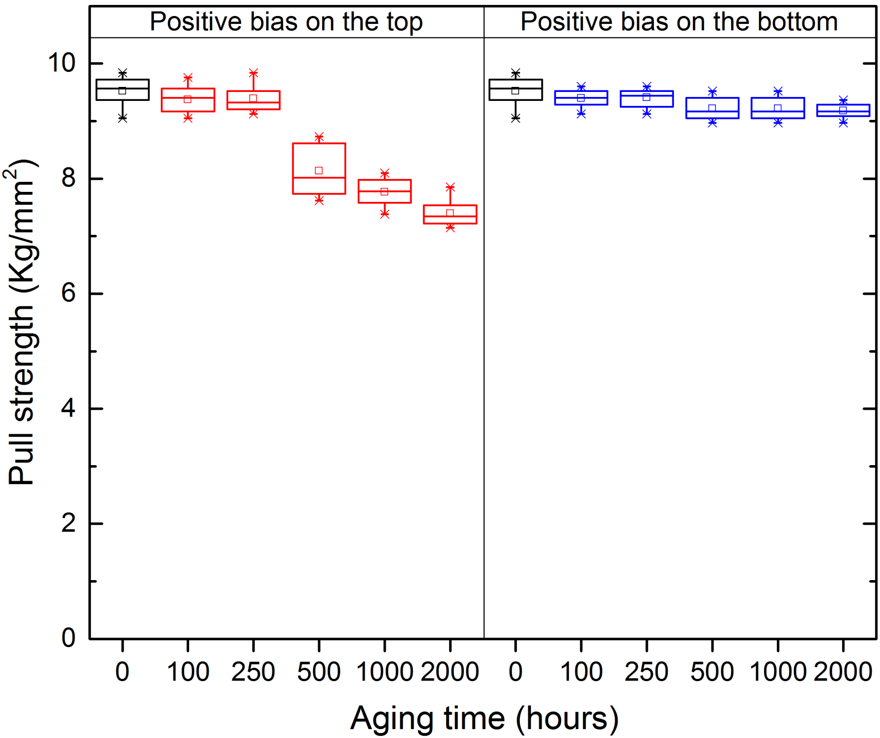

Figure 5.13: The pull strength of the PtPdAu/D2/PtPdAu pattern with 40 μm dielectric thickness. The pull strength decreased after the 500 hours aging with the positive bias applied on the top electrode. The pull test failure was at the interface of the bottom electrode and the dielectric layer.

Based on all the pull strength results, the bismuth concentration in the PtPdAu thick film paste contributed to the adhesion decrease during aging. Decreasing the bismuth concentration in the PtPdAu thick film paste delayed the first observed adhesion decrease from the 100 hours aging interval to the 500 hours aging interval. The adhesion decrease only occurred when the positive bias was applied to the top electrode.

5.3 Material analysis

5.3.1 Failure surface analysis

In the groups 1, 5, 9, 13, La1 and La3, the multilayer dielectrics lifted off from the bottom conductor layers in the pull tests. The failure surfaces of a test vehicle in group 13 were analyzed by EDS and all of the elemental concentrations were measured in weight percentage.

Figure 5.14 and table 5.3 show the results of bare fired PtPdAu thick film conductor surface. The conductor contains platinum (Pt), palladium (Pd), gold (Au). Bismuth (Bi) and oxygen (O) but no aluminum (Al), silicon (Si), nor barium (Ba).

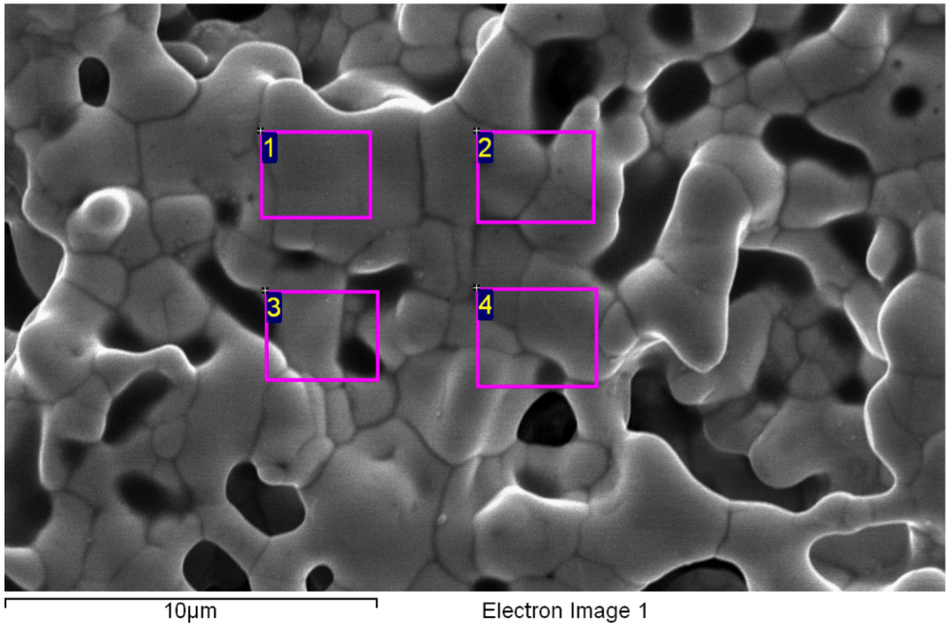

Figure 5.14: The bare PtPdAu thick film top surface as-built.

After the 2000 hours aging with a positive bias was applied to the top electrode, the dielectric-to-bottom conductor interfaces were separated during pull testing. The dielectric surface was carbon coated to increase its conductivity for SEM imaging. Both failure surfaces (on the PtPdAu conductor side and on the dielectric side) were analyzed by EDS. Results show that 2000 hours aged PtPdAu failure surface was covered with remnants of dielectric

Table 5.3: The elemental concentrations (wt%) of the bare PtPdAu top surface as-built, areas identified in figure 5.14.

Area	O	Al	Si	Pd	Ba	Pt	Au	Bi
1	4.1	0.0	0.0	6.8	0.0	8.0	74.5	5.6
2	3.9	0.0	0.0	7.0	0.0	8.6	74.3	6.2
3	5.5	0.0	0.0	7.8	0.0	7.1	72.9	6.7
4	3.7	0.0	0.0	8.1	0.0	9.0	74.9	4.3

material. Besides Au, Pt, Pd, Bi and O observed in the initial PtPdAu, we observed 1-4 wt% Al, 1-6 wt% Si, 1-8 wt% Ba on the interface surface and the O concentration increases significantly from 3-5 wt% to 17-28 wt% (Figure 5.15 and table 5.4). The Bi was observed on the dielectric failure surface with a concentration of 10-16 wt%. The Bi existed in the PtPdAu conductor and diffused into the dielectric during the firing processes in the thick film substrate fabrication (Figure 5.16 and table 5.5).

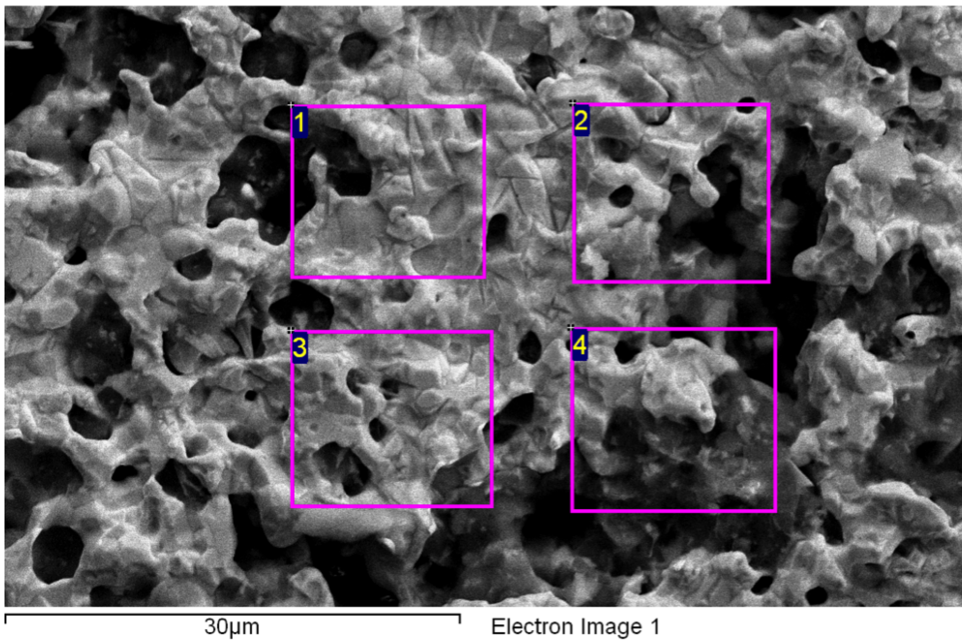

Figure 5.15: The failure surface on the PtPdAu side after the 2000 hours aging, separated during pull testing. The PtPdAu surface was covered with glass from the dielectric D2.

Table 5.4: The elemental concentrations (wt%) of the failure surface on the PtPdAu side, after the 2000 hours aging with positive bias on the top electrode, areas identified in figure 5.15.

Area	O	Al	Si	Pd	Ba	Pt	Au	Bi
1	22.4	1.2	1.5	6.5	2.2	8.1	52.0	6.2
2	21.5	1.9	2.7	4.3	4.2	6.6	54.7	4.2
3	17.2	1.7	1.0	7.0	1.2	9.0	57.4	5.5
4	27.6	3.9	5.7	3.5	7.8	3.3	0.3	7.9

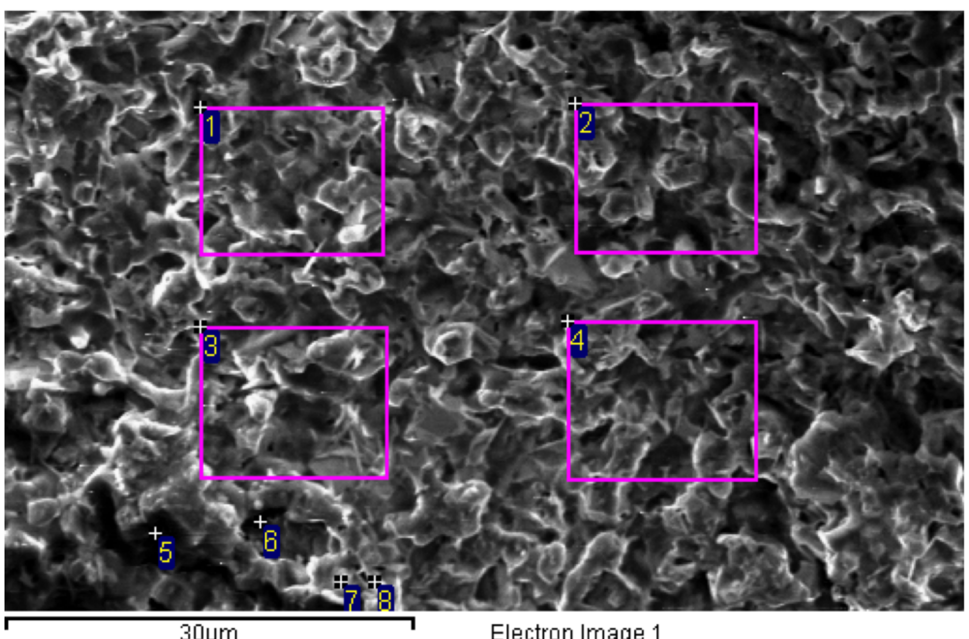

Figure 5.16: The failure surface on the dielectric D2 surface after the 2000 hours aging with positive bias on the top electrode, separated during pull testing. The Bi diffused into dielectric from PtPdAu during the firing process in manufacture.

Table 5.5: The elemental concentrations (wt%) of the failure surface on the D2 side after the 2000 hours aging, areas identified in figure 5.16.

Area	O	Al	Si	K	Ca	Ba	Bi
1	55.5	7.1	14.3	0.9	2.1	9.1	11.0
2	55.8	5.6	13.1	0.7	2.1	7.1	15.7
3	55.4	9.6	13.5	0.9	2.2	7.3	11.1
4	55.2	5.8	12.1	0.8	1.6	8.5	16.1

5.3.2 Interface analysis

In this section, the top and bottom dielectric (D2) interfaces were analyzed by EDS. Table 5.6 lists the sample information. The top electrode layers of samples 1 and 2, and the bottom conductor layers with substrates of samples 3 and 4, were polished away carefully to expose the dielectric interface. Gold was deposited on each interface to increase its electrical conductivity for SEM imaging. The minimal conductor residual on the dielectric was considered as an interface mark to stop the polishing process.

Table 5.6: The PtPdAu/D2/PtPdAu samples for SEM and EDS analysis on the top and bottom interfaces.

No.	Interface	Aging
1	Top conductor to D2	As-built
2	Top conductor to D2	2000 hours aging with positive bias on the top electrode
3	D2 to bottom conductor	As-built
4	D2 to bottom conductor	2000 hours aging with positive bias on the top electrode

Figure 5.17 and table 5.7 show the SEM image and EDS elemental concentrations at the initial interface of the top conductor and the D2 (sample 1). Beneath the conductor PtPdAu residual, the light grey areas 1-3 were amorphous glass with a higher Bi concentration (37-41 wt%). The black areas 4-6 contained only Al and O. The dark grey areas 7-9 were amorphous glass with a lower Bi concentration (5-7 wt%). Figure 5.18 and table 5.8 show SEM image and EDS elemental concentrations for the 2000 hours aged interface of the top conductor and the D2 (sample 2). The elemental concentrations remained relatively constant on the interface of top conductor and dielectric before and after aging.

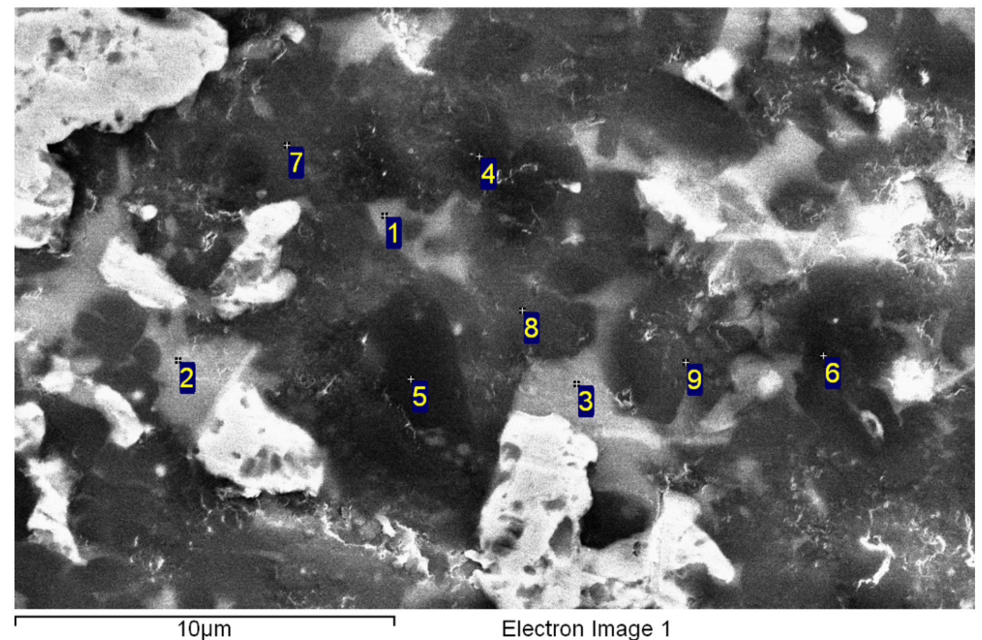

Figure 5.17: The SEM image of the initial interface of the top PtPdAu and the dielectric D2. The top conductor was polished away to expose the interface.

Table 5.7: The elemental concentrations (wt%) of the initial interface of the top PtPdAu and D2 , areas identified in figure 5.17.

Area	O	Al	Si	K	Ca	Ba	Bi
1	41.2	2.0	11.9	1.0	1.2	12.3	30.5
2	37.7	3.0	10.5	0.6	1.4	10.4	36.4
3	36.9	1.3	11.0	1.2	1.7	9.2	38.7
4	56.6	43.4	0.0	0.0	0.0	0.0	0.0
5	53.9	46.1	0.0	0.0	0.0	0.0	0.0
6	54.3	45.7	0.0	0.0	0.0	0.0	0.0
7	46.3	11.6	16.3	2.0	1.2	16.8	5.9
8	44.9	10.6	17.5	2.0	1.1	17.5	6.4
9	46.9	11.0	20.9	0.8	1.2	13.0	6.2

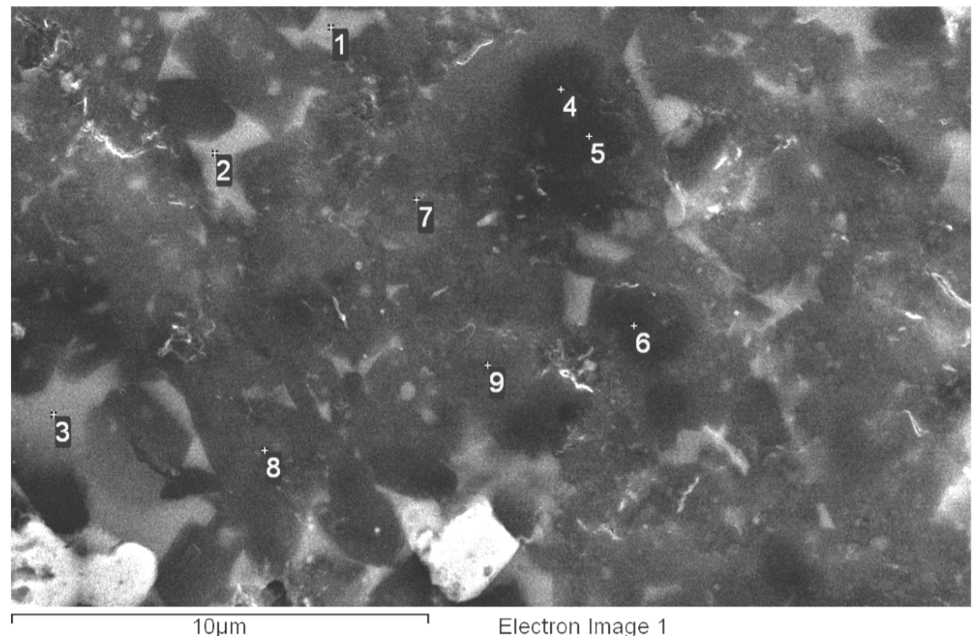

Figure 5.18: The SEM image of the 2000 hours aged interface of the PtPdAu and the dielectric D2. The top conductor was polished away to expose the interface.

Table 5.8: The elemental concentrations (wt%) of the interface of the top PtPdAu and the dielectric D2, after the 2000 hours aging, areas identified in figure 5.18.

Area	O	Al	Si	K	Ca	Ba	Bi
1	43.3	1.7	12.6	0.9	0.8	11.3	29.4
2	45.5	2.3	13.0	0.0	1.6	10.7	26.9
3	41.5	1.5	11.5	0.9	0.9	12.0	31.7
4	55.0	45.0	0.0	0.0	0.0	0.0	0.0
5	55.1	44.9	0.0	0.0	0.0	0.0	0.0
6	58.0	42.0	0.0	0.0	0.0	0.0	0.0
7	47.4	12.6	17.5	1.9	2.0	15.1	3.5
8	46.5	9.7	19.4	1.2	2.8	16.9	3.5
9	48.9	11.4	18.5	1.9	1.4	15.5	2.3

Figure 5.19 and table 5.9 show the SEM image and EDS results at the interfaces before aging (sample 3). The high Bi concentration glass (areas 1-3), and the low Bi concentration glass (areas 7-9) were observed at as-built interface of the dielectric D2 and the bottom PtPdAu, The SEM and EDS results of 2000 hours aged interface of the dielectric D2 and the

bottom PtPdAu (sample 4) show the same areas (figure 5.20 and table 5.10). All elemental concentrations at the interfaces remained relatively constant before and after aging.

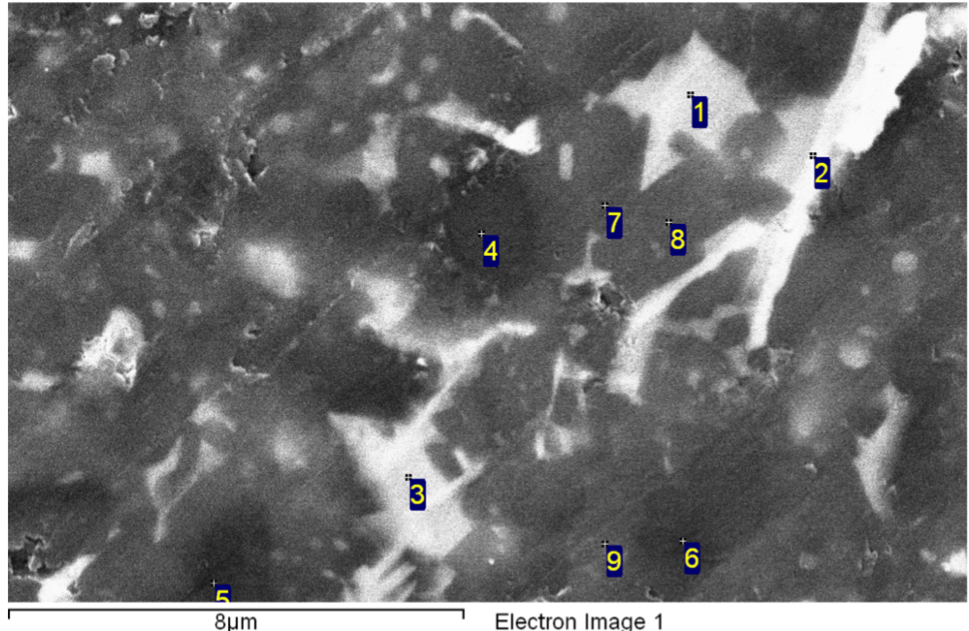

Figure 5.19: The SEM image of the as-built interface of the dielectric D2 and the bottom PtPdAu. The ceramic substrate and bottom PtPdAu were polished away to expose the interface.

Table 5.9: The elemental concentrations (wt%) of the interface of the D2 and the bottom PtPdAu as built, areas identified in figure 5.19.

Area	O	Al	Si	K	Ca	Ba	Bi
1	45.1	3.3	6.2	0.6	1.5	11.7	31.6
2	40.0	1.8	5.4	0.3	1.3	13.5	37.7
3	40.3	3.8	7.5	0.8	1.5	14.8	31.4
4	55.8	44.2	0.0	0.0	0.0	0.0	0.0
5	54.9	45.1	0.0	0.0	0.0	0.0	0.0
6	56.5	43.5	0.0	0.0	0.0	0.0	0.0
7	42.2	13.3	17.6	2.8	0.3	20.5	3.4
8	40.9	14.0	17.2	2.5	0.4	20.6	4.5
9	43.5	13.1	17.1	2.5	1.0	19.8	3.1

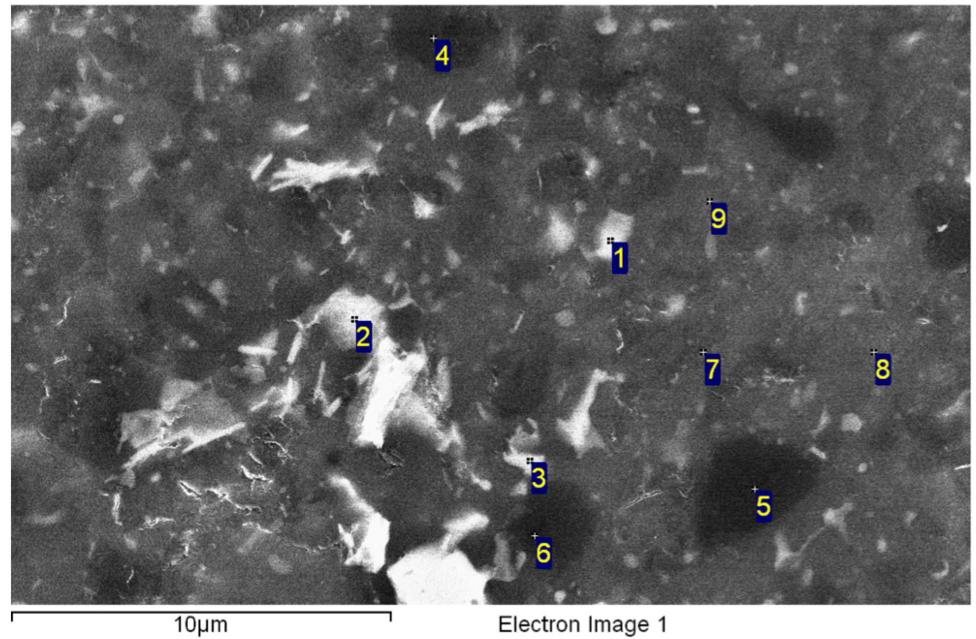

Figure 5.20: The SEM image of the 2000 hours aged interface of the dielectric D2 and the bottom PtPdAu. The ceramic substrate and bottom PtPdAu were polished away to expose the interface.

Table 5.10: The element concentrations (wt%) of the interface of the D2 and the bottom PtPdAu after 2000 hours aging, areas identified in figure 5.20.

Area	O	Al	Si	K	Ca	Ba	Bi
1	36.2	6.0	9.9	1.0	1.5	18.8	26.7
2	33.8	4.9	7.5	1.1	1.2	16.3	35.3
3	37.1	9.8	8.9	1.2	1.9	15.6	25.6
4	55.1	45.0	0.0	0.0	0.0	0.0	0.0
5	54.1	45.9	0.0	0.0	0.0	0.0	0.0
6	53.1	46.9	0.0	0.0	0.0	0.0	0.0
7	47.2	10.4	19.3	2.0	1.1	16.1	4.1
8	46.9	10.6	18.2	2.0	2.0	18.4	2.0
9	45.8	10.0	18.2	2.2	1.8	18.4	3.5

5.4 Summary

For the test vehicles fabricated with PtPdAu, the Bi in PtPdAu paste contributed to the adhesion loss from 10 Kg/mm^2 to 8 Kg/mm^2 at the interface of the dielectric and the bottom conductor. The adhesion loss of the test vehicles with high Bi concentration in thin dielectrics occurred after 100 hours aging when the positive biased voltage was applied to the top conductor. The test vehicles with thick dielectric or low Bi concentration showed adhesion loss after 500 hours aging when the positive biased voltage was applied to the top conductor. With the positive biased voltage applied to the bottom electrode, the failure surface was in the epoxy and the adhesion remained relatively constant before and after aging, regardless of the Bi concentration or dielectric thicknesses.

For the test vehicles fabricated with thick film Au, the failure surface was in the epoxy and the adhesion remained relatively constant before and after aging, regardless of the dielectric thicknesses or polarity in aging.

Future work is required to determine the mechanism responsible for the adhesion loss.

Chapter 6

Conclusion and Future Work

This dissertation reviewed high temperature electronic applications, high temperature electronic packaging, and thick film technology. Two conductive thick film pastes and two dielectric thick film pastes were evaluated with capacitor and interdigitated finger structures with 100 V bias in both polarities at 300°C for up to 2000 hours aging. The leakage current of PtPdAu capacitors with thin dielectrics (D1: 20 μm D2: 30 μm) increased significantly after a short time aging with both polarities. When positive bias on the top electrode, the value of leakage current was greater than with positive bias on the bottom electrode during aging. When the dielectric thicknesses were thick (D1: 30 μm D2: 40 μm), the leakage current remained relatively constant during 2000 hours aging. For Au capacitors, the leakage current remained relatively constant during 2000 hours aging regardless of the polarities or dielectric thicknesses (thin or thick). For interdigitated finger structure, the leakage current with all test vehicles remained relatively constant during 2000 hours aging, regardless of the thick film materials, dielectric thicknesses, and polarities.

Cross section and EDS analysis showed that during firing process, bismuth in the PtPdAu paste diffused into the multilayer dielectric layers from both top and bottom PtPdAu conductors, meeting in the dielectric center area for thin dielectrics. Electron traps in the dielectric with diffused Bi were observed by UV-vis spectroscopy. The energy of the electron traps were 3.2 - 3.5 eV.

The adhesion of multilayer thick film materials was also investigated on capacitor structures with 100 V bias in both polarities at 300°C for up to 2000 hours. For the test vehicles fabricated with the PtPdAu, the adhesion decreased and the dielectric layers lifted from the bottom electrodes in pull tests with the positive bias on the top electrode from 100

hours aging for thin dielectrics (D1: 20 μm D2: 30 μm), and from 500 hours aging for thick dielectrics (D1: 30 μm D2: 40 μm). When biased with the positive bias on the bottom electrode, adhesion remained relatively constant in pull tests and the failure surface was in the epoxy. For Au capacitors, adhesion was relatively constant during aging, regardless of the dielectric materials, thicknesses, and polarities.

The failure mechanism of adhesion loss between thick film PtPdAu and dielectrics requires further investigation.

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