Implementation of High Speed SAR ADC with Proposed Efficient DAC Architecture

By

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Abstract

A novel, high performance SAR ADC architecture is designed and fabricated in 130nm SiGe technology and 45nm soi technology. In the beginning fundamentals of ADC (Analog-to-Digital Convertor) are introduced and several types of ADC are studied, followed by concepts and details of SAR ADC (Successive Approximation ADC), which consists of sample and hold component, DAC, analog comparator, and SAR logic component. In this paper, the architectures and design details of DAC will be focused, while the design flow and details of other components will be briefly mentioned. The DAC architectures aiming at high speed switching, low power consumption, and minimized mismatch are proposed and fabricated into the whole ADC system. After that the measurements of the 1st fabrication version is presented and analyzed.

Acknowledgements

Pursuing MS degree in electrical and computer engineering department, Auburn University is one of my greatest experience. Three years ago, I learnt as a beginner, curious about everything in this field. And now I've started to do research and create new ideas in the field of analog IC design. This road is full of challenges and fabulous views.

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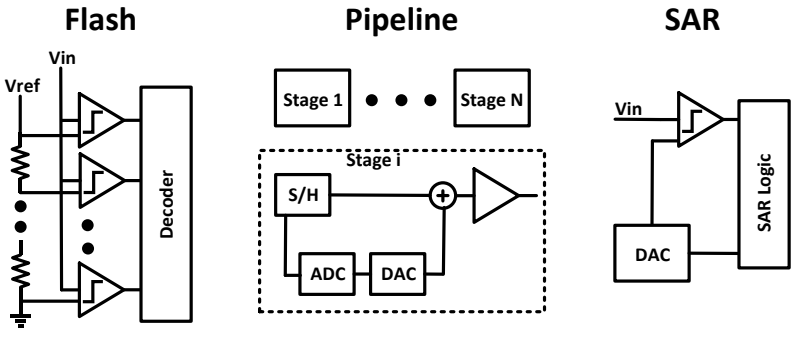
List of Abbreviations

ADC	Analog-to-Digital Convertor
SAR	Successive Approximation Register
DAC	Digital-to-Analog Convertor
S/H	Sample and Hold
LNA	Low Noise Amplifier
PLL	Phase-locked Loop
TI	Time-Interleaved

Chapter 1 Introduction

The world of wireless transceiver demands faster and more energy efficient ADC for various future application, such as 5G wireless communication standards, and industrial control system. Among all the ADC architectures, SAR ADCs are especially known for its extreme low power, and are mostly designed and utilized in low frequency and ultra-low power applications, such as medical instruments. Pipeline ADCs, on the other hand, are frequently utilized for the high frequency application [1]. Nevertheless, as the microelectronics technology develops with a magnificent speed these years, utilizing SAR ADCs and time-interleaved structure to fulfill high speed and low power requirement becomes possible. The comparison between 3 typical types of ADC is shown in the chart below.



Power	2^N	>N	1
Speed	1	<1	1/N
PW/Speed	2^N	>N	N

Figure 1.1 Comparison between Typical Structure of ADCs.

With small feature size fabrication technology, the transistor speed becomes negligible while considering the entire conversion cycle, which enable the speed of ADC accelerate magnificently. Nowadays wireless applications, such as portable device and smart data terminal, are particularly power hungry, thus requires power efficient design more than ever. Considering the speed advantage will eventually be replaced by time-interleaved structure, high resolution and low power should be the main concern in the future ADC design. This is where SAR ADC indicates its advantages. The challenge for SAR ADC design is also obvious: it's hard to achieve high resolution and high speed single core ADC. High resolution is difficult due to the acquisition noise becomes much larger in the LSB conversion steps, and acquisition noise is not likely to be reduced using typical comparator architectures. Single core high speed is also hard to achieve due to the special conversion procedure of SAR ADC, which means each cycle cannot be initialized until the cycles before it complete. These are just two basic problems remaining being resolved. Furthermore, the mismatch of capacitor array, the dissipation power, comparator decision precision and so many other problems also requires careful consideration.

In this paper, proposed architectures of SAR ADC aiming at high speed and 8 to 10 resolution performance are described. These proposed architectures have power efficient and fast switching DAC, high precision comparator, and fully accelerated logic. Among several components of ADC system, DAC, which is responsible for producing the comparator residue, is the emphasis of this paper. Several typical types and proposed high performance types of DAC will be described in detail.

This thesis is organized as follows:

Chapter 2 introduces fundamentals of several types of ADC and basic design principles; Chapter 3 will focus on the architecture of SAR ADC with examples of some typical SAR ADC models, and the design tools are also introduced at the end of this chapter; Chapter 4 indicates the proposed architectures of SAR ADC that are fabricated in 130 nm and 45 nm SOI technology; Chapter 5 indicates the measurements of the fabricated chips and analysis of these designs, after that the conclusion of thesis is addressed.

Chapter 2 Fundamentals of ADC

2.1 Introduction

Digital signal processing has become an efficient and plausible method in nowadays industrial field. For many fields, such as wireless communication, medical sensor system, and industry control, analog signal is required to be converted to digital signal for digital process. A high performance integrated data convertor plays a role to resolve these problems. In a wireless transceiver system, ADC plays an essential part to convert the intermediate frequency signal into digital code, while DAC does the opposite job. The performance of data convertor directly decides the digital processing outcome. [12]

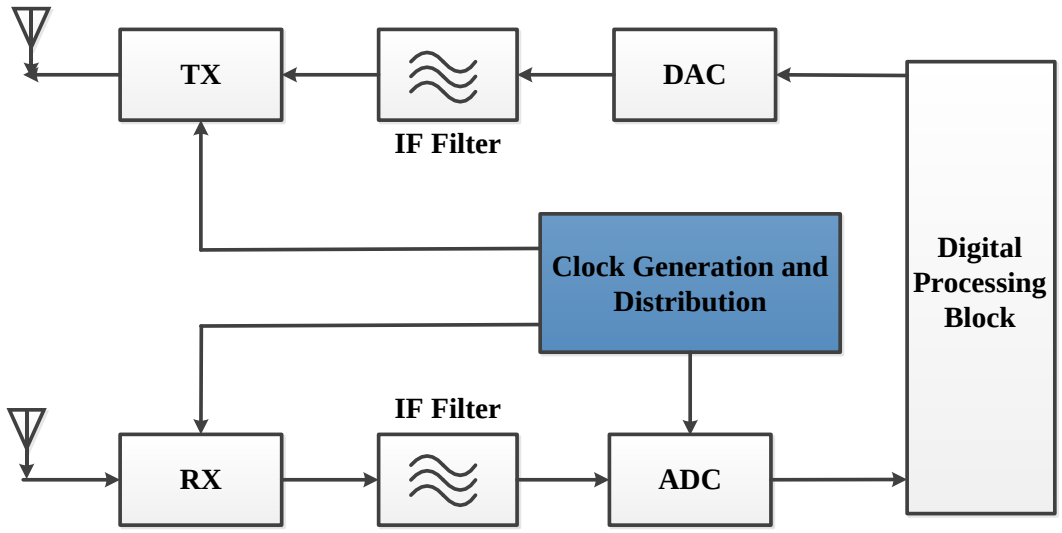


Figure 2.1 Wireless Transceiver Block Diagram.

As shown in figure 2.1, in the receiver path, after the antenna senses the input

analog signal, receiver will amplify the signal via LNA (Low Noise Amplifier), because the received signal is most likely to be very small. Then the amplified signal is down-converted using mixer, which is driven by on-chip oscillator. At last, ADC transfers the intermediate frequency signal into digital code. The entire system is clocked by the on-chip clock generation, usually played by PLL (Phase-Locked Loop). The analog part plays an indispensable role to process the received analog signal so that ADC is capable to convert it with minimized power consumption. If the analog integrated circuit is removed, ADC has to cover enormous wide band and burn extremely low power. These goals cannot be achieved using nowadays technology, so the analog integrated circuit is still of tons of values in industrial application. [2]

2.2 ADC Design Consideration

2.2.1 Sample Condition

According to Nyquist Criterion, the frequency of sampling signal has to be larger than or equal to twice the frequency of input signal so that the obtained discrete signal could be completely recovered to the input signal. Otherwise the problem that different frequency will appear in the frequency domain may occur. In most cases, this issue is called signal aliasing.

The aliasing problem could simply be understood using frequency domain. As shown in figure 2.2, when input signal is sampled into discrete signal in time domain, it actually duplicates itself at the sampling signal multiplying frequency. And this sampling frequency has to be larger than twice of the input signal band, otherwise the

signal will overlap each other. Thus the signal is distorted and cannot be easily recovered to the analog input.

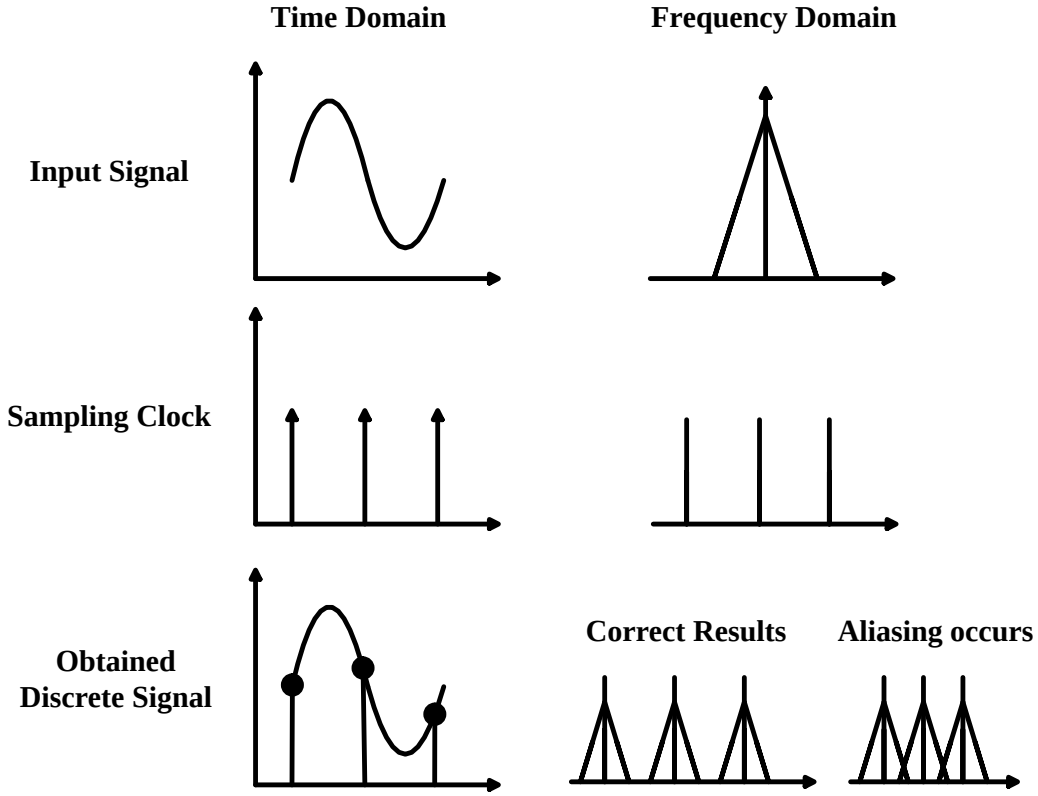


Figure 2.2 Sampling results in frequency domain in different conditions

The aliasing problem is usually avoided by using higher sampling clock, which is already decided by designer. Furthermore, it can be avoided by using a filter in the input path which only allow valid frequency signal to enter.

2.2.2 Quantization Error

Quantization error is the basic performance parameter of data convertor. Because ADC is responsible for transferring infinite analog signal to finite digital code, there has to be some errors even if the ideal ADC is utilized. The main method to measure the quantization error is to compare each quantization result with a continuous ramp

signal.

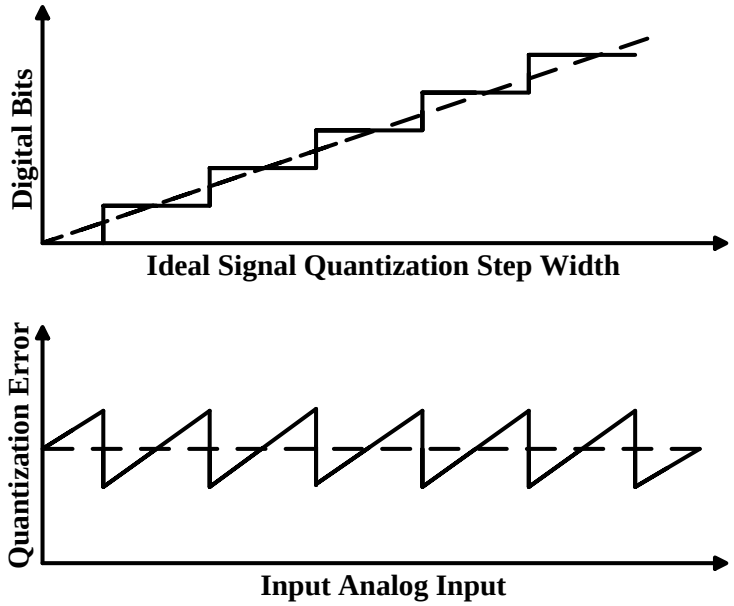


Figure 2.3 ADC Quantization Error in Ideal Condition

As shown in figure 2.3, the ideal quantization error follows uniform distribution and always shift between positive and negative half LSB. This indicates that the ADC designed requires no more than 1 LSB quantization error in measurements. This is the basic requirement of designing ADC.

2.2.3 ADC Resolution

The number of ADC digital output bits decides the ADC resolution. When input signal range is fixed, the more output bits are, the more resolution LSB could achieve. For instance, for a N-bits ADC, range of LSB is $V_{in}/2^N$. While the bits increase, the range of LSB will be smaller, thus achieves higher resolution. The sampled analog signal value could be expressed as weighted sum of all the digital bits.

$$Vout = Vref * (D_0 2^{-N} + D_1 2^{-N+1} + \cdots + D_{N-1} 2^{-1}) \quad (2.1)$$

2.3 ADC Metrics

2.3.1 DNL (Differential Non-linearity)

As illustrated in figure 2.3, for a given continuous analog input and given number of bits, the step width of each bit is fixed in the ideal case. For instance, for a 4-bits ADC and input signal equal to V_{in}, each step size is $V_{in}/2^4$ ideally. The DNL of each step is simply the difference between the ideal step size and actual output width.

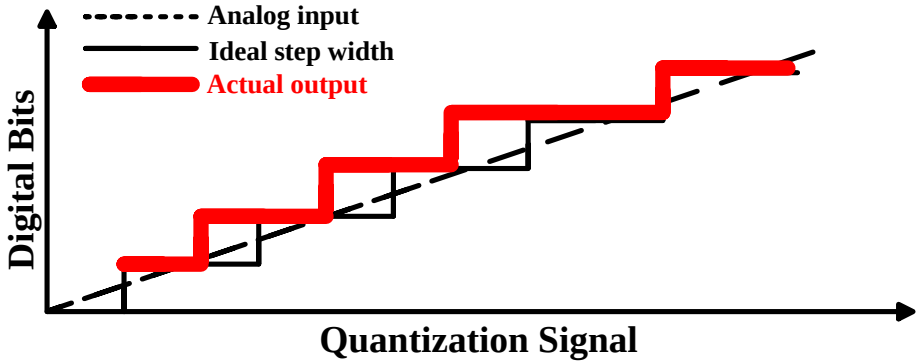


Figure 2.4 Difference between actual and ideal step size.

As shown in figure 2.4, in the first step, the actual step size is one half less than the ideal width, which leads to DNL in this step of -0.5. For the second, third, and last step, actual results equal to ideal width, so DNL in these steps equal to 0. In the fourth step, the actual result is one half longer than ideal width, so DNL in the fourth step equals to +0.5. These DNL results can be expressed in chart shown in figure 2.5.

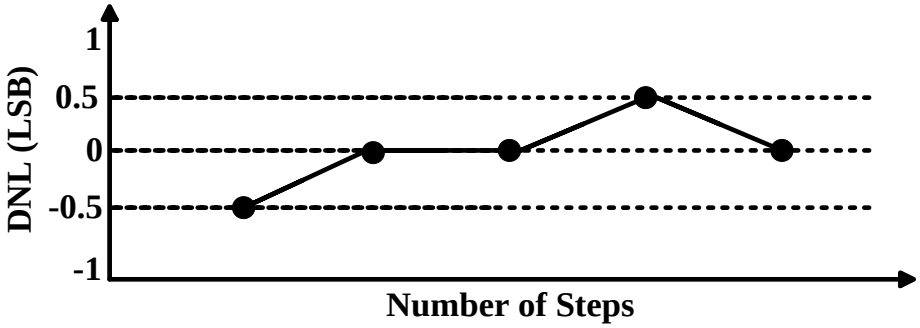


Figure 2.5 DNL chart of 5 step quantization results.

2.3.2 INL (Integral Non-linearity)

INL is defined as the cumulative sum of DNL in each step. It can be calculated as the difference between ideal transition entire value and actual transition value.

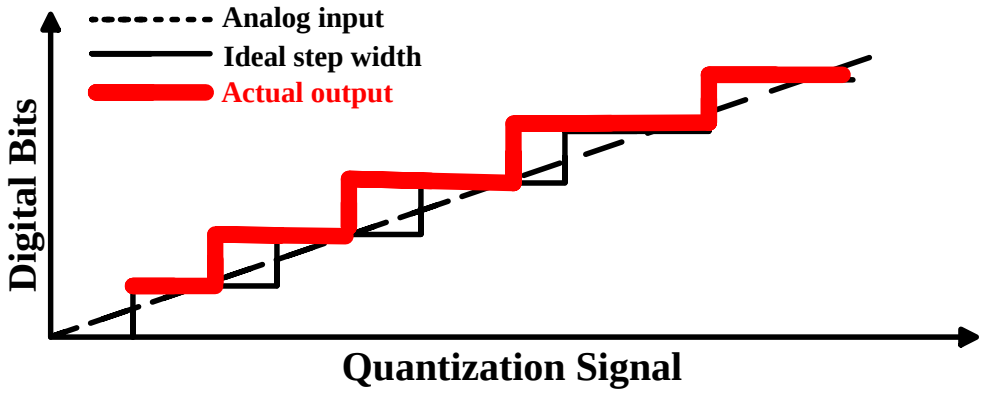


Figure 2.6 Difference between actual and ideal transition entire width.

Figure 2.6 indicates that in the first, second, and third step, the INL is -0.5 LSB. In the fourth step, there's a DNL larger than ideal step, so INL begins approaching 0. This is illustrated in the chart below.

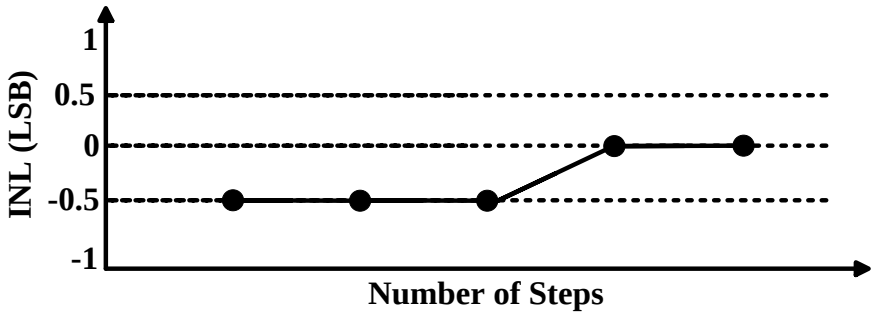


Figure 2.7 INL chart of 5 step quantization results.

2.3.3 Missing Digital Code

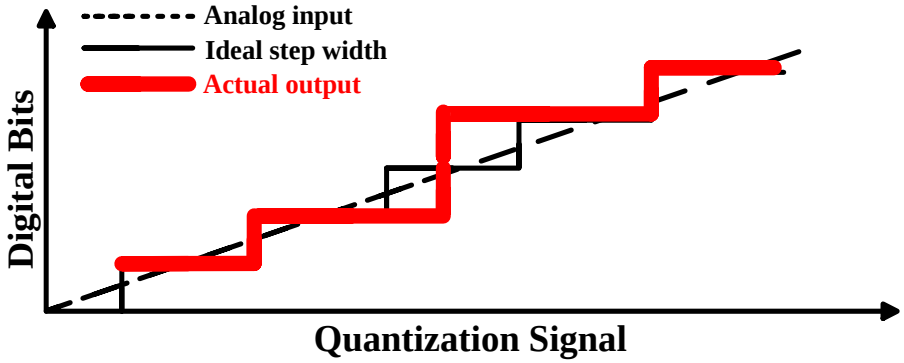


Figure 2.8 Missing digital code occurs when DNL = 1.

As shown in figure 2.8, due to the second and fourth quantization width is more than one half LSB longer than ideal step width, the third code is missed. DNL in the third step is -1. This is why in practical ADC design, measured DNL is required to be less than positive and negative one LSB. Otherwise there will be missing code in the digital outputs.

2.3.4 SNR (Signal-to-Noise Ratio)

The metrics introduced above are called static performance, since measuring these metrics is based on only DC input signal. The static performance is essential for the

transition accuracy test. Nevertheless, it cannot indicate the noise and high frequency performance of ADC. After all, ADC is supposed to transfer various analog input. Therefore, dynamic metrics are also needed for high frequency measurements.

SNR is defined as the ratio of rms (root mean square) value of input signal V_{pp} to the rms value of system noise. In the ideal case, the noise mainly consists of ideal quantization error, Therefore, the ideal ADC SNR can be calculated as follow:

$$V_{pp-input} = \frac{V_{ref}}{2\sqrt{2}} = \frac{2^N * (V_{LSB})}{2\sqrt{2}} \tag{2.2}$$

$$V_{noise} = \frac{V_{LSB}}{\sqrt{12}} \tag{2.3}$$

$$SNP = 20lg\frac{V_{pp-input}}{V_{noise}} = 6.02N + 1.76 \tag{2.4}$$

This result indicates that in the test of fabricated ADC chip, the SNR result should be close to this value.

2.3.5 SINAD (Signal-to-Noise-and-Distortion Ratio)

SINAD is a parameter covers not only system noise performance, but also all the harmonic distortion of the input signal. In a certain level, it indicates both the noise and linearity performance of ADC.

$$SINAD = 20lg\frac{V_{signal}}{V_{noise}+V_{distortion}} \tag{2.5}$$

2.3.5 ENOB (Effective Number of Bits)

In most cases, with a given ADC architecture and fixed power supply, the effective number of bits is fixed in a certain sampling clock. Due to its expression, ENOB is usually used to replace SINAD and to indicate the precision of ADC outputs. [16] It's the most direct way to judge the ADC performance.

$$ENOB = \frac{(SINAD-1.76)dB}{6.02\ dB/bit} \tag{2.6}$$

2.4 Architectures of Typical ADCs

2.4.1 Flash ADC

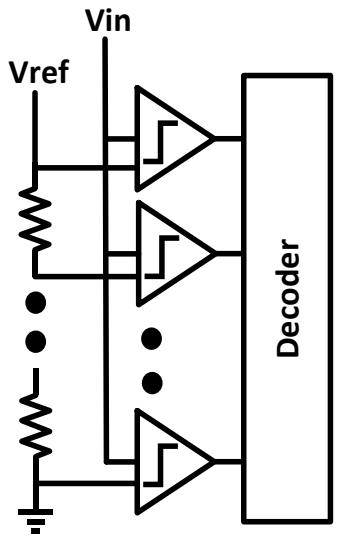


Figure 2.9 Basic architecture of flash ADC.

The most famous characteristics is ultra-fast speed. As shown in figure 2.9, it consists of reference resistive ladder, 2^{N-1} Comparators, and decoder to transfer the comparator results to digital code. For instance, if the input signal is larger than given reference, comparator will produce “1”. Otherwise comparator will produce “0”. And these results will be processed by decoder for the entire digital outputs. [14]

However, even if flash ADC has high transition speed, its main drawback is super high power consumption. Because N-bits flash ADC consists of 2^{N-1} comparators, the power is 2^{N-1} times of single comparator ADC architecture, such as SAR ADC. Due to this limitation, flash ADC usually cannot be designed to more than 5 bits. This is why flash ADC can’t satisfy many applications nowadays, such as WIFI communication, which requires at least 8 to 10 bits.

2.4.2 Pipeline ADC

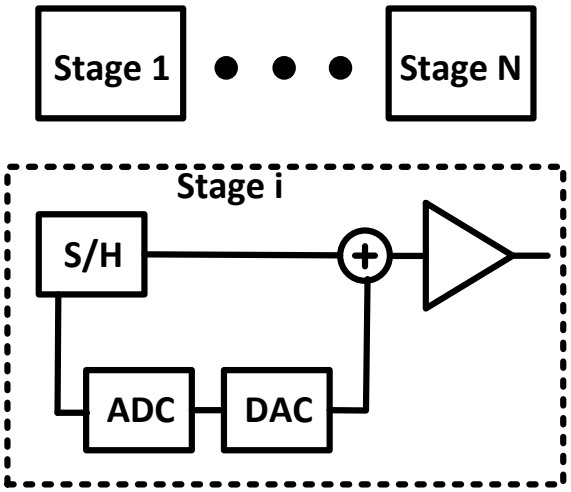


Figure 2.10 Block architecture of pipeline ADC.

A N-bits pipeline ADC consists of N conversion stages. Each stage consists of sample and hold component, comparator, and amplifier with a gain of 2. In each conversion stage, the comparator receives the input signal and determines whether the reference voltage is larger than it or not. According to comparator result, 2 different residues will be sent to the next stage. The first conversion stage takes N times clock cycle to complete, while the second to the last stage takes only 1 cycle per stage to complete. This is the reason of the name “pipeline”. Pipeline ADC is widely utilized in wireless communication system due to its high resolution and high conversion speed. The architecture of pipeline saves much more power than flash ADC so that it’s excellent to achieve high resolution goal. However, each stage requiring at least one amplifier is its main drawback, for it cost tons of power and also affects the linearity performance.

2.4.3 Sigma-Delta ADC

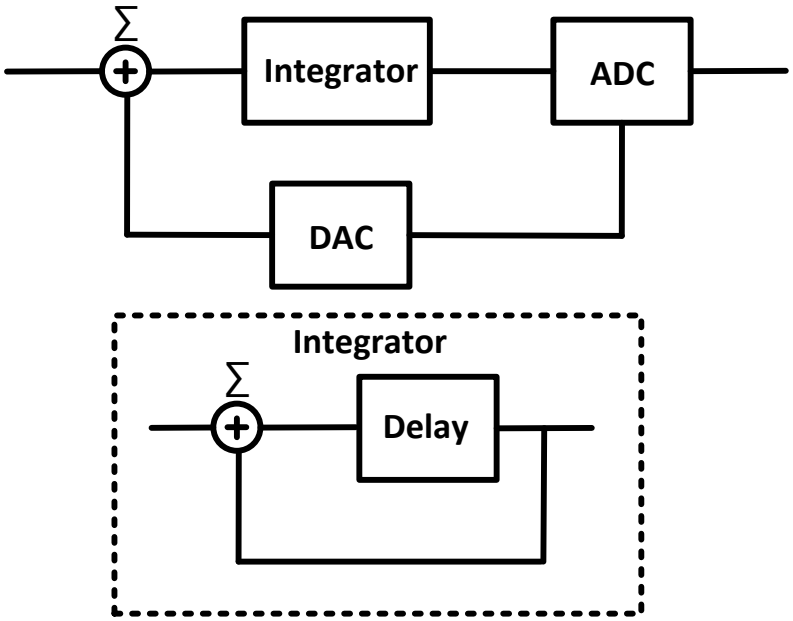


Figure 2.11 Block architecture of Sigma-Delta ADC.

As shown in figure 2.11, Sigma-Delta ADC consists of an integrator with delay and feedback loop, ADC serving as comparator, and feedback loop with a DAC to produce the comparator residue. The function of integrator is a LPF (low pass filter) to signal and a HPF (high pass filter) to noise. The increasing or decreasing trend of signal is detected by comparator, because it always gives "1" when receiving larger signal and "0" when receiving smaller signal. The noise performance is therefore improved because the noise power distribution is somehow modified. [3]

One of Sigma-Delta ADC's greatest feature is so-called "oversampling" ADC. As this paper mentioned before, ADC sampling frequency has to be larger than twice of the signal frequency. [11] However, in some practical projects, high frequency signal is required to be sampled by clock not fast enough. In usual cases, this will distort the

signal spectrum. So, this is the best opportunity for utilizing Sigma-Delta ADC.

2.4.4 Ramp ADC

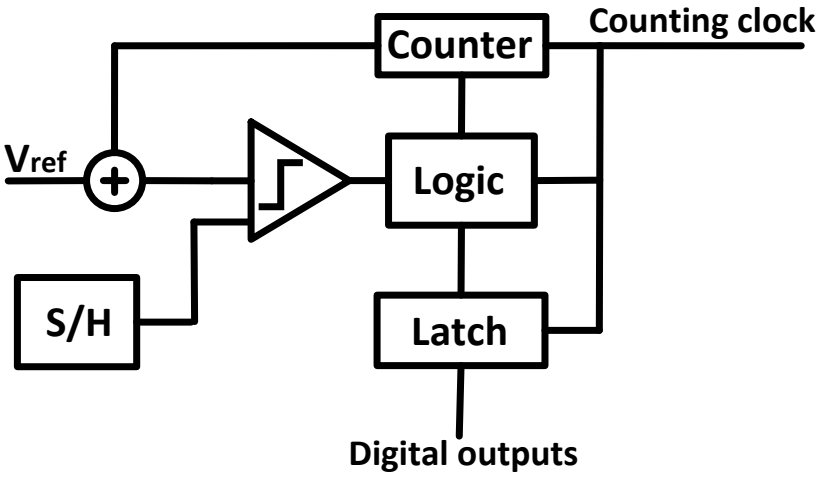


Figure 2.12 Block architecture of ramp ADC.

As shown in figure 2.12, ramp ADC consists of an integrator which produces newest residue to be compared with input, sample and hold, control logic to control the counter, latch to hold and send digital codes, and counter to count the input signal with a single slope. The counter counts each received input and send it to integrator, after that integrator will add it to reference voltage and produce a new residue. Then comparator will make comparison again. The input increase or decrease with a certain speed so that ramp ADC could transfer each analog value to digital codes.

Ramp ADC is also know as integrating ADC, for its function is to integrate the reference itself and keep counting. First of all, signal is sampled and sent to comparator. This is where the first comparison is made. After that, the reference is increased by integrator if the reference is smaller than input, and they are compared again. The reference keep increasing until it's roughly larger than input signal. Then ADC will

know the exact value of input. The increasing step of reference is decided by resolution of ramp ADC. The decision time of ramp ADC can be expressed as follow. [10]

$$T_{ramp} = RC\frac{V_{signal}}{V_{ref}} \tag{2.7}$$

According to equation 2.7, the speed of ramp ADC is related to circuit RC constant and reference voltage. First of all, signal is sampled and sent to comparator. This is where the first comparison is made. After that, the reference is increased very slowly to reach input voltage.

The main drawback of ramp ADC is input dependent conversion speed, though slowly approaching reference guarantees high resolution. A widely used updated version is dual-slope ramp ADC, which produces two references at the same time. One reference keeps decreasing while the other keeps increasing. Dual-slope architecture saves conversion speed but cost more power since integrator system is duplicated. [4]

2.4.5 SAR (Successive Approximation Register) ADC

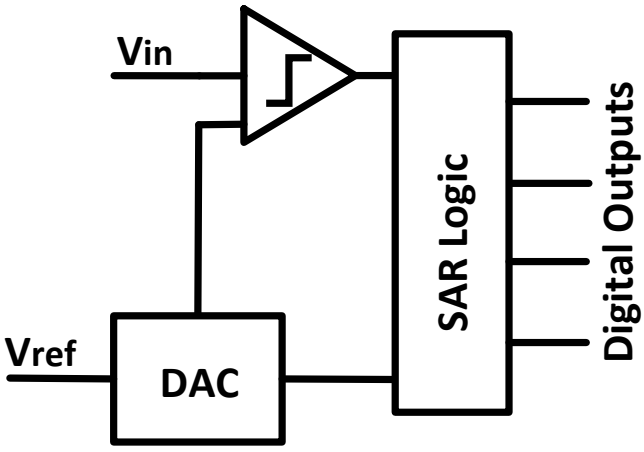


Figure 2.13 Block architecture of SAR ADC.

SAR (Successive Approximation Register) ADC consists of sample and hold component, comparator, DAC to generate reference residue, and SAR logic for DAC

controlling. As shown in figure 2.13, input signal is directly sampled to comparator, and then compared with original reference. Comparator sends “1” to SAR logic if input is larger than reference, otherwise it will send “0”. Afterwards SAR logic stores this bit as MSB, and accordingly control the DAC to produce a new residue. Then the comparator works again. The procedure will repeat from MSB to LSB. The residue produce follows binary search algorithm. First, reference covers full scale of input V_{pp}. Then reference is reduced to its half for new residue. Basically, if input is larger than reference, reference will be moved to upper half, otherwise it will be updated to the lower half.

SAR ADC’s main characteristic is low power. Because SAR ADC only contains one comparator, and doesn’t need any gain stage in most cases. In the ADC models mentioned before, amplifier is almost a must, which means extra power lost and system complexity. Amplifier design will also cost much more time because amplifier itself is a big topic. One comparator structure is another advantage of SAR ADC. In most cases, comparator power consumption is more than 80% of analog circuit power. For instance, flash ADC needs 2^{N-1} comparators, which means the power is also 2^{N-1} times of SAR ADC. Pipeline ADC has less comparator, so it can achieve high resolution. But for pipeline ADC, it still needs at least one comparator each cycle, which cost extra power and comparator design effort.

The main drawback of SAR ADC is slow speed and DAC linearity problem. Linearity is a big problem for SAR ADC design. Because SAR ADC accuracy depends on the reference residue produce, unstable reference may cause bad code in ambiguous

decision. This can be caused by DAC mismatch. There are two different kinds of DAC: resistive and capacitive. Both will suffer from resistor or capacitor mismatch especially in the LSB position. But there's many advanced schemes to overcome the non-linearity issue, which will be introduced in the following chapters. Because of slow conversion speed, SAR ADC cannot achieve high resolution as well. [15] However, as the technology develops, the speed of transistor becomes fast especially for logic circuit design. [13] Therefore, SAR ADC will become more competitive in the future communication application.

Chapter 3 SAR ADC Architectures

3.1 Introduction

Different architectures of ADC has been introduced in Chapter 2, and comparison of these architectures are addressed. This thesis will utilize SAR (Successive Approximation Register) ADC architecture for its low power, aiming at high speed conversion.

In this chapter, some published SAR architecture is introduced which will be helpful to understand the proposed architecture in chapter 4. Because the goal of proposed ADC architecture is high speed and competitive low power, this chapter will focus on high speed single core design. As the following will indicates, high speed SAR ADC (1 GS/s or larger) mostly utilized time-interleaved architecture. These proposed single core architectures are supposed to be interleaved in the future design and achieve 5G wireless standard requirements.

3.2 Classic design of SAR ADC architecture

3.2.1 Separate S/H architecture

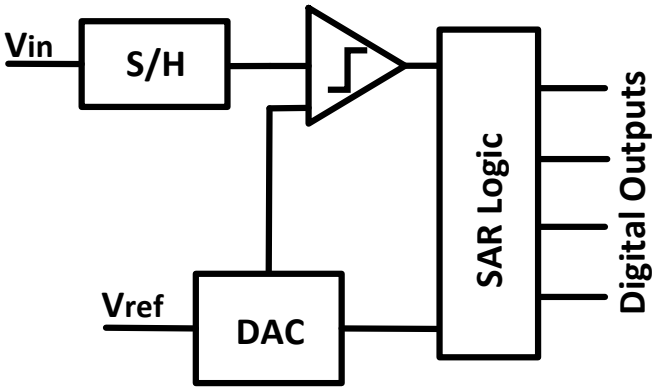


Figure 3.1 Separate S/H SAR architecture.

As shown in figure 3.1, separate S/H is utilized to sample input signal to one side of comparator, while reference generated by DAC is on the other side of comparator. After comparator make the first comparison, DAC is controlled by SAR logic and get ready for the next comparison. [17] This procedure will repeat until LSB is completed. The chart below illustrates how reference residue is changed in DAC.

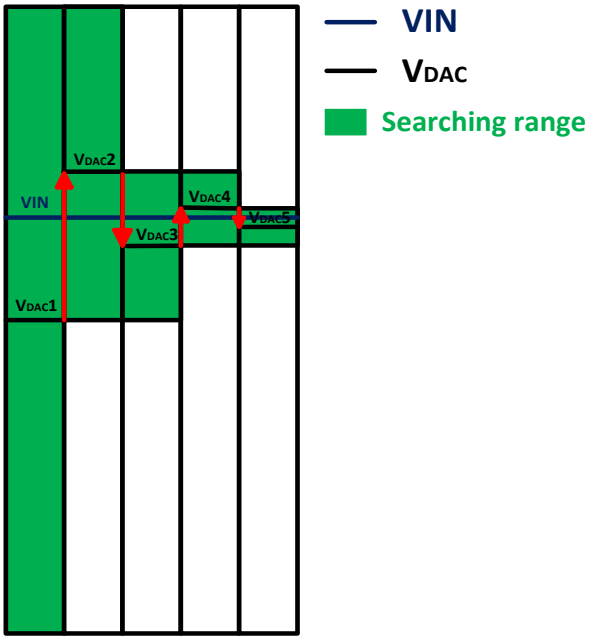


Figure 3.2 Reference residue change procedure in DAC.

Separate S/H architecture is utilized in many early designs. [5] The advantage of separate S/H architecture is DAC independent input capacitance. [6] However, the separate input capacitor costs more fabrication area, and the separate sample component costs more power.

3.2.2 DAC Connected S/H architecture

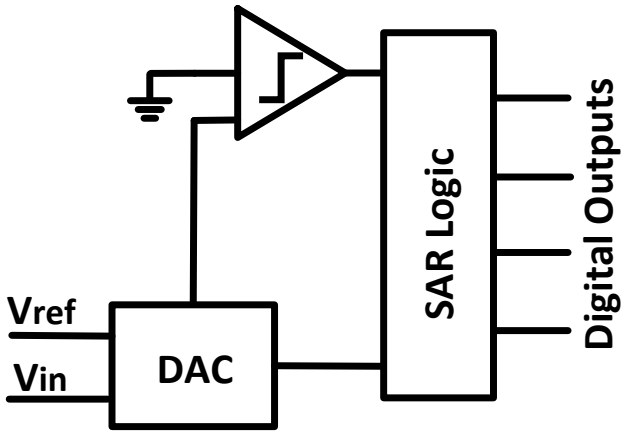


Figure 3.2 DAC connected S/H architecture.

As illustrated in figure 3.2, in this architecture sample and hold function is simply realized by a switch connected with DAC. The input signal and reference is sampled to top and bottom plate of capacitor array in DAC. First, comparator compare input signal with analog ground. Then SAR logic controls DAC to produce new residue according to comparator results. This procedure repeats until conversion of N-bits completes.

The reason that this architecture can be realized is very simple. While the comparison of separated S/H is made between V_{ref} and V_{in}, the comparison in this structure is actually made between ($V_{ref} - V_{in}$) and analog zero. The only difference is that before the comparison begins, it takes a little time for DAC to produce (V_{ref} -V_{in}) residue.

DAC connected S/H architecture is widely used in nowadays SAR ADC design. Numbers of high speed and low power models are built based on this architecture because of its structure simplicity. Because it eliminates dependent S/H and uses capacitive DAC as the ADC input capacitor, the area is significantly reduced. [18] Meanwhile, logic becomes simple and straightforward, which makes it possible to achieve high conversion speed.

3.2.3 TI (Time-Interleaved) SAR ADC

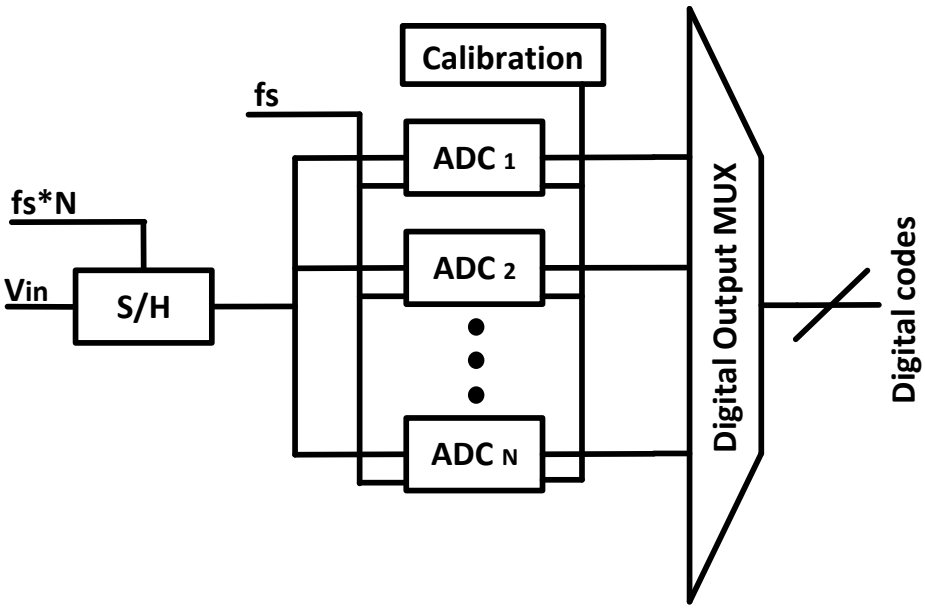


Figure 3.3 Time-interleaved ADC architecture.

TI (Time-Interleaved) SAR ADC has become popular in designs of recent years. [7] For high speed application such as WIFI, the ADC sample frequency is required to be larger than 500MSps, and resolution is supposed to be larger than 8 bits. Therefore, flash ADC is not an option because it costs too much power covering 8 bits. Pipeline is suitable for its high resolution and moderate power consumption. But the power consumption is still not competitive because pipeline is usually utilized for 10 to 20 bits

design. Also, for conversion speed faster than 1GSps or, pipeline is not suitable because it cannot reach several GSps sample frequency. Therefore, time-interleaved SAR ADC is the most suitable option for high speed and low power design.

As illustrated in figure 3.3, time-interleaved ADC consists of several single core ADC and align them with a certain time sequence. Suppose that each single core ADC operates at fs_{-1} sample frequency, and S/H circuit operates at fs_{-1}*N, after certain time of T_1, S/H receives N different voltages, and sends them to N single core ADC. Every single core ADC will process one of N signals. And digital codes will be aligned using the same sequence as ADC in the digital MUX. In many TI SAR ADC designs, digital outputs calibration and reference ADC are also utilized to calibrate the MUX outputs, thus achieves higher ENOB and SNR.

3.2 Studies of DAC design

3.2.1 Introduction to DAC design

DAC plays an essential part in SAR ADC architecture. The responsibility of DAC is to receive digital results from SAR logic, which is given by comparator, and utilize the digital code to generate a new residue so that comparator can continue working and obtain next bit.

As mentioned in the last chapter, this thesis will focus on DAC design. In Chapter 4 there will be more details about proposed DAC architecture. This chapter introduces some basic design architectures and schemes utilizing in DAC, and improvements will be shown in the next chapter.

3.2.2 Conventional DAC architecture

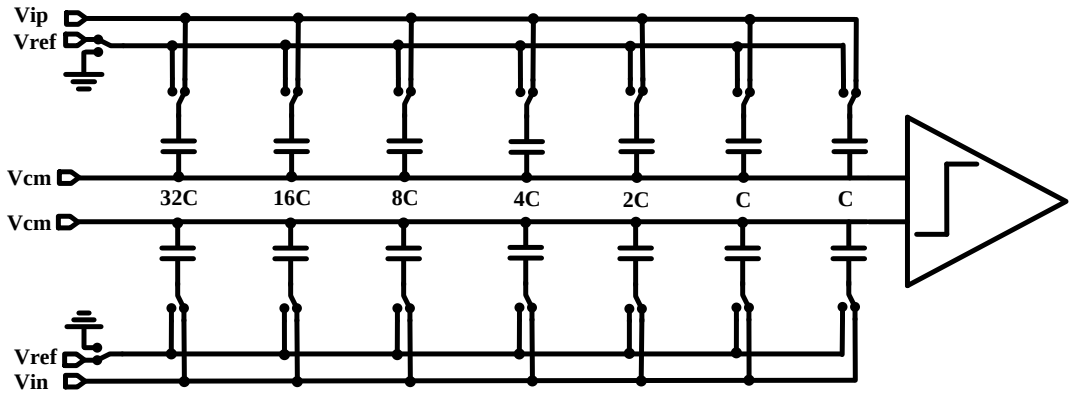


Figure 3.4 Conventional bottom plate sampling DAC architecture.

In almost every recent SAR ADC designs, capacitive DAC are utilized rather than resistive DAC, because of much lower power consumption, and small capacitor mismatch. Resistive DAC has higher power consumption because there is a constant current flow on each resistor in the resistor array, thus dramatically increases power. The architecture shown above is the most common model of capacitive DAC.

Figure 3.4 illustrates a 6-bits example of DAC, in which LSB capacitor is C and MSB capacitor is 32C. Capacitor array is distributed following binary search algorithm. At the beginning, reference voltage is sampled on the bottom plate of capacitors, and common mode voltage is sampled on top plate. After signal is sampled, bottom plates of all the capacitors are switched to input signal, thus produce $V_{residue} = V_{ref} – V_{in}$ on the top plates of capacitor array. Notice that the input signal is sampled into ADC differentially, in order to increase the full scale of input and increase LSB limitation noise, thus enable higher resolution. At two terminals of comparator, two differential input signals are compared, which is equivalent to comparing input signal with analog

ground.

3.2.3 Monotonic switch DAC architecture

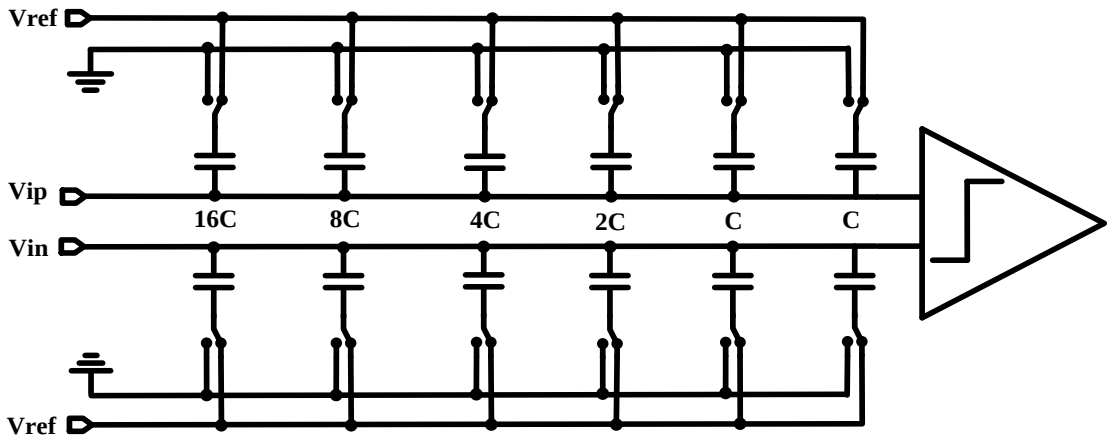


Figure 3.5 Monotonic switch DAC architecture.

Monotonic switch, also known as top plate sampling DAC model is initially proposed in design of C. C. Liu. [8] The advantage of monotonic switch DAC is straight sampling process and simple control logic. Most importantly, monotonic switch DAC eliminates the original MSB capacitor in conventional bottom sampling model mentioned before. Therefore, total capacitance of CDAC is reduced to its original half. As illustrate in figure 3.5, this model also shows an example of 6-bits DAC. However, MSB capacitor is reduced to 16C, compared to 32C in the conventional model.

Monotonic switch DAC is somewhat a milestone model because it enables SAR ADC to achieve several hundred MSps with single core model. In the early fabrication technology design, ADC entire conversion speed is mainly decided by DAC settling speed. In the designs following this architecture, many designs utilize monotonic switch scheme for high conversion speed. Proposed SAR ADC architecture in chapter 4 will

also use monotonic architecture.

3.2.4 Constant V_{cm} DAC architecture

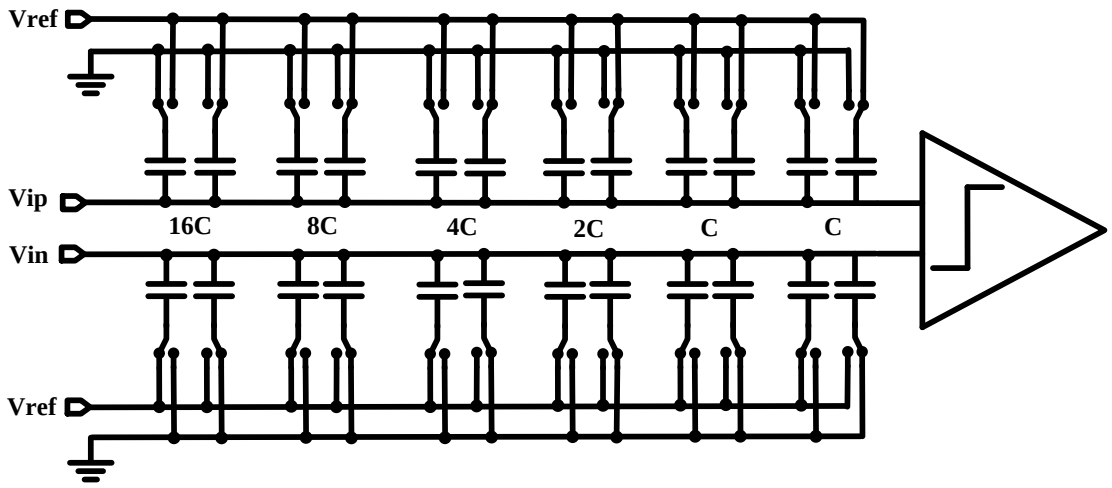


Figure 3.6 Constant V_{cm} DAC architecture.

Though monotonic switch DAC has the advantage of fast speed, it suffers from floating common mode voltage due to V_{cm} decreasing in every bit. As mentioned before, monotonic switch is basically every capacitor settling and down. This is the reason it is also named "St-and-Down" scheme. Every capacitor which is settled down will keep down during the entire conversion cycle. For instance, after 1st comparison result is sent to SAR logic, SAR logic will control MSB capacitor to settle. No matter which side of capacitor is settled, it always results in V_{cm} decreaing because there's only capacitor switch from V_{ref} to ground, but no capacitor switch oppositely. Therefore, common mode voltage will keep decreasing in this model, and results in metastability condition of comparator.

The architecture shown in figure 3.6 was initially proposed by Lucas Kull, IBM

corporation. [9] It utilize monotonic model for high speed and improve it to be constant common mode, thus maximize the comparator decision speed. As will be mentioned afterwards, decision speed of comparator architecture based on NMOS differential pair mostly relies on V_{GS} of NMOS differential pair, which is determined by V_{cm} in the architecture above. Therefore, original monotonic model is modified and achieve constant common mode with a cost of double capacitor array.

The algorithm of achieving constant common mode is shown using following expressions. This is an example of 3-bits ADC operation. Suppose that the input signal is already sampled onto capacitor array, the equations below indicate how V_{cm} is changed after first switch.

$$(V_{ip} - V_{ref}) \cdot 16C = (V_{cm+} - V_{ref}) \cdot 12C + V_{cm} \cdot 4C \tag{3.1}$$

$$V_{in} \cdot 16C = V_{cm-} \cdot 12C + (V_{cm-} - V_{ref}) \cdot 4C \tag{3.2}$$

Then the results of differentially V_{cm} is obtained as follow:

$$V_{cm+} = V_{ip} - \frac{V_{ref}}{4} \tag{3.3}$$

$$V_{cm-} = V_{in} + \frac{V_{ref}}{4} \tag{3.4}$$

Then the comparator result will be given in the following equation, which satisfies binary search algorithm.

$$V_{cm+} - V_{cm-} = V_{ip} - V_{in} - \frac{V_{ref}}{2} \tag{3.5}$$

And it's quite obvious that constant common mode is obtained, indicated by the following equation

$$V_{cm+} + V_{cm-} = V_{ip} + V_{in} \tag{3.5}$$

Unlike the architecture of original monotonic model, the negative part is eliminated, so V_{cm} will not be reduced as conversion is in progress.

However, this improvement suffers from a double capacitor array, which may produce more mismatch issue. Also, double capacitor array costs double fabrication area, but it's not a main concern since the fabrication area for SAR ADC is already sufficient in most cases nowadays.

3.2.5 Split-array DAC architecture

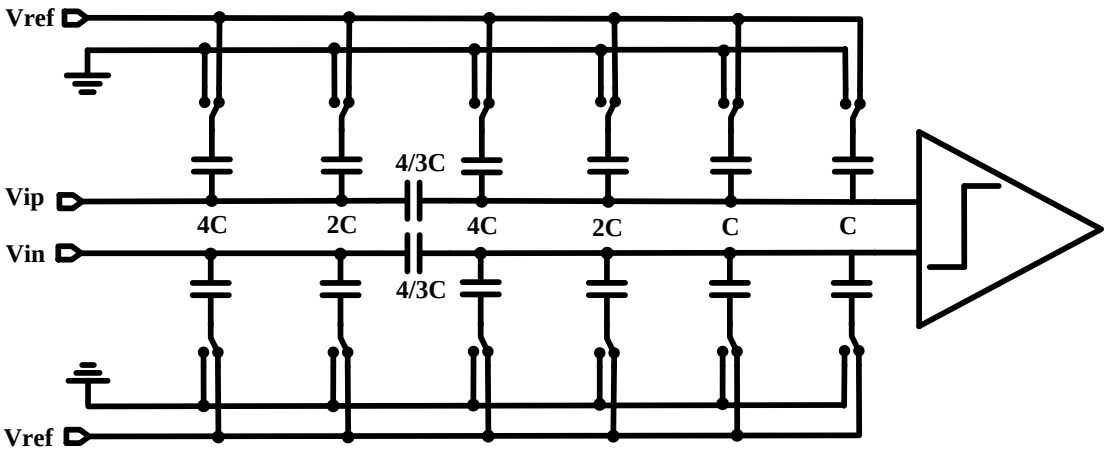


Figure 3.7 Split-array DAC architecture.

Split-array DAC is widely used in high speed SAR ADC design because of the significantly reduced capacitance. Figure 3.7 shows an example of 6-bits DAC utilizing monotonic switch scheme. Compared to the models described before, MSB capacitor is only 4C, 8 times smaller than conventional DAC architecture, and 4 times smaller than Set-and-Down architecture. This architecture dramatically reduces the capacitance to accelerate DAC settling speed. Around 5 years ago, almost every design aiming at more than 100GSps speed utilized this architecture.

As shown in figure 3.7, the secret weapon of split-array DAC is a series capacitor between MSB capacitors and LSB capacitors. Normally the series capacitor is placed in a middle place to balance MSB and LSB array and minimize the ratio between largest and unit capacitor. In the instance shown above, the equivalent output capacitance of MSB capacitor is C, and it allows the total capacitor array switches following binary search algorithm.

Disadvantage of split-array is obvious: the mismatch of capacitor array is usually out of control. This may result in low ENOB and hurts noise spectrum performance. In another word, there's always trade-off in analog circuit design. In most cases, high speed motivation will hurt power and precision performance. Designers must always keep these trade-offs in their mind.

3.2.6 Switch back DAC architecture

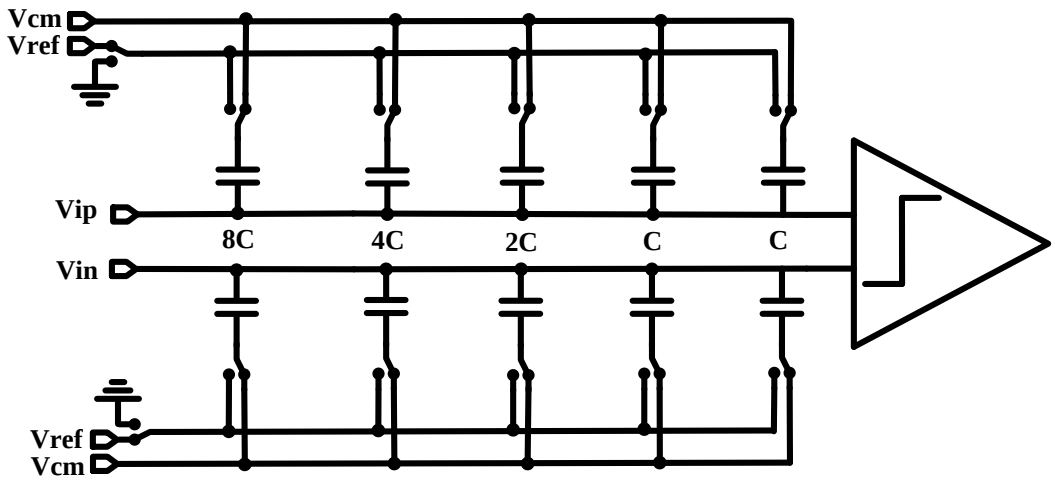


Figure 3.8 Switch back DAC architecture.

Switch back DAC architecture shown in figure 3.8 also utilizes Set-and-Down

switch to maximize settle speed and minimize capacitor mismatch. Compared with convention structure mentioned before, which contains a 32C as MSB capacitor, switch back DAC architecture only requires 8C as MSB capacitor for a 6-bits ADC. Compared with conventional Set-and-Down architecture, the MSB capacitor is further decreased and total capacitance becomes only half of the original one.

Switch back DAC utilizes a special scheme to control the switching of capacitor array. At the very beginning, input signal is sampled to the top plate of capacitor array differentially, operating the same as conventional monotonic switch. Then comparator directly compare the 2 inputs and send out first bit. While SAR logic receives the control signal, it controls the entire capacitor array on one differential side to switch from V_{ref} to ground, rather than only switching the MSB capacitor. Afterwards the capacitor is switched from ground to V_{ref} one by one in each bit cycle. Which side of capacitor is to be switched is decided by comparator results. This is the reason this scheme is called “Switch back”.

As explained in the last paragraph, the entire capacitor array on one differential side is switched to replace the function of only switching the first capacitor. Notice that if MSB capacitor is 8C, then it’s obvious that total capacitance is 16C, which equals to the largest capacitor in conventional monotonic architecture. Therefore, the largest capacitor is replaced by switching the entire capacitor array. Furthermore, to maintain the binary search of the bits afterwards, all the capacitors are switched on by one in a opposite direction. Then the complete job of DAC is fulfilled.

The switching process of a 3-bits conversion example is illustrated below:

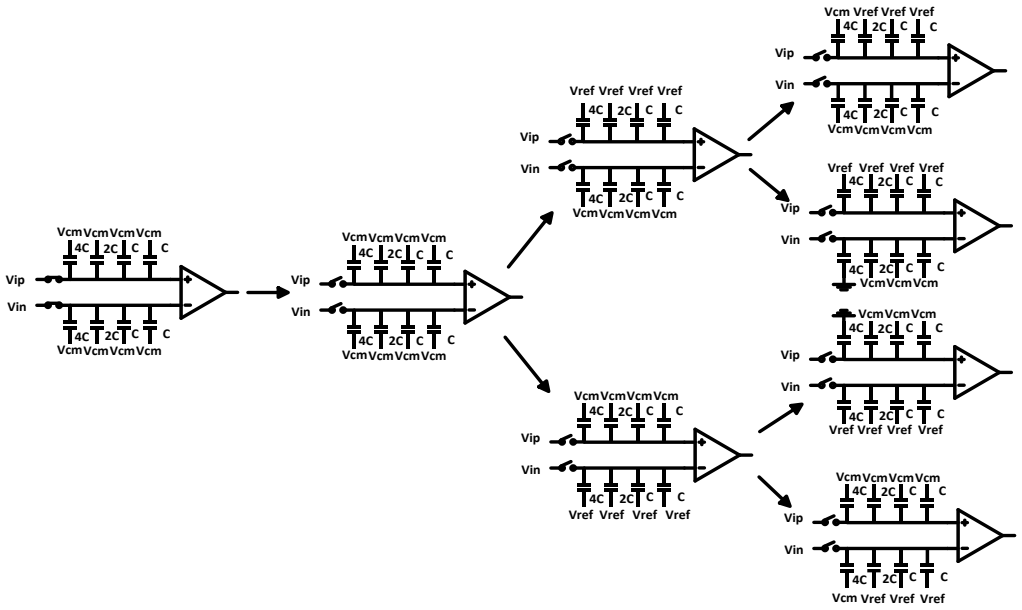


Figure 3.9 Switching process of switch back scheme in a 3-bits example.

3.2.7 Studies of redundancy

Redundancy is a technique that almost every SAR ADC designer utilizes in recent years. It significantly boosts the DAC conversion speed and succeed in avoiding some comparison error caused by limitation of comparator thermal noise. The cost of utilizing redundancy is covering one or two more bits in the original design. For instance, 11 or 12 bits are required for a 10 bits SAR ADC design which utilizes redundancy technique. This is where the name “redundancy” comes from. Instead of more bits to be fulfilled, the entire conversion speed is still far more boosted. This is because redundancy enables DAC to get rid of some useless settling time to boost the whole speed of system.

Before introduction to redundancy theory, it’s important to know why redundancy is needed in almost every DAC design.

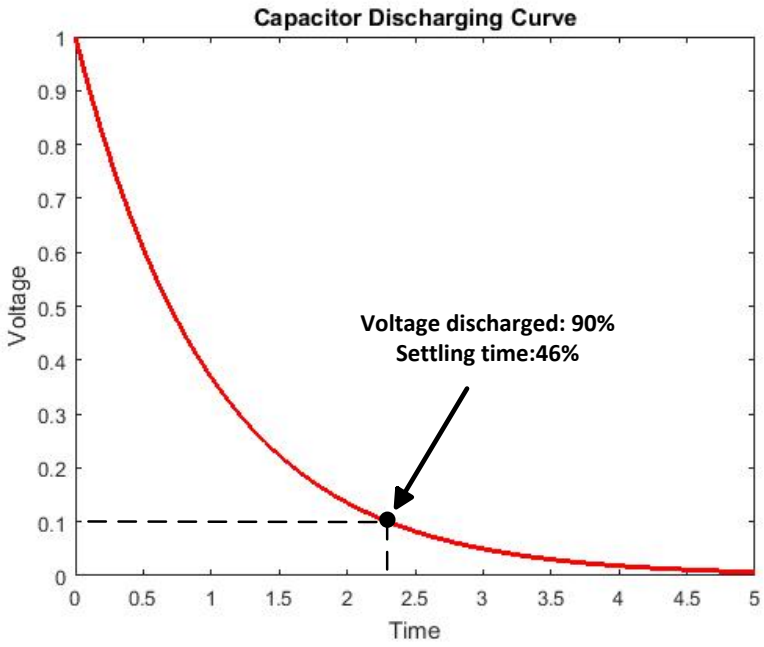


Figure 3.10 Capacitor discharging curve. (Voltage vs. Time)

Capacitor settling speed is proportional to RC constant of DAC and controlling switch. The voltage discharging speed can be expressed as follow:

$$V(t) = V_0 \cdot (e^{-\frac{t}{\tau}}) \tag{3.6}$$

Figure 3.10 indicates that as capacitor discharge voltage, the discharging speed is fast at the beginning, and becomes slower gradually afterwards. After a certain point, discharging speed becomes so slow that even a small amount of voltage takes long time to settle. As shown in figure 3.10, which is simulate using MATLAB, where logic and switch delay are ignored, 90% of voltage only takes 50% of settling time to settle. But the last 10% of voltage takes another 50% of time. The last part of voltage is very small part, but takes long time, which seems not worthful in a practical design. Then the question is: what if the last 10% of voltage is ignorable? Obviously, it will save a lot of time. Theoretically, it can even double the entire DAC settling speed. However, it leaves

a problem to be resolved: it can cause output errors if this part of voltage is eliminated. The elimination of the last small amount of voltage, which can be also called “partial settling”, will cause error if the voltage after settling is very close to input voltage. In this case, signal that is sent to comparator may be misleading and produce wrong code.

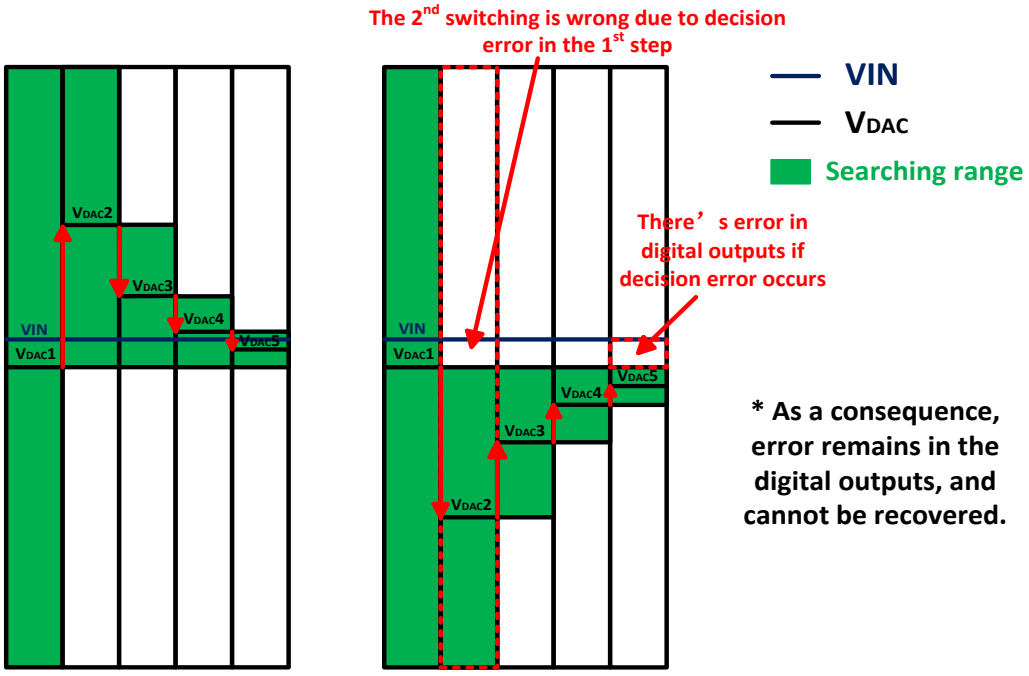


Figure 3.11 Decision error caused by partial settling.

As indicated in figure 3.11, in the first switch, input signal is very close to DAC residue. DAC is supposed to be switched to upper half in the following step, but it’s switched to the opposite side due to wrong control signal. The error will lead the entire searching range to the lower half, while input signal is not in that range. This will result in 1 LSB missing in the final outputs.

Redundancy technique is proposed to resolve the partial settling error problem. When DAC residue get too close to input value, and error occurs due to comparator

noise, redundancy is able to recover the error and change the wrong codes to correct ones. The figure below shows how redundancy works in a corresponding situation the same as figure showing above.

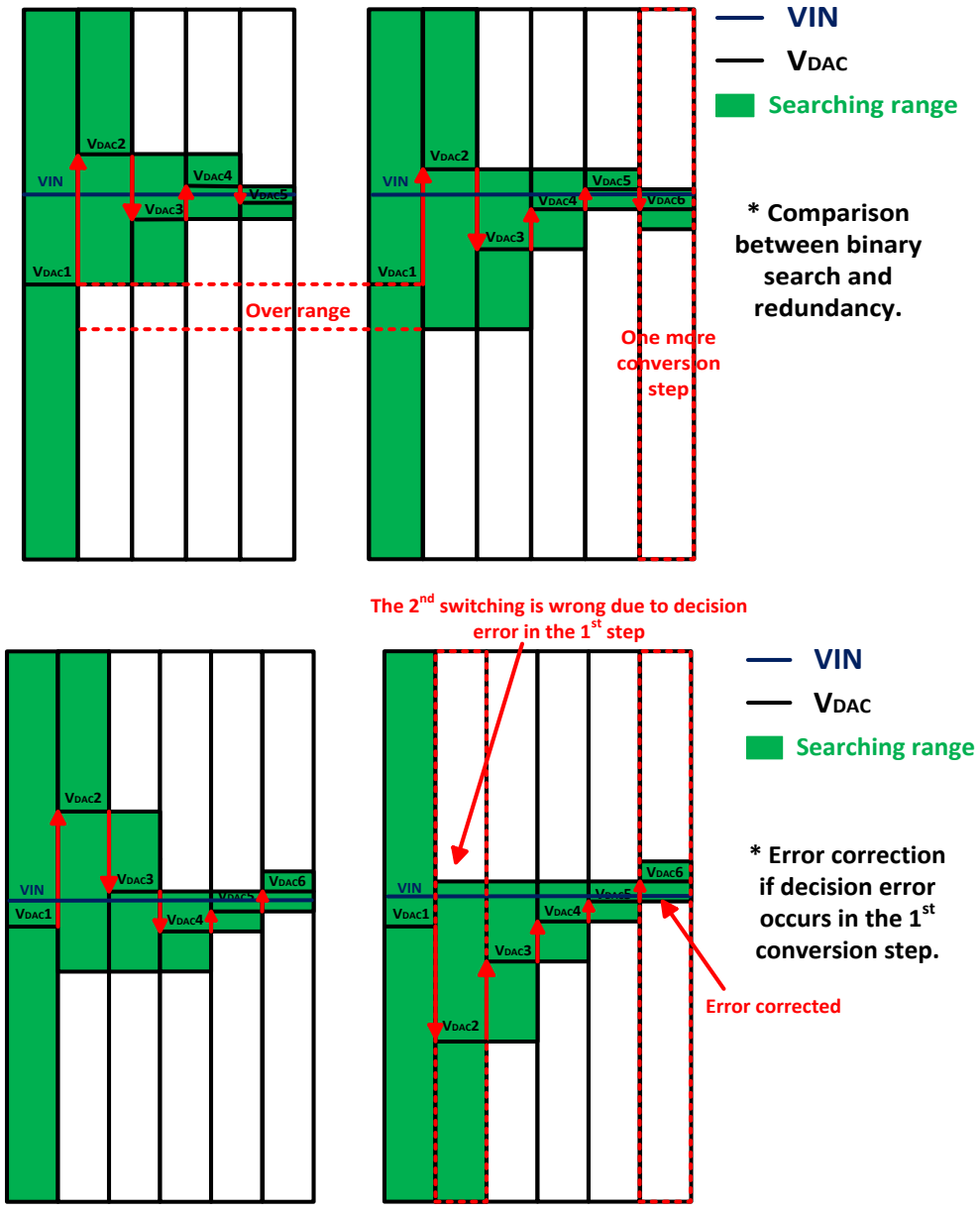


Figure 3.12 Redundancy working process.

As shown in the figure 3.12, to implement redundancy, there has to be at least one more bit. Even an extra bit is added, ADC resolution remains the same, which means

the LSB step is still not changed. What changes in the capacitor array is usually the 2nd capacitor and the capacitor before LSB. The 2nd capacitor becomes smaller so the switching step in 2nd step is smaller, thus provides a certain over range. The over range is the key to recover the wrong codes to correct ones. The figure has shown it quite clearly that after several steps of switching, the DAC residue get close to input signal again, rather than get the input voltage entirely out of searching range.

In the 2 cases shown above, the digital outputs may be different, but the analog value stays the same. Measurement stuffs simply need to add all the codes and their weights together to obtain the right analog value.

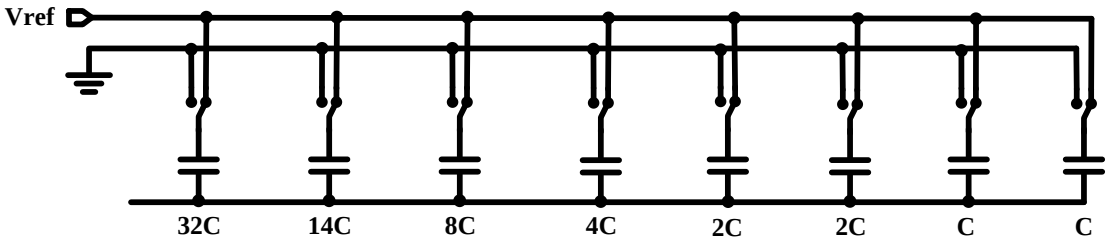


Figure 3.13 Capacitor array implemented with redundancy.

To implement the redundancy technique in capacitive DAC, the second capacitor and the capacitor before LSB is usually modified to produce over range. Generally, for an N-bits ADC implemented with redundancy which requires M steps to complete conversion (M >N), the redundancy follows the equation shown below.

$$2^M - 2^N = \sum_{i=1}^{M-1} 2^i \cdot q_i \tag{3.7}$$

Where q_i refers to the over range in the i-th step.

Chapter 4 Implementation of Proposed Architectures of SAR ADC

4.1 Introduction

Based on the fundamental architectures and advanced schemes described in Chapter 3, two proposed SAR ADC architectures are introduced in this chapter. The description will also focus on the system structure and DAC design and implementation, while other parts such as sample and hold, comparator, and SAR logic are briefly described.

These two proposed SAR ADCs are already fabricated in 130nm and 45nm SOI technology, and 130nm chip has been measured and will be listed in the next chapter. The chip layout and fabricate details such as pin map, decouple capacitor distribution will also be described in the last part of the chapter.

4.2 Proposed SAR ADC architecture

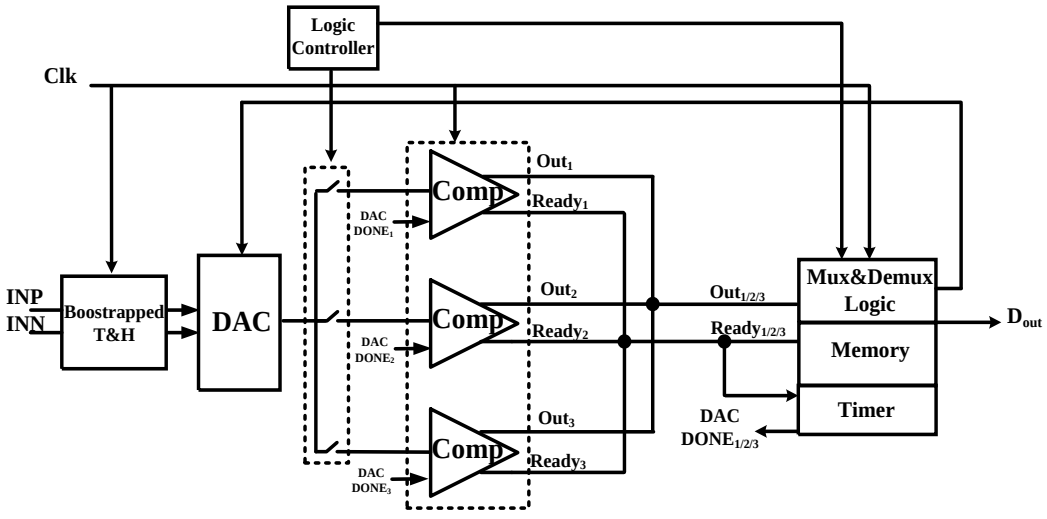


Figure 4.1 Proposed SAR ADC architecture with 3-way interleaved comparator.

The proposed SAR ADC architecture is designed aiming at 8-bits, 150MSps sample frequency, and 4 mW power consumption. Despite utilizing 130nm technology, comparatively slower than the advanced technology, the speed boost technique still achieves high speed performance.

Figure 4.1 shows the entire structure of proposed SAR ADC, which consists of a bootstrapped sample and hold, three-way interleaved comparator, fully self-controlled SAR logic, and high-performance DAC. Bootstrapped sample and hold is implemented with transistor cross coupling to enhance the sample signal and get rid of thermal noise. Three-way interleaved comparator is specially designed to maximize the ADC speed. During one sampling cycle, only 2 of 3 comparators are working, while the 3rd comparator is charged to V_{cm} and execute calibration. The 2 working comparators works in a certain sequence. For instance, the 1st comparator is responsible for odd number bits, while the 2nd comparator is responsible for the even number bits. The 2 comparators are organized in such sequence to get rid of the effects of reset time. For instance, after the 1st comparator completes the 1st bit comparison, it has to be reset before the next comparison. Therefore, the 2nd bit signals are sent to the 2nd comparator to save time. The working sequence of these 3 comparators are determined by a specially generated control signal.

SAR logic in the proposed architecture is also modified to minimize the logic delay time. The comparator outputs are directly sent to DAC switch without storing in the static D-flip flop, in order to save the storing logic delay, thus accelerate the DAC

control signal, and obtain the next residue faster. Besides, all these modifications are made based on the low power condition. Therefore, the entire conversion speed of SAR ADC is boosted with ignorable increasing power cost.

4.3 DAC design and implementation

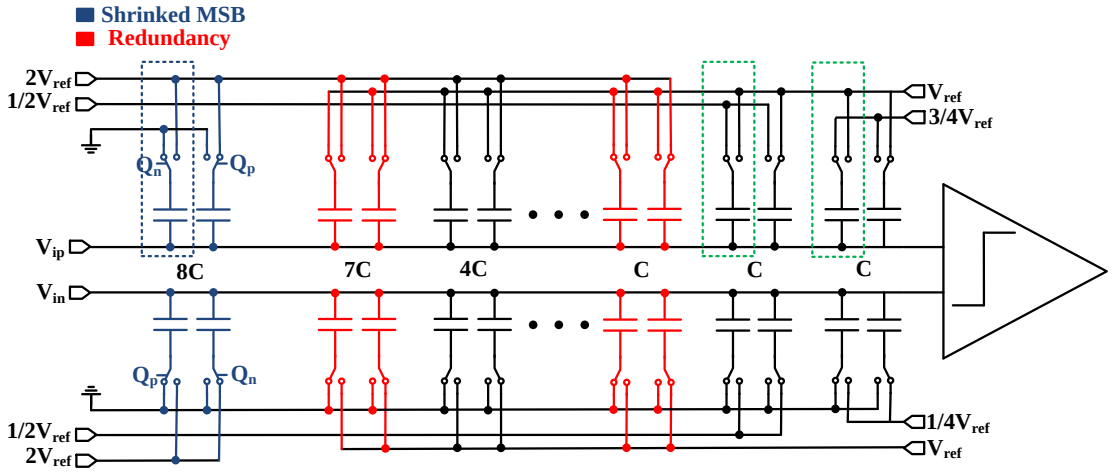


Figure 4.2 Proposed DAC architecture with shrinked MSB technique.

Figure 4.2 illustrates the proposed architecture of DAC, which utilizes constant common mode and Set-and-Down technique at the same time. A new technique called "shrinked MSB capacitor" is designed and applied to this architecture. Therefore, the settling speed is maximized and dissipation power is minimized.

Redundancy is implemented in the 2^{nd} to 5^{th} step. As illustrated in figure 4.2, the 2^{nd} bit is 7C, which is originally 8C. The 2^{nd} capacitor is modified too be 1 unit capacitor smaller. And there's another unit capacitor before the LSB capacitor. Originally the second capacitor is the same as the first capacitor. This is achieved by switching the first capacitor from 2 times of V_{ref} to ground.

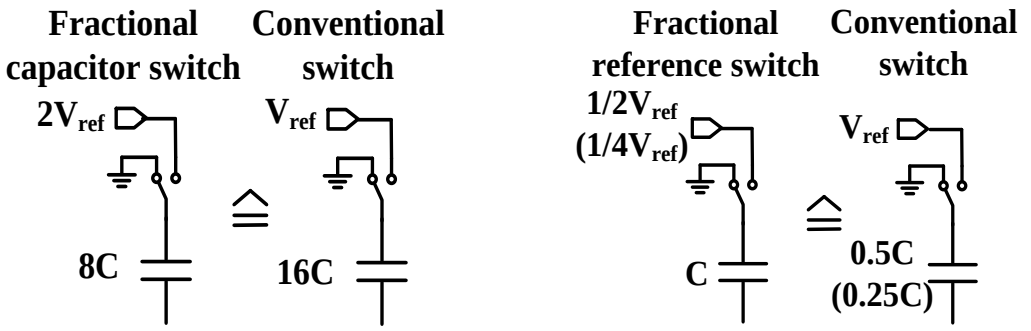


Figure 4.2 Two types of fractional switch.

As shown in figure 4.2, the shrinked MSB capacitor technique utilizes the theory of fractional capacitor switch. Because switching a capacitor from V_{ref} to ground is equivalent to switching half of it from $2V_{ref}$ to ground, MSB capacitor is thus reduced to its self to boost the settling speed and minimize capacitor array mismatch. Also, the last two LSB capacitors are increased to their 4 times and 2 times accordingly to minimize the mismatch and increase the unit capacitor, in order to increase the sample kT/C noise limitation.

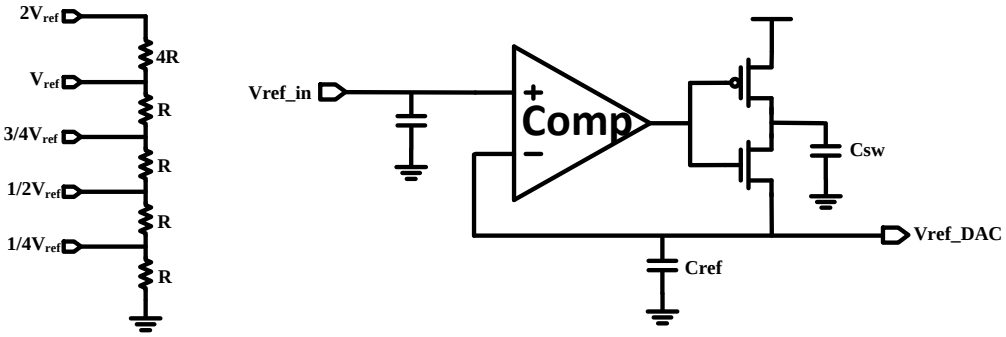


Figure 4.3 Reference generation.

Because of proposed MSB shrinked technique, several reference sources are needed to complete the entire transaction. Figure 4.3 shows how these desired reference sources

are generated. V_{ref_in} is the DAC input whose value equals to 2 times of V_{ref}. A resistive ladder is connecting to the DAC source and produce several different sources from $2V_{ref}$ to a quarter of V_{ref}. After every reference source, there's a self-charge and discharge system consisting of a comparator and charge/discharge capacitors. These reference charge/discharge system are used to keep reference constant and precise.

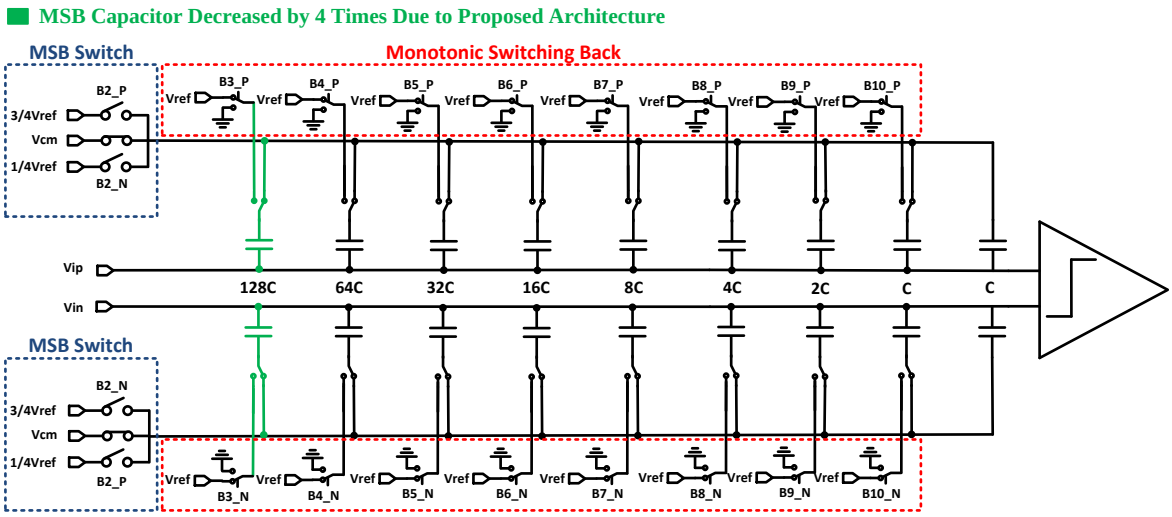


Figure 4.4 Proposed DAC architecture with constant common mode and switch back technique.

Figure 4.4 indicates another DAC design which is fabricated in 45nm SOI technology. The total SAR ADC architecture are basically the same, with three-way interleaved comparator and fast SAR logic design. DAC architecture is changed to a totally different version. This DAC architecture is featured by its common mode design to accelerate NMOS comparator decision and switch back technique to further minimize capacitor array and DAC mismatch.

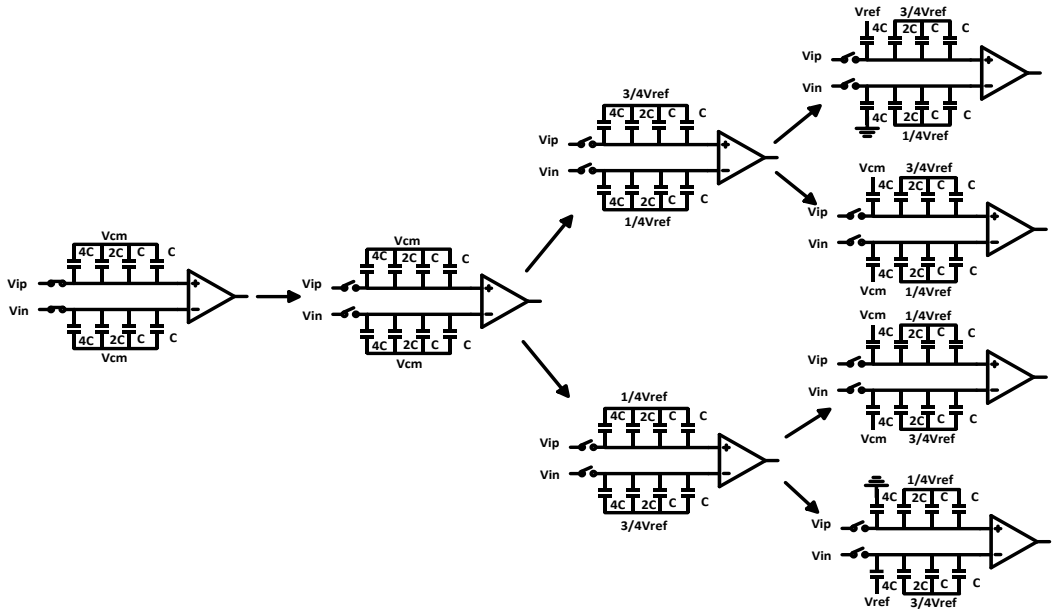


Figure 4.5 Proposed DAC switching procedure.

As shown in figure 4.5, DAC is initially charged to V_{cm}. After the first comparison, one differential side of capacitor array is switched to 3/4 V_{ref}, while the other side is switched to 1/4 V_{ref}. In the following steps, all the capacitors are switched back one by one, from 3/4V_{ref} to V_{ref}/GND, or from 1/4V_{ref} to V_{ref}/GND, according to comparator results. Using the same theory described in the last chapter, constant common mode is produced. Rather than doubling capacitor array, the proposed design utilizes various reference sources to be switched. Therefore, capacitor array size maintains to be minimum. The mismatch is also minimized due to MSB capacitor is decreased by 4 times.

DAC switch structure is illustrated below. Left side is responsible for the first bit switching, while the right side is controlling switch back afterwards.

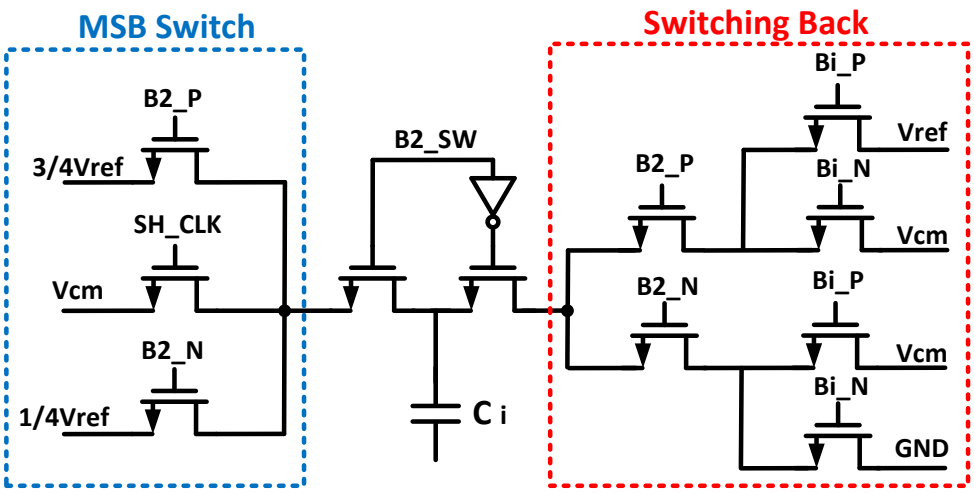


Figure 4.6 Proposed DAC switching.

4.4 Measurements

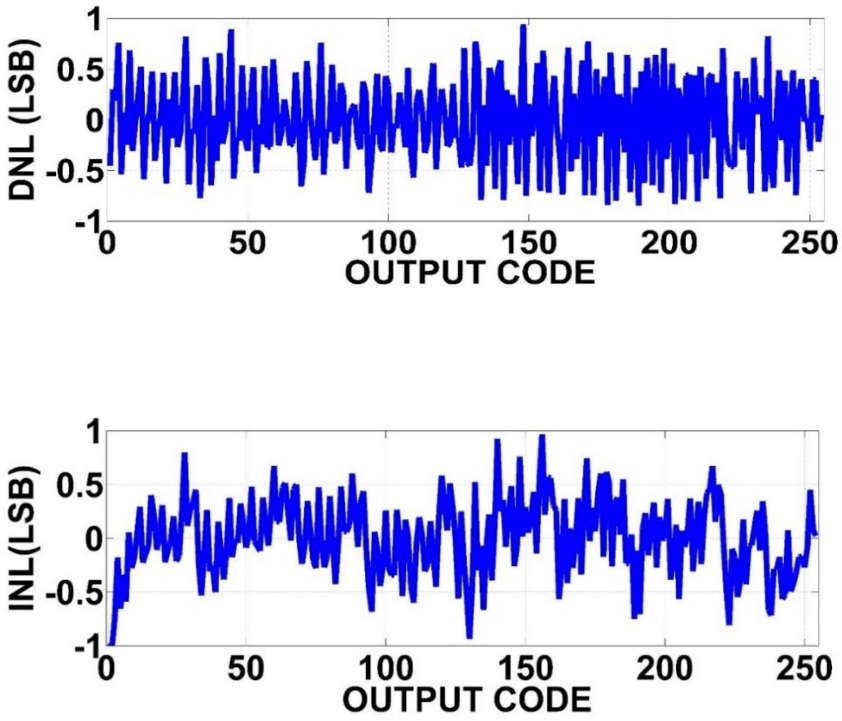


Figure 4.7 DNL&INL of proposed SAR ADC.

As shown in figure 4.7, DNL of proposed architecture ranges from +0.9389 to -0.8449 LSB. INL of proposed architecture ranges from +0.9667 to -1.006. Notice that

these measurements are obtained from 130nm fabrication results. INL is a little bit larger than 1 LSB, which might be affected by measurement device and environment.

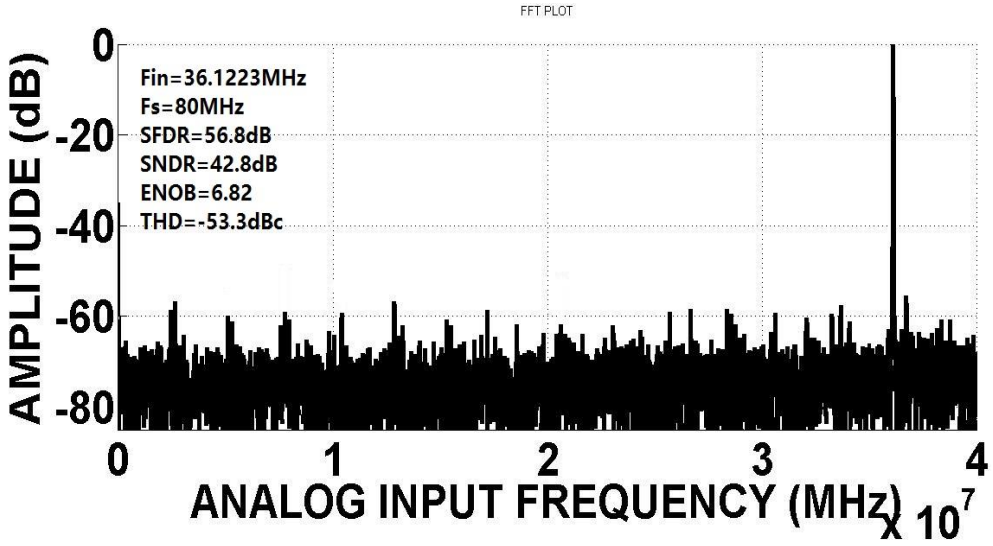


Figure 4.8 Output spectrum of proposed SAR ADC.

As shown in figure 4.8, proposed 8-bits SAR ADC achieves SFDR=56.8dB , SNDR=42.8dB . FoM is 221fJ/Conversion-step, calculated using the following equation:

$$FoM = \frac{Power}{f_s \cdot 2^{ENOB}} \tag{4.1}$$

Chapter 5 Conclusion

5.1 Conclusion of this work

SAR ADC has become a trend in nowadays ADC application, not only in low power application, but also high resolution and sample frequency performance requirements. Two proposed novel architectures of SAR ADC are described in this thesis and measurements are indicated. Boostrapped cross-coupling S/H and NMOS low power comparator are contained in this design. Two novel DAC architectures are proposed. Both is featured by minimized mismatch capacitor array and fast settling speed. The first type of DAC utilizes Set-and-Down switch, double capacitor array constant common mode, and shrinked MSB capacitor. The second type of DAC utilizes monotonic switch, fractional reference constant common mode, and switch back technique in order to decrease the entire capacitor.

8-bits and 10-bits models of SAR ADC are designed in this thesis. The 8-bits SAR ADC fabricated with 130nm technology has measured 80MSps sample frequency, 4.1mW , and 6.9 ENOB. The 10-bits SAR ADC fabricated with 45nm SOI technology is supposed to have 200MSps sample frequency, and 2mW power consumption.

The chip measurements and Cadence simulation results indicate that single core SAR ADC could also achieve competitive conversion speed and applicable resolution. SAR ADC will become more power efficient and suitable for high bandwidth application in the future.

5.2 Future work

Aiming at high bandwidth application, time-interleaved architecture will be the first consideration. Hopefully 4-way time-interleaved architecture will be applied to the 10-bits single core version and achieves 1GSps sample frequency. The time-interleaved architecture will be applied to 5G wireless communication standard product. Another version of high speed and high-resolution SAR ADC architecture is under designing and simulation. The goal is also to fulfill future 5G communication requirements.

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